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Professional™ 300 Series

Technical Manual
Volume 2 Options

Digital Equipment Corporation

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CONTENTS

INTRODUCTION

CHAPTER 1 TELEPHONE MANAGEMENT SYSTEM

1.1 Introduction 1-1
1.1.1 Related Documentation 1-1
1.1.2 Physical Description 1-2
1.1.2.1 TMS Controller Module 1-2
1.1.2.2 Telephone Line Interface (TLI) Module 1-3
1.1.2.3 Voice Unit 1-3
1.2 TMS System Level Functional Description 1-4
1.2.1 TMS Controller Module 1-4
1.2.1.1 Microprocessor Subsystem 1-6
1.2.1.2 CTI Bus Interface 1-6
1.2.1.3 Memory Subsystem 1-6
1.2.1.4 I/O Processing Subsystem 1-6
1.2.1.5 Communications Subsystem 1-7
1.2.1.6 Crossbar Switching Circuit 1-7
1.2.1.7 TLI/Voice Unit Interface 1-7
1.2.1.8 Call Progress Tone Detector 1-7
1.2.2 Telephone Line Interface (TLI) Module 1-8
1.2.2.1 Line Switching Relay Circuits 1-8
1.2.2.2 Line Coupling Circuit 1-8
1.2.2.3 Ring-In Detector Circuit 1-8
1.2.2.4 Off-Hook Detector Circuit 1-8
1.2.2.5 Voice Unit Interface 1-8
1.2.3 Voice Unit 1-8
1.2.3.1 8051 Microcomputer 1-9
1.2.3.2 Keyboard 1-9
1.2.3.3 LED Display 1-9
1.2.3.4 Speaker 1-9
1.2.3.5 Microphone 1-10
1.2.3.6 Remote Equipment Jack 1-10
1.3 Detailed Description 1-10
1.3.1 TMS Controller Module 1-10
1.3.1.1 8031 Microprocessor Subsystem 1-10
1.3.1.2 CTI Bus Interface Circuit Subsystem 1-14

1.3.1.3 Memory Subsystem 1-17
1.3.1.4 I/O Processing Subsystem 1-19
1.3.1.5 Communications Subsystem 1-21
1.3.1.6 Crossbar Switching Circuit 1-31
1.3.1.7 Call Progress Tone Detector 1-32
1.3.1.8 TLI/Voice Unit Interface Circuit 1-32
1.3.2 Telephone Line Interface (TLI) Module 1-34
1.3.2.1 Relay Circuits 1-35
1.3.2.2 Line Coupler Circuits 1-35
1.3.2.3 Ring-In Detector Circuit 1-36
1.3.2.4 Telset Off-Hook Detector Circuit 1-36
1.3.2.5 Voice Unit Interface 1-36
1.3.3 Voice Unit 1-36
1.3.3.1 System Overview 1-37
1.3.3.2 Detailed Description 1-39
1.4 Connector Descriptions 1-40
1.5 Hardware Specifications 1-43

CHAPTER 2 CP/M OPTION MODULE

2.1 Introduction 2-1
2.1.1 Related Documentation 2-2
2.1.2 Physical Description 2-2
2.2 Functional Description 2-3
2.2.1 Components 2-3
2.2.1.1 CTI Bus Interface Circuits 2-4
2.2.1.2 Z80 Microprocessor Circuits 2-4
2.2.1.3 Status Register Circuits 2-4
2.2.1.4 Processor Firmware Logic Circuits 2-5
2.2.1.5 RAM Logic Circuits 2-5
2.3 Theory of Operation 2-5
2.3.1 CTI Bus Interface Circuits 2-5
2.3.1.1 CTI Bus Access Interface 2-6
2.3.1.2 ROM Data and Address Register 2-7
2.3.1.3 Hardware Command Register 2-7
2.3.1.4 CP/M Option Module Status Register 2-7
2.3.1.5 Inbound Command and Data Register 2-7
2.3.1.6 Outbound Command and Data Register 2-7
2.3.2 Z80 Microprocessor Circuits 2-8
2.3.2.1 Processor Clock 2-8
2.3.2.2 I/O Multiplexer 2-8
2.3.2.3 Z80 Microprocessor 2-8
2.3.3 Z80 Status Register 2-9
2.3.3.1 Z80 Service Flag Buffer 2-10
2.3.3.2 Host Processor Service Flag Buffer 2-10
2.3.3.3 Command and Data Flag Buffer 2-11
2.3.3.4 Status Port 2-11
2.3.4 Processor Firmware Logic Circuits 2-11
2.3.4.1 Z80 ROM Selector 2-11
2.3.4.2 Z80 ROM 2-12

2.3.5 RAM Logic Circuits 2-12
2.3.5.1 Access Multiplex Logic 2-13
2.3.5.2 Address Multiplexer 2-13
2.3.5.3 Row/Column Address Strobe Delay 2-13
2.3.5.4 Read/Write Enable Logic 2-13
2.3.5.5 Memory Array 2-13
2.4 Connector J1 Description 2-13
2.5 Programming Registers 2-15
2.5.1 ROM Data Register (Base+0) 2-16
2.5.2 Status/Base +0 Reset Register (Base+2) 2-16
2.5.2.1 Nonmaskable Interrupt (NMI) Command Flag 2-16
2.5.2.2 RESET Flag 2-16
2.5.2.3 ROM Enable (ROMEN) Flag 2-16
2.5.2.4 Z80 Halt (ZHALT) Flag 2-16
2.5.2.5 Interrupt B (IRQB) Flag 2-17
2.5.2.6 Interrupt A (IRQA) Flag 2-17
2.5.3 Inbound/Outbound Command Register (Base+4) 2-17
2.5.3.1 Commands to the Host Processor 2-17
2.5.3.2 Software Commands From the Host Processor 2-17
2.5.3.3 Hardware Commands From the Host Processor 2-17
2.5.4 Inbound/Outbound Data Register (Base+6) 2-17
2.6 Operation 2-18
2.6.1 Power-Up 2-18
2.6.1.1 Z80 Self-Test 2-18
2.6.1.2 Interface Self-Test 2-20
2.6.2 Reset and NMI Hardware Commands 2-20
2.6.2.1 RESET Command 2-20
2.6.2.2 Nonmaskable Interrupt (NMI) Command 2-20
2.6.3 Host Processor Initiated Transfers 2-20
2.6.4 Z80 Microprocessor Initiated Transfers 2-21
2.6.5 Z80 Microprocessor Halt Recovery 2-21
2.6.6 Z80 ROM and RAM Accesses 2-21
2.7 Specifications 2-21

CHAPTER 3 DECNA CONTROLLER OPTION MODULE

3.1 Introduction 3-1
3.2 Physical Description 3-1
3.3 Specifications 3-2
3.4 Ethernet Overview 3-2
3.4.1 Main Physical Components 3-2
3.4.2 Ethernet Protocol 3-3
3.4.3 Transmission Frame Format 3-3
3.5 DECNA Functional Overview 3-4
3.5.1 Initialization 3-5
3.5.2 Transmission Overview 3-5
3.5.3 Reception Overview 3-6
3.6 CTI Bus Interface 3-6
3.6.1 Bus Transceivers, Bus Command Register, and Control Circuitry 3-6
3.6.1.1 Read/Write 3-6

3.6.1.2 Bus Transceivers 3-11
3.6.1.3 Bus Command Register 3-11
3.6.1.4 Slot Select Buffer 3-11
3.6.1.5 Bus Reply Generator 3-11
3.6.1.6 Control Register Interrupt Circuit 3-11
3.6.1.7 Host Interrupt Circuit 3-11
3.6.2 Memory Access Register 3-11
3.6.3 Control Register (Command Control Latch) 3-13
3.6.4 Memory Base Address Register and Write-Only Latch, and Base Address Comparator 3-16
3.6.5 Option ROM, Address ROM, and ROM Address Logic 3-18
3.6.5.1 Option ROM 3-18
3.6.5.2 Address ROM 3-18
3.6.5.3 ROM Address Logic 3-18
3.7 Dual-Ported Memory 3-20
3.7.1 Dynamic RAM 3-21
3.7.2 CTI Write/NI Write Selector 3-22
3.7.3 Dual-Ported Memory Controller 3-24
3.7.3.1 Clock and TTL-to-MOS Level Converter 3-24
3.7.3.2 8207 Programming Register 3-24
3.7.3.3 Arbiter Circuit 3-24
3.7.4 CTI Read/Write Decoder 3-27
3.7.5 Port A (CTI Data-to-Memory Buffer, Data Latch, and Address Latch) 3-29
3.7.5.1 CTI Data-to-Memory Buffer 3-29
3.7.5.2 CTI Memory Data Latch 3-29
3.7.5.3 CTI Address Latch 3-29
3.7.6 Port B (Network Interface Data-to-Memory Buffer, Memory Data Latch, and Address Latch) 3-31
3.7.6.1 NI Data-to-Memory Buffer 3-33
3.7.6.2 NI Memory Data Latch 3-33
3.7.6.3 NI Address Latch 3-33
3.8 Ethernet Interface 3-34
3.8.1 Ethernet Controller 3-34
3.8.1.1 Clock and TTL-to-MOS Level Converter 3-34
3.8.1.2 Ethernet Communications Controller Chip (82586) 3-34
3.8.1.3 Fail-Safe Time-Out Circuit 3-38
3.8.1.4 NI Internal Bus Controller 3-38
3.8.2 Ethernet Serial Interface 3-38
3.8.2.1 Manchester Code 3-41
3.8.2.2 Ethernet Serial Interface Encoder/Decoder 3-42
3.8.2.3 Transmit Clock TTL-to-MOS Level Converter 3-42
3.8.2.4 Receive Clock TTL-to-MOS Level Converter 3-42
3.8.2.5 Receive Data Resynchronizer and TTL-to-MOS Level Converter 3-42
3.8.2.6 Collision Clock Detect Circuit 3-43
3.8.2.7 Carrier Sense Circuit 3-43
3.8.3 Broadband Ethernet Compatibility Circuit 3-43

CHAPTER 4 PROFESSIONAL 380 EXTENDED BITMAP OPTION MODULE

4.1 Introduction 4-1
4.2 Functional Description 4-1
4.3 Detailed Description 4-2
4.3.1 Bus Interface Signals 4-3
4.3.2 Video Signals 4-4
4.3.3 Interchip Control Signals 4-5
4.3.4 Operational Power Levels 4-5
4.3.5 EBO Module Connector Pin Assignment 4-6
4.4 Hardware Specifications 4-6
4.4.1 Physical Specifications 4-6
4.4.2 Power Specifications 4-6
4.4.3 Environmental Specifications 4-7
4.4.3.1 Operating Environment 4-7
4.4.3.2 Operating Temperature 4-7
4.4.3.3 Operating Relative Humidity 4-7
4.4.3.4 Storage Environment 4-7
4.4.3.5 Storage Temperature 4-7
4.4.3.6 Storage Relative Humidity 4-7

CHAPTER 5 RD/RD52-A HARD DISK DRIVE CONTROLLER MODULE

5.1 General Information 5-1
5.1.1 Related Documentation 5-1
5.1.2 Hard Disk Drive Controller Module 5-2
5.2 Functional Components 5-2
5.2.1 Overview 5-2
5.2.2 CTI Bus Interface Circuits 5-4
5.2.3 Microprocessor (μP) Control Circuits 5-4
5.2.4 Disk Control and Status Circuits 5-4
5.2.5 Modified Frequency Modulation (MFM) Write Data Circuits 5-4
5.2.6 Modified Frequency Modulation (MFM) Read Data Circuits 5-5
5.3 Theory of Operation 5-5
5.3.1 CTI Bus Interface Circuits 5-6
5.3.1.1 CTI Bus I/O Controller 5-6
5.3.1.2 CTI Bus Data/Address Transceivers 5-6
5.3.1.3 STATUS/INIT Register 5-6
5.3.1.4 Address Buffer 5-6
5.3.1.5 Data I/O Ports 5-6
5.3.1.6 General Controller Module Access 5-7
5.3.2 μP Control Circuits 5-8
5.3.2.1 Internal I/O Bus Control 5-8
5.3.2.2 Memory Mapping and Access 5-8
5.3.2.3 Disk Read/Write Control Buffer 5-8
5.3.3 Disk Control and Status Circuits 5-10

5.3.3.1 Disk Control Signal Buffer 5-10
5.3.3.2 Disk Status Signal Buffer 5-10
5.3.4 MFM Write Data Circuits 5-10
5.3.4.1 Parallel-to-Serial Converter 5-12
5.3.4.2 CRC Generator/Checker 5-12
5.3.4.3 MFM Generator 5-12
5.3.5 MFM Read Data Circuits 5-12
5.3.5.1 Phase Lock Loop/Data Separator 5-12
5.3.5.2 Address Mark Detector 5-12
5.3.5.3 Serial-to-Parallel Converter 5-13
5.3.5.4 CRC Generator/Checker 5-13
5.3.6 Controller Data Flow Description 5-14
5.3.6.1 Drive Command Data Flow 5-14
5.3.6.2 Write Data Flow 5-14
5.4 Detailed Connector Descriptions 5-16
5.4.1 CTI Bus Interface J1 5-17
5.4.2 Disk Control/Status Connector J2 5-16
5.4.2.1 REDUCED WRITE CURRENT (Pin 2) 5-18
5.4.2.2 WRITE GATE (Pin 6) 5-18
5.4.2.3 HEAD SELECT (Pin 4, 14 and 18) 5-18
5.4.2.4 STEP (Pin 24) 5-18
5.4.2.5 DIRECTION IN (Pin 34) 5-18
5.4.2.6 DRIVE SELECT (Pin 26) 5-18
5.4.2.7 SEEK COMPLETE (Pin 8) 5-18
5.4.2.8 TRACK 000 (Pin 10) 5-18
5.4.2.9 WRITE FAULT (Pin 12) 5-18
5.4.2.10 INDEX (Pin 20) 5-18
5.4.2.11 READY (Pin 22) 5-19
5.4.2.12 RD50 5 MB (Pin 32) 5-19
5.4.3 Disk Data I/O Connector J3 5-19
5.4.3.1 DRIVE SELECTED (Pin 1) 5-19
5.4.3.2 MFM WRITE DATA (Pins 13 and 14) 5-19
5.4.3.3 MFM READ DATA (Pins 17 and 18) 5-19
5.5 Programming Registers 5-20
5.5.1 ID Register (774000) 5-20
5.5.2 ERROR/PRECOMP Register (774004) 5-21
5.5.2.1 DM Not Found (Bit 8) 5-21
5.5.2.2 TR000 Error (Bit 9) 5-21
5.5.2.3 Illegal/Aborted Command (Bit 10) 5-22
5.5.2.4 ID Not Found (Bit 12) 5-22
5.5.2.5 CRC Error ID Field (Bit 13) 5-22
5.5.2.6 CRC Error Data Field (Bit 14) 5-22
5.5.3 BACKUP REVISION/SECTOR ID Register (774006) 5-22
5.5.4 DATA BUFFER Register (774010) 5-23
5.5.5 CYLINDER ID Register (774012) 5-24
5.5.6 HEAD ID Register (774014) 5-24
5.5.7 STA 2/COMMAND Register (774016) 5-24
5.5.7.1 Restore 5-24
5.5.7.2 Read Sector 5-26

5.5.7.3 Write Sector 5-27
5.5.7.4 Format 5-27
5.5.7.5 Error Status 5-28
5.5.7.6 Data Request 5-28
5.5.7.7 Seek Complete 5-28
5.5.7.8 Write Fault 5-28
5.5.7.9 Disk Drive Ready 5-28
5.5.8 STATUS/INIT Register (774020) 5-29
5.5.8.1 OP ENDED 5-29
5.5.8.2 RESET/INITIALIZE 5-29
5.5.8.3 DRQ 5-29
5.5.8.4 BUSY 5-29
5.6 General Sequence of Operation 5-30
5.6.1 Read Sector, Write Sector, Format Command 5-30
5.6.1.1 Read Sector Command Follow-up Sequence 5-30
5.6.1.2 Write Sector and Format Command Preparation 5-30
5.6.1.3 Write Sector and Format Command Follow-up Sequence 5-30
5.6.2 Read After Write Verify Follow-up Sequence 5-31
5.6.3 Restore Command 5-31
5.6.4 Initialization Sequence 5-31
5.7 Specifications 5-32
5.7.1 Environmental 5-32
5.7.2 Power 5-32

CHAPTER 6 RD50/RD51 HARD DISK DRIVE

6.1 General Information 6-1
6.1.1 Related Documentation 6-1
6.1.2 Hard Disk Drive 6-2
6.2 Functional Components 6-2
6.2.1 Overview 6-2
6.2.2 Drive Mechanism 6-2
6.2.3 Spindle Motor Control Circuit 6-2
6.2.4 Power-Up Circuit 6-3
6.2.5 Fault Detection Circuit 6-3
6.2.6 Seek Circuit 6-3
6.2.7 Write Circuit 6-4
6.2.8 Read Circuit 6-4
6.3 Theory of Operation 6-4
6.3.1 Drive Mechanism Detailed Operations 6-4
6.3.1.1 Sealed Head and Disk Assembly (HDA) 6-4
6.3.1.2 Sensors and Hardware 6-9
6.3.2 Spindle Motor Control Circuit Detailed Operations 6-10
6.3.2.1 Motor Current Control 6-10
6.3.2.2 Spindle Motor Current Switching 6-12
6.3.3 Power-up Circuit Detailed Operations 6-12
6.3.3.1 Reset Signal Generation 6-12
6.3.3.2 Up to Speed Signal Generation 6-12
6.3.3.3 Recalibration Signal Generation 6-14

6.3.3.4 Ready Signal Generation 6-14
6.3.3.5 Recalibration Signal Generation Deselection 6-14
6.3.4 Fault Detection Circuit Detailed Operation 6-14
6.3.4.1 Head Selection Malfunction Detection 6-16
6.3.4.2 Power Unsafe Detection 6-16
6.3.4.3 Write Circuit Unsafe Detection 6-16
6.3.4.4 Write Status Detection 6-16
6.3.5 Seek Circuit Detailed Operation 6-17
6.3.5.1 Head Direction Selection 6-18
6.3.5.2 Step Pulse Selection 6-18
6.3.5.3 Step Pulse and Direction Signal Conversion 6-18
6.3.5.4 Track 0 Monitoring 6-18
6.3.5.5 Seek Complete Indicator 6-19
6.3.6 Write Circuit Detailed Description 6-19
6.3.7 Read Circuit Detailed Description 6-21
6.4 Connector Descriptions 6-24
6.4.1 Connector J1, Read/Write Module 6-24
6.4.1.1 REDUCED WRITE CURRENT (Pin 2) 6-26
6.4.1.2 WRITE GATE (Pin 6) 6-26
6.4.1.3 SEEK COMPLETE (Pin 8) 6-26
6.4.1.4 TRACK 000 (Pin 10) 6-26
6.4.1.5 WRITE FAULT (Pin 12) 6-26
6.4.1.6 HEAD SELECT (Pin 14 and 18) 6-26
6.4.1.7 INDEX (Pin 20) 6-26
6.4.1.8 READY (Pin 22) 6-26
6.4.1.9 STEP (Pin 24) 6-26
6.4.1.10 DRIVE SELECT (Pin 26) 6-26
6.4.1.11 DRIVE CAPACITY (Pin 32) 6-27
6.4.1.12 DIRECTION IN (Pin 34) 6-27
6.4.2 Connector J2, Read/Write Module 6-27
6.4.2.1 DRIVE SELECTED (Pin 1) 6-27
6.4.2.2 MFM WRITE DATA (Pins 13 and 14) 6-27
6.4.2.3 MFM READ DATA (Pins 17 and 18) 6-28
6.4.3 Connector J3, Read/Write Module 6-28
6.4.4 Connector J4, Read/Write Module 6-28
6.4.5 Connector J5, Read/Write Module 6-28
6.4.6 Connector J6, Read/Write Module 6-28
6.4.7 Connector J7, Read/Write Module 6-30
6.4.8 Connector J8, Read/Write Module 6-30
6.4.9 Connector J1, Motor Control Module 6-30
6.4.10 Connector J2, Motor Control Module 6-30
6.5 Maintenance Procedures 6-31
6.5.1 Preventive Maintenance 6-31
6.5.2 Test Point Locations 6-31
6.5.3 Jumper/Dip Switch Settings 6-32
6.6 Specifications 6-32
6.6.1 RD50 Disk Drive Specifications 6-32
6.6.1.1 Performance Specifications 6-32
6.6.1.2 Reliability Specifications 6-32

6.6.1.3 Functional Specifications 6-33
6.6.1.4 Electrical Specifications 6-33
6.6.1.5 Environmental Specifications 6-33
6.6.2 RD51 Disk Drive Specifications 6-34
6.6.2.1 Performance Specifications 6-34
6.6.2.2 Reliability Specifications 6-34
6.6.2.3 Functional Specifications 6-34
6.6.2.4 Electrical Specifications 6-35
6.6.2.5 Environmental Specifications 6-35

CHAPTER 7 RX50 CONTROLLER MODULE

7.1 General Information 7-1
7.1.1 Related Documentation 7-1
7.1.2 Controller Module 7-2
7.2 Functional Components 7-2
7.2.1 Overview 7-2
7.2.2 CTI Bus to Controller Memory Interface 7-3
7.2.3 Microprocessor to Controller Memory Interface 7-4
7.2.4 Disk Control and Status Interface 7-4
7.2.5 MFM Write Data Interface 7-4
7.2.6 MFM Read Data Interface 7-4
7.3 Theory of Operation 7-5
7.3.1 CTI Bus to Controller Memory Interface Detail 7-5
7.3.1.1 RX50 Module Initialization 7-5
7.3.1.2 Interrupt Signal Generation 7-8
7.3.1.3 RX50 Module Acknowledgment 7-8
7.3.1.4 Host Processor to Controller Memory Accessing 7-8
7.3.2 Microprocessor to Controller Memory Accessing 7-10
7.3.2.1 Command and Status Register Accessing 7-10
7.3.2.2 Sector Buffer Memory Accessing 7-12
7.3.3 Disk Control and Status Interface 7-13
7.3.3.1 Control and Status Signal Processing 7-14
7.3.3.2 Drive Select Signal Conversion 7-14
7.3.3.3 Drive Control Signal Gating 7-14
7.3.4 Write Data Interface Function 7-15
7.3.4.1 Write Data Bytes to Floppy Controller Transfers 7-15
7.3.4.2 MFM Encoding 7-17
7.3.4.3 Write Data Precompensation 7-17
7.3.4.4 MFM Write Data Synchronization 7-17
7.3.5 MFM Read Data Interface 7-18
7.3.5.1 Data Separator and Phase-Locked Loop Operation 7-18
7.3.5.2 Read Data Byte Conversion and Transfer 7-19
7.3.6 Module Data Flow 7-19
7.4 Detailed Connector Descriptions 7-20
7.4.1 CTI Bus Interface J1 7-20
7.4.2 Drive Interface Connector J2 7-22
7.4.2.1 TKG43 L Output Signal 7-23
7.4.2.2 SEL 0 through SEL 3 Output Signals 7-23

7.4.2.3 TK 00 L Input Signal 7-23
7.4.2.4 MOTOR PWR ON L Output Signal 7-23
7.4.2.5 DIR Output Signal 7-23
7.4.2.6 STEP L Output Signal 7-23
7.4.2.7 WRT DATA L Output Signal 7-23
7.4.2.8 WG L Output Signal 7-23
7.4.2.9 INDEX L Input Signal 7-23
7.4.2.10 WRT PRT L Input Signal 7-23
7.4.2.11 RD DATA L Input Signal 7-23
7.4.2.12 READY Input Signal 7-23
7.5 Programming 7-24
7.5.1 RX51D Identification Register (X00) 7-25
7.5.2 RX5CS0 Register (X04) 7-25
7.5.2.1 Command Mode Bits 7-25
7.5.2.2 Maintenance Status Mode 7-27
7.5.2.3 Read/Write Status Mode 7-28
7.5.3 RX5CS1 Register (X06) 7-28
7.5.3.1 Command Mode Bit 7-28
7.5.3.2 Maintenance Status Mode 7-28
7.5.3.3 Read/Write Status Mode 7-28
7.5.3.4 Extended Functions Mode 7-28
7.5.4 RX5CS2 Register (X10) 7-30
7.5.4.1 Command Mode 7-30
7.5.4.2 Maintenance Status Mode 7-30
7.5.4.3 Read/Write Status Mode 7-30
7.5.4.4 Extended Functions Mode 7-31
7.5.5 RX5CS3 Register (X12) 7-31
7.5.5.1 Maintenance Mode Status 7-31
7.5.5.2 Read/Write Status Mode 7-33
7.5.5.3 Extended Functions Mode 7-33
7.5.6 RX5CS4 Register (X14) 7-34
7.5.6.1 Maintenance Status Mode 7-34
7.5.6.2 Read/Write Status Mode 7-34
7.5.6.3 Extended Functions Mode 7-35
7.5.7 RX5CS5 Register (X16) 7-35
7.5.7.1 Read With Retries (000) 7-36
7.5.7.2 Write Sector With Deleted DATA MARK (001) 7-36
7.5.7.3 Report Format Parameters of Selected Diskette (010) 7-36
7.5.7.4 Set Format Parameters of Selected Diskette (011) 7-36
7.5.7.5 Report Controller Version Number (100) 7-37
7.5.7.6 Read and Compare (101) 7-37
7.5.8 RX5EB Empty Data Buffer (X20) 7-37
7.5.9 RX5CA Clear Address (X22) 7-38
7.5.10 RX5GO Start Command (X24) 7-38
7.5.11 RX5FB Fill Sector Buffer (X26) 7-38
7.5.12 Command and Status Register Summary 7-38
7.6 General Operating Sequence 7-39
7.6.1 Read/Write Operations 7-40
7.6.1.1 Read/Write Status 7-41

7.6.2 Maintenance Operations 7-41
7.6.2.1 Maintenance Status 7-41
7.6.3 Controller Initialization and Self-Test Sequence 7-41
7.7 Specifications 7-43
7.7.1 Electrical Specifications 7-43
7.7.2 Environmental Specifications 7-43
7.7.3 Physical Specifications 7-43

CHAPTER 8 RX50 DUAL DISKETTE DRIVE

8.1 General Information 8-1
8.1.1 Related Documentation 8-1
8.1.2 RX50 Dual Diskette Drive 8-1
8.1.3 Physical Description 8-2
8.1.4 Diskette Description 8-2
8.1.4.1 Diskette Handling and Storage 8-3
8.1.4.2 Write Protection of Diskettes 8-4
8.1.4.3 Diskette Loading/Unloading 8-4
8.1.5 Configuration Options 8-4
8.2 Functional Components 8-6
8.2.1 Seek and Interface Module Functions 8-6
8.2.2 Motor Control Module and Spindle Motor Function 8-7
8.2.3 Head Load Solenoid Function 8-8
8.2.4 Sensor Functions 8-8
8.2.5 Stepper Motor Function 8-8
8.2.6 Read/Write Module Function 8-8
8.2.7 RX50 Drive Set-up Sequence 8-8
8.3 Theory of Operation 8-8
8.3.1 Drive Mechanism 8-9
8.3.1.1 Diskette Positioning Mechanism 8-12
8.3.1.2 Spindle Drive Mechanism 8-12
8.3.1.3 Head Positioning Mechanism 8-12
8.3.1.4 Head Load Mechanism 8-13
8.3.1.5 Sensors 8-13
8.3.2 Select Circuit Detailed Operation 8-14
8.3.2.1 Drive Select Circuit 8-14
8.3.2.2 Motor Enable Circuit 8-16
8.3.2.3 Head Load Circuit 8-16
8.3.3 Motor Control Circuit 8-16
8.3.3.1 Frequency to Voltage Converter 8-18
8.3.3.2 Summer 8-19
8.3.3.3 Integrator 8-19
8.3.3.4 Gain Amplifier and Current Limiter 8-19
8.3.4 Head Load Solenoids and Indicators 8-19
8.3.5 Status Circuit 8-19
8.3.5.1 Write Protect Status Circuit 8-23
8.3.5.2 Diskette Present Status Circuits 8-23
8.3.5.3 Output Driver 8-23
8.3.5.4 +5 V Monitor 8-23

8.3.6 Status Sensors 8-24
8.3.6.1 Index Sensor 8-24
8.3.6.2 Diskette Present and Write Protect Sensor 8-25
8.3.7 Stepper Motor Circuits 8-26
8.3.7.1 Stepper Motor Driver 8-26
8.3.7.2 Track 0 Sensor 8-28
8.3.7.3 Track 0 Status Circuit 8-28
8.3.8 Read/Write Interface Circuit 8-28
8.3.8.1 Write Driver Circuit 8-28
8.3.8.2 Erase Gate Timer 8-31
8.3.8.3 Output Driver 8-31
8.3.9 Write Circuit 8-31
8.3.9.1 Write Current Generator 8-33
8.3.9.2 Voltage Reference 8-33
8.3.9.3 +12 V Gate 8-33
8.3.9.4 Differential Write Switch 8-33
8.3.9.5 Erase Gate Generator 8-33
8.3.9.6 Multiplexer 8-34
8.3.10 Read Circuit 8-34
8.3.10.1 Read Amplifier 8-36
8.3.10.2 Multiplexer 8-36
8.3.11 Write/Read Head 8-37
8.4 Intermodule Signal Definitions 8-37
8.4.1 Seek and Interface/Controller Module Connector J1 8-37
8.4.1.1 TKG43 L Input Signal 8-39
8.4.1.2 DRIVE SEL 0 thru DRIVE SEL 3 Input Signals 8-39
8.4.1.3 TRACK 0 L Output Signal 8-39
8.4.1.4 MOTOR ON L Input Signal 8-39
8.4.1.5 DIRECTION Input Signal 8-39
8.4.1.6 STEP L Input Signal 8-39
8.4.1.7 WRITE DATA L Input Signal 8-39
8.4.1.8 WRITE GATE L Input Signal 8-39
8.4.1.9 INDEX L Output Signal 8-40
8.4.1.10 WRITE PROTECT L Output Signal 8-40
8.4.1.11 READ DATA L Output Signal 8-40
8.4.1.12 READY Output Signal 8-40
8.4.2 Seek and Interface/Motor Control Modules Connector J4 8-40
8.4.2.1 MPWR H Input Signal 8-40
8.4.2.2 SIDE A L Input Signal 8-40
8.4.2.3 SIDE B L Input Signal 8-40
8.4.3 Seek and Interface/Read Write Modules Connector J9 8-41
8.4.3.1 DCOK L Output Signal 8-41
8.4.3.2 ±WRITE L Output Signals 8-41
8.4.3.3 R DATA H Input Signals 8-41
8.4.3.4 W GATE L Output Signal 8-41
8.4.3.5 WRITE CURRENT SWITCH Output Signal 8-41
8.4.3.6 ERASE GATE L Output Signal 8-41
8.4.3.7 SEL A L Output Signal 8-41
8.4.4 Seek and Interface Power Connector J3 8-42

8.4.5 Seek and Interface Connectors J2, J5, J6, J7, J8, J10, and J17 8-42
8.4.5.1 Side A Switches and Indicators Connector J2 8-42
8.4.5.2 Track 0 Sensor Connector J5 8-42
8.4.5.3 Side B Head Load Solenoid Connector J6 8-42
8.4.5.4 Stepper Motor Connector J7 8-42
8.4.5.5 Side B Switches and Indicators Connector J8 8-43
8.4.5.6 Side A Head Load Solenoid Connector J10 8-43
8.4.5.7 Drive Select Jumper J17 8-43
8.4.6 Motor Control Modules Connectors J4, J11, J16 8-43
8.4.6.1 Spindle Motor Connector J11 8-43
8.4.6.2 Front Panel Operational Indicators Connector J16 8-44
8.4.7 Read/Write Module Connectors J9, J14, J15 8-44
8.4.7.1 Side A Read, Write, and Erase Head Connector J14 8-44
8.4.7.2 Side B Read, Write, and Erase Head Connector J15 8-44
8.5 Specifications 8-45
8.5.1 Performance Specifications 8-45
8.5.2 Reliability Specifications 8-45
8.5.3 Functional Specifications 8-46
8.5.4 Electrical Specifications 8-46
8.5.5 Environmental Specifications 8-46
8.5.6 Mechanical Specifications 8-46

CHAPTER 9 RD52-A DISK DRIVE

9.1 Introduction 9-1
9.2 Product Description 9-1
9.3 Identifying Your RD52-A Disk Drive 9-1
9.4 RD52-A General Specifications 9-3
9.5 Related Documentation 9-3
9.6 RD52-A (30-21721-01) Disk Drive 9-4
9.6.1 General 9-5
9.6.2 Specifications 9-5
9.6.2.1 Physical Specifications 9-5
9.6.2.2 Performance Specifications 9-6
9.6.2.3 Functional Specifications 9-6
9.6.3 Power Requirements 9-6
9.6.3.1 DC Power 9-6
9.6.3.2 DC Power Connector 9-6
9.7 Physical Description 9-8
9.7.1 RD52-A Drive Mechanism 9-8
9.7.1.1 Base Casting 9-8
9.7.1.2 DC Spindle Drive Motor 9-8
9.7.1.3 Disk Stack 9-9
9.7.1.4 Head Stack 9-9
9.7.1.5 Optical Encoder 9-9
9.7.1.6 Rotary Positioner 9-9
9.7.1.7 Automatic Actuator Lock 9-9
9.7.2 Electromagnetic Interference (EMI) Band 9-10
9.7.3 Air Filtration 9-10

9.8 Operation 9-11
9.8.1 Operator Functions 9-11
9.8.1.1 Drive Select 9-11
9.8.1.2 Control Cable Termination 9-11
9.8.2 Functional Description 9-12
9.8.3 Drive Electronics 9-12
9.8.4 Encoder PCB 9-14
9.8.4.1 AGC Circuit 9-14
9.8.4.2 P1 and P2 Signal Generation 9-14
9.8.4.3 Track 0 9-16
9.8.5 Drive Control PCB 9-16
9.8.6 Actuator Positioning Circuits 9-18
9.8.6.1 Actuator Microprocessor 9-18
9.8.6.2 Recalibration 9-18
9.8.6.3 AGC Function 9-18
9.8.6.4 On Track Servoing (Coarse) 9-18
9.8.6.5 Fine Servoing 9-18
9.8.6.6 Ramped Mode Seeking 9-18
9.8.6.7 Slew Mode Seeking 9-18
9.8.7 Write Data Circuits 9-19
9.8.8 Read Data Circuits 9-20
9.8.8.1 Low Pass Filter/Differentiator 9-20
9.8.8.2 Zero Crossing Detector 9-20
9.8.8.3 Droop Ignore Circuit 9-20
9.8.9 Motor Microprocessor 9-21
9.8.9.1 Description 9-21
9.8.9.2 DC Motor Control 9-22
9.8.9.3 Motor Current 9-22
9.8.9.4 DC Motor Drive Circuit 9-24
9.8.9.5 WEDGE and INDEX Signals 9-25
9.8.9.6 WRITE FAULT 9-25
9.8.9.7 Power Faults 9-25
9.9 Interface 9-26
9.9.1 Control Signal Interface 9-26
9.9.1.1 General Description 9-26
9.9.1.2 Driver/Receiver 9-28
9.9.1.3 Control Signal Descriptions 9-28
9.9.2 Data Signal Interface 9-30
9.9.2.1 General Description 9-30
9.9.2.2 Driver/Receiver 9-30
9.9.2.3 Data Signal Descriptions 9-32
9.10 RD52-A (30-23227-02) Disk Drive 9-32
9.10.1 General 9-32
9.10.2 Specifications 9-32
9.10.2.1 Physical Specifications 9-32
9.10.2.2 Performance Specifications 9-34
9.10.2.3 Functional Specifications 9-34
9.10.3 Power Requirements 9-35
9.10.3.1 DC Power 9-35
9.10.3.2 DC Power Connector 9-35

9.11 Physical Description 9-36
9.11.1 Assemblies 9-36
9.11.1.1 Read/Write Interface PCB 9-36
9.11.1.2 Spindle/EMA Drive PCB 9-36
9.11.1.3 Servo Control PCB 9-36
9.11.1.4 Spindle Drive Mechanism 9-36
9.11.1.5 Positioning Mechanism 9-36
9.11.1.6 Read/Write Heads and Media 9-38
9.11.2 Air Filtration System 9-38
9.12 Operation 9-38
9.12.1 Operator Functions 9-38
9.12.1.1 Drive Select 9-38
9.12.1.2 Control Cable Termination 9-38
9.12.2 Drive Organization 9-39
9.12.3 Power Sequencing 9-39
9.12.4 Microprocessor Wake-Up Timing 9-39
9.12.4.1 Spindle Open Loop Acceleration Ramp 9-39
9.12.4.2 Spindle Driver 9-40
9.12.4.3 Servo Control of the Spindle 9-40
9.12.4.4 Watch-Dog Inhibitor 9-40
9.12.4.5 Actuator Disabling 9-41
9.12.4.6 Carriage Latch Release 9-41
9.12.4.7 Automatic Rezero Routine 9-41
9.12.5 Fault Finding 9-41
9.12.5.1 Error Detection 9-41
9.12.5.2 Power Fault Status Inhibitor 9-41
9.12.5.3 Power Faults 9-42
9.12.6 Interface Operations 9-43
9.12.7 Interface Logic 9-45
9.12.8 Servo Operations 9-46
9.12.8.1 Velocity Loop 9-46
9.12.8.2 Servo Status Reporting 9-46
9.12.8.3 Window Generator 9-47
9.12.8.4 Index Reporting 9-47
9.12.8.5 Servo AGC Circuit 9-47
9.12.8.6 EMA Driver Circuit 9-47
9.12.9 Read/Write Operations 9-47
9.12.9.1 Write Operations 9-49
9.12.9.2 Read Operations 9-49
9.12.9.3 Read Channel/Analog 9-49
9.12.9.4 Read Channel Digital 9-49
9.13 Interface 9-50
9.13.1 Interface Connectors 9-50
9.13.2 Control Signal Interface 9-50
9.13.2.1 General 9-50
9.13.2.2 Driver/Receiver 9-52
9.13.2.3 Control Signal Descriptions 9-52
9.13.3 Data Interface Signals 9-54
9.13.3.1 General 9-54
9.13.3.2 Driver/Receiver 9-54
9.13.3.3 Data Signal Descriptions 9-55

APPENDIX A DIAGNOSTIC, ERROR, AND DEVICE CODES

FIGURES

1-1	The Professional 300 Series Block Diagram	1-1
1-2	TMS Hardware Components	1-2
1-3	TMS Module Installation	1-3
1-4	Telephone Management System (TMS) Block Diagram	1-5
1-5	8031 Microprocessor Subsystem	1-11
1-6	Program Memory Read Cycle Timing	1-12
1-7	Data Memory Read Cycle Timing	1-13
1-8	Data Memory Write Cycle Timing	1-13
1-9	CTI Bus Interface Circuit Subsystem	1-15
1-10	Memory Subsystem	1-17
1-11	I/O Processing Subsystem	1-20
1-12	CODEC Circuit Subsystem	1-21
1-13	DTMF Circuit Subsystem	1-23
1-14	212A Modem Circuit Subsystem	1-26
1-15	Crossbar Signal Switch Functional Diagram	1-31
1-16	Call Progress Tone Detector Functional Diagram	1-32
1-17	TLI Module Functional Diagram	1-34
1-18	DTC11-B Voice Unit	1-36
1-19	Voice Unit Functional Block Diagram	1-38
2-1	Professional System Hardware Components	2-1
2-2	CP/M Option Module	2-2
2-3	Block Diagram	2-3
2-4	CTI Bus Interface Circuits	2-6
2-5	Z80 Microprocessor Circuits	2-8
2-6	Z80 Status Register Circuits	2-9
2-7	Z80 Microprocessor Firmware Logic	2-11
2-8	RAM Logic Circuits	2-12
2-9	Status Register Bit Assignments	2-16
3-1	DECNA Option Module, Transceiver Cable 5 Loopback Connector	3-1
3-2	Ethernet Elements (Example)	3-2
3-3	Ethernet Frame Format	3-3
3-4	DECNA Option Module Major Functional Block Diagram	3-4
3-5	DECNA Ethernet Interface	3-5
3-6	CTI Bus Interface	3-7
3-7	Bus Transceivers, Bus Command Registers, and Control Circuitry	3-8
3-8	Memory Access Register	3-11
3-9	Control Register (Command Control Latch)	3-13
3-10	Control Register Bit Values	3-14
3-11	Memory Read Base Address Register and Write-Only Latch, and Base Address Comparator	3-16
3-12	Dual-Ported Memory Base Address Register Bit Value	3-16
3-13	Option ROM, Address ROM, and ROM Address Logic	3-18
3-14	Dual-Ported Memory	3-20
3-15	Dynamic RAM	3-21
3-16	CTI Write/NI Write Selection	3-22

3-17 Dual-Ported Memory Controller 3-24
3-18 CTI Read/Write Decoder 3-28
3-19 Port A 3-29
3-20 Port B 3-31
3-21 Ethernet Interface 3-35
3-22 Ethernet Controller 3-35
3-23 Ethernet Serial Interface 3-39
3-24 Manchester Encoded Data 3-41
3-25 Broadband Compatibility Circuit 3-42
4-1 Professional 380 EBO Physical Layout 4-1
4-2 Extended Bitmap Option Functional Block Diagram 4-3
4-3 Connector J1 Pin Assignment 4-6
5-1 Controller Module System Relation 5-1
5-2 Controller Module 5-2
5-3 Controller Module Block Diagram 5-3
5-4 CTI Bus Interface Circuits 5-7
5-5 Microprocessor (μP) Control Circuits 5-9
5-6 Disk Control and Status Circuits 5-10
5-7 Modified Frequency Modulation (MFM) Write Data Circuits 5-11
5-8 MFM Read Data Circuits 5-13
5-9 Controller Module Data Flow Diagram 5-15
5-10 Controller Module Interface Signal Flow 5-16
6-1 Hard Disk Drive System Relation 6-1
6-2 Hard Disk Drive 6-3
6-3 Simple Block Diagram 6-3
6-4 Stepper Motor and Head Carriage Assembly 6-5
6-5 Air Flow Top View 6-7
6-6 Air Flow Side View 6-8
6-7 Spindle Motor Control Circuit Detail 6-11
6-8 Power-up Circuit Detail 6-13
6-9 Power-up Sequence Timing 6-14
6-10 Fault Detection Circuit Detail 6-15
6-11 Seek Circuit Detail 6-17
6-12 Seek Circuit Timing 6-19
6-13 Write Circuit Detail 6-20
6-14 Write Data Timing 6-21
6-15 Index Signal Timing 6-21
6-16 Read Circuit Detail 6-22
6-17 Read Data Timing 6-23
6-18 Interface Signal Connections 6-24
6-19 I/O Connector Locations 6-25
6-20 Internal Connection Locations 6-28
6-21 Read/Write Module Test Point Locations 6-31
7-1 RX50 Controller Module System Relation 7-1
7-2 RX50 Controller Module 7-2
7-3 RX50 Controller Module Block Diagram 7-3
7-4 CTI Bus to Controller Memory Interface Circuits 7-6
7-5 Microprocessor to Controller Memory Interface Circuits 7-11
7-6 Disk Control and Status Interface Circuits 7-13

7-7 MFM Write Data Interface Circuits 7-16
7-8 MFM Read Data Interface Circuits 7-18
7-9 RX50 Controller Module Interface Signal Flow 7-21
7-10 RX5CS0 Command Mode Bit Definitions 7-25
7-11 RX5CS0 Maintenance Status Mode Bit Definitions 7-27
7-12 RX5CS1 Command Mode Bit Definitions 7-28
7-13 RX5CS2 Command Mode Bit Definitions 7-30
7-14 RX5CS2 Extended Function Mode Bit Definitions 7-31
7-15 RX5CS3 Maintenance Mode Status Bit Definitions 7-32
7-16 RX5CS3 Extended Functions Mode Bit Definitions (Report) 7-33
7-17 RX5CS3 Extended Functions Mode Bit Definition (Set) 7-33
7-18 RX5CS4 Maintenance Status Mode Bit Definition 7-34
7-19 RX5CS4 Read/Write Status Mode Bit Definition 7-34
7-20 RX5CS4 Extended Functions Mode Bit Definition 7-35
7-21 RX5CS5 Bit Definitions 7-35
7-22 RX5CS5 Selectable Extended Functions 7-35
7-23 RX5EB Bit Definition 7-37
7-24 RX5FB Bit Definition 7-38
8-1 RX50 Dual Diskette System Relation 8-1
8-2 RX50 Dual Diskette Drive 8-2
8-3 The 5.25-inch Diskette 8-3
8-4 Write Protect Tab Application 8-4
8-5 Opening Access Doors 8-5
8-6 Inserting Diskette 8-5
8-7 Closing Access Doors 8-5
8-8 Simple Block Diagram 8-7
8-9 Mechanical Detail 8-9
8-10 Mechanical Operation 8-10
8-11 Select Circuit 8-15
8-12 Motor Control Circuit 8-17
8-13 Motor Control Wave Forms 8-18
8-14 Connections to Head Load Solenoids and Indicators 8-21
8-15 Status Circuit 8-22
8-16 Status Circuit Timing Relationships 8-23
8-17 Sensor 8-24
8-18 Stepper Motor Circuit 8-26
8-19 Stepper Motor Timing Relationships 8-27
8-20 Read/Write Interface Circuit 8-29
8-21 Write Data Timing Relationships 8-30
8-22 Read Data Timing Relationships 8-30
8-23 Write Circuit 8-31
8-24 Write Data to Head Current Conversion 8-33
8-25 Read Circuit 8-35
8-26 Head Signal to Read Data Conversion 8-36
8-27 RX50 Controller Module and Drive Interface Signal Flow 8-38
8-28 Seek and Interface Module Connector Locations 8-39
8-29 Motor Control Module Connector Locations 8-43
8-30 Read/Write Module Connector Locations 8-44
9-1 RD52-A ID Label Location 9-2

9-2 RD52-A Part Number Location 9-2
9-3 RD52-A Disk Drive 9-4
9-4 Drive Startup Current Profile 9-6
9-5 J3 Connector 9-7
9-6 RD52-A Mechanical Layout 9-8
9-7 Air Filtration System 9-10
9-8 PCB Jumper/Terminator Locations 9-11
9-9 RD52-A Block Diagram 9-13
9-10 RD52-A Drive Electronics 9-13
9-11 Encoder PCB Block Diagram 9-14
9-12 AGC Circuit 9-15
9-13 P1 and P2 Generation 9-15
9-14 Track 0 Detector 9-16
9-15 Control PCB Block Diagram 9-17
9-16 Write Circuit Block Diagram 9-19
9-17 Read Circuit Block Diagram 9-20
9-18 Motor Microprocessor 9-21
9-19 DC Motor Commutation Timing Diagram 9-22
9-20 DC Motor Drive Circuit (Simplified) 9-24
9-21 Wedge and Index Timing 9-25
9-22 Interface Connectors 9-27
9-23 J1 Connector 9-27
9-24 J2 Connector 9-27
9-25 Control Signal Driver/Receiver 9-28
9-26 Single Step Mode Timing 9-29
9-27 Buffered Step Mode Timing 9-29
9-28 Index Timing 9-30
9-29 General Control Timing 9-31
9-30 Data Signal Driver/Receiver 9-31
9-31 MFM Write Data Timing 9-33
9-32 MFM Read Data Timing 9-33
9-33 The RD52-A Disk Drive (30-23227-02) 9-33
9-34 Current Requirements 9-35
9-35 +12 V Startup Current 9-35
9-36 J3 Connector Layout 9-35
9-37 RD52-A Motor Assemblies 9-37
9-38 Jumper/Terminator Locations 9-38
9-39 RD52-A Block Diagram 9-39
9-40 Power Faults 9-42
9-41 Interface Logic 9-43
9-42 Read/Write Operations 9-48
9-43 Interface Connector Locations 9-50
9-44 J1 Connector 9-51
9-45 J2 Connector 9-51
9-46 Control Signal Driver/Receiver 9-52
9-47 Single Step Mode Timing 9-53
9-48 Buffered Step Mode Timing 9-53
9-49 Index Timing 9-54
9-50 Data Line Driver/Receiver 9-55
9-51 Read/Write Data Timing 9-55

TABLES

1-1	DTMF Transmit Receive Tone Pairs	1-24
1-2	DTMF Single Transmit Tones	1-24
1-3	212A Modem Test Signal Generation	1-28
1-4	RS232 Connector Signals	1-29
1-5	AT&T 212A Modem Switch Controls	1-30
1-6	AT&T 212A Modem Indicators	1-30
1-7	AT&T 212A Modem Option Jumpers	1-30
1-8	TLI Relay Control Signals	1-33
1-9	Status Indicator Signals	1-33
1-10	TLI Analog Control Signals	1-33
1-11	Voice Unit Control Signals	1-33
1-12	Telephone Line Interface Relay Control Signals	1-35
1-13	Voice Unit Interface Signals	1-36
2-1	Connector J1 Pin Description	2-14
2-2	Host Programming Registers	2-15
2-3	Z80 Self-Test Error Codes	2-19
2-4	Interface Self-Test Error Codes	2-19
2-5	Environmental Specifications	2-22
2-6	Power Specifications	2-22
3-1	Bus Transceivers, Bus Command Register, and Control Circuitry Signal Description	3-9
3-2	Memory Access Register Signal Description	3-12
3-3	Control Register Signal Description	3-15
3-4	Dual-Ported Memory Read Base Address Register, Write-Only Latch, and Base Address Comparator Signal Description	3-17
3-5	Option ROM, Address ROM, and ROM Address Logic Signal Description	3-19
3-6	Dynamic RAM Signal Description	3-22
3-7	CTI Write/NI Write Selector Signal Description	3-23
3-8	Dual-Ported Memory Controller Signal Description	3-25
3-9	CTI Read/Write Decoder Signal Description	3-28
3-10	Port A (CTI Data-to-Memory Buffer, Data Latch, and Address Latch) Signal Description	3-30
3-11	Port B (NI Data-to-Memory Buffer, Data Latch, and Address Latch) Signal Description	3-32
3-12	Ethernet Controller Signal Description	3-36
3-13	Ethernet Serial Interface Signal Description	3-40
3-14	Broad-Band Compatibility Circuit Signal Description	3-43
5-1	Connector J2 Pin Description	5-17
5-2	Connector J3 Pin Description	5-19
5-3	Programming Registers	5-20
5-4	Error Bit Definitions	5-21
5-5	Disk Drive Precompensation Cylinders	5-21
5-6	Sector ID Bit Definitions	5-23
5-7	Backup Revision Bit Definitions	5-23

5-8 Cylinder ID Bit Definitions 5-25
5-9 Head ID Bit Definitions 5-25
5-10 Command Byte Bit Definitions 5-25
5-11 Secondary Status Bit Definitions 5-25
5-12 STATUS/INIT Register Definitions 5-29
6-1 Control/Status Connector J1 6-25
6-2 Data I/O Connector J2 6-27
6-3 Power Connector J3 6-29
6-4 Motor Control Module Power Connector J4 6-29
6-5 HDA Connector J5 6-29
6-6 Index and LED Connector J6 6-29
6-7 Stepper Motor Connector J7 6-30
6-8 Track 0 Sensor Connector J8 6-30
6-9 Spindle Brake Connector J1 6-30
6-10 Spindle Motor Connector J2 6-31
7-1 RX50 Controller Memory Organization 7-4
7-2 Controller Module Responses to CTI Bus Addresses 20 through 26 7-9
7-3 Microprocessor Accesses to Addresses 20 through 26 7-12
7-4 Diskette Drive Select Signal Conversion 7-15
7-5 MFM Encoding 7-17
7-6 Precompensation MFM Data Pulse Shift 7-17
7-7 Connector J2 Pin Description 7-22
7-8 RX50 Controller Module Registers 7-24
7-9 Maintenance Status Mode Definitions 7-29
7-10 Read/Write Status Mode Definition 7-29
7-11 Command and Status Register Summary 7-39
7-12 Controller Initialization and Self-Test Sequence 7-42
8-1 Select Signals Jumper J17 Removed 8-14
8-2 Select Signals Jumper J17 Installed 8-14
8-3 Write Function Head Select 8-34
8-4 Read Function Head Select 8-36
9-1 Related Documentation 9-4
9-2 DC Power Requirements 9-7
9-3 Control Cable Pin Designations 9-28
9-4 Data Cable Pin Designation 9-31
9-5 J1/P1 Connector Pin Assignment 9-51
9-6 J2/P2 Connector Pin Assignment 9-54
A-1 System Error Numbers A-1
A-2 LED Display 1 ..... A-6
A-3 LED Display 2 ..... A-6
A-4 LED Display 3 ..... A-7
A-5 Bugcheck Codes A-8
A-6 Device Identification Codes A-9
A-7 I/O and DSW Codes A-11
A-8 POSSUM Error Codes A-16
A-9 MS-DOS Error Codes A-19

INTRODUCTION

Volume 2 of the *Professional 300 Series Technical Manual* documents design concepts and hardware functions of all available system options and option modules for the Professional 300 Series computer system.

MANUAL ORGANIZATION

Volume 2 contains information about all available system options and option modules. The following paragraphs describe this manual.

Chapter 1, Telephone Management System – describes the telephone management system, including the voice unit.

Chapter 2, CP/M 80 Option Module – describes the CP/M 80 option module and how it works in the Professional 300 computer system.

Chapter 3, DECNA Controller Option Module – describes the Digital Ethernet CTI Bus Network Adapter, how it connects to other devices, and how it works in the host system.

Chapter 4, Professional 380 Extended Bitmap Option Module – describes the Extended Bitmap Option (EBO) module for the Professional 380 and provides connector pin assignments.

Chapter 5, RD50/RD52 Hard Disk Drive Controller Module – describes RD50 and the RD52 Hard Disk Drive Controller module and provides a functional and detailed description of each circuit.

Chapter 6, RD50/RD51 Hard Disk Drive – describes how the RD50 Hard Disk Drive works. This chapter also describes how to remove and replace the hard disk drive read/write module.

Chapter 7, RX50 Controller Module – provides a functional and detailed description of each circuit in the RX50 Controller Module.

Chapter 8, RX50 Dual Diskette Drive – describes how the RX50 Dual Diskette Drive works.

Chapter 9, RD52 Hard Disk Drive – provides functional and detailed descriptions of the RD52 Hard Disk Drive.

RELATED INFORMATION

The following paragraphs describe where to find information that is not contained in this manual (*Professional 300 Series Technical Manual Volume 2*). The *Professional 300 Series Technical Manual Volume 1* describes the kernel system. Volume 2 describes all available system options. Both volumes contain operating descriptions, register information, and hardware specifications.

Field Service Information

Neither volume of the technical manual contains any system diagnostic procedures. Refer to the following two pocket service guides for any Field Service diagnostic and repair procedures.

Professional 350 Pocket Service Guide	(EK-PC350-PS)
Professional 380 Pocket Service Guide	(EK-PC380-PS)

Option Module Information

Refer to Chapter 11 in Volume 1 for more information about the CTI Bus Memory Option module.

Refer to Chapter 6 in Volume 1 for more information about the Professional 350 Extended Bitmap Option module.

The Real-Time Interface Module (RTI) provides the following three commonly used communications interfaces for data collection on a Professional 300 Series computer system.

- Serial Line Interface – Two full-duplex, asynchronous serial lines that conform to the EIA RS-232C/RS-423 communication standard.
- IEEE-488 Bus Port – An IEEE-488 port that handles bus protocol automatically in talker, listener, or controller-in-charge modes.
- Programmable Parallel Port – A 24-bit programmable parallel port with three operating modes, including handshaking and bidirectional modes for customized data interfaces.

You can find a detailed technical description of the Real-Time Interface Module in the *Real-Time Interface Module/Analog Data Module Technical Manual* (EK-PCRTI-TM).

The Analog Data Module (ADM) allows real-time collection of analog data. The ADM converts analog signals between −5 and +5 volts into 16-bit digital values, offering a resolution of one part in 65,536 (96 dB). A programmable preamplifier with autoranging extends the dynamic range to 132 dB. The ADM also provides an eight channel multiplexer, a programmable real-time clock, and a variety of triggering modes. The RTI is a necessary prerequisite for ADM operation.

You can find a detailed technical description of the Analog Data Module in the *Real-Time Interface Module/Analog Data Module Technical Manual* (EK-PCRTI-TM).

The following documents provide more information about system options for the Professional 300 Series computer system.

Title	PN
Professional 350 Pocket Service Guide	EK-PC350-PS
Professional 380 Pocket Service Guide	EK-PC380-PS
Professional 350 Illustrated Parts Breakdown	EK-PC350-IP
Professional 380 Illustrated Parts Breakdown	EK-PC380-IP
Professional 300 Series Owner Manual	AA-N587A-TH
Professional 300 Series Installation Guide	AZ-N626A-TH
Professional 350 User Guide For Hard Disk Systems	AA-N603A-TH
Professional 350 Field Maintenance Print Set	MP-01394-00
Professional 380 Field Maintenance Print Set	MP-01922-01
VR201 Field Maintenance Print Set	MP-01410-00
LK201 Field Maintenance Print Set	MP-01395-00
KEF11 Field Maintenance Print Set	MP-01473-00
KDJ11 Field Maintenance Print Set	MP-01957-01
VC241-B Field Maintenance Print Set	MP-01970-01
MSC11-B Field Maintenance Print Set	MP-02003-01

CHAPTER 1
TELEPHONE MANAGEMENT SYSTEM

1.1 INTRODUCTION

This chapter describes the telephone management system (TMS), which is represented by the shaded portion of Figure 1-1. The TMS provides modem and voice capabilities for the Professional 300 series computer.

1.1.1 Related Documentation

Refer to the *DTC11-A Field Maintenance Print Set* (MP-01654-01) while you read this chapter.

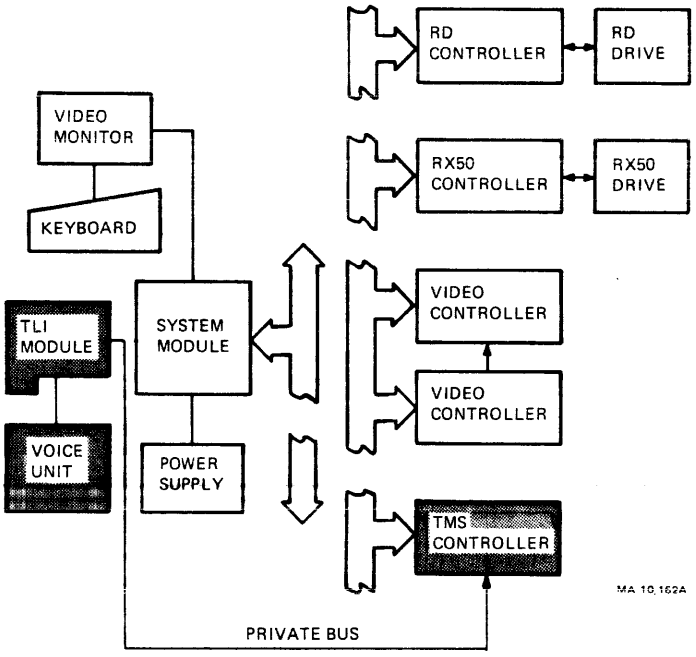


Figure 1-1 Professional 300 System Block Diagram

1.1.2 Physical Description

The TMS consists of three hardware components: the TMS controller module, the telephone line interface (TLI) module, and the optional voice unit (Figure 1-2).

1.1.2.1 TMS Controller Module – The TMS controller is a 30.5 cm × 13.3 cm (12 in × 5-1/4 in) module (Figure 1-2). It uses a zero insertion force (ZIF) connector to install into any open slot in the CTI Bus card cage. The TMS controller manages all telephone line operations to and from the Professional computer system.

The TMS controller is a field replaceable unit (FRU). Its part number is PN 54-15215. Figure 1-3 shows where the TMS controller module is installed.

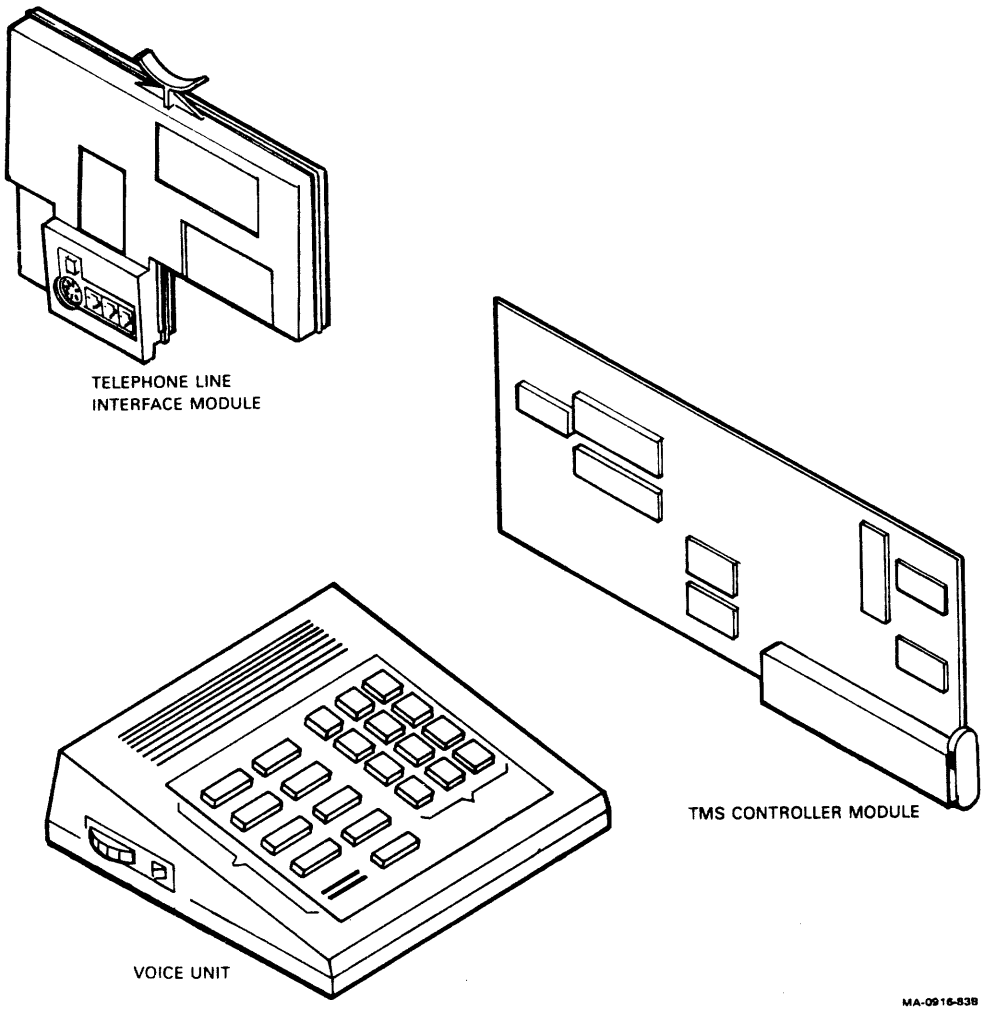


Figure 1-2 TMS Hardware Components

1.1.2.2 Telephone Line Interface (TLI) Module

The telephone line interface (TLI) is a nonstandard 19.1 cm × 13.3 cm × 2.5 cm (7-1/2 in × 5-1/4 in × 1 in) module that you install into a connector located just behind the card cage on the system module (Figure 1-3). The TLI provides an interface between the voice unit and the TMS controller, and between the Professional computer system and the public telephone network. The TLI provides this interface through the following four connectors (Figure 1-3).

Telephone set
Phone line 1
Phone line 2
Voice unit

The TLI is an FRU (PN 70-20405). Figure 1-3 shows where the TLI module is installed.

1.1.2.3 Voice Unit – The voice unit (Figure 1-2) is a 19.1 cm × 17.2 cm × 3.8 cm × 1.9 cm (7-1/2 in × 6-3/4 in × 1-1/2 × 3/4 in) intelligent desktop unit. It connects to the TMS controller by a signal and power cable that plugs into a circular DIN connector on the back of the TLI module. The voice unit contains an internal microphone and speaker, and a low profile keyboard for telephone dialing and voice file manipulation. The voice unit is an FRU (PN DTC11-B).

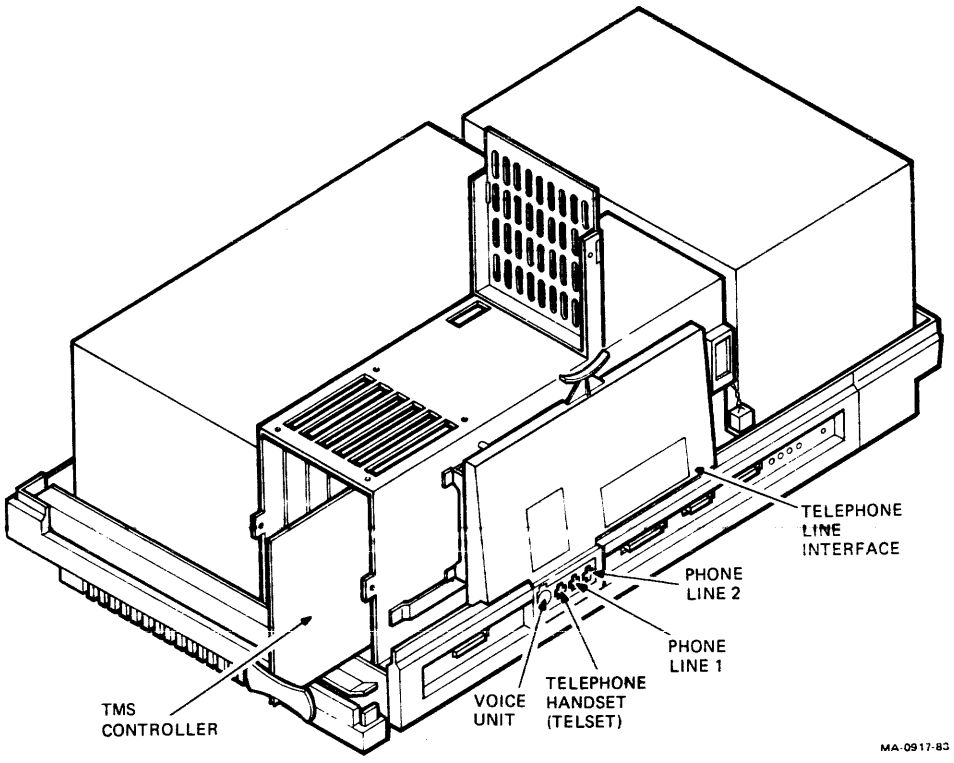


Figure 1-3 TMS Module Installation

1.2 TMS SYSTEM LEVEL FUNCTIONAL DESCRIPTION

The TMS manages telephone line communications in one of the following formats: digitized voice or dual-tone multifrequency (DTMF) data. This paragraph describes how TMS performs voice and data communications.

The TMS controller transmits and receives voice communications through the TLI module along one of two paths. One path channels voice communications directly to and from the telephone network over either of two connected lines: the voice unit or the customer's telephone handset. Both lines are connected to the TLI module.

NOTE

The telephone handset is always connected to phone line 1 through the telephone handset (Telset) connector on the TLI module. The telephone has control automatically whenever the handset is lifted from the cradle.

The other path transmits and receives voice communications through the TLI by using the coder/decoder (CODEC) logic on the TMS controller. The CODEC logic is used to store and retrieve voice communications, in digital form, on a system disk. This logic encodes analog voice data into digital data, and then decodes this digital data into analog voice.

The TMS controller uses a universal asynchronous receiver/ transmitter (UART), in the 8031 microprocessor, to perform dual-tone multifrequency (DTMF) data transactions. The serial data output is converted to a modulated analog signal for transmission over the public telephone network by a modem subsystem resident on the TMS controller. Data communications occur on one of two lines during any given transmit or receive cycle. For example, if data is being transmitted and/or received on line 2, line 1 can be used to support CODEC or DTMF communications.

Paragraphs 1.2.1 through 1.2.3 provide a functional description of each TMS component. Each component is described to the system block diagram level (Figure 1-4). Refer to the system block diagram while you read this section.

1.2.1 TMS Controller Module

The TMS controller module controls all telephone line operations. It consists of the following eight circuit subsystems.

Microprocessor subsystem
CTI Bus interface
Memory subsystem
I/O processing subsystem
Communications subsystem
Crossbar switching circuit
TLI/voice unit interface
Call progress tone detector

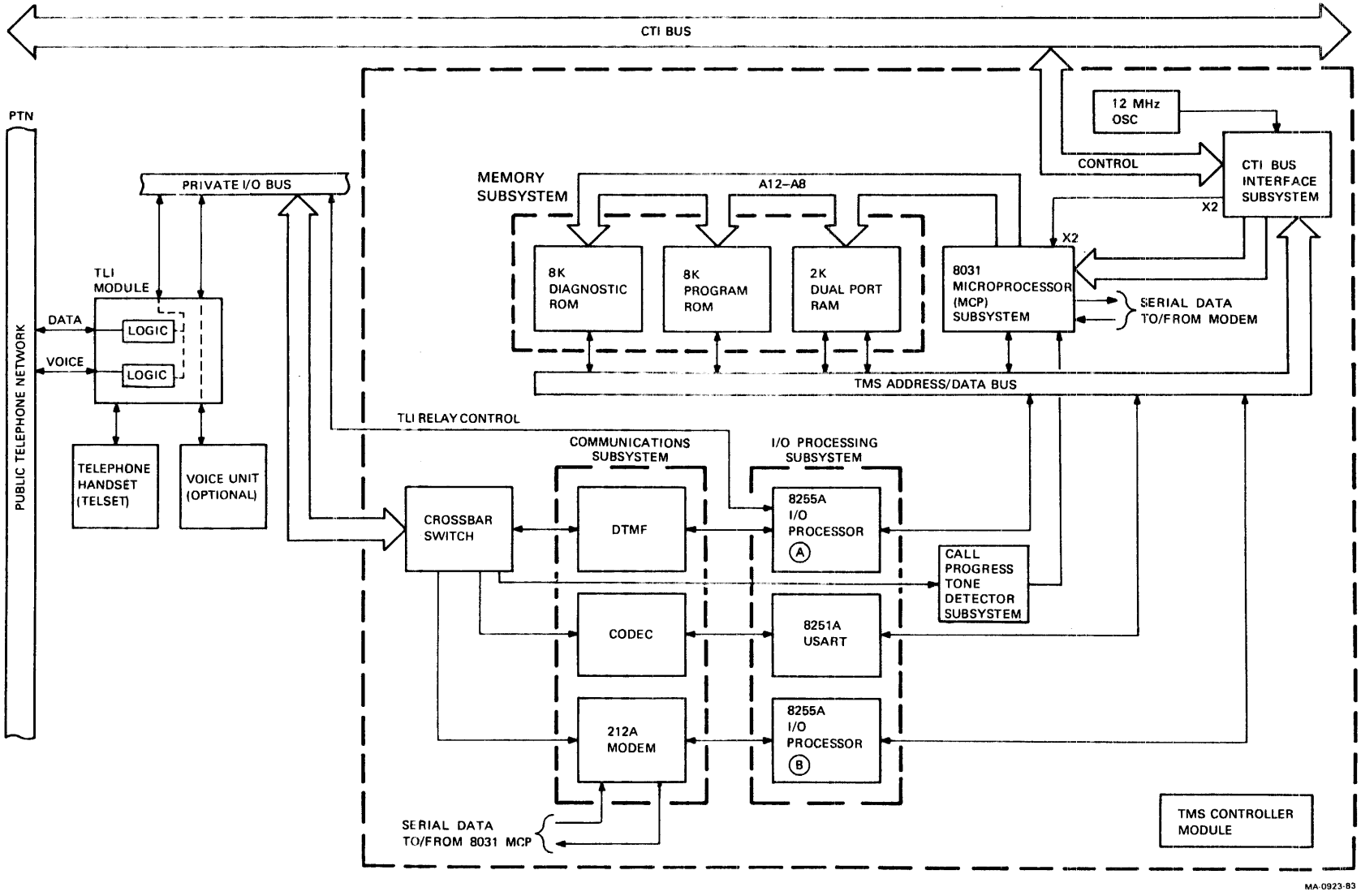


Figure 1-4 Telephone Management System (TMS) Block Diagram

1.2.1.1 Microprocessor Subsystem – The TMS controller uses an 8031 microprocessor to manage all TMS communications. The 8031 microprocessor controls all telephone line operations for the Professional computer system. It performs the following functions.

- Generates status and error messages to the Professional computer system
- Accepts control commands and data from the Professional computer system
- Controls the use of the TMS internal bus
- Controls the data paths between the TMS and the public telephone network

1.2.1.2 CTI Bus Interface – The TMS controller communicates with the Professional computer system through a shared memory interface called the CTI Bus interface. Under firmware control, the CTI Bus interface exchanges commands and data between the TMS microprocessor and the Professional computer system through the 2-kilobyte dual-ported random access memory (RAM) located on the TMS controller (Paragraph 1.3.1.3).

The CTI Bus interface consists of two programmable array logic (PAL) units and three drivers. It performs the following functions.

- Latches CTI Bus addresses and data onto the TMS internal bus
- Controls access to dual-ported RAM space
- Generates data transfer strobes
- Transfers data and commands between the TMS microprocessor and the Professional computer system

1.2.1.3 Memory Subsystem – The TMS memory subsystem consists of the following three memory logic circuits.

1. An 8-kilobyte read only memory (ROM) that contains the firmware used for the telephone management system
2. A second 8-kilobyte ROM that contains power-up and self-test diagnostics
3. A 2-kilobyte RAM that is a temporary holding area for data and command transfers between the Professional computer system and the TMS microprocessor

1.2.1.4 I/O Processing Subsystem – The TMS I/O processing subsystem consists of two 8255A programmable peripheral interface (PPI) I/O processors and one 8251A universal synchronous/asynchronous receiver/transmitter (USART) processor. These devices control the CODEC, DTMF, and modem subsystems (Paragraph 1.3.1.5).

The I/O processing subsystem device has the following functions.

- I/O processor A (8255A PPI) controls the operation of the DTMF subsystem and the TLI module.
- I/O processor B (8255A PPI) controls the operation of the modem subsystem.
- The 8251A USART controls the operation of the CODEC subsystem.

1.2.1.5 Communications Subsystem – The TMS communications subsystem consists of the following three circuit subsystems.

Coder/Decoder (CODEC) Circuit Subsystem
The CODEC circuit subsystem encodes voice to a digital format for storage on hard disk and decodes it back to analog for voice message playback through the voice unit, or for transmission over the telephone lines. A continuously variable slope delta (CVSD) CODEC integrated circuit is used for coding and decoding voice.

Dual-Tone Multifrequency (DTMF) Circuit Subsystem
The DTMF circuit subsystem allows data and command transmission to or from the Professional computer system from a remote pushbutton telephone handset or similar DTMF entry keypad. The DTMF circuit subsystem consists of the following two parts.

1. A DTMF transmitter integrated circuit

2. A DTMF receiver that consists of a decoder integrated circuit and a bandsplit filter integrated circuit

212A Modem Circuit Subsystem
A modem chip set, which consists of two integrated circuits, is used to implement the functionality of an AT&T 212A modem. This modem chip set supports low-speed frequency shift keyed (FSK) and high-speed differential phase shift keyed (DPSK) data communications.

1.2.1.6 Crossbar Switching Circuit – The crossbar switching circuit is two integrated circuits that provide complete signal switching paths for the TMS controller. Configured as a switch matrix, the crossbar switching circuit lets the host or TMS processor give any communications device access to the public telephone network. The crossbar signal switch also connects internal signal paths used to test the TMS hardware, and allows a local voice unit connection for recording voice messages on hard disk. Paragraph 1.3.1.6 provides more information about the crossbar switching circuit.

1.2.1.7 TLI/Voice Unit Interface – A collection of drivers and discrete components on the TMS controller form the interface to the TLI and the voice unit. The TLI/voice unit interface buffers the following four signals.

1. Digital and analog signals between the TMS controller and phone lines 1 and 2

2. Digital and analog signals between the TMS controller and the voice unit

3. Control signals from the TMS controller to the TLI

4. Ring and off-hook status signals from the phone lines to the TMS controller

1.2.1.8 Call Progress Tone Detector – A call progress tone detector is used to detect telephone dial tones and assist automatic call placement. This circuit detects audio energy from 350 Hz to 620 Hz.

1.2.2 Telephone Line Interface (TLI) Module

The telephone line interface (TLI) is a collection of circuits that provide an interface to the public telephone network, the voice unit, and the telephone handset. It consists of the following five circuit groups.

Line switching relay circuits
Line coupling circuit
Ring-in detector circuit
Off-hook detector circuit
Voice unit interface

1.2.2.1 Line Switching Relay Circuits – The TLI includes five line switching relay circuits. These relay circuits, under firmware control, manage all signal flow through the TLI to and from the public telephone network.

Each relay circuit has a dedicated control line to the I/O bus. Each circuit consists of an I/O bus line receiver, a relay driver, and a single-pole double-throw (SPDT) relay.

1.2.2.2 Line Coupling Circuit – The line coupling circuit is a hybrid circuit that consists of a line coupling transformer and a duplexer. Each coupler provides the following functions.

- Conversion from a 2-wire telephone loop to a 4-wire interface compatible with the telephone management system
- DC isolation between the public telephone network and the Professional computer system
- Amplification and coupling of transmitted signals between the public telephone network and the telephone management system

1.2.2.3 Ring-In Detector Circuit – The ring-in detector circuit provides line isolation and detects incoming ring signals from the public telephone network.

1.2.2.4 Off-Hook Detector Circuit – The off-hook detector circuit detects the presence of an off-hook current when the telephone handset is lifted off the telephone cradle. An optoisolator is used to detect the off-hook current.

1.2.2.5 Voice Unit Interface – The voice unit interface is a 7-line hardwire connection to the TMS controller through the TLI module. All data to and from the voice unit passes through the TLI module by way of this interface. The only exception is the reset line, which is generated on the TLI module.

1.2.3 Voice Unit

The voice unit is an intelligent desktop unit that provides keyboard entry, visual status indicators (LEDs), and connection to the public telephone network or CODEC subsystem. The voice unit consists of the following six functional components.

8051 microcomputer
Keyboard
LED display
Microphone
Speaker
Remote equipment jack

Communication with the TMS controller occurs through a pair of 120-baud serial data lines. The controller sends commands to the voice unit for the LED displays and analog voice circuits. The voice unit monitors and reports to the controller all keystrokes, foot switch status, and voice detect circuit status.

1.2.3.1 8051 Microcomputer – The voice unit uses an 8051 microcomputer to perform the following functions.

Monitor all keystrokes on the voice unit keyboard
Control the LED displays
Monitor and control the analog voice circuit
Monitor the foot switch
Report all status back to the TMS controller

1.2.3.2 Keyboard – The voice unit has one keyboard separated into two keypads. The numerical keypad is used for telephone dialing and/or inputting DTMF code sequences. The control keypad is used to create, edit, and manipulate voice files. It performs the following nine functions.

NOTE
The first seven functions listed are supported by applications software and can change depending on the applications package. The last two functions, Microph and ON/OFF, are hardwired and cannot change under software control.

1. **Record** – records voice messages onto the hard disk.

2. **FastFwd** – moves the hard disk forward to the next voice or document file.

3. **Insert** – lets you make a voice insert in the middle of a voice file.

4. **Pause** – temporarily stops voice recording or playback.

5. **Play** – plays back recorded voice messages for you to listen to on the internal speaker or headset.

6. **Rewind** – moves the hard disk back to the previous voice or document file.

7. **Comment** – lets you record a voice comment to a document file.

8. **Microph** – turns the microphone on and off.

9. **ON/OFF** – turns the numerical keypad on and off for telephone dialing.

1.2.3.3 LED Display – Nine LEDs on the back of the system unit show the current status (enabled or disabled) of each key on the control keypad. Each LED is next to a corresponding key and comes on when that key function is being used.

1.2.3.4 Speaker – An internal speaker or optional external headphones are used to monitor CODEC or telephone communications. The speaker contains the following five circuit groups.

Automatic level control (ALC) filter
ALC amplifier
ALC feedback circuit
Speaker power amplifier
Voice detection circuit

1.2.3.5 Microphone – A microphone circuit controls either the internal microphone or the optional external microphone. The microphone circuit contains the following five components and circuit groups.

External microphone jack
Sensitivity switch
Microphone preamplifier
ALC circuit
Seesaw control circuit

1.2.3.6 Remote Equipment Jack – A remote equipment jack connects the optional foot switch, external microphone, and headphones to the voice unit.

1.3 DETAILED DESCRIPTION

This section provides detailed descriptions of the TMS components. Complex timing sequences and computer operations are described only when necessary. Refer to the *DTC11-A Field Maintenance Print Set* while you read these descriptions.

All the illustrations in this section are functional block diagrams. Logic symbols indicate function and may not represent actual circuitry.

NOTE
For detailed information about the 8031 microprocessor and 8051 microcomputer architecture, refer to the Intel Peripheral Design Handbook (available from Intel Corporation).

1.3.1 TMS Controller Module

The TMS controller module controls all telephone line operations. An 8031 microprocessor manages the communications resources on the controller module. An 8-kilobyte ROM/EPROM contains the firmware for the TMS. A local bus (the TMS address and data bus) provides access to the memory, communications, and I/O circuit subsystems. Access to the TMS bus is through tristate buffers that also provide access to the CTI Bus processor. A CTI Bus interface circuit controls access to the TMS bus and also provides timing for the 8031 microprocessor.

The following paragraphs describe in detail each circuit subsystem on the TMS controller module.

1.3.1.1 8031 Microprocessor Subsystem – The telephone management system controls all telephone line operations through the 8031 microprocessor subsystem (Figure 1-5). This paragraph describes chip timing and bus cycle timing for the 8031 microprocessor.

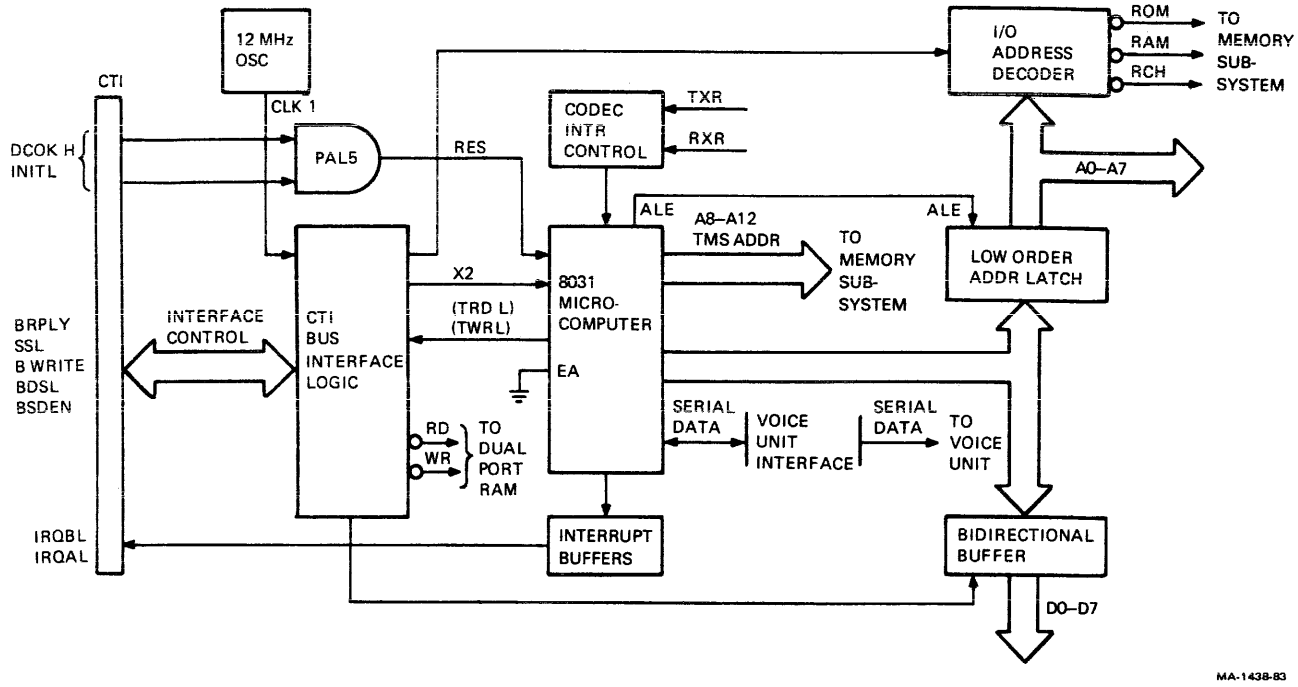


Figure 1-5 8031 Microprocessor Subsystem

8031 Chip Timing

A 12 MHz oscillator generates the clock signal required to synchronize all the 8031 internal operations. The clock pulse is fed to the CTI Bus interface logic and driven into the X2 pin of the 8031.

The external address (EA) pin is grounded. During a program fetch, program strobe enable L (PSEN L) goes high, which prompts the 8031 to fetch an instruction from the program memory ROM.

Under program control by the Professional, initialize L (INIT L) is driven low to reset the TMS, and is held low until power to the TMS is stable. When CTI Bus dc power OK L (DCOK) goes high, the 8031 starts the program from location 0000 in program memory.

If either PSEN L or DCOK L goes high, the 8031 starts the program.

8031 Bus Cycle Timing

The 8031 uses two memory cycles: the program memory cycle and the data memory cycle (Figures 1-6, 1-7, and 1-8). The program memory cycle allows the 8031 to gain access to the firmware ROM. The data memory cycle allows the 8031 to gain access to the 2-kilobyte dual-ported RAM and I/O processing subsystem. Figure 1-4 shows the relationship between the dual-ported RAM and the I/O processing subsystem.

Program Memory Cycle – The 8031 gains access to the program ROM through program memory cycles. Each program memory cycle is 12 clock pulses long (Figure 1-6). Two bytes of firmware are transferred from the TMS program ROM during each cycle.

NOTE

Each clock pulse is a period of time during any given program or data memory cycle. These time periods are called T1 through T12, at a 12 MHz clock rate where T equals 83.3 microseconds (μs).

During T2, address latch enable (ALE) is asserted, which places port P0 of the 8031 in a ready (float) state to generate the address for a 2-byte fetch from the program ROM. During T3, port P0 drives the low order addresses (A0–A7) onto the TMS address and data bus, where they are gated to the program ROM by the low order address latch. The high order addresses (A8–A12) are asserted during T3 and driven onto the TMS bus from port P2 to a page register. During T4, ALE is negated, which allows the assertion of the chip select signal (program strobe enable – PSEN) for the program ROM. PSEN enables the program ROM to drive the firmware data onto the TMS bus. This condition is held throughout T5 and T6, gating the two-byte firmware data to the 8031 at the end of T7.

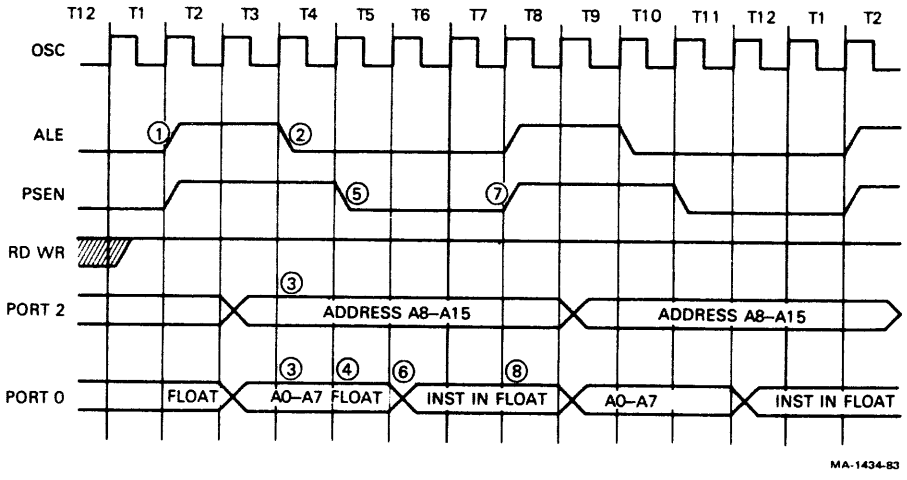


Figure 1-6 Program Memory Read Cycle Timing

Data Memory Cycle – The 8031 gains access to the buffer RAM and I/O devices through data memory cycles. Each data memory cycle is 12 clock pulses long. One byte of data is transferred per cycle.

For T2 through T4, the assertion/negation time sequence is the same as the program memory cycle. During a data memory read cycle (Figure 1-7), a read strobe (RD) is generated by the 8031 and asserted during T7. This state is held for six clock pulses from T7 through T12. Data is gated to the 8031 on a low to high transition, or when RD is asserted low.

During a data memory write cycle (Figure 1-8), data is driven onto the TMS address and data bus from the 8031 port P0 during T6 and held for nine clock pulses to T2. A write data strobe (WR) is asserted during T7 and held through T12. Addresses A0 through A7 are decoded by the I/O address latch to select the required memory or I/O device.

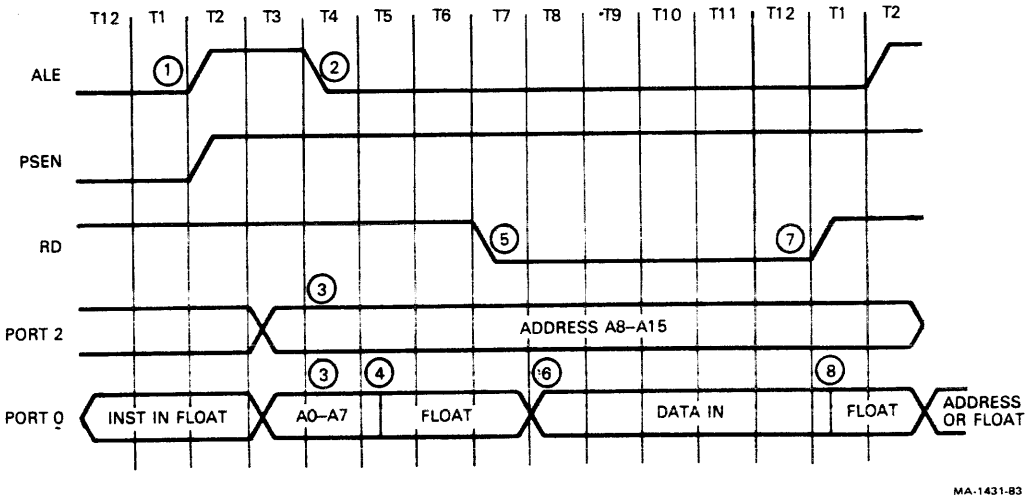


Figure 1-7 Data Memory Read Cycle Timing

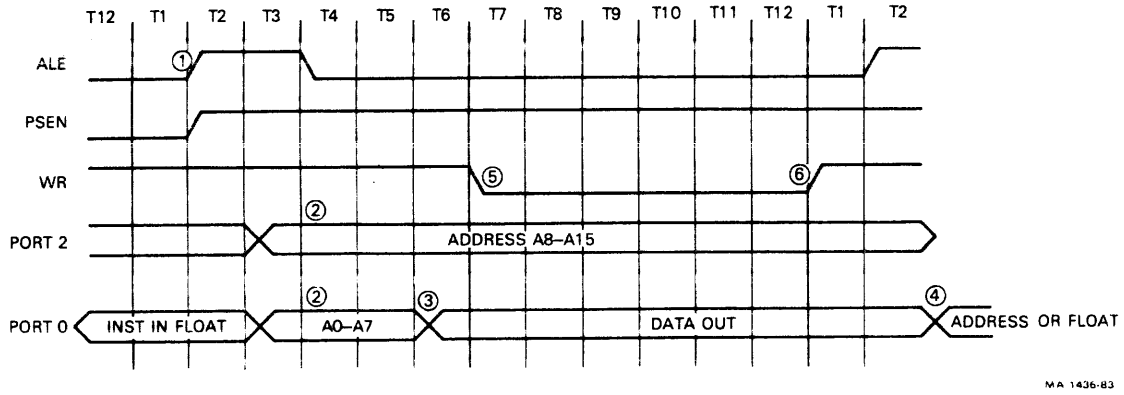


Figure 1-8 Data Memory Write Cycle Timing

1.3.1.2 CTI Bus Interface Circuit Subsystem – The TMS controller communicates with the Professional through the CTI Bus interface (Figure 1-9). The CTI Bus interface exchanges commands and data with the TMS 8031 microprocessor and the CTI microprocessor through buffers located in the dual-ported RAM.

The CTI Bus interface consists of the following three components.

Programmable array logic 1 (PAL1)
Programmable array logic 2 (PAL2)
CTI control bus buffer

The following three components control the CTI Bus interface function to the diagnostic ROM and the dual-ported RAM in the memory subsystem.

Programmable array logic 4 (PAL4)
Programmable array logic 5 (PAL5)
CTI Bus address and data latch

The CTI Bus interface exchanges data and commands between the TMS controller and the Professional microprocessor by performing the following functions.

CT/TMS memory cycle timing
CT/TMS memory cycle timing control
Address and data bus buffering

The TMS controller appears as 64 bytes of memory, mapped as the lower byte in 64 words. The first location is reserved for the 8-kilobyte serially accessed diagnostic ROM. The second location is reserved for a page pointer that selects the RAM page to be accessed through the remaining 62 locations (004–176). This pointer is initialized to 000 and scans the diagnostic ROM. One of the 32 buffers in dual-ported RAM is selected by loading the page pointer with 000 to 037.

On power-up, either the CTI Bus dc power okay (DCOK) signal or the initialize (INIT) signal generates a reset to the 8031 microprocessor. When the power-up self-test is complete, TMS ready (TRDY) is asserted and the CT/TMS memory cycle begins.

The CTI Bus interface latches a CTI Bus cycle address and TMS bus address to the TMS microprocessor. The interface waits until a memory cycle is complete, then interrupts the clocks to the 8031 microprocessor to perform the following functions.

- Gate the CTI Bus address and the TMS bus address to the TMS address and data bus
- Generate data transfer strobes
- Complete data transfers
- Release the 8031 microprocessor
- Wait for the CTI processor to finish its cycle

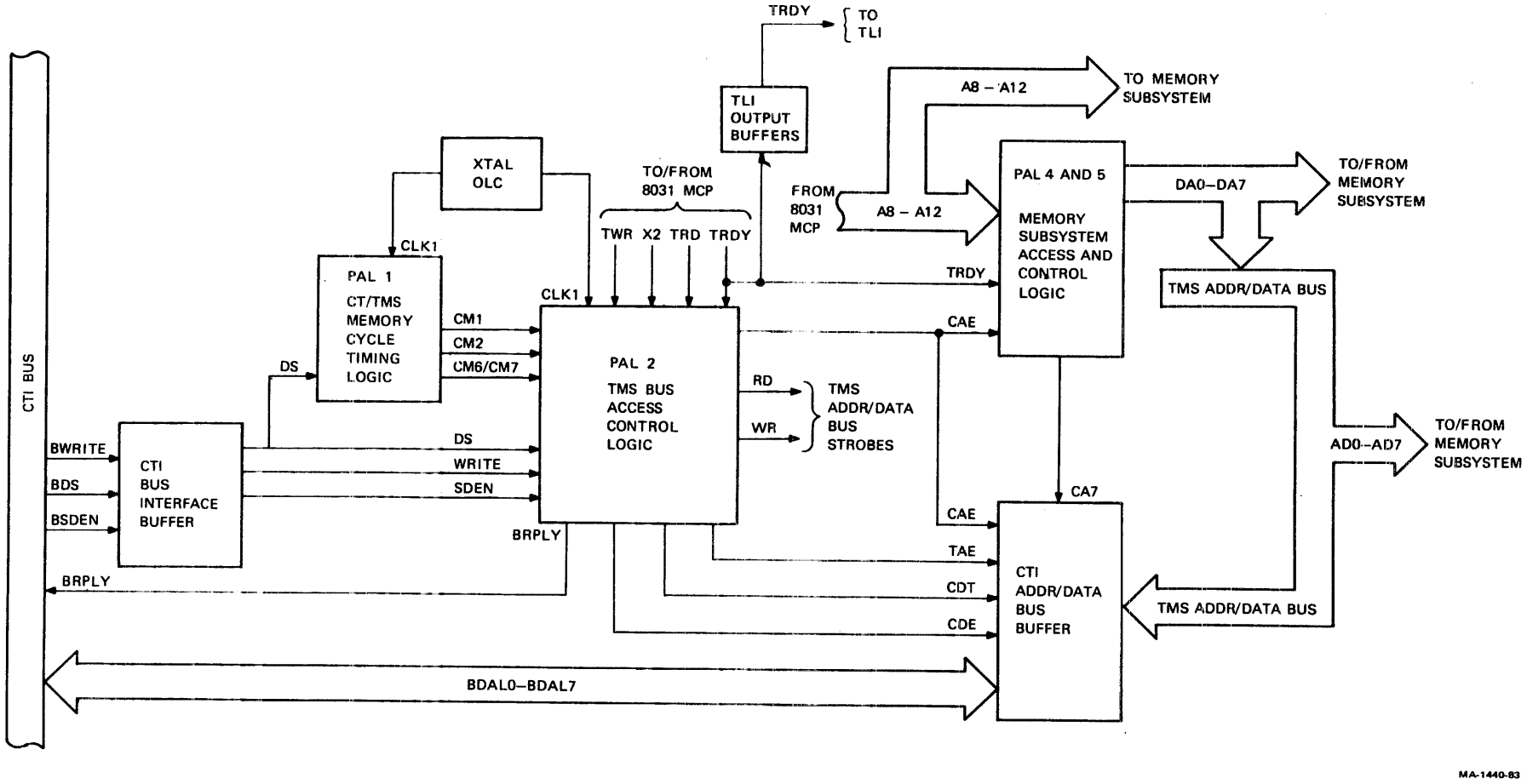


Figure 1-9 CTI Bus Interface Circuit Subsystem

CT/TMS Memory Cycle Timing
Programmable array logic 1 (PAL1) generates CT/TMS memory cycle timing. The CT request (CRQ) signal is a request for the TMS address and data bus from the Professional. CRQ is generated by the slot select (SS) decode signal from the CTI Bus, gated to the CTI interface circuit subsystem by the CTI Bus data strobe (DS), and sampled while a TMS processor cycle is in progress. This occurs after a previous CT/TMS memory cycle has ended. When address latch enable (ALE) is asserted, CRQ is reset (set high), if a previous CTI Bus cycle has completed (indicated by CM7 set high).

The second signal, CT/TMS memory cycle 1 (CM1), is set by a valid CRQ sampled during the first ALE clock cycle (Figure 1-6), and held until a TMS address and data bus cycle has completed.

CM1, generated by PAL2, represents the window through which a CT/TMS memory cycle occurs. This signal halts the 8031 clocks, switches the bus buffers on the TMS address and data bus, and controls the assertion of the TMS bus data strobes, write (WR) and read (RD).

The third signal, CM2, is the CT/TMS memory cycle data strobe. It lets addresses and data transfer between the CTI Bus and the TMS address and data bus.

The fourth, fifth, and sixth signals – CM3, CM4, and CM5 – are shift register delays in PAL1. These internal functions are not reflected in the CTI Bus interface functional diagram.

The seventh and eighth signals, CM6 and CM7, end a CT/TMS memory cycle by feeding back and inhibiting the first six bits. CM6 and CM7 remain asserted until the 8031 begins another CT/TMS memory cycle and the CTI Bus data strobe has been released. This tells the 8031 that the CTI processor has finished its memory cycle.

CT/TMS Memory Cycle Timing Control
PAL2 generates the strobes that control the TMS address and data bus and the 8031 processor clock.

The 12 MHz 8031 clock (X2) is gated by the CM1. The X2 clock is generated directly from the 12 MHz oscillator.

TMS address enable (TAE) and CT address enable (CAE) control the output latches that gate addresses from the 8031 or the CTI Bus onto the TMS address and data bus.

Write and read (WR and RD) are the TMS address and data bus data strobes. During a TMS microprocessor cycle, they are generated by the TMS write (TWR) and TMS read (TRD) strobes from the 8031. During a CT/TMS memory cycle, WR and RD are generated from the CTI Bus data strobe and write command.

CT data enable (CDE) and CT data transmit (CDT) control the bidirectional data bus buffer. Data are gated from the CTI Bus to the TMS address and data bus during a CM write cycle. Write data are latched by the CTI DS strobe. The data are latched from the TMS address and data bus to the CTI Bus during a CM read cycle by the slave data enable (SDEN) strobe. Then the data are enabled by the TMS ready (TRDY) control signal from the 8031. Read cycle data are latched by CM1 to let the cycle end while DS is being negated. These strobes hold the data on the CTI Bus until the negation of DS releases CM6 in PAL1. Contention on the TMS address and data bus is prevented by logic in the 8031 and in PAL1. If ALE is asserted, the 8031 data strobes are always negated. CT/TMS memory cycles are active only when ALE is asserted. When ALE is negated, CT/TMS memory cycles are inhibited and the 8031 data strobes are enabled.

The CTI Bus data transfer acknowledge signal bus reply (BRPLY) is generated by CM6. BRPLY is held by CM6 and DS until DS is released by the CTI Bus.

Address and Data Bus Buffering
The CTI Bus is connected to the TMS address and data bus by the bidirectional CTI address and data bus latch. (This corresponds to E13 and E1 on Sheet 2 of 6 in the *DTC11-A Field Maintenance Print Set.*) TMS appears on the least significant byte of each word. The upper eight bits are not connected.

Bidirectional latching is necessary to allow the fixed-length CT/TMS memory cycle to work with the asynchronous CTI Bus. Using DS to latch write cycle data, the CTI processor can deposit data into the dual-ported RAM and relinquish control before a memory cycle is complete.

The TMS controller is assigned 64 consecutive word addresses in the CTI Bus address space. CTI Bus data and address lines 1 through 6 (BDAL1–BDAL6) are sampled to form six bits of the TMS bus address. The I/O page select bit (CA7) extends that address to eight bits. Addresses are gated onto the TMS bus by CAE from PAL2.

1.3.1.3 Memory Subsystem – The memory subsystem (Figure 1-10) for the TMS controller consists of the following four components.

8031 program ROM
2-kilobyte dual-ported RAM
8-kilobyte diagnostic ROM
Memory address register

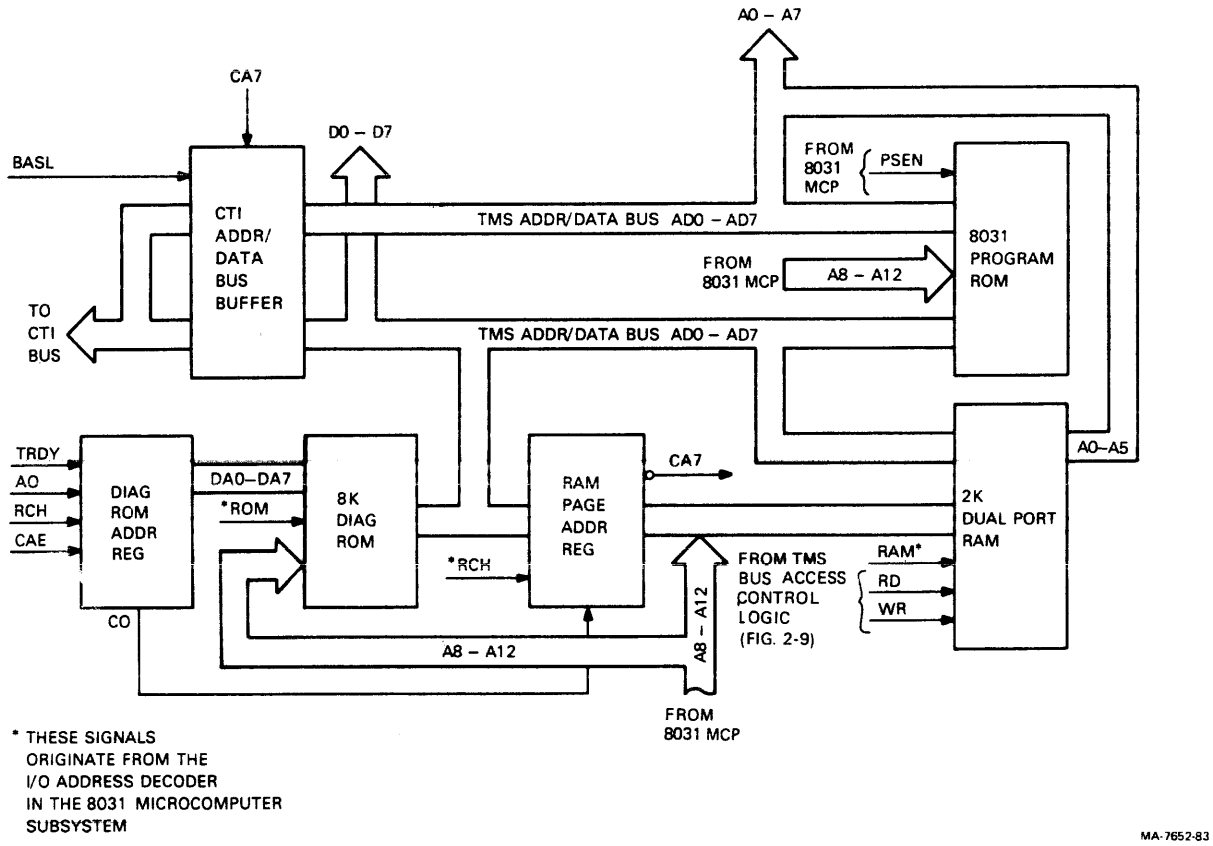


Figure 1-10 Memory Subsystem

8031 Program ROM
The 8031 program ROM has 8 kilobytes of read only memory. The TMS address bus (low order address lines A0–A7) and the TMS data bus (D0–D7) are tied directly to the program ROM. The high order address lines are tied directly to the ROM and the TMS data bus. The program ROM outputs data onto the bus when the 8031 asserts PSEN.

2-Kilobyte Dual-Port RAM
The TMS and CTI microprocessors use the 2-kilobyte dual-ported RAM to exchange data and commands. The RAM is configured into a series of 32 64-byte pages called interprocessor communication buffers. Each buffer provides 62 bytes of storage for commands and data. The first two locations of each buffer are reserved for the diagnostic ROM address register and the RAM page address register. These two locations can only be accessed by the firmware contained in the program ROM.

The RAM address and data lines are tied directly to the TMS address and data bus (AD0–AD7). The high order address lines (A8–A12) are tied to the RAM page register and the 8K diagnostic ROM. The RAM is enabled by the signal RAM, which is generated by the I/O address decoder in the 8031 microprocessor subsystem (Figure 1-5). Reads from and writes to the RAM are enabled by the RD and WR signals generated by the CTI Bus interface on the 8031 microprocessor subsystem (Figure 1-5).

8K Diagnostic ROM
The diagnostic ROM contains the TMS power-up self-test program for the TMS. The address bus for the diagnostic ROM is tied directly to the diagnostic ROM address register. The diagnostic ROM outputs its data onto the TMS address and data bus when the diagnostic ROM address register chip select (RCH) and chip select (ROM) signals are asserted.

Memory Address Register
The memory address register is implemented by two components on the memory subsystem: the diagnostic ROM address register and the RAM page address register. Each of these registers is a programmable array logic (PAL) circuit. The diagnostic ROM address register provides 13-bit addressing for the diagnostic ROM. The RAM page address register provides 6-bit page addressing for the dual-ported RAM.

The diagnostic ROM address register is implemented as a lowest significant bit (LSB) counter. The low order address lines (A0–A7) are implemented by the LSB counter to address the diagnostic ROM. The counter is clocked by RCH, which is generated by the I/O address decoder in the 8031 microprocessor subsystem.

The RAM page address register is implemented as a most significant bit (MSB) counter. The upper six bits of the counter are implemented as a 5-bit synchronous counter plus a 1-bit latch. The upper five bits of the MSB counter are used to address the 8-kilobyte diagnostic ROM. These bits are used as a page pointer to allow the CTI Bus to gain access to the dual-ported RAM through the CTI address latch and CTI data bus buffer.

NOTE
For detailed information on the logical mapping of the memory subsystem, refer to the Telephone Management System Programmer's Manual (AA-AD34A-TH) in the developer's tool kit.

1.3.1.4 I/O Processing Subsystem – The I/O processing subsystem (Figure 1-11) consists of the following two components.

Two 8255A I/O processors

One 8251A universal synchronous asynchronous receiver/transmitter (USART)

NOTE

For detailed information on the Intel 8255A I/O processor and 8251A USART, refer to the Intel Peripheral Design Handbook (available from Intel Corporation).

8255A I/O Processors

One 8255A I/O processor is controls the 212A modem. The other 8255A controls the DTMF circuitry and the telephone line interface module. This manual refers to the I/O processor that controls the DTMF circuitry and TLI module as I/O processor A. This manual refers to the other I/O processor, which controls the 212A modem, as I/O processor B (Figure 1-5).

I/O Processor A – I/O processor A controls the DTMF circuitry and the TLI module. Eight bits of parallel I/O are assigned to the TLI module. Thirteen bits of parallel I/O are assigned to the DTMF circuitry. Port A is eight inputs that read a 3-bit status from the TLI module and the DTMF receive data and data ready strobes.

Port B is eight inputs to the DTMF transmitter row and column keyboard inputs.

Port C is eight outputs. The lower five outputs are used to control the TLI module relays. The PC5, PC6, and PC7 ports of I/O processor A are not currently used.

I/O Processor B – I/O processor B controls the 7910 and 212A modem circuits. Port A is eight outputs to the 7910 modem. Outputs PA0 through PA4 select the modem operating or testing mode. Output PA5 sends a ring indication that informs the modem of an incoming call. Outputs PA6 and PA7 send a request to send signal to the modem.

Port B is eight outputs assigned to the 212A modem. Ports B0 through B3 control the 212A operating mode. Ports B4 through B7 control the 212A testing mode.

Port C is eight inputs from both modem circuits. Ports C0 through C3 read the 212A modem status. Ports C4 through C7 read the 7910 modem status.

NOTE

The 7910 modem is not used for the United States version of the TMS controller. The 7910 modem is intended for all markets outside the United States.

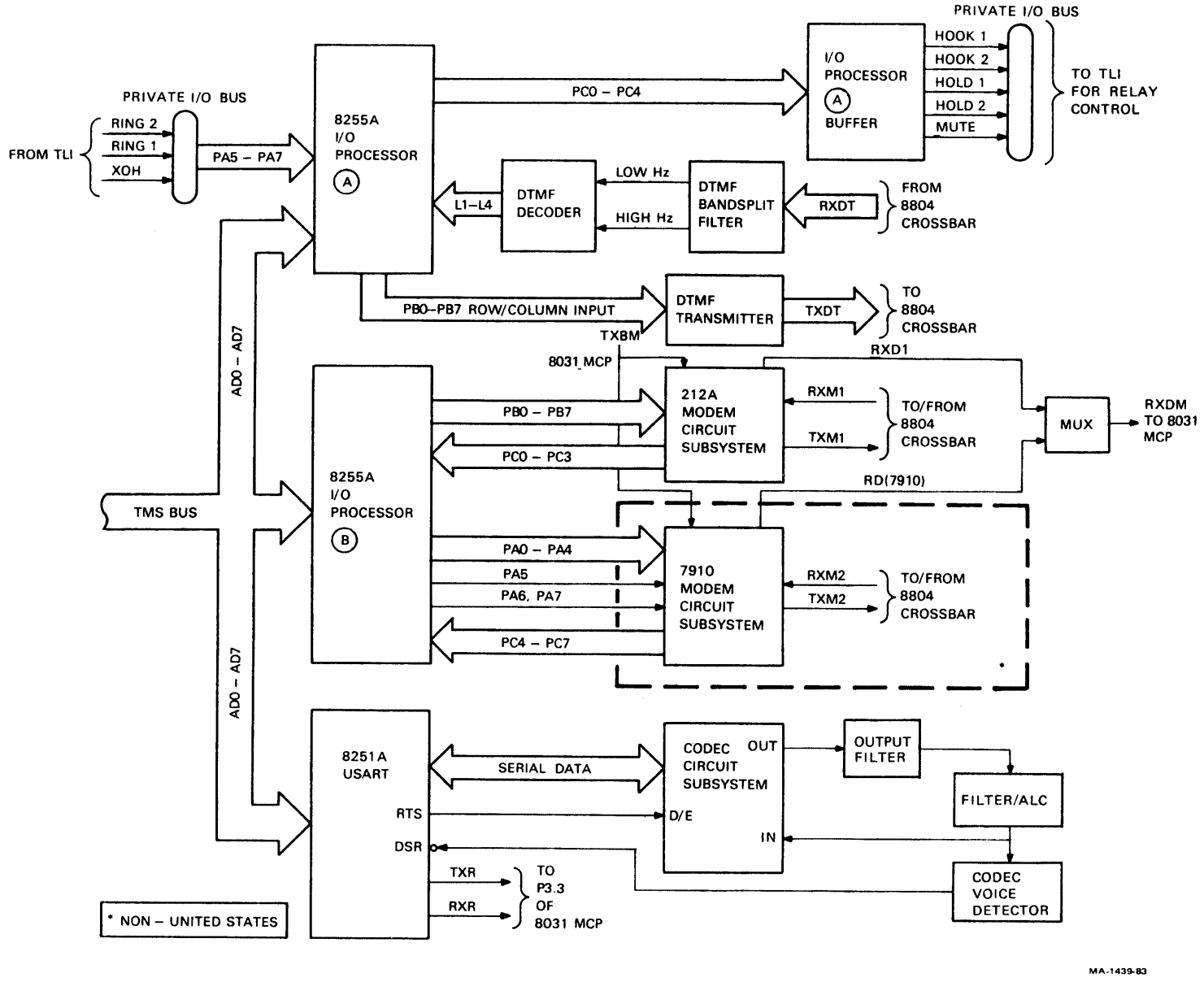


Figure 1-11 I/O Processing Subsystem

8251A USART
The 8251A USART controls the operation of the coder/decoder (CODEC) voice communication circuit. The USART is set to monitor continuously for voice detection. It is set to synchronous mode to receive and transmit a serial data stream at 32K bits per second.

The two status bits, receive ready (RXR) and transmit ready (TXR), are tied through a buffer to the 8031 microprocessor subsystem. RXR tells the 8031 that the USART is ready to receive another character. TXR tells the 8031 that the USART is ready to transmit another character.

The request to send (RTS) output is tied directly to the decode/encode (D/E) input on the CODEC. When RTS is asserted, it places the CODEC in either an encode mode or a decode mode. In encode mode, voice is converted from analog to digital format for storage on the hard disk; in decode mode, digital format voice is converted to analog for transmission.

The data set ready (DSR) input is tied to the CODEC voice detect (CVD) circuit. When it exceeds a threshhold voltage level, CVD goes high, which indicates that voice is present. Under the threshhold voltage level, CVD is low, which indicates that silence is present (no voice). In either case, CVD sets DSR to indicate that silence is present for compression when storing voice messages on the RD hard disk.

1.3.1.5 Communications Subsystem – The communications subsystem consists of the following three components.

Coder/decoder (CODEC) circuit subsystem
Dual-tone multifrequency (DTMF) circuit subsystem
212A modulator/demodulator (modem) circuit subsystem

CODEC Circuit Subsystem
The CODEC circuit subsystem consists of the following five components (Figure 1-12).

CODEC integrated circuit
Voice detection circuit
Automatic level control circuit
CODEC filter circuits
Timing circuit

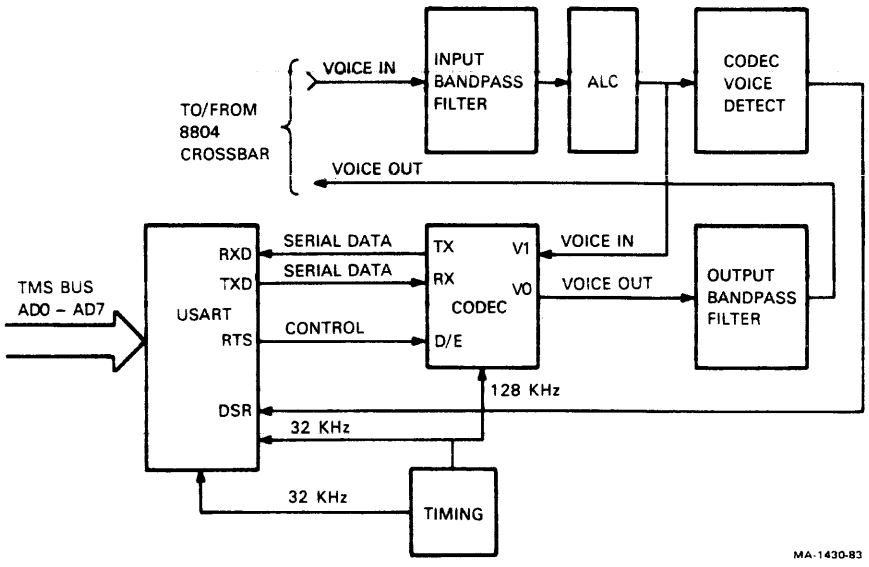


Figure 1-12 CODEC Circuit Subsystem

CODEC Integrated Circuit – A CODEC integrated circuit (IC) encodes and decodes voice to and from a 32K bits per second serial data stream for storage to hard disk, or transmission over the public telephone network. The CODEC IC exchanges commands and data with the 8031 microprocessor subsystem through a dedicated USART communication interface. The CODEC uses a continuously variable slope delta (CVSD) modulated scheme to accomplish voice encoding and decoding. The CODEC works as follows.

When the CODEC circuit is encoding voice to a 32K bits per second stream, the voice input comes in to the CODEC from the crossbar through an input filter and also to an automatic level control (ALC) circuit. The ALC compresses the dynamic range of the voice input, which is then sent simultaneously to the CODEC voice input (V1) and a CODEC voice detection (CVD) circuit. The CVD output is sent to the data set ready (DSR) input of the USART. The firmware samples the DSR bit to determine whether silence or voice is present. A status flag is posted to the 8031 microprocessor to indicate that a silence passage is present.

The voice input (V1) creates a feedback loop. V1 is then fed to a comparator in the CODEC IC along with voice output V0. The comparator senses whether the input is greater or less than the feedback signal. The comparator output goes through an analog to digital conversion, and then is integrated and fed back to the comparator. The integration produces a digital approximation of the analog input. The output is sent to the USART as a 32K bits per second serial data stream from the CODEC circuit output (TX).

When the CODEC is decoding voice from a 32K bits per second stream to analog, the transmit serial data (TXD) output from the USART is sent to the CODEC circuit input (RX). The serial data stream goes through the same internal comparator feedback loop, but in decode mode. The data stream is converted internally from digital to analog. The analog data stream is then output from V0 to an output bandpass filter, and from there is fed directly to the crossbar switching circuit.

Voice Detection Circuit – The voice detection circuit makes the best use of the allotted hard disk space by detecting periods of voice and separating them from the periods of silence.

The first stage of voice detection involves a voice energy level detector. The detector compares voice energy to a present threshold. If this threshold is exceeded, the signal is accepted as valid voice present. The next stage of voice detection involves an envelope detector. The envelope detector presents a digital representation of the total analog voice energy. If voice energy is not above the current threshold levels, that information is sent to the 8031 microcomputer via the DSR input of the 8251 USART. The firmware compresses periods of silence out of the voice data.

CODEC Filter Circuits – Two filters are used for noise rejection in the CODEC voice circuit: an input and output bandpass filter. Both filters are 5-pole elliptic low pass filters with a bandwidth of 100 Hz to 3700 Hz.

Dual-Tone Multifrequency (DTMF) Circuit Subsystem

The dual-tone multifrequency (DTMF) circuit subsystem is used for tone dialing and DTMF data communications. The DTMF is made up of a DTMF transmitter and a DTMF receiver (Figure 1-13).

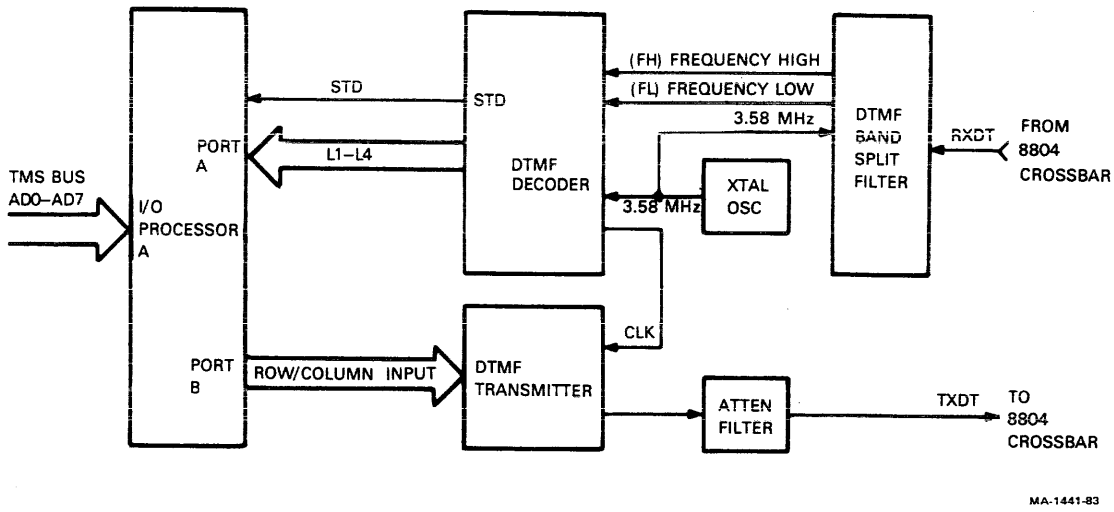


Figure 1-13 DTMF Circuit Subsystem

DTMF Transmitter – The DTMF transmitter performs tone dialing and data communications by accepting four row inputs and four column inputs from the Voice Unit 8051 microcomputer to select a tone pair. One of the four row inputs selects the corresponding row tone. One of the four column inputs selects the corresponding column tone.

Each row and column input to the transmitter is connected to port B of I/O processor A. DTMF tone pairs are turned on when the 8051 asserts one row input and one column input for the I/O processor to the DTMF transmitter. Single-column tones are selected when one column input only is asserted. Single-row tones are selected when any two or more column inputs and one row input are asserted.

The DTMF transmitter uses a color burst frequency (3.58 MHz) as a clock from the DTMF decoder. The clock signal is divided by the transmitter to synthesize the input row and column frequencies for transmission.

Table 1-1 lists the tone pair transmit/receive data patterns and their corresponding tone frequencies and keys. TX stands for the transmitted data from the transmitter. RX stands for the column and row inputs to the transmitter. The letter C stands for column and the letter R stands for row (for example, C1,R1 means column 1, row 1).

Table 1-2 lists the transmitter generated single tones and their tone frequencies.

Table 1-1 DTMF Transmit Receive Tone Pairs

Key	Transmit (TX) Data	Receive (RX) Data	Tone Frequencies
1	EE 1	C1,R1	C=1209/R=697
2	DE 2	C2,R1	C=1336/R=697
3	BE 3	C3,R1	C=1447/R=697
4	ED 4	C1,R2	C=1209/R=770
5	DD 5	C2,R2	C=1336/R=770
6	BD 6	C3,R2	C=1447/R=770
7	EB 7	C1,R3	C=1209/R=852
8	DB 8	C2,R3	C=1336/R=852
9	BB 9	C3,R3	C=1447/R=852
0	D7 A	C2,R4	C=1336/R=941
*	E7 B	C1,R4	C=1209/R=941
#	B7 C	C3,R4	C=1477/R=941
A	7E D	C4,R1	C=1633/R=697
B	7D E	C4,R2	C=1633/R=770
C	7B F	C4,R3	C=1633/R=852
D	77 0	C4,R4	C=1633/R=941

Table 1-2 DTMF Single Transmit Tones

Row/Column	Transmit (TX) Data	Tone Frequencies
R1	3E	697
R2	3D	770
R3	3B	852
R4	37	941
C1	EF	1209
C2	DF	1336
C3	BF	1477
C4	7F	1633

DTMF Receiver – The DTMF receiver consists of a DTMF decoder and a bandsplit filter.

The received data input (RXDT) is coupled to the DTMF bandsplit filter. The filter separates the RXDT input into two outputs: frequency high (FH) and frequency low (FL). The FH and FL filter outputs are tied to the corresponding inputs on the DTMF decoder. A logic high to the decoder causes the decoder to latch the FH and FL inputs from the filter to decoder outputs L1 through L4. When the decoder valid data strobe (STD) is asserted to the I/O processor, outputs L1 through L4 are latched to port A of the I/O processor.

The DTMF receiver uses a color burst frequency (3.58 MHz) generated by a crystal oscillator as a clock.

212A Modem Circuit Subsystem

The 212A modem performs both low-speed and high-speed data communications. It exchanges data and commands with the 8031 microprocessor subsystem through I/O processor B. Figure 1-4 shows the logical placement of the 212A modem circuit subsystem.

NOTE

The AM7910 modem is reserved for all markets outside the United States and is not discussed in this document.

The 212A modem circuit subsystem consists of the following six circuit groups (Figure 1-14).

212A modem chip set
Modem filter circuit
Carrier circuit
Carrier detector circuit
FSK demodulator
Modem timing circuit

The following section describes the 212A modem circuit subsystem as it applies to the telephone management system.

NOTE

Detailed descriptions of the modem chip internal circuits are proprietary information to Western Electric Company and are not presented in this manual.

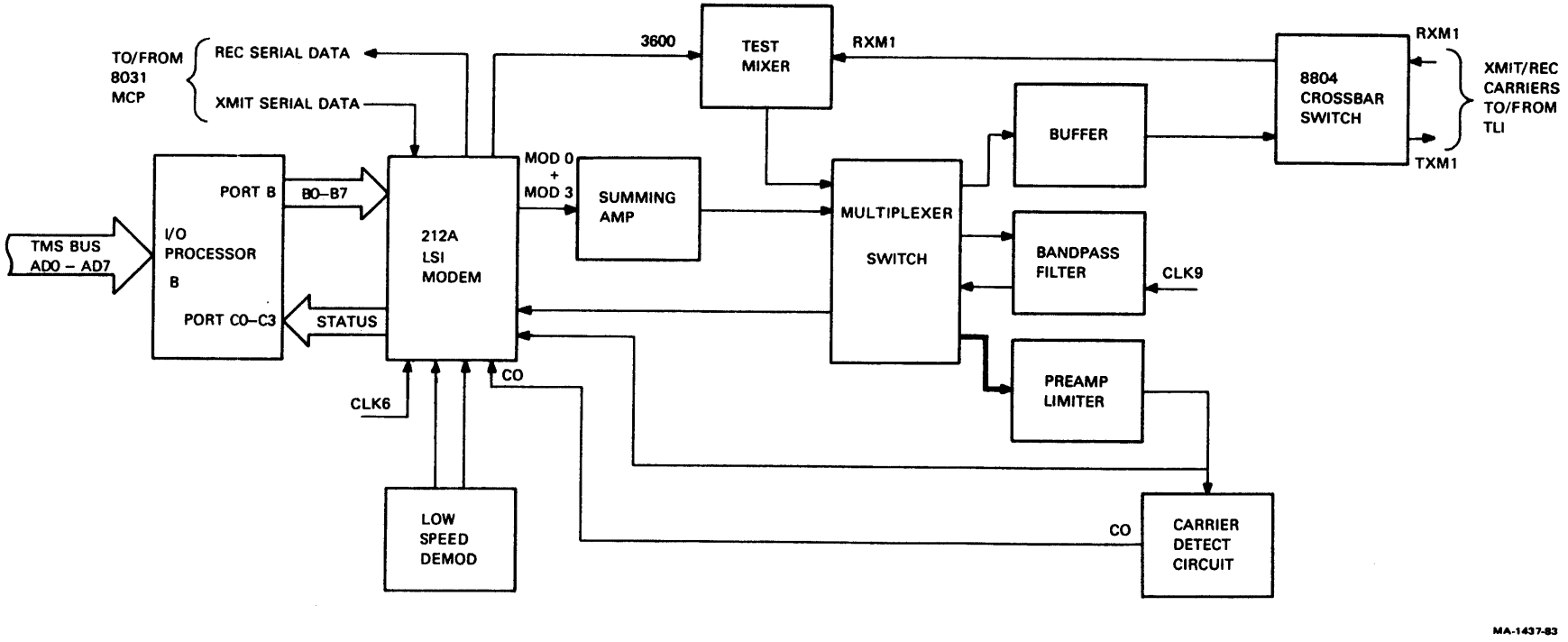


Figure 1-14 212A Modem Circuit Subsystem

212A Modem Chip Set – The primary modem circuits are contained in the 212A modem chip set. They are labeled as S2723 and S2759 on sheet 5 of 6 in the *DTC11-A Field Maintenance Print Set*. The S2723 contains the line control logic and the low-speed modem logic (frequency shift keying). The S2759 contains the high-speed modem logic (differential phase shift keying).

NOTE
For this discussion, the block diagram shows the modem chip set as a single functional unit.

The S2723 is compatible with the AT&T 103 modem. It uses frequency shift keying (FSK) and has the following 11 functions.

Low-speed transmitter
Part of low-speed demodulator
Line control logic
Automatic and manual speed selection
All low-speed test logic
Loss of carrier disconnect option
Receive space disconnect option
Send space disconnect option
Automatic answer option
High- and low-speed handshake sequence logic
Abort function timer

The S2759 is compatible with the AT&T 212A modem. It uses differential phase shift keying (DPSK) and has the following eight functions.

High-speed transmitter
High-speed demodulator
Transmitter phase-locked loop
Receiver timing recovery
All high-speed test logic
Asynchronous start/stop code option
Character length option
Respond to digital loop option

Modem Filter Circuit – The 212A modem chip set uses full-duplex mode for data communication. For each modem integrated circuit, the originating modem transmits in a passband at 1200 Hz. The answering modem transmits in a passband at 2400 Hz. A filter is needed to confine the bandwidth of the transmit carrier and to reject interference from the receive carrier.

In originate mode, the low-band filter is placed in the transmit carrier path, and the high-band filter is placed in the receive carrier path. In answer mode, the filters are swapped. A multiplexer is used as the switch (shown as the multiplexer switch block in Figure 1-14).

Carrier Circuit – The low-speed modem chip generates a square wave FSK modulated carrier. The high-speed modem chip generates a 3-bit sine wave approximation. These four signals are summed and buffered by a summing amplifier. The resulting transmit carrier (TXM1) is then sent to the appropriate filter. The filter output is sent to the multiplexer switch, and from there is driven by a buffer to the 8804 crossbar.

The receive carrier (RXM1) signal from the crossbar is first routed into the test mixer. The test mixer inverts RXM1, driving it into the multiplexing switch and to the appropriate filter.

In analog loopback mode, the high-speed S2759 modem toggles at 3600 Hz in high-speed mode or 3295 Hz in low-speed mode. This causes the internal comparator to mix RXM1 with the test clock frequency. The test clock and RXM1 heterodyne the looped-back transmit carrier (TXM1) into the opposite band so that it can be demodulated. Table 1-3 shows test signal generation.

The modem chip set cannot handle analog signals directly. A 2-part limiter circuit is needed to extract zero crossings from the receive carrier for demodulation by the 212A modem. This is shown as the preamplifier limiter in Figure 1-14.

The first part of the limiter circuit is a variable gain amplifier. At low input signal levels, feedback diodes are off. In this case, resistors form a 2-part divider network; the gain is about +45 dB. At high signal levels, feedback diodes are on. In this case, the feedback resistors are bypassed, which leaves a single divider. The purpose of this nonlinear gain characteristic is to compress the dynamic range of the received carrier from 40 dB to about 10 dB. This ensures that the second limiter stage gets a clean signal for zero crossing detection.

The second part of the limiter is a comparator. The comparator output is shifted from a −5 V to +5 V swing to a ground to +5 V swing.

Carrier Detector Circuit – The receive carrier detector has three parts. The first part is a level detector, with the threshold set by a voltage divider. The second part is a low pass filter. The third part is a fast attack slow decay timing circuit, where the signal is inverted for the required polarity.

Table 1-3 212A Modem Test Signal Generation

Mode	TXM1 Test Clocks		Clock Sum	Clock Difference
212 originate	1200	3600	4800	2400
212 answer	2400	3600	6000	1200
103 originate	1070	3295	4365	2225
103 originate	1270	3295	4565	2025
103 answer	2025	3295	5320	1270
103 answer	2225	3295	5520	1070

Note: All measurements are in hertz (Hz).

FSK Demodulator – The FSK demodulator has three parts. The first part is internal to the low-speed modem. The other parts are external.

The first part is an autocorrelator circuit. It converts the LIM input into a pulse train. The frequency is preserved, but the pulse width is constant and equal to the half cycle of the demodulation frequency (1170 Hz or 2125 Hz). The result is that the duty cycle of the SLIM output is more than 50 percent for frequencies over the demodulation carrier and less than 50 percent for frequencies below it.

The two external parts comprise a duty cycle detector.

The second part is a 4-pole low pass filter with a break frequency of about 260 Hz.

The third part is a comparator. Its output is level shifted to TTL voltage levels.

Modem Circuit Timing – The high-speed modem needs two clock frequencies. Both of them are harmonically related to the low-speed modem clocks. CLK6 (1.2288 MHz) drives both low- and high-speed modem ICs. CLK9 (153.6 kHz) drives the bandpass filters.

RS232 Correspondence – The 212A modem chip set was designed for use in an 212A standalone modem. On the TMS controller module, the corresponding IC pins are connected to parallel and serial ports in the 8031 microprocessor subsystem. Tables 1-4 through 1-7 list the IC pins.

Table 1-4 RS232 Connector Signals

Pin	EIA	RS232	Name	TMS Controller Connection
37	BA	2	TXD	8031 hardware UART, E12-11
40	BB	3	RXD	8031 hardware UART, E12-10
20	CB	5	CTS	Sensed by port E2.3
29	CC	6	DSR	Not connected
39	CD	20	DTR	Asserted through E42-4
21	CE	22	RING	Driven by port E1.2
8	CF	8	DCD	Not connected
5	CH	23	HSS	Driven by port E1.0
9	CI	12	HSI	Sensed by port E2.1
37	DA	24	TSET	Not connected
35	DB	15	TSET	Not connected
28	DD	17	RSET	Not connected

Table 1-5 AT&T 212A Modem Switch Controls

Pin	Function	8031 Microprocessor Connection
20	Talk/data	Driven by port E1.3
5	High speed	Driven by port E1.0
15	Digital loopback	Driven by port E1.6
34	Remote digital	Driven by port E1.5
32	Self-test	Test point on PCB; function implemented in firmware
25	Analog loopback	Driven by port E1.4

Table 1-6 AT&T 212A Modem Indicators

Pin	Function	8031 Microprocessor Connection
8	Null	Not connected
39	Data terminal ready	Assumed by TMS processor
29	Data set ready	Ignored by TMS processor
20	Clear to send	Sensed by port E2.3
9	High speed	Sensed by port E2.2

Table 1-7 AT&T 212A Modem Option Jumpers

Pin	Function	8031 Microprocessor Connection
33	Asynchronous/synchronous	Set to asynchronous
22	Character length	Strapped for 10 bits on pin 1
16	Digital loopback enable	Driven by port E1.7
36	Loss of carrier	Strapped enabled on pin 2
33	Send space disconnect	Strapped enabled on pin 3
28	Auto answer enable	Enabled
24	Digital loop indicate	Sensed by port E2.2
23	Mode (answer/originate)	Sensed by port E2.0

1.3.1.6 Crossbar Switching Circuit – The TMS controller uses an 8 × 8 crossbar signal switch (Figure 1-15) that connects the subsystems to each other and to the public telephone network. The 8 × 8 crossbar signal switch is implemented by using two 8 × 4 crossbar signal switches. Because the firmware recognizes the two switches as one unit, the functional diagram shows the two switches as one switch divided in two.

Each crosspoint switch within the crossbar either suppresses or transmits data between the subsystems being connected. The state of each crosspoint is controlled by 64 internal control latches (32 per crossbar) arranged in an 8 × 8 array that corresponds to the crossbar switch matrix. A logical high in a latch enables the corresponding crosspoint switch. A logical low disables the corresponding crosspoint switch.

When address enable (AE) is asserted, data is written from data lines D0 through D7 into the control latches selected by address lines A0 through A2.

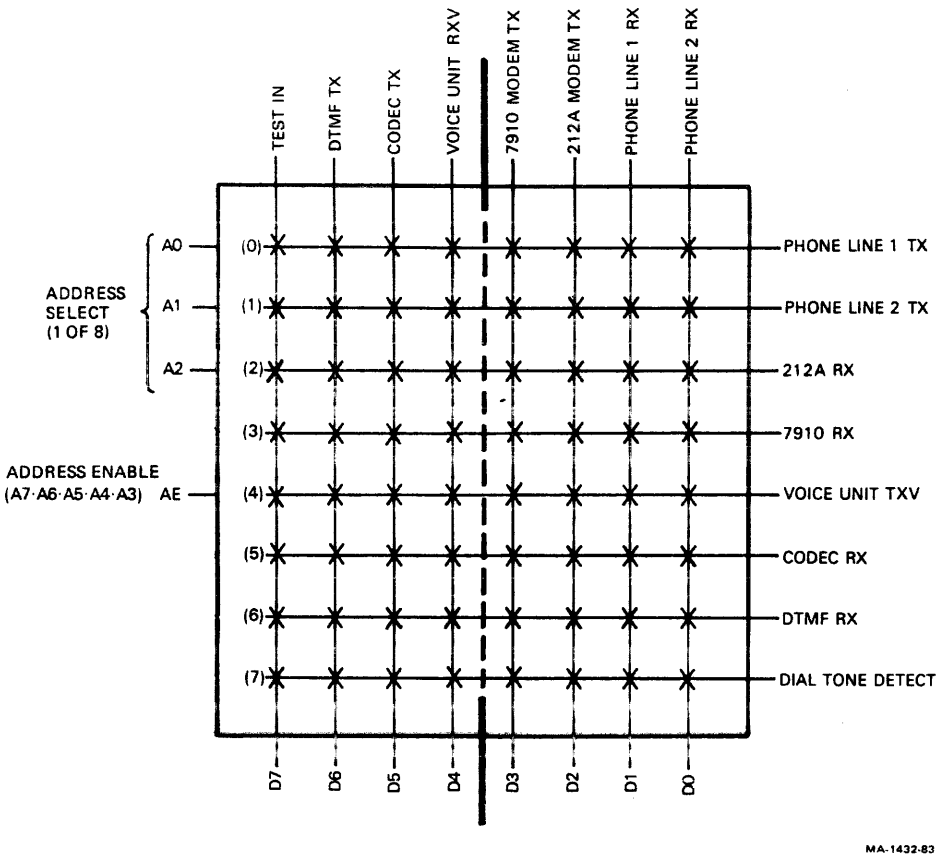


Figure 1-15 Crossbar Signal Switch Functional Diagram

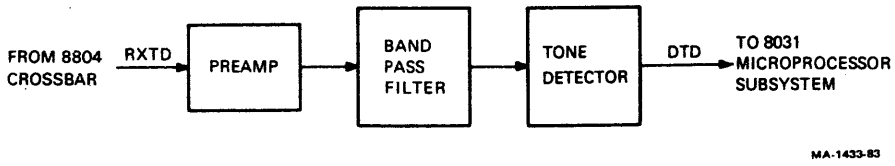


Figure 1-16 Call Progress Tone Detector Functional Diagram

1.3.1.7 Call Progress Tone Detector – The call progress tone detector helps automatic call placement by detecting call progress tones. The call progress tone detector consists of the following three components (Figure 1-16).

Preamplifier
Bandpass filter
Tone detector

The received signal to tone detector (RXTD) enters from the crossbar to a preamplifier. The preamplifier drives that signal through to a bandpass filter. The bandpass filter is designed to pass the following three signal frequencies.

Dial tone at 350 Hz and 440 Hz
Audible ringback at 440 Hz and 480 Hz
Busy signals at 480 Hz and 620 Hz

RXTD is driven to the tone detector. The tone detector drives RXTD as a logical high dial tone detect (DTD) to port 3.2 of the 8031 microprocessor.

1.3.1.8 TLI/Voice Unit Interface Circuit – The TMS controller communicates with the TLI and the voice unit by using a TLI/voice unit interface circuit. The TLI/voice unit interface circuit consists of the public I/O bus (Figure 1-5) and associated interface relay and coupling circuits. The public I/O bus is a 16-wire interface connection from J1 (the public I/O bus is a separated segment of J1 on the TMS controller) to the remote access connector J8 on back of the system module. (Refer to Table 5-31 in the *Professional 300 Series Technical Manual Volume 1*, (EK-PC300-V1.)

Tables 1-8 through 1-11 describe the signals that are routed through the TLI/voice unit interface circuit.

Table 1-8 TLI Relay Control Signals

Name	Bus Pin	RAM I/O Port	Function
HOOK1	J1-61	EA.0	Telephone line 1 hook relay
HOOK2	J1-62	EA.1	Telephone line 2 hook relay
HOLD1	J1-63	EA.2	Telephone line 1 hold relay
HOLD2	J1-64	EA.3	Telephone line 2 hold relay
MUTE	J1-65	EA.4	External telephone mute relay

Table 1-9 Status Indicator Signals

Name	Bus Pin	RAM I/O Port	Function
XOH	J1-66	E8.5	External telephone off-hook indicator
RING1	J1-67	E8.6	Telephone line 1 ring-in indicator
RING2	J1-68	E8.7	Telephone line 2 ring-in indicator

Table 1-10 TLI Analog Control Signals

Name	Bus Pin	RAM I/O Port	Function
TXP1	J1-69	F8.x	Transmits data to telephone line 1.
RXP1	J1-70	Fx.0	Receives data from telephone line 1.
TXP2	J1-71	F9.x	Transmits data to telephone line 2.
RXP2	J1-72	Fx.1	Receives data from telephone line 2.
TXV	J1-73	FC.x	Transmits data to voice unit.
RX	J1-74	Fx.4	Receives data from voice unit.

Table 1-11 Voice Unit Control Signals

Name	Bus Pin	8031 Port	Function
TXDV	J1-75	P1.3	Transmits data to voice unit.
RXDV	J1-76	P1.2	Receives data from voice unit.

1.3.2 Telephone Line Interface (TLI) Module

The TLI module is a collection of interface circuits between the public telephone network, the voice unit, and the TMS controller module. The TLI contains the following five circuits (Figure 1-17).

Relay circuits
Line coupler circuits
Ring-in detector circuit
Off-hook detector circuit
Voice unit interface

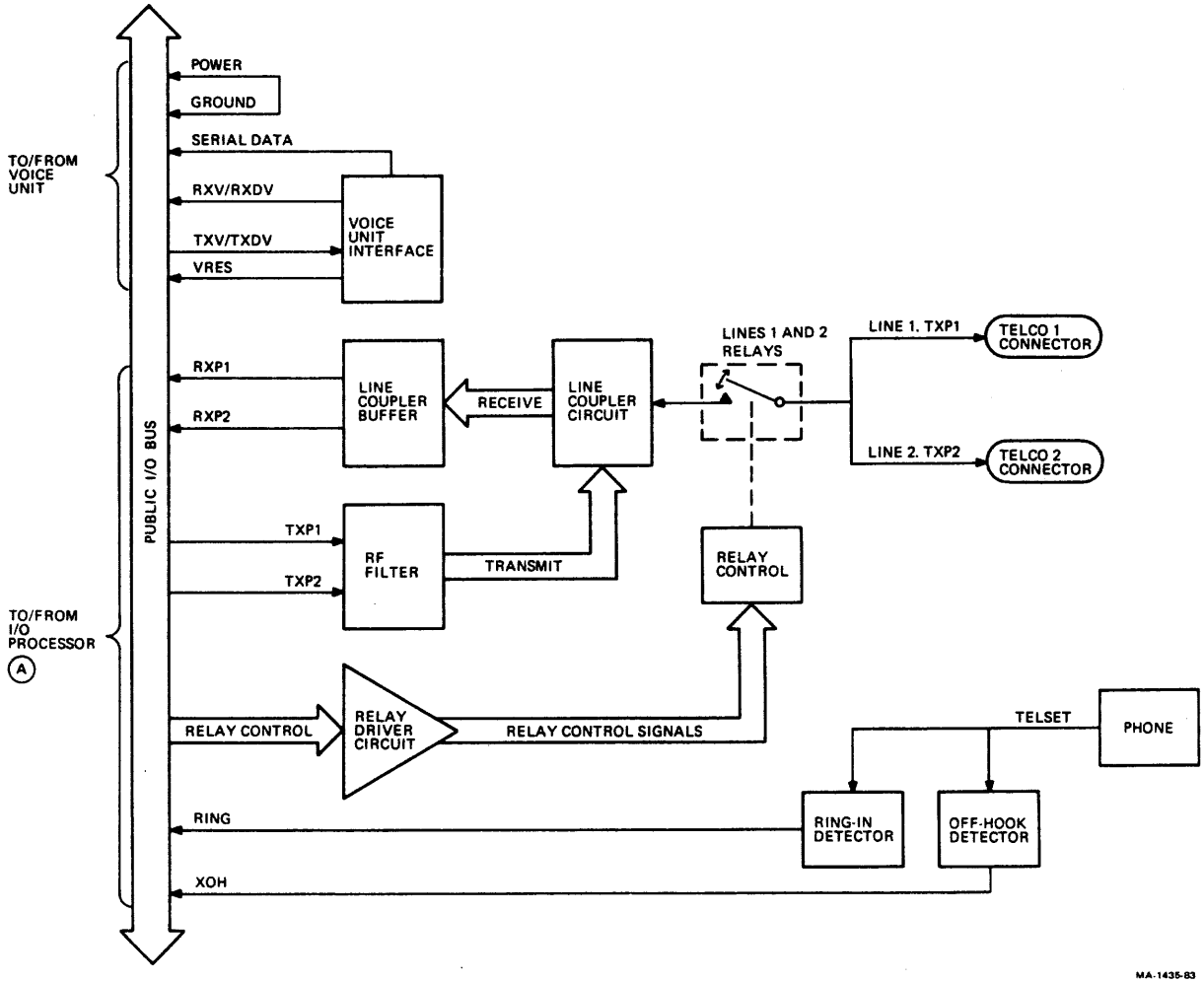


Figure 1-17 TLI Module Functional Diagram

1.3.2.1 Relay Circuits – The TLI has five relays. Each external telephone line (Telco) has a hook relay to control access to the TIP and RING signals. Each Telco line also has a hold relay for optional control over the A and A1 leads in multibutton systems. A mute relay can open the connection from Telco line 1 to the external telephone set.

Each relay circuit consists of the following three components.

Line receiver from I/O bus, with pull up
Relay driver
Single-pole double-throw (SPDT) relay

Each relay has one dedicated line on the public I/O bus. Relay controls can be driven push/pull or at open collector TTL levels. Relay control lines are asserted low.

Table 1-12 describes the relay control signals and their functions.

1.3.2.2 Line Coupler Circuits – Each Telco line has a line coupler circuit that consists of a transformer-based signal coupler hybrid and an IC buffer. The transformer provides dc isolation. It drives transmitted signals out and senses received signals coming in.

The line coupler circuit has two parts: a telephone line coupling transformer and a duplexing circuit. The coupling transformer provides 1700 Vdc isolation between the telephone line and the CTI processor. The transformer provides ac coupling between the Telco line and the duplexer circuit.

The duplexer has two parts: a line receiver and a differential amplifier. Transmitted analog signals from the I/O bus are ac-coupled to the line coupler. An amplifier buffers this signal into the coupling transformer.

The second amplifier senses and amplifies the incoming receive signal, and nulls out the transmitted signal.

The duplexer stage is configured as a noninverting amplifier in the receive direction. The original Telco signal is divided by the line impedance and a resistor, and sent to the line coupler.

The duplexer is configured as an inverting differential amplifier in the transmit direction. If the Telco line signal matches the voltage drop at the resistor, the transmitted signal will be nulled out.

Table 1-12 Telephone Line Interface Relay Control Signals

Signal	Function
HOOK1	Connects TMS to line 1.
HOOK2	Connects TMS to line 2.
HOLD1	Puts line 1 in a temporary hold state.
HOLD2	Puts line 2 in a temporary hold state.
MUTE	Temporarily disables the telephone set.

1.3.2.3 Ring-In Detector Circuit – Each telephone line out has a circuit to detect ring-in signaling from the telephone network. Its output is driven onto the public I/O bus. The ring-in detector circuit provides isolation, rejects dc, and rejects low level communications and voice signals.

1.3.2.4 Telset Off-Hook Detector Circuit – The TLI features a daisy chain connection from Telco line 1 to the telephone set. This circuit is controlled by the mute relay. An optocoupler circuit is placed in series with the telephone TIP signal lead to sense the off-hook (XOH) current. The current is inverted, buffered, and driven onto the public I/O bus.

1.3.2.5 Voice Unit Interface – The voice unit is connected to the CTI processor through the TLI. Power, voice signals, and serial data pass straight through the TLI. An additional circuit generates a reset to the voice unit based on a long space sent from the public I/O bus.

Table 1-13 describes the voice unit interface signals.

1.3.3 Voice Unit

The voice unit is an intelligent desktop terminal. It is used for voice file manipulation and telephone dialing over the public switched telephone network. It contains a 21-position keypad for voice file manipulation and a dedicated key array for telephone dialing. Figure 1-18 shows the DTC11-B voice unit.

Table 1-13 Voice Unit Interface Signals

Signal Name	Description
TXV	Transmits voice to voice unit speaker.
RXV	Receives voice from voice unit microphone.
RXDV	Receives serial data from voice unit.
VRES	Resets to voice unit 8051 microcomputer.

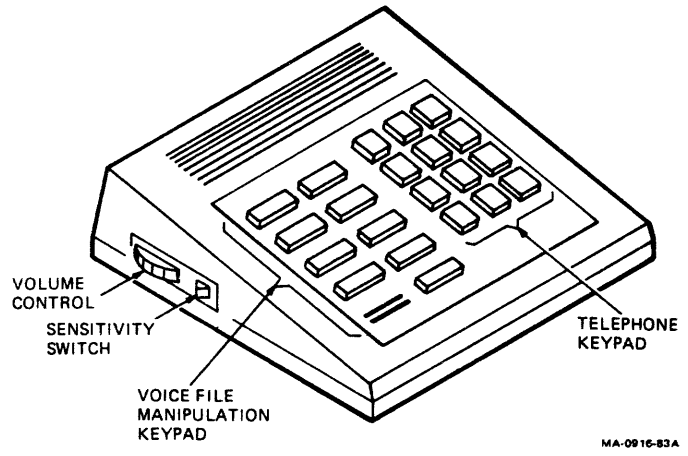


Figure 1-18 DTC11-B Voice Unit

1.3.3.1 System Overview – This paragraph is a functional description of the voice unit. Refer to Figure 1-19 while you read this description.

Data Paths
A full-duplex line (TXD/RXD) is used to exchange serial data between the CTI processor and the voice unit 8051 microcomputer. The CTI processor sends commands to control LED displays and to manipulate the analog voice circuits. The 8051 voice unit microcomputer controls and scans the keyboard, and reports key closures and status information to the CTI processor.

The 8051 microcomputer supervises all keypad activity and transmits key depression (closure) information to the TMS controller. The TMS firmware interprets this information and responds accordingly, subject to the software-defined operating system. The TMS controller then sends commands back to the 8051 microcomputer for setup and establishes the voice unit operating mode.

Operating Modes
The voice unit operates in three modes: Play, Telco, and Record.

1. In Play mode, the speaker control circuit is enabled. This allows stored audio on hard disk to be played back.

2. In Telco mode, the voice unit functions as a speaker phone for bidirectional communications between two users over the telephone lines.

3. In Record mode, the microphone control circuit is enabled. This allows audio messages to be encoded and stored onto hard disk.

Supplied Voltage
The Professional computer system supplies +12 V to power the voice unit. A local voltage regulator derives a +5 V supply from the +12 V supplied to the voice unit. The +5 V rail provides power to the voice unit microcomputer.

System Interface
The voice unit is connected to the Professional computer system through a 7-conductor shielded cable. The cable plugs directly into the DIN connector on the TLI.

The cable carries +12 V to power the voice unit. The remaining conductors connect the following components: two serial control lines, two analog signal lines, power return (ground), reset, and the cable shield.

Voice Unit Controls
The voice unit has two controls: volume control knob and a sensitivity switch (Figure 1-18).

1. Volume Control Knob – This thumbwheel control provides volume adjustment during Play and Telco modes. It is a miniature 10K audio-taper type. The volume control knob is on the left side of the voice unit. Clockwise rotation increases the volume.

2. Sensitivity Switch – A sensitivity switch is used to select between two detector sensitivity levels. The maximum sensitivity setting is when the switch is toward the front of the voice unit (Figure 1-18). This setting is used in normally quiet environments (for example, an office). The lower sensitivity setting is used where noise levels are high enough to interfere with the correct operation of the detector and arbitration circuitry.

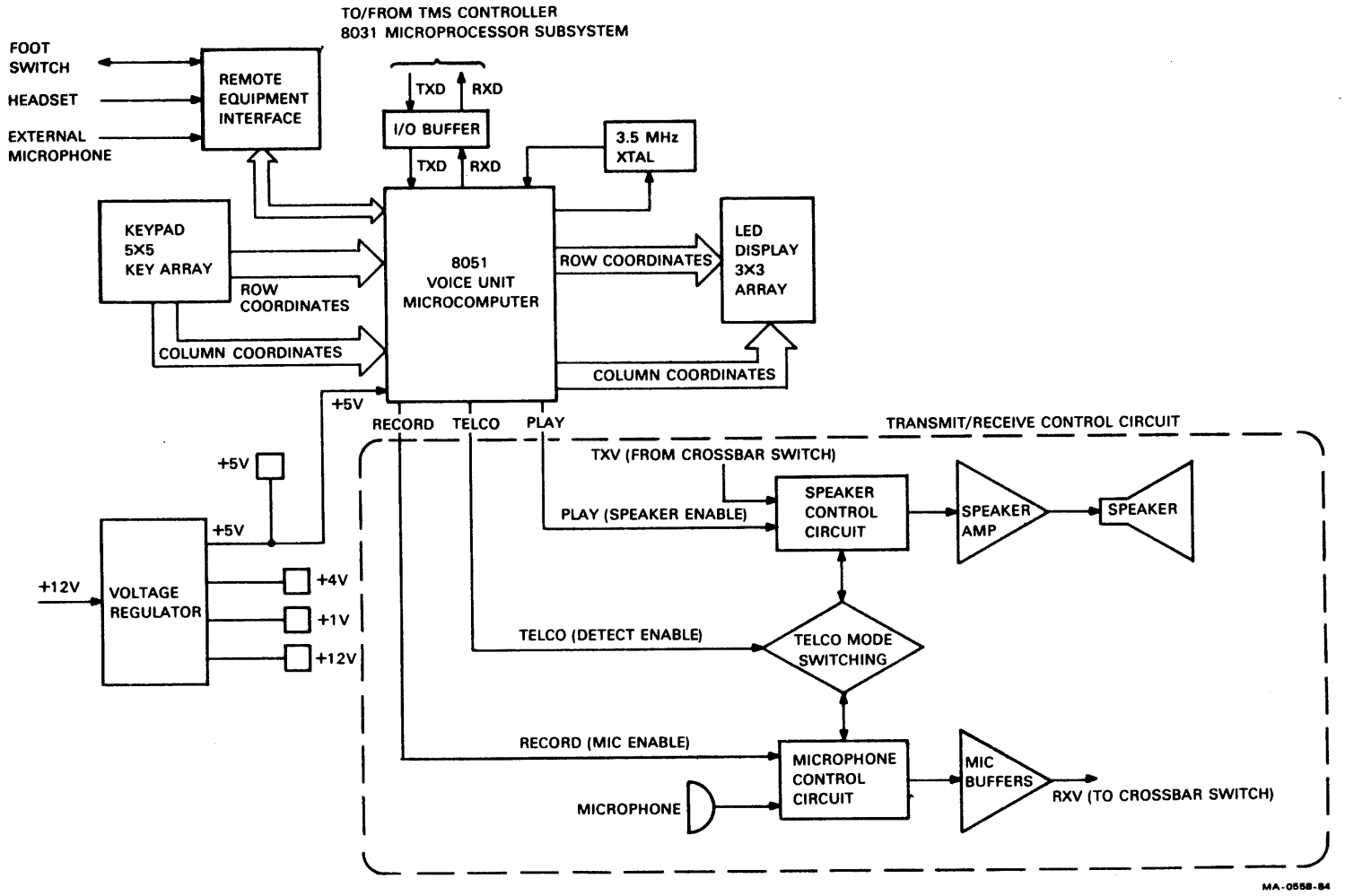


Figure 1-19 Voice Unit Functional Block Diagram

1.3.3.2 Detailed Description – This paragraph is a detailed description of the voice unit. Refer to Figure 1-19 as you read this description.

The voice unit consists of the following six circuits.

8051 microcomputer circuit
Keypad 5 × 5 array
LED display 3 × 3 array
Transmit/receive control circuit
Voltage regulator circuit
Remote equipment interface

Figure 1-19 is a functional block diagram of the voice unit. Refer to this figure as you read this paragraph.

8051 Microcomputer Circuit
The voice unit uses an 8051 microcomputer to perform all voice unit functions. A 3.5 MHz crystal oscillator provides the operating frequency for the 8051 microcomputer.

The 8051 performs the following functions for the voice unit.

1. It monitors the keypad and reports all key closures to the TMS controller via a 110 baud serial communication full-duplex link (TXD/RXD lines).

2. It responds to all commands sent to it from the TMS controller or CTI processor.

3. It operates the LED display 3 × 3 array.

For detailed information about the 8051 microcomputer, refer to any 8051-type microcontroller user's manual.

Keypad 5 × 5 Array
The voice unit keypad is a 5 × 5 array of 21 keys. The 8051 microcomputer monitors the keypad for x, y coordinate key closures. When a key closure is detected, the 8051 transmits the serial data (generated by the key closure) to the TMS controller.

Twelve keys form a dedicated 3 × 4 numeric array for dialing. The remaining nine keys are function keys, eight of which are user definable. The mute key is a dedicated function key and cannot be changed.

The keypad connects to the primary printed circuit board in the voice unit with a 16-conductor ribbon cable and connector. Ten conductors on the connector are used for the 5 × 5 switch array. The remaining six conductors transmit information from the 3 × 3 LED display.

LED Display 3 × 3 Array
An LED display 3 × 3 array displays the current status of each key. Each key has its own LED. The display control logic internal to the 8051 decodes the time-multiplexed LED display information. An inverting driver is used for signal level conversion to power the LED array.

Transmit/Receive Control Circuit
The transmit/receive control circuit consists of a speaker control circuit, a microphone control circuit, and a Telco mode switch. The microphone and speaker control circuits are analog switches (one per circuit) and voltage comparators. These two circuits are controlled by the Play and Record control lines from the 8051 microcomputer. The 8051 uses the control lines to switch states of two voltage comparators corresponding to the analog switch of each control circuit. Each analog switch turns on or off, depending on the selected operating mode. Once a switch is turned on, it is held in an on state by the 8051 until an alternate operating mode is chosen.

The Telco mode switch is a quad 2 to 1 multiplexer used for audio signal routing and control. In Telco mode, it routes the audio signals through an alternate path and enables the control circuit paths.

Voltage Regulator Circuit
The Professional computer system supplies the +12 V that powers the voice unit. The voltage regulator circuit converts +12 V to a regulated +5 V rail to power the voice unit 8051 microcomputer.

The regulator also converts from +12 V to +9.3 V to supply bias and reference voltages to the transmit/receive control circuit and the voltage-controlled amplifier circuits.

Remote Equipment Interface
The remote equipment interface circuit connects the following three optional devices to the voice unit.

External microphone
Headset
Foot switch

The three options connect to three miniature phone jacks on the right side of the voice unit. The connector jacks have tip-shunt switches that are activated when the accessory is plugged in. The headphone and microphone connectors are for 0.140-inch miniature plugs. The remote footswitch uses a 0.101-inch miniature plug.

1.4 CONNECTOR DESCRIPTIONS
The following chart lists the signals on connector J1.

Connector Pin	Signal Name
1	DCOK
2	
3	POK*
4	
5	INIT
6	
7	BDAL15
8	BDAL13
9	BDAL14*
10	BDAL12
11	SPARE 0
12	BDAL11
13	BRPLY
14	BDAL10*
15	

Connector Pin	Signal Name
16	BDAL9*
17	BMDEN*
18	BDAL*
19	WRITE*
20	BDAL7*
21	BWLB*
22	BDAL6*
23	BWLB*
24	BDAL5*
25	BSDEN*
26	BDAL4*
27	
28	BDAL3*
29	SS
30	BDAL2
31	IRQB
32	BDAL1
33	IRQA
34	BDAL 0
35	OPRES
36	
37	BDS
38	
39	BAS
40	
41	SPARE2*
42	SPARE3*
43	BDOS*
44	BDAL21*
45	BPO*
46	BDAL20*
47	BPI*
48	BDAL19*
49	SPARE4*
50	BDAL18*
51	
52	BDAL17*
53	BMER*
54	BDAL16*
55	BDMR*

* Not connected

Connector Pin	Signal Name	
56	BDMG*	
57	BBSY*	
58		
59	BCLK*	
60		
61	PIB1 (HOOK 1)	TLI relay control signals
62	PIB2 (HOOK 2)	
63	PIB3 (HOLD 1)	
64	PIB4 (HOLD 2)	
65	PIB5 (MUTE)	
66	PIB6 (XOH)	TLI status signals
67	PIB7 (RING 1)	
68	PIB8 (RING 2)	
69	PIB9 (TXP1)	TLI analog signals
70	PIB10 (RXP1)	
71	PIB11 (TXP2)	
72	PIB12 (RXP2)	
73	PIB13 (TXV)	Voice unit analog signals
74	PIB14 (RXV)	
75	PIB15 (TXDV)	Voice unit serial data signals
76	PIB16 (RXDV)	
77	NT +*	
78	NT −*	
79	NR +*	
80	NR −*	
81	NC +*	
82	NC −*	
83	RR*	
84	RV*	
85	GR*	
86	GV*	
87	BR*	
88	BV*	
89	MR*	
90	MV*	

* Not connected

1.5 HARDWARE SPECIFICATIONS

The hardware specifications for the TMS controller module and the TLI module are as follows.

Electronics	8031 microprocessor 16-kilobyte ROM, 2-kilobyte RAM Coder/decoder (CODEC) communications subsystem FSK modem subsystem DPSK modem subsystem DTMF communications subsystem
Data rates	
Low-speed mode	0 to 300 bits per second, asynchronous format
High-speed mode	1200 bits per second, character asynchronous format
Operation	
Low-speed mode	Asynchronous, binary, serial
High-speed 212 mode	Character asynchronous format
Operating mode	Full-duplex at all speeds
Line	2-wire switched network
Modem compatibility	
Low-speed mode	103J data sets
High-speed mode	212A data sets
Physical	
TMS controller	30.5 cm × 13.3 cm (12 in × 5-1/4 in)
TLI module	19.1 cm × 13.3 cm × 2.5 cm (7-1/2 in × 5-1/4 in × 1 in)

The hardware specifications for the voice unit are as follows.

Electronics	8051 microcomputer with internal ROM and RAM Low noise microphone preamplifier Local power amplifier Local electret microphone Miniature loudspeaker Volume control Microphone sensitivity control 21-switch keypad
Communications	2-line serial connection to TMS controller
Data rate	120 baud to TMS controller
Physical	19.01 cm × 17.2 cm × 3.8 cm × 1.9 cm (7-1/2 in × 6-3/4 in × 1-1/2 in × 3/4 in)

CHAPTER 2
CP/M OPTION MODULE

2.1 INTRODUCTION

The CP/M option module is the processor component that allows the Professional to run industry-standard 8-bit CP/M applications on the Professional computer system. This module uses the Professional computer system as a host processor to perform its I/O operations while this module runs CP/M software. This module has a Z80 microprocessor that runs the CP/M application programs. The module has 64 kilobytes of dynamic RAM, which gives it the full range of addressing capabilities.

Figure 2-1 shows the CP/M option module in relation to the other hardware components that make up the Professional computer system.

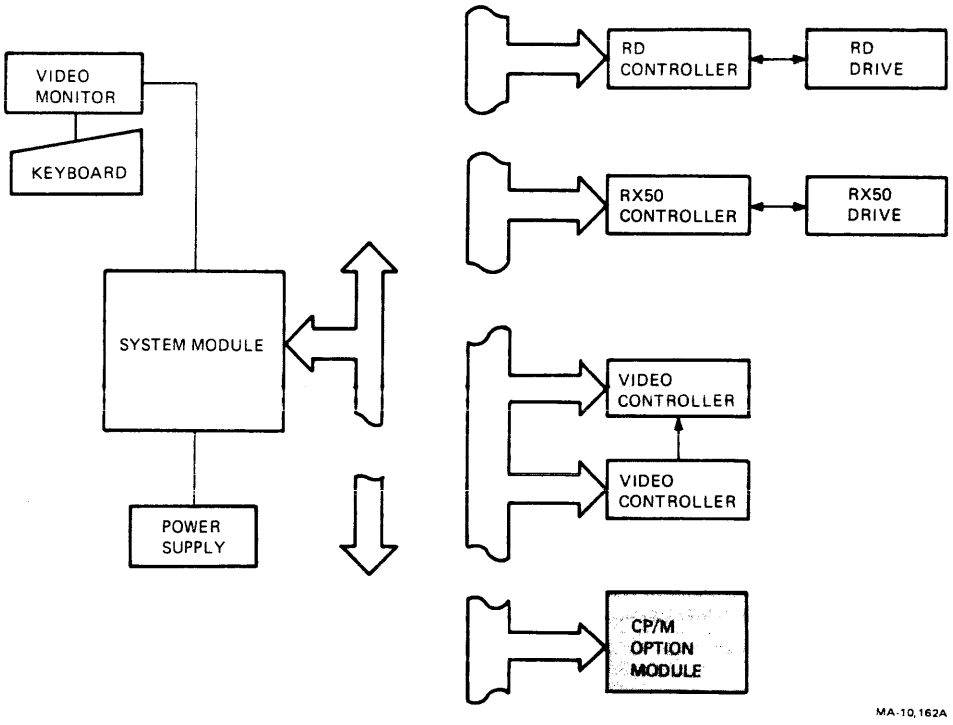


Figure 2-1 Professional System Hardware Components

2.1.1 Related Documentation

The following documents contain information about the CP/M option module.

Title	PN
CTI Bus Technical Manual	EK-00CTI-TM

This manual contains restricted information. You must have a license to order it.

Z80 Assembly Language Programming Manual	03-0002-01

This manual is not available from Digital. You can order it from the following company.

Zilog, Inc.
1315 Dell Avenue
Campbell, CA 95009

2.1.2 Physical Description

The CP/M option module (Figure 2-2) runs CP/M 80 software for the host processor. This module is a single 13.2 cm × 20.3 cm (5.2 in × 8 in) FRU (PN 54-15641) that mounts in any open CTI Bus option slot. A zero insertion force (ZIF) connector (J1) under the module connects the module to the host processor's CTI Bus. The ZIF connector allows the host processor to control the CP/M option module operations from the CTI Bus.

Paragraph 2.4 describes connector J1 and the signals that pass between the CP/M option module and the host processor.

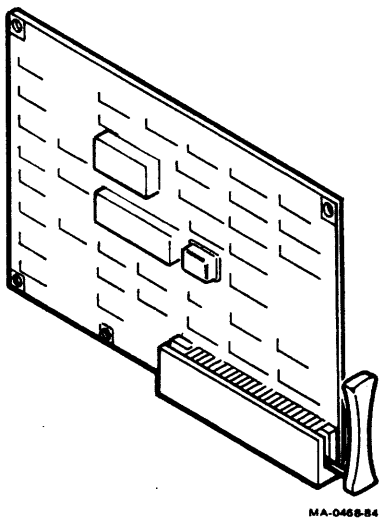


Figure 2-2 CP/M Option Module

2.2 FUNCTIONAL DESCRIPTION

This paragraph describes the CP/M option module on a functional level. It introduces the basic components that allow the module to operate.

To the host processor, the CP/M option module appears as a set of registers accessible from the CTI Bus. The host processor reads to and writes from these registers to issue commands to the module and to retrieve data from or send data to the module. The module runs Z80 microprocessor software for the host processor. The module relies on the host processor to perform all I/O operations and to service the module's requests. For more information about the registers, and the order in which the host processor gains access to them, see Paragraphs 2.5 and 2.6.

2.2.1 Components

The CP/M option module contains the following five circuit groups (Figure 2-3).

CTI Bus interface
Z80 microprocessor
Z80 status register
Z80 microprocessor firmware logic
RAM logic

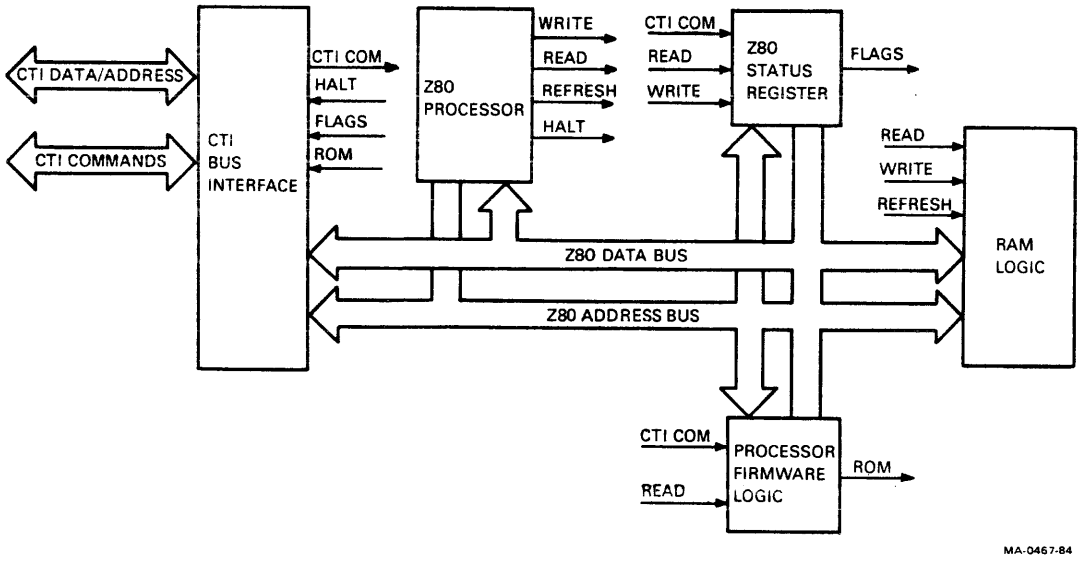


Figure 2-3 Block Diagram

2.2.1.1 CTI Bus Interface Circuits – The host processor gains access to the CP/M option module through these circuits by reading from and writing to the four module registers. (Paragraph 2.5 provides detailed information about the registers.) The CTI Bus interface circuits perform the following seven functions.

1. Provide the handshaking required for the host processor to gain access to the CP/M option module's registers

2. Provide the host processor with status information on the module

3. Allow the host processor to reset the CP/M option module and run the module's self-test

4. Allow the host processor to trap the Z80 microprocessor to the module's minimonitor which is in the Z80 microprocessor firmware logic, allows the host processor to down-line load the CP/M operating system for the Z80 microprocessor

5. Contain the ID ROM that identifies the module to the host processor

6. Provide a self-test for the CTI Bus interface circuits on the CP/M option module to the Z80 microprocessor

7. Pass interrupts to the host processor that will determine whether the host processor operates in interrupt or polling mode.

Paragraph 2.3.1 provides more information about how these circuits work.

2.2.1.2 Z80 Microprocessor Circuits – The Z80 microprocessor circuits are responsible for the CP/M option module's internal operations. These circuits perform the following functions.

1. Arbitrate the use of the internal data and address buses to control internal data flow

2. Run the Z80 microprocessor software

3. Gain access to RAM and Z80 microprocessor firmware logic.

Paragraph 2.3.2 provides more information about how these circuits work.

2.2.1.3 Status Register Circuits – The Z80 status register circuits monitor the data and command exchanges between the host processor and the CP/M option module. These circuits perform the following functions.

1. Monitor host processor access to the data and command registers in the CTI Bus interface circuits

2. Control the event flags and interrupt signals for the host processor and the Z80 microprocessor circuits

3. On request, provide all event status information to the Z80 microprocessor circuits over the internal data bus

Paragraph 2.3.3 provides more information about how these circuits work.

2.2.1.4 Processor Firmware Logic Circuits – The Z80 microprocessor firmware logic contains the Z80 self-test diagnostics and the minimonitor for the Z80 microprocessor. These circuits perform the following functions.

1. Monitor CTI Bus hardware commands from the CTI Bus interface logic and enable the Z80 ROM on command

2. Provide the Z80 self-test diagnostics and minimonitor code

Paragraph 2.3.4 provides more information about the operation of these circuits.

2.2.1.5 RAM Logic Circuits – The CP/M option module contains 64 kilobytes of dynamic RAM. This memory contains data and instructions to be executed by the Z80 microprocessor (CP/M 80 operating system and CP/M 80 applications programs). The Z80 microprocessor controls data storage and retrieval. (The host processor does not have direct access to the RAM contents.) Paragraph 2.3.5 provides more information about how these circuits work.

2.3 THEORY OF OPERATION

The CP/M option module has five circuit groups that work with the host processor to run Z80 microprocessor software. This paragraph describes these circuits at a detailed functional block diagram level to show how this operation occurs.

The host processor gains access to the CP/M option module by reading to and writing from the module's registers. Register access is defined as when the host processor gains access to the CTI Bus interface circuits. Paragraphs 2.5 and 2.6 provides detailed descriptions of the module's registers.

2.3.1 CTI Bus Interface Circuits

The following six CTI Bus interface circuits allow the host processor to gain access to the CP/M option module's registers (Figure 2-4).

CTI Bus access interface
ROM data and address register
Hardware command register
Module status register
Inbound command and data register
Outbound command and data register

These circuits allow the host processor to gain access to the CP/M option module's registers by doing the following two functions.

Addressing the CP/M option module registers.
Strobing command signals to the CP/M option module registers.

These two functions open the data paths for read or write operations.

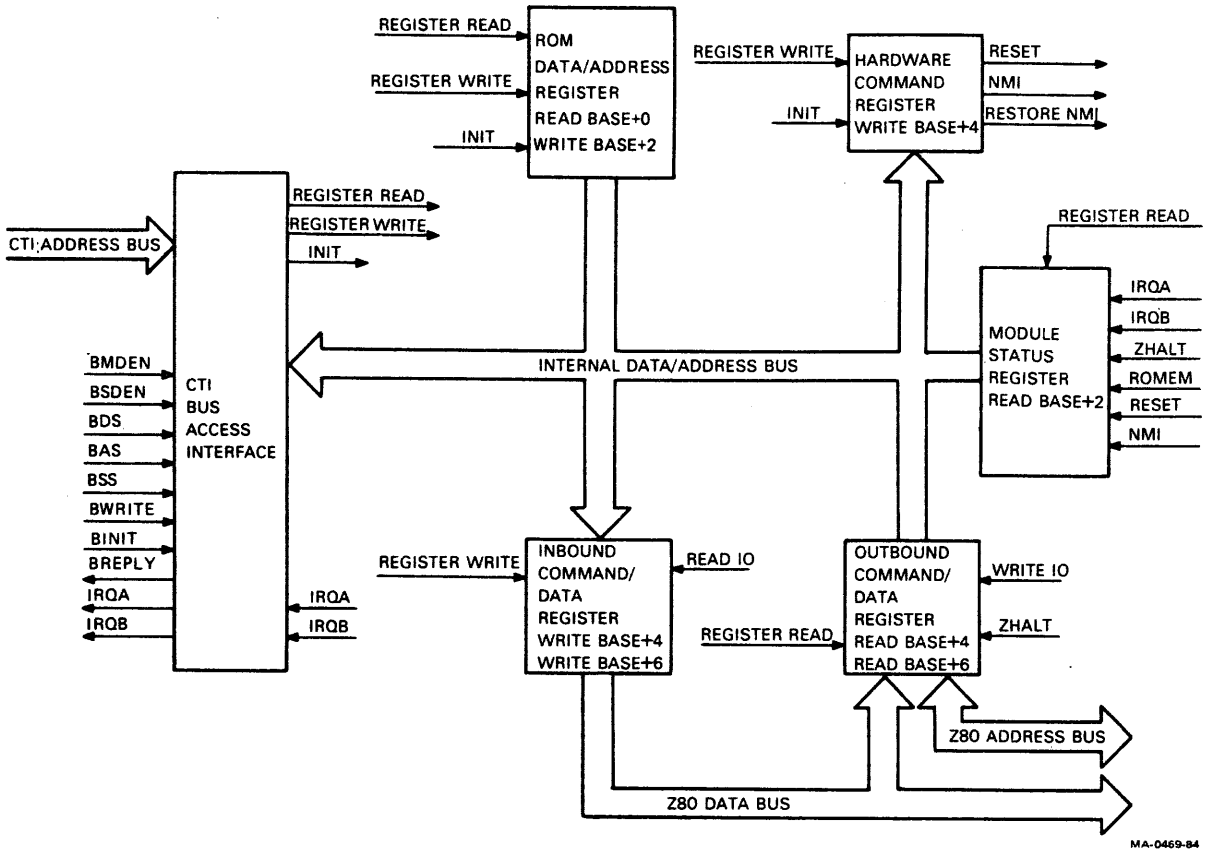


Figure 2-4 CTI Bus Interface Circuits

2.3.1.1 CTI Bus Access Interface – Figure 2-4 shows how the CTI Bus access interface receives and generates CTI bus control signals. This circuit decodes CTI Bus control signals from the host processor to generate register read, register write, and initialize signals for the CP/M option module. This circuit also generates the CTI Bus reply (BREPLY) signal for the host processor when the CP/M option module's slot select strobe (SS) and CTI Bus data strobe (BDS) activate during a data transfer.

The CTI Bus control signals enable data transfers between the CTI data and address bus and the internal data and address bus to and from the CP/M option module's registers. Refer to the *CTI Bus Technical Manual* for more information about protocol requirements and CTI Bus command signal usage and timing.

Two CTI Bus control signals (IRQA and IRQB) are interrupts for the host processor. The CTI Bus access interface acts only as a signal buffer and passes these interrupts from the Z80 status register circuits to the host processor.

The CTI Bus access interface also buffers the CTI Bus initialize (BINIT) signal for the CP/M option module. This signal resets the ROM data and address register, the hardware command register, and the command data flag in the Z80 status register circuits.

2.3.1.2 ROM Data and Address Register – The ROM data and address register consists of an address counter and a data ROM. The data ROM contains code that should be read and executed by the host processor at power-up. The first two bytes of this code are the ID code. This module has been assigned number 000043 (octal). The remaining bytes of the code are diagnostics for gaining access to the CP/M option module's registers. The format of the ROM code is defined in the *CTI Bus Technical Manual.*

Host processor reads to this register (base+0) cause a ROM data byte to transfer to the low byte of the CTI Bus. The ROM is addressed by a counter that increments after each read cycle to base+0. Writes to this register have no effect. Writing to base+2 clears the address counter for the data ROM. A bus INIT also clears the counter.

2.3.1.3 Hardware Command Register – The hardware command register receives the base+4 register write signal and the INIT commands from the CTI Bus access interface. Bit 7 of the internal data and address bus enables or disables this register for writing. If enabled, two data bits control the RESET, NMI, and RESTORNMI signals. These signals must be inactive for the CP/M option module to be enabled by a CTI Bus INIT signal or by writing again to the hardware command register.

The NMI signal enables the Z80 microprocessor firmware logic and is also sent to the Z80 microprocessor. The RESET signal enables the Z80 microprocessor firmware logic and resets the Z80 microprocessor independent of the NMI signal. Either signal generates the RESTORNMI signal, which deactivates the service flags in the Z80 status register circuits.

2.3.1.4 CP/M Option Module Status Register – The CP/M option module status register receives six status flags from the module's circuits. The register receives interrupt signals IRQA and IRQB from the Z80 status register circuits, ZHALT from the Z80 microprocessor, ROMEN from the Z80 microprocessor firmware logic, and RESET and NMI from the hardware command register. The host processor can read this register (base+2) at any time to determine the CP/M option module's present status.

2.3.1.5 Inbound Command and Data Register – Physically, the inbound command and data register is one register, but data is loaded into it by a register write to either base+4 or base+6. The host processor must wait for the Z80 microprocessor to read the stored data or command before the host processor writes to the register again, otherwise the previously written data or command is lost. The Z80 status register circuits generate the event flags for the host processor to indicate whether the Z80 microprocessor reads the data or command (Paragraph 2.3.3 provides more information about the Z80 status register).

2.3.1.6 Outbound Command and Data Register – Physically, the outbound command and data register is two registers. The Z80 microprocessor loads these registers at the same time. The contents of the low byte on the Z80 address bus are loaded into the command register (base+4). The contents of the Z80 data bus are loaded into the data register (base+6).

The host processor must retrieve the data register contents before it retrieves the command register contents. If the host processor reads the command register before it reads the data register, the Z80 microprocessor may overwrite the data register (Paragraph 2.3.3 provides more information about the Z80 status register).

When a Z80 microprocessor halt occurs, the command register contents clear. This tells the host processor, when the host processor reads the command register, that the Z80 microprocessor is halted.

2.3.2 Z80 Microprocessor Circuits

The Z80 microprocessor circuits (Figure 2-5) consist of a processor clock, an I/O multiplexer, and a Z80 microprocessor.

2.3.2.1 Processor Clock – The processor clock provides a 4.0 MHz clock to the Z80 microprocessor, Z80 microprocessor firmware logic circuits, and RAM logic circuits. The Z80 microprocessor uses this clock to synchronize all the CP/M option module operations.

2.3.2.2 I/O Multiplexer – The I/O multiplexer decodes the READ I/O and WRITE I/O signals for the Z80 microprocessor. These signals strobe the CTI Bus interface circuits, Z80 status register circuits, and processor firmware logic circuits. These signals are generated from the Z80 READ, Z80 WRITE, and IORQ (valid I/O address on Z80 address bus) signals, and the addressed I/O from the Z80 address bus.

2.3.2.3 Z80 Microprocessor – This is a 4.0 MHz Z80 microprocessor. The Z80 microprocessor has two sets of six general purpose registers that may be used as either individual 8-bit registers or 16-bit register pairs. The Z80 microprocessor also has two sets of accumulator and flag registers. In addition, the Z80 microprocessor contains a stack pointer, a program counter, a refresh register, and an interrupt register. For more information about the Z80 microprocessor, refer to the *Z80 Assembly Language Programming Manual.*

To reset the Z80 microprocessor, the host processor must issue the hardware reset command from the CTI Bus interface circuits. Paragraph 2.3.3.1 provides more information about how this signal is generated.

The Z80 microprocessor uses the WAIT signal from the Z80 microprocessor firmware logic to extend the instruction/data fetch time. This occurs because the Z80 ROM is slower than the CP/M option module RAM.

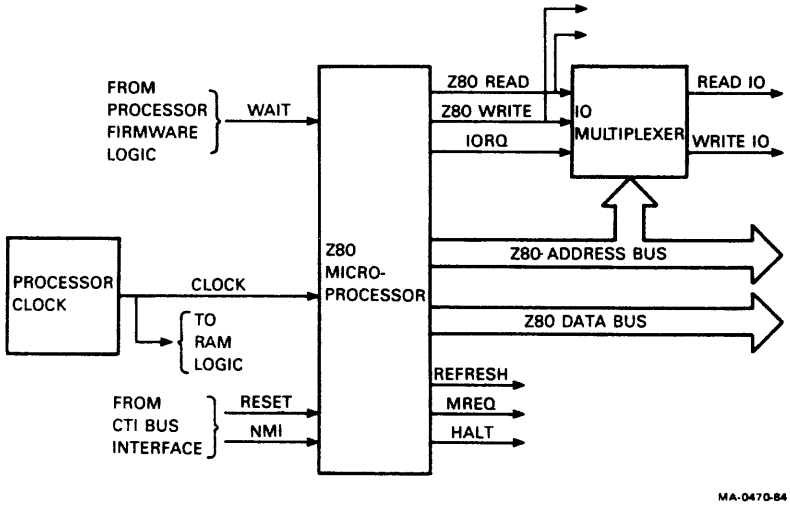


Figure 2-5 Z80 Microprocessor Circuits

The Z80 REFRESH signal controls the RAM circuit refresh cycles. Refreshes to memory occur during program execution and halt operations. Paragraph 2.3.5 provides more information about the RAM logic circuits.

The memory request (MREQ) signal indicates to the Z80 microprocessor firmware logic and RAM all valid memory access addresses on the Z80 address bus.

The HALT signal clears the outbound command register in the CTI Bus interface circuits, and then generates an interrupt signal in the Z80 status register circuits for the host processor. This halt indicates that the Z80 microprocessor executed a software halt instruction. The Z80 microprocessor remains halted until it receives a nonmaskable interrupt (NMI) or RESET command from the host processor via the CTI Bus interface circuits. NMI returns the Z80 microprocessor to the minimonitor in the Z80 ROM. RESET runs the Z80 self-test in the Z80 ROM, then returns the Z80 microprocessor to the minimonitor in the Z80 ROM.

2.3.3 Z80 Status Register

The Z80 status register circuits (Figure 2-6) pass data transfer information (event flags) to the Z80 microprocessor and the host processor. The Z80 status register consists of the following four circuits.

Z80 service flag buffer
Host processor service flag buffer
Command and data flag buffer
Status port

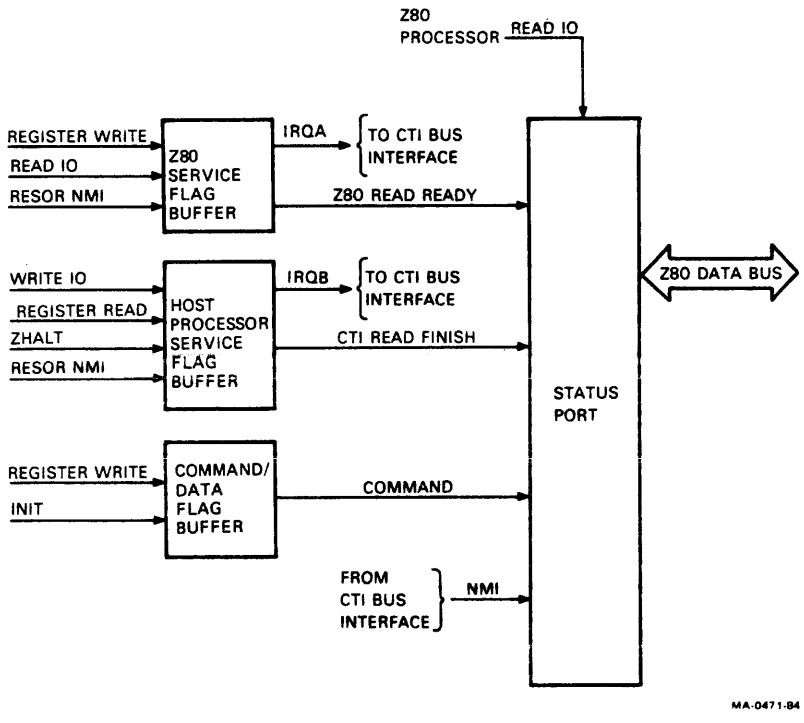


Figure 2-6 Z80 Status Register Circuits

2.3.3.1 Z80 Service Flag Buffer – The Z80 service flag buffer receives three types of signals. It receives the REGISTER WRITE signals, which load the inbound command and data register in the CTI Bus interface circuits, a READ IO signal from the Z80 microprocessor, and the RESTORNMI signal from the hardware command register in the CTI Bus interface circuits. The Z80 service flag buffer generates event flags (IRQA and Z80 read ready) from these signals for the host processor and the Z80 microprocessor.

When the host processor writes to the inbound command and data register, the write strobe (REGISTER WRITE) causes the Z80 service flag buffer to activate the Z80 READ READY signal for the status port. This signal indicates that the host processor sent a new command or new data to the module. When the Z80 microprocessor reads the data or command, READ IO gates the inbound command and data register contents to the Z80 data bus. Then the Z80 READ READY flag is deactivated, and the IRQA flag is activated. IRQA is a host processor status flag that indicates when the CP/M option module is ready for another command or more data. This flag remains active until another write access occurs to the inbound command and data register. This way, the host processor coordinates command and data transfers between the CP/M option module and the host processor.

When the host processor issues a RESET or NMI command via the hardware command register in the CTI Bus interface circuits, the RESTORNMI signal goes active. This sequence deactivates both the IRQA and Z80 READ READY flags until another transfer sequence occurs.

2.3.3.2 Host Processor Service Flag Buffer – The host processor service flag buffer receives four signals. It receives a WRITE IO strobe from the Z80 microprocessor, a REGISTER READ strobe from the CTI Bus interface circuits, a ZHALT command from the Z80 microprocessor, and a RESTORNMI command from the CTI Bus interface circuits. The host processor service flag buffer generates event flags (IRQB and CTI READ FINISH) from these signals for the host processor and the Z80 microprocessor.

When the Z80 microprocessor loads the outbound command and data register in the CTI Bus interface circuits by using the WRITE IO signal, the IRQB flag is activated. The IRQB flag goes to the host processor to indicate that there is a new command or new data in the outbound command and data register. When the host processor reads the register, the REGISTER READ strobe used to gate the register contents to the host processor deactivates the IRQB flag and activates the CTI READ FINISH flag for the status port. Another command or more data loaded into the outbound command and data register deactivates the CTI READ FINISH flag and activates the IRQB flag again. This way, the Z80 microprocessor coordinates command and data transfers between the CP/M option module and the host processor.

When the Z80 microprocessor executes a HALT command, the ZHALT goes active, then the IRQB and CTI READ FINISH flags are activated. As described in Paragraph 2.3.1.6, a halt clears the outbound command register, so a read by the host processor sees a halt condition for the module.

When the host processor issues a RESET or NMI command via the hardware command register in the CTI Bus interface circuits, the RESTORNMI signal goes active. This sequence deactivates the IRQA, IRQB, and Z80 READ READY flags until another transfer sequence occurs.

2.3.3.3 Command and Data Flag Buffer – The command and data flag buffer receives the REGISTER WRITE strobes that load a command or data into the inbound command and data register. If a command is loaded, the command flag (COM) sets. If data is loaded, the command flag clears. This sequence gives the Z80 microprocessor a way to determine whether data or a command was loaded when the Z80 READ READY flag was active.

During power-up or a CTI Bus initialize sequence (INIT active), the command and data flag buffer clears the command flag. Although this indicates data, it is the COM signal's default state. This default state is meaningless unless the Z80 READ READY flag is active.

2.3.3.4 Status Port – The status port is an addressable input device to the Z80 microprocessor. When the Z80 microprocessor strobes READ IO, the states of the Z80 READ READY, REGISTER READ FINISH, COM, and NMI flags are placed on the Z80 data bus for the Z80 microprocessor. The Z80 microprocessor must poll this status port.

2.3.4 Processor Firmware Logic Circuits

The processor firmware logic circuits (Figure 2-7) consist of a Z80 ROM selector and a Z80 ROM. These circuits provide the Z80 microprocessor with a self-test and a minimonitor.

2.3.4.1 Z80 ROM Selector – This circuit gives the host processor access to the Z80 ROM. One of two signals from the CTI Bus interface circuits, RESET or NMI, allows the Z80 microprocessor access to the Z80 ROM. When enabled, the ROMEN signal to the CTI Bus interface circuits goes active.

To enable the Z80 ROM, the Z80 ROM selector receives a Z80 READ signal, a MREQ signal, and an address from the Z80 address bus. When the address from the Z80 microprocessor is in the Z80 ROM range and the Z80 microprocessor is reading the address, the ROMSEL signal goes active. The Z80 microprocessor can synchronize with the data output from the Z80 ROM and the processor clock. The selector also provides a WAIT signal for the Z80 microprocessor.

The Z80 ROM selector is disabled by the Z80 microprocessor. A READ IO deactivates the ROMEN signal, which disables the Z80 ROM from further Z80 microprocessor access. The Z80 microprocessor cannot reactivate the selector. Only the RESET and NMI signals, generated in the CTI Bus interface circuits by the host processor, can reactivate the selector.

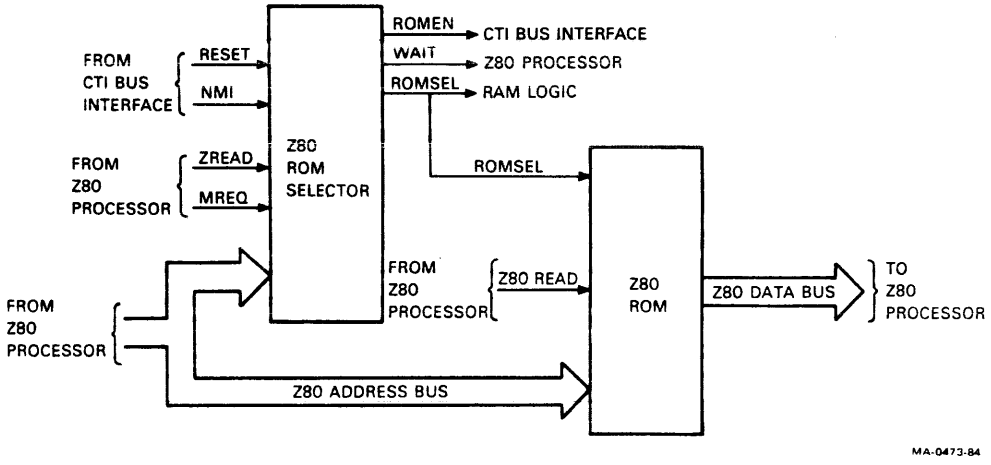


Figure 2-7 Z80 Microprocessor Firmware Logic

2.3.4.2 Z80 ROM - This is a 2K ROM with an address that begins at 0000 and ends at 07FF (hexadecimal). The Z80 ROM contains a self-test and a minimonitor. The contents of a ROM location are placed on the internal data bus for Z80 microprocessor access.

2.3.5 RAM Logic Circuits

The RAM logic circuits (Figure 2-8) provide 64 kilobytes of dynamic RAM for the CP/M option module. The Z80 microprocessor refreshes this RAM array after every instruction fetch. While halted with the software HALT command, the Z80 microprocessor executes NOPs to maintain memory refresh.

For a memory read operation, the RAM is addressable from 0000 to FFFF (hexadecimal) except when the boot ROM is enabled. For a memory write operation, the RAM is addressable from 0000 to FFFF (hexadecimal) no matter what state the boot ROM is in. (This ability is called shadow writing.)

The RAM logic consists of the following five circuits.

Access multiplex logic
Address multiplexer
Row/column address strobe delay
Read/write enable logic
Memory array

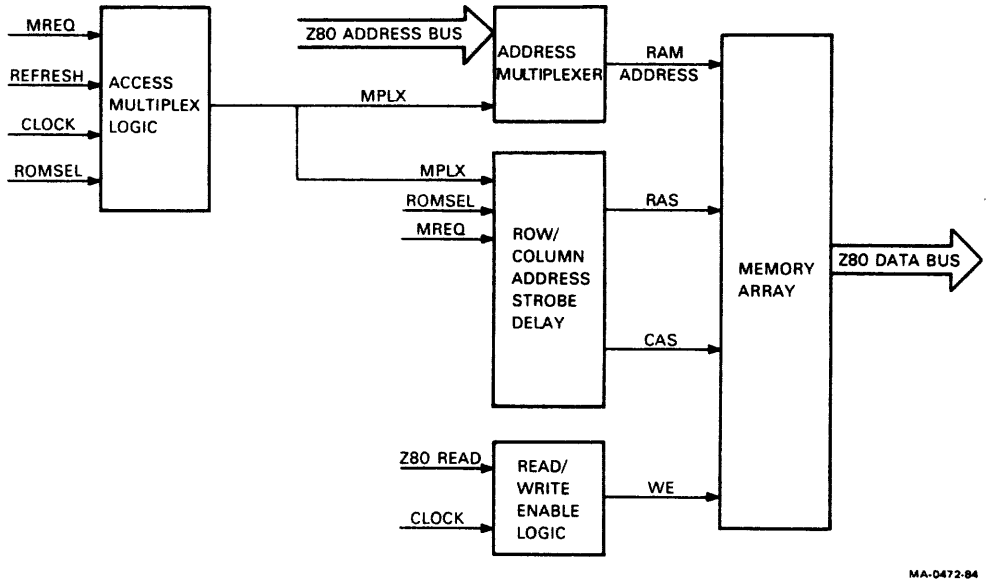


Figure 2-8 RAM Logic Circuits

2.3.5.1 Access Multiplex Logic – The access multiplexer logic controls a multiplex signal (MPLX) for the address multiplexer. The access multiplex logic is controlled by the memory request (MREQ), REFRESH, and CLOCK signals from the Z80 microprocessor and the ROMSEL signal from the Z80 microprocessor firmware logic circuits. These signals cause MPLX to go active (select the address high byte) or inactive (select the address low byte). The default state of MPLX is inactive.

During a refresh cycle the REFRESH signal goes active, which places the MPLX signal in the inactive state. During a memory access cycle, when the boot ROM is being addressed, MPLX remains inactive to prevent a column address strobe to the memory array.

For an actual RAM access cycle the MPLX signal should be inactive. This state allows the low byte on the address bus to be strobed as the row address to the RAM. When the MPLX signal goes active, the high byte on the address bus is strobed as the column address to the RAM.

2.3.5.2 Address Multiplexer – The address multiplexer selects either the low Z80 address bus byte or the high Z80 address bus byte to pass to the memory array as a RAM address. When asserted, the MPLX signal selects the high address byte. When deasserted, the MPLX signal selects the low address byte.

2.3.5.3 Row/Column Address Strobe Delay – The row/column address strobe delay controls the assertion of the row address and column address strobes (RAS and CAS) for the memory array. During an actual RAM access cycle, RAS asserts when the Z80 microprocessor asserts the MREQ signal. When the MPLX signal asserts at the next clock pulse, CAS asserts 20 ns later (nominal) and RAS deasserts 185 ns later. CAS remains asserted until MREQ deasserts. These delays allow the correct access sequence by the Z80 microprocessor to go to the memory array.

The row/column address strobe delay also receives the ROMSEL signal from the Z80 microprocessor firmware logic circuits. When the boot ROM is enabled, the ROMSEL signal prevents MPLX assertion, which prevents access to RAM.

2.3.5.4 Read/Write Enable Logic – The read/write enable logic uses the Z80 READ signal to control the write enable (WE) signal to the memory array. The clock gates the active or inactive state of Z80 READ to WE. When Z80 READ is active, WE is inactive. When Z80 READ is inactive, WE is active.

2.3.5.5 Memory Array – The memory array has 64 kilobytes of dynamic RAM, which consists of eight 64K × 1 parts. The Z80 microprocessor controls access to this memory. The timing requirements to gain access to this memory are performed by the access multiplex logic, address multiplexer, row/column address strobe delay, and read/write enable logic.

2.4 CONNECTOR J1 DESCRIPTION

This paragraph describes the signals passed between the CP/M option module and the host processor. Figure 2-2 shows the connector on the controller.

The CP/M option module uses the data/address lines and control lines of the CTI Bus to perform program data transfers. Refer to Chapter 5 in the *Professional 300 Series Technical Manual Volume I* for more information.

Table 2-1 lists the pin functions of the CP/M option module's J1 connector. The signal mnemonic column also describes each signal's asserted state. An L after the mnemonic indicates an asserted low state (logic zero). An H after the signal name indicates an asserted high state (logic high). The CP/M option module uses the standard CT100 60-pin zero insertion force (ZIF) connector. Table 2-1 also lists the pintouts, bus receivers, and drivers for connector J1.

Table 2-1 Connector J1 Pin Description

Pin	Signal Function	Signal Mnemonic
1	Not used	BDCOK H
2	+5 V	+5.0 V
3	Not used	
4	Ground	GND
5	Bus Initialize	BINIT L
6	−12 V	−12.0 V
7	Not used	BDAL 15 L
8	Not used	BDAL 13 L
9	Not used	BDAL 14 L
10	Not used	BDAL 12 L
11	Not used	
12	Not used	BDAL 11 L
13	Bus reply	BRPLY L
14	Not used	BDAL 10 L
15	Ground	GND
16	Not used	BDAL 09 L
17	Master data enable	BMDEN L
18	Not used	BDAL 08 L
19	Bus write	BWRITE L
20	Data/address bit 7	BDAL 07 L
21	Not used	BWLB L
22	Data/address bit 6	BDAL 06 L
23	Not used	BWHB L
24	Data/address bit 5	BDAL 05 L
25	Slave data enable	BSDEN L
26	Data/address bit 4	BDAL 04 L
27	Ground	GND
28	Data/address bit 3	BDAL 03 L
29	Slot select	SS L
30	Data/address bit 2	BDAL 02 L
31	Interrupt B	IRQB L
32	Data/address bit 1	BDAL 01 L
33	Interrupt A	IRQA L
34	Data/address bit 0	BDAL 00 L
35	Option present	OPRES L (GND)
36	Ground	GND
37	Data strobe	BDS L
38	+5 V	+5.0 V
39	Address strobe	BAS L
40	Not used	

Table 2-1 Connector J1 Pin Description (Cont)

Pin	Signal Function	Signal Mnemonic
41	Not used	
42	Not used	
43	Not used	BIOSEL L
44	Not used	BDAL 21 L
45	Not used	
46	Not used	BDAL 20 L
47	Not used	
48	Not used	BDAL 19 L
49	Not used	
50	Not used	BDAL 18 L
51	Ground	GND
52	Not used	BDAL 17 L
53	Not used	BMER L
54	Not used	BDAL 16 L
55	Not used	
56	Not used	
57	Not used	
58	+5 V	+5.0 V
59	Not used	
60	Ground	GND

2.5 PROGRAMMING REGISTERS

This paragraph describes the CP/M option module's programming (software) registers. These registers provide the only access to the Z80 microprocessor.

To the host processor, the CP/M option module contains four 8-bit registers for communication with the CTI Bus. Communication between the CP/M option module and the host processor occurs through these registers. Byte transfers perform all write operations to the registers. Undefined registers are reserved. Table 2-2 defines the CP/M option module's four programming registers.

Table 2-2 Host Programming Registers

Bus Address	Name	Access
Base+0	ROM data	Read only
Base+2	Status/base+0 reset	Read - status/write - base+0 reset
Base+4	Inbound/outbound command	Read/write
Base+6	Inbound/outbound data	Read/write

2.5.1 ROM Data Register (Base+0)

The ROM data register gives the host processor the CP/M option module's ID code and the diagnostics used by the host processor to test the module for correct operation.

This register is a ROM, which contains code for the host processor. The ROM is addressed by a counter that increments each time the register is read. Reading this register causes a byte from the ROM to be transferred onto the low byte of the CTI Bus. Writes to this register have no effect, and the high byte is always read as all zeros.

The first two bytes of the ROM are the ID code. This module is assigned number 000043 (octal). The remaining bytes of the ROM are code diagnostics for the module. The *CTI Bus Technical Manual* defines the format of the ROM code.

Paragraph 2.5.2 explains how to reset the ROM counter for this register by register access. BUS INIT also clears the counter.

2.5.2 Status/Base+0 Reset Register (Base+2)

This register has two functions. During a host processor read cycle, it contains status data for the host processor. During the write cycle, it resets the ROM data register address counter.

For a read cycle, the low byte contains flag status data in the bit locations shown in Figure 2-9.

2.5.2.1 Nonmaskable Interrupt (NMI) Command Flag – When active (0), the nonmaskable interrupt (NMI) command flag indicates that the host processor trapped the CP/M option module back to its minimonitor with a hardware command. NMI should not be left in its active state; this prevents handshaking to the Z80 microprocessor. Paragraph 2.5.3 provides the command register definition.

2.5.2.2 RESET Flag – When the reset flag is active (0), the Z80 microprocessor is in a reset state (it does not execute instructions or refresh memory). This flag sets when the host processor resets the CP/M option module with a CTI Bus INIT signal, or send a hardware RESET command. Paragraph 2.5.3 provides the command register definition.

At the transition from the active (0) to the inactive (1) state, the Z80 microprocessor begins running the Z80 self-test at address 0 in the Z80 ROM, then jumps to the minimonitor.

2.5.2.3 ROM Enable (ROMEN) Flag – When the ROM enable flag is active (0), the ROM contents are mapped into the lower 2K of memory for memory read accesses. This flag becomes a 1 when the Z80 microprocessor executes an IN A, (010H) instruction, which indicates that ROM is disabled and RAM occupies the entire addressing space.

2.5.2.4 Z80 Halt (ZHALT) Flag – When the Z80 halt flag is active (0), the Z80 microprocessor halts (it does not execute instructions but still refreshes memory). This bit becomes a 1 when the Z80 microprocessor leaves the halt state (by NMI or RESET). Paragraph 2.5.3 provides the command register definition.

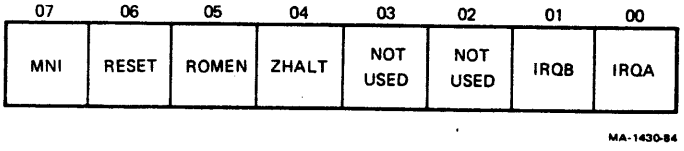


Figure 2-9 Status Register Bit Assignments

2.5.2.5 Interrupt B (IRQB) Flag – The interrupt B flag goes to 0 to indicate that the interrupt has become active (the Z80 microprocessor has written to base+4 and base+6). This bit becomes a 1 when the host processor reads base+4.

2.5.2.6 Interrupt A (IRQA) Flag – The interrupt A flag goes to 0 to indicate that the interrupt has become active (the Z80 microprocessor has read its inbound register). This bit becomes a 1 when the host processor writes to base+4 (or base+6 if data was sent to the Z80 microprocessor).

2.5.3 Inbound/Outbound Command Register (Base+4)
This register is a read/write command register for the CP/M option module. When read by the host processor, this register sends commands to the host processor from the Z80 microprocessor. The host processor writes commands to the CP/M option module for two modes: software commands for the Z80 microprocessor and hardware commands for the CP/M option module.

2.5.3.1 Commands to the Host Processor – The Z80 microprocessor loads software instructions (refer to the *Z80 Assembly Language Programming Manual*) for software decoding and execution by the host processor. The commands are coded as port numbers and decoded as I/O functions (for example, write character to terminal). Paragraph 2.6 provides more information about the operations that use this register.

2.5.3.2 Software Commands From the Host Processor – The host processor indicates that bits 0 through 6 contain a software command by setting bit 7 (1). These bits contain Z80 microprocessor software instructions (refer to the *Z80 Assembly Language Programming Manual*) for software decoding and execution by the Z80 microprocessor. The commands are coded as the value written to base+4. Paragraph 2.6 provides more information about the operations that use this register.

2.5.3.3 Hardware Commands From the Host Processor – The host processor indicates that bits 0 and 1 send a hardware command by clearing bit 7 (0). For this operation bits 2 through 6 are ignored. Bit 1 is the RESET command and bit 0 is the NMI command.

Writing a 1 to the hardware command register (a 0 to bit 1 and a 1 to bit 0) causes the Z80 microprocessor to jump to address 66 in the Z80 ROM. This address is the minimonitor for the Z80 microprocessor and will be executed after the host writes a 0 to bit 1 and a 0 to bit 0. The Z80 microprocessor does not run a self-test for this writing sequence.

Writing a 2 to the hardware command register (a 1 to bit 1 and a 0 to bit 0) forces the module to perform a power-up Z80 microprocessor reset. When the host processor releases the reset by writing a 0 to bit 1 and a 0 to bit 0, the Z80 microprocessor jumps to address 0000 (hexadecimal) in ROM. Address 0000 is the starting address of the self-test that will run before the Z80 microprocessor runs the minimonitor in the Z80 ROM.

Paragraph 2.6 provides more information about the operations that use this register.

2.5.4 Inbound/Outbound Data Register (Base+6)
This register is used for reading or writing data associated with a command in the inbound/outbound command register (base+4). The host processor must read the data in this register before it reads the associated command in the inbound/outbound command register, otherwise the data are lost. The command information determines the meaning of the data (for example, if the command writes a character to the terminal, this register contains the character to be written). For write operations to this register, the Z80 microprocessor must interpret the data. Paragraph 2.6 provides more information about the operations that use this register.

2.6 OPERATION

This paragraph describes in general how the CP/M option module operates. It explains the hardware command sequences in detail and includes diagnostic information.

2.6.1 Power-Up

When the CP/M option module is powered up, the Z80 microprocessor is in reset mode and the Z80 ROM is enabled, but all other flags are inactive. Paragraph 2.5 provides a definition of the status register (base+2). In reset mode, the module does not execute instructions or refresh memory.

The host processor reads the ROM data register (base+0). This register contains code to be executed by the host processor. The first two bytes of this code are the ID code. This module has been assigned number 000043 (octal). The remaining bytes are diagnostics that the host processor can run on the CP/M option module.

The diagnostics also tell the host to issue a hardware RESET command. The RESET command causes the Z80 microprocessor to run the Z80 self-test in the Z80 ROM, and then loop in the Z80 ROM minimonitor that is waiting for the host processor. When the host processor asks for the Z80 self-test results (see Table 2-3), the host can run the interface self-test it read from the ROM data register (see Table 2-4). The format of the ROM data register code is defined in the *CTI Bus Technical Manual*. Paragraph 2.5.1 and 2.5.2 provide information about accessing this register.

Writes to the ROM data register have no effect, and the high byte is always read as all zeros. Reading the ROM data register causes a byte to be read from the data ROM and transferred onto the low byte of the CTI Bus. The data ROM is addressed by a counter that increments each time this register is read. The data ROM counter is cleared by writing to the base+2 register. A bus INIT signal also clears the counter.

2.6.1.1 Z80 Self-Test – The hardware RESET command starts the Z80 self-test. This self-test checks the Z80 microprocessor, Z80 ROM, and RAM logic. The Z80 self-test consists of the following seven parts.

Z80 general purpose registers test
Z80 status register test
Z80 ROM test
Z80 high memory test
Z80 stack pointer test
Z80 worst case instruction test
Z80 low memory test

When the Z80 self-test is complete, the Z80 microprocessor reports the error. For error reporting to occur, the host processor must send the REPORT Z80 ERROR CODE software command to the CP/M option module after sending the hardware RESET command. After receiving the REPORT Z80 ERROR CODE software command, the CP/M option module sends the error code, followed by the 1's complement of the error code, to the host processor. If a fault is not detected, the Z80 self-test automatically enters into the minimonitor. Otherwise, the Z80 self-test loops forever and ignores all software commands.

Table 2-3 defines the octal error codes reported by the Z80 self-test. Note that bit 7 is set, which indicates a Z80 error code rather than an interface self-test error code.

Table 2-3 Z80 Self-Test Error Codes

Error Code	Definition
000	All components tested functioning correctly
201	Error in Z80 general purpose registers
202	Error in Z80 status register
203	Error in Z80 ROM
204	Error in Z80 high memory
205	Error in Z80 stack pointer
206	Error in worst case instruction, IX, or IY register*
207	Error in Z80 low memory
210	Unexpected interrupt

* Refer to the *Z80 Assembly Language Programming Manual*

Table 2-4 Interface Self-Test Error Codes

Error Code	Definition
0	All components tested functioning correctly
1	Error in Z80 status register
2	Error in Z80 self-test
3	Error in inbound/outbound command and/or data register
4	Error in Z80 halt
5	Error in Z80 NMI
6	Unexpected nonexistent memory trap

2.6.1.2 Interface Self-Test – The host self-test starts the interface self-test. This self-test checks the CTI Bus circuits, Z80 halt state, Z80 NMI state, and CP/M-generated interrupts (IRQA and IRQB). The interface self-test consists of the following five parts.

Z80 status register test
Z80 self-test
CTI Bus interface test
Halt test
NMI test

Because this self-test is interrupt driven, interrupts are checked in most of the tests. When this self-test is complete, the configuration table is updated with the correct error number, interrupts are disabled, and all vectors are restored.

Table 2-4 defines the octal error codes reported by the interface self-test.

2.6.2 Reset and NMI Hardware Commands

Two hardware commands, RESET and NMI, place the CP/M option module in known operation states (described in Paragraph 2.6.2.1 and 2.6.2.2). (Also see Paragraph 2.5). The host processor can send these commands to the CP/M option module at any time.

2.6.2.1 RESET Command – The RESET command causes all flags except ROMEN and RESET to become inactive. When the host issues this command, the Z80 microprocessor is enabled to access the Z80 ROM. This allows it to fetch and execute instructions at ROM location 0000 (hexadecimal). To perform a RESET operation, the host processor sets RESET in one instruction and then clears it in the next instruction.

2.6.2.2 Nonmaskable Interrupt (NMI) Command – The nonmaskable interrupt (NMI) command enables the ROM at the end of the current Z80 microprocessor instruction. Unlike RESET, NMI traps the Z80 microprocessor back to its minimonitor, and starts command execution at location 0066 (hexadecimal) in the Z80 ROM. NMI should not be left in its active state because then host processor handshaking is ignored by the CP/M option module. To perform an NMI operation, the host processor sets NMI in one instruction and clears it in the next instruction. However, a delay of up to nine microseconds may occur before the Z80 microprocessor recognizes NMI.

2.6.3 Host Processor Initiated Transfers

When the host processor loads the inbound/outbound data register (base+6) or the inbound/outbound command register (base+4), the Z80 READ READY flag (IRQA) sets. If the command register was loaded, the Z80 command and data flag sets, otherwise it stays as it was. The Z80 command and data flag clears during host processor writes to the data register.

If the host processor does not wait for the Z80 microprocessor to read previously written data (IRQA becoming active), the data can be lost. The Z80 microprocessor can poll a Z80 READ READY flag. If the flag is set, the Z80 microprocessor checks the value of the command and data flag to determine if the data register contains new data or the command register contains a new command. When the Z80 microprocessor reads either the command or data register, the IRQA flag sets for the host processor and the Z80 READ READY flag clears for the Z80 microprocessor.

When the host processor writes data to the data register (base+6), the Z80 microprocessor must interpret the data. Writing to register base+6 clears the Z80 microprocessor command and data flag.

When the Z80 microprocessor reads the data register, IRQA clears to tell the host processor that it can now rewrite the data register contents. This action also clears the command and data flag if it was set during a write to the command register.

To speed up data only transfers, the host processor can disable interrupts and use polling. If interrupts are disabled, an interrupt may be pending when the interrupts are enabled again.

2.6.4 Z80 Microprocessor Initiated Transfers

When the Z80 microprocessor loads the inbound/outbound command and data registers, the host processor READ FINISH flag (IRQB) becomes active. If the Z80 microprocessor does not wait for the host processor to read previously written data or commands (IRQB is still active), the previous information can be lost.

When the host processor reads the command register, the IRQA flag sets to signal the Z80 that it can now rewrite the command and data registers contents. If the host processor does not read the data register before the command register, the data register contents are lost. Therefore, the host processor must first read the data register (base+6) and then read the command register (base+4).

2.6.5 Z80 Microprocessor Halt Recovery

When the Z80 microprocessor executes a HALT instruction, the HALT L line on the Z80 microprocessor becomes active. This sequence generates a HALT flag. During a halt operation, the inbound/outbound command register (in the Z80 microprocessor to host processor direction) clears and the IRQB flag sets. While halted, the Z80 microprocessor executes NOPs to maintain the memory refresh state.

When the host processor reads base+4 and finds 00 (hexadecimal) in the command register, it decodes the data as a halt condition. The host processor may then set the NMI flag or reset the module.

2.6.6 Z80 ROM and RAM Accesses

The 2K Z80 ROM space, beginning at address 0000 and ending at 07FF (hexadecimal), contains the Z80 self-test and a minimonitor for the CP/M option module.

The Z80 microprocessor reads the Z80 ROM during power-up and at a hardware RESET or NMI command issued by the host processor.

The CP/M option module also contains 64 kilobytes of dynamic RAM, which consists of eight 64K × 1 RAM ICs. The Z80 microprocessor refreshes this RAM array from its refresh counter after every instruction fetch. While halted with the software HALT instruction, the Z80 microprocessor executes NOPs to maintain the memory refresh state. When the CP/M option module is reset, no refresh cycles occur and RAM data is lost.

For a Z80 microprocessor memory read operation, RAM is addressable from 0000 to FFFF (hexadecimal), except when ROMEN H is active. For a Z80 microprocessor memory write operation, RAM is addressable from 0000 to FFFF (hexadecimal) regardless of the state of ROMEN H (this is called shadow writing).

2.7 SPECIFICATIONS

Table 2-5 lists the CP/M option module's environmental specifications. Table 2-6 lists the controller's power specifications.

Table 2-5 Environmental Specifications

Specification	Minimum	Maximum
Temperature	5°C (41°F)	60°C (140°F)
Humidity	10%	95%
Wet bulb reading	–	32°C (90°F)
Dew point	2°C (36°F)	–

Table 2-6 Power Specifications

Voltage Requirements	Current
+5 V ±5%	1 A
−12 V ±5%	38 mA

CHAPTER 3
DECNA CONTROLLER OPTION MODULE

3.1 INTRODUCTION

This chapter is a physical and functional description of the Digital Ethernet CTI Bus Network Adapter (DECNA) controller option module. This chapter describes the DECNA option module, how it connects to other devices, and how it works on a hardware functional block level.

The DECNA option module is an Ethernet communications controller for Professional 300 series computer systems. It allows a computer to exchange data with other computers and work stations on a local area network that uses PRO/DECnet software, or with other networks that use the Ethernet communications system.

3.2 PHYSICAL DESCRIPTION

The DECNA option module (Figure 3-1) is a standard-size printed circuit board that installs into one option slot on a Professional 300 series computer system. This module has a single 90-pin zero insertion force (ZIF) connector (J1) and connects via the bus and system module to a 15-pin D-subminiature-type connector (NET 1) on the back of the Professional 300 Series system box.

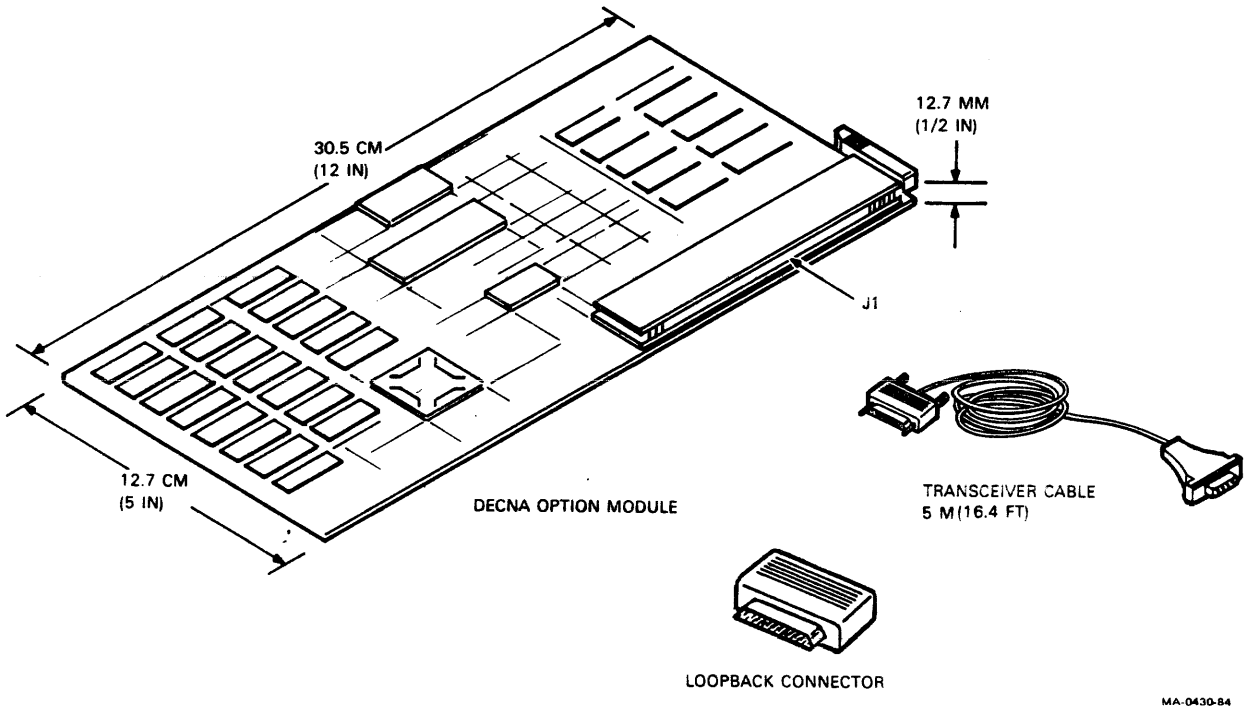


Figure 3-1 DECNA Option Module, Transceiver Cable 5 Loopback Connector

A 5 m (16.4 ft) PVC transceiver cable, with a thumbscrew connector on one end and a standard slide-lock connector on the other end, is supplied with the DECNA option module. A loopback connector and a maintenance diskette are also supplied.

3.3 SPECIFICATIONS

The DECNA option module performs specified data link and physical channel functions, which permit 10 Mbit is data communications between stations separated by up to 2.8 km (4923 ft). The DECNA option module complies with the Xerox/Intel/Digital Ethernet Specification Version 2.0.

The DECNA option module uses less than 3.0 A at +5 V, and does not draw any current from the +12 V supply. The Professional 300 host system provides up to +12 V at 0.5 A to the transceiver via the transceiver cable connector.

Physical Specifications

Height	12.7 cm (5 in)
Length	30.5 cm (12 in)
Width	12.7 mm (1/2 in)

Environmental Specifications

Temperature	15°C (59°F) to 32°C (90°F)
Humidity	20% to 80%
Wet bulb reading	25°C (77°F) maximum
Dew point	2°C (36°F) minimum

3.4 ETHERNET OVERVIEW

Ethernet is a local area high-speed (10 Mbits/s) communications network extending from several hundred to several thousand feet.

3.4.1 Main Physical Components

Ethernet includes the following main physical components (Figure 3-2).

1. 50 ohm coaxial cable with 50 ohm terminators on each end
2. Transceivers that transmit and receive signals on the coaxial cable

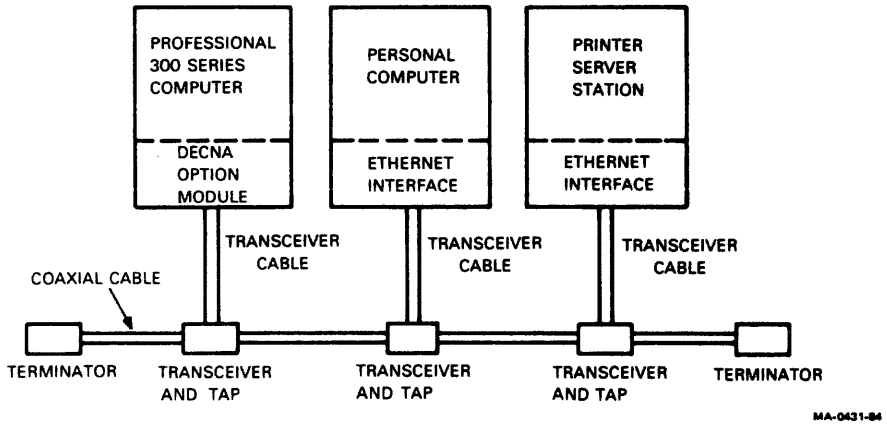


Figure 3-2 Ethernet Elements (Example)

3. Transceiver cables that connect the Ethernet interface to the transceivers

4. Ethernet interface (for example, the DECNA option module) that provides data encapsulation and decapsulation, network link management, and encoding/decoding of the signal to and from the transceivers

3.4.2 Ethernet Protocol

The Ethernet specifications, key elements are the rules for using the coaxial cable. These rules determine how a station transmits information over the coaxial cable. These rules are called CSMA/CD rules (Carrier Sense, Multiple Access, with Collision Detection). The Ethernet interface was designed to adhere to these rules.

Carrier Sense means that any station that wants to transmit monitors the line first to see if the cable is busy. The station waits until the cable is idle before transmitting.

Multiple Access means that any station can transmit. There is no central controller that decides which station can transmit and when it can transmit. This is distributed control, where all stations are equal and have equal access to the cable.

Collision Detection means that when the cable is free, a station can start transmitting. Any transmitting station monitors the line to detect any other station that is transmitting at the same time and causing a collision. If such a collision is detected, the transmitting station continues transmitting for a fixed time to make sure all other transmitting stations also detect the collision. This is called a "jam." After a jam, transmitting stations stop transmitting for a random period of time before trying again. The random wait period increases by an algorithm defined in the protocol so that collisions are resolved even if many terminals are colliding.

3.4.3 Transmission Frame Format

Figure 3-3 shows the Ethernet frame format for transmitting on the coaxial cable. The following text describes the Ethernet frame format.

The *Preamble* (64 bits) provides receive synchronization.

The *Destination Address* field (48 bits) specifies the station(s) for which the frame is intended. The address value can be: the physical address of one station, a multicast group address associated with one or more stations, or the broadcast address for simultaneous transmission to all network stations.

The *Source Address* field (48 bits) specifies the transmitting station's physical address. Each Ethernet interface has a unique physical address assigned to it when it is built. During transmission, the interface inserts its unique physical address into the source address field.

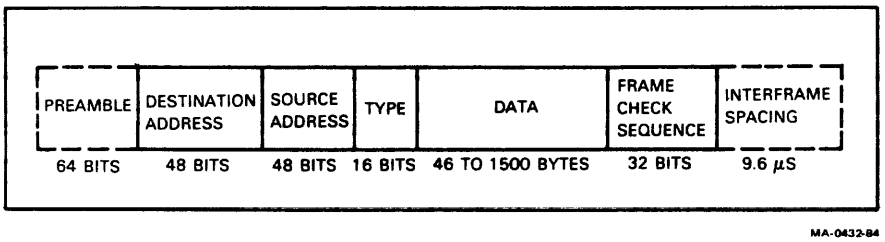


Figure 3-3 Ethernet Frame Format

The *Type* field is specified by the user for use by high level network protocols. This field tells the receiving station how to interpret the contents of the data field.

The *Data* field can contain a variable number of data bytes ranging from 46 to 1500 bytes. This field can accept less than 46 bytes by automatically inserting null characters to complete a 46-byte minimum frame size.

The *Frame Check Sequence* field (32 bits) contains a 32-bit cyclic redundancy check (CRC) value generated by the interface during transmission.

The *Interframe Spacing* consists of a minimum of 9.6μs quiet period at the end of the data packet.

3.5 DECNA FUNCTIONAL OVERVIEW

The DECNA option module accepts data from the Professional 300 series computer system, groups the data into message packets according to the Ethernet frame format, then sends the packets through the Ethernet network. The module also receives, decodes, and stores incoming message packets for computer system access.

The DECNA option module is functionally divided into the following three major circuits (Figure 3-4).

CTI Bus interface
Dual-ported memory
Ethernet interface

The *CTI BUS interface* is a slave interface. It provides buffers, latches, registers, and decoding logic for interfacing between the host system and the DECNA option module. It has direct link memory access to the dual-ported memory. The CTI Bus accesses registers via the I/O page. Paragraph 3.6 describes the CTI Bus Interface in detail.

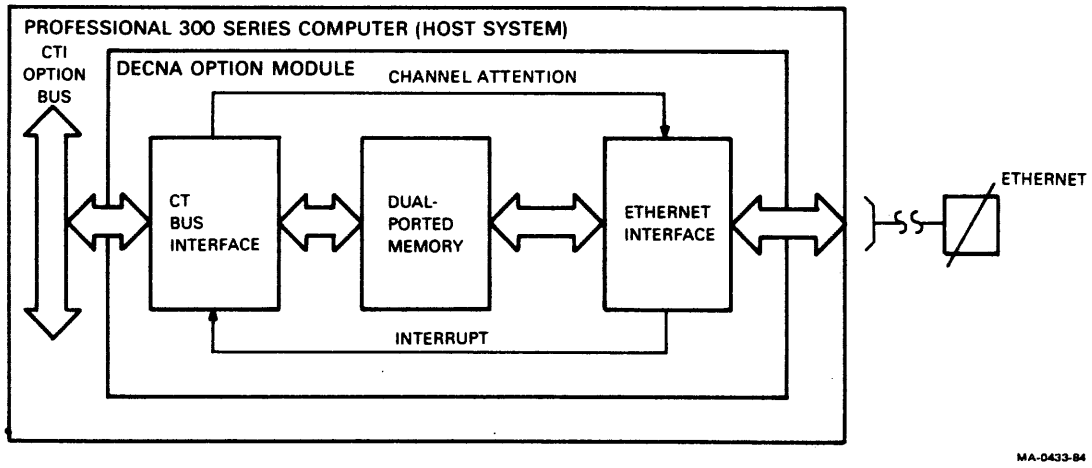


Figure 3-4 DECNA Option Module Major Functional Block Diagram

The *dual-ported memory* (128 kilobytes) provides a shared access area for the memory resident command, status, and data buffers. It is an extension of host system memory. The host system can use parts of the dual-ported memory to store data and Ethernet commands. The dual-ported memory appears in the 22-bit address space outside of the I/O page. It has large buffering capability and looks like slave memory on the CTI Bus. For transmission the host system loads the dual-ported memory. The Ethernet interface then transfers the stored data at any rate it wants. For reception, the dual-ported memory stores large amounts of incoming data, which the host system can access. The dual-ported memory is enabled or disabled by a software-accessible bit through the CTI Bus interface. Paragraph 3.7 describes the dual-ported memory in detail.

The *Ethernet interface* is further divided into two major circuits: the Ethernet communications controller and the Ethernet serial interface (Figure 3-5). The Ethernet communications controller handles the Ethernet data link layer protocol and controls how the DECNA option module uses the link. During transmission, the Ethernet interface collects information from shared memory, prepares packets for transmission, and controls packet transmission. During reception, the Ethernet interface assembles data received into word format and loads messages into shared memory. The Ethernet interface provides the Ethernet physical layer cable interface. This circuit generates 10 Mbits/s data rates, performs Manchester encoding/decoding of packet information, and monitors channel access. Paragraph 3.8 describes the Ethernet interface in detail.

3.5.1 Initialization

The entire DECNA option module is reset during power-up and can also be reset via software-controlled bits in a control register that is part of the CTI Bus interface. A memory reset bit in the control register resets the DECNA memory and an Ethernet interface reset bit resets the DECNA Ethernet interface. Paragraph 3.6 describes the CTI Bus interface control register.

3.5.2 Transmission Overview

During transmission, the host system processor writes the transmit command block and data packet into the dual-ported memory via the CTI Bus interface. The host system then raises and lowers the channel attention signal (CA) (Figure 3-5) to instruct the Ethernet Interface to locate, read, and process the next command. The Ethernet interface, after processing the command, gains access to the serial link, moves the data from the dual-ported memory, forms the data into Ethernet-formatted packets, then transmits the data packets to the destination node. When transmission is complete (or an attempt is complete), the Ethernet interface writes the transmit status into the dual-ported memory and asserts an interrupt signal to the host system. This signal tells the system to check transmission status.

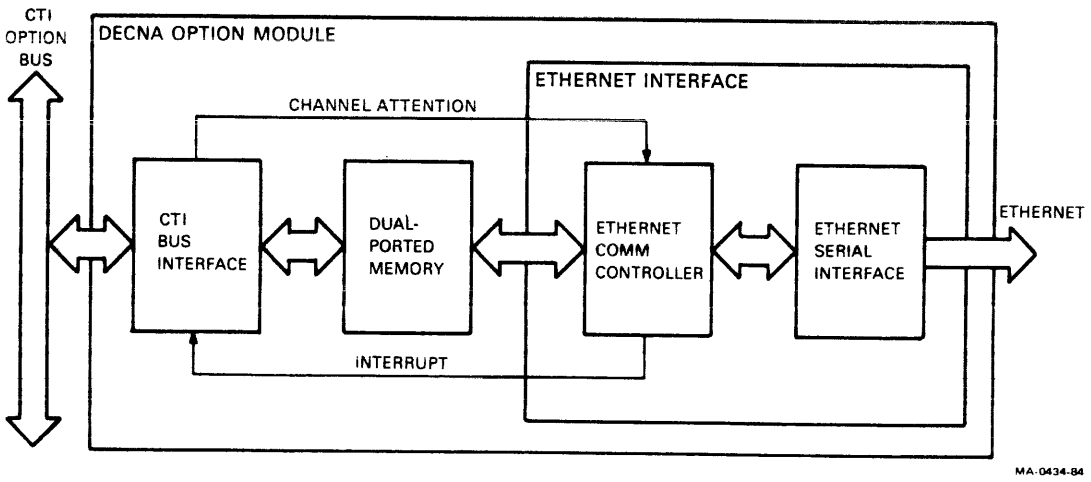


Figure 3-5 DECNA Ethernet Interface

3.5.3 Reception Overview

To receive, the host system gains access to the dual-ported memory to set up the receive buffer area(s) and the receive command block(s). The host system then raises and lowers the channel attention (CA) signal to instruct the Ethernet interface to locate, read, and process the command. The Ethernet interface then works without further intervention from the host system. The interface detects the beginning of packets, performs address checking, moves data and status to the dual-ported memory, maintains error counters, and provides an interrupt signal (Figure 3-5) to notify the host of the received packet(s).

3.6 CTI Bus INTERFACE

The CTI Bus interface (Figure 3-6) is a slave interface between the CTI Bus and the rest of the DECNA option module. The CTI Bus provides the bus transceivers, registers, control circuitry, and decoding logic needed to communicate with the Professional 300 series system module.

NOTE

Refer to the Professional 300 Series Technical Manual Volume 1 for a description of the Professional 300 Series system module.

The CTI Bus interface includes the following components.

Bus transceivers
Bus command register
Control circuitry
Memory read address register
Base address comparator
Memory access register
Control register
Option ROM
Address ROM
ROM address logic

The rest of Paragraph 3.6 describes these circuits to a functional block level. All block diagrams and signal descriptions in this section refer to *DECNA Field Maintenance Print Set* (MP 5415987-0-1).

3.6.1 Bus Transceivers, Bus Command Register, and Control Circuitry

Figure 3-7 shows the bus transceivers, bus command register, and control circuitry. These circuits enable read/write operations through the host system option bus. Paragraphs 3.6.1.1 through 3.6.1.7 describe read/write bus cycle timing and circuits. See Table 3-1 for signal descriptions.

3.6.1.1 Read/Write – Read/write operations occur in two distinct forms: memory access and I/O page access.

Memory access is a direct link of data address lines 0 through 16 (DAL 0–16) to the dual-ported memory.

I/O page access provides access to CTI Bus interface read/write registers via the uppermost 4-kilobyte segment of the host computer's addressing capability. Only the system module can gain access to the DECNA option module. The DECNA option module cannot communicate with other option modules through I/O page. The host computer allows the address of the DECNA option module in the I/O page to be assigned by the host system when the module is installed. The slot in which the option module is installed determines the address of the option. I/O references are decoded by the system module and a unique slot select (SS) signal is wired to the DECNA option module through the bus. The DECNA option module uses the slot select signal to determine if it is being accessed. Refer to the Professional 300 Series Technical Manual Volume 1 for the DECNA option module addressing range.

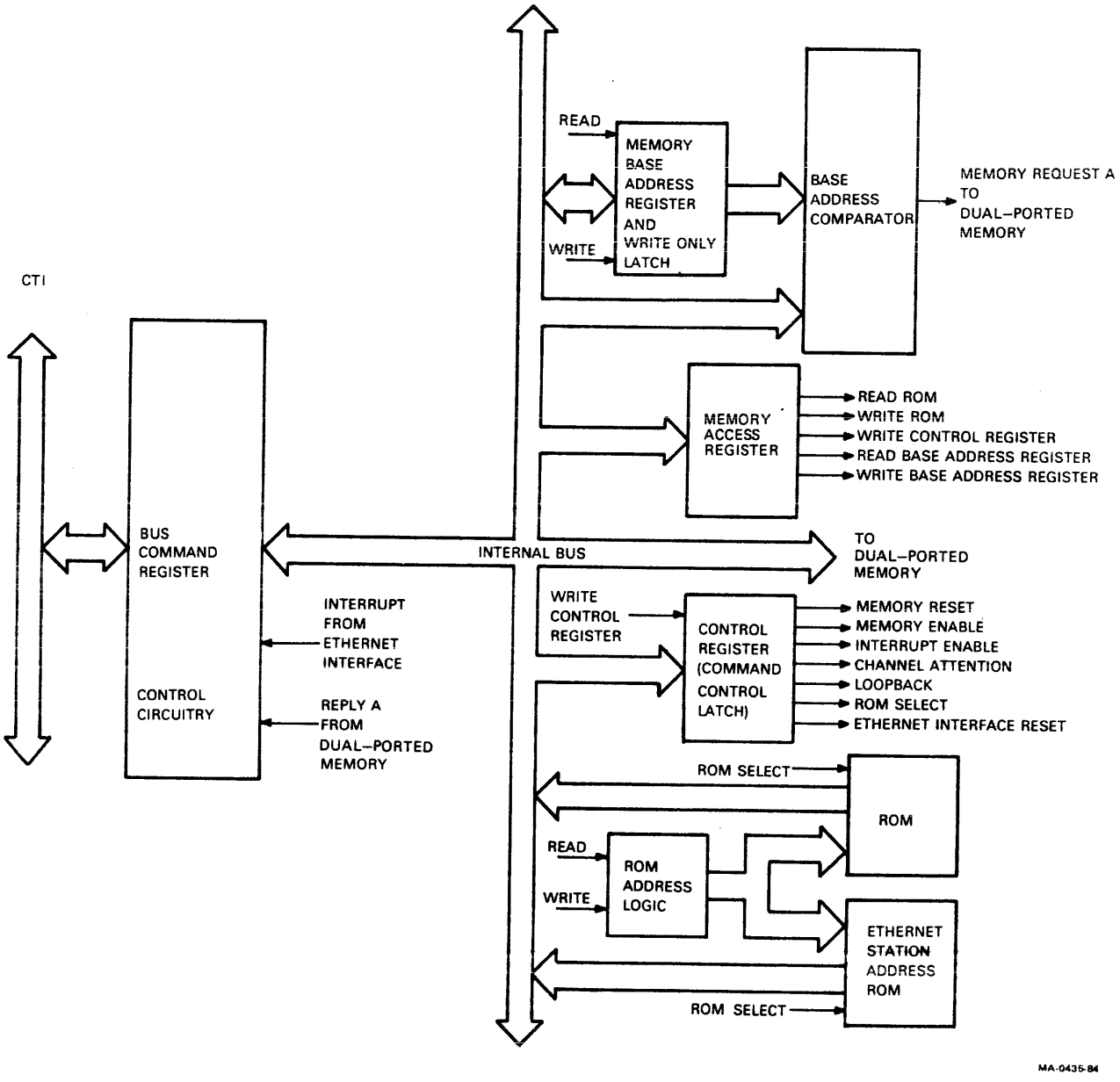


Figure 3-6 CTI Bus Interface

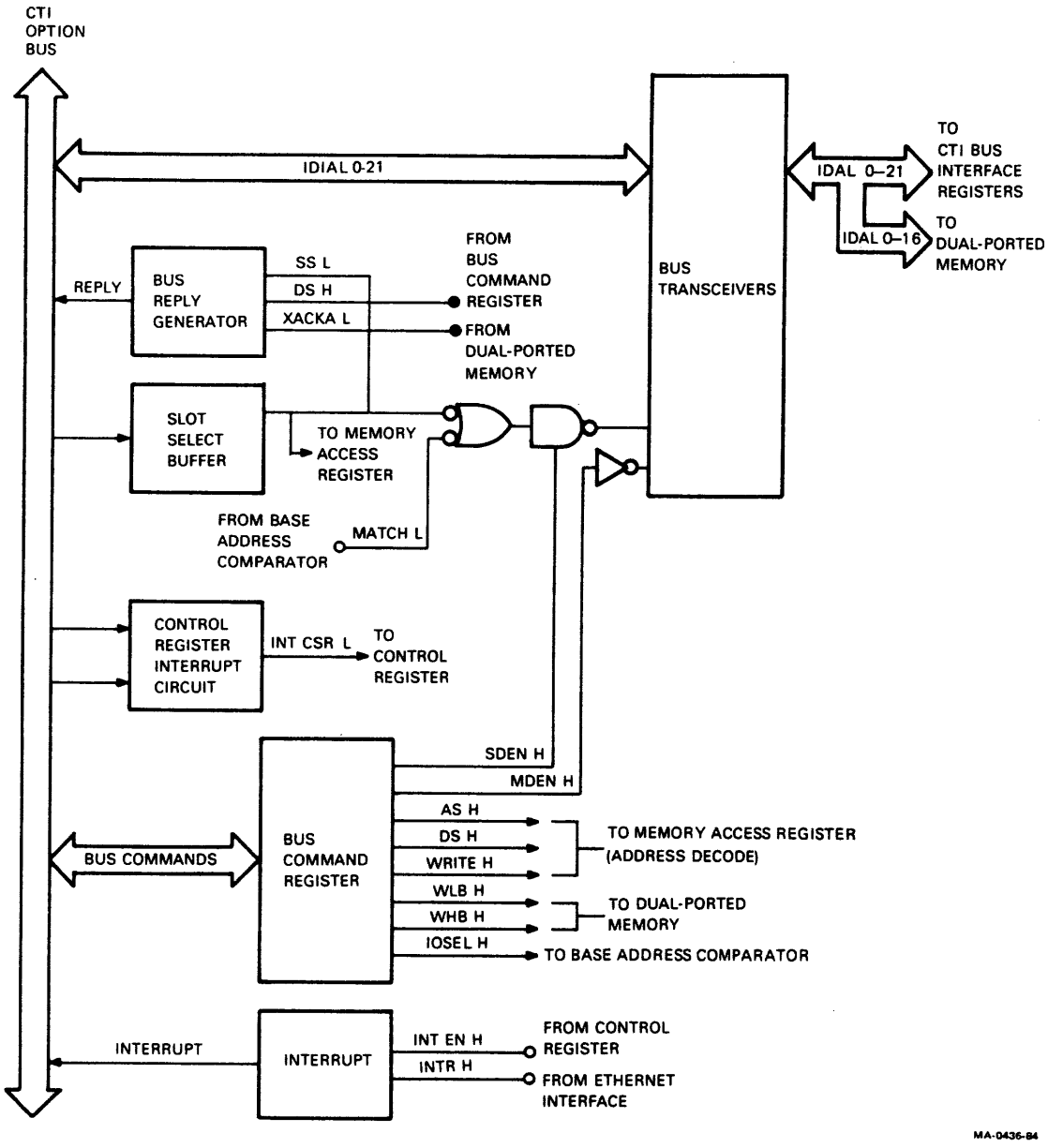


Figure 3-7 Bus Transceivers, Bus Command Registers, and Control Circuitry

Table 3-1 Bus Transceivers, Bus Command Register, and Control Circuitry Signal Description

Mnemonic	Signal Name	Active State (True)	Description
SDEN	Slave data Enable	H	SDEN is bus command register output. It enables bus transceivers to send data to the host system when SS L or MATCH L are true.
MATCH	Match low	L	MATCH is base address comparator output. It enables bus transceivers to send data to the host system.
MDEN	Master data enable	H	MDEN is bus command register output. It enables bus transceivers to receive address or data from the host system.
AS	Address strobe	H	AS is bus command register output. It enables address data latching from the host system into the memory access register.
DS	Data strobe	H	DS is bus command register output. It enables data transfer between the registers, memory, and host system.
WRITE	Write	H	WRITE is bus command register output. It enables the host processor to write words to the DECNA option module.
WLB	Write low byte	H	WLB is bus command register output. It enables the host processor to write low bytes to the DECNA memory.
WHB	Write high byte	H	WHB is bus command register output. It enables the host processor to write high bytes to the DECNA memory.

Table 3-1 Bus Transceivers, Bus Command Register, and Control Circuitry Signal Description (Cont)

Mnemonic	Signal Name	Active State (True)	Description
IOSEL	I/O select	H	IOSEL is bus command register output to the base address comparator. It is asserted by the host processor when accessing a location in the I/Opage of the address space. IOSEL disables access to the dual-ported memory.
SS	Slot select	H	SS enables the host processor to gain access to the DECNA registers. It is also used with XACKA L and DS H to generate a bus reply (RPLY L).
INT EN	Interrupt enable	H	INT EN is control register output. It gates the interrupt signal (INTR H) from the Ethernet interface to the host processor (BIRQA L).
INTR	Interrupt	H	INTR is Ethernet interface output gated by INT EN H to the host processor to signal the end of an operation.

3.6.1.2 Bus Transceivers – The bus transceivers (Figure 3-7) consist of buffers that provide an interface between the CTI Bus and the DECNA internal multiplex bus. In combination, the buffers drive and receive 22 data address lines (0 through 21) including 16 bits of data per byte to the dual-ported memory. See Table 3-1 for signal descriptions.

3.6.1.3 Bus Command Register – The bus command register (Figure 3-7) transfers bus commands to the DECNA option module bus transceivers, memory access register, base address comparator, bus reply generator, and dual-ported memory. See Table 3-1 for signal descriptions.

3.6.1.4 Slot Select Buffer – The slot select buffer (Figure 3-7) buffers the slot select signal (SS L) from the CTI Bus. The host system module asserts SS L while the address is being generated on the bus. SS L is true on the bus before the assertion of the address strobe signal (AS H). This allows SS L to be used in address decoding that occurs on the DECNA option module. See Table 3-1 for signal descriptions.

3.6.1.5 Bus Reply Generator – The bus reply generator (Figure 3-7) generates a reply signal for the host computer whenever the host computer gains access to the dual-ported memory via memory access or the DECNA read/write registers via the I/O page. See Table 3-1 for signal descriptions.

3.6.1.6 Control Register Interrupt Circuit – The control register interrupt circuit (Figure 3-7) uses signals from the system module to generate an initialize signal (INIT CSR L) that clears the control register. See Table 3-1 for signal descriptions.

3.6.1.7 Host Interrupt Circuit – The host interrupt circuit (Figure 3-7) gates an interrupt enable signal (INT EN H) from the control register with an interrupt signal (INTR H) from the Ethernet interface. The host interrupt circuit's output puts BIRQA L on the CTI Bus to notify the host computer that the Ethernet interface has completed an operation. See Table 3-1 for signal descriptions.

3.6.2 Memory Access Register

The memory access register (Figure 3-8) is an address decoder that provides read and/or write commands to the ROM address logic, control register, and base address comparator. See Table 3-2 for signal descriptions.

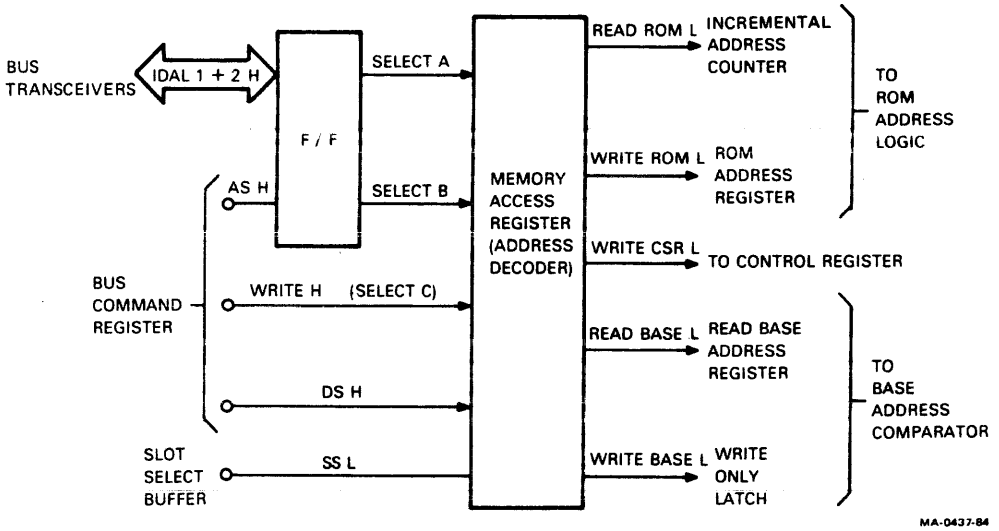


Figure 3-8 Memory Access Register

Table 3-2 Memory Access Register Signal Description

Mnemonic	Signal Name	Active State (True)	Description
AS	Address strobe	H	AS is bus command register output. It latches the input state of the flip-flops.
WRITE	Write	H	WRITE is bus command register output. It selects a write operation when true, and a read operation when not true.
DS	Data strobe	H	DS is bus command register output. It enables data decoding when SS L is true.
SS	Slot select	L	SS is slot select buffer output. It enables address decoding when DS H is true.
READ ROM	Read ROM	L	READ ROM is output to the ROM address logic. It enables the contents of the option ROM or Ethernet station address ROM to be read by the host system.
WRITE ROM	Write ROM	L	WRITE ROM is output to the ROM address logic. It enables the host system to reset the ROM pointer to zero.
WRITE CSR	Write control register	L	WRITE CSR is output to the control register. It enables a write to the control register.
READ BASE	Read base address	L	READ BASE is output to the base address comparator. It enables the host system to read the contents of the base address register.
WRITE BASE	Write base address	L	WRITE BASE is output to the base address comparator. It enables the host system to write the contents of the base address register.

3.6.3 Control Register (Command Control Latch)

The control register (Figure 3-9) is a software-accessible, write-only, byte-wide, command control latch. It controls the DECNA option module's main functions. The control register is accessed via WRITE CSR L from the memory access register and cleared (reset) by INIT CSR L from the control circuit. This register uses IDAL 0 through 7 to perform the following functions.

Reset memory

Enable dual-ported memory

Enable interrupts

Sends a channel attention (CA) signal to the Ethernet interface

Enable the Ethernet interface loopback

Select option ROM (self-test) or the address ROM

Reset the Ethernet interface

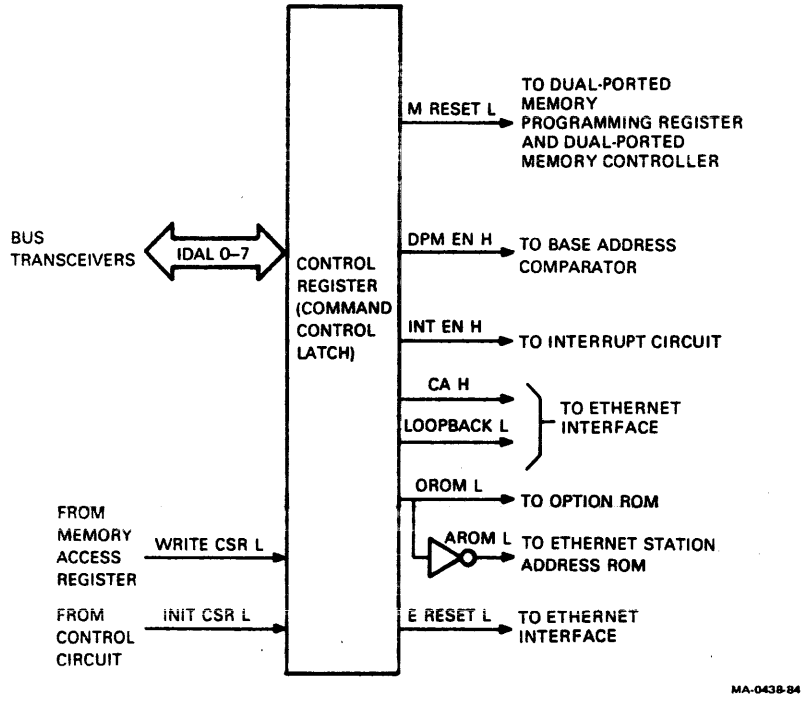


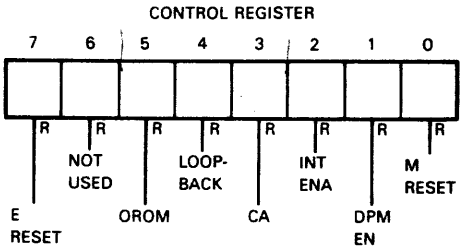
Figure 3-9 Control Register (Command Control Latch)

Figure 3-10 shows the control register signals and bit values.

At system power-up, reset, or bus reset, INIT CSR L is true and all seven bits in this register are set to 0, which resets the DECNA option module.

NOTE
The state of M RESET (bit 0) or E RESET (bit 7) does not affect the other control register bits.

See Table 3-3 for signal descriptions.



BIT VALUES		
BIT 0	0	RESET MEMORY
	1	NOT RESET MEMORY
BIT 1	0	DISABLE DUAL-PORTED MEMORY
	1	ENABLE DUAL-PORTED MEMORY
BIT 2	0	DISABLE INTERRUPTS
	1	ENABLE INTERRUPTS
BIT 3	0-1-0	SENDS CHANNEL ATTENTION TO THE ETHERNET INTERFACE
BIT 4	0	ENABLE ETHERNET INTERFACE LOOPBACK
	1	DISABLE ETHERNET INTERFACE LOOPBACK
BIT 5	0	SELECT OPTION ROM
	1	SELECT ADDRESS ROM
BIT 6	–	RESERVED
BIT 7	0	RESET ETHERNET INTERFACE
	1	NOT RESET ETHERNET INTERFACE

MA-0439-84

Figure 3-10 Control Register Bit Values

Table 3-3 **Control Register Signal Description**

Mnemonic	Signal Name	Active State (True)	Description
WRITE CSR	Write control register	L	WRITE CSR is memory access register output. It enables a write to the control register.
INIT CSR	Initiate (clear) control register	L	INIT CSR is memory access register output. It resets the control register.
M RESET	Memory reset	L	M RESET is ouput to the dual-ported memory. It resets the dual-ported memory only.
DPM EN	Dual-ported memory enable	H	DPM EN is output to base address comparator. It enables bus access to the dual-ported memory.
INT ENA	Interrupt enable	H	INT ENA is output to the BIRQA interrupt circuit. It gates the interrupt signal from the Ethernet interface to the host system.
CA	Channel attention	H	CA is output to the Ethernet interface. It alerts the Ethernet interface to process the next command.
LOOPBACK	Loopback	L	LOOPBACK is output to the Ethernet interface. It places the Ethernet interface in loopback mode.
OROM	Option ROM select	L	OROM is output to the option ROM. It selects the option ROM for a read by the host system.
AROM	Address ROM select	L	AROM is output to the address ROM. It selects the address ROM for a read by the host system.

3.6.4 Memory Base Address Register and Write-Only Latch, and Base Address Comparator

The memory base address register and write-only latch (Figure 3-11) is a software-accessible read/write register. It stores the high order address bits of the memory page. The base address comparator (Figure 3-12) compares the high order address bits in the base address register with the high order address bits from memory access (IDAL 17–21), which are coming in on the bus. If the bits match, the 128K block of dual-ported memory is accessible. The lower five bits of the dual-ported memory base address register determine the five high order address bits for the location of the 64K word dual-ported memory in the host system address space.

The high order bit (bit 7) of the base address register is a read-only bit that is set by the Ethernet interface. It indicates an error condition for a previously transmitted packet. This bit indicates that the no carrier sense signal (NCRS H) was present for an entire transmission. Once set, this error bit remains set until the base address register is read. See Table 3-4 for signal descriptions.

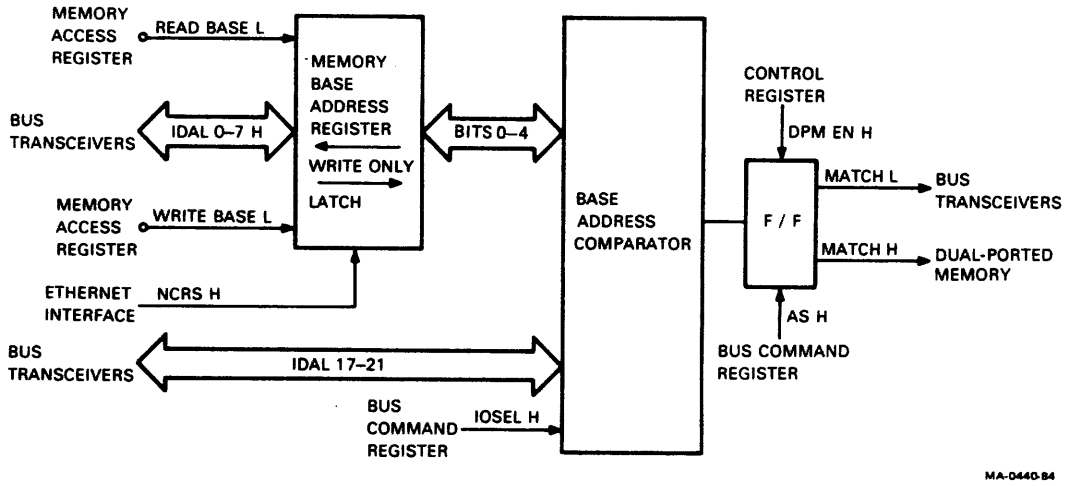


Figure 3-11 Memory Read Base Address Register and Write-Only Latch, and Base Address Comparator

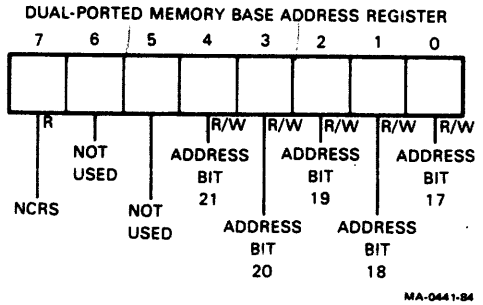


Figure 3-12 Dual-Ported Memory Base Address Register Bit Value

Table 3-4 Dual-Ported Memory Read Base Address Register, Write-Only Latch, and Base Address Comparator Signal Description

Mnemonic	Signal Name	Active State (True)	Description
READ BASE	Read base	L	READ BASE is memory access register output. It enables the host system to read the contents of the base address register.
WRITE BASE	Write base	L	WRITE EASE is memory access register output. It enables the host system to write the contents of the base address register.
NCRS	No carrier	H	NCRS is Ethernet interface output. It indicates an error condition on a previous transmission attempt.
IOSEL	I/O select	H	IOSEL is bus command register output. It disables the base address comparator.
DPM EN	Dual-ported memory enable	H	DPM EN is control register output. It enables the flip-flop operation to enable access to the dual-ported memory.
AS	Address strobe	H	AS is bus command register output. It changes the state of the flip-flop to generate MATCH H.
MATCH	Match low	L	MATCH L is output to the bus transceivers. It enables data transmission to the host system.
	Match high	H	MATCH H is output to the dual-ported memory. It enables data transmission from the host system to the dual-ported memory.

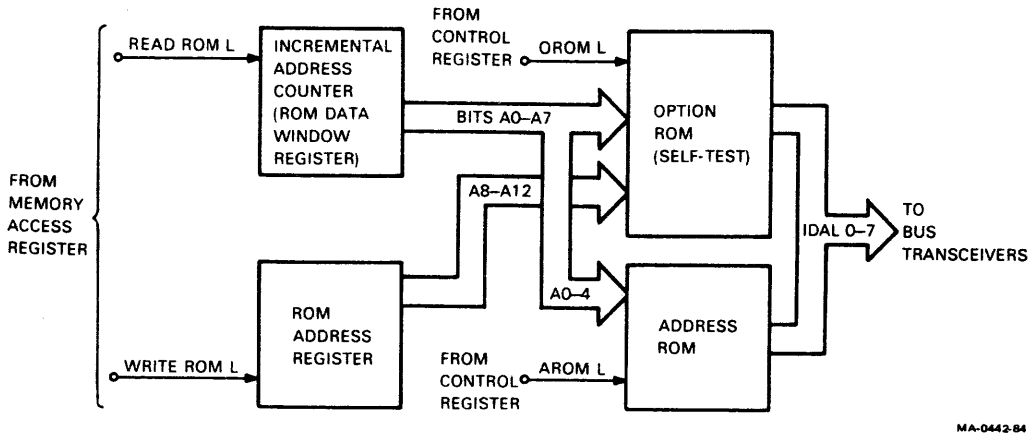


Figure 3-13 Option ROM, Address ROM and ROM Address Logic

3.6.5 Option ROM, Address ROM, and ROM Address Logic

This circuitry (Figure 3-13) provides access to the ROM for down-line loading boot code and diagnostics (option ROM). It also stores the unique Ethernet address of this particular DECNA option module (Ethernet station address ROM).

3.6.5.1 Option ROM – The option ROM (8 kilobytes) provides for down-line loading and storage of bootstrap code and diagnostic code for the DECNA option module. This code is host system processor code that can be read by the host through the ROM data window register, assembled into words in memory, and executed. The bootstrap procedure conforms to the Professional 300 Series boot specification. See Table 3-5 for signal descriptions.

3.6.5.2 Address ROM – The address ROM (32-byte PROM) stores the unique physical address (Ethernet station address) of this particular DECNA option module. The address is software readable. The first six bytes contain the unique address and are accessible via the ROM data window register. The next two bytes contain a checksum value for PROM contents and are also accessible through the ROM data window register. Checksum is calculated according to Ethernet Specification Version 2.0. See Table 3-5 for signal descriptions.

3.6.5.3 ROM Address Logic – ROM address logic consists of the ROM data window register and ROM address register. See Table 3-5 for signal descriptions.

The *ROM data window register* is a read-only, byte-wide register. In response to successive read operations, it provides sequential access to bytes of data stored in the option ROM or Ethernet station address ROM. This register increments by one for each read operation. Either the option ROM or Ethernet station address ROM can be selected for access by a bit (OROM L/AROM L) from the control Register. See Table 3-5 for signal descriptions.

The *ROM address register* is a software-accessible, write-only register. When WRITE ROM L is asserted, the ROM address logic resets and points to the first location of the option ROM or the Ethernet station address ROM. See Table 3-5 for signal descriptions.

Table 3-5 Option ROM, Address ROM, and ROM Address Logic Signal Description

Mnemonic	Signal Name	Active State (True)	Description
READ ROM	Read ROM	L	READ ROM is memory access register output. It enables the host system to read the contents of the option ROM or address ROM, depending on which ROM is selected (OROM L or AROM L). Sequential reads increment the ROM address pointer.
WRITE ROM	Write ROM	L	WRITE ROM is memory access register output. It enables the host system to write to the option ROM if the option ROM is selected (OROM L).
OROM	Option ROM select	L	OROM is control register output. It selects the option ROM for a read by the host system.
AROM	Address ROM select	L	AROM is control register output. It selects the address ROM for a read by the host system.

3.7 DUAL-PORTED MEMORY

The dual-ported memory (Figure 3-14) stores host instructions, data, and Ethernet controller commands. The host system gains access to the dual-ported memory through the CTI Bus interface and port A (asynchronous). The Ethernet accesses the dual-ported memory through the Ethernet interface and port B (synchronous). Port arbitration is accomplished as follows. The port most recently used for memory access has access priority in case both ports try to gain access at the same time.

The dual-ported memory includes the following components.

- 64K × 16 dynamic ram
- CTI write network interface (NI) write selector
- Dual-ported memory controller
- CTI read/write decoder
- Port a (CTI data-to-memory buffer, data latch, and address latch)
- Port B (NI data-to-memory buffer, data latch, and address latch)

The rest of Paragraph 3.7 describes these circuits to a functional block level. All block diagrams and signal descriptions in this section are derived from the *DECNA Field Maintenance Print Set* (MP-01895-01).

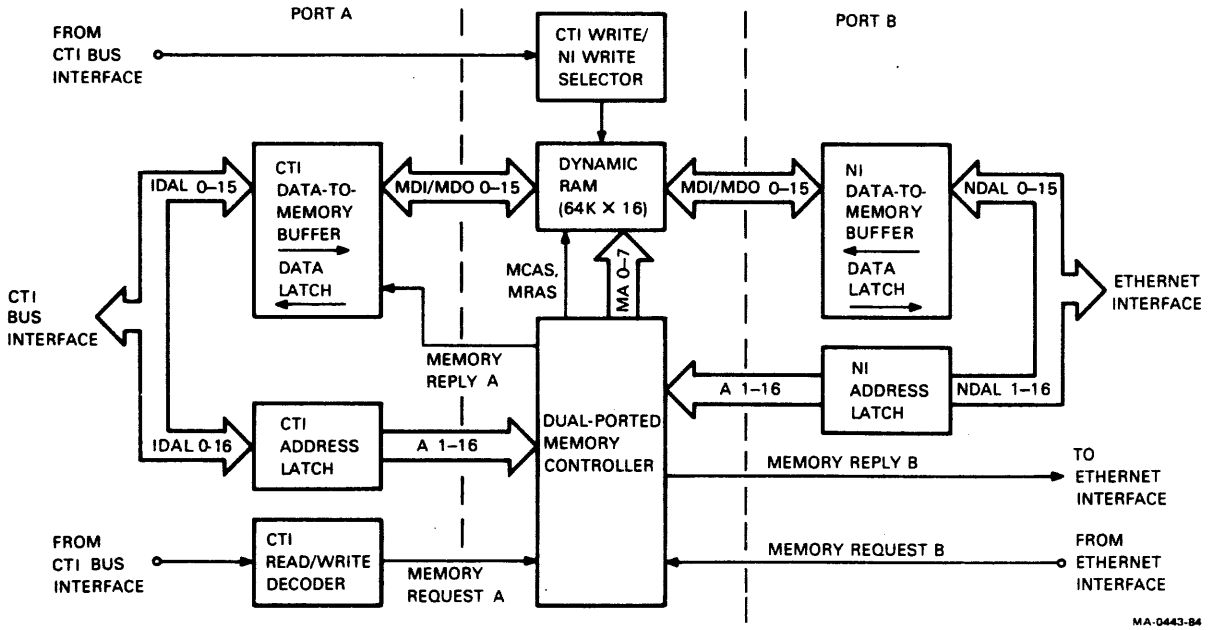


Figure 3-14 Dual-Ported Memory

3.7.1 Dynamic RAM

The dynamic RAM (Figure 3-15) is a 64K × 16 (128 kilobyte) array divided into two banks: a low-byte bank and high-byte bank. There are 16 memory data in (MDI 0–15) and 16 memory data out (MDO 0–15) lines to provide access to and from memory via port A or port B. Eight memory address (MA 0–7) lines provide row and column addressing from the dual-ported memory controller. Four memory row address strobe (MRAS 0–3) and four memory column address strobe (MCAS 0–3) signals from the dual-ported memory controller latch the row and column address present on the MA 0–7 lines. The CTI write/NI write selector selects a low and/or high byte. See Table 3-6 for signal descriptions.

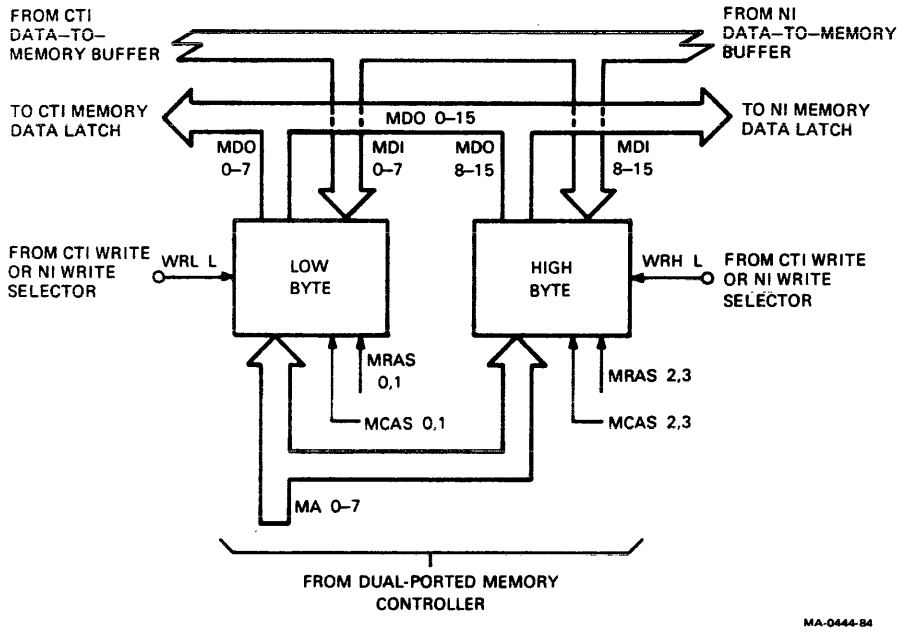


Figure 3-15 Dynamic RAM

Table 3-6 Dynamic RAM Signal Description

Mnemonic	Signal Name	Active State (True)	Description
MDI 0–15	Memory data input	H	MDI 0–15 are memory data input lines to RAM from port A or port B.
MDO 0–15	Memory data output	H	MDO 0–15 are memory data output lines from RAM to port A or port B.
MA 0–7	Memory address	H	MA 0–7 are dual-ported memory controller output. These memory address lines provide the row and column address.
MRAS 0–3	Memory row address strobe	L	MRAS 0–3 are dual-ported memory controller outputs. They latch the row address present on MA 0–7.
MCAS 0–3	Memory column address strobe	L	MCAS 0–3 are dual-ported memory controller outputs. They latch the column address present on MA 0–7 lines.
WRL	Write low byte	L	WRL is CTI write/NI write selector output. It writes a low byte.
WRH	Write high byte	L	WRH is CTI write/NI write selector output. It writes a high byte.

3.7.2 CTI Write/NI Write Selector

The CTI write/NI write selector (Figure 3-16) is a decoder that selects which port can gain access to memory for a write operation. When PSEL is true, the decoder outputs are determined by the states of the RWHB and RWLB inputs. When PSEL is not true, both decoder outputs are low. See Table 3-7 for signal descriptions.

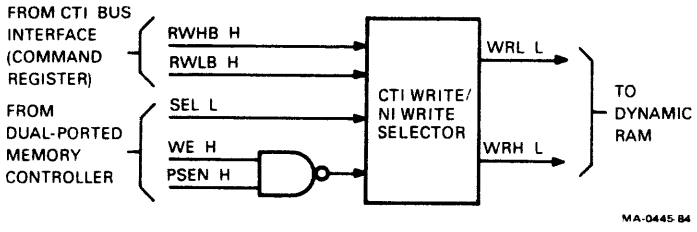


Figure 3-16 CTI Write/NI Write Selection

Table 3-7 CTI Write/NI Write Selector Signal Description

Mnemonic	Signal Name	Active State (True)	Description
RWHB	Read/write high byte	H	RWHB is CTI Bus interface command register output. It enables the host processor to write high bytes to the DECNA memory.
RWLB	Read/write low byte	H	RWLB is CTI Bus interface command register output. It enables the processor to write low bytes to the DECNA memory.
PSEL	Port select	L	PSEL is dual-ported memory controller output. It selects a port for the data transfer. When true, PSEL selects port A; when not true, it selects port B.
WE	Write enable	H	WE is dual-ported memory controller output. It enables a write operation when PSEN is true.
PSEN	Port select enable	H	PSEN is dual-ported memory controller output. It provides contention-free port exchange. When PSEN is true, PSEL cannot change state; when PSEN is not true, PSEL can change state.
WRL	Write low byte	L	WRL is output to the dynamic RAM low byte. It enables a write low byte operation.
WRH	Write high byte	L	WRH is ouptut to the dynamic RAM high byte. It enables a write high byte operation.

3.7.3 Dual-Ported Memory Controller

The dual-ported memory controller (Figure 3-17) is the heart of the dual-ported memory. It is a microcomputer that is programmed at power-up and driven by an 8 MHz clock. The dual-ported memory controller provides the necessary signals to address, refresh, and directly drive the dynamic RAM. It also provides arbitration circuitry to support dual-port access to the dynamic RAM. The controller controls asynchronous operation on port A and synchronous operation on port B. A programming register with a M RESET signal from the CTI Bus interface control register resets the controller chip and memory. See Table 3-8 for signal descriptions.

3.7.3.1 Clock and TTL-to-MOS Level Converter – The 8 MHz clock and TTL-to-MOS level converter provides the timing circuit that drives the dual-ported memory controller chip (8207). The 8 MHz is derived from a flip-flop that divides the output of a 16 MHz crystal by two. The 8 MHz signal is fed to a TTL-TO-MOS level converter, which generates the MCLK signal to drive the controller chip.

3.7.3.2 8207 Programming Register – The 8207 programming register is a serial-shift register that allows various designer-selectable options in the 8207 chip. When M RESET is asserted, the register is loaded with octal value 000176. When M RESET is deasserted, the contents of this register is loaded into the dual-ported memory controller chip via the PDI signal. The MUX signal provides a clock for shifting the register contents.

3.7.3.3 Arbiter Circuit – The arbiter circuit is a multiplexer that uses the 8207 chip MUX signal to provide enable signals to the port A and port B address latches.

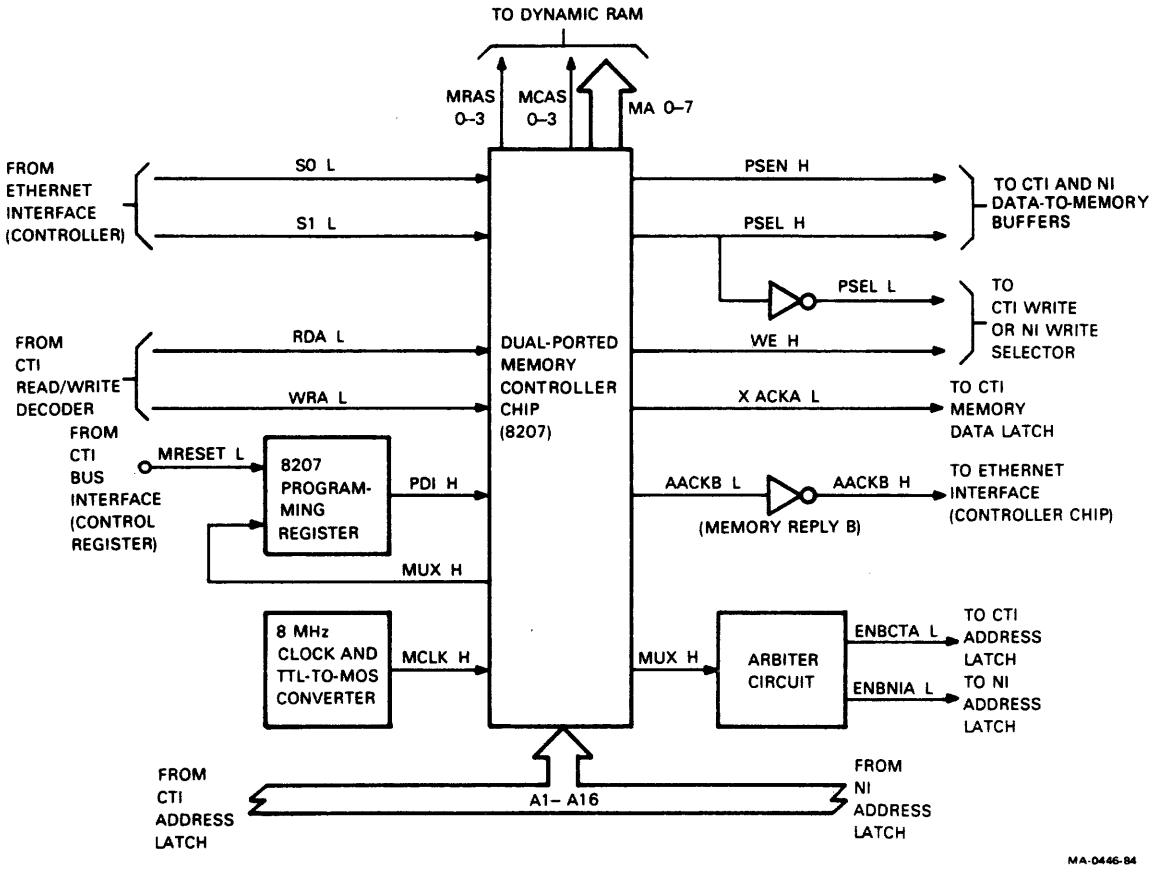


Figure 3-17 Dual-Ported Memory Controller

Table 3-8 Dual-Ported Memory Controller Signal Description

Mnemonic	Signal Name	Active State (True)	Description
A1–A16	Address low/high	H	A1–A8 provide low-order address inputs to generate a row address A9–A16 provide high-order address inputs to generate a column address
MA 0–7	Memory address	H	MA 0–7 are output to the dynamic RAM. They provide the row and column addresses of the selected port to the dynamic RAM.
MRAS 0–3	Memory row address strobe	H	MRAS 0–3 are output to the dynamic RAM. They latch the row address present on MA 0–7.
MCAS 0–3	Memory column address strobe	H	MCAS 0–3 are output to the dynamic RAM. They latch the column address present on MA 0–7.
M RESET	Memory reset	L	M RESET is CTI Bus interface control register output. It loads octal value 000176 into the programming register and resets the controller chip.
MUX	Multiplexor control	H	MUX provides serial-shifting of the value in the programming register during the initial programming phase after M RESET. During normal operation, it drives the arbiter circuit.
PDI	Program data input	H	PDI provides the initial programming value to the 8207 chip.

Table 3-8 Dual-Ported Memory Controller Signal Description (Cont)

Mnemonic	Signal Name	Active State (True)	Description
S0	Status 0	L	S0 is Ethernet interface controller output. It provides the write memory request command input for port B.
S1	Status 1	L	S1 is Ethernet interface controller output. It provides a read memory request command input for port B.
RDA	Read for port A	L	RDA is CTI read/write decoder output. It provides a read memory request command for port A.
WRA	Write for port A	L	WRA is CTI read/write decoder output. It provides a write memory request command for port A.
PSEN	Port select enable	H	PSEN is output to the CTI or NI data-to-memory buffers (port A or B). With PSEL, PSEN provides contention-free port exchange. When PSEN is not true, PSEL can change its state.
PSEL	Port select	H/L	PSEL is output to the CTI and NI data-to-memory buffers and the CTI write/NI write selector. It selects port A or B.
WE	Write enable	H	WE is output to the CTI write/NI write selector. It provides a write enable for the write operation.

Table 3-8 Dual-Ported Memory Controller Signal Description (Cont)

Mnemonic	Signal Name	Active State (True)	Description
XACKA	Transfer acknowledge port A	L	XACKA is output to the port A memory data latch. It enables the memory data latch and indicates that data on the bus is valid during a read cycle or can be removed from the bus during a write cycle via port A.
AACKB	Advanced acknowledge port B	H	AACKB is output to the Ethernet controller. It indicates that the processor can continue processing and that data will be available when required.
ENBCTA	Enable port A address	L	ENBCTA enables the port A address latch.
ENBNIA	Enable port B address	L	ENBNIA enables the port B address latch.
M CLOCK	Memory clock	H	M CLOCK provides timing for the dual-ported memory controller and the Ethernet interface controller.

3.7.4 CTI Read/Write Decoder

The CTI read/write decoder (Figure 3-18) decodes, for the dual-ported memory controller, which type of operation (read or write) that the host system is trying to perform. The decoder is gated by MATCH H and RDS H signals from the CTI Bus interface. When WRITE H from the CTI Bus interface command register is true, the decoder output WRA L is true, which specifies a write operation. When WRITE H is not true, the decoder output RDA L is true, which specifies a read operation. See Table 3-9 for signal descriptions.

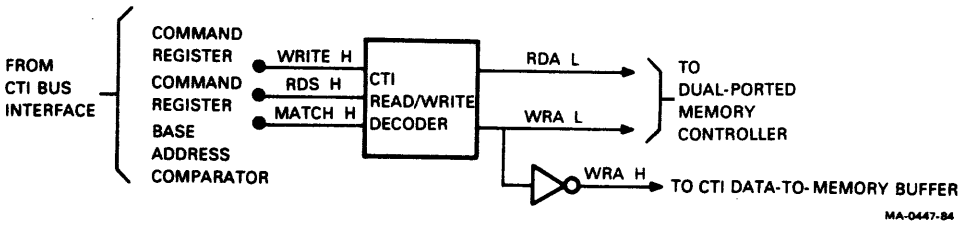


Figure 3-18 CTI Read/Write Decoder

Table 3-9 CTI Read/Write Decoder Signal Description

Mnemonic	Signal Name	Active State (True)	Description
WRITE	Write	H	WRITE is CTI Bus interface command register output. When true, WRITE specifies a write operation; when not true, WRITE specifies a read operation.
DS	Data strobe	H	DS is CTI Bus interface command register output. It enables the CTI read/write decoder.
MATCH	Match	H	MATCH is CTI Bus interface address comparator output. It enables the CTI read/write decoder.
RDA	Read port A	L	RDA is output to the dual-ported memory controller. It provides a read memory request command for port A.
WRA	Write port A	L	WRA L is output to the dual-ported memory controller. It provides a write memory request command for port A.
		H	WRA H is output to the port A data-to-memory buffer. It enables a host system write-to-memory operation.

3.7.5 Port A (CTI Data-to-Memory Buffer, Data Latch, and Address Latch)

Port A (Figure 3-19) consists primarily of a CTI data-to-memory buffer, a CTI memory data latch, and a CTI address latch. The host system, via the CTI Bus interface, accesses DECNA memory through port A. Communication between the host system and DECNA memory through port A is asynchronous. See Table 3-10 for signal descriptions.

3.7.5.1 CTI Data-to-Memory Buffer – The CTI data-to-memory buffer, when enabled by PSEL H, PSEN H, and WRA H, pass signals on internal data address lines 0–15 from the host system to the dynamic RAM via memory data input lines 0–15.

3.7.5.2 CTI Memory Data Latch – The CTI memory data latch, when enabled by XACKA L AND RDA L, pass signals on memory data output lines 0–15 from the dynamic RAM to the host processor via internal data address lines 0–15.

3.7.5.3 CTI Address Latch – The CTI address latch, when enabled by AS H and ENBCTA L, pass signals on internal data address lines 1–16 from the host system to the dual-ported memory controller via address lines 1–16.

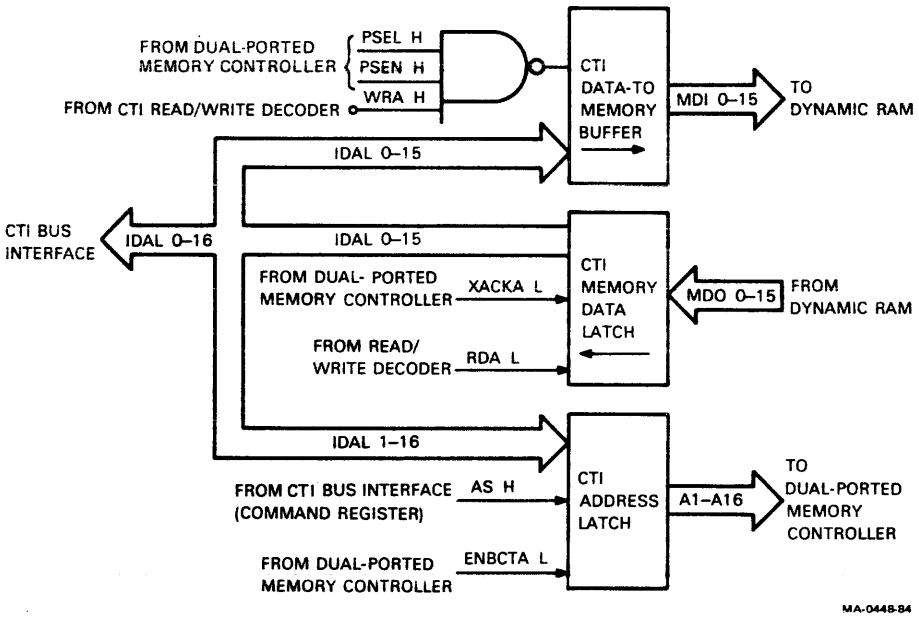


Figure 3-19 Port A

Table 3-10 Port A (CTI Data-to-Memory Buffer, Data Latch, and Address Latch) Signal Description

Mnemonic	Signal Name	Active State (True)	Description
IDAL 0–16	Internal data address lines	H	IDAL 0–16 are internal data address lines.
MDI 0–15	Memory data input	H	MDI 0–15 output to the dynamic RAM. They provide the memory data to the dynamic RAM.
MDO 0–15	Memory data output	H	MDO 0–15 are dynamic RAM output. They provide the memory data from the dynamic RAM.
A1–A16	Address low/high	H	A1–A16 are output to the dual-ported memory controller. A1–A8 provide the lower order address. A9–A16 provide the high order address.
PSEL	Port select	H	PSEL is dual-ported memory controller output. When true, PSEL selects port A; when not true, PSEL selects port B.
PSEN	Port select enable	H	PSEN is dual-ported memory controller output. It provides contention-free port exchange. When PSEN is not true, PSEL cannot change state; when PSEN is not true, PSEL can change state.
WRA	Write port A	H	WRA is CTI read/write decoder output. It is used with PSEL H and PSEN H to enable the data-to-memory buffer.
XACKA	Transfer acknowledge port A	L	XACKA is dual-ported memory controller output. It indicates that data on bus are valid during a read cycle, or that data can be removed from the bus during a write cycle.

Table 3-10 Port A (CTI Data-to-Memory Buffer, Data Latch, and Address Latch) Signal Description (Cont)

Mnemonic	Signal Name	Active State (True)	Description
RDA	Read port A	L	RDA is CTI read/write decoder output. It enables the memory data latch.
AS	Address strobe	H	AS is CTI Bus interface command register ouput. It enables latching of address data from the host system into the address latch.
ENBCTA	Enable CTI address	L	ENBCTA is dual-ported memory controller output. It enables the CTI address on A1–A16.

3.7.6 Port B (Network Interface Data-to-Memory Buffer, Memory Data Latch, and Address Latch)

Port B (Figure 3-20) consists primarily of a network interface (NI) data-to-memory buffer, an NI memory data latch, and an NI address latch. The Ethernet, via the Ethernet interface, accesses the DECNA memory through port B. Communication between the Ethernet and DECNA memory through port B is synchronous. See Table 3-11 for signal descriptions.

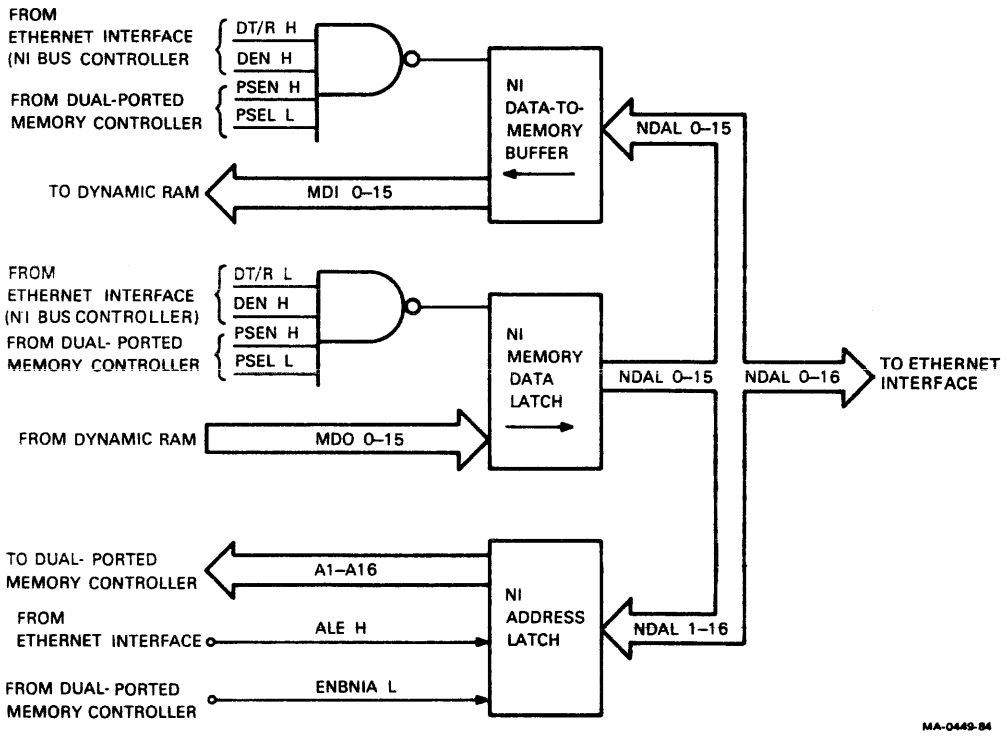


Figure 3-20 Port B

Table 3-11 Port B (NI Data-to-Memory Buffer, Data Latch, and Address Latch) Signal Description

Mnemonic	Signal Name	Active State (True)	Description
NDAL 0–16	Network data address lines	H	NDAL 0–16 are network data address lines.
MDI 0–15	Memory data input	H	MDI 0–15 are output to the dynamic RAM. They provide memory data to the dynamic RAM.
MDO 0–15	Memory data output	H	MDO 0–15 are dynamic RAM output. They provide memory data from the dynamic RAM.
A1–A16	Address low/high	H	A1–A16 are output to the dual-ported memory controller. A1–A8 provide the lower-order address. A9–A16 provide the higher-order address.
DT/R	Data transmit receive	H	DT/R H is Ethernet interface internal bus controller output. It establishes the direction of the data flow. When true (high), DT/R H enables data transmission from the Ethernet interface to memory.
		L	DT/R L is Ethernet interface internal bus controller output. It establishes the direction of the data flow. When true (low), DT/R L enables data transmission from memory to the Ethernet interface.
DEN	Data enable	H	DEN is Ethernet interface internal bus controller output. It enables data transfer between memory and the Ethernet interface.

Table 3-11 Port B (NI Data-to-Memory Buffer, Data Latch, and Address Latch) Signal Description (Cont)

Mnemonic	Signal Name	Active State (True)	Description
PSEN	Port select enable	H	PSEN is dual-ported memory controller output. It provides contention-free port exchange. When PSEN is true, PSEL cannot change state; when PSEN is not true, PSEL can change state.
PSEL	Port select	L	PSEL is dual-ported memory controller output. When true, PSEL selects port B; when not true, PSEL selects port A.
ALE	Address latch enable	H	ALE is Ethernet interface output. It strobes an address into the address latch. Latching occurs on the falling (high to low) transmission.

3.7.6.1 NI Data-to-Memory Buffer – The NI data-to-memory buffer, when enabled by DT/R, DEN H, PSEN H, and PSEL L, passes signals on network data address lines 0–15 from the Ethernet to the dynamic RAM via memory data input lines 0–15.

3.7.6.2 NI Memory Data Latch – The NI memory data latch, when enabled by DT/R, DEN H, PSEN H, and PSEL L, passes signals on the memory data output lines 0-15 from the dynamic RAM to the Ethernet via network data address lines 0–15.

3.7.6.3 NI Address Latch – The NI address latch, when enabled by ALE H and ENBNIA L, passes signals on the network data address lines 1–16 from the Ethernet to the dual-ported memory controller via address lines 1–16.

3.8 ETHERNET INTERFACE

The Ethernet interface (Figure 3-21) provides the Ethernet cable interface and handles the Ethernet data link layer protocol. The interface generates 10 Mbytes/s data rates, performs Manchester encoding/decoding of packet information, monitors channel access, and generally controls how the DECNA option module uses the link. The Ethernet interface includes the following major circuits.

Ethernet controller
Ethernet serial interface
Broadband compatibility circuit

The rest of Paragraph 3.8 describes these circuits to a functional block level. All block diagrams and signal descriptions in this section relate to *DECNA Field Maintenance Print Set* (MP-01895-01).

3.8.1 Ethernet Controller

The Ethernet controller (Figure 3-22) consists primarily of an Ethernet communications controller chip (82586) driven by an 8 MHz clock, a fail-safe time-out circuit, and an NI internal bus controller. Paragraph 3.8.1.1 through 3.8.1.4 describe these circuits. See Table 3-11 for signal descriptions.

3.8.1.1 Clock and TTL-to-MOS Level Converter – The 8 MHz clock and TTL-to-MOS level converter (Figure 3-22) provide the timing circuit that drives the Ethernet communications controller chip (82586). The 8 MHz is derived from a flip-flop that divides the output of a 16 MHz crystal by two. The 8 MHz signal that results is fed to the TTL-to-MOS level converter, which generates the MCLK signal to drive the controller chip. The TTL-to-MOS level converter also provides a TCLK signal to provide timing for the NI internal bus controller. See Table 3-11 for signal descriptions.

3.8.1.2 Ethernet Communications Controller Chip (82586) – The Ethernet communications controller chip (82586) (Figure 3-22) is a microcomputer that is programmed at system power-up. This controller chip handles the Ethernet data link layer protocol and generally controls how the DECNA option module uses the link. This chip is the controlling interface between the Ethernet serial interface, dual-ported memory, and CTI Bus interface.

During transmission, memory resident command blocks begin execution when the chip receives the channel attention signal (CA H) from the CTI Bus interface control register. A transition of CA from low to high to low instructs the controller chip to locate, read, and process the next command. The controller chip, after processing a transmit command, gains access to the serial link, moves the data from the dual-ported memory, forms the data into Ethernet-formatted packets, then transmits the data packets to the destination node. When transmission is complete (or an attempt is complete), the controller chip writes the transmit status into the dual-ported memory and asserts an interrupt signal (INTR H) to tell the host system to check transmit status.

To receive, the host system raises and lowers the channel attention signal (CA) after setting up the receive buffer areas and receive command blocks in the dual-ported memory. The controller chip then begins to process commands without further intervention from the host system. The chip detects the beginning of incoming packets, performs address checking, moves data and status to the dual-ported memory, maintains error counters, and asserts the interrupt signal (INTR H) to notify the host system of received packet(s).

See Table 3-12 for signal descriptions.

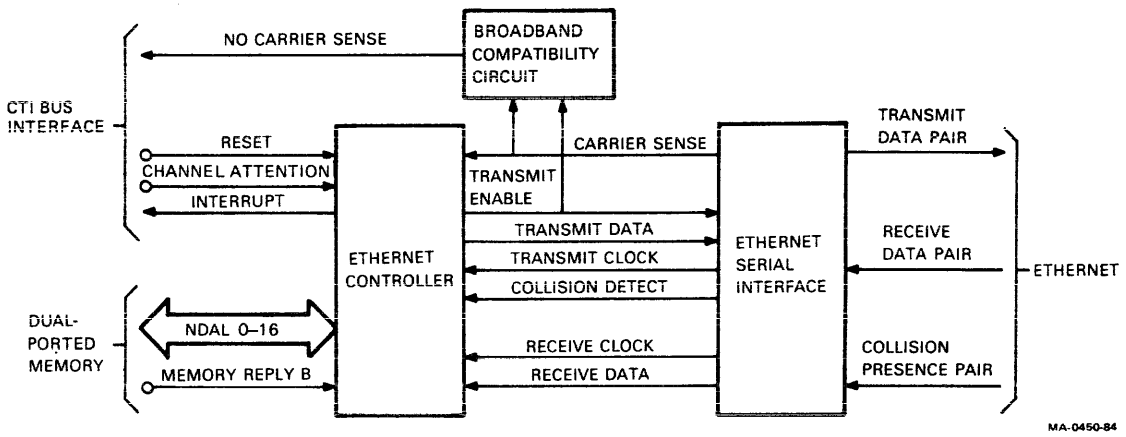


Figure 3-21 Ethernet Interface

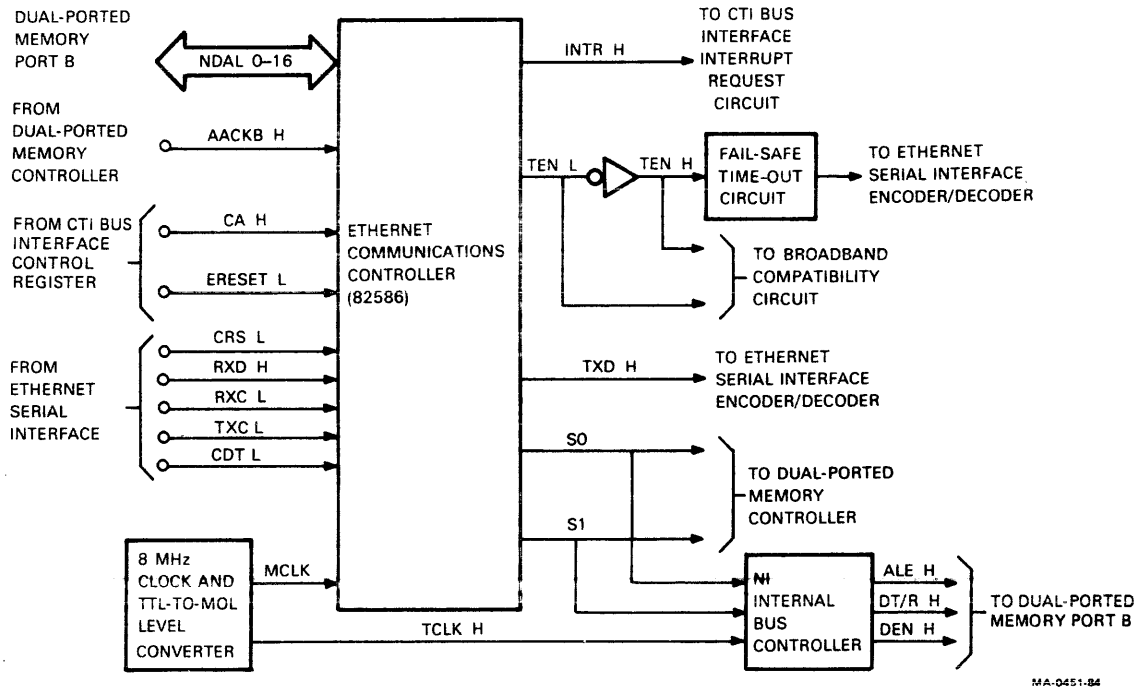


Figure 3-22 Ethernet Controller

Table 3-12 Ethernet Controller Signal Description

Mnemonic	Signal Name	Active State (True)	Description
NDAL 0–16	Network data address lines	H	NDAL 0–16 are network data address lines 0–16.
AACKB	Acknowldege	H	AACKB is dual-ported memory controller output. It provides an indication from addressed memory that the transfer cycle can be completed. When not true (low), AACKB causes wait states.
CA	Channel attention	H	CA is CTI Bus inteface control register output. It starts the execution of memory resident command blocks. CA is true for at least one system clock period.
E RESET	Ethernet reset	L	E RESET is CTI Bus interface control register output. It causes a total reset of the controller chip.
CRS	Carrier sense	L	CRS is Ethernet serial interface output. It notifies the controller that there is traffic on the serial link.
RXD	Receive data	H	RXD is Ethernet serial interface output. It decodes the receive serial data.
RXC	Receive data clock	L	RXC is Ethernet serial interface output. It is a clock signal derived from the receive data input. RCX provides timing information for the Ethernet controller.
TXC	Transmit data clock	L	TXC is Ethernet serial interface output. It provides transmit timing for the Ethernet controller.

Table 3-12 Ethernet Controller Signal Description (Cont)

Mnemonic	Signal Name	Active State (True)	Description
CDT	Collision detect	L	CDT is Ethernet serial interface output. It indicates that a collision has occured on the link.
MCLK	System clock	H	MCLK provides system clock timing.
TCLK	Clock	H	TCLK provides clock timing for the NI internal bus controller. It establishes when the command and control signals are generated.
INTR	Interrupt request	H	INTR is output to the CTI Bus interface. It interrupts the host computer.
TEN	Transmit enable	L	TEN enables the serial interface to transmit data. It is forced high after a reset.
TXD	Transmit data	H	TXD is output to the Ethernet serial interface encoder/decoder. It is serial data to be encoded.
S0, S1	Status	L	S0 and S1 are output to the dual-ported memory controller and the NI internal bus controller. They define the type of memory transfer during the current memory cycle. S0 and S1 generate memory control and timing signals in the NI internal bus controller.
ALE	Address latch enable	H	ALE is output to the dual-ported memory port B. It strobes an address into the port B address latch. Latching occurs on the falling (high to low) transition.

Table 3-12 Ethernet Controller Signal Description (Cont)

Mnemonic	Signal Name	Active State (True)	Description
DT/R	Data transmit/ receive	H	DTR is output to the dual-ported memory port B. It establishes the direction of the data flow. When true (high), DT/R enables data transmission from the Ethernet interface to memory. When not true (low), DT/R enables data transmission from memory to the Ethernet interface.
DEN	Data enable	H	DEN is output to the dual-ported memory port B. It enables data transfers between memory and the Ethernet interface.

3.8.1.3 Fail-Safe Time-Out Circuit – The fail-safe time-out circuit (Figure 3-22) provides a timer function. This circuit prevents the station from transmitting continuously for long periods of time. This circuit is important because long transmissions can disable the Ethernet communications link. The timer starts at the beginning of an Ethernet frame transmission and has a time-out of 28 ms. The timer resets each time transmission stops as a result of the transmit enable signal (TEN) being deasserted. If the timer runs out before TEN is deasserted, the Ethernet frame being transmitted is terminated. The timer then resets only when TEN is deasserted. See Table 3-12 for signal descriptions.

3.8.1.4 NI Internal Bus Controller – The NI internal bus controller (Figure 3-22) is clocked by the 8 MHz clock. The controller decodes status inputs S0 and S1 to provide control timing for port B to enable the data flow and establish the direction of the data flow. See Table 3-12 for signal descriptions.

3.8.2 Ethernet Serial Interface

The Ethernet serial interface (Figure 3-23) is the interface between the Ethernet controller and the Ethernet transceiver cable. The interface provides the Ethernet physical layer cable interface and performs Manchester encoding/decoding. It also provides carrier detection, collision detect signal processing, transmit and receive clock timing for the Ethernet controller, and a loopback capability.

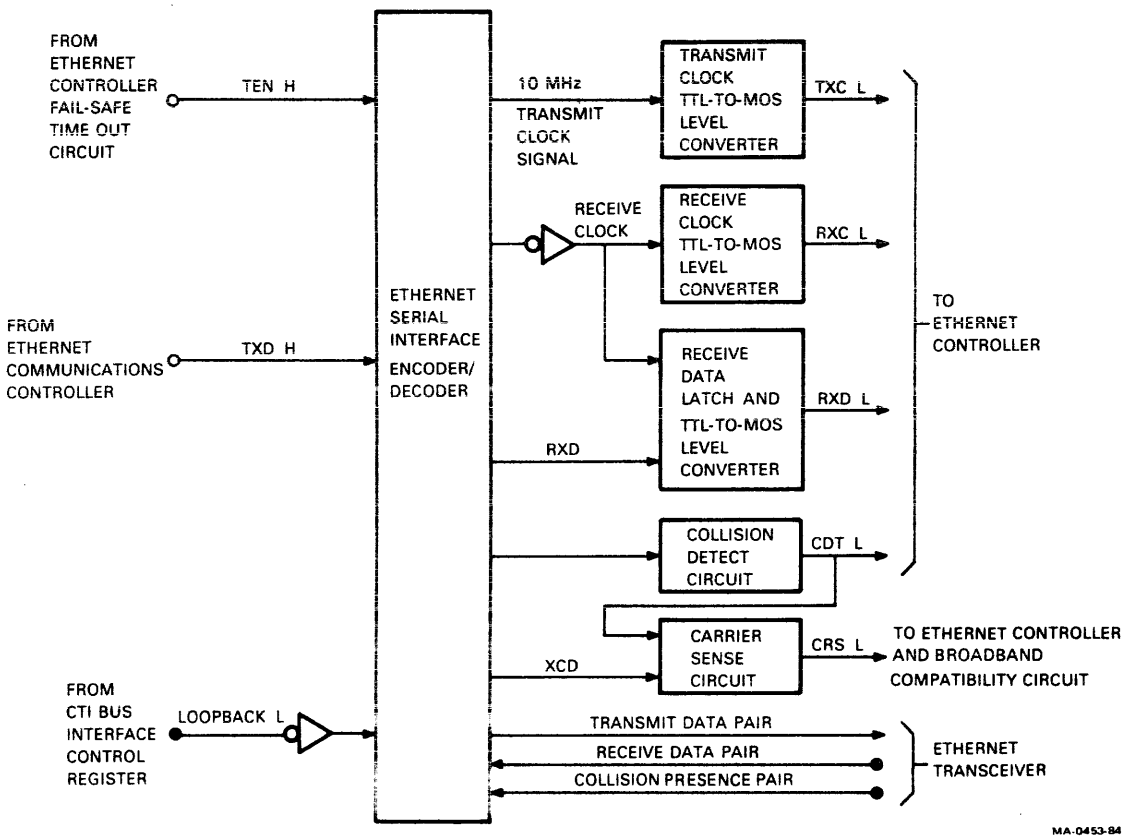


Figure 3-23 Ethernet Serial Interface

The Ethernet serial interface includes the following circuitry.

Ethernet serial interface encoder/decoder (MB502A)
Transmit clock TTL-to-MOS level converter
Receive clock TTL-to-MOS level converter
Receive data latch and TTL-to-MOS level converter
Collision detect circuit
Carrier sense circuit

The rest of Paragraph 3.8.2 describes these circuits to a functional block level. All block diagrams and signal descriptions in this section are derived from the *DECNA Field Maintenance Print Set* (MP5415987-0-1).

Refer to Table 3-13 for signal descriptions.

Table 3-13 Ethernet Serial Interface Signal Description

Mnemonic	Signal Name	Active State (True)	Description
TEN	Transmit enable	H	TEN is Ethernet fail-safe time-out circuit output. It enables transmit data pair. When TEN is not true (low), the transmit data pair signal is idle (high).
TXD	Transmit data	H	TXD is Ethernet controller output. It provides the serial data to be encoded. Serial data is supplied synchronously with the falling edge of the transmit data clock signal.
LOOPBACK	Loopback	L	LOOPBACK is CTI Bus interface control register output. It controls loopback mode operation.
TXC	Transmit data clock	L	TXC is output to the Ethernet controller. It provides the transmit timing for the Ethernet controller.
RXC	Receive data clock	L	RXC is output to the Ethernet controller. It provides receive timing for the Ethernet controller.
RXD	Receive data	L	RXD is output to the Ethernet controller. It receives serial data.
CRS	Carrier sense signal	L	CRS is output to the Ethernet controller and broadband compatibility circuit. It notifies the controller that there is traffic on the serial link.
CDT	Collision detect	L	CDT is output to the Ethernet controller. It notifies the controller that a collision has occurred.

Table 3-13 Ethernet Serial Interface Signal Description (Cont)

Mnemonic	Signal Name	Active State (True)	Description
TRANSMIT + and −	Transmit data pair		TRANSMIT is output to the Ethernet transceiver. It transmits Manchester encoded signals to the Ethernet transceiver.
RECEIVE + and −	Receive data pair		RECEIVE is Ethernet transceiver output. It receives Manchester encoded signals from the Ethernet transceiver.
COLLISION + and −	Collision presence pair		COLLISION is Ethernet transceiver output. It receives a 10 MHz square wave signal generated by the Ethernet transceiver.

3.8.2.1 Manchester Code – Manchester code is a signalling method that combines data and timing clock pulses into a single serial-encoded data stream (Figure 3-24). Each bit is split into two halves with the second half containing the inverse of the first half. A transition always occurs in the middle of each bit. During the first half of the bit, the encoded signal is the logical complement of the bit value being encoded. During the second half of the bit, the encoded signal is the uncomplemented value of the bit being encoded.

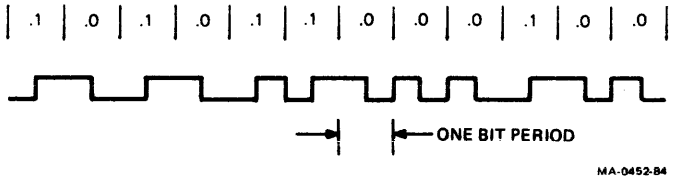


Figure 3-24 Manchester Encoded Data

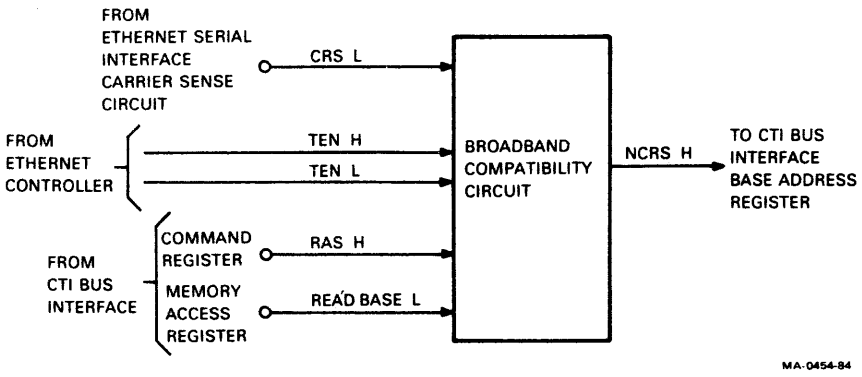


Figure 3-25 Broadband Compatibility Circuit

3.8.2.2 Ethernet Serial Interface Encoder/Decoder – The Ethernet serial interface encoder/decoder (Figure 3-25) is an MB502A chip. The encoder portion of this chip converts serial binary data into Manchester code. The decoder portion of this chip converts Manchester code into binary data and synchronous clock signals.

The *encoder* sends a 10 MHz transmit clock signal, which is converted to the MOS level, to the Ethernet controller. The Ethernet controller sends the TEN signal and transmit data signal (TXD) to the serial interface. The encoder transmits data on differential transmit data pair outputs to the transceiver cable.

The *decoder* receives data on the differential receive data pair inputs from the transceiver cable. It performs a carrier detect function and separates data and clock from the Manchester signal. (The carrier is derived from the receive inputs and passed to the ethernet controller via the carrier sense circuit.)

The encoder/decoder chip converts the collision detect inputs to a TTL output signal, which goes to the Ethernet controller and carrier sense circuit as a collision detect signal (CDT L). The incoming CDTL signal on the collision presence pair input is generated by the Ethernet transceiver. The Ethernet transceiver also simulates a collision at the end of each packet to test the DECNA collision detect circuitry.

The encoder/decoder chip also provides for a loopback operating mode. The loopback signal from the CTI Bus interface control register controls the loopback operating mode. In this mode, encoded data are routed internally to the decoder, the transmit outputs are idle, and the receive collision inputs are ignored. See Table 3-13 for signal descriptions.

3.8.2.3 Transmit Clock TTL-to-MOS Level Converter – The transmit clock TTL-to-MOS level converter (Figure 3-23) converts the 10 MHz transmit clock signal from the encoder/decoder to the MOS level. The converter then feeds the transmit clock signal that results (TXC L) to the Ethernet controller. Refer to Table 3-13 for signal descriptions.

3.8.2.4 Receive Clock TTL-to-MOS Level Converter – The receive clock TTL-to-MOS level converter (Figure 3-23) converts the receive clock signal from the encoder/decoder to the MOS level. The converter then feeds the receive clock signal that results (RXC L) to the Ethernet controller. Refer to Table 3-13 for signal descriptions.

3.8.2.5 Receive Data Resynchronizer and TTL-to-MOS Level Converter – The receive data resynchronizer and TTL-to-MOS level converter (Figure 3-23) supports Manchester encoded data reception. This circuit takes receive clock pulses and receive data from the serial interface encoder/decoder. Then, this circuit positions the data relative to RXC L so that a transition from RXC L to RXC H is centered on a data cell. See Table 3-13 for signal descriptions.

3.8.2.6 Collision Clock Detect Circuit – The collision clock detect circuit (Figure 3-23) is a level converter. It changes the 10 MHz collision signal from the serial interface encoder/decoder to a level (CDT L) required by the Ethernet controller chip. See Table 3-13 for signal descriptions.

3.8.2.7 Carrier Sense Circuit – The carrier sense circuit (Figure 3-23) generates the carrier sense (CRS L) signal for the Ethernet controller chip. It ORs the CDT L and XCD signals from the encoder/decoder to produce CRS L. When CRS L is deasserted, a 5μs one-shot time-out reinforces the CRS L deassertion so that CRS is not allowed to go active for the one-shot time-out period.

3.8.3 Broadband Ethernet Compatibility Circuit

The broadband Ethernet compatibility circuit (Figure 3-25) provides DECNA compatibility with a broadband Ethernet transceiver. In a broadband Ethernet system, the assertion of the carrier detected signal can be delayed up to 17 μs from the beginning of the transmission. During carrier detect in transmission mode, the Ethernet controller does not provide valid carier sense status. To determine the carrier sense status from a transmission on a broadband Ethernet system, a read-only error bit is provided in the CTI Bus interface memory base address register. This bit indicates that for some previously transmitted packet, the carrier sense was never asserted during the transmission. See Table 3-14 for signal descriptions.

Table 3-14 Broad-Band Compatibility Circuit Signal Description

Mnemonic	Signal Name	Active State (True)	Description
CRS	Carrier sense signal	L	CRS is Ethernet serial interface output. It indicates that traffic is on the link.
TEN	Transmit enable	H	TEN is Ethernet controller output. It indicates the beginning of transmission.
RAS	Read address strobe	H	RAS is CTI Bus interface command register output. It clocks the circuit's final stage.
NCRS	No carrier sense signal	H	NCRS is output to the CTI Bus interface memory read base address register. It indicates that, for a previously transmitted packet, CRS L was never asserted during the transmission.
READ BASE	Read base	L	READ BASE is CTI Bus interface memory access register output. It resets the broadband compatibility circuit.

CHAPTER 4
PROFESSIONAL 380 EXTENDED BITMAP OPTION MODULE

4.1 INTRODUCTION

Chapter 4 gives a functional and detailed desciption of the Professional 380 Extended Bitmap Option (EBO) module. Chapter 4 also provides the EBO module's physical, electrical, and environmental specifications, and the connector pin assignments.

4.2 FUNCTIONAL DESCRIPTION

The EBO module (Figure 4-1) is a daughter module for the Professional 380. The EBO module, which connects to the system module via a 64-pin connector (J1), adds two bitmapped video planes to the single plane on the system module.

The major components on the EBO module are two 8263 video gate arrays, and 32 64K × 1 dynamic RAMs. The video gate arrays contain the logic needed to communicate with the system module and EBO memory, and to perform video operations.

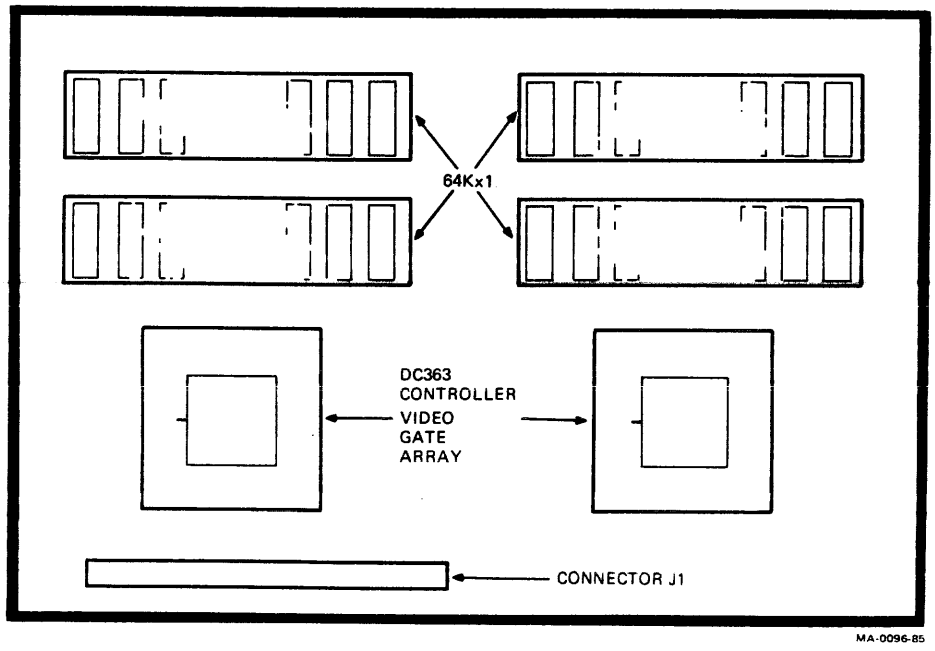


Figure 4-1 Professional 380 EBO Physical Layout

4.3 DETAILED DESCRIPTION

Two 8263 video gate array controllers (Figure 4-1) implement and control all EBO functionality. The gate arrays perform the following functions.

- Synchronize memory requests from the EBO bus interface logic with video refresh cycles
- Perform data transfers between the EBO data/address bus and EBO RAM
- Provide video signals, through the EBO bus interface logic, to the video generation integrated logic on the system module

The EBO memory and video gate array I/O registers share the 128K byte J11 microprocessor address space with the video generation integrated logic on the system module.

NOTE

Paragraph 6.4.4 in Chapter 6 of the Professional 300 Series Technical Manual Volume 1 describes the Professional 380 Video Generation Integrated Logic. This paragraph also describes how the J11 microprocessor address shares its space on the system module. Chapter 7 of the Professional 300 Series Technical Manual Volume 1 describes in detail the operation of the Bitmap Video Controller and EBO modules.

Figure 4-2 is a functional block diagram that shows the EBO module in relation to the rest of the system. The operation of the video memory for planes 2 and 3 on the EBO are identical to those on plane 1 on the system board.

Address and video memory information are loaded by the main system CPU using the IDAL Bus. The video memory for each plane has four screens of information.

If the EBO module is not present in the system, the SYNC signal is amplified by the plane 1 video generator and appears on the blue video line. If the EBO module is present in the system, the SYNC signal is amplified by the plane 2 video generator and appears on the green video line.

Connector J1 provides the power and all signals needed for extended bitmap operation. Paragraphs 4.3.1 through 4.3.4 describe the following EBO module signal groups.

Bus interface signals
Video signals
Interchip control signals
Operational power levels

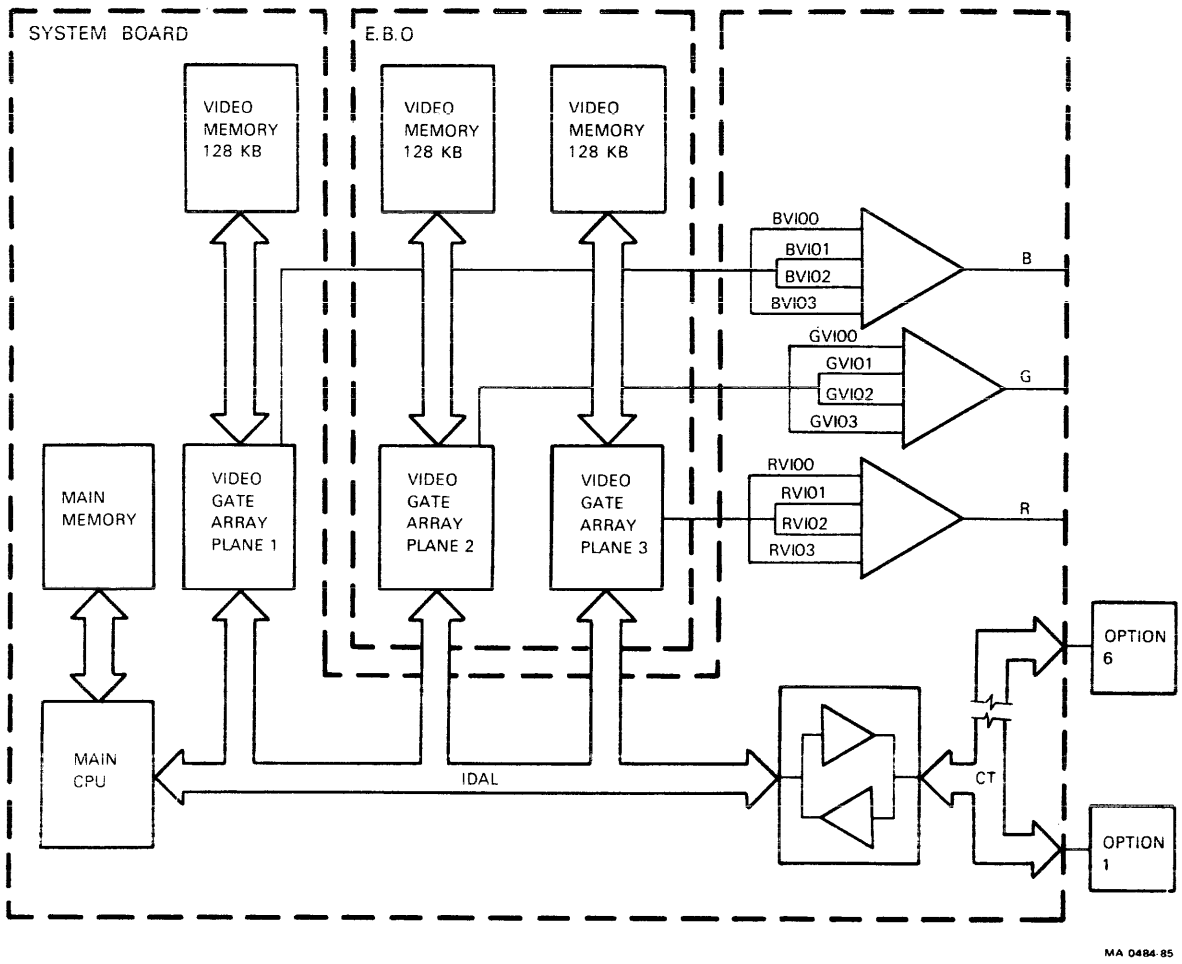


Figure 4-2 Extended Bitmap Option Functional Block Diagram

4.3.1 Bus Interface Signals

The following bus interface signals are needed to transfer information between the J11 microprocessor or a CTI Bus master, and the EBO module.

IDAL00 H through IDAL15 H – Internal Data/Address Line
These bidirectional signals are multiplexed with data and address information. All data transfers to and from the EBO module occur over these lines.

IDAL16 H through IDAL21 H – Internal Address Line
These are address signals only, which are driven by the system module. Data transfers do not occur on these lines.

IOSEL L – I/O Select
When this signal is driven low by the system module, an I/O operation is performed and memory references to the EBO module are disabled.

AS L – Address Strobe
When this signal is driven from a high to a low by the system module, the address information on IDAL00 H through IDAL21 H is latched internally in the video gate arrays.

DS L – Data Strobe
This signal is driven low by the system module during the data portion of each bus cycle.

SDEN L – Slave Data Enable
This signal is driven low by the system module during a read cycle. When a video gate array on the EBO is addressed (I/O operation), or video memory on the EBO is addressed, SDEN L enables the gate array to drive data onto IDAL00 H through IDAL15 H.

WLB L – Write Low Byte
This signal is driven low by the system module during the data portion of a write cycle when the low byte, or a word, is addressed.

WHB L – Write High Byte
This signal is driven low by the system module during the data portion of a write cycle when the high byte, or a word, is addressed.

SS 6 L – Slot Select 6
This signal is driven low by the system module during an I/O operation with the video logic on the system or EBO module.

INIT – Software Reset
When INIT is high, it is used as a reset for the video gate arrays. INIT is asserted high by the system module during a PDP-11 RESET instruction. INIT is also high when DCOK is high (when the power supply voltages are out of tolerance).

DCOK – Power Reset
The DCOK signal is asserted low by the system module when the power supply voltages are within the specified tolerance. When DCOK is high, it is used as a reset for the video gate arrays.

4.3.2 Video Signals
The following video signals on connector J1 synchronize the EBO video gate arrays to the video gate array on the system module (see Figure 6-2 in the *Professional 300 Series Technical Manual Volume 1*). This connector also provides the digital video signals from the EBO for the system module video amplifiers.

GVID0 H through GVID3 H – Green Video
These signals are the inputs to the green digital to analog (D/A) converter on the system module. The plane 2 video gate array normally drives these signals.

RVID0 H through RVID3 H – Red Video
These signale are the inputs to the red D/A converter on the system module. The plane 3 video gate array normally drives these signals.

BVID0 H through BVID3 H – Blue Video
These signals are the inputs to the blue D/A converter on the system module. The system module plane 1 video gate array normally drives these signals.

S1 L through S3 L – Serial Video
These are the serial video signals. S1 L is an output of the system module plane 1 video gate array. S2 L is an output of the EBO plane 2 video gate array. S3 L is an output of the EBO plane 3 video gate array. S1 L through S3 L are the select inputs for the color map in the video gate array.

HSYNC L – Horizontal SYNC Pulse
This signal is an output of the video gate array on the system module. The EBO uses HSYNC L to synchronize the video gate array horizontal counters to the gate array on the system module. HSYNC L is asserted low during a sync interval.

VSYNC L – Vertical SYNC Pulse
This signal is an output of the video gate array on the system module. The EBO module uses VSYNC L to synchronize the video gate array vertical counters to the gate array on the system module. VSYNC L is asserted low during a sync interval.

4.3.3 Interchip Control Signals
The interchip control signals coordinate the information exchange between the EBO bus interface and the three video gate arrays. (One video gate array is on the system module and two are on the EBO module.) These signals ensure that only one gate array can drive the bus at one time. The interchip control signals also include a 20.16 MHz clock from which all video timing is derived. The interchip control signals are described as follows.

WAITO L – WAIT Output
This signal is low when the WAIT OUTPUT signal is low from any one of the three video gate arrays. WAITO L is asserted low to indicate that a memory cycle is in progress.

DONE H – DONE
DONE H is low during a video operation by any of the gate arrays. When all the operations are complete, DONE H goes to a high logic level, which allows the video gate array on the system module to set the CSR DONE bit and generate IRQB.

EBO PRES L – EBO Present
The EBO module grounds EBO PRES L to inform the video gate array on the system module that an EBO module is installed. The gate array on the system module clears bit 13 of the CSR when an EBO module is present. EBO PRES L also changes the identification code of the video from 50 octal to 10050 octal when the EBO module is installed.

V20MHZ H – Video 20 MHz Clock
This is the 20.16-MHz video clock. All the video logic timing and synchronization is derived from V2DMHZ H.

4.3.4 Operational Power Levels
The EBO module uses +5 Vdc and ground (GND) for power.

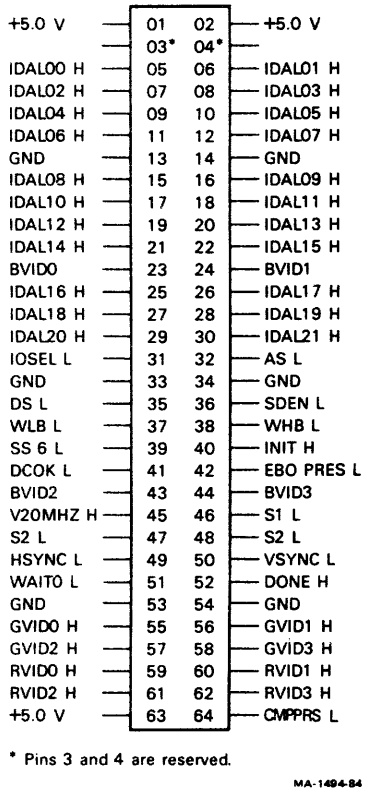


Figure 4-3 Connector J1 Pin Assignment

4.3.5 EBO Module Connector Pin Assignment

Connector J1 on the EBO module is a 64-pin female connector that mates with the EBO connector (J2) on the system module. This connection carries power and serves as the signal interconnect to the system module. Figure 4-3 shows the signal pin assignment for J1.

4.4 HARDWARE SPECIFICATIONS

The following paragraphs describe hardware specifications for the Professional 380 Extended Bitmap Option module.

4.4.1 Physical Specifications

The EBO module has the following physical specifications.

Length	8.00 in
Width	5.20 in
Height	0.75 in

4.4.2 Power Specifications

The EBO module has the following power requirements.

Voltage	+4.75 to +5.25 Vdc
Current	1.5 A (estimated)

4.4.3 Environmental Specifications

The EBO module is designed to comply with the Class C Environmental Specifications in DEC-STD-102 Revision C. The following paragraphs are a summary of the environmental requirements for operation and storage.

4.4.3.1 Operating Environment – The EBO module's operating environment is specified by altitude, relative humidity, and free air ambient temperature (DEC-STD-102 Revision C, Class C). If the EBO module is operating in an enclosure, the airflow requirements (Paragraph 5.1.4 in DEC-STD-102) must also be met.

4.4.3.2 Operating Temperature – The free air ambient temperature surrounding an operating EBO module must be within the following limits.

5°C (41°F) minimum
60°C (140°F) maximum

4.4.3.3 Operating Relative Humidity – The relative humidity for an operating EBO module must be within the limits specified below.

10% minimum
90% maximum

The wet bulb temperature must not exceed 32°C (90°F) and the dew point must not be less than 2°C (36°F).

4.4.3.4 Storage Environment – The EBO module storage environment is specified by altitude, relative humidity, and free air ambient temperature (DEC-STD-102 Revision C, Class C).

4.4.3.5 Storage Temperature – The storage temperature for an EBO module must be within the following limits.

−40°C (−40°F) minimum
66°C (151°F) maximum

4.4.3.6 Storage Relative Humidity – The relative humidity of the storage environment for the EBO module must be within the following limits.

10% minimum
90% maximum

CHAPTER 5
RD50/RD52-A HARD DISK DRIVE CONTROLLER MODULE

5.1 GENERAL INFORMATION

The RD50/RD52-A Hard Disk Drive Controller module is the interface component of the controller and drive subsystem. Figure 5-1 shows the hard disk controller module in relation to the other components in the Professional Series computer system.

The RD50 and RD52-A controller modules are functionally the same. The RD50 controller module supports only the RD50 and RD51 drives. The RD52-A controller supports the RD50, RD51, and RD52-A drives.

5.1.1 Related Documentation

The *Professional 350 Field Maintenance Print Set* (MP-01394-00) provides more information about the hard disk controller module.

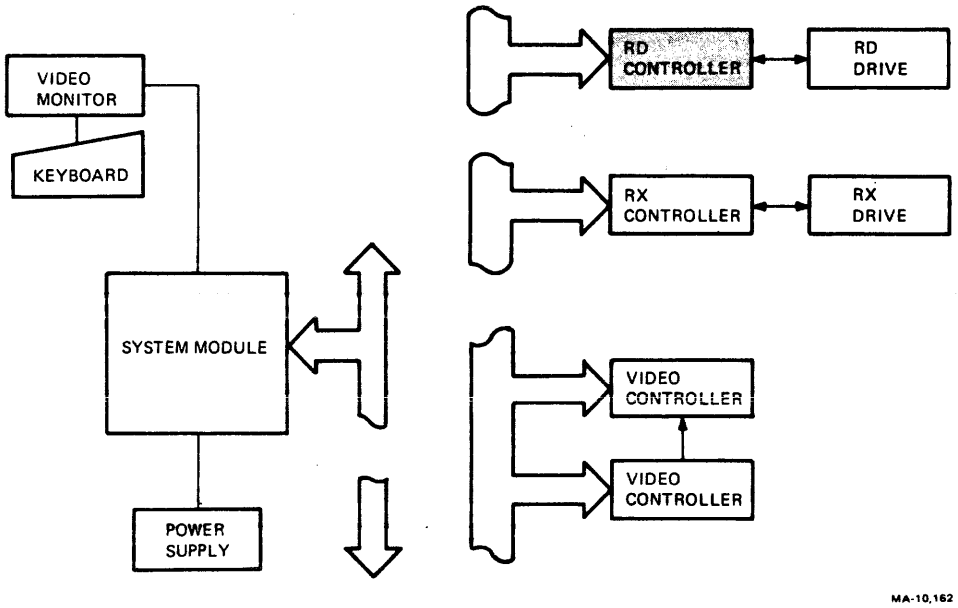


Figure 5-1 Controller Module System Relation

5.1.2 Hard Disk Drive Controller Module

The hard disk drive controller module connects a hard disk drive to the host processor (Figure 5-2). This controller module is a 12.7 cm × 30.5 cm (5.2 in × 12 in) field replaceable unit (PN 54-15134 for the RD50 and PN 54-15134-01 for the RD52). This controller module mounts in slot 1 of the computing terminal Interconnect bus (CTI Bus) option space. Three connectors on the controller module allow connection to the host processor's CTI Bus and the disk drive.

A zero insertion force (ZIF) connector (J1) at the bottom of the controller module makes the module compatible with the CTI Bus. This connector allows the host processor to control the controller module's operations from the CTI Bus.

A 20-pin connector (J2) at the top of the controller module allows a cable (PN 17-00282) to be connected from the controller module to the disk drive for data interfacing.

A 34-pin connector (J3) at the top of the controller module allows a cable (PN 17-00286) to be connected from the controller module to the disk drive for command and status signal interfacing.

Refer to Chapter 5 in the *Professional 300 Series Technical Manual, Volume 1* for the J1 connector description and signal definitions. Paragraph 5.4 gives the J2 and J3 connector descriptions and signal definitions.

5.2 FUNCTIONAL COMPONENTS

Paragraphs 5.2.1 through 5.2.6 describe the controller module's functional components.

5.2.1 Overview

The host processor sees the controller module as a set of registers accessible from the CTI Bus. The host processor reads and writes to these registers. It sends commands and data to, and retrieves data from the controller module. The controller module then enables the disk drive to seek the data location and retrieve or store the data for the host processor. Seek operations are embedded within the command sequence that the controller module accepts from the host processor. Refer to Paragraph 5.5 and 5.6 for more information about the registers and the sequence in which the host processor gains access to them.

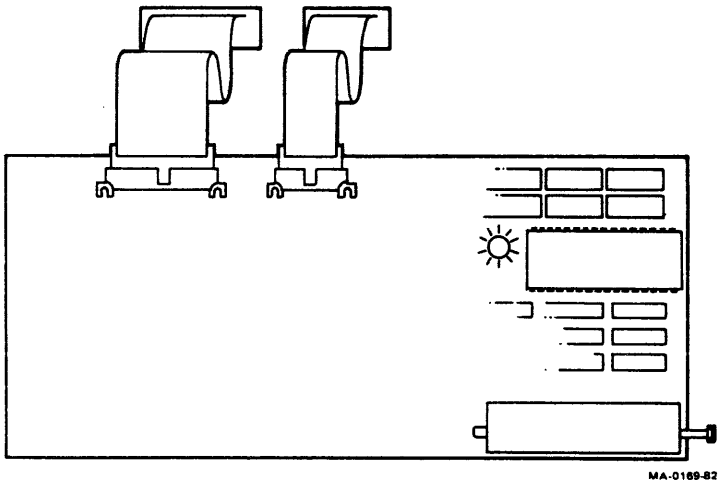


Figure 5-2 Controller Module

The controller module contains memory for use as a sector buffer and status and command storage. The microprocessor (μP) control circuits map the memory for both functions. Accesses to the status and command registers are mapped into predefined memory locations for use by the μP control circuits. Accesses to the sector buffer are mapped into sequential address locations for use by the μP control circuits.

Transfers between the controller module and the host processor are program controlled by the host processor. The host processor loads or unloads a sector buffer on the controller module by writing or reading to one of the registers. The controller module then encodes or decodes the data between the sector data buffer and the disk drive. The controller module performs data error detection for all data transfers between its sector buffer and the drive.

The controller module transfers data from the main memory to the disk surface as follows.

1. The host processor controls a data transfer from main memory to a sector buffer in the controller module.

2. The controller module then controls the data transfer from its sector buffer to the disk drive.

A data request from the host processor reverses the above steps for data transfers from the disk drive to main memory.

The following circuits in the controller module transfer data between the host processor and the disk drive (Figure 5-3).

- CTI Bus interface
- μP control
- Disk control and status
- Modified frequency modulation (MFM) write data
- Modified frequency modulation (MFM) read data

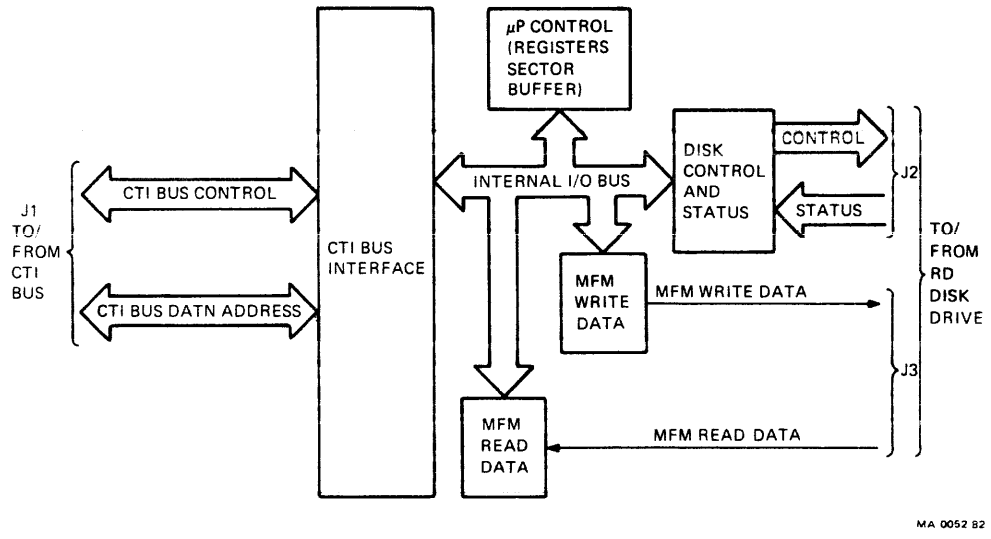


Figure 5-3 Controller Module Block Diagram

5.2.2 CTI Bus Interface Circuits

The host processor gains access to the controller module through the CTI Bus interface circuits. It does this by reading and writing to the controller module's eight registers. (See Paragraph 5.5 for detailed information about the registers.) For the host processor to access these registers, the CTI Bus interface circuits perform the following functions.

- Acknowledge addressing of its registers by the host processor
- Transfer data between the host processor and the controller
- Generate interrupts for the host processor when the controller needs service

See Paragraph 5.3.1 for more information about how these circuits work.

5.2.3 Microprocessor (μP) Control Circuits

The μP control circuits are responsible for the controller module's internal operations. These circuits perform the following functions.

- Arbitrate the use of the internal I/O bus to control the controller module's internal data flow
- Control access to the memory in the μP control circuits
- Generate the disk drive control signals from the commands received from the host processor

See Paragraph 5.3.2 for more information about how these circuits work.

5.2.4 Disk Control and Status Circuits

The disk control and status circuits transfer control and status information between the controller module and the disk drive. The μP control circuits control the disk control and status circuits to access drive status information from the disk drive, and pass drive control information to the disk drive.

The μP control circuits process all control and status information. The host processor accesses the μP control circuits through the CTI Bus interface circuits. The μP control circuits then run microprograms to compute the seek and select signals generated for the disk drive. The μP control circuits then cause the disk control and status circuits to transfer the control and status information between the controller module and the disk drive.

See Paragraph 5.3.3 for more information about how these circuits work.

5.2.5 Modified Frequency Modulation (MFM) Write Data Circuits

The modified frequency modulation (MFM) write data circuits convert data received from the host processor to MFM data for the disk drive. These circuits perform the following functions.

- Convert data bytes from the sector buffer in the μP control circuits to serial data
- Calculate then add two CRC bytes to the end of the serial data
- Convert the serial data to MFM data
- Generate status signals for the μP controller during conversion
- Transfer the MFM write data to the disk drive.

The host processor selects the controller module to perform a write operation by accessing registers in the μP control circuits through the CTI Bus interface circuits. The μP control circuits then run a microprogram. This microprogram allows the host processor to send data through the CTI Bus interface circuits, and then store the data in the sector buffer in the μP control circuits. The μP control circuits then cause the disk control and status circuits to transfer control and status information between the controller module and the disk drive. This sequence prepares and controls the disk drive to accept the data transfer. Then, the μP control circuits sequentially transfer the data stored in the sector buffer to the MFM write data circuits. The MFM write data circuits convert the data to MFM encoded data, and pass the MFM encoded data to the disk drive for storage.

See Paragraph 5.3.4 for more information about how these circuits work.

5.2.6 Modified Frequency Modulation (MFM) Read Data Circuits

The MFM read data circuits convert MFM data from the disk drive into data that the host processor retrieves from the controller module. These circuits perform the following functions.

- Search through the data on the disk drive to find the valid MFM encoded header
- Decode the MFM data that follows the header from the disk drive
- Convert the decoded data to bytes for the sector buffer in the μP control circuits
- Calculate two CRC bytes from the data read from the disk drive, and compare them to the values previously stored with the data
- Generate status signals for the μP controller during conversion

The host processor selects the controller module to perform a read operation by accessing registers in the μP control circuits through the CTI Bus interface circuits. The μP control circuits then run a microprogram. This microprogram causes the disk control and status circuits to send seek control signals to, and monitor status signals from, the disk drive. The disk drive then returns MFM encoded data to the MFM read data circuits. These circuits convert the MFM encoded data to byte data, which the μP control circuits then store in the sector buffer. After all the data is stored in the sector buffer, the host processor retrieves the data from the sector buffer through the CTI Bus interface circuits.

See Paragraph 5.3.5 for more information about how these circuits work.

5.3 THEORY OF OPERATION

The controller module has five circuit groups, which connect the disk drive to the host processor. Paragraphs 5.3.1 through 5.3.6 describe these circuits at a functional block diagram level and describes how they work together.

The host processor accesses the controller module by reading from and writing to the controller module's registers. The STATUS/INIT register is in the controller's circuits. The other registers are mapped into memory by the μP control circuits. The μP control circuits control all accesses to the controller module's memory. The memory is mapped as register space and sector buffer space.

The microprocessor on the controller module processes all host processor accesses to all registers except the STATUS/INIT register. Accesses to registers require microprocessor intervention, but appear as address locations to the host processor.

See Paragraphs 5.5 and 5.6 for detailed descriptions of the controller module registers.

5.3.1 CTI Bus Interface Circuits

The CTI Bus interface circuits allow the host processor access to the controller module registers. The CTI Bus interface circuits are as follows (Figure 5-4).

CTI Bus I/O controller
Data I/O port
CTI Bus data/address transceivers
Address buffer
STATUS/INIT register

The host processor gains access to the controller module through these circuits by passing an address to the circuits and then reading or writing the data. The host processor can address the STATUS/INIT register without intervention from the μP control circuits. To address the other seven registers, however, requires loading the address into the address buffer. The μP control circuits can then transfer data between the data I/O ports and the μP control circuits, over the internal I/O bus.

5.3.1.1 CTI Bus I/O Controller – Figure 5-4 shows the CTI Bus I/O controller receiving and generating CTI Bus control signals. The controller decodes CTI Bus control signals from the host processor and sends I/O control signals to the CTI Bus data/address transceivers, data I/O ports, address buffer, and the STATUS/INIT register. The following I/O control signals cause the circuits to receive data and addresses from the CTI Bus, or send data over the CTI Bus.

- **Interrupt Generation**
  Some of the CTI Bus control signals are interrupts and acknowledgements for the host processor. The CTI Bus I/O controller generates these interrupts from status signals it receives from the μP control circuits.

- **Controller Reset**
  Some of the CTI Bus control signals also generate a reset signal for the controller module. This reset signal initializes the μP control circuits and the MFM write data circuits.

5.3.1.2 CTI Bus Data/Address Transceivers – The CTI Bus data/address transceivers connect to the CTI Bus data/address lines. The I/O control signals cause the transceivers to transfer data and addresses between the CTI Bus and the controller module over internal data/address lines.

5.3.1.3 STATUS/INIT Register – When the STATUS/INIT register is addressed by the host processor, the CTI Bus I/O controller allows two things to happen. Either the controller status data is sent or the command signal, RESET, is received over the data/address lines. The reset signal initializes the μP control circuits and the MFM write data circuits. Accessing this register does not interrupt the μP controller circuits or the internal I/O bus.

5.3.1.4 Address Buffer – The address buffer receives three data/address lines from the CTI Bus data/address transceivers. When the host processor addresses any register except the STATUS/INIT register, this buffer is loaded with the bits that define access to one of the controller module's registers. The μP control circuits receive this register address.

5.3.1.5 Data I/O Ports – The data I/O port contains buffers to temporarily hold the data and commands transferred between the host processor and the controller module. The CTI Bus I/O controller allows the host processor to write or read data from the CTI Bus through the CTI Bus data/address transceivers to the data I/O port. The read and write strobes generated by the μP controller circuits allow the μP controller to access the data I/O port over the internal I/O bus.

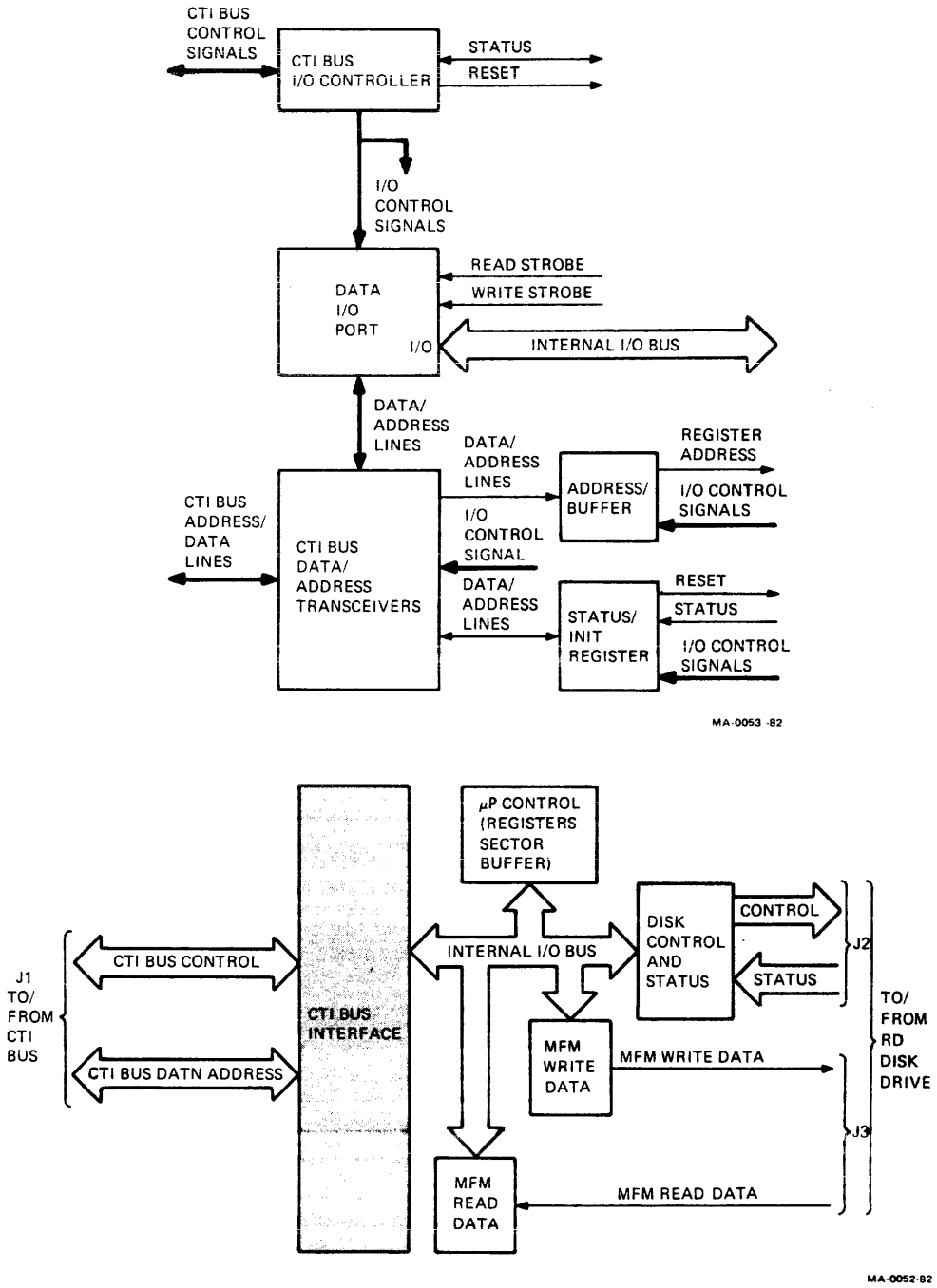


Figure 5-4 CTI Bus Interface Circuits

5.3.1.6 General Controller Module Access – While the controller module is performing a function, only the STATUS/INIT register can be accessed. No other controller module register can be accessed. Figure 5-3 shows the structure of the internal I/O bus. All data and command transfers occur over this bus. Interrupting the internal I/O bus while the controller module is performing a function is an illegal procedure.

5.3.2 μP Control Circuits

The μP control circuits are responsible for the controller module's internal operation (Figure 5-5). The μP control circuits are as follows.

Microprocessor
Microprogram ROMs
Data flow controller
Address/status buffer
Memory
Disk read/write controller

5.3.2.1 Internal I/O Bus Control – The μP control circuits control transfers over the internal, I/O bus by generating the addresses for the microprogram ROM's data flow controller. The addresses access the microprograms to execute the controller module functions. These addresses also generate read and write strobes to control transfers over the internal I/O bus.

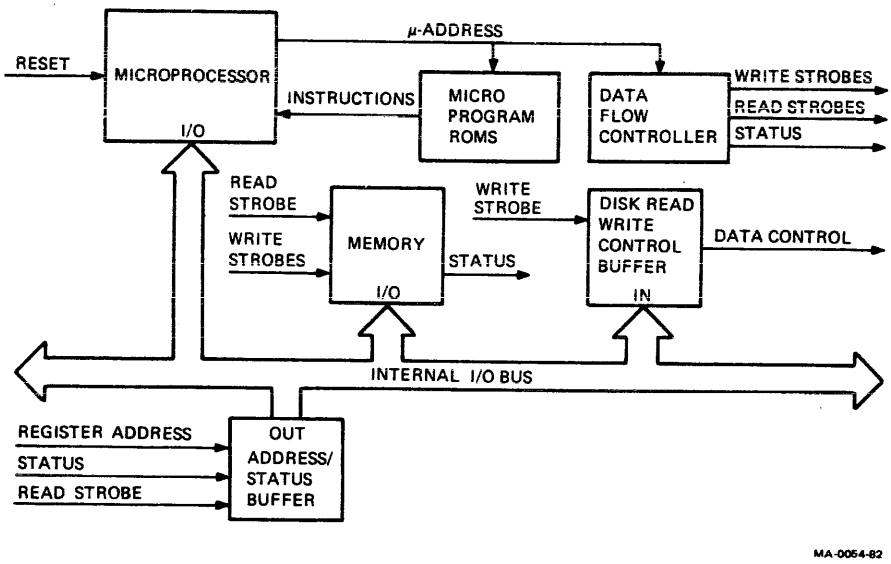
The read and write strobes control accesses to the memory, the address/status buffer, and the disk read/write control buffer over the internal I/O bus. The read and write strobes also go to the other controller circuits to control transfers over the internal I/O bus.

5.3.2.2 Memory Mapping and Access – The microprocessor maps accesses to the memory for status and command storage and sector buffer storage.

After the host processor addresses a register, except the STATUS/INIT register, the microprocessor causes the data flow controller to generate a read strobe. This strobe places the address/status buffer contents on the internal I/O bus. The microprocessor then maps the access to the memory, and causes the data flow controller to generate read and write strobes. These strobes transfer data between memory and the data I/O port in the CTI Bus interface circuits. Accesses to all other circuits are performed in the same way.

When the host processor accesses the sector buffer, the memory returns a full status indicator to the address/status buffer for use by the microprocessor.

5.3.2.3 Disk Read/Write Control Buffer – The microprocessor loads commands into the disk read/write control buffer. The buffer then generates data control signals to perform read and write functions between the controller module and disk drive. These signals set up the MFM write data circuits to send data to the disk drive or set up the MFM read data circuits to decode data received from the disk drive.



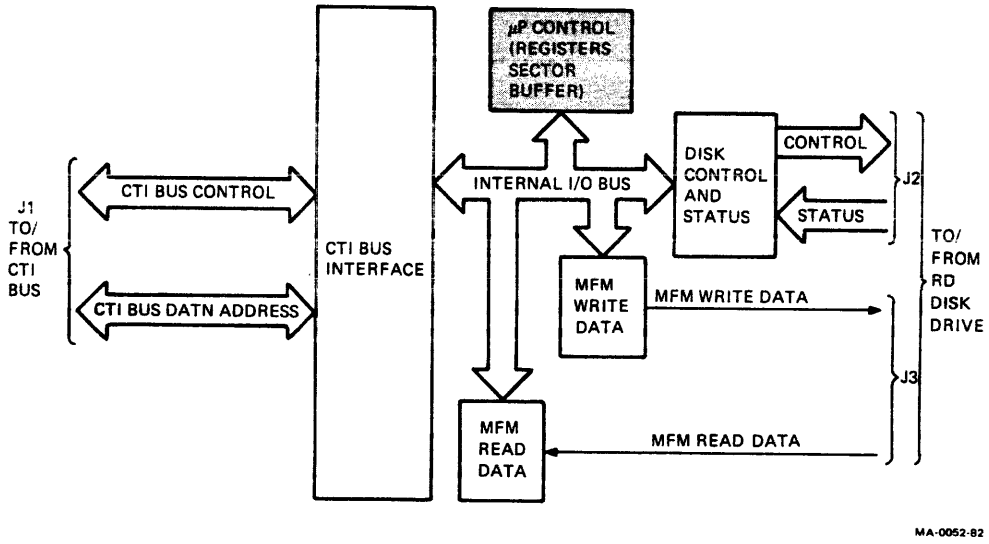


Figure 5-5 Microprocessor (μP) Control Circuits

5.3.3 Disk Control and Status Circuits – The disk control and status circuits transfer control and status information between the controller module and the disk drive (Figure 5-6). These circuits are used when the controller module performs read and write operations between the controller module and the disk drive. The disk control and status circuits are as follows.

Disk control signal buffer
Disk status signal buffer

Paragraphs 5.3.3.1 and 5.3.3.2 describe the buffers and their uses. Refer to Paragraph 5.4 for detailed information about the signals transferred between the controller module and disk drive by these buffers.

5.3.3.1 Disk Control Signal Buffer – This buffer passes disk control signals to the disk drive. Using write strobes, the μP control circuits load this buffer with control words on the internal I/O bus. The control words, generated by the μP control circuits, include select signals for the drive, write control signals, and seek control signals. The write control signals passed to the drive are also sent to the MFM write data circuits. This synchronizes control operations with the transmission of MFM write data to the disk drive.

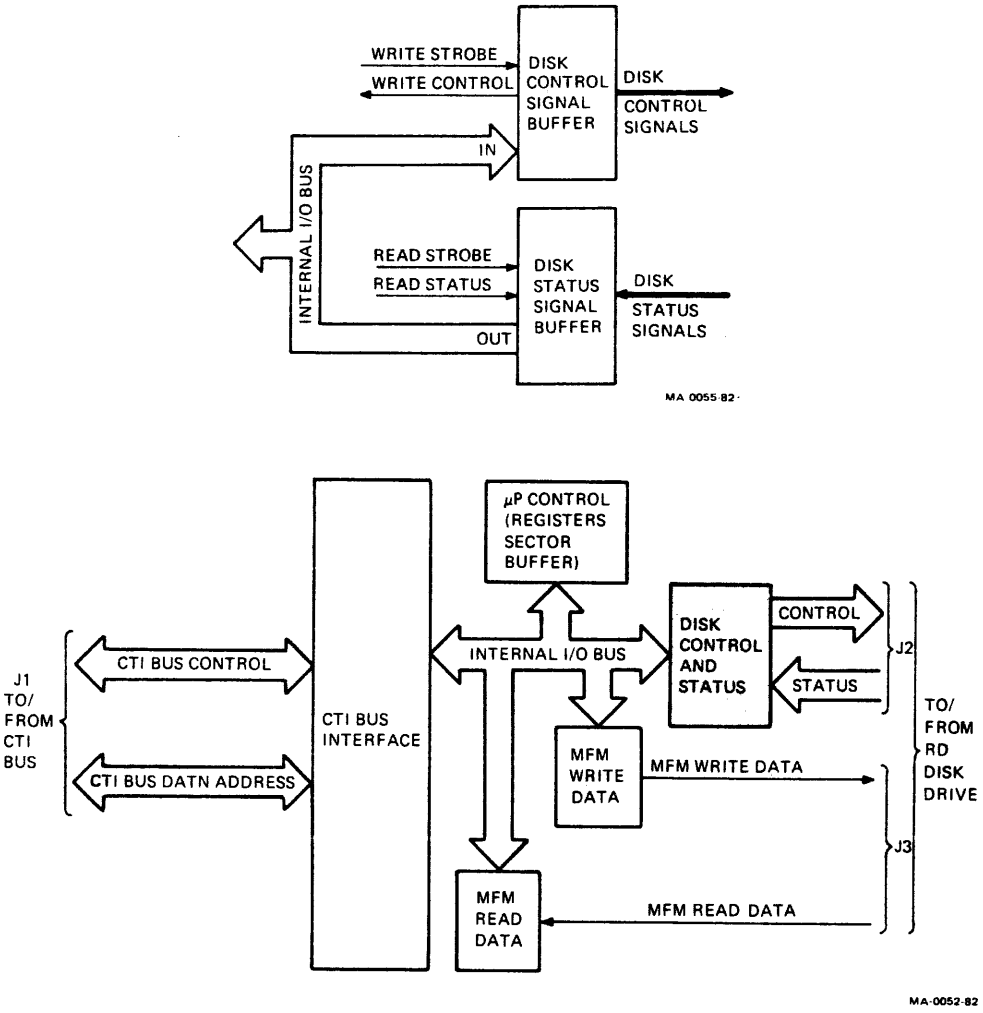


Figure 5-6 Disk Control and Status Circuits

5.3.3.2 Disk Status Signal Buffer – This buffer allows the μP control circuits to simultaneously access disk status information from the disk drive and read status information from the MFM read data circuits. When the μP control circuits generate a read strobe, the status information goes over the internal I/O bus to the μP control circuits. The disk status information is used when the controller module executes either a write or read function with the disk drive.

5.3.4 MFM Write Data Circuits

The MFM write data circuits convert byte data from the sector buffer to MFM data to be written to the disk (Figure 5-7). These circuits are used with the disk control and status circuits when the controller module performs a write data function to the disk drive. The disk control and status circuits select the drive, cause the drive to seek to the desired cylinder, and enable the drive to write to the disks. The MFM write data circuits convert the data the controller module received from the host processor to MFM data for the disk drive. The μP control circuits synchronize all operations and signal generation to perform the write function. The MFM write data circuit are as follows.

Write clock generator
Parallel-to-serial converter
CRC generator/checker
MFM generator

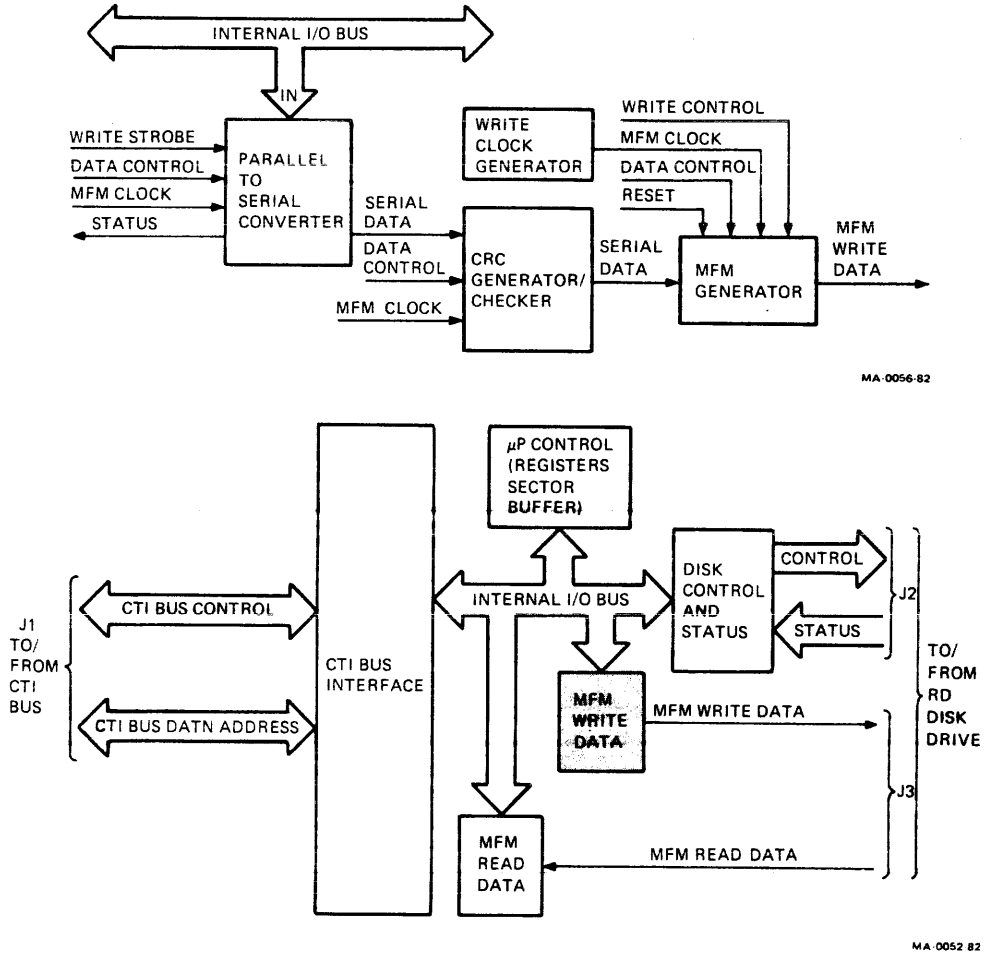


Figure 5-7 Modified Frequency Modulation (MFM) Write Data Circuits

5.3.4.1 Parallel-to-Serial Converter – The μP control circuits use a data control signal to enable the parallel-to-serial converter. The μP control circuits also issue a write strobe. This action loads a data byte from the sector buffer over the internal I/O bus into the parallel-to-serial converter. The MFM clock from the write clock generator serially shifts the data byte to the CRC generator/checker. When the converter generates a byte-shifted status signal, the μP control circuits load the next data byte into the converter.

5.3.4.2 CRC Generator/Checker – When the μP control circuits enabled the parallel-to-serial converter, they also initialized the CRC generator/checker with a data control signal. The MFM clock shifts the data from the parallel-to-serial converter through the CRC generator/checker to the MFM generator. During the shift the CRC generator/checker calculates two CRC bytes. Those bytes are added to the end of the write data when the μP control circuits issue an end-of-data control signal.

5.3.4.3 MFM Generator – The MFM generator receives a data control signal from the μP control circuits. This action initializes the generator before starting to convert the byte data to serial data. Write control signals from the disk control and status circuits indicate if the data is recorded on inner or outer tracks. They also indicate when the disk drive is enabled to write to the disks. The MFM generator can then select precompensation values and synchronize MFM write data transmission to the disk drive by using the drive write control signal.

After the MFM generator is set up to convert the write data to MFM write data, the MFM clock causes the MFM generator to generate precompensated MFM write data for the disk drive.

5.3.5 MFM Read Data Circuits

The MFM read data circuits convert MFM-encoded data read from the drive into 8-bit bytes for the sector buffer (Figure 5-8). The disk control and status circuits use the MFM read data circuits when the controller module performs a read data function with the disk drive. The disk control and status circuits select the drive, cause the disk drive to seek the desired cylinder, and enable the disk drive to read the disks. The μP control circuits synchronize all operations and signal generation to perform the read function. The MFM read data circuits are as follows.

Phase-lock loop/data separator (PLL/DP)
Address mark detector
Serial-to-parallel converter
CRC generator/checker

5.3.5.1 Phase Lock Loop/Data Separator – MFM read data is received from the disk drive via the phase-lock loop/data separator. The μP control circuits enable the phase-lock loop/data separator circuit with a data control signal to search for preambles.

Preambles indicate the start of MFM-encoded read data for each sector. A detected preamble causes the separator to generate a read status signal to the disk control and status circuits. The μP control circuits access this signal from the disk control and status circuits.

During a preamble, the phase-lock loop also locks to the MFM read data frequency and generates a delayed phase clock signal. The data separator then extracts the serial data from the MFM-encoded read data. Then, the phase-lock loop/data separator passes the serial data and data clocks to the address mark detector and the serial-to-parallel converter.

5.3.5.2 Address Mark Detector – The μP control circuits use a data control signal to enable the address mark detector. The detector searches for an address mark in the serial data and data clocks. When the mark is detected, an address mark signal initializes and enables the serial-to-parallel converter.

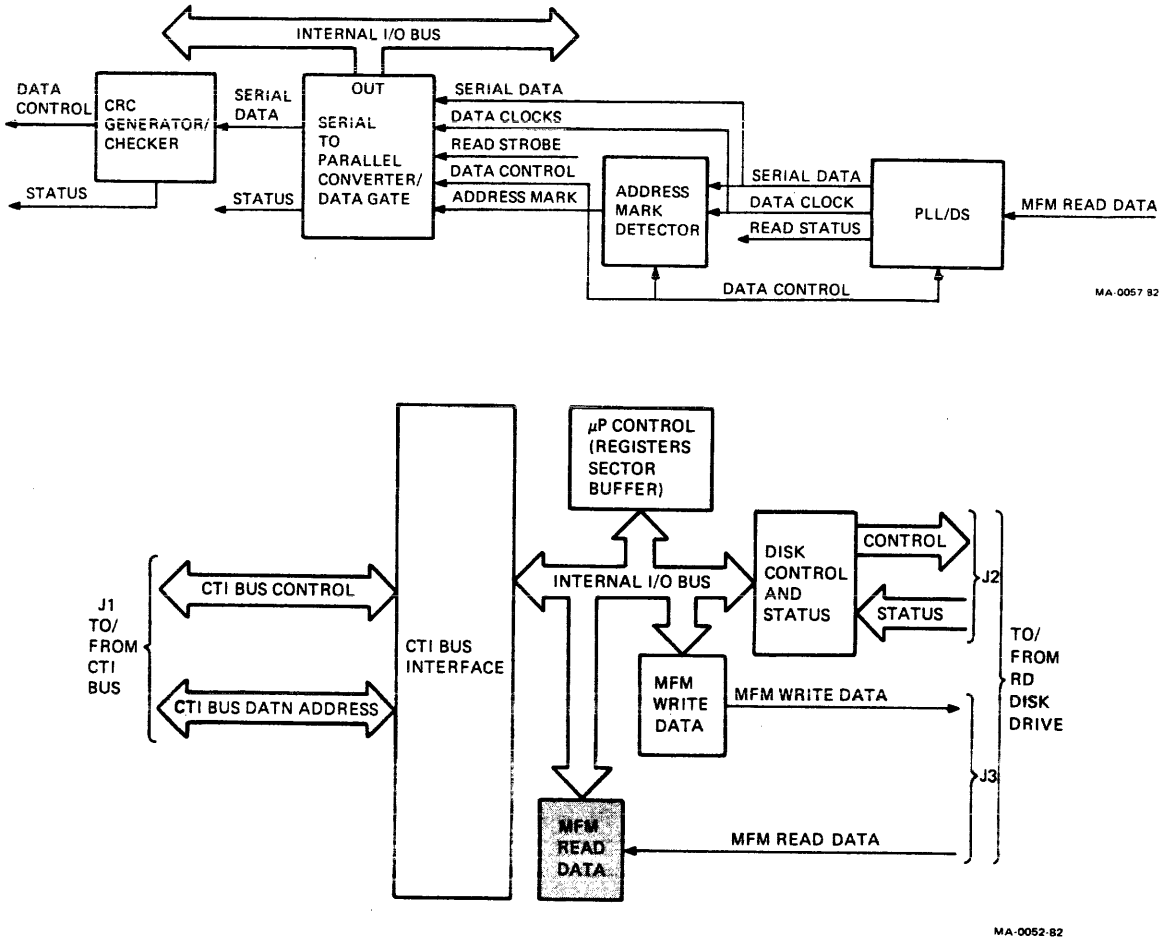


Figure 5-8 MFM Read Data Circuits

5.3.5.3 Serial-to-Parallel Converter – After the address mark detector enables the serial-to-parallel converter, the converter assembles byte data from the serial data and data clocks it receives from the phase lock loop/data separator. The converter assembles an 8-bit byte, then generates a byte ready status signal for the μP control circuits. The μP control circuits then generate a read strobe to retrieve the byte data over the internal I/O bus. This sequence continues until the μP control circuits retrieve all the necessary data.

5.3.5.4 CRC Generator/Checker – The μP control circuits initialize the CRC generator/checker before the read cycle begins. The serial-to-parallel converter assembles byte data and passes the serial data to the CRC generator/checker. The CRC generator/checker monitors the data, computes two CRC bytes, and compares the CRC bytes to the CRC bytes at the end of the serial data. If the data is valid, the CRC generator/checker generates a status signal for the μP controller circuits.

5.3.6 Controller Data Flow Description

Figure 5-9 shows the functional circuits described in Paragraphs 5.3.1 through 5.3.5 and the data flow discussed below. Paragraphs 5.3.6.1 and 5.3.6.2 describe two examples of data flow: a drive command data flow and a write data flow. These examples do not follow the microcode command sequences, but are presented to help you understand the controller module's capabilities.

5.3.6.1 Drive Command Data Flow – When the host processor sends a command to the disk drive, the following events occur.

- The host processor asserts the CTI Bus control signals in the correct sequence. Then, the controller module accepts the register address and data and loads them into the address buffer and data I/O port.
- The μP control circuits access the register address in the address/status buffer, then place the data in the assigned memory register location. The microprocessor interprets an access to the STA 2/COMMAND register as a go command.
- The μP control circuits perform the go command and calculate the necessary values.
- The μP control circuits place a data command word on the internal I/O bus and then load the word into the disk control signal buffer.
- The disk control signal buffer then asserts the disk control signals selected by the data command word for the disk drive.

5.3.6.2 Write Data Flow – When the host processor sends data to the drive for storage, the following events occur.

- Once the host processor issues a write command to the controller, the host processor then accesses the data register continually. The host processor then places data words for the register on the CTI Bus address/data lines. The host processor then asserts the CTI Bus control signals in the correct sequence, which activates the controller module. The controller module accepts the data and loads the data into the data I/O ports.
- The μP controller continually accesses the data I/O ports and transfers the data over the internal I/O bus to the memory sector buffer.
- When the transfer from the host processor to the controller module is complete, the controller module places the data words from the memory on the internal I/O bus. Then, the controller module loads the data word into the parallel-to-serial converter.
- The write clock generator clocks data through the MFM write data circuits, the parallel-to-serial converter, the CRC generator/checker, and the MFM generator.
- Once a data word shifts past the parallel-to-serial converter, a status signal is generated for the address status register. This signal tells the μP controller when to load another data word into the converter.
- The serial data goes to the CRC generator/checker. Two CRC bytes are calculated to be summed after the original write data is serially shifted out.
- The MFM generator continually receives the write data, encodes the data into MFM format, and sends it to the disk drive.

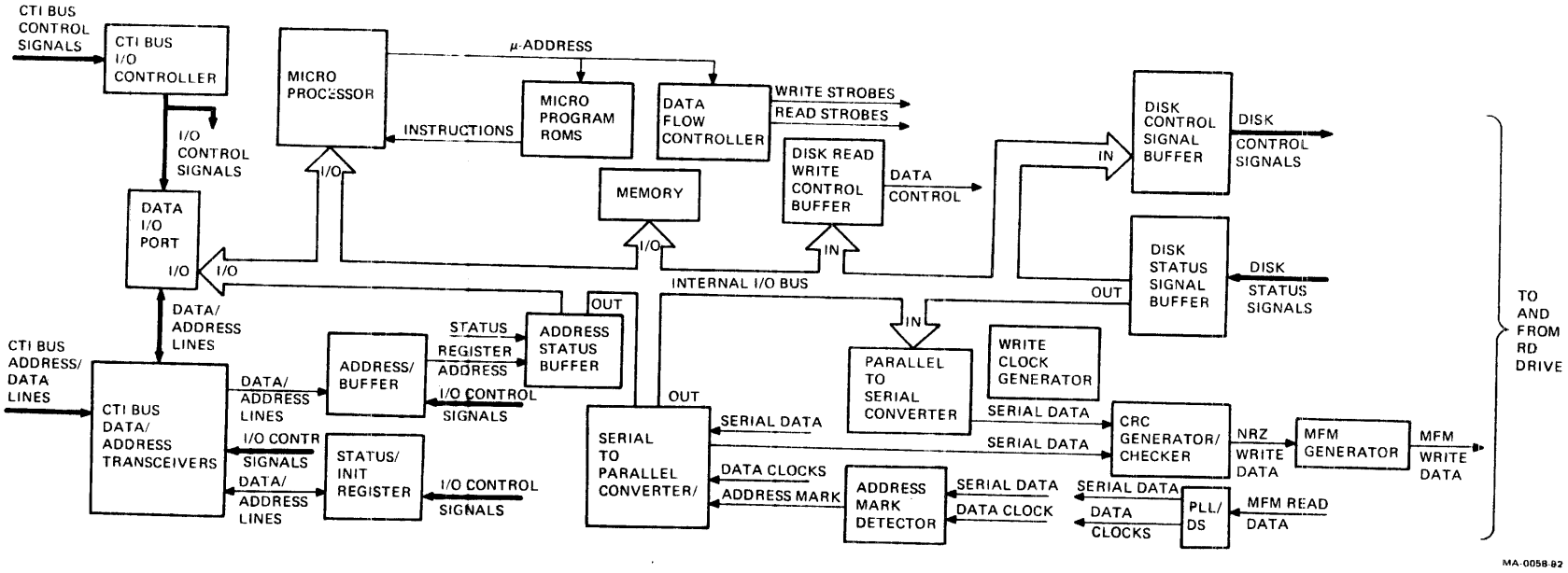


Figure 5-9 Controller Module Data Flow Diagram

5.4 DETAILED CONNECTOR DESCRIPTIONS

Paragraphs 5.4.1 through 5.4.3 describe the signals passed between the controller module, the disk drive, and the host processor. Figure 5-10 shows the connectors on the controller module, the signal names, and the signal flow.

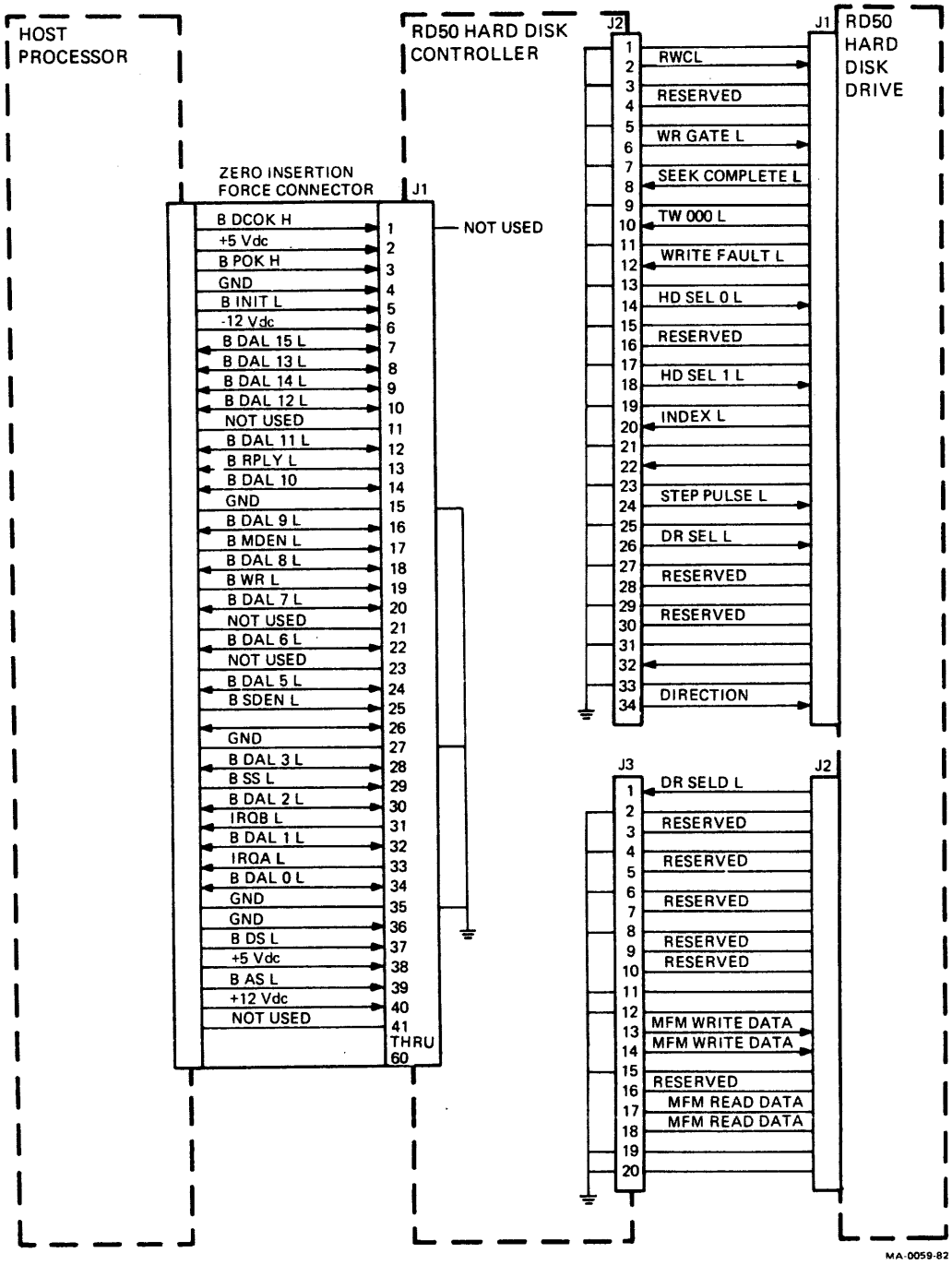


Figure 5-10 Controller Module Interface Signal Flow

5.4.1 CTI Bus Interface J1

The controller module uses the data/address and control lines of the CTI Bus to implement program data transfers.

5.4.2 Disk Control/Status Connector J2

Table 5-1 lists the pin functions of the controller module's J2 connector. The signal mnemonic column also describes the asserted state of each signal. An L after the mnemonic indicates an asserted low state (logic zero). An H after the signal name indicates an asserted high state (logic high).

Table 5-1 Connector J2 Pin Description

Pin	Signal Name	Signal Mnemonic
1	Ground	
2	Reduced write current	RWC L (RD50 only)
3	Ground	
4	HEAD SELECT 2	HEAD SEL 2 L
5	Ground	
6	Write gate	WR GATE L
7	Ground	
8	Seek complete	SEEK COMPLETE L
9	Ground	
10	Track 000	TK000 L
11	Ground	
12	Write fault	WRITE FAULT L
13	Ground	
14	Head select 20	HD SEL 0 L
15	Ground	
16	Unspecified	
17	Ground	
18	Head select 21	HD SEL 1 L
19	Ground	
20	Index	INDEX L
21	Ground	
22	Ready	READY L
23	Ground	
24	Step	STEP PULSE L
25	Ground	
26	Drive select 1	DR SEL L
27	Ground	
28	Reserved	
29	Ground	
30	Reserved	
31	Ground	
32	5 megabytes low	SMB L (RD50 only)
33	Ground	
34	Direction In	DIRECTION IN L

5.4.2.1 REDUCED WRITE CURRENT (Pin 2) – This signal is used with the RD50 hard disk drive only. When the controller module asserts this signal and write gate, the disk drive uses a lower value of write current for writing on the disk. When this signal is unasserted, the disk drive uses a higher value of write current.

A lower write current is used when writing to tracks 128 through 157 rather than through tracks 0 through 127. This happens because the heads fly lower over the inside tracks. When the heads are closer to the disk, a lower write current generates a weaker write magnetic field. Using a normal write current at the inside tracks of the RD50 would damage data in the adjacent tracks.

5.4.2.2 WRITE GATE (Pin 6) – This interface signal goes to the disk drive. The asserted state of this signal enables the write drivers when SEEK COMPLETE is asserted.

5.4.2.3 HEAD SELECT (Pin 4, 14 and 18) – These three signals (HD SEL 0, HD SEL 1, and HD SEL 2) go to the disk drive. They form a binary word to select one of up to eight disk drive heads.

5.4.2.4 STEP (Pin 24) – This interface signal goes to the disk drive. The STEP signal controls the movement of the read/write heads. The DIRECTION IN signal defines the direction of the movement.

5.4.2.5 DIRECTION IN (Pin 34) – This interface signal goes to the disk drive. When a step pulse is issued, this signal defines the movement direction of the read/write heads. The asserted state of DIRECTION IN selects head movement towards the center of the disk. An unasserted signal selects head movement towards track 0.

5.4.2.6 DRIVE SELECT (Pin 26) – This signal goes to the disk drive to tell the drive that the controller module is ready. This signal becomes unasserted if any of the following three events occur.

The host processor sends a reset command
POWER OK is unasserted on the CTI Bus
INIT is asserted on the CTI Bus

5.4.2.7 SEEK COMPLETE (Pin 8) – This signal comes from the disk drive. When asserted, SEEK COMPLETE indicates that the read/write heads have completed a seek command. When unasserted, all writing is inhibited. This signal becomes unasserted during any seek operation.

5.4.2.8 TRACK 000 (Pin 10) – This signal comes from the disk drive. When TRACK 000 is asserted, the read/write heads are positioned at track 0 (the outermost track).

5.4.2.9 WRITE FAULT (Pin 12) – This signal comes from the disk drive. When WRITE FAULT is asserted, one of the following conditions is detected and writing or read/write head motion is inhibited. The signal stays asserted until the condition is corrected.

- The heads receive current when the WRITE GATE signal is asserted.
- The DRIVE SELECT and WRITE GATE signals are asserted, but the heads do not receive current.
- Either there are multiple heads, no head, or a head is incorrectly selected.
- The dc voltages are out of tolerance.

5.4.2.10 INDEX (Pin 20) – This signal comes from the disk drive as a low-going pulse, and occurs once every disk revolution. The pulse indicates the beginning of the track.

5.4.2.11 READY (Pin 22) – This interface signal comes from the disk drive. When READY is asserted, it indicates that the drive is ready to read, write, or seek. If SEEK COMPLETE and READY are asserted, then the I/O signals are valid. When READY is deasserted, all writing and seeking actions are inhibited.

5.4.2.12 RD50 5 MB (Pin 32) – This signal comes from the disk drive and is used to determine the type of drive connected to the interface. RD50 5 MB is high when an RD50 is attached, and low for all other disk drives.

5.4.3 Disk Data I/O Connector J3

Table 5-2 lists the pin functions of the controller module's J3 connector. The signal mnemonic column also describes the asserted state of each signal. An L after the mnemonic indicates an asserted low state (logic zero). An H after the signal name indicates an asserted high state (logic high).

5.4.3.1 DRIVE SELECTED (Pin 1) – This signal comes from the disk drive. When DRIVE SELECTED is asserted, it indicates that the disk drive is selected.

5.4.3.2 MFM WRITE DATA (Pins 13 and 14) – This differential pair of signals goes to the disk drive and defines the transitions to be written on the disk surface. If WRITE GATE is asserted, a flux reversal occurs on the disk at the transition of +MFM WRITE DATA going more positive than the –MFM WRITE DATA. When the controller module reads data from the disk drive, this signal becomes unasserted. (+MFM WRITE DATA is more negative than –MFM WRITE DATA.)

5.4.3.3 MFM READ DATA (Pins 17 and 18) – This differential pair of signals comes from the disk drive and is recovered read data from the selected head. The transition of the +MFM READ DATA signal going more positive than the –MFM READ DATA signal represents a flux reversal from the selected head.

Table 5-2 Connector J3 Pin Description

Pin	Signal Name	Signal Mnemonic
1	Drive selected	DRV SELD L
2	Ground	
3	Reserved	
4	Ground	
5	Spare	
6	Ground	
7	Unspecified	
8	Ground	
9	Spare	
10	Spare	
11	Ground	
12	Ground	
13	+MFM write data	+MFM WRITE DATA H
14	–MFM write data	–MFM WRITE DATA H
15	Ground	
16	Ground	
17	+MFM read data	+MFM READ DATA H
18	–MFM read data	–MFM READ DATA H
19	Ground	
20	Ground	

5.5 PROGRAMMING REGISTERS

Paragraphs 5.5.1 through 5.5.8 describe the controller module registers. These registers access the sector buffer and the controller module's command modes.

The controller module has eight 16-bit registers for communication with the CTI Bus. These registers handle communication between the controller module and the host processor. All write operations to the registers are done by word transfers. Registers that are not defined are reserved. Table 5-3 defines the controller module's eight registers.

All the registers are available to the host processor unless the controller module is executing a function. This is indicated by a set BUSY bit in the STATUS/INIT register. The STATUS/INIT register can be accessed at all times.

NOTE

An addressing error occurs if the BUSY bit is set and then any register, except STATUS/INIT, is addressed. This sequence forces the host processor to perform a time-out trap to memory location 4. Refer to Chapter 5 in the Professional 300 Series Technical Manual Volume 1 for a detailed description of the time-out trap.

5.5.1 ID Register (774000)

This register is a read-only register. When read by the host, it returns a 16-bit ID of 0101 hexadecimal (000401 octal). This register indicates the controller module's starting address range.

NOTE

If the ID register is accessed when the BUSY bit is set in the STATUS/INIT register, the host processor performs time-out trap to memory location 4. Refer to Chapter 5 in the Professional 300 Series Technical Manual Volume 1 for a detailed description of the time-out trap.

Table 5-3 Programming Registers

Bus Address	Name	Type
774000	ID	Read Only (R/O)
774004	ERROR/PRECOMP	Read-Error/write-precompensation
774006	BACKUP REV/SECTOR ID	Read/write
774010	DATA BUFFER	Read/write
774012	CYLINDER ID	Read/write
774014	HEAD ID	Read/write
774016	STA 2/COMMAND	Read-STA 2/write-command
774020	STATUS/INIT	Read-Status/write-initialize

5.5.2 ERROR/PRECOMP Register (774004)

This register has two functions: the high byte contains error information and the low byte stores the cylinder address at which write precompensation starts.

NOTE

If this register is accessed when the BUSY bit is set in the STATUS/INIT register, the host processor performs a time-out trap to memory location 4. Refer to Chapter 5 in the Professional 300 Series Technical Manual Volume 1 for a detailed description of the time-out trap.

This register's high byte is read only for error information. This error information is valid only if the error bit is set in the STA 2/COMMAND register. A new command clears the high byte. Table 5-4 defines the high byte's error bits.

This register's low byte is write only. It stores the cylinder number at which write precompensation starts. A default precompensation value is stored in this byte during a software or hardware initialization of the controller module. The default value is cylinder number 128_{10} divided by 4. To use a different write precompensation point, divide the selected cylinder number by 4 and write the result into this register's low byte. Table 5-5 lists the precompensation cylinders for each disk drive.

5.5.2.1 DM Not Found (Bit 8) – This bit can only be set during a read sector command. It indicates that the data mark (DM) was not found after the requested ID field is successfully read.

5.5.2.2 TR000 Error (Bit 9) – This bit can only be set during a RESTORE command. It indicates that track 0 (TR000) was not found after the disk drive performed seeks through 1100 tracks.

Table 5-4 Error Bit Definitions

Bit Number	Function
08	DM (data mark) not found
09	TR000 error
10	Illegal/aborted command
11	Not used
12	ID not found
13	CRC error, ID field
14	CRC error, data field
15	Not used

Table 5-5 Disk Drive Precompensation Cylinders

Drive	Precompensation Cylinder
RD50	128
RD51	128
RD52	256

5.5.2.3 Illegal/Aborted Command (Bit 10) – This bit is set when any one of the following conditions occur.

- An invalid command is received.
- A command is received that cannot be executed based on status information from the disk drive (for example, write fault is present during a write sector command). The host must analyze other status bits to determine the cause of the error.
- A self-diagnostic error occurs during power-up or reset.

5.5.2.4 ID Not Found (Bit 12) – When this bit is set, it indicates that the requested sector was not found after two disk revolutions.

NOTE

When bit 12 is set, a restore command must be issued to return the drive to its track 0 reference point and clear the bit.

5.5.2.5 CRC Error ID Field (Bit 13) – When this bit is set, it indicates that a CRC error was found in the ID field. This bit can only be set if the comparing parameters (for example, cylinder number or sector number) match, but the CRC bytes do not match the computed CRC value.

5.5.2.6 CRC Error Data Field (Bit 14) – When this bit is set, it indicates that a CRC error was found in a data field during a read sector command. Although the data might be bad, the host can read the sector buffer.

5.5.3 BACKUP REVISION/SECTOR ID Register (774006)

This register is a 16-bit read/write register. This register's low byte identifies the sector address used in the current operation. Refer to Table 5-6 for the low byte bit definitions. This register's high byte identifies the last time the sector was backed up to off-line storage. Refer to Table 5-7 for the high byte bit definitions.

NOTE

If this register is accessed when the BUSY bit is set in the STATUS/INIT register, the host processor performs a time-out trap to memory location 4. Refer to Chapter 5 in the Professional 300 Series Technical Manual Volume 1 for a detailed description of the time-out trap.

NOTE

The sector ID byte can be read only after a read sector command is performed. It should not be read during an internal sector buffer transfer. Reading the byte during a transfer resets the internal sector buffer's address pointer to zero.

Table 5-6 Sector ID Bit Definitions

Bit Number	Function
0	Sector ID bit 0
1	Sector ID bit 1
2	Sector ID bit 2
3	Sector ID bit 3
4	Reserved
5, 6, 7	Not used

Table 5-7 Backup Revision Bit Definitions

Bit Number	Function
8	These bits are user definable.
9	Usually these bits indicate
10	the backup code to off-line
11	storage. The codes are user
12	defined.
13	
14	
15	

5.5.4 DATA BUFFER Register (774010)

This register is a 16-bit read/write register. It is the data transfer window between the controller module and the host. Accessing this register resets both the DRQ bit in the STATUS/INIT register and the data request bit in the STA 2/COMMAND register.

When another word is ready to be read from or written to the sector buffer, the DRQ and data request bits are set again. This sequence repeats until the buffer is completely read or written.

NOTE

If this register is accessed when the BUSY bit is set in the STATUS/INIT register, the host processor performs a time-out trap to memory location 4. Refer to Chapter 5 in the Professional 300 Series Technical Manual Volume 1 for a detailed description of time-out trap.

5.5.5 CYLINDER ID Register (774012)

This register is a 16-bit read/write register. It identifies the cylinder used in the current operation. Refer to Table 5-8 for the bit definitions.

NOTE

If this register is accessed when the BUSY bit is set in the STATUS/INIT register, the host processor performs a time-out trap to memory location 4. Refer to Chapter 5 in the Professional 300 Series Technical Manual Volume 1 for a detailed description of the time-out trap.

5.5.6 HEAD ID Register (774014)

This is a read/write register. It contains the ID of the surface/head used in the present operation. Refer to Table 5-9 for the bit definitions.

NOTE

If this register is accessed when the BUSY bit is set in the STATUS/INIT register, the host processor performs a time-out trap to memory location 4. Refer to Chapter 5 in the Professional 300 Series Technical Manual Volume 1 for a detailed description of the time-out trap.

5.5.7 STA 2/COMMAND Register (774016)

This register is a read/write register. The low byte contains the command used in the current operation; the high byte contains that operation's secondary status (STA 2). Refer to Table 5-10 for the bit definitions of the command byte. Refer to Table 5-11 for the bit definitions of the secondary status byte.

NOTE

If this register is accessed when the BUSY bit is set in the STATUS/INIT register, the host processor performs a time-out trap to memory location 4. Refer to Chapter 5 in the Professional 300 Series Technical Manual Volume 1 for a detailed description of time-out trap.

5.5.7.1 Restore – The restore command moves the read/write head assembly to track 0. This command is executed only if the DRIVE READY and SEEK COMPLETE signals are asserted and the WRITE FAULT signal is unasserted. Use this command after an ID not found error or an initialize.

After receiving the restore command, the controller module sets the BUSY bit in the STATUS/INIT register and tests for a TRACK 000 (TR000) signal.

If the TRACK 000 signal is asserted, the restore command is terminated. This sets the OP ENDED bit, and resets the BUSY bit in the STATUS/INIT register.

If the TRACK 000 signal is unasserted when it is tested, a step pulse is issued to the disk drive. Step pulses are issued to the disk drive until the read/write head assembly moves to track 0 (TRACK 000 signal asserted), or 1100 step pulses are issued.

Table 5-8 Cylinder ID Bit Definitions

Bit Number	Function
0	CYL ID bit 0
1	CYL ID bit 1
2	CYL ID bit 2
3	CYL ID bit 3
4	CYL ID bit 4
5	CYL ID bit 5
6	CYL ID bit 6
7	CYL ID bit 7
8	CYL ID bit 8
9	CYL ID bit 9
10–15	Not used

Table 5-9 Head ID Bit Definitions

Bit Number	Function
0	HD ID bit 0
1	HD ID bit 1
2	HD ID bit 2
3–15	Not used

Table 5-10 Command Byte Bit Definitions

Command	Bits 7654 3210
Restore	0001 0000
Read sector	0010 0000
Write sector	0011 0000
Format	0101 0000

Table 5-11 Secondary Status Bit Definitions

Bit Number	Function
8	Error status
9	0 (not used)
10	0 (not used)
11	Data request
12	Seek complete
13	Write fault
14	Drive ready
15	0 (not used)

If track 0 is found before 1100 step pulses are issued, the restore command is terminated with the OP ENDED bit only.

However, if after 1100 step pulses are issued and the TRACK 000 signal is still unasserted, the restore command is terminated. The OP ENDED bit is set in the STATUS/INIT register, the error bit is set in the STA 2/COMMAND register, and the TR000 error bit is set in the ERROR/PRECOMP register.

5.5.7.2 Read Sector - A read sector command causes the controller module to read one sector (256 16-bit words) from the drive to the sector buffer in the controller module.

When the read sector command is received, the BUSY bit is set in the STATUS/INIT register. A seek is then performed to the requested cylinder in the CYLINDER ID register. Once the head assembly is positioned over the destination cylinder, each sector ID field is read. The sector IDs are compared with the head address, sector address, and cylinder address specified for the read sector command.

Once the correct sector is found, the ID field CRC is verified. If the ID field is correct, the controller module then searches for the data mark.

When the data mark is detected, the data field is transferred to the sector buffer. The back-up revision ID byte is loaded into the high byte of the BACKUP REV/SECTOR ID register. The data field CRC is then checked.

Once the data field CRC value is read, the BUSY bit is reset and the DRQ bit is set in the STATUS/INIT register.

If the computed data field CRC value does not compare to the value read from the sector, the error bit is set in the STA 2/COMMAND register. The CRC error data field (bit 14) is then set in the ERROR/PRECOMP register.

If interrupts are enabled when the first DRQ bit is set, an interrupt to the host is generated. The host uses the DATA BUFFER register to check the error bit in the STA 2/COMMAND register or read a data word out of the internal sector buffer.

When the host reads the word from the DATA BUFFER register, the DRQ bit is reset. When the next word is ready, another DRQ is generated. This sequence repeats 256 times before the buffer is completely read. Once the sector buffer is empty, the OP ENDED bit is set in the STATUS/INIT register. This sequence indicates that the operation is complete.

During a read sector command, errors can occur that will terminate the command. If this occurs, the BUSY bit is reset and the OP ENDED bit is set in the STATUS/INIT register. Also, the error bit is set in the STA 2/COMMAND register. This sequence indicates that the ERROR/PRECOMP register contains detailed error information (refer to Paragraph 5.5.2). The following events terminate a command.

- The correct ID field cylinder address, head address, or sector address cannot be found within two disk revolutions. The ID not found error (bit 12) is set in the ERROR/PRECOMP register.

- The ID field cylinder address, head address, and sector addresses are found, but the computed ID field CRC does not match the recorded ID field CRC. The CRC error ID field (bit 13) is set in the ERROR/PRECOMP register.

- The data mark (DM) is not detected within 16 bytes of the ID field CRC or after two disk revolutions. The DM not found error (bit 8) is set in the ERROR/PRECOMP register.

5.5.7.3 Write Sector – The write sector command writes the internal sector buffer (256 16-bit words) to the specified cylinder, head, and sector of the disk.

When the write sector command is received, the DRQ bit is set in the STATUS/INIT register. If the interrupts are enabled, an interrupt is generated to the host.

The host then transfers a 16-bit data word to the DATA BUFFER register, which resets the DRQ bit. After the controller module stores the data word in the sector buffer, the controller module sets the DRQ bit again. This sequence repeats until 256 words are loaded into the sector buffer.

After the buffer is loaded, the BUSY bit is set in the STATUS/INIT register. A seek is then performed to the requested cylinder and the ID field is verified.

After the ID field is verified, the controller module turns on the write gate and writes to the specified cylinder, head, and sector. This includes the data preamble, the sync mark, the data mark, the data, the back-up revision level byte, the reserved bytes, and the two bytes of CRC.

After writing this information, the controller module resets the BUSY bit and sets the OP ENDED bit in the STATUS/INIT register. If the interrupts are enabled, the OP ENDED bit generates an interrupt to the host. This sequence indicates that the write operation is complete.

Two error conditions can occur during a write sector command: ID not found error and ID field CRC error. If either condition occurs, the operation terminates with the ERROR bit set in the STA 2/COMMAND register, the OP ENDED bit set and the BUSY reset in the STATUS/INIT register.

5.5.7.4 Format – This command is a special type of write command. It allows the host processor to format one track at a time and defines the physical location of each sector on the track.

To use this command, the host processor loads the cylinder ID and head ID of the track to be formatted into the CYLINDER ID register and the HEAD ID register. The host processor then loads the format command into the STA 2/COMMAND register.

When the controller module decodes the command, it generates the DRQs needed to load 256 words into the sector buffer. When the first DRQ occurs, the host processor loads the data buffer in the controller module with the sector ID assigned to the first sector after the INDEX signal.

When the second DRQ occurs, the host processor loads the data buffer with the sector ID assigned to the second sector after the INDEX signal. The host processor continues to assign sector IDs until it reaches the 17th DRQ.

From the 17th DRQ until the last DRQ, the host loads data into the data buffer. This operation assigns the fill character to be written into the sector.

To address the sectors sequentially from 0 to 15 the controller module loads each word with the corresponding sector address. (For example, word 0 with sector address 0, word 1 with sector address 1, word 2 with sector address 2.)

To interleave the sectors in a random pattern such as 0, 8, 1, 9, 2, 10, 3, 11, 4, 12, 5, 13, 6, 14, 7, and 15, the controller module loads each word with the random sector address. (For example, word 0 with sector address 0, word 1 with sector address 8, word 2 with sector address 1.) The disk drives used on the Professional 350 and 380 computer systems are formatted with a five to one interleave. The order of the sectors is 0, 13, 10, 7, 4, 1, 14, 11, 8, 5, 2, 15, 12, 9, 6, 3.

NOTE

The bit organization is the same for these words and the BACKUP REV/SECTOR ID register. (See Paragraph 5.5.3 and Table 5-6.)

Once the sector buffer is loaded, the controller module sets the BUSY bit in the STATUS/INIT register. The disk drive seeks to the specified cylinder and selects the head.

The controller module then waits for the INDEX signal from the disk drive. When the signal is received, the controller module turns on the write gate and writes the complete track.

The cylinder address used is the cylinder address stored in the CYLINDER ID register. The head address used is the head address stored in the HEAD ID register. The sector address for the first sector is word 0 of the sector buffer. The sector address for the second sector is word 1 of the sector buffer. The addressing continues in the same pattern.

The data fields, back-up revision bytes, and reserved bytes are set to zero.

After the track is completely written, the controller module resets the BUSY bit and sets the OP ENDED bit in the STATUS/INIT register. This sequence indicates that the operation is complete.

5.5.7.5 Error Status – This bit indicates that the ERROR/PRECOMP register contains a valid error status. This bit provides a fast way for the host to check if error information is stored in the ERROR/PRECOMP register. Once the error status bit is set, the host reads the ERROR/PRECOMP register and determines what caused the error.

5.5.7.6 Data Request – This bit (together with DRQ) is set when data is ready to be read from or written to the sector buffer. Reading from or writing to the DATA BUFFER register clears both this bit and DRQ. When another word is ready to be read from or written to the sector buffer, the DRQ and data request bits are set again. This sequence is repeated until the buffer is completely read or written.

5.5.7.7 Seek Complete – This bit indicates the condition of the seek complete signal from the disk drive. When set, this bit indicates that the drive is ready for reading or writing.

5.5.7.8 Write Fault – When this bit is set, it indicates that a write fault condition exists at the disk drive. If a write operation was performed when this fault condition occurred, data was not written correctly because of a failure in disk drive electronics. This bit can only be reset by turning the system power off and then on again.

5.5.7.9 Disk Drive Ready – When this bit is set, it indicates that the disk drive is ready to seek, read, or write.

5.5.8 STATUS/INIT Register (774020)

5his register may be read from or written to at any time. All other registers should only be accessed if the BUSY bit in this register is reset. Table 5-12 defines this register's bit.

5.5.8.1 OP ENDED – When this bit is set, it indicates that the operation specified in the command register is complete. The status of the completed operation is indicated in the STA 2/COMMAND register. If interrupts are enabled, this bit also causes an interrupt to the host. Reading or writing to the STA 2/COMMAND register resets the OP ENDED bit.

5.5.8.2 RESET/INITIALIZE – When this bit is set, it causes an initialization sequence (Paragraph 5.5.4).

5.5.8.3 DRQ – When this bit is set, it indicates a data transfer is needed. DRQ is cleared by accessing the DATA BUFFER register. When another word is ready to be read from or written to the sector buffer, the DRQ (data required) bit and the data request bit are set again. This sequence is repeated until the buffer is completely read or written.

If interrupts are enabled, this bit also causes an interrupt to the host processor.

5.5.8.4 BUSY – When this bit is set, it indicates that no other register can be accessed. This bit is set when the controller uses the internal I/O bus.

Table 5-12 STATUS/INIT Register Definitions

Bit Number	Function
0	Operation ended (read only)
1	Not used
2	Not used
3	Reset/initialize (write only)
4	Not used
5	Not used
6	Not used
7	Data transfer request (read only)
8	Reserved
9	Not used
10	Not used
11	Not used
12	Not used
13	Not used
14	Not used
15	Busy (internal I/O bus in use) (read only)

5.6 GENERAL SEQUENCE OF OPERATION

The controller module can store and recover data blocks of 256 16-bit words. The following sections describe the controller module's general sequence of operations.

5.6.1 Read Sector, Write Sector, Format Command

The host processor performs a read sector, write sector, or format command as follows.

- Reads the STATUS/INIT register (774020) and determines that the BUSY bit is not set.
- Loads the CYLINDER ID register (774012) with a cylinder address.
- Loads the ERROR/PRECOMP register (774004) with the write precompensation cylinder address, if the address is not cylinder 128.

> **NOTE**
> **The ERROR/PRECOMP register is loaded with the write precompensation cylinder address during initialization. It is not necessary to load it during each operation.**

- Loads the HEAD ID register (774014) with a head number.
- Loads the BACKUP REV/SECTOR ID register (774006) with a sector address and backup revision information.
- Enables controller module interrupts if the host processor wants them.
- Loads the STA 2/COMMAND register (774016) with a command.
- Waits for either a DRQ interrupt or the BUSY bit to be reset, and the DRQ bit to be set in the STATUS/INIT register.

5.6.1.1 Read Sector Command Follow-up Sequence – After the controller module completes a read sector command, the host checks the error bit in the STA 2/COMMAND register. If the error bit is reset, the host moves the DATA BUFFER register contents to main memory. After each word transfer, the host waits for another DRQ interrupt or loops on the DRQ bit in the STATUS/INIT register.

Both the DRQ bit and the data request bit are set after each data word is loaded into the DATA BUFFER register. After all 256 words are read, the OP ENDED bit is set in the STATUS/INIT register. If interrupts are enabled an OP ENDED interrupt is generated.

5.6.1.2 Write Sector and Format Command Preparation – Before the controller module executes a write sector or a format command, the host moves the first data word from main memory to the data buffer register. after each word transfer, the host waits for another drq interrupt or loops on the DRQ bit in the status/init register.

Both the DRQ bit and the data request bit are set when the controller module is ready to load the next data word into the DATA BUFFER register. After all 256 words are loaded, the controller module executes the command.

5.6.1.3 Write Sector and Format Command Follow-up Sequence – The controller module indicates a completed command by resetting the BUSY bit and setting the OP ENDED bit in the STATUS/INIT register. If interrupts are enabled, the controller module generates an OP ENDED interrupt. The host processor checks the error bit in the STA 2/COMMAND register to determine error-free write sector or format command completion.

5.6.2 Read After Write Verify Follow-up Sequence

A read after write verify operation occurs when a read sector command follows a write sector command on the same sector. After the read command is complete, the host processor verifies the data written to the disk.

After loading a read sector command into the STA 2/COMMAND register, the host waits for the DRQ bit to set. The host then checks the error bit in the STA 2/COMMAND register to verify the data.

5.6.3 Restore Command

The host processor performs a restore command as follows.

- Enables controller module interrupts in the central processor unit (CPU) if the host processor wants them.
- Loads the STA 2/COMMAND register with the restore command code.
- Waits for an OP ENDED interrupt, or for the BUSY bit to be reset and the OP ENDED bit to be set in the STATUS/INIT register.
- The host processor determines that an error free restore command is completed by checking the error bit in the STA 2/COMMAND register.

5.6.4 Initialization Sequence

The controller module executes a reset/initialize sequence for the following conditions.

- During the power-up sequence
- When the CTI Bus signal INIT is asserted
- When the CTI Bus signal P OK is deasserted, then asserted
- When the host processor sets the RESET/INITIALIZE bit in the STATUS/INIT register

If any one of the above conditions occur, the microprocessor does the following.

- Sets the BUSY bit in the STATUS/INIT register
- Performs an internal initialize sequence
- Performs an internal memory test
- Clears the internal sector buffer
- Clears the CYLINDER ID, HEAD ID, and BACKUP REV/SECTOR ID registers
- Stores a default write precompensation cylinder address of 128 in the PRECOMP byte
- Clears the ERROR byte in the ERROR/PRECOMP register

NOTE

During a power-up initialization sequence, the disk drive performs an automatic restore to track 0.

- Resets the BUSY bit and sets OP ENDED bit when the initialization sequence is complete

NOTE

After an initialization sequence, the DRIVE READY and SEEK COMPLETE bits must be set in the STA 2/COMMAND register before the host processor accesses any register except the STATUS/INIT register.

5.7 SPECIFICATIONS

The following paragraphs list the RD controller module specifications.

5.7.1 Environmental

Specification	Minimum	Nominal	Maximim
Temperature	10°C (50°F)	–	50°C (104°F)
Humidity	20%	–	80%
Wet bulb reading	–	–	28°C (82°F)
Dew point	2°C (36°F)	–	–
Temperature fluctuation	–	–	20°C (36°F) per hour
Power dissipation	–	49 W (steady state)	83 W (drive spin up)

5.7.2 Power

Voltage	Current
+ 5 V	4.8 A
−12 V	200 mA
+12 V	100 mA

CHAPTER 6
RD50/RD51 HARD DISK DRIVE

6.1 GENERAL INFORMATION

The RD50 or RD51 hard disk drive is one of the storage components of the controller and drive subsystem for the Professional 300 Series computer system. Figure 6-1 shows the hard disk drive in relation to other system components.

6.1.1 Related Documentation

The *Professional 350 Field Maintenance Print Set* (MP-01394-00) provides more information about the RD50 hard disk drive.

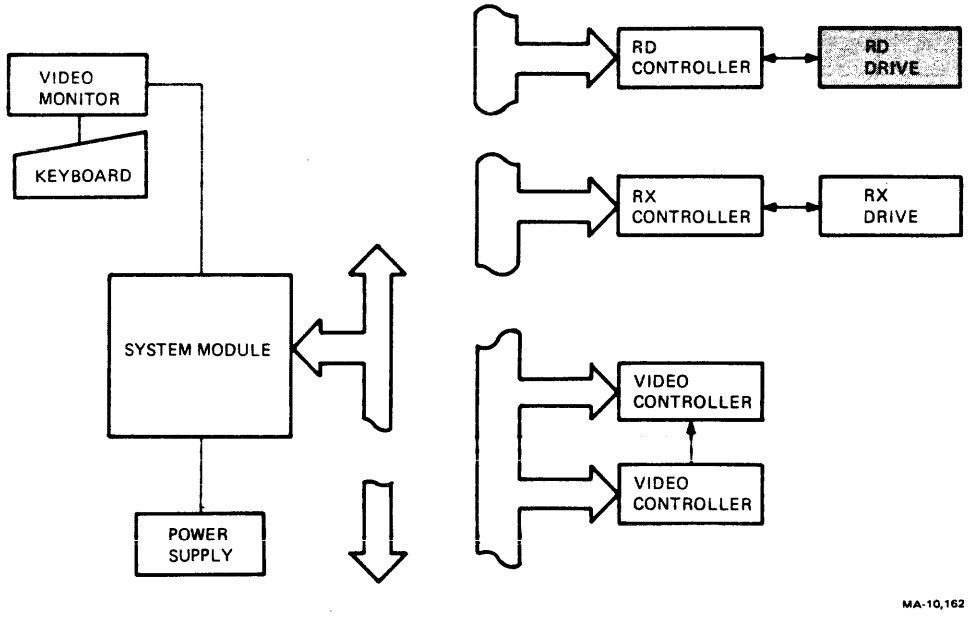


Figure 6-1 Hard Disk Drive System Relation

6.1.2 Hard Disk Drive

The hard disk drive, called a Winchester drive, is a 5.25 in (130 mm) nonremovable media disk drive. The disk drive allows the heads, which normally fly over the disk surface (media), to land when the disk drive is powered off. This disk drive uses lubricated media and lightly loaded (mechanically) read/write heads.

The RD50 disk drive stores 5 megabytes of data and the RD51 disk drive stores 10 megabytes of data.

High-bit densities on the media are achieved by flying the heads at a height of 20 microinches. This flying height requires a clean air environment. To ensure this, the head and disk assembly (HDA) is manufactured and sealed in an environmentally clean room.

A controller connects the disk drive to a host computer. The controller controls the drive operations and converts the data to or from the modified frequency modulation (MFM) format required by the disk drive.

6.2 FUNCTIONAL COMPONENTS

Paragraphs 6.2.1 through 6.2.8 describe the functions of the components that make up the disk drive.

6.2.1 Overview

The disk drive is a random access storage device, which uses two nonremovable 5.25-inch disks as storage media. Each disk surface uses one movable head to service 153 data tracks (306 tracks for the RD51). The disk drive's total formatted capacity is 5 megabytes – 16 sectors per track, 512 bytes per sector, 612 tracks per drive (1224 tracks for the RD51). Figure 6-2 shows the disk drive and Figure 6-3 shows the disk drives functional components.

This disk drive consists of a drive mechanism and two circuit modules. The drive mechanism contains the storage media and the supporting mechanical assemblies. One circuit module, the motor control module, contains the spindle motor control circuit. The other module, the read/write module, contains the following circuits.

Power-on circuit
Fault detection circuit
Seek circuit
Write circuit
Read circuit

Two connectors on the read/write module connect the disk drive to a controller module. A third connector on the read/write module connects the disk drive to a power source. A spring, located on the mounting plate, grounds the disk drive frame to the system chassis.

The disk drive is a field replaceable unit (PN RD50-A or RD51-A). The read/write module is a FRU of the disk drive (PN 29-24112-00). Chapter 5 in this document describes the two cables that connect the disk drive to a controller module. Chapter 10 in the *Professional 300 Series Technical Manual Volume I* describes the power cable that connects the disk drive to a power supply.

6.2.2 Drive Mechanism

The drive mechanism is a head and disk assembly (HDA) that contains a stepper motor, a head carriage assembly, a spindle motor, media, and sensors and hardware to support the HDA.

6.2.3 Spindle Motor Control Circuit

The spindle motor control circuit is located on the motor control module. This circuit keeps a brushless spindle motor rotating at a constant speed.

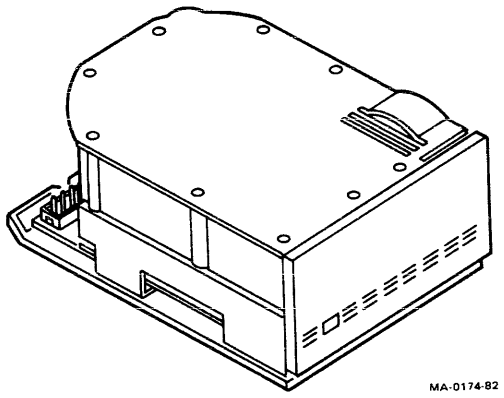


Figure 6-2 Hard Disk Drive

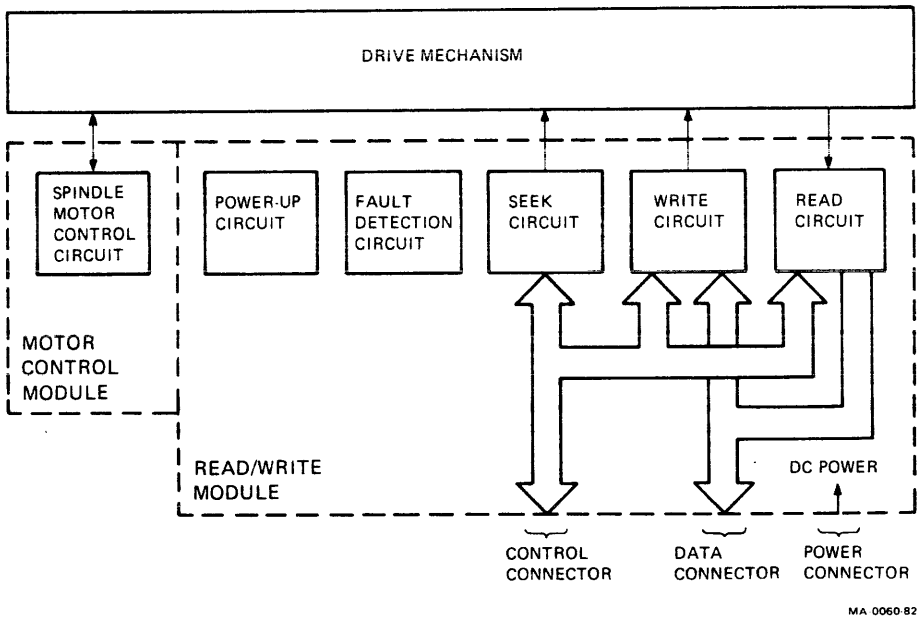


Figure 6-3 Simple Block Diagram

6.2.4 Power-Up Circuit

The power-up circuit provides the disk drive with a power-on sequence. This sequence allows the spindle motor time to rotate up to speed, forces a recalibration (recal) to the outer track of the media (track 0), and indicates that the disk drive is ready.

6.2.5 Fault Detection Circuit

The fault detection circuit monitors the disk drive for faults that could destroy stored data. When a fault is detected, this circuit generates a status signal for the controller module and disables the write circuit.

6.2.6 Seek Circuit

The seek circuit controls a stepper motor that actuates the head carriage assembly. This assembly positions the read/write heads over a data track. The seek circuit receives control signals directly from the controller module.

6.2.7 Write Circuit

The write circuit receives modified frequency modulated (MFM) data and control signals from the controller module. The circuit then generates the write current for the heads to store the data on the media as magnetic domains.

6.2.8 Read Circuit

The read/write heads sense the data recorded on the media. The read circuit then converts the data to MFM data pulses.

6.3 THEORY OF OPERATION

Paragraphs 6.3.1 through 6.3.7 describe the disk drive functions.

6.3.1 Drive Mechanism Detailed Operations

The drive mechanism is an HDA with supporting sensors and hardware. The sealed HDA consists of the following items.

Stepper motor and head carriage assembly
Spindle motor assembly and speed sensor circuit
Filters

The supporting sensors and hardware consist of the following items.

Index sensor
Track 0 sensor
Spindle brake
Spindle ground spring
Drive select indicator (LED)

6.3.1.1 Sealed Head and Disk Assembly (HDA) – The following paragraphs describe the items contained in the sealed head and disk assembly.

NOTE

The HDA is an environmentally sealed unit. Opening this unit or breaking its seals destroys the data stored on the media and the disk drive's reliability.

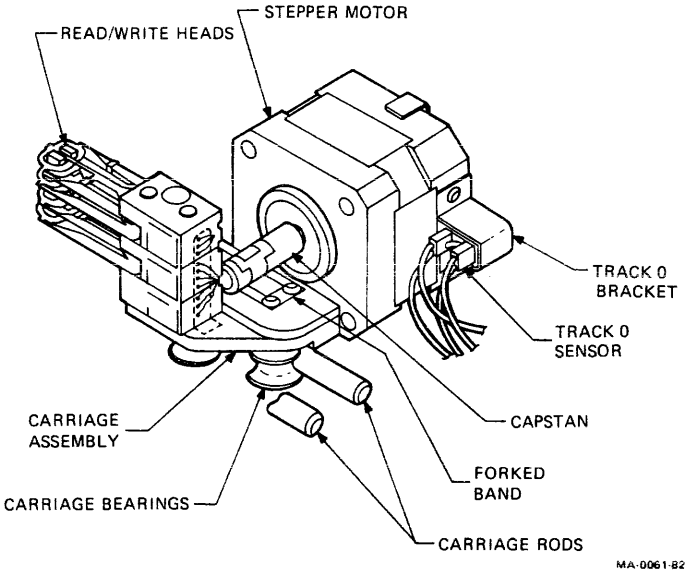
Stepper Motor and Head Carriage Assembly

Figure 6-4 shows the stepper motor and head carriage assembly. This assembly moves the flying read/write heads across rotating media and positions them over the data tracks. These tracks are 4000 microinches apart, and require close tolerances between all mechanical parts.

Three bearings rotate on shafts connected to the head carriage assembly. Each bearing makes a 2-point contact to a carriage rod. The bearings are arranged so that the two inner bearings roll on a common carriage rod and the outer bearing rolls on a second carriage rod.

A forked band wraps around the stepper motor's capstan and attaches to the head carriage assembly. As the stepper motor capstan rotates, the head carriage assembly moves out towards track 0, or in towards track 152.

The capstan rotates in 0.9 degree increments, called half steps. Two stepper motor cycles, or 1.8 degree of rotation, move the heads one full track.



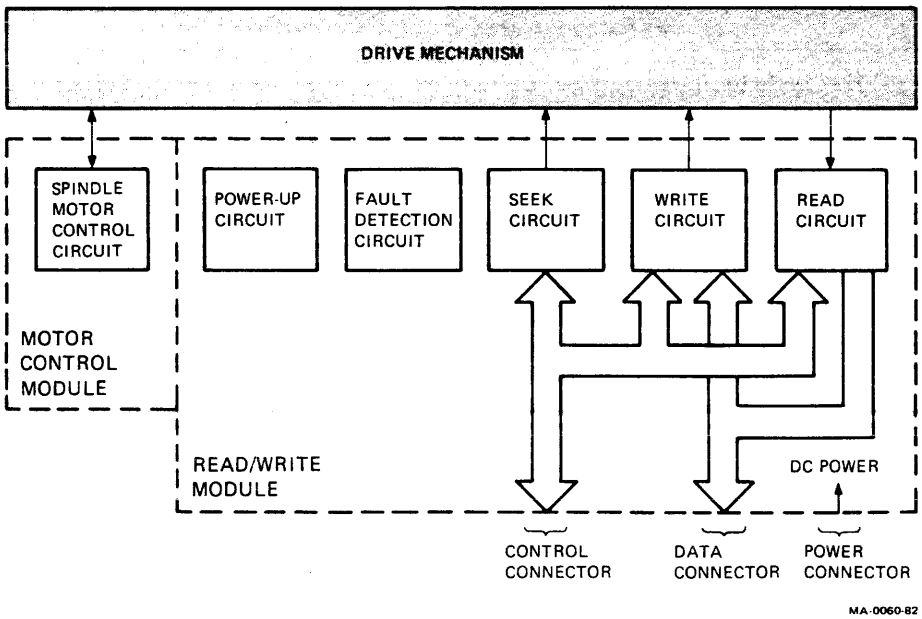


Figure 6-4 Stepper Motor and Head Carriage Assembly

Spindle Motor Assembly and Speed Sensor Circuit

NOTE

The spindle motor assembly is part of the HDA. Removing or disassembling this unit destroys the data stored on the media and the disk drive's reliability.

The spindle motor assembly consists of two disks attached to a spindle and rotated constantly at 3600 rpm by a brushless dc motor. A speed sensor circuit in the spindle motor sends a signal, which represents the spindle motor speed, to the spindle motor control circuit. The spindle motor control circuit then controls the spindle motor speed.

As the motor rotates the disks (media), an air cushion between the read/write heads and the media is created. This air cushion causes the heads to fly above the media at an average height of 20 microinches. This distance allows high density data recording.

When power is removed from the disk drive, the motor and media slow down and stop rotating. This removes the air cushion and allows the heads to land on the media.

Filters

NOTE

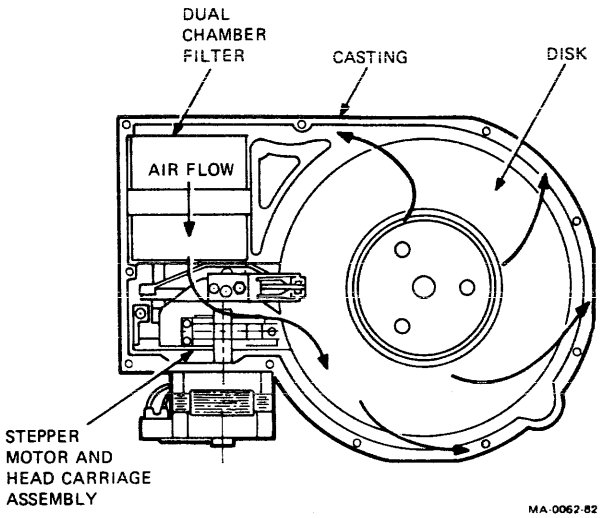
The filters are part of the HDA. Disassembling the HDA to access the filters destroys the data stored on the media and the disk drive's reliability.

The stepper motor, head carriage assembly, and spindle motor are all environmentally sealed in a casting. An air filtration system inside the sealed casting removes particles that would damage the heads and media.

The filtration system consists of a dual chamber filter. One chamber removes 0.3-μm particles from the air. The maintenance-free filter ensures clean air inside the sealed HDA for the life of the disk drive.

The other chamber is a filtered vent that allows pressure equalization between the sealed HDA and the outside environment. During normal operation there is no measurable air flow between the HDA and the outside environment.

Figures 6-5 and 6-6 show the air flow through the filtration system.



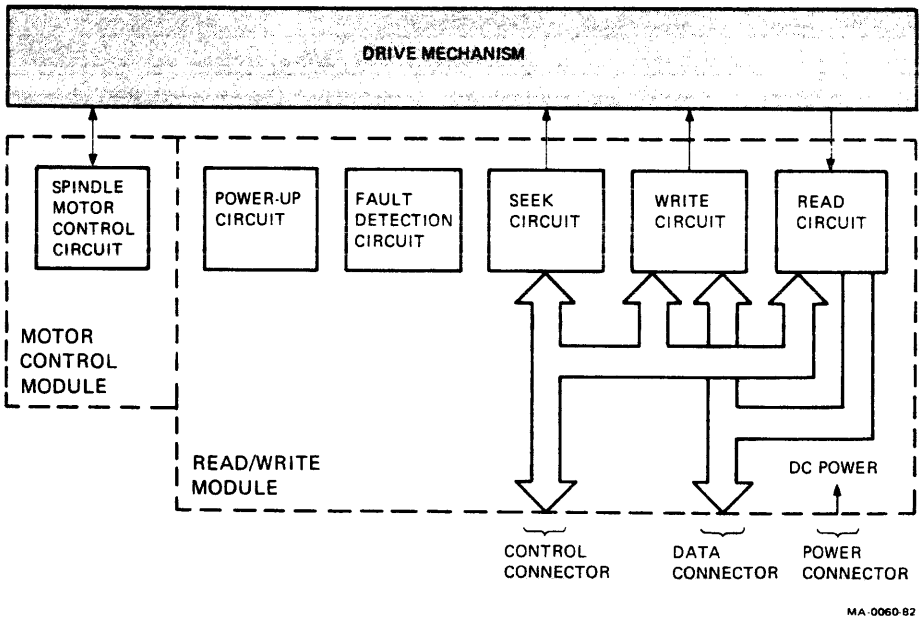
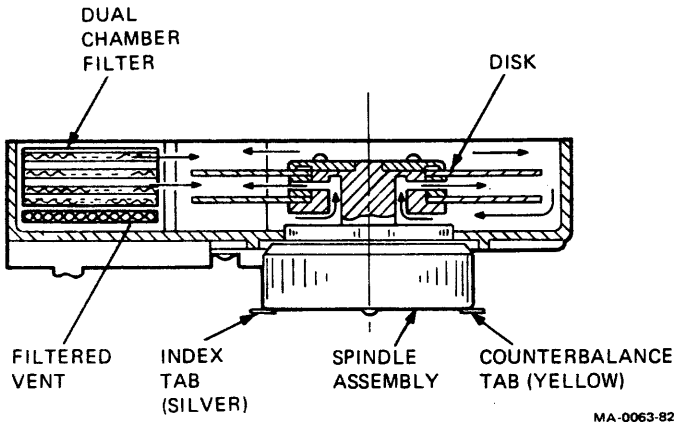


Figure 6-5 Air Flow Top View



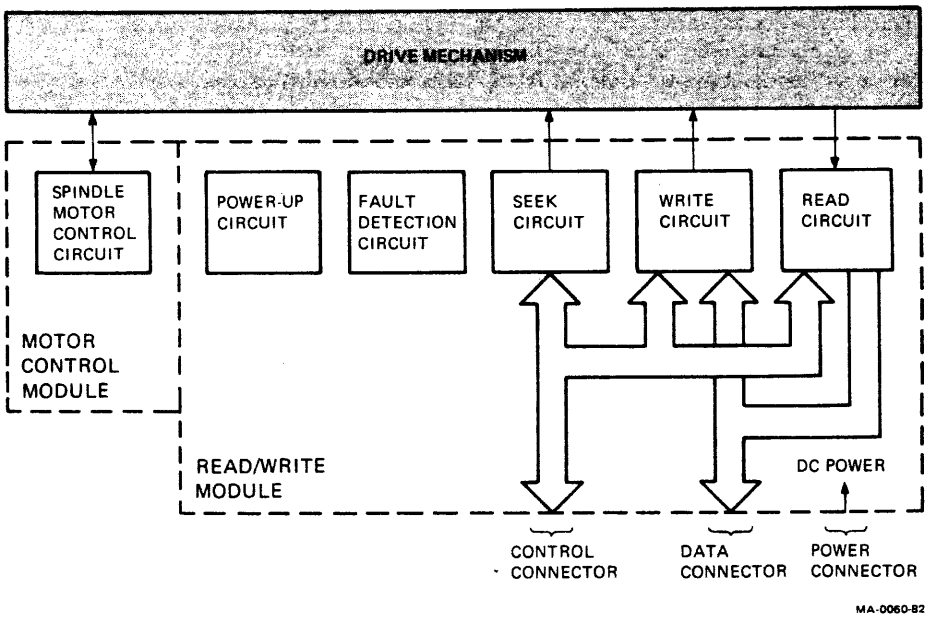


Figure 6-6 Air Flow Side View

6.3.1.2 Sensors and Hardware – The following paragraphs describe the drive mechanism's sensors and hardware.

Index Sensor
The spindle motor hub has two tabs. One tab is a ferrous metal tab used by the index sensor. The other tab is a nonferrous metal tab used for counter balancing. The index sensor is a transistor that responds to magnetic field variations. This response is called a *hall* effect. The index sensor is mounted on the HDA. The sensor is 0.030 inches away, at its closest point, from the ferrous metal tab on the spindle hub.

The ferrous tab distorts the sensor's magnetic field. The sensor generates a pulse (INDEX SENSE) to the write circuits in the read/write module.

Track 0 Sensor

NOTE
The track 0 sensor position is set when the drive mechanism is manufactured. Replacing or adjusting this sensor alters the position of track 0.

The track 0 sensor consists of an infrared light emitting diode (LED), a photo sensitive transistor, and a light interrupting tab on the stepper motor shaft. When the tab interrupts the light from the LED to the photo sensitive transistor, the transistor turns off. This generates a signal (TRK 0 SENSE) for the read/write module. This sequence occurs when the heads are near track 0.

Spindle Brake
A brake is mounted on the HDA near the spindle hub. This spindle brake minimizes head flutter, which occurs when the spindle motor slows down after power is removed from the disk drive. Head flutter is when the heads bounce over the media. This occurs when the slower disk rotation creates an unstable air cushion.

The spindle brake is a solenoid actuated brake pad. It is mounted on the HDA so that the brake pad is 0.010 inches from the spindle hub. When power is applied to the motor control module, the solenoid is activated. The activated solenoid pulls the brake pad away from the spindle hub, which allows the hub to spin freely.

When power is removed from the solenoid, the brake pad contacts and slows down the hub. This allows the heads to land on the media quickly, extending the life of the media and the heads.

Spindle Ground Spring
The spindle ground spring provides a discharge path for static electricity that builds up on the spindle and the media. This spring is bolted to the HDA so that a carbon contact touches the metal cone at the spindle motor's base. This contact discharges static electricity from the HDA.

Drive Select Indicator
The drive select indicator on the disk drive's front bezel comes on if the controller module has selected the RD50 disk drive. The controller module controls this indicator.

6.3.2 Spindle Motor Control Circuit Detailed Operations

The spindle motor control circuit is on the motor control module (Figure 6-7). The spindle motor control circuit performs the following functions.

- Provides the maximum allowable current to the spindle motor when power is first applied. This rapidly brings the motor up to speed.
- Monitors the speed of the motor and adjusts the current driving the motor. This keeps the motor rotating at a constant speed.

The spindle motor control circuit performs these functions in two stages. In the first stage, the HALL IN signal sets the current level required by the spindle motor. In the second stage, the HALL IN signal switches the current between the two spindle motor driver coils. This action produces the magnetic fields required by the spindle motor.

The motor control module receives +12 Vdc power from a power supply. This power is routed directly to a connector for the brake and a +6.2 Vdc regulator. The regulator provides operating voltages to the motor control module and a speed sensor circuit in the spindle motor.

6.3.2.1 Motor Current Control – Current coupled to the spindle motor is controlled by a speed comparator, a constant pulse width generator, and an integrator. These three circuit segments set the current level for the current drivers, and operate in two modes: start up and normal operation.

The speed comparator's output drives both the integrator and the constant width pulse generator. During start up the speed comparator controls the integrator, which provides the maximum current to the current drivers. As the spindle speed increases to normal, the speed comparator minimizes its effect over the integrator, and the constant width pulse generator controls the integrator.

The speed comparator receives the HALL IN signal from a speed sensor circuit in the spindle motor. This signal's frequency is twice the motor speed.

The speed comparator uses the falling edge of the HALL IN signal to discharge its capacitor. The capacitor's charge rate is set at the factory. The frequency of discharge and the charge rate together determine the width of a falling pulse from the comparator to the constant pulse width generator and integrator.

The constant pulse width generator uses the falling edge of the pulse from the speed comparator to generate a constant width falling pulse for the integrator. The average voltage level of these pulses represents the amount of current required by the spindle motor to maintain 3600 rpm.

When the spindle motor rotates slower than 3600 rpm, the ratio of falling pulse widths to rising pulse widths is greater than the established average. This causes the integrator to generate a higher average voltage. This voltage represents a higher current coupling by the current drivers, which causes the motor to speed up.

When the motor rotates faster than 3600 rpm, the ratio of falling pulse widths to rising pulse widths is less than the established average. This causes the integrator to generate a lower average voltage. This voltage represents a low current coupling by the current drivers, which causes the motor to slow down.

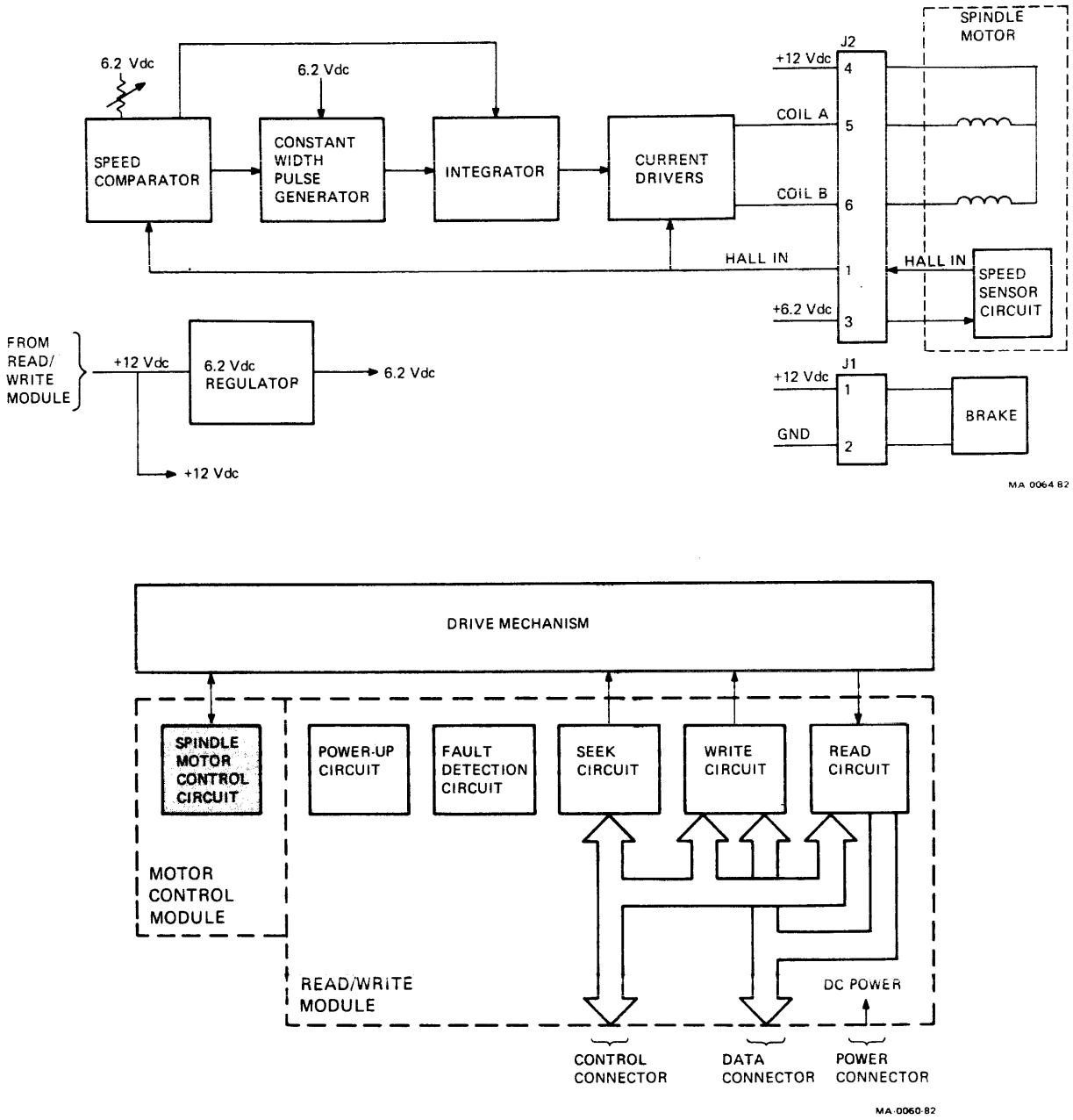


Figure 6-7 Spindle Motor Control Circuit Detail

6.3.2.2 Spindle Motor Current Switching – The current drivers switch the current between the spindle motor's two coils and act as a current limiter. These drivers are controlled by the integrator and the HALL IN signal from the spindle motor.

The current drivers normally operate within their linear amplifying range except when power is first applied. The integrator output level saturates the drivers when power is first applied, which provides the maximum current for the coils. This causes the motor to come up to speed quickly.

During normal operation the integrator output controls the level of current that the drivers provide through the motor coils, while the HALL IN signal switches the drivers to provide current through coil A or coil B.

If the motor is obstructed from rotating when the power is on, the drivers are permanently damaged. This prevents overloading the coils and damaging the spindle motor in the HDA.

6.3.3 Power-up Circuit Detailed Operations

The power-up circuits provide the disk drive with a power-up sequence. This sequence begins when either of the following conditions occur.

- Power is first applied to the drive.
- Power goes out of tolerance, then back into tolerance.

The power-up sequence initializes the drive as follows.

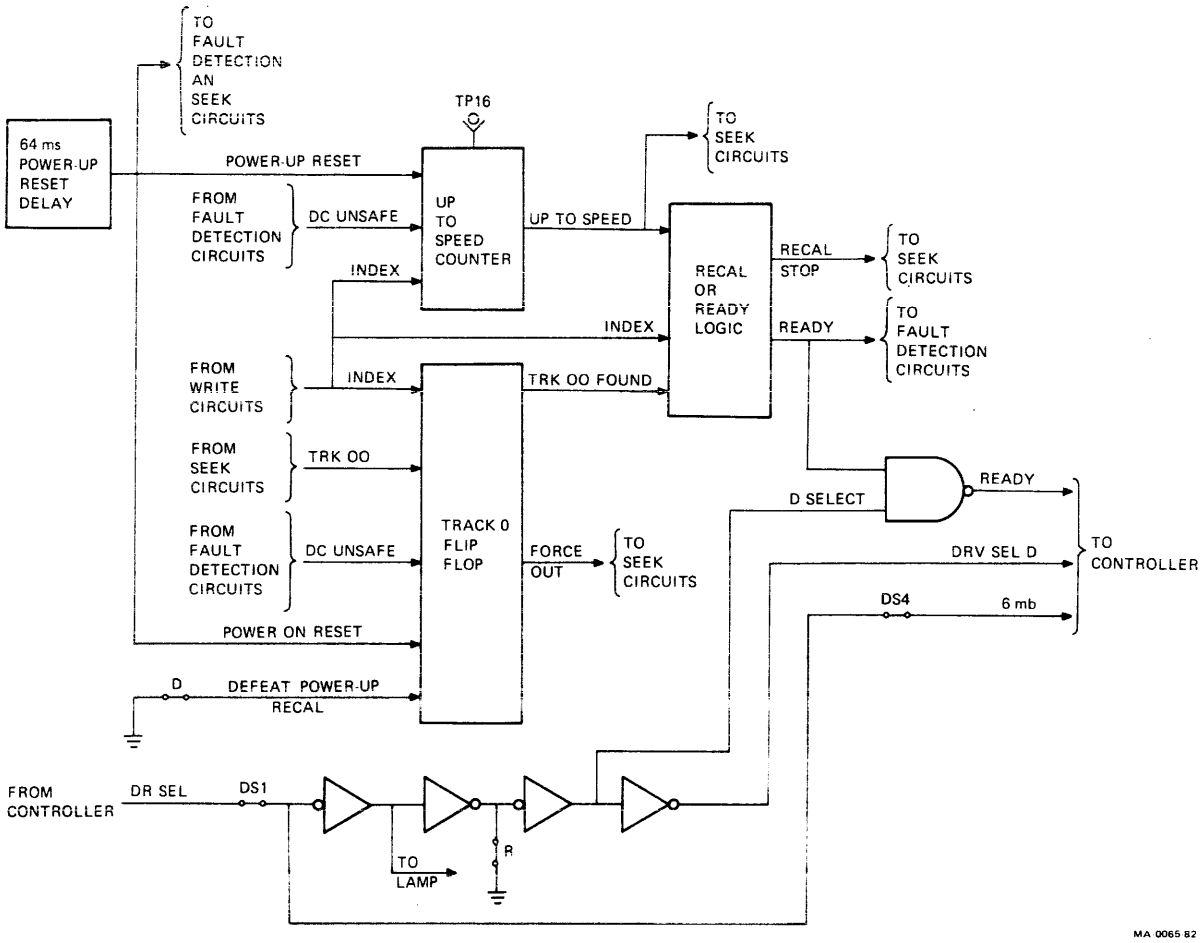
1. Generates a 64 ms POWER-ON RESET signal after the +5 Vdc current stablizes.
2. Counts 512 index pulses then generates the UP TO SPEED signal.
3. Generates recalibration signals for the seek circuit until the heads are over track 0.
4. Generates a READY signal when the heads are over track 0.

Figure 6-8 shows the power-up circuit in detail. Figure 6-9 shows a timing diagram and the relationship between drive control signals and signals generated by the power-up circuit.

6.3.3.1 Reset Signal Generation – When the system is first powered up, a POWER-UP RESET signal is asserted. This signal stays asserted for 64 ms after the +5 Vdc stabilizes, and resets the power-up, fault detection, and seek circuits.

6.3.3.2 Up to Speed Signal Generation – An up-to-speed counter controls an UP TO SPEED signal. This counter is reset when the POWER-UP RESET signal is asserted, or when the fault detection circuit asserts the DC UNSAFE signal.

This counter counts 512 index pulses from the write circuit after the power is stabilized, then asserts an UP TO SPEED signal. This signal enables the seek circuits and the recalibration or ready logic in the power-up circuit.



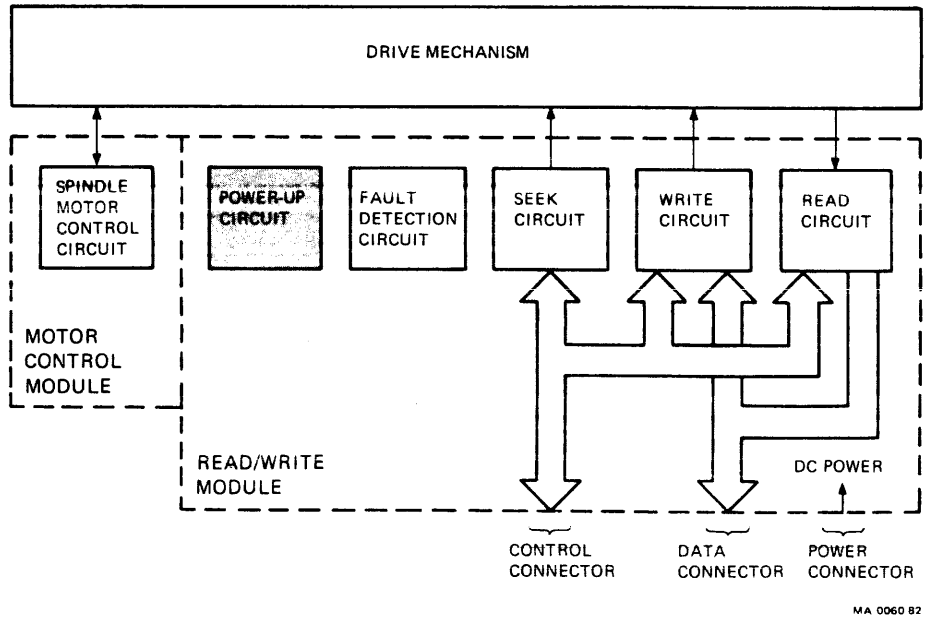


Figure 6-8 Power-up Circuit Detail

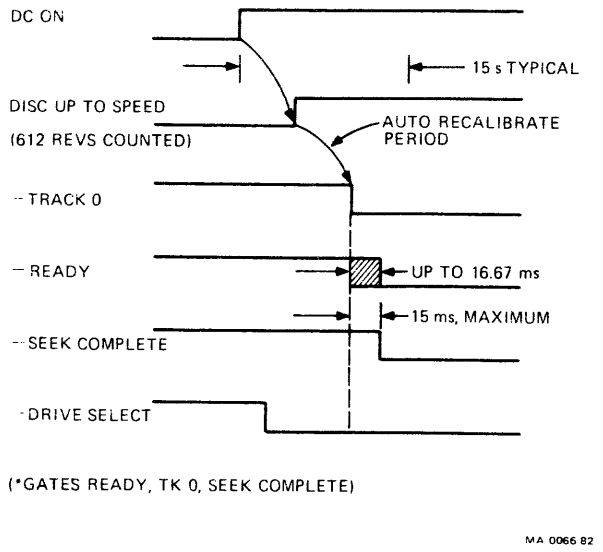


Figure 6-9 Power-up Sequence Timing

6.3.3.3 Recalibration Signal Generation – The power-up circuit controls two signals that recalibrate the disk drive to track 0: FORCE OUT and RECAL STEP. Both of these signals control the seek circuit to move the heads to track 0.

A track 0 flip-flop is reset by a POWER-UP RESET or a DC UNSAFE signal from the fault detection circuit. Resetting the flip-flop deasserts the TRK00 FOUND signal and asserts the FORCE OUT signal. The index pulse clocks the flip-flop with the state of the TRK00 signal. If the TRK00 signal is not asserted, the FORCE OUT signal remains asserted. If the TRK00 signal is asserted, the TRK00 FOUND signal is asserted and the FORCE OUT signal is deasserted.

The recalibration or ready logic is enabled when the UP TO SPEED signal is asserted. If the TRK00 FOUND signal is deasserted, the index signal generates RECAL STEP signals for the seek circuit. If the TRK00 found signal is asserted, the RECAL STEP signal is inhibited.

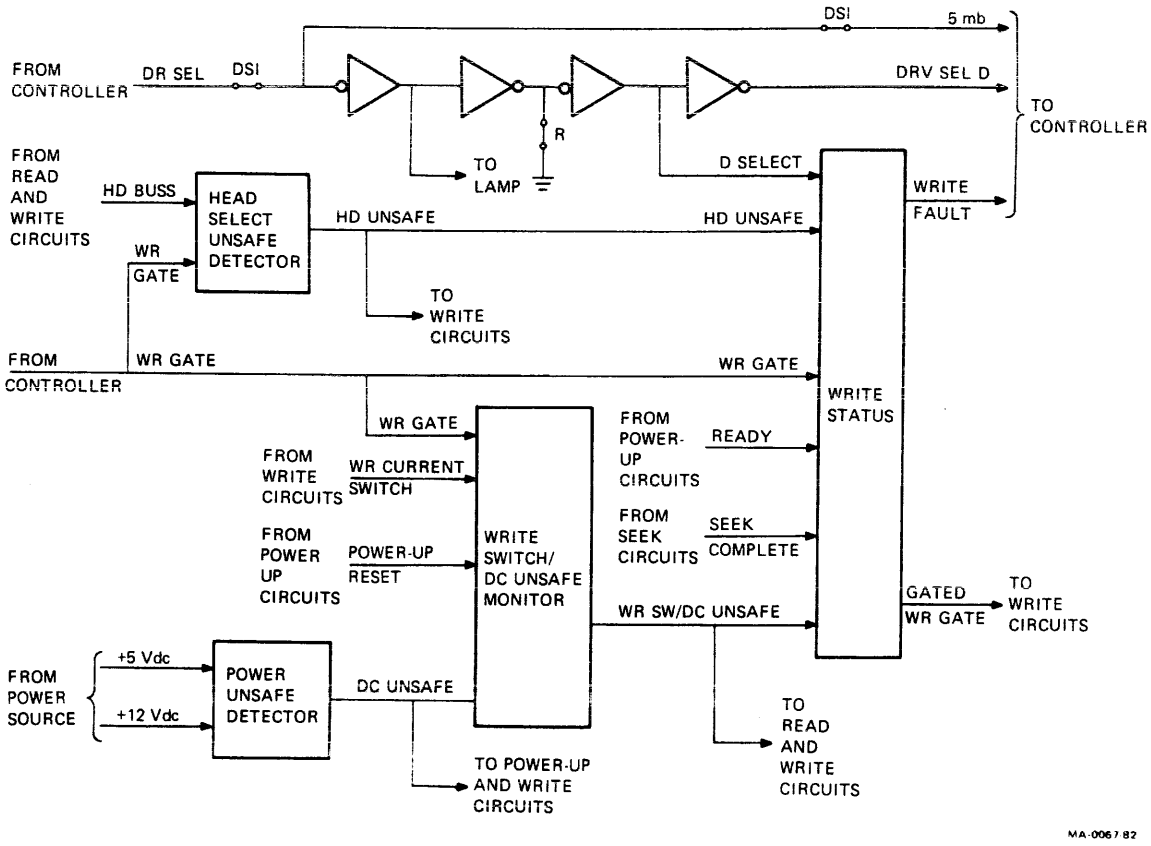
6.3.3.4 Ready Signal Generation – The recalibration or ready logic generates a ready signal for the fault detection circuit and the controller module. When the up-to-speed counter asserts the UP TO SPEED signal and the track 0 flip-flop asserts the TRK00 found signal, the READY signal is asserted. The READY signal indicates that the drive is initialized and ready to operate.

The logic state of the READY signal passes to the controller module when the drive select (DSELECT) signal is asserted. This signal asserts when the drive select (DRSEL) signal from the controller module is asserted, or when the radial jumper R is in place (Figure 6-9).

6.3.3.5 Recalibration Signal Generation Deselection – Recalibration signal generation during a power-up sequence can be prevented. A defeat power-up recalibration jumper must be in place to preset the track 0 flip-flop. The remaining sequences, power-up reset and up-to-speed, become the power-up sequence.

6.3.4 Fault Detection Circuit Detailed Operation

The fault detection circuit monitors the read/write module to protect the recorded data and read/write heads during circuit malfunctions, illegal operations, or commands. If faults are detected, the fault detection circuits disable or reset circuits on the read/write module. If no faults are detected, the fault circuit generates an enable signal for the write circuit. Figure 6-10 shows the fault detection circuit in detail.



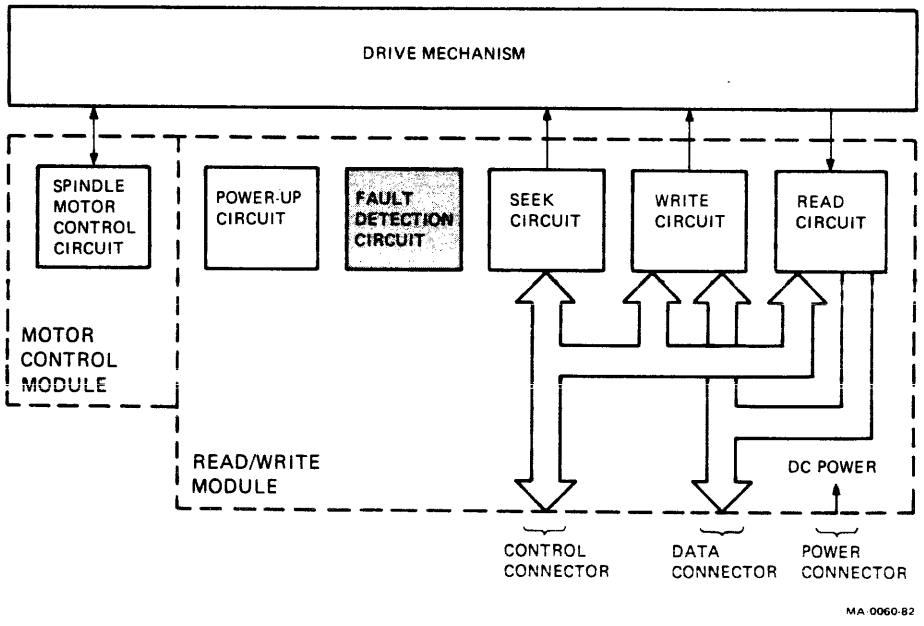


Figure 6-10 Fault Detection Circuit Detail

The fault circuit monitors the read/write module for the following faults.

Head selection malfunction
Unsafe voltage levels
Unsafe write circuit

6.3.4.1 Head Selection Malfunction Detection – The head select unsafe detector receives two signals: HD BUSS from the read and write circuits and WR GATE from the controller module. This detector monitors HD BUSS and WR GATE for the following faults.

- No head is selected.
- More than one head is selected.
- A head is selected for a read operation when a write operation is to be performed.
- A head is selected for a write operation when a read operation is to be performed.

If one of these faults exists, a HD UNSAFE signal is asserted, which inhibits the write circuit from operating. If none of these faults exist, the HD UNSAFE signal is deasserted. The HD UNSAFE signal is used by the write circuit and the write status logic in the fault detection circuit.

6.3.4.2 Power Unsafe Detection – The power unsafe detector monitors the +5 Vdc and +12 Vdc levels. If the level of either voltage is out of tolerance, the detector asserts a DC UNSAFE signal for the power-up, write, and seek circuits.

The following power levels are unsafe.

- If the +5 Vdc falls below 4.3 Vdc
- If the +12 Vdc falls below 9.5 Vdc

6.3.4.3 Write Circuit Unsafe Detection – The write circuit functions are monitored by the write switch/dc unsafe monitor. This monitor asserts a write current switch fault or power unsafe signal (WR SW/DC UNSAFE) to disable the write and read circuits.

The WR SW/DC UNSAFE signal is asserted if any of the following conditions exist.

- The write function is selected but no write current exists.
- A write current exists but the write function is not selected.
- The dc power is unsafe.
- The power-up reset signal is asserted.

6.3.4.4 Write Status Detection – The write status monitor generates two signals: a WRITE FAULT signal for the controller module and a GATED WR GATE for the write circuit. An asserted WRITE FAULT signal indicates that a fault exists in the disk drive. An asserted GATED WR GATE signal indicates that the proper conditions exist for performing a write function.

The state of the WRITE FAULT signal is sent to the controller module when the controller module selects the disk drive by asserting DRSEL, or by installing jumper R.

The WRITE FAULT signal is asserted when *any* of the following conditions exist.

A head unsafe condition exists.
The dc power is unsafe.
The write circuit is unstable.

A GATED WR GATE signal is asserted when *all* of the following conditions exist.

No faults are detected.
The power-up circuit asserts the READY signal.
The seek circuit asserts the SEEK COMPLETE signal.

6.3.5 Seek Circuit Detailed Operation

The seek circuit generates control signals for a stepper motor to move the read/write heads over any one of the tracks. This circuit is controlled by the controller module or the power-up circuit during a power-up sequence. Figure 6-11 shows the seek circuit in detail.

The seek circuits are inhibited from operating during the power-up sequence by the power-up circuit (POWER-UP RESET asserted), or during a dc-unsafe condition by the fault detection circuit (DC UNSAFE asserted). Inhibiting the seek circuits at these times protects read/write heads from damage.

The seek circuit generates stepper motor control signals as follows.

- Selects the direction to move the heads
- Receives step pulses
- Converts step pulse and direction signals to stepper motor control signals
- Monitors for a track 0 head location
- Indicates when the seek circuit is operating

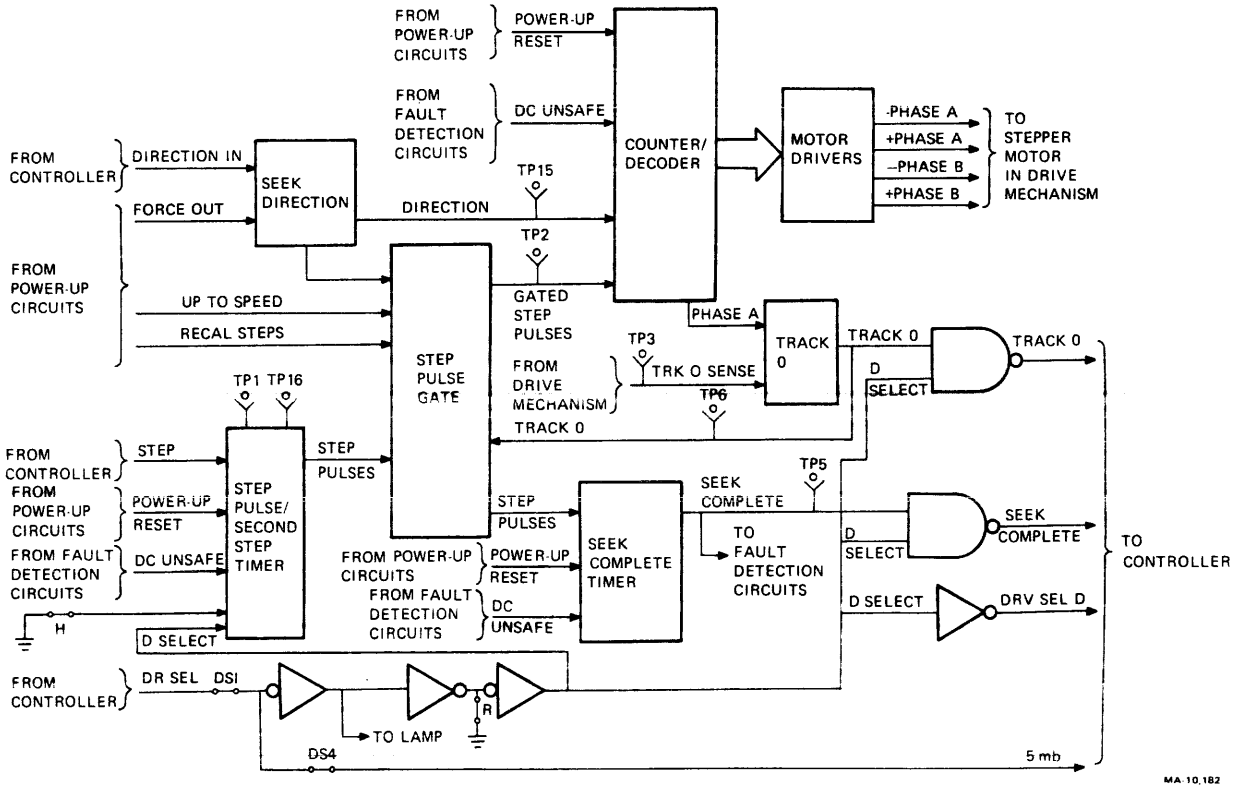


Figure 6-11 Seek Circuit Detail

6.3.5.1 Head Direction Selection – The controller module controls the direction that the heads move, toward the center of the disk or toward track 0. When the controller module asserts the DIRECTION IN signal, the heads move toward the center of the disk. When the controller mocule deasserts the DIRECTION IN signal, the heads move toward track 0.

During a power-up sequence the power-up circuit asserts a FORCE OUT signal. This signal selects head movement toward track 0.

6.3.5.2 Step Pulse Selection – Step pulses are normally generated for the counter/decoder by signals that the seek circuit receives from the controller module. The controller module sends step pulses and a DRSEL (DSELECT) signal to a step pulse/second step one shot. This one shot operates in both double-step or single-step modes.

The step pulses then pass through a step pulse gate. This gate passes these pulses from a step pulse/second step one shot, or the power-up circuit (RECAL STEP), as gated step pulses. This occurs when the following conditions exist.

- The UP TO SPEED signal from the power-up circuit is asserted.
- A head movement direction towards the center of the disk is selected when the heads are at track 0.

The controller module will burst pulses to the disk drive. These pulses will be accepted until the time after the last pulse exceeds 200 μs or until all step pulses are received. At either of these conditions the disk drive microprocessor stops accepting step pulses from the controller module and begins issuing step pulses to the stepper motor. Depending on the length of the seek, the microprocessor will select the optimum algorithm.

The RD51 disk drive's buffered seek operation significantly improves its seek performance as compared to the RD50 disk drive (which does not have this feature).

6.3.5.3 Step Pulse and Direction Signal Conversion – A counter/decoder and the motor drivers convert the direction and gated step pulses to stepper motor control signals. The DIRECTION signal causes the counter/decoder to count up or count down. The gated step pulses clock the counter in the counter/decoder.

The counter's output is decoded to generate signals that select the motor drivers. The motor drivers then generate the following motor control signals for the stepper motor.

−PHASE A
+PHASE A
−PHASE B
+PHASE B

6.3.5.4 Track 0 Monitoring – The seek circuits monitor for a track 0 head location. When the heads are over track 0, a TRACK 0 signal is asserted. The power-up circuit, step pulse gate, and controller module (TRACK000) use this signal. When the drive is selected, DSELECT is asserted.

The TRACK 0 signal is generated when the sensor on the disk drive mechanism asserts a TRK 0 SENSE signal, and the counter/decoder indicates a PHASE A stepper motor position.

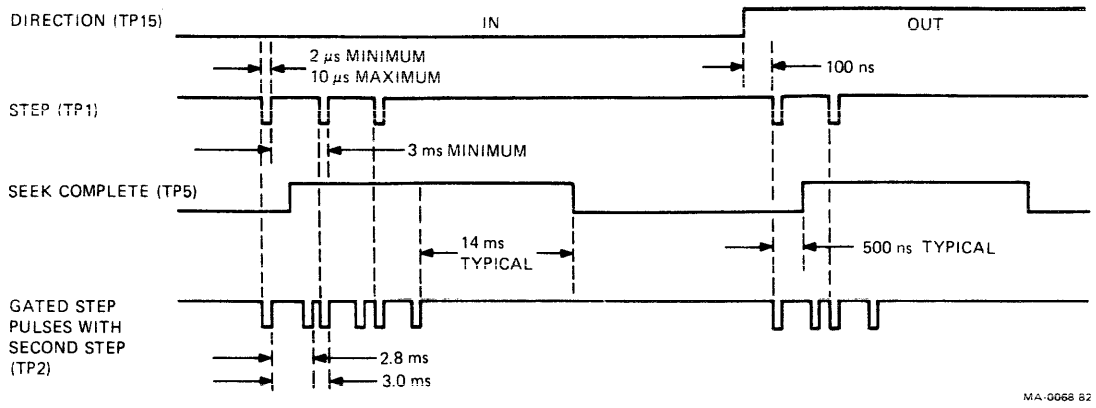


Figure 6-12 Seek Circuit Timing

6.3.5.5 Seek Complete Indicator – The seek complete timer monitors the step pulses. This timer asserts a SEEK COMPLETE signal when the seek circuit does not receive a step pulse for 14 ms or more (Figure 6-12). The SEEK COMPLETE signal is used by the fault detection circuit and the controller module.

6.3.6 Write Circuit Detailed Description

The write circuit converts MFM encoded data from the controller module to current pulses for the head coils. This creates a high flux magnetic field that orients the oxide coating on the media to form magnetic domains.

Figure 6-13 shows the write circuit in detail. Timing relationships between data and command signals (Figure 6-14) are described as follows.

A differental receiver, when enabled by the controller module (DSELECT asserted), passes encoded data (MFM WRITE DATA) to a flip-flop. This divides the data by two, which creates a rectangular wave that represents flux transitions. The MFM WRITE DATA signal drives a differential write switch (Figure 6-13).

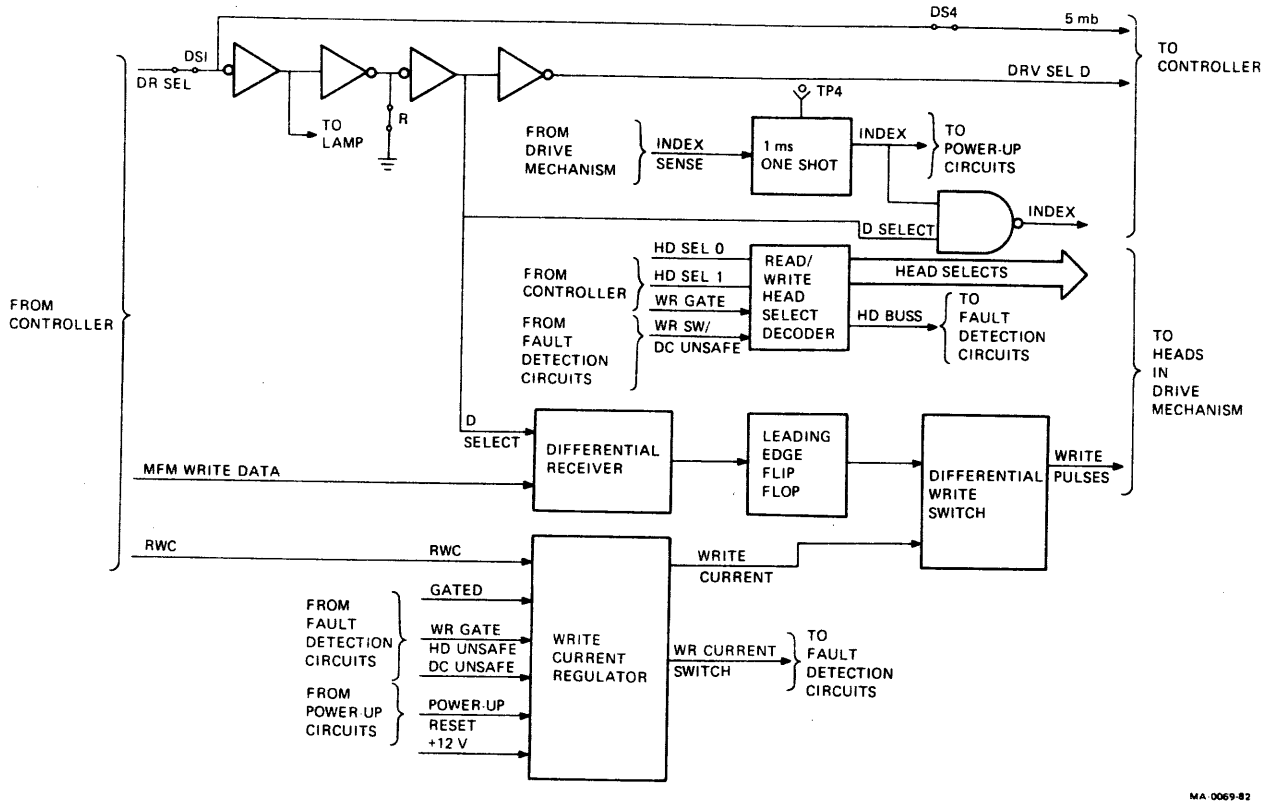
The differential write switch, when provided with WRITE CURRENT, controls the currents that drive a center-tapped read/write coil. The current reverses at each edge of the rectangular wave. Reversing the current creates alternating magnetic fields in the coils and magnetic domains on the media.

A write current regulator provides the WRITE CURRENT signal to the differential write switch. The regulator is also enabled and disabled by the fault detection and power-up circuits.

The write current regulator provides two levels of write current. The reduce write current (RWC) controlier signal selects these levels. One level of write current is used for recording data on the first half of the disk, RWC unasserted. The other current level is used for the second half of the disk, RWC asserted.

When the differential write switch generates the write currents, a read/write head select decoder asserts one of four head select signals for one of the four read/write heads. Each head select connects to the center tap of a read/write coil. The coils are selected for a write function by the controller module (HD SEL 0, HD SEL 1, and WR GATE). The fault detection circuits disable the decoder when WR SW/DC UNSAFE is asserted.

A one shot in the write circuit converts the INDEX SENSE signal from the drive mechanism to a 1 ms pulse (Figure 6-15). This pulse is a reference signal that indicates the start of the track. It is used by the power-up circuits and the controller module.



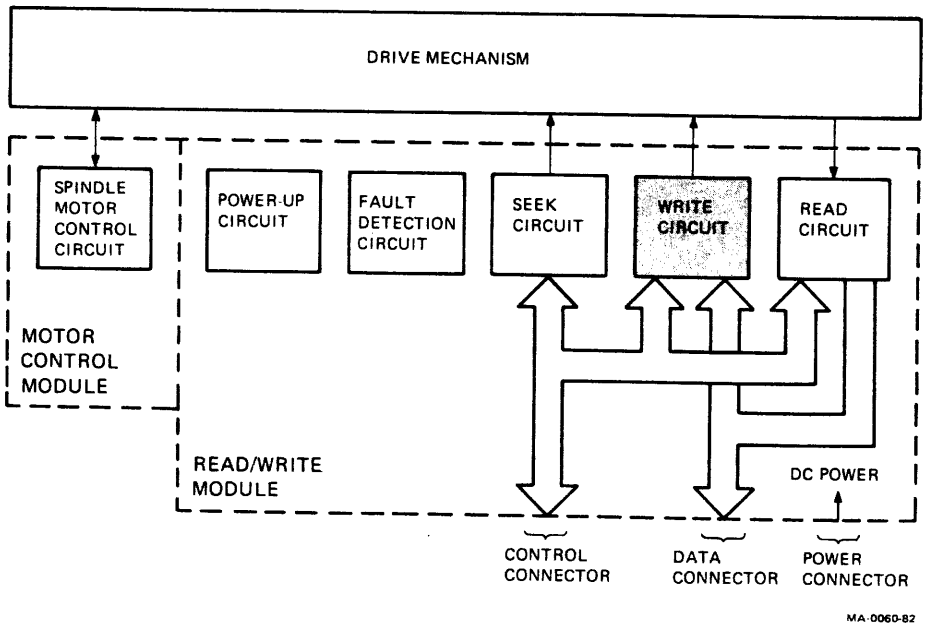


Figure 6-13 Write Circuit Detail

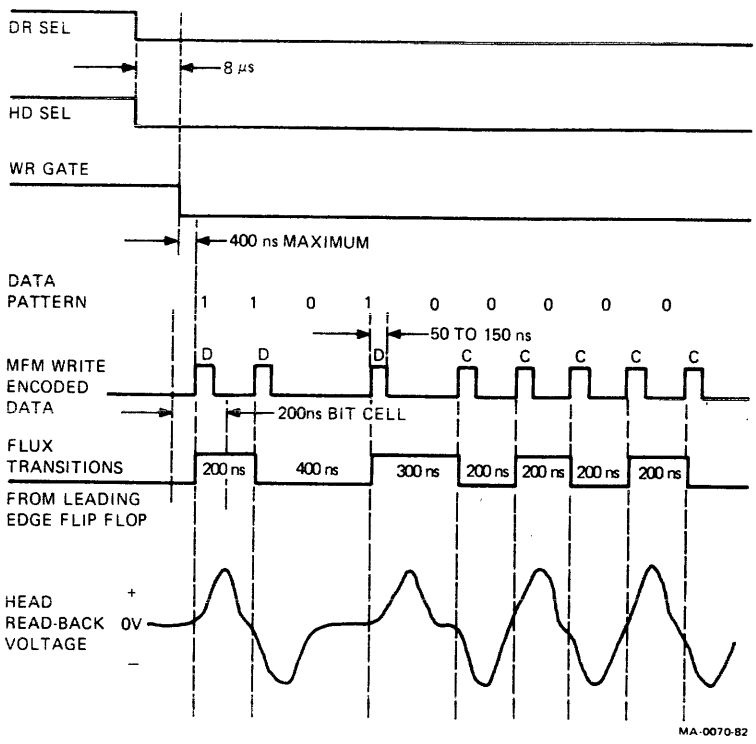


Figure 6-14 Write Data Timing

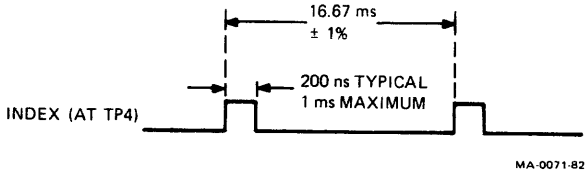


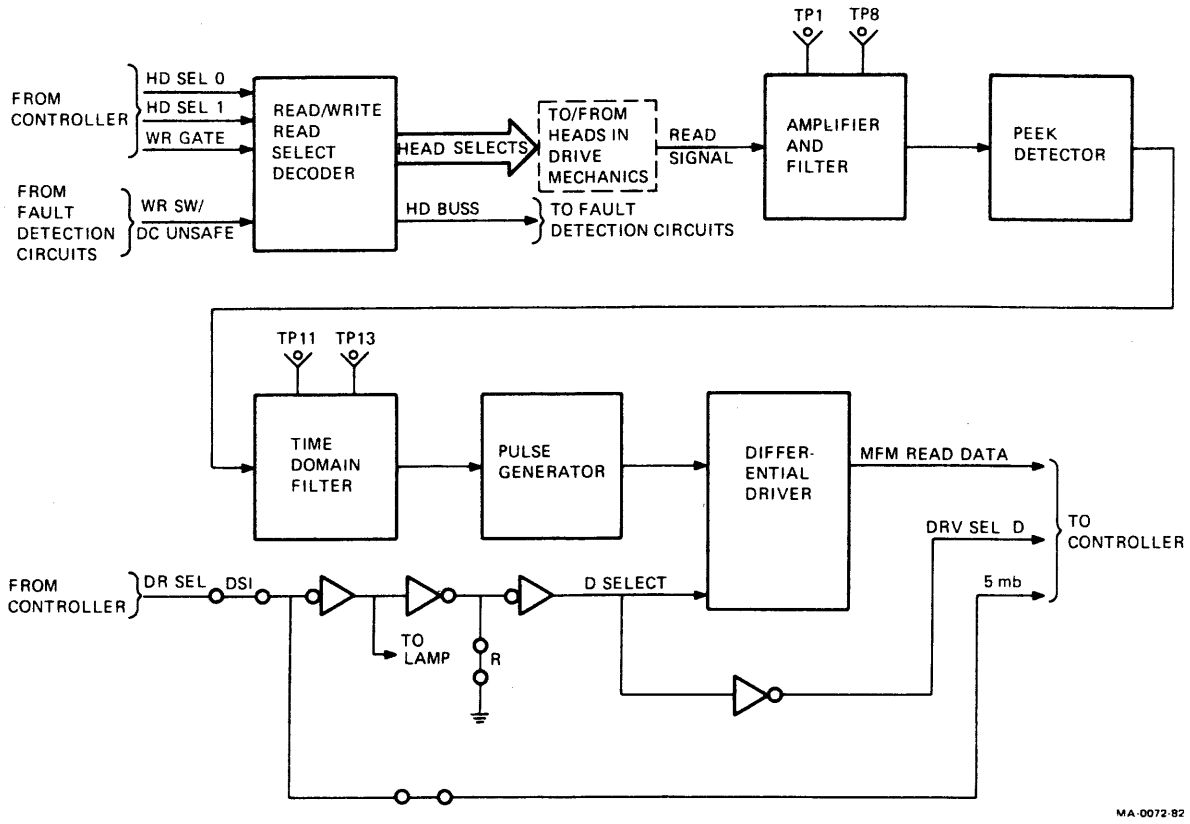
Figure 6-15 Index Signal Timing

6.3.7 Read Circuit Detailed Description

The read circuit converts flux transitions sensed by the read/write heads to MFM data pulses. The flux transitions reside on the media from previous write functions.

Figure 6-16 shows the read circuit in detail. Timing relationships between data and command signals (Figure 6-17) are described as follows.

For the amplifier/filter to receive a correct signal from the heads, the read/write head select decoder asserts one of four head select signals for one of the four read/write heads. Each head select connects to the center tap of a read/write coil. The coils are selected for a read function by the controller module (HD SEL 0, HD SEL 1, and WR GATE). The fault detection circuits disable the decoder when WR SW/DC UNSAFE is asserted.



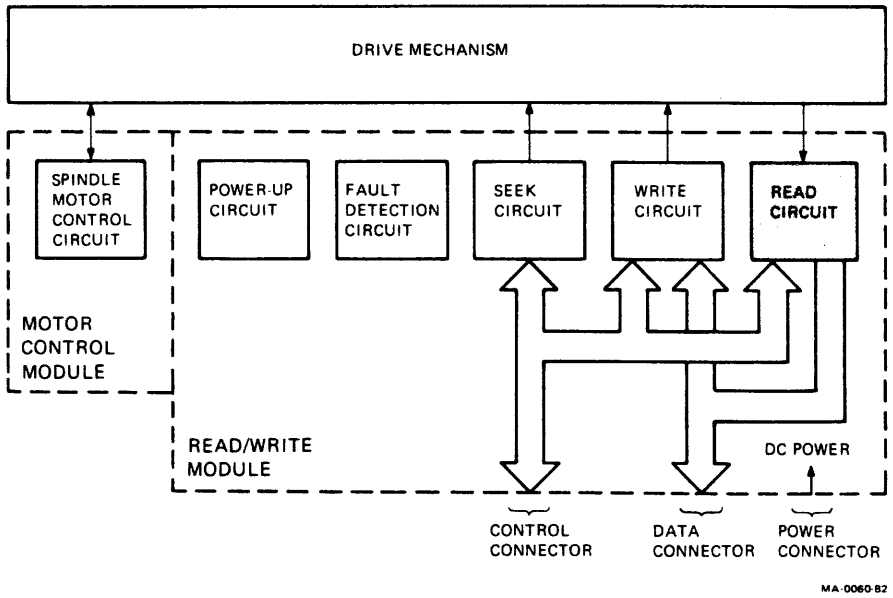


Figure 6-16 Read Circuit Detail

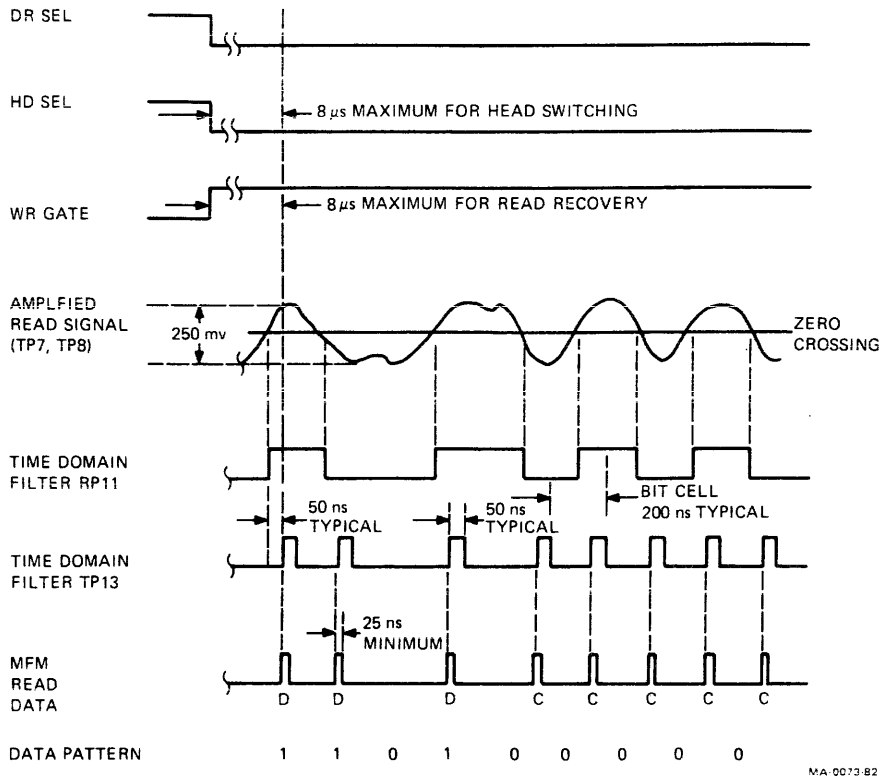


Figure 6-17 Read Data Timing

When the head is selected, the amplifier/filter receives a differential read signal from the read/write heads. The read signal is a low voltage analog signal that represents the flux reversals recorded on the media.

The signal is amplified 400 times and then passed through a 3.1 MHz low-pass filter. This signal is observable at test points TP7 and TP8 (Figure 6-17). The amplification allows the rest of the read chain to convert the analog data signal to a digital data signal.

The amplifier/filter passes the amplified read signal to a peak detector. The peak detector converts the differential read data signal to rectangular wave signals. Each transition of the signal represents the zero crossings of the analog signal. The peak detector passes this digital signal to a time domain filter.

The time domain filter stops noise mixed with the read data from passing to the pulse generator. This is done by comparing the digital signal to itself after a 50 ns delay. Both signals are observable at test points TP11 and TP13 (Figure 6-17).

The pulse generator then converts each transition of the filtered read data to a pulse, and sends the pulse to the differential driver. When the controller module enables the driver by asserting DRSEL, differential MFM READ DATA passes to the controller module.

6.4 CONNECTOR DESCRIPTIONS

Paragraph 6.4.1 through 6.4.4 define all signals that pass between the disk drive's modules. The signal definitions are grouped by common connectors.

6.4.1 Connector J1, Read/Write Module

This paragraph describes the control and status signals passed between the disk drive's read/write module and the controller module. Figure 6-18 shows the signal direction between the disk drive and the controller module. Figure 6-19 shows the location of the connector.

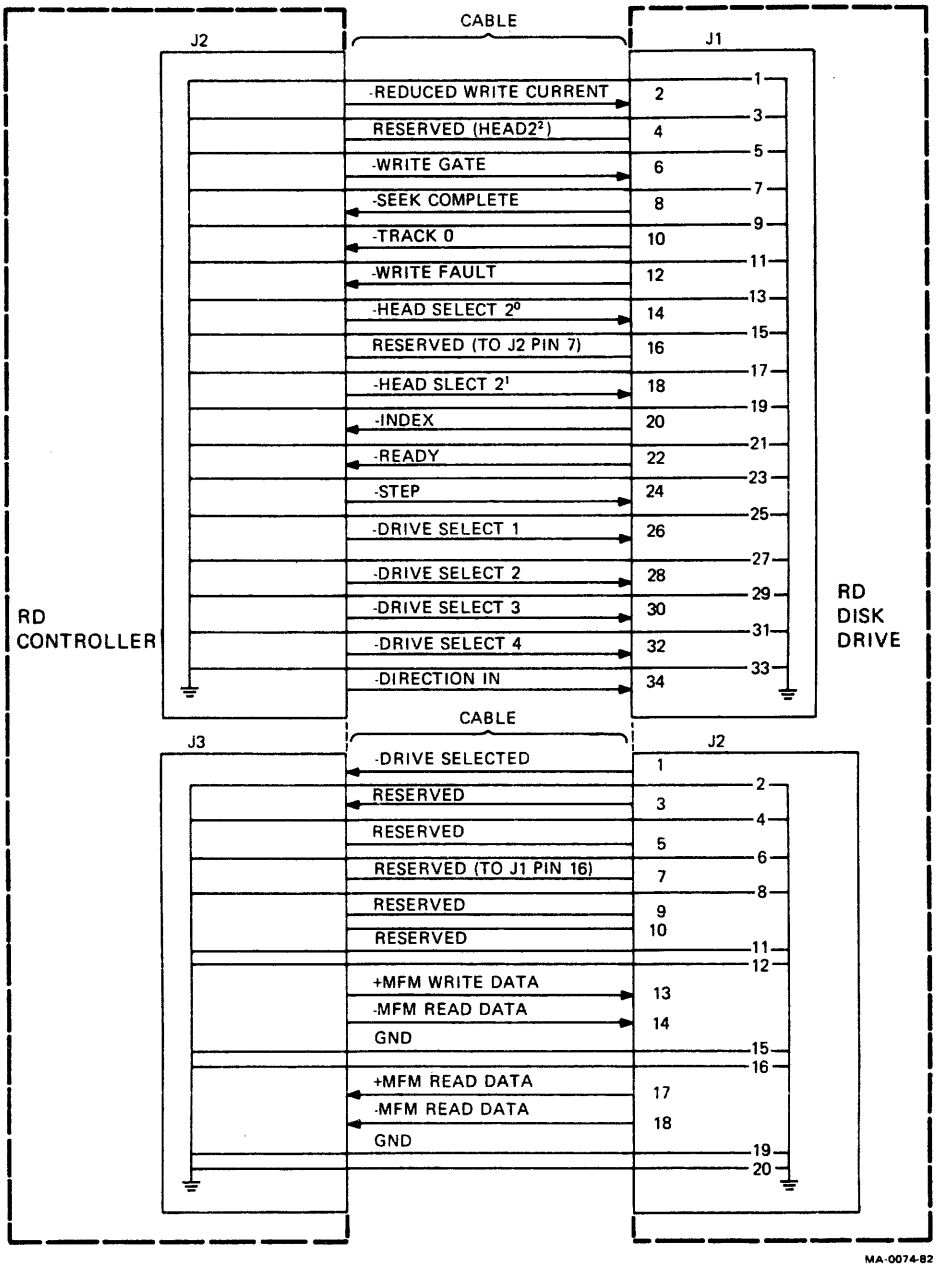


Figure 6-18 Interface Signal Connections

Table 6-1 lists the J1 connector's pin functions. The connector's odd-numbered pins are grounded and therefore are not discussed. The signal mnemonic column describes the signal's asserted state. An L after the mnemonic means an asserted low state. An H after the signal name means an asserted high state.

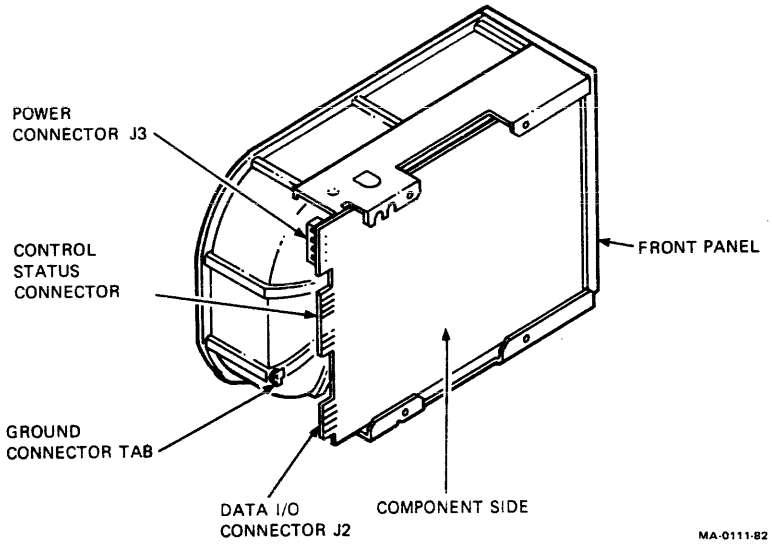


Figure 6-19 I/O Connector Locations

Table 6-1 Control/Status Connector J1

Pin	Signal Name	Signal Mnemonic
2	Reduced write current	RWC L
4	Reserved	
6	Write gate	WR GATE L
8	Seek complete	SEEK COMPLETE L
10	Track 000	TK000 L
12	Write fault	WRITE FAULT L
14	Head select 2^0	HD SEL 0 L
16	Unspecified	
18	Head select 2^1	HD SEL 1 L
20	Index	INDEX L
22	Ready	READY L
24	Step	STEP PULSE L
26	Drive select 1	DR SEL L
28	Reserved	
30	Reserved	
32	Drive capacity	5MB L
34	Direction in	DIRECTION IN L

6.4.1.1 REDUCED WRITE CURRENT (Pin 2) – The controller module asserts this signal. When this signal and WRITE GATE are asserted, the disk drive uses a lower value of write current for writing on the disk. When this signal is unasserted, the disk drive uses a higher value of write current.

The inner tracks need a lower write current than the outer tracks. Since the heads fly lower at the inner tracks, a lower write current ensures generating the proper magnetic fields. Using a high write current at inner tracks destroys data in the adjacent tracks.

6.4.1.2 WRITE GATE (Pin 6) – The controller module asserts this signal, which enables the write drivers when SEEK COMPLETE is asserted.

6.4.1.3 SEEK COMPLETE (Pin 8) – The disk drive asserts this signal to the controller module. This signal is asserted when the read/write module seek circuit does not receive a step pulse in 14 ms and the read/write heads have settled. If this signal is deasserted, writing is inhibited. SEEK COMPLETE is deasserted during any seek operation.

6.4.1.4 TRACK 000 (Pin 10) – The disk drive asserts this signal to the controller module. When the signal is asserted, the read/write heads are positioned over the outermost track (track 0).

6.4.1.5 WRITE FAULT (Pin 12) – The disk drive asserts this signal to the controller module. When the signal is asserted, one of the following conditions is detected and writing or seeking is inhibited. The signal remains asserted until the condition is corrected.

- The heads receive current when WRITE GATE is deasserted.
- DRIVE SELECT and WRITE GATE are asserted, but the read/write heads do not receive current.
- Multiple heads are selected, no head is selected, or head is incorrectly selected.
- The dc voltages are out of tolerance.

6.4.1.6 HEAD SELECT (Pin 14 and 18) – The controller module asserts the HD SEL 0 and HD SEL 1 signals. These signals are decoded to select one of four disk drive heads.

6.4.1.7 INDEX (Pin 20) – The disk drive asserts this signal to the controller module. The INDEX signal is an asserted pulse that occurs once per disks revolution. The leading edge of the pulse indicates the beginning of each track (sector 0).

6.4.1.8 READY (Pin 22) – The disk drive asserts this signal to the controller module. When this signal is asserted, the disk drive is ready to read, write, or seek. If SEEK COMPLETE and READY are asserted, the I/O signals are valid. When READY is deasserted, all writing and seeking actions are inhibited.

6.4.1.9 STEP (Pin 24) – The controller module asserts this signal to control the read/write head movement in the direction determined by the DIRECTION IN signal.

6.4.1.10 DRIVE SELECT (Pin 26) – The controller module asserts this signal, which selects the drive and the indicator on the bezel. This signal becomes deasserted if one of the following events occurs.

- The host resets the controller module.
- A power fault occurs in the host processor.

6.4.1.11 DRIVE CAPACITY (Pin 32) – The disk drive asserts this signal to the controller module. This signal is generated by the DRIVE SELECT signal on the RD50 disk drive only.

6.4.1.12 DIRECTION IN (Pin 34) – The controller module asserts this signal, which determines the direction of the read/write head movement when a step pulse is issued. The asserted state of DIRECTION IN selects head movement toward the center of the disk. A deasserted signal selects head movement toward track 0.

6.4.2 Connector J2, Read/Write Module

This paragraph describes the data signals passed between the disk drive's read/write module and the controller module. Figure 6-18 shows the signal direction between the disk drive and the controller module. Figure 6-19 shows the location of the connector.

Table 6-2 lists the J2 connector pin functions. The signal mnemonic column describes the signal's asserted state. An L after the mnemonic means an asserted low state (logic zero). An H after the signal name means an asserted high state (logic high).

6.4.2.1 DRIVE SELECTED (Pin 1) – The disk drive asserts this signal to the controller module when the disk drive is selected.

6.4.2.2 MFM WRITE DATA (Pins 13 and 14) – The controller module asserts this differential pair of signals and determines the transitions to be written on the disk surface. If WRITE GATE is asserted, the transition of the +MFM WRITE DATA line going more positive than the –MFM WRITE DATA line causes a flux reversal on the disk. While the controller module reads data from the disk drive, this signal is MFM WRITE DATA deasserted (+MFM WRITE DATA is more negative than –MFM WRITE DATA).

Table 6-2 Data I/O Connector J2

Pin	Signal Name	Signal Mnemonic
1	Drive selected	DRV SELD L
2	Ground	
3	Reserved	
4	Ground	
5	Spare	
6	Ground	
7	Reserved	
8	Ground	
9	Spare	
10	Spare	
11	Ground	
12	Ground	
13	+MFM write data	+MFM WRITE DATA H
14	–MFM write data	–MFM WRITE DATA H
15	Ground	
16	Ground	
17	+MFM read data	+MFM READ DATA H
18	–MFM read data	–MFM READ DATA H
19	Ground	
20	Ground	

6.4.2.3 MFM READ DATA (Pins 17 and 18) – The disk drive asserts this differential pair to define recovered read data from the selected head. The transition of the +MFM READ DATA line going more positive than the –MFM READ DATA line represents a flux reversal from the selected head.

6.4.3 Connector J3, Read/Write Module

Connector J3 on the read/write module receives power for the entire disk drive. Paragraph 6.6.2 lists these power requirements. Table 6-3 lists the J3 connector pin functions. Figure 6-19 shows the location of the connector.

6.4.4 Connector J4, Read/Write Module

Connector J4 on the read/write module passes power to the disk drive's motor control module. Table 6-4 describes the J4 connector pin functions. Figure 6-20 shows the location of the connector.

6.4.5 Connector J5, Read/Write Module

Connector J5 passes read, write, and head select signals between the read/write module and the HDA. Table 6-5 describes the J5 connector pin functions. Figure 6-20 shows the location of the connector.

6.4.6 Connector J6, Read/Write Module

Connector J6 passes signals between the read/write module, the index sensor and front bezel indicator. Table 6-6 describes the J6 connector pin functions. Figure 6-20 shows the location of the connector.

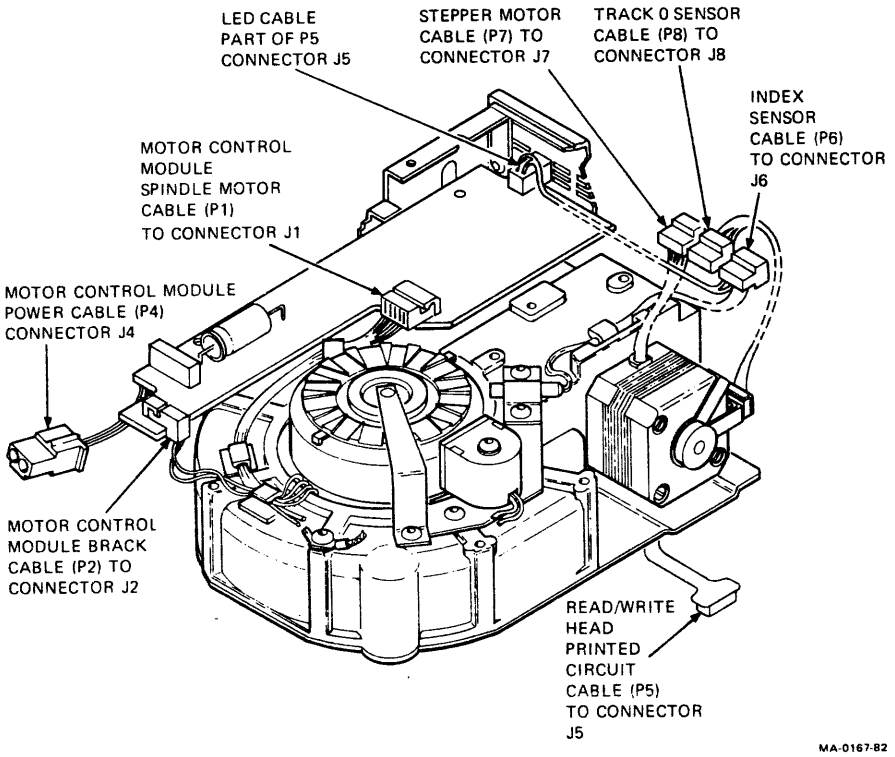


Figure 6-20 Internal Connection Locations

Table 6-3 Power Connector J3

Pin	Mnemonic	Function
1	+12 VDC	+12 Vdc
2	+12 V RETURN	Ground
3	+5 V RETURN	Ground
4	+5 VDC	+5 Vdc

Table 6-4 Motor Control Module Power Connector J4

Pin	Mnemonic	Function
1	+12 VDC	+12 Vdc
2	+12 V RETURN	Ground

Table 6-5 HDA Connector J5

Pin	Mnemonic	Function
1	+HEAD 0	+Head zero read and write data
2	HEAD SEL 0	Selects head zero
3	−HEAD 0	−Head zero read and write data
4	GND	Ground
5	+HEAD 1	+Head one read and write data
6	HEAD SEL 1	Selects head one
7	−HEAD 1	−Head one read and write data
8	GND	Ground
9	+HEAD 2	+Head two read and write data
10	HEAD SEL 2	Selects head two
11	−HEAD 2	−Head two read and write data
12	GND	Ground
13	+HEAD 3	+Head three read and write data
14	HEAD SEL 3	Selects head three
15	−HEAD 3	−Head three read and write data
16	GND	Ground

Table 6-6 Index and LED Connector J6

Pin	Mnemonic	Function
1	+ACTIVITY LED	+5 Vdc power source for indicator
2	−ACTIVITY LED	Indicator ground
3	GND	Spindle ground
4	INDEX SENSE	Index signal from sensor
5	+5 VDC	Power for index sensor

6.4.7 Connector J7, Read/Write Module

Connector J7 on the read/write module passes control signals to the stepper motor. Table 6-7 describes the J7 connector pin functions. Figure 6-20 shows the location of the connector.

6.4.8 Connector J8, Read/Write Module

Connector J8 passes signals between the read/write module and the track 0 sensor. Table 6-8 describes the J7 connector pin functions. Figure 6-20 shows the location of the connector.

6.4.9 Connector J1, Motor Control Module

Connector J1 on the motor control module passes power to the brake assembly. When power is applied to the brake assembly, the brake releases the spindle hub. Table 6-9 describes the J1 connector pin functions. Figure 6-20 shows the location of the connector.

6.4.10 Connector J2, Motor Control Module

Connector J2 on the motor control module passes controlled power signals to the spindle motor. Table 6-10 describes the J2 connector pin functions. Figure 6-20 shows the location of the connector.

Table 6-7 Stepper Motor Connector J7

Pin	Signal	Function
1	−PHASE B	Step motor control
2	+PHASE B	Step motor control
3	GND	Ground
4	−PHASE A	Step motor control
5	+PHASE A	Step motor control

Table 6-8 Track 0 Sensor Connector J8

Pin	Mnemonic	Function
1	GND	Ground
2	TRK 00 SENSE	Track 0 sensed
3	+5 VDC	Track 0 sensor power source
4	GND	Ground
5		Not used

Table 6-9 Spindle Brake Connector J1

Pin	Mnemonic	Function
1	+12 VDC	Brake release power source
2	GND	Ground

Table 6-10 Spindle Motor Connector J2

Pin	Mnemonic	Function
1	HALL IN	Sensed motor speed
2	GND	Ground
3	+6 VDC	Motor speed sensor power
4	+12 VDC	Motor power source
5	COIL A	Motor speed control
6	COIL B	Motor speed control

6.5 MAINTENANCE PROCEDURES

This paragraph describes the the field-serviceable portion of the disk drive. If field maintenance or repair is required, certain restrictions apply.

You must not open the environmentally sealed head and disk assembly (HDA). If the HDA is tampered with, the warranty for the disk drive is void. Any special tools or additional restrictions are described in the appropriate sections.

6.5.1 Preventive Maintenance

The disk drive does not require preventive maintenance.

6.5.2 Test Point Locations

Figure 6-21 shows the locations of all test points on the read/write module described in Paragraph 6.2. These test points are not accessible in the field and should not be touched by a Field Service technician.

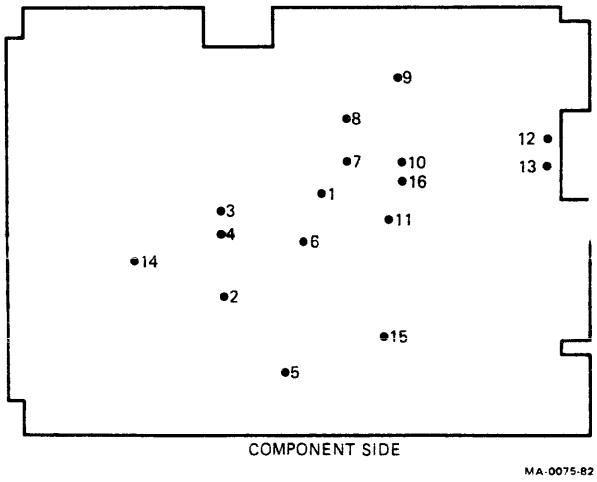


Figure 6-21 Read/Write Module Test Point Locations

6.5.3 Jumper/Dip Switch Settings

The disk drive has a set of jumper or dip switches to select the options described in Paragraph 6.3. If the disk drive contains a 14-pin chip with jumpers, all the jumpers are in place. If the disk drive contains a 14-pin dip switch, all jumpers are set to the on position. The chip is located in pins 1 through 7 and 9 through 15 of the 16-pin socket. No jumper is between pins 8 and 16 of the 16-pin socket.

These settings show that the disk drive is set to operate as follows.

- When power is first applied, the disk drive performs a recalibration to track 0.
- The seek circuit causes the stepper motor to move two steps for every step pulse received from the controller module. This occurs if the pulses are 2.8 ms or more apart.
- The controller module selects the disk drive for operation.

6.6 SPECIFICATIONS

The following paragraphs list the RD50 and RD51 disk drive specifications.

6.6.1 RD50 Disk Drive Specifications

6.6.1.1 Performance Specifications

Formatted Data Capacity	
Per drive	5.0 megabytes
Per surface	1.25 megabytes
Per track	8192 bytes
Sectors per track	16
Per sector	512 bytes
Transfer Rate	5.0 megabits/s
Access Time	
Track to track	3 ms
Average	170 ms
Maximum	500 ms
Head settling time	15 ms
Average Latency	8.33 ms

6.6.1.2 Reliability Specifications

Mean time to repair	30 minutes
Preventive maintenance	Not required
Error rates	
Soft read errors	1 per 10^{10} bits read
Hard read errors*	1 per 10^{12} bits read
Seek errors	1 per 10^{6} seeks

* Not recoverable within 8 retries

6.6.1.3 Functional Specifications

Rotating speed (r/min)	3600 ± 1%
Recording density (bits/in)	7690 maximum
Flux density (flux changes per inch)	7690 maximum
Track density (tracks/in)	255
Cylinders	153
Tracks	612
Read/write heads	4
Disks	2

6.6.1.4 Electrical Specifications

Power	Minimum	Middle	Maximum
+5 V	+4.75 V	+5.0 V	+5.25 V
Ripple	-	-	50 mV
Current	-	0.7 A	1.0 A
+12 V power	+11.4 V	+12.0 V	+12.6 V
Ripple	—	—	75 mV
Current	—	1.8 A	4.5 A*

6.6.1.5 Environmental Specifications

Ambient Temperature	
Operating	10° to 50°C (50° to 122°F)
Nonoperating	−40° to 66°C (−40° to 151°F)
Temperature Gradient	
Operating	11°C (20°F) per hour
Nonoperating	20°C (36°F) per hour
Maximum elevation	
Operating	2.4 km (8000 ft)
Nonoperating	9.1 km (30,000 ft)
Heat Dissipation	
Typical	25 W (85 Btu/hr)
Maximum	29 W (99 Btu/hr)
Relative Humidity	
Operating	20 to 80%
Nonoperating	10 to 95%

* Current draw for 20 seconds at power on.

Operating Shock

Half sine shock pulse of 10 G peak of 10 plus 3 ms duration applied perpendicular to each side.

Dimensions		
Height	82.55 mm	(3.25 in)
Width	146.05 mm	(5.75 in)
Depth	204.47 mm	(8.05 in)
Weight	2.27 kg	(5 lb)

6.6.2 RD51 Disk Drive Specifications

6.6.2.1 Performance Specifications

Formatted Data Capacity	
Per drive	10.0 megabytes
Per surface	2.5 megabytes
Per track	8,192 bytes
Sectors per track	16
Per sector	512 bytes
Transfer Rate	5.0 megabits/s
Access Time	
Track to track	3 ms
Average	85 ms
Head settling time	15 ms
Average latency	8.33 ms

6.6.2.2 Reliability Specifications

Mean time to repair	30 minutes
Error Rates	
Soft error rate	1 per 1010 bits read
Hard error rate	1 per 1012 bits read
Seek error rate	1 per 106 seeks

6.6.2.3 Functional Specifications

Rotating speed (r/min)	3600 ± 18
Recording density (bits/in)	9074
Track density (trades/in)	345
Cylinders	306
Tracks	1224
Read/write heads	4
Disks	2

6.6.2.4 Electrical Specifications

Power	Minimum	Middle	Maximum
+5 V	+4.75 V	+5.0 V	+5.25 V
Ripple	–	–	50 mV
Current	–	0.7 A	1.0 A
+12 V	+11.4 V	+12.0 V	+12.6 V
Ripple	–	–	75 mV
Current	–	1.8 A	4.5 A

6.6.2.5 Environmental Specifications

Ambient Temperature	
Operating	10° to 5°C (50° to 122°F)
Nonoperating	–40° to 66°C (–40° to 151°F)
Temperature Gradient	
Operating	11°C (20°F) per hour
Nonoperating	20°C (36°F) per hour
Maximum Elevation	
Operating	2.4 km (8000 ft)
Nonoperating	9.1 km (30,000 ft)
Heat Dissipation	
Typical	25 W (85 Btu/hr)
Maximum	29 W (99 Btu/hr)
Relative Humidity	
Operating	20 to 80%
Nonoperating	10 to 95%

Operating Shock
Half sine shock pulse of 10 G peak of 10 plus 3 ms duration applied perpendicular to each side.

Dimensions	
Height	82.55 mm (3.25 in)
Width	146.05 mm (5.75 in)
Depth	204.47 mm (8.05 in)
Weight	2.27 kg (5 lb)

CHAPTER 7
RX50 CONTROLLER MODULE

7.1 GENERAL INFORMATION

The RX50 controller module connects an RX50 dual diskette drive to the host processor. Figure 7-1 shows the controller module in relation to the other Professional 300 Series computer system components.

7.1.1 Related Documentation

The Professional 350 Field Maintenance Print Set (MP-01394-00) provides more information about the RX50 controller module.

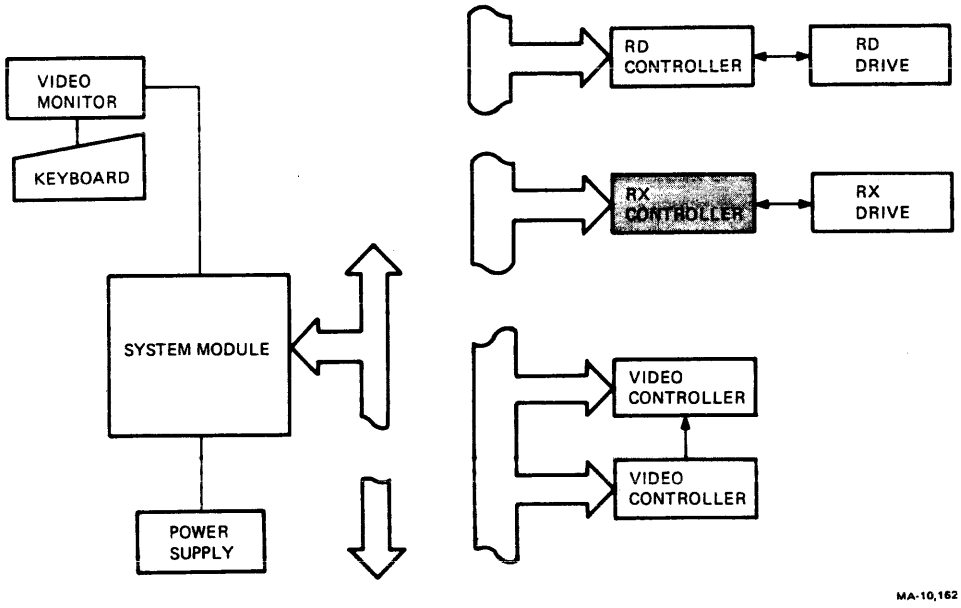


Figure 7-1 RX50 Controller Module System Relation

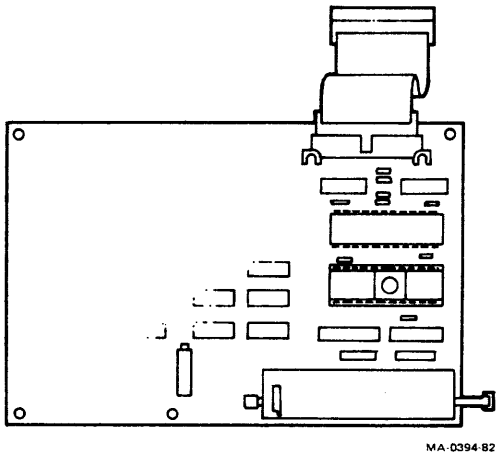


Figure 7-2 RX50 Controller Module

7.1.2 Controller Module

The RX50 controller module controls data transfers between the host processor and the RX50 dual diskette drive. This controller module is a field replaceable unit (PN 54-15058) that usually mounts in slot 2 of the CTI Bus option space. A single cable (PN 17-00285) connects the controller module to the diskette drive. Figure 7-2 shows the RX50 controller module and the diskette drive cable.

The controller module connects one RX50 dual diskette drive to the host processor which provides 819,200 bytes of storage. Commands, status, and data are transferred between the controller module and host processor by register-to-register accesses by the host processor. The controller module contains an auto-incrementing 512 8-bit byte sector buffer. This buffer holds the data transferred between the host processor and the diskette drive. Accesses to this buffer can be started or stopped without losing the sequential addressing.

The controller module performs implied seeks when performing a read or write operation with the sector and track specified in the command registers. All data is stored on the diskettes by using modified frequency modulated (MFM) data encoding.

7.2 FUNCTIONAL COMPONENTS

Paragraphs 7.2.1 through 7.2.6 describe the components of the RX50 controller module.

7.2.1 Overview

The controller module is a single 5.2 × 8 inch module compatible with the CTI backplane. A connector on the bottom of the controller module (J1) provides a connection path to the CTI Bus. A connector at the top of the controller module (J2) provides a connection path to the diskette drive.

The following steps describe how the controller module performs data transfers from main memory to the disk surface.

1. The host processor controls the data transfer between main memory and the sector data buffer in the controller module.

2. A microprocessor in the controller module then controls the data transfer between the sector data buffer and the diskette surface.

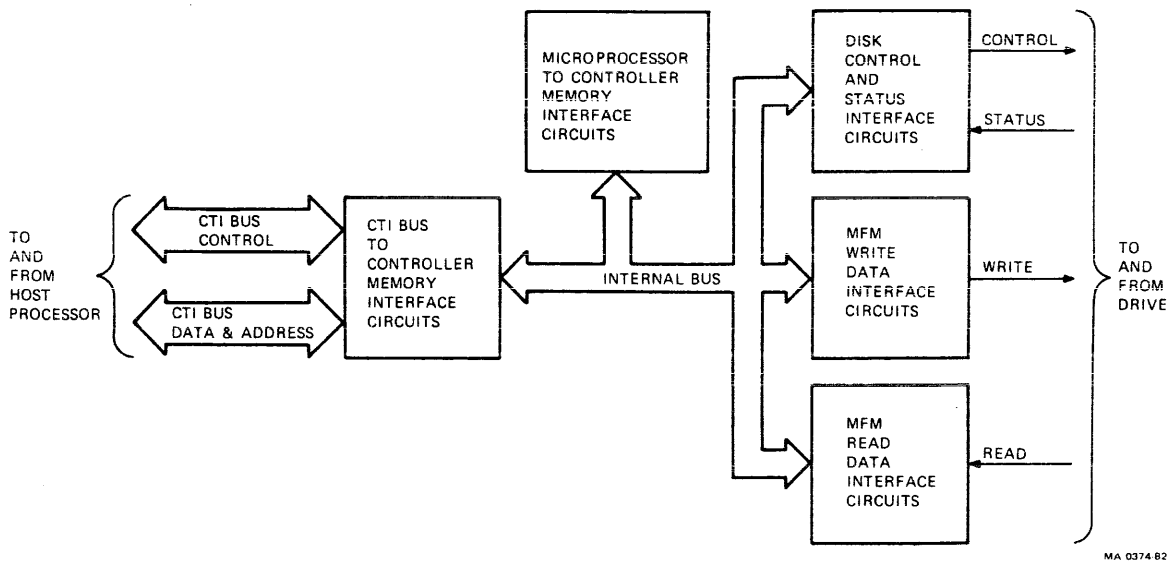


Figure 7-3 RX50 Controller Module Block Diagram

If the host processor requests data from the diskette drive, these steps are reversed.

The controller module performs the encoding, decoding, and data error detection for all transfers between the diskette surface and the sector buffer.

The following major circuits make up the RX50 controller module (Figure 7-3).

CTI Bus to controller memory interface
Microprocessor to controller memory interface
Diskette control and status interface
MFM write data interface
MFM read data interface

7.2.2 CTI Bus to Controller Memory Interface

The host processor accesses the controller module by reading and writing the controller memory. All accesses to the RX50 identification register and the RX50 control and status registers are relocated to byte locations in the lower half of the 1K controller memory. Table 7-1 describes this controller memory organization. The remaining 488 byte locations in the lower half of memory are reserved for future applications. All accesses to the RX50 data buffer registers are relocated to the upper half of the 1K controller memory. The 512 byte locations are used as the sector data buffer.

When the host processor accesses the controller memory, the CTI Bus to controller memory interface circuits perform the following operations.

- Acknowledge accesses to its registers (memory) by the host processor
- Decode CTI Bus control signals from the host processor
- Pass data between the host processor and the controller registers (memory)
- Generate interrupts for the host processor when the controller module completes a command

Table 7-1 RX50 Controller Memory Organization

Memory Address (Octal)	Byte Number	Function
1777 to 1000	1023 to 0512	Sector buffer sequential accesses to memory location 20 or 26
0777 to 0030	0511 to 0024	Reserved
0027 to 0020	0023 to 0016	Sector buffer relocation addresses and command addresses
0017 to 0010	0015 to 0008	Status registers
0007 to 0000	0007 to 0000	Command registers

7.2.3 Microprocessor to Controller Memory Interface

The microprocessor accesses the controller memory to retrieve commands and store status data. It then executes the commands and controls the internal data flow of the RX50 controller module.

The microprocessor arbitrates the use of the internal I/O bus for the disk control and status interface, MFM write data interface, and MFM read data interface circuits.

7.2.4 Disk Control and Status Interface

The disk control and status interface passes control and status information between the controller module and the RX50 diskette drive. The microprocessor I/O ports receive the drive status information from the diskette drive, and pass drive control information to the diskette drive.

7.2.5 MFM Write Data Interface

The MFM write data interface converts data in the sector buffer to MFM data for the diskette drive. These circuits perform the following operations.

- Convert the sector buffer contents to serial MFM encoded data
- Precompensate the MFM encoded data for varying bit densities on the diskettes
- Accumulate then add two CRC bytes to the end of the serial data
- Synchronize the MFM encoded data to a reference clock cycle
- Pass the MFM write data to the RX50 diskette drive

7.2.6 MFM Read Data Interface

The MFM read data interface converts MFM data read from the diskette drive into 8-bit bytes, and places them in the sector buffer. These circuits perform the following operations.

- Recover the MFM encoded data received from the diskette drive
- Convert the MFM encoded data to 8-bit bytes for the sector buffer
- Calculate two CRC bytes and compare them to the values stored with the received data

7.3 THEORY OF OPERATION

The RX50 controller module has five functions for storing and retrieving data on the RX50 diskette drive by the host processor. Paragraph 7.3.7 through 7.3.5 describe each of the following functions at a block diagram level.

CTI Bus to controller memory interface
Microprocessor to controller memory interface
Disk control and status interface
MFM write data interface
MFM read data interface

7.3.1 CTI Bus to Controller Memory Interface Detail

The host processor accesses the controller memory through the following circuits when the microprocessor is not executing a command. The host processor can write to the command registers, read the status registers, and read or write to the sector buffer. The CTI Bus to controller memory interface uses the following circuits (Figure 7-4).

CTI Bus control signal I/O buffer
CTI Bus data/address I/O buffer
Microprocessor
Read/write signal multiplexer
Address latch
Address decoder
Sector buffer address counter
Address multiplexer
Sector buffer/command and status registers (memory)

These circuits perform the following functions.

- Pass power okay signals (POK) and initialization signals (INIT) from the CTI Bus to the controller module
- Pass interrupt signals (IRQA and IRQB) from the controller module to the CTI Bus
- Acknowledge accesses to the controller address range with a reply signal (RPLY)
- Control data transfers between the controller memory and the CTI Bus

7.3.1.1 RX50 Module Initialization – The CTI Bus control signal I/O buffer receives a B POK H and a B INIT L signal from the host processor. These signals reset or initialize circuits in the controller module.

The B INIT L signal initializes the address latch, address decoder, sector buffer address counter, and the microprocessor. The B POK H signal initializes the address latch, address decoder, sector buffer address counter, microprocessor, and the controller module.

When the B INIT L signal is asserted on the CTI Bus, the INIT signal internal to the module is asserted. When the B POK H signal on the CTI Bus is deasserted, the POK signal internal to the module is deasserted and the INIT signal is asserted. The internal initialization signal generation does not depend on which function controls the internal bus.

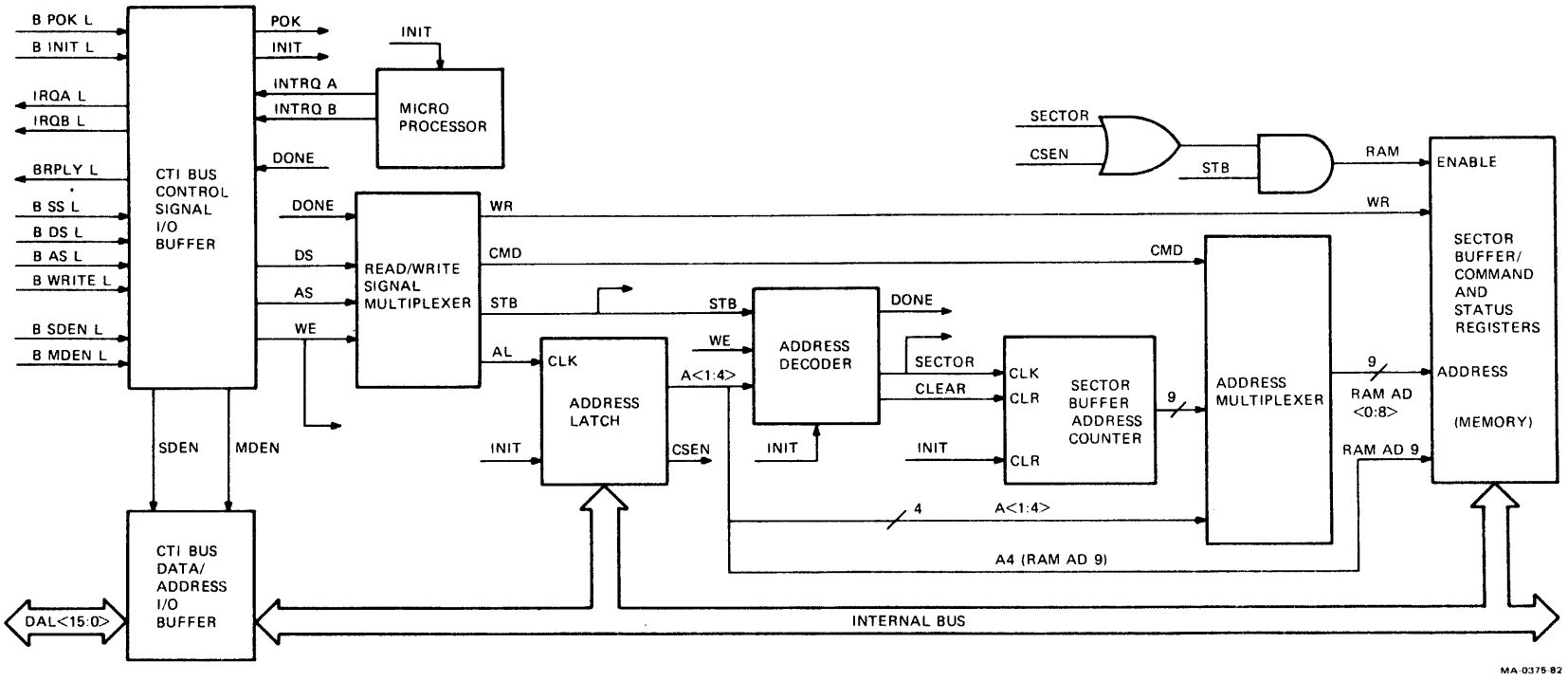


Figure 7-4 CTI Bus to Controller Memory Interface Circuits (Sheet 1 of 2)

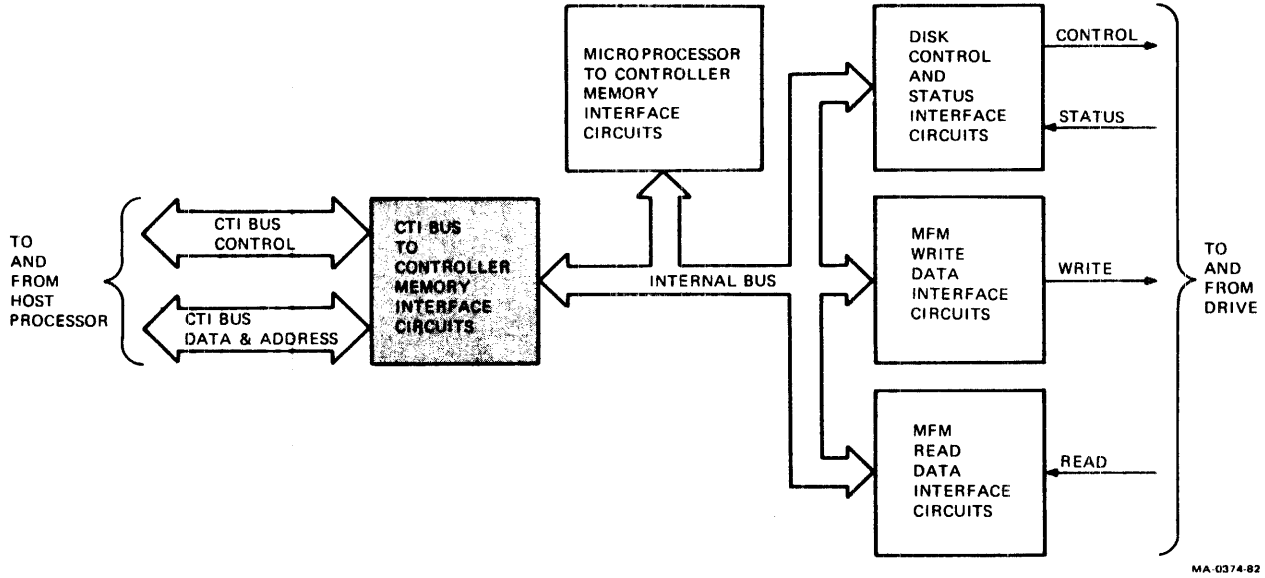


Figure 7-4 CTI Bus to Controller Memory Interface Circuits (Sheet 2 of 2)

7.3.1.2 Interrupt Signal Generation – The CTI Bus control signal I/O buffer passes two interrupt signals (INRQ A and INRQ B) from the microprocessor on the controller module to the CTI Bus (IRQA L and IRQB L). The IRQA interrupt signal indicates a command completed execution. The IRQB L interrupt signal indicates a volume change (the drive door was opened and closed).

Only the first volume change between read status commands generates the interrupt. Volume changes received from the diskette drive before the controller module receives a read status command do not generate interrupts.

7.3.1.3 RX50 Module Acknowledgment – The controller module responds to the CTI Bus by asserting the B RPLY L signal. This signal is generated by the module when the CTI Bus slot select signal (B SS L) and data strobe signal (B DS L) are asserted.

7.3.1.4 Host Processor to Controller Memory Accessing – If the microprocessor on the controller module is not executing any commands, the RX50 module memory can be addressed from the CTI Bus. The address decoder generates a deasserted DONE signal to indicate CTI Bus to controller module accessing.

The address decoder is shared by both the host processor and the microprocessor to access the memory. The read/write signal multiplexer, address latch, sector buffer address counter, and address multiplexer are also shared.

The memory on the controller module is addressed in two modes: command and status register memory addressing or sector buffer memory addressing. The command and status register mode allows random writing to the command registers and random reading of the status registers. The sector buffer mode allows sequential access to the 512 8-bit bytes. All memory locations are partially decoded and mapped into a 1K by 8-bit memory array. The module performs all memory address relocation operations for both modes. Memory accessing from the CTI Bus is done through the addresses listed in the programming section.

All accesses to the controller module from the host processor are addressed on word boundaries. When the host processor accesses the memory in the command and status memory range, the CTI Bus write signal is used as an address bit for memory. The controller module translates word accesses to byte accesses by shifting the address. It does not use the zero bit of the CTI Bus address. The address shift causes CTI Bus address bit 1 to become controller memory address bit 0, CTI Bus address bit 2 to become controller memory address bit 1, and so on. This change allows eight CTI Bus word address locations to be mapped into 16 controller memory address locations.

Command and Status Register Accessing

When the DONE signal is deasserted, the master device enable (B MDEN L) signal from the CTI Bus can enable the CTI Bus data/address I/O buffer to pass data and address on the CTI data/address lines to the internal bus. CTI Bus addresses in the 00 to 16 range access the command and status registers.

Once the address is on the internal bus, the CTI Bus address strobe (B AS L) passes to the read/write signal multiplexer and generates an address latch clock signal (AL). The AL signal clocks the address latch to accept four address bits (DAL 1, DAL 2, DAL 3, and DAL 4). This address goes to the address decoder and address multiplexer. Addresses in the 00 to 16 range disable the address decoder and the sector buffer address counter. This asserts the command and status enable signal (CSEN) to set up memory for a data transfer.

Once the data is present on the internal bus, the data strobe (B DS L) from the CTI Bus generates a data strobe (DS) from the CTI control signal I/O buffer to the read/write signal multiplexer. The multiplexer then generates a strobe (STB) for the memory. After the CSEN and STB signals are asserted, the memory is enabled for the data transfer.

Along with the data strobe, the read/write select (B WRITE L) signal on the CTI Bus passes to the read/write signal multiplexer as WE. An asserted WE signal asserts a write signal (WR) for the memory and asserts a command select signal (CMD) for the address multiplexer. This sequence selects a write operation to the command address range in the controller memory (addresses 00 to 07). When the WE signal is deasserted, both WR and CMD are deasserted. This selects a read operation to the status address range of the controller memory (addresses 10 to 17).

The address multiplexer uses the CMD signal and the four address bits from the address latch to generate an address for the memory. Since the memory is enabled when CSEN and STB signals are asserted, the address from the address multiplexer selects the desired location. WR specifies a write operation (internal bus to memory) or a read operation (memory to internal bus).

Sector Buffer Memory Accessing

Some of the same operations occur during a sector buffer memory access that occur during a command and status register access. The difference is that the address decoder and sector buffer address counter provide the address to the address multiplexer for the memory.

When the DONE signal is not asserted, the master device enable signal (B MDEN L) from the CTI Bus can enable the CTI Bus data/address I/O buffer to pass an address on the CTI data/address lines to the internal bus. CTI Bus addresses in the 20 to 26 range access the sector buffer registers.

Once the address is on the internal bus, the CTI Bus address strobe (B AS L) passes to the read/write signal multiplexer and generates an address latch clock signal (AL). The address latch accepts only four address bits (DAL 1, DAL 2, DAL 3, and DAL 4), then provides them to the address decoder and address multiplexer. Addresses in the 20 to 26 range enable the address decoder and the sector buffer address counter and deasserts the CSEN signal. Table 7-2 defines these addresses and their functions.

Table 7-2 Controller Module Responses to CTI Bus Addresses 20 through 26

Address	Operations Performed
20	A read operation generates a SECTOR signal. This increments the sector buffer address counter at the end of a memory access cycle. When STB is asserted, memory is enabled.
22	Accessing this address generates a CLEAR signal. This resets the sector buffer address counter.
24	Accessing this address asserts the DONE signal. This notifies the microprocessor that new commands were loaded into the memory. The host processor can now give control of the module to the microprocessor.
26	A write operation allows the decoder to synchronize the generation of a SECTOR signal with an asserted WE (Paragraph 7.5).

The sector buffer address counter provides a 9-bit address to the address multiplexer. The 10th address bit comes from the address latch (A4). This bit enables the address multiplexer to pass the sector buffer address counter output to the memory as well as select the high bank of memory locations directly (RAM 9).

The data strobe (B DS L) from the CTI Bus generates a data strobe (DS) from the CTI control signal I/O buffer to the read/write signal multiplexer. The multiplexer then generates a strobe (STB) for the memory. When the SECTOR and STB signals are asserted, the memory is enabled.

Along with the data strobe, the read/write select signal (B WRITE L) on the CTI Bus passes to the read/write signal multiplexer as WE. An asserted WE asserts a write signal (WR) for the memory. When the WE signal is deasserted, the WR signal is deasserted.

When address 26 is used for write operations (WR asserted), the sector buffer may be accessed to accept data from the internal bus. When address 20 is used for read operations (WR deasserted) the sector buffer places data on the internal bus.

7.3.2 Microprocessor to Controller Memory Accessing

The microprocessor can access the memory in the RX50 controller module after the host processor releases control of the module to the microprocessor (Figure 7-5). This is accomplished when the host processor accesses register 24. The address decoder asserts a DONE signal. This indicates microprocessor to controller memory accessing. The decoder is also used by the CTI Bus to memory interface function. Other items used by the CTI Bus for memory interface include the read/write signal buffer, address latch, sector buffer address counter, and address multiplexer.

As in the CTI Bus to memory interface function, the memory on the RX50 controller module is addressed in two modes, command and status register memory addressing and sector buffer memory addressing. The command and status register mode accesses addresses 0 through 16 of the memory. The sector buffer mode accesses addresses 512 through 1023 of the memory (upper 512 8-bit words). The controller module performs all the memory address relocation operations for both modes.

The microprocessor performs both read and write operations to the command and status registers. The microprocessor can clear any command register after that register has been read. This protects recorded data in case of circuit failures.

7.3.2.1 Command and Status Register Accessing – When the DONE signal is asserted, the microprocessor controls the output of the read/write signal multiplexer. The microprocessor can place addresses on the internal bus and assert the address latch enable signal (ALE). This causes the AL signal to load the address into the address latch. Addresses in the 00 to 16 range access the command and status registers.

The address latch accepts only four address bits (DAL 1, DAL 2, DAL 3, and DAL 4) for the address decoder and address multiplexer. Addresses in the 00 to 16 range disable the address decoder and the sector buffer address counter, and assert the command and status enable signal CSEN.

A microprocessor read or write signal (μPRD or μPWR) generates a strobe (STB) for the memory from the read/write signal multiplexer. When the CSEN and STB signals are asserted, the memory is enabled for read or write operations.

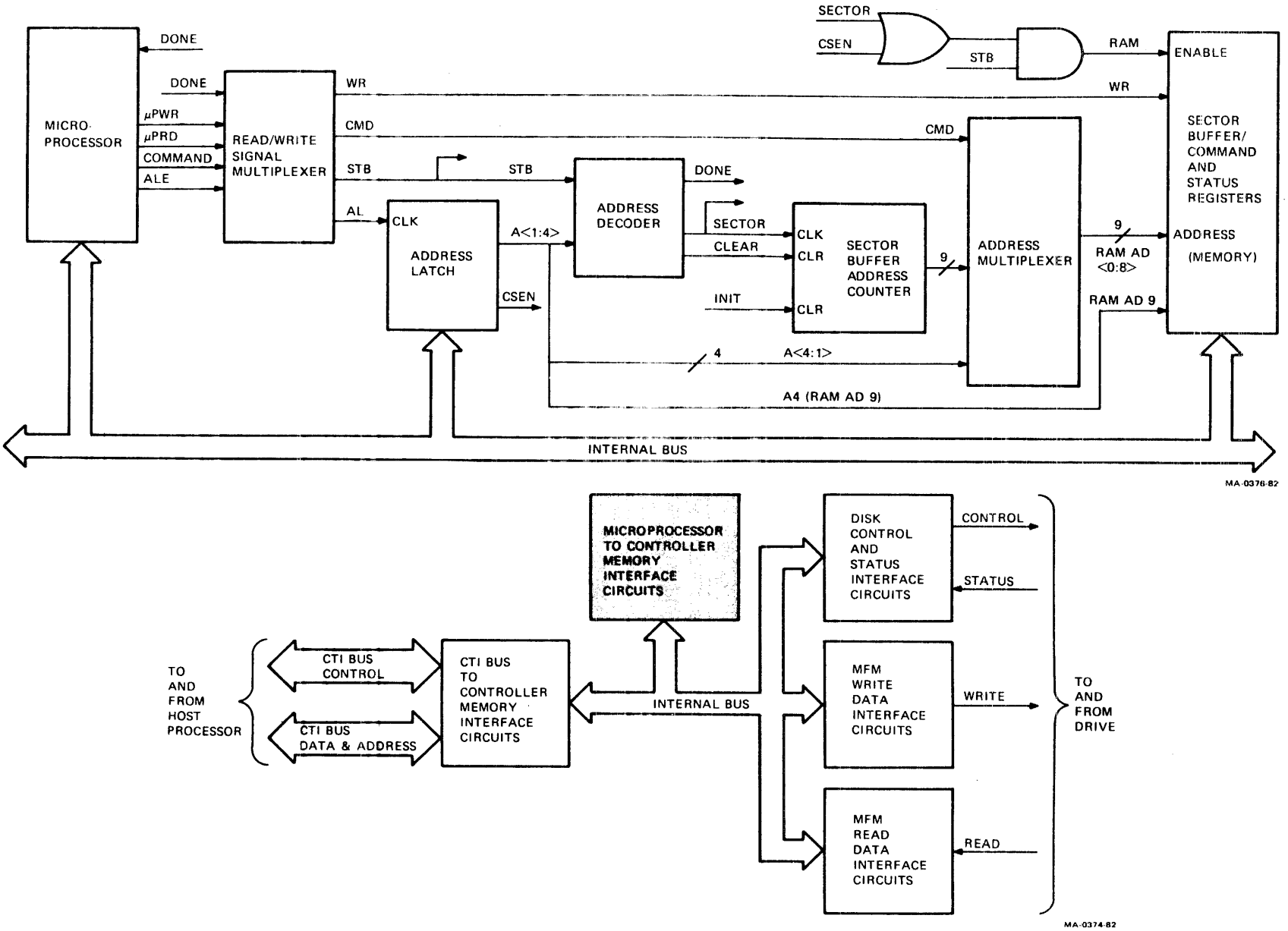


Figure 7-5 Microprocessor to Controller Memory Interface Circuits

The microprocessor specifies a command register access or a status register access with a COMMAND signal. An asserted COMMAND signal asserts CMD for the address multiplexer selecting command registers. A deasserted COMMAND signal deasserts CMD for the address multiplexer selecting status registers.

The address multiplexer uses the CMD signal and the four address bits from the address latch to generate an address for the memory. Since the memory is enabled by asserted CSEN and STB signals, the address from the address multiplexer selects the desired location. The μPWR asserts WR to specify a write operation (internal bus to memory), or deasserts WR to specify a read operation (memory to internal bus).

7.3.2.2 Sector Buffer Memory Accessing – Some of the same operations occur during a sector buffer memory access and a command and status register access. The difference is that the address decoder and sector buffer address counter provide the address to the address multiplexer for the memory.

When the DONE signal is asserted, the microprocessor controls the output of the read/write signal multiplexer. The microprocessor places addresses on the internal bus and asserts the address latch enable signal (ALE). This asserts the AL signal and loads the address into the address latch. Addresses in the 20 to 24 range access the sector buffer registers.

The address latch accepts only four address bits (DAL 1, DAL 2, DAL 3, and DAL 4), then provides them to the address decoder and address multiplexer. Addresses in the 20 to 24 range enable the address decoder and the sector buffer address counter, and deasserts the CSEN signal. Table 7-3 describes the operations that these addresses access for the microprocessor.

The sector buffer address counter provides a 9-bit address to the address multiplexer. The 10th address bit (RAM9 which is A4) comes from the address latch. This bit also enables the address multiplexer to pass the sector buffer address counter output to the memory, and selects the high bank of memory locations.

A microprocessor read or write signal (μPRD or μPWR) generates a strobe (STB) for the memory from the read/write signal multiplexer. When the SECTOR and STB signals are asserted, the memory is enabled for read or write operations.

The address multiplexer uses address latch bit A4 to select the sector buffer address counter output as the 9-bit address for the memory. Since the memory is enabled by asserted SECTOR and STB signals, the address from the address multiplexer and A4 (RAM A9) from the address latch select the desired location. The μPWR signal asserts WR to specify a write operation (internal bus to memory), or deasserts WR to specify a read operation (memory to internal bus).

Table 7-3 Microprocessor Accesses to Addresses 20 through 26

Address	Operations Performed
20	Read and write operations generate a SECTOR signal. This increments the sector buffer address counter at the end of a memory access cycle. When STB is asserted, memory is enabled.
22	Accessing this address generates a CLEAR signal. This resets the sector buffer address counter.
24	Accessing this address deasserts the DONE signal. This gives control of the module to the microprocessor.
26	This address is not used by the microprocessor to access the sector buffer.

7.3.3 Disk Control and Status Interface

The disk control and status interface passes disk control and status signals between the RX50 diskette drive and the RX50 controller module (Figure 7-6). The control signals for the diskette drive are generated after the command registers are loaded with commands by the host processor (Paragraph 7.3.1). The controller module receives the status signals from the diskette drive. These signals are used for timing during command execution.

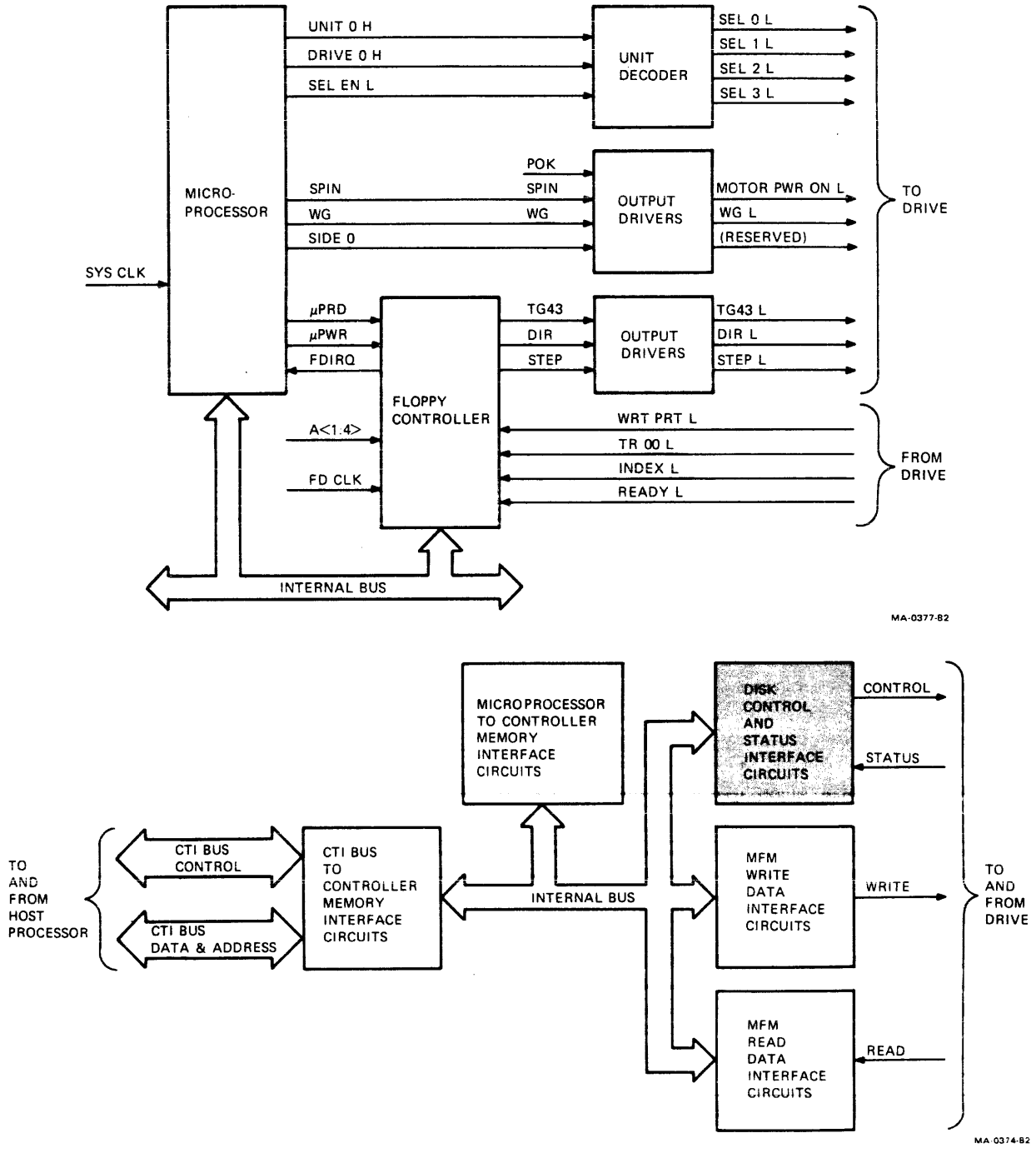


Figure 7-6 Disk Control and Status Interface Circuits

The following circuits allow the controller module to accept or generate the following signals.

Microprocessor
Controller module
Unit selection decoder
Output drivers

Commands loaded into the controller module registers generate the following control signals.

Drive select signals (SEL0 L, SEL1 L, SEL2 L, and SEL3 L)
Write enable signal (WG L)
RX50 drive spindle motor control signal (MOTOR PWR ON L)
Write current selection signal (TG43 L)
Track positioning signals (DIR L and STEP L)

The controller module accepts the following status signals from the diskette drive.

Selected diskette write protected (WRT PRT L)
Heads over track 0 (TK 00 L)
Beginning of track (INDEX L)
Drive ready for operation (READY L)

7.3.3.1 Control and Status Signal Processing – After the host processor loads the command registers and accesses the start command register (register address 24), the microprocessor directly accesses the registers (Paragraph 7.3.2). The microprocessor read and write signals (μPRD and μPWR) used during a microprocessor to memory interface function also control the access to the controller module through the internal bus. This allows the microprocessor to control the controller module operations and access the controller module registers when executing commands.

After the controller module executes a command, it generates an interrupt (FDIRQ) for the microprocessor. This signal indicates that the microprocessor can send another command to the controller module, or the microprocessor can read the controller module status registers.

None of the controller module status or command registers are directly accessible by the host processor. The microprocessor reads the controller module registers and transfers data over the internal bus to or from the memory for access by the host processor.

7.3.3.2 Drive Select Signal Conversion – The microprocessor generates four signals for selecting a diskette drive: UNIT 0, DRIVE 0, SEL EN, and SIDE. The SIDE signal is reserved for future use. A unit selection decoder decodes the remaining signals and generates the drive select signals, SEL0 L, SEL1 L, SEL2 L, or SEL3 L. Table 7-4 shows this conversion.

7.3.3.3 Drive Control Signal Gating – The microprocessor generates a write enable signal (WG) and a spindle motor control signal (SPIN) for the diskette drive. These signals are sent to the drive only when the power levels for the system are within tolerance. This protects data on the drive when power is first applied to the system, or during power loss situations.

Table 7-4 Diskette Drive Select Signal Conversion

Asserted Control Signals			Asserted Selects			
UNIT0 H	DRIVE0 H	SEL EN L	0	1	2	3
X	X	No	No	No	No	No
No	No	Yes	No	No	No	Yes
Yes	No	Yes	No	No	Yes	No
No	Yes	Yes	No	Yes	No	No
Yes	Yes	Yes	Yes	No	No	No

The WG and SPIN signals go to an output driver. The driver passes them to the diskette drive as WG L and MOTOR PWR ON L, respectively. When the power is in tolerance, a power okay signal (POK) from the CTI Bus (Paragraph 7.3.1) enables the microprocessor output to the diskette drive.

7.3.4 Write Data Interface Function

A write data interface function converts the sector buffer contents to precompensated MFM write data for the diskette drive (Figure 7-7). The following circuits also share this function.

Microprocessor
Controller module
Input write data sync
Precompensation ROM
Output write data sync
Clock generator

7.3.4.1 Write Data Bytes to Floppy Controller Transfers – After the controller module receives a write command from the host processor, a write data function is performed. The host processor loads the sector buffer with the data to be written to the diskette drive and accesses the start command register. The microprocessor then accesses the sector buffer.

The microprocessor read and write signals (μPRD and μPWR), used during a microprocessor to controller memory interface function, also control access to the controller module over the internal bus. The microprocessor can then control the controller module operations and access the floppy controller registers when executing commands.

After the controller module executes a command, it generates an interrupt (FDIRQ) for the microprocessor. This signal indicates that the microprocessor can send another command to the controller module, or the microprocessor can read the controller module status registers. When the controller module requires a data byte for conversion to MFM data, it generates a data request signal (DRQ) for the microprocessor.

The host processor cannot directly access the controller module data, status, or command registers. The microprocessor reads and writes commands and data to the floppy controller registers over the internal bus to or from the controller module memory.

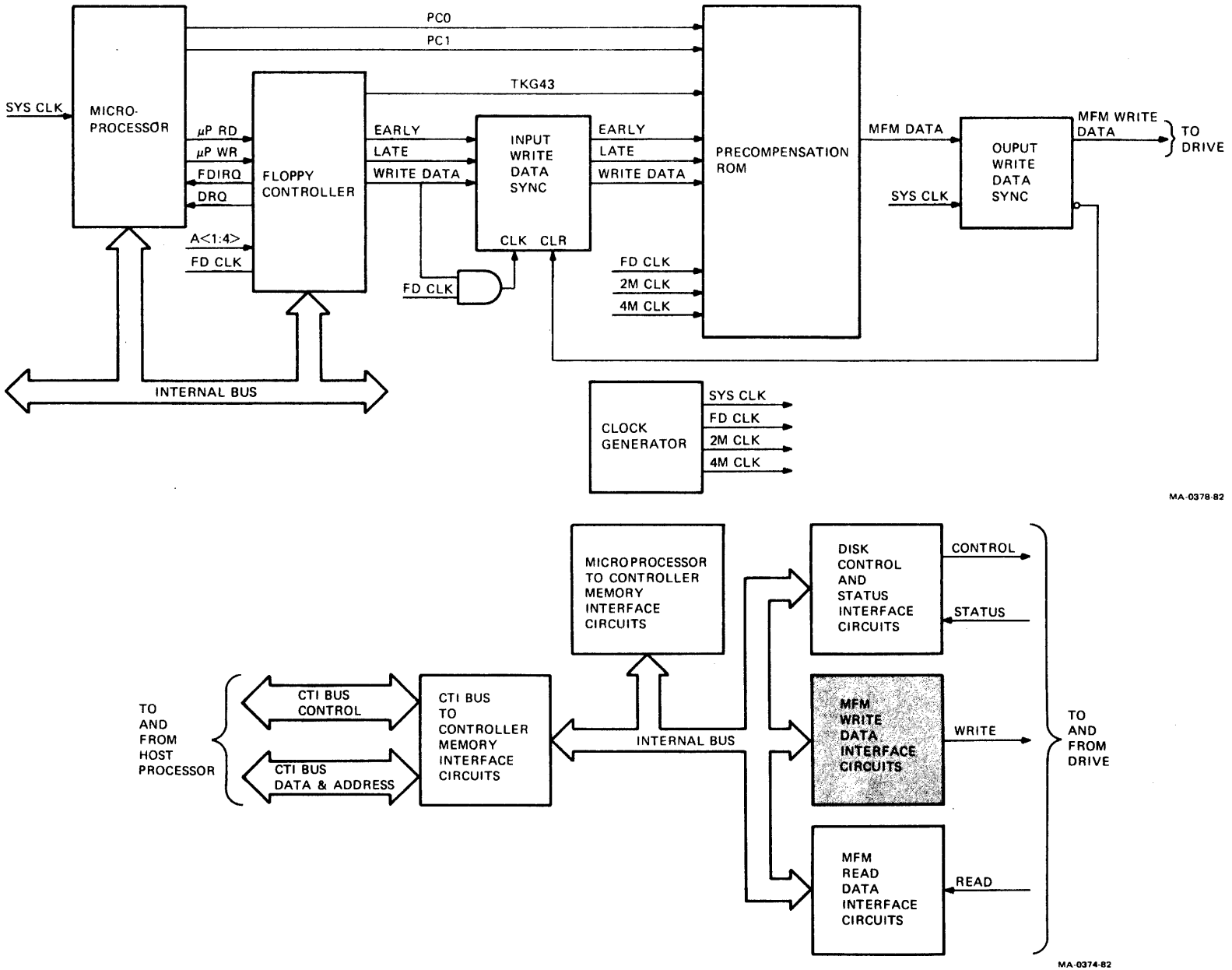


Figure 7-7 MFM Write Data Interface Circuits

7.3.4.2 MFM Encoding – The controller module converts the 8-bit data bytes to serial MFM data patterns (WRITE DATA) and generates select signals (EARLY and LATE). The select signals indicate when a pulse should be generated within a 4 μs bit frame. Table 7-5 shows how the controller module encodes MFM data.

As these signals are generated they pass to the input write data sync circuit. A 1 MHz clock (FDCLK) synchronizes the transfer of the EARLY, LATE, and WRITE DATA signals to the precompensation ROM.

7.3.4.3 Write Data Precompensation – After the controller module generates the encoding signals for MFM data recording, precompensation is performed. Precompensation is a technique used in high density recording. It shifts each MFM data pulse earlier or later than normal MFM data pulses. This compensates for the drifting of magnetic domains on the media. Drifting results from the repulsion of the magnetic domains at high densities.

The microprocessor sends two precompensation designation signals (PC0 and PC1) to the precompensation ROM. The controller module sends the TK43 signal, which designates write operations to the outer tracks (0–43) or inner tracks (44–79). Three clock signals (FDCLK, 2MCLK, and 4MCLK) shift the MFM data pulse, depending on which track the data is to be written.

Table 7-6 shows the bit shift characteristics for each group of tracks on the media.

7.3.4.4 MFM Write Data Synchronization – The precompensation ROM sends the MFM data to the output write data sync circuit for transfer to the diskette drive. This sync circuit, clocked at 8 MHz, allows the correct accessing time for the precompensation ROM to pass the serial MFM write data to the diskette drive.

Table 7-5 MFM Encoding

Data Already Sent		Data to be Sent		MFM
X	1	1	1	Early
X	0	1	1	Late
0	0	0	1	Early
1	0	0	0	Late

Table 7-6 Precompensation MFM Data Pulse Shift

	TK0-43	TK44-60	TK61-79
Early	125 ns	250 ns	375 ns
Late	125 ns	250 ns	375 ns

7.3.5 MFM Read Data Interface

The MFM read data interface function (Figure 7-8) converts the MFM encoded data from the diskette drive to 8-bit bytes for the sector buffer. The following circuits are used to perform this operation.

Microprocessor
Controller module
Data separator/phase-locked loop

7.3.5.1 Data Separator and Phase-Locked Loop Operation – The controller module controls the operation of the data separator and phase-locked loop. A variable frequency oscillator enable signal (VFOE) enables the data separator and phase-locked loop to lock onto the frequency and phase of the read data signal (RD DATA) received from the diskette drive. The data is locked in phase with read clock (RD CLK), derived from the read data, and passed to the controller module and microprocessor.

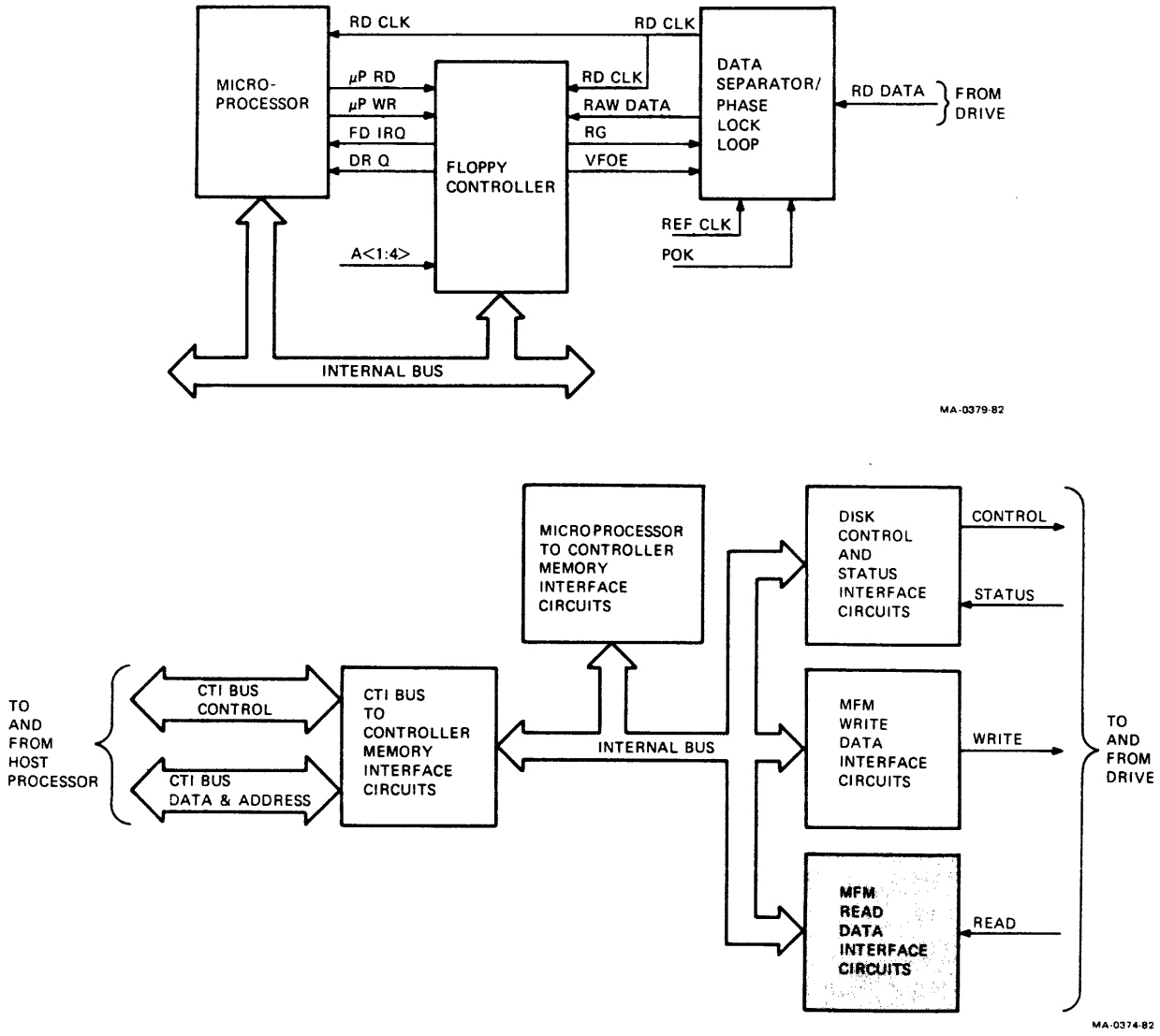


Figure 7-8 MFM Read Data Interface Circuits

Along with the read data, the data separator and phase-locked loop generates a data pulse (RAW DATA) for every RD DATA pulse from the diskette drive. The controller module searches for data fields of all 1s or 0s, then asserts a read gate signal (RG). When RG is asserted, the data separator and phase-locked loop synchronizes with the incoming read data.

After the data field of the target sector has been read, or a time-out error occurs, the controller module deasserts the VFOE signal. This enables the phase-locked loop to lock onto a 500 kHz signal (REF CLK) and stay within the capture range for the next read cycle.

7.3.5.2 Read Data Byte Conversion and Transfer – A read data operation is performed after the host processor loads the appropriate registers. The microprocessor read and write signals (μPRD and μPWR), used during a microprocessor to controller memory interface function, also control access to the controller module over the internal bus. This allows the microprocessor to control the controller module operations and access the controller module registers when executing commands.

After the controller module executes a command, it generates an interrupt (FDIRQ) for the microprocessor. This signal indicates that the microprocessor can send another command to the controller module, or the microprocessor can read the controller module status registers. When the controller module accumulates a data byte it decoded from the read data (RAW DATA), the controller module generates a data ready signal (DRQ) for the microprocessor.

None of the controller module data, status, or command registers are directly accessible by the host processor. The microprocessor reads and writes commands and data to the controller module registers over the internal bus to or from the memory.

7.3.6 Module Data Flow

This paragraph provides two examples of data flow, a drive command data flow and a write data flow. These examples do not follow the command sequences of the microcode, but are presented to help you understand the RX50 controller module capabilities.

Drive Command Data Flow

When the host processor sends a command to the diskette drive, the following events occur.

- The host processor sends the address of the register it wants to access to the controller module.
- The host processor asserts the CTI Bus control signals in the correct sequence. This activates the controller module to accept the address.
- The address is loaded into the address latch.
- The host processor places the data for the register on the CTI Bus address/data lines.
- The host processor asserts the CTI Bus control signals in the correct sequence. This activates the controller module to accept the data and load it into the sector buffer/command and status registers.
- The microprocessor then performs the command and calculates any values designated by the command.
- The microprocessor accesses the controller module registers to perform the designated command.
- The microprocessor and controller module generate the appropriate signals for the unit selection decoder and output drivers.

Write Data Flow
When the host processor sends data to the diskette drive for storage, the following events occur.

- The host processor sends the address of the register it wants to access to the controller module.
- The host processor asserts the CTI Bus control signals in the correct sequence. This activates the controller module to accept the address.
- The address is loaded into the address latch.
- The host processor then places data words for the register on the CTI Bus address/data lines, and asserts the CTI Bus control signals in the correct sequence. This activates the controller module to accept the data and load it into the sector buffer/command and status registers.
- When transferring data, the host processor continually accesses the data register to transfer data from the CTI Bus to the internal I/O bus to the sector buffer/command and status registers.
- When the transfer from the host processor to the controller module is complete, the microprocessor places the data words from the sector buffer on the internal I/O bus. The microprocessor then loads the data word into the controller module.
- The controller module and microprocessor then convert the data bytes to precompensated MFM data.
- For every data word shifted out, the controller module generates a status signal for the microprocessor to request another data word.
- The controller module accumulates and adds two CRC bytes after the original write data is serially shifted out.

7.4 DETAILED CONNECTOR DESCRIPTIONS
Paragraphs 7.4.1 and 7.4.2 describe the controller module connections.

7.4.1 CTI Bus Interface J1
The controller module uses the data/address and control lines of the CTI Bus to implement program data transfers. Figure 7-9 shows the J1 pin functions and signal directions. Refer to Chapter 5 in the *Professional 300 Series Technical Manual Volume 1* for more details.

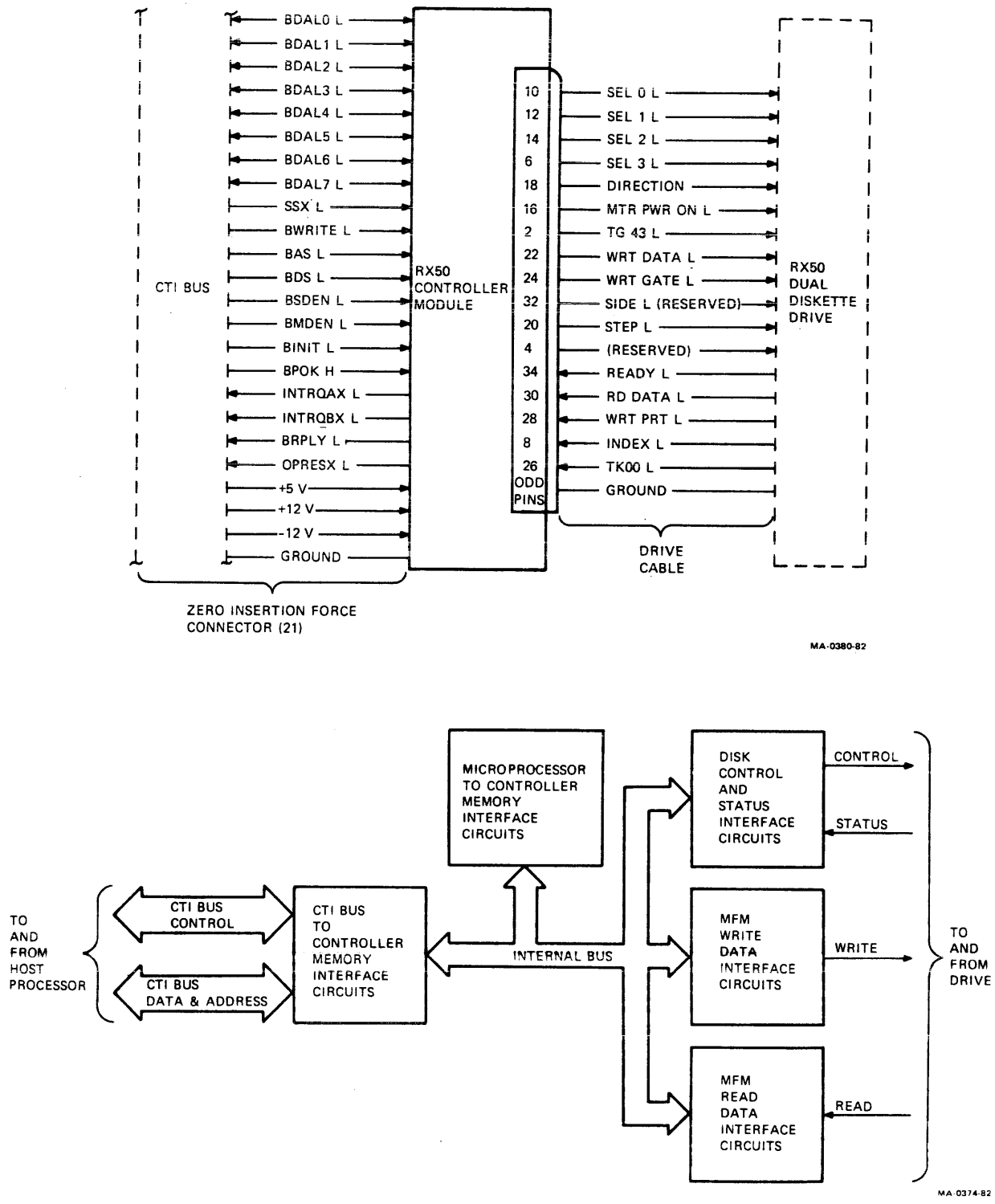


Figure 7-9 RX50 Controller Module Interface Signal Flow

7.4.2 Drive Interface Connector J2

Table 7-7 lists the J2 connector pin functions. The signal mnemonic column also describes each signal's asserted state. An L after the mnemonic indicates an asserted low state (logic zero). An H after the mnemonic indicates an asserted high state (logic high).

Table 7-7 Connector J2 Pin Description

Pin	Signal Name	Signal Mnemonic
1	Ground	
2	Track 43	TG 43 I
3	Ground	
4	Reserved	
5	Ground	
6	Drive select 3	SEL 3 L
7	Ground	
8	Index	INDEX L
9	Ground	
10	Drive select 0	SEL 0 L
11	Ground	
12	Drive select 1	SEL 1 L
13	Ground	
14	Drive select 2	SEL 2 L
15	Ground	
16	Motor power on	MOTOR PWR ON L
17	Ground	
18	Direction	DIR L
19	Ground	
20	Step pulse	STEP L
21	Ground	
22	MFM write data	WRT DATA L
23	Ground	
24	Write gate	WG L
25	Ground	
26	Track 0	TRK 00 L
27	Ground	
28	Write protect	WRT PRT L
29	Ground	
30	MFM read data	RD DATA
31	Ground	
32	Reserved	SIDE
33	Ground	
34	Drive ready	READY L

7.4.2.1 TKG43 L Output Signal – The controller module generates this signal and asserts it when writing data to tracks 44 through 79. In the asserted state, the selected diskette drive reduces the write current. This occurs because there are higher bit densities at the inner tracks.

7.4.2.2 SEL 0 through SEL 3 Output Signals – These signals select one of four diskettes to which the controller module connects.

7.4.2.3 TK 00 L Input Signal – This signal indicates that the read/write heads in the selected diskette drive are over track 0 (the outermost track). This indicator signal is valid only when a diskette drive is selected.

7.4.2.4 MOTOR PWR ON L Output Signal – This signal controls the spindle motor in the selected diskette drive. When this signal is asserted, the spindle motor rotates. The spindle motor reaches the rated rotating speed within 1/4 second after an asserted MOTOR PWR ON signal.

7.4.2.5 DIR Output Signal – This signal defines the moving direction of the selected read/write head when STEP output line is pulsed. Step out (moving away from the center of the disk) is defined as the HIGH level of this signal (logic 1). Step in (moving toward the center of the disk) is defined as the LOW level of this signal (logic 0).

7.4.2.6 STEP L Output Signal – Each time this signal is pulsed, the read/write heads in the selected diskette drive move one track. The heads move in the direction specified by the DIR signal. The minimum pulse width is 1 μs. The minimum time between step pulses is 6 ms. This signal is ignored by the diskette drive when WRITE GATE L is asserted, MOTOR ON L is deasserted, or the diskette drive is not selected.

7.4.2.7 WRT DATA L Output Signal – This signal is data to be stored on the diskette. The falling edge of each transition of the signal represents an MFM encoded clock or data pulse. Write pulses should not assert within 500 ns after WRITE GATE is asserted. A minimum of 36 ms for head settling is required after the last STEP pulse. Write pulses are ignored when WRITE GATE or MOTOR ON are deasserted, the diskette is write protected, no diskette is present, or no diskette drive is selected.

7.4.2.8 WG L Output Signal – This signal enables write operations of the selected diskette drive. This signal is ignored by the diskette drive if the selected diskette is write protected.

7.4.2.9 INDEX L Input Signal – The leading edge of this pulse signal indicates the detection of the index hole in the selected diskette drive side. The INDEX L pulse is valid 250 ms after MOTOR ON L is asserted.

7.4.2.10 WRT PRT L Input Signal – When asserted, this signal indicates that the write enable notch of the selected diskette in the diskette drive is masked. Writing of new data is also inhibited.

7.4.2.11 RD DATA L Input Signal – This signal is data retrieved from the diskette. RD DATA L is valid when the following conditions exist.

- 250 ms after MOTOR ON L is asserted
- 36 ms after the last STEP L pulse
- 1.3 ms after the WRITE GATE signal is deasserted
- 30 ms after the diskette drive is selected

7.4.2.12 READY Input Signal – This signal indicates that a diskette is present in the selected diskette drive.

7.5 PROGRAMMING

The controller module contains 11 registers for communication with the host CPU. Nine registers pass data, commands, and status information between the host processor and the controller module. Two registers are command-only registers. Addressing either of these registers performs a command, but reading or writing data has no affect.

Table 7-8 shows the functions, types, and addresses of the controller module registers described in this paragraph.

All communication between the controller module and the host processor is through these registers. All registers, except the data buffers, are accessed at random. The data buffers can only be accessed sequentially.

The CPU controls the registers unless the controller module is performing a command. The longest response time to finish any command is 4 seconds.

The control and status registers (CS0, CS1, CS2, CS3, CS4, and CS5) are used in four modes: command mode, read/write status mode, maintenance status mode, and extended function mode. The command mode allows the host processor to send commands to the controller module. The read/write status mode allows the host processor to read the status information of completed read sector or write sector commands. The maintenance status mode allows the host processor to read the status information of a completed maintenance command. The extended functions mode allows the host processor to access extended function commands or status information.

Table 7-8 RX50 Controller Module Registers

Description	Type	Address
RX5ID identification register	Read only	X00
RX5CS0 CSR 0	Read status/write command	X04
RX5CS1 CSR 1	Read status/write command	X06
RX5CS2 CSR 2	Read status/write command	X10
RX5CS3 CSR 3	Read status	X12
RX5CS4 CSR 4	Read status	X14
RX5CS5 CSR 5	Read status/write command	X16
RX5DEB data buffer output	Read only	X20
RX5CA clear address register	–	X22
RX5GO start command register	–	X24
RX5FB data buffer input	Write only	X26

NOTE

Address X02 (octal) is reserved for use by the CTI Bus protocol sequence. Writing to this register does not affect the RX50 controller module's operation. Reading this register provides a null word to the host processor.

To access the command mode, the host processor writes to CS0, CS1, CS2, CS3, and CS5. Writing to CS4 has no affect on the controller module operation. The registers are set up for read/write status mode, maintenance status mode, or are used in the extended status mode during a command mode access to CS0 (Paragraph 7.5.2.1). The selected status mode information can then be read from CS0, CS1, CS2, CS3, and CS4 after the host processor receives a command complete interrupt.

Paragraphs 7.5.2 through 7.5.7 provide the bit definitions for each CS register mode operation.

7.5.1 RX5ID Identification Register (X00)

Location X00 contains a unique fixed code that identifies the controller module to the host processor. This is a read-only register that returns an ID number of 04 (hexidecimal) on the BDAL 0–7 lines to the host processor.

7.5.2 RX5CS0 Register (X04)

In the command mode, this register is the primary control link between the host processor and the controller module. The host processor uses this register to command all functions to be performed by the controller module.

This register also selects the registers to contain read/write status information, maintenance status information, or to be used in the extended function mode while in the command mode.

7.5.2.1 Command Mode Bits – When the host processor writes to this 8-bit register from the BDAL 0–7 L lines, each bit is defined as shown in Figure 7-10.

Bits 1 and 2 – The following bits select the specified diskette drive and the function to be performed.

Bit 2	Bit 1	Selected Drive / Diskette
0	0	Drive 1 / diskette A
0	1	Drive 1 / diskette B
1	0	Drive 2 / diskette A
1	1	Drive 2 / diskette B

Bit 3 Extended Motor Time-out – This bit allows the host processor to extend the time that the spindle drive motor rotates after the last disk transfer operation is complete. When this bit is clear, the spindle rotates for 3 seconds after the last read/write command. When this bit is set, the spindle rotates for 30 seconds after the last read/write command.

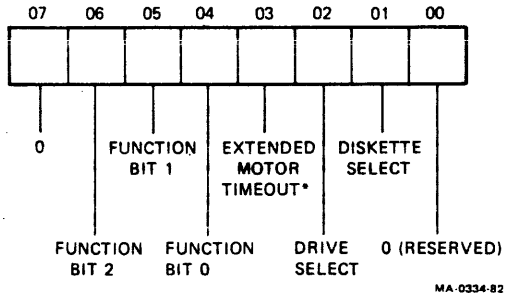


Figure 7-10 RX5CS0 Command Mode Bit Definitions

Bits 4, 5, and 6 – These three bits specify the function that the subsystem performs, and the mode information retrieved during a read register operation, as follows.

Bit 6	5	4	Function	Mode Type
0	0	0	Read status	Maintenance status
0	0	1	Main mode	Maintenance status
0	1	0	Restore drive	Maintenance status
0	1	1	RX INIT	Maintenance status
1	0	0	Read sector	Read/write status
1	0	1	Extend functions	Extended read/write status
1	1	0	Read address	Read/write status
1	1	1	Write sector	Read/write status

Read Status (000)
This function instructs the controller module to supply the current status of the selected diskette drive and diskette at the current track. During this function, no diskette drives are accessed or restored, and no maintenance tests are performed. After this function is complete, an INTRQA is asserted. Valid maintenance status information is contained in the RX5CS0 through RX5CS4 registers. The primary status of interest for this function is the current status (RX5CS3), which contains the volume changed information. All volume change bits are reset after this command, and INTRQB is re-enabled.

Maintenance Mode (001)
This function instructs the controller module to perform an internal self-diagnostic test routine and provide maintenance status information in the RX5CS0 through RX5CS4 registers.

The host processor obtains a profile of the operating status of the currently installed drives. The profile is used mainly for diagnostic exercises and system start-up. After this function is complete, an INTRQA is asserted. Valid maintenance status information is contained in the RX5CS0 through RX5CS4 registers.

Restore Drive (010)
This function instructs the specified diskette drive to seek to track 0. The host processor restores one diskette drive at a time without performing any read/write operations. Valid maintenance status information is contained in the RX5CS0 through RX5CS4 registers.

RX INIT (011)
This function instructs the controller module to restore both diskette drives to track 0, check the current drive status, and perform an internal self-test of the controller module. This function performs the same operation as the system start-up, or asserting the BINIT signal on the CTI Bus. After this function is complete, an INTRQA signal is asserted. Valid maintenance status information is contained in the RX5CS0 through RX5CS4 registers.

Read Sector (100)
This function instructs the controller module to read 512 data bytes from the specified diskette drive, diskette, track, and sector. It then stores the 512 data bytes in the sector buffer (accessed through the RX5EB register by the host processor) and updates the RX5CS0 through RX5CS3 registers with read/write status information. After this function is complete, an INTRQA is asserted.

Extend Functions (101)
This function instructs the controller module to access the RX5CS5 (X16) register for the actual function the controller module will perform. Refer to Paragraph 7.5.7 for details on the extended function commands.

Read Address (110)
This function instructs the controller module to read the first encountered header at the current track location of the selected diskette drive and diskette. The controller module then transfers six bytes to the sector buffer. These six bytes are the TRACK ADDRESS, SIDE ADDRESS, SECTOR ADDRESS, SECTOR LENGTH, HEADER CRC 1 and HEADER CRC 2 bytes, in that order. After the function is complete, an INTRQA is asserted. Valid read/write status information is contained in the RX5CS0 through RX5CS4 registers. The host processor accesses the sector buffer through the RX5EB register.

Write Sector (111)
This function instructs the controller module to transfer the sector buffer contents (the 512 bytes previously stored in the RX5FB by the host processor) to the specified diskette drive, diskette, track, and sector. The controller module then updates the RX5CS0 through RX5CS4 registers with read/write status information. After this function is complete, an INTRQA is asserted.

NOTE
The host processor needs no response to the INTRQA (disable INTRQA), and checks the DONE bit instead of INTRQA.

The internal bus is available to the host processor after the DONE bit is asserted.

The internal bus is available to the host processor 6 μs after INTRQA is asserted.

7.5.2.2 Maintenance Status Mode – The following status information is available to the host processor when the controller module performs any maintenance function (function code 000, 001, 010, or 011). The register contents can be read back from the controller module to the host processor. The contents are valid 6 μs after INTRQA is asserted or immediately after the DONE bit is set.

Figure 7-11 shows the bit definitions for the RX5CS0 register in maintenance status mode. The bit definitions are the same as for the RX5CS0 register in command mode.

Bit 3 – When asserted, this bit indicates that the controller module is not busy and the host processor can access all registers. If the controller is performing a command when the host processor tries to read this register (or any register), a null byte is returned and this bit is deasserted (0 = BUSY, 1 = DONE).

Bit 7 – When asserted, this bit indicates that an error occurred when the controller module performed the last function. To determine the cause of the error, the error code in RX5CS1 (error register X06) is read (0 = no error, 1 = error).

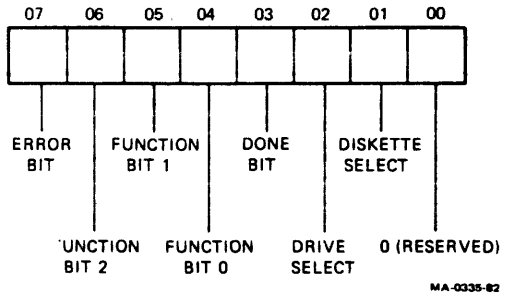


Figure 7-11 RX5CS0 Maintenance Status Mode Bit Definitions

7.5.2.3 Read/Write Status Mode – The contents of this register are the same as in the maintenance status mode when the controller module performs any read/write function (function code 100, 110, or 111). The contents can be read back from the controller module to the host processor. The contents are valid 6 μs after INTRQA is asserted or immediately after the DONE bit is set.

7.5.3 RX5CS1 Register (X06)

In the command mode, this register is loaded with the target track number by the host processor. In the extended function mode, this register is loaded with the number of tracks that the formatted diskette contains. This register is selected to contain maintenance status information, read/write status information, or extended function mode status information by command mode accesses to the RX5CS0 register.

7.5.3.1 Command Mode Bit – In the command mode, a data word that specifies the target track is written to this 8-bit register from the BDAL 0–7 lines. The accepted range of valid track numbers is 00 to 4F (hexadecimal). Figure 7-12 shows the bit definitions for the RX5CS1 register in command mode.

7.5.3.2 Maintenance Status Mode – The following maintenance status information is available to the host processor when the controller module performs any maintenance function (function code 000, 001, 010, or 011). The register contents can be read back from the controller module to the host processor. The contents are valid 6 μs after INTRQA is asserted, or immediately after the DONE bit is set.

The RX5CS1 register contains information that describes the cause of the error when the controller module performed the last maintenance command. Table 7-9 describes the register contents and the specific maintenance mode function error.

7.5.3.3 Read/Write Status Mode – The RX5CS1 register contains an error code for the host processor. The error code is issued if an error occurred when the controller module performed any read/write functions (function code 100, 101, 110, or 111) or extended functions (extended function code 000, 001, 010, 011, 100, or 101). The register contents can be read back from the controller module to the host processor. The contents are valid 6 μs after INTRQA is asserted, or immediately after the DONE bit is set.

Table 7-10 describes the error codes and the related errors.

7.5.3.4 Extended Functions Mode – When this register is used with any extended function command, it contains an error code for the host processor. The error code occurs after the function was commanded to execute.

This register mode is used with the set format parameters extended function command. It is loaded by the host processor with the track parameter for reading RX50 and non-RX50 formatted diskettes.

A 120 octal value reads a diskette with 80 tracks. A 50 octal value reads a diskette with 40 tracks.

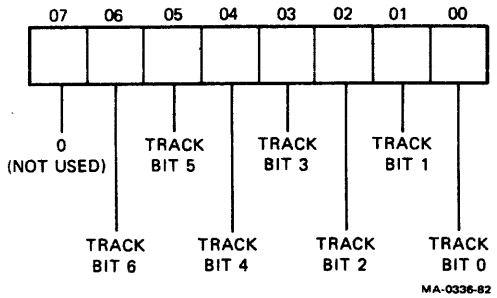


Figure 7-12 RX5CS1 Command Mode Bit Definitions

Table 7-9 Maintenance Status Mode Definitions

Octal Code	Error Code Meaning
300	Lower nibble of RAM failed to pass memory test
310	Higher nibble of RAM failed to pass memory test
320	No index pulse detected
330	Drive speed not within limit
340	Bad format or blank disk
350	Stepping error
360	PLL frequency not within limit
370	Bad data buffer

Table 7-10 Read/Write Status Mode Definition

Octal Code	Error Code Meaning
000	No error
010	Drive 0 track 00 sensor failed
020	Drive 1 track 00 sensor failed
030	Both drives failed to respond (no drives in system)
040	Tried to access unspecified track number
050	Drive fails to see home
060	Data record not found; DAM not found within 43 bytes after ID
070	ID record not found
100	Time-out for FD command done
110	Reserved
120	Selected diskette not ready
130	Diskette not installed correctly
140	ID CRC
150	Seek error
160	DRQ did not occur within 32 ms
170	Soft ID read error
200	Data CRC
210	Lost data (8051 did not respond to DRQ within 23 μs)
220	Tried to access an unavailable diskette
230	Drive not ready during write command
240	Drive not ready during read command
250	No sector matches specified sector
260	Diskette write protected on write command
270	Tried to access nonspecified sector number
354	Tried to set unsupported diskette parameters
364	Tried to read sector with deleted data mark
374	Tried to write to non-RX50 formatted diskette

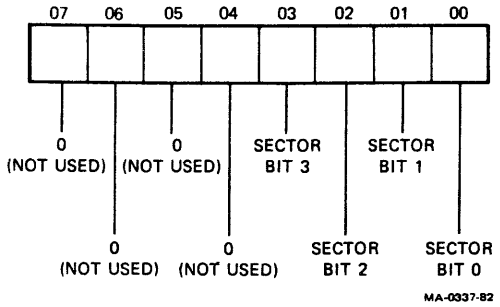


Figure 7-13 RX5CS2 Command Mode Bit Definitions

7.5.4 RX5CS2 Register (X10)

In the command mode, this register is loaded with the target sector number by the host processor. This register is selected to contain read/write status information, maintenance status information, or be used in the extended function mode by command mode accesses to the RX5CS0 register.

7.5.4.1 Command Mode – In the command mode, a data word that specifies the target sector number is written to this 8-bit register from the BDAL 0–7 lines. The accepted range of valid sector numbers is 01 to 0A (hexadecimal). Figure 7-13 shows the bit definitions for the RX5CS2 register in command mode.

7.5.4.2 Maintenance Status Mode – The following status information is available to the host processor when the controller module performs any maintenance function (function code 000, 001, 010, or 011). The contents of this register can be read back from the controller module to the host processor. The register contents are valid 6 μs after INTRQA is asserted, or immediately after the DONE bit is set.

The RX5CS2 register contains the current head position (track number) of the unit specified in the input command register. The bit definitions are the same as for the RX5CS1 register in command mode.

7.5.4.3 Read/Write Status Mode – This register contains status information for the host processor when the controller module performs a read sector (function code 100), read address (function code110), and write sector (function code 111) command. The information is also available when the controller module performs a read with retries (extended function code 000), a write sector with deleted data mark (extended function code 001), or a read and compare command (extended funtion code 101).

The register contents can be read back from the controller module to the host processor. The contents are valid 6 μs after INTRQA is asserted, or immediately after the DONE bit is set.

The RX5CS2 register contains the track number that was specified in the input track register. The bit definitions are the same as for the RX5CS1 register in command mode.

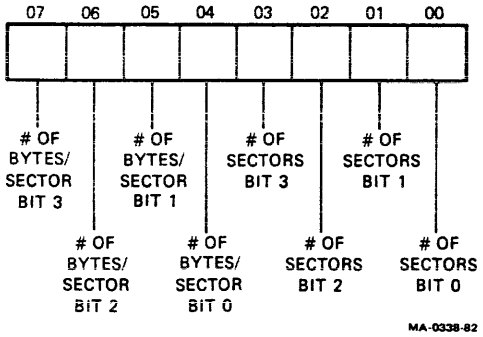


Figure 7-14 RX5CS2 Extended Function Mode Bit Definitions

7.5.4.4 Extended Functions Mode – This register mode is used with three extended functions commands: the report format parameters (extended function code 010), the set format parameters (extended function code 011), and the report controller version (extended function code 100) commands. Each extended function is described as follows.

- After performing a report format parameter function, the RX5CS2 register contains the track quantity of the specified diskette for the host processor. A 120 octal value indicates a diskette with 80 tracks. A 50 octal value indicates a diskette with 40 tracks.

- Before performing a set format parameter function, the host processor loads the RX5CS2 register with a value that indicates the sector quantity and capacity of the selected diskette. Bits 4 through 0 should be loaded with an 11 octal value to select 9 sectors per track, a 12 octal value to select 10 sectors per track, or a 20 octal value to select 16 sectors per track. Bits 7 through 5 should be loaded with a 2 octal value to select 256 bytes per sector or a 3 octal value to select 512 bytes per sector.

- After performing a report controller version extended function, the RX5CS2 register contains an octal number between 0 and 377. This number represents the microcode version of the RX50 controller module for the host processor.

Figure 7-14 shows the bit definitions for the RX5CS2 registers in extended functions mode.

7.5.5 RX5CS3 Register (X12)

This register is not used in the command mode. It contains the read/write status information, maintenance status information, or is used in the extended functions mode by command mode accesses to the RX5CS0 register.

7.5.5.1 Maintenance Mode Status – The following status information is available to the host processor when the controller module performs any maintenance function (function code 000, 001, 010, or 011). The register contents can be read back from the controller module to the host processor. The contents are valid 6 μs after INTRQA is asserted, or immediately after the DONE bit is set.

The lower nibble of the RX5CS3 register contains the status of the selected diskette drive specified by the input command register. During controller initialization, these four bits contain the status of drive 0 side A. If drive 0 does not exist, these bits contain the status of drive 1 side A.

The higher nibble of this register contains the updated volume status since the last read status command. The volume status bits are cleared after the read status command. During controller initialization, the controller module assumes that no media is placed in the diskette drives. The controller module tests for diskette presence and sets the corresponding VOLUME CHANGED bit if media is detected, but INTRQB is deasserted. INTRQB is enabled after the first read status command.

Figure 7-15 shows the bit definitions for the RX5CS3 register in maintenance status.

Bit 0 – Unit n is available.

A 0 means that the specified unit does not physically exist.
A 1 means that the specified unit does physically exist.

NOTE

Bits 0 and 1 are copied from the respective 2 bits in the RX5CS4 (system configuration) register for the specified diskette drive and side.

Bit 2 – Unit n is ready.

A 0 means that the specified unit is not ready.
A 1 means that the specified unit is ready.

Bit 3 – Unit n is write protected.

A 0 means that the specified unit is not write protected.
A 1 means that the specified unit is write protected.

Bit 4 – Volume 0 changed.

Bit 5 – Volume 1 changed.

Bit 6 – Volume 2 changed.

Bit 7 – Volume 3 changed.

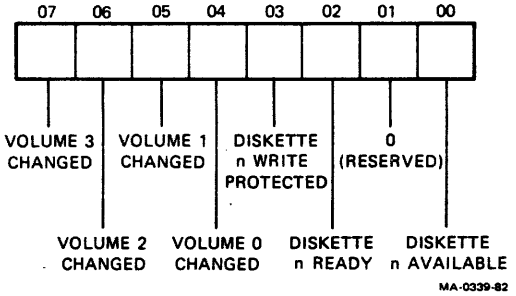


Figure 7-15 RX5CS3 Maintenance Mode Status Bit Definitions

A 0 means that the READY signal did not change since the last read status command.

A 1 means that the READY signal changed since the last read status command.

Any change in the READY signal from the diskette drive sets the associated volume bit. Only the first change after a read status command is performed asserts an INTRQB. Subsequent changes that occur before the next read status command are reported, but INTRQB is deasserted. INTRQB is re-enabled after the next read status command.

7.5.5.2 Read/Write Status Mode – This register mode is available to the host processor when the controller module performs a read sector function (function code 100), a read address function (function code 110), and a write sector command (function code 111). The information is also available when the controller module performs a read with retries (extended function code 000), write sector with deleted data mark (extended function code 001), or read and compare command (extended function code 101).

The contents are valid 6 μs after INTRQA is asserted, or immediately after the DONE bit is set.

The RX5CS3 register contains the sector number that was specified in the input sector register. The bit definitions are the same as for the RX5CS2 register in command mode.

7.5.5.3 Extended Functions Mode – This register mode is used with the report format parameters (extended function code 010) or the set format parameters (extended function code 011) commands. Each extended function is described as follows.

- After performing a report format parameter function, the RX5CS3 register contains values that indicate the sector quantity and capacity of the selected diskette for the host processor. Bits 4 through 0 contain an 11 octal value to indicate 9 sectors per track, a 12 octal value to indicate 10 sectors per track, or a 20 octal value to indicate 16 sectors per track. Bits 7 through 5 contain a 2 octal value to indicate 256 bytes per sector or a 3 octal value to indicate 512 bytes per sector.

Figure 7-16 shows the bit definitions for the RX5CS3 register in extended functions mode.

- Before performing a set format parameter function, the host processor loads the RX5CS3 register with a value to select the track density of the selected diskette. A 1 octal value for bits 1 and 0 selects a 48 track per inch diskette. A 2 octal value selects a 96 track per inch diskette. The remaining bits must be set as shown in Figure 7-17.

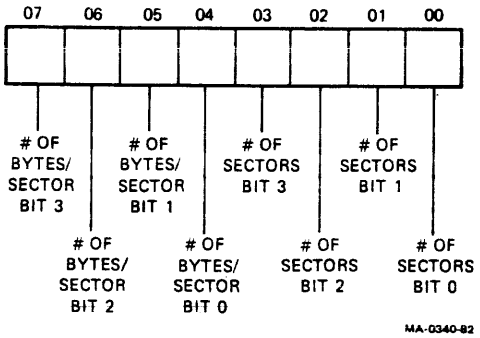


Figure 7-16 RX5CS3 Extended Functions Mode Bit Definitions (Report)

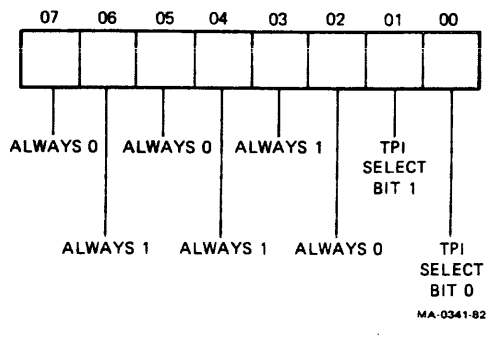


Figure 7-17 RX5CS3 Extended Functions Mode Bit Definition (Set)

7.5.6 RX5CS4 Register (X14)

This register is not used in the command mode. It contains read/write status information, maintenance status information, or is used in the extended functions mode as specified by command mode accesses to the RX5CS0 register.

7.5.6.1 Maintenance Status Mode – The following status information is available to the host processor when the controller module performs any maintenance function (function code 000, 001, 010, or 011). The register contents can be read back from the controller module to the host processor. The contents are valid 6 μs after INTRQA is asserted, or immediately after the DONE bit is set.

The RX5CS4 register contains a summary of the RX configuration that is available for use by the host processor. It is arranged in four groups of two bits each. Each group contains the status of each of the four possible diskette drive sides. It is updated when the controller module is initialized.

Figure 7-18 shows the bit definitions for the RX5CS4 register in maintenance status mode.

For all available bits:
A 0 means that the disk does not physically exist.
A 1 means that the disk does physically exist.

7.5.6.2 Read/Write Status Mode – The following status information is available to the host processor when the controller module performs a read sector function (function code 100), a read address function (function code 110), and write sector command (function code 111). The information is also available when the controller module performs a read with retries (extended function code 000), a write sector with deleted data mark (extended function code 001), or a read and compare command (extended function code 101).

The register contents can be read back from the controller module to the host processor. The contents are be valid 6 μs after INTRQA is asserted, or immediately after the DONE bit is set.

The contents of the RX5CS4 register are valid only when a SEEK error occurs while performing a command. This register contains the track address of the read/write heads. If no SEEK error occurs, this register contains all 0s.

Figure 7-19 shows the bit definition for the RX5CS4 register in read/write status mode.

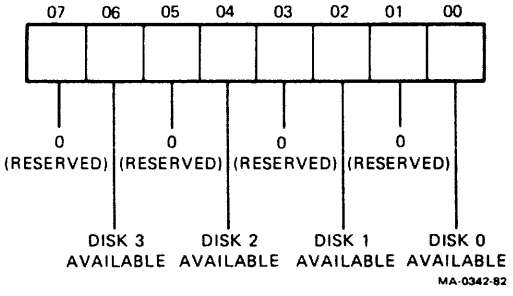


Figure 7-18 RX5CS4 Maintenance Status Mode Bit Definition

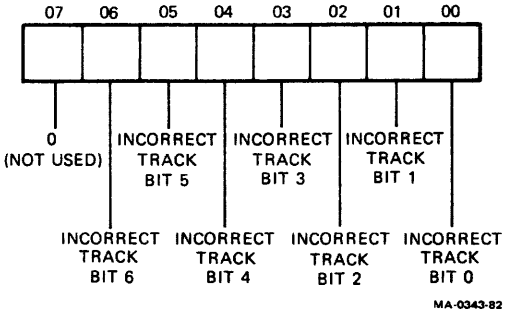


Figure 7-19 RX5CS4 Read/Write Status Mode Bit Definition

7.5.6.3 Extended Functions Mode – This register mode is used with the report format parameters (extended function code 010). After performing a report format parameter function, the RX5CS4 register contains a value that indicates the track density of the selected diskette for the host processor. A 1 octal value for bits 1 and 0 selects a 48 track per inch diskette. A 2 octal value selects a 96 track per inch diskette. The remaining bits must be set as shown in Figure 7-20.

7.5.7 RX5CS5 Register (X16)

This register selects the extended functions command to be performed when an extended functions (function code 101) command is indicated in the RX5CS0 register. The host processor loads this register with one of six codes to select one of six extended functions.

Figure 7-21 shows the bit definitions for this register.

Figure 7-22 shows the selectable extended functions.

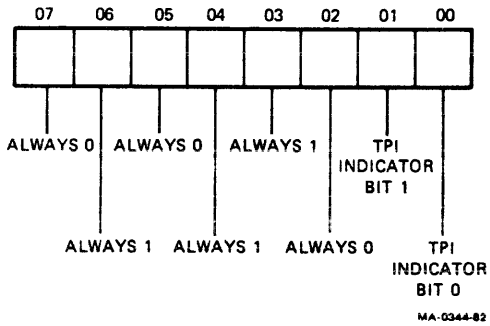


Figure 7-20 RX5CS4 Extended Functions Mode Bit Definition

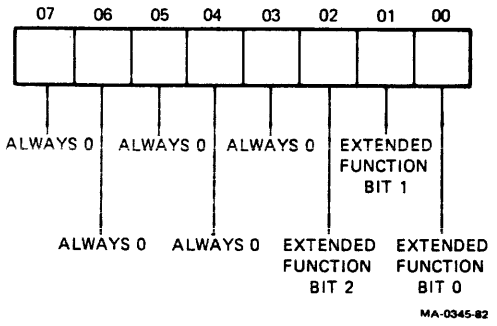


Figure 7-21 RX5CS5 Bit Definitions

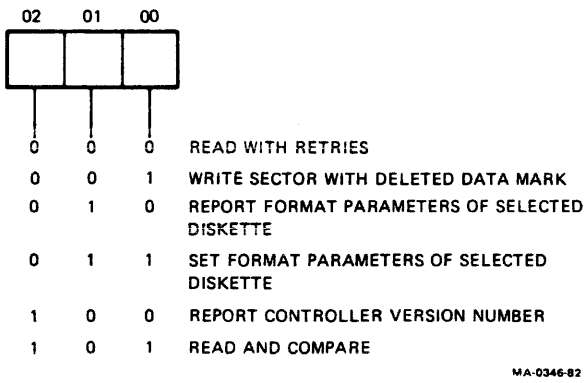


Figure 7-22 RX5CS5 Selectable Extended Functions

7.5.7.1 Read With Retries (000) – This extended function is the same as the read sector function, except the controller module repeats the read sector operation up to 10 times until it finds a good sector. Retries are performed when ID CRC, DATA CRC, DATA RNF, or LOST DATA errors are detected.

If an error is detected in all 10 retries, an INTRQA is asserted with the error bit set. The error register (RX5CS1) contains the error code that represents the last error occurrence. If a bad sector is detected, and a good sector is subsequently encountered, INTRQA is asserted and the error bit is cleared. The error register contains the appropriate error code for diagnostic purposes. The number of retries is not provided.

If no error is detected, the RX5CS0 through RX5CS4 registers contain the standard read/write status information as previously described.

7.5.7.2 Write Sector With Deleted DATA MARK (001) – This extended function is the same as a write sector function, except the deleted data mark is set in the sector header. Data is written from the sector buffer to the target track and sector as in the write sector function.

Performing a read sector function, or a read sector with retries extended function with a deleted data mark in the target track and sector, results in an error with code 364. The data is read and then placed into the sector buffer for the host processor.

After performing this command, the RX5CS0 through RX5CS4 registers contain the standard read/write status information as previously described.

7.5.7.3 Report Format Parameters of Selected Diskette (010) – This extended function and the set format parameters extended function read non-RX50 formatted diskettes. Four types of formatted diskettes are allowed: the RX50 formatted diskettes and three types of non-RX50 formatted diskettes.

NOTE

The report format parameters and set format parameters extended functions allow for data retrieval from diskettes. Data storage is allowed only on RX50 formatted diskettes. Attempts to store data on a non-RX50 formatted diskette result in an error with code 374 in RX5CS1.

All diskettes must be single-sided, soft-sectored, and use the MFM recording technique. The following diskette formats are allowed.

Format Type	Tracks/ Inch	Total Tracks	Sectors/ Track	Bytes/ Sector
RX50	96	80	10	512
Alternate	48	40	10	512
Alternate	48	40	9	512
Alternate	48	40	16	256

The detected parameters are indicated in the RX5CS2, RX5CS3, and RX5CS4 registers after the function is performed. See Paragraphs 7.5.4.4, 7.5.5.3 and 7.5.6.3 for more information.

7.5.7.4 Set Format Parameters of Selected Diskette (011) – This extended function and the report format parameters extended function read non-RX50 formatted diskettes. Four types of formatted diskettes are allowed: the RX50 formatted diskettes and three types of non-RX50 formatted diskettes.

NOTE

The report format parameters and set format parameters extended functions allow for data retrieval from diskettes. Data storage is allowed only on RX50 formatted diskettes. Attempts to store data on a non-RX50 formatted diskette result in an error with code 374 in RX5CS1.

All diskettes must be single-sided, soft-sectored, and use the MFM recording technique. The following diskette formats are allowed.

Format Type	Tracks/ Inch	Total Tracks	Sectors/ Track	Bytes/ Sector
RX50	96	80	10	512
Alternate	48	40	10	512
Alternate	48	40	9	512
Alternate	48	40	16	256

To select the parameters of the desired diskette, the host processor loads the RX5CS1, RX5CS2, and RX5CS3 registers before a read sector function or read and compare function is performed. Any attempt to set the diskette format to a type not previously listed, causes an error with a code of 354.

7.5.7.5 Report Controller Version Number (100) – After performing this extended function, the RX5CS2 register contains an octal number between 0 and 377. This number represents the microcode version of the RX50 controller module for the host processor.

7.5.7.6 Read and Compare (101) – This extended function is similar to a read sector function, except the host loads the sector buffer with data. Each byte read from the diskette is compared to its corresponding byte in the sector buffer. If the comparison fails for any byte, the error bit is set and an error code of 374 is located in the RX5CS1 register.

After performing this command, the RX5CS0 through RX5CS4 registers contain the standard read/write status information as previously described.

7.5.8 RX5EB Empty Data Buffer (X20)

This 8-bit wide 512-byte data buffer can be read by the host processor from the BDAL 0–7 L lines any time the controller module is not performing a command. See Paragraph 7.5.9 for more information about the sector data buffer.

Figure 7-23 shows the bit definitions for the RX5EB.

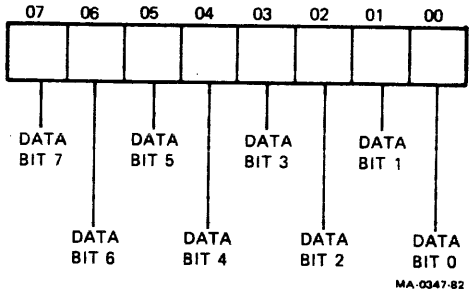


Figure 7-23 RX5EB Bit Definition

7.5.9 RX5CA Clear Address (X22)

Any access to this register by the host processor clears the sector data buffer address to zero.

The host processor and the controller module use a 512-byte sector buffer as an intermediate storage area for writing and reading sector information to and from the diskette. The controller module performs automatic address sequencing after each sector buffer access.

The address should be reset to zero before the host processor starts to either fill (access RX5FB X26) or empty (access RX5EB X20) the sector buffer. The fill or empty operations continue from the last accessed location if no intermediate clear address is issued.

The buffer is exactly 512 bytes long. Continued accesses after the 512th byte returns the pointer to location zero. Specific address information is not available for reading by the host processor.

7.5.10 RX5GO Start Command (X24)

If the host processor accesses this register, the controller module performs the function specified in the command registers. When commanding any function, this access should be the last in a series of instructions issued by the host processor. When the host processor accesses this register, the controller module gains control of the internal bus. After the controller module finishes performing the command it asserts INTRQA. Then 6 μs later, the host processor gains control of the controller module. The host processor can also gain control of the controller module after the DONE bit is set.

7.5.11 RX5FB Fill Sector Buffer (X26)

This 8-bit wide, 512-bytes sector buffer can be written to by the host processor from the BDAL 0–7 L lines any time the controller module is not performing a command. Figure 7-24 shows the bit definitions for the RX5FB.

7.5.12 Command and Status Register Summary

Table 7-11 is a summary of the RX4CS0 through RX5CS4 command and status registers.

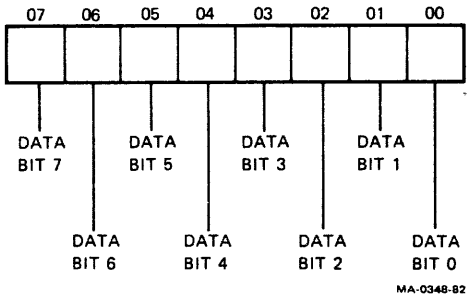


Figure 7-24 RX5FB Bit Definition

Table 7-11 Command and Status Register Summary

Register Write	Command Read	Read/Write Status	Maintenance Read	Extended Functions Read	Write
RX5CS0	Function	Function	Function	Function	Function
RX5CS1	Track*	Error code	Error code	Error code	Tracks¶
RX5CS2	Sector*	Track	Current track	Tracks/version‡	Sector+bytes/sector§
RX5CS3	None	Sector	Current status	Sector+bytes/sector§	TPI
RX5CS4	None	Incorrect track†	System configuration	TPI	None
RX5CS5	Extended	None	None	Extended	Extended

* Only used on read/write sector commands
† Only valid when Seek Error occurs
‡ Number of tracks or version number
§ Number of sectors and bytes per sector
¶ Number of tracks only

7.6 GENERAL OPERATING SEQUENCE

Command and status operations are performed in the following general sequence.

1. The host processor issues a command.
2. The controller module processes and performs the command internally.
3. The controller module then asserts INTRQA and DONE BIT.
4. The host processor responds to either the INTRQA or DONE BIT by reading the status registers to determine the results of the previously issued command.

The controller module asserts INTRQA after all functions are completed. The controller module uses INTRQB to alert the host processor of VOLUME changes.

Status items in the RX5CS0 register are always in the same place. For example, bits 0–2 contain the unit selected, bit 3 is the DONE bit, bits 4–6 contain the specified function, and bit 7 is set if an error occurred in the last command.

The RX5CS1 always contains an error code associated with the last command selected to perform. If the command is performed correctly, this register is cleared. However, if the command is a READ WITH RETRY command, then this register contains the error code of the error that occurred last. If the error bit in RX5CS0 is reset, it indicates that the command is completed. The RX5CS1 might still contain the error code of the last retry error before completion.

While the controller module is busy, any DATA-OUT addressed to the controller module is ignored. However a normal BUS REPLY is issued. Any DATA-IN addressed to the controller module results in a null response byte and a normal BUS REPLY.

The controller module performs automatic scanning of ready status for all drive sides. If the host processor does not issue any other commands within 1.3 ms after the last command is completed, scanning is performed every second. Any changes in the ready status for any drive side are reported to the host processor as a volume change through the INTRQB signal. For correct operation, the operating system should respond to an INTRQB with a read status function. This updates the current status register with the changed status, and clears the volume changed bits after the the command is completed. The controller module issues only one INTRQB between read status commands, no matter how many volume changes are detected.

If the READY signal of the selected unit changes while performing a command, then the command is aborted, the error bit is set, and the error register contains the appropriate error code.

On controller initialization, the CURRENT STATUS register indicates which volumes are currently installed in the diskette drives.

NOTE

If no commands are issued by the host processor within one second after the last command is completed, all drive sides are deselected.

7.6.1 Read/Write Operations

The host processor can store or retrieve data blocks of 512 8-bit bytes on one of the available drive side volumes. To store a data block, the host processor transfers the 512 bytes from the system memory to the sector data buffer contained in the controller module.

A single CTI Bus address, RX5EB register (X20), accesses the sector data buffer for read operations. A single CTI Bus address, RX5FB (X26), accesses the sector buffer for write operations. Accesses to these registers increment the internal sector data buffer pointer after each byte is transferred.

The sector data buffer is cleared by accessing the RX5CA (X22). The host processor specifies one of the 80 tracks to be the target track by loading the track number into the track register (RX5CS1 X06). The host processor then specifies one of the 10 sectors to be the target sector by loading the sector number into the sector register (RX5CS2 X10).

The host processor assembles the parameters required to complete the desired transfer in the RX5CS0 register (X04). The host processor can load these registers in any order. To start the command, the host processor accesses the RX5GO (X24) register, then waits for INTRQA or DONE bit to signal the end of the command.

The following is an example of the host processor sequence for a write sector command.

1. Accesses the RX5CA, which clears the data buffer address to zero
2. Loads the RX5DB with the 512 data bytes to be stored
3. Loads the RX5CS0 with the selected drive, function, and motor time-out option
4. Loads the RX5CS1 with the target track
5. Loads the RX5CS2 with the target sector
6. Accesses the RX5GO, which performs the command
7. Reads the RX5CS0 register when the controller module asserts an INTRQA or DONE bit, which determines the status when the command is completed.

7.6.1.1 Read/Write Status – There are five bytes of status available to the host processor after the controller module completes a read address, read, or write sector command. These bytes are contained in RX5CS0 through RX5CS4.

To determine successful disk transfers, the host processor reads the error bit in RX5CS0. This checks for errors and the performance of the correct function to the correct volume. If an error is detected, the host processor repeats the function or investigates the error cause by using the second byte available in the error register (RX5CS1). The next two available bytes verify that the function occurred on the track and sector (RX5CS2 and RX5CS3) that was specified in the command registers. The last of the five bytes contains the incorrect track number (RX5CS4). This is valid only when a seek error occurs. If a seek error did not occur in the last operation, these bytes will be all zeros. The incorrect track number is also the current head position when a seek error occurred.

NOTE

If a seek error occurs, the controller module automatically identifies the read/write head position. The host processor does not have to restore the diskette drive to reposition the read/write heads, but continues to issue the next command. If a seek error occurs several times, then the host processor might need to restore the diskette drive.

7.6.2 Maintenance Operations

The host processor can direct the controller module to perform an internal self-test. To do this, it specifies the maintenance mode function in the RX5CS0 (function code 001) and accesses the RX5GO register. Neither diskette drive is restored. Status information is contained in the RX5CS0 through RX5CS4 registers. An INTRQA or DONE bit indicates a completed function.

7.6.2.1 Maintenance Status – When the maintenance function is completed, the RX5CS0 through RX5CS4 registers contain the following profile of the current RX subsystem and its operating status.

RX5CS0 – contains the done indication and the error flag from the self-test. The select field contains the volume as specified in the input command. The function field contains the function as specified in the command (code 001).

RX5CS1 – contains the specific error code if an error occurred.

RX5CS2 – contains the current track address used during the maint command.

RX5CS3 – contains a status summary of the volume under test.

RX5CS4 – contains a copy of the system configuration that was connected at initialization.

RX5RDB – contains an incrementing pattern from 00 to FF and then a decrementing pattern from FF to 00 (hexadecimal). The host processor reads this as a final check of the data buffer integrity after a maintenance function. The data buffer contains the same pattern during controller initialization. Failure to detect this pattern indicates that a portion of the internal RAM test failed.

7.6.3 Controller Initialization and Self-Test Sequence

Table 7-12 summarizes the initialization and self-test operations the controller module performs when certain commands are performed.

Table 7-12 Controller Initialization and Self-Test Sequence

Activity	Read Status (000)	MAINT Mode (001)	Restore Unit (010)	RX INIT (011)	Power-up Bus INIT P OK
Drives restored	None	None	1*	2	2
Read media	No	Yes	No	No	No
Track 0 check	No	No	Yes	Yes	Yes
Memory check	No	Yes	No	Yes	Yes
PLL check	No	Yes	No	Yes	Yes
Step check	No	Yes	No	No	No
Format check	No	Yes	No	No	No
Speed check	No	Yes	No	No	No
Update current status register	Yes (A)	Yes (B)	Yes (B)	Yes (C)	Yes (C)
Update system configuration register	No	No	Yes	Yes	Yes

NOTES

1. **Resets VOLUME CHANGED bits after the command.**
2. **VOLUME CHANGED bits are not reset after the command.**
3. **Resets VOLUME CHANGED bits. In this case the controller sets the bits that indicates the presence of a volume.**

* The controller module restores the diskette drive specified in the command register.

7.7 SPECIFICATIONS

The RX50 controller module specifications are as follows.

7.7.1 Electrical Specifications

Power Dissipation

+5 Vdc ±5%	50 mV ripple maximum 800 mA maximum 4 W
+12 Vdc ±5%	100 mV ripple maximum 35 mA maximum 0.42 W
−12 Vdc ±5%	100 mV ripple maximum 35 mA maximum 0.42 W

7.7.2 Environmental Specifications

Temperature	10° to 50°C (50° 104°F)
Humidity	10% to 90%
Wet bulb reading	28°C (82°F)
Dew point	2°C (36°F)
Temperature fluctuation	20°C (36°F) per hour

7.7.3 Physical Specifications

Dimensions

Width	1.27 cm (0.5 in)
Length	20.32 cm (8 in)
Height	13.21 cm (5.2 in)
Weight	200 g (7.2 oz)
Cable length	10 ft maximum #28 AWG flat ribbon cable

Interface connector

CTI connector	60-pin ZIF connector (PN 12-18818-00)
RX connector	34-pin connector AMP 10216-8 or equivalent (PN 12-18762-00)

CHAPTER 8
RX50 DUAL DISKETTE DRIVE

8.1 GENERAL INFORMATION

The RX50 dual diskette drive is the storage component of the RX50 controller and drive subsystem for the Professional 300 Series computer system. Figure 8-1 shows the RX50 drive in relation to the other system components.

8.1.1 Related Documentation

The *Professional 350 Field Maintenance Print Set* (MP-01394-00) provides more information about the RX50 drive.

8.1.2 RX50 Dual Diskette Drive

The RX50 drive is a field replaceable unit (PN RX50-AA) that mounts in the Professional 300 system box. One cable connects the RX50 drive to a controller module (see Chapter 7). One power cable (PN 17-00281) connects the power supply to the RX50 drive.

The RX50 drive is a field replaceable unit rather than a field repairable unit. This chapter does not provide adjustment or alignment procedures, because of the test equipment required. The RX50 drive is adjusted and aligned when it is built.

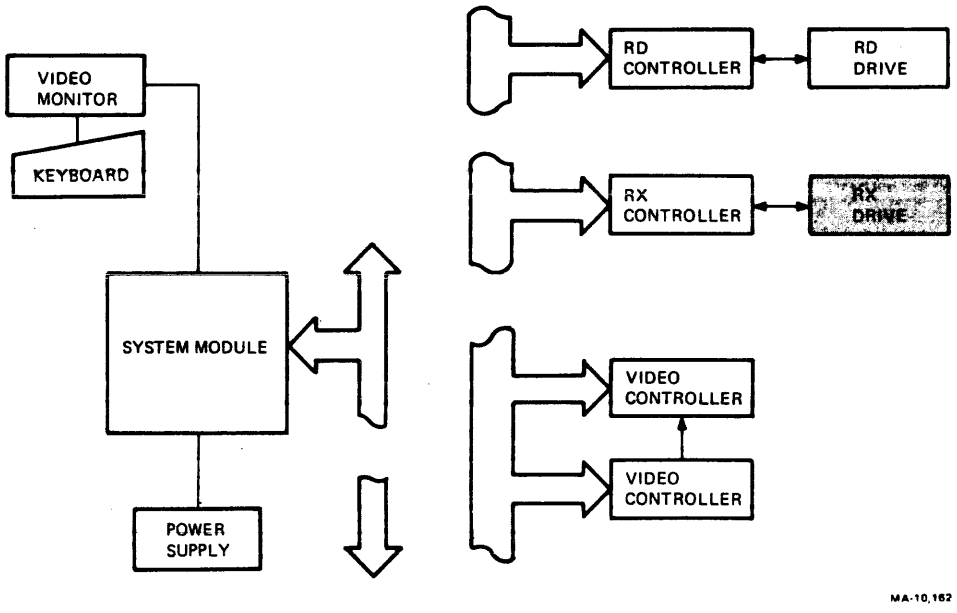


Figure 8-1 RX50 Dual Diskette System Relation

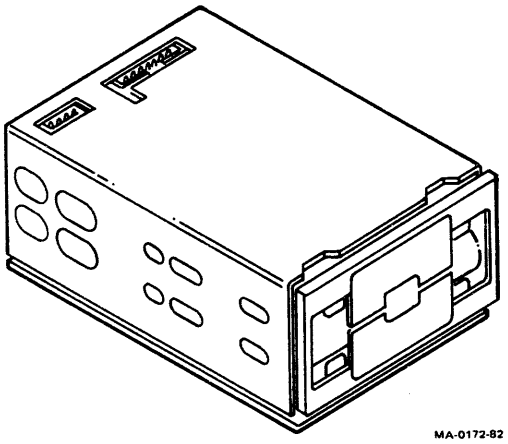


Figure 8-2 RX50 Dual Diskette Drive

8.1.3 Physical Description

Figure 8-2 shows the RX50 drive. The front bezel has two access slots with swinging doors to let you insert or remove diskettes. A head load indicator for each diskette slot comes on when that unit is in use.

NOTE

Do not open either access door if either indicator is on. This damages data stored on either diskette.

Internally, the RX50 drive has two counter-rotating spindles. The spindles are belt driven by a single dc motor/tachometer combination.

Each diskette has a read/write head located back-to-back between the diskettes on a head carriage assembly. The heads are positioned over each track by a single stepper motor/lead screw combination.

The electronic components are mounted on three PCBs. All motors and sensors plug into these boards. The power and interface cables from the controller module plug into one of the PCBs from the top rear of the RX50 drive.

8.1.4 Diskette Description

The RX50 drive uses standard 5.25 in (133.4 mm) square diskettes (Figure 8-3). The recording media is a magnetic oxide coated flexible mylar diskette, 5.125 in (130.2 mm) in diameter. This diskette is contained inside a protective jacket.

The media rotates freely inside the jacket, and is continuously cleaned by the jacket's soft fabric liner. The jacket has four openings: one each for the spindle, the read/write heads, the write protect sensor, and the index sensor.

The write-protect opening is a small square notch along one edge of the jacket. When this opening is covered, the diskette is write protected. For more information see Paragraph 8.1.4.2.

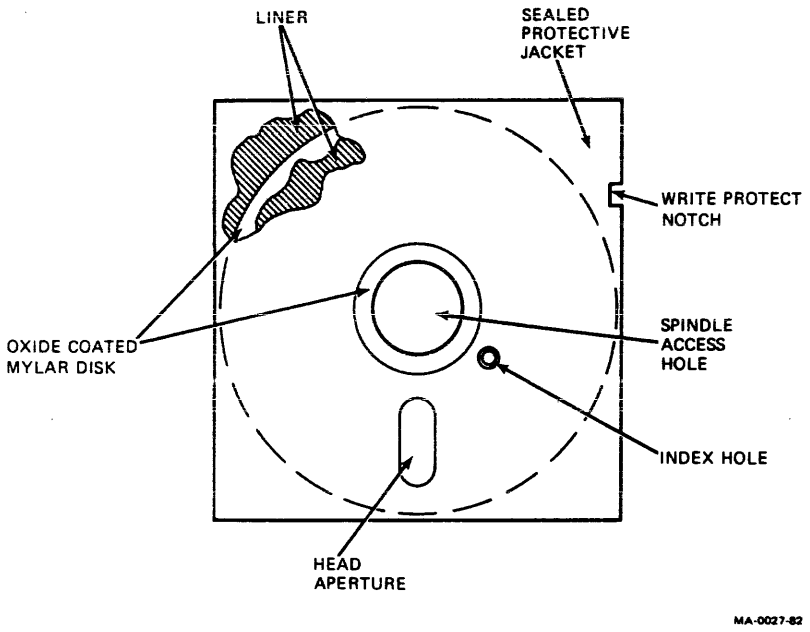


Figure 8-3 The 5.25-inch Diskette

8.1.4.1 Diskette Handling and Storage – Incorrect handling or storage of diskettes can destroy recorded data and damage the read/write head. Handle and store the diskettes as follows.

- Always return the diskette to its protective envelope when it is not installed in the RX50 drive.
- Always store diskettes vertically and loosely to prevent warping the jackets.
- Always mark the diskette jacket with a felt tip pen. Using a pencil or ballpoint pen creases the jacket and damages the mylar media inside.
- Always insert the diskette into the drive carefully. Never force the door closed if it seems to be stuck. This could crush your diskette.
- Never remove or insert a diskette if either indicator is on.
- Never open or close the diskette door if either indicator is on.
- Never touch the mylar recording surface where the jacket is cut away for the read/write heads. Fingerprints dirty the read/write heads and can cause data errors.
- Never store diskettes in direct sunlight or near heaters where temperatures can go above 52°C (125°F). High temperatures warp the jackets.
- Never bend or fold the diskette jacket.
- Never bring the diskette near any strong magnetic fields (5 gauss or more), or touch the diskette with any steel objects. This could erase or weaken the data on the diskette.

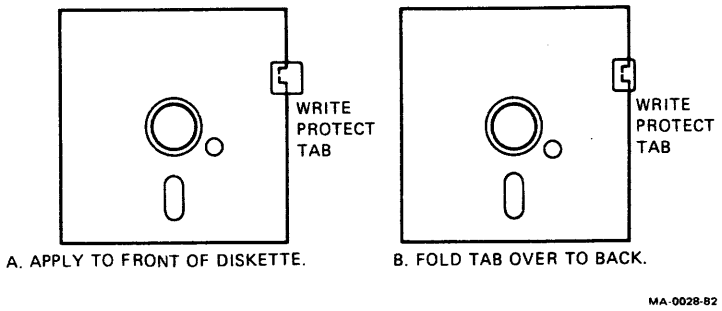


Figure 8-4 Write Protect Tab Application

8.1.4.2 Write Protection of Diskettes – The RX50 drive is equipped with a write-protect feature that protects the diskette from accidental writing. To write protect a diskette, cover the write-protect notch on the edge of the jacket. Most diskettes come with a package of adhesive-backed write-protect tabs.

If write-protect tabs are not available, you can use ordinary adhesive-backed labels. Figure 8-4 shows how to install write-protect tabs.

8.1.4.3 Diskette Loading/Unloading

NOTE
Do not open either RX50 drive door if either indicator is on.

To load a diskette into the RX50 drive, do the following steps.

1. Make sure that both indicators are not on.
2. Open the door for the desired drive side.
3. Correctly orient the diskette to the slot.
4. Insert the diskette until it hits a solid stop.
5. Close the door.

To open the door, press on the door half closest to the outside of the RX50 drive (Figure 8-5). The diskette should be oriented so that the read/write head access slot in the jacket is inserted into the drive first. The drive records on the surface of the diskette closest to the center of the drive (Figure 8-6).

To close the door, gently push the end of the door toward the center of the drive until it is flush with the front bezel (Figure 8-7). Each of the head load lamps on the front bezel come on when the controller module is accessing the diskette on the indicated side.

8.1.5 Configuration Options

An RX50 dual diskette drive can be configured for selection by one of two groups of select signals from the controller module.

One configuration of the RX50 drive does not need a jumper on connector J17 (see Paragraph 8.4.5.7). This enables controller signals DRIVE SEL 0 and DRIVE SEL 1 to select circuits in the drive (see Paragraph 8.3.2.1).

The other configuration of the RX50 drive needs a jumper (PN 12-14314-00) installed on connector J17. This enables controller signals DRIVE SEL 2 and DRIVE SEL 3 to select circuits in the drive.

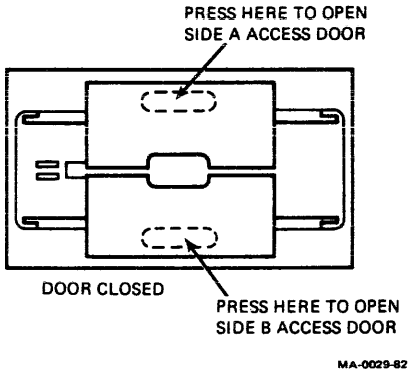


Figure 8-5 Opening Access Doors

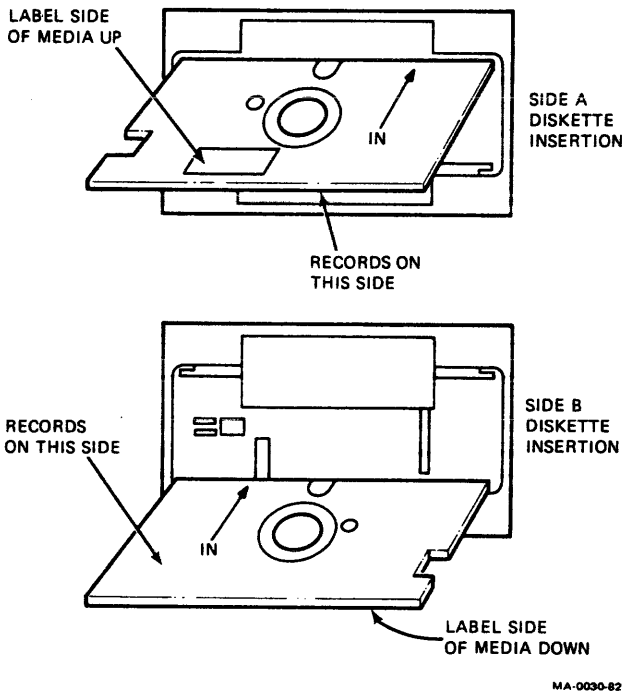


Figure 8-6 Inserting Diskette

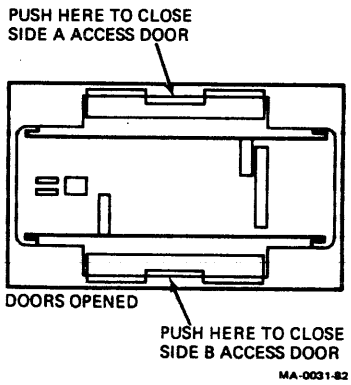


Figure 8-7 Closing Access Doors

8.2 FUNCTIONAL COMPONENTS

Figure 8-8 is a simple block diagram of the RX50 drive. It shows the drive's general operation and data flow.

The RX50 drive has the following elements to perform read, write, and seek operations.

- Seek and interface module
  Select circuits
  Status circuits
  Stepper motor circuit
  Read/write interface circuits

- Motor control module
  Motor control circuit

- Spindle motor

- Two head load solenoids

- Diskette sensors

- Stepper motor

- Read/write module
  Write circuits
  Read circuits

- Two read/write heads

8.2.1 Seek and Interface Module Functions

The seek and interface module has the following circuits.

Select circuits
Status circuits
Stepper motor circuits
Read/write interface circuits

The select circuits act as an interface between the controller module and the RX50 drive. These circuits perform the following functions.

Enable the motor control module
Select the head load solenoids
Select the sensors
Select and enable the circuits in the read/write module

The status circuits connect the sensors to the controller module. These circuits pass status signals to the controller module from the selected sensors.

The stepper motor circuits connect the controller module to the stepper motor. These circuits convert controller signals to stepper motor control signals.

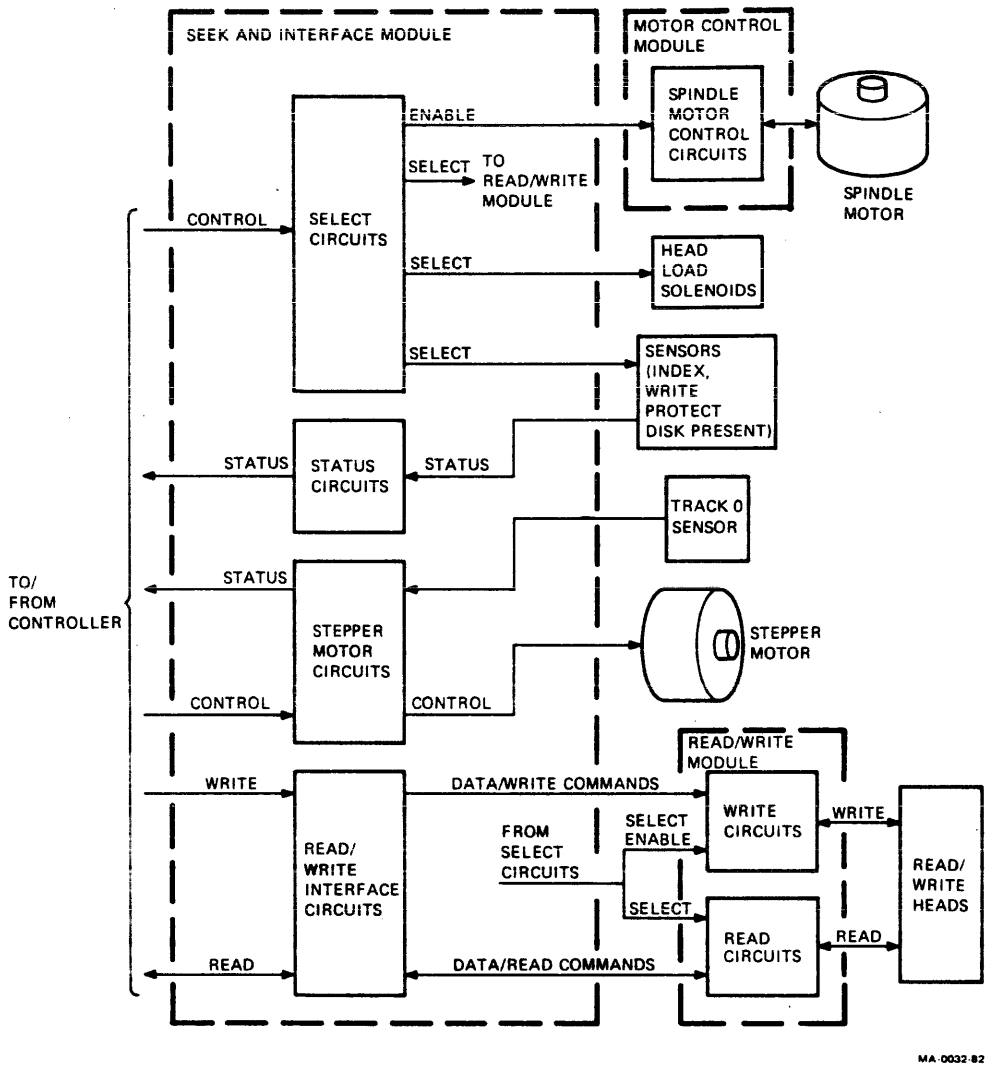


Figure 8-8 Simple Block Diagram

The read/write interface circuits connect the controller module and the read/write module. For a write operation, these circuits pass data and commands from the controller module to the read/write module. For a read operation, these circuits pass commands from the controller module to the read/write module and data from the read/write module to the controller module.

8.2.2 Motor Control Module and Spindle Motor Function

The motor control module contains spindle motor control circuits that control the spindle motor's rotating speed. These circuits are enabled to rotate the spindle motor or disabled to stop the spindle motor, by select circuits.

When enabled, these circuits provide current to the spindle motor to keep it rotating at a constant speed. When disabled, these circuits inhibit current to the spindle motor so it does not rotate.

As the spindle motor rotates, a belt drives two counter-rotating spindles. Each spindle rotates the media in a diskette.

8.2.3 Head Load Solenoid Function

The RX50 drive contains two head load solenoids, one for each read/write head. The selected solenoid releases the head load arm and pad. This applies pressure to the surface of the media and brings the read/write head in contact with the media.

8.2.4 Sensor Functions

The RX50 drive contains two groups of sensors, one group for each side. A sensor group is selected by the select circuits. Each sensor group senses the following conditions.

Presence of a diskette
Write protection status of a diskette
Index of a diskette
Track 0 home position

8.2.5 Stepper Motor Function

The RX50 drive contains a stepper motor that places read/write heads over a data track. The motor is controlled by the stepper motor circuits. As this motor rotates, a head carriage assembly moves the read/write heads over the medis in a linear plane.

8.2.6 Read/Write Module Function

The read/write module contains both read and write circuits. The read circuits convert the analog data sensed by the read/write heads to digital data. The write circuits generate the write currents for the read/write heads to record data on the media.

The read circuits receive a select signal from the select circuits. The select circuits select one of the two read/write heads. A read command from the read/write interface function then enables the read circuits to pass read data to the read/write interface circuits.

The write circuits are enabled by the select circuits. The select circuits select one of the two read/write heads. The write data and commands from the read/write interface circuits then control the currents generated by the write circuits for the heads.

8.2.7 RX50 Drive Set-up Sequence

Before read and write operations, the following set-up sequence must be done.

1. Execute a restore unit command. This turns on the spindle motor and causes it to seek track 0. See Chapter 7 for more information about the RX50 controller module.

2. Load the target track and sector registers. See Chapter 7 for more information.

3. Execute a read or write sector command. This causes the heads to load and the stepper motor to seek the target track. See Chapter 7 for more information.

8.3 THEORY OF OPERATION

Paragraphs 8.3.1 through 8.3.11 describe how the RX50 drive operates.

8.3.1 Drive Mechanism

Paragraph 8.3.1.1 through 8.5.1.5 describe the RX50 drive's mechanical operations. These operations use the following mechanisms to orient the diskettes, allow the modules to read and write to the diskette, and perform seek operations.

Diskette positioning
Spindle drive
Head positioning
Head load
Sensors

Figure 8-9 is an exploded view that shows the drive's mechanical detail. Figure 8-10 shows the drive's functional detail.

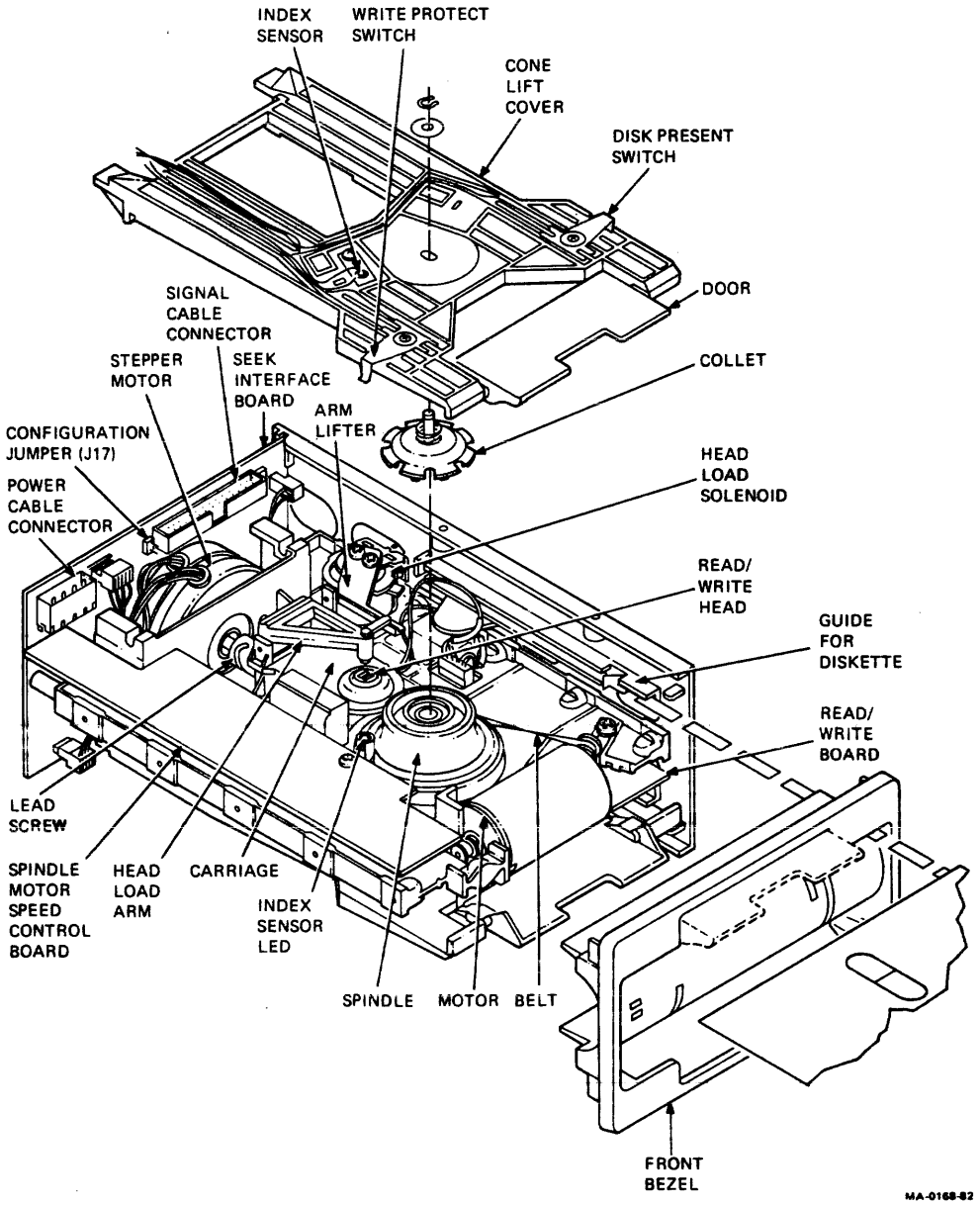


Figure 8-9 Mechanical Detail

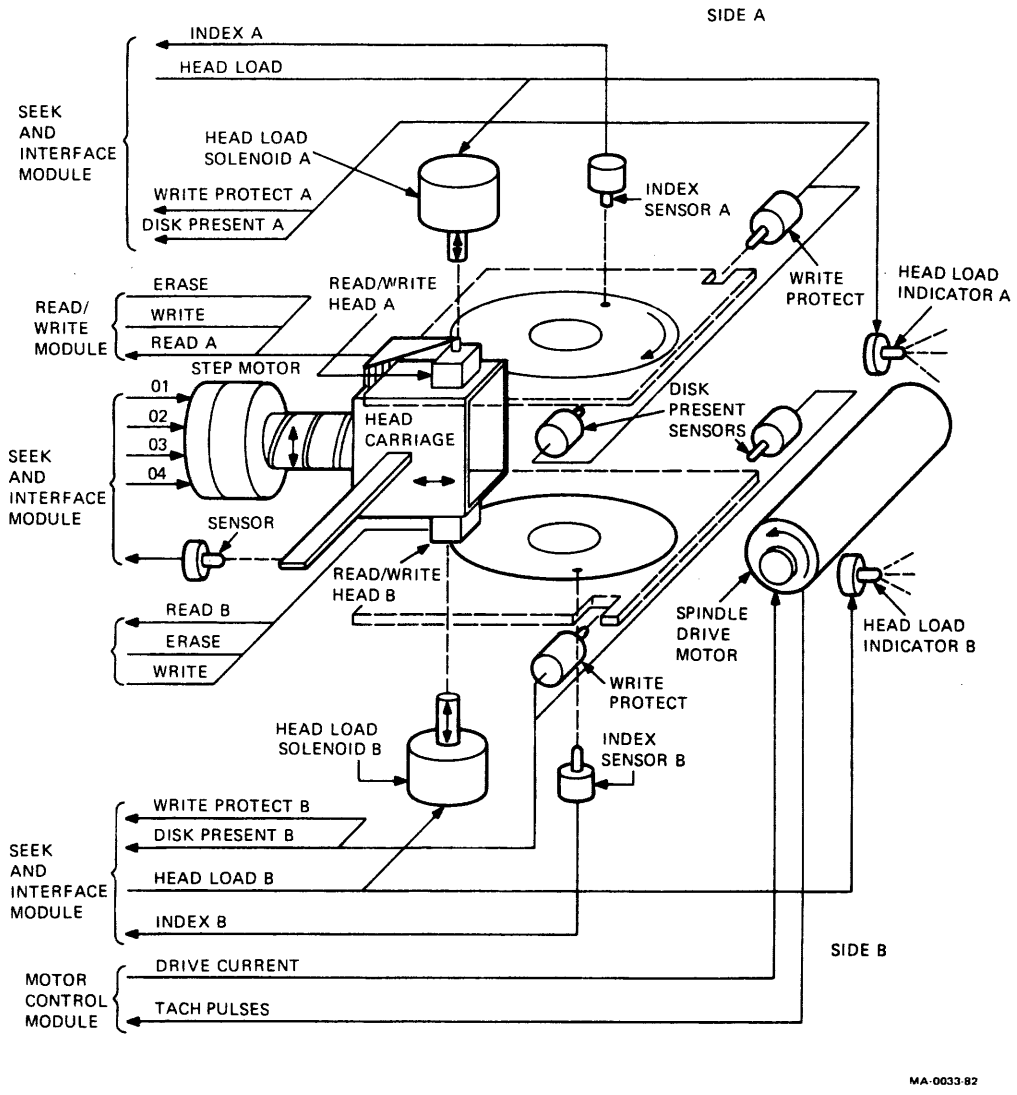


Figure 8-10 Mechanical Operation (Sheet 1 of 2)

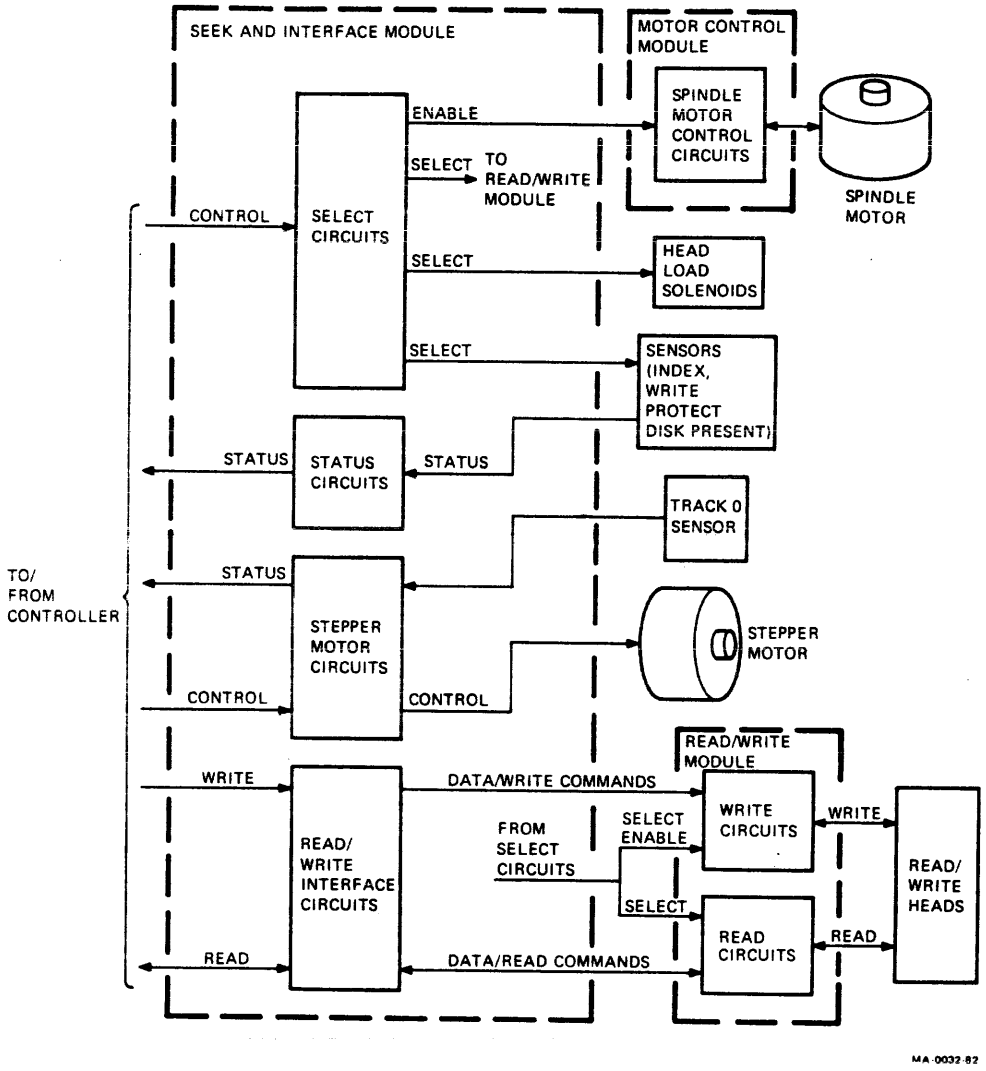


Figure 8-10 Mechanical Operation (Sheet 2 of 2)

8.3.1.1 Diskette Positioning Mechanism – With the front door open (either side A or B), a diskette slides easily in or out of the drive on grooves. These grooves are in the drive's side panels and have a solid backstop to help position the diskette.

Each front door operates a cone lift cover. When the door is closed, the cone lift cover moves over the diskette. A coller on the cone lift cover clamps the media, through the diskette jacket cutout, to the spindle.

The diskette lightly presses against a reference plane near the read/write head. This ensures the correct head to media height. The plane pushes the soft jacket liner against the media. This liner wipes the media surface clean before the media touches the read/write head.

Positioning the diskette in each drive side brings the switches in contact with the diskette. The switches pass status information, disk presence, and write protection to the seek and interface module. See Paragraph 8.3.1.5 for further information.

8.3.1.2 Spindle Drive Mechanism – The RX50 drive contains two counter-rotating spindles, one for each drive side. A single 12 Vdc spindle motor/tachometer combination drives the spindles with a belt. The motor rotates at 1800 rpm and the spindles rotate at 300 rpm.

The motor control module keeps the motor rotating at a constant 1800 rpm. The module compares the tachometer pulses from the motor to a constant reference. This comparison determines the motor's current requirements, which are provided by the motor control module. See Paragraph 8.3.3 for more information about the motor control modules.

8.3.1.3 Head Positioning Mechanism – A stepper motor control circuit on the seek and interface module controls a 4-phase motor. The stepper motor places the read/write heads over the data tracks on the media by rotating a grooved step cam lead screw. This action places a head carriage assembly over the 80 data tracks on the media. The stepper motor rotates in 15 degree increments, which moves the head carriage assembly one data track for each increment.

The grooved step cam lead screw has a flat spot between each track ramp. A ruby ball attached to the head carriage assembly runs in the groove. The flat spots on the lead screw prevent small angular vibrations from transferring to the ruby ball from the screw.

The head carriage assembly moves smoothly along two rods. Its position over the data tracks is determined by the location of the ruby ball in the lead screw. Two heads, which are back to back on the head carriage assembly, can be placed over any one of 80 data tracks on either diskette.

The head carriage assembly also contains a track 0 interrupter bar. This bar is sensed when the head carriage assembly is near track 0, and a signal is sent to the seek and interface module. See Paragraph 8.3.1.5 for more information.

8.3.1.4 Head Load Mechanism – A head load mechanism is a solenoid-actuated arm with a head load pad. When energized, the solenoid releases a head load pad arm to press against the media opposite the read/write head. The pad conforms the media to the contour of the read/write head. This ensures good head to media contact during read or write operations.

When the head load solenoid is de-energized, the head load pad arm is raised away from the media. This reduces wear on the media and the read/write head.

The head automatically unloads if any of the following conditions exist.

Either of the doors is open.
The spindle motor is off.
The drive side is not selected.
No diskette is present in the drive side.

The diskette drive's front bezel contains two head load indicators. Each indicator comes on when its corresponding head is loaded. These indicators warn the operator not to remove the diskette while the controller module is accessing it.

See paragraph 8.3.4 for more information about the control of the head solenoids and indicators.

8.3.1.5 Sensors – The diskette drive contains switch sensors and photo sensitive sensors for passing status information to the seek and interface module. Figure 8-10 shows that there are two sets of sensors for each drive side plus a single track 0 sensor. Each set of sensors provides disk presence, write protection, and index hole location information.

Track 0 Sensor
The track 0 sensor consists of a light emitting diode (LED) and a phototransistor. As the carriage assembly nears track 0, a tab passes between the diode and the phototransistor. This turns off the phototransistor and asserts the track 0 signal (TKOS H) to the seek and interface module. See Paragraph 8.3.7 for more information.

Diskette Present and Write-Protect Switch Sensors
Each drive side has a write-protect switch sensor and a diskette present switch sensor. A switch pair for each side is selected simultaneously. Signal SEL A L selects the switches for drive side A. Signal SEL B L selects the switches for drive side B.

When the door is closed, the switches come in direct contact with an inserted diskette. The switches are normally closed. However, inserting a write-protected diskette in the drive opens both switches. When the switches are open and selected, the DP and WP signals are asserted. These signals provide status signals to the seek and interface module. See Paragraph 8.3.6 for more information.

Index Sensor
Each index sensor consists of a LED and a photo transistor. As the index hole in the diskette passes through a sensor, the light from the diode passes through the hole and strikes the phototransistor. This causes the phototransistor to come on and assert the appropriate index signal, INDEX A L or INDEX B L, to the seek and interface module. See Paragraph 8.3.6 for further information.

8.3.2 Select Circuit Detailed Operation

Figure 8-11 shows the operating detail of the select circuit. The select circuit performs the following functions.

Pass an enable signal to the motor control module.
Generate a circuit enable signal.
Activate the head-load solenoids and their associated indicators.
Generate the sensor select and read/write head select signals.

These functions are performed by the following select circuit elements.

Drive select circuit
Motor enable circuit
Head load circuit

8.3.2.1 Drive Select Circuit – The RX50 drive decodes the four drive select lines, DRIVE SEL 0 L through DRIVE SEL 3 L, depending on the condition of J17 (the configuration jumper). With J17 open (without jumper), the drive select circuit decodes DRIVE SEL 0 L and DRIVE SEL 1. With J17 closed (with jumper), the drive select circuit decodes DRIVE SEL 2 L and DRIVE SEL 3.

The drive select circuit is enabled by a dc voltage status signal, SET H, from the status circuits. When the SET H signal is asserted, the drive select circuits decode the input signals and assert the output select signals.

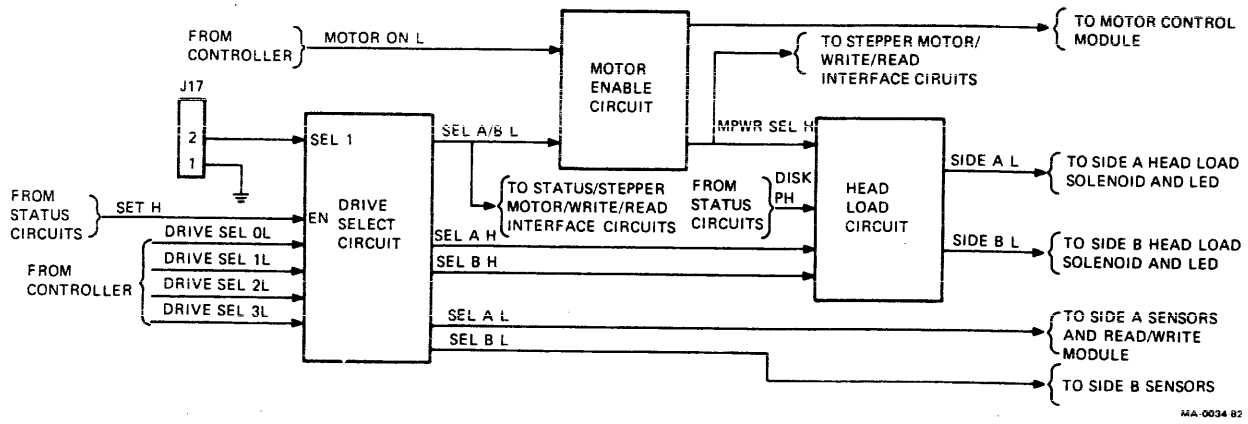
Table 8-1 shows how the asserted DRIVE SEL inputs control the SEL outputs when a jumper is not installed at J17. Table 8-2 shows how the asserted DRIVE SEL inputs control the SEL outputs when a jumper is installed at J17.

Table 8-1 Select Signals Jumper J17 Removed

Drive Select Inputs	Select Outputs A/B L	A L	B L	A H	B H
SEL 0 L	Yes	Yes	No	Yes	No
SEL 1 L	Yes	No	Yes	No	Yes
SEL 2 L	No	No	No	No	No
SEL 3 L	No	No	No	No	No

Table 8-2 Select Signals Jumper J17 Installed

Drive Select Inputs	Select Outputs A/B L	A L	B L	A H	B H
SEL 0 L	No	No	No	No	No
SEL 1 L	No	No	No	No	No
SEL 2 L	Yes	Yes	No	Yes	No
SEL 3 L	Yes	No	Yes	No	Yes



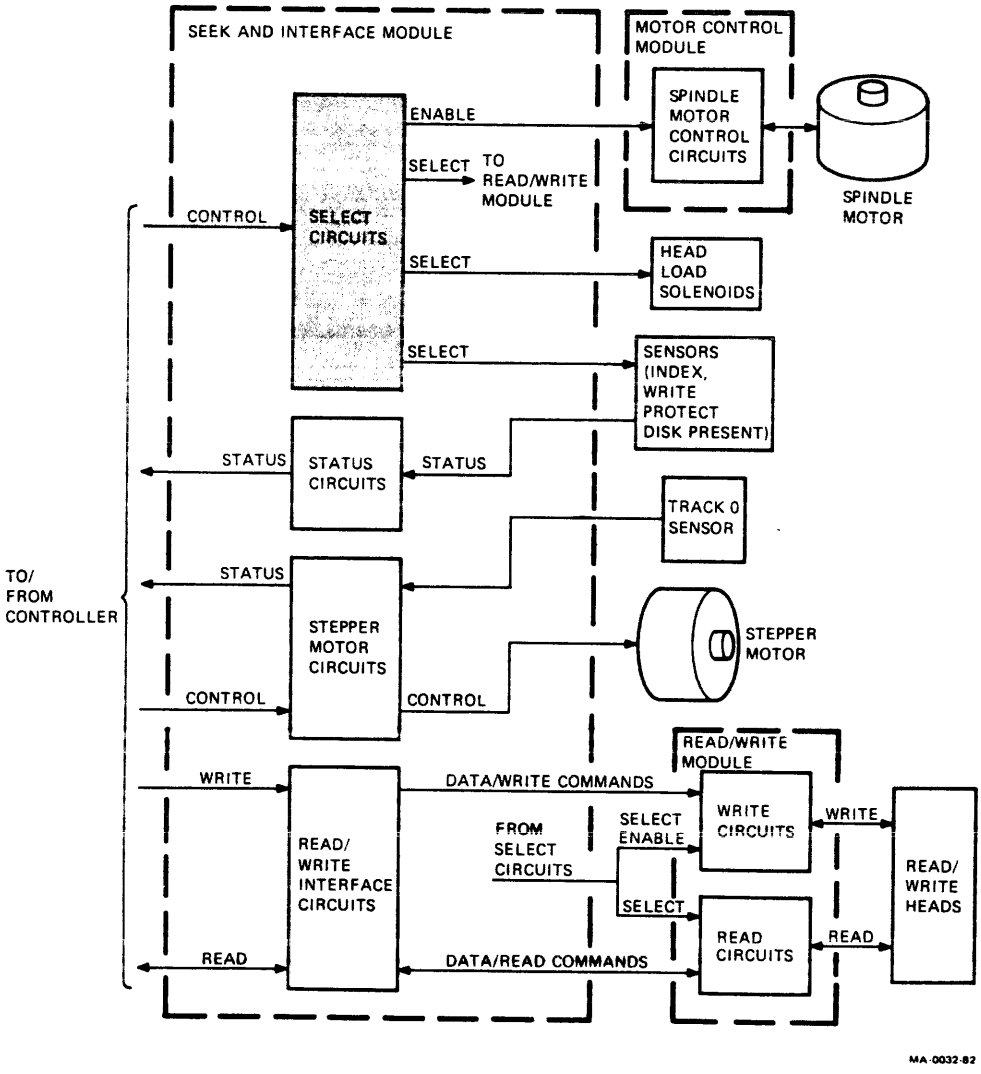


Figure 8-11 Select Circuit

8.3.2.2 Motor Enable Circuit – The motor enable circuit performs the following functions.

- Asserts a spindle motor control circuit enable signal, MPWR H, when the controller module asserts MOTOR ON L.

- Asserts a circuit enable signal, MPWR SEL H, when the diskette drive is selected (SEL A/B L asserted) and the spindle motor control circuit is enabled (MPWR H asserted).

When the diskette drive is selected and the motor is enabled, the head load circuits, stepper motor circuits, and the read/write interface circuits are enabled.

8.3.2.3 Head Load Circuit – The head load circuits assert one of two select signals, SIDE A L or SIDE B L. Each of these signals activates a head load solenoid and a head load indicator.

An asserted SEL A H or SEL B H signal asserts the corresponding side signal when the following conditions exist.

- A diskette is present in the selected side and the door is closed (DISK P H asserted).
- The drive is selected and the spindle motor is turned on (MPWR SEL H asserted).

8.3.3 Motor Control Circuit

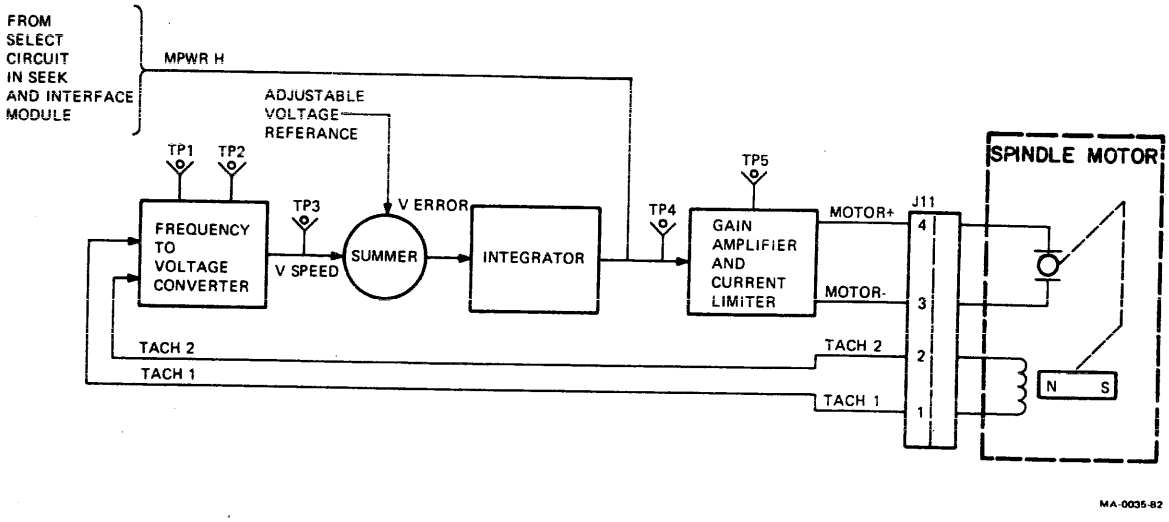
Figure 8-12 shows the operating detail of the spindle motor control circuits. These circuits receive dc power and an enable signal, MPWR H, from the seek and interface module.

When enabled, these circuits supply spindle motor drive current to the spindle motor. They also monitor the motor speed and regulate the motor current. This maintains the spindle motor's constant angular speed.

To perform these functions, this circuit consists of the following elements.

Frequency to voltage converter
Summer
Integrator
Gain amplifier and current limiter

Paragraphs 8.3.3.1 through 8.3.3.4 describe the motor control circuit elements.



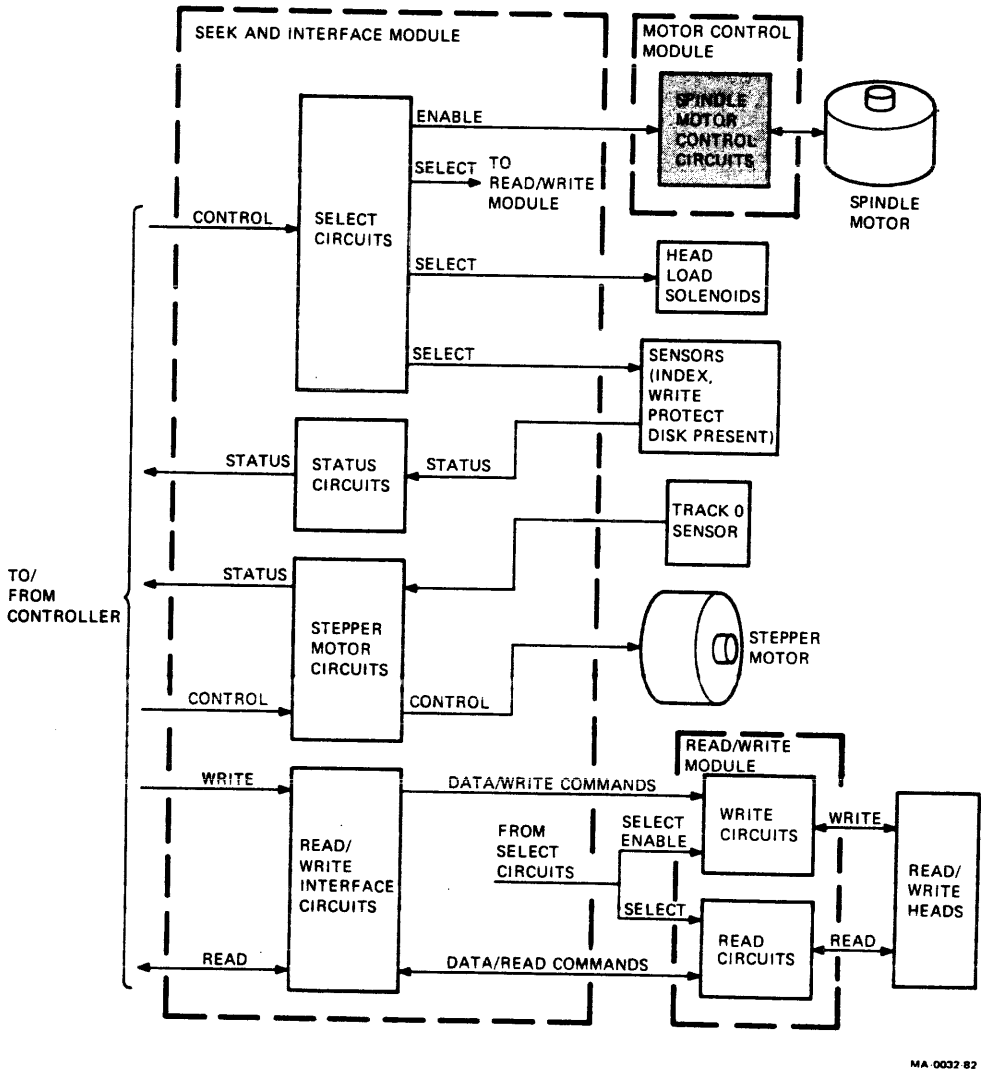


Figure 8-12 Motor Control Circuit

8.3.3.1 Frequency to Voltage Converter – The spindle motor contains a tachometer. When the motor is working, the tachometer returns sinusoidial signals, TACK 1 and TACK 2, to the frequency to voltage converter. These signals represent the motors angular rotation.

The tachometer signal is converted to a voltage. This voltage, VSPEED, represents the motors speed as follows.

1. Each zero voltage crossing of the tachometer signal converts to alternating pulses. These pulses are observable at test point TP1 (Figure 8-13).

2. The leading edge of each pulse generates a transition from 0 V to 5 V or 5 V to 0 V. These transitions, which appear as a rectangular wave, are observable at TP2 (Figure 8-13).

3. The low transitions are averaged with the high transitions. This forms a saw-tooth wave that rides at an average voltage level. This signal, the speed voltage, is observable at test point TP3 (Figure 8-13).

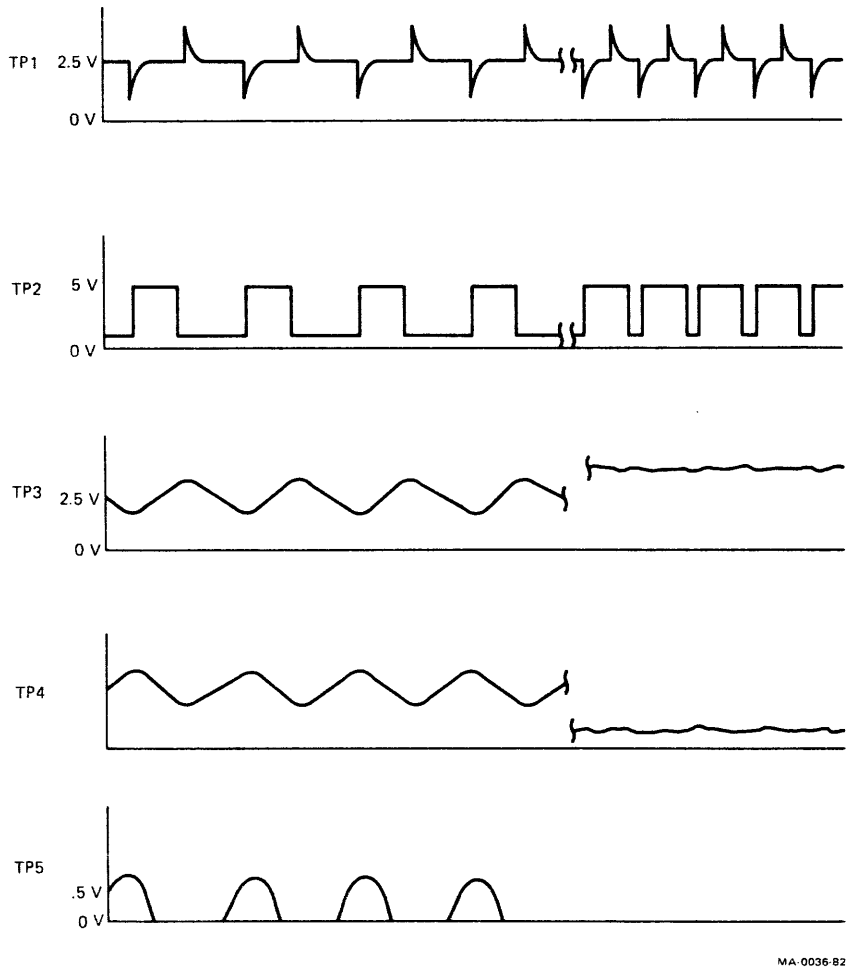


Figure 8-13 Motor Control Wave Forms

8.3.3.2 Summer – The summer adds a constant reference voltage to the speed voltage signal (VSPEED). This addition adjusts the average voltage level of the VSPEED signal to the linear range of the integrator and gain amplifier. The reference voltage is adjusted when the RX50 drive is built and is not field adjustable.

The summer output equals the speed error, VERROR, for the integrator.

8.3.3.3 Integrator – The integrator inverts the saw-tooth wave of the VERROR signal. This converts a decreasing average voltage to an increasing average voltage and vice versa. This inversion is needed because the sensed speed error voltage drops as the speed decreases. However, the motor needs more power to increase its speed and vice versa.

The integrator output is observable at test point TP4 (Figure 8-13). An asserted spindle motor control circuit enable signal, MPWR H, allows the integrator output to pass to the gain amplifier and current limiter. When MPWR H is deasserted, the gain amplifier and current limiter is disabled.

8.3.3.4 Gain Amplifier and Current Limiter – The gain amplifier couples power to the spindle motor. The current limiter limits the amount of power coupled to the motor. This protects the motor during circuit or hardware faults, and when the circuit is first enabled.

The gain amplifier works in its linear range except when the spindle motor control circuit is first enabled. When initially enabled, the gain amplifier is forced into saturation. This occurs because the motor's sensed speed causes the integrator to generate the maximum driving signal.

As the motor approches its required speed, the integrator generates a saw-tooth wave (see Paragraph 8.3.3.3). This signal operates the gain amplifier in its linear range.

The high peaks of saw-tooth wave turn the gain amplifier on and off, forming current pulses for the motor. These pulses are observable at test point TP5 as voltage pulses (Figure 8-13).

8.3.4 Head Load Solenoids and Indicators

Figure 8-14 shows the electrical connections to the head load solenoids and indicators that are controlled by the select circuits. The diskette drive has two solenoids and two indicators, one set for each drive side. The select logic activates one set at a time when the following conditions exist.

The spindle motor is operating.
A diskette is correctly inserted and the door is closed.
The drive side is selected.

8.3.5 Status Circuit

Figure 8-15 shows the detailed operation of the status circuits. Figure 8-16 shows the timing relationships between the circuit signals. These circuits perform the following functions.

Pass status signals from the diskette drive to the controller module.
Monitor the dc power for fluctuations.

These functions are performed by the following status circuit elements.

Write protect status circuit
Diskette present status circuit
Output drivers
+5 V monitor

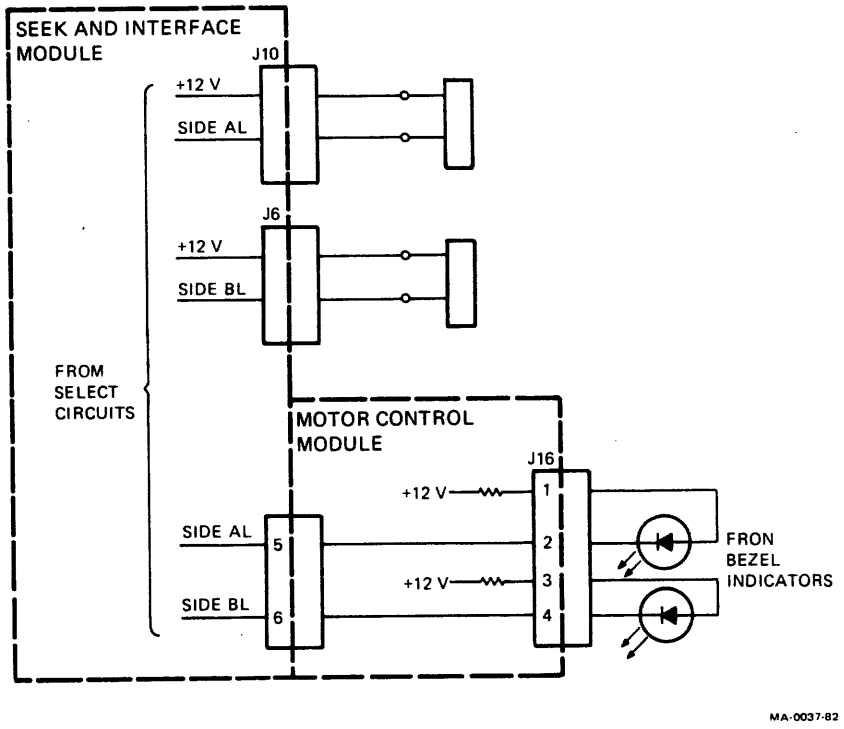


Figure 8-14 Connections to Head Load Solenoids and Indicators (Sheet 1 of 2)

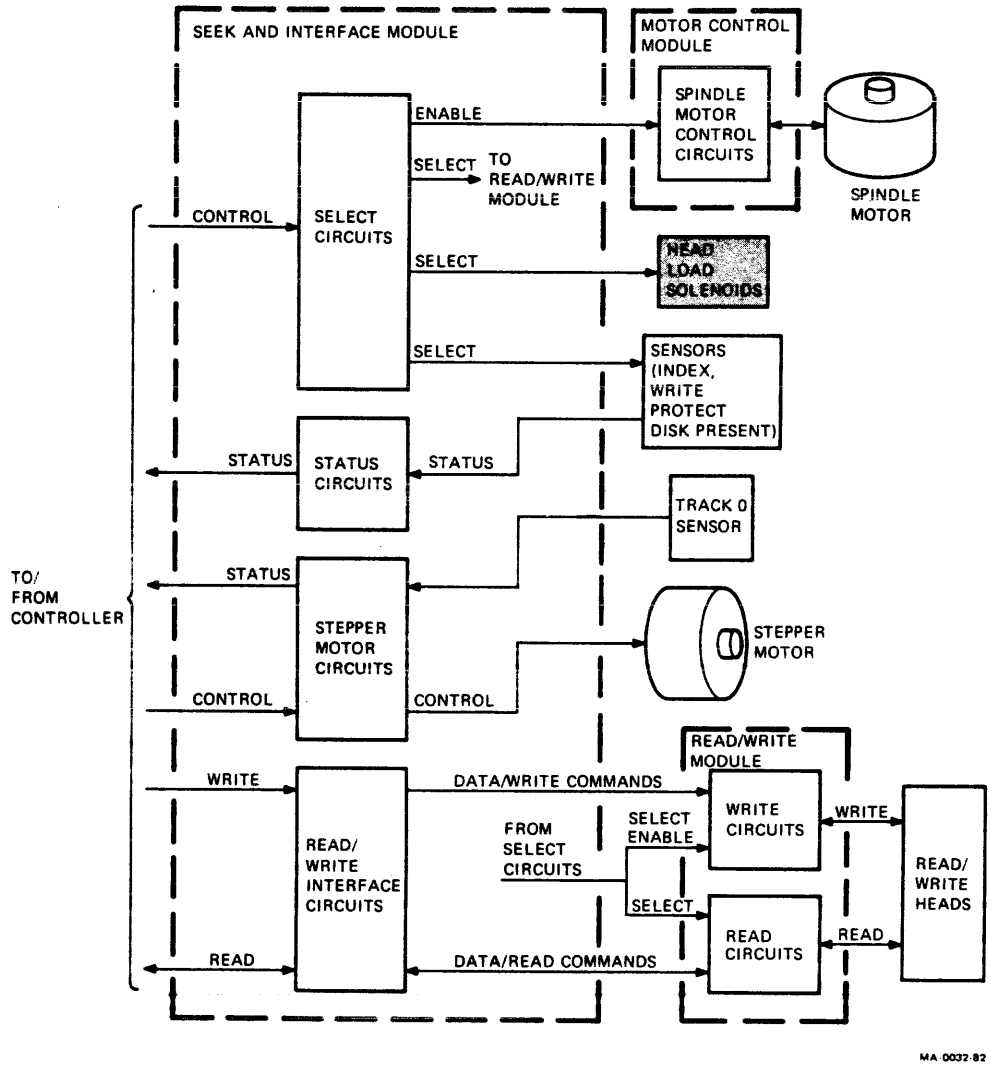


Figure 8-14 Connections to Head Load Solenoids and Indicators (Sheet 2 of 2)

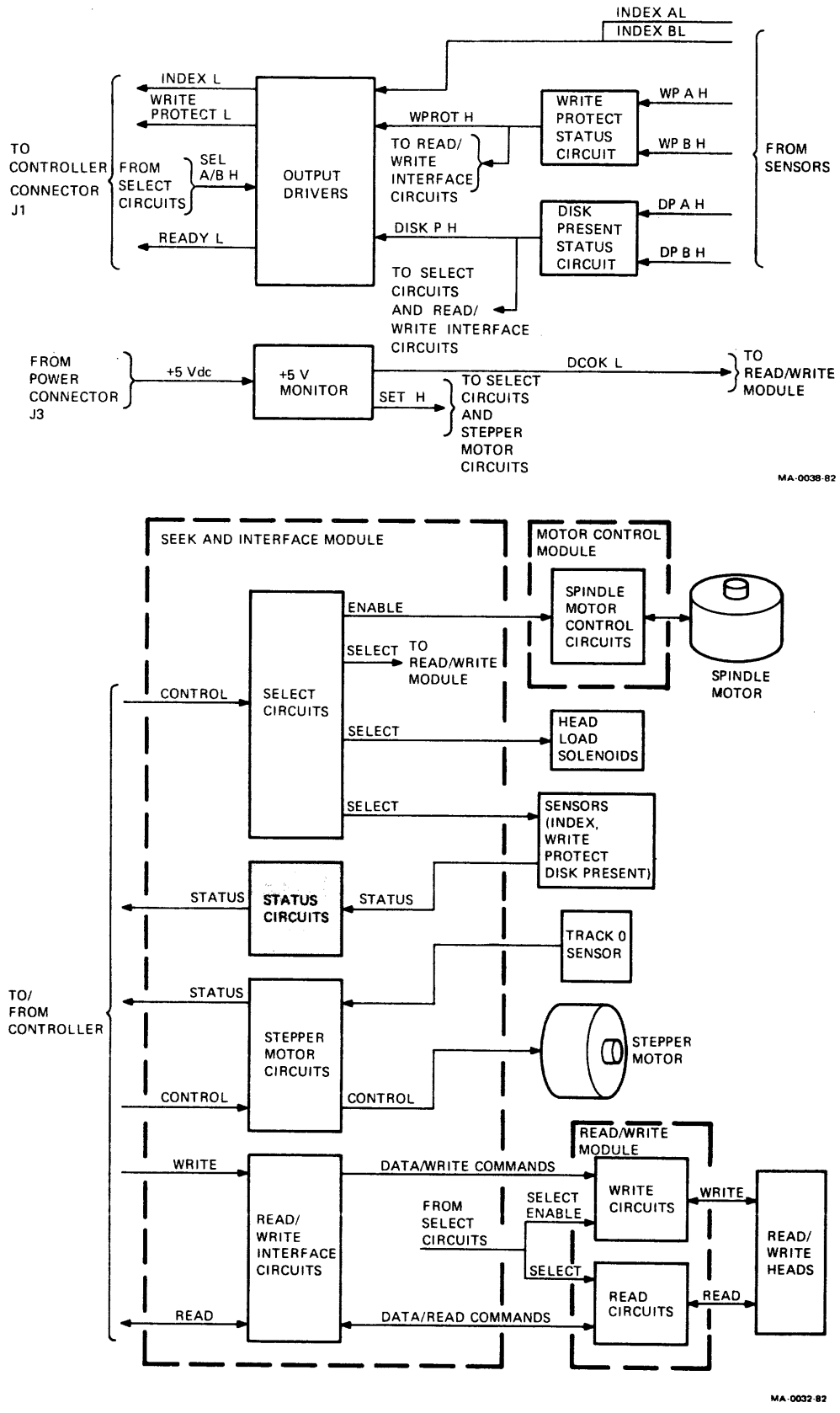


Figure 8-15 Status Circuit

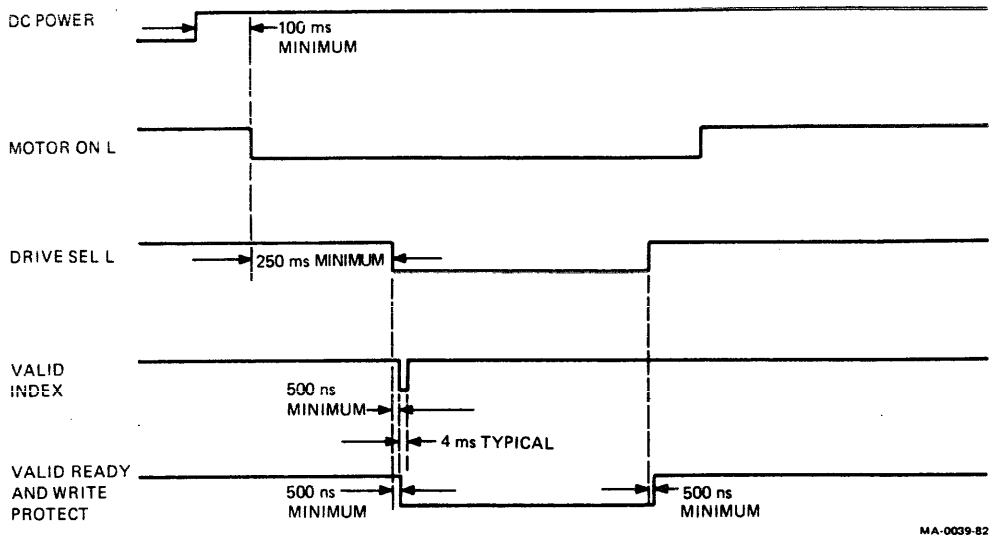


Figure 8-16 Status Circuit Timing Relationships

8.3.5.1 Write Protect Status Circuit – This circuit monitors the write protect status signals, WP A H and WP B H, from the write protect sensors (see Paragraph 8.3.6.2). If either signal is asserted, this circuit asserts the write protect signal, WPROT H, for the output drivers and the read/write interface circuits.

8.3.5.2 Diskette Present Status Circuits – This circuit monitors the diskette present status signals, DP A H and DP B H, from the diskette present sensors (see Paragraph 8.3.6.2). If either signal is asserted, this circuit asserts the diskette present signal, DISK P H, for the output drivers, select circuits, and the read/write interface circuits.

8.3.5.3 Output Driver – These drivers pass the status signals from the RX50 drive to the controller module. They are enabled by select circuits and when SEL A/B H is asserted. The output drivers pass the signal state of the index (see Paragraph 8.3.6.1), write protect, and diskette present signals as INDEX L, WRITE PROTECT L, and READY.

8.3.5.4 +5 V Monitor – This monitor generates enable and reset signals for the RX50 drive. It continually monitors the state of the drive's +5 V power. If the voltage goes out of tolerance, the monitor deasserts DCOK L and SET H.

The DCOK L signal enables the write circuits when they are selected. The SET H signal enables the select and stepper motor circuits.

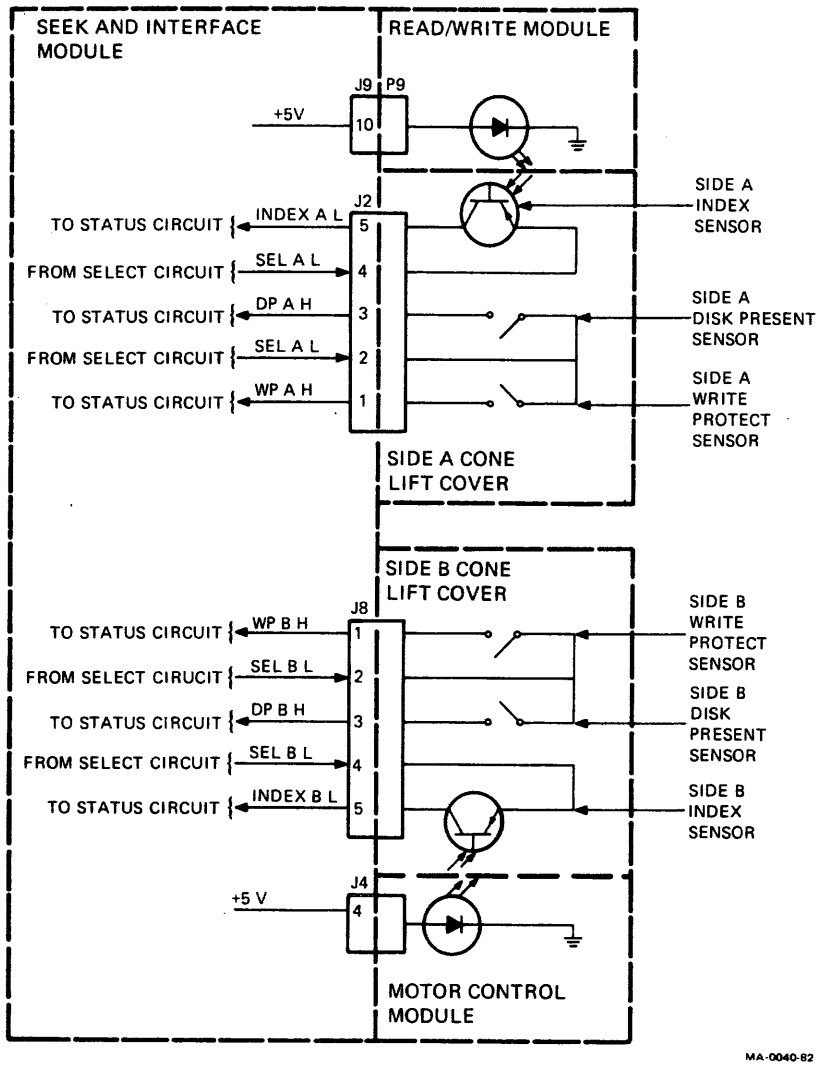


Figure 8-17 Sensor (Sheet 1 of 2)

8.3.6 Status Sensors

Figure 8-17 shows the detailed operation of the status sensors. These sensors are a series of LEDs with photo-sensitive transistors and switches. These sensors perform the following functions.

- Sense the location of the index hole in the media for the status circuits
- Sense the presence of the diskette for the status circuits
- Sense the write-protect status of the diskette for the status circuits

8.3.6.1 Index Sensor – The RX50 drive has two index sensors, one sensor for each drive side. Each index sensor consists of an LED and a photo-sensitive transistor. A select signal from the select circuits enables the photo-sensitive transistor. When the select signal is deasserted, the sensor is disabled.

When a sensor is enabled, it controls a status signal, INDEX A L or INDEX B L, for the status circuits. The signal is asserted when the index hole in the diskette passes through the selected sensor. The light from the LED then strikes the photo-sensitive transistor, turns it on, and asserts the index signal.

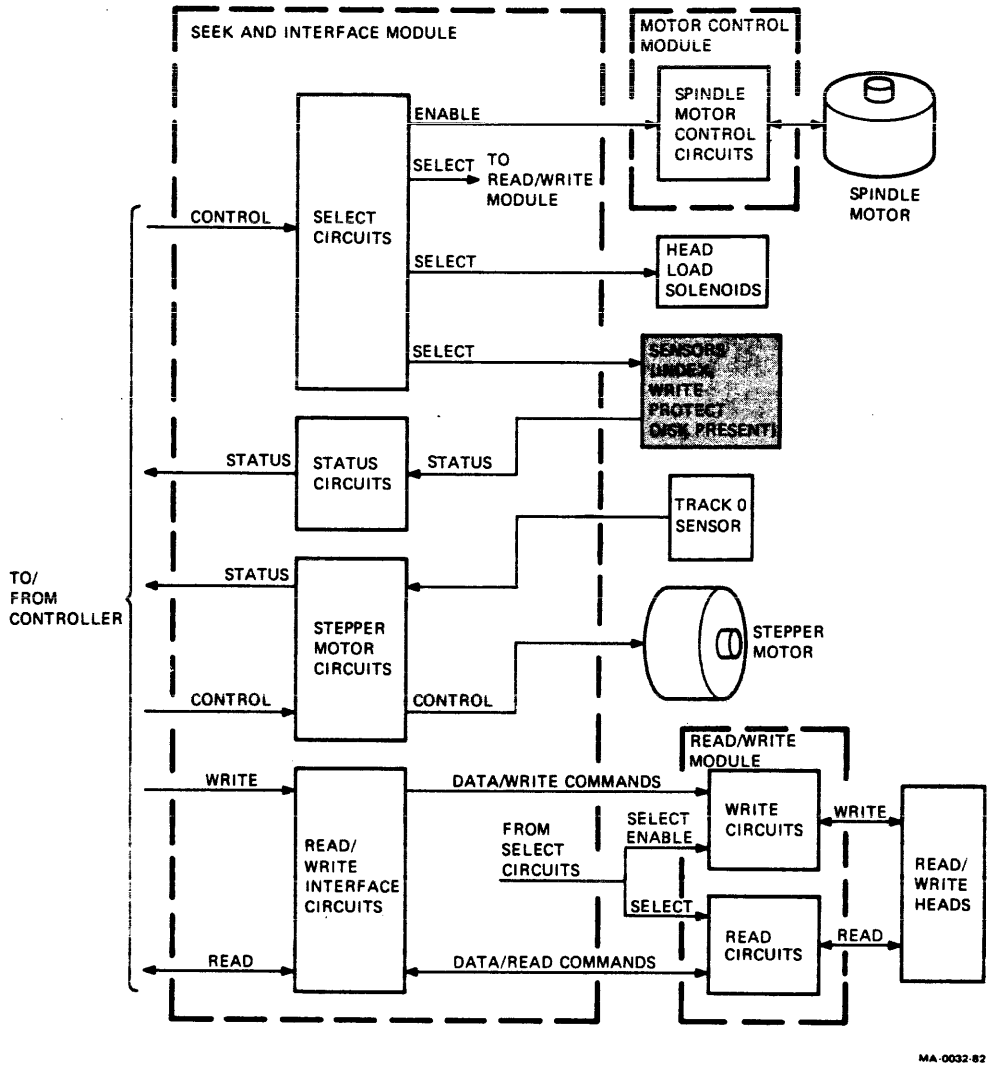


Figure 8-17 Sensor (Sheet 2 of 2)

8.3.6.2 Diskette Present and Write Protect Sensor – The RX50 drive has two sets of diskette present and write-protect sensors, one set for each drive side. Each sensor provides a status signal to the status circuits. The sensors are switches selected by the select circuits.

Each drive side has a write-protect switch and a diskette present switch. The switches for each side are selected as pairs. Signal SEL A L selects the switches for drive side A. Signal SEL B L selects the switches for drive side B.

When the door is closed, the switches come in direct contact with a diskette inserted in the drive side. The switches are normally closed. Inserting a write-protected diskette in the drive opens both switches. When the switches are open and selected, the diskette present and write-protect signals are asserted.

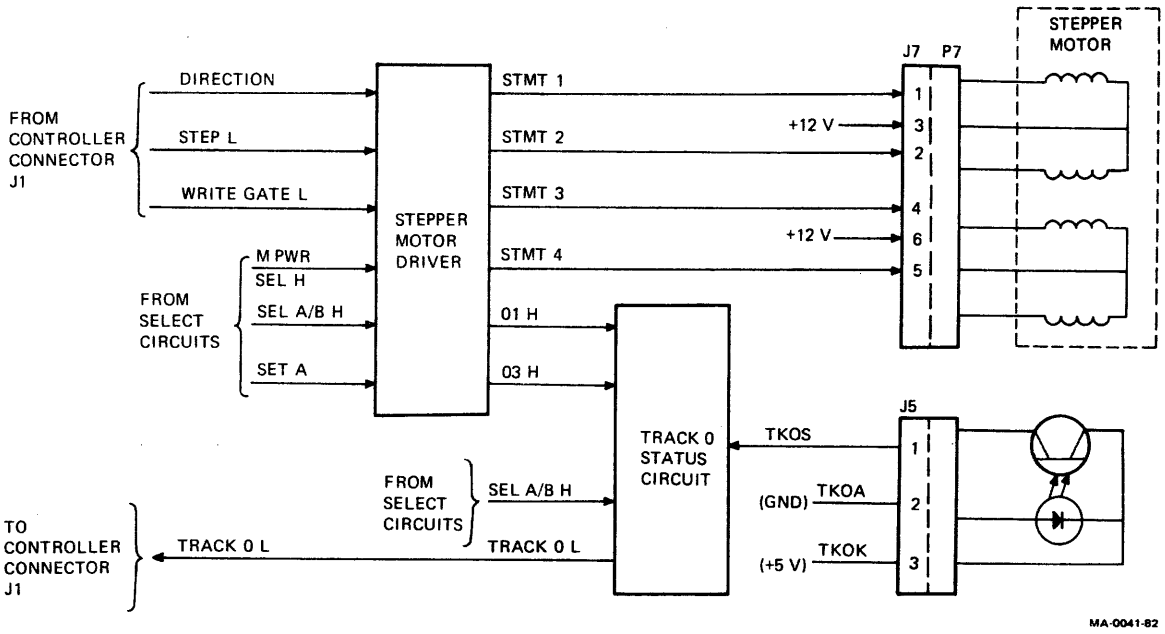


Figure 8-18 Stepper Motor Circuit (Sheet 1 of 2)

8.3.7 Stepper Motor Circuits

Figure 8-18 shows the detailed operation of the stepper motor circuits. Figure 8-19 shows the timing relationships between the circuit signals. These circuits perform the following functions.

Generate control signals that actuate the stepper motor
Pass a track 0 status signal to the controller module

These functions are performed by the following stepper motor circuit elements.

Stepper motor driver
Track 0 sensor
Track 0 status circuit

8.3.7.1 Stepper Motor Driver – The stepper motor driver decodes control signals from the controller moudle and generates phase control signals for the stepper motor coils. This driver also passes phase control signals to the track 0 status circuit. These signals indicate a possible track 0 head position.

The select and status circuits and the controller module enable the stepper motor driver. The driver needs asserted MPWR SEL H, SEL A/B H, and SET H signals, while WRITE GATE L is deasserted. These signal states indicate that the following conditions exist for the stepper motor driver operation.

The spindle motor is operating.
The drive is selected.
The +5 V power level is in tolerance.
The RX50 drive is not enabled for write operations.

The step motor controller generates four phase control signals for the operation of the step motor: STMT1, STMT2, STMT3, STMT4. These driver outputs are decoded from two controller signals, DIRECTION and STEP L. Figure 8-19 shows the timing relationships between the controller inputs and the driver outputs.

The DIRECTION signal indicates the direction in which the stepper motor rotates. The STEP L signal indicates the number of steps the motor moves.

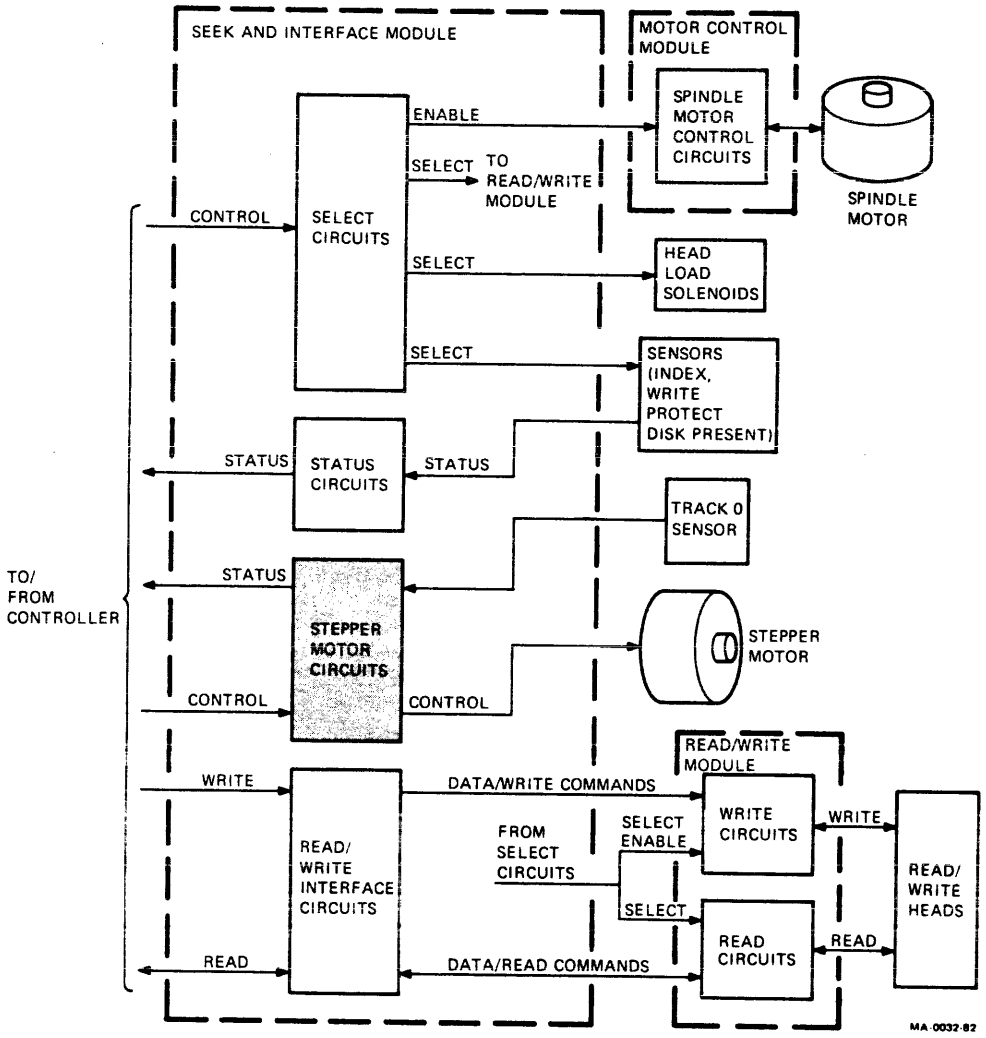


Figure 8-18 Stepper Motor Circuit (Sheet 2 of 2)

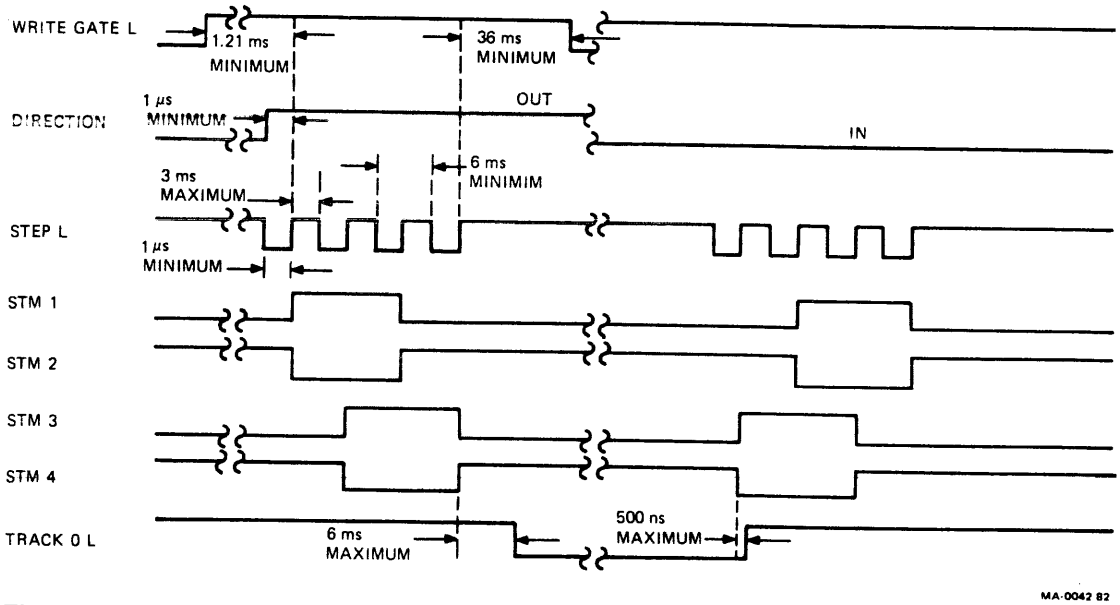


Figure 8-19 Stepper Motor Timing Relationships

8.3.7.2 Track 0 Sensor – The RX50 drive contains one track 0 sensor. This sensor consists of an LED and a photo-sensitive transistor, and is always enabled. When the heads are over track 0, 1, or 2, this sensor asserts a track 0 sense signal, TK0S, for the stepper motor circuits.

The TK0S signal is asserted when a tab on the carriage assembly passes through the sensor. The tab stops light from the LED from striking the photo-sensitive transistor. This turns off the transistor and asserts TK0S.

8.3.7.3 Track 0 Status Circuit – The track 0 status circuit monitors for a track 0 read/write head location. When the RX50 drive is selected, this circuit is enabled by the select circuits. When enabled, this circuit returns a track 0 status signal, TRACK 0 L, to the controller module.

The track 0 status circuit asserts the TRACK 0 L signal when the following conditions exist.

- The heads are over track 0, 1, or 2 (TK0S H asserted).
- The stepper motor driver asserts the zero phase signals to the motor (01 H and 03 H signals asserted).

8.3.8 Read/Write Interface Circuit

Figure 8-20 shows the read/write interface circuit operating detail. Figures 8-21 and 8-22 show the timing relationships between the circuit signals and valid data. These circuits perform the following functions.

- Pass write data from the controller module to the read/write module
- Pass write control signals from the controller module to the read/write module
- Generate an erase control signal for the read/write module
- Pass read data from the read/write module to the controller module.

These functions are performed by the following read/write interface circuit elements.

Write driver circuit
Erase gate timer
Output driver

8.3.8.1 Write Driver Circuit – When enabled, the write driver circuit passes write data and commands to the erase gate and read/write module. This circuit is enabled by the controller module, select circuits, and status circuits (Figure 8-20). The write driver circuit is enabled when the following conditions exist.

- The controller module selects a write function by asserting WRITE GATE L.
- The spindle motor is enabled and the RX50 drive is selected (MPWR SEL H asserted).
- A diskette is present in the selected side and the door is closed (DISK P H asserted).
- The diskette is not write protected (WPROT H asserted).

When enabled, the write driver circuits divide write data from the controller by two. The write driver circuits then pass the data on differential lines to the read/write module. This converts the write data pulses to leading edge triggered differential data. See Paragraph 8.3.9.4 for more information about the write data.

The driver also passes two control signals from the controller module to the read/write module, the WRITE GATE L signal as WRITE GATE and the TKG43 signal as WRITE CURRENT SWITCH. The WRITE GATE signal enables the write circuits in the read/write module. The WRITE CURRENT SWITCH signal controls the level of write current that the write circuits generate.

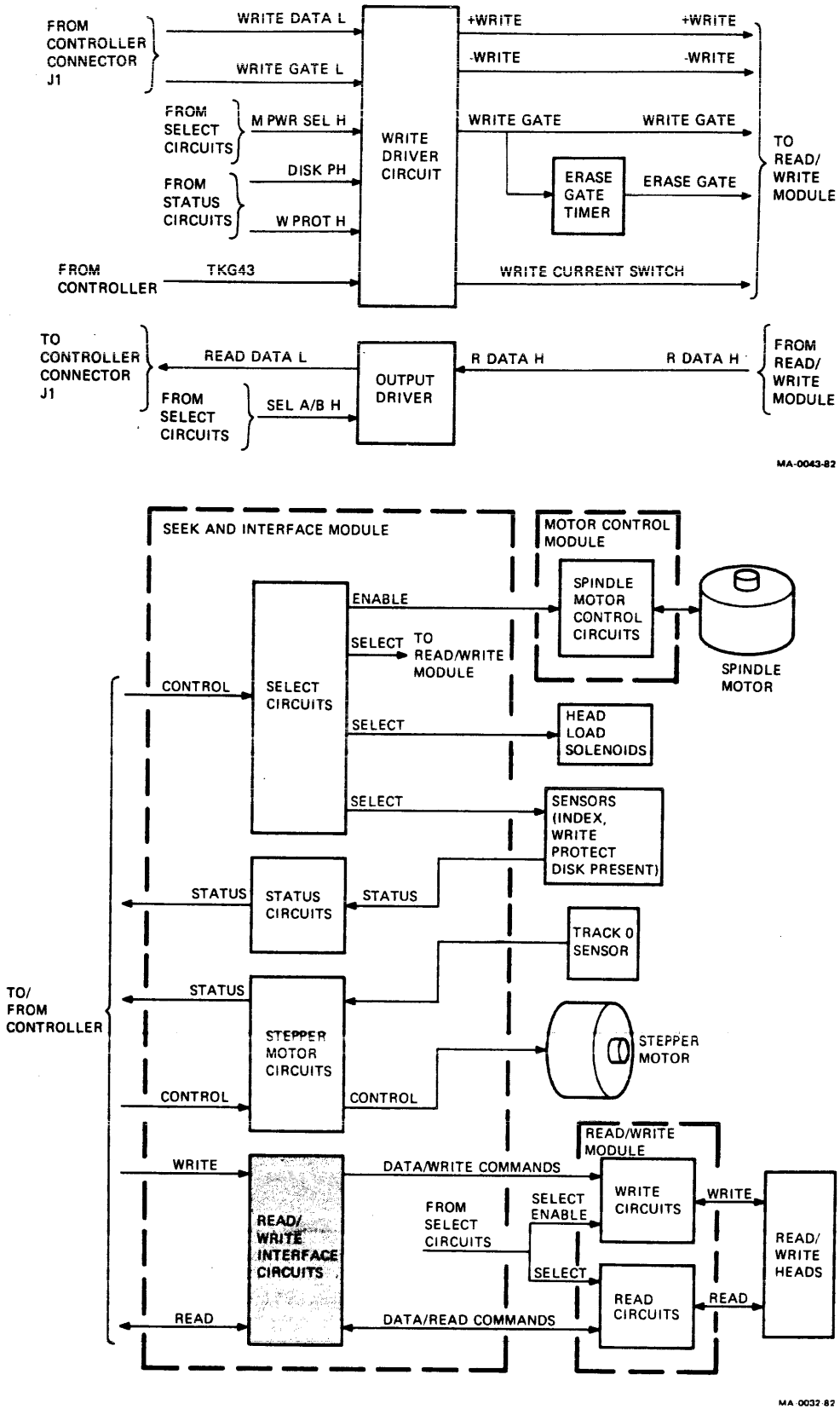


Figure 8-20 Read/Write Interface Circuit

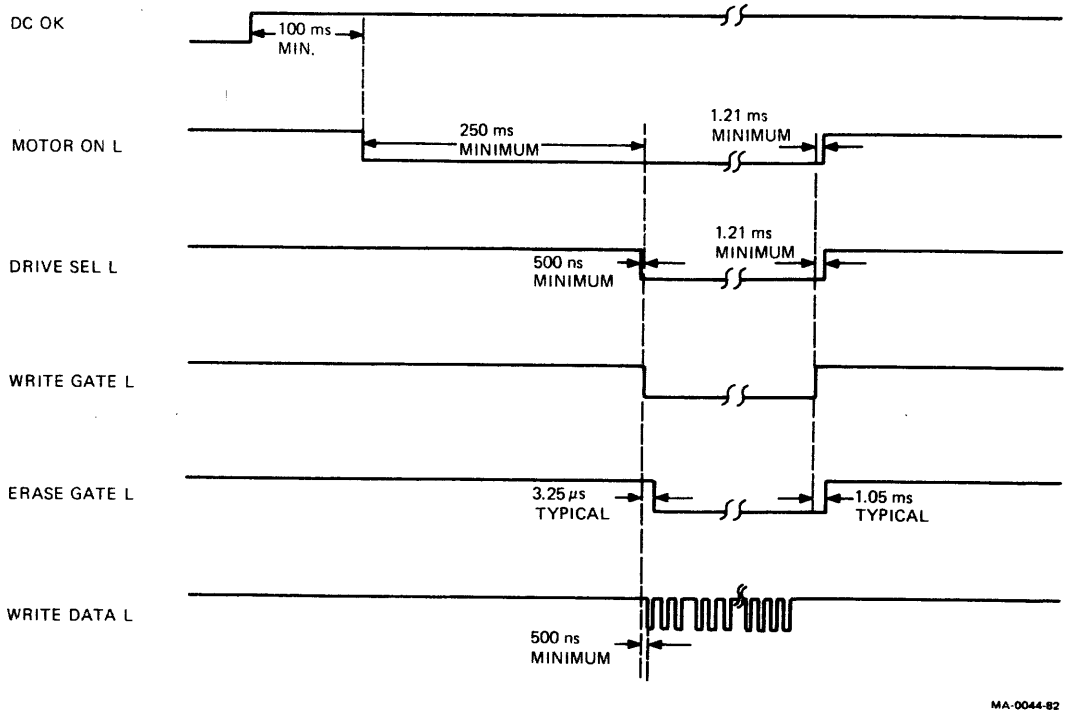


Figure 8-21 Write Data Timing Relationships

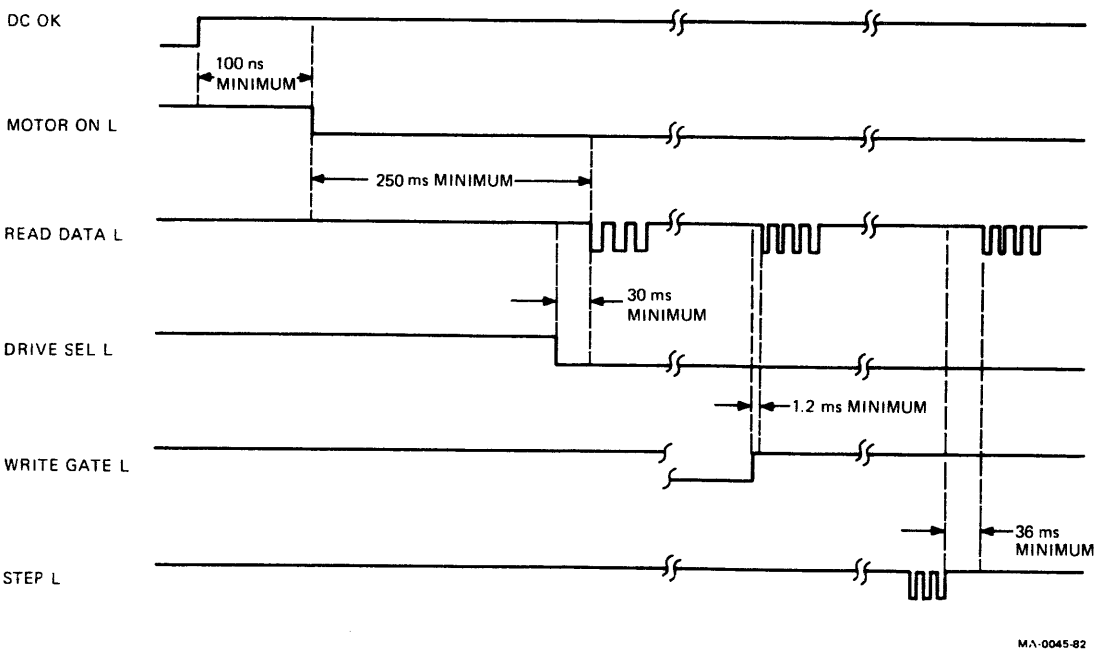


Figure 8-22 Read Data Timing Relationships

8.3.8.2 Erase Gate Timer – The erase gate timer delays the WRITE GATE signal to generate an ERASE GATE signal. This delay is necessary because of the read/write head design (see Paragraph 8.3.11). Figure 8-21 shows the relationship of ERASE GATE and WRITE GATE.

8.3.8.3 Output Driver – The output driver passes read data, R DATA H, from the read/write module to the controller module. Figure 8-22 shows the timing relationships between the circuit signals and the read data.

The output driver is enabled by the select logic when SEL A/B H is asserted. This signal state indicates that the RX50 drive is selected.

8.3.9 Write Circuit

Figure 8-23 shows the write circuit operating detail. These circuits perform the following functions.

- Generate write currents for the heads
- Generate an erase current for the heads
- Generate head select signals
- Protect the heads and previously written data when the dc power is out of tolerance

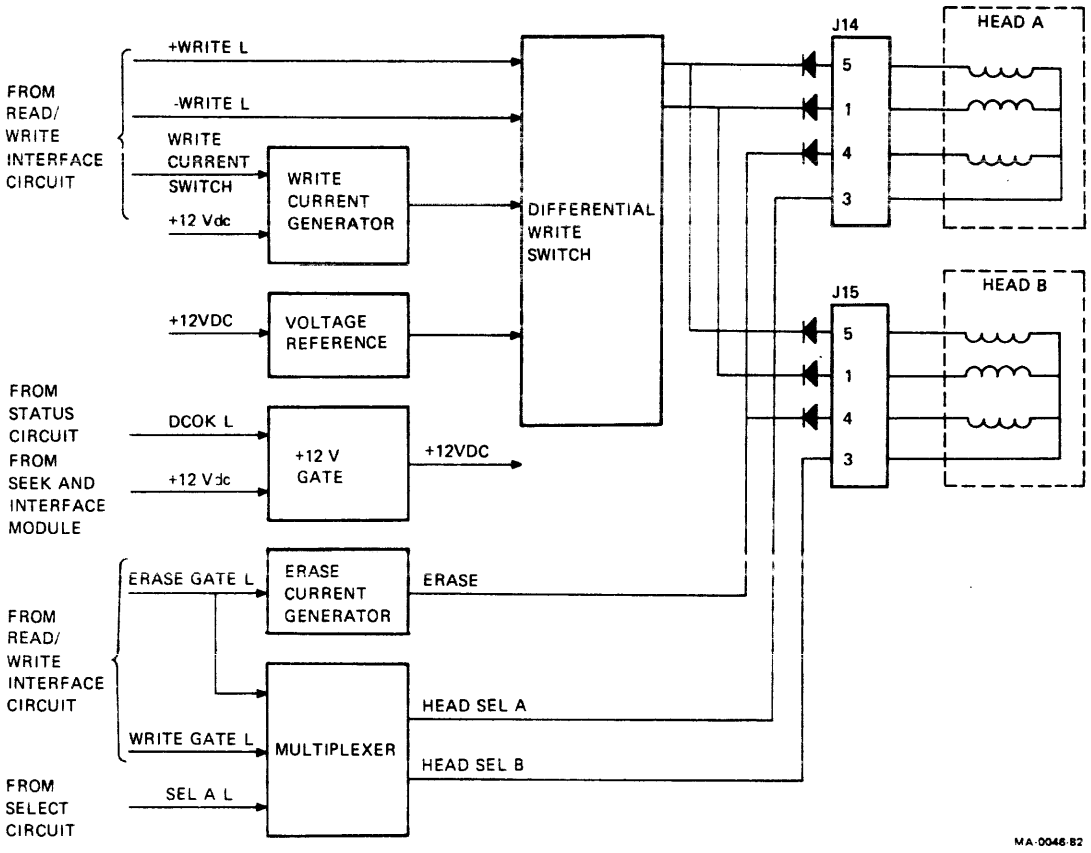


Figure 8-23 Write Circuit (Sheet 1 of 2)

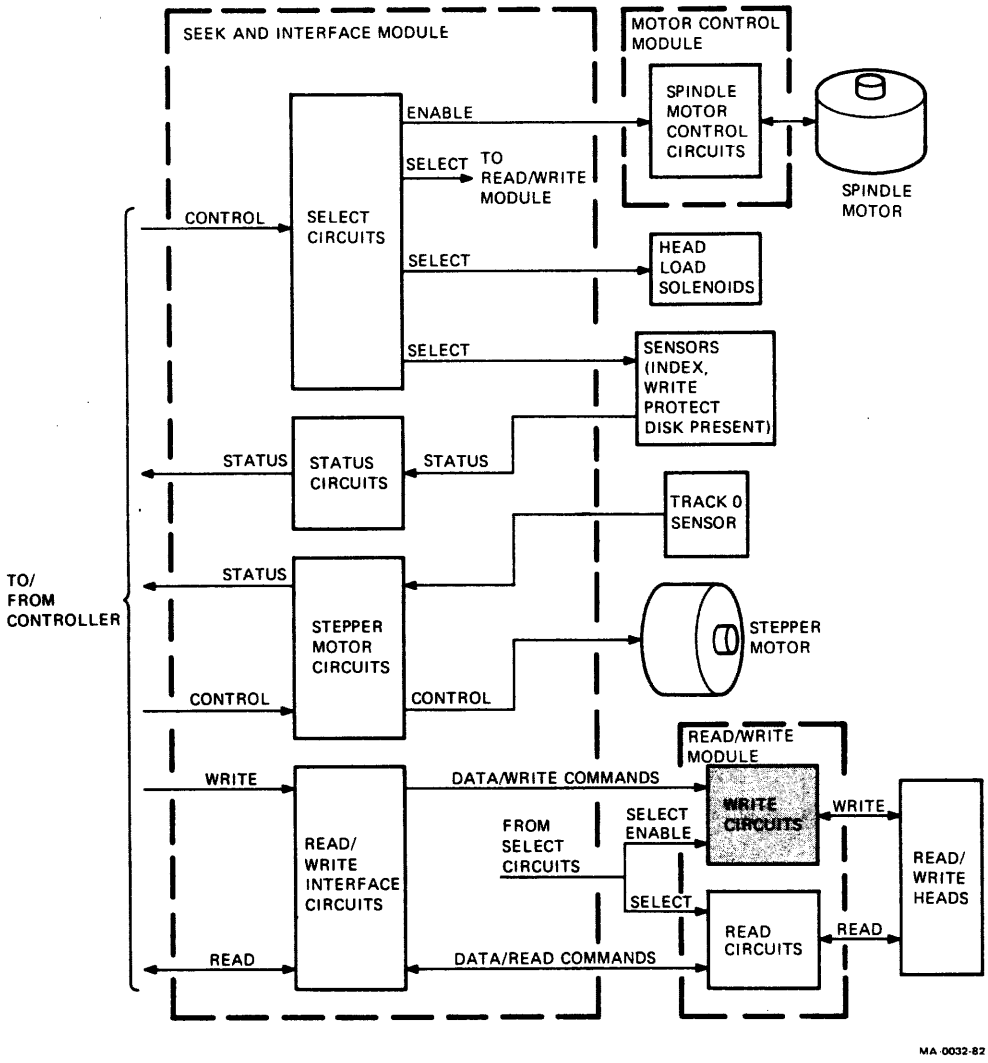


Figure 8-23 Write Circuit (Sheet 2 of 2)

These functions are performed by the following write circuit elements.

Write current generator
Voltage referance
+12 V gate
Differential write switch
Erase current generator
Multiplexer

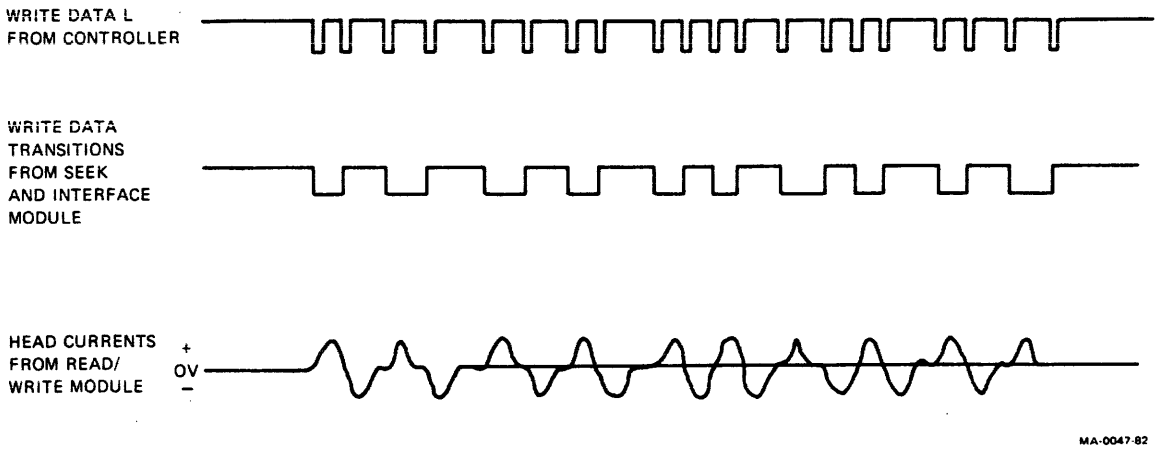


Figure 8-24 Write Data to Head Current Conversion

8.3.9.1 Write Current Generator – The write current generator provides a selectable current for the differential write switch. These currents are derived from the +12 V from the +12 V gate.

When the WRITE CURRENT SWITCH signal is asserted, a low current for the inner tracks (44 through 79) is provided to the differential write switch. When the WRITE CURRENT SWITCH signal is deasserted, a high current for the outer tracks (0 through 43) is provided to the differential write switch.

8.3.9.2 Voltage Reference – The voltage reference provides a stable voltage to the differential write switch. This voltage ensures that the outputs of the differential write switch are balanced.

8.3.9.3 +12 V Gate – The +12 V gate receives the read/write modules supply voltage (+12 Vdc) and a DCOK signal. If DCOK remains asserted, the gate passes +12 Vdc to the modules circuits. This ensures that the write circuits are disabled if a low power condition exists.

8.3.9.4 Differential Write Switch – The differential write switch converts the write data from the read/write interface circuits to write currents for the read/write heads. Figure 8-24 shows the conversion of WRITE DATA from the controller module (Paragraph 8.3.8.1) to write currents for the heads. For this conversion, the differential write switch requires a write current and a reference voltage.

The write currents, +WRITE and –WRITE, generate magnetic fields in the heads, which records data on the media. See Paragraph 8.3.11 for more information about the recording techniques.

8.3.9.5 Erase Gate Generator – The erase gate generator converts the ERASE GATE L signal to an ERASE current for the read/write heads. This current generates a magnetic field in the heads, which tunnel erases recorded data on the media. See Paragraph 8.3.11 For more information about the recording techniques.

8.3.9.6 Multiplexer – The multiplexer decodes three signals (ERASE GATE, WRITE GATE, and SELECT) to generate head select signals for a write function. Table 8-3 shows how the inputs assert the outputs (HEAD SEL A and HEAD SEL B).

8.3.10 Read Circuit

Figure 8-25 shows the detailed operation of the read circuits. These circuits perform the following functions.

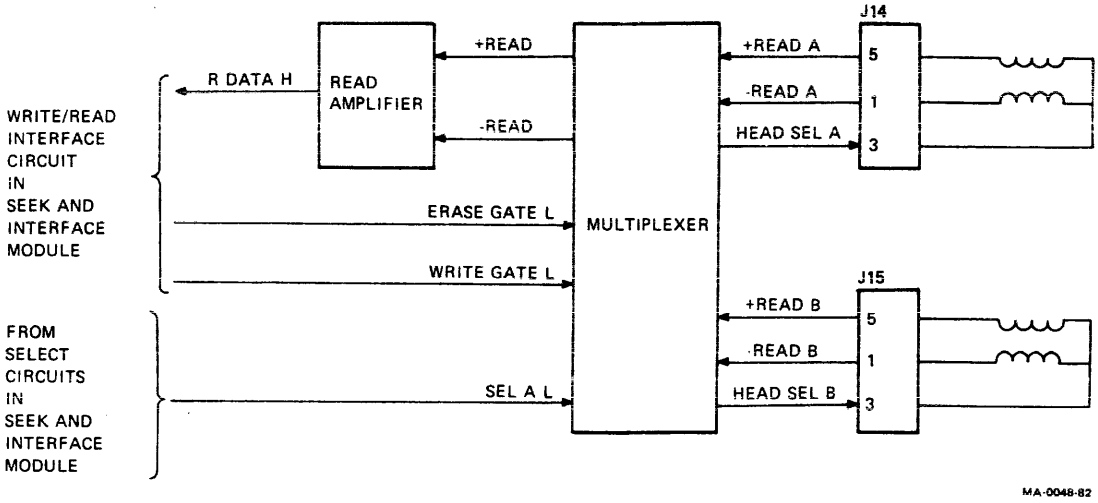
Select a read/write head and read data
Convert the analog read data to digital data

These functions are performed by the following read circuit elements.

Read amplifier
Multiplexer

Table 8-3 Write Function Head Select

Inputs			Outputs	
Erase Gate L	**Write Gate L**	**Select A L**	**Head Select A**	**Head Select B**
NO	No	No	Write not selected	
No	Yes	No	Yes	No
Yes	No	No	Yes	No
Yes	Yes	No	Yes	No
No	No	Yes	Write not selected	
No	Yes	Yes	No	Yes
Yes	No	Yes	No	Yes
Yes	Yes	Yes	No	Yes



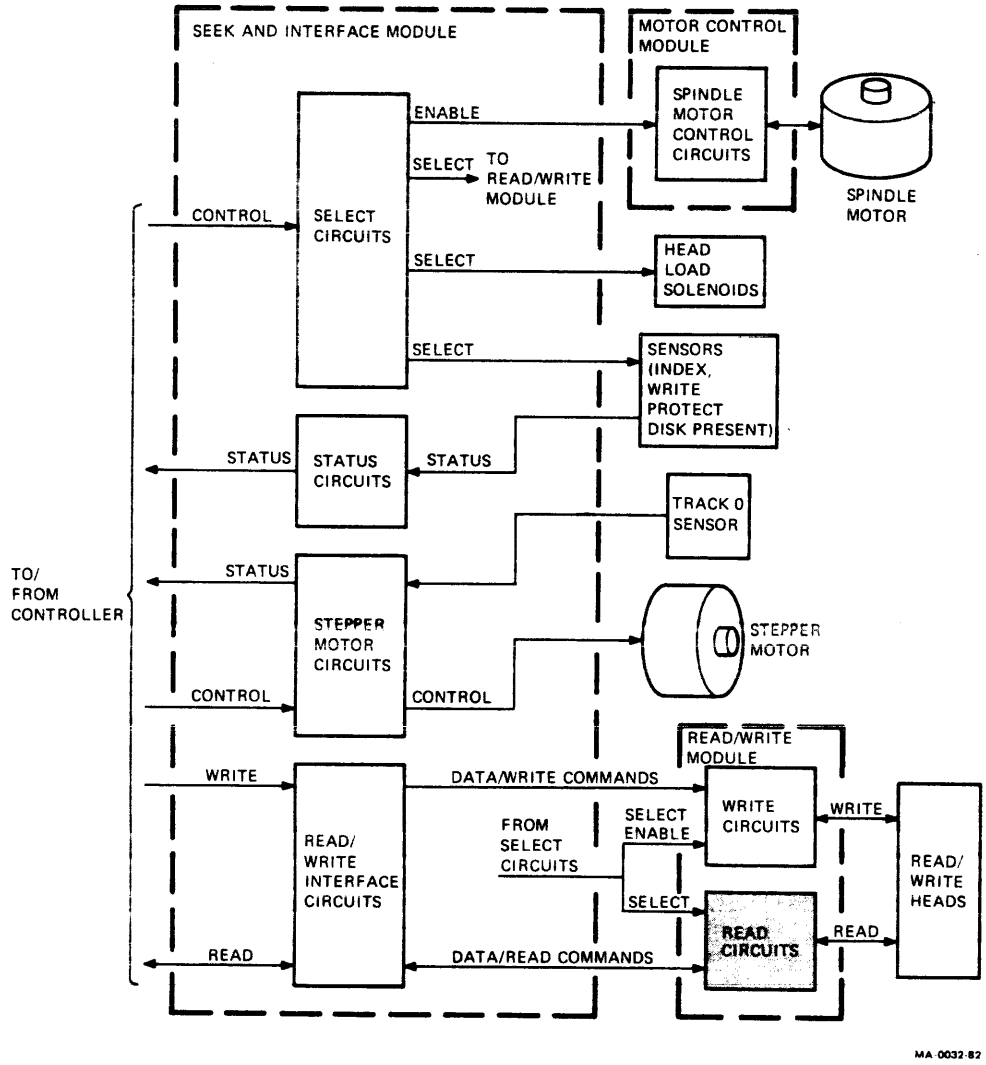


Figure 8-25 Read Circuit

8.3.10.1 Read Amplifier – The read amplifier converts analog read signals, developed in the read/write heads by the media, to digital read data for the read/write interface circuits. Magnetic flux reversals on the media generate the analog signals. These flux reversals represent previously recorded data and clocks. Figure 8-26 shows the possible frequency combinations and the conversion results.

8.3.10.2 Multiplexer – The multiplexer decodes three signals (ERASE GATE, WRITE GATE, and SELECT) to generate head select signals and select read data for the read amplifier. The write circuits use the same multiplexer, but the ERASE GATE L and WRITE GATE L signals are deasserted for a read function.

Table 8-4 shows how the seek and interface module inputs select read data and head select signals.

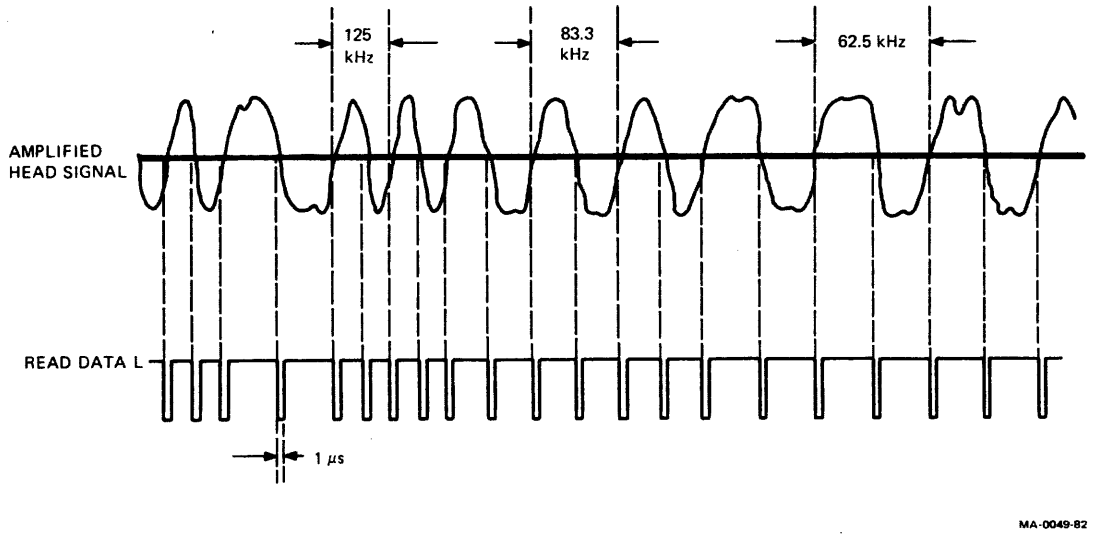


Figure 8-26 Head Signal to Read Data Conversion

Table 8-4 Read Function Head Select

Erase Gate L	Write Gate L	Select A L	Head Select A	Head Select B	Head Data
No	No	Yes	Yes	No	A
No	Yes	Yes	Read not selected		
Yes	No	Yes	Read not selected		
Yes	Yes	Yes	Read not selected		
No	No	No	No	Yes	B
No	Yes	No	Read not selected		
Yes	No	No	Read not selected		
Yes	Yes	No	Read not selected		

8.3.11 Write/Read Head

The RD50 drive has two read/write heads, one for each drive side. The heads are selected by either the write circuits or read circuits. Figure 8-23 shows the head connections for a write function and Figure 8-25 shows the head connections for a read function.

Each head consists of a read/write ferrite core wound with a differential coil. The head also contains a forked erase ferrite core wound with a coil. The erase core is behind the write core with the forked core straddling the write core. This causes the delayed erase gate signal. See Paragraph 8.3.8.2 for more information.

During write operations, current flows through the coils and generates a magnetic flux in the core. When the media passes under the read/write core, the surface of the media is magnetized in one direction. Reversing the current magnetizes the surface in the opposite direction.

The forked erase core trims the edges of the magnetized surface. This ensures off-track reading capability.

During read operations only the read/write core is used. The erase core is not used. When the media passes under the read/write core, the recorded flux reversals generate small alternating currents in the read/write coils. This current passes to the read circuits for conversion to digital data.

8.4 INTERMODULE SIGNAL DEFINITIONS

Paragraphs 8.4.1 through 8.4.7 define all the control and data signals that pass between the controller module and the RX50 drive, and between the modules of the RX50 drive. All the signals defined in these paragraphs are grouped by common connector for easy recognition.

8.4.1 Seek and Interface/Controller Module Connector J1

Paragraph 8.4.1.1 through 8.4.1.12 describe the signals passed between the seek and interface module and the RX50 controller module. Figure 8-27 shows the control and data interface signal direction between the controller module and the RX50 drive. The seek and interface module is part of the RX50 drive.

Figure 8-28 shows the location of J1 and other module connectors. Odd numbered pins are grounded and are not discussed. An L next to a signal name designates it as asserted low (logic 0). An H next to a signal name designates it as asserted high (logic 1).

Pin	Mnemonic	Function
2	TKG43 L	Controls write current level
4	Reserved	Not used
6	DRIVE SEL3 L	Selects drive side B if J17 installed
8	INDEX L	Indicates index mark of selected side
10	DRIVE SEL0 L	Selects drive side A if J17 not installed
12	DRIVE SEL1 L	Selects drive side B if J17 not installed
14	DRIVE SEL2 L	Selects drive side A if J17 installed
16	MOTOR ON L	Turns spindle motor on or off
18	DIRECTION	Controls head movement direction
20	STEP L	Controls head movement distance
22	WRITE DATA L	Data to be stored on diskette
24	WRITE GATE L	Activates write circuits
26	TRACK 0 L	Track 0 head location indicator
28	WRITE PROTECT L	Indicates selected diskette is write protected
30	READ DATA L	Data retrieved from diskette
32	Reserved	Not used
34	READY L	Indicates that selected drive side contains a diskette

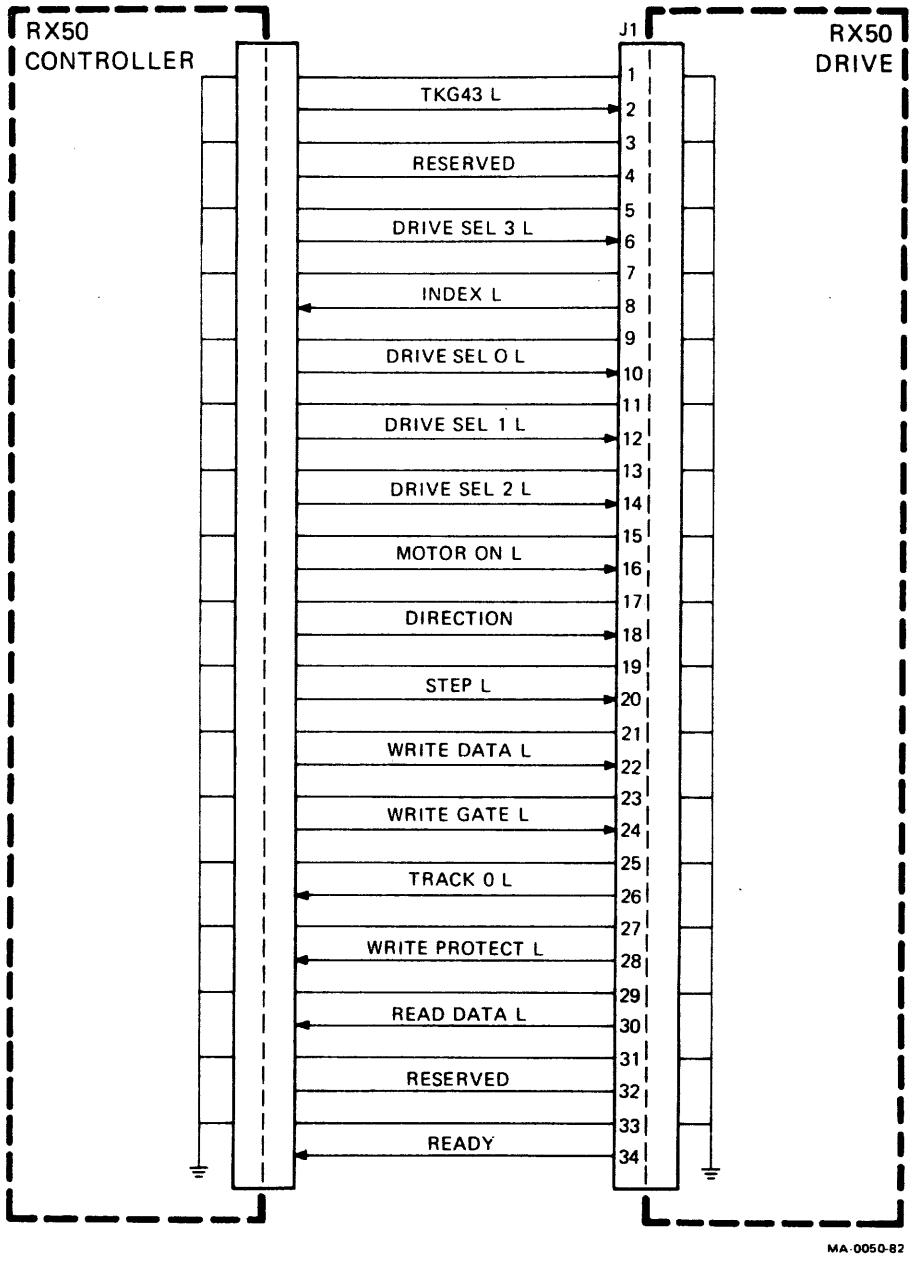


Figure 8-27 RX50 Controller Module and Drive Interface Signal Flow

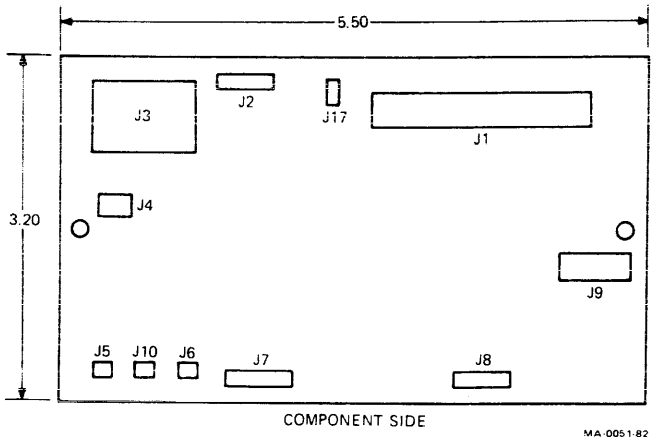


Figure 8-28 Seek and Interface Module Connector Locations

8.4.1.1 TKG43 L Input Signal – The controller module generates this signal. It is asserted when writing data to tracks 44 through 79. In the asserted state, the seek and interface module reduces the write current. In the deasserted state, the seek and interface module generates a normal write current.

8.4.1.2 DRIVE SEL 0 thru DRIVE SEL 3 Input Signals – These signals select the drive side (A or B) on which a function occurs. When J17 is not installed, DRIVE SEL 0 selects drive side A and DRIVE SEL 1 selects drive side B. When J17 is installed, DRIVE SEL 2 selects drive side A, and DRIVE SEL 3 selects drive side B.

8.4.1.3 TRACK 0 L Output Signal – This signal indicates that the heads are over track 0 (the outermost track). This signal is valid only when a drive side is selected.

8.4.1.4 MOTOR ON L Input Signal – This signal controls the motor control module, which controls the spindle motor. When this signal is asserted, the spindle motor rotates. The spindle motor reaches the rated rotating speed within 1/2 second after an asserted MOTOR ON signal.

8.4.1.5 DIRECTION Input Signal – This signal defines the head movement direction when the STEP input line is pulsed. Step-out (moving away from the center of the disk) is defined as the high level of this signal (logic 1). step-in (moving towards the center of the disk) is defined as the low level of this signal (logic 0).

8.4.1.6 STEP L Input Signal – When pulsed, this signal moves the heads. Each pulse moves one track space in the direction indicated by the DIRECTION signal. The minimum pulse width is 1 μs. The minimum width between step pulses is 6 ms. This signal is ignored when WRITE GATE L is asserted, MOTOR ON L is deasserted, or no drive side is selected.

8.4.1.7 WRITE DATA L Input Signal – This signal represents data to be stored on the diskette. Each transition to the asserted state reverses the current to the read/write heads. Write pulses must begin within 500 ns after WRITE GATE is asserted. A minimum of 36 ms is needed after the last STEP pulse occurs. Write pulses are ignored when WRITE GATE or MOTOR ON are deasserted, the diskette is write protected, no diskette is present, or no drive side is selected.

8.4.1.8 WRITE GATE L Input Signal – This signal enables writing and tunnel erasing of data to the diskette. This signal is ignored when the diskette is write protected.

8.4.1.9 INDEX L Output Signal – The leading edge of this pulse signal indicates the detection of the index hole in the selected drive side. The INDEX L pulse is valid 250 ms after MOTOR ON L is asserted. This indicator signal is invalid if no drive side is selected.

8.4.1.10 WRITE PROTECT L Output Signal – When asserted, this signal indicates that the write enable notch of the selected diskette is masked and the writing of new data is inhibited. This signal is invalid if no drive side is selected.

8.4.1.11 READ DATA L Output Signal – This signal represents data retrieved from the diskette. READ DATA L is valid 250 ms after MOTOR ON L is asserted, 36 ms after receiving the last STEP L pulse, 1.21 ms after WRITE GATE signal is deasserted, or 30 ms after the drive side is selected.

8.4.1.12 READY Output Signal – This signal indicates that a diskette is present in the selected drive side. It is valid only if a drive side is selected.

8.4.2 Seek and Interface/Motor Control Modules Connector J4

This section describes the signals passed between the seek and interface module and motor control module. Figure 8-28 shows the location of J4 and other module connectors. Power and ground signals are not described in detail. An L next to a signal name designates it as asserted low (logic 0). An H attached to a signal name designates it as asserted high (logic 1).

Pin	Mnemonic	Function
1,2	+12 V RET	Ground
3	MPWR H	Turns on spindle motor
4	+5 VDC	Side B index light emitting diode power source
5	SIDE A L	Drive A indicator control
6	SIDE B L	Drive B indicator control
7,8	+12 VDC	Spindle motor and control logic power source

8.4.2.1 MPWR H Input Signal – This signal controls the spindle motor. When the signal is asserted, the spindle motor control logic is enabled and the spindle motor turns on.

8.4.2.2 SIDE A L Input Signal – This signal controls the drive A operational indicator on the front panel. When the signal is asserted, the indicator comes on when the drive is in use.

8.4.2.3 SIDE B L Input Signal – This signal controls the drive B operational indicator on the front panel. When the signal is asserted, the indicator comes on when the drive is in use.

8.4.3 Seek and Interface/Read Write Modules Connector J9

This paragraph describes the signals passed between the seek and interface module and read/write module. Figure 8-28 shows the location of J9 and other module connectors. Power and ground signals are not described in detail. An L next to a signal name designates it as asserted low (logic 0). An H next to a signal name designates it as asserted high (logic 1).

Pin	Mnemonic	Function
1	DCOK L	Turns on +12 V power to module
2	+12 V RET	Ground
3	+WRITE L	+ Write data
4	R DATA H	Read data
5	W GATE L	Enables a write function
6	−WRITE L	− Write data
7	SIDE 0	Not used
8	WRITE CURRENT SWITCH	Controls the level of the write current
9	ERASE GATE L	Controls tunnel erase function
10	+5 VDC	Side B index light emitting diode power source
11	SEL A L	Head select control signal
12	+12 VDC	+12 V power source

8.4.3.1 DCOK L Output Signal – This signal controls the +12 V power on the read/write module. When this signal is asserted, +12 V power is applied to the write and erase circuits on the module. When this signal is deasserted, +12 V power is removed from the circuits to protect data on the diskette.

8.4.3.2 ±WRITE L Output Signals – This differential signal pair switches the direction of the write current in the read/write heads. The signals are alternately asserted but not simultaneously asserted. During write-protected or nonwrite operations both signals are deasserted.

8.4.3.3 R DATA H Input Signals – This signal is the data output of the read/write module to the seek and interface module. The signal contains positive going pulses that average 1 μs in duration. Positive going edges contain timing information to reconstruct nonreturn to zero (NRZ) data.

8.4.3.4 W GATE L Output Signal – This signal controls the write circuits on the read/write module. When asserted, this signal enables the write circuits. This signal is deasserted during both nonwrite and write-protected operations. This signal is also deasserted if the spindle motor is off, the drive side is not selected, the diskette is missing, or the diskette is in backwards.

8.4.3.5 WRITE CURRENT SWITCH Output Signal – This signal switches the write current level above and below track 44. This action minimizes peak shift in the heads and media due to close tolerances of the flux changes. When asserted, this signal enables a high write current when the heads are over tracks 0 through 43. When deasserted, this signal enables a low write current when the heads are over tracks 44 through 79.

8.4.3.6 ERASE GATE L Output Signal – This signal controls the current to the erase coils. When this signal is asserted, a current is produced in the selected erase coil. When writing is inhibited, this signal stays deasserted to disable the erase current.

8.4.3.7 SEL A L Output Signal – This signal selects one of the heads for read, write, and erase operations. When this signal is asserted, head A of drive side A is selected. When this signal is deasserted, head B of drive side B is selected.

8.4.4 Seek and Interface Power Connector J3

This paragraph describes the connector that receives power for the entire RX50 drive. Figure 8-28 shows the location of J3 and other RX50 connectors module. See Paragraph 8.2.4 for the power requirements.

Pin	Mnemonic	Function
1	+12 VDC	+12 Vdc
2	+12 VDC RET	Ground
3	+5 VDC RET	Ground
4	+5 VDC	+5 Vdc

8.4.5 Seek and Interface Connectors J2, J5, J6, J7, J8, J10, and J17

Paragraphs 8.4.5.1 through 8.4.5.7 describe the functions of the seek and interface module's remaining connectors. A brief description of signal functions is also provided. Figure 8-28 shows the location of these module connectors. An L next to a signal name designates it as asserted low (logic 0). An H next to a signal name designates it as asserted high (logic 1).

8.4.5.1 Side A Switches and Indicators Connector J2

Pin	Mnemonic	Function
1	WP A H	Write-protect indicator
2	SEL A L	Write-protect/diskette present indicator select
3	DP A H	Diskette present indicator
4	SEL A L	Index indicator select
5	INDEX A L	Index indicator

8.4.5.2 Track 0 Sensor Connector J5

Pin	Mnemonic	Function
1	TK0S H	Track 0 indicator
2	TK0A	Transmitter diode +5 V source
3	TK0K	Transmitter/receiver diode sink

8.4.5.3 Side B Head Load Solenoid Connector J6

Pin	Mnemonic	Function
1	+12 VDC	Head load solenoid power source
2	SIDE B L	Solenoid control signal

8.4.5.4 Stepper Motor Connector J7

Pin	Mnemonic	Function
1	STM1	Stepper motor phase 1 control
2	STM2	Stepper motor phase 2 control
3	+12 VDC	Stepper motor +12 Vdc power source
4	STM3	Stepper motor phase 3 control
5	STM4	Stepper motor phase 4 control
6	+12 VDC	Stepper motor +12 Vdc power source

8.4.5.5 Side B Switches and Indicators Connector J8

Pin	Mnemonic	Function
1	WP B H	Write-protect indicator
2	SEL B L	Write-protect/diskette present indicator select
3	DP B H	Diskette present indicator
4	SEL B L	Index indicator select
5	INDEX B L	Index indicator

8.4.5.6 Side A Head Load Solenoid Connector J10

Pin	Mnemonic	Function
1	+12 VDC	Head load solenoid power source
2	SIDE A L	Solenoid control signal

8.4.5.7 Drive Select Jumper J17

Pin	Mnemonic	Function
1	GND	Ground
2	SEL 1 H	This signal selects the drive configuration. When asserted with the jumper removed, DRIVE SEL 0 L and DRIVE SEL 1 L access the RX50 drive. When deasserted with the jumper installed, DRIVE SEL 2 L and DRIVE SEL 3 L access the RX50 drive.

8.4.6 Motor Control Modules Connectors J4, J11, J16

This paragraph describes the motor control module's connectors. Figure 8-29 shows the location of these connectors and other module connectors. Connector J4 connects to the seek and interface module's connector J4 (described in Paragraph 8.4.2).

8.4.6.1 Spindle Motor Connector J11

Pin	Mnemonic	Function
1	TACH 1	Half of tachometer differential pair
2	TACH 2	Half of tachometer differential pair
3	MOT RET	Spindle motor power return
4	+12 VDC	+12 V motor power source

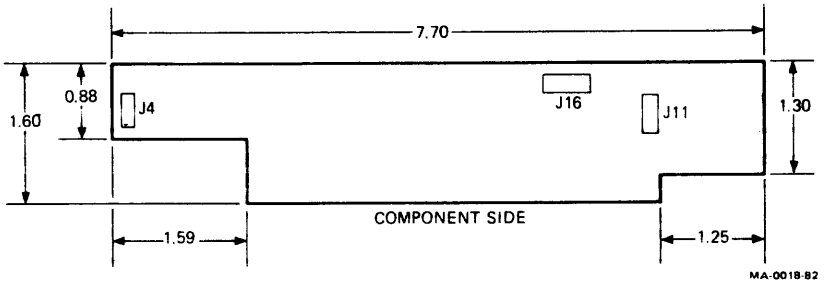


Figure 8-29 Motor Control Module Connector Locations

8.4.6.2 Front Panel Operational Indicators Connector J16

Pin	Mnemonic	Function
1	+12 VDC	Indicator power source for side A
2	SIDE A L	Side A indicator control signal
3	+12 VDC	Indicator power source for side B
4	SIDE B L	Side B indicator control signal

8.4.7 Read/Write Module Connectors J9, J14, J15

This section describes the connectors of the read/write module. Figure 8-30 shows the location of these connectors and other connectors of the module. Connector J9 connects to the seek and interface modules connector J9 and is described in Paragraph 8.4.3.

8.4.7.1 Side A Read, Write, and Erase Head Connector J14

Pin	Mnemonic	Function
1	HEAD SEL A	Side A head common
2	SHIELD	Head control line shield
3	ERASE COIL	Erase coil control line
4	+ COIL	+ Read/write coil control line
5	– COIL	– Read/write coil control line
6	-	Not used

8.4.7.2 Side B Read, Write, and Erase Head Connector J15

Pin	Mnemonic	Function
1	HEAD SEL B	Side B head common
2	SHIELD	Head control line shield
3	ERASE COIL	Erase coil control line
4	+ COIL	+ Read/write coil control line
5	– COIL	– Read/write coil control line
6	-	Not used

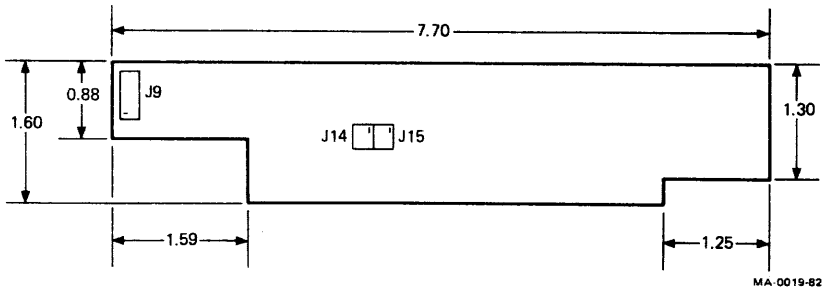


Figure 8-30 Read/Write Module Connector Locations

8.5 SPECIFICATIONS

The following paragraphs provide the specifications for the RX50 dual diskette drive.

8.5.1 Performance Specifications

Capacity (Formatted)	**MFM**	
Per drive	819,200	(800 kilobytes)
Per surface	409,600	(400 kilobytes)
Per track	5,120 bytes	
Diskette quantity	2	

Transfer Rate	**MFM**	
Per drive	250,000	bits/s

Access Time	**Minimum**	**Typical**	**Maximum**
Track to track	6 ms	–	–
Head settling time	–	–	30 ms
Head load time	–	–	30 ms
Rotational latency	–	100 ms	200 ms
Random access	–	164 ms	–
Drive motor start	–	–	500 ms

8.5.2 Reliability Specifications

Mean time between spindle motor failures	6000 POH at 30% duty cycle 2000 POH at 100% duty cycle
Mean time to repair	15 minutes
Error rates (typical random exerciser)	
Soft read errors	1 per 10^9 bits read
Hard read errors	1 per 10^{12} bits read
Seek errors	1 per 10^6 seeks
Media life	3×10^6 passes
Media insertion	1×10^4 insertions

8.5.3 Functional Specifications

Rotating speed (rpm)	300
Speed variations	−1.5% to +1.5% maximum
Flux density (track 79) (flux changes/in)	5576
Track density (tracks/in)	96
Tracks (per diskette)	80
Outside track radius	57.15 mm (2.25 in)
Inside track radius	36.51 mm (1.427 in)
Data sectors (soft)	10
Data bytes per sector	512
Index	1

8.5.4 Electrical Specifications

Requirement	Minimum	Typical	Maximum
5 V	4.75 V	5.0 V	5.25 V
Ripple	–	–	50 mV
Current	–	0.50 A	0.80 A
12 V	11.4 V	12.0 V	12.6 V
Ripple	–	–	100 mV
Standby current	–	0.12 A	0.25 A
Operating current (seeking)	–	1.25 A	1.8 A
Startup current for 0.25 seconds	–	–	2.7 A

8.5.5 Environmental Specifications

Ambient temperature	15° to 32°C (59°F to 90°F)
Relative humidity	20% to 80% noncondensing
Maximum wet bulb	25°C (78°F)
Shock and vibration	1 G acceleration
Shipping shock	2 G acceleration
Diskette jacket	40°C (40°F) maximum

8.5.6 Mechanical Specifications

Width	14.6.1 mm (5.75 in)
Height	82.55 mm (3.25 in)
Depth	215.9 mm (8.50 in)
Weight	2.18 kg (4.8 lb)
Operating power dissipation	17.5 W typical
Standby power dissipation	4.2 W typical

CHAPTER 9
RD52-A DISK DRIVE

9.1 INTRODUCTION

This chapter is a technical description of the RD52-A Disk Drive. There are two disk drives named RD52-A. Each RD52-A has a specific Digital part number (PN 30-21721-02 or PN 30-23227-02). Paragraph 9.3 shows you how to determine which RD52-A you have. Paragraph 9.4 contains RD52-A general specifications. Paragraph 9.5 lists documentation related to the RD52-A. Paragraphs 9.6 and 9.10 are technical descriptions of each RD52-A.

9.2 PRODUCT DESCRIPTION

The RD52-A is a 5.25-inch Winchester technology disk drive. It has a capacity of 30.97 megabytes using an 18-sector format, or 33.48 megabytes using a 16-sector format.

The RD52-A conforms to ST506/412 small disk interface requirements. This architecture uses a drive control bus and a read/write bus. The drive control bus can be connected either daisy-chained or radially between multiple drives and the host adapter module. The data bus is connected radially from the host adapter module.

The RD52-A is plug compatible with the RD50 and RD51 disk drives. These disk drives may not be directly interchangeable, however, due to different power consumption and controller/software limitations. Check your system documentation for compatability information.

The RD52-A needs no special tools or equipment to install or remove after appropriate system covers and shielding are removed. This disk drive does not need preventive maintenance or field adjustments. When power is removed, the disk drive automatically seeks to, lands on, and locks in a dedicated zone.

9.3 IDENTIFYING YOUR RD52-A DISK DRIVE

To determine which RD52-A disk drive you have, do the following.

1. Find the ID label on the RD52-A (Figure 9-1).

2. Find the part number, then use Figure 9-2 to determine which RD52-A you have.

   a. If you have the RD52-A with PN 30-21721-02, you can find its technical description in Paragraph 9.6.

   b. If you have the RD52-A with PN 30-23227-02, you can find its technical description in Paragraph 9.10.

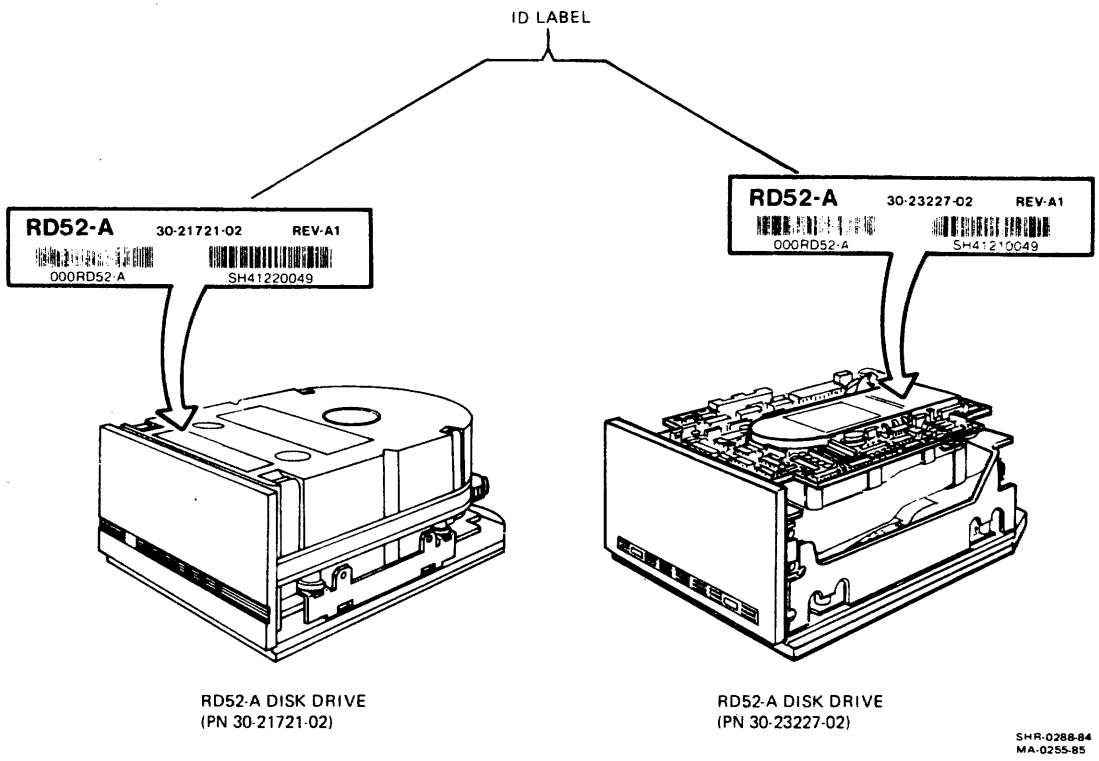


Figure 9-1 RD52-A ID Label Location

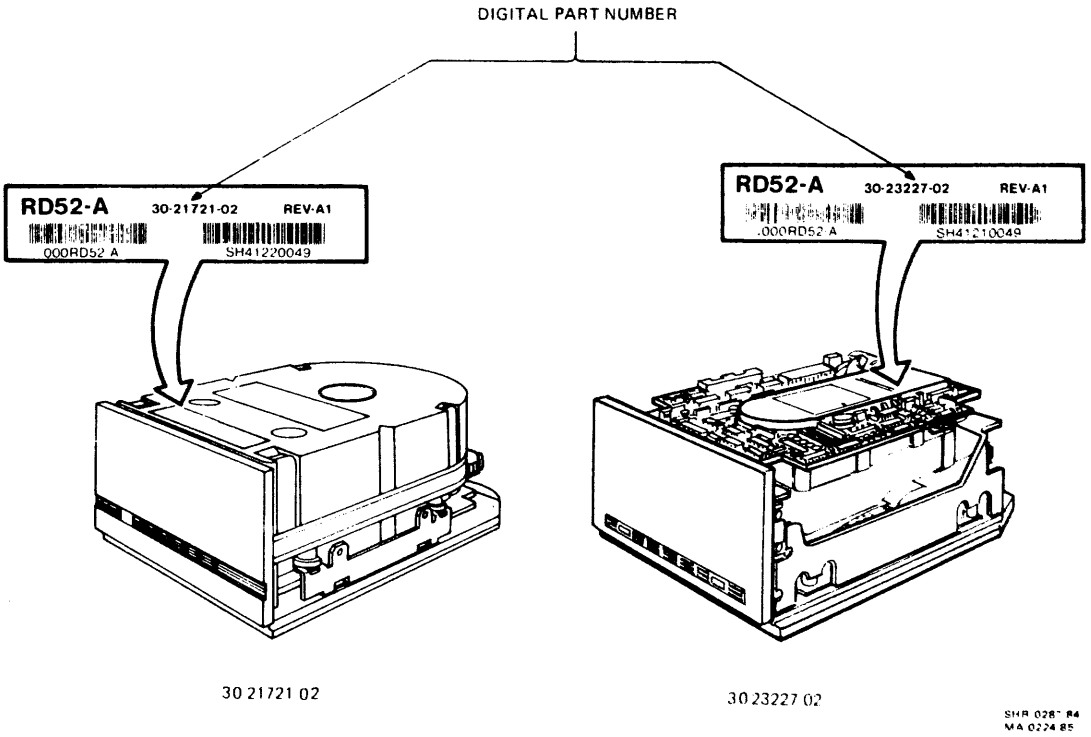


Figure 9-2 RD52-A Part Number Location

9.4 RD52-A GENERAL SPECIFICATIONS

Physical

Weight	3.18 kg (7.00 lb)
Height	8.25 cm (3.25 in)
Width	14.6 cm (5.75 in)
Depth	20.3 cm (8.00 in)

Power

Power consumption	42 W (typical) (See Paragraphs for maximum)	
	+5 V	**+12 V**
Current	1 A (typical) 1.5 A (maximum)	2.5 A (typical)
Voltage range	4.75 Vdc (minimum) 5.25 Vdc (maximum)	11.4 Vdc (minimum) 12.6 Vdc (maximum)
Maximum ripple	50 mV (peak to peak)	75 mV (peak to peak)

Environmental

	Operating	**Non-operating**
Temperature	10° to 50°C (50° to 122°F)	−40° to 56°C (−40° to 151°F)
Relative humidity	10% to 80%	8% to 95%
Altitude	2.4 km (8000 ft)	9.1 km (30,000 ft)
Heat dissipation	119 Btu/hr (typical) 148 Btu/hr (maximum)	

9.5 RELATED DOCUMENTATION

Table 9-1 lists Digital documentation related to the RD52-A.

Table 9-1 Related Documentation

Title	Document Number
Micro-PDP-11 System Unpacking and Installation Guide	EK-OLDP5-OD
Micro-PDP-11 System Technical Manual	EK-OLCP5-TM
Micro-PDP-11 System Owner's Manual	EL-OLCP5-OM
Micro-PDP-11 Pocket Service Guide	EK-OLCP5-PS
MicroVAX I Technical Description Manual	EK-KD32A-TD
MicroVAX I Owner's Manual	EK-KD32A-OM
MicroVAX I Pocket Service Guide	EK-KD32A-PS
MicroVAX II Owner's Manual	EK-UVAX2-OM
MicroVAX II Pocket Service Guide	EK-UVAX2-PS
Professional 300 Series Technical Manual (Volume 1)	EK-PC300-V1
Professional 300 Series Pocket Service Guide	EK-PC300-PS
Professional 380 Pocket Service Guide	EK-PC380-PS
Professional 350 Owner's Manual	EK-PC350-OM
Professional 380 Owner's Manual	EK-PC380-OM
RD52-A Illustrated Parts Breakdown	EK-RD52A-IP
RD52-D,-R Fixed Head Disk Drive Subsystem Owner's Manual	EK-LEP03-OM

9.6 RD52-A (30-21721-01) DISK DRIVE

There are two disk drive systems named RD52-A. Refer to Paragraph 9.3 to determine which RD52-A disk drive you have. Paragraphs 9-6 through 9.9 are a technical description of the RD52-A with PN 30-21721-02 (Figure 9-3).

Paragraphs 9.6.1 through 9.6.3 give a brief overview of the RD52-A, specifications, and external power requirements. Paragraph 9.7 is a physical description of the disk drive. Paragraph 9.8 describes operator functions and theory of operation. Paragraph 9.9 describes the two interface connectors (control and data) and gives connector dimensions, pin assignments, signal descriptions, and recommended driver/receiver combinations.

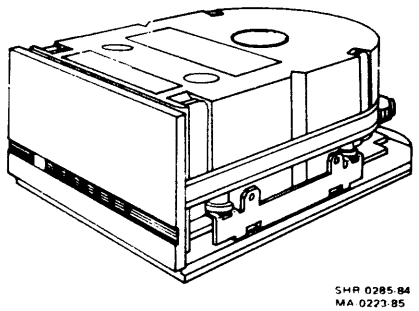


Figure 9-3 RD52-A Disk Drive

9.6.1 General

The RD52-A is a Winchester technology random access storage device that uses four nonremovable disks as storage media. Each disk surface uses one movable head to service its data tracks. The RD52-A uses a rotary head position actuator and a microprocessor-controlled positioner. Servo information is written on the lower surface of the second disk during a 290 μs "time wedge" just before index. To compensate for this once-per-revolution servo time, the disk drive's rotating speed is 2 percent slower than the typical 3600 rpm (3529 rpm). However, the RD52-A offers the advantage of using every disk surface for data storage, as opposed to a track following servo system that dedicates one entire disk surface to servo information.

The RD52-A does not need preventive maintenance or field adjustments. Check your specific system documentation for installation, removal, and maintenance information.

9.6.2 Specifications

9.6.2.1 Physical Specifications

Environmental Limits

	Operating	**Non-operating**
Ambient temperature	10° to 50°C (50° to 122°F)	−40° to 66°C (−40° to 151°F)
Ambient relative humidity	10% to 80%	8% to 95%
Altitude	2.4 km (8000 ft)	9.1 km (30,000 ft)

Mechanical dimensions

Height	8.25 cm (3.25 in)
Width	14.6 cm (5.75 in)
Depth	20.32 cm (8.00 in)
Weight	3.15 kg (7 lb)

Heat dissipation

23 W (79 Btu/hr) typical
(50% duty cycle between seeking and not seeking)

31 W (106 Btu/hr) maximum
(50% duty cycle between seeking and not seeking)

37 W (126 Btu/hr) worst case
(continuous seeking)

Shock and Vibration

	Operating	**Nonoperating**
Shock	10.0 G	20.0 G (5 - 500 Hz sinewave)
Vibration	0.25 G peak	1.00 G rms

Track Geometry

Width	0.0011 ± 0.0001 in
Spacing	0.0017 in
Track 0 radius	2.37 in (nominal)
Track 511 radius	1.47 in (nominal)
Shipping/landing zone	1.16 in (nominal)

9.6.2.2 Performance Specifications

Capacity (Unformatted)	
Per drive (megabytes)	42.66
Per surface (megabytes)	5.33
Per track (bytes)	10,416

Access Times (including head settling)	**Typical**	**Maximum**
Track to track	10 ms	12 ms
Average	45 ms	49 ms
Full stroke	80 ms	90 ms
Average latency	8.5 ms	

9.6.2.3 Functional Specifications

Nominal rotating speed (rpm)	3529
Maximum rotating speed (rpm)	3564
Minimum rotating speed (rpm)	3494
Maximum recording density (bits/in)	9200
Maximum flux density (flux changes/in)	9200
Track density (tracks/in)	591
Cylinders	512
Tracks	4096
Read/write heads	8
Disks	4
Index	1

9.6.3 Power Requirements

9.6.3.1 DC Power – Table 9-2 lists the voltage and current requirements for the dc power supplied to the disk drive. The RD52-A does not require power sequencing either off or on. Figure 9-4 shows the disk drive's startup current profile.

9.6.3.2 DC Power Connector – The dc power connector (P3) is a 4-pin AMP Mate-N-Lock connector (AMP PN 350211-1) on the solder side of the printed circuit board (PCB). The recommended mating connector (J3) is AMP PN 1-408424-0 using AMP pins PN 350078-4 (strip) or PN 61173-4 (loose piece). J3 pins are labeled on the J3 connector. Figure 9-5 shows the J3 connector signals and pin orientation.

Table 9-2 DC Power Requirements

Voltage		
Nominal	+12 V	+5 V
Current		
Typical	2.0 A (seeking)	0.7 A
Maximum	2.4 A (seeking)	1.0 A
Maximum	4.5 A (for 14 seconds)	
Regulation	±1.2 V	±0.25 V
Ripple and noise maximum	100 mv peak to peak	50 mv peak to peak

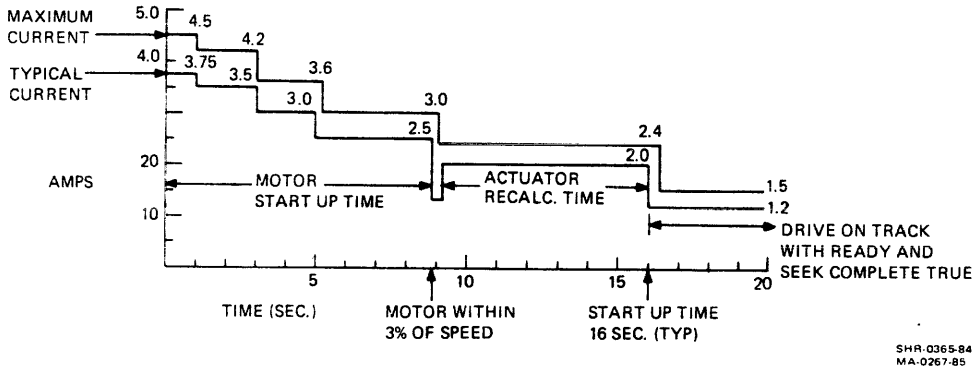
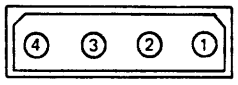


Figure 9-4 Drive Startup Current Profile



PIN 1 – +12 VOLTS
PIN 2 – +12 VOLT RETURN
PIN 3 – +5 VOLT RETURN
PIN 4 – +5 VOLTS

SHR-0366-84
MA-0268-85

Figure 9-5 J3 Connector

9.7 PHYSICAL DESCRIPTION

9.7.1 RD52-A Drive Mechanism

The drive mechanism consists of the disk drive's mechanical subassemblies sealed under a metal bubble. None of these need adjustments or are field repairable. The mechanical subassemblies are described in the Paragraphs 9.7.1.1 through 9.7.1.7 and shown in Figure 9-6.

9.7.1.1 Base Casting – The base casting is a single piece of cast aluminum alloy that provides a mounting surface for the rest of the drive mechanism. It has two machined holes for mounting the motor/spindle assembly and the positioner assembly. The outside top edge is flat to ensure an airtight seal with the metal bubble cover. It has surfaces for mounting the optical encoder, encoder PCB, and the upper magnet plate for the positioner motor. It also has mounting holes outside the bubble area for the control PCB and front bezel.

9.7.1.2 DC Spindle Drive Motor – The RD52-A has a dc spindle drive motor, which is controlled by an Intel 8048, single-chip microprocessor. Three hall effect devices provide position feedback to the microprocessor that performs the logic for commutation. An index signal is generated from an LED/phototransistor pair; output is generated as a TTL level from the motor. The LED shines light on the rim of the motor's rotor. This light is reflected and the phototransistor detects it as the INDEX signal when the unpainted portion of the rotor rim passes across the detector pair.

The disk stack is mounted on the dc motor. The motor is bolted to the base of the drive. The motor bearings are sealed from the disk and heads by a magnetic fluid seal.

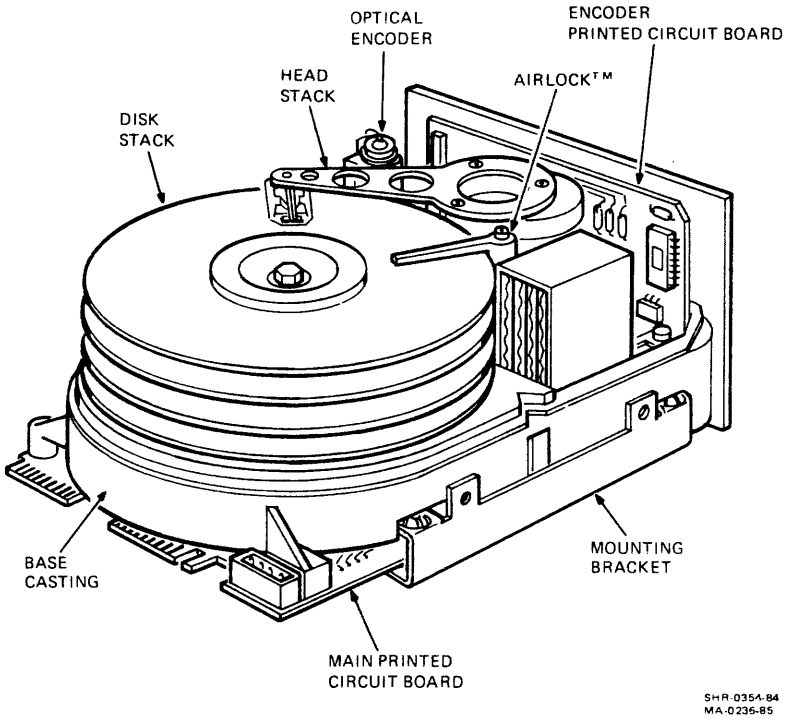


Figure 9-6 RD52-A Mechanical Layout

9.7.1.3 Disk Stack – The disk stack is attached to the dc spindle motor, which is bolted to the base casting. The disk stack consists of disks, disk spacers, a disk clamp, and a grounding system for the spindle. Four disks and spacers are clamped in place on the disk mounting hub. The disks are an aluminum alloy with a magnetic oxide coating, which is polished and lubricated. The lubrication prevents head and media wear when the heads touch the disk surface. Such contact only occurs outside the data area and when the disks are not rotating. The spindle's grounding system consists of the following parts.

- A steel button bonded to the bottom of the dc motor
- A carbon button bonded to a spring contact on the control PCB.

9.7.1.4 Head Stack – The head stack consists of the heads, head arms and counter balances, and the optical scale. The counter balances are castings whose shape and weight ensure that the mass center of the entire stack is at the center of the mounting hub. The optical scale is bonded to the second to lowest counter balance. The optical scale provides position feedback via the optical encoder (see Paragraph 9.7.1.5). The heads are Winchester slider-type heads with a 0.0011-inch track width mounted to spring steel flexures staked to the head arm. The head conductors are flexible cables routed in plastic guides and attached with adhesive. All head stack assemblies have an upper and lower head arm assembly. There are three head arm assemblies.

9.7.1.5 Optical Encoder – The optical encoder is a position-sensing device. It provides feedback for the closed loop system that controls head stack positioning. The encoder consists of a housing, an infrared LED, an optical reticle, and a multicell photodiode matrix.

The infrared LED is mounted in the housing above the reticle. The reticle, which sits above the photo diode, acts as a light mask to control the light that reaches the photo diode. The reticle is matched to a optical scale mounted on the head stack. As the head stack moves, light reaching the photo diode varies according to the match between the optical scale and the reticle. The light intensity is decoded into position information.

When the disk drive is built, certain precision adjustments are made. Among these adjustments are the clearance and angular portion of the reticle, relative to the scale.

9.7.1.6 Rotary Positioner – The positioner used in the RD52-A is a rotary voice coil actuator. The positioner's rotor consists of two flat, triangular coils. These coils are molded so they are perpendicular to the spindle shaft. This assembly is then mounted to the base so the coils are suspended in a permanent magnetic field. The field is created by two magnetic segments – one mounted above the coils and one mounted below the coils. The segments are polarized so current passing through the coils causes the positioner to rotate. Variations in current cause the positioner to rotate in either direction, or to stop moving.

9.7.1.7 Automatic Actuator Lock – The RD52-A uses a dedicated landing zone to ensure data integrity and prevent damage during shipment. Airlock™ is an entirely mechanical means of locking the head stack in the landing zone. The Airlock is an airvane mounted close to the edge of the disk stack. The airvane has an arm that intersects the actuator to hold the head stack in the landing zone when the disks are not rotating. As dc power is applied to the motor, and the disk stack starts rotating, an airflow is generated around the disk. As airflow increases with disk rotation the airvane and its arm rotate, which allows the head stack to move freely out of the landing zone.

™ Airlock is a trademark of Quantum Corporation.

9.7.2 Electromagnetic Interference (EMI) Band

A Winchester type drive is sensitive to electromagnetic interference (EMI) due to the low signal level at the read/write heads. Therefore, it is necessary to shield the heads from EMI. On the RD52-A, the base casting and cast cover provide most of the shielding. However, the sealing gasket at the intersection of these two castings causes a gap that needs shielding. An apparatus (wire mesh attached to a rubber strip) placed over the gap and clamped in place with a stainless steel band (strap) provides the shielding.

9.7.3 Air Filtration

Because the RD52-A is a Winchester-type disk drive, the heads fly very close to the media surface. The nominal flying height is 18 microinches.

The air circulating within the disk drive must be kept clean and free of particles. The RD52-A is assembled in a Class 100 purified air environment and then sealed in the metal bubble. During the life of the disk drive, the rotating disks act as an air pump to force the air through two internal filters. Figure 9-7 shows the airflow in the enclosed area of the disk drive. The lowest pressure area within the disk drive is at the top in the center of the spindle. A 0.3-micron breather filter is bonded in this area of the bubble. This filter allows outside air into the bubble enclosure to equalize internal and external pressure. The highest pressure area within the disk drive is at the outer edge of the disk. Bonded to the Airlock base at this location is another 0.3-micron filter called the circulation filter. Air is constantly pumped into the side of the filter nearest the disks, filtered and expelled from the side of the filter away from the disks. This area of the disk drive is at a lower pressure than at the edge of the disks; thus air circulates through the filter. This ensures a continuous flow of filtered air as soon as the disks start to rotate.

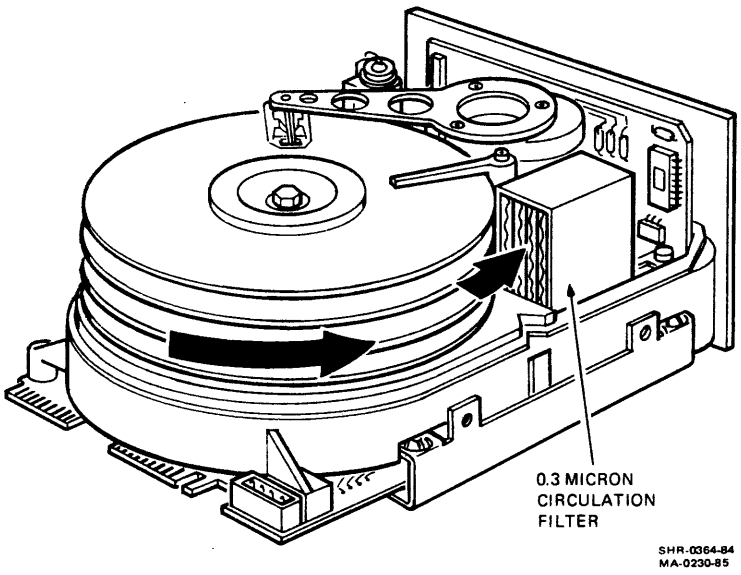


Figure 9-7 Air Filtration System

9.8 OPERATION

9.8.1 Operator Functions

Operator functions vary depending on the system in which the disk drive is installed. Paragraphs 9.8.1.1 and 9.8.1.2 describe the functions that an operator may perform: drive selection and control cable termination. Figure 9-8 shows the selection jumper and cable terminator on the RD52-A disk drive's control PCB.

9.8.1.1 Drive Select – Five jumpers are provided for logical drive number assignment. DS1, DS2, DS3, and DS4 cause the drive to be selected when the active drive select line matches the installed jumper. Jumper A, when installed, causes the drive to be selected constantly. Note that jumper A is not used in Digital applications.

9.8.1.2 Control Cable Termination – If the RD52-A is the last disk drive at the end of the control signal cable, a 220/330 ohm terminator pack must be installed at PCB location RN3. The terminator pack must be removed from RN3 if the RD52-A is not at the end of a string of drives. The terminator pack should be installed for all Digital applications.

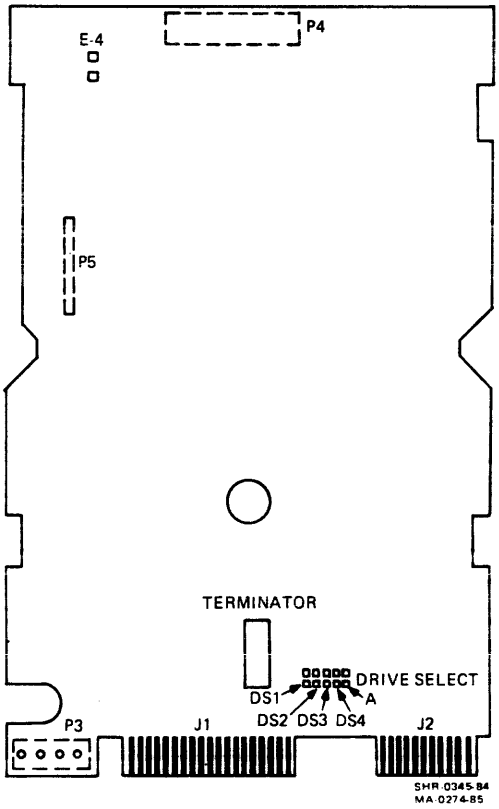


Figure 9-8 PCB Jumper/Terminator Locations

9.8.2 Functional Description

Figure 9-9 is a block diagram of the RD52-A. The spindle is driven from a dc motor mounted on the spindle shaft, which is powered from the +12 V supplied to the drive via the P3 connector. The dc motor causes the spindle to rotate the disk at 3529 rpm. The read/write head stack is mounted directly on the rotor of the rotary positioner. The rotary positioner is driven by power drivers, which are controlled by microprocessor-based circuitry on the control PCB. Head stack track and position feedback signals are provided by an optical encoder and glass scale assembly via the encoder PCB. On-track thermal compensation is obtained from servo data written in a 290 μs wedge on physical disk surface three. Optical position feedback and a servo wedge (which gives a hard track center) allow all the disk surfaces to be used for data storage, yet remain soft sectored. Read/write signals are obtained from, or written to, the disk via the head switching matrix on the encoder PCB and the heads mounted on the head stack. The drive control PCB contains the electronics for servo position decoding, the head stack positoner drive, the microprocessor that controls these functions, and read/write amplification and drive.

9.8.3 Drive Electronics

This paragraph describes the functions performed by the RD52-A electronics. Figure 9-10 is a block diagram of the RD52-A drive electronics. The drive electronics contain the following circuitry.

Interface buffers	These drivers and receivers buffer the control and data signals between the drive and the drive controller. Paragraph 9.9 describes the functions of the various interface signals.
DC power circuits	This circuitry provides power decoupling and regulation, as well as the power-up reset signal.
Read/write electronics	This circuitry provides the write current to record data and the circuits to detect recorded data.
Encoder PCB	This PCB contains the head switching matrix and circuits that generate track position signals from the signals provided by the scale and optical encoder.
Servo position detection	Using signals from the factory-recorded servo, this circuitry provides servo detection for fine head positioning.
Actuator drive circuits	This circuitry provides the power to drive the actuator and head stack assembly.
Actuator microprocessor	This single-chip processor controls the drive during its various operating modes. This processor takes the output of the encoder PCB and servo position-detection circuitry to generate track position signals to position the actuator.
Motor microprocessor	This single-chip processor controls start-up and speed control of the dc motor. It also provides index timing for the interface and servo detection and correction.

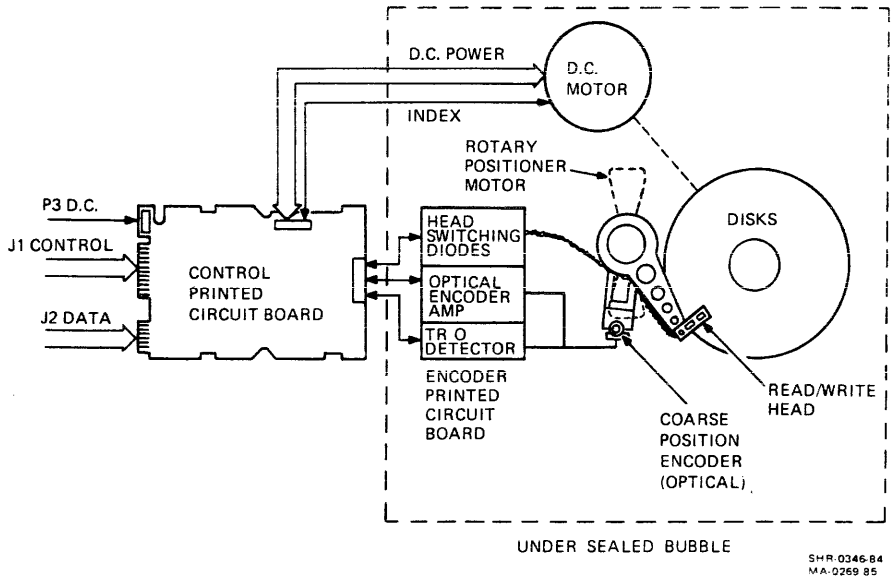


Figure 9-9 RD52-A Block Diagram

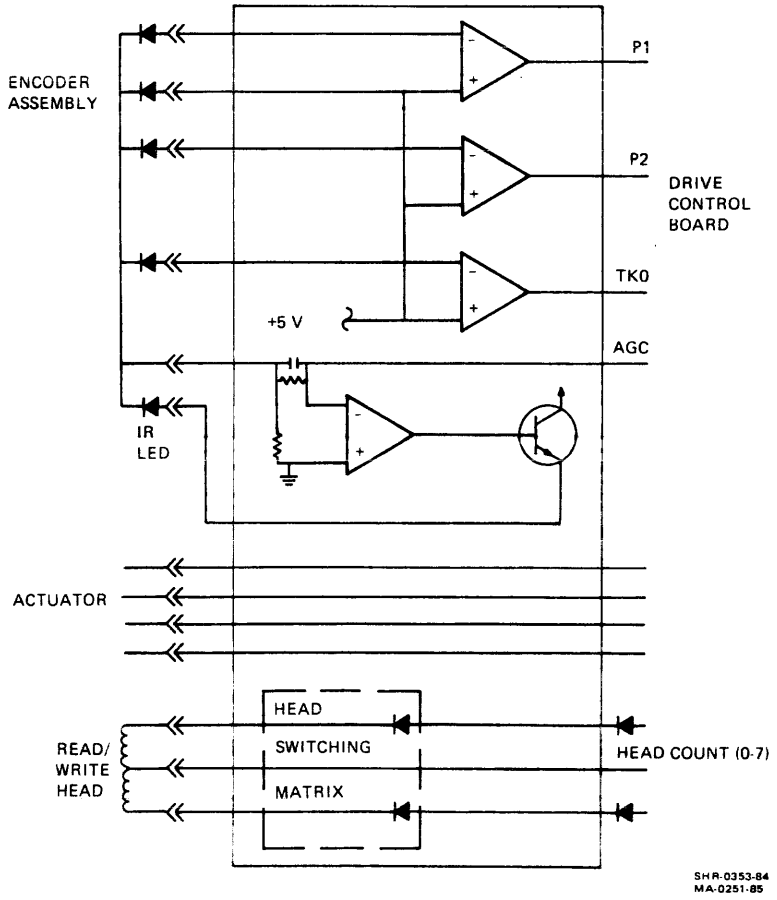


Figure 9-10 RD52-A Drive Electronics

9.8.4 Encoder PCB

Figure 9-11 is a functional block diagram of the encoder PCB. The encoder PCB contains the following parts.

- The photo diodes used for head switching
- A through-bubble connector (for the head signals, actuator drive signals, and actuator position signals)
- The operational amplifiers (op amps) used to detect the encoder photo cell outputs
- The automatic gain control (AGC) amplifier used to control the infrared LED drive current

9.8.4.1 AGC Circuit – Figure 9-12 shows the AGC circuit. Paragraph 9.7.1.5 describes the mechanical operation of the transducer scale, reticle, and photo cell.

9.8.4.2 P1 and P2 Signal Generation – Refer to Figure 9-13 for a schematic of P1 and P2 signal generation.

P1 and P2 are derived from two photodiodes in the encoder assembly. The resulting signals determine coarse track position and track crossings. Paragraph 9.7.1.5 describes the mechanical operation of the opticle scale, reticle, and photocell.

As the scale moves through the encoder gap, pseudo-sinusoidal signals are generated at P1 and P2 with a 90 degree phase difference created from the offset window the reticle provides. The infrared (IR) light that passes through the scale/reticle filter causes current to flow in the photodiode. This current varies as the amount of light detected by the photodiode varies with the movement of the scale. Current flow in the photodiode allows varying voltage into the operational amplifiers, which causes the voltage to swing proportionally at P1 and P2.

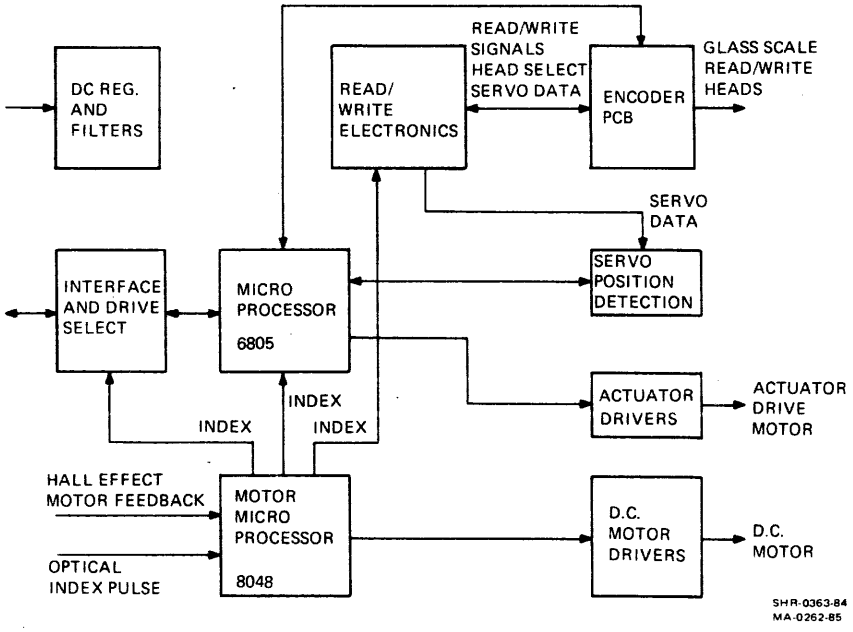


Figure 9-11 Encoder PCB Block Diagram

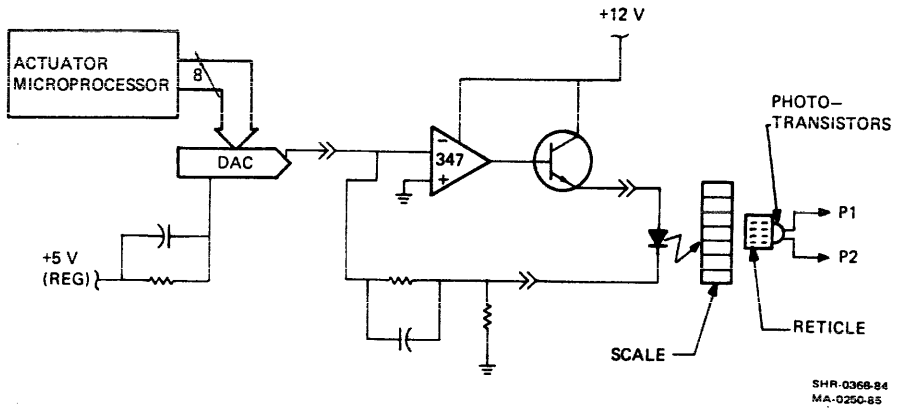


Figure 9-12 AGC Circuit

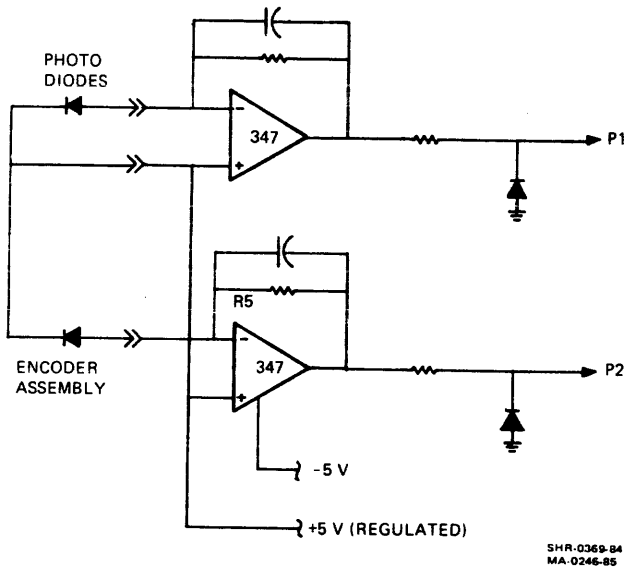


Figure 9-13 P1 and P2 Generation

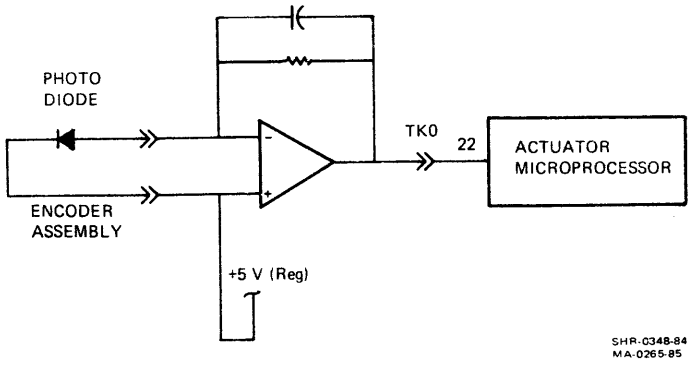


Figure 9-14 Track 0 Detector

9.8.4.3 Track 0 – A separate photocell determines track 0 in the encoder assembly. An opaque rectangle, next to the track scale, restricts LED light from the photodiode when near track 0. The phases of P1 and P2 signals determine the actual "rough" track 0 location after the track 0 flag was switched at some point within the "first" period of the P1 and P2 signals. An op amp detects the photodiode current and drives the input of the actuator microprocessor (see Figure 9-14).

Normally current flows (light enters the photodiode), which causes the output of the op amp to be low. When the light beam is broken by the track 0 area on the scale, current no longer flows and the output of the op amp is 5 V, signalling track 0.

9.8.5 Drive Control PCB

Figure 9-15 is a functional block diagram of the drive control PCB. The PCB is mounted on the bottom of the drive and connects on one end to the encoder PCB. The other end of the PCB provides edge contact fingers for control signal and data interface connectors. A connector is also provided for dc power application. The drive control PCB has two more connectors, one for the dc spindle motor, and the other for the faceplate LED.

Applying dc power to the disk drive starts the dc motor spinning after voltage levels have exceeded the minimum limit determined by the power on reset (POR) circuit. This causes the heads to lift off the disk surface and fly above the landing zone. When the motor microprocessor (via INDEX) detects the dc motor speed within 3 percent of nominal speed (3423 rpm), the motor microprocessor generates an UP TO SPEED signal to the actuator microprocessor to recall the actuator to cylinder 0. When this is done, the drive sets READY and SEEK COMPLETE at the control interface.

When DRIVE SELECT is driven true and matches the drive select jumper, the drive select logic enables the interface logic to gate control signals to and from the drive. The drive reads or writes data on the selected head at the present track, depending on the state of the WRITE GATE line.

To change the track location of the heads, the appropriate direction is selected via the direction line, and step pulses are issued. The step pulse can be sent in one of the following two modes.

Normal mode – Step pulses are sent less than every 1.5 ms.
Buffered mode – Step pulses are sent more than every 200 μs.

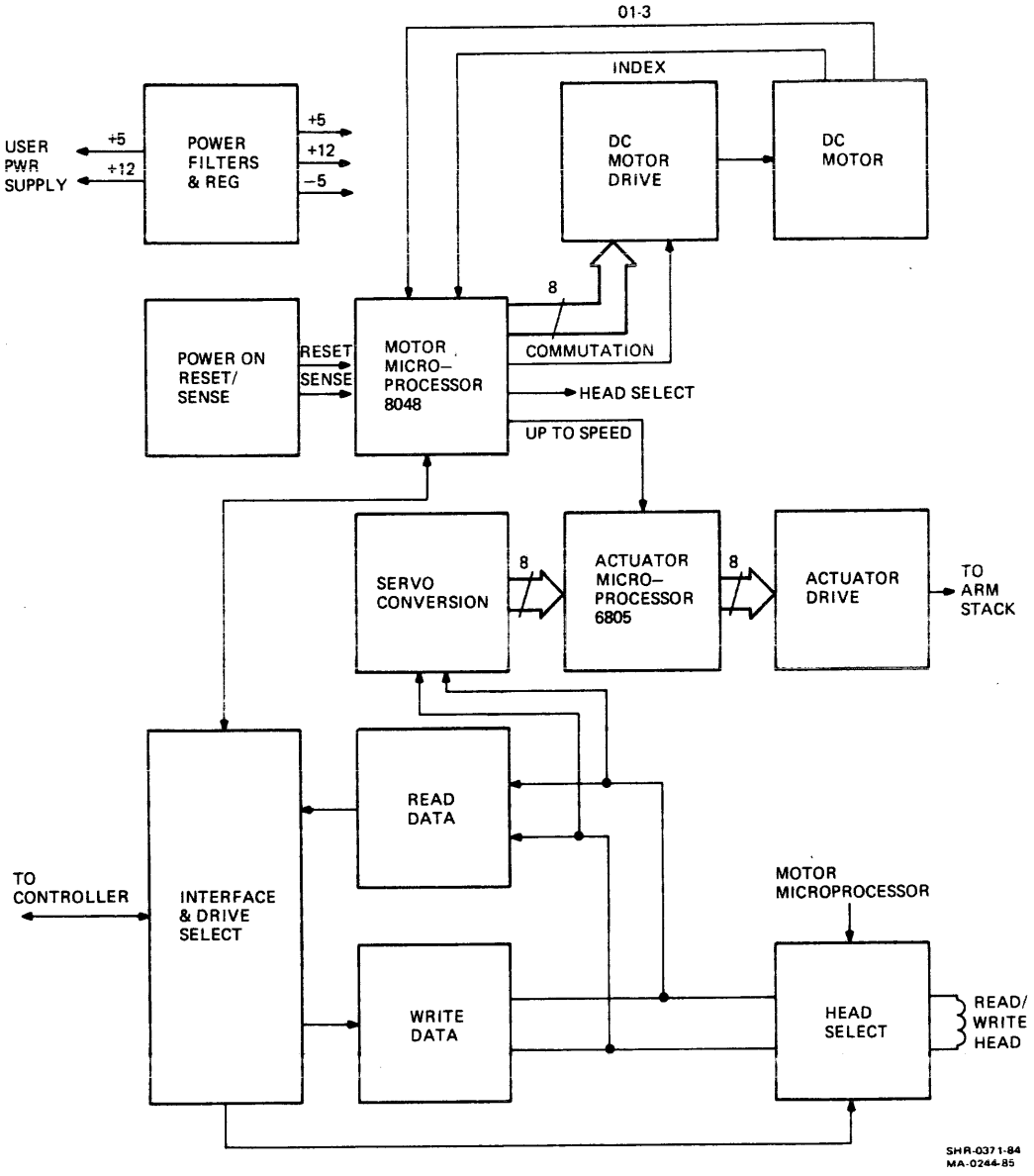


Figure 9-15 Control PCB Block Diagram

9.8.6 Actuator Positioning Circuits

9.8.6.1 Actuator Microprocessor – The actuator microprocessor is an 8-bit microcomputer with 112 bytes of RAM, timer/counter, and input/output (I/O) functions. It has 32 I/O lines, four of which are analog inputs (0–5 V). The RAM includes registers for the I/O ports and timers. It has 3.8 kilobytes of EPROM for program storage. The actuator microprocessor has 32 I/O lines, four of which can be analog inputs (0–5 V).

9.8.6.2 Recalibration – Upon power-up, the microprocessor initializes certain I/O pins, RAM locations, and interrupt lines. It then determines the phase orientation of the position signals, P1 and P2. The initial P1 and P2 values are then calibrated using their LED values. The actuator is then stepped out to track 0, which is determined by the level of the track 0 photocell and the relationship of P1 and P2. A handshake is established with the motor microprocessor for index time. The zone timers are initialized, and the zone table offsets are initialized to the present track 0 values. At this point, the control is passed to the main loop.

9.8.6.3 AGC Function – The actuator microprocessor performs the AGC function at index time and at the end of a seek. The LED values of the P1 and P2 position signals are increased or decreased based on the value (level) of the track 0 signal. The track 0 reference level is originally recorded (stored) during recalibration at about track 256. The AGC function is not used when the position signals are within four tracks of track 0.

9.8.6.4 On Track Servoing (Coarse) – The disk drive uses servoing to maintain the actuator in an on-track (stationary) position. The microprocessor controls head position by comparing the difference between the position signal voltage level (P1 or P2) and a reference value. The difference between these values is the error, and a correction value is sent to the actuator's digital to analog converter (DAC). The coarse servo loop occurs about every 150 μs, or about 100 times per revolution.

9.8.6.5 Fine Servoing – The microprocessor applies fine servo correction to the reference value in order to compensate for changes in head positioning accuracy due to thermal conditions.

Once per revolution, 290 μs prior to –INDEX, the drive peak detects and samples the factory written servo bursts. The servo bursts consist of an A and B burst placed between the data tracks on data surface 3. When reading the servo bursts (time wedge), the drive switches from the selected head to head 3 (see Paragraph 9.8.9.5 for more information about wedge and index signals). After –SEEK COMPLETE, the microprocessor limits fine servo corrections (to the reference value) to one DAC step per revolution. Before –SEEK COMPLETE, the microprocessor sends the full value required for correction.

9.8.6.6 Ramped Mode Seeking – The ramped mode is used for single step seeks and buffered seeks of 17 tracks or fewer.

In ramped mode, the actuator arm accelerates linearly until it is half the distance to its destination track. The actuator arm then decelerates linearly until it settles on the destination track. The actuator microprocessor controls positioning during a ramped mode seek by looking at the positive and negative slopes of the P1 and P2 signals.

9.8.6.7 Slew Mode Seeking – The slew mode of seeking is used for buffered seeks of 18 tracks or more. During slew mode, the actuator is accelerated to a terminal velocity. This is controlled for the first half of the seek. During the second half of the seek, the actuator is decelerated to a velocity determined by the number of "tracks to go" (number of tracks to the destination track).

If the seek length is an even number of tracks, the current position signal being servoed on, is the position signal used at the destination track. This is the same phase or plus 2 phases.

If the seek length is an odd number of tracks, position signals switch and wait for the first crossing of a switch point to decrease the number of tracks to go. This results in an even number of tracks to go. The position signal switched to, becomes the position signal used at the destination track.

9.8.7 Write Data Circuits

Figure 9-16 is a functional block diagram of the RD52-A disk drive's write circuits. The write data circuit ensures that the following conditions exist.

- The 5 V logic voltage is present.
- The disk drive is selected on track, and it is not wedge time (to prevent writing in the servo area).
- The WRITE GATE signal is active.

When these conditions exist, the write enable switch turns on the write current source.

When enabled, the write current source provides the write driver with 18 mA of write current. The write data circuit also provides a current-on signal (+IWON) used by the motor microprocessor to determine WRITE FAULT. The write driver receives its switching input from the write data receiver. The write driver applies the write current to both ends of the head coil (the head coil's center tap has been grounded by the head select switch).

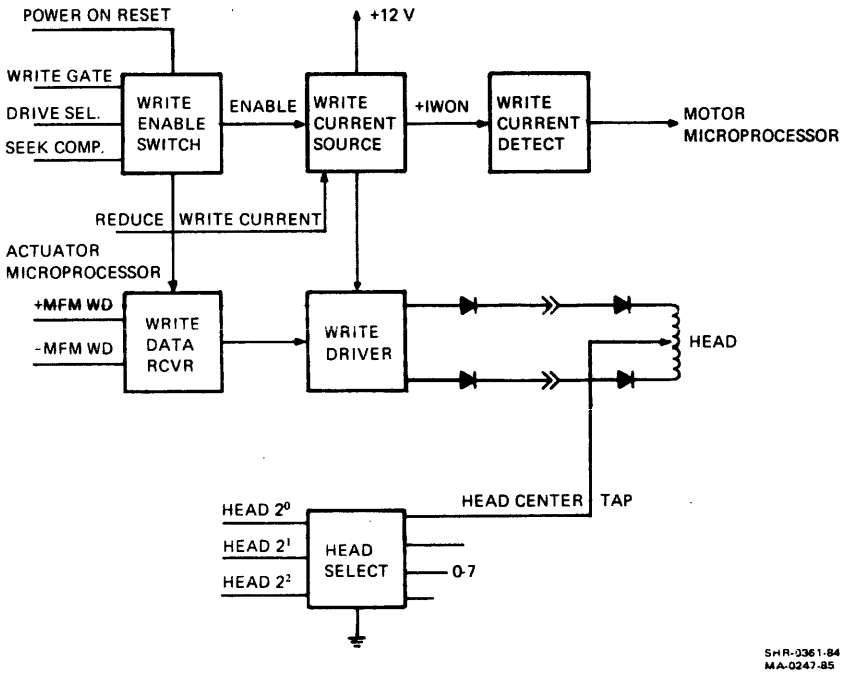


Figure 9-16 Write Circuit Block Diagram

9.8.8 Read Data Circuits

The block diagram in Figure 9-17 shows the functional areas of the RD52-A read channel. When the head select switch connects the center tap of the selected head to ground, the diodes in the head coupling network become forward biased. Magnetic flux changes passing by the head induce current into the coil. This current is coupled through the head coupling diodes and appears as small differential voltage changes at the amplifier's input. The amplifier boosts these changes that then travel through a low pass filter to eliminate unwanted high frequency noise. The signal is input to the differentiator, which converts the voltage peaks of the signal to zero voltage crossings. These zero voltage crossings represent the flux changes read from the disk. The differentiated signal passes through further low-pass filtering before being input to the zero crossing detector, where READ DATA pulses are created from the zero crossings. These READ DATA pulses are input to a line driver with differential output. The output of the line driver is the ±MFM READ DATA sent to the controller module via the 20-conductor data cable.

9.8.8.1 Low Pass Filter/Differentiator – After being amplified, the READ signal passes through some low-pass filtering before entering a differential amplifier where peaks (from flux transitions inducing head current) are converted to zero crossings.

A differential amplifier performs the differentiation and provides a voltage gain of 400. The output of the differentiator passes through two capacitors that remove the dc component from the signal. After more low-pass filtering, the signal goes to the zero crossing detector circuit.

9.8.8.2 Zero Crossing Detector – Up to this point, the read channel has detected, amplified, and filtered the flux changes recorded on the disk. It transformed the resultant voltage peaks through differentiation to zero crossings for easy detection. Now, the signal is input to a comparator, which detects the zero crossings and creates READ DATA pulses.

9.8.8.3 Droop Ignore Circuit – The droop ignore circuit prevents the pulse train from generating false data pulses due to droop. Droop is the tendency of the differentiated signal to droop toward 0 V. This may occur while the disk drive reads low frequency data patterns from the disk, and when noise or media imperfections cause the signal to cross zero between legitimate bits.

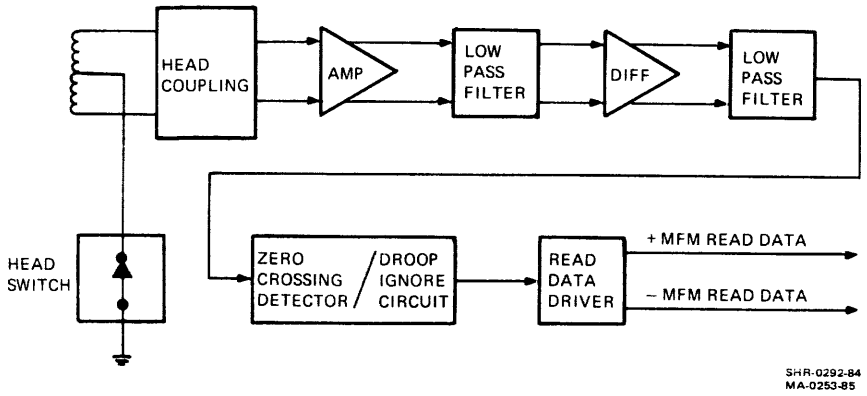


Figure 9-17 Read Circuit Block Diagram

9.8.9 Motor Microprocessor

9.8.9.1 Description – The motor microprocessor performs the following three major functions.

Motor-start and speed control
Wedge/index timing
WRITE FAULT detection

Refer to Figure 9-18 for a block diagram of the motor microprocessor. The microprocessor is an Intel 8048 8-bit microcomputer with 1 kilobyte of read-only memory (ROM), 64 bytes of RAM, 27 I/O lines, and an 8-bit timer.

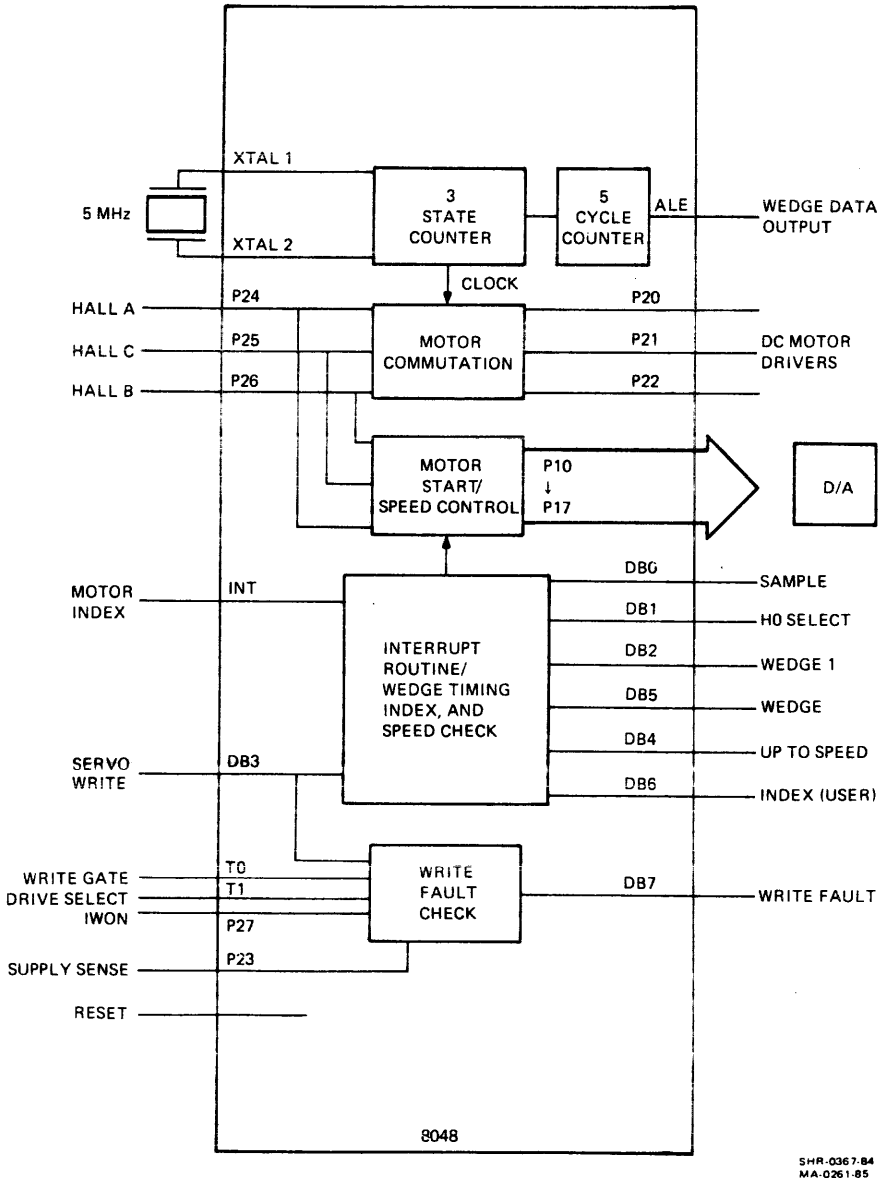


Figure 9-18 Motor Microprocessor

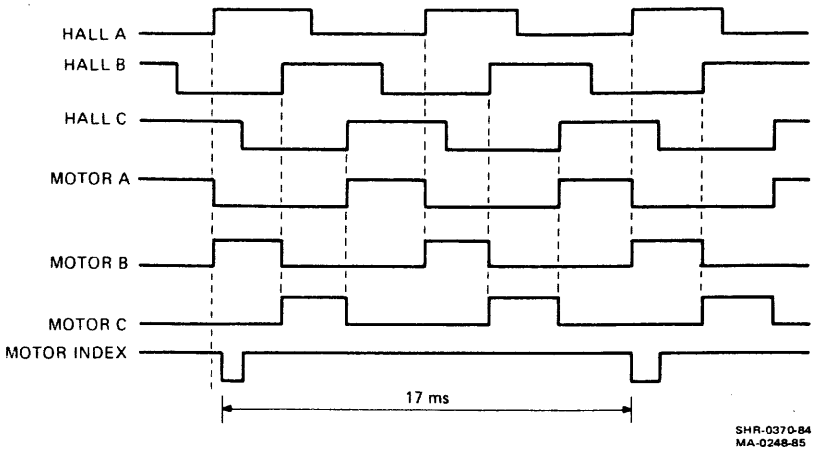


Figure 9-19 DC Motor Commutation Timing Diagram

9.8.9.2 DC Motor Control – The motor subassembly uses three signals to provide information to the microprocessor about the motor's rotor position. As the motor rotates, the rotor magnets pass by hall effect devices whose output is shaped by a comparator circuit (on the motor subassembly PCB). The three position signals generated by the hall effects are sent directly to the microprocessor and are continually monitored. When the motor changes position, the microprocessor changes the state of the three output signals accordingly to switch current through one of the three stator windings. Figure 9-19 shows the commutation timing for this sequence.

9.8.9.3 Motor Current – The position sensing subroutine controls the coil to which current is applied. The microprocessor determines the amount of current by sending an 8-bit word to a DAC. In this way the microprocessor selects the motor current as one of 256 values.

The microprocessor controls the motor current in the following two modes.

Start-up mode
Locked-on mode

Start-up Mode

Start-up mode is essentially open loop. Once dc power is up and the microprocessor is initialized, the hall signals are checked for motor movement. If no hall change occurs, the motor is not moving and program execution jumps to the beginning of the motor-start routine. If a hall change does occur, the microprocessor does a timing calculation to determine where to enter the motor-start routine. The microprocessor checks for hall changes to prevent over accelerating a rotating motor.

Current is applied in decreasing steps during the motor-start routine. A stationary motor begins at a maximum current of 3.75 A for one second. The microprocessor checks hall states and monitors commutation. If no hall change occurs, current is shut off for one second to allow the drivers to cool. The microprocessor repeats this sequence up to four times if the motor does not move. After the fifth try, the microprocessor aborts and lies idle, waiting for a reset (POR) signal.

Normally, after initial current is applied, the following sequence occurs.

3.5 A for 2 s
3.0 A for 2 s
2.5 A for 40 s (maximum)

While the above currents are applied, the microprocessor checks speed every tenth of a second in the commutation loop. When the speed is sufficient, (36 hall changes have occurred in 0.1 s), program execution transfers to the main loop. If nominal speed is not reached after 40 seconds, the microprocessor aborts and lies idle, waiting for a reset (POR) signal.

Locked-on Mode

The locked-on mode occurs as program control transfers from the motor-start routine to the main loop. At the same time, the program control checks the states of the hall signals and enters the main loop at the appropriate place. A 2-byte register counts instruction cycles between INDEX pulses to measure speed. When a hall change occurs, the program does commutation and jumps to the WRITE FAULT subroutine.

Once per motor revolution an INDEX pulse causes an interrupt routine execution. At this time, the wedge protect and index timing occur. The last part of the interrupt routine determines the motor current.

The speed count registers are now checked. The INDEX period (motor speed) must be ±3 percent of nominal speed (17 ms) for more than two seconds for the UP-TO-SPEED line to register true or false. This line resets the actuator microprocessor (if false), which causes READY to go false.

Next, the microprocessor performs an algorithm on the speed count error to calculate the value for output to the DAC. This sets the motor current for the next revolution (2 A, maximum). Control is returned to the main loop from the interrupt routine after the current value is sent and speed count registers reset.

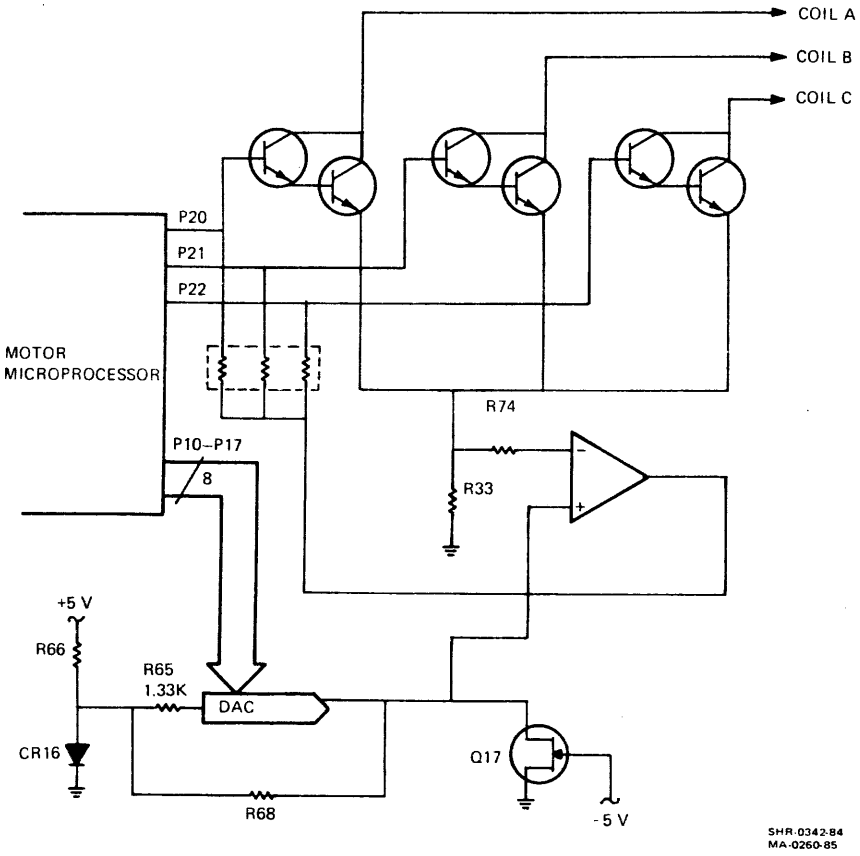


Figure 9-20 DC Motor Drive Circuit (Simplified)

9.8.9.4 DC Motor Drive Circuit – Figure 9-20 is a schematic diagram of the drive circuit. R66 and CR16 provide a reference voltage of 0.8 V across R65, which gives the DAC its reference current of 0.6 mA. R68 creates an output voltage which is sent to the op amp. When the DAC input from the microprocessor is 00 (hexadecimal), no current flows, so the output voltage (op amp input) is 0.8 V. With FF (hexadecimal) at the DAC input, full scale current flows through R68; this sets the op amp input at 0 V. The op amp maintains the DAC voltage across R33; thus, the microprocessor can set the motor current from 0 to 4 A in 256 steps.

Transistor Q17 clamps the DAC output to ground while the dc power supplies are rising. Signals at P20, 21, and 22 from the microprocessor are the commutation switches that send base current to one of the three Darlington transistors. These transistors sink current through their respective motor winding.

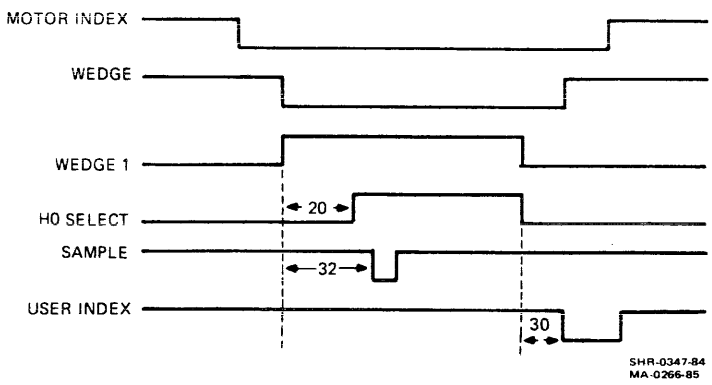


Figure 9-21 Wedge and Index Timing

9.8.9.5 WEDGE and INDEX Signals – The motor microprocessor software generates wedge timing. Beginning with an INDEX pulse (causing execution of the interrupt routine), the microprocessor generates three signals: WEDGE, WEDGE1, and H0 SELECT (see Figure 9-21). These signals disable the write drivers and the head select IC, and select the servo head's center tap. Another signal sent by the microprocessor, SAMPLE, causes the actuator microprocessor to begin reading servo data. WEDGE1 and H0 SELECT then go inactive, which re-enables head select control to the interface. After a 30 μs delay to allow for head switch settling, USER INDEX is sent to the interface.

9.8.9.6 WRITE FAULT – After each motor commutation in the main loop, the microprocessor performs a WRITE FAULT check (six times per revolution). At the beginning of the WRITE FAULT subroutine, a flag is cleared that becomes set if an interrupt (INDEX) occurs. This flag is checked at the end of the subroutine if a WRITE FAULT was determined. If the flag was set, the WRITE FAULT signal is considered invalid and is ignored. Execution then returns to the main loop.

To determine a WRITE FAULT, the program first determines the states of the –WRITE GATE and +IWON (Write Current On) signals. Next, SUPPLY SENSE is checked for dc voltage levels. If the 5 V is 9 percent low or the 12 V is 20 percent low, the SUPPLY SENSE signal is low, which causes a WRITE FAULT. If –WRITE GATE was determined high, and +IWON was determined low, no fault occurs and the program returns to the main loop. With the +IWON signal high, the program rechecks –WRITE GATE, allowing for a single transition during the signal polling before issuing a WRITE FAULT signal.

9.8.9.7 Power Faults – When the RD52-A senses a power fault (no power or out of specification), all power is removed from the rotary positioner and the spindle motor to protect the recorded data.

There is a return spring on the positioner that forces the head stack into the landing zone (the innermost area of the disks) whenever power is removed.

Removing power from the spindle motor causes the disks to stop rotating. As the disk rotation decreases, the airflow generated by the disk rotation also decreases. This loss of airflow causes the automatic actuator lock (AIRLOCK) to lock the head stack in the landing zone (see Paragraph 9.7.1.7 for more information about the AIRLOCK).

9.9 INTERFACE

The RD52-A uses two interface cables: a control cable and a signal or data cable. All control signals are digital (open collector TTL) and are relayed between the drive and host controller via connector J1. The data transfer signals are differential and relayed via connector J2. DRIVE SELECTED is a digital signal but is also transmitted via J2. DC power is relayed via connector J3. For more information about connector J3, see Paragraph 9.6.3.

The RD52-A has two interface connectors: one for control signals (J1) and one for data transfer signals (J2). Paragraphs 9.9.1.1 through 9.9.2.3 describe the signals, timing requirements, and interface cables associated with the two interface connectors. These paragraphs also describe the characteristics of the receiver/driver combinations used. Figure 9-22 shows the location of these two connectors.

Connection to J1 is through a 34-pin PCB edge connector. Figure 9-23 shows the connector's dimensions. The pins are numbered 1 through 34. The even pins are on the PCB's component side and the add pins are on the PCB's solder side. Pin 2 , which is labeled, is on the end of the PCB connector closest to the dc connector. A key slot is provided between pins 4 and 6. The recommended mating connector for P1 is AMP ribbon connector PN 88373-3.

Connection to J2 is through a 20-pin PCB edge connector. Figure 9-24 shows the connector's dimensions. The pins are numbered 1 through 20, with the even pins on the PCB's component side. The recommended mating connector for P2 is AMP ribbon connector PN 88373-6. A key slot is provided between pins 4 and 6.

9.9.1 Control Signal Interface

9.9.1.1 General Description – The control signals are both input (those originating outside the drive), and output (those originating within the drive). One type of control signal can be multiplexed in a multi-drive system. The other type of control signal can do the multiplexing. The control signals that do the multiplexing are DRIVE SELECT 1, DRIVE SELECT 2, DRIVE SELECT 3, and DRIVE SELECT 4, which are input signals. The input multiplexed signals are STEP, DIRECTION, HEAD SELECT 2^0, HEAD SELECT 2^1, HEAD SELECT 2^2, and WRITE GATE. The output multiplexed signals are TRACK 000, INDEX, READY, WRITE FAULT, and SEEK COMPLETE output signals. Up to four drives can be connected in a daisychain configuration that uses a single control signal cable. The last drive in the chain requires the terminator to be installed at PCB location RN36 (see Paragraph 9.8.1.2).

The output lines are driven with a TTL open collector output stage that can sink a maximum of 40 mA at the logic 0 (true) state, with a maximum voltage of 0.4 Vdc measured at the driver. When the line driver is in the logic 1 (false) state, the driver transistor is off and the collector cutoff current is 250 μA.

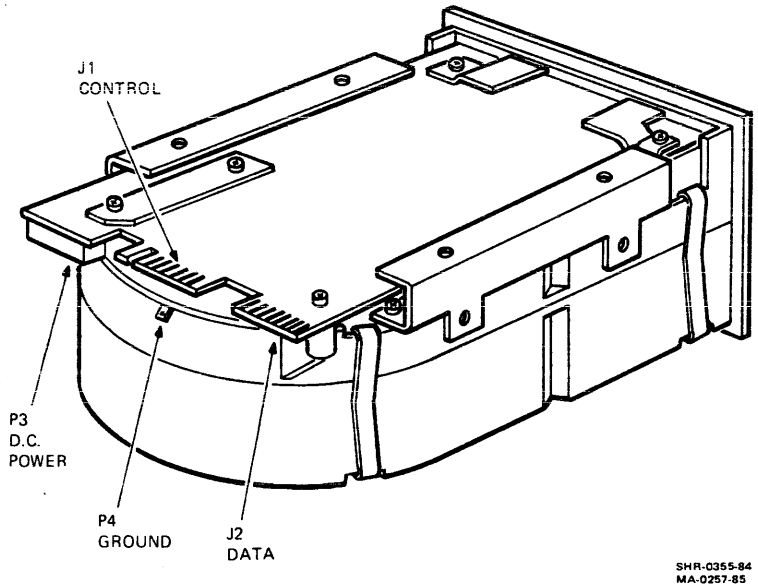


Figure 9-22 Interface Connectors

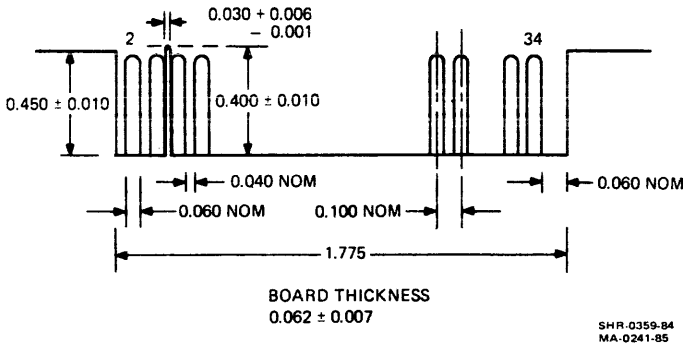


Figure 9-23 J1 Connector

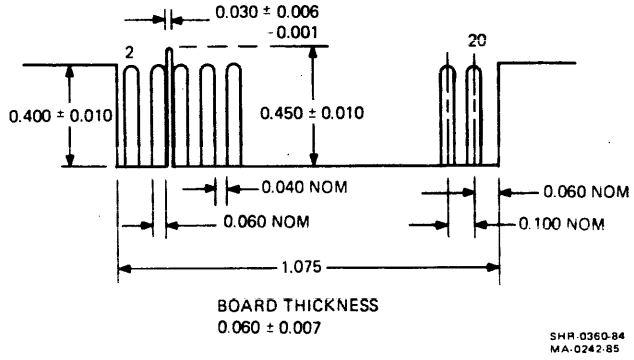


Figure 9-24 J2 Connector

9.9.1.2 Driver/Receiver – Figure 9-25 shows the recommended control signal driver/receiver combination. The maximum recommended cable length is 6 m (20 ft). Table 9-3 shows the control cable's pin designations.

9.9.1.3 Control Signal Descriptions – Unless stated otherwise, all control signals are enabled/gated with DRIVE SELECT. The function of each control signal is described as follows.

Input Signals

- –DRIVE SELECT 1, 2, 3, or 4
  A low level on one of these lines logically connects the selected drive to the control lines. Only one drive select line may be active at a time, and it selects the drive that has the matching drive select jumper installed.

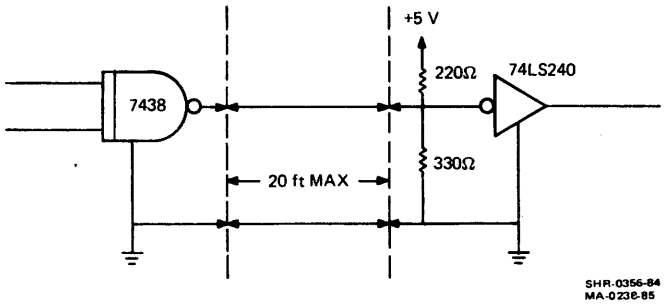


Figure 9-25 Control Signal Driver/Receiver

Table 9-3 Control Cable Pin Designations

Ground Return	Signal Pin	Signal Name
1	2	–N/A (reduced write current done automatically by microprocessor)
3	4	–HEAD SELECT 22
5	6	–WRITE GATE
7	8	–SEEK COMPLETE
9	10	–TRACK 0
11	12	–WRITE FAULT
13	14	–HEAD SELECT 2^0
15	16	–Reserved (to J2 Pin 7)
17	18	–HEAD SELECT 2^1
19	20	–INDEX
21	22	–READY
23	24	–STEP
25	26	–DRIVE SELECT 1
27	28	–DRIVE SELECT 2
29	30	–DRIVE SELECT 3
31	32	–DRIVE SELECT 4
33	34	–DIRECTION IN

- –DIRECTION IN
  A low level on this line defines the read/write head motion as in (toward the center of the disk away from track 0). A high level on this line defines the read/write head motion as out (toward the edge of the disk near track 0). Motion occurs with the receipt of a step pulse.

- –STEP
  A low pulse, at least 1.5 μs long, on this line causes the read/write head to move in the direction defined by the DIRECTION IN line. If STEP pulses occur at a rate equal to or greater than 1.5 ms between pulses, the heads move at the rate of the incoming steps (single step mode). If the incoming STEP pulse rate is equal to or less than 200 μs between pulses, the pulses are buffered into a counter. Motion occurs after the last STEP pulse is received (buffered step mode). See Figures 9-26 and 9-27 for step timing.

- –HEAD SELECT 20, 21, and 22
  These three lines provide a binary code to select one of the heads. The least significant bit is 20 and the heads are numbered 0 through 7. When all lines are low, head 7 is selected. Conversely, if all lines are high, head 0 is selected.

- –WRITE GATE
  A low level enables write data to be written on the disk.

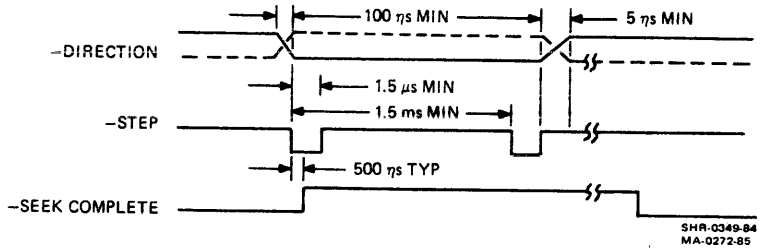


Figure 9-26 Single Step Mode Timing

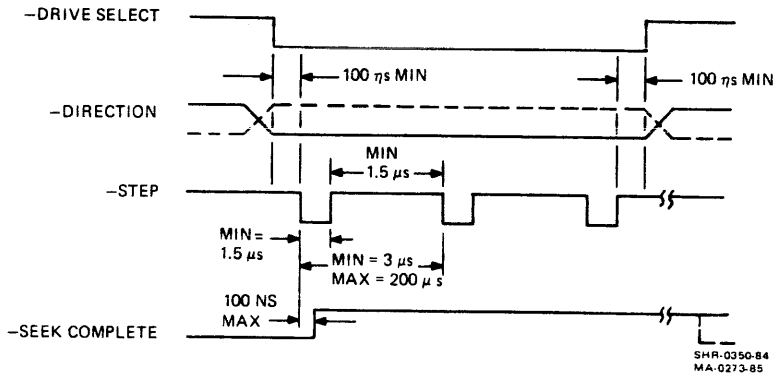


Figure 9-27 Buffered Step Mode Timing

Output Signals

- –TRACK 000
  A low level on this line shows that the read/write heads are at cylinder 0 (the outermost cylinder).

- –INDEX
  A low pulse of 50 μs on this line indicates the beginning of a track. The leading edge of this pulse must be used for all timing requirements. The pulse occurs once each revolution or every 17.00 μs. Figure 9-28 shows the index timing.

- –READY
  A low level on this line shows that the drive is up to speed and the interface signals are valid. When READY and SEEK COMPLETE are true, the drive is ready to read, write, or seek.

- –WRITE FAULT
  A low level on this line indicates:

  A drive is selected, WRITE GATE is true, and there is no write current.
  There is write current, but no WRITE GATE or DRIVE SELECTED.
  DC voltages are out of specification.

  –WRITE FAULT can be reset through the interface by deselecting and reselecting the drive, or by cycling power off and on after WRITE FAULT clears.

- –SEEK COMPLETE
  A low level on this line shows that the read/write heads have settled on a cylinder, and that a read, write, or another seek may occur. Writing is inhibited while this signal is false (high).

Figure 9-29 shows the general timing relationships between some of the control signals found in the RD52-A during the drive's power on and off cycle.

9.9.2 Data Signal Interface

9.9.2.1 General Description – Three signals are on the data interface cable. None of these signals are multiplexed. Two of the signals are differential in nature, MFM WRITE DATA (input) and MFM READ DATA (output). The other signal, DRIVE SELECTED, is a TTL open collector output.

9.9.2.2 Driver/Receiver – Figure 9-30 shows the recommended differential data signal driver/receiver combination. The maximum recommended cable length is 6 m (20 ft). Table 9-4 shows pin designations for the data cable.

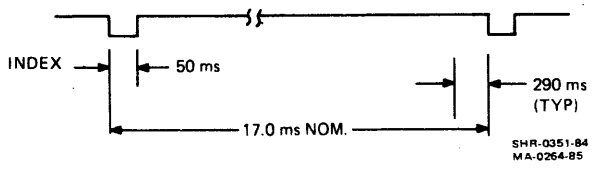


Figure 9-28 Index Timing

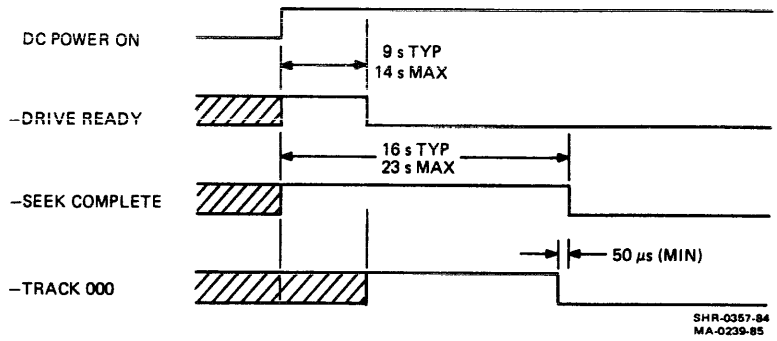


Figure 9-29 General Control Timing

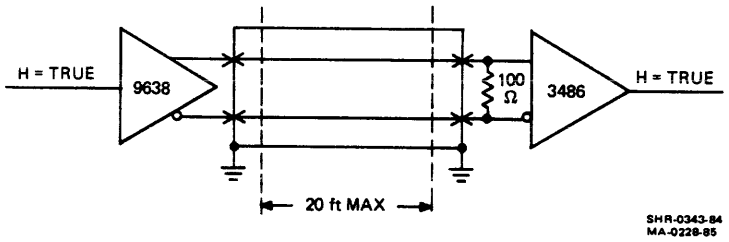


Figure 9-30 Data Signal Driver/Receiver

Table 9-4 Data Cable Pin Designations

Ground Return	Signal Pin	Signal Name
2	1	– DRIVE SELECTED
4	3	– NA
6	5	– NA
	7	– Reserved (to J1 pin 16)
8		
	9	– NA
	10	– NA
11		
12		
	13	+ MFM WRITE DATA
	14	– MFM WRITE DATA
15		
16		
	17	+ MFM READ DATA
	18	– MFM READ DATA
19		
20		

9.9.2.3 Data Signal Descriptions – The function of each data signal is described as follows.

- ±MFM WRITE DATA
  If there is a low level on the –WRITE GATE control line, the transition of the +MFM WRITE DATA line more positive than –MFM WRITE DATA causes a flux reversal to be written on the disk. Figure 9-31 shows the write data timing.

- ±MFM READ DATA
  If there is a high level on the WRITE GATE control line, the transition of the +MFM READ DATA line more positive than –MFM READ DATA shows that a flux reversal was detected on the track. Figure 9-32 shows the read data timing.

- –DRIVE SELECTED
  This open collector line goes low when the drive is selected by the appropriate drive select line.

9.10 RD52-A (30-23227-02) DISK DRIVE

There are two disk drive systems named RD52-A. Refer to Paragraph 9.3 to determine which RD52-A you have. Paragraphs 9.10 through 9.13 are a technical description of the RD52-A with PN 30-23227-02 (Figure 9-33).

Paragraph 9.10.1 through 9.10.3 give a brief overview of the RD52-A, specifications, and external power requirements. Paragraph 9.1 is a physical description of the drive. Paragraph 9.12 describes operator functions and theory of operation. Paragraph 9.13 describes the two interface connectors (control and data) and gives connector dimensions, pin assignments, signal descriptions, and the recommended driver/receiver combinations.

9.10.1 General

The RD52-A is a Winchester technology random access storage device that uses four nonremovable disks as storage media. Each disk surface uses one movable head to service its data tracks. The RD52-A uses a closed-loop servo system. The bottom surface of the lowest disk is dedicated to continuous servo positioning data.

The RD52-A does not need preventive maintenance or field adjustments. Check your specific system documentation for installation, removal and maintenance information.

9.10.2 Specifications

9.10.2.1 Physical Specifications

Environmental Limits

	Operating	**Non-operating**
Ambient temperature	10° to 50°C (50° to 122°F)	–40° to 66°C (–40° to 151°F)
Ambient relative humidity	8% to 80%	8% to 95%
Altitude	2.4 km (8000 ft)	9.1 km (30,000 ft)

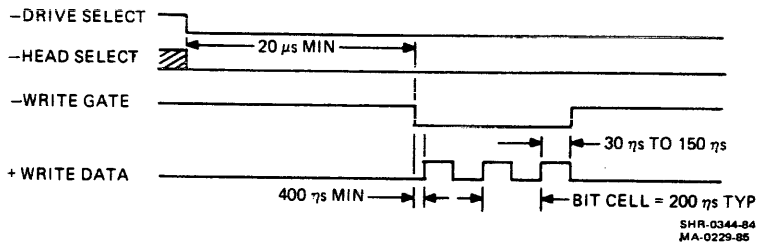


Figure 9-31 MFM Write Data Timing

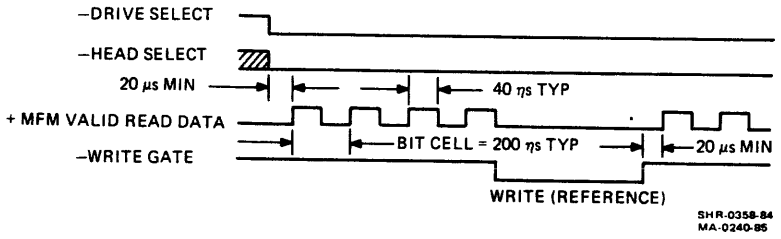


Figure 9-32 MFM Read Data Timing

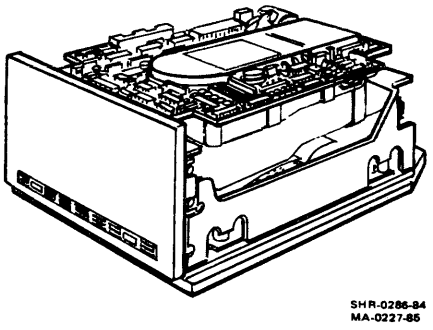


Figure 9-33 The RD52-A Disk Drive (30-23227-02)

Mechanical Dimensions

Height	8.25 cm (3.25 in)
Width	14.6 cm (5.75 in)
Depth	20.32 cm (8.00 in)
Weight	3.15 kg (7 lb)

Heat Dissipation

35 W (119 Btu/hr) typical
43.5 W (148 Btu/hr) maximum

Shock and Vibration

	Operating	**Nonoperating**
Shock	3 G x and z axes 0.8 G Y axis	30 G
Vibration	0.5 G at 10 – 500 Hz 0.1 inch at 2 – 10 Hz	2 G at 10 – 500 Hz 0.3 inch at 2 – 10 Hz

9.10.2.2 Performance Specifications

Capacity (unformatted)

Per drive (megabytes)	47.02
Per surface (megabytes)	6.61
Per Track (bytes)	10,416

Access Times (including head settling)

Track to track	6 ms
Average	33 ms
Full stroke	60 ms
Average latency	8.33 ms

9.10.2.3 Functional Specifications

Nominal rotating speed (rpm)	3600
Maximum rotating speed (rpm)	3636
Minimum rotating speed (rpm)	3564
Maximum recording density (bits/in)	8780
Maximum flux density (flux changes/in)	8780
Track density (tracks/in)	800
Cylinders	645
Tracks	4515
Read/write heads	7
Disks	4
Index	1

9.10.3 Power Requirements

9.10.3.1 DC Power – The voltages required to operate the drive are +5 Vdc and +12 Vdc. Figures 9-34 and 9-35 show the current requirements in more detail.

9.10.3.2 DC Power Connector – The dc power connector (J3) is a 4-pin AMP Mate-N-Lock connector (AMP PN 350211-1) on the component side of the bottom PCB. You can access this connector from the back of the drive. Digital recommends that you make the dc power connector with AMP PN 1-480424-0. Figure 9-36 shows the dc power connector pins.

VOLTAGE	MAX START	TYP START	MAX SEEK-ING	TYP SEEK-ING	MAX STEADY STATE	TYP STEADY STATE	MAX RIPPLE P-P
+5	1.5 AMP	1 AMP	1.5 AMP	1 AMP	1.5 AMP	1 AMP	50 mV
+12	4.5 AMP	3.8 AMP	3 AMP	2.5 AMP	2 AMP	1.5 AMP	50 mV

SHR-0362-84
MA-0225-85

Figure 9-34 Current Requirements

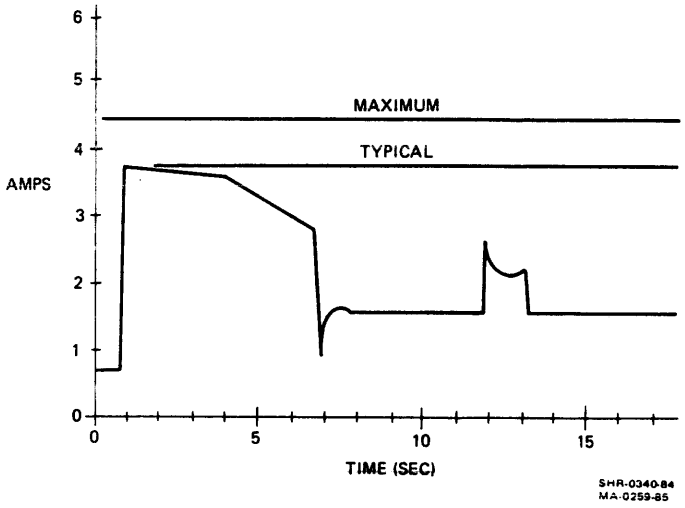


Figure 9-35 +12 V Startup Current

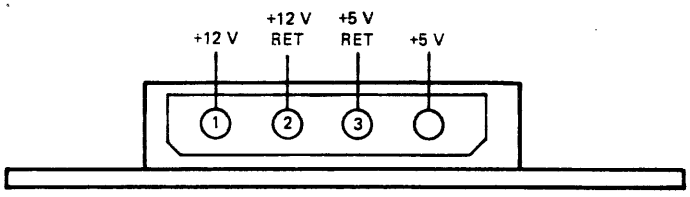


Figure 9-36 J3 Connector Layout

9.11 PHYSICAL DESCRIPTION

9.11.1 Assemblies

The RD52-A disk drive has the following six major assemblies.

Read/write interface PCB
Spindle/EMA drive PCB
Servo control PCB
Spindle drive mechanism
Positioning mechanism
Read/write heads and media

These assemblies are shown in Figure 9-37 and described in the following paragraphs.

9.11.1.1 Read/Write Interface PCB – The read/write interface PCB, to which all power, control and data signals are connected, provides the following functions.

- Receives power and regulates internal voltage
- Controls INPUT signal reception and internal distribution
- Controls OUTPUT signal accumulation, sequencing, and transmission
- Controls READ/WRITE signal bidirectional reception, conditioning and transmission
- Detects fault and generates Fault signals.

9.11.1.2 Spindle/EMA Drive PCB – The spindle/EMA drive PCB has a dedicated microcomputer and is mounted to the bottom of the sealed mechanical enclosure. This PDB derives its power from the read/write interface PCB and provides the following functions.

Power and speed control to the spindle drive motor
Power drive to the electromagnetic actuator (EMA)

9.11.1.3 Servo Control PCB – The servo control PCB has a dedicated microcomputer and is mounted to the top cover of the sealed mechanical enclosure. The servo control PCB provides the following functions.

- Controls and monitors signal sequencing during the power-up operation
- Receives the servo data that is read from the dedicated servo disk surface by the servo head
- Conditions the servo data and generates position signals
- Distinguishes between single and buffered step mode seeks, then for buffered step mode seeks, generates, detects, and controls the carriage velocity to ensure arrival at the desired cylinder
- Controls continuous position while on track

9.11.1.4 Spindle Drive Mechanism – A brushless dc spindle drive motor rotates the spindle at 3600 rpm (±1 percent). The motor is thermally isolated from the baseplate to minimize temperature transfer. The motor, spindle, and disk stack are dynamically balanced to eliminate vibration. A dedicated microcomputer provides complete control over the spindle rotation, and allows algorithm control of the motor start and stop.

9.11.1.5 Positioning Mechanism – The read/write heads are mounted on a ballbearing-supported linear carriage. The carriage is positioned by a linear voice coil motor and driven by the closed loop servo system.

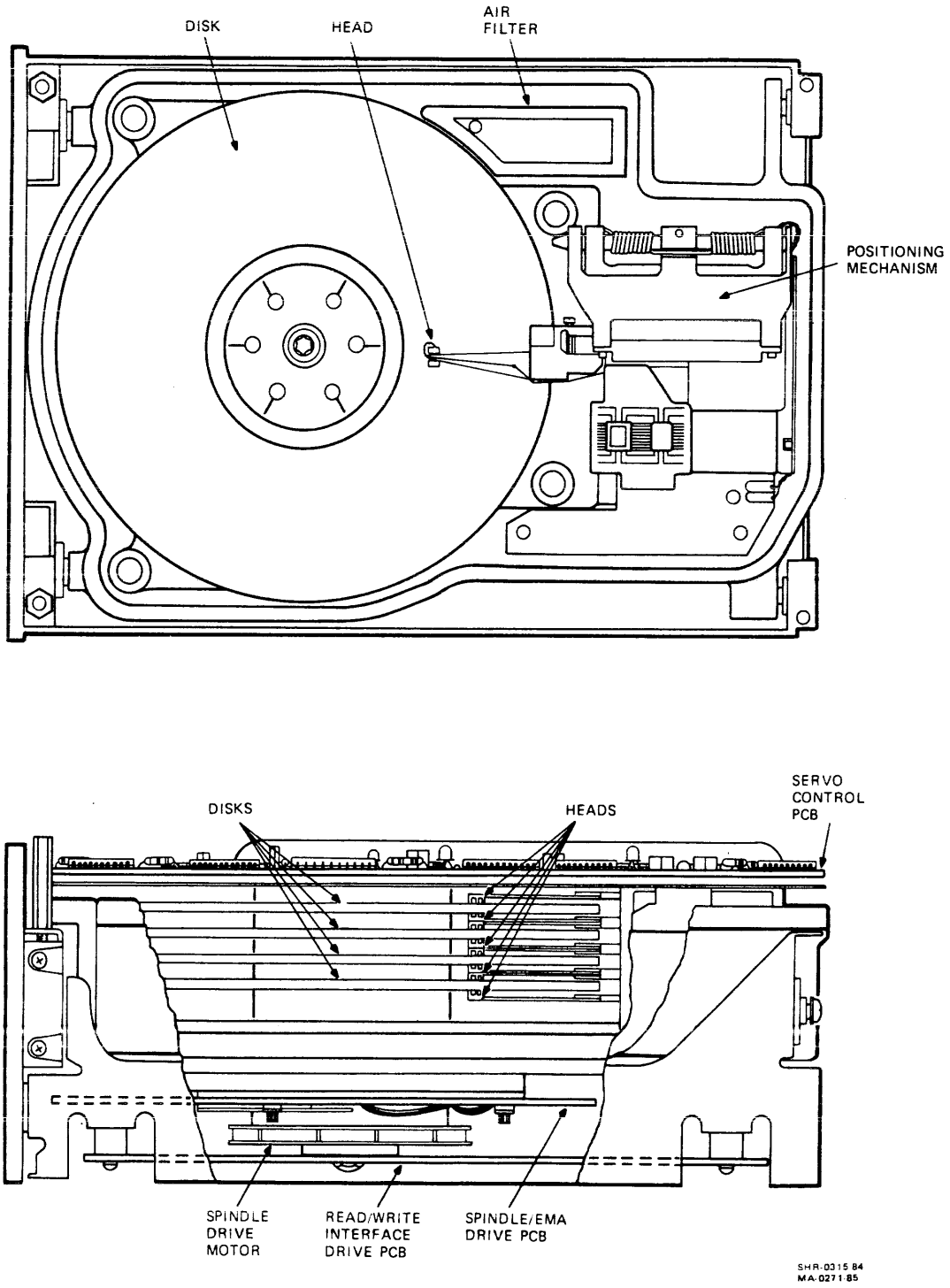


Figure 9-37 RD52-A Motor Assemblies

9.11.1.6 Read/Write Heads and Media – The recording media consists of a lubricated thin magnetic oxide coating on a 130 mm diameter aluminum substrate. This coating formulation, with the low load force/low mass Winchester type heads, ensure reliable contact start/stop operations. Data on each of the eight data surfaces (two surfaces per disk) is read or written by one read/write head. Each head accesses 645 data cylinders.

9.11.2 Air Filtration System

The disks and read/write heads are enclosed in a contamination-free mechanical enclosure. The RD52-A uses an integral recirculating air system with an absolute filter (Figure 9-37) to maintain a clean environment. The filter has a port that permits pressure equalization with the ambient air.

9.12 OPERATION

9.12.1 Operator Functions

Operator functions vary depending on the system in which the RD52-A is installed. The information in this subsection describes how the operator can select drives and terminate the control cable. Figure 9-38 shows the location of the drive select jumpers and the terminator on the read/write interface PCB.

9.12.1.1 Drive Select – Five jumpers are provided for logical drive number assignment. Drive select 1, 2, 3, and 4 cause the drive to be selected when the active drive select line matches the installed number. When installed, jumper R (radial) causes the drive to be selected constantly. The R jumper option is never used in Digital applications.

9.12.1.2 Control Cable Termination – If the RD52-A is the last drive at the end of the control signal cable, a 220/330 ohm terminator resistor pack must be installed. This terminator must be removed if the drive is not the last in a string of drives. In Digital applications, the terminator pack is always installed.

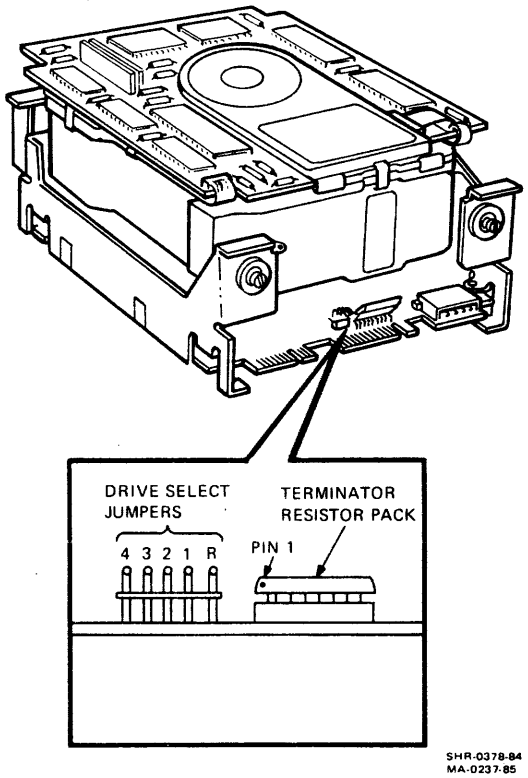


Figure 9-38 Jumper/Terminator Locations

9.12.2 Drive Organization

Figure 9-39 is a block diagram of the RD52-A. Paragraphs 9.12.3 through 9.12.9 describe RD52-A operation.

9.12.3 Power Sequencing

The +5 Vdc and +12 Vdc power can be applied in any order. The +12 Vdc must be applied to start the spindle drive motor. A microcomputer monitors the disk rotation. When the disks are spinning at 3600 rpm (±1 percent), the heads automatically recalibrate to track 0. When the heads arrive at track 0, the –TRACK 000 signal is activated. The –TRACK 000 signal precedes the –READY and –SEEK COMPLETE signals by less than 30 μs. The –READY signal is not activated if there is a fault condition. The drive can perform read, write, or seek operations only if the –READY signal is active.

9.12.4 Microprocessor Wake-Up Timing

9.12.4.1 Spindle Open Loop Acceleration Ramp – The RD52-A acceleration time (nominal) is about 10 seconds. The spindle accelerates in current limit, which is 3.5 A (see Figure 9-35).

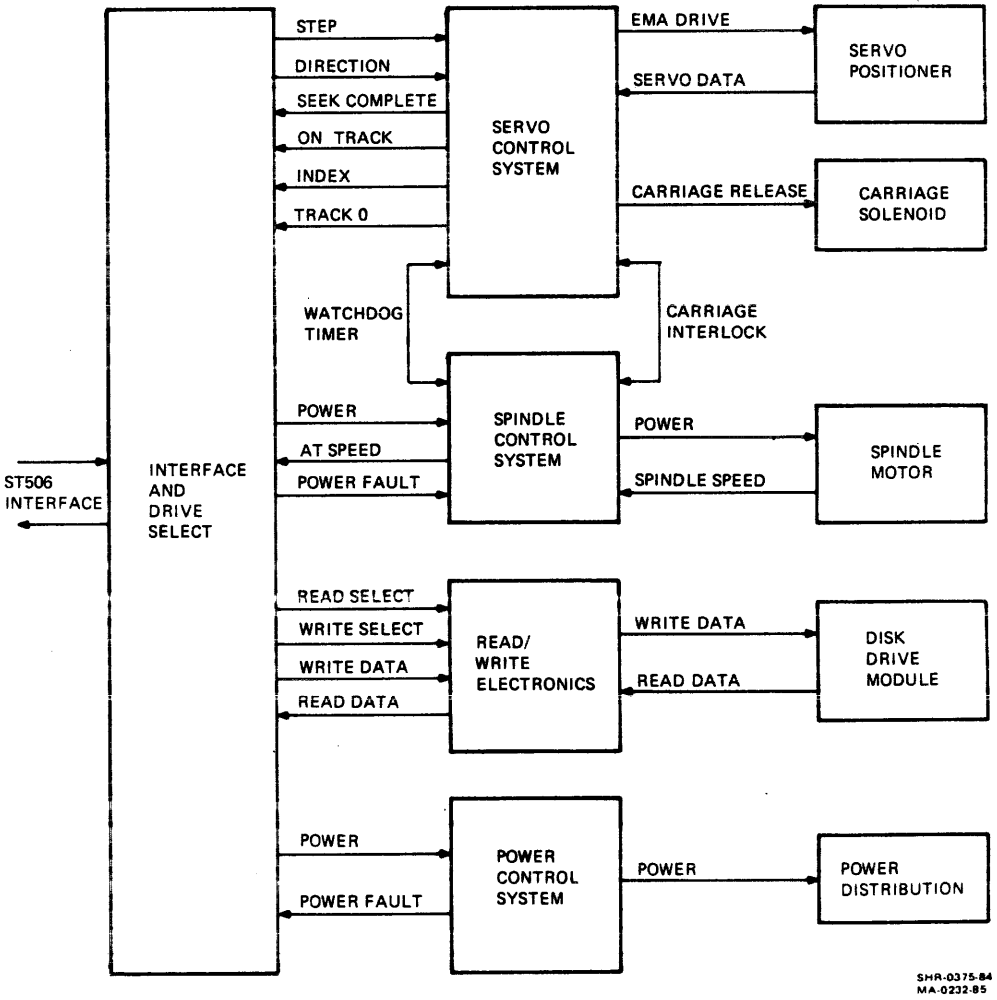


Figure 9-39 RD52-A Block Diagram

9.12.4.2 Spindle Driver – The spindle driver is a unipolar, 3-phase drive. The motor windings are connected in a Y configuration with the centertap connected to +12 Vdc.

9.12.4.3 Servo Control of the Spindle – Servo control of the spindle speed is done by integrating the speed error over time, and applying a correction factor to the spindle speed to keep the speed constant.

A timer initializes at the same point in each revolution. Since the timer runs independent of the program that runs the motor, it is used as a speed-checking device. If the timer is not at the correct value, the speed of the spindle is too fast or too slow.

A first check is made to see if the timer is within a certain range of values. If it is out of range, then a gross adjustment is made to the pulse size to correct the condition (the pulse width is set to maximum or minimum according to the condition). If the timer is within the correct range, the value is stored for later use. This value is checked to find out if the speed correction is positive (speed up) or negative (slow down).

The speed correction is done in the integrator part of the software.

The integrator does a repetitive summation of spindle-speed errors over time. The integrator works as follows.

1. If the speed error is a positive value and the previous value is positive, the two values are added and a positive limit check is done. If the sum is greater than the maximum, the maximum value is used.

2. If the speed error is positive and the previous value is negative, or the speed error is negative and the previous error is positive, the two values are added. The sum is the value used for the next revolution.

3. If the speed error is negative and the previous value is negative, the two values are added. The result is checked to see that the sum is not less than the minimum value. If the sum is less than the minimum, the minimum value is used.

The integrator causes the spindle to seek to 3600 rpm (the speed error value is 0 at this speed). The actual speed is determined by the accuracy of the microcomputer crystal and the resolution of the timer.

The spindle motor does not report ATSPEED until the spindle enters the servo state and goes through 256 revolutions.

The spindle microcomputer has only one interrupt. This interrupt is related to the watch-dog inhibitor.

9.12.4.4 Watch-Dog Inhibitor – The watch-dog inhibitor is a safety device that monitors communications between the servo microcomputer and the spindle microcomputer. Whenever a watch-dog pulse is received from the servo processor, the spindle processor is interrupted. The interrupt subroutine in the spindle processor reloads a register with a predefined value. This register is decremented with each spindle revolution. If the register is decremented to zero before it gets reloaded, a watch-dog time-out pulse is sent back to the servo processor, which causes the servo processor to restart.

The watch-dog software in the spindle processor acts like a one-shot to the servo processor. If the servo processor hangs up, it cannot send watch-dog pulses to the spindle processor. The watch-dog time-out then causes the servo processor to restart.

9.12.4.5 Actuator Disabling – The electromagnetic actuator (EMA) can be disabled by three different methods.

Servo position circuitry
Output line on the spindle microcomputer
Circuitry on the spindle/EMA PCB

Whenever it leaves the servo state, the spindle microcomputer disables the EMA. The circuitry on the spindle/EMA PCB also disables the EMA whenever a loss of +12 Vdc occurs on that PCB. When the +12 V loss occurs, the EMA is disabled and EMA retract is activated. The carriage is then retracted and latched, and read/write heads cannot move.

9.12.4.6 Carriage Latch Release – Applying 24 V to the carriage latch releases the latch. The latch release can be inhibited by pulling low the carriage latch control signal (C/L INHIBIT).

The high voltage necessary for the carriage latch (+24 Vdc) is produced by using the back electromagnetic force (EMF) of the spindle motor, which is then rectified.

Carriage release can only occur when the motor is up to speed (ATSPEED line is set). Once this line is set, the servo processor unlatches the carriage. When the ATSPEED line goes low, the carriage is retracted and latched again.

9.12.4.7 Automatic Rezero Routine – After the spindle comes up to speed, the initialization process calls up the automatic rezero routine to place the heads on track 0.

9.12.5 Fault Finding

9.12.5.1 Error Detection – Five error conditions exist for the spindle microcomputer to note safety concerns for the drive. By indicating the presence of these conditions, the spindle microcomputer guards against possible power transistor failure and head-to-disk wear. The error codes are listed as follows.

Error Number	Definition (When Invoked)
1	All sensors are low at the same time (start and servo states).
2	All sensors are high at the same time (start and servo states).
3	Four seconds or more elapse for each revolution (start state).
4	Servo state was not achieved within 512 revolutions (start state).
5.	Spindle speed is not 3600 ±1 percent rpm (servo state).

9.12.5.2 Power Fault Status Inhibitor – When the spindle is in the servo state and the carriage is released from the locked position, the spindle microcomputer checks for power faults twice per revolution. If there is a power fault on the first check, the spindle microcomputer sets a flag. If there is a power fault on the second check and a flag was set on the first, the motor is turned off and the drive stops. The drive remains stopped as long as there is a power fault and for another 30 seconds after a recovery.

If the flag is set on the first check and no power fault is detected during the second check, the flag is reset. If a power fault is only detected on the second check, nothing is done. This procedure effectively debounces the power fault line.

The spindle microcomputer handles brown-outs in two ways. First, a 5 V regulator is used on the 12 V line. Second, whenever the voltage to the processor reaches a point where an incorrect reset might occur, an active device forces a reset to the spindle microcomputer.

9.12.5.3 Power Faults – This paragraph describes how the system identifies power-related problems, and the messages that are generated when these problems occur. Figure 9-40 is a block diagram of the RD52-A power fault circuitry.

The power fault circuitry works through WRITE LOGIC, READY LOGIC, and the spindle microprocessor, and generates –WRITE FAULT, –READY, and –SEEK COMPLETE messages, respectively. These processes are described in more detail as follows.

Power Sense – The presence or absence of power is sensed by a comparator circuit that uses a 1 percent reference and 1 percent resistors.

The normal trip points are as follows.

10.53	12 V low
13.72	12 V high
4.51	5 V low
–7.90	8.6 V low (internal supply)
–9.26	8.6 V high (internal supply)

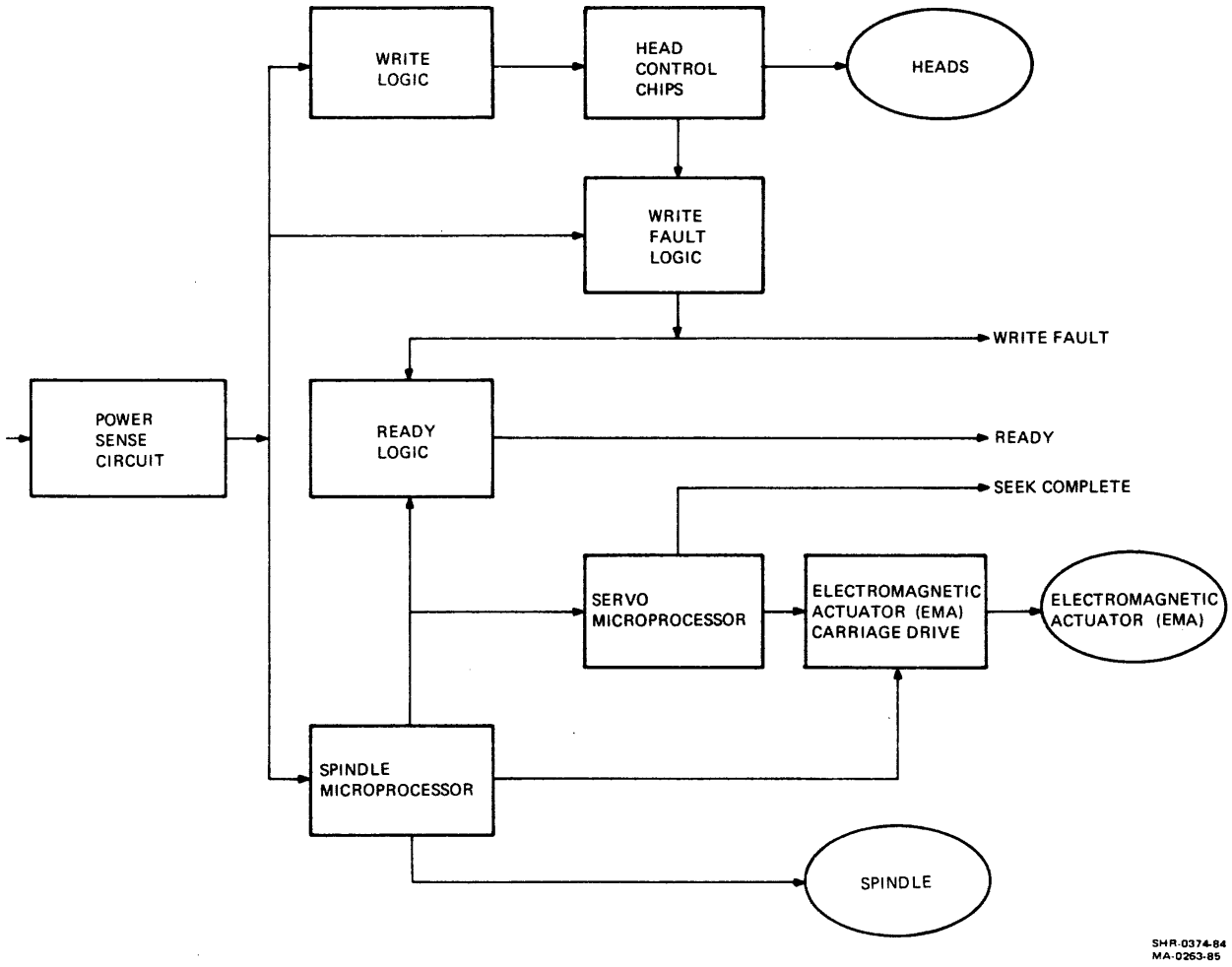


Figure 9-40 Power Faults

Write Logic – Power fault logic prevents writing when power fails. This is accomplished via the write logic block. –WRITE CURRENT and 104–WRITE SELECT are both directly disabled by the power fault circuitry. The not ready condition also inhibits both –WRITE SELECT and –WRITE DATA.

Ready Logic – The power fault circuitry feeds directly to the ready logic and looks for three conditions: power fault, write fault, or servo fault. A power fault that interacts with the ready logic shows up on the interface as NOT READY.

–Write Fault – When power is resumed after a power fault, –WRITE FAULT is reset. A –WRITE FAULT signal exists only in the true condition.

Spindle Microprocessor – The spindle microprocessor looks at the power fault line twice per revolution. If a power fault is seen twice per revolution, the spindle microprocessor retracts the carriage, spins down, and issues a NOT-AT-SPEED signal. NOT-AT-SPEED sends the servo microprocessor to its wake-up routine, and appears as a servo fault to the ready logic. The ready logic then sends NOT READY to the interface.

Abnormal Conditions – There are two known abnormal conditions. The first condition occurs when the 5 V regulator fails but 12 V is present. This condition causes the spindle to stop and then restart. This happens because the spindle works on 12 V only and the power fault line is invalid with 5 V dead. The second condition occurs if there is a short power fault during a write operation. In this case, the write operation is turned off, and -READY goes to NOT READY. As soon as the power condition is restored, writing is resumed and -READY goes to true.

When the power fault line becomes true, the system shuts down. There are two ways to apply braking to the spindle motor. First, reversing the commutation (applying reverse torque in the stop state) brakes the motor. Second, braking can be initiated by electronically shorting one of the motor phases (this only occurs if power is removed from the motor circuitry).

9.12.6 Interface Operations

The interface contains all of the circuits that link the drive to the controller and the drive subsystems to each other. It is composed of many separate logic elements that are best described individually (Figure 9-41).

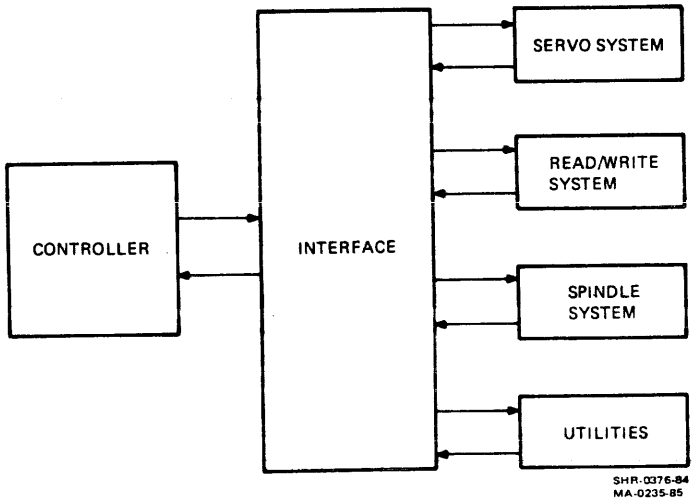


Figure 9-41 Interface Logic

The following lines link the illustrated sections.

Power – When power is supplied, the spindle spins up to speed and issues ATSPEED to the servo system and interface. Several system voltages are generated internally: −8.6, +6, +4, −5.2, −4, +8.

DRIVE SELECT – The user selects the drive in one of two modes: −DRIVE SELECT and RADIAL.

In RADIAL mode, the drive is selected constantly, enabling communication on the controller cables. The −DRIVE SELECTED signal is fed back to the controller.

In −DRIVE SELECT mode, the drive is selected when the controller selects a jumpered select line (see Paragraph 9.12.1). The drive that is selected enables communication on the controller cables, and −DRIVE SELECTED is fed back to the computer.

−TRACK 000 – After power is applied and the spindle is up to speed, the servo does seek to track 0. Track 0 information is written onto the servo track. When the servo is at track 0, it sends a −TRACK 000 signal to the controller module that is enabled by −DRIVE SELECT.

−INDEX – When the servo system is on-track, the interface detects an −INDEX signal and sends it to the index one-shot. The −INDEX signal is written onto the servo surface. The index one-shot signal (200 ms) is gated with −DRIVE SELECT and passed to the controller module.

−DIRECTION IN – The −DIRECTION IN line passes through a latch before it reaches the servo system. The latch is enabled when −STEP is active. When −STEP is inactive (high on the interface), the −DIRECTION IN line remains in its previous state. The −DIRECTION IN line is polled by the servo microprocessor after a step sequence.

−HEAD SELECT – The three head-select lines from the controller module are decoded along with the jumper option (factory set) for the four disk RD52-A version. The head-select lines are gated with the DRIVE SELECT signal before they pass on to the voltage translators and 104 read/write chip.

−READY – When a drive is selected, the ready line is activated if no faults are present. The following faults prevent −READY from being activated.

Spindle not at speed
−WRITE FAULT
Power fault

−STEP – The −STEP signal must be qualified before it can influence the drive. The following conditions qualify −STEP.

−DRIVE SELECTED
No −WRITE FAULT
No servo fault
No power fault
No −WRITE GATE
−STEP

When qualified, the signal passes to the servo system where the steps are counted. Also the qualified −STEP signal strobes the direction in latch and fires a one-shot, which is logically OR'ed with the −SEEK COMPLETE condition. This produces an early −SEEK-NOT-COMPLETE signal to cover for the servo processor's slow response time.

–SEEK COMPLETE – The –SEEK COMPLETE signal is sent true (low) when the servo processor has completed a seek and settled on a track. It is sent not true when a step occurs via a 200 s one-shot. The servo processor latches the –SEEK-NOT-TRUE condition when it discovers that a step command has occurred. For –SEEK COMPLETE to appear on the controller interface, the –DRIVE SELECTED condition must be true.

9.12.7 Interface Logic

The –SEEK COMPLETE signal also influences the write process. The –SEEK COMPLETE signal enables WRITE SELECT and WRITE DATA as they pass to the read/write circuits.

WRITE SELECT – The WRITE SELECT mode is selected if the following conditions exist.

The drive is ready (no faults).
–SEEK COMPLETE is true.
The drive is selected.
–WRITE GATE is active (from the controller).

WRITE DATA – WRITE DATA passed if the following signals are all true.

–SEEK COMPLETE
–DRIVE SELECTED
–WRITE GATE
–READY

WRITE CURRENT – WRITE CURRENT is gated identically to WRITE SELECT, with the addition of a WRITE BOOST signal, which is added when the servo is on the outer tracks.

–WRITE FAULT – WRITE FAULT is a signal captured in a latch, which can be set by an unsafe signal coming from the 104 read/write control chip. This chip produces an unsafe signal under the following conditions.

WRITE CURRENT without WRITE DATA
An open or short head with an attempt to write
WRITE CURRENT in read mode
For several microseconds after the start of a write operation.

The 104 FAULT signal is filtered to eliminate the microsecond fault glitch, and then passed onto the WRITE FAULT latch.

The WRITE FAULT latch can be reset by either a power fault or a false (high) –DRIVE NOT SELECTED.

The –WRITE FAULT condition also feeds back into the interface, where it inhibits steps and produces NOT READY. The NOT READY condition in turn gates both WRITE SELECT and WRITE DATA. A WRITE FAULT inhibits further writing or step acquisition until it is cleared by a power-down or by a drive deselect.

READ DATA – READ DATA is gated to the controller if the drive is selected and –WRITE GATE active is not being sent to the drive.

9.12.8 Servo Operations

9.12.8.1 Velocity Loop – Velocity loop is a process by which the optimal seek profile is obtained. This process is used to move the data heads from one track to another.

The optional seek profile is accomplished as follows.

- A velocity profile of the actual velocity is generated.
- A program velocity is then obtained. This is a square root function of the distance remaining to go (tracks remaining in a seek).

The velocity loop generates a reference velocity trajectory for the system to follow (approximately the square root function of the distance to go). The microprocessor keeps track of the number of tracks remaining in a seek. Based on this information, the microprocessor uses a look-up-table method and transmits a number to the digital-to-analog converter.

The velocity profile is an accurate measurement of actuator velocity. This measurement is done by a velocity transducer that uses position data generated by the servo head. The position signal itself is differentiated to obtain velocity and passes through a low-pass filter to attenuate the resonant frequency of the mechanical system.

After the optimal seek profile is obtained, the servo goes into the settle routine. This is done by entering a track follow mode that allows the head to stay on the center of the track.

9.12.8.2 Servo Status Reporting – Servo status reporting is described as follows.

–STEP

The step signal can be used in either the normal or buffered mode.

In normal mode, pulses can be sent at a rate so that no less than 2.8 ms occur between the rising edge of any two pulses.

In the buffered mode, pulses can be sent between 5 kHz and 800 kHz. When 200 μs have passed since the last pulse, the servo head starts head movement. When the heads start to move, the microprocessor ignores both the –STEP and –DIRECTION signals until the –SEEK COMPLETE signal is set true.

–READY

–READY is a drive status signal that, along with –SEEK COMPLETE, indicates that a drive is ready to accept a command. –READY goes true after the –TRACK 000 signal has completed.

–SEEK COMPLETE

–SEEK COMPLETE, along with the –READY signal, indicates that the selected drive is now ready to read, write, or seek.

–SEEK COMPLETE goes true about 2 ms after the head has arrived on track in buffered mode. In normal mode, it goes true about 6 ms after the last rising edge of the step line.

–SEEK COMPLETE goes false within 100 μs after the first rising edge of the –STEP line. If a step pulse is made more than 4 ms after the last pulse, but before –SEEK COMPLETE is set, then the –SEEK COMPLETE line may go true for a period of not more than 50 μs before going false again.

9.12.8.3 Window Generator – The servo signal decoder/window generator circuit processes the pulse train from the servo signal comparator. The circuit then provides four window pulses that further process the analog servo signal. The four windows are aligned to within 50 ns of their ideal position within each frame. The circuit locks to a frame sync pulse and updates the accuracy of the time lock at the start of each frame. An optional pulse within each frame carries more information about track type (track 0, data, guardband). The decoder circuit reads this information, checks its validity, and controls the guardband and track 0 outputs. Also, a once-per-revolution index pulse is generated.

–TRACK 000

The –TRACK 000 line goes low (true) when the decoder circuits sense cylinder 0. This line is true at all times after initial power up.

9.12.8.4 Index Reporting – INDEX is generated from the window generator logic. The leading edge is accurate to within 50 ns of the actual index.

9.12.8.5 Servo AGC Circuit – The servo AGC circuit amplifies the head signal to a proper level. The gain of the AGC amplifier is controlled by voltage generated by the peak detector circuit. The peak detector samples the four types of track and generates the voltage to control the gain of the AGC generator, so that the output level at the peak detector remains constant.

9.12.8.6 EMA Driver Circuit – The EMA driver is the portion of circuitry that converts the servo error information into drive current for motor positioning.

The inputs to the EMA driver circuit are the EMA/CTL, COMMON LOGIC EMA DISABLE, and COMMON LOGIC RETRACT signals. EMA/CTL is a bipolar analog voltage while the others are logic control signals.

9.12.9 Read/Write Operations – The read/write channel consists of several parts.

Control
Write channel
Read channel analog
Read channel digital

Figure 9-42 shows the relationships between these parts.

The control aspects of this channel are covered in Paragraph 9.13.

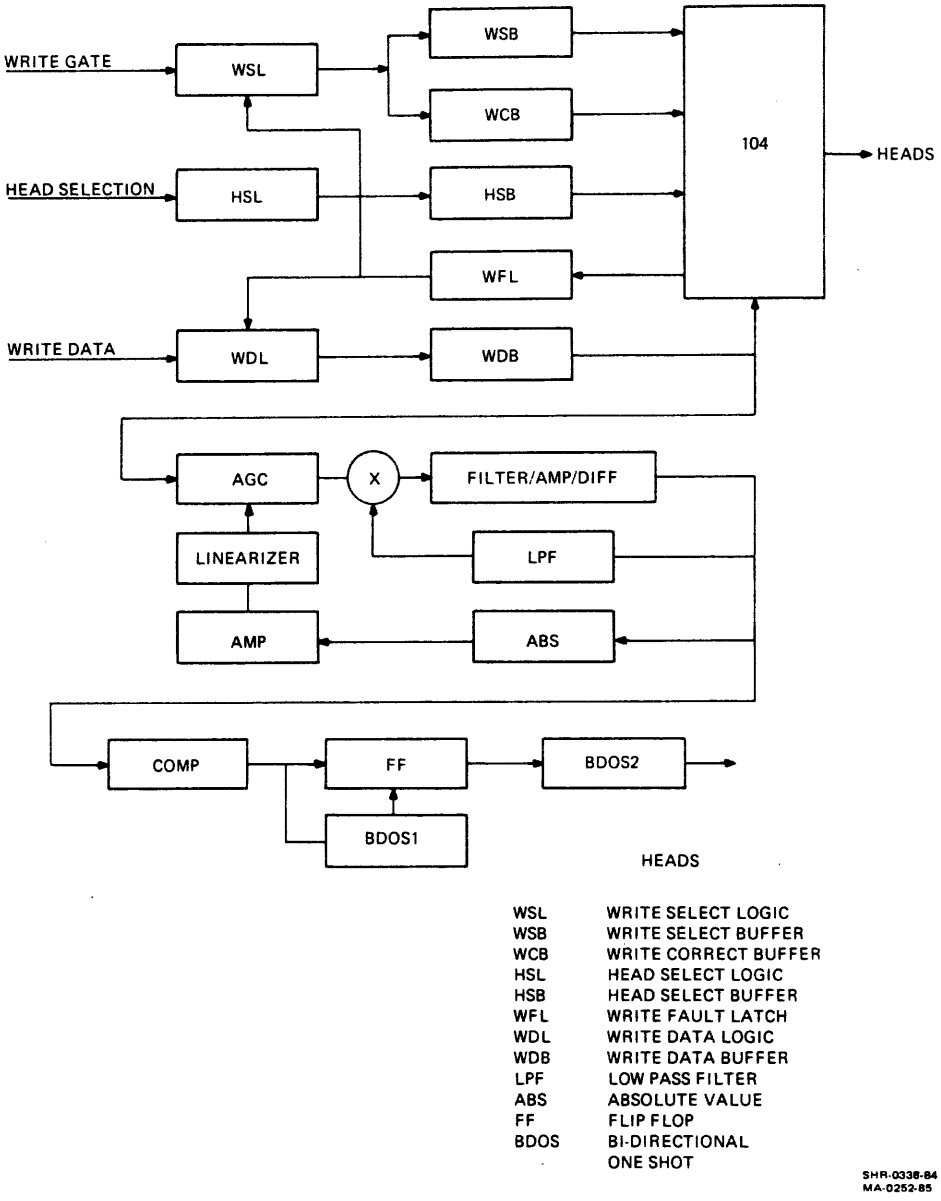


Figure 9-42 Read/Write Operations

9.12.9.1 Write Operations – Writing to the disks requires write selection, head selection, and write data. When –SEEK COMPLETE, –DRIVE SELECTED, –WRITE GATE, and –READY are active, the data passes to the 104 read/write chip. Head selection passes through to the 104 chips if the drive is selected. Selection of a nonexistent head inhibits 104 chip selection.

–WRITE FAULT is generated when:

A write is attempted to a bad head.
Write data is not active during a write attempt.
Write current is applied in a nonwrite mode.

–WRITE FAULT inhibits the passage of –WRITE GATE or –WRITE DATA to the 104 chips, and can be cleared by drive deselect or drive power-down.

Precise timing of the WRITE DATA pulses is necessary for satisfactory read/write operation.

The WRITE DATA applied should be precompensated for best performance. At the ID, 12 ns are needed. At the OD 0 ns is needed.

9.12.9.2 Read Operations – Reading data from the disks is accomplished when the following conditions exist.

Active –DRIVE SELECT
Inactive –WRITE FAULT
No existing fault condition
Drive –READY and –SEEK COMPLETE
Appropriate –HEAD SELECT line active
MFM READ DATA present to the host controller

9.12.9.3 Read Channel/Analog – The analog portion of the read channel consists of the head-to-disk interfaces, the 104 chips, and the post-read amplifier. The largest part of the filtering occurs at the head-to-disk interface. Flux transitions in the media produce a pulse whose 50 percent pulse width varies between 100 and 200 ns.

A second smaller filter is produced by the inductance, capacitance, and resistance of the head circuit. The 104 chips provide a nominal 35X gain without any appreciable filtering.

The pulse goes to an AGC circuit where it is boosted to approximately 50 mV (peak-to-peak), regardless of variations in input signal amplitude. The signal then passes through a 6-pole filter and is amplified and differentiated. The final read analog is nominally 6 V (peak-to-peak) differential.

Three feedback loops are embedded in the read channel to enhance performance. A low-pass filter and amplifier operating on the output prevent offsets from causing pulse-pairing errors. The AGC is linearized by another feedback loop, which is local to the AGC. Finally, the output amplitude is regulated by absolute value feedback to the AGC loop.

9.12.9.4 Read Channel Digital – The digital portion of the read/write channel is designed to work with 5 MHz MFM and to eliminate shoulder-induced zero crossings that would occur at the outer diameter. The read/write signal is first turned into a digital waveform by a fast comparator that detects zero crossings. This digital signal is simultaneously fed into a fast flip-flop and a precision bidirectional one shot. Shoulder-induced pulses are too short in to pass through both the flip-flop and one shot. A second bidirectional one shot converts the flip-flop outputs to pulse MFM data. This data is then routed via –DRIVE SELECT and NOT-WRITE to appear at the controller.

9.13 INTERFACE

The RD52-A uses two interface cables: a control cable and a signal or data cable. All control signals are digital (open collector TTL) and are relayed between the drive and host controller via connector J1. The data transfer signals are differential and relayed via connector J2. DRIVE SELECTED is a digital signal but is also transmitted via J2. Dc power is relayed via connector J3. See Paragraph 9.10.3 for more information about connector J3.

9.13.1 Interface Connectors

The RD52-A has two interface connectors: one for control signals (J1) and one for data interface signals (J2). This paragraph defines the signals, timing requirements, and interface cables associated with these two interface connectors. It also defines the characteristics of the receiver/driver combinations. Figure 9-43 shows the location of these two connectors.

Connection to J1 is through a 34-pin PCB edge connector. Figure 9-44 shows the connector dimensions. The pins are numbered 1 through 34, with the even numbered pins on the solder side of the PCB and the odd numbered pins on the component side of the PCB. A key slot is provided between pins 4 and 6. The recommended mating connector for P1 is the AMP ribbon connector with AMP PN 88373-3.

Connection to J2 is through a 20-pin PCB edge connector. Figure 9-45 shows the connector dimensions. The pins are numbered 1 through 20, with the even numbered pins on the solder side of the PCB and the odd pins on the component side of the PCB. A key slot is provided between pins 4 and 6. The recommended mating connector for P2 is the AMP ribbon connector with AMP PN 8373-6.

9.13.2 Control Signal Interface

9.13.2.1 General – There are two types of control input signals: signals to be multiplexed in a multiple drive system, and signals that do the multiplexing. The multiplexed lines are –WRITE GATE, –HEAD SELECT, –STEP and –DIRECTION IN. The multiplexer is –DRIVE SELECT. Table 9-5 shows the pin designations for the control cable.

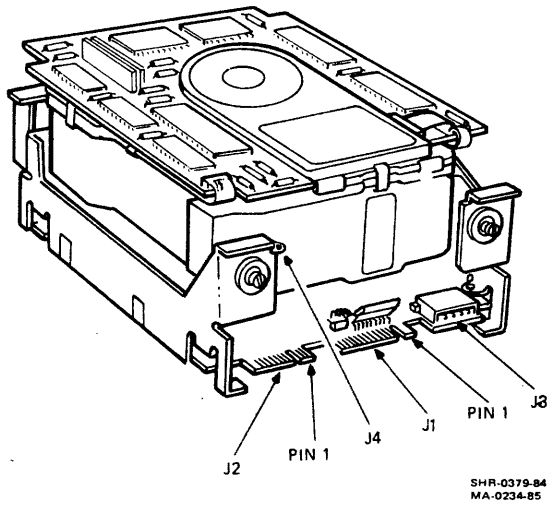


Figure 9-43 Interface Connector Locations

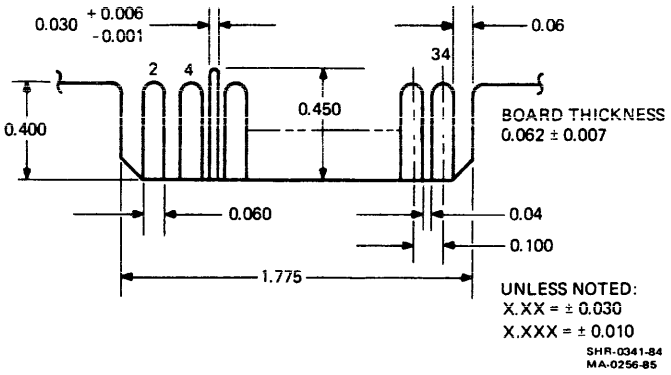


Figure 9-44 J1 Connector

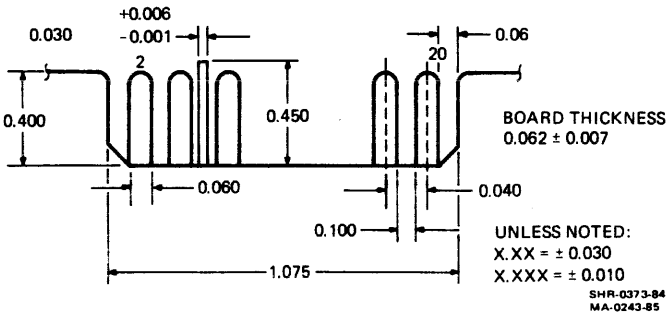


Figure 9-45 J2 Connector

Table 9-5 J1/P1 Connector Pin Assignment

Ground Return Pin	Signal Pin	Signal Name
1	2	–Not used*
3	4	–HEAD SELECT 22
5	6	–WRITE GATE
7	8	–SEEK COMPLETE
9	10	–TRACK 000
11	12	–WRITE FAULT
13	14	–HEAD SELECT 20
15	16	–Reserved (to J2 Pin 7)
17	18	–HEAD SELECT 21
19	20	–INDEX
21	22	–READY
23	24	–STEP
25	26	–DRIVE SELECT 1
27	28	–DRIVE SELECT 2
29	30	–DRIVE SELECT 3
31	32	–DRIVE SELECT 4
33	34	–DIRECTION IN

* Reduced write current may be transmitted without problems.

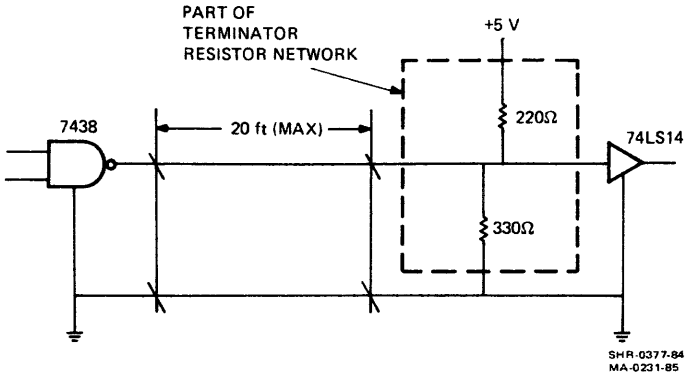


Figure 9-46 Control Signal Driver/Receiver

9.13.2.2 Driver/Receiver – Figure 9-46 shows the recommended control signal driver/receiver combination. The maximum recommended cable length is 6 m (20 ft).

9.13.2.3 Control Signal Descriptions – The control signals and the functions associated with active and inactive line settings are described as follows.

Input Signals

- –WRITE GATE
  When this line is active, it enables the write data to be written on the disk. The inactive state enables data to be read from the disk. Seek operations are also enabled when –WRITE GATE is inactive.

- –HEAD SELECT 2^0, 2^1, 2^2
  These lines provide a means to select read/write heads in a binary-coded sequence. When all –HEAD SELECT lines are inactive, HEAD 0 is automatically selected. When the drive is not selected, read/write heads are deselected. An illegal head address deselects all heads.

- –DIRECTION IN
  This signal defines the direction of the carriage and read/write head movement when the –STEP line is pulsed. An active –DIRECTION IN signal defines a seek toward the spindle. An inactive –DIRECTION IN signal defines a seek away from the spindle.

- –STEP
  This signal causes the read/write heads to move in the direction specified by –DIRECTION IN. Each –STEP pulse moves the heads one cylinder. There are two modes of –STEP operation: normal and buffered. In normal mode, the –STEP pulses may only occur at intervals of 3 ms or greater. The width of the pulse may range from 1.25 ms to 1.0 μs. In buffered mode, the –STEP pulse can occur at intervals between 2.5 μs and 500 μs. The minimum pulse width in buffered mode is 1.25 μs. Figures 9-47 and 9-48 show –STEP signal timing.

- –DRIVE SELECT 1, 2, 3, 4
  When active, this signal enables the drive interface signals to communicate with the host controller.

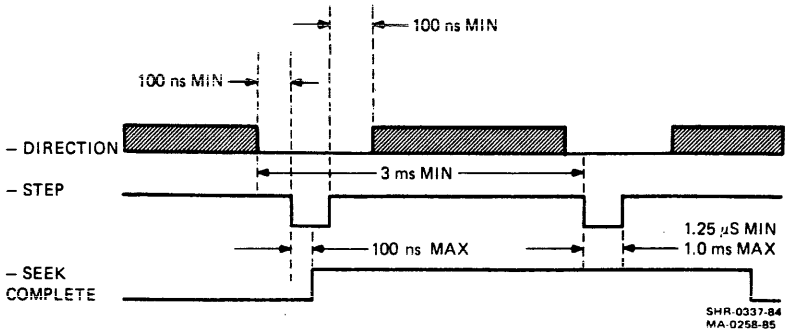


Figure 9-47 Single Step Mode Timing

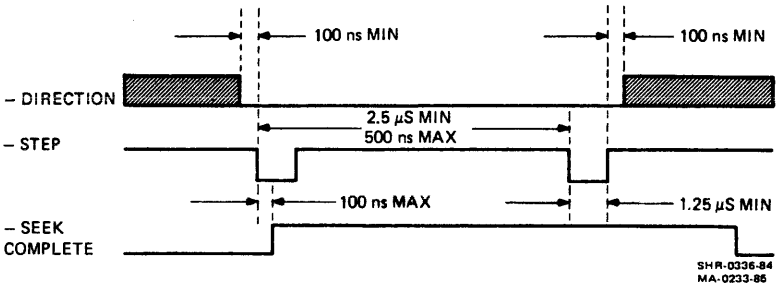


Figure 9-48 Buffered Step Mode Timing

Output Signals

- –SEEK COMPLETE
  This signal becomes active when the read/write heads settle on the desired cylinder at the end of a seek operation. Read or write operations can only be initiated if –SEEK COMPLETE is true. –SEEK COMPLETE goes inactive within 100 nsec after the leading edge of a –STEP pulse, or the first in a series of step pulses, or if +5 Vdc or +12 Vdc are lost momentarily.

- TRACK 000
  This signal becomes active when the read/write heads are positioned at track 0 (the outermost data track).

- –WRITE FAULT
  This signal becomes active when any of the following conditions exist in a selected disk drive.

–WRITE GATE is active and there is no write current.
Write current is present and –WRITE GATE is inactive.

Multiple heads are selected.
A valid selected head is shorted or open.
–WRITE GATE is active with no write data.

–WRITE FAULT is latched in the drive and can be cleared by a power-down or deselection of the drive.

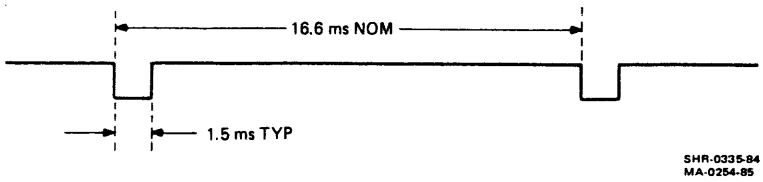


Figure 9-49 Index Timing

- –INDEX
  This signal is presented to the host controller from a selected disk drive once for each disk revolution. It represents the beginning of a track. Figure 9-49 shows INDEX timing.

- –READY
  This signal, with –SEEK COMPLETE, indicates that no drive faults exist. Therefore, the drive is selected and the power sequence is complete. The selected disk is ready to read, write, or seek.

9.13.3 Data Interface Signals

9.13.3.1 General – There are three signals on the data interface cable, none of which are multiplexed. Two of the signals are differential in nature (MFM WRITE DATA and MFM READ DATA). The other signal is –DRIVE SELECTED, which is a TTL open collector output. Table 9-6 shows the pin designations for the data cable.

9.13.3.2 Driver/Receiver – Figure 9-50 shows the recommended data signal driver/receiver combination. The maximum recommended cable length is 6 m (20 ft).

Table 9-6 J2/P2 Connector Pin Assignment

Ground Return Pin	Signal Pin	Signal Name
2	1	–DRIVE SELECTED
4	3	Reserved
6	5	Spare
8	7	Reserved (to J1 Pin 16)
9, 10		Spare
12	11	GND
	13	+MFM WRITE DATA
	14	–MFM WRITE DATA
16	15	GND
	17	–MFM READ DATA
	18	–MFM READ DATA
20	19	GND

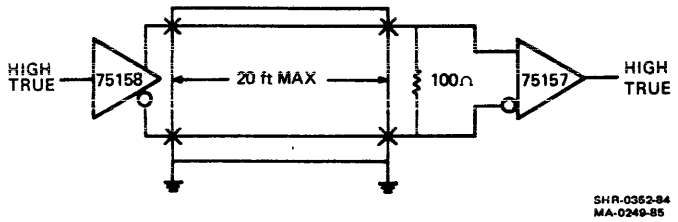


Figure 9-50 Data Line Driver/Receiver

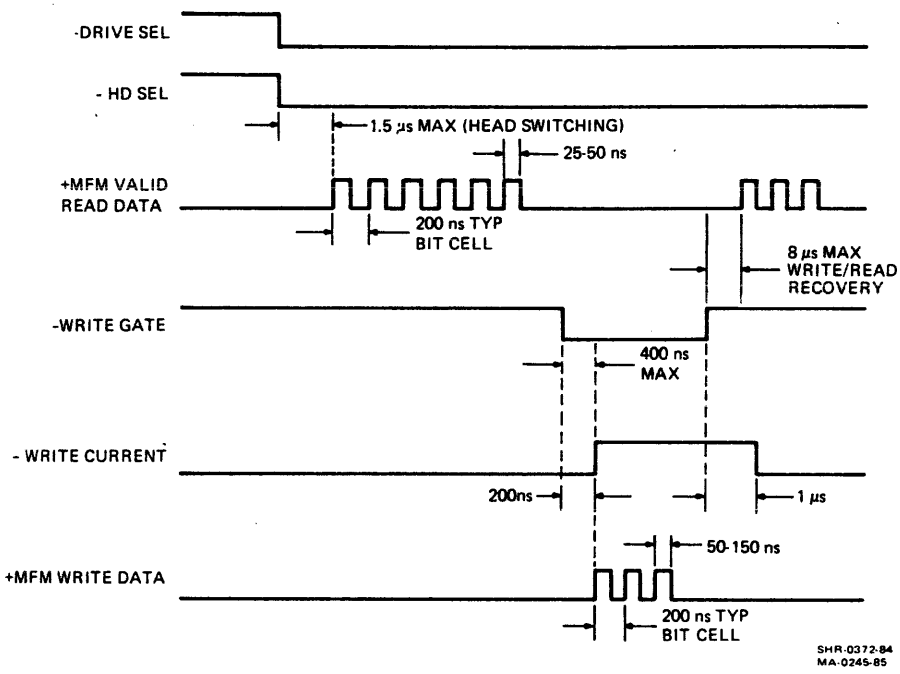


Figure 9-51 Read/Write Data Timing

9.13.3.3 Data Signal Descriptions - The functions of each data signal is described as follows.

- +MFM WRITE DATA/–MFM WRITE DATA
  The two differential MFM signal lines define the code to be written on the track. When +MFM WRITE DATA goes more positive than –MFM WRITE DATA, a transition (flux reversal) is created on the disk by the selected head. Figure 9-51 shows the read/write data timing.

- +MFM READ DATA/–MFM READ DATA
  The transitions (flux reversals) sensed by the selected head from a prerecorded track are transmitted to the host controller as MFM READ DATA. Figure 9-51 shows the read/write data timing.

- –DRIVE SELECTED
  The –DRIVE SELECTED line becomes active when the physical address matches the associated –DRIVE SELECT signal, or when the radial option is enabled.

APPENDIX A
DIAGNOSTIC, ERROR, AND DEVICE CODES

The following table lists the diagnostic errors that may occur on system power up. The error number column is in the following format.

sseeeee
iiiiii

Where "s" is a slot number, "e" is an error code number, and "i" is an ID number. The error codes for each ID code are listed below.

Table A-1 System Error Numbers

ID Number	Error Number	Description
000000	177777	Device not present (not displayed).
1	60	Keyboard is not functioning properly.
	75	Keyboard has a stuck key.
14	1	Unexpected interrupt or trap occurred with manual input device interface.
	200	Time out occurred during loopback testing of manual input device interface.
	201	Time out occurred while waiting for character to be received from manual input device interface.
	202	Overrun or framing error with manual input device interface.
	203	Data compare error with manual input device interface.
17	1	Unexpected interrupt or trap occurred with printer interface.
	200	Time out occurred during loopback testing of printer interface.
	201	Time out occurred while waiting for character to be received from printer interface.
	202	Overrun or framing error with printer interface.
	203	Data compare error with printer interface.

Table A-1 System Error Numbers (Cont)

ID Number	Error Number	Description
21	12	Time out occurred during data loopback testing of communication interface.
	13	Unexpected interrupt or trap occurred during communication interface testing.
	14	Unexpected external/status interrupt from communication interface
	15	Special receive condition interrupt from communication interface
	16	Data compare error with communication interface
	17	Undefined interrupt from communication interface
	20	Time out occurred during modem loopback testing of communication interface testing.
	21	Bad modem signals detected in communication interface.
23	21	Clock did not interrupt in proper time.
	25	Unexpected interrupt or trap occurred during clock testing.
24	22	Data compare error with battery backed up RAM
	23	Unexpected interrupt or trap occurred during battery backed up RAM testing.
25	1	No interrupts generated from interrupt controller.
	2	Unexpected interrupt or trap occurred during clock interface testing.
401	1	RD50 - Bad operation ended bit on power up.
	2	RD50 - Internal power-up self-test error
	3	RD50 - Bad bit/register sector, cylinder, or head registers
	4	RD50 - Busy bit did not go away.
	5	RD50 - Drive is not ready or seek incomplete.
	6	RD50 - Restore command did not cause an "A" interrupt.
	7	RD50 - Restore command did not set operation end bit.
	10	RD50 - Error bit set Restore command.
	11	RD50 - Incomplete read
	12	RD50 - Restore did not reach home during read test.
	13	RD50 - Error bit set on operation end.
	20	RD50 - Bad operation ended bit on power up.
	21	RD50 - Seek incomplete, write fault, or drive not ready
	22	RD50 - Bad bit/register sector, cylinder, or head registers
	23	RD50 - Read command time out
	24	RD50 - Unexpected interrupt or trap
	25	RD50 - Data mark not found.
	26	RD50 - Track 0 error.
	27	RD50 - Illegal/aborted command
	30	RD50 - ID not found.
	31	RD50 - CRC error, ID field
	32	RD50 - CRC error, data field

Table A-1 System Error Numbers (Cont)

ID Number	Error Number	Description
	33	RD50 – Unexpected operation end interrupt
	34	RD50 – Invalid operation end interrupt
	35	RD50 – Unexpected DRQ interrupt
	36	RD50 – Invalid DRQ interrupt
	37	RD50 – Restore command time out
2004	1	RX50 – Internal self-test time out
	2	RX50 – Unexpected interrupt or trap
	3	RX50 – Bad sector buffer
	10	RX50 – Bad drive 0 track 00 sensor
	20	RX50 – Bad drive 1 track 00 sensor
	30	RX50 – Both drives failed to respond.
	40	RX50 – Tried to access an unspecified track number.
	50	RX50 – Drive fails to see home.
	60	RX50 – Data record not found.
	70	RX50 – ID record not found.
	100	RX50 – Time out for FD command done.
	120	RX50 – Selected diskette is not ready.
	130	RX50 – Diskette not installed correctly.
	140	RX50 – ID CRC error
	150	RX50 – Seek error
	160	RX50 – Data ready signal (DRQ) did not respond in 32 ms.
	170	RX50 – Soft ID read error
	200	RX50 – Data CRC error
	210	RX50 – Lost data (8051 did not respond to DRQ within 23 μs).
	220	RX50 – Tried to access an unavailable diskette.
	230	RX50 – Drive not ready during write command.
	240	RX50 – Drive not ready during read command.
	250	RX50 – No sector matches the specified sector.
	260	RX50 – Diskette write protected on a write command.
	270	RX50 – Tried to access a nonspecified sector number.
	300	RX50 – The lower nibble of RAM failed to pass memory test.
	310	RX50 – The higher nibble of RAM failed to pass memory test.
	320	RX50 – No index pulse detected.
	330	RX50 – Drive speed not in limit.
	340	RX50 – Bad format or a blank disk.
	350	RX50 – Stepping error
	354	RX50 – Tried to set unsupported disk parameters.
	360	RX50 – Phase Lock Loop (PLL) frequency not in limit.
	364	RX50 – Tried to read a sector with a deleted data mark.
	370	RX50 – Data buffer is bad.
	374	RX50 – Tried to write a non-RX50 formatted disk.

Table A-1 System Error Numbers (Cont)

ID Number	Error Number	Description
50	2	PC380 video - Register failure
	3	PC380 video - Plane 1 memory failure
	4	PC380 video - Vertical retrace failure
	5	PC380 video - Counter register failure
	6	PC380 video - Plane 1 control, X, Y, or pattern register failure
	7	PC380 video - Plane 1 scroll register failure
	103	PC380 EBO - Plane 2 memory failure
	106	PC380 EBO - Plane 2 control failure
	107	PC380 EBO - Plane 2 scroll register failure
	203	PC380 EBO - Plane 3 memory failure
	206	PC380 EBO - Plane 3 control failure
	207	PC380 EBO - Plane 3 scroll register failure
1002	2	PC350 video - Register failure
	3	PC350 video - Plane 1 memory failure
	4	PC350 video - Vertical retrace failure
	5	PC350 video - Counter register failure
	6	PC350 video - Plane 1 control, X, Y, or pattern register failure
	7	PC350 video - Plane 1 scroll register failure
	103	PC350 EBO - Plane 2 memory failure
	106	PC350 EBO - Plane 2 control failure
	107	PC350 EBO - Plane 2 scroll register failure
	203	PC350 EBO - Plane 3 memory failure
	206	PC350 EBO - Plane 3 control failure
	207	PC350 EBO - Plane 3 scroll register failure
1403	2	PC350 video - Register failure
	3	PC350 video - Plane 1 memory failure
	4	PC350 video - Vertical retrace failure
	5	PC350 video - Counter register failure
	6	PC350 video - Plane 1 control, X, Y, or pattern register failure
	7	PC350 video - Plane 1 scroll register failure
	103	PC350 EBO - Plane 2 memory failure
	106	PC350 EBO - Plane 2 control failure
	107	PC350 EBO - Plane 2 scroll register failure
	203	PC350 EBO - Plane 3 memory failure
	206	PC350 EBO - Plane 3 control failure
	207	PC350 EBO - Plane 3 scroll register failure

Table A-1 System Error Numbers (Cont)

ID Number	Error Number	Description
10050	2	PC380 video – Register failure
	3	PC380 video – Plane 1 memory failure
	4	PC380 video – Vertical retrace failure
	5	PC380 video – Counter register failure
	6	PC380 video – Plane 1 control, X, Y, or pattern register failure
	7	PC380 video – Plane 1 scroll register failure
	103	PC380 EBO – Plane 2 memory failure
	106	PC380 EBO – Plane 2 control failure
	107	PC380 EBO – Plane 2 scroll register failure
	203	PC380 EBO – Plane 3 memory failure
	206	PC380 EBO – Plane 3 control failure
	207	PC380 EBO – Plane 3 scroll register failure
20050	2	PC380 video – Register failure
	3	PC380 video – Plane 1 memory failure
	4	PC380 video – Vertical retrace failure
	5	PC380 video – Counter register failure
	6	PC380 video – Plane 1 control, X, Y, or pattern register failure
	7	PC380 video – Plane 1 scroll register failure
	103	PC380 EBO – Plane 2 memory failure
	106	PC380 EBO – Plane 2 control failure
	107	PC380 EBO – Plane 2 scroll register failure
	203	PC380 EBO – Plane 3 memory failure
	206	PC380 EBO – Plane 3 control failure
	207	PC380 EBO – Plane 3 scroll register failure
30050	2	PC380 video – Register failure
	3	PC380 video – Plane 1 memory failure
	4	PC380 video – Vertical retrace failure
	5	PC380 video – Counter register failure
	6	PC380 video – Plane 1 control, X, Y, or pattern register failure
	7	PC380 video – Plane 1 scroll register failure
	103	PC380 EBO – Plane 2 memory failure
	106	PC380 EBO – Plane 2 control failure
	107	PC380 EBO – Plane 2 scroll register failure
	203	PC380 EBO – Plane 3 memory failure
	206	PC380 EBO – Plane 3 control failure
	207	PC380 EBO – Plane 3 scroll register failure
177776	375	Zero identification number occurred for longer than 20 seconds.
177776	377	Non-existent memory trap occurred for longer than 20 seconds.
Any ID	177777	Slot option untested (not displayed).
Any ID	374	Slot option generated identification number, but slot option detection hardware indicates that option is not present.
Any ID	376	Slot option has a bad ROM.

The following table defines the LED display during BSR execution in customer, console, or service mode. Please note that they are displayed in chronological order.

Table A-2 LED Display 1

LED	Definition
○ ○ ○ ○	System module
○ ○ ○ ●	Memory daughterboard
○ ○ ○ ○	System module
○ ○ ● ○	EBO daughterboard
● ● ● ○	Slot 1
● ● ○ ●	Slot 2
● ● ○ ○	Slot 3
● ○ ● ●	Slot 4
● ○ ● ○	Slot 5
● ○ ○ ●	Slot 6
● ● ● ●	Power-up self-test complete

● means the light is off.
○ means the light is on.

The following table defines the light display during BSR execution in manufacturing mode. Please note that they are displayed in chronological order.

Table A-3 LED Display 2

LED	Definition
○ ○ ○ ○	J11
○ ○ ○ ●	Onboard memory
○ ○ ● ○	Memory daughterboard
○ ○ ● ●	Interrupts
○ ● ○ ○	Clock and battery backed-up RAM
○ ● ○ ●	Communication interface
○ ● ● ○	Manual input device interface
○ ● ● ●	Printer interface
● ○ ○ ●	Plane memory
● ○ ● ○	Video gate array
● ○ ● ●	Plane 2 memory
● ● ○ ○	EBO 1 gate array
● ● ○ ●	Plane 3 memory
● ● ● ○	EBO 2 gate array
● ○ ○ ○	Slots (excluding on board video)
● ● ● ●	Power-up self-test complete

● means the light is off.
○ means the light is on.

The following table defines the light display after BSR execution in customer or console mode. Please note that they are displayed in a prioritized order where the most significant error takes precedence.

Table A-4 LED Display 3

LED	Definition
○ ○ ○ ○	System module
○ ○ ● ●	Unexpected interrupt or trap
○ ○ ○ ●	Memory daughterboard
○ ○ ● ○	EBO daughterboard
● ● ● ○	Slot 1
● ● ○ ●	Slot 2
● ● ○ ○	Slot 3
● ○ ● ●	Slot 4
● ○ ● ○	Slot 5
● ○ ○ ●	Slot 6
○ ● ● ○	Manual input device failure
○ ● ○ ●	No boot found
○ ● ○ ○	Video monitor not detected
● ○ ○ ○	Reserved
○ ● ● ●	Reserved
● ● ● ●	No errors detected

● means the light is off.
○ means the light is on.

The following is a table of bugcheck codes defined for P/OS V2.0. A bugcheck occurs after the system is booted and is recognizable by the picture of the Professional computer system with nothing highlighted and two numbers (the Professional 380 has eight numbers) on the right side of the screen.

Table A-5 Bugcheck Codes

Code	Code Number	Definition
BF.PKS	000100/??????	P/OS keyboard handler
BF.TTD	000200/??????	Terminal driver
BF.PTS	1004??/??????	P/OS terminal subsystem
BF.EXE	000300/??????	Exec – SSTSR, general
BE.IOT	000300/000000	IOT in system state
BE.STK	000300/000001	Stack overflow
BE.BPT	000300/000002	Trace trap or breakpoint
BE.ILI	000300/000003	Illegal instruction trap
BE.ODD	000300/000004	Odd address or other trap 4
BE.SGF	000300/000005	Segment fault
BE.NPA	000300/000006	A task on P/OS without a parent (aborted)
BE.EMT	000300/000007	EMT trap
BE.TRP	000300/000010	TRAP trap
BF.UP	000400/??????	System startup processing
BE.IN1	000400/000001	Can't install task CBOOT
BE.SP1	000400/000002	Can't spawn task CBOOT
BE.SP2	000400/000003	Can't spawn task CMAIN
BE.FNF	000400/000007	Required file not found
Professional/DECnet startup failure codes		
BE.DSC	000400/000010	DSR corrupt
BE.BDP	000400/000011	Bad dispatch
BE.NWB	000400/000012	No way to boot via DECNA
BE.DAF	000400/000013	DSR allocation failure
BE.VIU	000400/000014	DDM vector in use
BE.NPD	000400/000015	Required PDV not found
BE.NSD	000400/000016	Required hardware not present

The following table is a list of the device ID's for the Professional 300 Series Computer System.

Table A-6 Device Identification Codes

ID	Type	Device Name
000000	000	Unready option
000001	000	8 slot CTI backplane
000002	000	7 slot CTI backplane
000003	000	6 slot CTI backplane
000004	000	5 slot CTI backplane
000005	000	4 slot CTI backplane
000006	000	3 slot CTI backplane
000007	000	2 slot CTI backplane
000010	000	1 slot CTI backplane
000011	000	CT100 BASE processor (11/23, mmu)
000012	000	Floating point processor (FPP)
010012	000	PC352 FPP (integrated within J11)
000013	000	VT100 keyboard control
000014	000	LK200 keyboard control
000015	000	VT100 keyboard
000016	000	LK200 keyboard
000017	000	CT100 printer port
000020	000	CT100 speaker control
000021	004	CT100 communication port
000022	000	Not applicable
000023	000	CT100 time/date clock
000024	000	CT100 nonvolatile RAM (NVR)
000025	000	CT100 interrupt controller
000026	000	CT100 DIAG/ROM version 1.0 (first release)
010026	000	CT100 DIAG/ROM version 2.0 (IVIS)
000027	000	CT100 maintenance console port
000030	000	CT100 option present register
000031	000	CT100 serial number ROM
000032	000	CT100 monitor attachment
000033	000	CT100 primary RAM
000034	000	CT100 option RAM (256 kilobytes extended memory)
000035	000	PC352 base processor (J11,MNU)
000036	000	PC352 interrupt controller (integrated inside I/O gate array)
000037	000	PC352 base system ROM version 1.0 (1st Release)
000040	000	CT100 DMA test module

Table A-6 Device Identification Codes (Cont)

ID	Type	Device Name
000041	000	CTI telephone management service (TMS)
000042	004	CTI Ethernet controller
000043	000	CTI Z80/CPM softcard
000044	000	CTI T-11 softcard
000045	010	IVIS base module set
000046	000	IDLDR IEEE option (LDP)
000047	000	KANJI font module
000050	010	PC352 bit map video base module
000051	000	DRC11-AA parallel interface (LDP)
000052	000	DLC11-AA serial interface (LDP)
000053	000	ARC11-AA analog interface (LDP)
000054	002	MRC11-AA ROM option (LDP)
000060	000	DECtouch module (DTM)
000401	002	CTI RD50 5 1/4" Winchester disk controller
001002	010	CTI bit map video base module
001403	000	CTI bit map video extension
002004	001	CTI RX50 5 1/4" floppy diskette controller
002405	004	CTI fast serial line
003006	000	IVIS system module (no ROM)
010001	000	Tempest keyboard (shielded)
010050	000	PC352 bit map video extension
011002	000	IVIS bit map base module
011403	010	IVIS bit map video extension
030050	000	PC352 bit map extension and color map
176775	000	Experimental ID (with identical bytes)
177376	000	Experimental ID (with identical bytes)
177775	000	Experimental ID
177776	000	Experimental ID
177777	000	Escape ID (will be used after all ID codes are exhausted)

The following table contains the I/O and DSW codes.

Table A-7 I/O and DSW Codes

Signal	Decimal	Octal	Definition
IE.BAD	-01	177777	Bad parameters
IE.IFC	-02	177776	Invalid function code
IE.DNR	-03	177775	Device not ready
IE.VER	-04	177774	Parity error on device
IE.ONP	-05	177773	Hardware option not present
IE.SPC	-06	177772	Illegal user buffer
IE.DNA	-07	177771	Device not attached
IE.DAA	-08	177770	Device already attached
IE.DUN	-09	177767	Device not attachable
IE.EOF	-10	177766	End of file detected
IE.EOV	-11	177765	End of volume detected
IE.WLK	-12	177764	Write attempted to locked unit
IE.DAO	-13	177763	Data overrun
IE.SRE	-14	177762	Send/receive failure
IE.ABO	-15	177761	Request terminated (see table at end)
IE.PRI	-16	177760	Privilege violation
IE.RSU	-17	177757	Sharable resource in use
IE.OVR	-18	177756	Illegal overlay request
IE.BYT	-19	177755	Odd byte count (or virtual address)
IE.BLK	-20	177754	Logical block number too large
IE.MOD	-21	177753	Invalid UDC module #
IE.CON	-22	177752	UDC connect error
IE.NOD	-23	177751	Caller's nodes exhausted
IE.DFU	-24	177750	Device full
IE.IFU	-25	177747	Index file full
IE.NSF	-26	177746	No such file
IE.LCK	-27	177745	Locked from read/write access
IE.HFU	-28	177744	File header full
IE.WAC	-29	177743	Accessed for write
IE.CKS	-30	177742	File header checksum failure
IE.WAT	-31	177741	Attribute control list format error
IE.RER	-32	177740	File processor device read error
IE.WER	-33	177737	File processor device write error
IE.ALN	-34	177736	File already accessed on LUN
IE.SNC	-35	177735	File ID, file number check
IE.SQC	-36	177734	File ID, sequence number check
IE.NLN	-37	177733	No file accessed on LUN
IE.CLO	-38	177732	File was not properly closed
IE.NBF	-39	177731	OPEN - no buffer space available for file
IE.RBG	-40	177730	Illegal record size

Table A-7 I/O and DSW Codes (Cont)

Signal	Decimal	Octal	Definition
IE.NBK	−41	177727	File exceeds space allocated, no blocks
IE.ILL	−42	177726	Illegal operation on file descriptor block
IE.BTP	−43	177725	Bad record type
IE.RAC	−44	177724	Illegal record access bits set
IE.RAT	−45	177723	Illegal record attributes bits set
IE.RCN	−46	177722	Illegal record number - too large
IE.ICE	−47	177721	Internal consistancy error
IE.2DV	−48	177720	Rename - 2 different devices
IE.FEX	−49	177717	Rename - new file name already in use
IE.BDR	−50	177716	Bad directory file
IE.RNM	−51	177715	Can't rename old file system
IE.BDI	−52	177714	Bad directory syntax
IE.FOP	−53	177713	File already open
IE.BNM	−54	177712	Bad file name
IE.BDV	−55	177711	Bad device name
IE.BBE	−56	177710	Bad block on device
IE.DUP	−57	177707	ENTER – duplicate entry in directory
IE.STK	−58	177706	Not enough stack space (FCS or FCP)
IE.FHE	−59	177705	Fatal hardware error on device
IE.NFI	−60	177704	File ID was not specified
IE.ISQ	−61	177703	Illegal sequential operation
IE.EOT	−62	177702	End of tape detected
IE.BVR	−63	177701	Bad version number
IE.BHD	−64	177700	Bad file header
IE.OFL	−65	177677	Device off line
IE.BCC	−66	177676	Block check, CRC, or framing error
IE.ONL	−67	177675	Device online
IE.NNN	−68	177674	No such node
IE.NFW	−69	177673	Path lost to partner, this code must be odd
IE.DIS	−69	177673	Path lost to partner, disconnected (Same as NFW)
IE.BLB	−70	177672	Bad logical buffer
IE.TMM	−71	177671	Too many outstanding messages
IE.NDR	−72	177670	No dynamic space available, see also IE.UPN
IE.URJ	−73	177667	Connection rejected by user
IE.NRJ	−74	177666	Connection rejected by network
IE.EXP	−75	177665	File expiration date not reached
IE.BTF	−76	177664	Bad tape format
IE.NNC	−77	177663	Not ANSI 'D' format byte count
IE.NDA	−78	177662	No data available
IE.NLK	−79	177661	Task not linked to specified ICS/ICR interrupts

Table A-7 I/O and DSW Codes (Cont)

Signal	Decimal	Octal	Definition
IE.NST	−80	177660	Specified task not installed
IE.FLN	−81	177657	Device offline when offline request was issued
IE.IES	−82	177656	Invalid escape sequence
IE.PES	−83	177655	Partial escape sequence
IE.ALC	−84	177654	Allocation failure
IE.ULK	−85	177653	Unlock error
IE.WCK	−86	177652	Write check failure
IE.NTR	−87	177651	Task not triggered
IE.REJ	−88	177650	Transfer rejected by receiving CPU
IE.FLG	−89	177647	Event flag already specified
IE.DSQ	−90	177646	Disk quota exceeded
IE.IQU	−91	177645	Inconsistent qualifier usage
IE.RES	−92	177644	Circuit reset during operation
IE.TML	−93	177643	Too many links to task
IE.NNT	−94	177642	Not a network task
IE.TMO	−95	177641	Timeout on request, see also IS.TMO
IE.CNR	−96	177640	Connection rejected
IE.UKN	−97	177637	Unknown name
IE.SZE	−98	177636	Unable to size device
IE.MII	−99	177635	Media inserted incorrectly
IE.SPI	−100	177634	Spindown ignored
IS.PND	+00	0	Operation pending
IS.SUC	+01	1	Operation complete, success
IS.TNC	+02	2	Successful transfer but message truncated (receive buffer too small)
IS.DAO	+02	2	Successful but with data overrun (not to be confused with IE.DAO)
TTY success codes Low order byte is IS.SUC, high order byte is the termination character			
IS.CR	+3329	006401	Carriage return was terminator
IS.ESC	+6913	015401	Escape (altmode) was terminator
IS.CC	+769	001401	Control-C was terminator
IS.ESQ	−25855	115401	Escape sequence was terminator
IS.PES	−32767	100001	Partial escape sequence terminator
IS.EOT	+1025	002001	EOT was terminator (block mode input)
IS.TAB	+2305	004401	Tab was terminator (forms mode input)
IS.TMO	+2	000002	Request timed out

Table A-7 I/O and DSW Codes (Cont)

Signal	Decimal	Octal	Definition
IE.ABO related codes for mount/dismount failures			
AE.SYN	+07	000007	Syntax error
AE.NHM	+10	000012	Home block not found
AE.WRV	+11	000013	Wrong volume
AE.CHK	+12	000014	Checkpoint file still active
AE.SHA	+13	000015	Shadow recording still active
AE.MDM	+14	000016	Volume already marked for dismount
AE.MNT	+15	000017	Volume not mounted
AE.F11	+16	000020	Volume already mounted FILES-11
AE.FOR	+17	000021	Volume already mounted foreign
Directive Error Codes			
IE.UPN	−01	177777	Insufficient dynamic storage, see also IE.NDR
IE.INS	−02	177776	Specified task not installed
IE.PTS	−03	177775	Partition too small for task
IE.UNS	−04	177774	Insufficient dynamic storage for send
IE.ULN	−05	177773	Unassigned LUN
IE.HWR	−06	177772	Device handler not resident
IE.ACT	−07	177771	Task not active
IE.ITS	−08	177770	Directive inconsistent with task state
IE.FIX	−09	177767	Task already fixed/unfixed
IE.CKP	−10	177766	Issuing task not checkpointable
IE.TCH	−11	177765	Task is checkpointable
IE.RBS	−15	177761	Receive buffer is too small
IE.PRI	−16	177760	Privilege violation
IE.RSU	−17	177757	Resource in use
IE.NSW	−18	177756	No swap space available
IE.ILV	−19	177755	Illegal vector specified
IE.ITN	−20	177754	Invalid table number
IE.LNF	−21	177753	Logical name not found
Codes −22 through −79 are reserved.			
IE.AST	−80	177660	Directive issued/not issued from AST
IE.MAP	−81	177657	Illegal mapping specified
IE.IOP	−83	177655	Window has I/O in progress
IE.ALG	−84	177654	Alignment error
IE.WOV	−85	177653	Address window allocation overflow

Table A-7 I/O and DSW Codes (Cont)

Signal	Decimal	Octal	Definition
IE.NVR	−86	177652	Invalid region ID
IE.NVW	−87	177651	Invalid address window ID
IE.ITP	−88	177650	Invalid TI parameter
IE.IBS	−89	177647	Invalid send buffer size (.GT. 255.)
IE.LNL	−90	177646	LUN locked in use
IE.IUI	−91	177645	Invalid UIC
IE.IDU	−92	177644	Invalid device or unit
IE.ITI	−93	177643	Invalid time parameters
IE.PNS	−94	177642	Partition/region not in system
IE.IPR	−95	177641	Invalid priority (.GT. 250.)
IE.ILU	−96	177640	Invalid LUN
IE.IEF	−97	177637	Invalid event flag (.GT. 64.)
IE.ADP	−98	177636	Part of DPB out of user's space
IE.SDP	−99	177635	DIC or DPB size invalid
Success codes from directives – placed in the directive status word.			
IS.CLR	0	0	Event flag was clear
IS.SET	2	2	Event flag was set
IS.SPD	2	2	Task was suspended
IS.SUP	3	3	Logical name superseded

These are the errors from POSSUM. These codes are returned in word 1 of the status block upon return from a POSSUM call.

Table A-8 POSSUM Error Codes

Code	Code Number	Definition
+1	000001	Success
−1	177777	Directive error (word 2 contains $DSW)
−2	177776	I/O status error (word 2 = IOSB, word 3 = IOSB+2)
−3	177775	RMS error (word 2 contains STS, word 3 contains = STV)
−4	177774	Server specific error, codes returned in words 2 through 7
−5	177773	Interface error, specific error in word 2

Interface error subcodes are returned in word 2 and are as follows.

−1	177777	Feature not supported
−2	177776	Impure area invalid, missing
−3	177775	Invalid number of parameters (too few/too many)
−4	177774	Server not installed (server name in words 2 and 3)
−5	177773	Illegal device specification
−6	177772	User buffer too small for returned data
−7	177771	POSSUM/task incompatibility error – relink task

NOTE
PROATR and PRODIR have no server specific error codes.

These are the server specific error codes from PROFBI.

+ 1	000001	Success
− 1	177777	Illegal device
− 2	177776	Device not in system
− 3	177775	Failed to attach device
− 4	177774	Block 0 bad - disk unusable
− 5	177773	At least one of LBNs 0-25 is bad. Can't initialize.
− 6	177772	Bad block file overflow
− 7	177771	Unrecoverable error
− 8	177770	Device write locked
− 9	177767	Device not ready
−10	177766	Failed to write bad block file
−11	177765	Privilege violation
−12	177764	Device is an alignment cartridge
−13	177763	Fatal hardware error
−14	177762	Allocation failure
−15	177761	I/O error sizing device
−16	177760	Allocation for sys file exceeds volume limit
−17	177757	Homeblock allocate write error
−18	177756	Bootblock write error – disk unusable
−19	177755	Index file bitmap I/O error

Table A-8 POSSUM Error Codes (Cont)

Code	Code Number	Definition
−20	177754	Bad block header I/O error
−21	177753	MFD file header I/O error
−22	177752	Null file header I/O error
−23	177751	Checkpoint file header I/O error
−24	177750	MFD write error
−25	177747	Storage bitmap file header I/O error
−26	177746	Failed to read bad block descriptor file
−27	177745	Volume name too long
−28	177744	Unrecognized disk type
−29	177743	Preallocation insufficient to fill first index file header
−30	177742	Preallocated too many headers for single header index file
−31	177741	Preallocation insufficient to fill 1st, 2nd index file headers
−32	177740	Bad block limit exceeded for device
−33	177737	Driver not resident
−34	177736	Bitmap too large - increase cluster factor
−35	177735	Storage bitmap I/O error
−36	177734	Homeblock I/O error
−37	177733	Index file header I/O error
−38	177732	Dismount of device failed
−39	177731	Cannot mount device foreign
−40	177730	Cannot mount device FILES-11
−41	177727	Cannot format DZ - no software support
−42	177726	Cannot detach device
−43	177725	Checkpoint file header overflow,specify smaller checkpoint file
−44	177724	Illegal character(s) in volume name
−45	177723	Cannot format DZ – no hardware support
−46	177722	Cannot format DZ – speed out of range
These are the server specific error codes from PROLOG.		
−1	177777	Error in parsing the SET DEFAULT string.
−2	177776	Cannot determine type of service requested.
These are the server specific error codes from PROTSK.		
+ 1	000001	Successful install
− 1	177777	Task name in use
− 2	177776	File not found
− 3	177775	Specified partition too small
− 4	177774	Task and partition base mismatch
− 7	177771	Length mismatch common block
− 8	177770	Base mismatch common block
− 9	177767	Too many common block requests
−11	177765	Checkpoint area too small
−13	177763	Not enough APRs for task image

Table A-8 POSSUM Error Codes (Cont)

Code	Code Number	Definition
−14	177762	File not task image
−15	177761	Base address must be on 4k boundary
−16	177760	Illegal first APR
−18	177756	Common block parameter mismatch
−20	177754	Common block not loaded
−22	177752	Task image virtual address overlaps common block
−23	177751	Task image already installed
−24	177750	Address extensions not supported
−26	177746	Checkpoint space too small, using checkpoint file
−27	177745	No checkpoint space, assuming not checkpointable
−29	177743	Illegal UIC
−30	177742	No pool space
−31	177741	Illegal use of partition or region
−32	177740	Access to common block denied
−33	177737	Task image I/O error
−34	177736	Too many LUNs
−35	177735	Illegal device
−36	177734	Task may not be run
−37	177733	Task active
−39	177731	Task fixed
−40	177730	Task being fixed
−41	177727	Partition busy
−43	177725	Common/task not in system
−44	177724	Region or common fixed
−45	177723	Can't do receive from requestor
−46	177722	Can't attach to requestor
−47	177721	Invalid request
−48	177720	Can't return result parameter
−49	177717	Error encountered on file open operation
−50	177716	Error encountered on file close operation
−51	177715	Can't get file LBN to process label blocks
−52	177714	No taskname specified in batch request, no name in label block
−53	177713	Unable to create or map to region
PROVOL has the following server specific error codes.		
−1	177777	File is not a system image
−2	177776	Invalid boot device

The following table shows the MS-DOS power up error codes.

Table A-9 MS-DOS Error Codes

Error Codes (octal)	
Code Number	**Definition**
1	Diag is too big or loaded too high
2	Diag exited without setting status
3	Unexpected NXM trap
4	NXM trap referencing CSR's
5	NXM trap referencing 8086 memory
6	Can't load 8086 program in reset vector
7	Program changed by running it
10	Program didn't run or change memory
11	Bad 8086 memory
12	Program killed by memory test
Error codes defined by the base system module.	
374	Device not in "option present" register
375	ID read as 0
376	Error check failed on contents of ROM on device
377	Bus time out trap reading device ID