digital

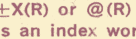
pdp11

INSTRUCTION LIST

GENERAL REGISTER ADDRESSING

Mode	Description	Symbolic	Time (μs) src	dst
0	register	R	0.0	0.0
1	register deferred	@R or (R)	1.5	1.4
2	auto-increment	(R)+	1.5	1.4
3	auto-increment deferred	@(R)+	2.7	2.6
4	auto-decrement	−(R)	1.5	1.4
5	auto-decrement deferred	@−(R)	2.7	2.6
6	indexed	±X(R)	2.7	2.6
7	indexed deferred	@±X(R) or @(R) (±X is an index word)	3.9	3.8

PC REGISTER ADDRESSING



Mode	Description	Symbolic	Time (μs) src	dst
2	immediate	#n	1.5	1.4
3	absolute	@#A	2.7	2.6
6	relative	A	2.7	2.6
7	relative deferred	@A	3.9	3.8

LEGEND

OP FIELDS

- ▪ Byte(1)/Word(0)
- SS Source Field (6 bits)
- DD Destination Field (6 bits)
- R Register
- XX Offset (8 bits)
- ⊻ Exclusive or
- v Inclusive or
- ∧ And

CONDITION CODES

- * Conditionally set
- – not affected
- 0 cleared
- 1 set

TIME

For all times 0.6μs

- more if odd byte
- #0.5μs less if not mode 0
- ⁻1.1μs less if conditions for branch not met
- °1.2μs more if odd byte

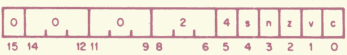
All times ± 20%

MNEMONIC	INSTRUCTION	OP CODE	Cond Codes NZVC	Time (μs)
Double Operand Group: OPR src, dst				
MOV(B)	MOVe	▪1SSDD	**0–	2.3
CMP(B)	CoMPare	▪2SSDD	****	2.3#
BIT(B)	BIt Test	▪3SSDD	**0–	2.9#
BIC(B)	BIt Clear	▪4SSDD	**0–	2.9
BIS(B)	BIt Set	▪5SSDD	**0–	2.3
ADD	ADD	06SSDD	****	2.3
SUB	SUBtract	16SSDD	****	2.3
Subroutine Call: JSR reg, dst				
JSR	Jump to SubRoutine	004RDD	——	4.4
Subroutine Return: RTS reg				
RTS	ReTurn from Subroutine	00020R	——	3.5
Operate Group: OPR				
HALT	HALT	000000	——	1.8
WAIT	Wait for InTerrupt	000001	——	1.8
RTI	ReTurn from Interrupt	000002	****	4.8
—	breakpoint trap (vector at 14)	000003	****	9.3
IOT	Input/Output Trap (vector at 20)	000004	****	9.3
RESET	RESET	000005	——	20.0 msec
EMT	EMulator Trap (vector at 30)	104000-104377	****	9.3
TRAP	TRAP (vector at 34)	104400-104777	****	9.3

MNEMONIC	INSTRUCTION	OP CODE	Cond Codes NZVC	TIME (μs)
Single Operand Group: OPR dst				
CLR(B)	CLeaR	▪ 050DD	0100	2.3
COM(B)	COMplement	▪ 051DD	**01	2.3
INC(B)	INCrement	▪ 052DD	***–	2.3
DEC(B)	DECrement	▪ 053DD	***–	2.3
NEG(B)	NEGate	▪ 054DD	****	2.3
ADC(B)	ADd Carry	▪ 055DD	****	2.3
SBC(B)	SuBtract Carry	▪ 056DD	****	2.3
TST(B)	TeST	▪ 057DD	**00	2.3#
ROR(B)	ROtate Right	▪ 060DD	****	2.3°
ROL(B)	ROtate Left	▪ 061DD	****	2.3°
ASR(B)	Arith. Shift Right	▪ 062DD	****	2.3°
ASL(B)	Arith. Shift Left	▪ 063DD	****	2.3°
JMP	JuMP	0001DD	——	1.2
SWAB	SWAp Bytes	0003DD	**00	2.3

Condition Codes Operator: OPR

Condition Code Operators set or clear condition code bits. Indicated bits are set if S = 1 and cleared otherwise.



1.5

CLC	CLEAR C	000241	——0	1.5
CLV	CLEAR V	000242	—0—	1.5
CLZ	CLEAR Z	000244	–0—	1.5
CLN	CLEAR N	000250	0——	1.5
SEC	SET C	000261	——1	1.5
SEV	SET V	000262	—1—	1.5
SEZ	SET Z	000264	–1—	1.5
SEN	SET N	000270	1——	1.5
——	No Operation	000240	——	1.5
——	No Operation	000260	——	1.5

MNEMONIC	INSTRUCTION	OP CODE	TIME (μs)
Conditional Branches: B —— loc			
BR	BRanch always	000400+XXX	2.6
BNE	Branch if Not Equal (zero) (Z=0)	001000+XXX	2.6⁻
BEQ	Branch if EQual (zero) (Z=1)	001400+XXX	2.6⁻
BGE	Branch if Greater or Equal (zero) (N⊻V=0)	002000+XXX	2.6⁻
BLT	Branch if Less Than (zero) (N⊻V=1)	002400+XXX	2.6⁻
BGT	Branch if Greater Than (zero) (Zv(N⊻V)=0)	003000+XXX	2.6⁻
BLE	Branch if Less or Equal (zero) (Zv(N⊻V)=1)	003400+XXX	2.6⁻
BPL	Branch if PLus (N=0)	100000+XXX	2.6⁻
BMI	Branch if MInus (N=1)	100400+XXX	2.6⁻
BHI	Branch if Higher (C∨Z=0)	101000+XXX	2.6⁻
BLOS	Branch if LOwer or Same (CvZ=1)	101400+XXX	2.6⁻
BVC	Branch if oVerflow Clear (V=0)	102000+XXX	2.6⁻
BVS	Branch if oVerflow Set (V=1)	102400+XXX	2.6⁻
BCC (or BHIS)	Branch if Carry Clear (C=0)	103000+XXX	2.6⁻
BCS (or BLO)	Branch if Carry Set (C=1)	103400+XXX	2.6⁻

XXX Offset (8 bits)

INSTRUCTION FORMATS

double operand group: OPR src, dst

subroutine call: JSR reg, dst

subroutine return: RTS reg

single operand group: OPR dst

condition code operators: OPR

conditional branches: Bxx loc

HARDWARE Multiply—Divide (KEII-A)

OP/REG	ADDRESS	READ	WRITE
DIV Divide	777300	READ ZERO'S	LOAD DIVISOR, START DIVIDE
AC	777302	READ AC	LOAD AC
MQ	777304	READ MQ	LOAD MQ, SIGN EXTENDS INTO AC
MUL Multiply	777306	READ ZERO'S	LOAD MULTIPLICAND, START MULTIPLY
SC SR	777310 777311	READ SC AND SR	LOAD SC AND LOAD SR BITS 0, 6,7
NOR Normalize	777312	READ SC	START NORMALIZE
LSH Logical Shift	777314	READ ZERO'S	LOAD SC, START LOGICAL SHIFT
ASH Arithmetic Shift	777316	READ ZERO'S	LOAD SC, START ARITHMETIC SHIFT

PROCESSOR REGISTER ADDRESSES

General Registers (Addressable only by console)
R0—177700 R1—177701
R2—177702 R3—177703
R4—177704 R5—177705
R6—177706 R7—177707

Console Switches (Addressable only by processor and console)
SWR—177570

Processor Status (Addressable only by processor and console)
PS—177776

DEVICE REGISTER ADDRESSES

Device	CSR	DBR	VECTOR
Teletype Keyboard	177560	177562	60 BR4
Teletype Printer	177564	177566	64 BR4
Reader (PC11)	177550	177552	70 BR4
Punch (PC11)	177554	177556	74 BR4
Line Clock (KW11-L)	177546	—	100 BR6
Line Printer (LP11)	177514	177516	200 BR4
DECtape (TC11/TU56)	177340	177350	214 BR5
Control	177342		
Word Count	177344		
Current Address	177346		
DECdisk (RC11/RS64)	177444	177456	210 BR5
	177446		
Look Ahead	177440		
Disk Address	177442		
Word Count	177450		
Current Address	177452		
Maintenance	177454		
DECdisk (RF11/RS11)	177460	177472	204 BR5
Word Count	177462		
Current Address	177464		
Disk Address	177466		
Disk Address Ext.	177470		
Maintenance	177474		
Disk Segment	177476		

BOOTSTRAP LOADER

LOC	CONT	LOC	CONT
*744	16701	*764	2
*746	26	*766	*400
*750	12702	*770	5267
*752	352	*772	177756
*754	5211	*774	765
*756	105711	*776	177560 (TK) or 177550 (PR)
*760	100376		
*762	116162		

ABSOLUTE LOADER

START ADDRESS

*500

MEM SIZE	*
4K	17
8K	37
12K	57
16K	77
20K	117
24K	137
28K	157

ODT SUMMARY

ODT indicates readiness to accept commands by typing * or by opening a location by printing its contents.

ODT-11

n/	opens word n
/	reopens last word opened
CR	closes open location
LF	opens next location
↑	opens previous location
←	opens relatively addressed word
n;G	goes to word n and starts execution
n;B	sets breakpoint at word n
;B	removes breakpoint
$B/	opens breakpoint status word
;P	proceeds from breakpoint
k;P	proceeds from breakpoint, stops on k^{th} encounter
$M/	opens mask for word search
n;W	searches for words which match n
n;E	searches for words which address word n
n/ (contents) m;0	calculates offsets of n with respect to m

ODT-11X—In addition to the commands of the regular version, the extended version has the following:

n\	opens byte
\	reopens last byte opened
@	opens the absolutely addressed word
>	opens the word to which the branch refers
<	opens next location of previous sequence
n;mB	(m between 0 and 7) sets breakpoint m at word n
;mB	removes breakpoint m
;B	removes **all** breakpoints
$B/	opens breakpoint 0 status word

ASCII 7-Bit Octal Code	Char.	ASCII 7-Bit Octal Code	Char.	ASCII 7-Bit Octal Code	Char.	ASCII 7-Bit Octal Code	Char.
000	NUL	040	SP	100	@	140	`
001	SOH	041	!	101	A	141	a
002	STX	042	"	102	B	142	b
003	ETX	043	#	103	C	143	c
004	EOT	044	$	104	D	144	d
005	ENQ	045	%	105	E	145	e
006	ACK	046	&	106	F	146	f
007	BEL	047	'	107	G	147	g
010	BS	050	(	110	H	150	h
011	HT	051	)	111	I	151	i
012	LF	052	*	112	J	152	j
013	VT	053	+	113	K	153	k
014	FF	054	,	114	L	154	l
015	CR	055	-	115	M	155	m
016	SO	056	.	116	N	156	n
017	SI	057	/	117	O	157	o
020	DLE	060	0	120	P	160	p
021	DC1	061	1	121	Q	161	q
022	DC2	062	2	122	R	162	r
023	DC3	063	3	123	S	163	s
024	DC4	064	4	124	T	164	t
025	NAK	065	5	125	U	165	u
026	SYN	066	6	126	V	166	v
027	ETB	067	7	127	W	167	w
030	CAN	070	8	130	X	170	x
031	EM	071	9	131	Y	171	y
032	SUB	072	:	132	Z	172	z
033	ESC	073	;	133	[	173	{
034	FS	074	<	134	\	174	|
035	GS	075	=	135	]	175	}
036	RS	076	>	136	↑	176	~
037	US	077	?	137	←	177	DEL

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