DEC TRNcontroller 100

Hardware Installation

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This guide describes how to configure and install the DEC ™ TRNcontroller 100 Q–bus-to-Token Ring Adapter (DEQRA) in a VAX™ Q–bus-based computer. It also describes how to run power-up diagnostic tests to validate the hardware functionality of the DEQRA board after installation.

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Preface

Purpose of this Guide

This guide describes how to configure and install the DEC TRNcontroller 100 Q-Bus-to-Token Ring Adapter (DEQRA) in a Digital Equipment Corporation VAX ™ Q–bus-based computer. It also describes how to run power-up diagnostic tests to validate the hardware functionality of a DEQRA board after installation.

Intended Audience

This guide is intended for Digital Customer Services personnel and self-maintenance customers who install and maintain the DEQRA board in the backplane of a Digital VAX host computer. The installer should be familiar with the following host computer operations or features:

- Startup and shutdown procedures
- Printed circuit module installation and removal procedures
- Input/Output (I/O) cable installation and routing techniques
- Hardware configuration

Associated Documents

Additional information about the DEC TRNcontroller 100 product can be found in the following documents:

- *DEC TRNcontroller 100 Hardware Description and Debugging*

  Provides a detailed description of the DEC TRNcontroller 100 and describes its theory of operation. This guide also describes the use of the debugging tool ODT.

- *DEC Token Ring Network Device Driver for VMS Installation*

  Describes how to install the TRDRIVER software.

- *DEC Token Ring Network Device Driver for VMS Use and Programming*

  Describes how to use the VMS Network Control Program (NCP) to configure the DEQRA in a DECnet–VAX environment.

- *Token Ring Access Method, IEEE STD 802.5-1989*

  Specifies the formats and protocols used by the Token-Passing medium access control (MAC) sublayer, the physical layer, and the means of attachment to the token-passing ring physical medium.

- *VMS System Generation Utility Manual*

  Describes the System Generation Utility (SYSGEN) for use on VAX processors.

Conventions

Table 1 lists the conventions used in this guide.

Table 1 Document Conventions

Convention	Description
NOTE	Contains information that may be of special importance to the user.
CAUTION	Contains information to prevent damage to software or hardware.
`Special Type`	Indicates examples of system output or user input. Special type in red indicates user input.
Return	Indicates that you press the Return key.
Ctrl/Z	Indicates that in examples you press the Ctrl key and the Z key, simultaneously.

1

Overview

This chapter provides a brief product and installation overview for the DEC™ TRNcontroller 100 Q-Bus-to-Token Ring adapter (DEQRA).

The DEQRA works with the DEC Token Ring Network Device Driver for VMS (TRDRIVER) as a system. The TRDRIVER software provides a programmable interface to the DEQRA in a DECnet™-VAX environment. You should install the DEQRA hardware module before you install the TRDRIVER software. The TRDRIVER installation procedure requires information made available during the first part of the DEQRA installation. Refer to the *DEC Token Ring Network Device Driver for VMS Installation* guide for information on installing the TRDRIVER.

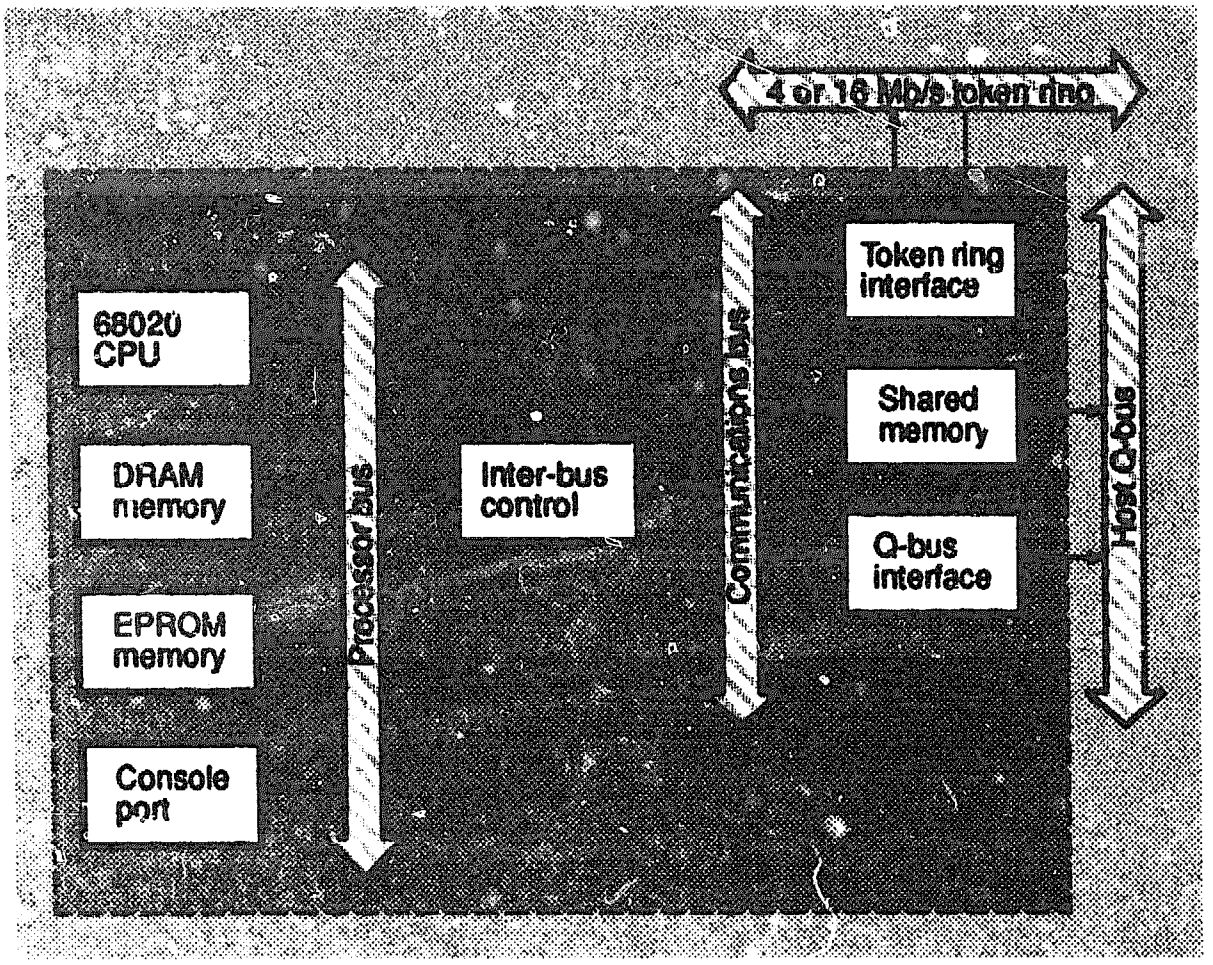
The time involved in installing both the hardware and the software components is approximately 15 minutes. The exact installation time depends on your media and on your system configuration.

1.1 DEC TRNcontroller 100 Description

The DEQRA is a single-board computer that has a central processing unit, random access memory, programmable read-only memory, token-ring interface circuitry, and host interface circuitry. The DEQRA provides the communication link between Q–bus-based Digital Equipment Corporation VAX computers and an IEEE 802.5 industry standard 4 Mbits or 16 Mbits token ring network. In addition, the DEQRA is mountable in any peripheral position of a suitably configured Digital Equipment Corporation VAX computer using a Q–bus and is physically compatible with Digital's EMI shielded, BA200/400 series enclosures.

Figure 1–1 shows a block diagram of the DEQRA controller.

Figure 1–1 DEQRA Block Diagram



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The processing capacity of the DEQRA relieves the host computer of the resource-consuming burden associated with data transmission, protocol handling, and so on. The microcomputer intelligence in the DEQRA, combined with the control software downloaded from the Digital host, perform all the routine and special tasks associated with message transmission and reception.

In addition, the DEQRA has a direct token-ring port connector built into its recessed handle that uses a BN26P series cable to connect the DEQRA to the token ring network.

1.2 Hardware/Software Installation Procedure

Figure 1–2 illustrates the installation procedure for the DEC TRNcontroller 100 hardware and software. Figure 1–2 also provides the titles of the individual books that allow you to accomplish the installations.

Figure 1–2 DEQRA/TRDRIVER Installation Flowchart

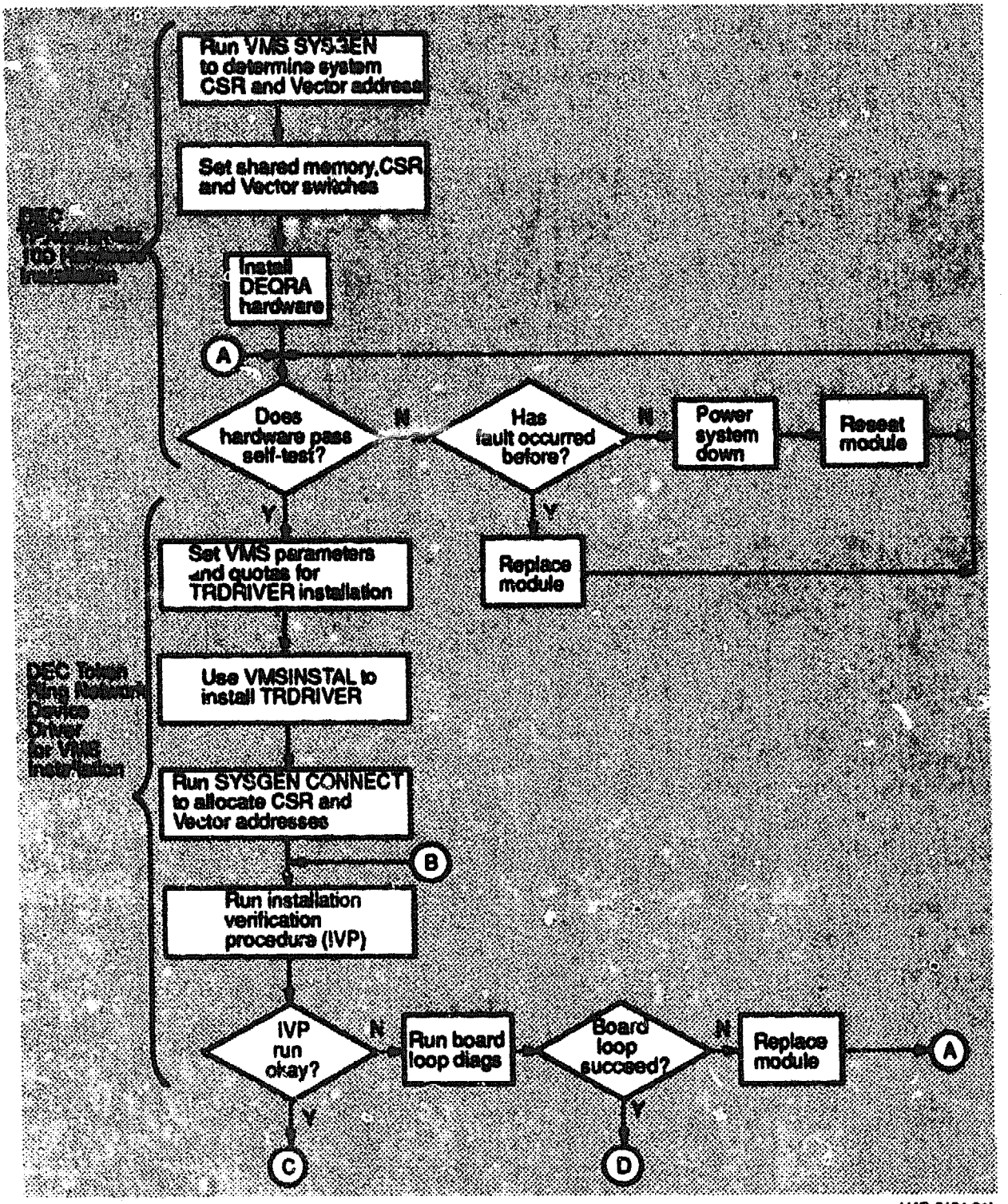

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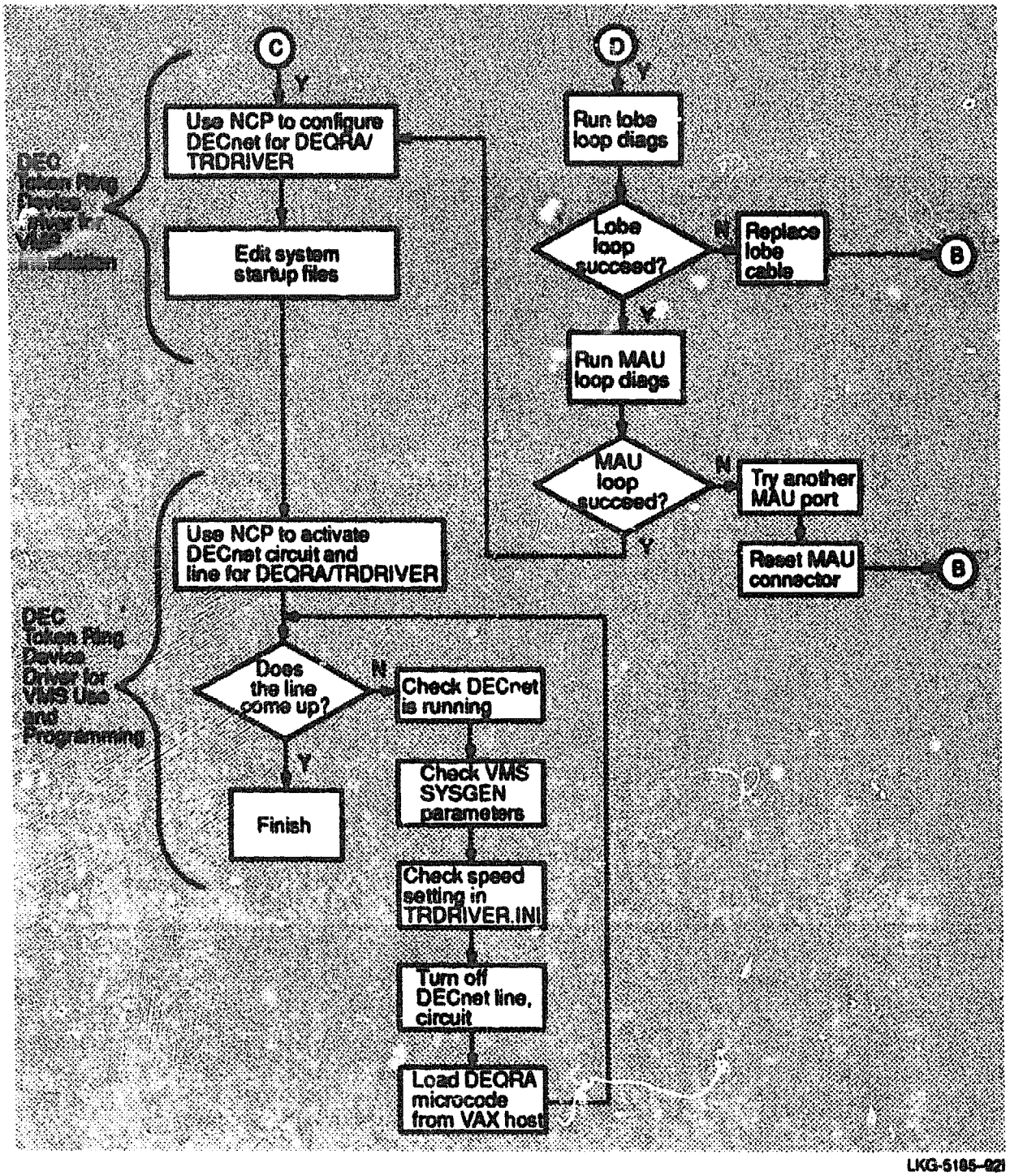
Figure 1–2 (Cont.) DEQRA/TRDRIVER Installation Flowchart



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2

DEQRA Technical Specifications

This chapter describes the power and environmental requirements for the DEC TRNcontroller 100 Q-bus to Token Ring Adapter (DEQRA).

2.1 Power Requirements

Table 2–1 defines the power requirements for the DEQRA that the host power supply must meet. You must consider all peripheral devices in the system when figuring power supply constraints.

Table 2–1 DEQRA Power Requirements

	Token Ring	Maximum Current Drain	
		+5 Vdc	+12 Vdc
DEQRA	4 or 16 Mbits token ring	5.0 amps	0.1 amps

2.2 Environmental Requirements

To ensure reliable operation of the DEQRA and its host system, the room in which the equipment is installed should provide cool, filtered, humidified air. The temperature within the room should be held as stable as possible to prevent thermal-related failures.

Keep the humidity high enough to reduce the static electricity that low humidity can contribute to.

Table 2–2 defines the environmental requirements for the DEQRA.

Table 2–2 DEQRA Environmental Requirements

Environmental Specification	Range		Recommended Operating Condition
Temperature	Operating, Nonoperating,	10° to 40°C –40° to 65°C	20°C
Humidity	Noncondensing	10% to 90%	45%

3

Antistatic Precautions and Inspection Procedures

This chapter explains how to unpack and inspect the DEQRA board. Also included in this chapter, are the antistatic precautions you should adhere to when unpacking, inspecting, and handling the DEQRA board.

3.1 Antistatic Precautions

The DEQRA board contains integrated circuits that are sensitive to electrostatic discharge (ESD). Improper handling and ESD can damage the DEQRA and result in symptoms ranging from unreliable operation to failure.

CAUTION

Never handle the DEQRA when it is outside of its protective bag without wearing a static-guard wrist strap or taking an equivalent grounding precaution. A disposable static-guard wrist strap is shipped with each DEQRA board.

ATTENTION

Vous ne devez pas manipuler le module DEQRA une fois sorti de son sac antistatique sans porter un bracelet antistatique ou sans prendre une précaution équivalente de mise à la terre. Un bracelet antistatique est fourni avec le module DEQRA.

PRECAUCIÓN

No se debe manipular la DEQRA cuando se encuentre fuera de la bolsa protectora, si no se lleva puesta una muñequera antiestática o se toman precauciones equivalentes con vistas a la conexión a tierra. Las placas DEQRA se entregan con una muñequera desechable del tipo citado.

VORSICHT

Legen Sie die mitgelieferte antistatische Gelenkmanschette an, bevor Sie die DEQRA-Karte aus der Schutzhülle nehmen und damit arbeiten.

Standard ESD handling precautions are sufficient to protect the DEQRA. If you are not familiar with these techniques, take the following precautions:

- Place the antistatic grounding strap (provided) around your wrist.
- Leave the DEQRA board inside its antistatic plastic bag until you are ready to inspect, configure, or install the board.
- Keep the solder side of the DEQRA in direct contact with the antistatic bag, when inspecting or configuring the board.
- Discharge any electro-static charge from your body before installing the DEQRA board or removing it from the computer. To do this, place a hand on the conductive metal surface of the computer chassis.
- Return the board to the antistatic bag immediately after inspection, configuration, or removal from the host backplane.

3.2 Initial DEQRA Inspection Procedure

Observing normal antistatic precautions (see Section 3.1), unpack and inspect the DEQRA using the following procedure:

1. Remove all DEQRA components (i.e. DEQRA board, hardware, and documentation) from their shipping packages.
2. Check the packing list against the items shipped. Table 3–1 is a list of items shipped with the DEQRA.
3. Remove the DEQRA board from its antistatic plastic bag and check the overall appearance of the board for damage that may have occurred during shipping.

Table 3–1 DEQRA Option Contents

DEQRA Option	Enclosure Type	Components
DEQRA-CA	BA200/400	DEQRA controller board
		Gap filler panel kit [1](part number 70-24505-01)
		TRDRV/VMS license letter
		TRDRV/VMS H-kit [2]
		DEC TRNcontroller 16 Hardware Installation

[1]The gap filler panel kit contains two gap filler assemblies (part number 70-24071-01).

[2]The TRDRV/VMS H-kit is part of the DEQRA, but is shipped separately.

4

Hardware Configuration and Installation

This chapter explains how to configure and install the DEQRA board. Specifically it explains how to:

- Locate and define the key components needed to configure the DEQRA
- Select the shared memory base address
- Select the control/status register (CSR) address
- Select the interrupt vector address
- Position the shared memory ENABLE jumper (JP1)
- Install the DEQRA into the host computer
- Powerup the DEQRA

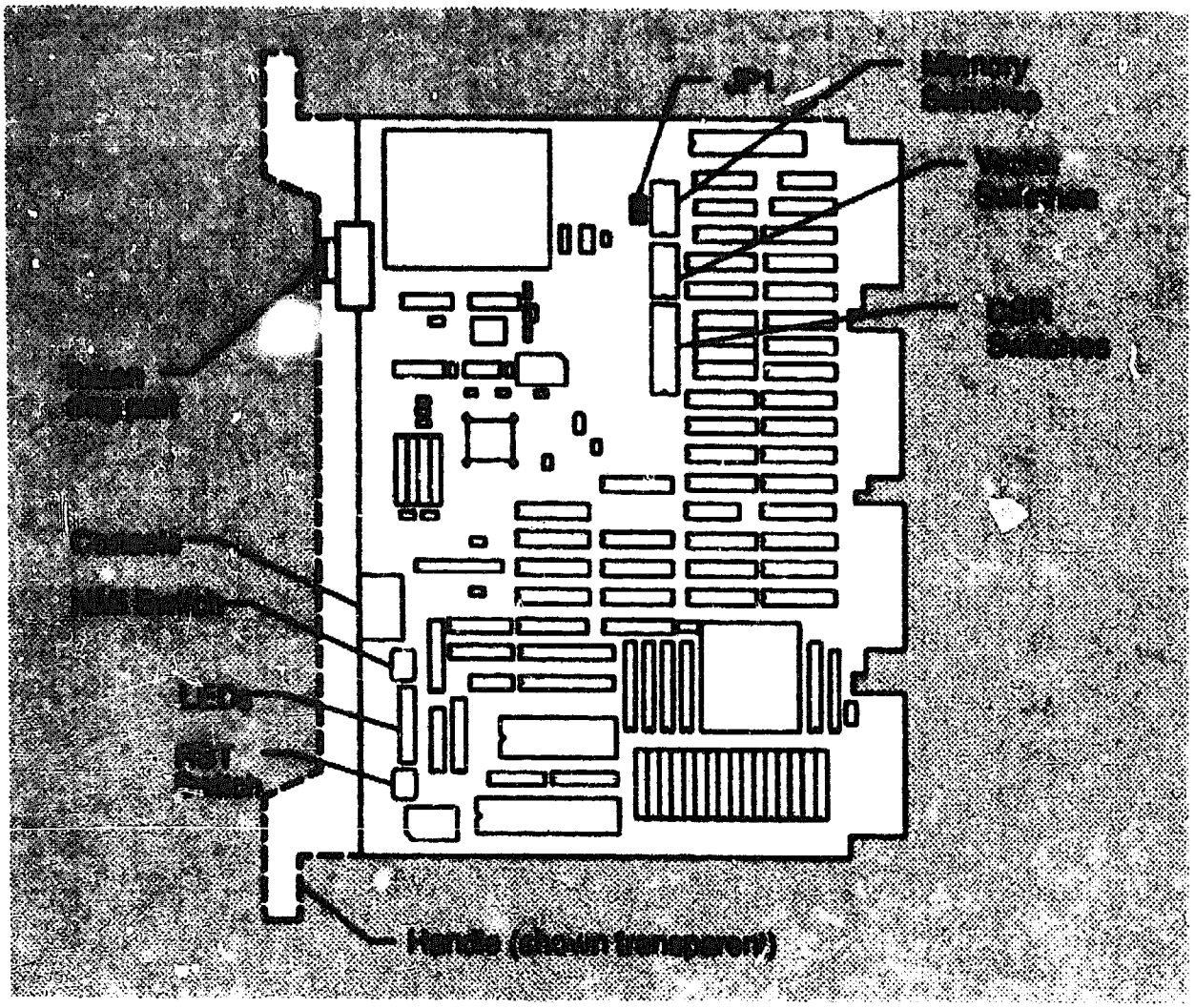
4.1 TRNcontroller 100 Switches, Jumpers, and Diagnostic Indicators

The DEQRA has several components that control its operation and signify status. Table 4–1 lists these components and their respective functions. See Figure 4–1 for the locations of these components.

Table 4–1 DEQRA Board Components

Component	Function
Nonmaskable interrupt switch (NMI)	The NMI switch places the DEQRA processor into the online debugging mode (ODT68). This switch is not used in normal operation.
Reset switch (RST)	The RST switch causes the DEQRA processor to reset and run onboard powerup diagnostics. This switch is not used in normal operation.
Q–bus address switches (CSR_SW)	The eleven individual switches on the DEQRA's control/status register (CSR) switchpack determine the address of the board's CSR.
Shared memory switches (MEM SW)	The three shared memory switches determine one-half megabyte increments of shared Q–bus memory space.
Vector address switches	The seven vector address switches select the 7xx vector address area or the 3xx vector address area.
Jumper (JP1)	The JP1 jumper determines whether the DEQRA's shared memory is visible to the host at powerup. In normal operation the jumper is set so the DEQRA's shared memory is visible.
Diagnostic Light Emitting Diodes (LEDs)	These eight LEDs indicate the status of the DEQRA diagnostic tests or application software. See chapters 4 and 5 for the actual diagnostic tests and LED displays.

Figure 4–1 DEQRA Board Components



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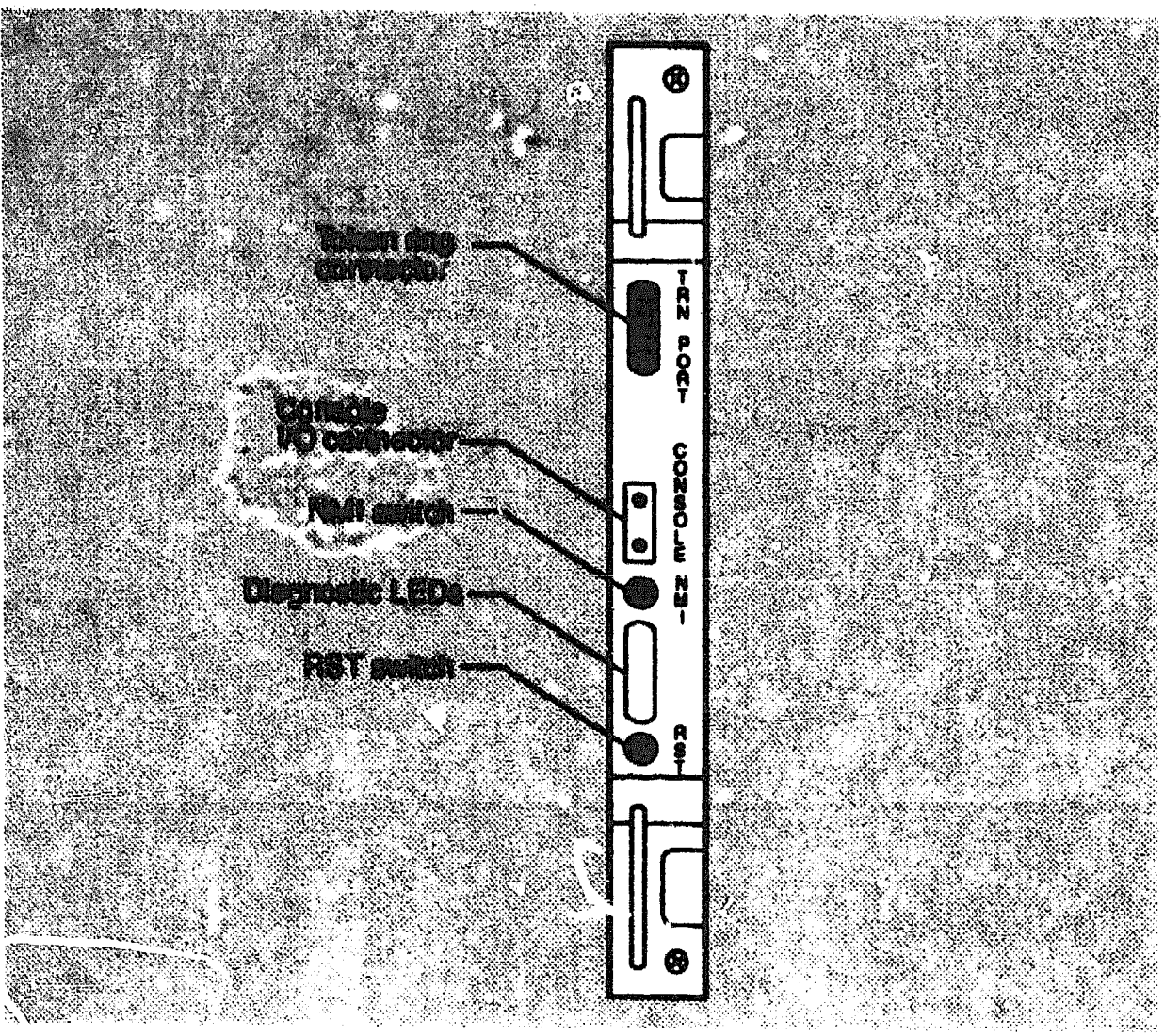
4.2 TRNcontroller 100 Ports

The DEQRA board uses its handle to house the token ring connector and the console I/O connector ports. See Figure 4–2 for the location of these connector ports.

Figure 4–2 TRNcontroller 100 Ports



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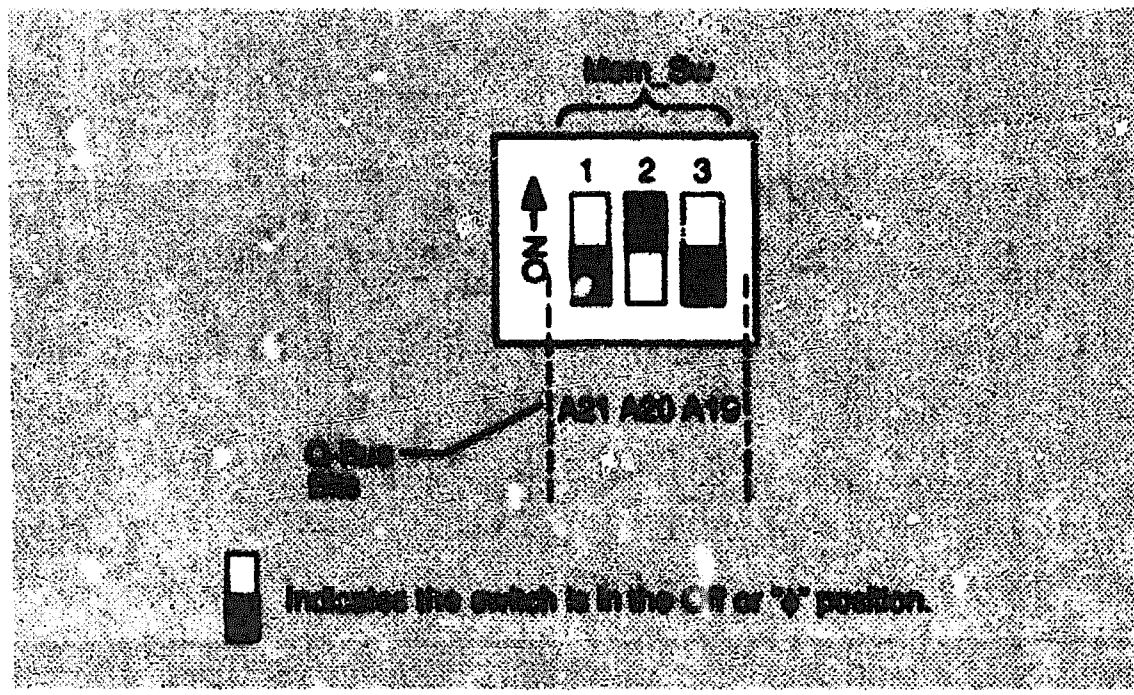
4.3 Selecting the Shared Memory Base Address

You must set the Q–bus base address for the onboard 512k bytes of shared memory before installation. If you install more than one DEQRA in a system, or if you install another Q–bus module using a Q–bus address, ensure that the addresses do not overlap. Each module must have a unique base address.

Select the base address by setting the three memory address switches shown in Figure 4–3. Table 4–2 shows the address range and the corresponding switch settings.

Figure 4–3 Shared Memory Switches MEM_SW



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	Switch Numbers			
Address Range	1 (A21)[1]	2 (A20)	3 (A19)	Comments
00000000-01777777	0	0	0	Illegal
02000000-03777777	0	0	1	
04000000-05777777	0	1	0	
06000000-07777777	0	1	1	
10000000-11777777	1	0	0	
12000000-13777777[2]	1	0	1	
14000000-15777777[3]	1	1	0	
16000000-17777777	1	1	1	Illegal

[1]Corresponding address bit.

[2]The default address for the DEQRA begins at address 12000000 and ends at address 13777777.

[3]The default address for a second DEQRA, if one exists, begins at address 14000000 and ends at address 15777777.

4.4 Selecting the CSR and Interrupt Vector Addresses

The DEQRA is a full floating Q22 Bus device (Type D). This allows the CSR and interrupt vector addresses to be located anywhere in the floating address and vector space. However, the CSR address assigned must be a higher value than all other devices in the system, and there must be a gap of at least 4 bytes left open between the last device register and the beginning of the first DEQRA CSR address. The interrupt vector you select must be beyond the highest in use. For more information on device CSR and vector assignments refer to the *VMS System Generation (SYSGEN) Utility Manual*.

In VMS V5.5, the DEQRA is not supported by AUTOCONFIGURE, and you must manually assign an address and give that information during the installation so that the CONNECT command can be used in the supplied startup file.

You can obtain the system CSR and vector addresses of all system options, excluding the DEQRA, by using VMS for both the MicroVAX ™ 3000 and VAX 4000 systems. To use VMS to find the system CSR and vector addresses, enter the following command at the DCL prompt ($):

```
$ RUN SYS$SYSTEM:SYSGEN Return
```

The VMS system places you at the SYSGEN> prompt. Enter the SHOW /CONF command to display the system configuration of all system options, excluding the DEQRA.

```
SYSGEN>SHOW /CONF [Return]
```

The SHOW /CONF command returns the device name, number of units, CSR address, and the vector number of all devices in the system. The following is an example of the entire show configuration process:

```
$ RUN SYS$SYSTEM:SYSGEN [Return]
SYSGEN>SHOW /CONF [Return]

        System CSR and Vectors

Name: PIA  Units: 1  Nexus:0  (640)
Name: ESA  Units: 1  Nexus:0  (640)
Name: PUA  Units: 1  Nexus:1  (UBA)  CSR: 772150   Vector1: 154  Vector2:000
Name: PTA  Units: 1  Nexus:1  (UBA)  CSR: 774500   Vector1: 260  Vector2:000
Name: TXA  Units: 8  Nexus:1  (UBA)  CSR: 760440   Vector1: 300  Vector2:304
Name: PKA  Units: 1  Nexus:1  (UBA)  CSR: 761300   Vector1: 310  Vector2:000
```

With the system CSR and vector addresses displayed you can select the DEQRA CSR and interrupt vector address locations. It is recommended that you select a CSR address and an interrupt vector address that are beyond the last system CSR address and vector address.

Once you have identified the DEQRA CSR and interrupt vector addresses, set the DEQRA CSR address and vector address switches (refer to Sections 4.4.1 and 4.4.2). Be sure to write down the CSR and interrupt vector addresses. They will be needed for the software installation.

4.4.1 Setting the DEQRA CSR Address Switches

You set the CSR address of the DEQRA board by using the 11 CSR address switches shown in Figure 4–4.

Figure 4–4 Selecting the CSR Address

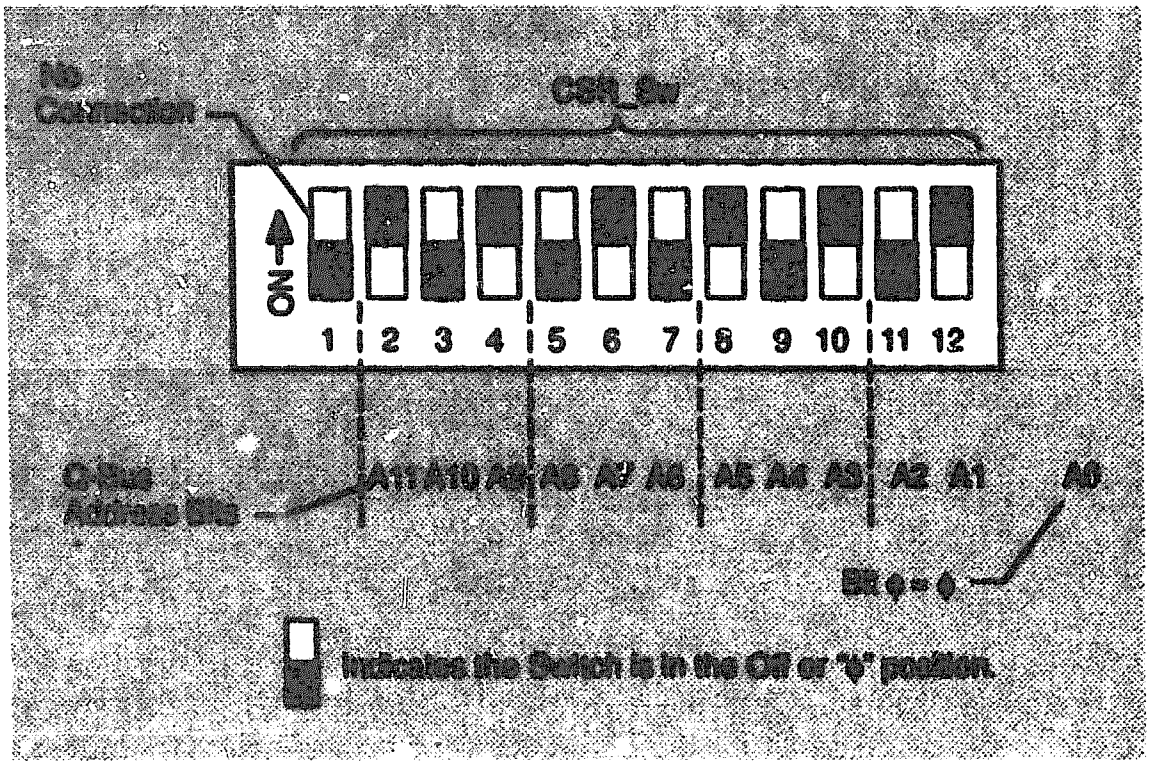

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Table 4–3 lists the addresses and corresponding switch settings.

Table 4–3 CSR Switch Settings

		CSR Switch Numbers[1,2]										
Base Address	Q-Bus Address	2	3	4	5	6	7	8	9	10	11	12
		A11[3]	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
2000 0000	760000	0	0	0	0	0	0	0	0	0	0	0
2000 0002	760002	0	0	0	0	0	0	0	0	0	0	1
2000 0004	760004	0	0	0	0	0	0	0	0	0	1	0
2000 0006	760006	0	0	0	0	0	0	0	0	0	1	1
.	.					.						
.	.					.						
.	.					.						
2000 02E4	761344[4]	0	0	1	0	1	1	1	0	0	1	0
.	.					.						
.	.					.						
.	.					.						
2000 0FFA	767772	1	1	1	1	1	1	1	1	1	0	1
2000 0FFC	767774	1	1	1	1	1	1	1	1	1	1	0
2000 0FFE	767776	1	1	1	1	1	1	1	1	1	1	1

[1]Switch on = 1, Switch off = 0

[2]Switch 1 is not used.

[3]Corresponding address bit

[4]The default CSR address for the first DEQRA is 761344 and 761346 for the second DEQRA.

4.4.2 Setting the DEQRA Vector Address Switches

You set the interrupt vector address of the DEQRA board by using the seven vector address switches shown in Figure 4–5.

Figure 4–5 Selecting the Interrupt Vector Address

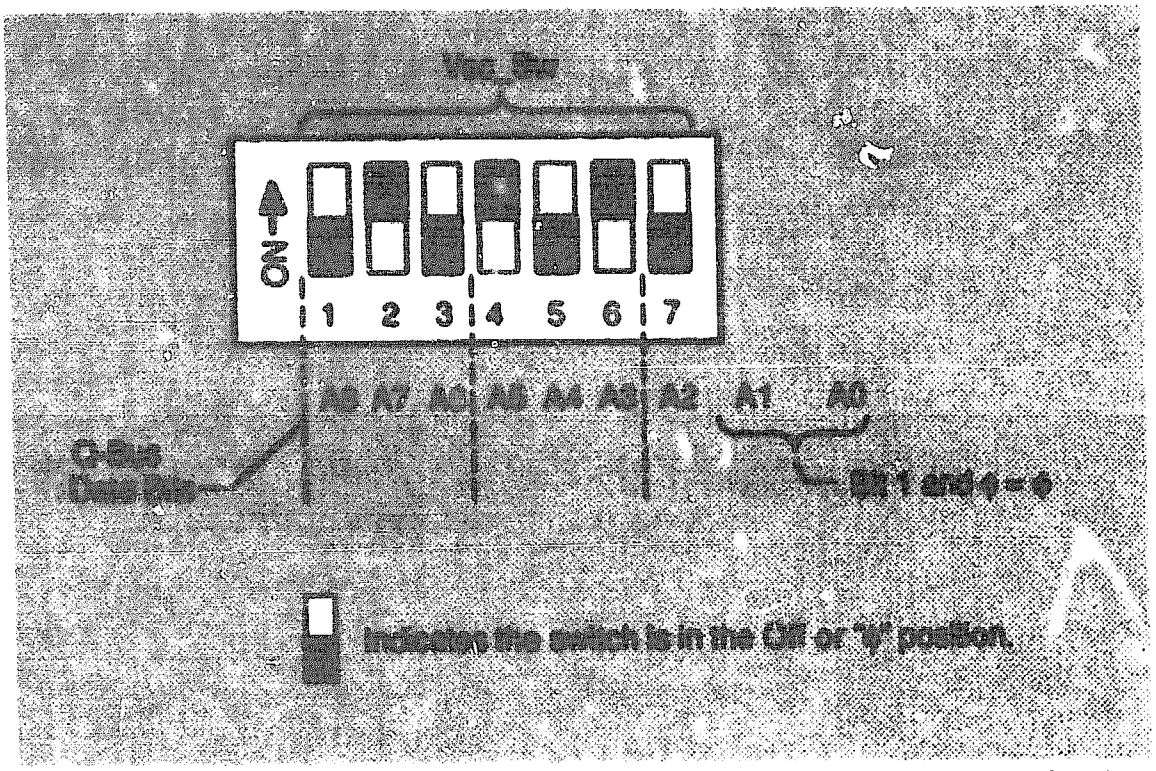

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Table 4–4 lists the addresses and corresponding switch settings.

Table 4–4 Vector Switch Settings

	Vector Switch Numbers[1]						
Vector Address	1(A8)[2]	2(A7)	3(A6)	4(A5)	5(A4)	6(A3)	7(A2)
300[3]	0	1	1	0	0	0	0
304	0	1	1	0	0	0	1
310	0	1	1	0	0	1	0
314	0	1	1	0	0	1	1
320	0	1	1	0	1	0	0
.				.			
.				.			
.				.			
760	1	1	1	1	1	0	0
764	1	1	1	1	1	0	1
770	1	1	1	1	1	1	0
774	1	1	1	1	1	1	1

[1] Switch on = 1, Switch off = 0

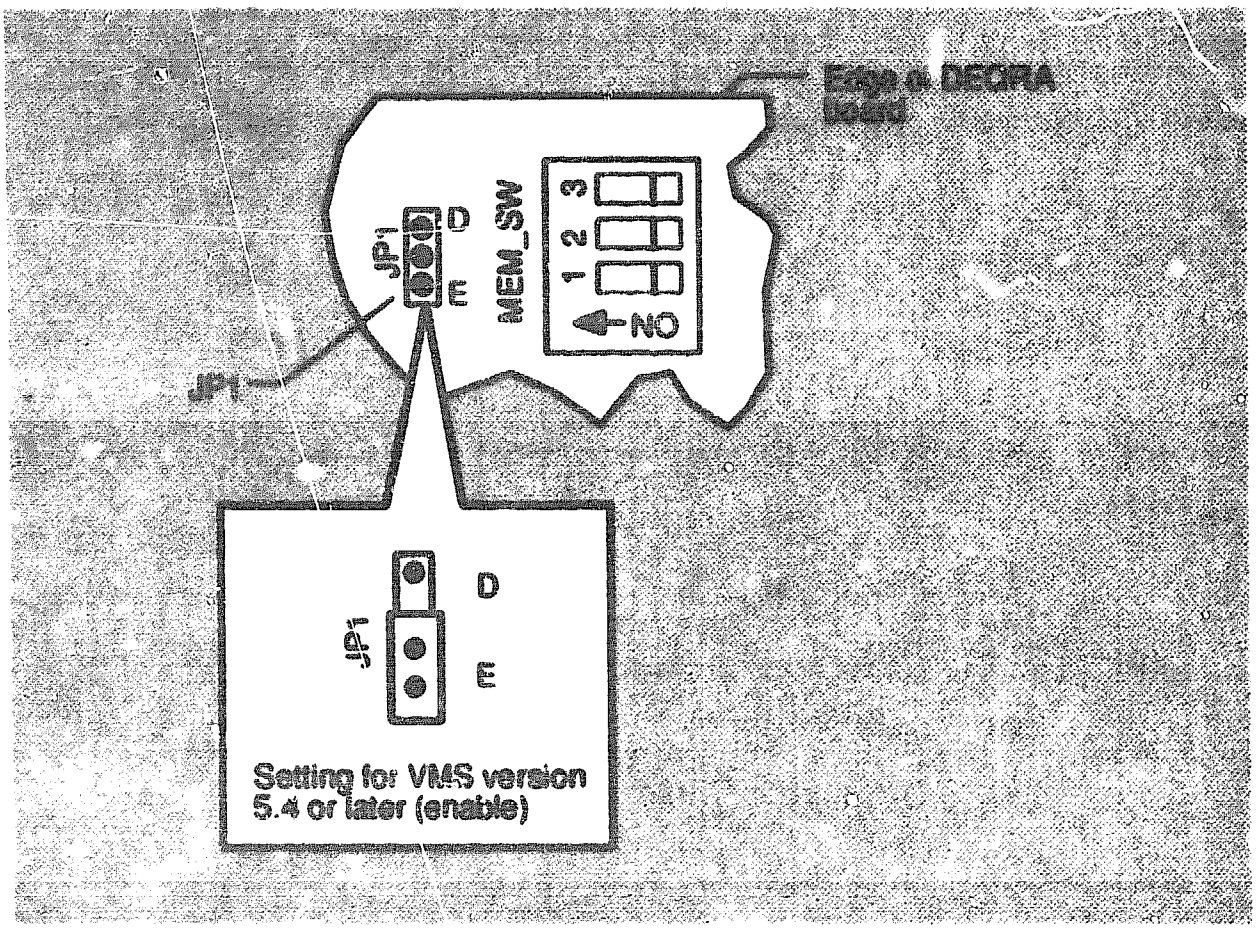
[2] Corresponding address bit

[3] Default address

4.5 Positioning Jumper JP1

Jumper JP1 determines whether the DEQRA's shared memory is visible to the host at powerup. To do so, place JP1 between the center post and the pin labeled "E". See Figure 4–6. The default position for JP1 is "E".

Figure 4–6 Location and Position of Jumper JP1



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4.5 Installing the DEQRA Board

You can mount the DEQRA board in any peripheral position of a BA200/400 series enclosure. The DEQRA requires only one slot for installation. You cannot install more than two DEQRA devices in a single VAX system.

To install the DEQRA board in a BA200/400 series enclosure, use the following procedure:

1. Ensure the host CPU is fully functional.
2. Ensure the host power supply can meet the DEQRA current drain of 5.0 amps at +5 volts dc or 0.1 amps at +12 volts dc.
3. Release the two 1/4-turn captive screws holding the blank cover to the card cage on the slot that will receive the DEQRA board.
4. Pull the blank cover away from the card cage.
5. Check the slot immediately before and after the slot the DEQRA is to be installed into. If a module with a blank bulkhead cover or a flush handle is in either or both slot positions then you must install a gap filler assembly. To install the gap filler assembly refer to Section 4.7.
6. Check the host and backplane slot that will receive the DEQRA board and confirm that the power is off.

NOTE

Make sure that all circuit board positions (slots) in the backplane between the CPU board and the DEQRA board are occupied. All intermediate positions must be occupied by a full board or a bus grant continuity card (M9047) for the bus grant signals to be extended to the DEQRA board

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7. Ensure that the interrupt vector switches (Section 4.4.2), shared memory switches (Section 4.3), CSR address switches (Section 4.4.1), and jumper JP1 (Section 4.5) are configured for the specific installation.
8. Place the DEQRA board in a vertical position with the TRN port at the top and gently slide the DEQRA board into the card edge guides of the selected slot, seating it partially into the backplane.

CAUTION

The DEQRA board will be severely damaged if inserted into the backplane backwards.

Be very careful not to scrape adjacent boards or use undue force. Lack of care may break off components.

ATTENTION

Si vous insérez LE contrôleur DEQRA à l'envers dans LE porte-cartes, vous risqueriez de gravement l'endommager.

Manipulez les composantes avec précautions, sinon vous risqueriez de les briser. Évitez de les entrechoquer avec les modules voisins ou d'exercer une force excessive en les mettant en place.

PRECAUCIÓN

El controlador DEQRA sufrirá daños de consideración si se inserta al revés en la placa posterior de interconexiones ("backplane").

No se deben raspar las placas adyacentes ni presionar demasiado sobre ellas, puesto que pueden partirse sus componentes.

VORSICHT

Die Komponenten aufder DEQRA Karte werden beschädigt, wenn diese verkehrt herum in den Steckrahmen geschoben wird.

Achten Sie darauf, daß Sie bei der Installation andere Module und Karten nicht beruhven, und gehen Sie behutsam vor. Andernfalls können Teile beschädigt werden oder abbrechen.

---

9. Once the DEQRA board is seated and aligned in the backplane, lock the board in place by simultaneously pushing the top release lever down and pulling the bottom release lever up.
10. Fasten the two 1/4-turn captive screws on the DEQRA board handle.

11. Write the slot location of the DEQRA on the system's backplane configuration label. This label is usually located on one of the backplane enclosure covers.

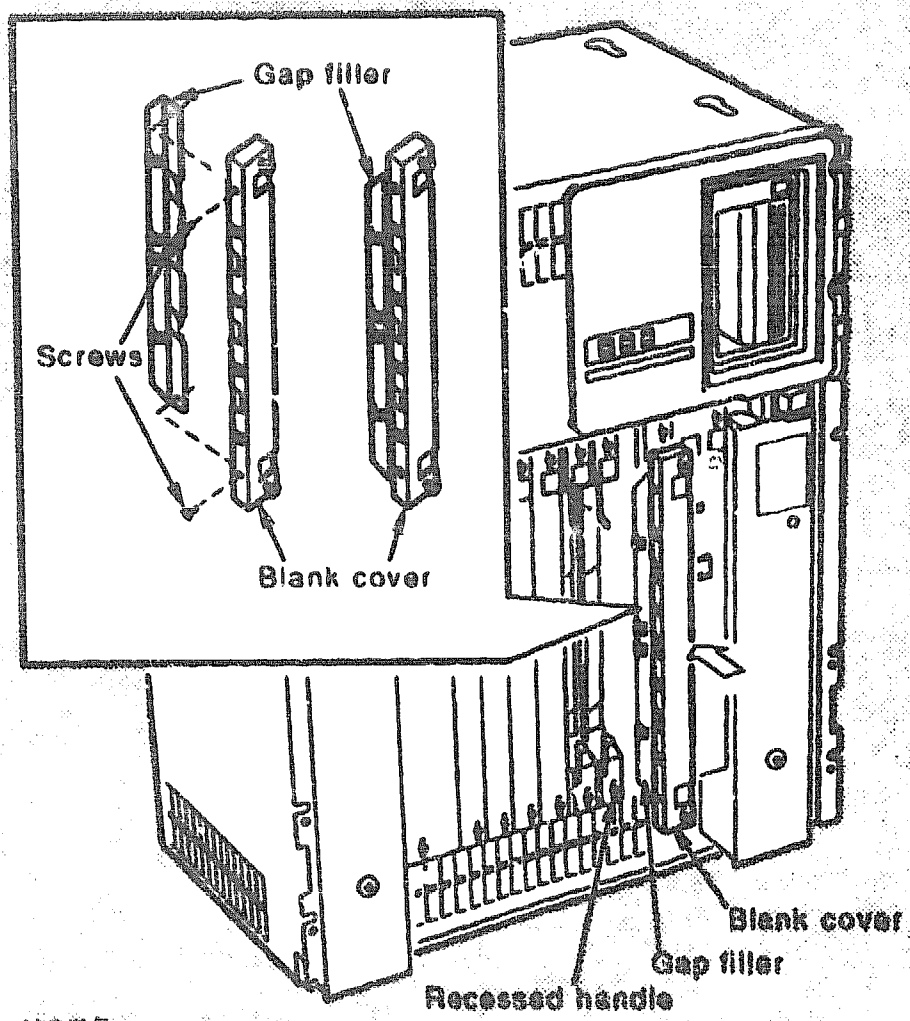
4.7 Installing the Gap Filler Assembly

The gap filler assembly (part number 70-24071-01), supplied with the DEQRA, is required if a module with a blank bulkhead cover or a flush handle is located in the slot immediately before or after the DEQRA's recessed-handle. Without the gap filler assembly, circuitry on the modules are exposed allowing electromagnetic energy to leak to the outside of the enclosure.

Install the gap filler assembly as follows:

1. Using the two screws and one of the gap filler assemblies supplied with the filler panel kit (part number 70-24505-01), attach the gap filler assembly to the top and the bottom of the side of the bulkhead cover or the flush handle that fits next to the DEQRA. Make sure the gap filler assembly fits into the tab indentations on the blank bulkhead cover or the flush handle. See Figure 4–7.
2. Place the blank bulkhead cover with the gap filler assembly on the card edge.
3. Insert the flush handle module with the gap filler assembly attached into the card slot.
4. Ensure that there is correct grounding, with no open spaces between the two modules.
5. Do not fasten the 1/4-turn captive screws until you have installed the DEQRA module.

Figure 4–7 Attaching the Gap Filler Assembly



NOTE:

The gap filler is mounted onto the blank cover to close the open space between the recessed module and the blank cover.

LKG-6734-92I

4.8 Connecting the DEQRA to the Token Ring Network

After you install the DEQRA, connect the DEQRA to the token ring network by using a BN26P, lobe cable. To do this, insert the nine pin d-subminiature end of the lobe cable into the TRN Port in the DEQRA handle and the data connector end of the cable into the token ring network.

With the DEQRA connected to the token ring network, do the following:

1. Perform the powerup procedures in Section 4.9.
2. Install the device driver software. Refer to the *DEC Token Ring Network Device Driver for VMS Installation* for the device driver loading procedure.
3. Start the network.
4. Perform loop tests to verify the DEQRA installation. Refer to *DEC Token Ring Network Device Driver for VMS Use and Programming* for a description of the loop tests.

4.9 Powering Up the DEQRA

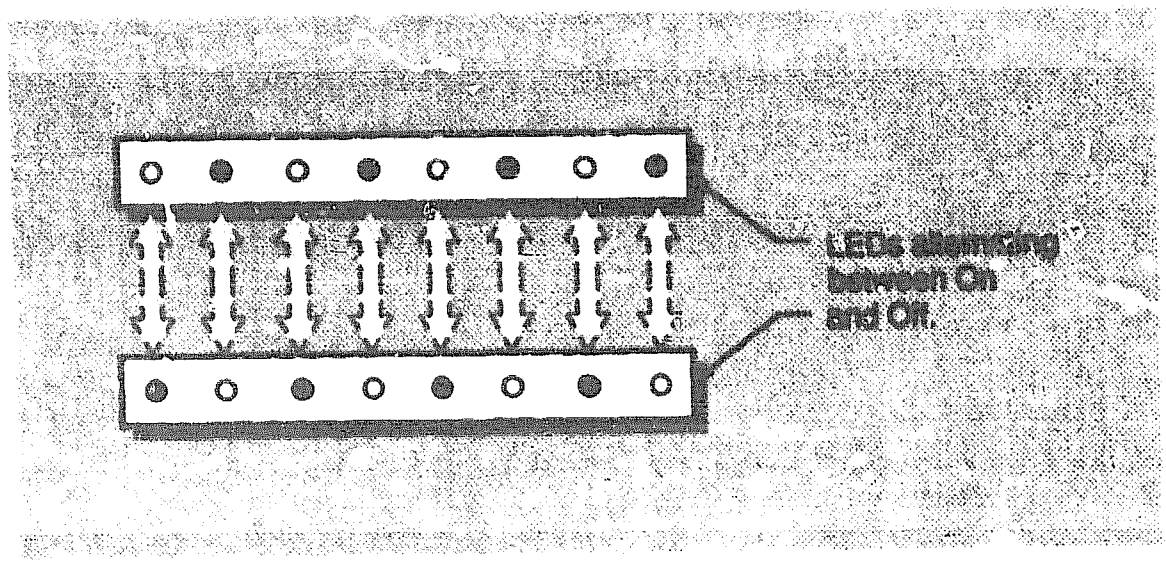
Use the following procedure to power up the host system and run the DEQRA power-up diagnostics used to validate the hardware functionality of the DEQRA board.

1. Apply power to the host system and observe the diagnostic LED light pattern. See Figure 4–1 for LED location. After approximately one minute the LEDs should display an alternating pattern with every other light on, as shown in Figure 4–3.

   This pattern signifies that all diagnostic tests ran without error.
2. If this alternating light pattern is not displayed, push the red RST button on the DEQRA board (see Figure 4–1) to restart the diagnostic tests.
3. If, after one minute, the LED pattern is other than the alternating pattern shown in Figure 4–3, replace the DEQRA board.
4. After you install the DEQRA and initially test it, replace the covers of the host computer securely. This ensures the necessary air flow for all of the boards installed in the host machine. Ensure that all ground straps are in place.

For more information on the powerup and reset diagnostics, refer to Chapter 5.

Figure 4–8 LED Display Pattern for Successful Internal Diagnostics



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5

DEQRA Reset Test Sequence

The DEQRA is reset when:

- The board is first powered up
- The reset button on the board edge is pressed
- A software reset is sent by the host

When the board is first powered up, it is placed in the enable mode, and a long reset is performed. The tests performed during a long reset validate the control circuitry, processor and Z-BUS memory and peripheral devices, interrupt operation, bus error logic, EPROM checksum, and concurrent bus execution features of the DEQRA hardware.

Once the first long reset is completed, an inhibit diagnostics pattern is written into memory, and all subsequent board resets are short unless the board is again placed in the enable mode. The tests performed during a short reset are a basic subset of the tests executed during a long reset. This prevents downloaded code and device setups from being overwritten or altered by a full reset.

During resets, not all possible tests are performed. The TMS test, which sends signals out to the token-ring, is skipped to prevent test signals from inadvertently being sent out onto active lines.

This chapter explains the reset test sequence consisting of:

- Basic checks
- Device tests
- Download preparation

Test status and error reporting may be monitored either by viewing the LEDs or by connecting a terminal to the console port on the board edge.

5.1 Basic Checks

Before the DEQRA executes a reset test, it first executes a set of initialization procedures. The DEQRA then performs the basic system checks to insure the board is operating correctly. These checks include setting up the console port and testing the memory used by the CPU for the vector tables and scratch memory. Table 5–1 lists the basic checks tests and associated LED displays.

In most cases, if a test fails, the diagnostic LED display for that test blinks continuously and the board does not complete the reset sequence; however, for a catastrophic error, the board may be unable to blink the LED display.

Table 5–1 Basic Checks

LED Display During Test	Routine
○○○○●○○○	Disable Shared Memory
○○○●○○○○	Console Initialization
○○●○○○○○	System RAM Test
○○●●○○○○	System Initialization
○○●●●○○○	Finish Basic Tests

5.1.1 Enable or Disable Shared Memory Routine

The enable or disable routine determines the jumper position and enables or disables the shared memory accordingly. If the jumper is in the D position, this routine disables the shared memory.

The DEQRA's shared memory is visible on the host Q–bus following any condition causing a reset. Some host operating systems and hardware platforms require that the shared memory be disabled during the system initialization. Jumper JP1 is used to accomplish this and provide the capability to configure the DEQRA for the target system. Enable is the normal position for JP1.

The successful completion of this test indicates that the following hardware is functioning properly:

- EPROM decoding, selection, and control logic
- 68020 address, data, and control circuitry
- Data acknowledge logic for external devices

LED display during test:

5.1.2 Console Initialization Routine

The console initialization routine initializes the MFP device serial port registers for proper console operation at 9,600 bits and then transmits a character stream to the console. If the character stream is properly displayed on the console, the USART portion of the MFP is operational.

The 68091 multi-function peripheral device contains the universal synchronous /asynchronous receiver transmitter (USART) used as the DEQRA console.

The console port default settings are as follows:

- Number of bits - 8
- Parity - no parity
- Stop bits - no stop bits

The successful completion of this test indicates that the following hardware is functioning properly:

- MFP decoding, selection, and acknowledge logic
- MFP bus interface and USART registers
- RS-232 driver, and console cable (if the character stream is displayed correctly)

LED display during test:

o o o ● o o o o

5.1.3 System RAM Test Routine

The system RAM test routine performs a non-destructive, write-read, test of each RAM location between addresses 800000 and 810000. The test verifies that the memory required for the system stack, vector tables, and program variables are performing correctly. All possible combinations of byte, word, and longword transactions are tested at each byte offset address.

This routine does not depend on RAM. The routine uses the processor's registers to store all temporary values. The test is non-destructive since the contents of each memory location is saved before being overwritten with the test patterns. Each location is restored with its initial contents after it has been tested.

The successful completion of this test indicates that the following hardware is functioning properly:

- Data acknowledge logic for the memory system
- 68020 private memory controller, address multiplexers, and refresh logic
- 68020 dynamic bus sizing logic

LED display during test:

5.1.4 System Initialization Routine

The system initialization routine initializes the system stack, the vector table, the test status variables, and the variables used by the ODT68 debugging tool.

LED display during test:

o o ● ● o o o o

5.1.5 Finish Basic Tests Routine

The finish basic tests routine examines the contents of the short reset tests memory location to determine whether the confidence tests should be executed or skipped.

The confidence tests are always executed during a long initialization, but they are not run during a short initialization. By default, the confidence tests are enabled at power-up, and the confidence tests are run as part of the initialization process. After the confidence tests have been completed (after the start bootloader routine) the confidence tests are inhibited.

If the confidence tests are enabled, the next test to be executed is the bus error test. If the confidence test is inhibited, the start bootloader routine is executed. The confidence tests are inhibited as part of the start bootloader routine.

LED display during test:

o o ● ● ● o o o

5.2 Device Tests

Device tests are performed by the DEQRA board during a long reset. The tests are performed after the basic checks have successfully completed. Below is a list of the device tests shown in the order they are executed. For an in-depth description of each device test, refer to the *DEC TRNcontroller 100 Description and Debugging* manual.

1. Bus Error
2. EPROM
3. MFP 68901
4. CPU-bus RAM
5. Z-BUS RAM
6. CIO Z8036
7. Token-Ring RAM
8. TMS380™
9. Interrupt

Table 5–2 illustrates the device tests and the associated LED displays. The device tests are not performed during a short reset, the board prepares to download an application instead.

In most cases, if a test fails, the diagnostic LED display for that test blinks continuously and the board does not complete the reset sequence; however, for a catastrophic error, the board may be unable to blink the LED display.

Table 5–2 Device Tests

LED Display During Test	Test or Routine
oeeeeeee	Bus Error Test
oeeeeeeo	Bus Error Test *cont'd*
oeeeeeoo	EPROM Checksum Test
oeeeeeoe	Checksum Test *cont'd*
oeeeeeeo	Checksum Test *cont'd*
oeeeeeoo	MFP 68901 Test

(continued on next page)

Table 5–2 (Cont.) Device Tests

LED Display During Test	Test or Routine
○●●●○○○●	MFP 68901 Test *cont'd*
○●●●○○●○	MFP 68901 Test *cont'd*
○●●●○●○○	Restore Console
○●●●●○○○	CPU-bus RAM Test
○●●●●○○●	CPU-bus RAM Test *cont'd*
○●●●●○●○	CPU-bus RAM Test *cont'd*
●○○○○○○○	Z-BUS RAM Test
●○○○○○○●	Z-BUS RAM Test *cont'd*
●○○○○○●○	Z-BUS RAM Test *cont'd*
●○○○●○○○	Token-Ring RAM Test
●○○○●○○●	TMS380 Test
●○○○●○●○	Interrupt Test

5.3 Download Preparation

After the basic checks and the device tests have successfully completed, the DEQRA board is ready for an application to be downloaded. In preparing for the download process, the start bootloader routine executes the INHIBIT command to disable future device test execution, transmits the firmware revision level to the console, initializes the CIO for use as the DEQRA's host interface CSR, and starts the bootloader routine.

Table 5–3 illustrates the download preparation tests and the associated LED displays.

In most cases, if a test fails, the diagnostic LED display for that test blinks continuously and the board does not complete the reset sequence; however, for a catastrophic error, the board may be unable to blink the LED display.

Table 5–3 Download Preparation

LED Display During Test	Routine
●●●●●●●●	Start Bootloader
●●●●●●●●	Bootloader Processing
●●●●●●●●	Bootloader Processing
●●●●●●●●	Downloading Application
●●●●●●●●	Download Complete

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