DELQA

digital™

Technical Manual

Order Number: EK-DELQA-TM-001

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of
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PREFACE

The DELQA module is a communications option which connects the Q-Bus to an Ethernet (IEEE 802.3 10BASE2) local area network (LAN).

This manual describes how the DELQA communications module functions internally. It provides information on the main hardware components and data paths within the module.

This manual is intended for use by Digital Field Service Support and experienced Customer engineers.

NOTE
Installation, programming and diagnostic information is contained in the Delqa User's Guide. EK-DELQA-UG.

The chapters are as follows:

CHAPTER 1 introduces the DELQA module.

CHAPTER 2 describes the main operations of the DELQA module, and the system port interface to the Q-Bus.

CHAPTER 3 describes how the components of the DELQA module work together on the backport bus.

APPENDIX A summarises the details of the principal Integrated Circuits in the DELQA module.

APPENDIX B describes the Ethernet Network Management protocol.

Notes and Warnings Notes and warnings are defined as follows:

- A **NOTE** contains general information
- A **WARNING** is designed to prevent personal injury.

Related publications

Communications Options Mini-Reference Manual: Volume IV (Ethernet) (EK-CMINI-RM)

DECnet Maintenance Operations Protocol (MOP) Functional Specification V3.0.0 (AA-X436A-TK)

DECnet-RSX System Manager's Guide (AA-H224C-TC)

DECnet-VAX System Manager's Guide (AA-H803C-TE)

DELQA Field Maintenance Print Set (MP-02379-01)

Ethernet: A Local Area Network, Data Link Layer, and Physical Layer Specifications (AA-K759B-TK)

Ethernet Installation Guide (EK-ETHER-IN)

H4000 Ethernet Transceiver Technical Manual (EK-H4000-TM)

Introduction to Local Area Networks (EB-22714-18)

NOTE

When installed in a Micro-PDP11 or a MicroVAX, this equipment has been tested with a Class A computing device and has been found to comply with part 15 of FCC Rules. Operation in a residential area may cause unacceptable interference to radio and TV reception requiring the operator to take whatever steps are necessary to correct the interference.

CHAPTER 1
INTRODUCTION

1.1 SCOPE

This chapter introduces the main functions of the DELQA (Digital Ethernet Local-Area-Network to Q-Bus Adapter), and its main components. The sections are as follows:

Section 1.2 **FUNCTIONAL OVERVIEW**
Section 1.3 **TECHNICAL OVERVIEW**

1.2 FUNCTIONAL OVERVIEW

The DELQA module is a DIGITAL Ethernet Local Area Network to Q-Bus Adapter. It fits on the Q-Bus as a communications option for connecting processors from the PDP-11 and MicroVAX families to an Ethernet or IEEE 802.3 local area network (LAN).

1.2.1 Normal Mode and DEQNA-Lock Mode

The DELQA module operates in one of two switchable modes: Normal mode or DEQNA-lock mode.

In **Normal mode**, DELQA supports the following functions:

- Maintenance Operations Protocol (MOP) messages for Remote BOOT, Request ID, Transmit System ID and Loopback.
- IEEE 802.3 Maintenance Messages for XID (Transmit ID) and TEST on NULL LSAP (Link-layer Service Access Point) access points
- Self-test on powerup and via host command.
- Single Ethernet physical address (the first of any specified in a setup packet to replace the default held in Station Address ROM)
- Multiple Ethernet Multi-cast addresses
- All standard DEQNA functions, except multiple Ethernet physical addresses and the automatic enabling of the on-board sanity timer at powerup.

In **DEQNA-lock mode**, DELQA provides functional compatibility with DEQNA modules, but at the expense of losing some Normal mode functions. The functions supported are:

- Multiple Ethernet physical addresses
- Multiple Ethernet Multi-cast addresses
- Sanity timer (Switch enabled on powerup).

The operating mode is selected at powerup by the setting of the mode switch (S3) on-board the DELQA module.

If mode switch S3 is closed, the module operates in Normal mode; subsequently, host software can use the Vector Address Register (VAR15) to set the operating mode to either Normal mode or DEQNA-lock mode. If mode switch S3 is open, the operating mode is fixed as DEQNA-lock, and this cannot be altered by software. Use of DEQNA-lock mode is not recommended.

Host software can determine whether the module is a DELQA or a DEQNA by using bit 0 in the Vector Address Register.

1.2.2 Module Interfaces

The DELQA is a microprocessor-based device which provides all the logic necessary to connect to the Ethernet. It acts as a data communications controller, executing the physical layer protocol and part of the data link layer protocol (as defined by the seven-layer OSI model). The protocol functions include synchronisation, format conversions, encoding and decoding, formatting data packets and data link management.

The DELQA enables programs that execute higher levels of protocol, such as DECnet, to communicate with their peers over the Ethernet link.

The DELQA module performs all the channel access functions necessary to achieve maximum throughput with minimum intervention from the host processor, including:

- Block-mode Direct Memory Access (DMA) to host memory
- Control DMA, which uses Buffer Descriptor Lists (BDLs) in host memory to sequence transfers between data buffers in the host and in the DELQA.

The DELQA implements some of the Maintenance Operation Protocol (MOP) functions on request from a remote station without host intervention. These functions include host reboot, loopback operations, and system identification.

1.2.3 Module Operations

The DELQA module transfers data between buffers in host memory and the Ethernet transceiver. The main data flow operations are as follows:

1. Transfer of data between host memory buffers and shared RAM in the DELQA.
2. Conversion of data and status information between the host format and that used in the DELQA module.
3. Transfer of formatted data packets between shared RAM and the Ethernet connector.

The data is formatted in packets of between 60 and 1514 data bytes at a higher level of protocol. The DELQA module calculates and appends a four byte CRC (Cyclic Redundancy Check) to transmit packets, and strips the CRC from receive packets. Therefore, the full length of a packet on the Ethernet is between 64 and 1518 bytes.

Figure 1–1 shows how transmit and receive data is passed between the main functional components of the DELQA module.

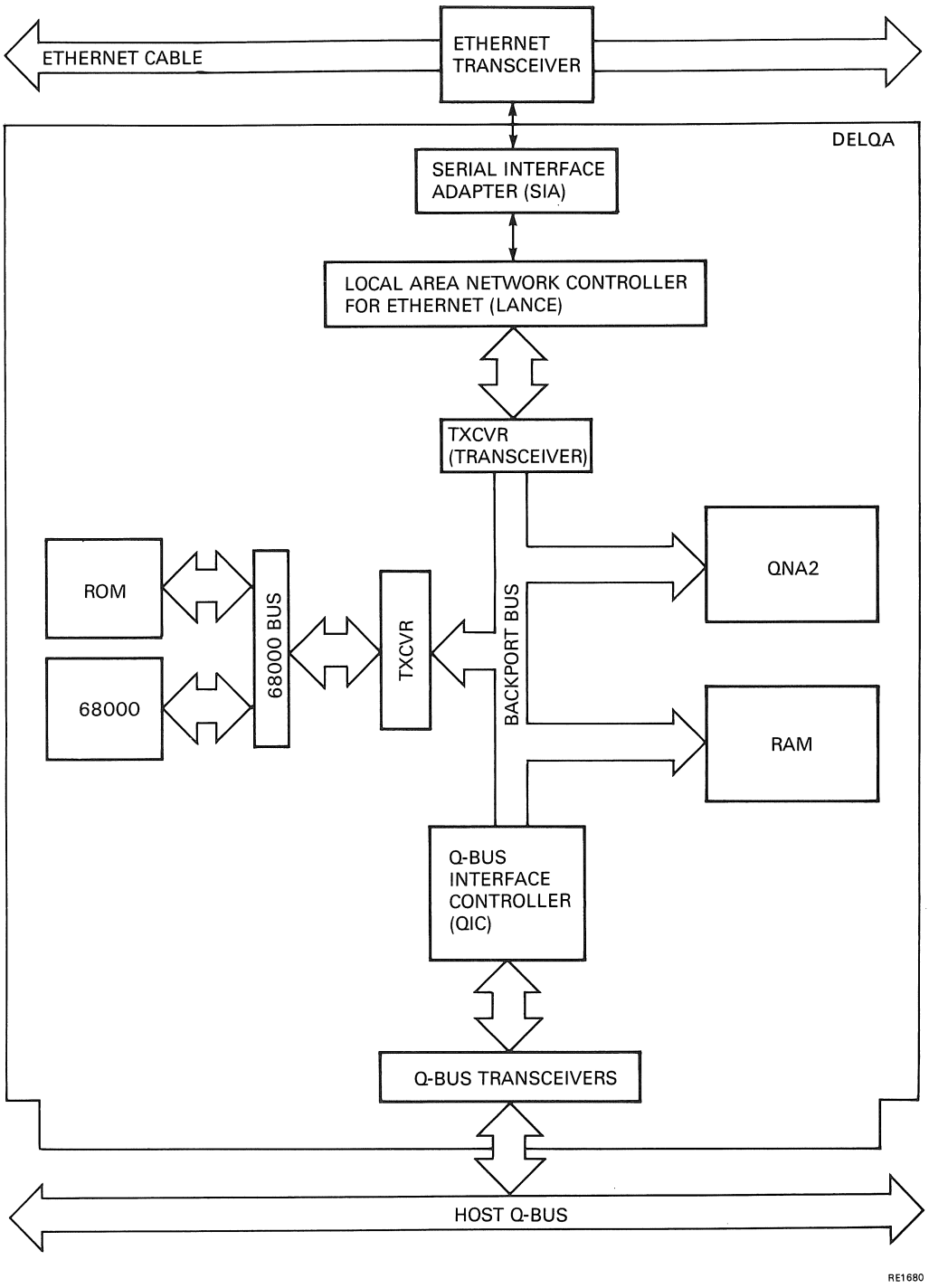


Figure 1–1 DELQA Functional Block Diagram

1.2.4 Protocol Functions

The Physical Channel Functions and the Data Link Functions are described in this section.

1.2.4.1 Physical Channel Functions

The DELQA module transmits and receives at 10 Mbit/s. It provides physical channel functions that are specific to Ethernet and necessary for the interface to the DIGITAL H4*xxx* Ethernet transceiver. DELQA executes the following functions:

During transmission

- Encodes serial data in Manchester format
- Recognises heartbeat signals from the DIGITAL H4*xxx* transceiver, verifying that the transceiver is monitoring collision detect signals
- Monitors the self-test collision detect signal from the DIGITAL H4*xxx* Ethernet transceiver.

During reception

- Senses transmission carrier from any Ethernet station
- Decodes the incoming serial bit-stream from its Manchester format.

1.2.4.2 Data Link Functions

The DELQA module provides the following Ethernet-specific functions at the data link layer:

During transmission

- Generates the 64-bit preamble for synchronisation
- Provides parallel-to-serial conversion of the frame
- Calculates the 32-bit CRC value and places it in the packet sequence field for transmission
- Attempts automatic, multiple re-transmissions upon receiving a collision detect signal.

During reception

- Checks the 32-bit CRC value in each incoming packet
- Performs address filtration, either to match an incoming message to the physical address of the module, or to accept messages broadcast to a group of stations
- Synchronises to the preamble, and removes it prior to processing
- Provides serial-to-parallel conversion of the frame.

The Ethernet provides a datagram service; that is, sending a packet does not guarantee that it will reach its destination. The software for the protocol layers above data link is responsible for checking that a packet has been received, and for recovering from conditions where it has not been received.

1.2.5 Q-Bus Interface

As bus master of the Q-Bus, the host can program the DELQA module by means of eight word-length registers in the I/O page of the Q-Bus memory map. The DELQA acts as bus slave to support access from the Q-Bus to these on-board locations.

Four of the I/O page addresses are write-only registers, used to pass the start addresses of the BDLs for transmit and receive buffers. Two are read/write registers: the Control and Status Register (CSR) and the Vector Address Register (VAR).

The lower bytes of each of the first six addresses are read-only registers, used to access the Station Address (SA) ROM. The SA ROM contains the 48-bit physical address of the DELQA module in the Ethernet LAN.

The DELQA can act as bus master to the Q-Bus, in order to implement DMA transfers (either block mode or non-block mode) between RAM on-board the DELQA and BDLs or data buffers in host memory.

Figure 1–2 shows the Q-Bus memory map for the DELQA module.

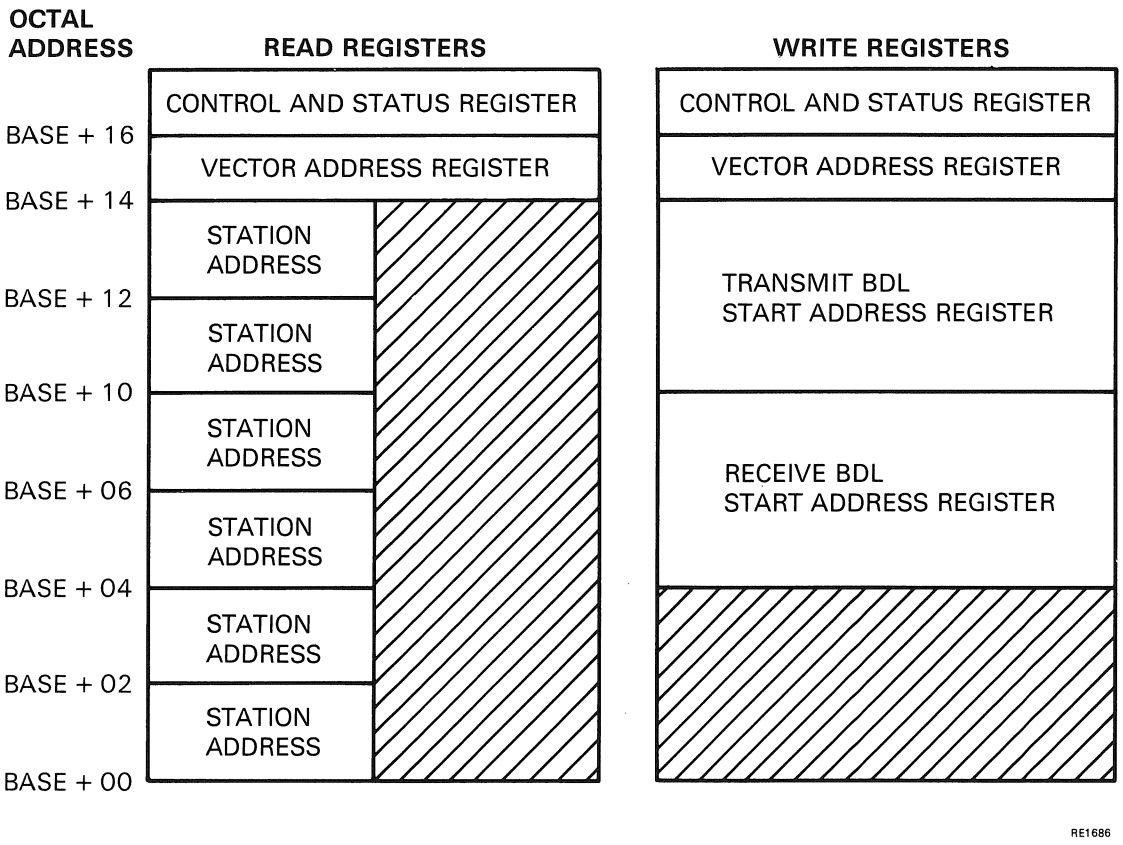


Figure 1–2 Host I/O Page Map

1.3 TECHNICAL OVERVIEW

The DELQA option comprises one dual-height Q-Bus module, a bulkhead interconnect panel and associated cables. The DELQA module plugs into the Q-Bus backplane and fits into the Q-Bus enclosure. It is physically and electrically connected to the H4*xxx* transceiver using the bulkhead panel assembly and the appropriate transceiver cable.

1.3.1 Module Components

On the DELQA board there are five main integrated circuits to perform the main module operations (refer to Section 1.2.3). These operations are controlled by the on-board microprocessor. Data storage is provided by shared RAM. Figure 1–3 shows the major components of the DELQA module and their interconnections.

1.3.1.1 Integrated Circuits

The principal integrated circuits in the DELQA module are:

1. **Q-Bus Interface Controller (QIC)**

   This gate array provides a DMA path between the host system memory and the shared memory on the DELQA board, and between SA ROM and host memory. The QIC also allows the host system access to the internal registers of the DELQA.

2. **68000 Microprocessor**

   This is the 16-bit microprocessor which controls the DELQA and performs the necessary conversions of the frame data between host buffer format and Ethernet packet format.

3. **Q-Bus Network Arbitrator (QNA2)**

   This gate array provides access to the backport bus, arbitrating between the QIC, the 68000 microprocessor, and the LANCE.

4. **Local Area Network Controller for Ethernet (LANCE)**

   This is a VLSI circuit which performs bidirectional DMA between shared RAM and the Serial Interface Adapter (SIA).

5. **Serial Interface Adapter (SIA)**

   This is a VLSI circuit which links the LANCE to the H4*xxx* Ethernet transceiver. The SIA provides Manchester encoding of data transmitted, and decoding of data received.

1.3.1.2 On-board Memory

The DELQA module contains both preprogrammed ROM and static RAM, as follows:

1. Firmware ROM contains 12Kwords of Master Control Program for the module (executed by the 68000 microprocessor). In addition the firmware ROM contains 4Kbytes of self-test diagnostic code and 4Kbytes of PDP-11 boot/diagnostic code for a PDP-11 host. (MicroVAX systems provide equivalent boot/diagnostic code for their own host system ROM).

2. Station Address (SA) ROM. (32 bytes) contains, in the first six bytes, the default physical address of the DELQA module. The SA ROM also contains a 2 byte checksum which is accessible to host software.

3. Shared RAM (16Kwords) provides the memory for data packet buffers, Buffer Descriptor Lists (BDLs) the Vector Address Register, the LANCE initialisation block (which includes the physical address of the module) and firmware data structures.

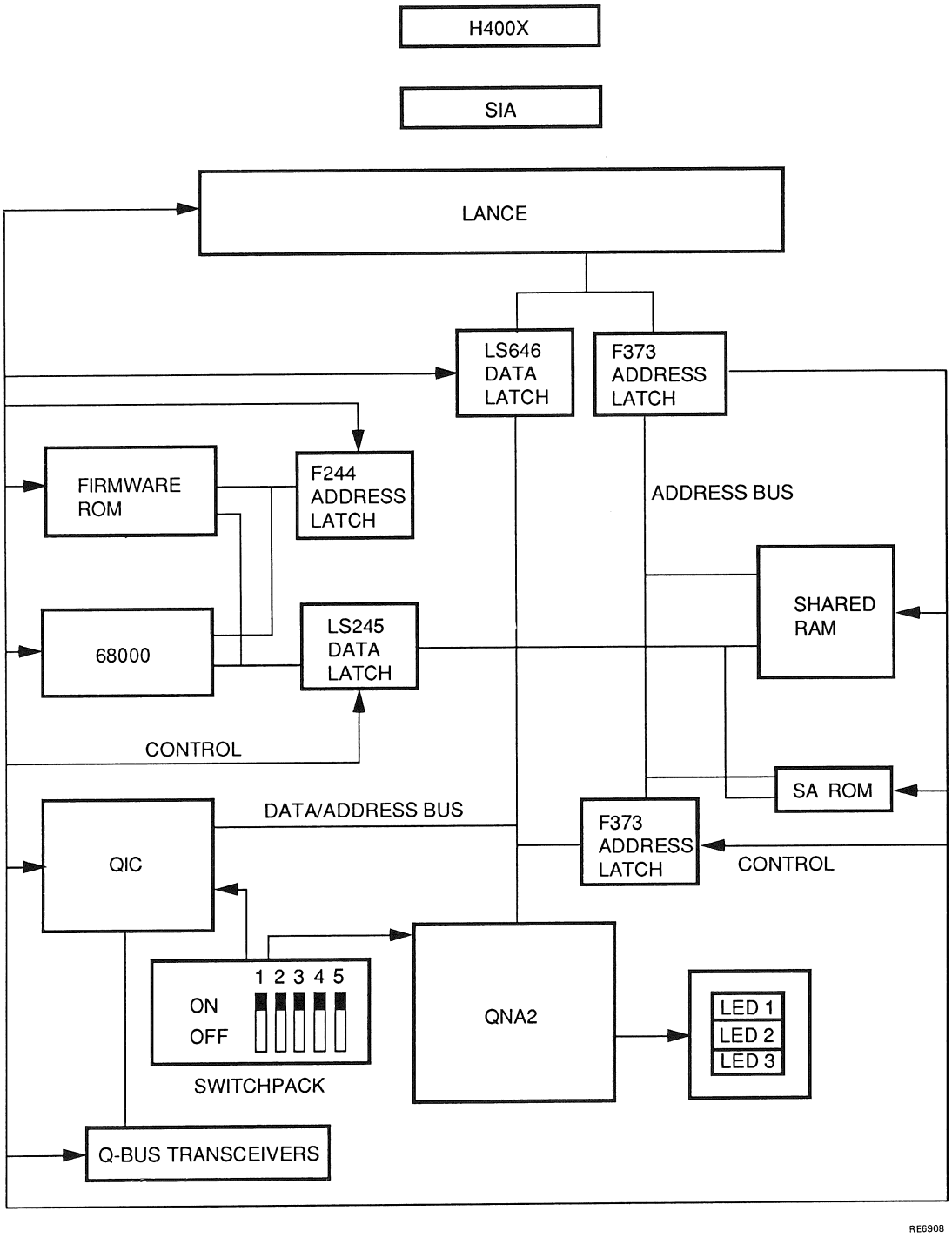


Figure 1–3 DELQA Hardware Block Diagram

1.3.2 Module Processing Operations

The operation of the DELQA can be broken down into processing modules, as follows:

1. The QIC transfers data between Q-Bus memory and shared RAM, as follows:
   - Block-mode (or non-block-mode) DMA (block size up to 16 words) to transfer data buffers directly to and from shared RAM

- Control DMA (block size up to four words) to transfer control information and Buffer Descriptor List (BDL) entries. Control DMA does not use block-mode.

2. The 68000 microprocessor translates data and status information between the format recognised by the host system and that recognised by the LANCE.
3. The QNA2 provides access to the backport bus, arbitrating between (in order of priority): the QIC, the 68000 microprocessor, and the LANCE. It also provides all the gating and strobing signals necessary for these devices to access shared memory.
4. The LANCE and the SIA operate together to transfer the translated packets between shared RAM and the H4*xxx* Ethernet transceiver.

   The SIA uses Manchester coding to encode transmitted data and decode received data. The SIA detects and synchronises with incoming data, and passes it on to the LANCE. The LANCE checks the destination address, and, if it matches any of the module addresses, transfers the data direct by DMA into shared RAM.
5. The 68000 microprocessor controls the operation of the DELQA module, including chip initialisation and module self-test (implemented on powerup or initiated by host software).

1.3.3 Network Integrity Functions

The DELQA module provides the following features for network integrity:

- Quick-verify self-test diagnostics for powerup, boot, and via host command.
- Sanity timer to monitor host software
- Controller loopback
- Maintenance Operations Protocol (MOP) messages for Remote Monitor Console (RMC) operations: Remote BOOT, Request ID, Transmit System ID
- Maintenance Operations Protocol (MOP) messages for Ethernet Channel Test (ECT): Loopback
- Maintenance Operations Protocol (MOP): datalink counters, maintained and stored by DELQA
- IEEE 802.3 Maintenance Messages for XID (Transmit ID) and TEST on NULL Link-layer Service Access Points (LSAPs).

To assist in fault diagnosis and network management, the DELQA can also operate in promiscuous addressing mode. Effectively, this disregards the internal address filter logic. This allows the DELQA to accept all packets received from the network, and to verify the integrity of the received data by performing a 32-bit CRC check on each received packet. All transmissions (normal, loopback, and Setup) reset the sanity timer without affecting its status (enabled or disabled).

1.3.3.1 Self-test Diagnostics

In Normal mode, the DELQA executes a comprehensive self-test on powerup. This takes approximately five seconds to complete.

The firmware ROM on the DELQA contains 4 KBytes of PDP-11 boot/diagnostic code. If the module is controlled by a PDP host, the host can execute this code in order to increase fault coverage. This enables the DELQA to determine that it is operating correctly, before it attempts to access the Ethernet.

1.3.3.2 Sanity Timer

The sanity timer acts as a check that the host software is operating effectively. If the host communications driver fails to reset the timer periodically, the timer initiates a system reboot at the host.

1.3.3.3 Controller Loopback Modes

In internal loopback, the DELQA loops all messages through the module, and the host can neither send nor receive Ethernet messages.

Internal loopback may be entered either by the host command (set CSR08) or at device powerup. The behaviour of the device differs according to its mode.

- **In Normal mode**, the characteristics of internal loopback depend upon how loopback was initiated.
  a. From Host command, no Ethernet access is possible.
  b. From device powerup, certain types of MOP messages may be processed by the DELQA (that is; MOP boot if enabled by S4, Ethernet loop channel, and Request System ID).
- **In DEQNA-lock mode**, no Ethernet access is possible.

1.3.3.4 Remote Console Commands

When operating in Normal mode, the DELQA responds to the following MOP remote console commands:

- System Identification Request from another Ethernet station. The DELQA sends the current System ID parameters from shared RAM
- System ID Transmission is sent periodically to a Multi-cast Ethernet address
- Remote Trigger command from another Ethernet station. The DELQA verifies the request, and then causes the host system to reboot by negating BDCOK on the Q-Bus interface in order to simulate a powerup restart.

1.3.3.5 Ethernet Channel Loopback

DELQA recognises Ethernet loopback test messages. The module checks to determine whether to forward or return the incoming message. Messages are received, decoded, and re-transmitted by DELQA independently of host software. Normal messages are passed through as usual.

CHAPTER 2
FUNCTIONAL DESCRIPTION

2.1 SCOPE

This chapter describes the main operations of the DELQA module, and its system port interface with the Q-Bus. The sections are as follows:

Section 2.2 **MODULE OPERATIONS**
Section 2.3 **SYSTEM PORT INTERFACE**
Section 2.4 **NETWORK SUPPORT**

2.2 MODULE OPERATIONS

The DELQA module transfers data between buffers in host memory and the Ethernet transceiver. The main operations are as follows:

1. Transfer of data between host memory buffers and shared RAM in the DELQA.
2. Conversion of data and status information between host format and that used in the DELQA module.
3. Arbitration of access requests on the backport bus.
4. Transfer of encapsulated data packets between shared RAM and the Ethernet connector.
5. DELQA module control.

The data is brought together at a higher level of protocol to form packets of between 60 and 1514 data bytes. The DELQA module calculates and appends a four byte CRC to transmit packets, and strips the CRC from receive packets. Therefore, the full length of a packet on the Ethernet is between 64 and 1518 bytes.

2.2.1 Q-Bus Transfers

The QIC is a dual-ported device: one set of data and address lines is connected to the Q-Bus; the other interfaces with the backport bus in the DELQA module. In the data DMA path, each port is double buffered, and each port is controlled by sequencer logic in the QIC.

The QIC supports DMA between the Q-Bus and shared RAM:

1. Block-mode or (non-block-mode) data DMA.
2. Non-block-mode control DMA.

These two types are described in the next sections.

2.2.1.1 Data DMA

The QIC can execute up to 16 words of block-mode DMA between Q-Bus system memory and shared RAM each time it acquires control of the Q-Bus. The transfer must consist of either read only instructions, or write only instructions.

When executing DMA transfers to block-mode memory, the QIC relinquishes the backport bus whenever:

1. The transfer reaches a 16 word boundary.
2. Another device is requesting the Q-Bus when the transfer reaches a 7 word boundary. This causes the QIC to relinquish the bus at the 8 word boundary.

2.2.1.2 Control DMA

The QIC can also handle up to four words of control DMA, using mixed read and write instructions to access BDLs. This is known as control DMA; it is used to transfer status information as well as to access descriptors, as follows:

1. Buffer Descriptor Fetch. This instruction acquires the Q-Bus, executes one non-block-mode write and three block-mode read instructions, then relinquishes the Q-Bus.
2. Chain Descriptor Fetch. As for Buffer Descriptor Fetch.
3. Store status. This instruction acquires the Q-Bus, executes two non-block-mode write instructions, then relinquishes the Q-Bus.

2.2.1.3 Non-block-mode DMA

When executing transfers to non-block-mode memory, the QIC relinquishes the Q-Bus whenever it reaches a four-word boundary.

2.2.1.4 Data and Status Conversion

The 68000 microprocessor handles:

1. Formatting of buffers for transmission.
2. Reformatting of packets received from the Ethernet.
3. Conversion of status information for both transmit and receive messages.

Figure 2–1 shows the data transfers involved in formatting the message data.

2.2.2 Backport Bus Arbitration

The QNA2 controls access to the backport bus on the DELQA module, arbitrating between access requests from the QIC, the 68000 microprocessor, and the LANCE. The QNA2 provides all the gating and the strobing signals necessary for these devices to access the shared RAM.

Figure 2–2 shows the control and gating signals that the QNA2 generates to control the backport bus.

2.2.3 Ethernet Transfers

Ethernet transfers are handled by the LANCE (Local Area Network Controller for Ethernet) in conjunction with the SIA (Serial Interface Adapter).

2.2.3.1 Transmission

When the 68000 has translated a data frame into a packet suitable for transmission, the LANCE transfers it by DMA from the shared RAM to the SIA. The SIA Manchester encodes the data, and sends the packet using the Ethernet connector and bulkhead assembly to the Ethernet.

2.2.3.2 Reception

When the SIA detects activity on the Ethernet, it synchronises with the preamble of the incoming message. The SIA then decodes the data and transfers the packet to the LANCE. The LANCE filters the destination address. If the address on the incoming packet matches one of the addresses in module memory, the LANCE transfers the data by DMA to the RAM.

2.2.4 Master Module Control

The 68000 microprocessor executes the master control program for the DELQA module. The master control program is held as firmware in the ROM associated with the microprocessor on the 68000 bus, and executes the following functions:

1. Conversion of control and status information.
2. Initialisation of QIC and LANCE on powerup.
3. DELQA self-test on powerup or initiated by host.
4. Interrupt control.

The QNA2 contains the CSR (Control and Status Register), and the DELQA IR (Interrupt Register) for the DELQA module.

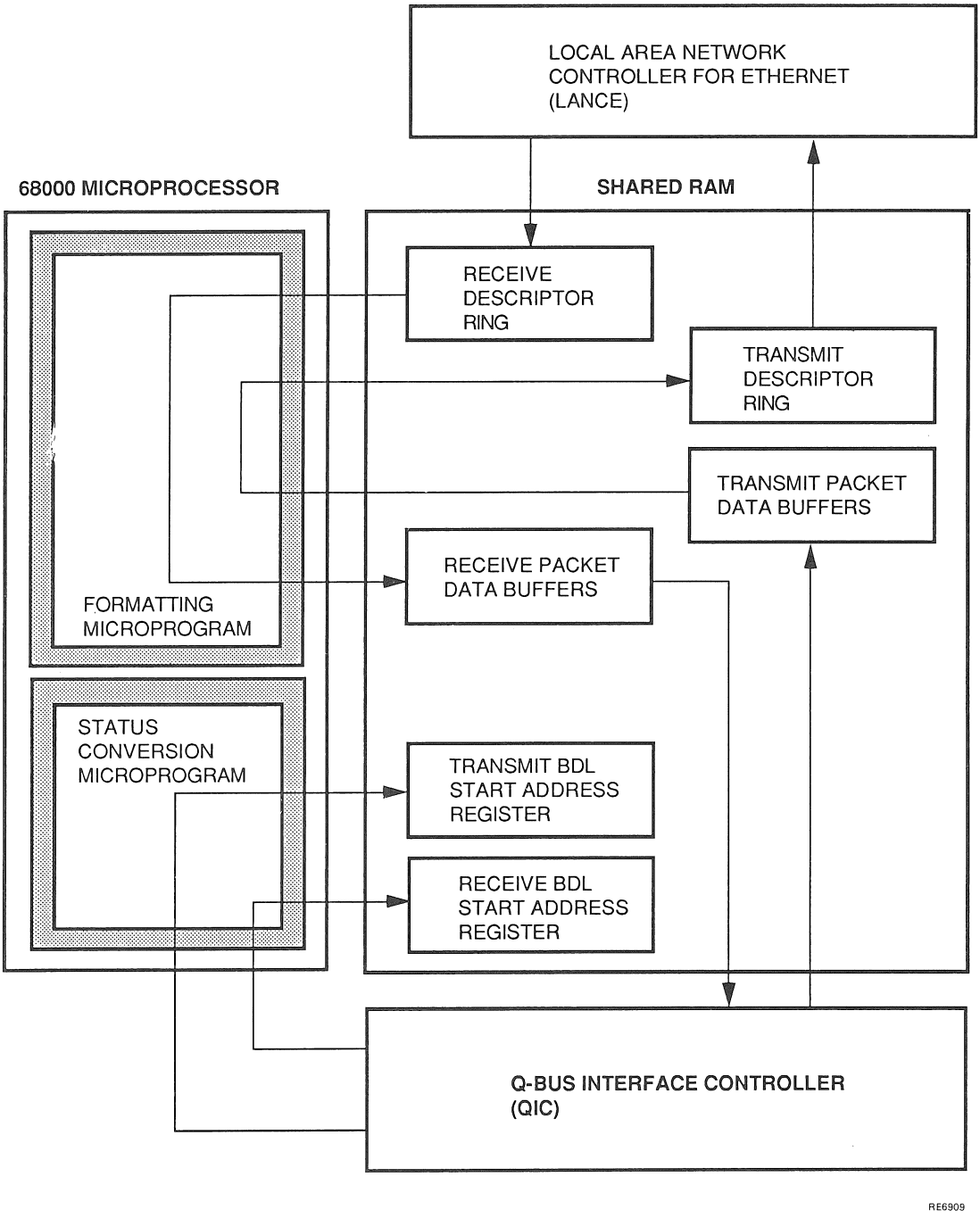


Figure 2–1 DELQA Data Path

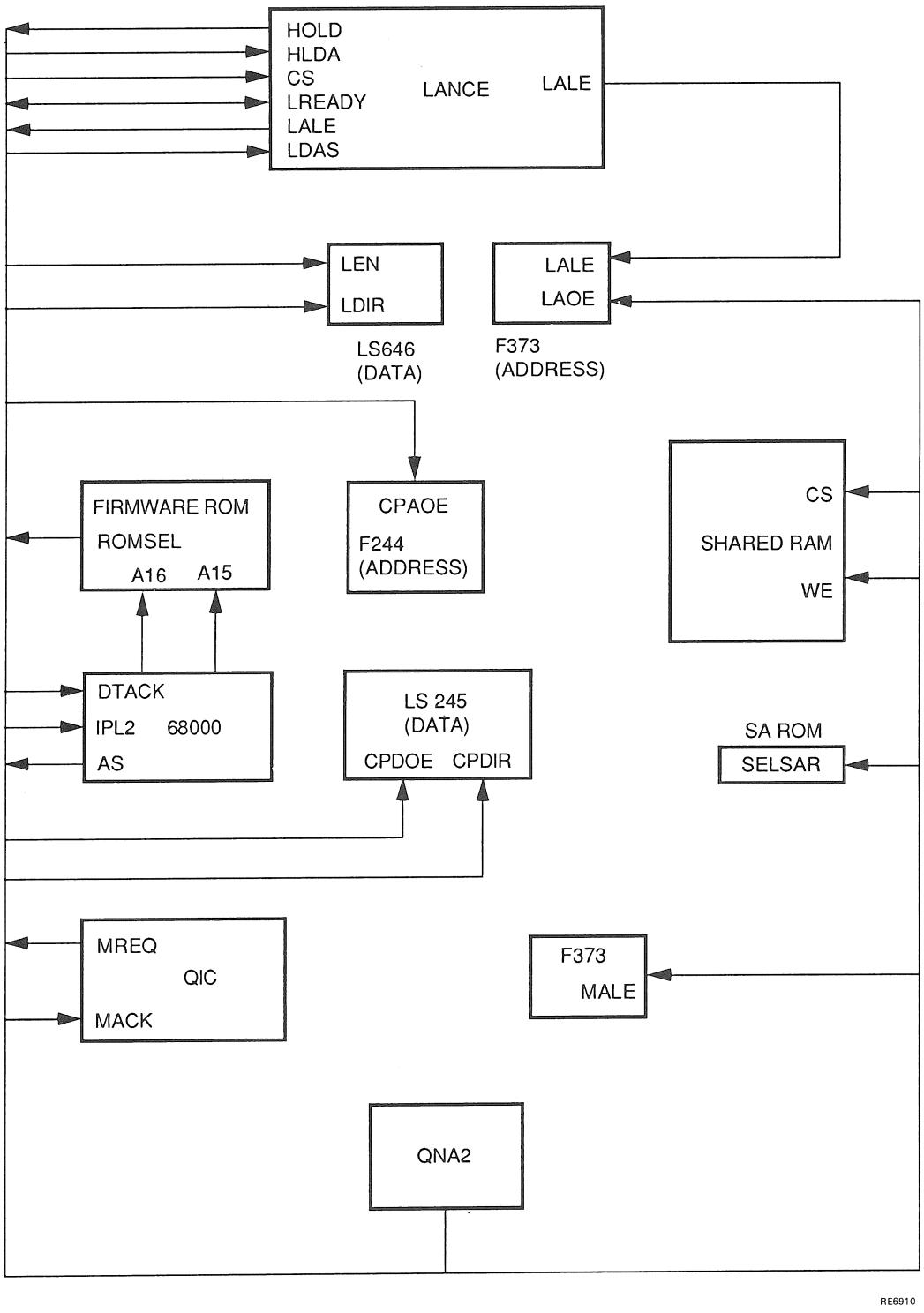


Figure 2–2 Backport Control Functions

2.3 SYSTEM PORT INTERFACE

The DELQA is accessed through twelve registers which are mapped into the Input/Output page of Q-Bus address space in the host system. When it receives the valid address of one of the registers from the bus master, the DELQA responds as a bus slave.

2.3.1 Port Registers

The address mapping implemented by the QIC enables the host system to access the following internal registers in the DELQA:

1. **Control and Status Register (CSR).**

   This is a one-word, read/write register held in the QNA2.

2. **Vector Address Register (VAR).**

   This is a one-word, read/write register held in the shared RAM.

3. **Receive BDL Start Address Register.**

   Transmit BDL Start Address Register (BDL SARs).

   These are two-word, write-only registers that are maintained by the host in shared RAM.

4. **Station Address ROM.**

   This is a set of six read only memory bytes (the lower bytes of the first six words in the DELQA space).

All the registers are word addressable only. The 68000 microprocessor can access these registers directly from the backport bus.

2.3.2 Memory Map

The host system can access the DELQA registers as a block of eight word addresses in the Input/Output page.

The base page address is selected by switch settings on the module. There are five switches on the DELQA board: S1 to S5. S1 selects the I/O base page address for the module, as listed in Table 2–1.

Table 2–1 DELQA Unit I/O Base Addresses

S1	Base Address	Unit	Module
CLOSED	17774440	DELQA 1	DELQA or DEQNA
OPEN	17774460	DELQA 2	DELQA or DEQNA

2.3.3 Setup

The setup packet is the only mechanism, other than the DELQA control registers (CSR and VAR), by which the host software can send commands, status, and control functions to the DELQA module.

The setup packet can be used to initialise the following functions within the DELQA module.

- Multi-cast address or promiscuous filtering for address recognition
- Timeout value for the sanity timer
- Up to 14 sixbyte Ethernet addresses that the DELQA module is to recognise
- MOP configuration and control.

2.3.3.1 Setup Information

The setup packet contains three main groups of information which the host software can issue to the DELQA.

1. **Target address information** contains the Ethernet physical and Multi-cast addresses for which the DELQA is to receive messages.
2. **Control parameters** specify special reception modes (such as promiscuous or all Multi-cast) and sanity timer timeout values.
3. **MOP information** is used to read and change MOP parameters.

Setup packets may contain either one or two of these groups of information. A combination of the specified length of the setup packet and the value of the first byte of the setup packet buffer indicates which groups of information are present.

Table 2–2 explains all the possible combinations of information groups.

Table 2–2 Setup Packet: Information Group Combinations

Information Groups (Maximum 2)	Packet Length in Bytes (Octal)	Value of Byte 1
Target addresses (Group A or B) only	177 or less	
Target addresses and control parameters	200 to 377	Zero
Target addresses and MOP Element Blocks (MEBs)	400 exactly	Non-zero

More than one setup packet may be issued. Each setup packet overwrites completely the setup area up to the 200 byte offset, but the MOP area between the 200 byte and 256 byte offset is overwritten only if the MOP flag is set at the start of the packet. Therefore, the only useful setup packet lengths are 177, between 200 and 377, or 400 (octal) bytes.

The host should maintain a copy of the current setup data, in order to recreate the correct 14 addresses (which cannot be read back from the DELQA) whenever the setup information is modified. Since the DELQA can only have two types of setup packet information per setup packet, the DELQA will accumulate all setup packet information, unless re-specified in a subsequent setup packet. Although setup packets may be repeatedly issued to the DELQA to modify parameters or to read internal values (that is, counters, system ID parameters), only one setup packet should be outstanding to the DELQA at a time.

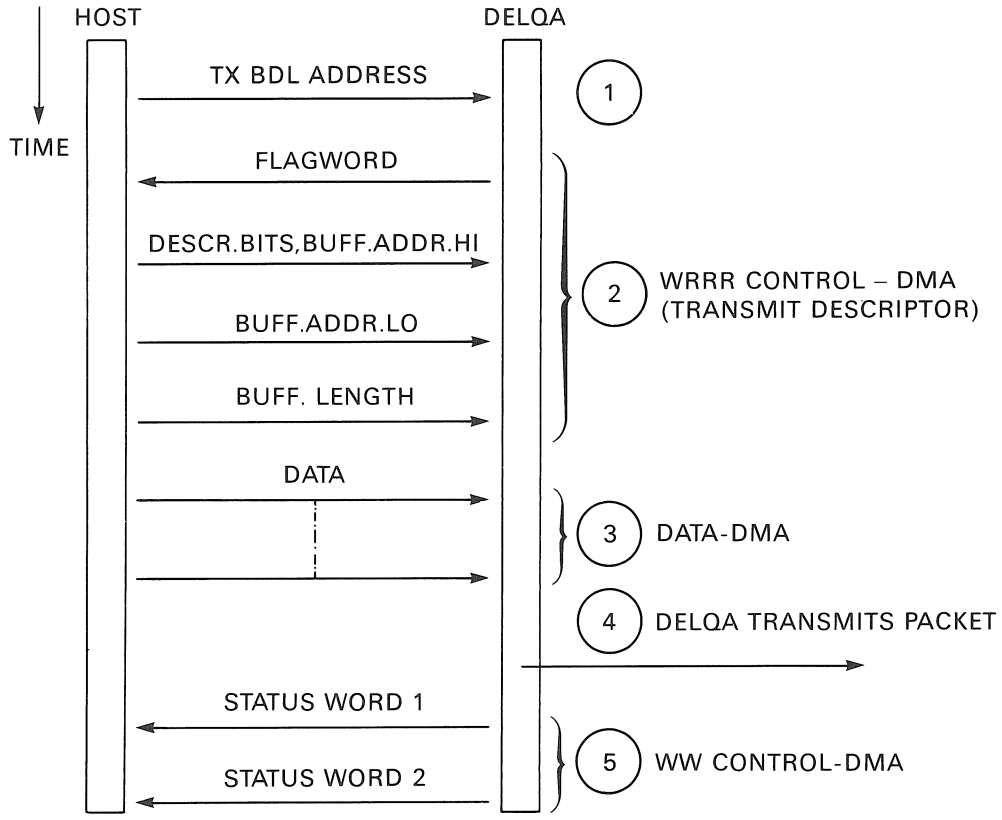
2.3.4 Transmit Packet

The host initiates transmission by first setting up a Transmit BDL, and then writing its address to the Transmit BDL Start Address register in the DELQA module.

The transmit buffers should be set up before attempting to set up the Transmit BDL. A transmit buffer can be up to 1514 bytes in length; this is the maximum number of bytes allowed in an Ethernet packet, excluding the four CRC bytes.

To complete the transmission, the DELQA executes the following steps:

1. Read the descriptor bits, and act on the buffer descriptor information as follows:



1. HOST WRITES TX BDL ADDRESS TO DELQA
2. DELQA FETCHES HOST DESCRIPTOR (WRITE-READ-READ-READ CONTROL-DMA)
3. DELQA DMAs DATA BUFFER FROM HOST
4. DELQA TRANSMITS PACKET
5. DELQA WRITES TRANSMIT STATUS TO HOST (WRITE-WRITE CONTROL-DMA)
6. THE DELQA WILL CONTINUE TO FETCH AND PROCESS HOST DESCRIPTORS UNTIL IT FINDS A DESCRIPTOR WITH THE VALID BIT CLEAR

RE4622

Figure 2–3 Transmit Sequence (No Chaining)

2. If the Valid bit is set, the DELQA accesses the start address and buffer length fields, reads the relevant buffer, transfers the contents to its on-board shared RAM, updates the status words, and continues to the next descriptor.
3. If the Valid bit is clear, the DELQA marks the end of the current BDL. The DELQA ceases to access the BDL and its associated buffers.
4. If the chain bit is set, the DELQA links to the BDL, via the start address indicated in the buffer address field, and continues to the next descriptor.

5. If the End-of-Message bit D<13> is set, the DELQA generates the preamble and CRC for the message, and transmits the complete message packet over the Ethernet. Then it updates the status words in the latest buffer descriptor with the outcome of the transmission. (If CSR06 Interrupt Enable is set, the DELQA also generates a transmit interrupt request to indicate that a message has been transmitted.)

To achieve acceptable transmission rates, the DELQA executes control DMA (to set up the next data DMA transfer), data DMA, and data transmissions in parallel. The host software reads the status or contents of buffers only after the DELQA has returned the transmission status to the status word bits.

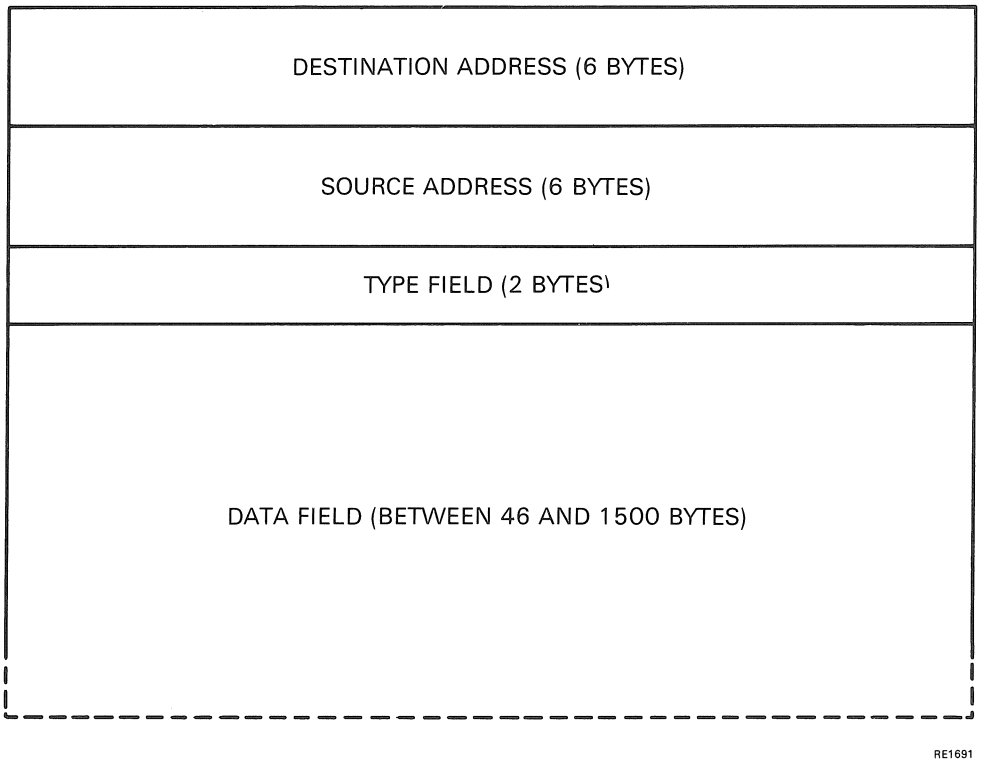


Figure 2–4 Ethernet Packet Format

2.3.5 Transmit Programming

The host software for packet transmission is responsible for the following actions.

1. Establish the location and contents of the transmit message buffers.
2. Initialize the start address and descriptor bits for each buffer descriptor in the Transmit BDL.
3. Write all the data fields within the transmit packet, including destination address (6 bytes), source address (6 bytes), type field (2 bytes), and data (between 46 and 1500 bytes).

   The DELQA hardware supplies the CRC automatically.
4. Clear the Valid bit in the last descriptor of the BDL.
5. Set the Valid bit in all the previous descriptors of the BDL.
6. Write the start address of the BDL to the BDL Start Address register on-board the DELQA, to initiate transmissions.

The host software should also provide an interrupt service routine to:

- Check the status and availability of transmit buffers
- Check CSR04 (Transmit List Invalid) to ensure that previous list processing has completed
- Check CSR02 (NXM) in case the interrupt was caused by a memory access error.
- Write 1 to clear CSR07 (Transmit Interrupt Request), if the bit is set.

2.3.6 Transmission Errors

In status word 1 of the last BDL entry for the transmitted message, the following status bits in the transmit buffer descriptor record transmission errors.

S1<09>	Abort	Excess collisions: there have been more than 15 attempts to transmit this packet. Check S1<12> in Transmit Status Word 1 in case the Ethernet circuit is faulty (see below).
S1<12>	Loss	Loss of carrier during transmission, usually due to a short circuit on the Ethernet. However, Loss does not abort transmission, because it may be set during a normal collision recovery.

NOTE
In the DEQNA bits 11 and 12 of Transmit Status Word 1 have different functions for Carrier Status.

The Time Domain Reflectometry (TDR) counter (S2<09:00>) is a 10 MHz counter which is enabled by the DELQA when a carrier signal is detected, and disabled when the carrier stops or a collision is detected. The contents of the TDR counter are valid only when Abort (S1<09>) is set, and may be used as a relative measure of the distance through the network between the module and the supposed fault or collision.

2.3.7 Receive Packet

The host initiates reception by first setting up a Receive BDL, and then writing its start address to the DELQA module.

To complete the receive process in response to activity on the Ethernet, the DELQA executes the following steps.

1. Read the descriptor bits, and act on the buffer status as follows.
   - If the Valid bit is cleared, it marks the end of the current BDL. The DELQA ceases to access the BDL and its associated buffers.
   - If the Chain bit is set, the DELQA links to the BDL whose start address is indicated in the buffer address field, and continues from step 2.
   - If the Valid bit is set, the DELQA accesses the start address and buffer length fields, reads the next part of the incoming message into the indicated buffer from its on-board shared RAM, and continues from step 2.
2. If the message ends, the DELQA terminates reception, and updates the status words in the last buffer descriptor used. (If CSR06 is set, the DELQA also generates a receive interrupt request to indicate that a message has been received.)

2.3.8 Receive Programming

The host software for packet reception is responsible for the following actions.

1. Establish the location and contents of the receive message buffers.

   Sufficient receive buffers should be allocated for at least one packet of the maximum expected length, in order to ensure that a receive interrupt request is generated before the next incoming message arrives.

NOTE
No interrupt is generated if there are not enough valid receive buffers in the Receive BDL to accommodate a complete packet.

2. Initialize the start address and descriptor bits for each buffer descriptor in the Receive BDL.
3. Initialize Status Word 2 of all the descriptors in the Receive BDL with unequal high and low bytes. (The DELQA makes the high and low bytes both equal to the received byte length, to indicate when the receive data is valid.)
4. Clear the Valid bit of the last BD in the BDL. Set the Valid bit in all BDs in the BDL except the last BD.
5. Set CSR00 (Receiver Enable) to enable Ethernet packet reception.
6. Write the start address of the BDL to the BDL Start Address register on-board the DELQA, to initiate reception.

The host software should provide an interrupt service routine to:

- Check the status and availability of receive buffers
- Check CSR05 (Receive List invalid) to ensure that previous list processing has completed.
- Write 1 to clear CSR15 (Receive Interrupt Request) if this bit is set.
- Check CSR02 (NXM) in case the interrupt was caused by a memory access error

2.4 NETWORK SUPPORT

In Normal mode, the DELQA is capable of implementing the following Ethernet MOP functions (a subset of DECnet operations) without host intervention:

1. Respond to Trigger Instruction to re-boot local system.
2. Loopback assistance.
3. Transmit System ID.
4. Respond to Request System ID.

In Normal mode, the DELQA processes the following Link-layer Service Access Point (LSAP) messages when used on an IEEE 802.3 local area network:

1. NULL TEST (Loopback).
2. NULL XID (Transmit ID).

2.4.1 Remote Trigger Instruction

The Trigger instruction enables a remote node on the Ethernet to request a system reboot.

When it recognises a Trigger instruction from another node, the DELQA module:

1. Decodes the instruction.
2. Validates its verification code (if programmed to do so by a setup packet from host software).
3. If the instruction requests a reboot of the host system, the QIC negates the signal BDCOK on the Q-Bus in order to force a system reboot.
4. Finally, host software must re-initialise the verification code.

The DELQA module checks:

1. Whether verification is required.
2. COMM BOOT or SYSTEM BOOT requested.

The Remote Boot option is enabled with option switch S4 open and mode switch S3 closed.

2.4.2 Loopback Assistance

Loopback messages can be transmitted to the DELQA module over the Ethernet to verify the connection. These are node-to-node connections at the lowest levels of protocol, and do not involve host software at either end. This facility is used by DECnet Network Management software to run diagnostic tools from a remote node on the Ethernet.

2.4.3 Transmit System ID

Identification messages enable certain DECnet and Network Interconnect Exerciser (NIE) utilities to map the nodes on an Ethernet network.

On powerup, the DELQA module automatically transmits its system identification over the Ethernet. The identification message contains at least the device type at the node, and its Ethernet address; host software may use a setup packet to add more information to the message. The message is broadcast every 10 minutes +/- 2 minutes 11 seconds.

2.4.4 Request System ID

On powerup, the DELQA module in Normal mode recognises Request System Identification messages on the Ethernet. In response, the module transmits a copy of its current System Identification message.

2.4.5 IEEE 802.3 Network Support: NULL Link-layer Service Access Points

In Normal mode DELQA implements IEEE 802.2 Logical Link control messages when they are received on a NULL Link-layer Service Access Point (LSAP) within an IEEE 802.3 standard local area network.

These messages can be used to interrogate and test many link layer service points per node. Therefore, IEEE 802.2 Logical Link control messages which are received on a non-NULL LSAP are passed on to the host system as normal datagrams.

The messages supported are:

1. **TEST Message**

   The IEEE 802.2 TEST message is similar in function to the Loopback Message on Ethernet networks.

2. **XID (Transmit ID) Message**

   The IEEE 802.2 XID (Transmit ID) message is similar in function to the MOP Remote Console Request System ID Messages on an Ethernet network.

   DELQA does not broadcast IEEE 802.2 XID messages automatically as it does with MOP System IDs since it is not required by the IEEE 802.2 protocols.

For details of this message format and protocol, refer to the ANSI/IEEE Draft International Standard 802.2 Logical Link Control.

2.4.6 Datalink Counters

The DELQA maintains in shared RAM a set of datalink counters of bytes and packets transferred successfully and in error. A setup packet provides host software with a mechanism for reading these counters locally.

CHAPTER 3
TECHNICAL DESCRIPTION

3.1 SCOPE

This chapter describes how the components of the DELQA module work together on the backport bus. The sections are as follows:

Section 3.2 **ARCHITECTURE**
Section 3.3 **Q-BUS INTERFACE**
Section 3.4 **ETHERNET INTERFACE**
Section 3.5 **BACKPORT BUS**
Section 3.6 **MODULE CONTROL**

3.2 ARCHITECTURE

3.2.1 Overview

The DELQA module is built around a backport bus which passes data between the QIC, shared RAM, and the LANCE. A 68000 microprocessor handles formatting, module control, and initialization. The QIC, the QNA2, and the 68000 microprocessor are surface-mounted devices.

The QIC handles the interface with the Q-Bus protocols, and the LANCE handles the interface with the Ethernet protocols. Shared RAM is used as an intermediate buffer store.

The QNA2 arbitrates between the 68000, the LANCE and the QIC, for access to the backport bus. The QNA2 provides all the control signals for succsessful data transfer The QNA2 contains the DELQA control and status register (CSR) and the Interrupt Register(IR).

Firmware ROM contains both the master control program for the DELQA module and 4Kbytes of PDP-11 boot/diagnostic code for the Q-Bus system. The firmware ROM can be addressed only by the 68000 microprocessor.

The Station Address (SA) ROM is preprogrammed with the 48-bit default physical address of the DELQA module in the Ethernet LAN.

Figure 3–1 shows the principal control signal paths through the DELQA module.

3.2.2 Selection Switches

The DELQA has five manual selection switches: S1 to S5. These are part of a switchpack on the DELQA board.

Table 3–1 describes how the switches are used. Figure 3–2 shows the selection switch signals.

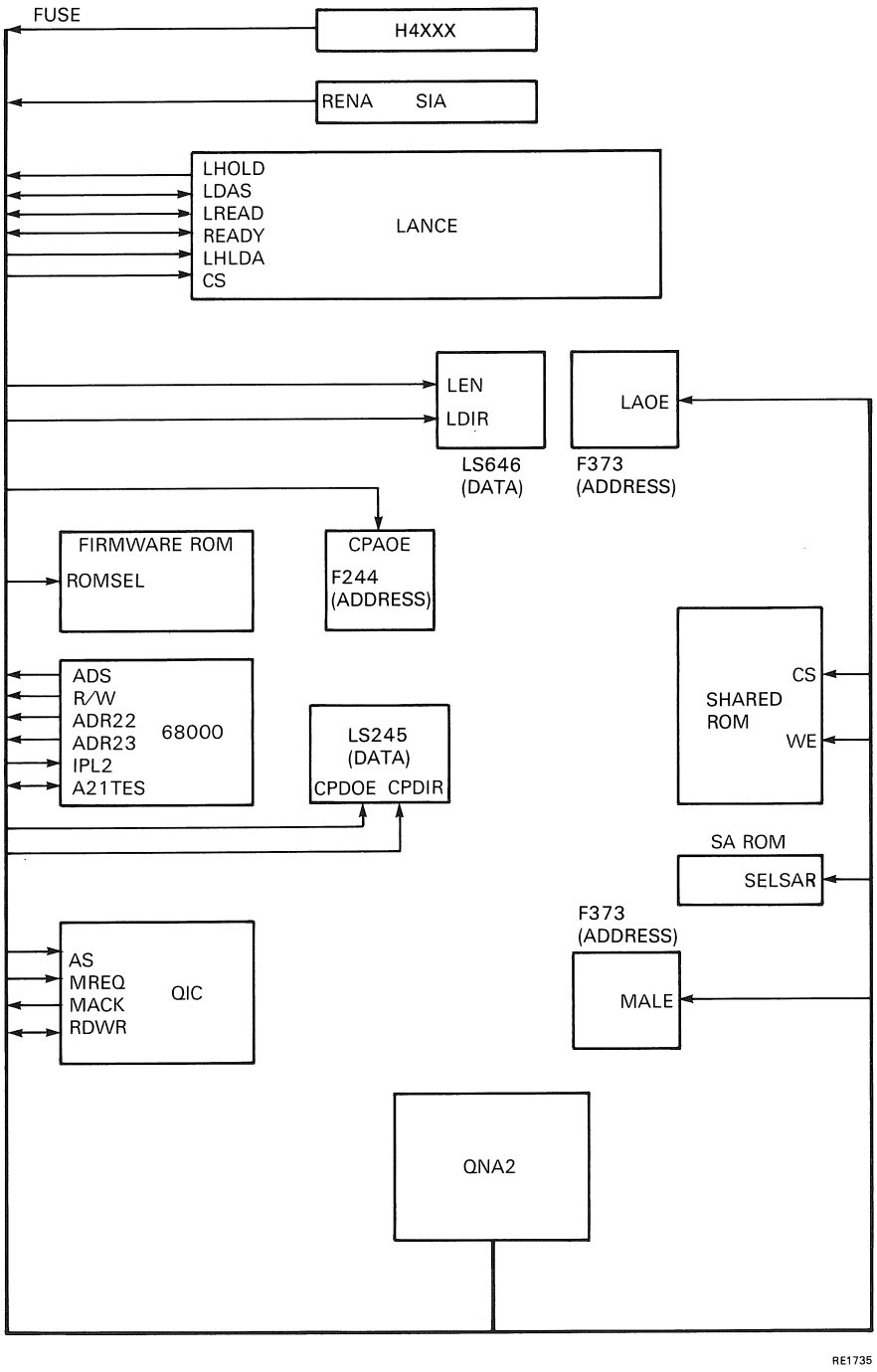


Figure 3–1 QNA2 Control Signals

Table 3–1 DELQA Module: Switch Options

S1	Select Module Address. This switch selects the base address of the module on the Q-Bus.

S1	Base Address	Unit	Module
CLOSED	17774440	DELQA 1	DELQA or DEQNA
OPEN	17774460	DELQA 2	DELQA or DEQNA
S2	NOT USED		

S3/S4 DELQA Mode and Options. Switch S3 selects whether Normal mode or DEQNA-lock mode is enabled.

When switch S3 is closed, Normal mode is enabled, and host software can switch the module between Normal mode and DEQNA-lock mode. When Normal mode is selected using switch S3, the DELQA supports MOP operations, but the MOP operation for Remote BOOT can be enabled by setting switch S4 to open.

When switch S3 is open, DEQNA-lock mode is enabled. In this mode MOP operations are not supported, and switch S4 determines whether the sanity timer is enabled automatically on powerup.

Switch S3	S4	Normal	DEQNA-lock	Remote BOOT	Other MOP functions	Auto Sanity Timer
CLOSED	CLOSED	enabled			enabled	
CLOSED	OPEN	enabled		enabled	enabled	
OPEN	CLOSED		enabled			
OPEN	OPEN		enabled			enabled
S5	NOT USED	Reserved for DEQA-T M7516-YM		closed open	enable Turbo mode Disable "	"

3.2.3 Clocks

The clock signals in the DELQA module run from a 40MHz oscillator located at the Ethernet end of the board.

The main clock signal is divided by two to produce two antiphase 20MHz clock signals. One of these is fed into the X1 input of the SIA, where it is used to generate the 10MHz Transmit Clock signal to the LANCE. The other clock is fed to the QIC and the QNA2, so that these two chips can operate synchronously at 20MHz.

The QNA2, as bus controller, generates the 10MHz clock that drives the 68000 microprocessor.

Figure 3–2 shows the main clock signals.

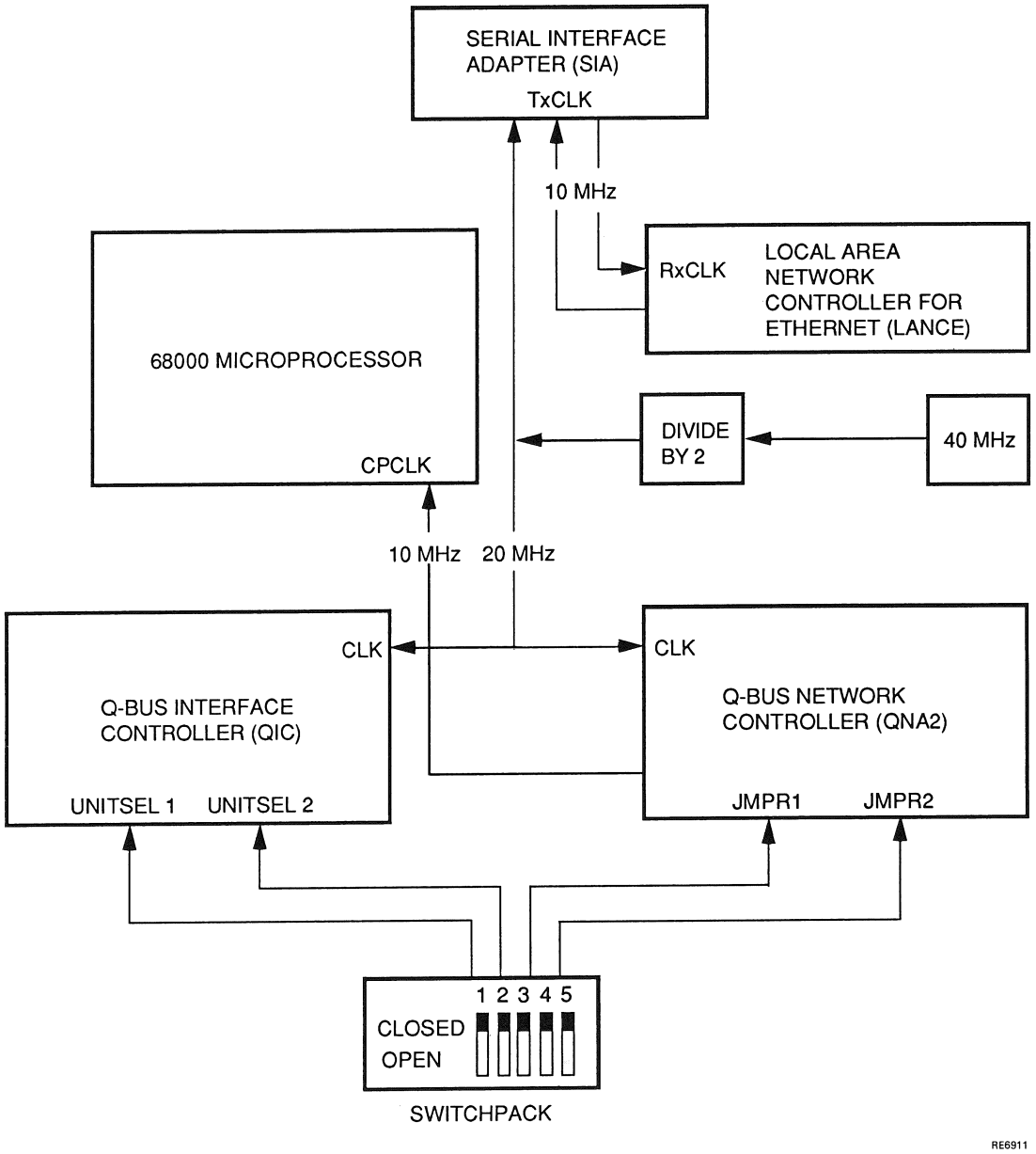


Figure 3–2 DELQA Clocks and Selection Switches

3.2.4 POWER LOADING

Table 3–2 DELQA and transceiver power requirements

Function	Typical Voltage	Typical Current	Maximum Current	Backplane Pins
TTL level	+ 5V +/-0.25V	2.4A +/-10%	2.7A	BV1, AA2, BA2
TTL ground				AJ1, AM1, AT1 BJ1, BM1, AC2, BC2
Transceiver power	+12V +/-0.60V	0.5A +/-10%	1.5A (Note)	BD2
Transceiver ground				BT1

NOTE

At powerup, the surge current of the transceiver can cause certain power supplies to current limit or even to fail. These failures can also be caused during powered-up connect. There is no surge protection on the DELQA module. The bulkhead assembly must incorporate a 1.5A/250V slo-blo fuse.

Two fuses provide protection for the DELQA module and associated equipment:

- A 1.5 A/250 V slo-blo ™ 1.25 inch by 0.25 inch glass fuse (order number 90-07213) protects the transceiver and its associated external wiring. The fuse may be replaced with another fuse of the same type, a Littlefuse™ type 31301.5, a BEL FUSE™ type 3SB1.5, or an equivalent. The 1.25 inch (3.8 cm) fuse holder (order number 12-22255-03) is located in the bulkhead assembly (not on the DELQA board).
- A 5.0 A/125 V axial lead picofuse (order number 12-05747-00) protects the DELQA module and internal wiring. The picofuse is fitted on the DELQA board near the bulkhead cable connector, it looks like a resistor and is soldered to the board in the same way. It should be replaced only by trained personnel.

3.3 Q-BUS INTERFACE

3.3.1 Overview

The QIC (Q-Bus Interface Controller) handles the Q-Bus interface protocols. To provide a complete Q-Bus interface, four octal bus transceivers and two sets of quad transceivers are connected between the Q-Bus and the QIC. The QIC shares a 20MHz clock input with the QNA2.

The QIC provides complete Q-Bus slave control logic for host access to the DELQA I/O registers.

On the Q-Bus side, the QIC supports control DMA and data DMA, using block-mode to achieve the highest possible speeds. The QIC generates two control signals to change the direction of the DC021 transceivers:

1. DC012IN controls the direction of transfer of the three DC021 transceivers connected to the Q-Bus data/address lines, BDAL<21:0>.
2. TSACK (Transmit DMA Selection Acknowledge) controls the direction of transfer for the fourth DC021 transceiver, which carries the bus control signals that enable the QIC to act as Q-Bus master for DMA.

On the backport side, the QIC supports DMA transfers to and from shared RAM along 16 data/address lines. The QIC is controlled through a series of registers that are accessed by the 68000 microprocessor.

Figure 3–3 shows the Q-Bus interface. Table 3–3 summarizes the signals and pinouts.

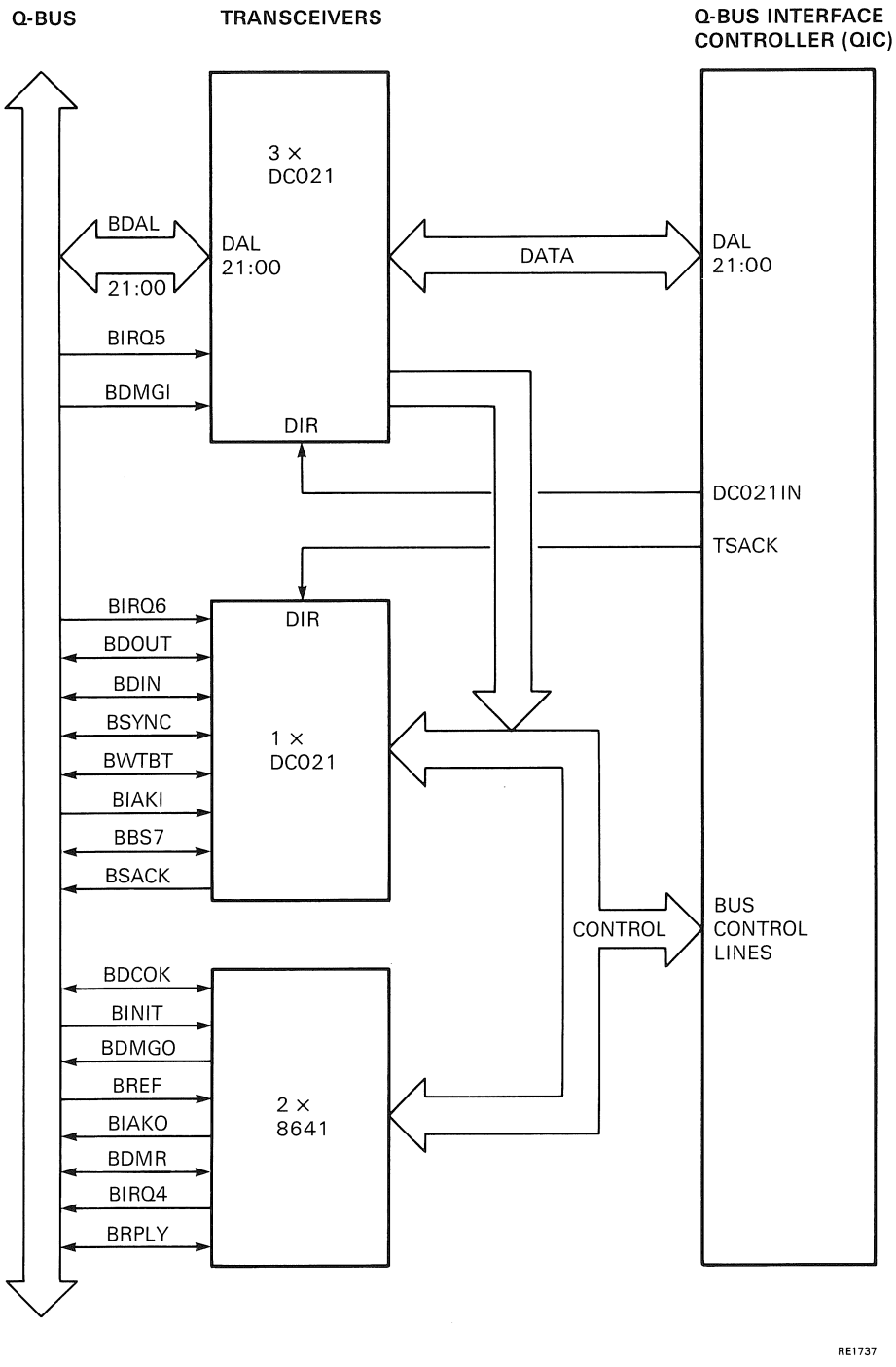


Figure 3–3 Q-Bus Interface (hardware)

Table 3–3 Q-Bus Connector Pins and Signals

Pin	Signal	Description	Pin	Signal	Description
AA1	BIRQ5	Interrupt lines	AA2	+5V	
AB1	BIRQ6		AB2		
AC1	BDAL16 L	Data/Control lines	AC2	GND	
AD1	BDAL17 L		AD2		
AE1			AE2	BDOUT L	Bus Control lines
AF1			AF2	BRPLY L	
AH1			AH2	BDIN L	
AJ1	GND		AJ2	BSYNC L	
AK1			AK2	BWTBT L	
AL1			AL2	BIRQ4 L	Interrupt lines
AM1	GND		AM2	BIAKI L	
AN1	BDMR L	DMA Control	AN2	BIAKO L	
AP1	BHALT L		AP2	BBS7 L	Bus Control
AR1	BREF L	Q-Bus control	AR2	BDMGI L	DMA Control
AS1			AS2	BDMGO L	
AT1	GND	FUSE H sink	AT2	BINIT L	Bus Control
AU1			AU2	BDAL0 L	Data/Address lines
AV1			AV2	BDAL1 L	
BA1	BDCOK H	DC Power OK	BA2	+5V	
BB1	BPOK	Power OK	BB2		
BC1	BDAL18 L	[Data/	BC2	GND	

Table 3–3 (Cont.) Q-Bus Connector Pins and Signals

Pin	Signal	Description	Pin	Signal	Description
BD1	BDAL19 L	[Address	BD2	+12V (XCVR)	Transceiver
BE1	BDAL20 L	[lines	BE2	BDAL2 L	
BF1	BDAL21 L		BF2	BDAL3 L	Data/ Address lines
BH1			BH2	BDAL4 L	
BJ1	GND		BJ2	BDAL5 L	
BK1			BK2	BDAL6 L	
BL1			BL2	BDAL7 L	
BM1	GND		BM2	BDAL8 L	
BN1	BSACK L	DMA Control	BN2	BDAL9 L	
BP1	BIRQ7 L	Interrupt	BP2	BDAL10 L	Data/ Address lines
BR1			BR2	BDAL11 L	
BS1			BS2	BDAL12 L	
BT1	GND	(XCVR) Transceiver	BT2	BDAL13 L	
BU1			BU2	BDAL14 L	
BV1	+5V		BV2	BDAL15 L	

Notes:

1. **(XCVR)** indicates isolated power connections through the DELQA to the Ethernet transceiver cable connector.
2. **BC2** is tied to the ground plane of the module and serves as a pull-down sink through approximately 14K Ohms for the Ethernet Connector signal FUSE H.

The QIC is reset from the QBUS when BDCOK is regated and BINITL is asserted. The assersion of BINITL also causes a reset sequence to the remainder of the DELQA module. On the falling edge of RINITH a 2000ns pulse resets the QNA2 and a 150ms pulse resets the 68000 and the LANCE.

3.3.2 Initialization

The backport is reset when the Q-Bus RINITH signal transitions from 1 to 0. The backport is also reset when CSR Bit 01 (software reset) is transitioned from 1 to 0.

Initialization code will cause the 68000 to examine the reason for the backport reset. Possible reset causes are:

Table 3–4 Backport Reset

	DCOK	RINITH	TDCOK
Powerup	1	X	0
Q-Bus Init	0	1	0
DELQA Initiated boot	X	X	1
Software Reset	0	0	0

The bits DCOK, RINITH and TDCOK are contained in the QIC registers.

The QIC can initiate a reboot of its Q-BUS host by negating TDCOK. This will occur whenever the TDCOK bit in the QIC Mode Register is toggled to 1.

3.3.3 DMA Functions

The QIC can request, accept, and relinquish ownership of the Q-Bus, for both data DMA and control DMA accesses to the host database.

There are separate addressing and buffering mechanisms for data DMA and control DMA. This allows control DMA requests to take priority over data transfers in progress; when the control DMA is complete, the data transfer is restarted from where it left off.

3.3.3.1 Data DMA

During data DMA transfers, the 21-bit Q-Bus address counter is connected to DAL<21:01>, with DAL<00> held at zero. During a transfer, data transferred between the Q-Bus and the backport bus is double-buffered within the QIC. The 16-bit backport address counter is connected to BPDAL<00,15:01> to support transfers of up to 128 Kbytes.

Double buffering inside the QIC allows for the signal setup, hold and access times of Q-Bus and backport bus, and for high speed, pipelined transfers through the chip.

If control DMA is attempted during data DMA, the QIC:

1. Relinquishes control of the Q-Bus
2. Requests control for a control DMA transfer (non-block-mode).
3. Completes the control DMA transfer, and relinquishes control of the bus.
4. Requests control of the bus in order to resume data DMA transfers.

The QIC recognizes 16-word boundaries because there is no RREF (Refresh) from the bus slave.

3.3.3.2 CONTROL DMA

During Control DMA transfers, the 21-bit Q-BUS address counter is connected to DAL<21:01>, with DAL<00> held at zero. Control information is passed along a latched path through the QIC using single byte or single word transfers.

This is the same path that is used when the host accesses the QIC as bus slave. If the host requests an I/O page access at the same time as the 68000 requests a control DMA transfer, the host request takes priority.

3.4 ETHERNET INTERFACE

3.4.1 Overview

The LANCE (Local Area Network Controller for Ethernet) and the SIA (Serial Interface Adapter) operate together to provide a complete interface from the backport bus to the Ethernet. To provide fault isolation required by IEEE 802.3, a transformer is inserted in the path between the 51A and the transceiver cable connector.

On the backport side of the LANCE, two bus transceivers isolate the LANCE from the backport data bus, and two latches isolate the LANCE from the backport address bus (arbitrated by the QNA2). The SIA takes a 20MHz clock input from the DELQA clock, and uses it to generate a 10MHz clock, which it also passes to the LANCE for synchronization.

The SIA provides Manchester encoding of data for transmission, and decodes received data. The LANCE supplies and checks the 32-bit CRC that is appended to all Ethernet packets.

During transmission the LANCE polls the transmit buffer descriptor list for buffer descriptors that it owns. When it finds an entry that it owns it DMAs the data from shared RAM into internal FIFO. It prefixes the 64-bit preamble to the packet and sends the data to the SIA as a serial bit stream. When the packet has been transmitted, or if an error occurs, the LANCE will update the relevent buffer descriptor.

During reception, the SIA detects and synchronizes to the incoming bit stream from the Ethernet. The LANCE checks the destination address contained in the package against its list of addresses. If it finds a match, the LANCE will DMA the data from its internal FIFO in to buffer memory. When the reception is completed, or if an error occurs, the LANCE will update the relevant entry in the receiver buffer descriptor list.

The SIA communicates only with the LANCE and the Ethernet interface. The LANCE acts as backport bus master for all data transfers, and as bus slave for the 68000 microprocessor to program its internal registers. It communicates with the QNA2 in order to access the backport bus and transfer data to and from shared RAM.

Figure 3–4 shows the Ethernet interface.

3.4.2 Initialization

The LANCE initializes itself on request from the 68000. The 68000 writes an Initialization block from 68000 ROM to shared RAM, and programs the LANCE CSR to locate the block. The LANCE reads the block to determine mode of operation, address recognition parameters, and buffer descriptor ring pointers.

3.4.2.1 Destination Addresses

The LANCE can be programmed to match three different types of address from an incoming packet, as follows:

1. **48-bit destination address**

   This is programmed as the unique address of the DELQA. Usually, the initialization block is programmed to include the physical address from the SA (Station Address) PROM, but DECnet software reprograms the address in order to reflect the current DECnet node number. (SA ROM still stores a permanent record of the default physical address.)

2. **Multicast address filter**

   This is programmed using a logical address mask in the initialization block.

3. **Promiscuous mode**

   In this mode the LANCE is programmed to accept all incoming packets. This mode is set using the mode register in the initialization block.

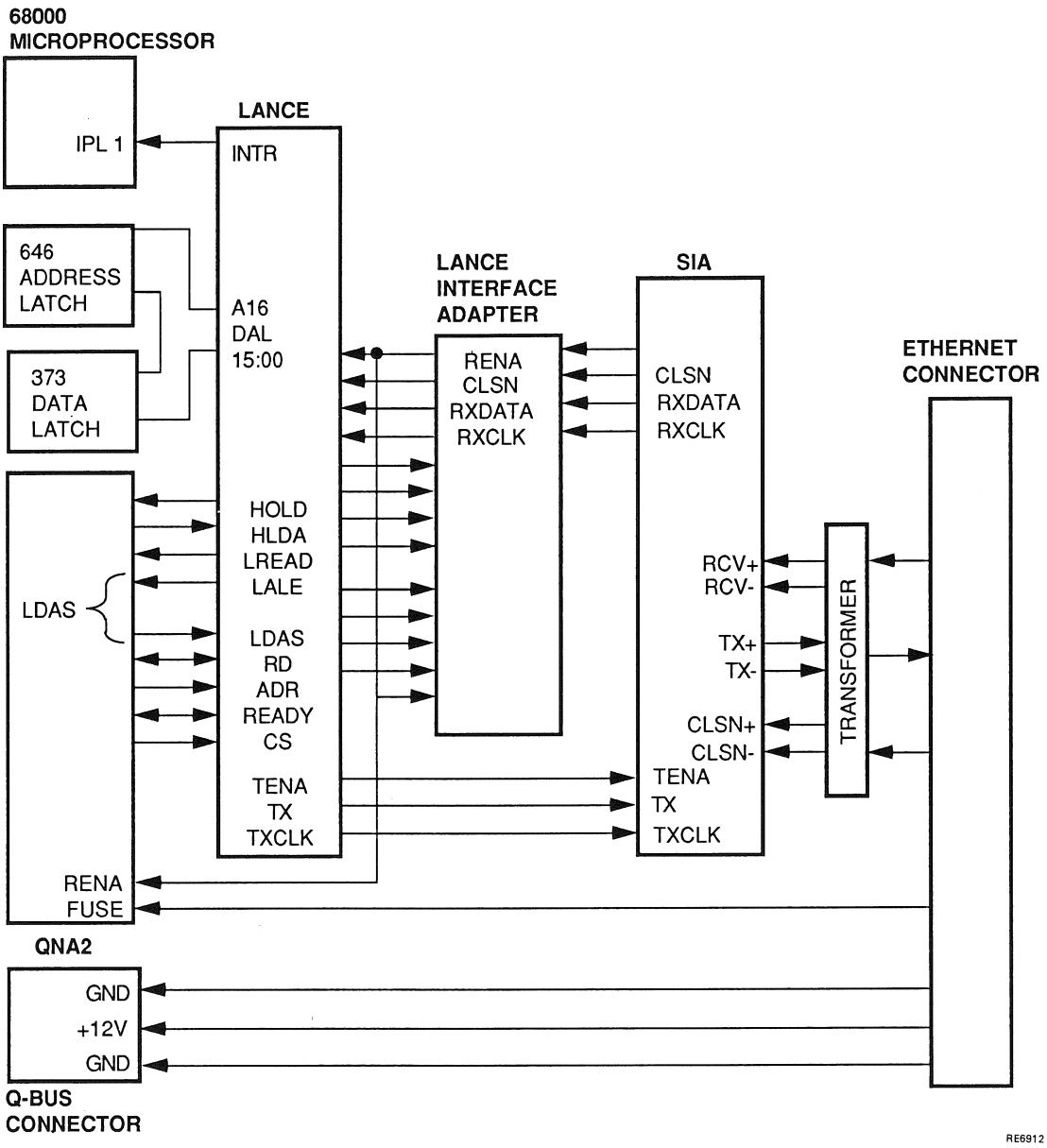


Figure 3–4 Ethernet Interface (hardware)

3.4.2.2 LANCE Memory Structures

There are three memory structures accessed by the LANCE:

1. **Initialization Block** (12 words) contains the operating parameters for the device: mode of operation; physical address; logical address mask; location of receive and transmit descriptor rings; number of entries in receive and transmit descriptor rings.
2. **Receive Message Descriptor Rings (rMDR) and Transmit Buffer Descriptor Rings (tMDR)**. Two ring structures, one each for incoming and outgoing packets. Each entry is four words long, comprising: data buffer address, length, and status.
3. **Data buffers** for packet buffering.

These memory structures are set up in shared RAM by the 68000 microprocessor. The 68000 then writes the Initialization Block Start Address (IADR) to CSR1 and CSR2 in the LANCE, and the LANCE loads itself with the information contained in the Initialization Block.

Refer to Appendix A for details.

3.4.3 Transmission

The LANCE polls the transmit Message Descriptor Ring (MDR) automatically every 1.6 milliseconds whenever it is not searching out receive buffers for incoming packets.

The polling consists of searching the status words of the transmit Message Descriptor Ring (MDR) for a buffer descriptor marked as OWNed by the LANCE. Then the LANCE executes two more read operations to collect the transmit buffer address and its buffer byte count.

Where the buffers are chained, the LANCE looks ahead once during the current transfer in order to find the next buffer. If it does not OWN the next MDR entry, it sets the UFLO and BUFF error bits in CSR0. When it empties a buffer, the LANCE clears the OWN status bit for that buffer.

The interpacket gap time on the Ethernet is a minimum of 9.6 microseconds, starting on the falling edge of the SIA signal RENA.

In transmit mode, the host supplies the destination address, source address, and length field. The LANCE appends preamble, sync, and CRC to the frame.

If an error occurs, the current buffer transmission is abandoned, causing an interrupt to the 68000 microprocessor.

3.4.4 Reception

The polling consists of searching the status words of the receive Message Descriptor Ring (MDR) for a buffer descriptor marked as OWNed by the LANCE. Then the LANCE executes two more read operations to collect the receive buffer address and its buffer byte count.

If the LANCE OWNs a receive buffer when an incoming packet arrives, it looks ahead once between transfers to find the next OWN buffer. This involves three separate one-word read operations. If the buffers for incoming packet need to be chained, and the LANCE has not found the next buffer, it sets the BUFF and/or the OFLO bits in CSR0.

When an incoming packet arrives, the LANCE checks to see if it owns a receive buffer. If not it will poll the receive ring once for a buffer. If it does not own the buffer it will set the MISS bit in CSR0, and will not poll the receive ring until the packet ends.

The interpacket gap time on the Ethernet is a minimum of 9.6 microseconds, starting on the falling edge of the SIA signal RENA. If a new packet arrives within 4.1 microseconds of this edge, it can only be received correctly if at least eight bits of the preamble are left.

In receive mode, the LANCE strips the preamble and sync bits, and transfers data and CRC to shared RAM. The LANCE discards runt packets of less than 64 bytes (which are usually due to a collision).

The LANCE can handle up to seven dribbling bits when a received packet terminates, so long as the CRC accounts for them. If there are both dribbling bits and a CRC error, then a Framing Error is flagged in the Receive Message Descriptor.

If an error occurs, the current buffer reception is abandoned, causing an interrupt to the 68000 microprocessor.

3.4.5 Collision Detection

The SIA reports a collision on the Ethernet to the LANCE by asserting CLSN. It leaves TENA asserted for between 32 and 40 additional bit times in order to transmit the collision jam signal pattern. The jam pattern is any pattern other than the CRC bytes. The LANCE completes the preamble or the current byte transmission before starting to transmit the jam pattern.

The LANCE makes up to 16 retransmission attempts before reporting a collision.

If CLSN is asserted during reception, the reception is terminated at once, either because of an address mismatch with an internal pointer, or as a runt packet. A late collision (occurring after 64 byte times, or 51.2 milliseconds) is not recognized in receive mode.

3.4.6 Buffering

The LANCE operates two types of DMA transfer to shared RAM: single word DMA, and burst mode DMA.

Single word DMA is used to access the Transmit and Receive Message Descriptor Rings (MDRs), and to read the initialization block. Burst mode is used to transfer Transmit or Receive messages in eight consecutive reads or writes.

Bus cycles are a minimum of 600 nanoseconds. Burst mode transfers are separated by a gap of at least 700 nanoseconds.

Separate MDRs describe transmit and receive operations. Up to 128 tasks may be queued upon each MDR.

Each message descriptor entry is four words long. Each descriptor in a ring is marked as OWNed by either the LANCE or the host (the 68000 microprocessor). The status of a descriptor can only be changed while the descriptor is OWNed, and ownership can only be relinquished, never taken.

The location of the descriptor rings is programmed in the initialization block.

3.5 BACKPORT BUS

3.5.1 Overview

The QNA2 (Q-Bus Network Arbitrator) arbitrates requests for access to the backport bus. It then implements the control function appropriate to the access request that it has granted. Priority of access is in the order QIC, 68000, LANCE.

The QNA2 input FUSE monitors the power indicator from the H4*xxx* Ethernet transceiver. The QNA2 also drives the on-board LEDs that indicate: powerup, loopback testing, citizenship (CQ) tests, and normal operation.

Table 3–5 shows how the memory space on the backport bus is used.

Table 3–5 68000 Backport Address Map

IC	Word address Octal	Binary
LANCE RDP	70 000 000	111 000 000 000 000 000 000 000
LANCE RAP	60 000 000	110 000 000 000 000 000 000 000
QIC Base	40 377 440	100 000 011 111 111 100 100 000
QNA2 CSR	20 177 416	010 000 001 111 111 100 001 110
QNA2 IR	20 177 436	010 000 001 111 111 100 011 110
SA ROM	20 177 400	010 000 001 111 111 100 000 000
Shared RAM	20 000 000	010 000 000 000 000 000 000 000
68000 ROM	00 000 000	000 000 000 000 000 000 000 000

3.5.2 Backport Interface Timing

The 20 MHz CLOCK input to the QNA2 is shared with the QIC. This ensures the synchronous operation between the QNA2 and the QIC. The QNA2 further divides this 20MHz clock to produce a 10MHz clock for the 68000 microprocessor.

The antiphase version of the QNA2 clock is passed to the SIA which uses it to generate a 10MHz clock. This clock is passed to the LANCE as TXCLK.

3.5.3 Error Recovery

Errors in accesses to host memory and in Ethernet transmit and receive operations are flagged in the Control and Status Register.

The error conditions are recorded originally in the QIC Attention Register or the LANCE CSR0. The 68000 responds to a backport interrupt from these devices by examining the relevant register, transferring the information to the DELQA CSR, and generating a Q-Bus interrupt to the host system.

The LANCE flags network errors in CSR0, to be examined by the 68000 following a backport interrupt. System errors include:

1. Babbling transmitter attempts to transmit more than 1518 bytes
2. Collision detection circuitry not functioning
3. Packet missed due to insufficient buffers
4. Memory acknowledge timeout.

Packet errors are recorded in the relevant buffer descriptor entries. Packet errors include:

1. Invalid CRC
2. Framing error
3. Overflow or underflow
4. Insufficient buffers.

The LANCE contains a 10MHz time domain reflectometry counter to aid the location of faults in an Ethernet cable.

Figure 3–5 shows the main DMA control signals.

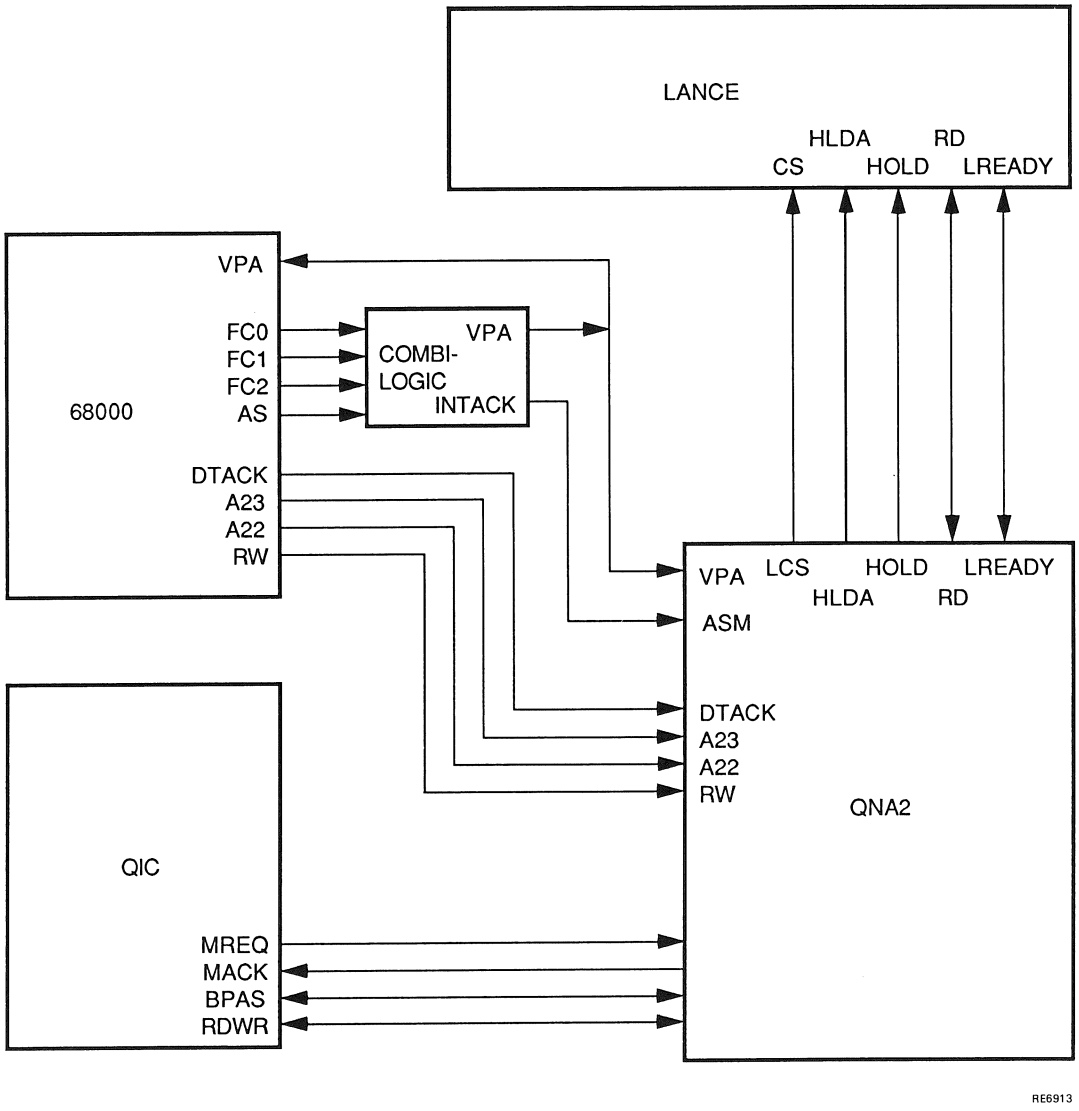


Figure 3–5 DMA Control Signals

3.6 MODULE CONTROL

3.6.1 Interrupts

In the DELQA module there are three interrupt lines to the 68000 microprocessor, as follows:

1. From the QIC
2. From the QNA2
3. From the LANCE

The ATTN (Attention) signal from the QIC to the 68000 is the result of a logical OR operation on several status condition bits within the QIC. It alerts the microprocessor, which can then interrogate the QIC backport attention register. Bits in this register are cleared when written to one, or when the QIC is reset by the QBUS.

Figure 3–6 shows the main interrupts control logic.

3.6.2 Sanity Timer

The sanity timer is enabled and reset by the host software. After the timer is enabled, the software must reset it periodically; otherwise it counts to its preset limit and times out.

When the sanity timer times out, the Q-Bus line DCOK is negated for approximately 3.6 microseconds. This resets the host system, and invokes the primary bootstrap (depending how the jumpers are set up in the host processor).

On reset the timeout defaults to four minutes, but it can be changed during setup mode to any factor of four within the range 1/4 second to 64 minutes. The timer can also be disabled by host software command.

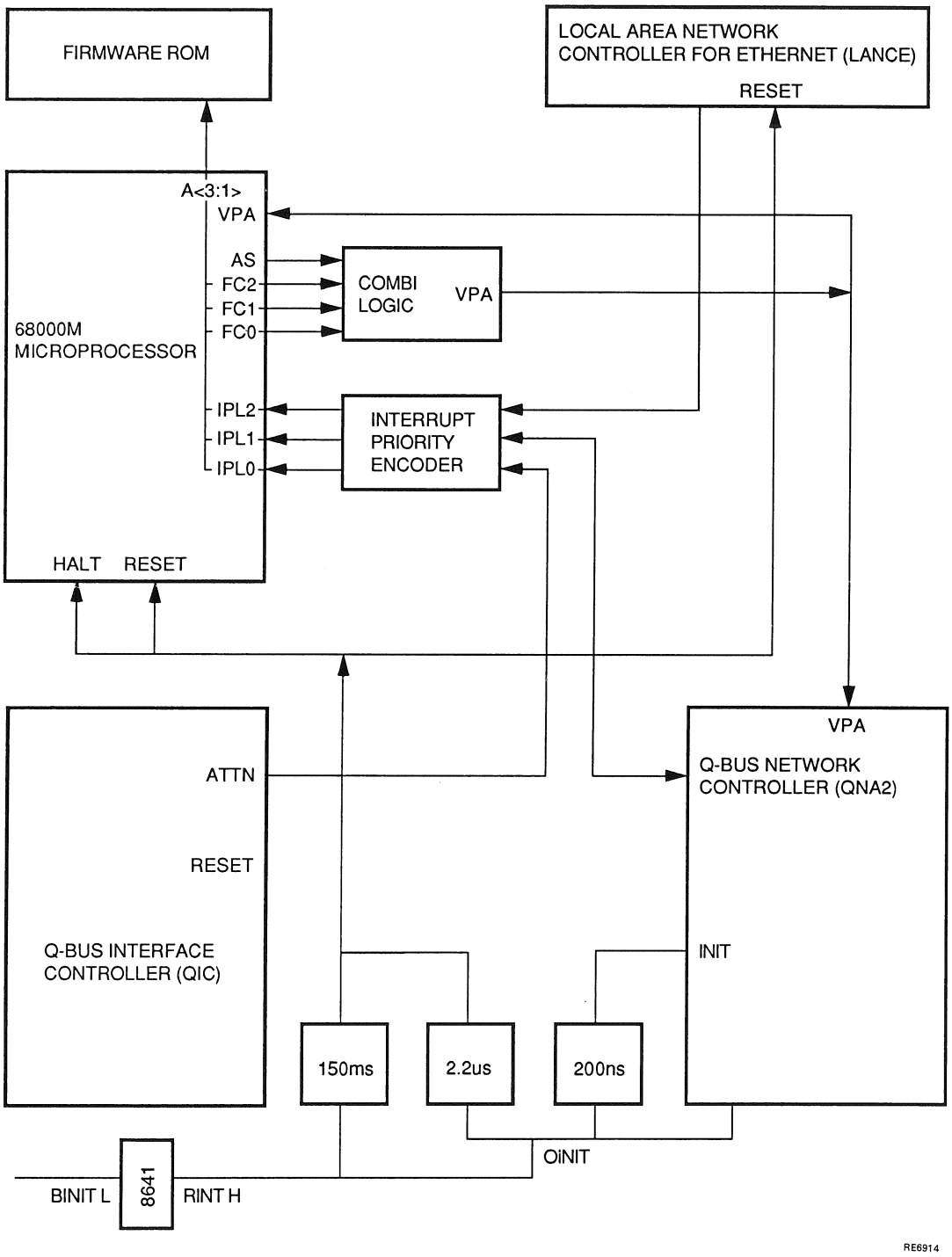


Figure 3–6 DELQA Interrupt and Reset Signals

APPENDIX A
IC DESCRIPTIONS

A.1 SCOPE

This appendix contains some basic data on the main Integrated Circuits in the DELQA. The sections are as follows:

Section A.2 **68000 Microprocessor**

Section A.3 **Q-Bus Interface Controller (QIC)**

Section A.4 **Q-Bus Network Arbitrator (QNA2)**

Section A.5 **AM7990 Local Area Network Controller for Ethernet (LANCE)**

Section A.6 **AM7991 Serial Interface Adapter (SIA)**

Each section includes the following (where relevant):

1. Overview.
2. Signals and pinout.
3. Addressing, memory structures, and registers.
4. Error recovery.

For more detailed information, refer to the manufacturer's data sheets. Other components on the DELQA board are well described in the standard references, and are not included here.

NOTE
Not ALL the features described in these sections are used by the DELQA.

A.2 68000 MICROPROCESSOR

A.2.1 Overview

The 68000 is a 16-bit microprocessor which has a 32-bit internal architecture. The 68000 is located on the top side of the DELQA board. Its main features are:

- 16-bit asynchronous data bus
- 23-bit asynchronous address bus, capable of addressing 16 Mbytes in conjunction with the data strobe signals UDS and LDS
- Eight 32-bit data registers
- Seven 32-bit address registers
- Memory-mapped I/O
- Compatibility with 6800-series peripheral ICs
- Single +5V power supply
- Mounted in a PLCC package.

The architecture of the 68000 is shown in simplified form in Figure A–1.

A.2.2 Signals and Pinout

The signals to and from the 68000 microprocessor fall into logical groups. The functions, signals and pinouts of these groups are described in Table A-1, and shown in Figure A–2.

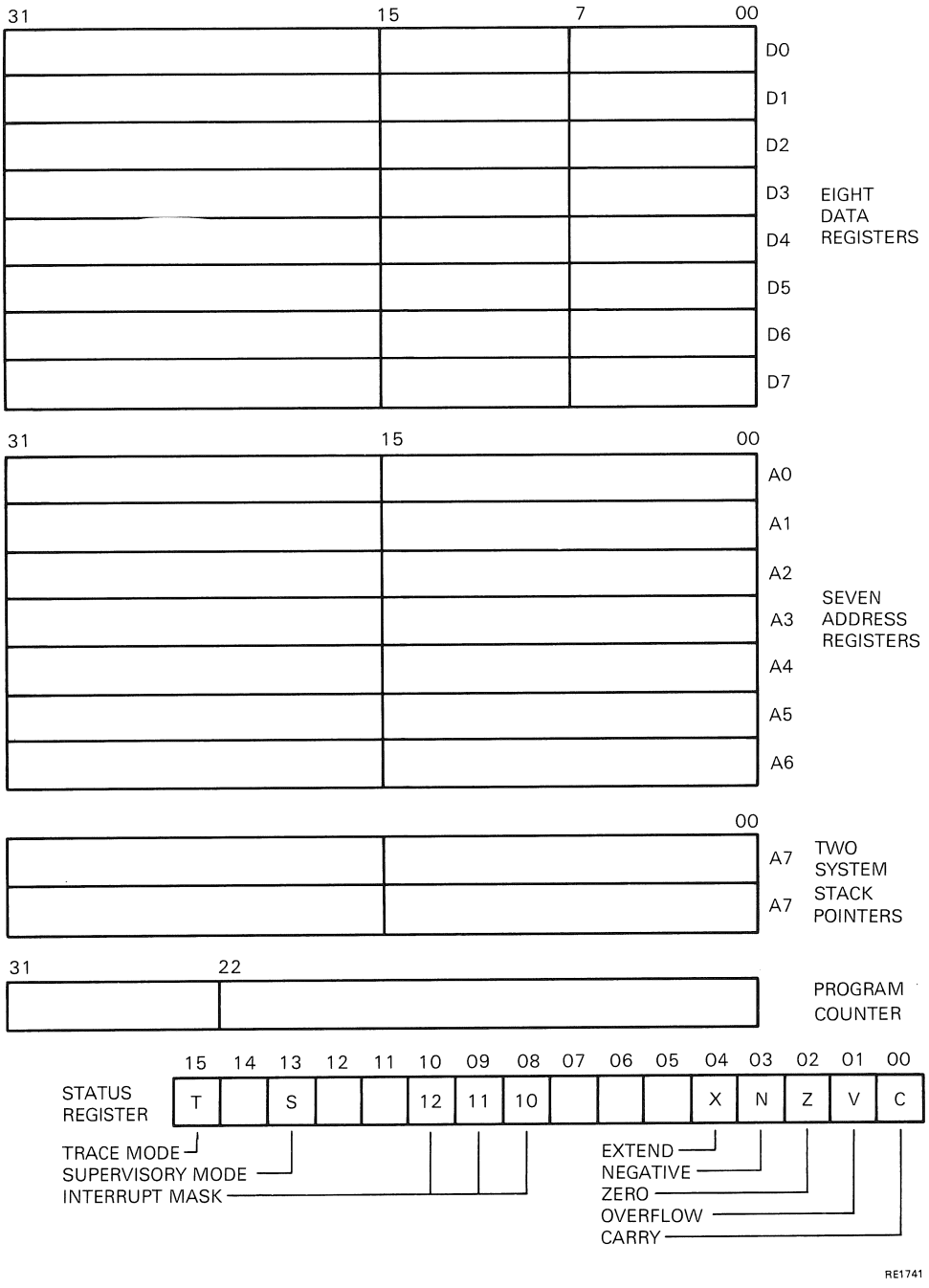


Figure A–1 68000 Block Diagram

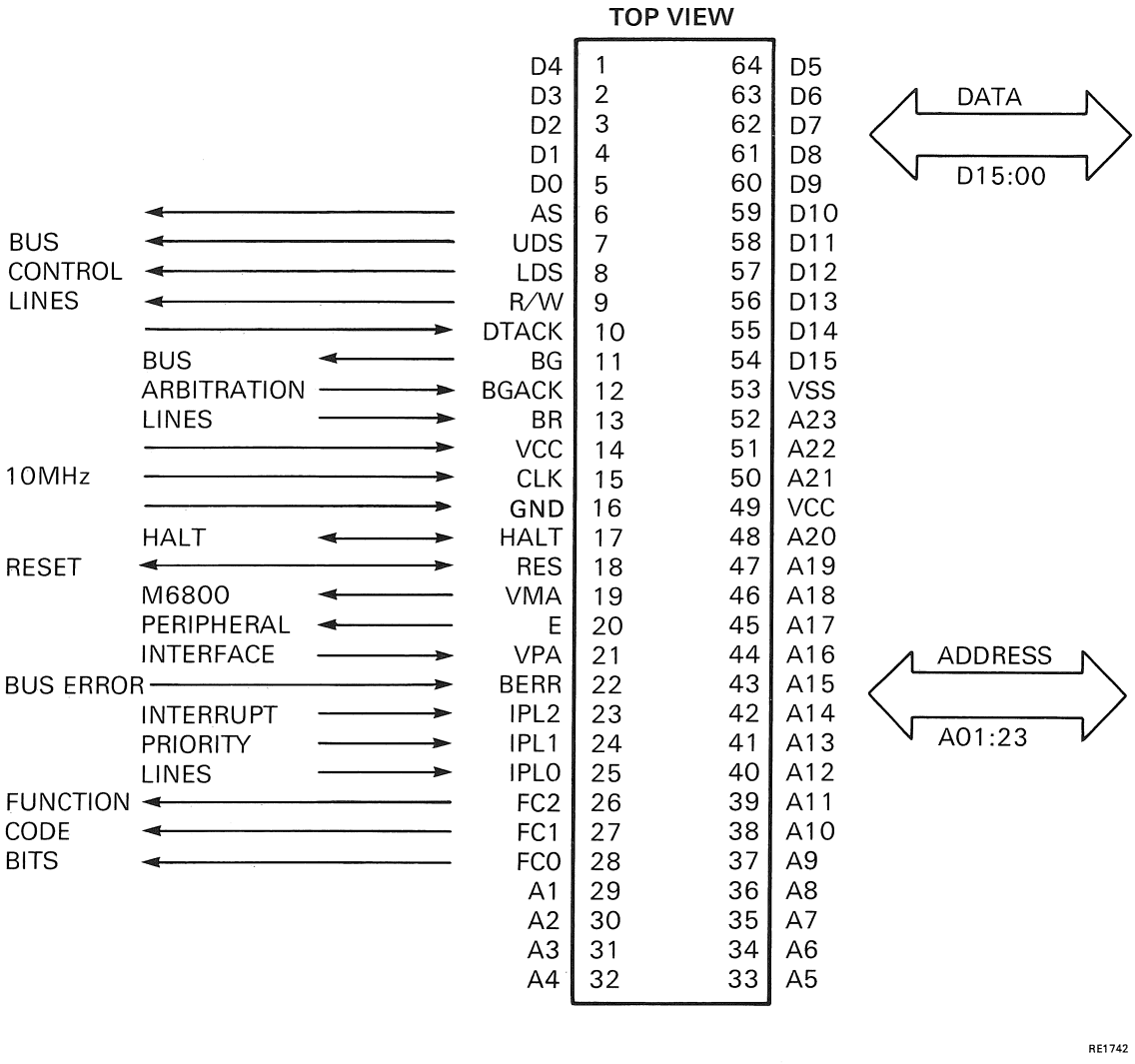


Figure A–2 68000 Pinouts

Address and Data Bus

Table A–1 68000 Signal Descriptions

Pin	Name	Sense	Description
01:05 54:64	D<04:00> D<15:05>	I/O Hi	Data Bus Lines D0:D15. 16-bit bus to transfer words or bytes. Lines D0:D7 are also used to receive a vector number during an interrupt-acknowledge cycle.
29:32 33:48 50:52	A<01:04> A<05:20> A<21:23>	O Hi	Address Bus Lines A1:A23. 23-bit bus to address 16 MBytes in conjunction with Data Strobes UDS and LDS. Lines A3:A1> are also used to signal the interrupt level while an interrupt is being serviced. In the DELQA, A20 selects the firmware ROM.

Asynchronous Bus Control

Pin	Name	Sense	Description
06	AS	O Lo	Address Strobe to indicate that a valid memory address is on the address bus.
07 08	UDS LDS	O Lo	Data Strobes to indicate whether data for transfer is on the upper, the lower, or both bytes of the data bus. (No Connection)
09	R/W	O Hi	Read to indicate direction of data.
		Lo	Write transfer to the data bus latches.
10	DTACK	I Lo	Data Transfer Acknowledge to complete a data transfer. The data bus cycle is extended until DTACK so that slow devices or memories can synchronise with the cycle.

Bus Arbitration (Not used)

Pin	Name	Sense	Description
13	BR	I Lo	Bus Request from a device for bus control.
11	BG	O Lo	Bus Grant gives control of the bus.
12	BGACK	I Lo	Bus Grant Acknowledge from a device confirms that it has taken control of the bus.

Interrupt Priority

23 24 25	IPL2 IPL1 IPL0	I Lo	Interrupt Priority Lines IPL<2:0> encode the priority of an interrupting device or process in the range 0 (no interrupt) to 7 (highest priority). IPL2 is the MSB.

Table A–1 (Cont.) 68000 Signal Descriptions

Pin	Name	Sense	Description
Function Code			
28 27 26	FC0 FC1 FC2	O Hi	Function Code Lines FC<2:0> indicate the state (user or supervisor) and type of cycle (data, program, interrupt) executed:

FC2	FC1	FC0	State	Cycle
0	0	0	User	Reserved
0	0	1	User	Data
0	1	0	User	Program
0	1	1	User	Reserved
1	0	0	Supervisor	Reserved
1	0	1	Supervisor	Data
1	1	0	Supervisor	Program
1	1	1	Supervisor	Interrupt

Pin	Name	Sense	Description
M68000 Peripheral Interface			
21	VPA	I Lo	Valid Peripheral Address indicates that the device or memory addressed is type M68000 and that data transfer should be synchronised to Enable (E).
19	VMA	O Lo	Valid Memory Address indicates, in response to VPA, that a valid address is on the address bus and that the 68000 is synchronised to the Enable Signal. (Not used.)
20	E	O Hi	Enable is the standard enable clock signal for M68000 systems. (Not used.)
System Control and Timing			
17	HLT	I/O Lo	Halt is a bidirectional line that either receives an external halt from, or sends a halt signal to, external devices. When generated internally the instruction halts the processor. When HLT is asserted by an external device, the 68000 halts at the end of the current bus cycle. A halted 68000 can be restarted only by an external Reset. HLT also interacts with RES and BERR.

Table A–1 (Cont.) 68000 Signal Descriptions

Pin	Name	Sense	Description
18	RESET	I/O Lo	Reset is a bidirectional line that either receives an external reset from, or sends a reset signal to, external devices. When generated internally the instruction resets all external devices without affecting the 68000. When RES and HLT are asserted by an external device, all devices are reset and the 68000 executes its reset vector at interrupt level 7 (non-maskable; highest priority).
22	BERR	I Lo	Bus Error terminates the current bus cycle due to an error. If HLT is asserted, the 68000 prepares to rerun the cycle, and does so when HLT is negated. If HLT is negated, the 68000 executes its bus error vector. (Pullup resistor.)
15	CLK	I Hi	Clock input from the QNA2, frequency 10MHz.

Power Supply

Pin	Name	Sense	Description
14,49	Vcc	I	+5V Power rail.
16,53	Vss		Gnd Earth rail.

A.2.3 Addressing

The 68000 uses an asynchronous bus structure with separate address and data buses. The processor executes read and write cycles to transfer bytes and words from and to shared buffer RAM, using the function code and bus control signals to control the transfer.

The Test and Set (TAS) instruction operates on bytes only to provide interprocessor communication. The instruction is executed by an indivisible read-modify-write cycle; during this cycle AS (Address Strobe) is asserted throughout.

Bus arbitration is controlled using the Bus Arbitration signals to determine whether the 68000 or an external device is acting as bus master.

A.3 Q-BUS INTERFACE CONTROLLER (QIC)

A.3.1 Overview

This section describes the DIGITAL Q-Bus Interface Controller (QIC). It is intended only to describe the functions of the QIC that are used in the DELQA module. It is not a complete QIC specification; nor does it include details of Q-Bus operations.

The QIC is a general-purpose Q-Bus Interface Controller, which provides complete Q-Bus slave control logic. The QIC is packaged in an 84-pin plastic leaded chip-carrier (plcc). Together with 2 8641-2 and 4 DC021 transceivers, the QIC forms a complete Q-Bus interface design.

All internal registers are dual-ported for access from the Q-Bus of the host system and the backport bus of the module.

On the Q-Bus side, the QIC uses control DMA (based on Buffer Deescriptor Lists) and data DMA, using block-mode to achieve the highest possible speeds.

On the backport side, the QIC uses DMA to transfer data to and from shared buffer RAM and on-board registers (if supported by the module). The backport has 16 data/address lines and up to four control lines. The main controller can program the QIC registers and initiate DMA transfers to and from the Q-Bus.

Internally the QIC provides:

- Complete Q-Bus slave control logic
- I/O page addressing, with: slave address matching and a programmable base-address register.
- DMA arbitration and control, both block-mode and non-block-mode
- 22-bit Q-Bus DMA address register/counter
- 15-bit DMA word-count register
- 16-bit backport DMA address register/counter and control
- 22-bit host DMA access mechanism using BDL (Buffer Descriptor Lists) stored in host memory.
- Multi-level interrupt control
- Non-existent-memory (NXM) timeout
- Holdoff timer to separate DMA requests so that other units can access the Q-Bus
- Ability to initiate host reboot.

The architecture of the QIC is shown in the block diagram.

A.3.2 Signals and Pinouts

The signals for each pin of the QIC are shown in Figure A–3, and the signals are described in Table A–2. Some of the QIC signals share pins on the IC, and the circuit designer will have chosen one function or the other.

Some modules do not use all the functions provided by the QIC. Unused outputs are not connected; unused inputs are tied high or low as appropriate.

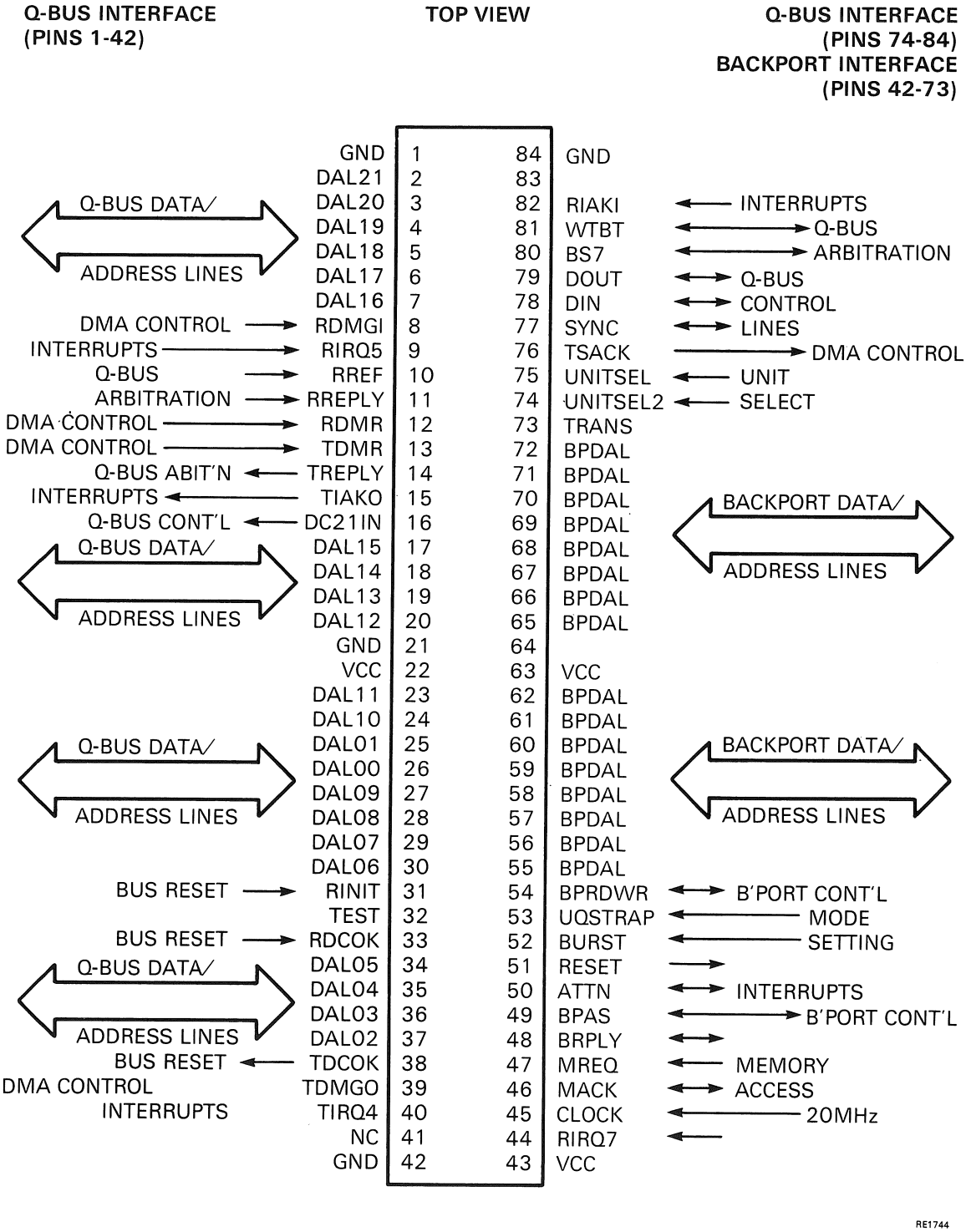


Figure A–3 QIC Pinouts

Table A–2 QIC Signal Descriptions

QIC to Q-Bus Interface: Address and Data Bus Control

02:05	DAL<21:18>	I/O Hi	Data/Address Lines, connected as follows to the DC021 transceivers:
06:07	DAL<17:16>		DAL<15:08> to DC021 number 3;
17:20	DAL<15:12>		DAL<21:20,07:02> to DC021 number 2;
23:24	DAL<11:10>		DAL<19:16,01:00> to DC021 number 1;
25:26	DAL<01:00>		DAL<00> is held low for data DMA, high for control DMA transfers.
27:30	DAL<09:06>		
34:37	DAL<05:02>		DAL<21:18> are Address lines.
			DAL<17:16> are Memory parity/Address lines.
			DAL<15:00> are Data/Address lines.

QIC to Q-Bus Interface: DMA Control

Pin	Name	Sense	Description
08	RDMGI	I Hi	Receive DMA Grant In (with pulldown resistor), from the Q-Bus signal BDGMI (receive), using DC021 number 1.
12	RDMR	I Hi	Receive DMA Request, which connects to the Q-Bus signal BDMR (receive), using 8641 transceiver number 2.
13	TDMR	O Hi	Transmit DMA Request, which is sent to the Q-Bus signal BDMR (transmit), using 8641 transceiver number 2.
39	TDMGO	O Hi	Transmit DMA Grant Out, which is sent to the Q-Bus signal BDMGO (transmit), using 8641 transceiver number 1 (with a pulldown resistor).
76	TSACK	O Lo	Transmit DMA Selection Acknowledge, which controls the direction of transfer of DC021 number 4.

QIC to Q-Bus Interface: Interrupts control

Pin	Name	Sense	Description
09	RIRQ5	I Hi	Receive Interrupt Request Level 5 (with pulldown resistor), from the Q-Bus signal BIRQ5 (receive), using DC021 transceiver number 1.
15	TIAKO	O Hi	Transmit Interrupt Acknowledge Out, which is sent to the Q-Bus signal BIAKO, using DC021 number 4 (with a pulldown resistor).
40	TIRQ4	O Hi	Transmit Interrupt Request Level 4, which is sent to the Q-Bus signal BIRQ4 (transmit), using 8641 transceiver number 2.
41	TIRQ6	O Hi	No connection.
44	RIRQ7	I Hi	Tied inactive low.
82	RIAKI	I Hi	Receive Interrupt Acknowledge In (with pulldown resistor), from the Q-Bus signal BIAKI, using DC021 number 4.

Table A–2 (Cont.) QIC Signal Descriptions

Pin	Name	Sense	Description
83	RIRQ6	I Hi	Receive Interrupt Request Level 6 (with pulldown resistor), from the Q-Bus signal BIRQ6 (receive), using DC021 number 1.

QIC to Q-Bus Interface: Address and Data Bus Control

Pin	Name	Sense	Description
11	RREPLY	I Hi	Receive Reply, from the Q-Bus signal BRPLY (receive), using 8641 transceiver number 2.
14	TREPLY	O Hi	Transmit Reply, which is sent to the Q-Bus signal BRPLY (transmit), using 8641 transceiver number 2.
80	BS7	I/O Hi	Bank Select 7 (tristate signal), which connects to the Q-Bus signal BBS7, using DC021 number 4.
81	WTBT	I/O Hi	Write Byte (tristate signal), which connects to the Q-Bus signal BWTBT, using DC021 number 4.
16	DC021IN	O Hi	DC021 Input controls the direction of transfer of DC021 numbers 1 to 3.

QIC to Q-Bus Interface: Address and Data Bus Control

Pin	Name	Sense	Description
77	SYNC	I/O Hi	Synchronise (tristate signal), which connects to the Q-Bus signal BSYNC, using DC021 number 4.
78	DIN	I/O Hi	Data Input (tristate signal), which connects to the Q-Bus signal BDIN, using DC021 number 4.
79	DOUT	I/O Hi	Data Output (tristate signal), which connects to the Q-Bus signal BDOUT, using DC021 number 4.

QIC to Q-Bus Interface: Bus Control

Pin	Name	Sense	Description
10	RREF	I Hi	Refresh, from the Q-Bus signal BREF, using 8641 transceiver number 1.
31	RINIT	I Hi	Receive Initialise, from the Q-Bus signal BINIT, using 8641 transceiver number 1. This signal is asserted each time the Q-Bus host executes a Reset instruction.
33	RDCOK	I Lo	Receive DCOK, from the Q-Bus signal BDCOK (receive), using 8641 transceiver number 1. When RINIT is active at the same time, the QIC asserts ATTN to alert the 86000 microprocessor.
38	TDCOK	O Lo	Transmit DCOK, which is sent to the the Q-Bus signal BDCOK (transmit), using 8641 transceiver number 1.

Table A–2 (Cont.) QIC Signal Descriptions

QIC to Q-Bus Interface: Unit Select

Pin	Name	Sense	Description
74 75	UNITSEL<2> UNITSEL<1>	I Hi	Unit Select pins at powerup are reflected in mode register 2, bits <15:14>. UNITSEL<1> is connected to a test point to provide an external select facility.
75	EXTSEL	I Hi	External Select.

QIC to Q-Bus Interface: Power

Pin	Name	Sense	Description
1, 21, 42, 64, 84	Gnd		Signal ground.
22,43, 63	Vcc		+5V Power rail.

QIC to Backport Interface: Address and Data Bus

Pin	Name	Sense	Description
72:65	BPDAL<15:08>	I/O Hi	Backport Data/Address Lines (tristate)
62:55	BPDAL<07:00>		

QIC to Backport Interface: System Control and Timing

Pin	Name	Sense	Description
32	TEST	I Lo	Test mode. Tied inactive high.
45	CLOCK	I	20MHz TTL clock, shared with QNA2.
53	UQSTRAP	I Hi	Tied inactive low.

QIC to Backport Interface: Memory Access

Pin	Name	Sense	Description
47	MREQ	O Hi	Memory Request, sent to QNA2 during backport DMA to request access to shared buffer RAM, and negated one clock pulse after MACK is received in response.
46	MACK	I Hi	Memory Acknowledge, received in response to MREQ during backport DMA. This enables both the DMA address onto the backport bus, BPDAL<15:00>, and also BPAS, BPRDWR, and BPRPLY. This signal must be synchronous to the 20 MHz clock.

Table A–2 (Cont.) QIC Signal Descriptions

QIC to Backport Interface: Backport Bus Control

Pin	Name	Sense	Description
49	BPAS	I/O Lo	Backport Address Strobe (tristate, with pullup resistor) indicates that a valid address on BPDAL<15:00> can be latched on the asserting edge.
54	BPRDWR	I/O Hi LO	Backport Read/Write (tristate signal) Lo indicates the direction of transfer. BPRDWR is asserted through most of the transfer cycle. In Read operations, BPRDWR is negated after the QIC latches the data, so that the backport master can start reading.

QIC to Backport Interface: DMA Control

Pin	Name	Sense	Description
48	BPRPLY	I/O Hi	Tied high.
52	DMARDY	I Lo	This pin is used to indicate to the QIC that backport transfer should not be attempted, when negated (high). Host I/O page accesses, vector fetches and control DMA are unaffected by the state of this pin.
73	TRANS	I/O Hi	Not used - Tied Low.

QIC to Backport Interface: Interrupt Control

Pin	Name	Sense	Description
50	ATTN	O Lo	Attention asserts an interrupt to the 68000, in order to indicate an error or a completion.
51	RESET	O Lo	Not used.

A.3.3 Q-bus Addressing

The QIC must be initialised by the 68000 on power up. When the QIC powers up its registers are visible to the 68000 via the backport bus at either address 81FF00 or 81FF20, depending on the state of MR1<06>. The state of MR1 is dependant on the setting of UNITSEL2 at power up.

In order to enable host access, the base address register must be programmed according to the setting of switch 1 at power up. The 68000 can read the value of the switch in bit 15 of QIC Mode Register 2. (81ff24)

The I/O page addresses are determined by:

15	I/O Page
0	17774440
1	17774460

The base address is programmed as follows:

11111BBBBBBBBBBB0 - for Q-Bus (18-bit address range)

111111111BBBBBBBBBBB0 - for Q22-Bus systems (22-bit address range)

where BBBBBBBBBBB is programmed into IOBAR (81FF22). These 12 bits relate to the corresponding 12 bits in the Q-Bus I/O page address.

Thus to program an I/O page address of 17774440 the bits 110010010000 should be written to IOBAR bits <12:1>. In addition bit <13> must be written to 1, to enable internal QIC comparison.

The QIC will do a backport DMA read/write whenever one of these addresses is accessed by the host. The QIC determines the address (16 bits) that it will put on the backport by the following:

11111111XXXXXXX0

The number of X's is determined by the block size ie if the block size (programmed in QIC mode register 2) is set to 8 then bits <3:1> are set to X. If a block size of 32 is programmed then bits <5:1> are set to X. In the case of the DELQA the block size is 8 so the QIC maps to:

111111110000YYY0

The value of Y bits correspond directly to the Q-Bus address in those bit locations. Thus Q-Bus address 17774440 corresponds to backport address 1111111100000000 and 17774454 corresponds to:

1111111100001100 (FF0CH)

The DELQA must place the vector address on the Q-Bus DALs with the QIC fetching the vector from the backport as part of the Q-Bus interrupt acknowledge cycle. The backport address used by the QIC is computed as follows:

1111LLLLLLLLXXX0

The value L is programmed into QIC register 81FF34 (Control Mask / Dir / BP-Addr) by the 68000.

The value XXX is determined by the interrupt type. Only vector 1 is used on the DELQA.

XXX - 100 VECTOR 1

XXX - 101 VECTOR 2

This register is also used to hold the address for Control - DMA's according to:

XXX - 000 CDMA WORD 1

XXX - 001 CDMA WORD 2

XXX - 010 CDMA WORD 3

XXX - 011 CDMA WORD 4

Thus when the QIC is programmed to perform a Control DMA it will read or write the relevant data from address:

1111LLLLLLLLXXX0

where value L is programmed into QIC register 81FF34 (Control Mask/Dir/BP-Addr) by the 68000 and XXX is determined by the word involved in the transfer.

A.3.4 QIC Registers

Table A-3 lists the QIC registers and their relative position in the backport memory map.

Table A–3 Registers

Number	Register
00	Mode Register 1
01	Q-Bus I/O base address register (IOBAR)
02	Mode Register 2
03	Attention register
04	Data DMS Q-Bus address counter (HI)
05	Data DMA Q-Bus address counter (LOW)
06	Backport DMA byte counter
07	Backport DMA address counter
08	Contol DMA Q-Bus address counter (HI)
09	Control DMA Q-Bus address counter (LOW)
10	Control DMA Mask/Dir/BP-Addr
11	Asserts RS<0> (not used)
12	Asserts RS<1> (not used)

A.4 QNA2 Q-BUS NETWORK ARBITRATOR

A.4.1 OVERVIEW

The QNA2 is packaged in a 68-pin, surface-mounted plastic leaded chip-carrier (plcc). The device is created with an LSI logic 2220-cell gate array.

The QNA2 controls access to the multiport memory system on the a backport bus. It arbitrates between requests from the QIC, the LANCE, and the 68000 microprocessor, granting access rights to these three devices on a shared time basis.

Access is granted according to the following order of priority:

1. QIC
2. 68000 microprocessor
3. LANCE.

The QNA2 implements the following control functions:

- Arbitration of access rights for QIC, 68000 microprocessor and LANCE
- Read/Write control logic for RAM and ROM accesses
- Read/Write control logic for QIC registers and LANCE registers
- Read/Write control logic for QNA2 registers
- LANCE and QIC DMA control
- 68000 control.

The architecture of the QNA2 is shown in the block diagram.

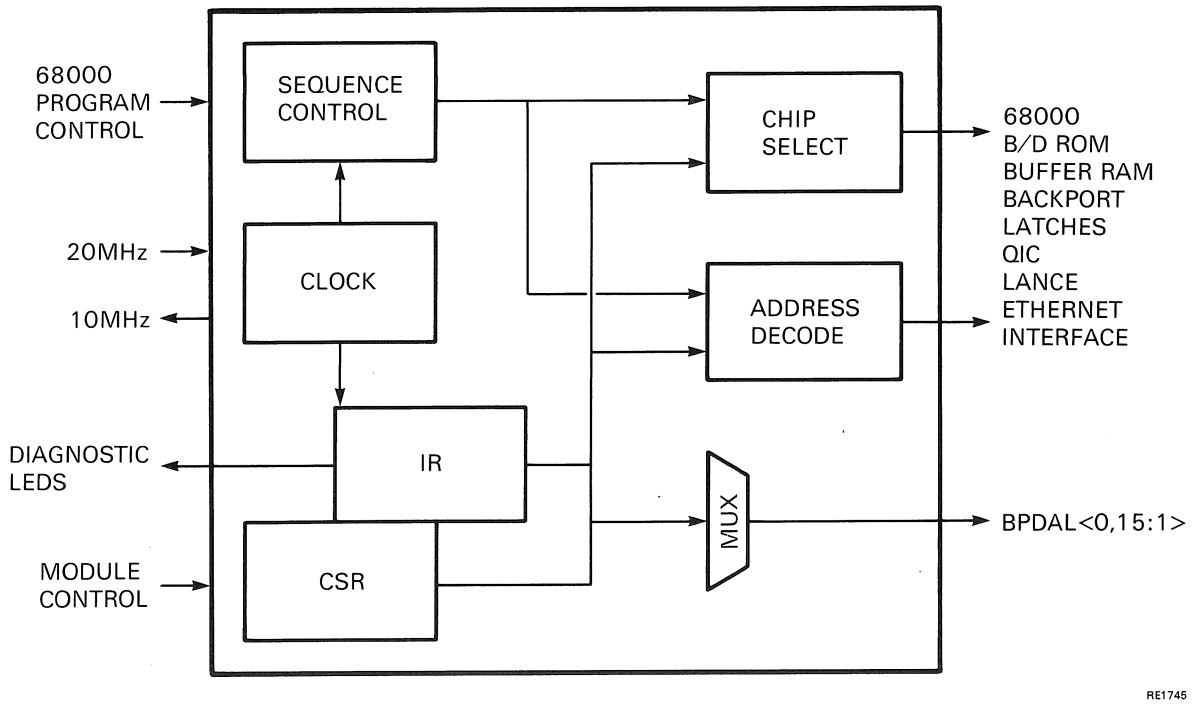


Figure A–4 QNA2 Block Diagram

A.4.2 SIGNALS AND PINOUT

The QNA2 controls all the gating on the DELQA board. It employs combinational logic to examine the access requests asserted on the backport bus, and then executes the appropriate control function for the request with the highest priority.

The three control sequences implemented by the QNA2 are:

1. QIC DMA transfers:
   a. Read/Write access to the QNA2 CSR.
   b. Read/Write access to shared RAM.
   c. Read only access to Station Address ROM.
2. 68000 microprocessor:
   a. Read/Write access to shared RAM.
   b. Read/Write access to QIC and QNA2 registers.
   c. Read/Write access to the LANCE.
   d. Read access to firmware ROM.
   e. Read access to Station Address ROM.
3. LANCE DMA transfers:
   a. Read/Write access to shared RAM.

A.4.2.1 QNA2 Signal Descriptions

Table A–4 QNA2 Signal Descriptions

Backport Interface: Address and Data Bus

Pin	Name	Sense		Description
02:04	BPDAL<13:15>	I/O	Hi	Backport Data/Address lines, used as follows:
47:50	BPDAL<00:03>			BPDAL<15:00> data word transfers;
53:56	BPDAL<08:11>			BPDAL<07:00> control byte transfers;
63:67	BPDAL<04:07,12>			BPDAL<00,15:01> Backport DMA.

Backport Interface: QIC

Pin	Name	Sense		Description
05	MREQ	I	Hi	QIC request for access to RAM or to QNA2 registers. No synchronisation needed since QIC and QNA2 share a 20MHz clock.
06	MACK	O	Hi	Acknowledge MREQ.
07	BPRDWR	I/O	Hi/Lo	Backport Read/Write indicates direction of data transfer. Hi-to-Lo transition terminates a slave read access by enabling the tristate gates.

Table A–4 (Cont.) QNA2 Signal Descriptions

Pin	Name	Sense		Description
08	BPAS	O	Lo	Backport Strobe latches a QIC register address for a slave read or write.

Module Control and Timing

Pin	Name	Sense		Description
09	CLOCK	I	Hi	20 MHz clock (shared with QIC).
13	INIT	I	Lo	Initialise pulse clears all register bits and output functions, and sets the control sequencer to idle.
16	JMPR3	I	Lo	Select access time for 68000 ROM: Hi = 150ns.; Lo = 250ns. Preset to Lo. If Hi, DTACK is generated 100 ns. earlier.
21	JMPR2	I	Hi	Select Option, connected to option switch S4 of the 5-way switchpack, and reflected in IR bit 10. For DEQNA-Lock mode (mode switch S3=0): select sanity timer. For Normal mode (mode switch S3=1): select MOP Remote Boot.
22	JMPR1	I	Hi	Select Mode, connected to switch S3 of the 5-way switchpack, and reflected in IR bit 5. S3=1=Normal mode; S3=0=DEQNA-Lock mode.
32	OINIT	O	Lo	The state of this pin is the inversion of CSR bit 1 (SR)

Diagnostic Signals

10	LED2	O	Lo	Diagnostic output to LED2 driver.
11	LED1	O	Lo	Diagnostic output to LED1 driver.
12	LED0	O	Lo	Diagnostic output to LED0 driver.
20	ELOOP	O	Hi	Ethernet Loopback, reflects CSR bit 9 and selects the MSB of Station Address ROM.

Ethernet Interface

Pin	Name	Sense		Description
14	RENA	I	Hi	Receive Enable signal from the SIA.
15	FUSE	I	Hi	Power indicator from the BULKHEAD FUSE. This signal is fed directly to CSR bit 12.

Backport Interface: LANCE

Pin	Name	Sense		Description
19	LADR	O	Hi	LANCE Address Select, (re)set each time ADS (Address Strobe) is asserted with ADR21 (un)set.

Table A–4 (Cont.) QNA2 Signal Descriptions

Pin	Name	Sense		Description
23	LREAD	I/O	Hi/Lo	LANCE Read indicates the direction of transfer (Hi=read; Lo=write) for both slave and DMA accesses.
24	LDAS	I/O	Lo/Hi	LANCE Data Strobe to/from the LANCE,asserted by: a. 68000-to-LANCE read/write control sequence. b. LANCE DMA read/write cycle. (Pullup resistor).
25	LHLDA	O	Lo	LANCE Hold Acknowledge, asserted in response to LHOLD only when there is no valid slave access by the 68000.
26	LHOLD	I	Lo	LANCE DMA Request. (Pullup resistor).
36	LREADY	I/O	Lo/Hi	LANCE DMA Ready, used as follows: Lo - the QNA2 control sequence responds to a LANCE DMA cycle; Hi - the LANCE indicates completion of 68000 slave accesses.
37	LCS	O	Lo	LANCE Chip Select, asserted for each complete 68000 read/write cycle.
43	LEN	O	Lo	LANCE Data Latch Enable (backport bus).
44	LCAB	O	Hi	LANCE Data Latch from backport bus, allowing the LANCE control sequencer to terminate in its own time when: a. 68000 writes to the LANCE; b. LANCE DMA reads RAM.
45	LDIR	O	Hi	LANCE Data Latch Direction, presented before LENL to avoid tristate overlaps.
57	LAOE	O	Lo	LANCE Address Output enables the address latches on DMA cycles. (The address is latched by LALE from the LANCE).

Backport Interface: 68000

Pin	Name	Sense		Description
27	IPL2	O	Lo	Interrupt Level 2, asserted to 68000 as the result of a host write to the CSR, VAR, TXBDL, RXBDL or after the QNA2 timer has expired.
28	R/W	I	Hi/Lo	Read/Write from 68000.
29	ADS	I	Lo	Address Strobe from 68000
30	CPCLK	O	Hi	10MHz clock for the 68000 microprocessor.
31	VPA	I	Lo	Valid Peripheral Access, the result of a NAND operation on FC0+FC1+FC2 and the inverse of ASM, indicating an active interrupt acknowledge cycle. This inhibits 68000 access cycles.
33	DTACK	O	Lo	Data Transfer Acknowledge to 68000.

Table A–4 (Cont.) QNA2 Signal Descriptions

Pin	Name		Sense	Description
38	A21TES	I/O	Hi/Lo	Address Bit 21/Test, used with ADS to clock in BPDAL21 and assert LADR.
39:40	ADR<22:23>	I	Hi	Address Bits <23:22> indicate to the control sequencer the device addressed: 00 68000 to ROM access 01 68000 to RAM access 10 68000 to QIC access 11 68000 to LANCE access
46	CPDIR	O	Hi	Control Port Direction for the 68000 data transceivers.
58	CPDOE	O	Lo	Control Port Data Output Enable for the 68000 data transceivers.
59	CPAOE	O	Lo	Control Port Address Output Enable for the 68000 address latch.
Backport Interface: Memory				
41	SELROM	O	Lo	Select 68000 Firmware ROM.
42	SELSAR	O	Lo	Select Station Address ROM.
61	MWE	O	Lo	Memory Write Enable.
62	MCSL	O	Lo	Memory Chip Select.
Backport Interface: Backport Bus Control				
Pin	**Name**		**Sense**	**Description**
60	MALE	O	Lo	Memory Address Latch selects the two F373 latches on the backport bus. The associated DMA cycle may be initiated by 68000 or QIC.
Power lines				
Pin	**Name**			**Description**
01,18,35,52	Vss			Signal ground.
17,34,51,68	Vcc			+5V Power rail.

A.4.2.2 Pinout

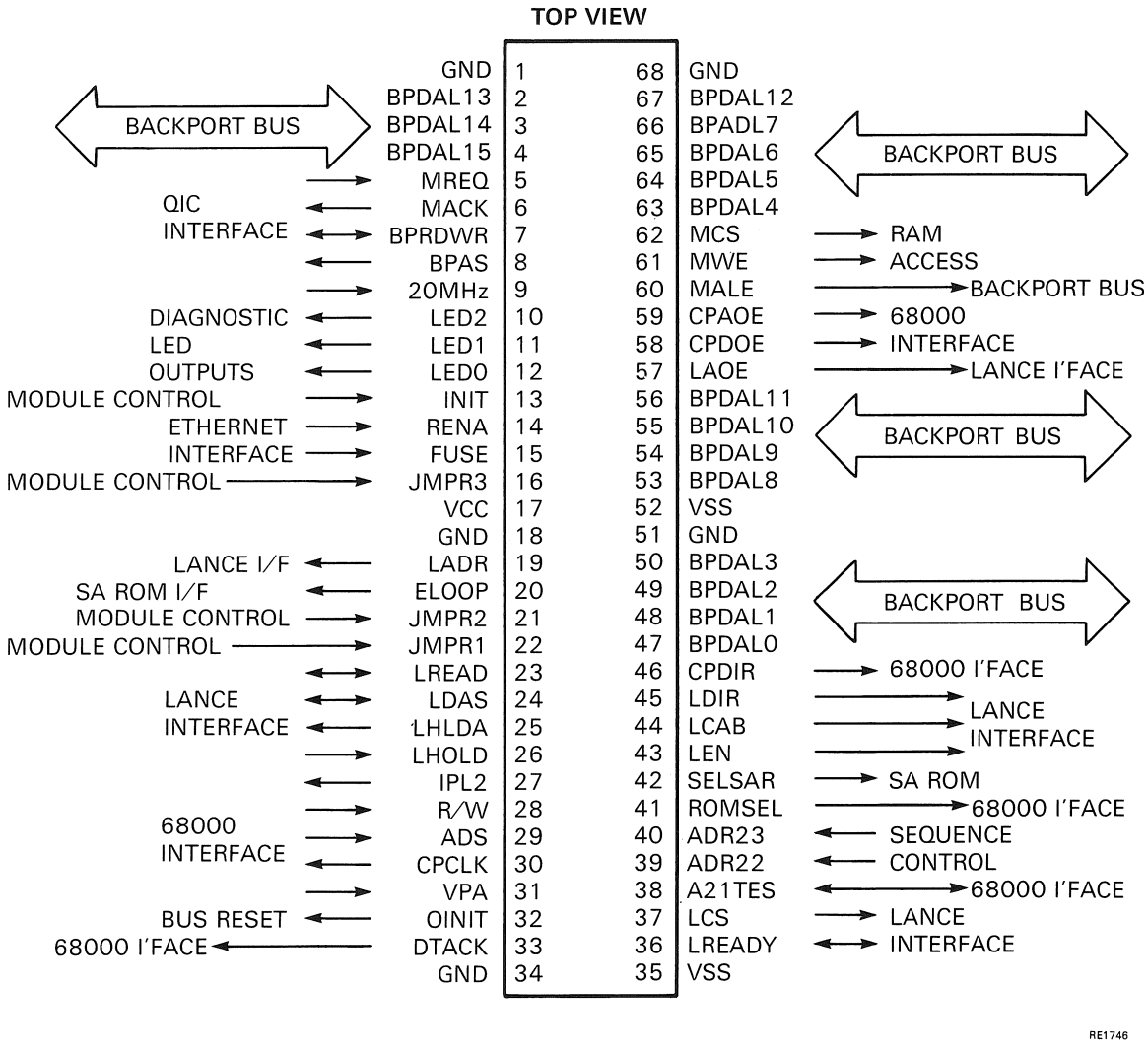


Figure A–5 QNA2 Pinout

A.4.2.3 Addressing

Table A-5 lists the QNA2 registers together with their backport memory map addresses, while Tables A-6 and A-7 contain their bit definitions.

Table A–5 QNA2 Registers

Backport Address (HEX)	Register
40FF0E	Control and status Register (CSR)
40FF1E	Interrupt Register (IR)

Table A–6 CSR Register Bit Definitions

Bit Number		Access by 68000	Access by QIC	Description
0	RE	R	R/W	Receiver Enable
1	SR	R	R/W	Software Reset
2	NI	R/W	R	Non-Existent
3	BD	R	R/W	Boot/Diagnostic ROM Load
4	XL	R/W	R	Transmit List invalid
5	RL	R/W	R	Receive List invalid
6	IE	R	R/W	Interrupt enable
7	XI	RW	RW	Transmit interrupt
8	IL	R	R/W	Internal Loopback
9	EL	R/W	R/W	External Loopback
10	SE	R	R/W	Sanity Timer enable
11	RR	-	-	Reserved
12	OK	R	R	Fuse OK
13	CA	R	R	Carrier from SIA
14	PE	R/W	R	Parity error
15	RI	R/W	R/W	Receive interrupt

NOTE

All bits except 04/05 are cleared at powerup and on software reset. Powerup and software reset have no effect on bit 12.

Table A–7 Interrupt Register Bit Definitions

Bit Number	Access by 68000	Access by QIC	Description
0	R/W		Timer interrupt
1	R/W		CSR write interrupt
2	R/W		Vector write interrupt
3	R/W		TX BDL write interrupt
4	R/W		RX BDL write interrupt
5	R/W		JMPR 1
6	R/W		SAROM Select
7	-		-
8	-		-
9	-		-
10	-		-
11	-		-
12	JMPR 2		
13	R/W		LED 2
14	R/W		LED 1
15	R/W		LED 0

NOTE
All bits except 13:15 are cleared at powerup and on software reset. Powerup and software reset have no effect on bits 12 and 5.

A.5 AM7990 LOCAL AREA CONTROLLER FOR ETHERNET (LANCE)

A.5.1 Overview

The LANCE operates with the SIA (from the same family of LSI devices) to provide a complete interface between the backport bus and the Ethernet cable. The LANCE is a 10Mbit/sec MOS device in a 48-pin package. It implements the following facilities for the link level of the Ethernet protocol:

- CSMA/CD network access
- Memory management using on-board DMA
- Error reporting
- Packet handling

- Microprocessor interface.

In transmit mode, the LANCE initiates a DMA cycle to transfer data from shared RAM. It prefaces the data with the standard preamble and synchronisation pattern, and it calculates and appends a 32-bit CRC.

In receive mode, the SIA asserts Carrier Present to the LANCE, in order to indicate that two signals are available: Receive Data and Receive Clock. The LANCE uses Receive Clock to clock in the Receive Data signals. Then it calculates and compares the CRC to the CRC checksum at the end of the packet. If the two values do not match, the LANCE sets an error bit and flags an interrupt to the 68000 microprocessor.

There are three addressing modes:

- Physical addressing, in which a 48-bit destination address at the front of an incoming packet is compared with the node address written to the LANCE at initialisation
- Multi-cast addressing, in which the LANCE accepts all incoming packets for a certain class of node
- Promiscuous operation, in which the LANCE accepts all incoming packets.

In its buffers, the LANCE sets up circular task queues known as descriptor rings. The tasks are used for transmit and receive operations; up to 128 tasks may be queued for execution.

The architecture of the QIC is shown in Figure A–6.

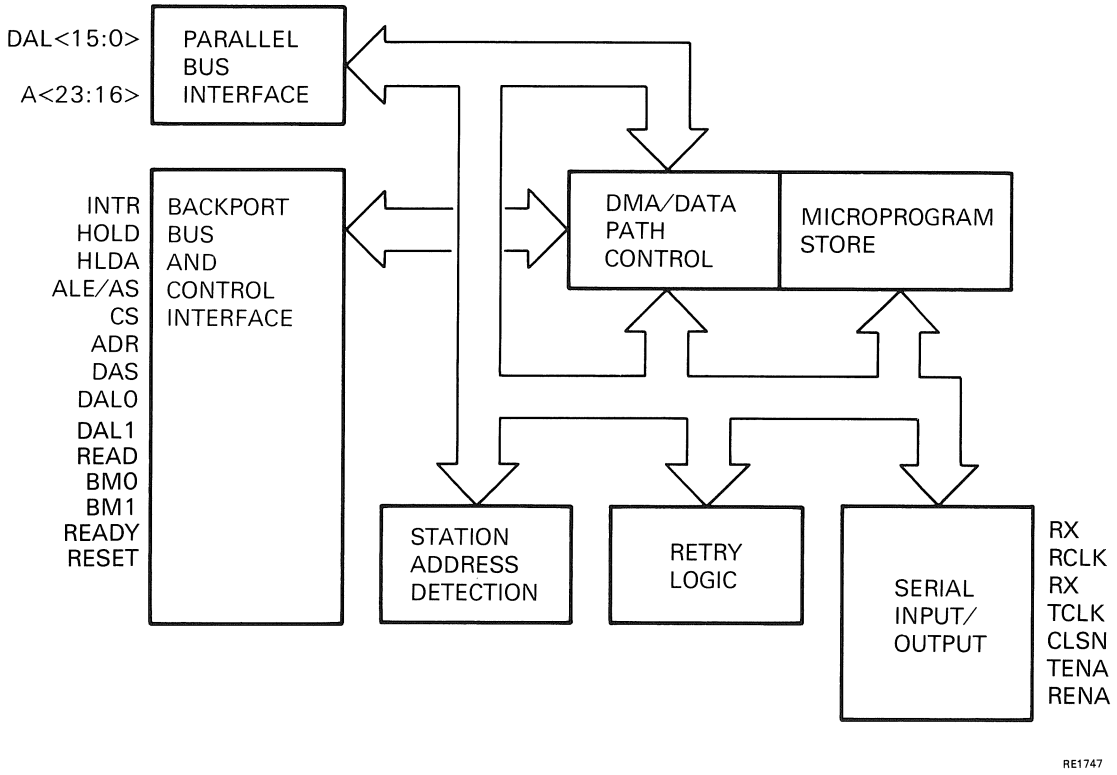


Figure A–6 AM7990 LANCE Block Diagram

A.5.2 Signals and Pinout

The signals to and from each QIC port fall into logical groups. The functions, signals and pinouts of these groups are shown in Figure A–7 and described in Table A–8.

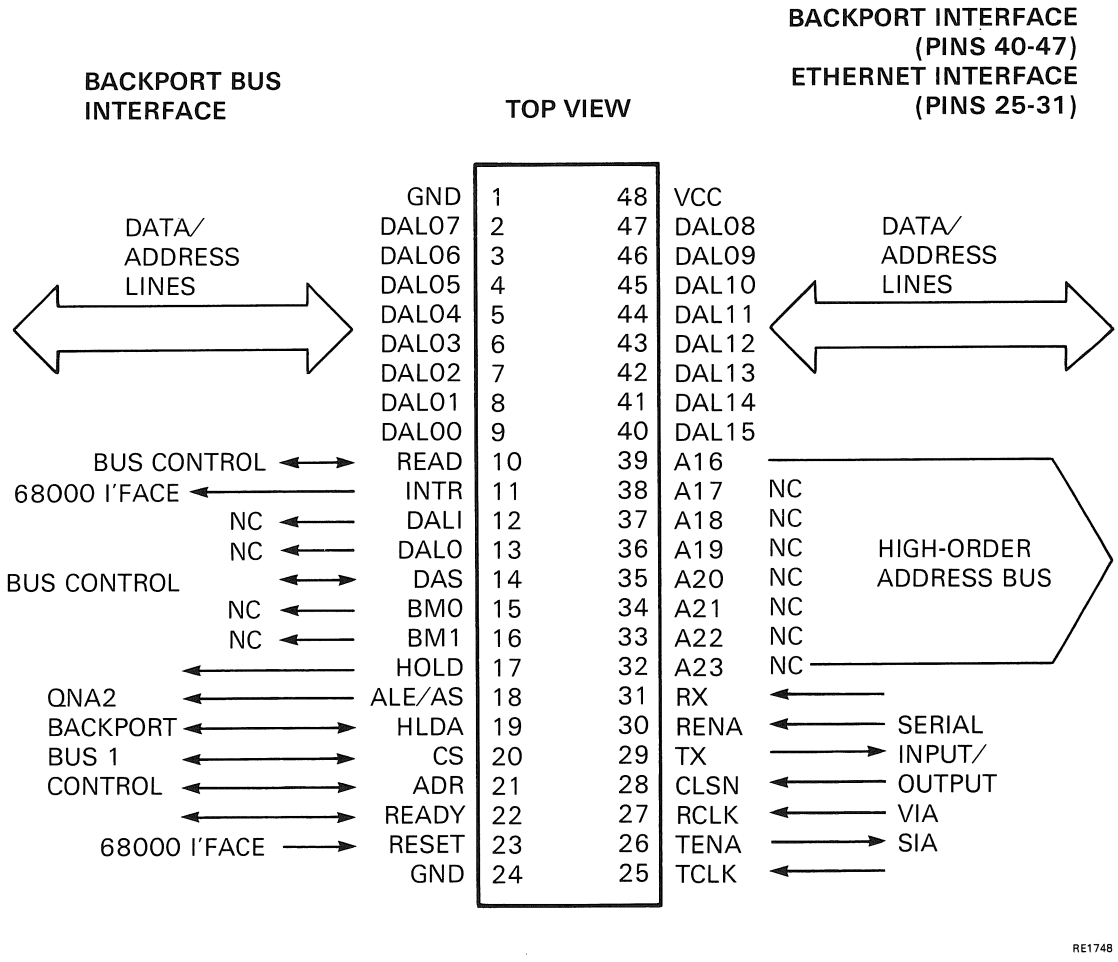


Figure A–7 AM7990 LANCE Pinouts

Table A–8 AM7990 LANCE Signal Definitions

Backport Interface: Address and Data Bus

02:09	DAL<07:00>	I/O Hi	Data/Address lines (tristate). During
40:47	DAL<15:08>		address select, A<23:16> contains the
32:39	A<23:16>	O Hi	upper 16 address bits.

Backport Interface: Backport Bus Control

Pin	Name	Sense	Description
10	READ	I/O Hi	Read indicates the direction of data transfer. Reading when the LANCE is bus master; writing when LANCE is bus slave.
12	DALI	O Lo	Data/Address Line In (tristate).
13	DALO	O Hi	Data/Address Line Out (tristate). (Not used).
14	DAS	I/O Lo	Data Strobe (tristate).
15	BM0/BYTE	O Lo/Hi	Byte Mask/Byte.
16	BM1/BUSAKO	O Lo/Lo	Byte Mask/Bus Request Daisy Chain Output. These tristate signals are programmable through bit 0 of CSR3. (No Connection.)
17	HOLD/BUSRQ	O Lo/Lo	Bus Hold Request (open drain). This signal is programmable through bit 0 of CSR3 (Pullup resistor).
18	ALE/AS	O Lo/Hi	Address Latch Enable. This tristate signal is programmable through bit 1 of CSR3 (Pullup resistor).
19	HLDA	I Lo	Bus Hold Acknowledge, asserted in response to HOLD to make the LANCE bus master.
20	CS	I Lo	Chip Select puts the LANCE into bus slave mode for a data transfer to or from the LANCE registers. This signal must not be asserted with HLDA.
21	ADR	I Hi	Register Address Port Select.
22	READY	I/O Lo	Data Transfer Ready (open drain).

Table A–8 (Cont.) AM7990 LANCE Signal Definitions

SIA Interface: Ethernet I/O

Pin	Name	Sense	Description
10	READ	I/O Hi	Read indicates the direction of data.
25	TCLK	I Hi	Transmit Clock (10MHz).
26	TENA	O Hi	Transmit Enable.
27	RCLK	I Hi	Receive Clock (10MHz square wave).
28	CLSN	I Hi	Collision (logical input).
29	Tx	O Hi	Transmit output bit stream.
30	RENA	I Hi	Receive Enable (logical input) indicates that a carrier is present on the Ethernet channel.
31	Rx	I Hi	Receive input bit stream (input).

SIA Interface: 68000 Interrupts Control

Pin	Name	Sense	Description
11	INTR	O Lo	Interrupt (open drain; pullup resistor).
23	RESET	I Lo	Bus Reset Request causes LANCE to stop, clear its internal logic, and idle.

Power lines

Pin	Name	Sense	Description
01	Vss		Signal ground.
48	Vcc	I	+5V Power rail.

A.5.3 LANCE Addressing

The LANCE has four Control and Status Registers, which are programmed from the 68000 microprocessor through two ports on the backport bus: the Register Data Port (RDP), and the Register Address Port (RAP).

To access the registers, the QNA2 first asserts CS to put the LANCE into bus slave mode. The 68000 then writes a CSR select code to the LANCE, which stores the code in its Register Address Port. Subsequent read/write accesses affect only the CSR selected.

A.5.4 LANCE Registers

Table A–9 lists the LANCE registers.

Table A–9 LANCE Registers

Register		Description
RAP	Register Address Port	Read/Write.
RDP	Register Data Port	Read/Write.
CSR0	Control and Status Register 0	Transmit/Receive error flags.
CSR1	Control and Status Register 1	Initialisation Block address.
CSR2	Control and Status Register 2	Initialisation Block address.
CSR3	Control and Status Register 3	Defines bus master interface.

A.5.5 LANCE Buffers

Table A–10 lists the contents of the Initialisation Block. Table A–11 lists the contents of the Descriptor Rings.

Table A–10 LANCE Initialisation Block

Bit/Name	Description
IADR + 0	Mode Register.
15 PROM	Promiscuous addressing mode.
14:07	Reserved.
06 INTL	Internal Loopback.
05 DRTY	Disable Retry on transmission.
04 COLL	Force Collision (diagnostic).
03 DTCR	Disable Transmit CRC (enables Multi-cast addressing in external loopback).
02 LOOP	Enable Loopback.
01 DTX	Disable Transmitter.
00 DRX	Disable Receiver.
IADR + 02	Physical Address (PA) .
47:00 PADR	Physical Address of LANCE .
IADR + 08	Logical Address Filter (LAF) .
63:00 LADRF	64-bit logical address mask.

Table A–11 LANCE Descriptor Ring Pointers

Bit/Name	Description
IADR + 18	Receive Descriptor Ring Pointer.
15:13 RLEN	Receive Ring Length, expressed as power of two.
12:08	Reserved.
07:00 RDRA	Receive Descriptor Ring (base) Address.
IADR + 20	Transmit Descriptor Ring Pointer.
15:13 TLEN	Transmit Ring Length, expressed as power of two.
12:08	Reserved.
07:00 TDRA	Transmit Descriptor Ring (base) Address.

Table A–12 LANCE Four-Word Descriptor Ring Formats

Receive Message Descriptor 0 (RMD0)

Bit/Name	Description
15:00 LADR	Low order 16 address bits of buffer described. Written by the host and unchanged.

Receive Message Descriptor 1 (RMD1)

Bit/Name	Description
15 OWN	Descriptor owned by LANCE (not host).
14 ERR	Error = OR operation on FRAM, OFLO, CRC, BUFF.
13 FRAM	Framing Error (not just CRC error).
12 OFLO	Overflow (internal silo).
11 CRC	CRC Error.
10 BUFF	Buffer Error (OWN bit zero, or silo overflow).
09 STP	Start of Packet.
08 ENP	End of Packet.
07:00 HADR	High order 8 address bits of buffer described.

Receive Message Descriptor 2 (RMD2)

15:12	Must be ones
11:00 BCNT	Buffer Byte Count (2's complement), written by host and unchanged.

Receive Message Descriptor 3 (RMD3)

Bit/Name	Description
15:12	Reserved.
11:00 MCNT	Message Byte Count (in BCD), when ERR is clear and ENP is set. Written by host and unchanged.

Transmit Message Descriptor 0 (TMD0)

Bit/Name	Description
15:00 LADR	Low order 16 address bits of buffer described. Written by the host and unchanged.

Transmit Message Descriptor 1 (TMD1)

Bit/Name	Description
15 OWN	Descriptor owned by LANCE (not host).

Table A–12 (Cont.) LANCE Four-Word Descriptor Ring Formats

Bit/Name	Description
14 ERR	Error = OR operation on LCOL, LCAR, UFLO, RTRY.
13	Reserved.
12 MORE	More than one retry needed.
11 ONE	Exactly one retry needed.
10 DEF	Transmit Deferred, due to busy channel.
09 STP	Start of Packet.
08 ENP	End of Packet.
07:00 HADR	High order 8 address bits of buffer described.

Transmit Message Descriptor 2 (TMD2)

Bit/Name	Description
15:12	Must be ones.
11:00 BCNT	Buffer Byte Count (2's complement), written by host and unchanged.

Transmit Message Descriptor 3 (TMD3)

15 BUFF	Buffer Error (OWN bit zero, or silo underflow).
14 UFLO	Underflow error. Message truncated due to late data from memory.
13	Reserved.
12 LCOL	Late Collision (channel slot time elapsed).
11 LCAR	Loss of Carrier (RENA negated during transmission).
10 RTRY	Retry Error, after either one or 16 attempts.
09:00 TDR	Time Domain Reflectometry (valid for RTRY).

A.5.6 Logical Address Filter

The LANCE maps each incoming 48-bit logical address from the Ethernet to the 64-bit logical address mask (stored at IADR+08 in the Initialisation Block).

If the first bit of the incoming physical address is set (PADR<0>=1), the address is passed to the logical address filter, which contains four 16-bit registers. All 48-bits of the incoming address are passed through the CRC circuit. The six high-order bits of the resultant 32-bit CRC are strobed into a register, where they are decoded to select a single bit position in the LAF. If that bit in the LAF is set, the incoming address is accepted.

This provisional assessment is then checked by comparing the full incoming logical address with the list of valid logical addresses that is stored in shared RAM.

The broadcast address does not go through this decoding process.

Table A–13 shows how LAF bit positions correspond to logical addresses.

Table A–13 LANCE Logical Address Filter Mask

Logical Filter Register	LAF bit	Destination Address (hex)	Logical Filter Register	LAF bit	Destination Address (hex)
LAF0	0	85	LAF2	32	21
LAF0	1	A5	LAF2	33	01
LAF0	2	E5	LAF2	34	41
LAF0	3	C5	LAF2	35	71
LAF0	4	45	LAF2	36	E1
LAF0	5	65	LAF2	37	C1
LAF0	6	25	LAF2	38	81
LAF0	7	05	LAF2	39	A1
LAF0	8	2B	LAF2	40	8F
LAF0	9	0B	LAF2	41	BF
LAF0	10	4B	LAF2	42	EF
LAF0	11	6B	LAF2	43	CF
LAF0	12	EB	LAF2	44	4F
LAF0	13	CB	LAF2	45	6F
LAF0	14	8B	LAF2	46	2F
LAF0	15	BB	LAF2	47	0F
LAF0	16	C7	LAF2	48	63
LAF0	17	E7	LAF2	49	43

Table A–13 (Cont.) LANCE Logical Address Filter Mask

Logical Filter Register	LAF bit	Destination Address (hex)	Logical Filter Register	LAF bit	Destination Address (hex)
LAF0	18	A7	LAF2	50	03
LAF0	19	87	LAF2	51	23
LAF0	20	07	LAF2	52	A3
LAF0	21	27	LAF2	53	83
LAF0	22	67	LAF2	54	C3
LAF0	23	47	LAF2	55	E3
LAF0	24	69	LAF2	56	CD
LAF0	25	49	LAF2	57	ED
LAF0	26	09	LAF2	58	AD
LAF0	27	29	LAF2	59	8D
LAF0	28	A9	LAF2	60	0D
LAF0	29	89	LAF2	61	2D
LAF0	30	C9	LAF2	62	6D
LAF0	31	E9	LAF2	63	4D

A.6 AM7991 SERIAL INTERFACE ADAPTER (SIA)

A.6.1 Overview

The SIA is a Manchester encoder/decoder which interfaces between the LANCE TTL logic and the Ethernet transceiver. It is a 24-pin package, and is located close to the Ethernet connector.

The SIA acquires clock and data within six bit-times, and decodes Manchester data with less than +/-20ns phase jitter at 10MHz. In order to minimise false start conditions, the SIA provides both guaranteed signal threshold limits and transient noise suppression circuitry in both data and collision paths.

A.6.2 Signal Description

The signals to and from the SIA fall into two logical groups. The functions, signals and pinouts of these groups are shown in Figure A–9 and described in Table A–14.

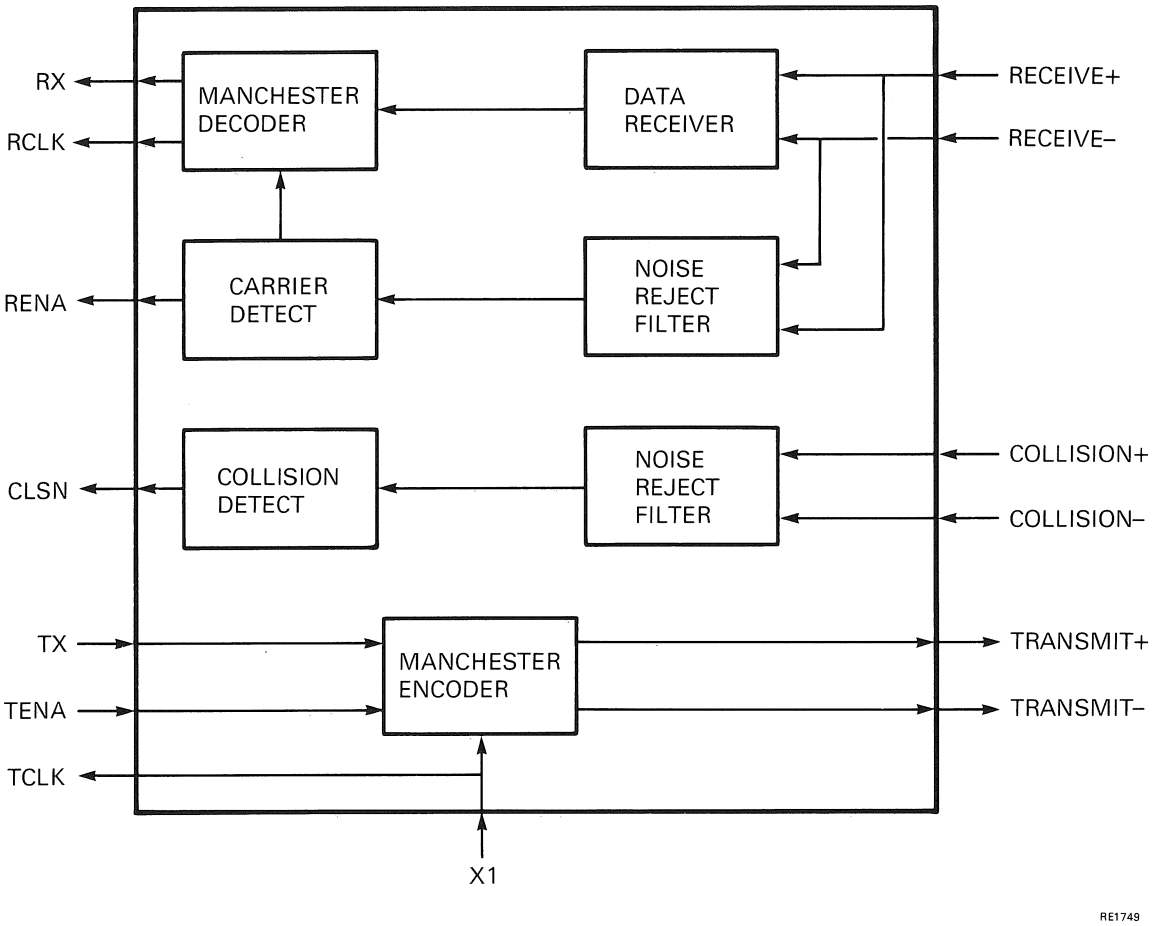


Figure A–8 AM7991 SIA Block Diagram

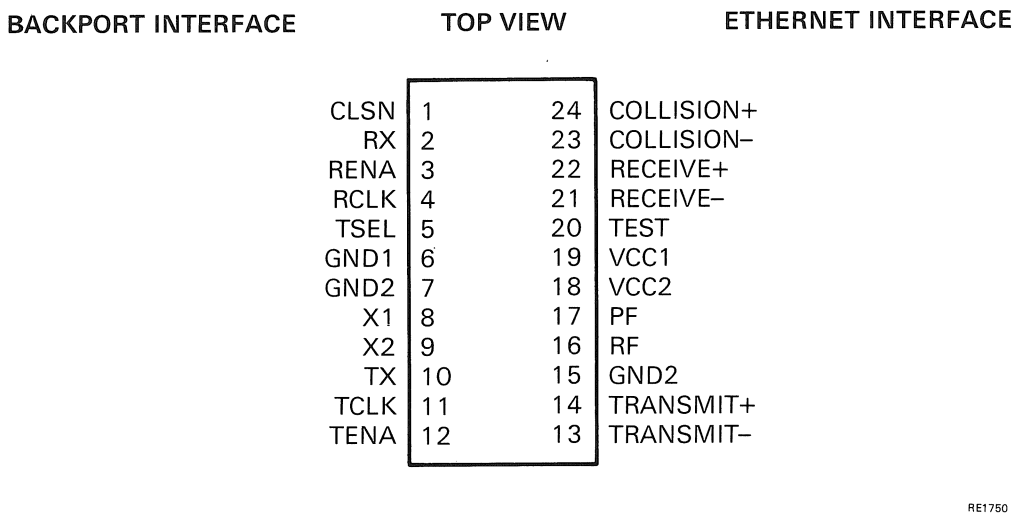


Figure A–9 AM7991 SIA Pinouts

Table A–14 AM7991 SIA Signal Definitions

Backport Interface

Pin	Name	Sense	Description
01	CLSN	O Hi	Collision
02	Rx	O Hi	Receive Data (TTL output)
03	RENA	O Hi	Receive Enable (TTL output)
04	RCLK	O Hi	Receive Clock (TTL output)
05	TSEL	I/O Hi	Transmit Mode Select (open collector output/sense amplifier input). When the transmitter is idle: TSEL low selects Transmit+ positive with respect to Transmit-; TSEL high selects Transmit+ equal to Transmit-.
06	Gnd1		High current ground
07	Gnd2		Logic ground
08	X1	I Hi	Biased crystal oscillator, used to generate TCLK
09	X2		Biased crystal oscillator, used to generate TCLK
10	Tx	I Hi	Transmit (TTL compatible)
11	TCLK	O Hi	Transmit Clock (TTL; symmetrical). This is also input to the LANCE
12	TENA	I Hi	Transmit Enable (TTL compatible)
15	Gnd3		Ground for voltage controlled oscillator
16	RF	O	Receive Frequency. A reference voltage for the receive path phase detector and and timing noise immunity circuits
17	PF	I	Phase Filter control voltage for phase lock loop damping (receive path)
18	Vcc2		+5V Power rail for voltage controlled oscillator in phase lock loop
19	Vcc1		High current and logic supply
20	TEST	I Lo	Test control

Table A–14 (Cont.) AM7991 SIA Signal Definitions

Pin	Name	Sense	Description
Ethernet Interface			
13	Transmit-	O	Transmit. Differential line outputs into terminated transmission lines
14	Transmit+	O	Transmit. Differential line outputs into terminated transmission lines
21	Receive-	I	Differential line inputs
22	Receive+	I	Differential line inputs
23	Collision+	I	Differential collision inputs, which do not affect data path functions.
24	Collision-	I	Differential collision inputs, which do not affect data path functions.

A.6.3 Noise Margins

On input the static noise margin for received carrier detection is -175mV to -275mV. Transient noise of less than 10nsec. in the collision path, and 16nsec. in the data path, are also rejected. The SIA will decode jittered data of up to +/-20nsec.

APPENDIX B
NETWORK MANAGEMENT

B.1 SCOPE

This appendix outlines the Ethernet Network Management protocol.

B.2 NETWORK CONTROL

To control access, Ethernet uses Carrier Sense Multiple Access with Collision Detection (CSMA/CD). This is a distributed channel allocation procedure under which every station receives all the transmissions from every other station. Each station can detect overlapping transmissions by other stations, and must wait for the bus to become idle before transmitting its message. There is no central or hierarchical control for this distributed process.

B.2.1 Ethernet Transmission

The data link layer checks that the network bus is clear of any baseband signal before it starts to transmit. When the channel is clear, the data link layer passes the data packet to the physical layer as a stream of bits. The physical layer precedes the data with an encoded preamble that allows the other nodes on the channel to synchronise their clocks. Then the physical layer starts to translate the binary encoded data into Manchester-phase-encoded signals.

Throughout the transmission, the physical layer monitors the correct energy level for transmission without contention in the channel. If the energy level exceeds this, then the physical layer sends a collision detect signal to the data link layer.

The collision detect signal can only be detected by a node that is transmitting.

B.2.2 Ethernet Reception

In the absence of other traffic on the channel, the physical layers of all other nodes in the network sense the carrier signal from a transmitting node. They alert their respective data link layers with a carrier sense signal, in order to delay any conflicting attempts to transmit.

The physical layer of each receiving node synchronises to the incoming preamble, receives the encoded bits from the cable, and translates the phase-encoded signal to binary encoded data, discarding the preamble.

At each of the receiving nodes, the binary bits are passed to the data link layer, which has been alerted to its arrival by the carrier sense signal. As the bit stream arrives, the data link layer checks the destination address. If the data is intended for that node, the packet is inspected for damage and alignment, before being passed on to higher levels of protocol with an indication of its condition. If the packet is not intended for that node, the bit stream is halted.

The physical layer continues to receive encoded bits from the channel until the carrier goes off.

B.2.3 Ethernet Contention

When two nodes simultaneously determine that the channel is free, and start to transmit, a collision occurs. Ethernet is designed to cater for such collisions by re-transmission following on a collision detect signal.

The Ethernet packet is specified to have a minimum length of 64 bytes because the time it takes to transmit such a packet over the maximum Ethernet configuration is slightly less than the time it takes for a collision detect signal to travel from one end of the network to the other and back again. (The elapse time for a round-trip signal is known as the network **slot time**).

This means that the collision detect signal from a node at the other end of the network has time to reach any originating node before that node has completed transmission of the packet that caused the collision. The originating node can then re-transmit the correct packet.

On receipt of a collision detect signal the data link layer at the transmitting node:

1. Continues to transmit the packet, in order to cause a **jam** that will be noticed by all other nodes.

2. **Backs off** and schedules a re-transmission attempt. The delay before re-transmission is an integral multiple of the slot time. The multiple is selected at random by each node for each collision.

The bits from a collision are known as a **runt packet** because the physical layers at all the receiving nodes accept the bits as though they were from a valid packet. However, the data link layers reject runt packets because they are always shorter than the shortest Ethernet packet.

B.2.4 Ethernet Fault Detection

Data integrity is maintained by the 32-bit CRC for each packet. This is handled by the data link layer protocol. Several network maintenance features are also built into the system:

1. **Time Domain Reflectometry**. Whenever a packet is transmitted, the transmitting node starts a timer and notes the times of all collisions. If the collision times are not random, but predictable and due to some physical fault, then the location of the fault be determined by time/speed/distance calculations.

2. **Time-limited operations**. Both controller and transceiver are designed to time out any transmission that is significantly longer than the Ethernet specification.

3. **Power supply monitor**. The controller monitors the power line direct from the transceiver; and the transceiver provides a positive test signal to the controller after every transmission to verify its operation.

4. **Loopback diagnostics**, both local and remote, are provided.

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