

LPS11

TEST #2

MD-11-DZLPD-C

EP-DZLPD-C-DL-A

OCT 1976

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IDENTIFICATION

PRODUCT CODE: MAINDEC-11-DZLPO-C
PRODUCT NAME: LABORATORY PERIPHERAL SYSTEM
DIAGNOSTIC TEST II
DATE: MAY 21, 1976
MAINTAINER: DIAGNOSTIC GROUP

FIRST PRINTING, 1973

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MD-11-02LPS-1

1. TESTS

TESTS AND EXERCISES THE "LPS". THE PROGRAM
 IS SELF-STARTING AND WHEN INITIATED WILL TYPE THE PROGRAM TITLE.
 THE PROGRAM IS COMPARISON. THE PROGRAM THEN TYPES A 'CR' AND
 A KEYBOARD MONITOR MODE FOR A LETTER TO BE TYPED.
 THESE TESTS MAY BE RUN IN ANY ORDER IT IS INTERACTIVE.
 LOGIC TESTS ARE RUN FIRST AND PROVED FULLY OPERATIONAL.
 THE PROGRAM IS POSSIBLE VIA THE TELETYPE. TYPING A 'C'
 (CONTAINED VIA TYPING THE 'CNTR' AND 'C' KEYS SIMULTANEOUSLY)
 WHILE RUNNING ANY TEST WILL ENABLE THE PROGRAM TO RETURN TO
 THE KEYBOARD MONITOR AND AWAIT A NEW LETTER DESIGNATOR TO BE
 TYPED. TYPING A 'M' WHILE IN MONITOR MODE WILL ENABLE THE LETTER
 DESIGNATORS TO BE RETYPED. IF RUNNING ON A NON-SWITCH REGISTER OF
 TYPING A 'CTRL G' WILL ALLOW THE CHANGING OF A SOFTWARE SWITCH REGISTER.

2. REQUIREMENTS (EQUIPMENT)

- A. PDP-11 COMPUTER WITH 8K OF MEMORY.
- B. TELETYPE
- C. LPS11 OPTION BOX WITH:
 - LPSKW REAL TIME CLOCK CONTROL AND/OR
 - LPSDR DIGITAL INPUT-OUTPUT CONTROL AND/OR
 - LPSVC POINT PLOT SCOPE CONTROL
 LPSDRA IS SUPPORTED BY A SEPERATE DIAGNOSTIC (MD-11-02LPS)

3. LOADING PROCEDURE

- A. USE STANDARD PROCEDURE FOR LOADING BINARY TAPES.

4. STARTING PROCEDURE

THE PROGRAM IS SELF STARTING WITH A RESTART ADDRESS OF '174' OR
 RE-INITIALIZED AT ADDRESS '200'.
 (FOR ADDITIONAL STARTING ADDRESSES REFER TO 11.)

5. CONSOLE SWITCH SETTINGS

- A. ALL SWITCHES SHOULD BE DOWN (0) WHEN THE PROGRAM IS STARTED.
- B. REFER TO THE INDIVIDUAL TEST DESCRIPTIONS FOR APPLICABLE
 CONSOLE SWITCH SETTINGS
- C. REFER TO 15. FOR SOFTWARE SWITCH REGISTER OPERATION.

* TYPE 'CARRIAGE RETURN' (CR) TO TERMINATE ALL INPUT DATA.

6. CLOCK LOGIC TEST

A. THE "CLOCK LOGIC TEST" IS DESIGNED TO TEST INDIVIDUAL BITS IN THE CONTROL AND STATUS REGISTERS, COUNT PRESET BUFFER AND COUNTER ALONG WITH PROPER OPERATION UNDER INTERRUPT CONTROL MODE CONTROL

B. STARTING SEQUENCE

1. TYPE 'A' TO RUN THE CLOCK LOGIC TEST.
2. THE PROGRAM WILL THEN EXECUTE THE CLOCK LOGIC TEST.

C. CONTROL SWITCHES

1. TYPING 'C' AT ANY TIME WILL ENABLE THE PROGRAM TO EXIT 'CLOCK LOGIC' TEST AND RETURN TO THE MONITOR.

2. CONTROL SWITCH FUNCTIONS

CONSOLE SW11=0	NORMAL RUN (2048 PASSES TEST)
CONSOLE SW11=1	SUPPRESS SUBPROGRAM INTERACTIONS
CONSOLE SW13=0	PRINT ERROR MESSAGE
CONSOLE SW13=1	INHIBIT ERROR MESSAGE
CONSOLE SW14=0	INHIBIT SCOPE MODE
CONSOLE SW14=1	RUN SCOPE MODE
CONSOLE SW15=0	CONTINUE AFTER TYPING ERROR
CONSOLE SW15=1	HALT ON ERROR

D. ERRORS

ON ENCOUNTERING AN ERROR (DATA SWITCHES DOWN) THE ERROR ADDRESS AND THE CONTENTS OF THE CLOCK STATUS AND CLOCK PRESET BUFFER ARE TYPED OUT.

E. RESTRICTIONS

NO CONNECTIONS SHOULD BE MADE TO THE SCHMITT TRIGGER.

F. TEST TIME

IT TAKES APPROXIMATELY 60 SECONDS TO RUN THE CLOCK LOGIC TEST AND RING THE TELETYPE BELL.

7. DIGITAL INPUT-OUTPUT

A. THIS TEST IS DESIGNED TO TEST THE LPSDR (DIGITAL INPUT-OUTPUT) LOGIC FOR THIS TEST THE EXTERNAL JUMPER CABLE MUST BE INSTALLED TO TEST THE DATA INPUT/OUTPUT REGISTERS AND THE CONTROL SIGNALS. IF THIS EXTERNAL JUMPER CABLE IS NOT INSTALLED, ONLY A MINIMAL LOGIC TEST CAN BE PERFORMED.

B. STARTING SEQUENCE

1. TYPE 'B' TO RUN THE 'DIGITAL I/O LOGIC' TEST.
2. THE PROGRAM WILL THEN EXECUTE THE DIGITAL I/O LOGIC TEST.

C. CONTROL SWITCHES

1. TYPING 'C' WILL CAUSE THE PROGRAM TO EXIT THE 'DIGITAL I/O LOGIC' TEST AND RETURN TO THE MONITOR.

2. CONSOLE SWITCH FUNCTION

CONSOLE SW06=0*	EXTERNAL JUMPER CABLE CONNECTED
CONSOLE SW06=1*	EXTERNAL JUMPER CABLE NOT CONNECTED
	*= ACTIVATE SWITCH BEFORE SELECTING TEST
CONSOLE SW11=0	NORMAL RUN
CONSOLE SW11=1	SUPPRESS SUBPROGRAM INTERACTIONS
CONSOLE SW13=0	PRINT ERROR MESSAGES
CONSOLE SW13=1	INHIBIT ERROR MESSAGES
CONSOLE SW14=0	INHIBIT SCOPE MODE
CONSOLE SW14=1	SCOPE MODE
CONSOLE SW15=0	CONTINUE AFTER TYPING ERROR
CONSOLE SW15=1	HALT ON ERROR

D. LOGIC ERRORS

ON ENCOUNTERING AN ERROR (DATA SWITCHES DOWN) THE ERROR ADDRESS AND THE CONTENTS OF THE DIGITAL I/O STATUS, OUTPUT AND INPUT REGISTERS ARE TYPED OUT.

E. RESTRICTIONS

NONE

F. TEST TIME

IT TAKES APPROXIMATELY 30 SECONDS TO RUN THE DIGITAL I/O LOGIC TEST AND RING THE TELETYPE BELL.

B. POINT PLOT SCOPE LOGIC TEST

A. THIS TEST IS DESIGNED TO TEST THE LPSVC SCOPE CONTROL LOGIC
ALL USABLE BITS OF THE STATUS REGISTER ARE TESTED.

B. STARTING SEQUENCE

1. TYPE 'C' TO RUN THE SCOPE LOGIC TEST.
2. THE PROGRAM WILL THEN EXECUTE THE SCOPE LOGIC TEST.

C. CONTROL SWITCHES

1. TYPEING 'C' AT ANY TIME WILL ENABLE THE PROGRAM TO EXIT
AND RETURN TO THE MONITOR.

2. CONSOLE SWITCHES FUNCTION

CONSOLE SW05=0*	611/613 NOT CONNECTED
CONSOLE SW05=1*	611/613 CONNECTED
	*= ACTIVATE SWITCH BEFORE SELECTING TEST

D. LOGIC ERRORS

ON ENCOUNTERING AN ERROR (DATA SWITCHES DOWN) THE ERROR ADDRESS
AND THE CONTENTS OF THE VC STATUS, X AXIS AND Y AXIS
REGISTERS ARE TYPED OUT ON THE TELETYPE

E. RESTRICTIONS

IF 611/613 STORAGE SCOPE IS CONNECTED, IT MUST HAVE POWER ON.

F. TEST TIME

IT TAKES APPROXIMATELY 10 SECONDS TO RUN THE SCOPE LOGIC TEST.

9. POINT PLOT VISUAL DISPLAY TEST

A. THIS TEST IS DESIGNED TO AID IN THE ADJUSTING AND ALIGNMENT OF THE VR14/20 OR 611/613 SCOPE ON THE LPSVC DISPLAY CONTROL.

B. STARTING SEQUENCE

1. TYPE 'D' TO RUN THE VISUAL DISPLAY TEST.
2. THE PROGRAM WILL THEN EXECUTE THE VISUAL DISPLAY TEST.

C. CONTROL SWITCHES

1. TYPING 'C' AT ANY TIME WILL ENABLE THE PROGRAM TO EXIT AND RETURN TO THE MONITOR.

CONSOLE SWITCHES -----	FUNCTION -----
CONSOLE SW08=0	LOOP THRU DISPLAY TEST
CONSOLE SW08=1	SELECT TEST IN SW 00-02
CONSOLE SW04=0*	PLOT CHARACTERS IN FAST INTENSIFY MODE (VR14/20)
CONSOLE SW04=1*	PLOT CHARACTERS IN NORMAL INTENSIFY MODE (611/613)
	*= ACTIVATE SWITCH BEFORE SELECTING TEST
CONSOLE SW00-02=0	DISPLAY A HORIZONTAL LINE
CONSOLE SW00-02=1	DISPLAY A VERTICAL LINE
CONSOLE SW00-02=2	DISPLAY A SQUARE
CONSOLE SW00-02=3	DISPLAY A "X"
CONSOLE SW00-02=4	DISPLAY CHARACTER SET
CONSOLE SW00-02=5	DISPLAY CHANNEL TEST <VR14/VR20>
CONSOLE SW00-02=6	DISPLAY COLOR PATTERN <VR20>
CONSOLE SW00-02=7	DISPLAY ERASE AND PHOSPOR <611/613>

D. ERRORS

NO PROVISIONS ARE MADE FOR LOGIC ERRORS. THE ONLY ERRORS IN THIS TEST ARE CHECKED VISUALLY.

E. RESTRICTIONS

IF VR14/VR20, CHANNEL SWITCH MUST BE SET TO "1 & 2" POSITION.
 IF VR20, COLOR SWITCH MUST BE SET IN THE REMOTE POSITION.
 IF 611/613, POWER MUST BE APPLIED.

F. EXECUTION TIME

IT TAKES APPROXIMATELY 90 SECONDS TO THIS TEST.

10. VISUAL DISPLAY TEST DESCRIPTIONS

DISPLAY HORIZONTAL LINE

A HORIZONTAL LINE IS DISPLAYED ON THE SCOPE BY INITIALLY SETTING THE X AND Y DAC'S TO ZERO AND THEN INCREMENTING THE X VALUE WHILE HOLDING THE Y VALUE AT ZERO. THE POINTS ARE DISPLAYED USING THE DISPLAY INTERRUPT ENABLED.

DISPLAY VERTICAL LINE

A VERTICAL LINE IS DISPLAYED ON THE SCOPE IN THE SAME MANNER AS FOR A HORIZONTAL LINE EXCEPT NOW THE Y VALUE IS INCREMENTED WHILE HOLDING THE X VALUE AT ZERO.

DISPLAY SQUARE

A SQUARE IS DISPLAYED BY INITIALLY SETTING THE X AND Y VALUES TO NEGATIVE FULL SCALE, THEN X IS INCREMENTED TO POSITIVE FULL SCALE (BOTTOM LINE) THEN Y IS INCREMENTED TO POSITIVE FULL SCALE (RIGHT LINE) THEN X IS DECREMENTED TO NEGATIVE FULL SCALE (TOP LINE) AND FINALLY Y IS DECREMENTED TO NEGATIVE FULL SCALE (LEFT LINE). MODE 01 (INTENSIFY ON LOADING X) AND MODE 10 (INTENSIFY ON LOADING Y) ARE USED.

DISPLAY X

AN X IS DISPLAYED BY INITIALLY SETTING THE X AND Y VALUES TO NEGATIVE FULL SCALE AND THEN INCREMENTING BOTH TO POSITIVE FULL SCALE (LOWER LEFT TO UPPER RIGHT DIAGONAL) THEN X IS RESET TO NEGATIVE FULL SCALE, Y REMAINS AT POSITIVE FULL SCALE AND THEN X IS INCREMENTED WHILE Y IS DECREMENTED UNTIL BOTH REACH FULL SCALE AGAIN (UPPER LEFT TO LOWER RIGHT DIAGONAL). MODE 01 (INTENSIFY ON LOADING X) IS USED.

DISPLAY ALPHA-NUMERIC CHARACTER SET

THE ALPHABET AND NUMBERS 1 THRU 0 ARE DISPLAYED.

DISPLAY CHANNEL 1 AND CHANNEL 2

THE TEXT "CHANNEL 1" IS DISPLAYED ON CHANNEL 1 SWITCH POSITION. THE TEXT "CHANNEL 2" IS DISPLAYED ON CHANNEL 2 SWITCH POSITION. THE COMBINED MESSAGE WILL APPEAR IF THE CHANNEL SELECTOR SWITCH IS IN THE 1 & 2 POSITION.

DISPLAY COLOR PATTERN

THIS ROUTINE WILL DISPLAY A BOX AROUND THE OUTER DEGE OF THE SCREEN AND A SMALL "X" IS DISPLAYED IN THE CENTER. THIS PATTERN IS PLOTTED IN GREEN AND THEN IN RED. THE END RESULT IS THAT ALL DOTS (RED AND GREEN) CONVERGE AND THE PATTERN WILL APPEAR TO BE ORANGE IN COLOR. THIS TEST IS USED TO ADJUST THE COMPENSATION GAIN AMPLIFIER IN THE VR20 DISPLAY.

PHOSPHOR AND ERASE TEST

THIS ROUTINE WILL FIRST ERASE THE 611/613 SCREEN AND THEN START INT THE UPPER RIGHT CORNOR AND FILL THE SCREEN DOWNWARD. THIS TEST

11. ADDITIONAL STARTING ADDRESSES

INCLUDED IN THIS PROGRAM ARE SEVERAL 'MINI' TEST TO AID IN THE CHECKING OF THE UNIQUE NON-PROGRAMABLE HARDWARE TO THE LPS-11 OPTION BOX.

SA	TEST DESCRIPTION
---	-----
204	MANUAL SA OF THE CLOCK LOGIC TEST
210	MANUAL SA OF THE DIGITAL I/O LOGIC TEST
214	MANUAL SA OF THE SCOPE LOGIC TEST
220	MANUAL SA OF THE VISUAL SCOPE TEST
224	MINI-TEST OF SCHMITT TRIGGER #1
230	MINI-TEST OF SCHMITT TRIGGER #2
234	MINI-TEST OF CLOCK OVERFLOW
240	MINI-TEST OF RELAYS

12. OPERATOR VARIABLE LOCATIONS

LOCATION 1000 CONTAINS THE LPS STARTING DEVICE ADRESS
LOCATION 1002 CONTAINS THE LPS STARTING DEVICE VECTOR
LOCATION 1004 CONTAINS THE LPS A TO D BR LEVEL
LOCATION 1006 CONTAINS THE LPS CLOCK BR LEVEL
LOCATION 1010 CONTAINS THE LPS DIGITAL I/O BR LEVEL
LOCATION 1012 CONTAINS THE LPS DISPLAY BR LEVEL
LOCATION 1014 CONTAINS THE DELAY CONSTANT FOR MEMORY AND/OR CPU SPEED
(1 IF AN 11/20, 2 IF AN 11/45 ETC.)
LOCATION 1016 CONTAINS THE TTY FILLER COUNT
LOCATION 1020 CONTAINS THE TTY FILLER CHARACTER
LOCATION 170 CONTAINS THE SOFTWARE SWITCH REGISTER VALUE
LOCATION 172 CONTAINS THE SOFTWARE DISPLAY REGISTER VALUE

13. MISC. INFORMATION

IF THE PROGRAM WAS LOADED BY ACT-11 OR DDP, THE CLOCK LOGIC, SCOPE LOGIC AND SCOPE VISUAL WILL BE RUN.
THIS PROGRAM DOES NOT SUPPORT THE "APT" HOOKS.

14. MINI-TEST DESCRIPTIONS

SCHMITT TRIGGER #1

THE PURPOSE OF THIS MINI-TEST IS TO QUICK VERIFY THE OPERATION OF SCHMITT TRIGGER #1 ON THE CLOCK LOGIC MODULE. THIS IS DONE BY THE OPERATOR ROTATING THE THRESHOLD KNOB FROM END TO END OR CHANGING THE SLOPE SWITCH BETWEEN + OR -. THE PROGRAM WILL RING THE TTY BELL AND UPDATE THE NUMBER IN THE LPS DISPLAY LEDS UPON EACH SCHMITT TRIGGER #1 FLAG. ROTATING SCHMITT TRIGGER #2 THRESHOLD KNOB OR SWITCH SHOULD NOT CAUSE SCHMITT TRIGGER #1 TO FIRE.

SCHMITT TRIGGER #2

THE PURPOSE OF THIS MINI-TEST IS TO QUICK VERIFY THE OPERATION OF SCHMITT TRIGGER #2 ON THE CLOCK LOGIC MODULE. THIS IS DONE BY THE OPERATOR ROTATING THE THRESHOLD KNOB FROM END TO END OR CHANGING THE SLOPE SWITCH BETWEEN + OR -. THE PROGRAM WILL RING THE TTY BELL AND UPDATE THE NUMBER IN THE LPS DISPLAY LEDS UPON EACH SCHMITT TRIGGER #2 FLAG. ROTATING SCHMITT TRIGGER #1 THRESHOLD KNOB OR SWITCH SHOULD NOT CAUSE SCHMITT TRIGGER #2 TO FIRE.

CLOCK OVERFLOW

THE PURPOSE OF THIS MINI-TEST IS TO VERIFY THE OUTPUT OF THE CLOCK OVERFLOW LOGIC TO THE FRONT PANNEL. THE CLOCK IS ENABLED TO RUN AND OVERFLOW AT A FAST RATE.
THE OUTPUT MUST BE VERIFIED WITH THE USE OF AN OSCILLOSCOPE.

RELAY TEST

THE PURPOSE OF THIS MINI-TEST, IS TO ALLOW THE OPERATOR TO VERIFY THE PROPER OPERATION OF BOTH RELAYS. THIS IS ACCOMPLISHED BY SWITCHING THE RELAYS AT A SLOW RATE TO ALLOW THE OPERATOR TO CHECK THE CONTINUITY OF THE RELAY CONTACTS.

15. SOFTWARE SWITCH REGISTER OPERATION

THE PROGRAM SUPPORTS NON-SWITCH REGISTER CPU TYPES. THIS IS ACCOMPLISHED BY TYPING A "CTRL G". THE RESPONSE WILL REPORT THE OLD VALUE AND WAIT FOR A NEW VALUE. THE OPERATOR NOW INPUTS THE NEW VALUE AND TERMINATES IT WITH A "CR". IF THE OPERATOR TYPES A "CR" WITH NO INPUT, THE SOFTWARE SWITCH REGISTER IS SET TO 0. UPON TERMINAING, THE PROGRAM WILL RESUME THE APPROPATE TEST.

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.TITLE LPS DIAGNOSTIC TEST II MAINDEC-11-DZLPD-C
.ENABL ABS,AMA
.LIST ME
.NLIST MC,MD,CND

100000
040000
020000
010000
004000
002000
001000
000400
000200
000100
000040
000020
000010
000004
000002
000001

BIT15=100000
BIT14=40000
BIT13=20000
BIT12=10000
BIT11=4000
BIT10=2000
BIT9=1000
BIT8=400
BIT7=200
BIT6=100
BIT5=40
BIT4=20
BIT3=10
BIT2=4
BIT1=2
BIT0=1

;SWITCH REGISTER DEFINITIONS AND FUNCTIONS:

100000
040000
020000
010000
004000
002000
001000
000400
000200
000100
000040
000020
000010
000004
000002
000001

SW15=100000
SW14=40000
SW13=20000
SW12=10000
SW11=4000
SW10=2000
SW09=1000
SW08=400
SW07=200
SW06=100
SW05=40
SW04=20
SW03=10
SW02=4
SW01=2
SW00=1

=1, HALT ON ERROR
=1, LOOP ON CURRENT TEST
=1, SUPPRESS ERROR TYPEOUT

=1, SUPPRESS 'SUBPROGRAM' ITERATIONS
=1, FORCE TYPEOUT (REPEATIBILITY)

;LPSVC SELECT TEST IN SR 0-2

=1, LPSDR JUMPER NOT CONNECTED
:
:
:
;LPSVC VISUAL PATTERN
;LPSVC VISUAL PATTERN
;LPSVC VISUAL PATTERN

;REGISTER DEFINITIONS

000000
000001
000002
000003
000004
000005
000006
000007

R0=%0
R1=%1
R2=%2
R3=%3
R4=%4
R5=%5
SP=%6
PC=%7

```

506
507
508 000024 012352
509 000026 000340
510
511 000060 011734
512 000062 000340
513
514 000030 012452
515 000032 000340
516 000034 013016
517 000036 000340
518
519 000046 002012
520
521 000052 000052
522
523 000170 000000
524 000172 000000
525 000174 000137 001352
526 000200 000137 001120
527 000204 000137 002054
528 000210 000137 006014
529 000214 000137 010034
530 000220 000137 014534
531 000224 000137 017414
532 000230 000137 017430
533 000234 000137 017364
534 000240 000137 017300
535
536 104400
537 104000
538 104001
539 104002
540 104003
541 104004
542 104005
543 104006
544 104007
545
546 001000
547 001000 170400
548 001002 000340
549 001004 000300
550 001006 000300
551 001010 000200
552 001012 000200
553 001014 000001
554 001016 000002
555 001020 000000
556 001022 177776
557 001024 177560
558 001026 177562
559 001030 177564
560 001032 177566
561 001034 177570

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:LOAD TRAP CATCHER INTO LOC'S 0-1000

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      . =24
      PWRFAL           ;POWER FAIL HANDLER
      340
      . =60
      XTTYIN          ;TELEPRINTER KEYBOARD ROUTINE
      340
      . =30
      EMTSRV          ;EMT TRAP, EMT DISPATCH SERVICE
      340
      LOGERR          ;TRAP TRAP, LOGIC ERROR TRAP
      340
      . =46
      LOGICAL
      . =52
      0
      . =170
SOFTSW: 0           ;SOFTWARE SWITCH REGISTER VALUE
SOFTDI: 0
      JMP MONITR     ;PROGRAM 'RESTART' ADDRESS
      JMP INIT       ;INITIALIZATION ADDRESS
      JMP CKTEST     ;MANUAL SA OF CLOCK TEST
      JMP IOTEST     ;MANUAL SA OF DIGITAL I/O LOGIC TEST
      JMP VCTEST     ;MANUAL SA OF SCOPE LOGIC TEST
      JMP VISUAL     ;MANUAL SA OF SCOPE VISUAL TEST
      JMP ST1        ;MINI-TEST SCHMITT TRIGGER #1
      JMP ST2        ;MINI-TEST SCHMITT TRIGGER #2
      JMP CKOVFL     ;MINI-TEST CLOCK OVERFLOW
      JMP RELAY      ;MINI-TEST RELAY CONTACT

```

:TRAP EQUIVALENCE TABLE:

```

ERROR=TRAP           ;LOGIC TEST ERROR ROUTINE
PRINT=EMT            ;MESSAGE PRINTER ROUTINE
SCOPE0=EMT+1        ;SCOPE SUBROUTINE (1)
SCOPE=EMT+2         ;LOGIC TEST SCOPE SUBROUTINE (4000)
SCOPE1=EMT+3        ;LOGIC TEST SCOPE SUBROUTINE (10)
SPACE=EMT+4         ;TYPE 'N' SPACES
PRTOCT=EMT+5        ;OCTAL PRINT ROUTINE
TTYIN=EMT+6         ;TELETYPE INPUT ROUTINE
TSTTKS=EMT+7        ;SUBROUTINE TO TEST FOR KEYBOARD FLAG

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      . =1000
LPSADD: 170400       ;LPS STARTING ADDRESS
LPSVCT: 340          ;LPS STARTING VECTOR
ADBRL: 300           ;A TO D BR LEVEL
CKBRL: 300           ;CLOCK BR LEVEL
DIOBRL: 200          ;DIGITAL I/O BR LEVEL
VCBRL: 200           ;SCOPE BR LEVEL
PDPDLY: 1            ;1 FOR 11/20 2 FOR 11/45
FILLS: 2             ;TTY FILLER COUNT
FILCHR: 0            ;TTY FILLER CHARACTER
PSW: 177776
TKS: 177560
TKB: 177562
TPS: 177564
TPB: 177566
SWR: 177570         ;OR LOC. 170 IF RUNNING WITH NO SWITCH REGISTER

```

562	001036	177570	DISPLA:	177570	
563	001040	000000	PASSCT:	0	
564	001042	004000	ICCOUNT:	4000	
565					
566					
567					
568	001044	170400	ADCS:	170400	;A TO D STATUS/CONTROL REGISTER
569	001046	170402	ADDBR:	170402	;A TO D CONVERTED VALUE <READ ONLY>
570					;A TO D LED DISPLAY LIGHTS <WRITE ONLY>
571					
572	001050	170404	CSR:	170404	;CLOCK STATUS/CONTROL REGISTER
573	001052	170406	CSB:	170406	;CLOCK PRESET BUFFER
574					
575	001054	170410	GRSTAT:	170410	;DIGITAL I/O STATUS/COMMAND REGISTER
576	001056	170412	GRDAI:	170412	;DIGITAL I/O INPUT REGISTER <READ ONLY>
577	001060	170414	GRDIO:	170414	;DIGITAL I/O OUTPUT REGISTER
578					
579	001062	170416	VCSTAT:	170416	;POINT PLOT STATUS REGISTER
580	001064	170420	VCXREG:	170420	;POINT PLOT X AXIS
581	001066	170422	VCYREG:	170422	;POINT PLOT Y AXIS
582	001070	170424	VCEXT:	170424	;EXTERNAL DAC REGISTER
583					
584	001072	170415	GRBHC:	170415	;DIGITAL I/O OUTPUT REGISTER <HIGH BYTE>
585					
586					
587					
588	001074	000340	ADINT:	340	;A TO D INTERRUPT VECTOR
589	001076	000342	ADINT1:	342	
590					
591	001100	000344	CKV:	344	;CLOCK INTERRUPT VECTOR
592	001102	000346	CKVS:	346	
593					
594	001104	000350	GRIVA:	350	;DIGITAL INPUT INTERRUPT VECTOR
595	001106	000352	GRIVSA:	352	
596					
597	001110	000354	GRIVB:	354	;DIGITAL OUTPUT INTERRUPT VECTOR
598	001112	000356	GRIVSB:	356	
599					
600	001114	000360	VCIV:	360	;DISPLAY INTERRUPT VECTOR
601	001116	000362	VCIVS:	362	
602					

```

603                                     :THIS ROUTINE IS EXECUTED ON LOADING THE PROGRAM
604
605 001120 013706 014444 INIT:  MOV  STACK,SP          ;INIT STACK POINTER=1000
606 001124 012777 000340 177670  MOV  #340,SPSW
607 001132 000005 RESET          ;CLEAR THE WORLD
608 001134 012700 001044  MOV  #ADCS,RO
609 001140 013701 001000  MOV  LPSADD,R1
610 001144 012702 000013  MOV  #13,R2
611 001150 010120 INIT1A: MOV  R1,(0)+
612 001152 062701 000002  ADD  #2,R1
613 001156 005302  DEC  R2
614 001150 001373  BNE  INIT1A
615 001152 013737 001060 001072  MOV  GRDIO,GRBHIO
616 001170 052737 000001 001072  BIS  #1,GRBHIO
617 001176 012700 001074  MOV  #ADINT,RO
618 001202 013701 001002  MOV  LPSVCT,R1
619 001206 012702 000012  MOV  #12,R2
620 001212 010120 INIT1B: MOV  R1,(0)+
621 001214 062701 000002  ADD  #2,R1
622 001220 005302  DEC  R2
623 001222 001373  BNE  INIT1B
624 001224 012737 001240 000004  MOV  #15,SWR          ;LOAD TRAP RETURN
625 001232 005777 177576  TST  SWR             ;TEST IF SWITCH REGISTER
626 001236 000407  BR   2$             ;BR IF YES
627 001240 022626 1$:  CMP  (SP)+,(SP)+
628 001242 012737 000170 001034  MOV  #170,SWR        ;LOAD LOC. 170 INTO ADDRESS
629 001250 012737 000172 001036  MOV  #172,DISPLA
630 001256 005037 013642 2$:  CLR  NOLEDS
631 001262 012737 001342 000004  MOV  #INITIC,SWR
632 001270 005077 177552  CLR  ADCBR
633 001274 000240  NOP
634 001276 012737 000006 000004  MOV  #6,SWR
635 001304 005737 000042  TST  SWR
636 001310 001402  BEG  3$
637 001312 000137 001400  JMP  INIT2
638 001316 012777 000100 177500 3$:  MOV  #100,ATKS
639 001324 005037 014442  CLR  PRINT1
640 001330 104000  PRINT          ;CALL MESSAGE PRINTER VIA 'EMT'
641 001332 013644  TITLE        ;TYPE PROGRAM HEADER.
642 001334 104000  INITA:  PRINT
643 001336 014165  MES4          ;PRINT THE TEST CALL LETTERS.
644 001340 000417  BR   INIT2        ;GO AND AWAIT COMMAND.
645 001342 012737 177777 013642  INIT1C: MOV  #-1,NOLEDS
646 001350 000002  RTI
647  MONITR: MONITOR SUBROUTINE. ENTER VIA 'IC' OR A RESTART AT LOCATION '200'.
648 001352 000005  RESET          ;INITIALIZE ON ENTRY
649 001354 013706 014444  MOV  STACK,SP        ;RESET STACK POINTER
650 001360 012777 000340 177434  MOV  #340,SPSW
651 001356 012777 000100 177430  MOV  #100,ATKS
652  PRINT          ;ENABLE TTY INTERRUPTS
653  CNTRLC         ;CALL MESSAGE PRINTER
654  ;TYPE 'IC'

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000024 INIT2: MOV @PWRFAL, @2024 ;SET UP POWER FAIL
000024 MOV @6, @204 ;SET UP BUSS ERROR
000024 CLR @206
177446 MOV @ADINT!, @ACINT
000024 CLR @ADINT!
177440 MOV @CKVS, @CKV
000024 CLR @CKV$
177432 MOV @GRIVSA, @GRIVA
000024 CLR @GRIVSA
177424 MOV @GRIVSB, @GRIVB
000024 CLR @GRIVSB
000024 CLR @SCOPE$
000024 MOV @INITA, @VECTR ;SET UP 'A' VECTOR ADDRESS.
000024 SR @R5, @LED$
000042 TST @2042
001632 BEO .+6
000100 JMP @WHAT ;ENABLE KEYBOARD INTERRUPT
000024 PRINT @100, @TKS ;PRINT ' ' TO INDICATE MONITOR READY
000024 OUT ;WAIT FOR TTY ENTRY
000040 TTYIN ;ENABLE LOWER CASE
000101 BIC @BITS, @INSUF ;TEST FOR 'A'
000101 CMPB @'A', @INSUF ;TEST FOR 'A'
000101 BNE .+6
002054 JMP @CKTEST ;YES RUN 'CLOCK LOGIC TEST'
000102 CMPB @'B', @INSUF ;TEST FOR 'B'
000102 BNE .+6 ;NOT 'B'
000102 JMP @IOTEST ;YES RUN 'I/O LOGIC TEST'
000103 CMPB @'C', @INSUF ;TEST FOR 'C'
000103 BNE .+6 ;NOT 'C'
000137 JMP @VCTEST ;YES RUN 'SCOPE LOGIC TEST'
000104 CMPB @'D', @INSUF ;TEST FOR 'D'
000104 BNE .+6 ;NOT 'D'
014534 JMP @VISUAL ;YES RUN 'VISUAL DISPLAY TEST'
INIT3: PRINT ;ILLEGAL ENTRY
@MARK ;TYPE ' '
BR INIT2 ;WAIT AGAIN

```

: CLOCK LOGIC TEST
:*****

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73:59
74:00

002054 000005
002056 104000
002058 014030
002060 005030
002062 001040
002064 013777 001040 176742
002066 013777 014444
002068 012706 176716
002070 005077
002072 012706 002132 013414
002074 052777 000100 176724
002120 005077 176724
002122 005077 176722
002130 104002
002132 012777 177777 176712
002134 022777 177777 176704
002140 001401
002142 104400
002144 104400
002146 001401
002148 104400
002150 104400
002152 104002
002154 012777 052525 176670
002156 022777 052525 176662
002158 001401
002160 104400
002162 104400
002164 104400
002166 104400
002168 104400
002170 104400
002172 104400
002174 104002
002176 012777 025252 176646
002178 022777 025252 176640
002180 001401
002182 104400
002184 104400
002216 104003
002220 012777 177777 176624
002222 000005
002224 005777 176616
002226 001401
002228 104400
002230 104400
002232 104400
002234 104400
002236 104400
002240 052777 000100 176556

CKTEST: RESET
PRINT
RES2 :IDENTIFY TEST
CTEST1: CLR PASSCT
BEGIN: MOV PASSCT,DISPLA
MOV STACK,SP
CLR @PSW
MOV @KWT0+2,RETURN :SET UP RESTART OF PROGRAM
BIS @BIT6,@TKS
:TEST FOR NO BUSS ERRORS
CLR @CSR
CLR @CSB
:TEST THE COUNTER PRESET BUFFER
KWT0: SCOPE
MOV @-1,@CSB :LOAD PRESET BUFFER
CMP @-1,@CSB
BEQ .+4 :BRANCH IF EQUAL
ERROR :ERROR, COUNTER PRESET FAILED TO LOAD
KWT2: SCOPE
MOV @52525,@CSB :LOAD PRESET BUFFER
CMP @52525,@CSB
BEQ .+4 :BRANCH IF EQUAL
ERROR :ERROR, COUNTER PRESET FAILED TO LOAD
KWT3: SCOPE
MOV @25252,@CSB :LOAD PRESET
CMP @25252,@CSB
BEQ .+4 :BRANCH IF EQUAL
ERROR :ERROR, COUNTER PRESET FAILED TO LOAD
:TEST INIT TO CLEAR COUNT PRESET BUFFER WHEN IT IS =-!
KWT4: SCOPE1
MOV @-1,@CSB
RESET
TST @CSB
BEQ .+4
ERROR :ERROR, INIT FAILED TO CLEAR CSB
BIS @BIT6,@TKS

002356
002360
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002374
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002446
002454
002462
002464
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104002
012777 000100 176462
022777 000100 176454
001401
104400

;TEST MODE INTERRUPT ENABLE (BIT 6) CAN BE SET AND CLEARED

KWT10: SCOPE
MOV #100,0CSR
CMP #100,0CSR
BEQ .+4
ERROR ;ERROR, CSR NOT = 100

;TEST MODE (BIT 8) CAN BE SET AND CLEARED

104002
012777 000400 176440
022777 000400 176432
001401
104400

KWT11: SCOPE
MOV #400,0CSR
CMP #400,0CSR
BEQ .+4
ERROR ;ERROR, CSR NOT = 400

;TEST MODE (BIT 9) CAN BE SET AND CLEARED

104002
012777 001000 176416
022777 001000 176410
001401
104400

KWT12: SCOPE
MOV #1000,0CSR
CMP #1000,0CSR
BEQ .+4
ERROR ;ERROR, CSR NOT = 1000

;TEST ST#1 START ENABLE (BIT 13) CAN BE SET AND CLEARED

104002
012777 020000 176374
022777 020000 176366
001401
104400

KWT14: SCOPE
MOV #20000,0CSR
CMP #20000,0CSR
BEQ .+4
ERROR ;ERROR, CSR NOT = 200000

```

859
860 ;TEST ST#1 INTERRUPT ENABLE (BIT 14) CAN BE SET AND CLEARED
861
862 002466 104002 KWT15: SCOPE
863 002470 012777 040000 176352 MOV #40000,@CSR
864 002476 022777 040000 176344 CMP #40000,@CSR
865 002504 001401 BEQ .+4
866 002506 104400 ERROR ;ERROR, CSR NOT = 40000
867
868 ;TEST THAT THE DONE (BIT 7) CAN BE SET AND CLEARED
869
870 002510 104002 KWT16: SCOPE
871 002512 012777 000200 176330 MOV #BIT7,@CSR ;SET THE DONE BIT
872 002520 105777 176324 TSTB @CSR
873 002524 100401 BMI .+4
874 002526 104400 ERROR ;ERROR, CSR NOT = 200
875 002530 105777 176314 TSTB @CSR
876 002534 100401 BMI .+4
877 002536 104400 ERROR ;ERROR CSR NOT = 200
878 002540 005077 176304 CLR @CSR
879 002544 005777 176300 TST @CSR
880 002550 001401 BEQ .+4
881 002552 104400 ERROR ;ERROR CSR NOT = 0
882
883 ;TEST THAT THE ST FLAG (BIT 15) CAN BE SET AND CLEARED
884
885 002554 104002 KWT17: SCOPE
886 002556 012777 100000 176264 MOV #BIT15,@CSR ;SET BIT 15
887 002564 005777 176260 TST @CSR
888 002570 100401 BMI .+4
889 002572 104400 ERROR ;ERROR CSR NOT 100000
890 002574 005777 176250 TST @CSR
891 002600 100401 BMI .+4
892 002602 104400 ERROR ;ERROR CSR NOT 100000
893 002604 005077 176240 CLR @CSR
894 002610 005777 176234 TST @CSR
895 002614 001401 BEQ .+4
896 002616 104400 ERROR ;ERROR CSR NOT = 0
897
898 ;TEST THAT THE ST FLAG DOES NOT SET FROM THE OUTSIDE SOURCE
899
900 002620 104002 KWT18: SCOPE
901 002622 005077 176222 CLR @CSR
902 002626 005037 014506 CLR TEMP
903 002632 005777 176212 KWT18A: TST @CSR
904 002636 100001 BPL .+4
905 002640 104400 ERROR ;ERROR ST1 SET IN ERROR
906 002642 005237 014506 INC TEMP
907 002646 001371 BNE KWT18A

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002650	104003		
002652	005077	176172	
002656	052777	010000	176164
002664	005777	176160	
002670	100401		
002672	104400		
002674	104002		
002676	005077	176146	
002702	012777	020000	176140
002710	052777	010000	176132
002716	032777	000001	176124
002724	001001		
002726	104400		

:TEST MAINT ST1 CAN SET ST1 FLAG

KWT19: SCOPE1

```

CLR      @CSR
SIS      @BIT12,@CSR
TST      @CSR
SMI      .+4
ERROR

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:MAINT ST1

:ERROR, ST1 FLAG FAILED TO SET

:TEST THAT WHEN ST1 FIRES AND ST1 START ENABLE =!

: THAT THE ENABLE COUNTER GETS SET

KWT20: SCOPE

```

CLR      @CSR
MOV      @BIT13,@CSR
BIS      @BIT12,@CSR
BIT      @BIT0,@CSR
BNE      .+4
ERROR

```

:SET ST1 START ENABLE

:MAINT ST1

:TEST BIT 0

:ST1 START ENABLE AND ST1

:FAILED TO SET ENABLE COUNTER

```

931          ;TEST THAT MODE 1 AND BIT 10 (MAINT. ST 2) SET BIT 7
932
933 002730 104002          KWT22: SCOPE
934 002732 005077 176112 CLR          @CSR          ;CLEAR STATUS
935 002736 005077 176110 CLR          @CSB          ;CLEAR PRESET
936 002742 012777 001000 176100 MOV          #BIT9,@CSR      ;LOAD MODE
937 002750 052777 002000 176072 BIS          #BIT10,@CSR     ;FIRE ST 2
938 002756 105777 176066 TSTB        @CSR          ;TEST BIT 7
939 002762 100401          BMI          .+4
940 002764 104400          ERROR          ;ERROR, ST 2 FAILED TO SET BIT 7
941
942          ;TEST THAT THE COUNTER CAN BE LOADED
943
944 002766 104002          KWT23: SCOPE
945 002770 005077 176054 CLR          @CSR          ;CLEAR STATUS
946 002774 012777 177777 176050 MOV          #-1,@CSB       ;LOAD PRESET AND COUNTER
947 003002 012777 001401 176040 MOV          #1401,@CSR     ;LOAD MODE AND ENABLE COUNT
948 003010 005077 176036 CLR          @CSB          ;SHOULD ONLY CLEAR PRESET
949 003014 052777 002000 176026 BIS          #BIT10,@CSR     ;FIRE ST
950 003022 022777 177777 176022 CMP          #-1,@CSB       ;TEST THE NUMBER
951 003030 001401          BEQ          .+4
952 003032 104400          ERROR          ;ERROR, COUNTER FAILED TO LOAD PROPERLY
953
954          ;TEST THAT THE COUNTER CAN BE LOADED
955
956 003034 104002          KWT24: SCOPE
957 003036 005077 176006 CLR          @CSR          ;CLEAR STATUS
958 003042 012777 125252 176002 MOV          #125252,@CSB   ;LOAD PRESET AND COUNTER
959 003050 012777 001401 175772 MOV          #1401,@CSR     ;LOAD MODE AND ENABLE COUNT
960 003056 005077 175770 CLR          @CSB          ;SHOULD ONLY CLEAR PRESET
961 003062 052777 002000 175760 BIS          #BIT10,@CSR     ;FIRE ST
962 003070 022777 125252 175754 CMP          #125252,@CSB   ;TEST THE NUMBER
963 003076 001401          BEQ          .+4
964 003100 104400          ERROR          ;ERROR, COUNTER FAILED TO LOAD PROPERLY
965
966          ;TEST THAT THE COUNTER CAN BE LOADED
967
968 003102 104002          KWT25: SCOPE
969 003104 005077 175740 CLR          @CSR          ;CLEAR STATUS
970 003110 012777 052525 175734 MOV          #52525,@CSB    ;LOAD PRESET AND COUNTER
971 003116 012777 001401 175724 MOV          #1401,@CSR     ;LOAD MODE AND ENABLE COUNT
972 003124 005077 175722 CLR          @CSB          ;SHOULD ONLY CLEAR PRESET
973 003130 052777 002000 175712 BIS          #BIT10,@CSR     ;FIRE ST
974 003136 022777 052525 175706 CMP          #52525,@CSB    ;TEST THE NUMBER
975 003144 001401          BEQ          .+4
976 003146 104400          ERROR          ;ERROR, COUNTER FAILED TO LOAD PROPERLY
977

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1002
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: TEST THAT THE COUNTER COUNTS UP
: USE MAINT COUNT
: USE MAINT ST2
: USE MODE 2
: USE RATE 1 (1MHZ)

003150 005037 014506
003154 104002
003156 005077 175666
003162 005077 175664
003166 012777 001002 175654
003174 052777 002000 175646
003202 027737 175644 014506
003210 001402
003212 104400
003214 000416
003216 105777 175626
003222 100402
003224 104400
003226 000411
003230 052777 004000 175612
003236 042777 000200 175604
003244 005237 014506
003250 001351

CLR TEMP
KWT26: SCOPE
CLR @CSR
CLR @CSB
MOV #1002, @CSR
KWT26A: BIS #BIT10, @CSR
CMP @CSB, TEMP
BEQ .+6
ERROR
BR KWT30
TSTB @CSR
BMI IS
ERROR
BR KWT30
BIS #BIT11, @CSR
BIC #BIT7, @CSR
INC TEMP
BNE KWT26A

; MAINT ST2
; MAINT COUNT FAILED
; TEST DONE FLAG
; ERROR, CKBF TO BF FAILED TO SET DONE
; MAINT COUNT
; CLEAR BIT 7
; BRANCH IF NOT FULL COUNT

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1004
1005 ;TEST THAT THE COUNTER COUNTS UP
1006 ;MAKE SJRE THAT THE CLOCK SELECTION LOGIC WORKS
1007 ;USE MAINT COUNT <100KHZ>
1008 ;USE MAINT ST2
1009 ;USE MODE 2
1010 ;RATE #100KHZ
1011
1012 003252 104003 KWT30: SCOPE1
1013 003254 005077 175570 CLR @CSR ;CLEAR CLOCK STATUS
1014 003260 005077 175566 CLR @CSB ;CLEAR PRESET
1015 003254 012777 001004 175556 MOV #1004,@CSR ;LOAD STATUS
1016 003272 052777 002000 175550 BIS #BIT10,@CSR ;MAINT ST2
1017 003300 005777 175546 TST @CSB ;TEST PRESET
1018 003304 001401 BEQ .+4
1019 003306 104400 ERROR ;ERROR PRESET INCREMENTED IN ERROR
1020 003310 012737 000012 014454 MOV #10,COUNT ;SET UP A COUNTER
1021 003316 052777 004000 175524 KWT30A: BIS #BIT11,@CSR ;GENERATE MAINT COUNT
1022 003324 005337 014454 DEC COUNT
1023 003330 001372 BNE KWT30A ;BR
1024 003332 052777 002000 175510 BIS #BIT10,@CSR ;MAINT ST2
1025 003340 022777 000001 175504 CMP #1,@CSB ;
1026 003346 001401 BEQ .+4
1027 003350 104400 ERROR ;ERROR, CLOCK PRESET BUFFER
1028 ;COUNTED IN ERROR, FAULT IS PROBILY IN THE
1029 ;CLOCK DOWN COUNT OR RATE SELECTION LOGIC
1030

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1031 ;TEST THAT THE COUNTER COUNTS UP
1032 ;MAKE SURE THAT THE CLOCK SELECTION LOGIC WORKS
1033 ;USE MAINT COUNT <10KHZ>
1034 ;USE MAINT ST2
1035 ;USE MODE 2
1036 ;RATE #10KHZ
1037
1038 003352 104003 KWT31: SCOPE1
1039 003354 005077 175470 CLR @CSR ;CLEAR CLOCK STATUS
1040 003360 005077 175466 CLR @CSB ;CLEAR PRESET
1041 003364 012777 001006 175456 MOV #1006,@CSR ;LOAD STATUS
1042 003372 052777 002000 175450 BIS #BIT10,@CSR ;MAINT ST2
1043 003400 005777 175446 TST @CSB ;TEST PRESET
1044 003404 001401 BEQ .+4
1045 003406 104400 ERROR ;ERROR PRESET INCREMENTED IN ERROR
1046 003410 012737 000144 014454 MOV #100,COUNT ;SET UP A COUNTER
1047 003416 052777 004000 175424 KWT31A: BIS #BIT11,@CSR ;GENERATE MAINT COUNT
1048 003424 005337 014454 DEC COUNT
1049 003430 001372 BNE KWT31A ;BR
1050 003432 052777 002000 175410 BIS #BIT10,@CSR
1051 003440 022777 000001 175404 CMP #1,@CSB ;
1052 003446 001401 BEQ .+4
1053 003450 104400 ERROR ;ERROR, CLOCK PRESET BUFFER
1054 ;COUNTED IN ERROR, FAULT IS PROBILY IN THE
1055 ;CLOCK DOWN COUNT OR RATE SELECTION LOGIC
1056

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1057
1058
1059 :TEST THAT THE COUNTER COUNTS UP
1060 :MAKE SURE THAT THE CLOCK SELECTION LOGIC WORKS
1061 :USE MAINT COUNT <1KHZ>
1062 :USE MAINT ST2
1063 :USE MODE 2
1064 :RATE #1KHZ
1065 003452 104003 KWT32: SCOPE1
1066 003454 005077 175370 CLR @CSR ;CLEAR CLOCK STATUS
1067 003460 005077 175366 CLR @CSB ;CLEAR PRESET
1068 003464 012777 001010 175356 MOV #1010,@CSR ;LOAD STATUS
1069 003472 052777 002000 175350 BIS #BIT10,@CSR ;MAINT ST2
1070 003500 005777 175346 TST @CSB ;TEST PRESET
1071 003504 001401 BEQ .+4
1072 003506 104400 ERROR ;ERROR PRESET INCREMENTED IN ERROR
1073 003510 012737 001750 014454 MOV #1000.,COUNT ;SET UP A COUNTER
1074 003516 052777 004000 175324 KWT32A: BIS #BIT11,@CSR ;GENERATE MAINT COUNT
1075 003524 005337 014454 DEC COUNT
1076 003530 001372 BNE KWT32A ;BR
1077 003532 052777 002000 175310 BIS #BIT10,@CSR
1078 003540 022777 000001 175304 CMP #1,@CSB
1079 003546 001401 BEQ .+4
1080 003550 104400 ERROR ;ERROR, CLOCK PRESET BUFFER
1081 ;COUNTED IN ERROR, FAULT IS PROBILY IN THE
1082 ;CLOCK DOWN COUNT OR RATE SELECTION LOGIC
1083

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1084 :TEST THAT THE COUNTER COUNTS UP
1085 :MAKE SURE THAT THE CLOCK SELECTION LOGIC WORKS
1086 :USE MAINT COUNT <100HZ>
1087 :USE MAINT ST2
1088 :USE MODE 2
1089 :RATE #100HZ
1090
1091 003552 104003 KWT33: SCOPE1
1092 003554 005077 175270 CLR @CSR ;CLEAR CLOCK STATUS
1093 003560 005077 175266 CLR @CSB ;CLEAR PRESET
1094 003564 012777 001012 175256 MOV #1012,@CSR ;LOAD STATUS
1095 003572 052777 002000 175250 BIS #BIT10,@CSR ;MAINT ST2
1096 003600 005777 175246 TST @CSB ;TEST PRESET
1097 003604 001401 BEQ .+4
1098 003606 104400 ERROR ;ERROR PRESET INCREMENTED IN ERROR
1099 003610 012737 023420 014454 MOV #10000.,COUNT ;SET UP A COUNTER
1100 003616 052777 004000 175224 KWT33A: BIS #BIT11,@CSR ;GENERATE MAINT COUNT
1101 003624 005337 014454 DEC COUNT
1102 003630 001372 BNE KWT33A ;BR
1103 003632 052777 002000 175210 BIS #BIT10,@CSR
1104 003640 022777 000001 175204 CMP #1,@CSB
1105 003646 001401 BEQ .+4
1106 003650 104400 ERROR ;ERROR, CLOCK PRESET BUFFER
1107 ;COUNTED IN ERROR, FAULT IS PROBILY IN THE
1108 ;CLOCK DOWN COUNT OR RATE SELECTION LOGIC

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1109
1110 ;TEST THAT THE COUNTER COUNTS UP
1111 ;MAKE SURE THAT THE CLOCK SELECTION LOGIC WORKS
1112 ;USE MODE 2
1113 ;USE MAINT ST1
1114 ;RATE #EXTURNAL
1115
1116 003652 005037 014506          CLR      TEMP
1117 003656 104003          KWT34:  SCOPE1
1118 003660 005077 175164          CLR      @CSR
1119 003664 005077 175162          CLR      @CSB
1120 003670 012777 001014 175152  MOV      #1014,@CSR ;MODE 2 EXTERNAL CLOCK RATE
1121 003676 052777 002000 175144  KWT34A: BIS      #BIT10,@CSR ;MAINT ST 2
1122 003704 027737 175142 014506  CMP      @CSB,TEMP ;COMPARE BUFFER TO PRESET
1123 003712 001402          BEQ      .+6
1124 003714 104400          ERROR ;EXTERNAL CLOCDAILED TO COUNT
1125 003716 000406          BR      KWT35 ; THE COUNTER, CHECK THE RATE SELECTION
1126 003720 052777 010000 175122  BIS      #BIT12,@CSR ;MAINT ST1
1127 003726 005237 014506          INC      TEMP
1128 003732 001361          BNE      KWT34A
1129
1130 ;TEST EXTURNAL INTERVAL FROM ZERO BASE (MODE 3)
1131
1132 003734 104003          KWT35:  SCOPE1
1133 003736 005077 175106          CLR      @CSR
1134 003742 012777 025252 175102  MOV      #25252,@CSB
1135 003750 012777 001402 175072  MOV      #1402,@CSR
1136 003756 052777 002000 175064  BIS      #BIT10,@CSR
1137 003764 022777 025252 175060  CMP      #25252,@CSB
1138 003772 001401          BEQ      .+4
1139 003774 104400          ERROR ;ERROR, MODE 3 FAILED TO LOAD CLCCK
1140 ; PRESET BUFFER
1141 003776 052777 002000 175044  BIS      #BIT10,@CSR
1142 004004 022777 000000 175040  CMP      #0,@CSB
1143 004012 001401          BEQ      .+4
1144 004014 104400          ERROR ;ERROR, MODE 3 FAILED TO ZERO CLOCK COUNTER

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1145
1146 ;TEST THAT RESET CLEARS RATE SELECT BITS
1147
1148 004016 104002 KWT36: SCOPE1
1149 004020 012777 000016 175022 MOV #BIT3!BIT2!BIT1,@CSR ;SET MODE BITS
1150 004026 000005 RESET
1151 004030 005777 175014 TST @CSR
1152 004034 001401 BEQ .+4
1153 004036 104400 ERROR ;ERROR, RESET FAILED TO CLEAR RATE BITS
1154
1155 ;TEST THAT RESET CLEARS MODE SELECT BITS
1156
1157 004040 104003 KWT37: SCOPE1
1158 004042 012777 001400 175000 MOV #BIT9!BIT8,@CSR ;SET MODE BITS
1159 004050 000005 RESET
1160 004052 005777 174772 TST @CSR
1161 004056 001401 BEQ .+4
1162 004060 104400 ERROR ;ERROR, RESET FAILED TO CLEAR MODE BITS
1163
1164 ;TEST THAT RESET CLEARS ST1 FLAG,ST1 INTERRUPT ENABLE AND ST1 START ENABLE
1165
1166 004062 104003 KWT38: SCOPE1
1167 004064 012777 160000 174756 MOV #BIT15!BIT14!BIT13,@CSR ;SET ST1 FLAG,INT ENABLE AND ST1 START ENABLE
1168 004072 000005 RESET
1169 004074 005777 174750 TST @CSR
1170 004100 001401 BEQ .+4
1171 004102 104400 ERROR ;ERROR, RESET FAILED TO CLEAR ST1 LOGIC
1172
1173 ;TEST THAT RESET CLEARS DONE FLAG AND DONE INTERRUPT ENABLE
1174
1175 004104 104003 KWT39: SCOPE1
1176 004106 012777 000300 174734 MOV #BIT7!BIT6,@CSR ;SET DONE FLAG AND INTERRUPT ENABLE
1177 004114 000005 RESET
1178 004116 005777 174726 TST @CSR
1179 004122 001401 BEQ .+4
1180 004124 104400 ERROR ;ERROR, RESET FAILED TO CLEAR DONE FLAG OR DONE
1181
1182 ;TEST THAT RESET CLEARS COUNTER ENABLE
1183
1184 004126 104003 KWT40: SCOPE1
1185 004130 012777 000001 174712 MOV #BIT0,@CSR ;LOAD COUNTER ENABLE
1186 004136 000005 RESET
1187 004140 005777 174704 TST @CSR ;TEST STATUS
1188 004144 001401 BEQ .+4
1189 004146 104400 ERROR ;ERROR, RESET FAILED TO CLEAR COUNTER ENABLE
1190
1191
1192 004150 052777 000100 174646 BIS #BIT6,@TKS

```

:TEST CLOCK TO COUNT UP AT ALL FREQUENCIES (MODE 0)
:TEST THAT CLOCK ENABLE DOES CLEAR ON DONE FLAG
:1MHZ

000003 006004
004470
174652
000001 174640

KWT41: SCOPE1
MOV #3.RATE
JSR PC_UPCNT
TSTB 2CSR
BMI .+4
ERROR
BIT #BIT0.2CSR
BFE .+4
ERROR

:SELECT MODE 0, 1MHZ., GO
:ERROR, 1MHZ FAILED TO COUNT
:ERROR, MODE 0 FAILED TO CLEAR COUNTER ENABLE

:TEST CLOCK TO COUNT UP AT ALL FREQUENCIES
:100 KHZ

000005 006004
004470
174614
000001 174602

KWT42: SCOPE1
MOV #5.RATE
JSR PC_UPCNT
TSTB 2CSR
BMI .+4
ERROR
BIT #BIT0.2CSR
BFE .+4
ERROR

:SELECT MODE 0, 100KHZ., GO
:ERROR, 100KHZ. FAILED TO COUNT
:ERROR MODE 0 FAILED TO CLEAR COUNT ENABLE

:10 KHZ

000007 006004
004470
174556
000001 174544

KWT43: SCOPE1
MOV #7.RATE
JSR PC_UPCNT
TSTB 2CSR
BMI .+4
ERROR

:SELECT MODE 0, 10KHZ., GO
:ERROR, 10 KHZ. FAILED TO COUNT

:TEST CLOCK TO COUNT UP AT ALL FREQUENCIES
:1KHZ

000011 006004
004470
174532
000001 174520

KWT44: SCOPE1
MOV #11.RATE
JSR PC_UPCNT
TSTB 2CSR
BMI .+4
ERROR

:SELECT MODE 0, 1 KHZ. GO
:ERROR, 1KHZ FAILED TO COUNT

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1360

004630 :04003
004632 000005
004634 012777 000340 174160
004636 005077 174202
004638 012777 004712 174224
004640 012777 040000 174166
004642 012700 000010
004644 013777 014514 174126
004646 052777 010000 174146
004648 005300
004650 001376
004652 104400
004654 000415

000340 174160
174202
004712 174224
040000 174166
000010
014514 174126
010000 174146
005300
001376
104400
000415
004740 174156
000010
174070

:TEST THAT THE SCHMITT TRIGGER INTERRUPTS AT LEVEL INDICATED -1

```
KWTSO: SCOPE1  
RESET  
MOV #340, @PSW  
CLR @CSR  
MOV #KWTSOA, @CKV :SET UP INTERRUPT RETURN VECTOR  
MOV #BIT14, @CSR :ENABLE INTERRUPT  
MOV #10, R0  
MOV BRLEV1, @PSW :LOWER PRIOR.  
BIS #BIT12, @CSR  
DEC R0  
BNE .-2  
ERROR :ERROR, CLOCK INTERRUPT FAILED TO OCCUR.  
BR KWTS1 :CHECK FOR PROPER BR LEVEL  
:SHOULD BE LEVEL 6 (300)
```

:SUBTEST, TEST THAT IF PRIORITY IS LOWERED AGAIN
:NO INTERRUPT SHOULD OCCUR

```
KWTSOA: CMP (SP)+, (SP)+  
MOV #KWTSOB, @CKV :RESET THE VECTOR  
MOV #10, R0  
CLR @PSW  
DEC R0  
BNE .-2 :DELAY  
BR KWTS1  
KWTSOB: CMP (SP)+, (SP)+  
ERROR :ERROR, INT DONE B FAILED TO CLEAR INT REG B
```

:TEST THAT THE CLOCK INTERRUPTS AT LEVEL INDICATED -1 (MODE 0)

```

1350
1351
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1354 004744 104003
1355 004746 000005
1356 004750 012777 000340 174044
1357 004756 012777 005042 174114
1358 004764 012777 000340 174110
1359 004772 005077 174052
1360 004776 012777 177774 174046
1361 005004 012777 000102 174036
1362 005012 012700 000200
1363 005016 013777 014514 173776
1364 005024 052777 000001 174016
1365 005032 005300
1366 005034 001376
1367 005036 104400
1368 005040 000401
1369
1370 005042 022626
1371
1372
1373
1374 005044 104003
1375 005046 012777 000340 173746
1376 005054 005077 173770
1377 005060 013777 001102 174012
1378 005066 012777 000000 174006
1379 005074 012777 040000 173746
1380 005102 012700 000010
1381 005106 052777 010000 173734
1382 005114 005300
1383 005116 001376
1384 005120 012700 000100
1385 005124 000005
1386 005126 005077 173670
1387 005132 005300
1388 005134 001376

```

KWT51: SCOPE1

```

RESET
MOV #340, @PSW
MOV #KWT51A, @CKV ;LOAD VECTOR
MOV #340, @CKVS
CLR @CSR
MOV #-4, @CSB ;LOAD PRESET
MOV #BIT6!BIT1, @CSR ;LOAD RATE AND INT ENABLE
MOV #200, R0 ;SET UP DELAY
MOV BRLEV1, @PSW
BIS #BIT0, @CSR ;CLOCK
JEC R0
BNE #-2 ;DELAY
ERROR ;ERROR, CLOCK FAILED TO INTERRUPT
BR KWT52

```

KWT51A: CMP (SP)+, (SP)+

:TEST THAT RESET CLEARS INT REQ B

KWT52: SCOPE1

```

MOV #340, @PSW
CLR @CSR ;CLEAR STATUS
MOV @CKV, @CKV ;LOAD VECTOR
MOV #0, @CKVS
MOV #BIT14, @CSR ;LOAD INT ENABLE
MOV #10, R0
BIS #BIT12, @CSR ;FIRE ST
DEC R0
BNE #-2 ;DELAY
MOV #100, R0
RESET
CLR @PSW
DEC R0
BNE #-2

```

```

1389 ;TEST THAT THE CLOCK DOES NOT INTERRUPT AT LEVEL INDICATED
1390
1391 005136 104003 KWT53: SCOPE1
1392 005140 012777 000340 173654 MOV #340,@PSW ;SET PROCESSOR PRIORITY 5
1393 005146 012777 005230 173724 MOV #KWT53A,@CKV ;SET UP INTERRUPT RETURN STATUS
1394 005154 012777 000340 173720 MOV #340,@CKVS
1395 005162 005077 173662 CLR @CSR
1396 005166 012777 177774 173656 MOV #-4,@CSB
1397 005174 012777 000102 173646 MOV #102,@CSR ;ENABLE INTERRUPT
1399 005202 013777 014516 173612 MOV BRLEV3,@PSW
1399 005210 052777 000001 173632 BIS #BIT0,@CSR
1400 005216 012700 000100 MOV #100,@R0
1401 005222 005300 DEC R0
1402 005224 001376 BNE .-2
1403 005226 000401 BR .+4
1404 005230 104400 KWT53A: ERROR ;ERROR, INTERRUPT OCCUR IN ERROR AT LEVEL INDICA
1405 005232 000005 RESCT
1406
1407 ;TEST THAT THE CLOCK DOES NOT INTERRUPT AT LEVEL INDICATED +1
1408
1409 005234 104003 KWT54: SCOPE1
1410 005236 012777 000340 173556 MOV #340,@PSW ;SET PROCESSOR PRIORITY 6
1411 005244 012777 005326 173626 MOV #KWT54A,@CKV ;SET UP INTERRUPT RETURN
1412 005252 012777 000340 173622 MOV #340,@CKVS
1413 005260 005077 173564 CLR @CSR
1414 005264 012777 177774 173560 MOV #-4,@CSB
1415 005272 012777 000102 173550 MOV #102,@CSR ;INTERRUPT ENABLE
1416 005300 013777 014520 173514 MOV BRLEV3,@PSW
1417 005306 052777 000001 173534 BIS #BIT0,@CSR
1418 005314 012700 000100 MOV #100,@R0
1419 005320 005300 DEC R0
1420 005322 001376 BNE .-2 ;DELAY LONG ENOUGH TO ALLOW INTERRUPT
1421 005324 000401 BR .+4
1422 005326 104400 KWT54A: ERROR ;ERROR, INT SHOULDN'T HAVE OCCURRED
1423 005330 005077 173514 CLR @CSR ;STOP CLOCK
1424 005334 013777 001102 173536 MOV CKVS,@CKV
1425 005342 005077 173534 CLR @CKVS
1426 005346 000005 RESET
1427 005350 005077 173446 CLR @PSW
1428 005354 052777 000100 173442 BIS #BIT6,@TKS

```

1429
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1432 005362 104003
1433 005364 004537 005604
1434 005370 000002
1435 005372 000002
1436 005374 000001
1437 005376 000036
1438 005400 104400
1439 005402 003401
1440 005404 104400
1441
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1444 005406 104003
1445 005410 004537 005604
1446 005414 000004
1447 005416 000002
1448 005420 000001
1449 005422 000454
1450 005424 104400
1451 005426 003401
1452 005430 104400
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1456 005432 104003
1457 005434 004537 005604
1458 005440 000006
1459 005442 000002
1460 005444 000001
1461 005446 005670
1462 005450 104400
1463 005452 003401
1464 005454 104400
1465
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1468 005456 104003
1469 005460 004537 005604
1470 005464 000010
1471 005466 000002
1472 005470 000001
1473 005472 072460
1474 005474 104400
1475 005476 003401
1476 005500 104400

:TEST 1MHZ REPEATABILITY

KWT55: SCOPE1
JSR RS.REPEAT
2
2
1
30.
ERROR
BLE .+4
ERROR

:TEST REPEATIBILITY
:CLOCK RATE
:CLOCK DEV.
:MIN. COUNT
:DELAY
:ERROR, FAILED TO REACH MIN. COUNT
:ERROR, CLOCK REPEATIBILITY >2

:TEST 100 KHZ REPEATABILITY

KWT56: SCOPE1
JSR RS.REPEAT
4
2
1
300.
ERROR
BLE .+4
ERROR

:TEST REPEATIBILITY
:CLOCK RATE
:CLOCK DEV.
:MIN. COUNT
:DELAY
:ERROR, FAILED TO REACH MIN. COUNT
:ERROR, CLOCK REPEATIBILITY >2

:TEST 10 KHZ REPEATABILITY

KWT57A: SCOPE1
JSR RS.REPEAT
6
2
1
3000.
ERROR
BLE .+4
ERROR

:CLOCK RATE
:CLOCK DEV.
:MIN. COUNT
:DELAY
:ERROR, FAILED TO REACH MIN. COUNT
:ERROR CLOCK REPEATABILITY >2

:TEST 1KHZ REPEATABILITY

KWT60: SCOPE1
JSR RS.REPEAT
10
2
1
30000.
ERROR
BLE .+4
ERROR

:CLOCK RATE
:CLOCK DEV.
:MIN. COUNT
:DELAY
:ERROR, FAILED TO REACH MIN. COUNT
:ERROR CLOCK REPEATABILITY >2

```

1478 ;TEST 100HZ REPEATIBILITY
1479
1480
1481 005502 104003 KWT61: SCOPE1
1482 005504 004537 005604 JSR R5,REPEAT
1483 005510 000012 ;CLOCK RATE
1484 005512 000002 ;CLOCK DEV.
1485 005514 000001 ;MIN. COUNT
1486 005516 177777 ;DELAY
1487 005520 104400 ;ERROR, FAILED TO REACH MIN. COUNT
1488 005522 003401
1489 005524 104400 ;ERROR CLOCK REPEATABILITY >2
1490
1491
1492 ;TEST LINE REPEATABILITY
1493
1494 005526 104003 KWT62: SCOPE1
1495 005530 004537 005604 JSR R5,REPEAT
1496 005534 000016 ;CLOCK RATE
1497 005536 000001 ;CLOCK DEV.
1498 005540 000001 ;MIN. COUNT
1499 005542 000000 ;DELAY
1500 005544 104400 ;ERROR, FAILED TO REACH MIN COUNT
1501 005546 003401
1502 005550 104400 ;ERROR, CLOCK REPEATABILITY >+1
1503
1504 ;BELL ON PASS COMPLETE
1505
1506 005552 104003 TSTEND: SCOPE1 ;LOGICAL END OF THE TEST
1507 005554 000005 RESET
1508 005556 005737 000042 TST 0042
1509 005562 001402 BEQ HERE
1510 005564 000137 001752 JMP WHATB
1511
1512 HERE: JSR PC,BELL ;REPORT END OF PASS
1513 005574 005237 001040 INC PASSCT
1514 005580 000137 002066 JMP BEGIN

```

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:SUBROUTINE TO TEST THE CLOCK REPEATIBILITY
:FIRST CLEAR CLOCK STATUS AND PRESET BUFFER
: THEN ENABLE THE CLOCK TO COUNT AT A RATE.
: DECREMENT RO FOR SOME PERIOD OF TIME, WHEN RO = 0
: FIRE THE ST #2 AND CAUSE THE COUNTER TO LOAD THE PRESET REGISTER
: SAVE THE PRESET VALUE AND REPEAT THIS OPERATION AGAIN
: THEN COMPARE THE FIRST TIMED VALUE TO THE SECOND TIMED VALUE
: (MACHINE AND MEMORY TIMING NOT IMPORTANT)
: TO BE WITHIN THE VALUE SPECIFIED BY LOCATION CNTDEV
: IF GREATER THAN EXPECTED IT IS AN ERROR.
: ALSO TEST THAT THE COUNTER HAS REACHED A MIN. COUNT

REPEAT: CLR QCSR ;STOP THE CLOCK
CLR QCSB ;CLEAR THE BUFFER
MOV (R5)+,RATE ;SET UP RATE
MOV (R5)+,CNTDEV ;SET UP CNT. DEV
MOV (R5)+,MINCNT ;SET UP MIN COUNT
MOV (R5)+,CKDLY ;SAVE DELAY
JSR PC,10\$;DUMMY - TO CHARGE THE "CACHE"
JSR PC,10\$;ENABLE THE CLOCK
MOV RO,\$GDDAT ;SAVE 1ST RESULTS
JSR PC,10\$;ENABLE THE CLOCK
MOV RO,\$BDDAT ;SAVE THE 2ND RESULT
MOV \$GDDAT,RO ;GET 1ST RESULT
SUB \$BDDAT,RO ;SUBTRACT SECOND RESULT
BPL 3\$
NEG RO
CMP \$BDDAT,MINCNT ;COMPARE TO MIN. COUNT
BGE 4\$;BRANCK IF GREATER
MOV MINCNT,TEMP ;LOAD TEMP FOR TYPE-OUT
RTS R5
4\$: TST (R5)+ ;UPDATE THE STACK
CMP RO,CNTDEV ;COMPARE TO DEVEATION
RTS R5
10\$: MOV CKDLY,RO ;LOAD DELAY COUNT
BIS #BIT10!BIT9,RATE ;ENABLE ST MODE
MOV RATE,QCSR ;LOAD RATE
I, QCSR ;ENABLE THE CLOCK
1\$: DEC RO ;DELAY
BNE 1\$
BIS #BIT10,QCSR ;MAINT ST FIRE
MOV QCSB,RO ;READ THE RESULT
CLR QCSR ;STOP CLOCK
CLR QCSB ;CLEAR BUFFER
PC ;EXIT

\$GDDAT: 0
\$BDDAT: 0
RATE: 0 ;CLOCK RATE
CNTDEV: 0 ;CLOCK DEV.
MINCNT: 0 ;MIN. COUNT
CKDLY: 0

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```

:*****
:DIGITAL INPUT-OUTPUT LOGIC TEST
:*****

IOTEST: RESET
        PRINT
        MESJ          ;IDENTIFY TEST

ITEST1: CLR          PASSCT
IOTSTA: MOV          #DRT0+2, RETURN
        MOV          PASSCT, @DISPLA
        MOV          STACK, SP
        CLR          @PSW
        BIS          #BIT6, @TKS

;TEST FOR NO BUSS ERRORS

        CLR          @GRSTAT
        CLR          @GRDAI
        CLR          @GRDIO

DRT0:  SCOPE1
        MOV          #-1, @GRDIO      ;ALL ONES TO REGISTER
        CMP          #-1, @GRDIO
        BEQ          .+4
        ERROR          ;REG WILL NOT HOLD ONES

DRT1:  SCOPE
        MOV          #-1, @GRDIO
        RESET          ;SET DATA TO ALL ONES
        TST          @GRDIO          ;SHOULD CLEAR REGISTER
        BEQ          .+4
        ERROR          ;REG FAILED TO CLEAR

DRT2:  BIS          #BIT6, @TKS
        SCOPE1
        MOV          #52525, @GRDIO
        CMP          #52525, @GRDIO
        BEQ          .+4
        ERROR          ;DATA NOT=52525

DRT3:  SCOPE
        MOV          #125252, @GRDIO
        CMP          #125252, @GRDIO
        BEQ          .+4
        ERROR          ;DATA NOT=125252

```

L03

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 DZLPDC.P11 04-APR-76 00:00

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1615	006212	104003				DRT4:	SCOPE1		
1616	006214	012777	177777	172636			MOV	#-1,@GRDIO	
1617	006222	105077	172632				CLRB	@GRDIO	;CLEAR LOW BYTE
1618	006226	017737	172626	014506			MOV	@GRDIO,TEMP	
1619	006234	022737	177400	014506			CMP	#177400,TEMP	
1620	006242	001401					BEQ	+.4	
1621	006244	104400					ERROR		;BYTE LOW FAILED TO CLEAR
1622									
1623	006246	104002				DRT5:	SCOPE		
1624	006250	012777	177777	172632			MOV	#-1,@GRDIO	
1625	006256	105077	172610				CLRB	@GRBHIO	;CLEAR HIGH BYTE
1626	006252	017737	172572	014506			MOV	@GRDIO,TEMP	
1627	006270	022737	000377	014506			CMP	#377,TEMP	
1628	006276	001401					BEQ	+.4	
1629	006300	104400					ERROR		;HIGH BYTE CLEAR FAILED
1630									
1631	006302	005037	014506				CLR	TEMP	
1632	006306	104002				DRT6:	SCOPE		
1633	006310	113777	014506	172542		DRT6A:	MOV8	TEMP,@GRDIO	;LOAD THE OUTPUT
1634	006316	123777	014506	172534			CMP8	TEMP,@GRDIO	
1635	006324	001402					BEQ	+.6	;BRANCH IF EQUAL
1636	006326	104400					ERROR		;ERROR, L . BYTE HAS BAD DATA
1637	006330	000405					BR	DRT7	
1638	006332	105237	014506				INCB	TEMP	
1639	006336	001364					BNE	DRT6A	
1640									
1641	006340	005037	014506				CLR	TEMP	
1642	006344	104002				DRT7:	SCOPE		
1643	006346	113777	014506	172516		DRT7A:	MOV8	TEMP,@GRBHIO	;LOAD THE HIGH BYTE
1644	006354	123777	014506	172510			CMP8	TEMP,@GRBHIO	
1645	006362	001402					BEQ	+.6	;BRANCH IF EQUAL
1646	006364	104400					ERROR		;ERROR, HIGH BYTE IN ERROR
1647	006366	000403					BR	DRT8	
1648	006370	105237	014506				INCB	TEMP	
1649	006374	001364					BNE	DRT7A	

```

1650
1651 ;RELAY #1 TEST
1652
1653 006376 104003 DRT8: SCOPE1
1654 006400 012777 000001 172446 MOV #BIT0, @GRSTAT ;SET BIT 0
1655 006406 022777 000001 172440 CMP #BIT0, @GRSTAT ;TEST IT
1656 006414 001401 BEQ .+4
1657 006416 104400 ERROR ;ERROR, RELAY 1 FAILED TO SET
1658
1659 ;RELAY #2 TEST
1660
1661 006420 104002 DRT9: SCOPE
1662 006422 012777 000400 172424 MOV #BIT8, @GRSTAT ;SET RELAY 2
1663 006430 022777 000400 172416 CMP #BIT8, @GRSTAT
1664 006436 001401 BEQ .+4
1665 006440 104400 ERROR ;ERROR, RELAY 2 FAILED TO SET
1666
1667 ;TEST OUTPUT DATA ACCEPT FLAG
1668
1669 006442 104002 DRT10: SCOPE
1670 006444 012777 100000 172402 MOV #BIT15, @GRSTAT ;SET BIT 15
1671 006452 022777 100000 172374 CMP #BIT15, @GRSTAT
1672 006450 001401 BEQ .+4
1673 006462 104400 ERROR ;ERROR, BIT 15 FAILED TO SET
1674
1675 ;TEST OUTPUT INTERRUPT ENABLE
1676
1677 006464 104002 DRT11: SCOPE
1678 006466 012777 000340 172326 MOV #340, @PSW ;RAISE PRIORITY
1679 006474 012777 040000 172352 MOV #BIT14, @GRSTAT ;LOAD BIT 14
1680 006502 022777 040000 172344 CMP #BIT14, @GRSTAT
1681 006510 001401 BEQ .+4
1682 006512 104400 ERROR ;ERROR BIT 14 FAILED TO SET
1683
  
```

```

1684
1685
1686 ;TEST INPUT DATA READY FLAG
1687 006514 104002 DRT12: SCOPE
1688 006516 012777 000200 172330 MOV #BIT7,@GRSTAT ;SET BIT 7
1689 006524 022777 000200 172322 CMP #BIT7,@GRSTAT
1690 006532 001401 BEQ .+4
1691 006534 104400 ERROR ;ERROR, BIT 7 FAILED TO SET
1692
1693 ;TEST INPUT INTERRUPT ENABLE
1694
1695 006536 104002 DRT13: SCOPE
1696 006540 012777 000340 172254 MOV #340,@PSW
1697 006546 012777 000100 172300 MOV #BIT6,@GRSTAT ;SET BIT 6
1698 006554 022777 000100 172272 CMP #BIT6,@GRSTAT
1699 006562 001401 BEQ .+4
1700 006564 104400 ERROR ;ERROR, BIT 6 FAILED TO SET
1701
1702 ;TEST THAT RESET CLEARS THE DIGITAL STATUS REGISTER
1703
1704 006566 104002 DRT14: SCOPE
1705 006570 012777 000340 172224 MOV #340,@PSW
1706 006576 012777 140701 172250 MOV #BIT15!BIT14!BIT8!BIT7!BIT6!BIT0,@GRSTAT
1707 006604 000005 RESET
1708 006606 005777 172242 TST @GRSTAT
1709 006612 001401 BEQ .+4
1710 006614 104400 ERROR ;ERROR, RESET FAILED TO CLEAR DIGITAL STATUS REG
1711
1712 006516 005077 172200 CLR @PSW
1713 006622 052777 000100 172174 BIS #BIT6,@TKS

```


:TEST THAT THE INPUT CAN INTERRUPT
:USE MAINT. BIT

007230 005077 171706
007232 104003
007234 000005
007236 005077 171676
007238 000340 171636
007240 012777 171712
007242 007232 171706
007244 000340 171706
007246 001112 171702
007248 012777 171676
007250 005077 171600
007252 052777 171526
007254 000240
007256 000000

DRT22: CLR 2GRSTAT
SCOPE1
RESET
CLR 2GRSTAT :CLEAR STATUS
MOV 2340,2PSW :RAISE PRIOR
MOV 2DRT22A,2GRIVA :LOAD RETURN VECTOR
MOV 2340,2GRIVSA :
MOV GRIVSB,2GRIVB :LOAD OUTPUT VECTOR
MOV 20,2GRIVSB
CLR 2PSW
BIS 2BITS,2GRSTAT :MAINT. INT C
NOP
HALT :ERROR, INPUT FAILED TO INTERRUPT

:SUB-TEST, TEST THAT IF PSW IS LOWERED AGAIN NO INTERRUPT WILL OCCUR
: IF INTERRUPT OCCURS 'INT DONE C' FAILED TO CLEAR INT C FLOP

007258 013777 001106 171644
007260 005077 171642
007262 005077 171552
007264 000240
007266 000240

DRT22A: MOV GRIVSA,2GRIVA :LOAD INPUT VECTOR
CLR 2GRIVSA
CLR 2PSW :LOWER PRIOR.
NOP
NOP

:TEST THAT THE OUTPUT DOES INTERRUPT
:USE MAINT. BIT

007268 005077 171574
007270 104003
007272 000005
007274 005077 171564
007276 012777 000340 171524
007278 013777 001106 171600
007280 012777 000000 171574
007282 012777 007344 171570
007284 012777 000340 171564
007286 005077 171470
007288 052777 020000 171514
007290 000240
007292 000000

DRT25: CLR 2GRSTAT :CLEAR STATUS
SCOPE1
RESET
CLR 2GRSTAT :CLEAR STATUS
MOV 2340,2PSW
MOV GRIVSA,2GRIVA :LOAD INPUT VECTOR
MOV 20,2GRIVSA
MOV 2DRT25A,2GRIVB :LOAD OUTPUT VECTOR
MOV 2340,2GRIVSB
CLR 2PSW
BIS 2BIT13,2GRSTAT :MAINT. INTERRUPT
NOP
HALT :OUTPUT FAILED TO INTERRUPT

:SUB-TEST, TEST THAT IF PSW IS LOWERED AGAIN, NO INTERRUPT WILL OCCUR
: IF IT DOES, 'INT DONE D HIGH' FAILED TO CLEAR 'INT D' FLOP

007294 013777 001112 171536
007296 005077 171534
007298 005077 171440
007300 000240
007302 000240

DRT25A: MOV GRIVSB,2GRIVB :LOAD OUTPUT VECTOR
CLR 2GRIVSB
CLR 2PSW
NOP
NOP

```

18574 007452 104003
18575 007452 000005
18576 007456 012777 000340 171336
18577 007464 005077 171364
18578 007470 012777 007532 171406
18579 007476 012777 007532 171404
18580 007504 013777 014514 171310
18581 007512 052777 020040 171334
18582 007520 000240
18583 007522 000240
18584 007524 000240
18585 007526 000240
18586 007530 104400
18587 007532 022626
18588 007534 104003
18589 007536 000005
18590 007540 032777 000100 171266
18591 007546 001402
18592 007550 000137 007654
18593 007554 012777 000340 171240
18594 007562 005077 171266
18595 007566 012777 007652 171310
18596 007574 012777 007652 171306
18597 007602 013777 014514 171212
18598 007610 012777 040100 171236
18599 007616 012777 000000 171234
18600 007624 017700 171226
18601 007630 000240
18602 007632 000240
18603 007634 000240
18604 007636 042777 040100 171210
18605 007644 000240
18606 007646 104400
18607 007650 000401
18608 007652 022626

```

:PRE INTERRUPT SETUP

```

DRT29: SCOPE1
      BIC      #177437,DIOBRL
      BNE     .+4
      HALT
      CMP     #340,DIOBRL
      SNE     .+4
      HALT
      MOV     DIOBRL, BRLEV1
      SUB     #40, BRLEV1
      MOV     DIOBRL, BRLEV2
      MOV     DIOBRL, BRLEV3
      ADD     #40, BRLEV3

```

```

;BR LEVEL INDICATED FOR DIGITAL I/O WAS 0.
;BR LEVEL INDICATED FOR DIGITAL I/O WAS 7

```

:TEST FOR INTERRUPT FROM DIGITAL I/O ON LEVEL INDICATED -1

```

DRT29: SCOPE
      RESET
      MOV     #340, PPSW      ;RAISE PSW
      CLR     JGRSTAT        ;CLEAR ENABLES
      MOV     #DRT29A, JGRIVA ;SET UP VECTORS
      MOV     #DRT29A, JGRIVB
      MOV     BRLEV1, PPSW    ;LOWER PSW
      BIS     #BIT13!BITS, JGRSTAT ;GENERATE MAINT. INTERRUPT
      NOP
      NOP
      NOP
      NOP
      ERROR

```

:ERROR, NO INTERRUPT FROM DIGITAL I/O

DRT29A: CMP (SP)+, (SP)+

:TEST FOR INTERRUPT FROM DIGITAL I/O ON LEVEL INDICATED -1

```

DRT29B: SCOPE1
      RESET
      BIT     #BIT6, JPSWR    ;TEST SWITCH
      BEQ     .+6
      JMP     DRT30          ;BYPASS THIS TEST
      MOV     #340, PPSW
      CLR     JGRSTAT
      MOV     #DRT29C, JGRIVA ;IN CASE OF INTERRUPT
      MOV     #DRT29C, JGRIVB
      MOV     BRLEV1, PPSW
      MOV     #BIT14!BIT6, JGRSTAT
      MOV     #0, JGRDIO      ;OUTPUT
      MOV     JGRDAI, RO      ;INPUT
      NOP
      NOP
      NOP
      BIC     #BIT14!BIT6, JGRSTAT
      NOP
      ERROR
      BR     DRT30
DRT29C: CMP (SP)+, (SP)+

```

:ERROR, NO DIGITAL I/O INTERRUPT OCCURED

:TEST FOR NO INTERRUPT FROM DIGITAL I/O ON LEVEL INDICATED

```

1998 007654 104003          DRT30: SCOPE1
1999 007656 000005          RESET
1900 007660 012777 000340 171134  MOV      #340,JPSW
1901 007666 005077 171162  CLR      JGRSTAT      :CLEAR STATUS
1902 007672 012777 007752 171204  MOV      #DRT30A,JGRIVA :IN CASE OF INTERRUPT
1903 007700 012777 007752 171202  MOV      #DRT30A,JGRIVB :
1904 007706 013777 014516 171106  MOV      BRLEV2,JPSW
1905 007714 012777 040100 171132  MOV      #BIT14!BIT6,JGRSTAT :LOAD INT. ENABLE
1906 007722 012777 000000 171130  MOV      #C,JGRDIO      :OUTPUT
1907 007730 017700 171122  MOV      JGRDAI,RO      :INPUT
1908 007734 000240          NOP
1909 007736 000240          NOP
1910 007740 000240          NOP
1911 007742 042777 040100 171104  BIC      #BIT14!BIT6,JGRSTAT :DON'T LEAVE IT SET
1912 007750 000401          BR      .+4           :WITH NO INTERRUPT, BRANCH OVER HALT
1913 007752 104400          DRT30A: ERROR      :ERROR, INTERRUPT OCCURED AT BR INDICATED
1914
1915 007754 104003          SCOPE1
1916 007756 000005          RESET
1917 007760 013777 001106 171116  MOV      GRIVSA,JGRIVA  :FOR FALSE INTERRUPT
1918 007766 005077 171114  CLR      JGRIVSA
1919 007772 013777 001112 171110  MOV      GRIVSB,JGRIVB
1920 010000 005077 171106  CLR      JGRIVSB
1921
1922          :LOGICAL END OF 'DIGITAL I/O LOGIC TEST'
1923
1924 010004 000005          RESET
1925 010006 005737 000042  TST     #42
1926 010012 001402          BEQ     .+6
1927 010014 000137 001764  JMP     WHATC
1928 010020 004737 012472  JSR     7,BELL      :REPORT END OF PASS
1929 010024 005237 001040  INC     PASSCT
1930 010030 000137 006026  JMP     IOTSTA

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0:0034 000005
0:0036 104000
0:0040 014110
0:0042 005037 001040
0:0046 013706 014444
0:0052 013777 001040 170756
0:0050 012737 010116 013414
0:0066 005077 170730
0:0072 052777 000100 170724

0:0100 005077 170756
0:0104 005077 170754
0:0110 005077 170752

0:0114 104002
0:0116 000005
0:0120 105777 170736
0:0124 100401
0:0126 104400

0:0130 104003
0:0132 052777 000100 170654
0:0140 012777 000002 170714
0:0146 022777 000202 170706
0:0154 001401
0:0156 104400

0:0160 104002
0:0162 012777 000004 170672
0:0170 022777 000204 170664
0:0176 001401
0:0200 104400

0:0202 104002
0:0204 012777 000010 170650
0:0212 022777 000210 170642
0:0220 001401
0:0222 104400

```
*****
LPSVC POINT PLOT SCOPE CONTROL
*****

VCTEST: RESET
PRINT
MESS ; IDENTIFY TEST
VTEST1: CLR PASSCT

VCTST0: MOV STACK, SP
MOV PASSCT, @DISPLA
MOV @VCT0+2, RETURN
CLR @PSW
BIS @BIT6, @TKS

; TEST FOR NO BUSS ERRORS

CLR @VCSTAT
CLR @VCXREG
CLR @VCYREG

; TEST THAT RESET SETS READY BIT

VCT0: SCOPE
RESET
TSTB @VCSTAT ; TEST READY
BMI .+4 ; ERROR, VCSTAT NOT = 200
ERROR

; TEST THAT FAST INTENSIFY (BIT 1) CAN BE SET AND CLEARED

VCT1: SCOPE1
BIS @BIT6, @TKS
MOV @BIT1, @VCSTAT ; LOAD DISPLAY STATUS
CMP @BIT7!@BIT1, @VCSTAT ; TEST STATUS
BEQ .+4 ; ERROR, VC STATUS NOT = 202
ERROR

; TEST THAT MODE (BIT 2) CAN BE SET AND CLEARED

VCT2: SCOPE
MOV @BIT2, @VCSTAT ; LOAD DISPLAY STATUS
CMP @BIT7!@BIT2, @VCSTAT ; TEST STATUS
BEQ .+4 ; ERROR, VC STATUS NOT = 204
ERROR

; TEST THAT MODE (BIT 3) CAN BE SET AND CLEARED

VCT3: SCOPE
MOV @BIT3, @VCSTAT ; LOAD DISPLAY STATUS
CMP @BIT7!@BIT3, @VCSTAT ; TEST STATUS
BEQ .+4 ; ERROR, VC STATUS NOT = 210
ERROR
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H04

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1985  
1986 ;TEST THAT EXT DEL (BIT 4) CAN BE SET AND CLEARED  
1987  
1988 010324 104002 VCT4: SCOPE  
1989 010326 012777 000020 170626 MOV #BIT4,AVCSTAT ;LOAD DISPLAY STATUS  
1990 010324 022777 000220 170620 CMP #BIT7!BIT4,AVCSTAT ;TEST STATUS  
1991 010242 001401 BEQ .+4  
1992 010244 104400 ERROR ;ERROR, VC STATUS NOT = 220  
1993  
1994 ;TEST THAT INTERRUPT ENABLE (BIT 6) CAN BE SET AND CLEARED  
1995  
1996 010246 104002 VCT5: SCOPE  
1997 010250 012777 000100 170604 MOV #BIT6,AVCSTAT ;LOAD DISPLAY STATUS  
1998 010256 022777 000300 170576 CMP #BIT7!BIT6,AVCSTAT ;TEST STATUS  
1999 010264 001401 BEQ .+4  
2000 010266 104400 ERROR ;ERROR, VC STATUS NOT = 300  
2001  
2002 ;TEST THAT CHANNEL (BIT 9) CAN BE SET AND CLEARED  
2003  
2004 010270 104002 VCT6: SCOPE  
2005 010272 012777 001000 170562 MOV #BIT9,AVCSTAT ;LOAD DISPLAY STATUS  
2006 010300 022777 001200 170554 CMP #BIT9!BIT7,AVCSTAT ;TEST STATUS  
2007 010306 001401 BEQ .+4  
2008 010310 104400 ERROR ;ERROR, VC STATUS NOT = 1200  
2009  
2010 ;TEST THAT STORE (BIT 10) CAN BE SET AND CLEARED  
2011  
2012 010312 104002 VCT7: SCOPE  
2013 010314 012777 002000 170540 MOV #BIT10,AVCSTAT ;LOAD DISPLAY STATUS  
2014 010322 022777 002200 170532 CMP #BIT10!BIT7,AVCSTAT ;TEST STATUS  
2015 010330 001401 BEQ .+4  
2016 010332 104400 ERROR ;ERROR, VC STATUS NOT = 2200  
2017  
2018 ;TEST THAT WRITE THRU (BIT 11) CAN BE SET AND CLEARED  
2019  
2020 010334 104002 VCT8: SCOPE  
2021 010336 012777 004000 170516 MOV #BIT11,AVCSTAT ;LOAD DISPLAY STATUS  
2022 010344 022777 004200 170510 CMP #BIT11!BIT7,AVCSTAT ;TEST STATUS  
2023 010352 001401 BEQ .+4  
2024 010354 104400 ERROR ;ERROR, VC STATUS NOT = 4200  
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010360
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010462
010464
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010470
010476
010504
010512
010514
010516
010524
010526

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;TEST THAT THE X REGISTER (BITS 0-11) CAN BE SET AND CLEARED
VCT11: SCOPE
MOV      #2525,2VCXREG      ;LOAD X REGISTER
CMP      #2525,2VCXREG
BEQ      .+4
ERROR    ;ERROR, VC X REGISTER NOT = 2525

VCT12: SCOPE
MOV      #5252,2VCXREG      ;LOAD X REGISTER
CMP      #5252,2VCXREG
BEQ      .+4
ERROR    ;ERROR, VC X REGISTER NOT = 5252

;TEST THAT THE Y REGISTER (BITS 0-11) CAN BE SET AND CLEARED
VCT15: SCOPE
MOV      #2525,2VCYREG      ;LOAD Y REGISTER
CMP      #2525,2VCYREG
BEQ      .+4
ERROR    ;ERROR, VC Y REGISTER NOT = 2525

VCT16: SCOPE
MOV      #5252,2VCYREG      ;LOAD Y REGISTER
CMP      #5252,2VCYREG
BEQ      .+4
ERROR    ;ERROR, VC Y REGISTER NOT = 5252

;TEST THAT THE X-Y REGISTER CAN HOLD DIFFERENT DATA
VCT17: SCOPE
MOV      #1234,2VCXREG      ;LOAD X REGISTER
MOV      #4321,2VCYREG      ;LOAD Y REGISTER
CMP      #1234,2VCXREG
BEQ      .+4
ERROR    ;ERROR, SELECT X REGISTER INCORRECTLY

CMP      #4321,2VCYREG
BEQ      .+4
ERROR    ;ERROR, SELECTED Y REGISTER INCORRECTLY

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2068
2069 ;TEST THAT WHEN INTENSIFY BIT IS SET THAT THE READY BIT CLEARS
2070 ; AND THEN SETS AFTER A DELAY
2071
2072 010530 104002 SCOPE
2073 010532 012700 000100 MOV #100,RO
2074 010536 012777 000001 170316 MOV #BIT0,AVCSTAT ;INTENSIFY
2075 010544 105777 170312 TSTB AVCSTAT ;TEST READY
2076 010550 100001 BPL .+4 ;IS IT CLEARED ?
2077 010552 104400 ERROR ;READY FAILED TO CLEAR
2078 010554 105777 170302 VCTST2: TSTB AVCSTAT ;TEST READY
2079 010550 100403 BMI VCTST3 ;SET EXIT
2080 010552 005300 DEC RO ;DELAY
2081 010564 001373 BNE VCTST2
2082 010566 104400 ERROR ;READY FAILED TO SET AFTER A DELAY
2083
2084 ;TEST THAT WHEN COLOR IS CHANGED READY CLEARS AND THEN SETS AFTER A DELAY
2085
2086 010570 104003 VCTST3: SCOPE1
2087 010572 012700 000400 MOV #400,RO ;SET UP A DELAY
2088 010576 012777 000400 170256 MOV #BIT8,AVCSTAT ;CHANGE TO RED
2089 010604 032777 000400 170250 BIT #BIT8,AVCSTAT ;TEST COLOR BIT
2090 010612 001001 BNE .+4 ;IS IT SET ?
2091 010614 104400 ERROR ;ERROR, COLOR BIT FAILED TO SET
2092 010616 105777 170240 TSTB AVCSTAT ;TEST READY
2093 010622 100001 BPL .+4 ;IS IT CLEARED ?
2094 010624 104400 ERROR ;ERROR, VC STATUS READY FAILED TO CLEAR
2095 010626 105777 170230 VCTST4: TSTB AVCSTAT ;TEST READY
2096 010632 100403 BMI VCTST5 ;IS IT SET ?
2097 010634 005300 DEC RO ;NO, DELAY
2098 010636 001373 BNE VCTST4
2099 010640 104400 ERROR ;ERROR, READY FAILED TO SET AFTER A COLOR CHANGE
2100
2101 ;TEST THAT WHEN COLOR IS CHANGED READY CLEARS AND THEN SETS AFTER A DELAY
2102
2103 010642 104001 VCTST5: SCOPE0
2104 010644 012700 020000 MOV #20000,RO ;SET UP A DELAY
2105 010650 012777 000000 170204 MOV #0,AVCSTAT ;CHANGE TO GREEN
2106 010656 032777 000400 170176 BIT #BIT8,AVCSTAT ;TEST COLOR BIT
2107 010664 001401 BEQ .+4
2108 010666 104400 ERROR ;ERROR, COLOR BIT FAILED TO CLEAR
2109 010670 105777 170166 TSTB AVCSTAT ;TEST READY
2110 010674 100001 BPL .+4 ;DID IT CLEAR
2111 010676 104400 ERROR ;ERROR, READY FAILED TO CLEAR
2112 010700 105777 170156 VCTST6: TSTB AVCSTAT ;TEST READY
2113 010704 100403 BMI VCTST7
2114 010706 005300 DEC RO
2115 010710 001373 BNE VCTST6
2116 010712 104400 ERROR ;ERROR, READY FAILED TO SET AFTER A COLOR CHANGE

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2117
2118          ;TEST THAT MODE 1 (INTENSIFY ON X)
2119          ;CLEARS THE READY FLAG AND THEN SETS IT
2120
2121          010714 104001          VCTST7: SCOPED
2122          010716 012700 000100          MOV      #100,RO          ;SET UP DELAY
2123          010722 012777 000C04 170132          MOV      #BIT2,AVCSTAT ;LOAD MODE 1
2124          010730 105777 170126          TSTB    AVCSTAT        ;TEST READY
2125          010734 100401          BMI      .+4
2126          010736 104400          ERROR          ;ERROR, MODE 1 SHOULD NOT CLEAR READY UNTIL X IS
2127
2128          010740 005077 170120          CLR      AVCXREG        ;ADDRESS X AXIS
2129          010744 105777 170112          TSTB    AVCSTAT        ;TEST READY
2130          010750 100001          BPL      .+4
2131          010752 104400          ERROR          ;ERROR, MODE 1 LOAD X FAILED TO CLEAR READY FLAG
2132
2133          010754 105777 170102          VCTST8: TSTB    AVCSTAT ;TEST READY
2134          010760 100403          BMI      VCTST9         ;SET NEXT TEST
2135          010762 005300          DEC      RO             ;DELAY
2136          010764 001373          BNE      VCTST8        ;TEST READY AGAIN
2137          010766 104400          ERROR          ;ERROR, READY FAILED TO SET
2138          ; AFTER MODE 1 OPERATION
2139
2140
2141          ;TEST THAT MODE 2 (INTENSIFY ON Y)
2142          ;CLEARS THE READY FLAG AND THEN SETS IT
2143
2144          010770 104003          VCTST9: SCOPED
2145          010772 012700 000100          MOV      #100,RO          ;SET UP DELAY
2146          010776 012777 000010 170056          MOV      #BIT3,AVCSTAT ;LOAD MODE 2
2147          011004 105777 170052          TSTB    AVCSTAT        ;TEST READY
2148          011010 100401          BMI      .+4
2149          011012 104400          ERROR          ;ERROR, MODE 2 SHOULD NOT CLEAR READY UNTIL Y IS
2150
2151          011014 005077 170046          CLR      AVCYREG        ;ADDRESS Y AXIS
2152          011020 105777 170036          TSTB    AVCSTAT        ;TEST READY
2153          011024 100001          BPL      .+4
2154          011026 104400          ERROR          ;ERROR, MODE 2 LOAD Y FAILED TO CLEAR READY FLAG
2155
2156          011030 105777 170026          VCTS10: TSTB    AVCSTAT ;TEST READY
2157          011034 100403          BMI      VCTS11         ;SET NEXT TEST
2158          011036 005300          DEC      RO             ;DELAY
2159          011040 001373          BNE      VCTS10        ;TEST READY AGAIN
2160          011042 104400          ERROR          ;ERROR, READY FAILED TO SET
2161          ; AFTER MODE 2 OPERATION

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2162          ;TEST THAT WHEN ERASE BIT IS SET THAT THE READY BIT
2163          ;CLEARS AND THEN SETS AFTER A DELAY
2164
2165 011044 104003          VCTS11: SCOPE1
2166 011046 032777 000040 167760 BIT      #BIT5,%SWR
2167 011054 001424          BEQ      AVCT12
2168 011056 012700 000002          MOV      #2,R0
2169 011062 005037 014506          CLR      TEMP
2170 011066 052777 012000 167766 BIS      #BIT12!BIT10,%VSTAT ;CLEAR DELAY
2171 011074 105777 167762          TSTB    %VSTAT ;SET BIT 12
2172 011100 100001          BPL      .+4 ;TEST THAT READY CLEARS
2173 011102 104400          ERROR ;ERROR, READY FAILED TO RESET
2174          ; UPON SETTING ERASE BIT
2175
2176 011104 105777 167752          TST11A: TSTB    %VSTAT ;TEST FOR READY
2177 011110 100406          BMI      AVCT12 ;BRANCH IF SET
2178 011112 005337 014506          DEC      TEMP ;DELAY
2179 011116 001372          BNE      TST11A ;BRANCH IF NOT READY
2180 011120 005300          DEC      R0 ;DECREMENT COUNTER
2181 011122 001370          BNE      TST11A ;BRANCH IF NOT COMPLETED
2182 011124 104400          ERROR ;ERROR, ERASE CLEARED READY AND FAILED
2183          ; TO SET READY AFTER A DELAY
2184
2185          ;TEST THAT THERE IS A TIME DIFFERENCE BETWEEN FAST INTENSIFY
2186          ; AND NOT FAST INTENSIFY
2187
2188 011126 104001          AVCT12: SCOPED
2189 011130 005000          CLR      R0 ;CLEAR R0
2190 011132 012777 000001 167722 MOV      #BIT0,%VSTAT ;START DISPLAY NOT FAST INTEN.
2191 011140 105777 167716          VCTS12: TSTB    %VSTAT ;TEST READY
2192 011144 100403          BMI      VCTS13 ;IT IS SET
2193 011146 005200          INC      R0 ;INCREMENT R0
2194 011150 001373          BNE      VCTS12 ;TEST AGAIN
2195 011152 104400          ERROR ;ERROR, READY FAILED TO SET
2196
2197 011154 005001          VCTS13: CLR      R1 ;CLEAR R1
2198 011156 012777 000002 167676 MOV      #BIT1,%VSTAT ;FAST INTEN.
2199 011164 052777 000001 167670 BIS      #BIT0,%VSTAT ;START DISPLAY
2200 011172 105777 167664          VCTS14: TSTB    %VSTAT ;TEST READY
2201 011176 100403          BMI      VCTS15 ;IS IT SET
2202 011200 005201          INC      R1 ;NO, INCREMENT R1
2203 011202 001373          BNE      VCTS14 ;TEST AGAIN
2204 011204 104400          ERROR ;ERROR, READY FAILED TO SET
2205          ; WHEN IN FAST INTENSIFY
2206 011206 160001          VCTS15: SUB      R0,R1
2207 011210 042701 000007          BIC      #7,R1
2208 011214 001001          BNE      .+4 ;ARE THEY EQUAL ?
2209 011216 104400          ERROR ;ERROR, NO TIME DIFFERENCE BETWEEN FAST INTENSIF

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2210
2211
2212 ;PRE-INTERRUPT SETUP
2213 011220 042737 177437 001012 BIC #177437,VCBRL ;MASK TO PSW
2214 011226 001001 BNE .+4
2215 011230 000000 HALT ;LOCATION VCBRL CONTAINED A BR LEVEL 0
2216 011232 022737 000340 001012 CMP #340,VCBRL ;
2217 011240 001001 BNE .+4 ;TEST FOR BR 7
2218 011242 000000 HALT ;LOCATION VCBRL CONTAINS BR LEVEL 7
2219
2220 011244 013737 001012 014514 MOV VCBRL,BRLEV1 ;SET UP BR LEVELS
2221 011252 162737 000040 014514 SUB #40,BRLEV1 ; -1
2222 011250 013737 001012 014516 MOV VCBRL,BRLEV2 ; 0
2223 011266 013737 001012 014520 MOV VCBRL,BRLEV3 ; +1
2224 011274 062737 000040 014520 ADD #40,BRLEV3
2225
2226 ;TEST THAT THE LPSVC DOES NOT INTERRUPT
2227
2228 011302 104003 SCOPE1
2229 011304 012777 000340 167510 MOV #340,@PSW
2230 011312 013706 014444 MOV STACK,SP ;SET UP THE STACK POINTER
2231 011316 000005 RESET
2232 011320 012777 011354 167566 MOV #15,@VCIV ;SET VECTOR
2233 011326 005077 167470 CLR @PSW
2234 011332 012777 000100 167522 MOV #BIT6,@VCSTAT ;SET INTERRUPT ENABLE
2235 011340 005000 CLR RD
2236 011342 005300 DEC RD
2237 011344 001376 BNE -2
2238 011346 005077 167510 CLR @VCSTAT ;CLEAR INTERRUPT ENABLE
2239 011352 000401 BR VCTS20 ;NEXT TEST
2240
2241 011354 104400 15: ERROR ;UNEXPECTED DISPLAY INTERRUPT

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;TEST THAT THE DISPLAY DOES INTERRUPT A LEVEL INDICATED -1

VCTS20: SCOPE1

011356 104003
011360 000005
011362 012777 000340 167432
011370 013706 014444
011374 012777 011434 167512
011402 012700 000400
011406 013777 014514 167406
011414 012777 000101 167440
011422 005300
011424 001376
011426 005077 167430
011432 104400

RESET
MOV #340, JPSW
MOV STACK, SP ;SET UP STACK
MOV #VCRET1, JVCIV ;SET INTERRUPT VECTOR
MOV #400, RO ;SET UP DELAY
MOV BRLEV1, JPSW
MOV #BIT6!BIT0, JVCSTAT ;START DISPLAY
DEC RO ;DELAY
SNE -2
CLR JVCSTAT ;DO NOT LET INTERRUPT ENABLE SET
ERROR ;DISPLAY FAILED TO INTERRUPT

;TEST THAT THE DISPLAY DOES NOT INTERRUPT A LEVEL INDICATED

VCRET1: SCOPE1

011434 104003
011436 000005
011440 012777 000340 167354
011446 013706 014444
011452 012777 011506 167434
011460 012700 000400
011464 013777 014516 167330
011472 012777 000101 167362
011500 005300
011502 001376
011504 000403
011506 005077 167350
011512 104400

RESET
MOV #340, JPSW
MOV STACK, SP ;SET UP STACK
MOV #VCRET2, JVCIV ;SET INTERRUPT VECTOR
MOV #400, RO ;SET UP DELAY
MOV BRLEV2, JPSW
MOV #BIT6!BIT0, JVCSTAT ;START DISPLAY
DEC RO ;DELAY
BNE -2
BR OP55
VCRET2: CLR JVCSTAT ;DO NOT LET INTERRUPT ENABLE SET
ERROR ;DISPLAY INTERRUPTED IN ERROR

VCRET2: CLR

011514 013777 001116 167372
011522 000005

OP55: MOV VCI5, JVCIV ;RESTORE INTERRUPT VECTOR
RESET


```

012304 002304      MOV      (SP)+,R4
012303 000003      MOV      (SP)+,R3
012302 000003      MOV      (SP)+,R2
012301 000003      MOV      (SP)+,R1
012300 000003      MOV      (SP)+,R0
012276 000003      CMP      (SP)+,(SP)+
012275 000003      JMP      @VECTR
012274 000003      SPCHR1:  CMPB   #3,R1
012273 000003      BNE     +6
012272 000003      JMP     MONTR
012271 000003      CMPB   #177,R1
012270 000003      BNE     SPCHR3
012269 000003      TST    CHRCNT
012268 000003      BEQ    INPUTA
012267 000003      DEC    CHRCNT
012266 000003      MOV    #134,R1
012265 000003      TST    -(R4)
012264 000003      BR     OUTPTA
012263 000003      SPCHR3:  CMPB   #54,R1
012262 000003      BEQ    INPUTB
012261 000003      SPCHR4:  CMPB   #15,R1
012260 000003      BNE     IS
012259 000003      PRINT
012258 000003      CALF
45:      MOV    (SP)+,R5
012257 000003      MOV    (SP)+,R4
012256 000003      MOV    (SP)+,R3
012255 000003      MOV    (SP)+,R2
012254 000003      MOV    (SP)+,R1
012253 000003      MOV    (SP)+,R0
012252 000003      RTI
012251 000003      IS:     CMPB   #7,R1
012250 000003      BNE     SPCHR5 ;BR IF NOT
012249 000003      PRINT
012248 000003      CNTRLG
012247 000003      PRTOCT
012246 000003      SOFTSW
012245 000003      PRINT
012244 000003      NEWSWR
012243 000003      TTYIN
012242 000003      CLR    R1
012241 000003      MOV    #INBUF,R0
012240 000003      23:   TST    (R0)
012239 000003      BEQ    35
012238 000003      MOV    (R0)+,R2
012237 000003      BIC    #17770,R2
012236 000003      ASL   R1
012235 000003      ASL   R1
012234 000003      ASL   R1
012233 000003      ADD   R2,R1
012232 000003      BR    25
012231 000003      35:   MOV    R1,SOFTSW
012230 000003      BR
012326 104000      SPCHR5: PRINT
012325 01441E      JMARK

```

```

: YES, EXIT VIA 'IA' VECTOR ADDRESS.
: CHAR. = 'IC'
: NO, NOT 'IC'
: YES, EXIT TO MONITOR
: CHAR. = 'RUBOUT'
: IGNORE CHAR. & EXIT
: IS RUBOUT LEGAL?
: NO, IGNORE IT

: TYPE '\ ' TO INDICATE RUBOUT
: POP OFF LAST CHARACTER
: WAIT FOR NEXT CHARACTER
: TEST FOR '.'
: LEGAL CHAR. SAVE IT
: TO 'CARRIAGE RETURN' TO TERMINATE
: NO, CONTINUE
: YES, TYPE 'CR-LF'

```

```

: EXIT
: TEST IF CTRL G
: REPORT OLD
: ASK FOR NEW
: CLEAR NEW
: LOAD NEW POINTER
: TEST FOR TERM
: BR IF TERM
: GET A VALUE
: MASK

```

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: SAVE SWITCH VALUE
: OTHERWISE TYPE '?'

```

012332 000606
012334 000000

012352

010046
010146
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BR NEWIN
INBUF: 0

: WAIT FOR NEW ENTRY
: CHARACTER STORAGE BUFFER

:POWER FAIL HANDLER
= +14

PWFAL: MOV R0, -(SP)
MOV R1, -(SP)
MOV R2, -(SP)
MOV R3, -(SP)
MOV R4, -(SP)
MOV R5, -(SP)
MOV R4, -(SP)
MOV SP, PROC
MOV #FWRUP, R24
HALT

:POWER LP HANDLER

PWRUP: MOV #340, RPSW
MOV PROC, SP
MOV (SP)+, R24
MOV (SP)+, R25
MOV (SP)+, R24
MOV (SP)+, R23
MOV (SP)+, R22
MOV (SP)+, R21
MOV (SP)+, R20
RESET
PRINT
MSG2:
JMP MONTR

000024
014450
012406 000024

166406

001352

012452 011546
012454 162716 000002
012456 011546 000000
012458 005716
012460 001001
012462 000000
012464 006316
012466 042716 177001
012468 062716 012512
012470 011546 000000
012510 000136

:EMT DISPATCH SERVICE ROUTINE
:ARGUMENT OF EMT IS EXTRACTED AND USED AS OFFSET TO OBTAIN POINTER
:TO THE SELECTED SUBROUTINE.

EMTSRV: MOV (SP) -(SP) :GET PC FOR TO RETURN
SUB #2,(SP) :PC OF EMT
MOV @1(SP), (SP) :GET EMT
TST (SP) :IS EMT VALID?
BNE EMTOK
HALT :INVALID EMT
EMTOK: ASL (SP) :MULTIPLY EMT ARG BY '2'
BIC #177001,(SP) :CLEAR UNWANTED BITS
ADD #EMTTAB,(SP) :POINTER TO SUBROUTINE ADDRESS
MOV @1(SP), (SP) :SUBROUTINE ADDRESS
JMP @1(SP)+ :GO TO SUBROUTINE

:EMT DISPATCH TABLE

EMTTAB: TYPMES :MESSAGE PRINT ROUTINE
SCOPEI :SCOPE ROUTINE
SCOPEC :LOGIC TEST SCOPE ROUTINE
SCOPEH :LOGIC TEST SCOPE LOOP (10)
XSPACE :SUBROUTINE TO TYPE SPACES
OCTPRY :OCTAL PRINT ROUTINE
XTTYIN :TELEPRINTER SERVICE ROUTINE
TKSFLG :SUBROUTINE TO TEST FOR KEYBOARD FLAG
SCOPEI :SCOPE ROUTINE

:MESSAGE PRINT ROUTINE, ENTERED VIA EMT DISPATCH HANDLER.
:ROUTINE PICKS UP CONTENTS OF THE 'PC' AND USES THIS AS
:THE ADDRESS OF MESSAGE TO BE TYPED.

2500				
2501				
2502				
2503				
2504	012534	000240		
2505	012536	000240		
2506	012540	017605	000000	
2507	012544	062716	000002	
2508	012550	105777	166254	
2509	012554	100375		
2510	012556	122715	000100	
2511	012552	001001		
2512	012564	000002		
2513	012566	122715	000045	
2514	012572	001403		
2515	012574	112577	166232	
2516	012600	000763		
2517	012602	012777	000015	166222
2518	012610	105777	166214	
2519	012614	100375		
2520	012616	012777	000012	166206
2521	012624	013737	001016	012660
2522	012632	105777	166172	
2523	012636	100375		
2524	012640	113777	001020	166164
2525	012646	005337	012660	
2526	012652	100367		
2527	012654	105725		
2528	012656	000734		
2529	012660	000000		
2530				
2531				
2532				
2533				
2534	012662	000240		
2535	012664	000240		
2536	012666	017605	000000	
2537	012672	062716	000002	
2538	012676	012737	000006	012776
2539	012704	012737	000376	013002
2540	012712	000401		
2541	012714	006115		
2542	012716	006115		
2543	012720	006115		
2544	012722	111537	013000	
2545	012726	143737	013002	013000
2546	012734	052737	000260	013000
2547	012742	132777	000200	166060
2548	012750	100374		
2549	012752	113777	013000	166052
2550	012760	012737	000370	013002
2551	012766	005337	012776	
2552	012772	001350		
2553	012774	000002		
2554	012776	000000		
2555	013000	000000		

```

TYPMES: NOP
          NOP
          MOV      2(SP),R5      ;GET THE MESSAGE ADDRESS FROM START
          ADD      #2,(SP)      ;SET UP STACK TO EXIT
TYPERA:  TSTB    2TPS
          BPL      TYPERA      ;WAIT FOR TTY DONE
          CMPB    #100,(R5)    ;TEST FOR '2'
          BNE     TYPERA1     ;BRANCH IF NO EQUAL
          RTI      ;OTHERWISE EXIT
TYPERA1: CMPB    #45,(R5)     ;TEST FOR '%'
          BEQ     TYPECL     ;IF = TYPE 'CR-LF'
TYPERA2: MOVVB   (R5)+,2TPB   ;OUTPUT CHAR.
          BR      TYPERA
TYPECL:  MOV     #15,2TPB    ;TYPE 'CR'
          TSTB   2TPS
          BPL    #-4
          MOV    #12,2TPB
          MOV    FILL5,2S    ;LOAD COUNTER
1S:      TSTB   2TPS        ;TEST FLAG
          BPL   1S
          MOVB  FILCHR,2TPB ;LOAD FILLER CHARACTER
          DEC   2S          ;DONE
          BPL   1S
          TSTB (R5)+      ;INCREMENT BUFFER
          BR   TYPERA
2S:      0

```

:SUBROUTINE TO TYPEOUT A '6' DIGIT OCTAL NO. THE 'PC' CONTAINS
:THE ADDRESS OF 'WORD' TO BE TYPED

```

OCTPRT: NOP
          NOP
          MOV      2(SP),R5      ;THE ADDRESS OF WORD TO BE TYPED
          ADD      #2,(SP)      ;SET UP STACK TO EXIT
          MOV      #6,10S
          MOV      #376,MASK    ;MASK FOR FIRST BIT
          BR      .+4
1S:      ROL      (R5)
          ROL      (R5)
          ROL      (R5)
          MOVVB   (R5),11S
          BICB    MASK,11S
          BIS     #260,11S
          BITB    #200,2TPS
          BPL    #-6          ;WAIT FOR PRINTER READY
          MOVVB   11S,2TPB    ;PRINT CHAR.
          MOV     #370,MASK    ;MASK FOR NEXT '5' DIGITS
          DEC     10S
          BNE     1S
          RTI
10S:     0
11S:     0

```

2556	013002	000376		
2557				
2558	013004	105777	166014	
2559	013010	100001		
2560	013012	104006		
2561	013014	000002		
2562				
2563				
2564	013016	104007		
2565	013020	037727	166010	020000
2566	013026	001125		
2567	013030	012737	013314	000004
2568	013036	011637	014462	
2569	013042	162737	000002	014462
2570	013050	004537	013524	
2571	013054	014462		
2572	013056	017737	165766	014470
2573	013064	017737	165762	014472
2574	013072	017737	165756	014474
2575	013100	017737	165754	014476
2576	013106	017737	165744	014500
2577	013114	017737	165742	014464
2578	013122	017737	165736	014466
2579	013130	017737	165732	014504
2580	013136	013737	014506	014502
2581	013144	012737	000006	000004
2582	013152	005737	014442	
2583	013156	001006		
2584	013160	104000		
2585	013162	014411		
2586	013164	104000		
2587	013166	013723		
2588	013170	005237	014442	
2589	013174	104000		
2590	013176	014411		
2591	013200	104005		
2592	013202	014462		
2593	013204	104004		
2594	013206	104005		
2595	013210	014470		
2596	013212	104004		
2597	013214	104005		
2598	013216	014472		
2599	013220	104004		
2600	013222	104005		
2601	013224	014474		
2602	013226	104004		
2603	013230	104005		
2604	013232	014476		
2605	013234	104004		
2606	013236	104005		
2607	013240	014500		
2608	013242	104004		
2609	013244	104005		
2610	013246	014464		
2611	013250	104004		

```

MASK: 376
:SUBROUTINE TO TEST FOR THE KEYBOARD FLAG BEING SET
TKSFLG: TSTB      JTKS      :FLAG SET?
          BPL      .+4      :NO, EXIT
          TTYIN     :YES, INQUIRE
          RTI

:ENTERED WITH SYSTEM TRAP CALL (ERROR)
LOGERR: TSTTKS      :TEST FOR KEYBOARD INTERRUPT
          BIT        @SWR, #20000 :TEST FOR INHIBIT PRINT OUT
          BNE        CK          :INHIBIT, CHECK FOR HALT
          MOV        @LGERR2, @#4 :SET UP FOR BUSS ERROR
          MOV        (SP), KSTOR3 :PC OF FAILING ROUTINE
          SUB        #2, KSTOR3
          JSR        S, LEDS
          KSTOR3
          MOV        @CSR, KSTOR6  :SAVE CLOCK STATUS
          MOV        @CSB, KSTOR7  :SAVE CLOCK PRESET
          MOV        @GRSTAT, KSTOR8 :SAVE I/O STATUS
          MOV        @GRDIO, KSTOR9 :SAVE I/O OUTPUT
          MOV        @GRDAI, KSTR10 :SAVE I/O INPUT
          MOV        @VCSTAT, KSTOR4 :SAVE VC STATUS
          MOV        @VCXREG, KSTOR5 :SAVE X AXIS
          MOV        @VCYREG, KSTR12 :SAVE Y AXIS
          MOV        TEMP, KSTR11  :SAVE TEMP
          MOV        #6, @#4      :RESET BUSS ERROR
          TST        PRINT1
          BNE        LGERR1
          PRINT
          CRLF
          PRINT
          MESI
          INC        PRINT1
LGERR1: PRINT        :OUTPUT CARRIAGE RETURN AND LINE FEED
          CRLF
          PRTOCT
          KSTOR3
          SPACE
          PRTOCT
          KSTOR6
          SPACE
          PRTOCT
          KSTOR7
          SPACE
          PRTOCT
          KSTOR8
          SPACE
          PRTOCT
          KSTOR9
          SPACE
          PRTOCT
          KSTR10
          SPACE
          PRTOCT
          KSTOR4
          SPACE

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2612 013252 104005 PRT0CT
2613 013254 014466 KSTORS
2614 013256 104004 SPACE
2615 013260 104005 PRT0CT
2616 013262 014504 KSTR12
2617 013264 104004 SPACE
2618 013266 104005 PRT0CT
2619 013270 014502 KSTR11
2620 013272 104004 SPACE
2621 013274 105777 165530 TSTB @TPS
2622 013300 100375 BPL -4
2623 013302 005777 165526 CK: TST @SWR ;CHECK SR FOR HALT SWITCH
2624 013306 100001 SPL .+4 ;BRANCH IF NOT SET
2625 013310 000000 HALT ;HALT ON ERROR UP
2626 013312 000002 RTI ;RETURN TO MAIN LINE
2627 013314 062716 000002 LGERR2: ADD #2.(SP)
2628 013320 000002 RTI
2629
2630
2631 ;SCOPE AND/OR ITERATION LOOP FOR SOME TEST 4000 TIMES
2632
2633 013322 104007 SCOPEC: TSTTKS ;TEST FOR KEYBOARD INIT
2634 013324 032777 040000 165502 BIT #40000,@SWR ;TEST SR FOR SCOPE
2635 013332 001015 BNE SCOPEB ;YES SCOPE
2636 013334 032777 004000 165472 BIT #4000,@SWR ;NO-TEST FOR ITERATION
2637 013342 001016 BNE SCOPEG ;INHIBIT ITERATION
2638 013344 005737 001040 TST PASSCT ;TEST IF FIRST PASS
2639 013350 001413 BEQ SCOPEG ;BR IF FIRST PASS -- QUICKK PASS
2640 013352 023737 013412 001042 CMP SCOPEF,ICOUNT ;COMPARE CURRENT COUNT TO MAX NUMBER
2641 013360 001407 SCOPEJ: BEQ SCOPEG ;EXIT-DONE
2642 013362 005237 013412 INC SCOPEF ;INCREMENT COUNT
2643 013366 022606 SCOPEB: CMP (6)+,SP ;REPOSITION STACK
2644 013370 012677 165426 MOV (6)+,@PSW ;RESTORE PREVIOUS PROCESSOR STATUS
2645 013374 000177 000014 JMP @RETURN ;REPEAT TEST
2646 013400 005037 013412 SCOPEG: CLR SCOPEF ;CLEAR COUNT
2647 013404 011637 013414 MOV @SP,RETURN ;SAVE SCOPE RETURN POINTER
2648 013410 000002 RTI ;RETURN INLINE-NEXT TEST
2649 013412 000000 SCOPEF: 0 ;COUNT LOCATION FOR ITERATION LOOP
2650 013414 002130 RETURN: KWTO ;ADDRESS OF LAST TEST
2651
2652 ;SCOPE AND/OR INTERATION LOOP FOR SOME TESTS 10 TIMES
2653
2654 013416 104007 SCOPEH: TSTTKS
2655 013420 032777 040000 165406 BIT #40000,@SWR
2656 013426 001357 BNE SCOPEB
2657 013430 032777 004000 165376 BIT #4000,@SWR
2658 013436 001360 BNE SCOPEG
2659 013440 005737 001040 TST PASSCT ;TEST IF FIRST PASS
2660 013444 001755 BEQ SCOPEG ;BR IF YES
2661 013446 023727 013412 000010 CMP SCOPEF,#10
2662 013454 000741 BR SCOPEJ
2663
2664 ;SCOPE LOOP FOR SOME TEST 1 TIME
2665
2666 013456 104007 SCOPEI: TSTTKS ;TEST KEYBOARD
2667 013460 032777 040000 165346 BIT #40000,@SWR

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2668 013466 001337          BNE      SCOPEB
2669 013470 000743          BR       SCOPEG
2670
2671 013472 104000          BELL:    PRINT
2672 013474 013504          ENDPAS
2673 013476 104000          BELLA:   PRINT
2674 013500 013521          RING
2675 013502 000207          RTS      PC           :EXIT
2676
2677 013504 042445 042116 050040 ENDPAS:  .ASCII  '%END PASS  @'
2678 013512 051501 020123 020040
2679 013520 100
2680 013521 007      007      100 RING:    .BYTE  7,7,100
2681          .EVEN
2682
2683
2684          ;: LAC: THE LPS DISPLAY LIGHTS
2685
2686 013524 012737 000006 013632 LEDS:    MOV      #6,CNTLED
2687 013532 005037 013640          CLR      LEDSV3
2688 013536 013537 013634          MOV      @5+,LEDSV1
2689 013542 005737 013642          TST      NOLEDS
2690 013546 001401          BEQ      LEDSA
2691 013550 000205          RTS
2692 013552 013737 013634 013636 LEDSA:   MOV      LEDSV1,LEDSV2
2693 013560 042737 177770 013636          BIC      #177770,LEDSV2
2694 013566 113737 013640 013637          MOVB    LEDSV3,LEDSV2+1
2695 013574 013777 013636 165244          MOV      LEDSV2,@ADDBR
2696 013602 006237 013634          ASR      LEDSV1
2697 013606 006237 013634          ASR      LEDSV1
2698 013612 006237 013634          ASR      LEDSV1
2699 013616 005237 013640          INC      LEDSV3
2700 013622 005337 013632          DEC      CNTLED
2701 013626 001351          BNE      LEDSA
2702 013630 000205          RTS      S
2703
2704 013632 000006          CNTLED:  6
2705 013634 000000          LEDSV1:  0
2706 013636 000000          LEDSV2:  0
2707 013640 000000          LEDSV3:  0
2708 013642 000000          NOLEDS:  0
2709

```

Line	Code 1	Code 2	Code 3	Code 4	Code 5	Message
2710						
2711						:MESSAGES
2712	013644	022445	046045	051520		TITLE: .ASCII '%%LPS DIAGNOSTIC TEST II (MAINDEC-11-DZLPC-C)'
2713	013652	042040	040511	047107		
2714	013660	051517	044524	020103		
2715	013666	042524	052123	044440		
2716	013674	020111	046450	044501		
2717	013702	042116	041505	030455		
2718	013710	026461	055104	050114		
2719	013716	026504	024503	100		
2720						
2721	013723	040	050040	020103	MES1:	.ASCII " PC "
2722	013730	020040				
2723	013732	045503	052123	052101		.ASCII "CKSTAT "
2724	013740	040				
2725	013741	103	041113	043125		.ASCII "CKBUFF "
2726	013746	020106				
2727	013750	047511	052123	052101		.ASCII "IOSTAT "
2728	013756	040				
2729	013757	111	026517	052517		.ASCII "IO-OUT "
2730	013764	020124				
2731	013766	044440	026517	047111		.ASCII " IO-IN "
2732	013774	040				
2733	013775	126	051503	040524		.ASCII "VCSTAT "
2734	014002	020124				
2735	014004	041526	040530	051530		.ASCII "VCXAXS "
2736	014012	040				
2737	014013	126	054503	054101		.ASCII "VCYAXS "
2738	014020	020123				
2739	014022	052040	046505	040120		.ASCII " TEMP "
2740						
2741	014030	021045	046103	041517	MES2:	.ASCII "'CLOCK LOGIC TEST' "
2742	014036	020113	047514	044507		
2743	014044	020103	042524	052123		
2744	014052	022442	100			
2745	014055	045	042042	043511	MES3:	.ASCII "'DIGITAL I/O LOGIC TEST' "
2746	014062	052111	046101	044440		
2747	014070	047457	046040	043517		
2748	014076	041511	052040	051505		
2749	014104	021124	040045			
2750	014110	021045	041523	050117	MES5:	.ASCII "'SCOPE LOGIC TEST' "
2751	014116	020105	047514	044507		
2752	014124	020103	042524	052123		
2753	014132	022442	100			
2754	014135	045	053042	051511	MES6:	.ASCII "'VISUAL DISPLAY TEST' "
2755	014142	040525	020114	044504		
2756	014150	050123	040514	020131		
2757	014156	042524	052123	022442		
2758	014164	100				
2759	014165	045	054524	042520	MES4:	.ASCII "'TYPE LETTER ' ' TO RUN DESIRED TEST:' "
2760	014172	046040	052105	042524		
2761	014200	020122	020047	020047		
2762	014206	047524	051040	047125		
2763	014214	042040	051505	051111		
2764	014222	042105	052040	051505		
2765	014230	035124	045			

2766	014233	047	023501	041475	.ASCII	''A'=CLOCK LOGIC%''
2767	014240	047514	045503	046040		
2768	014246	043517	041511	045		
2769	014253	047	023502	041475	.ASCII	''B'=I/O LOGIC%''
2770	014260	047457	046040	043517		
2771	014266	041511	045			
2772	014271	047	023503	051475	.ASCII	''C'=SCOPE CONTROL LOGIC%''
2773	014276	047503	042520	041440		
2774	014304	047117	051124	046117		
2775	014312	046040	043517	041511		
2776	014320	045				
2777	014321	047	023504	053075	.ASCII	''D'=VISUAL SCOPE DISPLAY%''
2778	014326	051511	040525	020114		
2779	014334	041523	050117	020105		
2780	014342	044504	050123	040514		
2781	014350	022531	100			
2782						
2783	014353	136	022503	100	CNTRLC: .ASCII	'%a'
2784						
2785	014357	136	040101		CNTRLA: .ASCII	'%a'
2786	014362	043536	047445	042114	CNTRLG: .ASCII	'%OLD SWR = a'
2787	014370	051440	051127	036440		
2788	014376	040040				
2789	014400	020040	042516	020127	NEWSWR: .ASCII	' NEW = a'
2790	014406	020075	100			
2791						
2792	014411	045	100		CRLF: .ASCII	'%a'
2793						
2794	014413	045	040056		COT: .ASCII	'%.a'
2795						
2796	014416	020077	100		GMARK: .ASCII	'? a'
2797	014421	045	047520	042527	MES21: .ASCII	'%POWER FAILURE a'
2798	014426	020122	040506	046111		
2799	014434	051125	020105	100		
2800						
2801		014442			.EVEN	
2802						
2803						

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014534 000005
014536 104000
014540 014135
014542 005037 001040
014546 013706 014444
014552 013777 001040 164256
014550 012737 014626 013414
014566 005077 164230
014572 042737 000002 015564
014600 032777 000020 164220
014606 001003
014610 052737 000002 015564
014616 052777 000100 164200

014624 013700 001064
014630 013701 001066
014634 004737 014656

014640 013700 001066
014644 013701 001064
014650 004737 014656
014654 000433

014656 005077 164200
014662 013704 001062
014666 012737 000700 014532
014674 004737 017254
014700 012703 007760
014704 013702 014526
014710 012711 004000
014714 012710 000000
014720 060210
014722 005214
014724 105714
014726 100376
014730 021003
014732 001372
014734 004737 017142
014740 000763
014742 000207

```
*****  
: VISUAL DISPLAY TEST  
*****  
VISUAL: RESET  
PRINT  
MES6  
VTEST2: CLR PASSCT  
VSLALO: MOV STACK,SP ;LOAD THE STACK POINTER  
MOV PASSCT,DISPLA ;LOAD PASS COUNT  
MOV #PICO+2,RETURN ;LOAD RETURN ADDRESS  
CLR JPSW  
BIC #BIT1,MODE  
BIT #BIT4,JSWR  
BNE VSLCA  
BIS #BIT1,MODE  
VSLCA: BIS #BIT5,JKS ;ENABLE KEYBOARD  
  
:DISPLAY HORIZONTAL LINE _GING INTERRUPT, NON STORE DISPLAY.  
PICO: MOV VCXREG,R0  
MOV VCYREG,R1  
JSR PC,PBB  
  
:DISPLAY A VERTICAL LINE  
PIC1: MOV VCYREG,R0  
MOV VCXREG,R1  
JSR PC,PBB  
BR PIC3  
  
PBB: CLR JVCSTAT  
MOV VCSTAT,R4  
MOV #700,TICKS  
JSR PC,CHTIME ;CHECK TIMER  
PB: MOV #7760,R3 ;SET HIGH LIMIT  
PD: MOV INCR,R2 ;INITIALIZE INCREMENTS BETWEEN POINTS  
PEEA: MOV #4000,(1)  
MOV #0,(0)  
PE: ADD R2,(0) ;INCREMENT  
INC (4) ;INTENSIFY  
TSTB (4)  
BPL #-2  
CMP (0),R3 ;DONE ALL POINTS?  
BNE PE ;NO  
JSR PC,TIMER  
BR PEEA  
RTS PC
```



```

015322 012737 000140 014532 :PLOT NON STORE CHARACTER SET
015330 004737 017254 PIC6: MOV #140,TICKS
015334 012737 170000 015570 PIC6A: JSR PC,CHTIME :CHECK TIME
015342 012737 004000 015566 MOV #170000,XPOS
015350 005077 163506 MOV #4000,YPOS
015354 004737 015372 CLR @VCSTAT
015360 004737 017142 JSR PC,PIC6B
015364 000763 BR PIC6A
015366 000137 016070 JMP PIC7
015372 012737 177734 015572 PIC6B: MOV #-36,CHARCOL :CHARACTERS PER ROW
015400 013705 001062 MOV VCSTAT,R5
015404 012702 015576 MOV #A,R2
015410 004737 015424 GEN1: JSR PC,CHAR
015414 005227 015572 INC CHARCOL
015420 001373 BNE GEN1
015422 000207 RTS PC

015424 013737 015566 015574 :PLOT CHARACTER
015432 042715 000016 CHAR: MOV YPOS,YPT
015436 013777 015570 163420 BIC #16,(5)
015444 013777 015566 163414 MOV XPOS,@VCXREG
015452 105777 163404 MOV YPOS,@VCYREG
015456 100375 CHAR4: TSTB @VCSTAT
015460 053715 015564 BIS MODE,(5) :ENABLE FAST INTENSIFY ON LOADING Y
015464 012704 000020 MOV #20,R4
015470 012700 177773 MOV #-5,R0
015474 012701 177771 CHAR1: MOV #-7,R1
015500 112203 MOVB (2)+,R3 :INITIALIZE COLUMN COUNT
015502 106103 CHAR2: ROLB R3 :INITIALIZE ROW COUNT
015504 100006 BPL CHAR3 :PUT CHARACTER POINTS IN R3
015506 013777 015570 163350 MOV XPOS,@VCXREG :NO
015514 013777 015566 163344 MOV YPOS,@VCYREG
015522 105777 163334 CHAR3: TSTB @VCSTAT
015526 100375 BPL CHAR3
015530 060437 015566 ADD R4,YPOS
015534 005201 INC R1 :+1 TO ROW
015536 001361 BNE CHAR2 :FINISH ROW
015540 013737 015574 015566 MOV YPT,YPOS :REINITIALIZE ROW FOR NEXT COLUMN
015546 060437 015570 ADD R4,XPOS
015552 005200 INC R0 :+1 TO COLUMN COUNT
015554 001347 BNE CHAR1
015556 060437 015570 ADD R4,XPOS
015562 000207 RTS PC :EXIT

015564 000010 MODE: 10
015566 000000 YPOS: 0 :CONTAINS Y POSITION AT ANY GIVEN TIME
015570 000000 XPOS: 0 :CONTAINS X POSITION AT ANY GIVEN TIME
015572 000000 CHARCOL: 0
015574 000000 YPT: 0

```

3023						
3024	015576	176	021	021	A:	.BYTE 176,21,21,21,176
3025	015501	021	176			
3026	015603	177	111	111	B:	.BYTE 177,111,111,111,66
3027	015506	111	056			
3028	015510	076	101	101	C:	.BYTE 76,101,101,101,42
3029	015513	101	042			
3030	015515	177	101	101	D:	.BYTE 177,101,101,101,76
3031	015520	101	076			
3032	015522	177	111	111	E:	.BYTE 177,111,111,111,101
3033	015525	111	101			
3034	015527	177	011	011	F:	.BYTE 177,11,11,11,1
3035	015532	011	001			
3036	015534	076	101	121	G:	.BYTE 76,101,121,121,62
3037	015537	121	062			
3038	015541	177	010	010	H:	.BYTE 177,10,10,10,177
3039	015544	010	177			
3040	015546	000	101	177	I:	.BYTE 0,101,177,101,0
3041	015551	101	000			
3042	015552	060	100	100	J:	.BYTE 60,100,100,100,77
3043	015556	100	077			
3044	015560	177	010	024	K:	.BYTE 177,10,24,42,101
3045	015563	042	101			
3046	015565	177	100	100	L:	.BYTE 177,100,100,100,100
3047	015570	100	100			
3048	015572	177	004	010	M:	.BYTE 177,4,10,4,177
3049	015575	004	177			
3050	015577	177	004	010	N:	.BYTE 177,4,10,20,177
3051	015702	020	177			
3052	015704	076	101	101	O:	.BYTE 76,101,101,101,76
3053	015707	101	076			
3054	015711	177	011	011	P:	.BYTE 177,11,11,11,6
3055	015714	011	006			
3056	015716	076	101	121	Q:	.BYTE 76,101,121,141,176
3057	015721	141	176			
3058	015723	177	011	031	R:	.BYTE 177,11,31,51,106
3059	015726	051	106			
3060	015730	046	111	111	S:	.BYTE 46,111,111,111,62
3061	015733	111	062			
3062	015735	001	001	177	T:	.BYTE 1,1,177,1,1
3063	015740	001	001			
3064	015742	077	100	100	U:	.BYTE 77,100,100,100,77
3065	015745	100	077			
3066	015747	037	040	100	V:	.BYTE 37,40,100,40,37
3067	015752	040	037			
3068	015754	177	020	010	W:	.BYTE 177,20,10,20,177
3069	015757	020	177			
3070	015761	143	024	010	X:	.BYTE 143,24,10,24,143
3071	015764	024	143			
3072	015766	003	004	170	Y:	.BYTE 3,4,170,4,3
3073	015771	004	003			
3074	015773	141	121	111	Z:	.BYTE 141,121,111,105,103
3075	015776	105	103			
3076	016000	000	102	177	N1:	.BYTE 0,102,177,100,0
3077	016003	100	000			
3078	016005	142	121	111	N2:	.BYTE 142,121,111,105,102

F06

PS DIAGNOSTIC TEST II MAINDEC-11-DZLPO-C
DZLPOC.P11 04-APR-76 00:00

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016010	105	102			
016012	042	101	111	N3:	.BYTE 42,101,111,111,66
016013	111	066			
016014	030	024	022	N4:	.BYTE 30,24,22,177,20
016022	177	020			
016024	047	105	105	N5:	.BYTE 47,105,105,105,71
016027	105	071			
016031	076	111	111	N6:	.BYTE 76,111,111,111,62
016034	111	062			
016036	101	041	021	N7:	.BYTE 101,41,21,11,7
016041	011	007			
016043	066	111	111	N8:	.BYTE 66,111,111,111,66
016046	111	066			
016050	046	111	111	N9:	.BYTE 46,111,111,111,76
016053	111	076			
016055	076	121	111	N0:	.BYTE 76,121,111,105,76
016060	055	076			
016062	030	000	000	SPACER:	.BYTE 0,0,0,0,0
016065	000	000			

016070

.EVEN

3100					:CHANNEL 1 CHANNEL 2	
3101	016070	012737	000300	014532	PIC7: MOV	#300,TICKS ;SET UP A TIMER
3102	016076	004737	017254		JSR	PC,CHTIME ;CHECK TIMER
3103	016102	013705	001062		MOV	VCSTAT,R5 ;SET UP R5 FOR STATUS REGISTER POINTER
3104	016106	012777	000000	162746	PIC7AA: MOV	#0,AVCSTAT ;SET UP SCOPE CONTROL
3105	016114	012737	003000	015570	MOV	#3000,XPOS ;LOAD X POSITION
3106	016122	012737	005000	015566	MOV	#5000,YPOS ;LOAD Y POSITION
3107	016130	012737	000011	016264	MOV	#9,P7CNT ;SAVE THE NUMBER OF CHARACTERS
3108	016136	012737	016270	016266	MOV	#CH1,P7PNT ;SAVE CHANNEL 1 POINTER
3109	016144	017702	000116		PIC7A: MOV	#P7PNT,R2 ;MOVE MESSAGE POINTER INTO R2 FOR DISPLAY ROUTINE
3110	016150	004737	015424		JSR	PC,CHAR ;DISPLAY A CHARACTER
3111	016154	062737	000002	016266	ADD	#2,P7PNT ;ADD 2 TO THE MESSAGE POINTER
3112	016162	005337	016264		DEC	P7CNT ;DECREMENT CHARACTER COUNT
3113	016166	001366			BNE	PIC7A ;NOT FINISHED WITH ALL CHARACTERS
3114	016170	012777	001000	162664	MOV	#1000,AVCSTAT
3115	016176	012737	003000	015570	MOV	#3000,XPOS ;SET UP X POS FOR CHANNEL 2
3116	016204	012737	003000	015566	MOV	#3000,YPOS ;SET UP Y
3117	016212	012737	000011	016264	MOV	#9,P7CNT ;SET UP CHARACTER COUNT
3118	016220	012737	016312	016266	MOV	#CH2,P7PNT ;SET UP CHANNEL 2 POINTER
3119	016226	017702	000034		PIC7B: MOV	#P7PNT,R2 ;SET UP
3120	016232	004737	015424		JSR	PC,CHAR ;DISPLAY A CHARACTER
3121	016236	062737	000002	016266	ADD	#2,P7PNT ;ADD 2 TO THE POINTER
3122	016244	005337	016264		DEC	P7CNT ;DECREMENT COUNT
3123	016250	001366			BNE	PIC7B ;NOT FINISHED
3124	016252	004737	017142		JSR	PC,TIMER ;CHECK THE RUNTIME OF THIS ROUTINE
3125	016256	000713			BR	PIC7AA ;NOT FINISHED
3126	016260	000137	016334		JMP	PIC100 ;FINISHED, NEXT TEST
3127	016264	000000			P7CNT: 0	
3128	016266	000000			F7PNT: 0	
3129	016270	015610			CH1: C	
3130	016272	015641			H	
3131	016274	015576			A	
3132	016276	015677			N	
3133	016300	015677			N	
3134	016302	015622			F	
3135	016304	015665			L	
3136	016306	016062			SPACEA	
3137	016310	016000			N1	
3138	016312	015610			CH2: C	
3139	016314	015641			H	
3140	016316	015576			A	
3141	016320	015677			N	
3142	016322	015677			N	
3143	016324	015622			F	
3144	016326	015665			L	
3145	016330	016062			SPACEA	
3146	016332	016000			N2	
3147						

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3148
3149
3150 :COLOR PINCUSHION-COLORS SHOULD OVERLAY TO BECCME ORANGE
3151 :DRAW A BOX AROUND THE SCREEN AND A "X" IN THE CENTER
3152 :DRAW IN GREEN THEN IN RED
3153
3154 016334 005005 PIC100: CLR R5 ;SET UP FOR COLOR PATTERN
3155 016336 012737 000240 014532 MOV #240,TICKS
3156 016344 004737 017254 JSR PC,CHTIME ;CHECK TIMER
3157 016350 013701 001064 PIC10: MOV VCXREG,R1
3158 016354 013702 001066 MOV VCYREG,R2
3159 016350 013703 001062 MOV VCSTAT,R3
3160 016364 012704 000100 MOV #100,R4
3161 016370 012777 000000 152466 PIC10A: MOV #0,VCXREG
3162 016376 012777 000000 162462 MOV #0,VCYREG
3163 016404 105713 TSTB (3) ;TEST CONTROL FOR READY
3164 016406 100376 BPL -2
3165 ;BOTTOM LINE
3166 016410 012713 000004 MOV #4,(3) ;SET UP MODE
3167 016414 050513 BIS R5,(3) ;SET UP COLOR BIT
3168 016416 012700 000077 MOV #77,R0
3169 016422 105713 PIC10B: TSTB (3) ;CHANGE IN COLOR. WAIT FOR DONE
3170 016424 100376 BPL -2
3171 016426 060411 ADD R4,(1) ;ADD R4 TO XPOS
3172 016430 005300 DEC R0
3173 016432 001373 BNE PIC10B ;NO
3174 016434 105713 TSTB (3) ;WAIT FOR LAST DOT
3175 016436 100376 BPL -2
3176 ;RIGHT LINE
3177 016440 112713 000010 MOVB #10,(3) ;CHANGE MODE
3178 016444 050513 BIS R5,(3) ;COLOR BIT
3179 016446 012700 000077 MOV #77,R0
3180 016452 105713 PIC10C: TSTB (3) ;WAIT
3181 016454 100376 BPL -2
3182 016456 060412 ADD R4,(2) ;ADD R4 TO YPOS
3183 016460 005300 DEC R0
3184 016462 001373 BNE PIC10C ;NO
3185 016464 105713 TSTB (3) ;WAIT FOR LAST DOT
3186 016466 100376 BPL -2
3187 ;TOP LINE
3188 016470 112713 000004 MOVB #4,(3) ;CHANGE MODE
3189 016474 050513 BIS R5,(3) ;COLOR BIT
3190 016476 012700 000077 MOV #77,R0
3191 016502 105713 PIC10D: TSTB (3) ;READY
3192 016504 100376 BPL -2
3193 016506 160411 SUB R4,(1) ;SUB R4 FROM XPOS
3194 016510 005300 DEC R0
3195 016512 001373 BNE PIC10D ;NO
3196 016514 105713 TSTB (3) ;WAIT FOR LAST DOT
3197 016516 100376 BPL -2
3198 ;LEFT LINE
3199 016520 112713 000010 MOVB #10,(3) ;CHANGE MODE
3200 016524 050513 BIS R5,(3) ;COLOR BIT
3201 016526 012700 000077 MOV #77,R0
3202 016532 105713 PIC10E: TSTB (3) ;READY
3203 016534 100376 BPL -2

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3204	016536	160412		SUB	R4,(2)	:SUB R4 FROM YPOS
3205	016540	005300		DEC	RO	
3206	016542	001372		BNE	PIC10E	:NO
3207	016544	105713		TSTB	(3)	:WAIT FOR LAST DOT
3208	016546	100376		BPL	.-2	
3209						
3210						
3211	016550	105013				
3212	016552	012704	000040	PIC11: CLRB	(3)	:CLEAR CONTROL
3213	016556	012712	002000	MOV	#40,R4	:SET UP R4
3214	016562	011211		MOV	#2000,(2)	:SET UP Y POS
3215	016564	112713	000004	MOV	(2),(1)	:SET UP X POS
3216	016570	050513		MOV	#4,(3)	:SET UP CONTROL
3217	016572	012700	000100	BIS	R5,(3)	:COLOR BIT
3218	016576	105713		MOV	#100,RO	
3219	016600	100376		PIC11A: TSTB	(3)	:WAIT FOR READY
3220	016602	060412		BPL	.-2	
3221	016604	060411		ADD	R4,(2)	:ADD R4 TO YPOS
3222	016606	005300		ADD	R4,(1)	:ADD R4 TO XPOS
3223	016610	001372		DEC	RO	
3224	016612	105713		BNE	PIC11A	:NO
3225	016614	100376		TSTB	(3)	
3226	016616	012712	006000	BPL	.-2	
3227	016622	012711	002000	MOV	#6000,(2)	:CHANGE Y POS
3228	016626	012700	000100	MOV	#2000,(1)	:CHANGE X POS
3229	016632	105713		MOV	#100,RO	
3230	016634	100376		PIC11B: TSTB	(3)	:READY
3231	016636	160412		BPL	.-2	
3232	016640	060411		SUB	R4,(2)	:SUB R4 FROM YPOS
3233	016642	005300		ADD	R4,(1)	:ADD R4 TO XPOS
3234	016644	001372		DEC	RO	
3235	016646	105713		BNE	PIC11B	:NO
3236	016650	100376		TSTB	(3)	:WAIT FOR LAST POINT
3237	016652	032705	000400	BPL	.-2	
3238	016656	001006		BIT	#400,R5	:TEST COLOR BIT
3239	016660	052705	001400	BNE	PIC11C	
3240	016664	005013		BIS	#1400,R5	
3241	016666	105713		CLR	(3)	
3242	016670	100376		TSTB	(3)	
3243	016672	000626		BPL	.-2	
3244	016674	005005		BR	PIC10	
3245	016676	005013		PIC11C: CLR	R5	
3246	016700	105713		CLR	(3)	
3247	016702	100376		TSTB	(3)	
3248	016704	004737	017142	BPL	.-2	
3249	016710	000617		JSR	PC_TIMER	:HAS TIME EXPIRED ?
3250				BR	PIC10	

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3251
3252
3253 ;PHOSPHOR AND ERASE TEST
3254 016712 012737 000002 014532 PIC12: MOV #2,TICKS
3255 016720 004737 017254 JSR PC,CHTIME ;CHECK TIMER
3256 016724 004737 016776 PIC12A: JSR PC,CLAVC ;ERASE THE SCREEN
3257 016730 004737 017042 JSR PC,LOADVC ;LOAD THE SCREEN
3258 016734 004737 017142 JSR PC,TIMER ;CHECK THE TIME
3259 016740 000771 BR PIC12A
3260 016742 004737 016776 JSR PC,CLAVC
3261
3262 016746 000005 PIC20: RESET
3263 016750 005737 000042 TST #42
3264 016754 001402 BEQ .+6
3265 016756 000137 002002 JMP WHATE
3266 016762 004737 013472 JSR PC,BELL ;REPORT END OF PASS
3267 016766 005237 001040 INC PASSCT
3268 016772 000137 014546 JMP VSJALO
3269
3270 016776 012777 002000 162056 CLRVC: MOV #BIT10,AVCSTAT ;ENABLE STORE
3271 017004 052777 010000 162050 BIS #BIT12,AVCSTAT ;ERASE THE SCREEN
3272 017012 012700 000020 MOV #20,R0 ;SET UP DELAY
3273 017016 005001 CLR R1
3274
3275 017020 105777 162036 CLRVCA: TSTB AVCSTAT ;TEST FOR READY
3276 017024 100405 BMI CLRVCB ;BRANCH IF SET
3277 017026 005301 DEC R1 ;DELAY
3278 017030 001372 BNE CLRVCA
3279 017032 005300 DEC R0 ;DELAY
3280 017034 001371 BNE CLRVCA
3281 017036 104400 ERROR ;ERROR, ERASE FAILED TO SET READY AFTER A DELAY
3282
3283 017040 000207 CLRVCB: RTS PC
3284
3285 017042 005077 162014 LOADVC: CLR AVCSTAT ;CLEAR STATUS
3286 017046 012737 007777 014510 MOV #7777,TEMP1
3287 017054 013700 001062 MOV VCSTAT,R0
3288 017060 013701 001064 MOV VCXREG,R1
3289 017064 013702 001066 MOV VCYREG,R2
3290 017070 012710 002000 MOV #BIT10,(0) ;SET STORE MODE
3291 017074 013712 014510 MOV TEMP1,(2)
3292 017100 012711 007777 LODVCA: MOV #7777,(1)
3293 017104 000402 BR LODVCC
3294 017106 162711 000010 LODVCB: SUB #10,(1)
3295 017112 005210 LODVCC: INC (0)
3296 017114 000240 NOP
3297 017116 105710 TSTB (0)
3298 017120 100376 BPL .-2
3299 017122 022711 000007 CMP #7,(1)
3300 017126 001367 BNE LODVCB
3301 017130 104007 TSTTKS ;TEST FOR INPUT FLAG
3302 017132 162712 000003 SUB #3,(2)
3303 017136 001360 BNE LODVCA
3304 017140 000207 RTS PC

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3305
3306
3307
3308
3309
3310 017142 017737 161666 014530 TIMER: MOV JSR,TIMSV
3311 017150 104007 TSITKS
3312 017152 032737 000400 014530 TIMERA: BIT #BIT8,TIMSV
3313 017160 001006 BNE TIMER2 ;BIT 8 SET ?
3314 017162 005337 014532 DEC TICKS ;NO. DECREMENT TICKS
3315 017166 001002 BNE TIMER1
3316 017170 062716 000002 ADD #2,(6) ;ADD 2 TO STACK POINTER
3317 017174 000207 TIMER1: RTS PC ;RETURN
3318
3319
3320 ; SWR 8=1 SELECT TEST TO LOCK ON
3321 ; SWR 2-0= TEST NUMBER
3322
3323 017176 042737 177770 014530 TIMER2: BIC #177770,TIMSV
3324 017204 006337 014530 ASL TIMSV
3325 017210 062737 017234 014530 ADD #ROUTPT,TIMSV
3326 017216 017737 175306 014530 MOV #TIMSV,TIMSV
3327 017224 013706 014444 MOV STACK,SP
3328 017230 000177 175274 TIMER4: JMP #TIMSV
3329
3330 017234 014624 POLTPT: PICO ;DISPLAY A HORIZONTAL LINE
3331 017236 014640 PIC1 ;DISPLAY A VERTICAL LINE
3332 017240 014744 PIC3 ;DISPLAY A SQUARE
3333 017242 015150 PIC4 ;DISPALY A "X"
3334 017244 015322 PIC6 ;DISPLAY CHARACTER SET
3335 017246 016070 PIC7 ;DISPLAY CHANNEL TEST
3336 017250 016334 PIC100 ;DISPLAY COLOR PATTERN
3337 017252 016712 PIC12 ;DISPLAY ERASE AND PHOSPHOR TEST
3338 017254 013737 001014 014514 CHTIME: MOV PDPDLY,BRLEVI
3339 017262 005337 014514 CHTMA: DEC BRLEVI
3340 017266 001403 BEQ CHTMB
3341 017270 006337 014532 ASL TICKS
3342 017274 000772 BR CHTMA
3343 017276 000207 CHTMB: RTS PC

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3344                                     :SLOW RELAY SWITCH TEST
3345
3346 017300 013706 014444 RELAY: MOV STACK,SP ;LOAD THE STACK
3347 017304 052777 000401 161542 BIS #BIT8,BIT0,@GRSTAT ;LOAD RELAYS
3348 017312 004737 017332 JSR PC,DLY
3349 017316 042777 000401 161530 BIC #BIT8,BIT0,@GRSTAT ;CLEAR RELAYS
3350 017324 004737 017332 JSR PC,DLY
3351 017330 000763 BR RELAY
3352
3353 017332 013737 001014 014456 DLY: MOV PDPDLY,DELAY
3354 017340 005037 017362 CLR DELAY1
3355 017344 005237 017362 DLYA: INC DELAY1
3356 017350 001375 SNE DLYA
3357 017352 005337 014456 DEC DELAY
3358 017356 001372 BNE DLYA
3359 017360 000207 RTS PC
3360 017362 000000 DELAY1: 0
3361
3362                                     ;SCOPE OUTPUT OF CLOCK OVERFLOW
3363
3364 017364 013706 014444 CKOVFL: MOV STACK,SP
3365 017370 012777 177766 161454 MOV #-10,@CSB ;LOAD COUNTER PRESET
3366 017376 012777 000403 161444 MOV #403,@CSR ;LOAD RATE AND MODE
3367 017404 105777 161440 SOCOA: TSTB @CSR
3368 017410 100375 BPL SOCOA
3369 017412 000764 BR CKOVFL
3370
3371                                     ;TEST FOR SCHMITT TRIGGER #1 AND #2
3372
3373 017414 005037 014510 ST1: CLR TEMP1
3374 017420 042737 100000 017470 BIC #BIT15,STST
3375 017426 000406 BR STSA
3376
3377 017430 012737 001000 014510 ST2: MOV #1000,TEMP1 ;LOAD MODE
3378 017436 052737 100000 017470 BIS #BIT15,STST
3379 017444 013706 014444 STSA: MOV STACK,SP
3380 017450 005037 014462 CLR KSTOR3
3381 017454 013777 014510 161366 STSB: MOV TEMP1,@CSR ;LOAD STATUS
3382 017462 004537 013524 JSR 5,LEDS
3383 017466 014462 KSTOR3
3384
3385 017470 005777 161354 STST: TST @CSR ;TST OR TSTB
3386 017474 100375 BPL STST
3387 017476 005077 161346 CLR @CSR ;CLEAR BIT 15
3388 017502 005237 014462 INC KSTOR3
3389 017506 004737 013476 JSR PC,BELLA
3390 017512 000760 BR STSB
3391
3392
3393 001120 .END INIT

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KWT34A	003676	1121#	1128						
KWT35	003734	1125#	1132#						
KWT36	004016	1148#							
KWT37	004040	1157#							
KWT38	004062	1156#							
KWT39	004104	1175#							
KWT4	002216	785#							
KWT40	004126	1184#							
KWT41	004156	1197#							
KWT42	004214	1210#							
KWT43	004232	1222#							
KWT44	004276	1232#							
KWT45	004322	1242#							
KWT46	004346	1252#							
KWT47	004372	1262#							
KWT48	004430	1276#							
KWT49	004542	1285#	1335#						
KWT5	002246	796#							
KWT50	004630	1323#							
KWT50A	004712	1327#	1341#						
KWT50B	004740	1342#	1348#						
KWT51	004744	1335#	1347#	1354#					
KWT51A	005042	1357#	1370#						
KWT52	005044	1366#	1374#						
KWT53	005136	1391#							
KWT53A	005230	1393#	1404#						
KWT54	005234	1409#							
KWT54A	005326	1411#	1422#						
KWT55	005362	1432#							
KWT56	005406	1444#							
KWT57A	005432	1456#							
KWT6	002270	804#							
KWT60	005456	1468#							
KWT61	005502	1481#							
KWT62	005526	1493#							
KWT7	002312	812#							
KWT8	002334	820#							
L	015665	3046#	3135	3144					
LEDS	013524	669#	2570	2686#	3382				
LEDSA	013552	2690	2692#	2701					
LEDSV1	013634	2688#	2692	2696*	2697*	2699*	2705#		
LEDSV2	013636	2692#	2693*	2694*	2695	2706*			
LEDSV3	013640	2687#	2694	2699*	2707#				
LGERR1	013174	2583	2589#						
LGERR2	013314	2567	2627#						
LOADVC	017042	3257	3285#						
LOADVCA	017100	3292#	3303						
LOADVCB	017106	3294#	3300						
LOADVCC	017112	3293	3295#						
LOGERR	013016	516	2564#						
LOGICA	002012	519	728#						
LOW	014522	2830#	2890*	2898	2899	2935*	2945	2961	
LPSADD	001000	547#	609						
LPSVCT	001002	548#	618						
M	015672	3048#							
MASK	013002	2529*	2545	2550*	2556#				

VCT6	010270	2004#												
VCT7	010312	2012#												
VCT8	010334	2020#												
VCXREG	001064	580#	1949*	2030*	2031	2036*	2037	2058*	2060	2128*	2202*	2304	2578	2855
		2852	2894	2898*	2940	2993*	3004*	3157	3161*	3288				
VCYREG	001066	581#	1950*	2044*	2045	2050*	2051	2059*	2064	2150*	2211*	2313	2579	2856
		2861	2895	2899*	2941	2994*	3005*	3158	3162*	3289				
VISUAL	014534	530	690	2840#										
VSLOA	014616	2850	2852#											
VSJALO	014546	2844#	3268											
VTEST1	010042	723	1938#											
VTEST2	014542	724	2843#											
W	015754	3058#												
WHAT	001632	673	696#	732										
WHATA	001740	707	709	711	715#									
WHATB	001752	716	718#	1509										
WHATC	001764	719	721#	1927										
WHATD	001776	724#	2321											
WHATE	002002	722	725#	3265										
WHATI	002032	699	738#											
WHAT2	002040	701	740#											
WHAT3	002046	703	742#											
X	015761	3070#												
XPOS	015570	2975*	2993	3004	3012*	3015*	3020#	3105*	3115*					
XSPACE	011702	2330#	2334	2494										
XTTYIN	011734	511	2341#	2496										
Y	015766	3072#												
YPOS	015566	2976*	2991	2994	3005	3009*	3011*	3019#	3106*	3116*				
YPT	015574	2991*	3011	3022#										
Z	015773	3074#												
\$BDDAT	006002	1537*	1539	1542	1563#									
\$GDDAT	006000	1535*	1538	1562#										
.	= 017514	507#	510#	513#	518#	520#	522#	546#	672	680	683	686	699	713
		768	774	780	789	799	807	815	823	832	840	848	856	865
		873	876	880	888	891	895	904	916	927	939	951	963	975
		992	1018	1026	1044	1052	1071	1079	1097	1105	1123	1138	1143	1152
		1161	1170	1179	1188	1201	1204	1214	1217	1226	1236	1246	1255	1267
		1271	1280	1283	1308	1311	1333	1346	1366	1383	1398	1402	1403	1420
		1421	1439	1451	1463	1475	1488	1500	1592	1599	1606	1612	1620	1628
		1635	1645	1656	1664	1672	1681	1690	1699	1709	1717	1721	1727	1735
		1741	1751	1762	1845	1848	1877	1912	1926	1957	1966	1974	1982	1991
		1999	2007	2015	2023	2032	2038	2046	2052	2061	2065	2076	2090	2093
		2107	2110	2125	2130	2147	2152	2172	2208	2214	2217	2237	2254	2263
		2285	2296	2305	2314	2320	2331	2389	2441#	2519	2540	2548	2559	2622
		2624	2801#	2877	2905	2913	2921	2929	2952	2958	2964	3099#	3164	3170
		3175	3181	3186	3192	3197	3203	3208	3219	3225	3230	3236	3242	3247
		3264	3298											

. ABS. 017514 000

ERRORS DETECTED: 0
DEFAULT GLOBALS GENERATED: 0

DZLPDC, DZLPDC. SEQ/SOL/CRF/DS:ERFZ/EN:ABS=DSKM:DZLPDC.P11

J07

LPS DIAGNOSTIC TEST II MAINDEC-11-DZLPO-C MACY11 27(1006) 16-SEP-76 21:04 PAGE 88
DZLPOC.P11 04-APR-76 00:00 CROSS REFERENCE TABLE -- USER SYMBOLS

RUN-TIME: 9 23 3 SECONDS
RUN-TIME RATIO: 256 37=5.8
CORE USED: 10K (.19 PAGES)

