

DR11B

DIAGNOSTIC -
MD-11-DZDRB-D

EP-DZDRB-D-DL-A
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FICHE 1 OF 1

NOV 1976
digital
MADE IN USA

This microfiche card contains a grid of frames, each displaying diagnostic data for an MD-11 aircraft. The data is organized into columns and rows, with some frames containing text and others containing graphical representations like bar charts or histograms. The text is small and difficult to read due to the low resolution of the microfiche. The overall layout is a dense grid of information.

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OF THE DRBA ARE CALCULATED AND CHECKED. THERE IS A JSR TO THE NORMAL SUB-ROUTINE BEFORE THIS ROUTINE IS EXITED. THE PROGRAM WILL HALT IF ERROR IS SET, READY IS CLEAR, OR READY AND ERROR ARE CLEAR.

5.2.6 DATCHK

THIS ROUTINE IS ENTERED. CHECK INBUF AFTER A MAINTENANCE MODE OPERATION. THE CONTENTS OF INBUF AND THE CONTENTS OF CHKBUF ARE CHECKED TO SEE THAT THEY ARE THE SAME. THE NUMBER OF COMPARISONS MADE IS DETERMINED BY THE CONTENTS OF BUFLN.

5.2.7 NORMAL

THE ROUTINE IS ENTERED FROM INTA AND FROM SOME TESTS WHICH DON'T USE INTA. THE NUMBER OF THE DRINV+2 IS PUT INTO DRINV AND THE DRYS IS CLEARED. IF THE DR11-B INTERRUPTS UNDER THESE CONDITIONS THE PDP-11 WILL HALT AT DRYS. THE PROCESSOR STATUS WORD IS RESTORED TO LEVEL 7 AND THE ROUTINE IS EXITED.

5.2.8 DATOCK

AFTER A STRING OF DATO'S HAS BEEN COMPLETED THIS ROUTINE CHECKS THAT THE CORRECT DATA PATTERN (52525) WAS TRANSFERRED TO INBUF. THE NUMBER OF COMPARISONS MADE IS DETERMINED BY THE CONTENTS OF BUFLN. AN ADDITIONAL CHECK IS MADE ON BUFLN+2 TO INSURE THAT TOO MANY WORDS WEREN'T TRANSFERRED.

5.2.9 ERRCHK

THIS ROUTINE CLEARS IE AND HALTS IF ERROR IS SET.

5.2.10 TRAPCATCHER

THIS IS A SERIES OF INSTRUCTIONS STARTING AT LOCATION 0 DESIGNED TO DETECT AND ISOLATE UNEXPECTED TRAPS AND INTERRUPTS TO THE TRAP AND INTERRUPT VECTOR AREA OF MEMORY.

EACH VECTOR ENTRANCE ADDRESS IS LOADED WITH THE ADDRESS OF THE NEXT LOCATION. THE NEXT LOCATION IS LOADED WITH A HALT (000000). THUS AN ILLEGAL TRAP OR INTERRUPT WILL CAUSE A HALT AT THE TRAP LOCATION PLUS TWO.

IF A HALT OCCURS IN THE TRAP OR INTERRUPT AREA, EXAMINE REGISTER SIX, IT WILL CONTAIN THE CURRENT STACK ADDRESS. THE CONTENTS OF THE CURRENT STACK ADDRESS IS THE VALUE OF THE LOCATION COUNTER WHEN THE TRAP OR INTERRUPT OCCURRED.

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000001
160000

000240
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104000
000001
000002
000004
000010
000020
000040
000100
000200
000400
001000
002000
004000
010000
020000
040000
100000

000004

000000
000030
000030 011072
000032 000340

```

      .ABS
      .MCALL .HEADER,STARS
*****
*****
:TITLE MAINDEC-11-DZDRB-D
: *COPYRIGHT (C) 1971,1976
: *DIGITAL EQUIPMENT CORP.
: *MAYNARD, MASS. 01754
: *
: *PROGRAM BY POMFRET,JONES.CONDON
: *
: *THIS PROGRAM WAS ASSEMBLED USING THE PDP-11 MAINDEC SYSMAC
: *PACKAGE (MAINDEC-11-DZQAC-C2), SEPT 14, 1976.
: *
$TN=1
$SWR=160000 ;:HALT ON ERROR, LOOP ON TEST, INHIBIT ERROR TYP0UT
*****
:REVIS0 BY ALAN BOSTICK JUNE 1976
:MODIFIED FOR SOFTWARE SWITCH REGISTER
:INCLUDING DYNAMIC LOADING OF SWR
*****
*****

```

```

NOP=000240
SCOPE=TRAP
HLT=EMT
BIT0=000001
BIT1=000002
BIT2=000004
BIT3=000010
BIT4=000020
BIT5=000040
BIT6=000100
BIT7=000200
BIT8=000400
BIT9=001000
BIT10=002000
BIT11=004000
BIT12=010000
BIT13=020000
BIT14=040000
BIT15=100000

BUSERR=000004

;LOAD TRAP CATCHER INTO 0 THRU 777.

.=0
.=30
PRINT
340

```

```

000034 011650
000036 000340
000176 000176
000000 000000
000200 012706 013566
000204 005077 000604
000210 005002
000212 012702 012433
000216 004767 012240
000222 012702 012403
000226 004767 012230
000232 000167 000634
001000

```

```

.=34
SCOPEC
340
.=176
SWREG: 0
.=200
MOV #BUFF,%6 ;SET UP STACK LIMIT
CLR @PSW
CLR %2
MOV #SHEAD,%2
JSR %7,TTOUT
MOV #SMAIN,%2
JSR %7,TTOUT
JMP SUSWR
.=1000

```

```

:*****
: START OF BACK-TO-BACK DR11-B
:*****

```

```

001000 000402
001002 000167 006276
001006 000167 006212
001012 177570
001014 177776
001016 172410
001020 172412
001022 172414
001024 172416
001026 000126
001030 000240
001032 000124
001034 052525
001036 173000
001040 013570
001042 014572
001044 000000
001046 000000
001050 000000
001052 000000
001054 000000
001056 177560
001060 177562
001062 177564
001064 177566
001066 000000
001070 000000
001072 013746 000006
001076 013746 000004
001102 012737 001122 000004
001110 022777 177777 177574
001116 001402
001120 000404

```

```

MSTART: BR MSX ;MASTER START
SSTART: JMP SSI ;SLAVE START
MSX: JMP MSI
SR: 177570
PSW: 177776
DRWC: 172410
CRBA: 172412
DRST: 172414
DRDB: 172416
DRVS: 126
DRINL: 240
DRINV: 124
NPR1: 52525
DIOMEM: 173000
INBUF: XINBUF
CHKBUF: XCHKBU
BUFLN: HALT
LENCHK: HALT
BRWAIT: HALT
WLEN: HALT
RDYCHK: HALT
TKS: 177560
TKB: 177562
TPS: 177564
TPB: 177566
FNCCNT: HALT
INBUF1: HALT

```

```

SUSWR: MOV @#6,-(SP) ;SAVE VECTORS
MOV @#4,-(SP)
MOV #64,@#4 ;SET UP FOR TIMEOUT
CMP #-1,@SR ;REFERENCE HARDWARE SWITCH REGISTER
BEQ 65$
BR 66$

```

```

546 001122 022626          645:  CMP      (SP)+,(SP)+      ;ADJUST STACK
547 001124 012767 000176 177660 655:  MOV      #SWREG,SR      ;POINT TO SOFTWARE SWITCH REG
548 001132 012637 000004          665:  MOVL    (SE)+,R#4      ;RESTORE VECTORS
549 001136 012637 000006          MOV      (SP)+,R#6
550 001142 022767 000176 177642  CMP      #SWREG,SR      ;IS S. IREG USED
551 001150 001002          BNE     BEGIN
552 001152 004767 010646  JSR     PC,CNTLU      ;ALLOW SWREG TO BE LOADED
553 001156 012777 000340 177630 BEGIN:  MOV      R,40,PSW      ;PROC. A LEVEL #7
554 001164 012767 001156 010542  MOV      #BEGIN,RETURN

```

```

;*****
; TEST 0 CAN ALL DR11-B REG BE ADDRESSED WITHOUT ERROR?
;*****

```

```

555 001172 104400          SCOPE
556 001174 012767 001234 176602  MOV      #ERRA,BUSEPR  ;BUS ERROR VECTOR TO ERRA
557 001202 010700          MOV      %7,%0        ;PC TO R0
558 001204 005277 177606  INC      @DRWC        ;ADDRESS DRWC
559 001210 010700          MOV      %7,%0        ;PC TO R0
560 001212 005277 177602  INC      @DRBA        ;ADDRESS DRBA
561 001216 010700          MOV      %7,%0        ;PC TO R0
562 001220 005077 177576  CLP      @DRST        ;ADDRESS DRST
563 001224 010700          MOV      %7,%0        ;PC TO R0
564 001226 005277 177572  INC      @DRDB        ;ADDRESS DRDB
565 001232 000401          BR      .+4          ;MADE IT - BRANCH OVER HALT
566 001234 104000  ERRA:  HLT
567 001236 012767 000006 176540  MOV      #6,BUSEPR   ;BUS ERROR, R0 HAS PC OF ERROR
568 001244 104400          SCOPE

```

```

;*****
; TEST 1 DOES RESET CLEAR DRWC?
;*****

```

```

569 001246 012767 000010 010454  MOV      #10,ICOUNT
570 001254 012777 177777 177534  MOV      #-1,@DRWC   ;ALL ONES J DRWC
571 001262 004767 010464  JSR     %7,CKSWR
572 001266 000005          RESET          ;INIT
573 001270 005777 177522  TST     @DRWC        ;LOOKING FOR Z-BIT TO SET
574 001274 001401          BEQ     .+4        ;DID DRWC GET CLEARED?
575 001276 104000          HLT
576 001300 104400          SCOPE

```

```

;*****
; TEST2 DOES RESET CLEAR DRBA?
;*****

```

```

577 001302 104400          SCOPE
578 001304 012777 177777 177506  MOV      #-1,@DRBA   ;ALL ONES TO DRBA
579 001312 004767 010434  JSR     %7,CKSWR

```

MO1

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DZDRB.P11

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```

602 001316 000005 RESET ;INIT
603 001320 005777 177474 TST @DRBA ;LOOKING FOR Z-BIT TO SET
604 001324 001401 BEQ .+4 ;DID DRBA GET CLEARED?
605 001326 104000 HLT ;DRBA NOT CLEAR

*****
; TEST3 CAN ALL DRWC BITS BE SET?
*****

613 001330 104400 SCOPE
614 001332 012767 004000 01C370 MOV #4000,ICOUNT
615 001340 012777 177777 177450 MOV #-1,@DRWC ;SET ALL BITS IN DRWC
616 001345 022777 177777 177442 CMP #-1,@DRWC ;LOOKING FOR Z-BIT TO SET
617 001354 001401 BEQ .+4 ;SEE IF ALL BITS GOT SET
618 001356 104000 HLT ;ALL BITS AREN'T SET

*****
; TEST4 CAN BITS 15-01 IN DRBA BE SET?
*****

625 001360 104400 SCOPE
626 001362 012777 177776 177430 MOV #-2,@DRBA ;SET BITS 15-01 IN DRBA
627 001370 022777 177776 177422 CMP #-2,@DRBA ;LOOKING FOR Z-BIT TO SET
628 001376 001401 BEQ .+4 ;SEE IF BITS 15-01 GOT SET
629 001400 104000 HLT ;BITS 15-01 AREN'T SET

*****
; TEST6 TEST THAT FNCT1 CAN BE SET AND CLEARED
*****

638 001402 104400 SCOPE
639 001404 052777 000002 177410 BIS #BIT1,@DRST ;SET FNCT1
640 001412 032777 000002 177402 BIT #BIT1,@DRST ;TEST FNCT1
641 001420 001001 BNE .+4 ;IS IT SET?
642 001422 104000 HLT ;FNCT1 IS CLEAR
643 001424 042777 000002 177370 BIC #BIT1,@DRST ;CLEAR FNCT1
644 001432 032777 000002 177362 BIT #BIT1,@DRST ;TEST FNCT1
645 001440 001401 BEQ .+4 ;WAS IT CLEAR
646 001442 104000 HLT ;FNCT1 WAS SET

*****
; TEST7 TEST THAT FNCT2 CAN BE SET AND CLEARED
*****

655 001444 104400 SCOPE
656 001446 052777 000004 177346 BIS #BIT2,@DRST ;SET FNCT2
657 001454 032777 000004 177340 BIT #BIT2,@DRST ;TEST FNCT2

```

```

001462 001001
001464 104000
001466 042777 000004 177326
001468 032777 000004 177320
001470 001401
001472 104000

```

```

BNE .+4 ;IS IT SET?
HLT ;FNCT2 IS CLEAR
BIC #BIT2,ADRST ;CLEAR FNCT2
BIT #BIT2,ADRST ;TEST FNCT2
BEQ .+4 ;WAS IT CLEAR?
HLT ;FNCT2 WAS SET

```

```

*****
TEST10 TEST THAT FNCT3 CAN BE SET AND CLEARED
*****

```

```

001474 000010 177304
001476 000010 177276
001478 000010 177254
001480 000010 177256

```

```

SCOPE
BIS #BIT3,ADRST ;SET FNCT3
BIT #BIT3,ADRST ;TEST FNCT3
BNE .+4 ;IS IT SET?
HLT ;FNCT3 IS CLEAR
BIC #BIT3,ADRST ;CLEAR FNCT3
BIT #BIT3,ADRST ;TEST FNCT3
BEQ .+4 ;WAS IT CLEAR?
HLT ;FNCT3 WAS SET

```

```

*****
TEST11 TEST THAT XBA16 CAN BE SET AND CLEARED
*****

```

```

001482 000020 177242
001484 000020 177234
001486 000020 177222
001488 000020 177214

```

```

SCOPE
BIS #BIT4,ADRST ;SET XBA16
BIT #BIT4,ADRST ;TEST XBA16
BNE .+4 ;IS IT SET?
HLT ;XBA16 IS CLEAR
BIC #BIT4,ADRST ;CLEAR XBA16
BIT #BIT4,ADRST ;TEST XBA16
BEQ .+4 ;IS IT CLEAR?
HLT ;XBA16 WAS SET

```

```

*****
TEST12 TEST THAT XBA17 CAN BE SET AND CLEARED
*****

```

```

001490 000040 177200
001492 000040 177172
001494 000020 177150
001496 000020 177152

```

```

SCOPE
BIS #BIT5,ADRST ;SET XBA17
BIT #BIT5,ADRST ;TEST XBA17
BNE .+4 ;IS IT SET?
HLT ;XBA17 IS CLEAR
BIC #BIT4,ADRST ;CLEAR XBA17
BIT #BIT4,ADRST ;TEST XBA17
BEQ .+4 ;IS IT CLEAR?
HLT ;XBA17 WAS SET

```

```

*****
TEST13 TEST THAT IE CAN BE SET AND CLEARED
*****

```

```

001498 000030 177136
001500 000030 177130

```

```

SCOPE
BIS #BIT6,ADRST ;SET IE
BIT #BIT6,ADRST ;TEST IE

```

```

001502 000000 000000
001504 000000 000000
001506 000000 000000
001508 000000 000000
001510 000000 000000
001512 000000 000000
001514 000000 000000
001516 000000 000000
001518 000000 000000
001520 000000 000000
001522 000000 000000
001524 000000 000000
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001590 000000 000000
001592 000000 000000
001594 000000 000000
001596 000000 000000
001598 000000 000000
001600 000000 000000

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00000000 00000000 104400 SCOPE
00000000 00000000 012777 MOV #400,ICOUNT
00000000 00000000 000340 MOV #340,IPSW :STATUS AT LEVEL 7
00000000 00000000 000200 BIT #BIT7,DRST :CHECK READY BIT
00000000 00000000 001010 BNE P6INV :IS IT SET
00000000 00000000 004767 JSR %7,CKSWR
00000000 00000000 000005 RESET :INIT TO SET READY
00000000 00000000 002777 BIT #BIT7,DRST :SEE IF READY IS SET NOW
00000000 00000000 001001 BNE .+4 :IS READY SET?
00000000 00000000 104000 HLT :READY CAN'T BE SET BY INIT
00000000 00000000 002654 P7INV: MOV #P7ERR,DRINV :SET UP INT VECTOR
00000000 00000000 000100 BIS #BIT6,DRST :SET IE
00000000 00000000 000240 NOP
00000000 00000000 000100 BIC #BIT6,DRST ;DR11-B DIDN'T INTERRUPT - CLEAR IE
00000000 00000000 000401 BR .+4
00000000 104000 P7ERR: HLT ;DR11-B INTERRUPTED, BUT IT SHOULDN'T HAVE

:*****
: TEST26 TEST THAT DR11-B DOES NOT INTERRUPT WITH PROC AT LEVEL 6
:*****

00000000 00000000 104400 SCOPE
00000000 00000000 000300 MOV #300,IPSW :STATUS AT LEVEL 6
00000000 00000000 000200 BIT #BIT7,DRST :CHECK READY BIT
00000000 00000000 001010 BNE P6INV :IS IT SET?
00000000 00000000 004767 JSR %7,CKSWR
00000000 00000000 000005 RESET :INIT TO SET READY
00000000 00000000 002777 BIT #BIT7,DRST :SEE IF READY IS SET NOW
00000000 00000000 001001 BNE .+4 :IS READY SET?
00000000 00000000 104000 HLT :READY CAN'T BE SET BY INIT
00000000 00000000 002744 P6INV: MOV #P6ERR,DRINV :SET UP INT VECTOR
00000000 00000000 000100 BIS #BIT6,DRST :SET IE
00000000 00000000 000240 NOP
00000000 00000000 000100 BIC #BIT6,DRST ;DR11-B DIDN'T INTERRUPT - CLEAR IE
00000000 00000000 000401 BR .+4
00000000 104000 P6ERR: HLT ;DR11-B INTERRUPTED, BUT IT SHOULDN'T HAVE

:*****
: TEST27 TEST THAT DR11-B DOES NOT INTERRUPT WITH PROC AT LEVEL 5
:*****

00000000 00000000 104400 SCOPE
00000000 00000000 002750 MOV #240,IPSW :STATUS AT LEVEL 5
00000000 00000000 002777 BIT #BIT7,DRST :CHECK READY BIT
00000000 00000000 001010 BNE P5INV :IS IT SET?
00000000 00000000 004767 JSR %7,CKSWR
00000000 00000000 000005 RESET :INIT TO SET READY
00000000 00000000 002777 BIT #BIT7,DRST :SEE IF READY IS SET NOW
00000000 00000000 001001 BNE .+4 :IS IT SET?
00000000 00000000 104000 HLT :RDY CAN'T BE SET BY INIT
00000000 00000000 003034 P5INV: MOV #P5ERR,DRINV :SET UP INT VECTOR
00000000 00000000 000100 BIS #BIT6,DRST :SET IE
00000000 00000000 000240 NOP
00000000 00000000 000100 BIC #BIT6,DRST ;DR11-B DIDN'T INTERRUPT - CLEAR IE
00000000 00000000 000401 BR .+4
00000000 104000 P5ERR: HLT ;DR11-B INTERRUPTED, BUT IT SHOULDN'T HAVE

```



```

003304 104400
003306 005777 175510
003312 100027
003314 032777 020000 175500
003322 001401
003324 104000
003326 032777 040000 175466
003334 001410
003336 042777 040000 175456
003344 032777 040000 175450
003352 001401
003354 104000
003356 005077 175436
003362 005777 175434
003366 001401
003370 104000
003372 012777 177777 175416
003400 012777 001034 175412
003406 005077 175412
003412 012777 052525 175414
003420 012777 003464 175404
003426 012777 000005 175372
003434 005077 175354
003440 012777 000101 175354
003446 005067 000002
003452 005227 000001
003456 001375
003460 104000
003462 000424
003464 004767 003312
003470 005777 175322
003474 001401
003476 104000
003500 022777 001036 175312
003506 001401
003510 104000
003512 022777 052525 175304
003520 001401
003522 104000
003524 004767 003162
003530 022626
003532 000403
003534 005077 175262
003540 000662

SCOPE
TNPRI: TST @DRST ;CHECK ERROR BIT
        BFL NPRDY ;IS IT CLEAR?
        BIT @BIT13,@DRST ;CHECK ATTN
        BEQ .+4 ;IS ATTN CLEAR
        HLT ;ATTN IS SET
        SIT @BIT14,@DRST ;CHECK NEX
        N1413 ;IS NEX CLEAR?
        BIT @BIT14,@DRST ;TRY TO CLEAR NEX
        BIT @BIT14,@DRST ;CHECK AGAIN
        BEQ .+4 ;NEX STILL SET
        HLT ;NEX CAN'T BE CLEARED BY MOVING A 0 TO IT
N1413: CLR @DRBA ;TRY TO CLEAR BACF
        TST @DRST ;CHECK ERROR BIT AGAIN
        BEQ .+4 ;IS IT CLEAR
        HLT ;ERROR CAUSED BY SOMETHING OTHER THAN NEX,ATTN, OR BACF
NPRDY: MOV #-1,@DRWC ;SET UP FOR 1 TRANSFER
        MOV @NPR1,@DRBA ;TRANSFER FROM BUS ADDRESS IN NPR1
        CLR @DRDB ;GET READY TO RECEIVE DATA
        MOV @52525,NPR1 ;SET UP TRANSFER DATA
        MOV @INTB,@DRINV ;INTERRUPT VECTOR TO INTB
        MOV @5,@DRVS ;INTERRUPT PRIORITY TO LEVEL 5
        CLR @PSW ;LET THE DR11-B INTERRUPT
        MOV @101,@DRST ;IE AND DO TO DRST
        CLR @5+2 ;WAIT FOR NPR AND INTERRUPT
        INC @1
        BNE @3
        HLT ;NO DR11-B INTERRUPT
INTB: BR T33CLR ;CLEAR IE
        JSR %7,ERRCHK
        TST @DRWC ;TEST DRWC
        BEQ .+4 ;IS DRWC EQUAL TO ZERO?
        HLT ;DRWC NOT EQUAL TO ZERO
        CMP @NPR1+2,@DRBA ;COMPARE CORRECT DRBA WITH DRBA
        BEQ .+4 ;IS THE DRBA CORRECT?
        HLT ;DRBA IS WRONG
        CMP @52525,@DRDB ;CHECK FOR CORRECT DATA
        BEQ .+4 ;DATA GET TRANSFERRED?
        HLT ;BAD DATA IN DRDB
T33CLR: BR %7,NORMAL ;RESTORE STACK
        CMP (%6)+,(%6)+ ;GO TO NEXT TEST (NPR OUT)
        BR TNPRI ;CLEAR IE
        CLR @DRST ;TRY TEST AGAIN
        BR TNPRI

*****
: TEST 34 TEST FOR 1 DATO NPR TRANSFER (WITH 1968 IN USER SLOTS)
*****
TNPRI: SCOPE
        MOV #-1,@DRWC ;SET UP FOR 1 TRANSFER
        MOV @NPR1,@DRBA ;TRANSFER TO BUS ADDRESS IN NPR1
        CLR NPR1 ;GET READY TO RECEIVE DATA
        MOV @52525,@DRDB ;SET UP TO TRANSFER DATA
        MOV @INTC,@DRINV ;INTERRUPT VECTOR TO INTC
        MOV @DRINL,@DRVS ;INTERRUPT STATUS TO LEVEL DRINL
        CLR @PSW ;PRCC STATUS TO ZERO
        MOV @103,@DRST ;IE, FNCT1(C1 CONTROL), AND DO TO DRST

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1050 003620 005067 000002          CLR      15+2          ;WAIT FOR NPR AND INTER
1051 003624 005227 000001          IS:      INC          #1
1052 003630 001375          BNE     15
1053 003632 104000          HLT
1054 003634 000424          BR      T34CLR          ;NO DR11-B INTERRUPT
1055 003636 004767 003140          INTC:   JSR      %7,ERRCHK ;CLEAR IE
1056 003642 005777 175150          TST     @DRWC          ;TEST DRWC
1057 003646 001401          BEQ     .+4            ;IS DRWC EQUAL TO ZERO?
1058 003650 104000          HLT          ;DRWC EQUAL TO ZERO
1059 003652 022777 001036 175140          CMP     @NPR1+2,@DRBA ;COMPARE CORRECT DRBA WITH DRBA
1060 003660 001401          BEQ     .+4            ;IS THE DRBA CORRECT?
1061 003652 104000          HLT          ;DRBA IS WRONG
1062 003664 026727 175144 052525          CMP     NPR1,@52525    ;CHECK FOR CORRECT DATA
1063 003672 001401          BEQ     .+4            ;CORRECT DATA TRANSFERRED?
1064 003674 104000          HLT          ;BAD DATA
1065 003676 004767 003010          JSR     %7,NORMAL
1066 003702 022626          CMP     (%6)+,(%6)+   ;RESTORE STACK
1067 003704 000403          BR      T35           ;GO TO NEXT TEST
1068 003706 025077 175110          T34CLR: CLR     @DRST  ;CLEAR IE
1069 003712 000713          BR      TNPRO         ;TRY TEST AGAIN

:*****
: TEST 35 STRING OF 10 DATI'S (WITH M968 IN USER SLOTS)
:*****
T35: SCOPE
MOV     #20,BUFLEN      ;LENGTH OF BUFFER=20
JSR     %7,LODBUF      ;LOAD THE BUFFER WITH INCREMENTING PATTERN
ASR     BUFLEN          ;BUFLEN=10
MOV     BUFLEN,WLEN     ;PREPARE NUMBER FOR DRWC
NEG     WLEN            ;2'S COMPLEMENT OF BUFLEN
MOV     WLEN,@DRWC     ;SET UP DRWC
MOV     INBUF,@DRBA    ;SET UP DRBA
MOV     #-1,@DRDB      ;MAINT AIDE
MOV     @INTA,@DRINV   ;INT VECTOR TO INTA
MOV     DRINL,@DRVS    ;INT VECTOR TO PRIORITY DRINL
CLR     @PSW           ;LET THE DR11-B INTERRUPT
MOV     #101,@DRST     ;IE AND DO TO DRST
BR      .              ;WAIT FOR INTERRUPT
CMP     #7,@DRDB       ;CHECK THAT WORD #10 OF INBUF IS IN DRBA
BEQ     .+4            ;IS IT?
HLT     .              ;BAD DATA IN DRDB

:*****
: TEST 36 STRING OF 10 DATO'S (WITH M968 IN USER SLOTS)
:*****
SCOPE
MOV     #20,BUFLEN      ;LENGTH OF BUFFER=20
JSR     %7,LODBUF      ;LOAD THE BUFFER WITH INCREMENTING PATTERN
ASR     BUFLEN          ;BUFLEN=10
MOV     BUFLEN,WLEN     ;PREPARE NUMBER FOR DRWC
NEG     WLEN            ;2'S COMPLEMENT OF BUFLEN
MOV     WLEN,@DRWC     ;SET UP DRWC
MOV     INBUF,@DRBA    ;SET UP DRBA
MOV     #52525,@DRDB   ;SET UP DRDB
MOV     @INTA,@DRINV   ;INTERRUPT VECTOR TO INTA

```

```

1106 004114 016777 174710 174704
1107 004122 005077 174666
1108 004126 012777 000103 174666
1109 004134 000777
1110 004136 004767 002572
1111
1112
1113
1114
1115 004142 104400
1116 004144 012767 000200 174672
1117 004152 004767 002276
1118 004156 016767 174562 174666
1119 004164 005467 174662
1120 004170 016777 174656 174620
1121 004176 016777 174636 174614
1122 004207 012777 177777 174512
1123 004212 012777 006556 174612
1124 004220 016777 174604 174600
1125 004226 005077 174562
1126 004232 012777 000101 174562
1127 004240 000777
1128 004242 022777 000177 174554
1129 004250 001401
1130 004252 104000
1131
1132
1133
1134 004254 104400
1135 004256 012767 000201 174560
1136 004264 004767 002164
1137 004270 005367 174550
1138 004274 016767 174544 174550
1139 004302 005467 174544
1140 004306 016777 174540 174502
1141 004314 016777 174520 174476
1142 004322 012777 052525 174474
1143 004330 012777 006556 174474
1144 004336 016777 174466 174462
1145 004344 005077 174444
1146 004350 012777 000103 174444
1147 004356 000777
1148 004360 004767 002350
1149
1150
1151
1152
1153 004364 104400
1154 004366 012777 177776 174422
1155 004374 016777 174436 174416
1156 004402 012777 004436 174422
1157 004410 016777 174414 174410
1158 004416 005077 174372
1159 004422 012777 000163 174372
1160 004430 005237 177560
1161 004434 104000

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MOV DRINL,DRVS ;INTERRUPT VECTOR TO PRIORITY DRINL
CLR DRPSW ;LET THE DR11-B INTERRUPT
MOV #103,DRST ;IE, FNCT1(C1 CONTROL), AND GO TO DRST
BR ;WAIT FOR INTERRUPT
JSR %7.DATOCK ;CHECK INBUF

;*****
; TEST 37 STRING OF 200 DATI'S
;*****
SCOPE
MOV #200,BUFLEN ;LENGTH OF BUFFER=200
JSR %7.LOGBUF ;LOAD THE BUFFER WITH INCREMENTING PATTERN
MOV BUFLEN,WLEN ;PREPARE NUMBER FOR DRWC
NEG WLEN ;2'S COMPLEMENT OF BUFLEN
MOV WLEN,DRWC ;SET UP DRWC
MOV INBUF,DRBA ;SET UP DRBA
MOV #-1,DRDB ;MAINT AIDE
MOV #INTA,DRINV ;INT VECTOR TO INTA
MOV DRINL,DRVS ;INT VECTOR TO PRIORITY DRINL
CLR DRPSW ;LET THE DR11-B INTERRUPT
MOV #101,DRST ;IE AND GO TO DRST
BR ;WAIT FOR INTERRUPT
CMP #177,DRDB ;CHECK THAT WORD #200 OF INBUF IS IN DRBA
BEQ .+4 ;IS IT?
HLT ;BAD DATA IN DRDB

;*****
; TEST 40 STRING OR 200 DATO'S
;*****
SCOPE
MOV #201,BUFLEN ;LENGTH OF BUFFER=201
JSR %7.LOGBUF ;LOAD THE BUFFER WITH INCREMENTING PATTERN
DEC BUFLEN ;BUFLEN=200
MOV BUFLEN,WLEN ;PREPARE NUMBER FOR DRWC
NEG WLEN ;2'S COMPLEMENT OF BUFLEN
MOV WLEN,DRWC ;SET UP DRWC
MOV INBUF,DRBA ;SET UP DRBA
MOV #52525,DRDB ;SET UP DRDB
MOV #INTA,DRINV ;INTERRUPT VECTOR TO INTA
MOV DRINL,DRVS ;INTERRUPT VECTOR TO PRIORITY DRINL
CLR DRPSW ;LET THE DR11-B INTERRUPT
MOV #103,DRST ;IE, FNCT1, AND GO TO DRST
BR ;WAIT FOR INTERRUPT
JSR %7.DATOCK ;CHECK INBUF

;*****
; TEST 42 TEST THAT DOING A DATO TO THE DIODE MEMORY CAUSES NEX
;*****
SCOPE
MOV #-2,DRWC ;SET UP DRWC
MOV DIOMEM,DRBA ;SET UP DRBA
MOV #NEXCHK,DRINV ;INTERRUPT VECTOR TO NEXCHK
MOV DRINL,DRVS ;INTERRUPT STATUS TO LEVEL DRINL
CLR DRPSW ;LET THE DR11-B INTERRUPT
MOV #163,DRST ;IE, FNCT1, XBA17, XBA16, AND GO TO DRST
INC #177560 ;WAIT FOR INTERRUPT
HLT ;NO DR11-B INTERRUPT

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1162 004436 005777 17436J NEXCHK: TST @DRST ;TEST DRST
1163 004442 001001 BNE .+4 ;ERROR SET?
1164 004444 104000 HLT ;ERROR NOT SET
1165 004446 105777 174350 TSTB @DRST ;TEST FOR READY
1166 004452 001001 BNE .+4 ;READY SET?
1167 004454 104000 HLT ;READY ISN'T SET
1168 004456 032777 040000 174336 BIT @BIT14,@DRST ;CHECK NEX
1169 004464 001001 BNE .+4 ;NEX SET?
1170 004466 104000 HLT ;NEX IS CLEAR
1171 004470 022626 CMP (%)+,(%)+ ;RESTORE THE STACK
1172 004472 004767 002214 JSR @7,NORMAL

:*****
: TEST 43 TEST THAT BAOF FORCES ERROR AND READY AND THAT BAOF IS
: CLEARED BY CLEARING THE DRBA OR A RESET
:*****
1178 004476 104400 SCOPE
1179 004500 012767 000010 005222 MOV @10,ICOUNT
1180 004506 012777 177760 174302 MOV @-20,@DRWC ;SET UP DRWC
1181 004514 012777 177776 174276 MOV @-2,@DRBA ;SET UP DRBA FOR PROC STATUS ADDRESS
1182 004522 012777 004556 174302 MOV @BAOFCK,@DRINV ;INTERRUPT VECTOR TO BAOFCK
1183 004530 016777 174274 174270 MOV DRINL,@DRVS ;INTERRUPT STATUS TO LEVEL DRINL
1184 004536 005077 174252 CLR @PSW ;LET THE DR11-B INTERRUPT
1185 004542 012777 000163 174252 MOV @163,@DRST ;I.E. FNCT1, XBA17, XBA16, AND GO TO DRST
1186 004550 005237 177560 INC @177560 ;WAIT FOR INTERRUPT
1187 004554 104000 HLT ;NO DR11-B INTERRUPT
1188 004556 022626 174236 BAOFCK: CMP (%)+,(%)+ ;RESTORE THE STACK
1189 004560 005777 174236 TST @DRST ;TEST DRST
1190 004564 100401 BMI .+4 ;ERROR SET?
1191 004566 104000 HLT ;ERROR NOT SET
1192 004570 105777 174226 TSTB @DRST ;TEST FOR READY
1193 004574 100401 BMI .+4 ;READY SET?
1194 004576 104000 HLT ;READY ISN'T SET
1195 004600 042777 040000 174214 BIT @BIT14,@DRST ;CLEAR NEX
1196 004606 032777 060000 174206 BIT @60000,@DRST ;CHECK NEX AND ATTN
1197 004614 001401 BEQ .+4 ;ARE THEY CLEAR?
1198 004616 104000 HLT ;NEX AND/OR ATTN IS SET
1199 004620 005777 174176 TST @DRST ;TEST FOR ERROR
1200 004624 100401 BMI .+4 ;IS ERROR SET?
1201 004626 104000 HLT ;ERROR IS CLEAR
1202 004630 005077 174164 CLR @DRBA ;CLEAR BAOF
1203 004634 005777 174162 TST @DRST ;CHECK ERROR
1204 004640 100001 BPL .+4 ;SHOULD BE CLEAR
1205 004642 104000 HLT ;CLEARING DRBA DIDN'T CLEAR BAOF
1206
1207 004644 012777 177776 174146 MOV @-2,@DRBA ;SET UP DRBA FOR PROC STATUS ADDRESS
1208 004652 012777 004706 174152 MOV @BAOCK1,@DRINV ;INTERRUPT VECTOR TO BAOCK1
1209 004660 016777 174144 174140 MOV DRINL,@DRVS ;INTERRUPT STATUS TO LEVEL DRINL
1210 004666 005077 174122 CLR @PSW ;LET THE DR11-B INTERRUPT
1211 004672 012777 000163 174122 MOV @163,@DRST ;I.E., XBA17, XBA16, FNCT1, AND GO TO DRST
1212 004700 005237 177560 INC @177560 ;WAIT FOR INTERRUPT
1213 004704 104000 HLT ;NO DR11-B INTERRUPT
1214 004706 022626 174106 BAOCK1: CMP (%)+,(%)+ ;RESTORE THE STACK
1215 004710 005777 174106 TST @DRST ;TEST DRST
1216 004714 100401 BMI .+4 ;ERROR SET?
1217 004716 104000 HLT ;ERROR NOT SET

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1218 004720 105777 174076
1219 004724 100401
1220 004726 104000
1221 004730 042777 040000 174064
1222 004736 032777 060000 174056
1223 004744 001401
1224 004746 104000
1225 004750 005777 174046
1226 004754 100401
1227 004756 104000
1228 004760 004767 004766
1229 004764 000005
1230 004766 005777 174030
1231 004772 000001
1232 004774 104000
1233 004776 004767 001710
1234
1235
1236
1237
1238 005002 104400
1239 005004 012767 000010 004716
1240 005012 012777 177777 174004
1241 005020 004767 004726
1242 005024 000005
1243 005026 005777 173772
1244 005032 001401
1245 005034 104000
1246
1247
1248
1249
1250 005036 104400
1251 005040 012767 004000 004662
1252 005046 012777 177777 173750
1253 005054 022777 177777 173742
1254 005062 001401
1255 005064 104000
1256
1257
1258
1259
1260 005066 104400
1261 005070 012777 052525 173726
1262 005076 022777 052525 173720
1263 005104 001401
1264 005106 104000
1265 005110 012777 125252 173706
1266 005116 022777 125252 173700
1267 005124 001401
1268 005126 104000
1269
1270
1271
1272
1273 005130 104400

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TSTB 2DRST ;TEST FOR READY
BMT .+4 ;READY SET?
HLT ;READY ISN'T SET
BIC #BIT14,2DRST ;CLEAR NEX
BIT #60000,2DRST ;CHECK NEX AND ATTN
BEQ .+4 ;ARE THEY CLEAR?
;NEX AND/OR ATTN IS SET
TST 2DRST ;TEST FOR ERROR
BMT .+4 ;IS ERROR SET?
HLT ;ERROR IS CLEAR
JSR %7,CKSWR
RESET ;INIT
TST 2DRST ;CHECK ERROR
BPL .+4 ;SHOULD BE CLEAR
HLT ;RESET DIDN'T CLEAR BAOF
JSR %7,NORMAL

:*****
: TEST 44 TEST THAT RESET CLEARS DRDB
:*****
SCOPE
MOV #10,ICOUNT
MOV #-1,2DRDB ;ALL ONES TO DRDB
JSR %7,CKSWR
RESET ;INIT
TST 2DRDB ;LOOKING FOR Z-BIT TO SET
BEQ .+4 ;DID DRDB GET CLEARED?
HLT ;DRDB NOT CLEAR

:*****
: TEST 45 TEST THAT ALL DRDB BITS CAN BE SET
:*****
SCOPE
MOV #4000,ICOUNT
MOV #-1,2DRDB ;SET ALL BITS IN DRDB
CMP #-1,2DRDB ;LOOKING FOR Z-BIT TO SET
BEQ .+4 ;SEE IF ALL BITS GOT SET
HLT ;ALL DRDB BITS AREN'T SET

:*****
: TEST 46 TEST THAT DRDB CAN HOLD ALTERNATE ONE'S AND ZERO'S
:*****
SCOPE
MOV #052525,2DRDB ;ALT 0'S AND 1'S TO DRDB
CMP #052525,2DRDB ;LOOKING FOR Z-BIT TO SET
BEQ .+4 ;DOES DRDB HAVE THE CORRECT PATTERN?
HLT ;DRDB IS WRONG
MOV #125252,2DRDB ;ALT 1'S AND 0'S TO DRDB
CMP #125252,2DRDB ;LOOKING FOR Z-BIT TO SET
BEQ .+4 ;DOES DRDB HAVE THE CORRECT PATTERN
HLT ;DRDB IS WRONG

:*****
: TEST 47 INCREMENTING PATTERN TO WRAP-AROUND IN DRDB
:*****
SCOPE

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1274 005132 005067 004572          CLR      ICOUNT
1275 005133 005001          CLR      %1          ;SET-UP
1276 005134 005077 173660      CLR      @DRDB      ;SET-UP
1277 005140 005077 173654      INCDB:  CMP      %1,@DRDB ;SEE IF THEY ARE EQUAL
1278 005144 020177 173654          BEQ      .+4          ;ARE THEY EQUAL?
1279 005150 001401          HLT      ;THEY'RE NOT EQUAL
1280 005152 104000          HLT      ;GET NEXT NUMBER
1281 005154 005277 173644      INC      @DRDB      ;GET NEXT NUMBER
1282 005160 005201          INC      %1          ;GET NEXT NUMBER
1283 005162 001370          BNE     INCDB      ;DONE WITH TEST? IF NOT CONTINUE
1284
1285 ;*****
1286 ;TEST 50 TEST THAT RESET SETS READY AND CLEARS ALL OTHER
1287 ;DRST BITS (WITH M968 INSERTED)
1288 ;*****
1289 005164 104400          SCOPE
1290 005166 004767 004560      JSR      %7,CKSWR
1291 005172 000005          RESET     ;INIT
1292 005174 032777 000200 173620  BIT      #BIT7,@DRST ;CHECK DRST
1293 005202 001001          BNE     .+4          ;IS READY SET?
1294 005204 104000          HLT      ;READY IS CLEAR
1295 005206 032777 177577 173606  BIT      #177577,@DRST ;CHECK DRST
1296 005214 001401          BEQ     .+4          ;ARE THEY ALL CLEAR?
1297 005216 104000          HLT     ;A BIT OTHER THAN READY IS SET IN THE DRST
1298
1299 ;*****
1300 ;TEST 51 TEST THAT BA00 READS AS A ZERO WITH MAINT BOARD INSERTED
1301 ;*****
1302 005220 104400          SCOPE
1303 005222 012767 004000 004500      MOV     #4000,ICOUNT
1304 005230 032777 000001 173552  BIT     #BIT0,@DRBA  ;TEST BIT 0 OF DRBA
1305 005236 001401          BEQ     .+4          ;IS IT CLEAR?
1306 005240 104000          HLT     ;BA00 IS SET
1307
1308
1309 ;*****
1310 ;TEST 52 TEST THAT GO CLEARS READY
1311 ;*****
1312 005242 104400          SCOPE
1313 005244 012767 004000 004456      MOV     #4000,ICOUNT
1314 005252 012777 177600 173536      MOV     #-200,@DRWC ;SET-UP DRWC
1315 005260 016777 173554 173532      MOV     INBUF,@DRPA ;SET-UP DRPA
1316 005266 105777 173530          TSTB   @DRST        ;CHECK READY
1317 005272 100401          BMI   .+4          ;IS READY SET?
1318 005274 104000          HLT   ;READY IS CLEAR
1319 005276 012777 000011 173516      MOV     #11,@DRST   ;FNCT3 (NON-BURST) AND GO TO DRST
1320 005304 105777 173512          TSTB   @DRST        ;CHECK READY
1321 005310 100001          BPL   .+4          ;IS READY CLEAR?
1322 005312 104000          HLT   ;READY IS STILL SET
1323 005314 005067 173534          CLR   RDYCHK        ;CLEAR READY CHECK
1324 005320 105777 173476      TSTRDY: TSTB   @DRST ;CHECK READY
1325 005324 100406          BMI   DONE          ;IF SET GO TO DONE
1326 005326 062767 000004 173520      ADD    #4,RDYCHK    ;CHECKING TIME FOR READY TO BE SET
1327 005334 100401          BMI   .+4          ;IF RDYCHK GETS NEGATIVE IT TOOK TOO LONG
1328 005336 000770          BR    TSTRDY        ;CHECK AGAIN
1329 005340 104000          HLT   ;READY GOT CLEARED BUT NEVER SET AGAIN

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M02

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1330 005342 000240
1331
1332
1333
1334
1335 005344 104400
1336 005346 012777 177760 173442
1337 005354 016777 173456 173436
1338 005362 012777 005416 173442
1339 005370 012777 000200 173430
1340 005376 005077 173412
1341 005402 012777 000163 173412
1342 005410 005277 173442
1343 005414 104000
1344 005416 005777 173400
1345 005422 100401
1346 005424 104000
1347 005426 012777 005474 173376
1348 005434 005077 173360
1349 005440 042777 000062 173354
1350 005446 012777 177777 173342
1351 005454 005277 173342
1352 005460 005067 000002
1353 005464 005227 000001
1354 005470 001375
1355 005472 104000
1356 005474 005777 173322
1357 005500 100401
1358 005502 104000
1359
1360 005504 062706 000010
1361 005510 004767 001176
1362
1363
1364
1365
1366 005514 104400
1367 005516 012767 000200 173320
1368 005524 004767 000724
1369 005530 016767 173310 173314
1370 005536 005467 173310
1371 005542 016777 173304 173246
1372 005550 016777 173264 173242
1373 005556 012777 177777 173240
1374 005564 012777 006556 173240
1375 005572 016777 173232 173226
1376 005600 005077 173210
1377 005604 012777 000111 173210
1378 005612 005267 173232
1379 005616 032767 000001 173224
1380 005624 001403
1381 005626 000001
1382 005630 000240
1383 005632 000401
1384 005634 000777
1385 005636 022777 000177 173160

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DONE: MOP ;GO TO NEXT TEST
;*****
;TEST 55 TEST THAT GIVING A DO WITHOUT CLEARING A PREVIOUS ERROR
;CAUSES ANOTHER INTERRUPT
;*****
SCOPE
MOV #20,DRWC ;SET-UP DRWC
MOV DIOMEM,DRBA ;SET-UP DRBA
MOV #ERRD0,DRINV ;INTERRUPT VECTOR TO ERRD0
MOV #200,DRVS ;INTERRUPT STATUS TO LEVEL 4
CLR APSW ;LET THE DR11-B INTERRUPT
MOV #163,DRST ;IE, XBA17,XBA16, FNCT1 AND GO TO DRST
INC ATKS ;WAIT FOR INTERJPT
HLT ;NO DR11-B INTERRUPT
ERRD0: TST DRST ;TEST DRST
BMI .+4 ;ERROR SET?
HLT ;ERROR IS CLEAR - SHOULD HAVE NEX
MOV #ERRD01,DRINV ;INTERRUPT VECTOR TO ERRD01
CLR DRBA ;PREVENT CAUSING ANOTHER ERROR
BIC #62,DRST ;CLEAR XBA17, XBA16, AND FNCT1
MOV #-1,DRWC ;SET-UP DRWC
INC DRST ;DO TO DRST
CLR IS+2
IS: INC #1
BNE IS
HLT ;NO DR11-B INTERRUPT
ERRD01: TST DRST ;CHECK ERROR
BMI .+4 ;ERROR SET?
HLT ;ERROR IS CLEAR - SHOULD BE SET BECAUSE
;PREVIOUS ERROR WAS NOT CLEARED
ADD #10,%6 ;REPOSITION THE STACK
JSR %7,NORMAL
;*****
;TEST 56 STRING OF 200 DATI'S NON-BURST MODE
;*****
SCOPE
MOV #200,BUFLEN ;LENGTH OF BUFFER=200
JSR %7,LODBUF ;LOAD THE BUFFER WITH INCREMENTING PATTERN
MOV BUFLN,WCLN ;PREPARE NUMBER FOR DRWC
NEG WCLN ;2'S COMPLEMENT OF BUFLN
MOV WCLN,DRWC ;SET-UP DRWC
MOV INBUF,DRBA ;SET-UP DRBA
MOV #-1,DRDB ;MAINT AIDE
MOV #INTA,DRINV ;INT VECTOR TO INTA
MOV DRINL,DRVS ;INT VECTOR TO PRIORITY DRINL
CLR APSW ;LET THE DR11-B INTERRUPT
MOV #111,DRST ;IE, FNCT3, AND DO TO DRST
INC BRWAIT ;USE A WAIT OR BR. INSTRUCTION
BIT #BIT0,BRWAIT ;SEE WHICH ONE
BEQ DATINB ;BIT 0 CLEAR=BR.
WAIT ;WAIT FOR INTERRUPT
BR .+4
DATINB: BR
CMP #177,DRDB ;CHECK THAT WORD #200 OF INBUF IS IN DR9A

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0055644 104401
0055646 104000
0055650 104400
0055652 012767 000201 173164
0055660 004767 000570
0055664 005367 173154
0055670 016767 173150 173154
0055676 005467 173150
0055702 016777 173144 173106
0055710 016777 173124 173102
0055716 012777 052525 173100
0055724 012777 006556 173100
0055732 016777 173072 173066
0055740 005077 173050
0055744 012777 000113 173050
0055752 005267 173072
0055756 032767 000001 173064
0055764 001403
0055766 000001
0055770 000240
0055772 000401
0055774 000777
0055776 004767 000732

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      BEQ      .+4      ;IS IT?
      HLT      ;BAD DATA IN DRDB

:*****
:      TEST 57 STRING OF 200 DATO'S NON-BURST MODE
:*****
      SCOPE
      MOV      #201, BUFLN      ;LENGTH OF BUFFER=201
      JSR      %7, LOOBUF      ;LOAD THE BUFFER WITH INCREMENTING PATTERN
      DEC      BUFLN           ;BUFLN=200
      MOV      BUFLN, WCLN     ;PREPARE NUMBER FOR DRWC
      NEG      WCLN           ;2'S COMPLEMENT OF BUFLN
      MOV      WCLN, @DRWC    ;SET UP DRWC
      MOV      INBUF, @DRBA   ;SET UP DRBA
      MOV      #52525, @DRDB  ;SET UP DRDB
      MOV      #INTA, @DRINV  ;INTERRUPT VECTOR TO INTA
      MOV      DRINL, @DRVS   ;INTERRUPT VECTOR TO PRIORITY DRINL
      CLR      @PSW          ;LET THE DR11-B INTERRUPT
      MOV      #113, @DRST    ;IE, FNCT3, FNCT1, AND DC TO DRST
      INC      BRWAIT        ;USE A WAIT OR BR. INSTRUCTION
      BIT      #BIT0, BRWAIT ;BIT 0 CLEAR=BR.
      BEQ      DATONB
      WAIT
      NOP
      BR      .+4
DATONB: BR      ;WAIT FOR INTERRUPT
      JSR      %7, DATOCK    ;CHECK INBUF

:*****
:      TEST 60 TEST THAT FUNCTION BITS INCREMENT WITH MAINT MODE TRANSFERS
:*****
      SCOPE
      MOV      #10, BUFLN     ;SET-UP BUFLN FOR LOOBUF AND CHKBUFF
      MOV      INBUF, @DRBA   ;SET-UP DR2A
      JSR      %7, LOOBUF     ;LOAD INBUF
      JSR      %7, CHKBFF    ;LOAD CHKBUFF
      CLR      @DRST         ;INIT FOR STARTING
      MOV      #1, FNCCNT     ;GET READY FOR CHECKING
      MOV      #1, BUFLN     ;CHANGE IS NECESSARY FOR INTA ROUTINE
      MOV      INBUF, INBUF1  ;SAVE INBUF
      MOV      #INTA, @DRINV  ;INTERRUPT VECTOR TO INTA
      MOV      DRINL, @DRVS   ;INTERRUPT VECTOR PRIORITY TO DRINL
      CLR      @PSW          ;LET THE DR11-B INTERRUPT
      MOV      #-1, @DRWC    ;SET-UP FOR I TRANSFER
      BIS      #10101, @DRST ;MAINT IE AND DC TO DRST
      WAIT
      NOP
      MOV      @DRST, %1     ;FAKE-OUT RETURN ADDRESS CHANGING
      BIC      #600, %1     ;LOWER BYTE OF DRST TO R!
      ASR      %1           ;GET RID OF READY AND CYCLE BECAUSE OF MAINT MODE
      CMPB    FNCCNT, %1    ;MOVE IT RIGHT ONE PLACE
      BEQ      .+4          ;CHECK AGAINST FNCCNT
      HLT      ;SHOULD BE EQUAL
      INC      FNCCNT       ;FUNCTION BITS DIDN'T INCREMENT IN MAINT MODE
      CMP      #10, FNCCNT  ;GET READY FOR NEXT PASS
      BEQ      MFCHK        ;ONLY 10 BECAUSE FNCT3-1 GO TO ZERO
      MFCHK

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000000 172656      200      02, INBUF      : FAKE-OUT INTA ROUTINE
000001 172657      201      20, 0000      : DO IT AGAIN
000002 172658      202      07, BUFLEN     : SET UP FOR DATCHK (10 FNCT CHECKS, 7 TRANSFERS)
000003 172659      203      INBUF, INBUF    : RESTORE INBUF
000004 172660      204      07, DATCHK    : CHECK DATA

*****
: TEST 61 TEST FOR 10 MAINT MODE TRANSFERS
*****
SCOPE
MOV      010, BUFLEN      : BUFLEN=10
MOV      BUFLEN, WLEN     : PREPARE NUMBER FOR DRWC
MOV      WLEN, WLEN      : 2'S COMPLEMENT OF BUFLEN
MOV      07, LOOBUF      : LOAD IN BUFFER WITH INCREMENTING PATTERN
MOV      07, CHKBUF      : LOAD CHECK BUFFER WITH MODIFIED INCREMENTING PATTERN
MOV      WLEN, DRWC      : SET UP DRWC
MOV      INBUF, DRBA      : SET UP DRBA
MOV      01, DRDB      : MAINT AIDE
MOV      INTA, DRINV      : INTERRUPT VECTOR TO INTA
MOV      DRINL, DRVS      : INTERRUPT STATUS AT PRIORITY DRINL
CLR      DRPSW            : LET DR11-B INTERRUPT
MOV      010101, DRST     : MAINT, IE, AND GO TO DRST
BR       : WAIT FOR INTERRUPT
JSR      07, DATCHK

*****
: TEST 62 TEST FOR 200 NPR TRANSFERS IN MAINT MODE
*****
SCOPE
MOV      200, BUFLEN      : LENGTH OF BUFFER = 200
MOV      BUFLEN, WLEN     : PREPARE NUMBER FOR DRWC
MOV      WLEN, WLEN      : 2'S COMPLEMENT OF BUFLEN
MOV      07, LOOBUF      : LOAD INBUF WITH INCREMENTING PATTERN
MOV      07, CHKBUF      : LOAD CHKBUF WITH MODIFIED INCREMENTED PATTERN
MOV      WLEN, DRWC      : SET UP DRWC
MOV      INBUF, DRBA      : SET UP DRBA
MOV      01, DRDB      : MAINT AIDE
MOV      INTA, DRINV      : INT VECTOR TO INTA
MOV      DRINL, DRVS      : INT VECTOR AT PRIORITY DRINL
CLR      DRPSW            : LET THE DR11-B INTERRUPT
MOV      010101, DRST     : FOLLOWING TO DRST: MAINT(12), IE(06), DR(00)
BRWAIT   : USE A WAIT OR BR. INSTRUCTION
BIT      0, BRWAIT        : SEE WHICH ONE
BRANCH   : BIT 0 CLEAR = BR.

+4
BRANCH: BR      :
JSR      07, DATCHK      : CHECK THAT CORRECT DATA WAS TRANSFERRED

SCOPE
JMP      BELL            : DO IT ALL AGAIN.
LCOOBUF: MOV     INBUF, 02 : MOVE STARTING ADDRESS OF INBUF TO R2
CLR      LENCHK          : CLEAR LENGTH CHECK
CLR      02, INBUF       : CLEAR STARTING ADDRESS OF INBUF AND INC BY 2
LOADA:  INC     LENCHK    : INC LENGTH CHECK BY 1
CMP      LENCHK, BUFLEN  : CHECK FOR DONE

```



```

172060 172054      CMP      LENCHK,BUFLEN      :SEE IF THE BUFFER HAS BEEN CHECKED
                  COMPRA      :BUFFER CHECKED?
                  .+4          :CHECK END OF BUFFER + 1
                  .+4          :SEE IF TOO MANY WORDS WERE TRANSFERRED
                  .+4          :TOO MANY
                  .+4          :EXIT
000100 172012  ERRCHK:  BIT16,DRST      :CLEAR IE
172006              DRST      :CHECKING FOR ERROR
                  .+4          :ERROR SET?
171776              BIT16,DRST      :ERROR BIT IS SET
                  .+4          :CHECKING READY BIT
                  .+4          :IS ROY SET
                  .+4          :FALSE ENTRY - ERROR AND READY ARE CLEAR
                  .+4          :EXIT
:*****
:***** BELL ON PASS COMPLETE *****
:*****
000200 177566  SECT:  MOV      R20,R177566
177564              YSTB      R177564
                  .+4
000200 177565  MOV      RDR11,R2
177567              JSR      R7,TTOUT
:*****
:***** ROUTINE TO CHECK FOR TRACE TRAP TO BE RUN WITH PROGRAM *****
:*****
000470 010000  TRTRAP: JSR      R7,CKSWR      :CHECK FO CONT G
000472              BIT16  R10000,DR      :SHOULD WE RUN WITH TRACE TRAP
000474              BEQ     YESTR1      :YES
000476              TST     YESTR1      :NO HAVE WE RAN WITH TRACE TRAP ON
000478              BEQ     TRPA        :IF SO RESTORE PREVIOUS CONTENTS
000480              MOV     YESTR1,14
000482              MOV     YESTR2,16
000484              BIC     R20,RPSW
000486              JMP     TRPB
000488              TRPA:  JMP     BEGIN      :CLEAR TRACE TRAP
000490              TRPB:  0                :START OF TEST WITH TRACE OFF
:*****
:***** SAVE OLD CONTENTS. SET UP FOR TRACE TRAP *****
:*****
000710 016767  YESTR:  MOV      14,YESTR1      :SAVE ODT PC
000712              MOV     16,YESTR2      :SAVE ODT STATUS
000714              MOV     YESRT,14        :NEW TRAP VECTOR
000716              CLR     16            :NEW CONDITION CODES
000718              CLR     RPSW
000720              COM     TRPB
000722              BMI     .+10
000724              BIS     R20,RPSW
000726              JMP     BEGIN
000728              :SET TRACE TRAP
000730              :START OF TEST WITH TRACE ON
000732              YESTR1: 0                :STORAGE FOR ODT PC
000734              YESTR2: 0                :STORAG FOR ODT STATUS
000736              YESRT:  RTI            :RETURN TO PROGRAM FROM TRAP
000738              :RTI FAILED

```



```

1752 007474 010146
1753 007476 010046
1754 007500 000115
1755
1756
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1775
1776
1777

```

```

MOV R1, -(R6)
MOV R0, -(R6)
JMP (R5) ;R5 HOLDS RETURN ADDRESS

```

```

:*****
: SUBROUTINE TO POP ALL REGISTERS OFF THE STACK
:*****

```

```

RESALL: TST (R6)+
MOV (R6)+, R0
MOV (R6)+, R1
MOV (R6)+, R2
MOV (R6)+, R3
MOV (R6)+, R4
RTS R5

```

```

:*****
: ROUTINE TO SET UP INTERRUPT VECTORS
:*****

```

```

1778 007520 016700 171306
1779 007524 012720 007600
1780 007530 016710 171274
1781 007534 012767 011072 170256
1782 007540 016767 171262 170262
1783 007550 005067 170260
1784 007554 016767 171250 170254
1785 007562 005000
1786 007564 005001
1787 007566 005002
1788 007570 005003
1789 007572 005004
1790 007574 005005
1791 007576 000207

```

```

SETVEC: MOV DRINV, R0 ;R0 IS VECTOR ADDRESS
MOV DRINS, (R0)+ ;PUT SERVICE ADDRESS INTO VECTOR
MOV DRINL, (R0) ;PUT PRIORITY INTO VECTOR+2
MOV DRINT, 30 ;SET UP EMT ADDRESS
MOV DRINL, 32 ;SET UP EMT PRIORITY LEVEL
CLR 34
MOV DRINL, 36 ;SET UP TRAP ADDRESS
CLR R0 ;INITIALIZE REGISTERS
CLR R1
CLR R2
CLR R3
CLR R4
CLR R5
RTS R7

```

```

:*****
: PRIMARY INTERRUPT SERVICE ROUTINE.
: SETS UP JBLFAG WITH ADDRESS OF JOB TO BE RUNSTARS
:*****

```

```

1761 007600 005767 177414
1762 007604 001402
1763 007606 104000
1764 007610 000000
1765 007612 032777 004000 171202
1766 007620 001411
1767 007622 005767 177370
1768 007626 001002
1769 007630 104000
1770 007632 000000
1771 007634 016767 177356 177356
1772 007642 000002
1773 007644 105777 171152
1774 007650 100402
1775 007652 104000
1776 007654 000000
1777 007656 005767 177332

```

```

DRINS: TST JBFLAG ;HAS THE PREVIOUS INTERRUPT BEEN SERVICED?
BEQ DRINO
HLT ;NO
HALT ;CHECK FOR ERROR
DRINC: BIT #DSTATC, DRST ;BRANCH IF NO ERROR
BEQ DRIN3 ;IS THERE AN ERROR SERVICE ROUTINE?
TST NEXJOB+2 ;BRANCH IF THERE IS.
BNE DRIN1
HLT ;ERROR INTERRUPT, NO ERROR SERVICE.
DRIN1: MOV NEXJOB+2, JBFLAG ;SET UP JOBFLAG WITH ADDRESS OF SERVICE ROUTINE
RTI
DRIN3: TSTB DRST ;CHECK READY
BMI DRIN2 ;BRANCH IF SET
HLT
DRIN2: TST NEXJOB ;INTERRUPT WITHOUT ERROR OR READY
;IS THERE A READY SERVICE ROUTINE

```

```

007662 001002 BNE .+6 ;BRANCH IF THERE IS.
007664 104000 HLT
007666 000000 HLT
007668 177320 177322 MOV NEXJOB,JBFLAG ;READY INTERRUPT, NO READY SERVICE
007670 000002 RTI ;SET UP JOBFLAG WITH SERVICE ROUTINE ADDRESS

```

```

*****
: MASTER'S INTERRUPT SERVICE ROUTINES
: ROUTINE A, SEGMENT 0
: FILL BUFFER AND TRANSMIT
: *****

```

```

007700 012700 011034 JOBAD: MOV #LISTA,R0 ;R0 IS XMIT LIST ADDRESS
007704 012701 011046 MOV #LISTA1,R1 ;LISTA1 WILL BE REC LIST
007710 012021 MOV (R0)+,(R1)+ ;START WITH BUS ADDRESSES EQUAL
007712 012002 MOV (R0)+,R2 ;R2 HOLDS WORD COUNT OF XMIT
007714 010211 MOV R2,(R1) ;MAKE REC WORD COUNT THE SAME
007716 005402 NEG R2 ;MAKE WORD COUNT POSITIVE
007720 006302 ASL R2 ;TRANSFORM INTO BYTE COUNT
007722 060241 ADD R2,-(R1) ;ADD TO REC BUS ADDRESS
007724 005010 CLR (R0) ;CLEAR OFFSET IN XMIT LIST
007726 024040 CMP -(R0),-(R0) ;LEAVE R0=LISTA=XMIT LIST

```

```

007730 022767 000100 177264 CMP #100,JBcnt ;ENOUGH PASSES FOR BELL?
007736 003010 BGT JOBAD ;BRANCH IF NOT ENOUGH
007740 105737 177564 JOBACB: TSTB @#177564 ;TTY READY?
007744 100375 BPL JOBACB
007746 012737 000207 177556 MOV #207,@#177566 ;RING BELL
007754 005067 177242 CLR JBcnt ;RESET JOB COUNT
007760 004767 000704 JOBADA: JSR R7,SETBUF ;FILL UP XMIT BUFFER WITH SPECIAL BINARY COUNT
007764 012700 011034 MOV #LISTA,R0
007770 004767 000370 JSR R7,XMIT ;TRANSMIT DATA TO SLAVE
007774 012767 010012 177212 MOV #JOB1,NEXJOB ;JOB1 IS NEXT
010002 012767 000000 177206 MOV #0,NEXJOB+2 ;NO ERROR RECOVERY
010010 000002 RTI ;RETURN TO BACKGROUND VIA TRAP

```

```

*****
: ROUTINE A, SEGMENT 1
: FLUSH A BUFFER AND RECEIVE DATA
: *****

```

```

010012 012700 011046 JOB1: MOV #LISTA1,R0 ;PUT REC LIST ADDRESS INTO R0
010016 004767 000574 JSR R7,FLUSH ;FLUSH BUFFER
010020 012700 011046 MOV #LISTA1,R0
010026 004767 000406 JSR R7,MREC ;RECEIVE DATA FROM SLAVE
010032 012767 010050 177154 MOV #JOB2,NEXJOB ;JOB2 IS NEXT
010040 012767 000000 177150 MOV #0,NEXJOB+2 ;NO ERROR RECOVERY
010046 000002 RTI

```

```

*****
: ROUTINE A, SEGMENT 2
: CHECKS TRANSMITTED DATA WITH RECEIVED
: *****

```

```

010050 012700 011034 JOB2: MOV #LISTA,R0 ;XMIT BUFFER LIST
010054 012701 011046 MOV #LISTA1,R1 ;REC BUFFER LIST
010060 004767 000642 JSR R7,BUFCHK ;COMPARE THE TWO BUFFERS

```

```

18934 010064 042777 000100 170730
18935 010072 012777 000100 170722
18936 010100 012767 000100 177106
18937 010106 012767 000000 177102
18938 010114 035267 177102
18939 010120 000002

```

```

BIC #IE,DRST ;GLITCH INTERRUPT
MOV #IE,DRST
MOV #JOB0,NEXJOB ;REPEAT JOB0
MOV #0,NEXJOB+2
INC JBCNT ;ADVANCE COUNT
RTI

```

```

;*****
; SLAVE'S INTERRUPT SERVICE ROUTINES
;*****
JOB1: IGNORE FIRST READY INTERRUPT
;*****

```

```

18947 010122 012767 000000 177064
18948 010130 012767 010140 177060
18949 010136 000002

```

```

SJOB1: MOV #0,NEXJOB ;NO MORE READY INTERRUPTS
MOV #SJOB2,NEXJOB+2 ;UNTIL ATTN INTERRUPT
RTI

```

```

;*****
; JOB2: WAIT FOR COMMAND
;*****

```

```

18955 010140 032777 004000 170654
18956 010146 001002
18957 010150 104000
18958 010152 000000
18959 010154 005001
18960 010156 016702 170640
18961 010162 012703 000010
18962 010166 012704 004000
18963 010172 016705 170626
18964 010176 012700 011062
18965 010202 004767 000122
18966 010206 012700 011060
18967 010212 016010 000004
18968 010216 066710 170516
18969 010222 012077 170572
18970 010226 012077 170564
18971 010232 005077 170564
18972 010236 032777 002000 170556
18973 010244 001405
18974 010246 032777 000400 170546
18975 010254 001774
18976 010256 000412
18977 010260 012700 011060
18978 010264 004767 000356
18979 010270 052777 000004 170524
18980 010276 042777 000400 170516
18981 010304 052777 000101 170510
18982 010312 012767 010122 176674
18983 010320 012767 010140 176670
18984 010326 000002

```

```

SJOB2: BIT #DSTATC,DRST ;TEST FOR INTER
BNE SJOB2A
HLT
SJOB2A: CLR R1 ;ERROR OTHER THAN DSTATC
MOV DRST,R2 ;SET UP FOR PARAMETERS
MOV #FNCT3,R3 ;R2 IS STATUS ADDRESS
MOV #DSTATC,R4 ;R3 IS FUNCTION BIT 3
MOV DRDB,R5 ;R4 IS INTERRUPT BIT
MOV #LISTB+2,R0 ;R5 IS DATA BUFFER ADDRESS
JSR R7,HNDCHK ;STORE PARAMETERS HERE STARTING WITH WORD COUNT
MOV #LISTB,R0 ;GET PARAMETERS
MOV 4(R0),(R0) ;R0 IS TOP OF LIST
ADD INBUF,(R0) ;MOVE OFFSET TO TOP
MOV (R0)+,DRBA ;TOP OF LIST IS BUFFER START + OFFSET
MOV (R0)+,DRWC ;SET UP BUS ADDRESS
CLR DRST ;SET UP WORD COUNT
BIT #DSTATB,DRST ;CLEAR ALL FUNCTION BITS
BEQ SJOB2C ;WHICH DIRECTION
BIT #CYCLE,DRST ;BRANCH IF RECIEVE (LEAVE FNCT1 CLEAR FOR DATI'S)
BEQ SJOB2B ;WAIT FOR MASTER TO SET CYCLE
BR SJOB2D ;BRANCH IF NOT SET
MOV #LISTB,R0 ;GO DO THE COMAND
JSR R7,BLUSH ;BLUSH THE BUFFER
BIS #FNCT2,DRST ;SET FNCT2 FOR DATO'S
BIC #CYCLE,DRST ;CLEAR CYCLE
SJOB2C: BIS #IE!GO,DRST ;EXECUTE COMMAND AND INTERRUPT WHEN DONE
MOV #SJOB1,NEXJOB ;IGNORE READY INTERRUPT
MOV #SJOB2,NEXJOB+2 ;WAIT FOR ATTN INTERRUPT
RTI

```

```

;*****
; SLAVE ROUTINE TO ACCEPT PARAMETERS FROM MASTER
;*****

```



```

1946
1947
1948 010524 012077 170270
1949 010530 011077 170262
1950 010534 005001
1951 010536 016702 170260
1952 010542 012703 000010
1953 010546 012704 004000
1954 010552 016705 170246
1955 010556 011015
1956 010560 050312
1957 010562 030412
1958 010564 001776
1959 010566 022015
1960 010570 001402
1961 010572 104000
1962 010574 000000
1963 010576 040312
1964 010600 030412
1965 010602 001376
1966 010604 005201
1967 010606 020167 176400
1968 010612 002761
1969 010614 000207

PRMXFR: MOV (R0)+,DORBA ;FIRST WORD IN LIST IS ADDRESS
          MOV (R0),DORWC ;SECOND WORD IN LIST IS WORD COUNT
          CLR R1 ;R1 COUNTS PARAMETERS TRANSFERRED
          MOV DRST,R2 ;R2 IS THE STATUS ADDRESS
          MOV #FNCT3,R3 ;R3 USED FOR FUNCTION BIT 3
          MOV #DSTATC,R4 ;R4 USED FOR INTERRUPT BIT
          MOV DRDB,R5 ;R5 IS THE DATA BUFFER ADDRESS
PRMXF1: MOV (R0),(R5) ;SET UP DRDB WITH PARAMETER
          BIS R3,(R2) ;CALL SLAVE'S ATTN
PRMXF2: BIT R4,(R2) ;WAIT FOR REPLY
          SEQ PRMXF2 ;BRANCH IF ATTN CLEAR
          CMP (R0)+,(R5) ;COMPARE PARAMETER SENT WITH SLAVE'S ECHO
          BEQ PRMXF3 ;BRANCH IF EQUAL
          HALT ;PARAMETER DID NOT ECHO
PRMXF3: BIC R3,(R2) ;DROP SLAVE'S ATTN
PRMXF4: BIT R4,(R2) ;WAIT FOR REPLY
          BNE PRMXF4 ;BRANCH IF ATTN SET
          INC R1 ;ADVANCE PARAMETER COUNT
          CMP R1,NURDXF ;ALL PARAMETER XFERRED?
          BLT PRMXF1 ;BRANCH IF NOT DONE
          RTS R7 ;RETURN WHEN ALL PARAMETERS TRANSFERRED AND CHECKED.

;*****
; ROUTINE TO CLEAR BUFFER
; ENTER WITH R0 POINTING TO TRANSFER LIST
;*****

1970
1971
1972
1973
1974
1975
1976 010616 005005
1977 010620 004767 000030
1978 010624 004767 000004
1979 010630 002775
1980 010632 000432

FLUSH: CLR R5 ;SET R5 TO ZIP
        JSR R7,BSETUP ;SET UP REGISTERS
FLUSH1: JSR R7,BUFPUT ;STORE ITEM IN BUFFER
        BLT FLUSH1
        BR BUFOUT ;STOP WHEN BUFFER FULL

1981
1982 010634 010521
1983 010636 060303
1984 010640 005504
1985 010642 005202
1986 010644 000207

BUFPJT: MOV R5,(R1)+ ;PUT R5 INTO BUFFER
         ADD R5,R3 ;INCLUDE IN CHECKSUM
         ADC R4
         INC R2 ;ADVANCE WORD COUNT
         RTS R7 ;RETURN WITH STATUS SET

;*****
; ROUTINE TO FILL BUFFER WITH ALL ONE'S
; ENTER WITH R0 POINTING TO TRANSFER LIST
;*****

1987
1988
1989
1990
1991
1992 010646 012705 177777
1993 010652 000762

BLUSH: MOV #-1,R5 ;SET R5 TO ALL ONE'S
        BR FLUSH+2

;REGISTER SETUP ROUTINE
BSETUP: MOV (R0)+,R1 ;R1 IS BUS ADDRESS
         MOV (R0)+,R2 ;R2 IS WORD COUNT
         TST (R0)+ ;SKIP OVER OFFSET
         CLR R3 ;CLEAR LOW CHECKSUM
         CLR R4 ;CLEAR HIGH CHECKSUM
         RTS R7 ;RETURN

```



```

2058 011016 000207
2059 011020 104000
2060 011022 012105
2061 011024 060503
2062 011026 005504
2063 011030 005202
2064 011032 000207
2065 011034 013570
2066 011036 177605
2067 011040 000000
2068 011042 000000
2069 011044 000000
2070 011046 000000
2071 011050 000000
2072 011052 000000
2073 011054 000000
2074 011056 000000
2075 011060 013570
2076 011062 000000
2077 011064 000000
2078 011066 000000
2079 011070 000000
2080 011072 004767 000654
2081 011076 037727 167710 020000
2082 011104 001401
2083 011106 000002
2084 011110 012667 000172
2085 011114 012667 000170
2086 011120 024646
2087 011122 012777 000215 167734
2088 011130 105777 167726
2089 011134 100375
2090 011136 012777 000212 167720
2091 011144 105777 167712
2092 011150 100375
2093 011152 010267 000122
2094 011156 010367 000120
2095 011162 010467 000116
2096 011166 016702 000114
2097 011172 004767 000114
2098 011176 012777 000240 167660
2099 011204 105777 167652
2100 011210 100375
2101 011212 016702 000072

```

```

      RTS      R7      ;RETURN IF CHECKSUM OK.
CHKSM2: HLT
      GETBUF: MOV     (R1)+,R5 ;GET ITEM OUT OF BUFFER
      ADD     R5,R3      ;ADD TO CHECKSUM
      ADC     R4
      INC     R2
      RTS      R7      ;ADVANCE WORD COUNT

LISTA: XINBUF          ;START OF XMIT BUFFER
      -123.           ;WORD COUNT
      0              ;OFFSET
      0              ;CHECKSUM LOW
      0              ;CHECKSUM HIGH

LISTA1: 0              ;START OF REC BUFFER
      0              ;WORD COUNT
      0              ;OFFSET
      0              ;CHECKSUM LOW
      0              ;CHECKSUM HIGH

LISTB: XINBUF          ;SLAVE'S ECHO BUFFER
      0
      0
      0

;*****
;      ENTERED WITH SYSTEM TRAP CALL(HLT)
;      PRINT OUT THE ERROR PC AND STATUS REGISTER
;*****

PRINT: JSR      %7,CKSWR
      BIT      @SR,#20000 ;TEST FOR INHIBIT PRINT ON
      BEQ     .+4         ;BRANCH TO PRINT
      RTI     ;INHIBIT, RETURN TO MAIN STREAM
      MOV     (6)+,SAVPC ;PC OF FAILING ROUTINE
      MOV     (6)+,SAVCC ;CC OF ERROR CONDITION
      CMP     -(6),-(6) ;REPOSITION THE STACK
      MOV     #215,@TPB ;CR
      TSTB   @TPS
      BPL    .-4
      MOV     #212,@TPB ;LINE FEED
      TSTB   @TPS
      BPL    .-4
      MOV     %2,SAVR2 ;SAVE R2
      MOV     %3,SAVR3 ;SAVE R3
      MOV     %4,SAVR4 ;SAVE R4
      MOV     SAVPC,%2
      JSR     %7,PRTAB ;PRINT OCTAL NUMBER
      MOV     #240,@TPB
      TSTB   @TPS ;SPACE BETWEEN WORDS
      BPL    .-4
      MOV     SAVCC,%2

```

011216	004767	000070			JSR	%7.PRTAB	:PRINT OCTAL NUMBER
011222	012777	000240	167634		MOV	#240,2TPB	:PRINT SPACE
011230	105777	167626			TSTB	2TPS	:PRINTER DONE
011234	100375				BPL	-4	:BRANCH WHEN NOT DONE
011236	017702	167550			MOV	2DRST,%2	:GET DR118 STATUS
011242	004767	000044			JSR	%7.PRTAB	:PRINT OCTAL NUMBER
011246	016702	000026			MOV	SAVR2,%2	
011252	016703	000024			MOV	SAVR3,%3	
011256	016704	000022			MOV	SAVR4,%4	
011262	004767	000464			JSR	%7.CKSWR	
011266	005777	167520			TST	2SR	:CHECK SR FOR HALT SWITCH
011272	100001				BPL	.+4	
011274	000000				HALT		:HALT ON ERROR UP
011276	000002				RTI		:RETURN TO MAINLINE
011300	000000						
011302	000000			SAVR2:	0		
011304	000000			SAVR3:	0		
011306	000000			SAVR4:	0		
011310	000000			SAVPC:	0		
011310	000000			SAVCC:	0		
011312	005067	000260		PRTAB:	CLR	BINCT	
011316	005067	000252			CLR	WGCT	
011322	012704	011602			MOV	#LIST,%4	:GET LIST ADDRESS
011326	142777	000177	167526		BICB	#177,2TPS	:CLR INT FLAG
011334	012767	000005	000236		MOV	#5,ASCNT	
011342	012767	000007	000220		MOV	#7,SEVEN	
011350	012767	000001	000214		MOV	#1,DECML	
011356	105777	167500		WAIT1:	TSTB	2TPS	
011362	100375				BPL	WAIT1	
011364	005702				TST	%2	
011366	100404				BMI	MINUS	:NEG SIGN PRINT 1
011370	012777	000260	167466		MOV	#260,2TPB	:POS SIGN PRINT 0
011376	000403				BR	START	
011400	012777	000261	167456	MINUS:	MOV	#261,2TPB	
011406	016703	000156		START:	MOV	SEVEN,%3	:PUT MASK IN R3
011412	010267	000150			MOV	%2,TOODLE	:GET READY TO DOODLE NUMBER IN TOODLE
011416	005167	000144			COM	TOODLE	:COMPENSATES FOR COMPLEMENT DURING BIC
011422	046703	000140			BIC	TOODLE,%3	:AND IN OCTAL CHARACTER
011426	001410				BEQ	WRTCC	:ZERO, WRITE 0 IN LIST
011430	066767	000136	000136	MKNUM:	ADD	DECML,WGCT	:COUNT UP TO
011436	005267	000134			INC	BINCT	:AND RECORD
011442	026703	000126			CMP	WGCT,%3	:SAME BINARY WEIGHT
011446	001370				BNE	MKNUM	:KEEP COUNTN
011450	062767	000260	000120	WRTCC:	ADD	#260,BINCT	:ADD ASCII PREFIX
011456	016724	000114			MOV	BINCT,(4)+	:WRITE ASCII CHAR IN LIST
011462	066767	000102	000102		ADD	SEVEN,DECML	:EXPAND BINARY WEIGHT
011470	005067	000100			CLR	WGCT	
011474	005067	000076			CLR	BINCT	
011500	005367	000074			DEC	ASCNT	
011504	001410				BEQ	XLIST	:5 CHAR IN LIST
011506	012703	000003			MOV	#3,%3	:SET %3 FOR ADD LOOP
011512	066767	000052	000050	MOADD:	ADD	SEVEN,SEVEN	:MAKING SEVENTY BY SEVEN
011520	005303				DEC	%3	
011524	001373				BNE	MOADD	
011526	000730				BR	START	:NY SEVEN SET GET NY OCTAL
011528	012767	000005	000044	XLIST:	MOV	#5,ASCNT	:SEND 5 CHAR TO TTY

11-23398-2
111
111
111

```

000100 166360 15: BIC 0100,2TP5
000137 .EMPTY: RTS 0100,2TP5
000041 BFC 0100,2TP5
166334 15: BFC 0100,2TP5
166330 BFL 0100,2TP5
000020 .RET: INC 0100,2TP5
012560 MOV 0100,2TP5
000006 .REST: BR 0100,2TP5

012560 012564 .RETR: .BYTE 15,12,01
012564 012568 .SAV: 0
012568 012572 .BUFF: 0
012572 012576 .XINBUF: 0
012576 012580 .XCHKBU: 0
012580 012584 .END: 0

```

: CLEAR POINTER TO CHARACTER
: RETURN
: CHECK FOR RETURN TERMINATOR
: TYPE CHARACTER
: SET UP NEW POINTER
: FOR STACK POINTER 100 LOCATIONS

011572	2140*	2153	2159*	2191*										
0201036	525*	1155	133*											
0201037	525*	1330*												
0201038	518*	56*	600*	603	626*	627	842*	843	846*	847	870*	871	874*	
0201039	1206*	1011*	1027	1043*	1059	1082*	1103*	1121*	1141*	1155*	1181*	1202*	1207*	
0201024	1203	1315*	1337*	1348*	1372*	1399*	1419*	1458*	1477*	152*	1869*	1948*		
	1252*	1253	1261*	1262	1265*	1266	1276*	1277	1280*	1373*	1395	1400*	1459*	
0201030	1438*	1863	1954											
	1472*	1047	1085	1106	1124	1144	1157	1183	1209	1375	1402	1427	1461	
0207630	1481*	1744	1746	1748										
0207632	1751*	892*	911*	931*	950*	956*	1014*	1046*	1084*	1105*	1123*	1143*	1156*	
0207633	1751*	1209*	1338*	1347*	1374*	1401*	1426*	1460*	1479*	1543*	1742			
0207612	1765*	1765*												
0207634	1765*	1765*												
0207635	1765*	1765*												
0207636	1765*	1765*												
0207637	1765*	1765*												
0207638	1765*	1765*												
0207639	1765*	1765*												
0207640	1765*	1765*												
0207641	1765*	1765*												
0207642	1765*	1765*												
0207643	1765*	1765*												
0207644	1765*	1765*												
0207645	1765*	1765*												
0207646	1765*	1765*												
0207647	1765*	1765*												
0207648	1765*	1765*												
0207649	1765*	1765*												
0207650	1765*	1765*												
0207651	1765*	1765*												
0207652	1765*	1765*												
0207653	1765*	1765*												
0207654	1765*	1765*												
0207655	1765*	1765*												
0207656	1765*	1765*												
0207657	1765*	1765*												
0207658	1765*	1765*												
0207659	1765*	1765*												
0207660	1765*	1765*												
0207661	1765*	1765*												
0207662	1765*	1765*												
0207663	1765*	1765*												
0207664	1765*	1765*												
0207665	1765*	1765*												
0207666	1765*	1765*												
0207667	1765*	1765*												
0207668	1765*	1765*												
0207669	1765*	1765*												
0207670	1765*	1765*												
0207671	1765*	1765*												
0207672	1765*	1765*												
0207673	1765*	1765*												
0207674	1765*	1765*												
0207675	1765*	1765*												
0207676	1765*	1765*												
0207677	1765*	1765*												
0207678	1765*	1765*												
0207679	1765*	1765*												
0207680	1765*	1765*												
0207681	1765*	1765*												
0207682	1765*	1765*												
0207683	1765*	1765*												
0207684	1765*	1765*												
0207685	1765*	1765*												
0207686	1765*	1765*												
0207687	1765*	1765*												
0207688	1765*	1765*												
0207689	1765*	1765*												
0207690	1765*	1765*												
0207691	1765*	1765*												
0207692	1765*	1765*												
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0207694	1765*	1765*												
0207695	1765*	1765*												
0207696	1765*	1765*												
0207697	1765*	1765*												
0207698	1765*	1765*												
0207699	1765*	1765*												
0207700	1765*	1765*												
0207701	1765*	1765*												
0207702	1765*	1765*												
0207703	1765*	1765*												
0207704	1765*	1765*												
0207705	1765*	1765*												
0207706	1765*	1765*												
0207707	1765*	1765*												
0207708	1765*	1765*												
0207709	1765*	1765*												
0207710	1765*	1765*												
0207711	1765*	1765*												
0207712	1765*	1765*												
0207713	1765*	1765*												
0207714	1765*	1765*												
0207715	1765*	1765*												
0207716	1765*	1765*												
0207717	1765*	1765*												
0207718	1765*	1765*												
0207719	1765*	1765*												
0207720	1765*	1765*												
0207721	1765*	1765*												
0207722	1765*	1765*												
0207723	1765*	1765*												
0207724	1765*	1765*												
0207725	1765*	1765*												
0207726	1765*	1765*												
0207727	1765*	1765*												
0207728	1765*	1765*												
0207729	1765*	1765*												
0207730	1765*	1765*												
0207731	1765*	1765*												
0207732	1765*	1765*												
0207733	1765*	1765*												
0207734	1765*	1765*												
0207735	1765*	1765*												
0207736	1765*	1765*												
0207737	1765*	1765*												
0207738	1765*	1765*												
0207739	1765*	1765*												

UNSUB	0111310	2099*	2113	2132*															
UNSUB	0111306	2100*	2108	2131*															
UNSUB	0111300	2105*	2120	2128*															
UNSUB	0111303	2108*	2121	2129*															
UNSUB	0111304	2109*	2123	2130*															
UNSUB	1044000	452*	563	575*	590	599	613	625	638	655	672	685	699	711					
		724	737	750	809	827	941	854	859	822	900	922	941	950					
		994	1041	1075	1096	1115	1134	1153	1179	1208	1230	1250	1273	1283					
		1301	1312	1335	1366	1392	1417	1451	1470	1491									
		1919*																	
		2191*	2200*	2211	2218														
		491	2209*																
		2215	2217*	2219*	2223*														
		2214	2216	2219*															
		2010*	2016																
		1806*	2009*																
		1658	1674	1742*															
		2139*	1674	2159	2165*	2190*													
		1676	2149	1522															
		1677	1847*	1855*	1833														
		1856	1849																
		1854*	1859*																
		1873	1875																
		1873	1877*																
		1876	1891*																
		540*	541*	546	548	549	1626*												
		543*	543	547*	550	1583	2093	2124	2136	2210	2213	2238	2250	2294*					
		513*																	
		513	1672*																
		2146	2148*	2168															
		503	540*																
		494*	547																
		2233*	2254*	2255*	2238	2277*	2278*	2290*	2284										
		2236*	2242*	2243*	2275*	2277*	2279*	2290*	2284										
		2301			2244	2259*	2259	2252	2269	2271	2279*	2280	2294*	2298*					
		534*	2242	2293*	2298														
		533*	1342*	2240	2292*	2295*	2296												
		1035	1041*	1070															
		995*	1037																
		2149*	2150*	2151	2179*														
		536*	2099*	2102*	2110*	2115*	2145*	2147*	2172*	2301*	2347*								
		535*	2100	2103	2111	2116	2137*	2141	2170	2176	2299	2339*	2345						
		1586	1590*																
		1591*	1601*																
		1582*																	
		1324*	1328																
		2257	2292*																
		2296*	2297																
		2299*	2300																
		500	502	1576	2247	2249	2253	2265	2274	2334*	2348	2354							
		1022	1036*																
		1054	1069*																
		1068	1075*																
		2141*	2142																
		2170*	2171	2175															
		521*	1079*	1080*	1081	1100*	1101*	1102	1119*	1119*	1120	1138*	1139*	1140					
		1369*	1370*	1371	1396*	1397*	1398	1453*	1454*	1457	1472*	1473*	1476						

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NOV 11 1976
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CHARGE OF JURY AT 10:15 AM
FEDERAL BUREAU OF INVESTIGATION
U.S. DEPARTMENT OF JUSTICE
MEMPHIS, TENNESSEE
NOV 11 1976

