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11-22-75

2011 LOGIC TESTS

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11-22-75

11-22-75

MAINTENANCE-11-0202A-0-0
DESCRIPTION

DJ:1 LOGIC TESTS

1. ABSTRACT

THIS PROGRAM TESTS THE LOGIC OF THE CONTROL REGISTER IN MAINTENANCE MODE AT THE RIGHT LEVEL AND WHETHER IT RECEIVES CORRECTLY. THE PROGRAM SHOULD BE RUN FOR 10 MINUTES WITH SWITCHES DOWN.

2. REQUIREMENTS

2.1 EQUIPMENT

POP-11 STANDARD COMPUTER WITH CONSOLE TELETYPE UP TO 16 BILI ASYNCHRONOUS MULTIPLEXERS.

2.2 STORAGE

THIS PROGRAM USES ALL OF BK, EXCEPT ASS LOADER.

2.3 PRELIMINARY PROGRAMS

NONE

3. LOADING PROCEDURE

USE STANDARD PROCEDURE FOR ASS TAPES.

4. STARTING PROCEDURE

4.1 CONTROL SWITCH SETTINGS

SEE 5.1 (ALL DOWN FOR WORST CASE TESTING)

4.2 STARTING ADDRESS

THE PROGRAM SHOULD ALWAYS BE STARTED AT 1000. IT MAY BE RESTARTED AT 1000 AFTER ALL PARAMETERS HAVE BEEN SET.

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MAINDEC-11-DZCJA-D-D
DESCRIPTION

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4.3 PROGRAM AND OPERATOR ACTION

- 1) LOAD PROGRAM INTO MEMORY USING ABS LOADER.
- 2) LOAD ADDRESS 200.
- 3) IF HARDWARE SWITCH REGISTER IS AVAILABLE, SET SWITCHES (SEE SEC. 5.1) ALL DOWN FOR WORST CASE. PRESS START.
- 4) IF SWITCH-LESS PROCESSOR SIMPLY PRESS START.
- 5) ENTER PARAMETERS (SEE SEC. 5.3) AS THEY ARE REQUESTED.
- 6) THE PROGRAM WILL LOOP AND BELL WILL RING ONCE EVERY PASS.
- 7) A MINIMUM OF TWO PASSES SHOULD ALWAYS BE RUN.

5. OPERATING PROCEDURE

5.1 OPERATIONAL SWITCH SETTINGS

AT SA 200, ALL SWITCHES DOWN IS WORST CASE TESTING. EACH SUBTEST WILL BE LOOPED UPON UNTIL COMPLETION OF 16 PASSES OF THAT SUBTEST. THE BELL WILL RING UPON COMPLETION OF A PASS OF THE ENTIRE PROGRAM. ALTERNATE PASS WILL RUN WITH THE 1-BIT SET.

THE SWITCH SETTINGS ARE:

```

SW<15> = 1 ..... HALT ON ERROR
SW<14> = 1 ..... SCOPE LOOP
SW<13> = 1 ..... INHIBIT PRINTOUT
SW<12> = 1 ..... INHIBIT TRACE TRAPPING
SW<11> = 1 ..... INHIBIT ITERATIONS OF SUBTEST
SW<10> = 1 ..... BELL ON ERROR
SW<09> = 0 ..... BELL ON PASS COMPLETE
SW<08> = 1 ..... LOOP ON ERROR
SW<07> = 1 ..... LOOP ON TEST IN SW<7:0>
    
```

THIS PROGRAM HAS BEEN MODIFIED TO RUN ON A PROCESSOR WITH OR WITHOUT A HARDWARE SWITCH REGISTER. WHEN FIRST EXECUTED THE PROGRAM TESTS THE EXISTENCE OF A HARDWARE SWITCH REGISTER. IF NOT FOUND A SOFTWARE SWITCH REGISTER LOCATION (SWREG=LOC. 176) IS DEFAULTED TO. IF THIS IS THE CASE, UPON EXECUTION THE CONTENTS OF THE SWREG ARE DUMPED IN OCTAL ON THE CONSOLE TTY AND ANY CHANGES ARE REQUESTED

(I.E.) SWR=XXXXXX NEW=

POSSIBLE RESPONSES ARE:

1. <CR> IF NO CHANGES ARE TO BE MADE.
2. 6 DIGITS 0-7 TO REPRESENT IN OCTAL THE NEW SWITCH REGISTER VALUE: LAST DIGIT FOLLOWED BY <CR>.
3. 'U' TO ALLOW REENTERING VALUE IF ERROR IS

000000-11-00000-0
000000.P11

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COMMITTED KEYING IN SWREG VALUE.

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BUILT INTO THE PROGRAM IS THE ABILITY TO DYNAMICALLY CHANGE THE CONTENTS OF SWREG DURING PROGRAM EXECUTION. BY STRIKING PG (UNTIL G) ON CONSOLE TTY THE OPERATOR SETS A REQUEST FLAG TO CHANGE THE CONTENTS OF SWREG, WHICH IS PROCESSED IN KEY AREAS OF THE PROGRAM CODE (IE) ERROR ROUTINES, AFTER HALTS END OF PASS, AND OTHER APPLICABLE AREAS.

5.2 SUBROUTINE ABSTRACTS

5.2.1 SCOPE

THIS SUBROUTINE CALL (VIA A TRAP INSTRUCTION) IS PLACED BETWEEN EACH SUBTEST IN THE INSTRUCTION SECTION. IT RECORDS THE STARTING ADDRESS OF EACH SUBTEST AS IT IS BEING ENTERED IN LOCATION "LAD". IF A SCOPE LOOP IS REQUESTED, THE CURRENT SUBTEST WILL BE LOOPED UPON. SW<11> ON A 1 INHIBITS ITERATION OF SUBTESTS. THE CONTENTS OF "LAD" MAY BE USED TO DETERMINE THE LAST SUBTEST SUCCESSFULLY COMPLETED.

5.2.2 HLT

THIS ROUTINE (CALLED BY AN EMT INSTRUCTION) PRINTS OUT AN ERROR MESSAGE (SEE 6.1). IF SW<9> IS ON A 1 AND A HLT IS EXECUTED, THE SUBTEST WILL BE LOOPED UPON UNTIL IS CONSECUTIVE GOOD PASSES ARE COMPLETED. TO INHIBIT TYPEOUTS, PUT SW<13> ON A 1. TO RING THE BELL ON AN ERROR, PUT SW<13> ON A 1.

5.2.4 TRTRAP

IF SW<12> IS ON A 0, THE T-BIT WILL BE SET ON ALTERNATE PASSES. WHEN THE T-BIT IS SET, THE PROCESSOR TRAPS AFTER EACH INSTRUCTION. THE FIRST INSTRUCTION EXECUTED UPON TRAPPING IS AN "RTI" OR "RTT" WHICH RETURNS TO THE INTERRUPTED SEQUENCE OF INSTRUCTIONS. THIS SEQUENCE IS CONTINUED UNTIL THE END OF THE PROGRAM IS REACHED.

5.2.5 TRAPCATCHER

A ".+2" - "HALT" SEQUENCE IS REPEATED FROM 0 - 56 TO DETECT ANY UNEXPECTED TRAPS AND A ".+2" - "IOT" SEQUENCE IS REPEATED FROM 50 - 775 TO DETECT ANY UNEXPECTED INTERRUPTS. THIS ANY UNEXPECTED TRAPS WILL HALT AT THE VECTOR + 2. ANY UNEXPECTED INTERRUPTS WILL RESULT IN AN ERROR "HLT" IN "IOTRAP".

L01

MAINDEC-11-DZDJA-D
DZDJA.P11

DJ11 LOGIC TESTS

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(RN) = CONTENTS OF GENERAL REGISTER "N" FROM NONE TO
FOUR OF THESE MAY BE TYPED DEPENDING ON THE NUMBER

MAINDEC-11-DZDJA-D-D
DESCRIPTION

DJ11 LOGIC TESTS

FOLLOWING THE HLT: E.G.. HLT+3 WOULD TYPE (R1)
THRU (R3); HLT (BY ITSELF) WOULD STOP AFTER TYPING
ADR AND DJADR.

TO FIND THE FAILING TEST, LOOK AT THE LISTING ABOVE THE
ADDRESS TYPED. IN MOST CASES THE COMMENT BESIDE THE HLT
TELLS WHAT WAS BEING CHECKED AND WHAT WAS EXPECTED. ALSO, A
LIST OF THE PROBABLE FAILING LOGIC IS GIVEN IN THE COMMENTS
AT THE BEGINNING OF THE TEST.

6.2 ERROR RECOVERY

RESTART AT 200 OR 1000.

6.3 ERROR COUNTER

AN ERROR COUNT IS KEPT IN "ERRORS" (LOC 1202). IT CAN BE
CLEARED FROM THE CONSOLE, BY RESTARTING AT 200, OR BY
RELOADING THE PROGRAM.

7. RESTRICTIONS

IF MORE THAN ONE DJ11 IS TESTED AT A TIME, THE DEVICE
ADDRESSES AND THE VECTOR ADDRESSES MUST ALL BE CONTIGUOUS.

IF THIS PROGRAM IS RUN WITH A MONITOR, I.E. ACT11 OR DDP,
THE DEVICE ADDRESSES MUST FOLLOW THE FLOATING ADDRESS
CONVENTION. DJ11'S WILL BE FIRST, STARTING AT 160010..

8. MISCELLANEOUS

8.1 EXECUTION TIME

DUE TO THE VARIOUS BAUD RATES AVAILABLE AND THE ABILITY TO
CHECK UP TO 8 DJ11'S AT ONCE, THE EXECUTION TIME CAN BE
ANYWHERE FROM 15 SECONDS TO THREE AND A HALF HOURS. THE
FOLLOWING TYPICAL TIMES ARE FOR ONE DJ11 WITH ALL LINES AT
THE SAME SPEED, 8 LEVEL CODE, 2 STOP BITS, AND NO PARITY ON
A PDP-11/20 WITHOUT TRACE TRAPPING. FOR MULTIPLE DJ11'S,
MULTIPLY THESE TIMES BY THE NUMBER OF UNITS SELECTED FOR
TEST.

BAUD RUN TIME

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110 00:18:00
134.5 00:15:00

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MAINDEC-11-DZDJA-
DZDJA.D.P11

DJ11 LOGIC TESTS

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150 00:13:00
300 00:05:30

001642 012702 016512 : CHECK STRING FOR VALID DIGITS, TERMINATOR, AND 'P'
001638 004737 016354 : CHECK

```
001505 000004 017244 GETADR: TYPE, MSGADR ;TYPE "FIRST DJ11 ADDRESS"  
001504 004537 016216 JSR, R5, READIN ;READ INPUT FROM TTY AND SAVE  
001503 001230 .WORD DEVADR ;IN DEVADR  
001502 000000 BNE GETADR ;BRANCH IF BAD INPUT  
001501 005737 001230 TST DEVADR  
001500 001003 BNE IS ;  
001499 012737 001312 MOV DEFADR, DEVADR  
001498 042737 000000 IS: BIC #7, DEVADR  
001497 022737 163000 CMP #16000, DEVADR  
001496 101355 BHI GETADR
```

```
BEGIN: MOV #ICNT, SP ;SET UP STACK POINTER  
JSR PC, SUSWAR ;CHECK FOR SWITCH REGISTER  
MOV #14, R0  
MOV #YESRT, (R0)+ ;TRACE TRAP VECTOR (14)  
MOV #340, (R0)+ ;IOT VECTOR (20)  
MOV #IOTRAP, (R0)+ ;IOT VECTOR (20)  
MOV #340, (R0)+  
MOV #PDOWNS, (R0)+ ;POWER FAIL VECTOR (24)  
MOV #340, (R0)+  
MOV #EMTS, (R0)+ ;EMT VECTOR (30)  
MOV #340, (R0)+  
MOV #TRAPS, (R0)+ ;TRAP VECTOR (34)  
MOV #340, (R0)+  
MOV #IS, J#10  
SXT R0 ;CHECK FOR PDP-11/40 OR 45  
MOV #RTI, 2#YESRT  
MOV #RTI, 2#6  
MOV #400, J#177774 ;SET UP STACK LIMIT TO 1000  
CLR #6  
MOV #12, J#10  
CLR ERRORS ;CLEAR ERROR COUNTER  
CLR PCNT ;CLEAR PASS COUNTER  
CLR PCNT+2  
TST #42 ;CHECK FOR ACT11 OR DDP PRESENT  
GETADR ;BRANCH IF NONE  
JSR PC, AUTO ;GO TO SUBROUTINE TO "MAP" DJ11 ON THE SYS  
JMP RESTAR ;SKIP OPERATOR ACTION
```

```
GETADR: TYPE, MSGADR ;TYPE "FIRST DJ11 ADDRESS"  
JSR, R5, READIN ;READ INPUT FROM TTY AND SAVE  
.WORD DEVADR ;IN DEVADR  
BNE GETADR ;BRANCH IF BAD INPUT  
TST DEVADR  
BNE IS ;  
MOV DEFADR, DEVADR  
IS: BIC #7, DEVADR  
CMP #16000, DEVADR  
BHI GETADR
```

```
GETVEC: TYPE, MSGVEC ;TYPE "VECTOR ADDRESS:"  
JSR, R5, READIN ;READ INPUT FROM TTY AND SAVE  
.WORD VECADR ;IN VECADR  
BNE GETVEC ;BRANCH IF BAD INPUT  
TST VECADR ;CHECK FOR CR  
BNE IS  
MOV #300, VECADR ;SET TO FIRST FLOATING VECTOR  
IS: BIC #7, VECADR ;CLEAR TO MODULO 10  
CMP #300, VECADR ;CHECK FOR LOW LIMIT  
BGT GETVEC  
CMP #1000, VECADR ;CHECK FOR UPPER LIMIT  
BLE GETVEC
```

```
GETNUM: TYPE, MSGNUM ;TYPE "NUMBER OR UNITS:"  
JSR PC, READS ;READ INPUT FROM THE TTY  
: CHECK STRING FOR VALID DIGITS, TERMINATOR, AND 'P'  
MOV #INPUT, R2 ;POINTS TO INPUT STRING
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002304 012706 001230
002310 005737 001322
002314 001410
002316 022737 000176 001316
002324 001001
002326 034737 017770
002332 005037 001322
002336 012700 000300
002342 005720
002344 010060 177776
002350 012720 000004
002354 022700 001000
002360 001370
002362 062737 000010 001210
002370 062737 000010 001220
002376 062737 000004 001306
002404 006337 001310
002410 023737 001304 001234
002416 002416
002420 005037 001304
002424 013737 001230 001210
002432 013737 001232 001220
002440 012737 001236 001306
002446 012737 000001 001310
002454 005237 001304
002460 013701 001210
002464 062701 000002
002470 010137 001212
002474 062701 000002
002500 010137 001214

002504 062701 000002
002510 010137 001216
002514 013701 001220
002520 005721
002522 010137 001222
002526 005721
002530 010137 001224
002534 005721
002536 010137 001226
002542 005037 001200
002546 005037 015770
002552 104400

RESTAR: RESET :ISSUE RESET
MOV #ICNT, SP :SET UP STACK POINTER
TST FTIME
BEQ CLRVEC
CMP #SWREG, SWR
SNE CLRVEC
JSR PC, CNTLU
CLR FTIME
CLRVEC: MOV #300, R0 :BEGINNING OF FLOATING VECTORS
1\$: TST (R0)+
MOV R0, -2(R0) :":+2"
MOV #IOT, (R0)+ :":IOT"
CMP #1000, R0
BNE 1\$
ADD #10, CSR :UPDATE DEVICE ADDRESS TO NEXT UNIT
ADD #10, RCVVEC :UPDATE DEVICE VECTOR ADDRESS
ADD #4, DJLEN :MOVE CHAR TABLE POINTER
ASL DJPAR :UPDATE PARITY FLAG MARKER
CMP DJJUT, UNITS
BLT 2\$
CLR DJJUT
MOV DEVADR, CSR
MOV VECADR, RCVVEC
MOV #LENGTH, DJLEN :INIT CHAR TABLE POINTER
MOV #1, DJPAR :INIT PARITY FLAG MARKER
2\$: INC DJJUT
MOV CSR, R1 :SET UP ALL THE REGISTER ADDRESSES
ADD #2, R1 :ADD 2
MOV R1, RBUF :SET UP RECEIVER BUFFER
ADD #2, R1 :ADD 2
MOV R1, TCR :SET UP TRANSMITTER CONTROL REG
AND BREAK STATUS REG
ADD #2, R1 :ADD 2
MOV R1, TBUF :SET UP TRANSMITTER BUFFER
MOV RCVVEC, R1 :POINTER FOR VECTOR SETUP
TST (R1)+ :INC R1
MOV R1, RCVLVL :SET INT LVL
TST (R1)+ :INC R1
MOV R1, XMTVEC :TRANSMITTER VECTOR
TST (R1)+ :INC R1
MOV R1, XMTLVL :XMT INT LVL ADR
CLR ICNT
CLR LAD
SCOPE

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: TEST 1: TEST ABILITY TO REFERENCE CSR WITHOUT TRAPPING
: AND ABILITY TO CLR CSR.
: PROBABLE FAULTY LOGIC: M105; M7285 (D2-6) E29
:*****

```
TST1:  MOV  #15, 2#4      ;SET UP TIME-OUT TRAP VECTOR
        MOV  #LEVEL7, 2#6
        TST  2CSR        ;REFERENCE CSR (READ)
        CLR  2CSR        ;CLEAR CSR (WRITE)
        ADC  2CSR        ;CHECK CSR (READ AND WRITE)
        BEQ  2$          ;BRANCH IF OK
        HLT                ;CSR NOT CLEARED

        BR   2$          ;SKIP ISR

1$:    MOV  (SP)+, R1     ;SAVE RTI ADR FOR TYPING
        HLT+1           ;CAN'T REFERENCE CSR!

        TST  (SP)+       ;FINISH CLEARING STACK
2$:    MOV  #5, 2#4
        CLR  2#6
        SCOPE
```

: TEST 2: TEST THAT CSR BIT1 CAN BE SET AND CLEARED
: PROBABLE FAULTY LOGIC: M7285 (D2-2) E25, E7, (D2-4) E47, E64
:*****

```
TST2:  MOV  #BIT1, 2CSR  ;SET BIT1
        BIT  #BIT1, 2CSR ;CHECK THAT BIT1 IS SET
        BNE .+4          ;BRANCH IF OK
        HLT                ;CSR BIT1 FAILED TO SET

        BIT  #177775, 2CSR ;CHECK THAT NO OTHER BIT SET
        BEQ .+4          ;BRANCH IF OK
        HLT                ;EXTRA BIT SET IN CSR

        CLR  2CSR        ;CLEAR BIT1
        BIT  #BIT1, 2CSR ;CHECK THAT BIT1 IS CLEARED
        BEQ .+4          ;BRANCH IF OK
        HLT                ;CSR BIT1 FAILED TO CLEAR

        SCOPE
```

: TEST 3: TEST THAT CSR BIT2 CAN BE SET AND CLEARED
: PROBABLE FAULTY LOGIC: M7285 (D2-2) E25, E7, (D2-4) E47, E64
:*****

```
TST3:  MOV  #BIT2, 2CSR  ;SET BIT2
        BIT  #BIT2, 2CSR ;CHECK THAT BIT2 IS SET
        BNE .+4          ;BRANCH IF OK
        HLT                ;CSR BIT2 FAILED TO SET
```

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002726 032777 177773 176254 BIT #177773,0CSR ;CHECK THAT NO OTHER BIT SET
002734 001401 BEQ .+4 ;BRANCH IF OK
002736 104000 HLT ;EXTRA BIT SET IN CSR

002740 005077 176244 CLR 0CSR ;CLEAR BIT2
002744 032777 000004 176235 BIT #BIT2,0CSR ;CHECK THAT BIT2 IS CLEARED
002752 001401 BEQ .+4 ;BRANCH IF OK
002754 104000 HLT ;CSR BIT2 FAILED TO CLEAR

002756 104400 SCOPE

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:*****
:TEST 4: TEST THAT CSR BIT5 CAN BE SET AND CLEARED
:PROBABLE FAULTY LOGIC: M7285 (D2-2) E4,E18, (D2-4) E47,E67
:*****

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002760 012777 000100 176222 TST4: MOV #BIT5,0CSR ;SET BIT5
002766 032777 000100 176214 BIT #BIT5,0CSR ;CHECK THAT BIT5 IS SET
002774 001001 BNE .+4 ;BRANCH IF OK
002776 104000 HLT ;CSR BIT5 FAILED TO SET

003000 032777 177677 176202 BIT #177677,0CSR ;CHECK THAT NO OTHER BIT SET
003006 001401 BEQ .+4 ;BRANCH IF OK
003010 104000 HLT ;EXTRA BIT SET IN CSR

003012 005077 176172 CLR 0CSR ;CLEAR BIT5
003016 032777 000100 176164 BIT #BIT5,0CSR ;CHECK THAT BIT5 IS CLEARED
003024 001401 BEQ .+4 ;BRANCH IF OK
003026 104000 HLT ;CSR BIT5 FAILED TO CLEAR

003030 104400 SCOPE

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:*****
:TEST 5: TEST THAT CSR BIT8 CAN BE SET AND CLEARED
:PROBABLE FAULTY LOGIC: M7285 (D2-2) E6,E18, (D2-4) E47,E31
:*****

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003032 012777 000400 176150 TST5: MOV #BIT8,0CSR ;SET BIT8
003040 032777 000400 176142 BIT #BIT8,0CSR ;CHECK THAT BIT8 IS SET
003046 001001 BNE .+4 ;BRANCH IF OK
003050 104000 HLT ;CSR BIT8 FAILED TO SET

003052 032777 177377 176130 BIT #177377,0CSR ;CHECK THAT NO OTHER BIT SET
003060 001401 BEQ .+4 ;BRANCH IF OK
003062 104000 HLT ;EXTRA BIT SET IN CSR

003064 005077 176120 CLR 0CSR ;CLEAR BIT8
003070 032777 000400 176112 BIT #BIT8,0CSR ;CHECK THAT BIT8 IS CLEARED
003076 001401 BEQ .+4 ;BRANCH IF OK
003100 104000 HLT ;CSR BIT8 FAILED TO CLEAR

003102 104400 SCOPE

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:*****
:TEST 6: TEST THAT CSR BIT10 CAN BE SET AND CLEARED
:PROBABLE FAULTY LOGIC: M7295 (D2-2) E30,E24, (D2-4) E47,E31
:*****

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003104	012777	002000	176076	TST6:	MOV	#BIT10,0CSR	:SET BIT10
003112	032777	002000	176076		BIT	#BIT10,0CSR	:CHECK THAT BIT10 IS SET
003120	001001				BNE	.+4	:BRANCH IF OK
003122	104000				HLT		:CSR BIT10 FAILED TO SET
003124	032777	175777	176056		BIT	#175777,0CSR	:CHECK THAT NO OTHER BIT SET
003132	001401				BEQ	.+4	:BRANCH IF OK
003134	104000				HLT		:EXTRA BIT SET IN CSR
003136	005077	176046			CLR	0CSR	:CLEAR BIT10
003142	032777	002000	176040		BIT	#BIT10,0CSR	:CHECK THAT BIT10 IS CLEARED
003150	001401				BEQ	.+4	:BRANCH IF OK
003152	104000				HLT		:CSR BIT10 FAILED TO CLEAR
003154	104400						SCOPE

 :TEST 7: TEST THAT CSR BIT12 CAN BE SET AND CLEARED
 :PROBABLE FAULTY LOGIC: M7285 (D2-2) E5,E1. (D2-4) E47,E31

003156	012777	010000	176024	TST7:	MOV	#BIT12,0CSR	:SET BIT12
003164	032777	010000	176016		BIT	#BIT12,0CSR	:CHECK THAT BIT12 IS SET
003172	001001				BNE	.+4	:BRANCH IF OK
003174	104000				HLT		:CSR BIT12 FAILED TO SET
003176	032777	167777	176004		BIT	#167777,0CSR	:CHECK THAT NO OTHER BIT SET
003204	001401				BEQ	.+4	:BRANCH IF OK
003206	104000				HLT		:EXTRA BIT SET IN CSR
003210	005077	175774			CLR	0CSR	:CLEAR BIT12
003214	032777	010000	175766		BIT	#BIT12,0CSR	:CHECK THAT BIT12 IS CLEARED
003222	001401				BEQ	.+4	:BRANCH IF OK
003224	104000				HLT		:CSR BIT12 FAILED TO CLEAR
003226	104400						SCOPE

 :TEST 10: TEST THAT CSR BIT14 CAN BE SET AND CLEARED
 :PROBABLE FAULTY LOGIC: M7285 (D2-2) E3,E1. (D2-4) E47,E31

003230	012777	040000	175752	TST10:	MOV	#BIT14,0CSR	:SET BIT14
003236	032777	040000	175744		BIT	#BIT14,0CSR	:CHECK THAT BIT14 IS SET
003244	001001				BNE	.+4	:BRANCH IF OK
003246	104000				HLT		:CSR BIT14 FAILED TO SET
003250	032777	137777	175732		BIT	#137777,0CSR	:CHECK THAT NO OTHER BIT SET
003256	001401				BEQ	.+4	:BRANCH IF OK
003260	104000				HLT		:EXTRA BIT SET IN CSR
003262	005077	175722			CLR	0CSR	:CLEAR BIT14
003266	032777	040000	175714		BIT	#BIT14,0CSR	:CHECK THAT BIT14 IS CLEARED
003274	001401				BEQ	.+4	:BRANCH IF OK

M02

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TST10: TEST BIT14 OF CSR

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003276 104000

HLT

:CSR BIT14 FAILED TO CLEAR

003300 104400

SCOPE

:TEST 11: TEST THAT RECEIVER ENABLE (BIT0 OF THE CSR, CAN BE SET
AND CLEARED, AND THAT CLEAR MOS (BIT3) IS WRITE ONLY.
:PROBABLE FAULTY LOGIC: M7285 (D2-2) E26,E36,E7,E24, (D2-8) E17,E14,E15

003302 012777 000004 175700

TST11: MOV #BIT2, @CSR

:SET MAINTENANCE MODE (BIT2)

003310 005005

CLR R5

:SET UP COUNTER

003312 052777 000010 175670

1\$: BIS #BIT3, @CSR

:SET CLEAR MOS (BIT3)

003320 017701 175664

MOV @CSR, R1

:SAVE CSR

003324 032701 000010

BIT #BIT3, R1

:CHECK CLEAR MOS (BIT3)

003330 001401

BEQ .+4

:BRANCH IF OK

003332 104001

HLT+1

:CLEAR MOS (BIT3) SET (WRITE-ONLY).

003334 032701 000020

BIT #BIT4, R1

:CHECK CLEAR MOS FLAG

003340 001403

BEQ 2\$

:BRANCH IF CLEARED

003342 105305

DECB R5

:WAIT FOR MOS TO CLEAR

003344 001365

BVE 1\$

:BRANCH IF MORE TIME

003346 104001

HLT+1

:CLEAR MOS FLAG (BIT4) FAILED TO CLEAR

003350 022701 000004

2\$: CMP #BIT2, R1

:CHECK THAT ONLY MAINTENANCE BIT SET

003354 001401

BEQ .+4

:BRANCH IF OK

003356 104001

HLT+1

:CLEAR MOS CLEARED MAINTENANCE

003360 052777 000001 175622

BIS #BIT0, @CSR

:SET RECEIVER ENABLE

003366 017701 175616

MOV @CSR, R1

:SAVE CSR

003372 032777 000001 175610

BIT #BIT0, @CSR

:CHECK THAT RECEIVER ENABLE SET

003400 001001

BNE .+4

:BRANCH IF OK

003402 104001

HLT+1

:RECEIVER ENABLE FAILED TO SET

003404 022777 000005 175576

CMP #5, @CSR

:CHECK REST OF CSR

003412 001401

BEQ .+4

:BRANCH IF OK

003414 104001

HLT+1

:CSR ERROR

003416 042777 000001 175564

NOTE: IF THE TTY MODULE IS BEING USED AND DONE (BIT7) IS SET,
THE ERROR COULD BE DUE TO MAINTENANCE OR CLEAR MOS NOT WORKING.

:R1 = CONTENTS OF CSR

003424 017701 175560

BIC #BIT0, @CSR

:CLEAR RECEIVER ENABLE

003430 022777 000004 175552

MOV @CSR, R1

:SAVE CSR

003436 001401

CMP #BIT2, @CSR

:CHECK CSR

003440 104001

BEQ .+4

:BRANCH IF OK

003442 104400

HLT+1

:RECEIVER ENABLE DIDN'T CLEAR

003442 104400

HLT+1

:OR OTHER CSR BIT SET

003442 104400

HLT+1

:R1 = CONTENTS OF CSR

SCOPE

:TEST 12: TEST THAT CSR RESPONDS PROPERLY TO BYTE COMMANDS
:PROBABLE FAULTY LOGIC: M7285 (D2-4) E47

ALSO CHECK THAT THE RIGHT LINE NO. (C) APPEARS IN TO_FF

PROBABLE FAULTY LOGIC: M7295 (D2-5 ALL, D2-6, E23, E32, E33, E19) ...

LINE	TEST	STATUS	DESCRIPTION
10000	TEST 1	OK	...
10001	TEST 2	OK	...
10002	TEST 3	OK	...
10003	TEST 4	OK	...
10004	TEST 5	OK	...
10005	TEST 6	OK	...
10006	TEST 7	OK	...
10007	TEST 8	OK	...
10008	TEST 9	OK	...
10009	TEST 10	OK	...
10010	TEST 11	OK	...
10011	TEST 12	OK	...
10012	TEST 13	OK	...
10013	TEST 14	OK	...
10014	TEST 15	OK	...
10015	TEST 16	OK	...
10016	TEST 17	OK	...
10017	TEST 18	OK	...
10018	TEST 19	OK	...
10019	TEST 20	OK	...
10020	TEST 21	OK	...
10021	TEST 22	OK	...
10022	TEST 23	OK	...
10023	TEST 24	OK	...
10024	TEST 25	OK	...
10025	TEST 26	OK	...
10026	TEST 27	OK	...
10027	TEST 28	OK	...
10028	TEST 29	OK	...
10029	TEST 30	OK	...
10030	TEST 31	OK	...
10031	TEST 32	OK	...
10032	TEST 33	OK	...
10033	TEST 34	OK	...
10034	TEST 35	OK	...
10035	TEST 36	OK	...
10036	TEST 37	OK	...
10037	TEST 38	OK	...
10038	TEST 39	OK	...
10039	TEST 40	OK	...
10040	TEST 41	OK	...
10041	TEST 42	OK	...
10042	TEST 43	OK	...
10043	TEST 44	OK	...
10044	TEST 45	OK	...
10045	TEST 46	OK	...
10046	TEST 47	OK	...
10047	TEST 48	OK	...
10048	TEST 49	OK	...
10049	TEST 50	OK	...
10050	TEST 51	OK	...
10051	TEST 52	OK	...
10052	TEST 53	OK	...
10053	TEST 54	OK	...
10054	TEST 55	OK	...
10055	TEST 56	OK	...
10056	TEST 57	OK	...
10057	TEST 58	OK	...
10058	TEST 59	OK	...
10059	TEST 60	OK	...
10060	TEST 61	OK	...
10061	TEST 62	OK	...
10062	TEST 63	OK	...
10063	TEST 64	OK	...
10064	TEST 65	OK	...
10065	TEST 66	OK	...
10066	TEST 67	OK	...
10067	TEST 68	OK	...
10068	TEST 69	OK	...
10069	TEST 70	OK	...
10070	TEST 71	OK	...
10071	TEST 72	OK	...
10072	TEST 73	OK	...
10073	TEST 74	OK	...
10074	TEST 75	OK	...
10075	TEST 76	OK	...
10076	TEST 77	OK	...
10077	TEST 78	OK	...
10078	TEST 79	OK	...
10079	TEST 80	OK	...
10080	TEST 81	OK	...
10081	TEST 82	OK	...
10082	TEST 83	OK	...
10083	TEST 84	OK	...
10084	TEST 85	OK	...
10085	TEST 86	OK	...
10086	TEST 87	OK	...
10087	TEST 88	OK	...
10088	TEST 89	OK	...
10089	TEST 90	OK	...
10090	TEST 91	OK	...
10091	TEST 92	OK	...
10092	TEST 93	OK	...
10093	TEST 94	OK	...
10094	TEST 95	OK	...
10095	TEST 96	OK	...
10096	TEST 97	OK	...
10097	TEST 98	OK	...
10098	TEST 99	OK	...
10099	TEST 100	OK	...

PROBABLE FAULTY LOGIC: M7295 (D2-5 ALL, D2-6, E23, E32, E33, E19) ...

LINE	TEST	STATUS	DESCRIPTION
10000	TEST 1	OK	...
10001	TEST 2	OK	...
10002	TEST 3	OK	...
10003	TEST 4	OK	...
10004	TEST 5	OK	...
10005	TEST 6	OK	...
10006	TEST 7	OK	...
10007	TEST 8	OK	...
10008	TEST 9	OK	...
10009	TEST 10	OK	...
10010	TEST 11	OK	...
10011	TEST 12	OK	...
10012	TEST 13	OK	...
10013	TEST 14	OK	...
10014	TEST 15	OK	...
10015	TEST 16	OK	...
10016	TEST 17	OK	...
10017	TEST 18	OK	...
10018	TEST 19	OK	...
10019	TEST 20	OK	...
10020	TEST 21	OK	...
10021	TEST 22	OK	...
10022	TEST 23	OK	...
10023	TEST 24	OK	...
10024	TEST 25	OK	...
10025	TEST 26	OK	...
10026	TEST 27	OK	...
10027	TEST 28	OK	...
10028	TEST 29	OK	...
10029	TEST 30	OK	...
10030	TEST 31	OK	...
10031	TEST 32	OK	...
10032	TEST 33	OK	...
10033	TEST 34	OK	...
10034	TEST 35	OK	...
10035	TEST 36	OK	...
10036	TEST 37	OK	...
10037	TEST 38	OK	...
10038	TEST 39	OK	...
10039	TEST 40	OK	...
10040	TEST 41	OK	...
10041	TEST 42	OK	...
10042	TEST 43	OK	...
10043	TEST 44	OK	...
10044	TEST 45	OK	...
10045	TEST 46	OK	...
10046	TEST 47	OK	...
10047	TEST 48	OK	...
10048	TEST 49	OK	...
10049	TEST 50	OK	...
10050	TEST 51	OK	...
10051	TEST 52	OK	...
10052	TEST 53	OK	...
10053	TEST 54	OK	...
10054	TEST 55	OK	...
10055	TEST 56	OK	...
10056	TEST 57	OK	...
10057	TEST 58	OK	...
10058	TEST 59	OK	...
10059	TEST 60	OK	...
10060	TEST 61	OK	...
10061	TEST 62	OK	...
10062	TEST 63	OK	...
10063	TEST 64	OK	...
10064	TEST 65	OK	...
10065	TEST 66	OK	...
10066	TEST 67	OK	...
10067	TEST 68	OK	...
10068	TEST 69	OK	...
10069	TEST 70	OK	...
10070	TEST 71	OK	...
10071	TEST 72	OK	...
10072	TEST 73	OK	...
10073	TEST 74	OK	...
10074	TEST 75	OK	...
10075	TEST 76	OK	...
10076	TEST 77	OK	...
10077	TEST 78	OK	...
10078	TEST 79	OK	...
10079	TEST 80	OK	...
10080	TEST 81	OK	...
10081	TEST 82	OK	...
10082	TEST 83	OK	...
10083	TEST 84	OK	...
10084	TEST 85	OK	...
10085	TEST 86	OK	...
10086	TEST 87	OK	...
10087	TEST 88	OK	...
10088	TEST 89	OK	...
10089	TEST 90	OK	...
10090	TEST 91	OK	...
10091	TEST 92	OK	...
10092	TEST 93	OK	...
10093	TEST 94	OK	...
10094	TEST 95	OK	...
10095	TEST 96	OK	...
10096	TEST 97	OK	...
10097	TEST 98	OK	...
10098	TEST 99	OK	...
10099	TEST 100	OK	...

E03

TEST 22: MASTER TRANSMIT SCAN ENABLE

17465E 58: BIC #BIT0, #R1
MOV #20SR, R1
BPL HLT+1
SCOPE

17465E 58: BIC #BIT0, #R1
MOV #20SR, R1
BPL HLT+1
SCOPE

: THEN MASTER TRAN SCAN ENABLE
: CLEAR IT OUT
: CHECK AND SAVE TRAN READY
: BRANCH IF OK
: TRAN READY DIDN'T CLEAR.

: TEST 22: TEST THAT INTERRUPT DOES NOT OCCUR AT LEVEL 7
: PROBABLE FAULTY LOGIC: M7821 WIRING, PROPER PRIORITY CHIP

17465E 58: BIC #BIT0, #R1
MOV #20SR, R1
BPL HLT+1
SCOPE

17465E 58: BIC #BIT0, #R1
MOV #20SR, R1
BPL HLT+1
SCOPE

: TEST 22: TEST THAT INTERRUPT DOES NOT OCCUR AT LEVEL 7
: PROBABLE FAULTY LOGIC: M7821 WIRING, PROPER PRIORITY CHIP

: SET UP XMTR INTERRUPT VECTOR
: AT LEVEL 7
: CLEAR PS LEVEL
: SET PS TO LEVEL 7
: SET TRAN MASTER INT. ENABLE
: SET TRAN CONTROL BIT, LINE C
: WAIT
: OK, BRANCH IF NO INTERRUPT

17465E 58: BIC #BIT0, #R1
MOV #20SR, R1
BPL HLT+1
SCOPE

17465E 58: BIC #BIT0, #R1
MOV #20SR, R1
BPL HLT+1
SCOPE

: SHOULD'N'T HAVE INTERRUPTED AT LEVEL 7
: MOVE NEW RTI ADR ONTO STACK

17465E 58: BIC #BIT0, #R1
MOV #20SR, R1
BPL HLT+1
SCOPE

17465E 58: BIC #BIT0, #R1
MOV #20SR, R1
BPL HLT+1
SCOPE

: SET UP XMTR INTERRUPT VECTOR
: AT LEVEL 7
: CLEAR PS LEVEL
: SET PS TO LEVEL 7
: SET TRAN MASTER INT. ENABLE
: SET TRAN CONTROL BIT, LINE C
: WAIT
: OK, BRANCH IF NO INTERRUPT

SCOPE

SCOPE

: TEST 23: TEST THAT INTERRUPT DOES NOT OCCUR AT LEVEL 6
: PROBABLE FAULTY LOGIC: M7821 WIRING, PROPER PRIORITY CHIP

17465E 58: BIC #BIT0, #R1
MOV #20SR, R1
BPL HLT+1
SCOPE

17465E 58: BIC #BIT0, #R1
MOV #20SR, R1
BPL HLT+1
SCOPE

: SET UP XMTR INTERRUPT VECTOR
: AT LEVEL 7
: CLEAR PS LEVEL
: SET PS TO LEVEL 6
: SET TRAN MASTER INT. ENABLE
: SET TRAN CONTROL BIT, LINE C
: WAIT
: OK, BRANCH IF NO INTERRUPT

17465E 58: BIC #BIT0, #R1
MOV #20SR, R1
BPL HLT+1
SCOPE

17465E 58: BIC #BIT0, #R1
MOV #20SR, R1
BPL HLT+1
SCOPE

: SHOULD'N'T HAVE INTERRUPTED AT LEVEL 6
: MOVE NEW RTI ADR ONTO STACK

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DJ11 LOGIC TESTS
TEST TRANSMIT INTERRUPT LEVEL

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TST23:

END23: MOV XMTLVL, @XMTVEC
MOV #IOT, @XMTLVL
CLR @TCR
CLR @CSR
BIC #340, @#PS

004654 012777 001226 174442
004656 012777 000004 174436
004658 005077 174420
004660 005077 174410
004662 042737 000340 177776
004666 104400

SCOPE

:TEST 24: TEST THAT INTERRUPT DOES NOT OCCUR AT LEVEL 5
:PROBABLE FAULTY LOGIC: M7821 WIRING, PROPER PRIORITY CHIP

TST24: MOV #ISR24, @XMTVEC ;SET UP XMTR INTERRUPT VECTOR
MOV #340, @XMTLVL ;AT LEVEL 7
BIC #340, @#PS ;CLEAR PS LEVEL
BIS #240, @#PS ;SET PS TO LEVEL 5
MOV #040400, @CSR ;SET TRAN MASTER INT. ENABLE
MOV #BITC, @TCR ;SET TRAN CONTROL BIT, LINE C
IS: MOV @CSR, R1 ;WAIT
BPL IS
BR END24 ;OK, BRANCH IF NO INTERRUPT

004664 012777 004664 174406
004666 012777 000340 174402
004668 042737 000340 177776
004670 052737 000240 177776
004672 012777 040400 174342
004674 012777 000001 174340
004676 017701 174330
004678 100375
004680 000404

ISR24: HLT ;SHOULDN'T HAVE INTERRUPTED AT LEVEL 5
MOV #END24, (SP) ;MOVE NEW RTI ADR ONTO STACK
RTI

004684 104000
004686 012716 004674
004688 000002

END24: MOV XMTLVL, @XMTVEC
MOV #IOT, @XMTLVL
CLR @TCR
CLR @CSR
BIC #340, @#PS

004684 012777 001226 174322
004686 012777 000004 174316
004688 005077 174300
004690 005077 174270
004692 042737 000340 177776
004696 104400

SCOPE

:TEST 25: TEST THAT INTERRUPT OCCURS AT LEVEL 4
:PROBABLE FAULTY LOGIC: M7821 WIRING, PROPER PRIORITY CHIP

TST25: MOV #ISR25, @XMTVEC ;SET UP XMTR INTERRUPT VECTOR
MOV #340, @XMTLVL ;AT LEVEL 7
BIC #340, @#PS ;CLEAR PS LEVEL
BIS #200, @#PS ;SET PS TO LEVEL 4
MOV #040400, @CSR ;SET TRAN MASTER INT. ENABLE
MOV #BITC, @TCR ;SET TRAN CONTROL BIT, LINE C
IS: MOV @CSR, R1 ;WAIT
BPL IS
HLT ;SHOULD HAVE INTERRUPTED AT LEVEL 4
BR END25 ;CONTINUE

004696 012777 005006 174266
004698 012777 000340 174262
004700 042737 000340 177776
004702 052737 000200 177776
004704 012777 040400 174222
004706 012777 000001 174220
004708 017701 174210
004710 100375
004712 104000
004714 000404

ISR25: MOV #END25, (SP) ;MOVE NEW RTI ADR ONTO STACK
RTI

004716 012716 005014
004718 000002

H03

001226 173742
000340 173736
177776
005306 104400

```
END27: MOV XMTLVL, @XMTVEC
        MOV #IOT, @XMTLVL
        CLR @TCR
        CLR @CSR
        BIC #340, @PS
        SCOPE
```

:TEST 30: TEST THAT INTERRUPT OCCURS AT LEVEL 1
:PROBABLE FAULTY LOGIC: M7821 WIRING, PROPER PRIORITY CHIP

005310 012777 005366 173706
005316 012777 000340 173702
005324 042737 000340 177776
005332 052737 000040 177776
005340 012777 040400 173642
005346 012777 000001 173640
005354 017701 173630
005360 100375
005362 104000
005364 000403

```
TST30: MOV #ISR30, @XMTVEC ;SET UP XMTR INTERRUPT VECTOR
        MOV #340, @XMTLVL ;AT LEVEL 7
        BIC #340, @PS ;CLEAR PS LEVEL
        BIS #040, @PS ;SET PS TO LEVEL 1
        MOV #040400, @CSR ;SET TRAN MASTER INT. ENABLE
        MOV #BITC, @TCR ;SET TRAN CONTROL BIT, LINE C
IS: MOV @CSR, R1 ;WAIT
     BPL IS
     HLT ;SHOULD HAVE INTERRUPTED AT LEVEL 1
     BR END30 ;CONTINUE
```

005366 012716 005374
005372 000002

```
ISR30: MOV #END30, (SP) ;MOVE NEW RTI ADR ONTO STACK
        RTI
```

005374 013777 001226 173622
005382 012777 000004 173616
005410 005077 173600
005414 005077 173570
005420 042737 000340 177776
005426 104400

```
END30: MOV XMTLVL, @XMTVEC
        MOV #IOT, @XMTLVL
        CLR @TCR
        CLR @CSR
        BIC #340, @PS
        SCOPE
```

:TEST 31: TEST THAT INTERRUPT OCCURS AT LEVEL 0
:PROBABLE FAULTY LOGIC: M7821 WIRING, PROPER PRIORITY CHIP

005430 012777 005506 173566
005436 012777 000340 173562
005444 042737 000340 177776
005452 052737 000000 177776
005460 012777 040400 173522
005466 012777 000001 173520
005474 017701 173510
005500 100375
005502 104000
005504 000403

```
TST31: MOV #ISR31, @XMTVEC ;SET UP XMTR INTERRUPT VECTOR
        MOV #340, @XMTLVL ;AT LEVEL 7
        BIC #340, @PS ;CLEAR PS LEVEL
        BIS #000, @PS ;SET PS TO LEVEL 0
        MOV #040400, @CSR ;SET TRAN MASTER INT. ENABLE
        MOV #BITC, @TCR ;SET TRAN CONTROL BIT, LINE 0
IS: MOV @CSR, R1 ;WAIT
     BPL IS
     HLT ;SHOULD HAVE INTERRUPTED AT LEVEL 0
     BR END31 ;CONTINUE
```

005506 012716 005514
005512 000002

```
ISR31: MOV #END31, (SP) ;MOVE NEW RTI ADR ONTO STACK
        RTI
```

```

005514 013777 001226 173502
005516 012777 000004 173476
005518 005077 173460
005520 005077 173450
005540 042737 000340 177776
005546 104400
005562 004737 015566 015770
005566 052777 000001 173420
005567 017701 173410
005568 100375
005569 012777 000377 173406
005570 005000
005571 005305
005572 001376 173366
005574 005777
005576 100405
005578 005200
005580 001371 173354
005582 017701
005584 104001
005586 032701 070000
005588 001401

```

```

END31: MOV XMTLVL, @XMTVEC
MOV @IOT, @XMTLVL
CLR @CSR
CLR @CSR
BIC #340, @#PS

SCOPE

CLR TIMER ; INITIALIZE TIMER
MOV #.+6, LAD ; RESET LOOP ADDRESS

```

```

*****
TEST 32: TEST THAT LINE 0 CAN TRANSMIT AND
RECEIVE A CHARACTER. (377)
15: CHECKS THAT DONE SETS IN REASONABLE TIME.
25: CHECKS THAT CHAR PRESENT IS IN FI/FO
35: CHECKS THAT NO ERRORS IN FI/FO
45: CHECKS THAT RIGHT LINE # (0) IN FI/FO
55: CHECKS FOR RIGHT CHARACTER LENGTH
65: CHECKS THAT CORRECT DATA WAS RECEIVED
75: CHECKS THAT CHARACTER PRESENT CLEARS
85: CHECKS THAT DONE CLEARS
PROBABLE FAULTY LOGIC: M7285 (D2-7) ALL; M7279 ALL; UART CARD 003 SERIES
*****

```

```

INITIALIZE
DEVICE"CSR"REGISTER

ST32: JSR PC, @#INITD SET:
;BIT2 = MAINTENANCE
;BIT3 = CLEAR MOS
;BIT8 = MASTER XMTR SCAN ENB

;WAIT FOR MOS TO CLEAR

SET:
;BIT0 = RECEIVER ENABLE

LCP32: BIS #BIT0, @CSR ;SET XMTR CONTROL BIT, LINE 0
MOV @CSR, R1 ;WAIT FOR XMTR READY
BPL LCP32
MOV #377, @RBUF ;SEND A RUBOUT
CLR R0 ;CLEAR COUNTER
15: DECB R5 ;SHORT WAIT LOOP
BNE 15
TSTB @CSR ;WAIT FOR DONE
BMI 25 ;BRANCH WHEN DONE
INC R0 ;TIME COUNTER
BNE 15 ;BRANCH IF NOT TIME-OUT
MOV @CSR, R1 ;SAVE CSR
HLT+1 ;DONE NEVER CAME UP
;R1 = CONTENTS OF CSR

25: BIS R0, TIMER ;SAVE TIMER
MOV @RBUF, R1 ;READ THE FI/FO
BMI .+4 ;BRANCH IF CHARACTER READY
;CHARACTER READY DIDN'T SET
;R1 = CONTENTS OF RBUF
35: BIT #70000, R1 ;CHECK FOR ERROR BITS
BEQ .+4 ;BRANCH IF NONE

```

TST32:

TEST ALL OF LINE 0 TRANSMIT AND RECEIVE LOGIC

1498 005660 104001
 1499
 1500
 1501
 1502
 1503
 1504
 1505
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 1539
 1540

005662 010102
 005664 042702 170377
 005670 000302
 005672 122702 000000
 005676 001401
 005700 104001
 HLT+1

48: MOV R1, R2
 SIO #170377, R2
 SWAB R2
 CMPB #0, R2
 BEQ .+4
 HLT+1

:ERROR IN RECEIVED CHAR
 :R1 = CONTENTS OF RBUF
 :BIT14=UART OVERRUN
 :BIT13=FRAMING ERROR
 :BIT12=PARITY ERROR
 :DUPLICATE DATA WORD
 :MASK LINE #
 :LINE # IN LOW BYTE
 :CHECK LINE #
 :BRANCH IF OK
 :WRONG LINE # RECEIVED
 :R1 = CONTENTS OF RBUF
 :BITS8-11 = LINE #

005702 117702 173400
 005705 130201
 005710 001401
 005712 104002

58: MOV8 00LEN, R2
 BIT8 R2, R1
 BEQ .+4
 HLT+2

58: MOV8 00LEN, R2
 BIT8 R2, R1
 BEQ .+4
 HLT+2

:GET MASK OF CHARACTER
 :CHECK CHAR LENGTH.
 :BRANCH IF OK
 :WRONG CHARACTER LENGTH
 :R1=DATA FROM FI,FO
 :R2=MASK (BITS SET NOT EXPECTED)

005714 105102
 005716 120102
 005720 001401
 005722 104002

68: COM3 R2
 CMPB R1, R2
 BEQ .+4
 HLT+2

68: COM3 R2
 CMPB R1, R2
 BEQ .+4
 HLT+2

:REVERSE THE MASK
 :CHECK THE ACTUAL DATA
 :BRANCH IF OK
 :WRONG CHAR LEN OR DATA ERROR
 :R1=DATA FROM FI,FO COMPLETE WORD
 :R2=DATA (LOW BYTE) EXPECTED

005724 017701 173262
 005730 100001
 005732 104001

78: MOV 0RBUF, R1
 BPL .+4
 HLT+1

78: MOV 0RBUF, R1
 BPL .+4
 HLT+1

:READ FI/FO
 :BRANCH IF CHAR PRESENT NOT SET
 :CHARACTER PRESENT STAYED SET

005734 017701 173250
 005740 022701 100405
 005744 001401
 005746 104001

88: MOV 0CSR, R1
 CMP #100405, R1
 BEQ .+4
 HLT+1

88: MOV 0CSR, R1
 CMP #100405, R1
 BEQ .+4
 HLT+1

:SAVE THE CSR
 :CHECK THE CSR
 :BRANCH IF OK
 :DONE DIDN'T CLEAR OR OTHER CSR ERROR

005750 005077 173240
 005754 005077 173230
 005760 104400

CLR 0TCR
 CLR 0CSR
 SCOPE

CLR 0TCR
 CLR 0CSR
 SCOPE

:CLEAR TCR
 :CLEAR CSR

 :TEST 33: TEST THAT LINE 1 CAN TRANSMIT AND
 :RECEIVE A CHARACTER. (377)
 :18: CHECKS THAT DONE SETS IN REASONABLE TIME.
 :28: CHECKS THAT CHAR PRESENT IS IN FI/FO
 :38: CHECKS THAT NO ERRORS IN FI/FO
 :48: CHECKS THAT RIGHT LINE # (1) IN FI,FO
 :58: CHECKS FOR RIGHT CHARACTER LENGTH
 :68: CHECKS THAT CORRECT DATA WAS RECEIVED
 :78: CHECKS THAT CHARACTER PRESENT CLEARS
 :88: CHECKS THAT DONE CLEARS
 :PROBABLE FAULTY LOGIC: M7285 (D2-?) ALL; M7279 ALL; UART CARD 003 SERIES

005762 004737 015566

TST33:

INITIALIZE
 DEVICE"CSR"REGISTER
 JSR FC, 0#INITD SET:
 :BIT2 = MAINTENANCE

K03

MAINTEN-11-0203A-0
2703AD.P11

0311 LOGIC TESTS
TEST ALL OF LINE 1 TRANSMIT AND RECEIVE LOGIC

MAY 11 27(732) 21-SEP-76 13:43 PAGE 34

ST33:

1594
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1596
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1600
1601
1602
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1607
1608
1609

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005756 052777 000002 173220
005774 017701 173210
006000 100375
006002 012777 000377 173206
006010 005000
006012 105305
006014 001276
006016 105777 173166
006022 100405
006024 005200
006026 001371
006030 017701 173154
006034 104001
006036 050037 001302
006042 017701 173144
006046 100401
006050 104001
006052 032701 070000
006056 001401
006060 104001
006062 010102
006064 042702 170377
006070 000302
006072 122702 000001
006076 001401
006100 104001
006102 117702 173200
006106 130201
006110 001401
006112 104002
006114 105102
006116 120102
006120 001401
006122 104002
006124 017701 173062
006130 100001
006132 104001

```

```

:BIT3 = CLEAR MOS
:BIT8 = MASTER XMTR SCAN ENB
SET:
:BIT0 = RECEIVER ENABLE
:SET XMTR CONTROL BIT. LINE 1
:WAIT FOR XMTR READY
:SEND A RUBOLT
:CLEAR COUNTER
:SHORT WAIT LOOP
:WAIT FOR DONE
:BRANCH WHEN DONE
:TIME COUNTER
:BRANCH IF NOT TIME-OUT
:SAVE CSR
:DONE NEVER CAME UP
:R1 = CONTENTS OF CSR
:SAVE TIMER
:READ THE FI/FO
:BRANCH IF CHARACTER READY
:CHARACTER READY DIDN'T SET
:R1 = CONTENTS OF RBUF
:CHECK FOR ERROR BITS
:BRANCH IF NONE
:ERROR IN RECEIVED CHAR
:R1 = CONTENTS OF RBUF
:BIT14=UART OVERRUN
:BIT13=FRAMING ERROR
:BIT12=PARITY ERROR
:DUPLICATE DATA WORD
:MASK LINE#
:LINE # IN LOW BYTE
:CHECK LINE #
:BRANCH IF OK
:WRONG LINE # RECEIVED
:R1 = CONTENTS OF RBUF
:BITS8-11 = LINE #
:GET MASK OF CHARACTER
:CHECK CHAR LENGTH.
:BRANCH IF OK
:WRONG CHARACTER LENGTH
:R1=DATA FROM FI/FO
:R2=MASK (BITS SET NOT EXPECTED)
:REVERSE THE MASK
:CHECK THE ACTURAL DATA
:BRANCH IF OK
:WRONG CHAR LEN OR DATA ERROR
:R1=DATA FROM FI/FO (COMPLETE WORD)
:R2=DATA (LOW BYTE) EXPECTED
:READ FI/FO
:BRANCH IF CHAR PRESENT NOT SET
:CHARACTER PRESENT STAYED SET
:R1 = CONTENTS OF RBUF

```

:WAIT FOR MOS TO CLEAR

LOP32:

1\$:

2\$:

3\$:

4\$:

5\$:

6\$:

7\$:

M03

17000
17001
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17021
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17200

000000 0042000
000000 0003000
000000 1227000
000000 0014001
000000 104001

006330 117702
006330 130201
006330 001401
006330 104002

006314 105102
006316 120102
006320 001401
006322 104002

006324 017701
006330 100001
006332 104001

006334 017701
006340 022701
006344 001401
006346 104001

006350 005077
006354 005077
006360 104000

170377
000002
173000
172662
172650
172640
172630

48: MOV R1 R2
BIC #1+0377, R2
SWAB R2, R2
CMPB #2, R2
BEQ .+4
HLT+1

53: MOVB 000LEN, R2
BITB R2, R1
BEQ .+4
HLT+2

58: COMB R2
COMB R1, R2
BEQ .+4
HLT+2

75: MOV 0RBUF, R1
BPL .+4
HLT+1

85: MOV 0CSR, R1
CMP #100405, R1
BEQ .+4
HLT+1

CLR 0TOR
CLR 0CSR
SCOPE

:BIT14=LART OVERRUN
:BIT13=FRAMING ERROR
:BIT12=PARITY ERROR
:DUPLICATE DATA WORD
:MASK LINE #
:LINE # IN LOW BYTE
:CHECK LINE #
:BRANCH IF OK
:WRONG LINE # RECEIVED
:R1 = CONTENTS OF RBUF
:BITS8-11 = LINE #
:GET MASK OF CHARACTER
:CHECK CHAR LENGTH.
:BRANCH IF OK
:WRONG CHARACTER LENGTH
:R1=DATA FROM FI/FO
:R2=MASK (BITS SET NOT EXPECTED)
:REVERSE THE MASK
:CHECK THE ACTURAL DATA
:BRANCH IF OK
:WRONG CHAR LEN OR DATA ERROR
:R1=DATA FROM FI/FO (COMPLETE WORD)
:R2=DATA (LOW BYTE) EXPECTED
:READ FI/FO
:BRANCH IF CHAR PRESENT NOT SET
:CHARACTER PRESENT STAYED SET
:R1 = CONTENTS OF RBUF
:SAVE THE CSR
:CHECK THE CSR
:BRANCH IF OK
:DONE DIDN'T CLEAR OR OTHER CSR ERROR
:R1 = CONTENTS OF CSR
:CLEAR TOR
:CLEAR CSR

:TEST 35: TEST THAT LINE 3 CAN TRANSMIT AND
RECEIVE A CHARACTER. (377)
: 15: CHECKS THAT DONE SETS IN REASONABLE TIME.
: 25: CHECKS THAT CHAR PRESENT IS IN FI/FO
: 35: CHECKS THAT NO ERRORS IN FI/FO
: 45: CHECKS THAT RIGHT LINE # (3) IN FI/FO
: 55: CHECKS FOR RIGHT CHARACTER LENGTH
: 65: CHECKS THAT CORRECT DATA WAS RECEIVED
: 75: CHECKS THAT CHARACTER PRESENT CLEARS
: 85: CHECKS THAT DONE CLEARS
:PROBABLE FAULTY LOGIC: M7285 (D2-7) ALL; M7279 ALL; UART CARD 003 SERIES

006362 004737 01556E

: INITIALIZE
: DEVICE"CSR"REGISTER
:SET:
:BIT2 = MAINTENANCE
:BIT3 = CLEAR MOS
:BIT9 = MASTER XMTR SCAN ENB

```

1722                                     :WAIT FOR MOS TO CLEAR
1723                                     :
1724                                     :
1725                                     :
1726                                     :
1727                                     :
1728                                     :
1729                                     :
1730                                     :
1731                                     :
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1735                                     :
1736                                     :
1737                                     :
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1748                                     :
1749                                     :
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1763                                     :
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1765                                     :
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1772                                     :
1773                                     :
1774                                     :
1775                                     :
1776                                     :
1777                                     :

006266 052777 000010 172620 LOP35:  BIS      #BIT3, R1CR
006374 C17701 172610           MOV     3CSR, R1
006400 100375           SPL     LOP35
006402 012777 000377 172606           MOV     #377, R1BUF
006410 005000           CLR     RC
006412 105305           1$:    DECB   RS
006414 001376           BNE     1$
006416 105777 172566           TSTB   3CSR
006422 100405           SMI     2$
006424 005200           INC     RC
006426 001371           BNE     1$
006430 017701 172554           MOV     3CSR, R1
006434 104001           HLT+1
006436 050037 001302           2$:    BIS     RC, TIMER
006442 017701 172544           MOV     RBUF, R1
006446 100401           BMI     .+4
006450 104001           HLT+1
006452 032701 070000           3$:    BIT     #70000, R1
006456 001401           BEQ     .+4
006460 104001           HLT+1
006462 010102           4$:    MOV     R1, R2
006464 042702 170377           BIC     #170377, R2
006470 000302           SWAB   R2
006472 122702 000002           CMPB   #3, R2
006476 001401           BEQ     .+4
006500 104001           HLT+1
006502 117702 172600           5$:    MOV     DJLEN, R2
006506 130201           BITB   R2, R1
006510 001401           BEQ     .+4
006512 104002           HLT+2
006514 105102           6$:    COMB   R2
006516 120102           CMPB   R1, R2
006520 001401           BEQ     .+4
006522 104002           HLT+2
006524 017701 172462           7$:    MOV     RBUF, R1
006530 100001           BPL     .+4
006532 104001           HLT+1
006534 017701 172450           8$:    MOV     3CSR, R1
006540 022701 100405           CMP     #100405, R1

```

```

SET:
:BIT0 = RECEIVER ENABLE
:SET XMTR CONTROL BIT, LINE 3
:WAIT FOR XMTR READY
:SEND A RUBOUT
:CLEAR COUNTER
:SHORT WAIT LOOP
:WAIT FOR DONE
:BRANCH WHEN DONE
:TIME COUNTER
:BRANCH IF NOT TIME-OUT
:SAVE CSR
:DONE NEVER CAME UP
:R1 = CONTENTS OF CSR
:SAVE TIMER
:READ THE FI/FO
:BRANCH IF CHARACTER READY
:CHARACTER READY DIDN'T SET
:R1 = CONTENTS OF RBUF
:CHECK FOR ERROR BITS
:BRANCH IF NONE
:ERROR IN RECEIVED CHAR
:R1 = CONTENTS OF RBUF
:BIT14=UART OVERRLN
:BIT13=FRAMING ERROR
:BIT12=PARITY ERROR
:DUPLICATE DATA WORD
:MASK LINE#
:LINE # IN LOW BYTE
:CHECK LINE #
:BRANCH IF OK
:WRONG LINE # RECEIVED
:R1 = CONTENTS OF RBUF
:BITS8-11 = LINE #
:GET MASK OF CHARACTER
:CHECK CHAR LENGTH.
:BRANCH IF OK
:WRONG CHARACTER LENGTH
:R1=DATA FROM FI/FO
:R2=MASK (BITS SET NOT EXPECTED)
:REVERSE THE MASK
:CHECK THE ACTURAL DATA
:BRANCH IF OK
:WRONG CHAR LEN OR DATA ERROR
:R1=DATA FROM FI/FO (COMPLETE WORD)
:R2=DATA (LOW BYTE) EXPECTED
:READ FI/FO
:BRANCH IF CHAR PRESENT NOT SET
:CHARACTER PRESENT STAYED SET
:R1 = CONTENTS OF RBUF
:SAVE THE CSR
:CHECK THE CSR

```


TRANSMIT AND RECEIVE LOGIC

Header information including file name and date: FILE NAME: ... DATE: ...

Table with columns for address, data, and control signals. Address range: 000000 to 000040. Includes labels like 'R1', 'R2', 'R3'.

Assembler code comments and instructions. Includes: SET: BIT0 = RECEIVER ENABLE; SET XMTR CONTROL BIT, LINE 0; WAIT FOR XMTR READY; SEND A RUBOUT; CLEAR COUNTER; SHORT WAIT LOOP; WAIT FOR DONE; BRANCH WHEN DONE; TIME COUNTER; BRANCH IF NOT TIME-OUT; DONE CSR; DONE NEVER CAME LP; CONTENTS OF CSR; READ THE FIFO; BRANCH IF CHARACTER READY; CHARACTER READY DIDN'T SET; R1 = CONTENTS OF RBUF; CHECK FOR ERROR BITS; BRANCH IF NONE; ERROR IN RECEIVED CHAR; R1 = CONTENTS OF RBUF; CHECK FOR PARITY ERROR; IN PARITY ERROR; INDICATE DATA WORD; CHECK LINE # IN 101 BYTE; CHECK LINE #; CHECK LINE #; R1 = CONTENTS OF RBUF; CHECK MASK OF CHARACTER; CHECK CHAR LENGTH; BRANCH IF OK; WRONG CHARACTER LENGTH; R1 = DATA FROM FI FO; CHECK MASK (BITS SET NOT EXPECTED); INVERSE THE MASK; CHECK THE ACTUAL DATA; BRANCH IF OK; WRONG CHAR LEN OR DATA ERROR; R1 = DATA FROM FI FO, COMPLETE WORD; R1 = DATA (LOW BYTE) EXPECTED; READ FI FO; BRANCH IF CHAR PRESENT NOT SET; CHARACTER PRESENT STAYED SET; R1 = CONTENTS OF RBUF; CHECK THE CSR.

007333 000000
007334 000000
007335 000000
007336 000000
007337 000000
007338 000000
007339 000000
007340 000000
007341 000000
007342 000000
007343 000000
007344 000000
007345 000000
007346 000000
007347 000000
007348 000000
007349 000000
007350 000000
007351 000000
007352 000000
007353 000000
007354 000000
007355 000000
007356 000000
007357 000000
007358 000000
007359 000000
007360 000000
007361 000000
007362 000000
007363 000000
007364 000000
007365 000000
007366 000000
007367 000000
007368 000000
007369 000000
007370 000000
007371 000000
007372 000000
007373 000000
007374 000000
007375 000000
007376 000000
007377 000000
007378 000000
007379 000000
007380 000000
007381 000000
007382 000000
007383 000000
007384 000000
007385 000000
007386 000000
007387 000000
007388 000000
007389 000000
007390 000000
007391 000000
007392 000000
007393 000000
007394 000000
007395 000000
007396 000000
007397 000000
007398 000000
007399 000000
007400 000000

```

44:  MOV     R1, R2
      UNK   #140377, R2
      UNK   R2, R2
      COMB  #6, R2
      BEQ   .+4
      HALT+1

55:  MOV     R2, LEN, R2
      BIT8  R2, R1
      BEQ   .+4
      HALT+2

66:  COMB   R2, R2
      COMB  R1, R2
      BEQ   .+4
      HALT+2

78:  MOV     RBJF, R1
      BEQ   .+4
      HALT+1

88:  MOV     CSR, R1
      COMB  #1004CS, R1
      BEQ   .+4
      HALT+1

CLR  R2CR
CLR  R2CSR
SCOPE

```

```

:BIT12=PARITY ERROR
:DUPLICATE DATA WORD
:MASK LINE #
:LINE # IN LOW BYTE
:CHECK LINE #
:BRANCH IF OK
:WRONG LINE # RECEIVED
:R1 = CONTENTS OF RBJF
:BITS8-11 = LINE #
:GET MASK OF CHARACTER
:CHECK CHAR LENGTH.
:BRANCH IF OK
:WRONG CHARACTER LENGTH
:R1=DATA FROM FI/FO
:R2=MASK (BITS SET NOT EXPECTED)
:REVERSE THE MASK
:CHECK THE ACTUAL DATA
:BRANCH IF OK
:WRONG CHAR LEN OR DATA ERROR
:R1=DATA FROM FI/FO (COMPLETE WORD)
:R2=DATA (LOW BYTE) EXPECTED
:READ FI/FO
:BRANCH IF CHAR PRESENT NOT SET
:CHARACTER PRESENT STAYED SET
:R1 = CONTENTS OF RBJF
:SAVE THE CSR
:CHECK THE CSR
:BRANCH IF OK
:DONE DIDN'T CLEAR OF OTHER CSR ERROR
:R1 = CONTENTS OF CSR
:CLEAR TCR
:CLEAR CSR

```

```

*****
TEST 41: TEST THAT LINE 7 CAN TRANSMIT AND
RECEIVE A CHARACTER. (377)
14: CHECKS THAT DONE SETS IN REASONABLE TIME.
38: CHECKS THAT CHAR PRESENT IS IN FI-FO
39: CHECKS THAT NO ERRORS IN FI-FO
48: CHECKS THAT RIGHT LINE # (7) IN FI-FO
58: CHECKS FOR RIGHT CHARACTER LENGTH
68: CHECKS THAT CORRECT DATA WAS RECEIVED
78: CHECKS THAT CHARACTER PRESENT CLEARS
88: CHECKS THAT DONE CLEARS
:PROBABLE FAULTY LOGIC: M7285 (D2-7) ALL; M7279 ALL; JART CARD 003 SERIES
*****

```

```

INITIALIZE
DEVICE"CSR"REGISTER
TEST41: JSR   PC,   @INITD
:WAIT FOR MOS TO CLEAR
SET:
:BIT2 = MAINTENANCE
:BIT3 = CLEAR MOS
:BIT8 = MASTER XMTR SCAN ENB
SET:

```


TRANSMIT AND RECEIVE LOGIC

:R1 = CONTENTS OF CSR
:CLEAR TCR
:CLEAR CSR

BTOR
BCSR
DJLEN
*.+E. LAC
MOV

015770

TEST 42: TEST THAT LINE 8 CAN TRANSMIT AND
RECEIVE A CHARACTER. (377)
1\$: CHECKS THAT DONE SETS IN REASONABLE TIME.
3\$: CHECKS THAT CHAR PRESENT IS IN FI/FO
4\$: CHECKS THAT NO ERRORS IN FI/FO
5\$: CHECKS THAT RIGHT LINE # (8) IN FI/FO
6\$: CHECKS FOR RIGHT CHARACTER LENGTH
7\$: CHECKS THAT CORRECT DATA WAS RECEIVED
8\$: CHECKS THAT CHARACTER PRESENT CLEARS
9\$: CHECKS THAT DONE CLEARS

***** PROBABLE FAULTY LOGIC: M7285 (D2-7) ALL; M7279 ALL; UART CARD 003 SERIES *****

INITIALIZE
DEVICE "CSR" REGISTER

SET42: JSR PC, @INITD SET:
:BIT2 = MAINTENANCE
:BIT3 = CLEAR MOS
:BIT3 = MASTER XMTR SCAN ENB

WAIT FOR MOS TO CLEAR
SET:
:BIT0 = RECEIVER ENABLE

LOP42: BIS #BITB, BTOR :SET XMTR CONTROL BIT, LINE 8
MOV BCSR, R1 :WAIT FOR XMTR READY

BFL LOP42 :SEND A RUBOUT
MOV #377, BTBUF :CLEAR COUNTER
CLR RD :SHORT WAIT LOOP
DECB RS

5: BNE 1\$:WAIT FOR DONE
TSTB BCSR :BRANCH WHEN DONE
BMI RS :TIME COUNTER
INC RD :BRANCH IF NOT TIME-OUT
BNE 1\$:SAVE CSR
MOV BCSR, R1 :DONE NEVER CAME UP
HLT+1 :R1 = CONTENTS OF CSR

2\$: BIS RD, TIMER :SAVE TIMER
MOV BTBUF, R1 :READ THE FI/FO
BMI .+4 :BRANCH IF CHARACTER READY
HLT+1 :CHARACTER READY DIDN'T SET

3\$: BIT #70000, R1 :R1 = CONTENTS OF RBUF
BEQ .+4 :CHECK FOR ERROR BITS
HLT+1 :BRANCH IF NONE
:ERROR IN RECEIVED CHAR
:R1 = CONTENTS OF RBUF
:BIT14=UART OVERRUN
:BIT13=FRAMING ERROR

007650 052777 000400 171374
007651 017701 171364
007652 100375
007653 012777 000377 171362
007654 005000
007655 105305
007656 001376
007657 105777 171342
007658 100405
007659 005200
007660 001371
007661 017701 171330
007662 104001
007663 050037 001332
007664 017701 171320
007665 100401
007666 104001
007667 032701 070000
007668 001401
007669 104001

010012	052777	001000	171174	:	BIS	#BIT9,	QTCR	:BIT0 = RECEIVER ENABLE
010020	017701	171164		LOP43:	MOV	QCSR,	R1	:SET XMTR CONTROL BIT, LINE 9
010024	100375				BPL	LOP43		:WAIT FOR XMTR READY
010026	012777	000377	171162		MOV	#377,	QTBUF	:SEND A RUBOUT
010034	005000			1\$:	CLR	RD		:CLEAR COUNTER
010036	025305				DECB	R5		:SHORT WAIT LOOP
010040	001376				SNE	1\$		
010042	105777	171142			TSTB	QCSR		:WAIT FOR DONE
010046	100405				BMI	2\$:BRANCH WHEN DONE
010050	005200				INC	RD		:TIME COUNTER
010054	001371				SNE	1\$:BRANCH IF NOT TIME-OUT
010058	017701	171130			MOV	QCSR,	R1	:SAVE CSR
010060	104001				HLT+1			:DONE NEVER CAME UP
010062	050037	001302		2\$:	BIS	RD,	TIMER	:R1 = CONTENTS OF CSR
010066	017701	171120			MOV	QRBUF,	R1	:SAVE TIMER
010070	100401				BMI	+.4		:READ THE FI/FO
010074	104001				HLT+1			:BRANCH IF CHARACTER READY
010076	032701	070000		3\$:	BIT	#70000,	R1	:CHARACTER READY DIDN'T SET
010080	001401				BEQ	+.4		:R1 = CONTENTS OF RBUF
010084	104001				HLT+1			:CHECK FOR ERROR BITS
								:BRANCH IF NONE
								:ERROR IN RECEIVED CHAR
								:R1 = CONTENTS OF RBUF
								:BIT14=UART OVERRUN
								:BIT13=FRAMING ERROR
								:BIT12=PARITY ERROR
								:DUPLICATE DATA WORD
010106	010102			4\$:	MOV	R1,	R2	:MASK LINE #
010110	042702	170377			BIC	#170377,	R2	:LINE # IN LOW BYTE
010114	002302				SHAB	R2		:CHECK LINE #
010116	122702	000011			CMPB	#9,	R2	:BRANCH IF OK
010120	001401				BEQ	+.4		:WRONG LINE # RECEIVED
010124	104001				HLT+1			:R1 = CONTENTS OF RBUF
								:BITS8-11 = LINE #
010126	117702	171154		5\$:	MOVW	QDYLEN,	R2	:GET MASK OF CHARACTER
010130	130201				BITB	R2,	R1	:CHECK CHAR LENGTH.
010134	001401				BEQ	+.4		:BRANCH IF OK
010136	104002				HLT+2			:WRONG CHARACTER LENGTH
								:R1=DATA FROM FI/FO
								:R2=MASK (BITS SET NOT EXPECTED)
								:REVERSE THE MASK
010140	105102			6\$:	COMB	R2		:CHECK THE ACTUAL DATA
010142	120102				CMPB	R1,	R2	:BRANCH IF OK
010144	001401				BEQ	+.4		:WRONG CHAR LEN OR DATA ERROR
010146	104002				HLT+2			:R1=DATA FROM FI/FO (COMPLETE WORD)
								:R2=DATA (LOW BYTE) EXPECTED
010150	017701	171036		7\$:	MOV	QRBUF,	R1	:READ FI/FO
010154	100001				BPL	+.4		:BRANCH IF CHAR PRESENT NOT SET
010156	104001				HLT+1			:CHARACTER PRESENT STAYED SET
								:R1 = CONTENTS OF RBUF
010160	017701	171024		8\$:	MOV	QCSR,	R1	:SAVE THE CSR
010164	022701	100405			CMP	#100405,	R1	:CHECK THE CSR
010170	001401				BEQ	+.4		:BRANCH IF OK
010172	104001				HLT+1			:DONE DIDN'T CLEAR OR OTHER CSR ERROR

K04

MAINDEC-11-DZDJA-D
DZDJA.D.F11

TST43:

DJ11 LOGIC TESTS
TEST ALL OF LINE 9 TRANSMIT AND RECEIVE LOGIC

MAY11 27(732) 21-SEP-76 13:43 PAGE 47

000000
000001
000002
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000011
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000036
000037

010174 005077 171014
010200 005077 171004
010204 104400

CLR JTCR
CLR JCSR
SCOPE

:R1 = CONTENTS OF CSR
:CLEAR TCR
:CLEAR CSR

:TEST 44: TEST THAT LINE 10 CAN TRANSMIT AND
RECEIVE A CHARACTER. (377)
1\$: CHECKS THAT DONE SETS IN REASONABLE TIME.
2\$: CHECKS THAT CHAR PRESENT IS IN FI/FO
3\$: CHECKS THAT NO ERRORS IN FI/FO
4\$: CHECKS THAT RIGHT LINE # (10) IN FI/FO
5\$: CHECKS FOR RIGHT CHARACTER LENGTH
6\$: CHECKS THAT CORRECT DATA WAS RECEIVED
7\$: CHECKS THAT CHARACTER PRESENT CLEARS
8\$: CHECKS THAT DONE CLEARS
:PROBABLE FAULTY LOGIC: M7285 (D2-7) ALL; M7279 ALL; JART CARD DC3 SERIES

: INITIALIZE
: DEVICE"CSR"REGISTER

010206 004737 015566

TST44: JSR PC, @*INITD

SET:
:BIT2 = MAINTENANCE
:BIT3 = CLEAR MOS
:BITS = MASTER XMTR SCAN ENB

:WAIT FOR MOS TO CLEAR

SET:
:BIT0 = RECEIVER ENABLE

010212 052777 002000 170774
010220 017701 170764
010224 100375
010226 012777 000377 170762
010234 005000
010236 105305
010240 001376
010242 105777 170742
010246 100405
010250 005200
010252 001371
010254 017701 170730
010260 104001

LOP44: BIS #BIT10, JTCR
MOV JCSR, R1
BPL LOP44
MOV #377, JTBUF
CLR RC
1\$: DECB R5
BNE 1\$
TSTB JCSR
BMT 2\$
INC RD
BNE 1\$
MOV JCSR, R1
HLT+1

:SET XMTR CONTROL BIT, LINE 10
:WAIT FOR XMTR READY
:SEND A RUBOUT
:CLEAR COUNTER
:SHORT WAIT LOOP
:WAIT FOR DONE
:BRANCH WHEN DONE
:TIME COUNTER
:BRANCH IF NOT TIME-OUT
:SAVE CSR
:DONE NEVER CAME UP
:R1 = CONTENTS OF CSR

010262 050037 001302
010266 017701 170720
010272 100401
010274 104001

2\$: BIS RD, TIMER
MOV JTBUF, R1
BMT .+4
HLT+1

:SAVE TIMER
:READ THE FI/FO
:BRANCH IF CHARACTER READY
:CHARACTER READY DIDN'T SET

010276 032701 070000
010302 001401
010304 104001

3\$: BIT #70000, R1
BEQ .+4
HLT+1

:R1 = CONTENTS OF RBUF
:CHECK FOR ERROR BITS
:BRANCH IF NONE
:ERROR IN RECEIVED CHAR

010306 010102

4\$: MOV R1, R2

:R1 = CONTENTS OF RBUF
:BIT14=UART OVERRUN
:BIT13=FRAMING ERROR
:BIT12=PARITY ERROR
:DUPLICATE DATA WORD

```

2338 010310 042702 170377 BIC #170377,R2 :MASK LINE#
2339 010314 000302 SWAB R2 :LINE # IN LOW BYTE
2340 010316 122702 000012 CMPB #10., R2 :CHECK LINE #
2341 010322 001401 BEQ .+4 :BRANCH IF OK
2342 010324 104001 HLT+1 :WRONG LINE # RECEIVED
2343 :R1 = CONTENTS OF RBUF
2344 :BITS8-11 = LINE #
2345 010326 117702 170754 5$: MOVB @DJLEN, R2 :GET MASK OF CHARACTER
2346 010332 130301 BITB R2, R1 :CHECK CHAR LENGTH.
2347 010334 001401 BEQ .+4 :BRANCH IF OK
2348 010336 104002 HLT+2 :WRONG CHARACTER LENGTH
2349 :R1=DATA FROM FI/FO
2350 :R2=MASK (BITS SET NOT EXPECTED)
2351 010340 105102 6$: COMB R2 :REVERSE THE MASK
2352 010342 120102 CMPB R1, R2 :CHECK THE ACTUAL DATA
2353 010344 001401 BEQ .+4 :BRANCH IF OK
2354 010346 104002 HLT+2 :WRONG CHAR LEN OR DATA ERROR
2355 :R1=DATA FROM FI/FO (COMPLETE WORD)
2356 :R2=DATA (LOW BYTE) EXPECTED
2357 010350 017701 170636 7$: MOV @RBUF, R1 :READ FI/FO
2358 010354 100001 BPL .+4 :BRANCH IF CHAR PRESENT NOT SET
2359 010356 104001 HLT+1 :CHARACTER PRESENT STAYED SET
2360 010360 017701 170624 8$: MOV @CSR, R1 :SAVE THE CSR
2361 010364 022701 100405 CMP #100405,R1 :CHECK THE CSR
2362 010370 001401 BEQ .+4 :BRANCH IF OK
2363 010372 104001 HLT+1 :DONE DIDN'T CLEAR OR OTHER CSR ERROR
2364 :R1 = CONTENTS OF RBUF
2365 010374 005077 170514 CLR @TCR :CLEAR TCR
2366 010400 005077 170604 CLR @CSR :CLEAR CSR
2367 010404 104400 SCOPE

```

```

:*****
:TEST 45: TEST THAT LINE 11 CAN TRANSMIT AND
: RECEIVE A CHARACTER.
:
: 1$: CHECKS THAT DONE SETS IN REASONABLE TIME.
: 2$: CHECKS THAT CHAR PRESENT IS IN FI/FO
: 3$: CHECKS THAT NO ERRORS IN FI/FO
: 4$: CHECKS THAT RIGHT LINE # (11) IN FI/FO
: 5$: CHECKS FOR RIGHT CHARACTER LENGTH
: 6$: CHECKS THAT CORRECT DATA WAS RECEIVED
: 7$: CHECKS THAT CHARACTER PRESENT CLEARS
: 8$: CHECKS THAT DONE CLEARS
:PROBABLE FAULTY LOGIC: M7295 (D2-7) ALL; M7279 ALL; UART CARD D33 SERIES
:*****

```

```

:
: INITIALIZE
: DEVICE"CSR"REGISTER
:
: TST45: JSR PC, @*INITD SET:
: :BIT2 = MAINTENANCE
: :BIT3 = CLEAR MOS
: :BIT8 = MASTER XMTR SCAN ENB
:
: WAIT FOR MOS TO CLEAR
:
: SET:
: :BIT0 = RECEIVER ENABLE
:

```

M04

MAINDEC-11-32DJA-D
0200P.P.11

TST45:

DJ11 LOGIC TESTS
TEST ALL OF LINE 11 TRANSMIT AND RECEIVE LOGIC

MADY:1 27(732) 21-SEP-76 13:43 PAGE 49

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010412 052777 004000 170574 BIS #BIT11, @TCR ;SET XMTR CONTROL BIT, LINE 11
010420 017701 170564 LOP45: MOV @CSR, R1 ;WAIT FOR XMTR READY
010424 100379 BPL LOP45
010426 012777 000377 170562 MOV #377, @TBUF ;SEND A RUBOUT
010434 005000 CLR R0 ;CLEAR COUNTER
010436 105305 1$: DECS R5 ;SHORT WAIT LOOP
010440 001376 SNE 1$
010442 105777 170542 TSTB @CSR ;WAIT FOR DONE
010446 100405 BMI 2$ ;BRANCH WHEN DONE
010450 005202 INC R0 ;TIME COUNTER
010452 001371 BNE 1$ ;BRANCH IF NOT TIME-OUT
010454 017701 170530 MOV @CSR, R1 ;SAVE CSR
010456 104001 HLT+1 ;DONE NEVER CAME UP
;R1 = CONTENTS OF CSR
010462 050037 001302 2$: BIS R0, @TIMER ;SAVE TIMER
010466 017701 170520 MOV @RBUF, R1 ;READ THE FI/FO
010472 100401 BMI .+4 ;BRANCH IF CHARACTER READY
010474 104001 HLT+1 ;CHARACTER READY DIDN'T SET
;R1 = CONTENTS OF RBUF
010476 032701 070000 3$: BIT #70000, R1 ;CHECK FOR ERROR BITS
010502 001401 BEQ .+4 ;BRANCH IF NONE
010504 104001 HLT+1 ;ERROR IN RECEIVED CHAR
;R1 = CONTENTS OF RBUF
;BIT14=UART OVERRUN
;BIT13=FRAMING ERROR
;BIT12=PARITY ERROR
;DUPLICATE DATA WORD
010506 010102 4$: MOV R1, R2 ;MASK LINE#
010510 042702 170377 BIC #170377, R2 ;LINE # IN LOW BYTE
010514 000302 SWAB R2 ;CHECK LINE #
010516 122702 000013 CMPB #11, R2 ;BRANCH IF OK
010522 001401 BEQ .+4 ;WRONG LINE # RECEIVED
010524 104001 HLT+1 ;R1 = CONTENTS OF RBUF
;BITS8-11 = LINE #
010526 117702 170554 5$: MOVB @CJLEN, R2 ;GET MASK OF CHARACTER
010532 130201 BITB R2, R1 ;CHECK CHAR LENGTH.
010534 001401 BEQ .+4 ;BRANCH IF OK
010536 104002 HLT+2 ;WRONG CHARACTER LENGTH
;R1=DATA FROM FI/FO
;R2=MASK (BITS SET NOT EXPECTED)
;REVERSE THE MASK
010540 105102 6$: COMB R2 ;CHECK THE ACTUAL DATA
010542 120102 CMPB R1, R2 ;BRANCH IF OK
010544 001401 BEQ .+4 ;WRONG CHAR LEN OR DATA ERROR
010546 104002 HLT+2 ;R1=DATA FROM FI/FO (COMPLETE WORD)
;R2=DATA (LOW BYTE) EXPECTED
010550 017701 170436 7$: MOV @RBUF, R1 ;READ FI/FO
010554 100001 BPL .+4 ;BRANCH IF CHAR PRESENT NOT SET
010556 104001 HLT+1 ;CHARACTER PRESENT STAYED SET
;R1 = CONTENTS OF RBUF
010560 017701 170424 8$: MOV @CSR, R1 ;SAVE THE CSR
010564 022701 100405 CMP #100405, R1 ;CHECK THE CSR
010570 001401 BEQ .+4 ;BRANCH IF OK
010572 104001 HLT+1 ;DONE DIDN'T CLEAR OR OTHER CSR ERROR
;R1 = CONTENTS OF CSR
010574 005 77 170414 CLR @TCR ;CLEAR TCR

```

010600 005077 170404
010604 104400
010606 005237 001306
010612 012737 010620 015770

CLR QCSR :CLEAR CSR
SCOPE
INC DJLEN
MOV #.+6. LAD

TEST 46: TEST THAT LINE 12 CAN TRANSMIT AND
RECEIVE A CHARACTER. (377)
1\$: CHECKS THAT DONE SETS IN REASONABLE TIME.
2\$: CHECKS THAT CHAR PRESENT IS IN FI/FO
3\$: CHECKS THAT NO ERRORS IN FI/FO
4\$: CHECKS THAT RIGHT LINE # (12) IN FI/FO
5\$: CHECKS FOR RIGHT CHARACTER LENGTH
6\$: CHECKS THAT CORRECT DATA WAS RECEIVED
7\$: CHECKS THAT CHARACTER PRESENT CLEARS
8\$: CHECKS THAT DONE CLEARS
PROBABLE FAULTY LOGIC: M7285 (D2-7) ALL; M7279 ALL; UART CARD DC3 SERIES

INITIALIZE
DEVICE"CSR"REGISTER

010620 004737 015566

ST46: JSR PC, @*INITD SET:
:BIT2 = MAINTENANCE
:BIT3 = CLEAR MOS
:BITS = MASTER XMTR SCAN ENB

:WAIT FOR MOS TO CLEAR

SET:
:BIT0 = RECEIVER ENABLE

010624 052777 010000 170362

LOP46: BIS #BIT12, @TCR :SET XMTR CONTROL BIT, LINE 12
MOV @CSR, R1 :WAIT FOR XMTR READY

010632 017701 170352

010636 100375

010640 012777 000377 170350

010646 005000

010650 105305

010652 001376

010654 105777 170320

010660 100405

010662 005200

010664 001371

010666 017701 170316

010672 104001

1\$: DEC R5 :SHORT WAIT LOOP
BNE 1\$
TSTB @CSR :WAIT FOR DONE
BMI 2\$:BRANCH WHEN DONE
INC R0 :TIME COUNTER
BNE 1\$:BRANCH IF NOT TIME-OUT
MOV @CSR, R1 :SAVE CSR
HLT+1 :DONE NEVER CAME UP

010674 050037 001302 2\$:

010700 017701 170306

010704 100401

010706 104001

2\$: BIS R0, TIMER :SAVE TIMER
MOV @RBUF, R1 :READ THE FI/FO
BMI .+4 :BRANCH IF CHARACTER READY
HLT+1 :CHARACTER READY DIDN'T SET
3\$: BIT #70000, R1 :R1 = CONTENTS OF RBUF
BEQ .+4 :CHECK FOR ERROR BITS
HLT+1 :BRANCH IF NONE
:ERROR IN RECEIVED CHAR
:R1 = CONTENTS OF RBUF

010710 032701 070000 3\$:

010714 001401

010716 104001

4\$: MOV R1, R2 :DUPLICATE DATA WORD
:BIT14=UART OVERRUN
:BIT13=FRAMING ERROR
:BIT12=PARITY ERROR

010720 010102

4\$: MOV R1, R2


```

0111330 000016 CMPB #14., R2
0111334 000017 BEQ .+4
0111336 000018 HLT+1

0111340 000019 SET: MOV R0,LEN, R0
0111342 000020 TMBR R0, R0
0111344 000021 TMBR R0, R0
0111346 000022 HLT+2

0111350 000023 SET: MOV R0, R0
0111352 000024 HLT+2

0111356 000025 SET: MOV R0, R0
0111358 000026 HLT+2

0111360 000027 SET: MOV R0, R0
0111362 000028 HLT+2

0111364 000029 SET: MOV R0, R0
0111366 000030 HLT+2

0111368 000031 SET: MOV R0, R0
0111370 000032 HLT+2

0111372 000033 SET: MOV R0, R0
0111374 000034 HLT+2

0111376 000035 SET: MOV R0, R0
0111378 000036 HLT+2

0111380 000037 SET: MOV R0, R0
0111382 000038 HLT+2

0111384 000039 SET: MOV R0, R0
0111386 000040 HLT+2

0111388 000041 SET: MOV R0, R0
0111390 000042 HLT+2

0111392 000043 SET: MOV R0, R0
0111394 000044 HLT+2

0111396 000045 SET: MOV R0, R0
0111398 000046 HLT+2

0111400 000047 SET: MOV R0, R0
0111402 000048 HLT+2

0111404 000049 SET: MOV R0, R0
0111406 000050 HLT+2

0111408 000051 SET: MOV R0, R0
0111410 000052 HLT+2

0111412 000053 SET: MOV R0, R0
0111414 000054 HLT+2

0111416 000055 SET: MOV R0, R0
0111418 000056 HLT+2

0111420 000057 SET: MOV R0, R0
0111422 000058 HLT+2

0111424 000059 SET: MOV R0, R0
0111426 000060 HLT+2

0111428 000061 SET: MOV R0, R0
0111430 000062 HLT+2

0111432 000063 SET: MOV R0, R0
0111434 000064 HLT+2

0111436 000065 SET: MOV R0, R0
0111438 000066 HLT+2

0111440 000067 SET: MOV R0, R0
0111442 000068 HLT+2

0111444 000069 SET: MOV R0, R0
0111446 000070 HLT+2

0111448 000071 SET: MOV R0, R0
0111450 000072 HLT+2

0111452 000073 SET: MOV R0, R0
0111454 000074 HLT+2

0111456 000075 SET: MOV R0, R0
0111458 000076 HLT+2

0111460 000077 SET: MOV R0, R0
0111462 000078 HLT+2

0111464 000079 SET: MOV R0, R0
0111466 000080 HLT+2

0111468 000081 SET: MOV R0, R0
0111470 000082 HLT+2

0111472 000083 SET: MOV R0, R0
0111474 000084 HLT+2

0111476 000085 SET: MOV R0, R0
0111478 000086 HLT+2

0111480 000087 SET: MOV R0, R0
0111482 000088 HLT+2

0111484 000089 SET: MOV R0, R0
0111486 000090 HLT+2

0111488 000091 SET: MOV R0, R0
0111490 000092 HLT+2

0111492 000093 SET: MOV R0, R0
0111494 000094 HLT+2

0111496 000095 SET: MOV R0, R0
0111498 000096 HLT+2

0111500 000097 SET: MOV R0, R0
0111502 000098 HLT+2

0111504 000099 SET: MOV R0, R0
0111506 000100 HLT+2

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:CHECK LINE #
:BRANCH IF OK
:WRONG LINE #
:RI = CONTENTS OF CSR
:BITSB-11 = LINE #
:GET MASK OF CHARACTER
:CHECK CHAR LENGTH.
:BRANCH IF OK
:WRONG CHARACTER LENGTH
:DATA FROM FIFO NOT RECEIVED
:CHARACTER MASK
:CHECK THE MASK DATA
:BRANCH IF OK
:WRONG CHAR LENGTH OR DATA
:DATA FROM FIFO
:DATA FROM FIFO
:WRONG CHAR PRESENT NOT SET
:CHARACTER PRESENT NOT SET
:RI = CONTENTS OF CSR
:SAVE THE CSR
:CHECK THE CSR
:BRANCH IF OK
:ONE DIDN'T CLEAR OR OTHER CSR ERROR
:RI = CONTENTS OF CSR
:CLR CSR
:CLR CSR

```

```

*****
TEST S1: TEST THAT LINE 14 CAN TRANSMIT AND
RECEIVE A CHARACTER. (377)
:CHECKS THAT DONE BITS IN REASONABLE TIME.
:CHECKS THAT CHAR PRESENT IS IN FIFO
:CHECKS THAT NO ERRORS IN FIFO
:CHECKS THAT RIGHT LINE # (15) IN F: FO
:CHECKS FOR RIGHT CHARACTER LENGTH
:CHECKS THAT CORRECT DATA WAS RECEIVED
:CHECKS THAT CHARACTER PRESENT CLEARS
:CHECKS THAT DONE CLEARS
RECEIVABLE FAULTY LOGIC: M7285 (2R-1) ALL: M7279 ALL: JART JARD 000 SER:55
*****

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0111420 000077 SET: MOV R0, R0
0111422 000078 HLT+2
0111424 000079 SET: MOV R0, R0
0111426 000080 HLT+2
0111428 000081 SET: MOV R0, R0
0111430 000082 HLT+2
0111432 000083 SET: MOV R0, R0
0111434 000084 HLT+2
0111436 000085 SET: MOV R0, R0
0111438 000086 HLT+2
0111440 000087 SET: MOV R0, R0
0111442 000088 HLT+2
0111444 000089 SET: MOV R0, R0
0111446 000090 HLT+2
0111448 000091 SET: MOV R0, R0
0111450 000092 HLT+2
0111452 000093 SET: MOV R0, R0
0111454 000094 HLT+2
0111456 000095 SET: MOV R0, R0
0111458 000096 HLT+2
0111460 000097 SET: MOV R0, R0
0111462 000098 HLT+2
0111464 000099 SET: MOV R0, R0
0111466 000100 HLT+2

```

```

:INITIALIZE
:DEVICE CSR REGISTER
SET:
:BIT0 = MAINTENANCE
:BIT1 = CLEAR MOS
:BIT2 = MASTER XMTA SCAN ENB
:BITC = RECEIVER ENABLE
:SET XMTA CONTROL BIT. LINE 15
:WAIT FOR XMTA READY

```

011510 011514 011516 011518 011519 011520 011521 011522 011523 011524 011525 011526 011527 011528 011529 011530 011531 011532 011533 011534 011535 011536 011537 011538 011539 011540 011541 011542 011543 011544 011545 011546 011547 011548 011549 011550 011551 011552 011553 011554 011555 011556 011557 011558 011559 011560 011561 011562 011563 011564 011565 011566 011567 011568 011569 011570 011571 011572 011573 011574 011575 011576 011577 011578 011579 011580 011581 011582 011583 011584 011585 011586 011587 011588 011589 011590 011591 011592 011593 011594 011595 011596 011597 011598 011599 011600

167550 167552 167556 167558 170377 000017 167542 105102 167424 167412 167402 167372 104400

15 TRANS AND RECEIVE LOGIC

```

13:  STBUF      :SEND A RUBOUT
      CLR COUNTER
      SHORT WAIT LOOP

14:  WAIT FOR DONE
      BRANCH WHEN DONE
      TIME COUNTER
      BRANCH IF NOT TIME-OUT
      SAVE CSR
      DONE NEVER CAME UP
      R1 = CONTENTS OF CSR
      SAVE TIMER
      READ THE FI/FO
      BRANCH IF CHARACTER READY
      CHARACTER READY DIDN'T SET
      R1 = CONTENTS OF RBUF
      CHECK FOR ERROR BITS
      BRANCH IF NONE
      ERROR IN RECEIVED CHAR
      R1 = CONTENTS OF RBUF
      BIT14=UART OVERRUN
      BIT13=FRAMING ERROR
      BIT12=PARITY ERROR
      DUPLICATE DATA WORD
      MASK LINE #
      LINE # IN LOW BYTE
      CHECK LINE #
      BRANCH IF OK
      WRONG LINE # RECEIVED
      R1 = CONTENTS OF RBUF
      BITS8-11 = LINE #
      GET MASK OF CHARACTER
      CHECK CHAR LENGTH.
      BRANCH IF OK
      WRONG CHARACTER LENGTH
      R1=DATA FROM FI/FO
      R2=MASK (BITS SET NOT EXPECTED)
      REVERSE THE MASK
      CHECK THE ACTUAL DATA
      BRANCH IF OK
      WRONG CHAR LEN OR DATA ERROR
      R1=DATA FROM FI/FO (COMPLETE WORD)
      R2=DATA (LOW BYTE) EXPECTED
      READ FI/FO
      BRANCH IF CHAR PRESENT NOT SET
      CHARACTER PRESENT STAYED SET
      R1 = CONTENTS OF RBUF
      SAVE THE CSR
      CHECK THE CSR
      BRANCH IF OK
      DONE DIDN'T CLEAR OR OTHER CSR ERROR
      R1 = CONTENTS OF CSR
      CLEAR TCR
      CLEAR CSR

15:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

16:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

17:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

18:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

19:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

20:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

21:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

22:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

23:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

24:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

25:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

26:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

27:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

28:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

29:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

30:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

31:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

32:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

33:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

34:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

35:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

36:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

37:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

38:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

39:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

40:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

41:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

42:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

43:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

44:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

45:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

46:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

47:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

48:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

49:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

50:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

51:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

52:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

53:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

54:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

55:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

56:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

57:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

58:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

59:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

60:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

61:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

62:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

63:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

64:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

65:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

66:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

67:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

68:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

69:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

70:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

71:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

72:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

73:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

74:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

75:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

76:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

77:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

78:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

79:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

80:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

81:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

82:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

83:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

84:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

85:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

86:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

87:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

88:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

89:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

90:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

91:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

92:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

93:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

94:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

95:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

96:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

97:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

98:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

99:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

100:  MOV R0, R1
      MOV RBUF, R1
      BPT .+4
      HLT+1

```


H05

TESTS

012046 004737 015556
012048 004737 015556
012050 004737 015556
012052 004737 015556
012054 004737 015556
012056 004737 015556
012058 004737 015556
012060 004737 015556
012062 004737 015556
012064 004737 015556
012066 004737 015556
012068 004737 015556
012070 004737 015556
012072 004737 015556
012074 004737 015556
012076 004737 015556
012078 004737 015556
012080 004737 015556
012082 004737 015556
012084 004737 015556
012086 004737 015556
012088 004737 015556
012090 004737 015556
012092 004737 015556
012094 004737 015556
012096 004737 015556
012098 004737 015556
012100 004737 015556
012102 004737 015556
012104 004737 015556
012106 004737 015556
012108 004737 015556
012110 004737 015556
012112 004737 015556
012114 004737 015556
012116 004737 015556
012118 004737 015556
012120 004737 015556
012122 004737 015556
012124 004737 015556
012126 004737 015556
012128 004737 015556
012130 004737 015556
012132 004737 015556
012134 004737 015556

JSR PC, @XMIT2
MOV @CSR, R1
BNE @R1, +4
DEC R0
BNE @R0, +4
MOV @100405, R1
BNE @R1, +4
MOV @RBUF, R1
BPL @R1, +4
CLR @TCR
CLR @CSR
SCOPE

:SAVE CSR
:CHECK FOR DONE
:BRANCH IF OK
:DONE CAME UP!
:MOS MUST NOT HAVE CLEARED
:TIMER COUNT
:CHECK CSR
:BRANCH IF OK
:CSR ERROR
:CHECK RBUF
:BRANCH IF OK
:RBUF NOT EMPTY!

TEST 53: TEST THAT TRANSMITTER READY CLEARS WHEN RBUF IS
NOTE: DUE TO THE DOUBLE BUFFERING BY THE CPU, RBUF MUST
MUST BE LOADED TO INSURE SEEING TRANS. BY READY CLEAR
PROBABLE FAULTY LOGIC: M7285 02-6 E39, E33, E49

INITIALIZE
DEVICE CSR REGISTER
TESTS: JSR PC, @XMIT2
:WAIT FOR MOS TO CLEAR
SET:
@BIT0 = RECEIVER ENABLE
18: BIS @BIT0, @TCR :TRANS CONTROL LINE 0
MOV @CSR, R1 :WAIT FOR XMIT READY
BPL @R1, +4
25: MOV @RBUF, R1 :TRANSMIT A 1
MOV @CSR, R1 :WAIT FOR XMIT READY
BPL @R1, +4
MOV @RBUF, R1 :TRANSMIT A 2
MOV @CSR, R1 :CHECK FOR XMIT READY
BPL @R1, +4 :BRANCH IF XMIT READY CLEARED
HLT, +1 :TRANSMITTER READY FAILED TO CLEAR
R1 = CONTENTS OF CSR
33: MOV TIMER, R0 :SET UP TIMER
DECB R0 :SHORT WAIT LOOP
BNE @R0, +4
MOV @CSR, R1 :SAVE CSR FOR THE RECORD
BP @R1, +2 :NOP FOR TIMING

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DJ11 LOGIC TESTS
TEST TRANSMIT READ1

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TST53:

012136	005300		DEC	R0	:TIMER COUNT
012140	001371		BNE	35	:BRANCH IF MORE TIME
012142	022701	102605	CMP	#100605,R1	:CHECK CSR
012146	001401		BEG	.+4	:BRANCH IF OK
012150	104001		HLT+1		:DONE DIDN'T SET OR OTHER CSR ERROR
012152	017701	167034	MOV	2RBUF, R1	:R1 = CONTENTS OF CSR
012156	100401		SMT	.+4	:CHECK RBUF FOR CHAR PRESENT
012160	104001		HLT+1		:BRANCH IF CHAR PRESENT
012162	022701	100201	CMP	#100001,R1	:CHAR PRESENT MISSING
012166	001401		BEG	.+4	:R1 = CONTENTS OF RBUF
012170	104001		HLT+1		:CHECK THE DATA
012172	017701	167014	MOV	2RBUF, R1	:BRANCH IF OK
012176	100401		SMT	.+4	:RECEIVER ERROR
012180	104001		HLT+1		:R1 = CNTENTS OF RBUF
012182	022701	100202	CMP	#100002,R1	:CHECK RBUF FOR SECOND CHAR
012186	001401		BEG	.+4	:BRANCH IF CHAR PRESENT
012190	104001		HLT+1		:CHAR PRESENT MISSING
012192	017701	166774	MOV	2RBUF, R1	:R1 = CONTENTS OF RBUF
012196	100001		BPL	.+4	:CHECK THE DATA
012200	104001		HLT+1		:BRANCH IF OK
012202	022701	166762	MOV	2CSR, R1	:RECEIVER ERROR
012206	022701	100405	CMP	#100405,R1	:R1 = CNTENTS OF RBUF
012210	001401		BEG	.+4	:CHECK FOR NO MORE CHARACTERS
012214	104001		HLT+1		:BRANCH IF CHAR PRESENT CLEARED
012216	005077	166752	CLR	2TCR	:CHAR PRESENT NOT CLEAR!
012220	005077	166742	CLR	2CSR	:R1 = CONTENTS OF RBUF
012224	104400		SCOPE		:SAVE CSR
					:CHECK CSR
					:BRANCH IF OK
					:CSR ERROR
					:R1 = CONTENTS OF CSR
					:CLEAR TCR
					:CLEAR CSR

:TEST 54: TEST THAT RECEIVER ENABLE ON A 0 INHIBITS DONE
AND CHARACTER PRESENT.
:PROBABLE FAULTY LOGIC: M7285 (D2-7) E32, E15

012250	012777	000414	166732	TST54:	MOV	#414,	2CSR	:BIT2 = MAINTENANCE
								:BIT3 = CLEAR MOS
								:BIT6 = MASTER TRAN SCAN ENB
012256	032777	000020	166724	105:	BIT	#BIT4,	2CSR	:WAIT FOR MOS TO CLEAR
012264	001374				BNE	105		
012266	052777	000000	166720		BIS	#BIT0,	2TCR	:SET XMTR CONTROL BIT, LINED
012274	017701	166710		15:	MOV	2CSR,	R1	:WAIT FOR XMTR READY
012280	100375				BPL	15		
012282	012777	000252	166706		MOV	#252,	2TBLF	:SEND AN "*"
012286	013700	001302			MOV	TIMER,	R0	:SET UP TIMER
012294	105305			25:	DECB	R5		:SHORT WAIT LOOP
012296	001376				BNE	25		
012298	017701	166664			MOV	2CSR,	R1	:SAVE CSR FOR TYPING

```

012324 105701 TSTB R1 ;CHECK FOR DONE
012326 100002 BPL 3$ ;BRANCH IF NOT SET
012330 104001 HLT+1 ;DONE SET WHEN RCV ENB CLR
;R1=CONTENTS OF CSR
012332 000402 BR 4$
012334 005300 3$: DEC RO ;TIMER COUNT
012336 001366 SNE 2$ ;BRANCH IF MORE TIMER
012340 017701 166646 4$: MOV @RBUF, R1 ;CHECK AND SAVE FI/FO
012344 100001 BPL .+4 ;BRANCH IF OK
012346 104001 HLT+1 ;CHARACTER PRESENT IN FI/FO
;R1=DATA FROM FI/FO
012350 005277 166634 INC @CSR ;SET RECEIVER ENABLE
012354 017701 166630 5$: MOV @CSR, R1 ;SAVE CSR
012360 105701 TSTB R1 ;CHECK FOR DONE
012362 100403 BMI 6$ ;BRANCH IF OK
012364 105300 DECB RO ;SHORT TIMER
012366 001372 SNE 5$
012370 104001 HLT+1 ;DONE DIDN'T COME UP WHEN RECEIVER ENABLED
;UART SHOULD HAVE HELD A CHARACTER
;R1 = CONTENTS OF CSR
012372 017701 166614 6$: MOV @RBUF, R1 ;CHECK FOR CHARACTER PRESENT
012376 100401 BMI .+4 ;BRANCH IF OK
012400 104001 HLT+1 ;CHARACTER PRESENT MISSING
;R1 = CONTENTS OF RBUF
012402 005077 166606 CLR @TCR ;CLR TRANS CONTROL REG
012406 104400 SCOPE

```

```

:*****
:TEST 55: TEST THAT HALF DUPLEX (BIT1) DISABLES THE RECEIVER UARTS.
:PROBABLE FAULTY LOGIC: M7285 (D2-4) E32, E17, E22, (D2-2) E5, E1
:*****

```

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012410 004737 015556 TST55: JSR PC, @#INITC ;INITIALIZE
;BIT1 = HALF DUPLEX
;BIT2 = MAINTENANCE
;BIT3 = CLEAR MOS
;BIT8 = MASTER TRAN SCAN ENB
;WAIT FOR MOS TO CLEAR
;BITC = RECEIVER ENABLE
;SET XMTR CONTROL BIT, LINEC
;WAIT FOR XMTR READY
012414 012777 000001 166572 1$: MOV @BITC, @TCR
012422 017701 166562 MOV @CSR, R1
012426 100375 BPL 1$
012430 012777 000252 16656C MOV #252, @TBUF ;SEND AN "*"
012436 013700 001302 MOV TIMER, RO ;SET UP TIMER
012442 105305 2$: DECB R5 ;SHORT WAIT LOOP
012444 001376 BNE 2$
012446 017701 166536 MOV @CSR, R1 ;SAVE CSR
012452 105701 TSTB R1 ;CHECK FOR DONE
012454 100002 BPL 3$ ;BRANCH IF NOT SET
012456 104001 HLT+1 ;DONE SET WHEN HALF DUPLEX (BIT1) SET
;R1=CONTENTS OF CSR
012460 000402 BR 4$
012462 005300 3$: DEC RO ;TIMER COUNT
012464 001366 SNE 2$ ;BRANCH IF MORE TIMER

```

K05

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TST55:

DJ11 LOGIC TESTS
TEST HALF DUPLEX

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012466 017701 166520
012472 100001
012474 104001

012476 042777 000002 166504
012504 000240
012506 000240
012510 000240
012512 000240
012514 017701 166472
012520 100001
012522 104001

012524 005077 166464

012530 104400

4\$: MOV RBUF, R1 ;CHECK AND SAVE FI/FO
BP .+4 ;BRANCH IF OK
HLT+1 ;CHARACTER PRESENT IN FI/FO
;RI=DATA FROM FI/FO

BIC #BIT1, DCSR ;CLEAR HALF DUPLEX BIT
NOP
NOP
NOP
NOP
5\$: MOV RBUF, R1 ;CHECK FOR CHAR PRESENT
BPL .+4 ;BRANCH IF CHAR NOT PRESENT
HLT+1 ;CHAR PRESENT AFTER H/D CLEARED
;RI = CONTENTS OF RBUF

CLR DTCR ;CLR TRANS CONTROL REG

SCOPE

:TEST 56: TEST THAT RECEIVER INTERRUPT DOES NOT OCCUR AT LEVEL 5
:PROBABLE FAULTY LOGIC: M7921 WIRING, PROPER PRIORITY CHIP

012532 012777 012620 166460
012540 012777 000340 166454
012546 042737 000340 177776
012554 052737 000240 177776
012562 004737 015546

012566 012777 000001 166420
012574 017701 166410
012600 100375
012602 012777 000025 166406
012610 105777 166374
012614 100375
012616 000404

012620 104000
012622 012716 012630
012626 000002

012630 017701 166356
012634 100401
012636 104001

012640 022701 100025
012644 001401
012646 104001

012650 012777 001222 166342

TST56: MOV #ISR56, DRCVVEC ;SET UP XMTR INTERRUPT VECTOR
MOV #340, DRCVLVL ;AT LEVEL 7
BIC #340, D#PS ;CLEAR PS LEVEL
BIS #240, D#PS ;SET PS TO LEVEL 5
JSR PC, D#INITB ;SET:
;BIT2 = MAINTENANCE
;BIT3 = CLEAR MOS
;BIT6 = RECEIVER INTERRUPT ENABLE
;BIT8 = MASTER TRANS SCAN ENABLE
;WAIT FOR MOS TO CLEAR
;BIT0 = RECEIVER ENABLE
;SET TRAN CONTROL BIT, LINE C

1\$: MOV #BIT0, DTCR ;SET TRAN CONTROL BIT, LINE C
MOV DCSR, R1 ;WAIT
BPL 1\$
2\$: MOV #25, DTCR ;SEND #25
TSTB DCSR ;WAIT FOR DONE
BPL 2\$
BR END56 ;OK, BRANCH IF NO INTERRUPT

ISR56: HLT ;SHOULDN'T HAVE INTERRUPTED AT LEVEL 5
MOV #END56, (SP) ;MOVE NEW RTI ADDR ONTO STACK
RTI

END56: MOV RBUF, R1 ;READ THE CHARACTER
BMI .+4 ;BRANCH IF CHAR PRESENT
HLT+1 ;CHAR PRESENT MISSING
;RI = CONTENTS OF RBUF

CMP #100025, R1 ;CHECK THE DATA
BEQ .+4 ;BRANCH IF OK
HLT+1 ;RECEIVED DATA ERROR
;RI = CONTENTS OF RBUF

MOV RCVLVL, DRCVVEC

L05

3056 012656 012777 000004 166336 MOV #IOT, @RCVLVL
3057 012664 005077 166324 CLR @TCR
3058 012670 005077 166314 CLR @CSR
3059 012674 042737 000340 177776 BIC #340,@#PS
3070 012702 104400 SCOPE

:TEST 57: TEST THAT RECEIVER INTERRUPT OCCURS AT LEVEL 4
:PROBABLE FAULTY LOGIC: M7821 WIRING, PROPER PRIORITY CHIP

3071 012704 012777 012774 166306 TST57: MOV #ISR57, @RCVVEC ;SET UP XMTR INTERRUPT VECTOR
3072 012712 012777 000340 166302 MOV #340, @RCVLVL ;AT LEVEL 7
3073 012720 042737 000340 177776 BIC #340, @#PS ;CLEAR PS LEVEL
3074 012726 052737 000200 177776 BIS #200, @#PS ;SET PS TO LEVEL 4
3075 012734 004737 015546 JSR PC, @#INIT9 ;SET:
3076 ;BIT2 = MAINTENANCE
3077 ;BIT3 = CLEAR MOS
3078 ;BIT6 = RECEIVER INTERRUPT ENABLE
3079 ;BIT8 = MASTER TRANS SCAN ENABLE
3080 ;WAIT FOR MOS TO CLEAR
3081 ;BIT0 = RECEIVER ENABLE
3082 012740 012777 000001 166246 IS: MOV #BIT0, @TCR ;SET TRAN CONTROL BIT, LINE 0
3083 012746 017701 166236 MOV @CSR, R1 ;WAIT
3084 012752 100375 BPL IS
3085 012754 012777 000025 166234 ES: MOV #25, @TBUF ;SEND #25
3086 012762 105777 166222 TSTB @CSR ;WAIT FOR DONE
3087 012766 100375 BP 25
3088 012770 104000 HLT ;SHOULD HAVE INTERRUPTED AT LEVEL 4
3089 012772 000403 BR ENDS7 ;CONTINUE
3090 012774 012716 013002 ISR57: MOV #ENDS7,(SP) ;MOVE NEW RTI ADR ONTO STACK
3091 013000 000002 RTI
3092 013002 017701 166204 ENDS7: MOV @RBUF, R1 ;READ THE CHARACTER
3093 013006 100401 BMI .+4 ;BRANCH IF CHAR PRESENT
3094 013010 104001 HLT+1 ;CHAR PRESENT MISSING
3095 ;R1 = CONTENTS OF RBUF
3096 013012 022701 100025 CMP #100025,R1 ;CHECK THE DATA
3097 013016 001401 BEQ .+4 ;BRANCH IF OK
3098 013020 104001 HLT+1 ;RECEIVED DATA ERROR
3099 ;R1 = CONTENTS OF RBUF
3100 013022 013777 001222 166170 MOV RCVLVL, @RCVVEC
3101 013030 012777 000004 166164 MOV #IOT, @RCVLVL
3102 013036 005077 166152 CLR @TCR
3103 013042 005077 166142 CLR @CSR
3104 013046 042737 000340 177776 BIC #340,@#PS
3105 013054 104400 SCOPE

:TEST 60: TEST FI/FO OVERRUN
: THE FI/FO BUFFER SHOULD HOLD 64 CHARACTERS.
:

MOS

MAY 1970-11-02 DJ11 LOGIC TESTS
TEST FI/FO OVERRUN

TEST FI/FO OVERRUN

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: PROBABLE FAULTY LOGIC: M7285 (D1-7) E32, E17, E22 (D2-2) E5, E1
:*****

: INITIALIZE
: DEVICE "CSR" REGISTER

013056 004737 015566

TST60: JSR PC, 2*INITD SET:
:BIT2 = MAINTENANCE
:BIT3 = CLEAR MOS
:BIT8 = MASTER XMTR SCAN ENB

: WAIT FOR MOS TO CLEAR

SET:
:BIT0 = RECEIVER ENABLE

013062 012777 177777 166124

MOV #177777, 2*CR : TRANS CONTROL BIT, ALL LINES
MOV #100, RO : SET UP COUNTER - 64. CHAR FI/FO BLFF
18: MOV 2*CSR, R1 : SAVE AND WAIT FOR TRANS READY

013070 012700 000100

013074 017701 166110

013100 100375

013102 000377 166110

013106 032701 020000

013112 001401

013114 104001

BPL IS : TRANSMIT LINE # ON LINE
SWAB 2*BUF : CHECK FI/FO OVERRUN
BIT #BIT13, R1 : BRANCH IF OK
BEQ .+4 : FI/FO OVERRUN TOO SOON
HLT+1 : R1=CONTENTS OF CSR
: COUNT DOWN

013116 005300

013120 001365

DEC RO
BNE IS

013122 013700 001302

013126 017701 166056

013132 100375

013134 105305

013136 001376

013140 017701 166044

013144 100401

013146 104001

28: MOV TIMER, RO : SET UP TIMER
MOV 2*CSR, R1 : WAIT FOR XMTR READY
BPL 28
38: DECB R5 : SHORT WAIT LOOP
BNE 38
MOV 2*CSR, R1 : SAVE CSR FOR THE RECORD
BMI .+4 : BRANCH IF TRANS READY
HLT+1 : TRANS READY MISTEROUSLY

013150 005300

013152 001370

DEC RO : R1=CONTENTS OF CSR
BNE 38 : TIME 3 CHARACTER LENGTHS
: BRANCH IF MORE TIME

: FI/FO SHOULD NOW BE FULL

013154 105701

013156 100401

013160 104001

013162 022701 100605

013166 001401

013170 104001

TSTB R1 : CHECK THAT DONE IS SET
BMI .+4 : BRANCH IF OK
HLT+1 : DONE DIDN'T COME UP!
: R1 = CONTENTS OF CSR
CMP #100605, R1 : CHECK THAT FI/FO NOT OVERRUN
BEQ .+4 : BRANCH IF OK
HLT+1 : FI/FO OVERRUN SET
: OR SOME OTHER CSR ERROR
: R1=CONTENTS OF CSR

:*****
: TEST 60A: TEST THAT FI/FO OVERRUN COMES UP WHEN 65TH CHARACTER
: IS RECEIVED WITHOUT READING FI/FO
:*****

013172 000377 166020

013176 013700 001302

T60A: SWAB 2*BUF : SEND 65TH CHARACTER
MOV TIMER, RO : SET UP TIMER

013056
013062
013070
013074
013100
013102
013106
013112
013114
013116
013120
013122
013126
013132
013134
013136
013140
013144
013146
013150
013152
013154
013156
013160
013162
013166
013170
013172
013176

N05

MAINDEC-11-DZDJA-D
DZDJA.D.P11 TST60:

DJ11 LOGIC TESTS
TEST FI/FO OVERRUN

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```

3178 013202 105305      11$:  DECB  R5      ;SHORT WAIT LOOP
3179 013204 001376      BNE   11$
3180 013206 017701 165776  MOV  JCSR,R1    ;SAVE CSR
3181 013212 032701 023000  BIT  #BIT13,R1  ;CHECK FI/FO OVERRUN
3182 013216 001003      BNE   12$      ;BRANCH WHEN SET
3183 013220 005300      DEC  R0        ;TIMER
3184 013222 001367      BNE   11$      ;BRANCH IF MORE TIME
3185 013224 104001      HLT+1         ;FI/FO OVERRUN DIDN'T COME UP

```

```

3186 013226 022701 120605 12$:  CMP   #120605,R1 ;CHECK TOTAL CSR
3187 013232 001401      BEQ   .+4      ;BRANCH IF OK
3188 013234 104001      HLT+1         ;SOMETHING IN CSR FOULED UP

```

```

:*****
:TEST 50B:  TEST THAT READING THE RECEIVER BUFFER CAUSES FI/FO
:           OVERRUN TO CLEAR.
:           NOTE:  BECAUSE OF TIMING OF THE FI/FO, FI/FO OVERRUN CAN COME
:           BACK UP AFTER READING ONE CHARACTER, SO A SECOND MUST
:           BE READ TO INSURE THAT FI/FO OVERRUN IS CLEAR.
:*****

```

```

3189 013236 012700 000002  T50B: MOV  #2, R0    ;SET UP COUNTER - 2 CHARACTERS
3190 013242 017701 165744 21$:  MOV  RBUF, R1   ;CHECK AND SAVE FIRST CHAR IN FI/FO
3191 013246 100401      BMI   .+4      ;BRANCH IF CHAR PRESENT
3192 013250 104001      HLT+1         ;CHARACTER PRESENT GONE!

```

```

3193 013252 032701 070000      BIT  #070000,R1 ;CHECK RECEIVER ERRORS
3194 013256 001401      BEQ   .+4      ;BRANCH IF OK
3195 013260 104001      HLT+1         ;RECEIVER ERROR

```

```

3196 013262 010102      MOV  R1, R2    ;PUT LINE # IN R2
3197 013264 000302      SWAB R2
3198 013266 042702 177760  BIC  #177760,R2
3199 013272 120102      CMPB R1, R2   ;CHECK DATA (=LINE#)
3200 013274 001401      BEQ   .+4      ;BRANCH IF OK
3201 013276 104001      HLT+1         ;WRONG DATA RECEIVED

```

```

3202 013300 005300      22$:  DEC  R0        ;COUNT CHARACTERS
3203 013302 001403      BEQ   24$      ;BRANCH WHEN DONE
3204 013304 105305      23$:  DECB R5        ;SHORT WAIT LOOP - GIVE FI/FO TIME
3205 013306 001376      BNE   23$
3206 013310 000754      BR   21$      ;GO READ ANOTHER

```

```

3207 013312 017701 165672 24$:  MOV  JCSR, R1   ;SAVE CSR
3208 013316 022701 100605  CMP  #100605,R1 ;CHECK THAT FI/FO OVERRUN CLEARED
3209 013322 001401      BEQ   .+4      ;BRANCH IF OK
3210 013324 104001      HLT+1         ;FI/FO OVERRUN DIDN'T CLR

```

```

3211 013324 104001      HLT+1         ;OR SOMEOTHER CSR PROBLEM
3212 013324 104001      HLT+1         ;R1=CONTENTS OF CSR

```



```

TEST 62:
014312 017701 164676 MOV 2BCSR, R1 :CHECK AND SAVE BCSR
014314 022701 177777 CMP 2BCSR, R1 :CHECK THAT ALL THE BITS ARE SET
014316 001401 BEQ .+4 :BRANCH IF OK
014318 104001 HLT+1 :BIT(S) OF BCSR FAILED TO SET

014326 005077 164660 CLR 2BCSR :CLEAR BCSR
014328 017701 164656 MOV 2BCSR, R1 :CHECK THAT IT CLEARED AND SAVE
014330 001401 BEQ .+4 :BRANCH IF CLR
014332 104001 HLT+1 :BIT(S) OF BCSR FAILED TO CLEAR

014342 104400 SCOPE

```

```

*****
TEST 63: TEST THAT LINED CAN TRANSMIT AND RECEIVE A BREAK
ALSO CHECKS FRAMING ERROR(RBUF BIT13)
ALSO CHECKS PARITY ERROR(RBUF BIT12)
IF ODD PARITY IS SELECTED
PROBABLE FAULTY LOGIC: M7295 (D2-2) E5, E1, (D2-3) E16, E2, E19, E35
*****

```

```

014344 004707 015536 TEST63: JSR PC, @INITA :INITIALIZE
:BIT2 = MAINTENANCE
:BIT3 = CLEAR MOS
:BIT10 = R/W BCSR
:WAIT FOR MOS TO CLEAR
:BIT0 = RECEIVER ENABLE
:SEND BREAKS, LINE C
:SET UP TIMER
:SHORT WAIT LOOP

014350 000001 164636 MOV 2BCSR, R1 :SAVE CSR
014352 001302 18: MOV TIMER, R0 :CHECK FOR DONE
014354 005305 DEC8 R5 :BRANCH WHEN DONE
014356 001376 164616 BNE 2BCSR, R1 :WAIT A WHILE
014358 005701 YSTB R1 :DONE NEVER CAME UP
014360 004404 BMI 2BCSR, R1 :R1=CONTENTS OF CSR
014362 005200 INCR R0
014364 001270 BNE 18
014366 104001 HLT+1

014374 000430 24: BR 45
014376 002205 CMP #2205, R1 :CHECK REST OF CSR
014378 001401 BEQ .+4 :BRANCH IF OK
014380 104001 HLT+1 :CSR ERROR
:R1=CONTENTS OF CSR

014386 017701 164570 MOV 2RBUF, R1 :GET DATA FROM FI FO
014388 004401 BMI .+4 :BRANCH IF OK
014390 104001 HLT+1 :CHARACTER PRESENT NOT LF
:R1=CONTENTS OF RBUF

014396 002701 020000 BIT #020000, R1 :CHECK FOR FRAMING ERROR
014398 001001 BNE .+4 :BRANCH IF OK
014400 104001 HLT+1 :FRAMING ERROR NOT UP
:R1=CONTENTS OF RBUF

014406 132737 001310 001276 BITB DJPAR, PARITY :CHECK ODD PARITY FLAG
014408 001404 BEQ 35 :BRANCH IF NOT
014410 002701 BIT #010000, R1 :CHECK PARITY ERROR
014412 001005 BNE 45

```


014700 000000
014701 000000
014702 000000
014703 000000
014704 000000
014705 000000
014706 000000
014707 000000
014708 000000
014709 000000
014710 000000
014711 000000
014712 000000
014713 000000
014714 000000
014715 000000
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014717 000000
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014703 000000
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014702 000000
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014701 000000 000000 000000 000000 000000 000000 000000 000000 000000
014702 000000 000000 000000 000000 000000 000000 000000 000000 000000
014703 000000 000000 000000 000000 000000 000000 000000 000000 000000
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014705 000000 000000 000000 000000 000000 000000 000000 000000 000000
014706 000000 000000 000000 000000 000000 000000 000000 000000 000000
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014719 000000 000000 000000 000000 000000 000000 000000 000000 000000
014720 000000 000000 000000 000000 000000 000000 000000 000000 000000

:CHECK DATA FROM FI FO
:BRANCH IF OK
:CHARACTER PRESENT NOT LP
:R1 = LINE #
:R2 = CONTENTS OF RBUF

:CHECK FOR FRAMING ERROR
:BRANCH IF OK
:FRAMING ERROR NOT LP
:R1 = LINE #
:R2 = CONTENTS OF RBUF

:SET LINE #
:R1 = LINE #
:R2 = CONTENTS OF RBUF

:CHECK ODD PARITY FLAG
:BRANCH IF NOT
:CHECK PARITY ERROR
:ODD PARITY SHOULD CAUSE PARITY ERROR
:R1 = LINE #
:R2 = CONTENTS OF RBUF

:CHECK PARITY ERROR
:BRANCH IF OK
:EVEN PARITY OR NO PARITY
:SHOULDN'T CAUSE PARITY ERROR
:R1 = LINE #
:R2 = CONTENTS OF RBUF

:CHECK UART OVERRUN
:BRANCH IF OK
:UART OVERRUN SET!!
:R1 = LINE #
:R2 = CONTENTS OF RBUF

:MOV R2, R3
:SWAB R3
:OR R3, R2
:AND R3, R3
:OR R3, R3
:MOV R1, R3
:BEQ R1, R3
:HLT+2

:CHECK DATA

```

TST64:

```

014722 001401 BEQ .+4 :BRANCH IF OK
014724 104002 HLT+2 :WRONG DATA RECEIVED
:R1 = LINE #
:R2 = CONTENTS OF RBUF
014726 017702 164260 MOV 3RBUF, R2 :READ FI/FO AGAIN
014730 100001 BPL .+4 :BRANCH IF OK
014734 104002 HLT+2 :EXTRA CHAR IN FI/FO
:R1 = LINE #
:R2 = CONTENTS OF RBUF
014736 005077 164252 CLR 3BCSR :CLEAR BREAK CONTROL REG
014742 005201 INC R1 :COUNT LINES
014744 006204 ASL R4 :UPDATE LINE MARKER
014746 103000 BCC LOP64 :BRANCH IF MORE LINES

014750 005077 164234 CLR 3CSR :CLEAR CSR
014754 104400 SCOPE

014756 012737 000002 015772 MOV #2, TIMES

```

```

:*****
:TEST 55: TEST THAT RESET CLEARS ALL BUFFERS
:NOTE: THE FI/FO BUFFER IS NOT COMPLETELY CLEARED
: BY RESET; ONLY CHARACTER PRESENT IS CLEARED.
:PROBABLE FAULTY LOGIC: M7285 (D2-8) E13
:*****

```

```

014754 002737 000340 177775 TST65: BIS #340,3#PS :SET PROCESSOR TO LEVEL 7
014772 012777 177777 164214 MOV #177777,3TCR :SET ALL TCR BITS
015000 012777 052507 164202 MOV #052507,3CSR :SET ALL R/W BITS OF CSR
015006 012777 177777 164200 MOV #177777,3BCSR :SET ALL BREAK CONTROL BITS SEND BREAKS:
:NOTE: ALL LINES SHOULD BE SENDING BREAKS, BUT NONE SHOULD BE RECEIVING
: BECAUSE THE HALF DUPLEX BIT IS SET
015014 012777 177777 164174 MOV #177777,3TBUF :LOADING TRANS BUFF WHEN BREAK BIT SET
: SHOULD DO NOTHING
015022 000005 RESET :CLEAR THE WORLD
015024 013737 001210 015034 MOV CSR,16 :CHECK CSR AND SAVE
015032 013701 MOV 3(PC)+,R1
15: 000000
015036 001401 BEQ .+4
015040 104001 HLT+1

015042 017701 164146 MOV 3TCR,R1 :CHECK TCR AND SAVE
015046 001401 BEQ .+4
015050 104001 HLT+1

015052 017701 164136 MOV 3BCSR,R1 :CHECK BCSR AND SAVE
015056 001401 BEQ .+4
015060 104001 HLT+1

015062 017701 164124 MOV 3RBUF,R1 :CHECK RBUF AND SAVE
015066 100001 BPL .+4
015070 104001 HLT+1

015072 017701 164120 MOV 3TBUF,R1 :CHECK TBUF AND SAVE
015076 001401 BEQ .+4
015100 104001 HLT+1

```

J06

MA:NDCC-11-020JA-D
020JAP.P11

TST66:

DJ11 LOGIC TESTS
TEST RESET

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015102
015104
015106
015112
015114
015122
015130
015134
015142
015150
015156
015160
015166
015174
015200
015204
015206
015212
015214
015216
015220
015222
015226
015232
015234
015236
015242
015244
015246
015252
015254
015260
015262
015266
015270
015272
015274
015300
015302

104400
035001
012703 100000
035004
042737 000340 177776
052737 000200 177776
012700 000001
012777 000010 164046
012777 010505 164040
032777 000020 164032 105:
001374
012777 015274 164032
012777 000240 164026
010077 164014
035777 164004
010477 164004
105204
001371
105703
001376
017702 163762
022702 110505
001401
104002
017702 163750
100001
104002
062703 000400
005201
032701 000003
001002
005237 001306
006300
103341
000417
017702 163712
100401
104002

SCOPE

:TEST 66: SEND A BINARY COUNT PATTERN ON EACH LINE
:PROBABLE FAULTY LOGIC: COULD BE ALMOST ANYWHERE!

TST66: CLR R1 :SET UP LINE COUNTER
MOV #100000,R3 :SET UP RCV DATA
CLR R4 :SET UP TRANS DATA
BIC #340, @#PS :CLEAR PROCESSOR PRIORIT:
BIS #200, @#PS :SET PRIORITY TO 4
MOV #1, R0 :SET UP LINE MARKER
MOV #10, @CSR :CLEAR MOS
MOV #010505, @CSR :BIT0 = RECEIVE ENABLE
 :BIT2 = MAINTENANCE
 :BIT6 = RECEIVER INTERRUPT ENB
 :BIT8 = TRANS SCAN ENABLE
 :BIT12= STATUS ENABLE
 :WAIT FOR MOS TO CLEAR
105: BIT #BIT4, @CSR
BNE 105
MOV #ISR66, @RCVVEC :SET UP RECEIVER INTERRUPT VECTOR
MOV #240, @RCV_LVL
15: MOV R0, @TCR :TRANS CONTROL, ONE LINE AT A TIME
25: TST @CSR :WAIT FOR TRANS READY
BPL @R0
MOV #4, @RBUF :SEND DATA
INCB R4, :BINARY COUNT
35: BNE @R0 :WAIT FOR RECEIVER DONE
MOV @CSR, R2 :SAVE CSR
CMP #110505, R2 :CHECK CSR
BEQ .+4 :BRANCH IF OK
HLT+2 :CSR ERROR
 :R1=LINE #
 :R2=CONTENTS OF CSR
MOV @RBUF, R2 :CHECK CHARACTER PRESENT
BPL .+4 :BRANCH IF JK
HLT+2 :CHARACTER PRESENT SET!!
 :R1=LINE #
 :R2=CONTENTS OF CSR
45: ADD #400, R3 :UPDATE LINE # IN EXPECTED DATA
INC R1 :UPDATE LINE #
BIT #3, R1 :CHECK FOR FOURTH LINE
BNE 45 :BRANCH IF NOT
INC @JLEN :MOVE CHARACTER LENGTH POINTER
ASL R0 :UPDATE LINE MARKER
BCC 15 :BRANCH IF MORE
BR END66 :SKIP ISR
ISR66: MOV @RBUF, R2 :READ FIRST DATA
BMI 115 :BRANCH IF CHARACTER PRESENT
HLT+3 :INTERRUPT BUT NO CHAR PRESENT

TST65:

```

0738 ;R1=LINE #
0739 ;R2=CONTENTS OF RBUF
0740 ;R3=EXPECTED DATA
0741 015304 020203 11$: CMP R2 R3 ;CHECK THE DATA
0742 015306 001401 BEQ .+4 ;BRANCH IF OK
0743 015300 04003 HLT+3 ;DATA ERROR
0744 ;R1=LINE #
0745 ;R2=CONTENTS OF RBUF
0746 ;R3=EXPECTED DATA
0747 015312 105203 INCB R3 ;UPDATE EXPECTED DATA
0748 015314 147703 163766 BICB DJLEN, R3 ;MASK CHARACTER LENGTH
0749 015320 001403 BEQ 2$ ;BRANCH OUT IF DATA=C
0750 015322 017702 163664 MOV RBUF, R2 ;READ MORE DATA
0751 015326 100766 BMI 11$ ;BRANCH IF MORE
0752 015330 000002 12$: RTI ;RETURN
0753
0754 015332 162737 000004 001306 ENDS: SUB #4, DJLEN ;RESET CHAR LENGTH POINTER
0755 015340 013777 001222 163652 MOV RCVLVL, JRCVVEC ;RESTORE RECEIVER INT. VEC
0756 015346 012777 000004 163646 MOV #IOT, JRCVLVL
0757 015354 005077 163634 CLR JTCR ;CLEAR TCR
0758 015360 005077 163624 CLR JCSR ;CLEAR CSR
0759 015364 104400 SCOPE
0760
0761 015366 012737 000020 015772 MOV #20, TIMES
0762 015374 023737 001304 001234 CMP DJUNT, UNITS ;CHECK FOR LAST UNIT
0763 015402 002002 BEG DCNE ;BRANCH IF LAST UNIT
0764 015404 000137 002302 JMP RESTAR ;JUMP IF NOT
0765
0766 015410 DONE:
0767 015410 004737 017640 JSR PC, KBCINT
0768 015414 062737 000001 001206 ADD #1, PCNT+2 ;ADD 1 TO THE PASS COUNT
0769 015422 005537 001204 ADC PCNT ;MAKE IT DOUBLE PREC.
0770 015426 032777 002000 163662 BIT #SW10, JSWR ;RING THE BELL?
0771 015434 001004 BNE 1$ ;NO!
0772 015436 000004 000007 TYPE .BELL ;RING THE BELL
0773 015442 000004 000177 TYPE ,177 ;TYPE A FILLER FOR 11/05
0774 015446 005046 1$: CLR -(6) ;CLEAR TRACE TRAP
0775 015450 032777 010000 163640 BIT #SW12, JSWR ;RUN WITH TRT?
0776 015456 001010 BNE 2$ ;SKIP T BIT
0777 015460 005137 015532 COM .TBIT ;COMPLIMENT FLAG
0778 015464 100005 BPL 2$ ;SKIP IF PLUS
0779 015466 052716 000020 BIS #20, (6) ;SET TRACE TRAP
0780 015472 012746 015526 MOV #3$, -(6) ;JUMP TO START OF TEST
0781 015476 000002 RTI ;RETURN
0782 015500 012746 015506 2$: MOV #4$, -(6) ;JUMP TO START OF TEST
0783 015504 000002 RTI ;RETURN
0784 015506 013700 000042 4$: MOV #42, RD ;GET MONITOR ADDRESS
0785 015512 001405 BEQ 3$ ;IF NONE
0786 015514 000005 RESET ;RESET AND
0787 015516 SENDAD =
0788 015516 004710 JSR 7, (0) ;GO TO MONITOR
0789 015520 000240 NOP ;SAVE RCOM
0790 015522 000240 NOP ;FOR
0791 015524 000240 NOP ;ACT11
0792 015526 000137 002302 3$: JMP RESTAR ;RETRN
0793

```

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015600

000000
000002
012777 002014 163444
000413
012777 000514 163434
000407
012777 000416 163424
000403
012777 000414 163414
005000
005200
001004
011600
162700 000002
104000
032777 000020 163370
001366
052777 000001 163360
000207

.TBIT: 0 ;T BIT FLAG
YESRT: RTI ;RETLPM FROM TRACE TRAP
INITIALIZATION ROUTINE
DEVICE CSR REGISTER
ON FAILURE: REGISTER D CONTAINS ERROR ADDRESS
SET:
:BIT01 = HALF DUPLEX
:BIT02 = MAINTENANCE
:BIT03 = CLEAR MOS
:BIT05 = RECEIVER INTERRUPT ENABLE
:BIT08 = MASTER XMTR SCAN ENB
:BIT10 = R/W BCSR
:WAIT FOR MOS TO CLEAR
:SET:
:BIT00 = RECEIVER ENABLE
INITA: MOV #2014, @CSR ;SET
BR INTR ;BIT(S)2,3,10 THEN 0
INITB: MOV #514, @CSR ;BIT(S)2,3,6,8 THEN 0
BR INTR
INITC: MOV #416, @CSR ;BIT(S)1,2,3,9 THEN 0
BR INTR
INITD: MOV #414, @CSR ;BIT(S)2,3,9 THEN 0
INITR: CLR RC
IS: INC RC ;ANTI HANG
BNE 2S ;ROUTINE
MOV (SP), R0 ;RECORD SUBROUTINE CALL RETURN
SUB #2, R0 ;FORM CALL ADDRESS FOR DISPLAY
HLT ;BIT#4 OF DEVICE CSR FAILED TO CLEAR
2S: BIT #BIT4, @CSR ;TEST HAS MOS CLEARED
BNE 1S ;NO BRANCHES
BIS #1, @CSR ;SET
RTS PC ;BIT00 RECEIVE ENABLE
;CONTINUE

:
: \$SCOPE SCOPE LOOP HANDLER
: THIS ROUTINE HANDLES THE ITERATIONS, LOOPING, ERROR
: LOOPING, AND THE DISPLAYING OF THE TEST NUMBER.

MO6

MANUFC-11-0000A-0
 11/17/76

0111 LOGIC TESTS
 SCOPE LOOP HANDLER

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:"SCOPE" IS PLACED BETWEEN EACH SUBTEST IN THE TEST AND
 RECORDS THE STARTING ADDRESS OF THE SUBTEST IN "LAD:"

3850											
3851											
3852											
3853	015632	004737	017640			TRAPS:	JSR	PC,	KBDINT		
3854	015636	002777	000400	163452			BIT	*SW8,2SWR		:LOOP ON SPEC. TEST?	
3855	015644	001404					BEQ	IS		:NO LOOP ON SPEC. TEST	
3856	015646	127737	163444	001200			CMPB	2SWR,ICNT		:ON RIGHT TEST? *SW7-C*	
3857	015654	001434					BEQ	OVERS		:NOT RIGHT TEST	
3858	015656	002777	040000	163432	1\$:		BIT	*SW14,2SWR		:LOOP ON TEST?	
3859	015664	001026					BNE	KITS		:LOOP ON TEST IS SET	
3860	015666	002777	004000	163422			BIT	*SW11,2SWR		:KILL ITERATIONS	
3861	015674	001012					BNE	SVLADS		:YES - KILL ITERATIONS	
3862	015676	105737	001201				TSTB	ICNT+1		:FIRST ONE?	
3863	015702	001404					BEQ	2\$:BRANCH IF FIRST	
3864	015704	123737	015772	001201			CMPB	TIMES,ICNT+1		:DONE?	
3865	015712	001013					BNE	KITS		:BRANCH IF NOT	
3866	015714	112737	000001	001201	2\$:		MCVB	#1,ICNT+1		:FIRST ITERATION	
3867	015722	105237	001200			SVLADS:	INCB	ICNT		:COUNT TEST NUMBERS	
3868	015726	011637	015770				MOV	(6) LAD		:SAVE LOOP ADDRESS	
3869	015732	013737	001200	001320			MOV	ICNT,2*DISPLAY		:DISPLAY TEST NO. AND ITERATION COUNT	
3870	015740	000002					RTI			:RETURN	
3871											
3872	015742	105237	001201			KITS:	INCB	ICNT+1		:INC THE ITERATION COUNT	
3873	015746	013737	001200	001320	OVERS:		MOV	ICNT,3*DISPLAY		:SET UP DISPLAY	
3874	015754	105737	015770				TST	LAD		:FIRST ONE?	
3875	015760	001760					BEQ	SVLADS		:YES	
3876	015762	013716	015770				MOV	LAD,(5)		:FUDGE RETURN ADDRESS	
3877	015766	000002					RTI			:FIXES PS	
3878											
3879	015770	000000				LAD:	0			:LOOP ADDRESS	
3880	015772	000000				TIMES:	20			:RUN 20 TIMES	

: \$HLT ERROR TIMEOUT HANDLER

: THIS ROUTINE PRINTS OUT ERROR MESSAGES STARTING WITH THE
: ADDRESS OF THE "HLT". IT ALSO COUNTS THE NUMBER OF ERRORS
: AND HAS THE CAPABILITY OF LOOPING ON ERROR, BELL ON ERROR,
: "HALT" ON ERROR, AND INHIBIT TIMEOUTS. AN OPTIONAL ARGUMENT
: (HLT+3) WILL BE PLACED IN "HLTCT\$:" FOR ADITIONAL TYPEOUTS.

015774
016000
016006
016010
016014
016020
016026
016030
016040
016044
016052
016050
016064
016070
016100
016104
016110
016112
016114
016120
016126
016130
016132
016136
016142
016144
016146
016152
016156
016164
016170
016172
016200
016204
016206
016212
016214

004737 017640
032777 002000 163310
001402
000004 000007
005237 001202
032777 020000 163270
001026
000004 016034
011637 016144
162737 000002 016144
117737 000066 016142
013705 016144
004737 016562
000004 016074
004737 016146
005777 163206
004737 017640
032777 001000 163170
001001
000002
000002
004737 017640
032777 001000 163170
001001
000002
015037 001201
000137 015742
000000
000000
013705 01210
004737 016562
042737 007700 016204
105337 016142
100411
062737 000100 016204
000004 017241
010005
004737 016562
000764
000207

EMTS: JSR PC, KBDINT
BIT #SW10,2SWR
BEQ 1\$
TYPE BELL
1\$: INC ERRORS
BIT #SW13,2SWR
BNE 2\$
TYPE ..+2
MOV (6),HLTADR
SUB #2,HLTADR
MOV8 \$HLTADR,HLTCT\$
MOV HLTADR,TTY
JSR PC,PRINTR
TYPE ..+2
JSR PC,ERRORS
2\$: TST 2SWR
BPL .+4
HALT
JSR PC,KBDINT
BIT #SW9,2SWR
BNE .+4
RTI
CLRB ICNT+1
JMP KITS
HLTCT\$: 0
HLTADR: 0
ERRORS:
MOV CSR,TTY
JSR PC,PRINTR
BIC #7700,2\$
1\$: DECB HLTCT\$
BMI 3\$
ADD #100,2\$
TYPE SPACE
2\$: MOV %0,TTY
JSR %7,PRINTR
BR 1\$
3\$: RTS PC

: BELL ON ERROR?
: NO - SKIP
: RING BELL
: COUNT THE NUMBER OF ERRORS
: SKIP TIMEOUT IF SET
: SKIP TYPEOUTS
: .ASCIZ <15><12>
: PUT ADDRESS OF I INSTRUCTION ON STACK
: FUDGE ADDRESS
: GET HLT ARGUMENT
: TYPE HLTADR IN OCTAL
: TYPE LEADING ZERO'S
: .ASCIZ " "
: GO TO USER ERROR ROUTINE
: HALT ON ERROR
: SKIP IF CONTINUE
: HALT ON ERROR!
: CHECK FOR INHIBIT LOOP ON ERROR
: SKIP IF LOOP ON ERROR
: RETURN
: CLEAR ITERATION COUNT
: LOOP ON TEST UNTIL NO ERRORS
: HLT ARGUMENT
: LAST HLT INSTRUCTION EXECUTED
: TYPE CSR IN OCTAL
: TYPE LEADING ZERO'S
: TYPE REGISTER X IN OCTAL

ROUTINES

SUBROUTINE TO SAVE INPUT AS TOTAL NUMBER

```

      SUBROUTINE SAVEIN (N)
      DIMENSION T(100)
      COMMON /SAVEIN/ T
      IF (N) GOTO 1
      READ (5,*) N
      IF (N) GOTO 1
      DO 10 I=1,N
      READ (5,*) T(I)
      10 CONTINUE
      WRITE (6,*) T
      RETURN
      END

```

```

      SUBROUTINE SAVEIN (N)
      DIMENSION T(100)
      COMMON /SAVEIN/ T
      IF (N) GOTO 1
      READ (5,*) N
      IF (N) GOTO 1
      DO 10 I=1,N
      READ (5,*) T(I)
      10 CONTINUE
      WRITE (6,*) T
      RETURN
      END

```


=====

*****			*****			*****			*****			*****			*****		
346	346	346	346	346	346	346	346	346	346	346	346	346	346	346	346	346	
353	353	353	353	353	353	353	353	353	353	353	353	353	353	353	353	353	
356	356	356	356	356	356	356	356	356	356	356	356	356	356	356	356	356	
363	363	363	363	363	363	363	363	363	363	363	363	363	363	363	363	363	
365	365	365	365	365	365	365	365	365	365	365	365	365	365	365	365	365	
367	367	367	367	367	367	367	367	367	367	367	367	367	367	367	367	367	
371	371	371	371	371	371	371	371	371	371	371	371	371	371	371	371	371	
372	372	372	372	372	372	372	372	372	372	372	372	372	372	372	372	372	
373	373	373	373	373	373	373	373	373	373	373	373	373	373	373	373	373	
374	374	374	374	374	374	374	374	374	374	374	374	374	374	374	374	374	
375	375	375	375	375	375	375	375	375	375	375	375	375	375	375	375	375	
376	376	376	376	376	376	376	376	376	376	376	376	376	376	376	376	376	

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M07

		3904*	2875*	2398*	3038*	3083*	3128*	3478*	3554*	3662	3767*	3842*	2853*	3897*
		3902*	3904*	3908*	3920*	3929*	3934*	3995*	4038*	4193*	4208*	4209*	4220*	4222*
		4240*												
PCNT	001204	537*	592*	593*	3768*	3769*	3794							
PDOWN\$	016744	537*	4040*	4062										
PRINTR	C16562	3902	3920	3927	4007*	4232								
PRINTS	016572	693	687	4009*										
PS	= 177776	486*	1234*	1235*	1250*	1262*	1263*	1278*	1290*	1291*	1306*	1318*	1319*	1334*
		1346*	1347*	1362*	1374*	1375*	1390*	1402*	1403*	1418*	1430*	1431*	1446*	3026*
		3037*	3069*	3081*	3082*	3114*	3240*	3241*	3299*	3300*	3366*	3652*	3694*	3695*
		3961	3965*											
SYSTEMP	016352	3961*	3965	3968*										
TUP\$	017010	4049	4052*											
PLVECS	C17100	4040*	4041*	4049*	4071*									
ROUF	001212	540*	752*	1492	1523	1575	1606	1658	1689	1741	1772	1826	1857	1909
		1940	1992*	2023	2075	2106	2160	2191	2243	2274	2326	2357	2409	2440
		2494	2525	2577	2608	2660	2691	2743	2774	2827	2855	2905	2913	2921
		2962	2975	3011	3020	3057	3102	3201	3261	3266	3325	3356	3405	3428
		3501	3535	3581	3630	3675	3721	3735	3750					
RCVLEV	001222	3546*	760*	3035*	3065	3066*	3080*	3110	3111*	3243*	3360	3361*	3706*	3755
		3756*												
RCVVEC	001220	545*	739*	746*	759	3034*	3065*	3079*	3110*	3242*	3301*	3360*	3705*	3755*
READIN	016216	600	611	3933*	4234									
READS	016364	623	661	690	705	3934	3970*							
RESTAR	002202	532	597	663	671	673	724*	3764	3792	4055				
RETURN	017236	4120*												
RO	=:000000	487*	573*	574*	575*	576*	577*	578*	579*	580*	581*	592*	593*	595*
		664*	668*	676*	720*	721	732*	733	734*	735*	736	1112*	1115*	1121
		1153*	1156*	1164	1202*	1207*	1211*	1214*	1491*	1486*	1491	1564*	1569*	1574
		1647*	1652*	1657	1730*	1735*	1740	1815*	1820*	1825	1898*	1903*	1909	1991*
		1986*	1991	2064*	2069*	2074	2149*	2154*	2159	2232*	2237*	2242	2215*	2323*
		2325	2398*	2403*	2408	2483*	2489*	2493	2566*	2571*	2576	2649*	2654*	2659
		2732*	2737*	2742	2788*	2789*	2790*	2791*	2793	2839*	2849*	2893*	2898*	2950*
		2959*	2970*	2999*	3008*	3136*	3144*	3147*	3156*	3177*	3193*	3200*	3221*	3255*
		3281*	3324*	3341*	3343	3389*	3394*	3485*	3491*	3562*	3569*	3696*	3707	3731*
		3784*	3828*	3930*	3833*	3834*	4042	4051*	4159*	4163	4165*	4171*	4172	
R1	=:000001	488*	626*	628	630	632*	645	646*	647*	648*	650*	651*	653*	655
		657	665*	666*	677*	682	685*	686	688*	716	750*	751*	752	753*
		754	756*	757	758*	759	760	761	762	763	764	787*	951*	952*
		956	962	968*	980*	996*	997	1005*	1006	1020*	1030*	1042*	1043	1049*
		1061*	1062	1070*	1071	1095*	1095*	1113*	1122*	1123*	1124*	1125	1134*	1150*
		1167	1186*	1203*	1212*	1220*	1238*	1266*	1294*	1322*	1350*	1378*	1406*	1424*
		1478*	1488*	1492*	1496	1503	1512	1519	1523*	1527*	1528	1561*	1571*	1575*
		1579	1586	1595	1601	1606*	1610*	1611	1644*	1654*	1659*	1662	1669	1679
		1684	1689*	1693*	1694	1727*	1737*	1741*	1745	1752	1761	1767	1772*	1776*
		1777	1812*	1822*	1826*	1830	1837	1846	1852	1857*	1861*	1862	1835*	1925*
		1909*	1913	1920	1929	1935	1940*	1944*	1945	1978*	1998*	1992*	1996	2003
		2012	2018	2023*	2027*	2028	2061*	2071*	2075*	2079	2086	2095	2101	2106*
		2110*	2111	2145*	2156*	2160*	2164	2171	2180	2196	2191*	2195*	2196	2229*
		2239*	2243*	2247	2254	2263	2269	2274*	2278*	2279	2312*	2322*	2326*	2330*
		2337	2346	2352	2357*	2361*	2362	2395*	2405*	2409*	2413	2420	2439*	2430*
		2440*	2444*	2445	2480*	2490*	2494*	2498	2505	2514	2520	2525*	2539*	2530*
		2563*	2573*	2577*	2581	2588	2597	2603	2608*	2612*	2613	2646*	2656*	2650*
		2664	2671	2680	2686	2691*	2695*	2696	2729*	2739*	2743*	2747	2751*	2753*
		2763	2774*	2778*	2779	2814*	2827*	2830*	2831	2843*	2844	2851	2855*	2853*
		2886*	2889*	2896*	2901	2905*	2909	2913*	2917	2921*	2925*	2926	2941*	2953*

4-772 1044-1045
 4-773 1046-1047
 4-774 1048-1049

4-775 1050-1051
 4-776 1052-1053
 4-777 1054-1055

4-778 1056-1057
 4-779 1058-1059
 4-780 1060-1061

4-781 1062-1063
 4-782 1064-1065
 4-783 1066-1067

4-784 1068-1069
 4-785 1070-1071
 4-786 1072-1073

4-787 1074-1075
 4-788 1076-1077
 4-789 1078-1079

4-790 1080-1081
 4-791 1082-1083
 4-792 1084-1085

4-793 1086-1087
 4-794 1088-1089
 4-795 1090-1091

4-796 1092-1093
 4-797 1094-1095
 4-798 1096-1097

4-799 1098-1099
 4-800 1100-1101
 4-801 1102-1103

4-802 1104-1105
 4-803 1106-1107
 4-804 1108-1109

4-805 1110-1111
 4-806 1112-1113
 4-807 1114-1115

4-808 1116-1117
 4-809 1118-1119
 4-810 1120-1121

4-811 1122-1123
 4-812 1124-1125
 4-813 1126-1127

4-814 1128-1129
 4-815 1130-1131
 4-816 1132-1133

4-817 1134-1135
 4-818 1136-1137
 4-819 1138-1139

16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1

4-820 1140-1141
 4-821 1142-1143
 4-822 1144-1145

4-823 1146-1147
 4-824 1148-1149
 4-825 1150-1151

4-826 1152-1153
 4-827 1154-1155
 4-828 1156-1157

4-829 1158-1159
 4-830 1160-1161
 4-831 1162-1163

4-832 1164-1165
 4-833 1166-1167
 4-834 1168-1169

4-835 1170-1171
 4-836 1172-1173
 4-837 1174-1175

4-838 1176-1177
 4-839 1178-1179
 4-840 1180-1181

4-841 1182-1183
 4-842 1184-1185
 4-843 1186-1187

4-844 1188-1189
 4-845 1190-1191
 4-846 1192-1193

4-847 1194-1195
 4-848 1196-1197
 4-849 1198-1199

4-850 1200-1201
 4-851 1202-1203
 4-852 1204-1205

4-853 1206-1207
 4-854 1208-1209
 4-855 1210-1211

4-856 1212-1213
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4-859 1218-1219
 4-860 1220-1221
 4-861 1222-1223

4-862 1224-1225
 4-863 1226-1227
 4-864 1228-1229

4-865 1230-1231
 4-866 1232-1233
 4-867 1234-1235

TESTS
USER SYMBOLS

40220			
40220			
40220	4022	40220	

