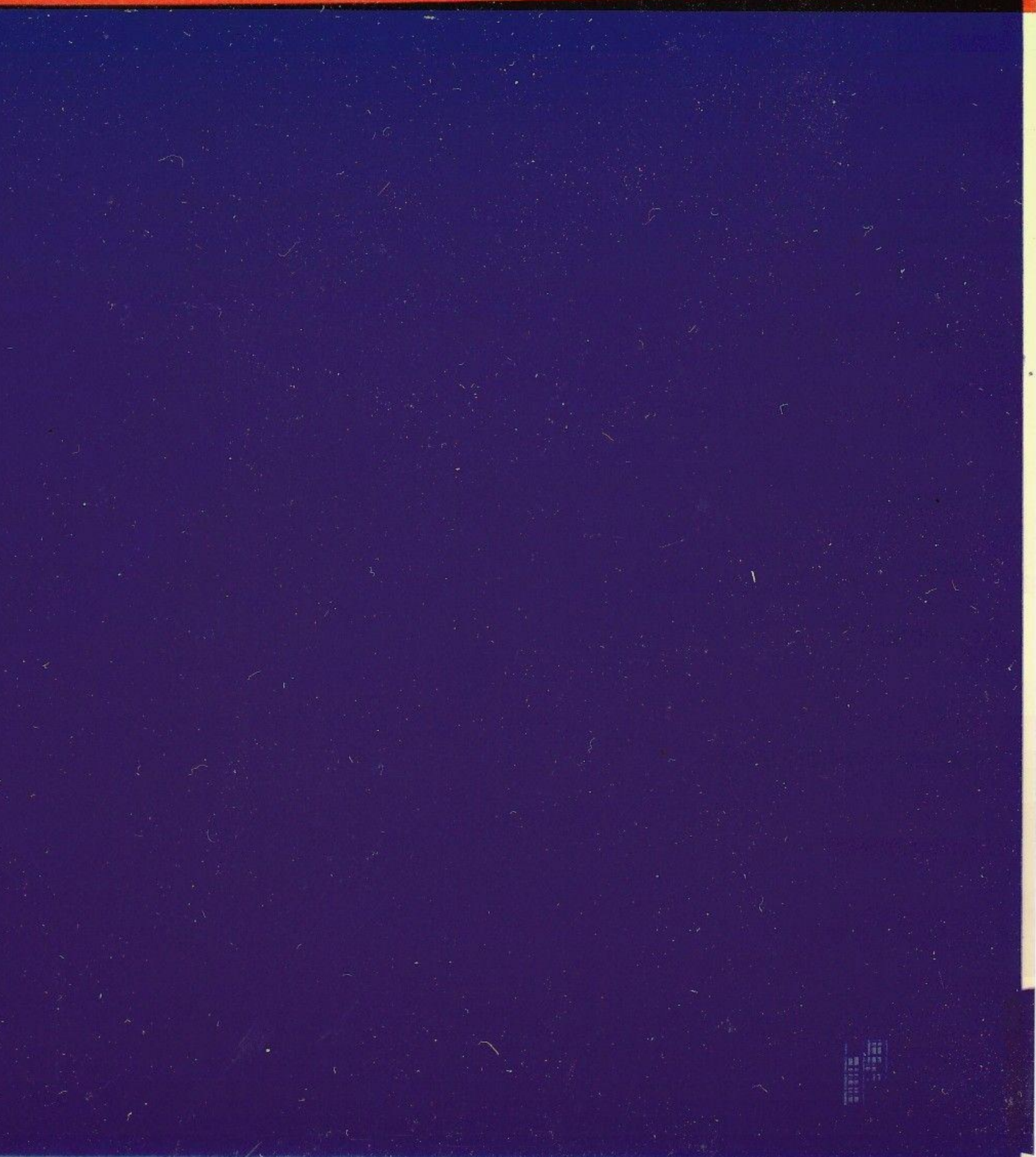


DH11

LOGIC TEST
MD-11-DZDHC-B

EP-DZDHC-B-DL-A
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IDENTIFICATION

PROJECT CODE: RAJNCEC-11-CZC-4-B-D
 PROJECT NAME: DUAL TRANSMITTER AND RECEIVER
 LOGIC TEST
 DATE: APRIL 1976
 REVISION: DIAGNOSTIC GROUP
 AUTHOR: MICHAEL DAVIS

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ABSTRACT

THE D41 TRANSMITTER AND RECEIVER LOGIC TEST CHECKS
THE D41 TRANSMITTER AND RECEIVER FUNCTIONS.
FUNCTIONS TESTED INCLUDE INTERRUPTS, OPERATION OF
TRANSMITTER NAR LOGIC, AND OPERATION OF RECEIVER SILO LOGIC.

4.3 (CONT'D)

4.3.1.6 TYPE IN THE ADDRESS OF THE RECEIVER INTERRUPT VECTOR FOR THE DH11 TO BE TESTED FOLLOWED BY <CARRIAGE RETURN>

NOTE: WORDS IN ANGLE BRACKETS, I.E. <CARRIAGE RETURN> MEAN THAT THE TELETYPE KEY WITH THE NAMED FUNCTION SHOULD BE PRESSED

IF AN INCORRECT ADDRESS IS ENTERED, THE PROGRAM WILL TYPE "?" AND WILL REPEAT THE SECOND MESSAGE OF 4.3.1.5

4.3.1.7 THE PROGRAM WILL TYPE "CONTROL REGISTER ADDRESS-" AND WAIT FOR AN INPUT FROM THE TELETYPE KEYBOARD

4.3.1.8 TYPE IN THE ADDRESS OF THE SYSTEM CONTROL REGISTER OF THE DH11 TO BE TESTED FOLLOWED BY <CARRIAGE RETURN>

IF AN INCORRECT ADDRESS IS TYPED, THE PROGRAM WILL TYPE "?" AND WILL THEN REPEAT THE MESSAGE OF 4.3.1.7

4.3.1.9 THE PROGRAM WILL TYPE "R" TO INDICATE THAT IT IS ABOUT TO START TESTING, AND THEN TESTING WILL BEGIN

4.3.2 PROGRAM RESTART WITH ALL SWITCHES DOWN

4.3.2.1 PERFORM 4.3.1.2 TO 4.3.1.5

4.3.2.2 THE PROGRAM WILL TYPE "DH11 XXXX" AND WILL THEN CONTINUE AS DESCRIBED IN 4.3.1.9

4.3.3 PROGRAM RESTART WITH SW00=1

4.3.3.1 LOAD ADDRESS 000200

4.3.3.2 SET SW01=1

4.3.3.3 PRESS START

4.3.3.4 THE PROGRAM WILL PERFORM AS DESCRIBED IN 4.3.1.5 TO 4.3.1.9

4.3.4 PROGRAM RESTART WITH SW01=1

4.3.4.1 LOAD ADDRESS 000200

4.3.4.2 SET SW01=1

4.3.4.3 PRESS START

4.3.4.4 THE PROGRAM WILL TYPE "DH11 XXXX" AND WILL THEN TYPE "TEST PC-" AND WILL WAIT FOR AN INPUT FROM THE TELETYPE KEYBOARD

4.3.4.5 TYPE IN THE ADDRESS OF THE TEST AT WHICH THE PROGRAM IS TO BE STARTED FOLLOWED BY <CARRIAGE RETURN>

4.3.4.6 THE PROGRAM WILL TYPE R TO INDICATE THAT IT HAS STARTED AND WILL START TESTING AT THE SELECTED TEST.

NOTE: CARE MUST BE TAKEN WHEN THIS FEATURE IS USED, SINCE THERE IS NO PROTECTION AGAINST SELECTING AN ADDRESS THAT IS IN THE MIDDLE OF A TEST

NOTE: IF IT IS DESIRED TO LOOP ON THE TEST THAT IS SELECTED SET SW14=1 BEFORE ENTERING THE TEST ADDRESS

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5. OPERATING PROCEDURE

5.1 OPERATIONAL SWITCH SETTINGS

SW15=1. HALT ON ERROR
SW14=1. LOOP ON CURRENT TEST
SW13=1. SUPPRESS ERROR TYPEOUT
SW11=1. INHIBIT ITERATIONS
SW10=1. ESCAPE TO NEXT TEST ON ERROR
SW09=1. FREEZE VARIABLE PARAMETER IN CURRENT TEST
SW01=1. START PROGRAM AT SELECTED TEST
SW00=1. CHANGE PARAMETERS AT PROGRAM RESTART

5.2 SUBROUTINE ABSTRACTS

5.2.1 TRAPCATCHER (LOCATIONS 000000-000776)

THIS ROUTINE IS USED TO INTERCEPT UNEXPECTED INTERRUPTS AND TRAPS. THE AREA FROM 000000-000776 IS LOADED WITH THE FOLLOWING SEQUENCE

2
0
4
0
0
772
0
776
0

IF AN UNEXPECTED INTERRUPT OR TRAP OCCURS, THE PROGRAM WILL HALT WITH THE PC 2 GREATER THAN THE ADDRESS TO WHICH THE PROGRAM TRAPPED. THE PROCESSOR STACK MAY BE EXAMINED TO DETERMINE WHERE THE PROGRAM WAS WHEN THE TRAP OR INTERRUPT OCCURED.

5.2.2 START (PROGRAM INITIALIZATION)

THIS ROUTINE INITIALIZES ALL PROGRAM FLAGS AND COUNTERS. TYPES THE PROGRAM TITLE MESSAGE, AND INPUTS THE VECTOR AND CONTROL REGISTER ADDRESSES OF THE DMI TO BE TESTED.

5.2.3 BEGIN (PROGRAM START AND RESTART)

THIS ROUTINE IS ENTERED IMMEDIATLY AFTER "START" AND EACH TIME A PROGRAM PASS HAS BEEN COMPLETED. THE ROUTINE SETS UP THE PROCESSOR STACK AND STATUS WORD AND THEN TRANSFERS CONTROL TO THE TEST AT WHICH TESTING WILL BEGIN. IF SW01=0 WHEN THIS ROUTINE IS ENTERED TESTING WILL START AT T1 (TEST 1). IF SW01=1 WHEN THIS ROUTINE IS ENTERED, TESTING WILL START AT THE PC ENTERED FROM THE TELETYPE KEYBOARD.

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5.2.4 EOP (END OF PASS)

THIS ROUTINE IS ENTERED ONCE PER PASS AFTER ALL TESTS HAVE BEEN COMPLETED. THIS ROUTINE TYPES THE MAINDEC IDENTIFICATION CODE OF THE PROGRAM, CLEARS ERROR FLAGS AND UPDATES THE PASS COUNT. IF THE PROGRAM WAS LOADED UNDER ACT11 OR DDP, THE ROUTINE CHECKS FOR RETURN TO THE ACT11 OR DDP MONITOR. IF THE PROGRAM IS NOT UNDER MONITOR CONTROL, THE ROUTINE TRANSFERS TO BEGIN.

5.2.5 SCOPER (SCOPE LOOP AND ITERATION HANDLER)

THIS ROUTINE IS ENTERED EACH TIME A TEST IS COMPLETED. THE ROUTINE CHECKS FOR THE FOLLOWING UPON ENTRY
A) IF SW10=1, THE ROUTINE WILL TRANSFER TO THE NEXT TEST IN SEQUENCE, AFTER CLEARING ERROR FLAGS.
B) IF SW11=1, THE ROUTINE WILL TRANSFER TO THE NEXT TEST SEQUENCE, AFTER CLEARING ERROR FLAGS.
C) IF SW14=1, THE ROUTINE WILL LOOP ON THE CURRENT TEST REGARDLESS OF THE ITERATION COUNT.

IF NONE OF THE ABOVE IS TRUE, THE ROUTINE WILL ADD 1 TO THE COUNT OF TEST ITERATIONS, AND COMPARE THIS VALUE TO THE NUMBER OF ITERATIONS THAT SHOULD BE PERFORMED. IF THESE NUMBERS ARE EQUAL, THE ROUTINE WILL TRANSFER TO THE NEXT TEST IN SEQUENCE. IF THE NUMBERS ARE NOT EQUAL, THE TEST CURRENTLY IN PROGRESS WILL BE REPEATED.

5.2.6 SCOP1R (FREEZE ON CURRENT DATA)

THE CALL TO THIS ROUTINE FOLLOWS IMMEDIATELY AFTER THE CALL TO THE ERROR HANDLER IN THOSE TESTS THAT HAVE VARIABLE PARAMETERS. THIS ROUTINE IS ALWAYS ENTERED IN THOSE TESTS, WHETHER OR NOT AN ERROR OCCURS. IF SW09=1, THE ROUTINE WILL TRANSFER CONTROL BACK TO THE TEST AT A POINT WHICH WILL ALLOW REPEATING THE FUNCTION UNDER TEST CONTINUOUSLY WITH THE SAME DATA. IF THIS OPTION IS SELECTED, THE ROUTINE "SCOPER" IS NEVER ENTERED AND ITERATION COUNTS WILL NOT BE UPDATED.

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5.2.7 ERRORS (ERROR HANDLER)

THIS ROUTINE IS ENTERED UPON ERROR DETECTION ONLY. WITH ALL CONSOLE SWITCHES DOWN, THE ROUTINE PROCEEDS AS FOLLOWS:

- A) THE PC OF THE INSTRUCTION THAT CALLED THE ERROR HANDLER IS ACCESSED THRU THE STACK, AND WHEN THE EMT INSTRUCTION ITSELF IS FETCHED. THE 8 LSB OF THE EMT INSTRUCTION ARE THE ERROR CODE. THIS CODE IS USED TO ACCESS A TABLE OF ERROR MESSAGES AND ERROR DATA STORAGE LOCATIONS.
- B) IF THE TEST THAT FAILED DID NOT FAIL PREVIOUSLY DURING THIS PASS, A COMPLETE ERROR REPORT IS MADE IF THE TEST THAT FAILED FAILED MOR THAT ONCE DURING THE CURRENT PASS, ONLY THE DATA RELATING TO THE FAILUER IS TYPED. IF SW13=1, NO ERROR TYPEOUT IS MADE.
- C) THE ROUTINE NOW CHECKS FOR HALT ON ERROR. IF SW15=1 THE PROGRAM WILL HALT WITH THE PC OF THE CALL TO THE ERROR ROUTINE IN RO. IF SW15=0, THE PROGRAM WILL NOT HALT, BUT WILL CHECK FOR ESCAPE TO NEXT TEST.
- D) IF SW10=0, THE ROUTINE WILL RETURN TO THE TEST IN PROGRESS. IF SW10=1, THE ROUTINE WILL ABORT THE CURRENT TEST, AND TRANSFER TO THE NEXT TEST IN SEQUENCE, THRU THE ROUTINE "SCOPER".

5.2.8 TRPSRV (TRAP DECODE AND DISPATCH)

THIS ROUTINE DECODES THE 9 LSB OF THE TRAP INSTRUCTION THAT CAUSED TH PROGRAM INTERRUPT, AND TRANSFERS CONTROL TO THE ROUTINE THRU THE TABLE "TRPTAB" USING THE 9 LSB OF THE TRAP INSTRUCTION AS AN OFFSET TO THE POINTER TO THE ROUTINE TO BE ENTERED.

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- 5.3 PROGRAM AND OR OPERATOR ACTION
- 5.3.1 PROGRAM START WITH ALL SWITCHES DOWN
 - 5.3.1.1 REFER TO SECTIONS 4.3.1 AND 4.3.2 FOR INITIAL PROGRAM BEHAVIOR.
 - 5.3.1.2 AFTER "R" HAS BEEN TYPED BY THE PROGRAM, TEST EXECUTION WILL BEGIN. EACH TEST WILL BE REPEATED A SELECTED NUMBER OF ITERATIONS (SEE LISTING FOR EXACT NUMBER FOR EACH TEST) AND THEN THE PROGRAM WILL PROCEED TO THE NEXT TEST.
 - 5.3.1.3 WHEN ALL ITERATIONS HAVE BEEN COMPLETED, THE PROGRAM WILL TYPE "DZDHX" AND THEN RESTART TESTING AT TEST 1 (LOCATION T1 IN THE PROGRAM).
 - 5.3.1.4 IF AN ERROR OCCURS, THE PROGRAM WILL TYPE AN APPROPRIATE ERROR MESSAGE, AND THEN CONTINUE THE TEST IN PROGRESS.
- 5.3.2 PROGRAM START WITH SW00=1
THE PROGRAM WILL PERFORM AS DESCRIBED IN 4.3.1 AND 5.3.1
- 5.3.3 PROGRAM START WITH SW01=1
 - 5.3.3.1 REFER TO SECTION 4.3.4 FOR INITIAL PROGRAM BEHAVIOR
 - 5.3.3.2 TEST EXECUTION WILL START AT THE ADDRESS SPECIFIED AND WILL CONTINUE AS DESCRIBED IN 5.3.1.2
 - 5.3.3.3 AFTER "DZDHX" HAS BEEN TYPED, THE PROGRAM WILL RESUME TESTING AT TEST 1
- 5.3.4 PROGRAM OPERATION WITH SW15=1
SAME AS 5.3.1, EXCEPT THAT IN THE CASE OF AN ERROR, THE PROGRAM WILL HALT AFTER THE ERROR TYPEOUT, AND THE PC+2 OF THE CALL TO THE ERROR ROUTINE WILL BE DISPLAYED IN RO.
- 5.3.5 PROGRAM OPERATION WITH SW13=1
SAME AS 5.3.1 EXCEPT THAT NO ERROR TYPEOUTS WILL OCCUR
- 5.3.6 PROGRAM OPERATION WITH SW11=1
SAME AS 5.3.1 EXCEPT THAT EACH TEST WILL BE REPEATED ONCE ONLY
- 5.3.7 PROGRAM OPERATION WITH SW10=1
SAME AS 5.3.1, EXCEPT THAT IN THE CASE OF AN ERROR THE CURRENT TEST WILL BE ABORTED, AND THE PROGRAM WILL PROCEED TO THE NEXT TEST IN SEQUENCE.

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5. (CONT'D)

5.3.8 PROGRAM OPERATION WITH SW14=1. OR SW09=1

THESE FUNCTIONS ARE NORMALLY USED FOR TROUBLE SHOOTING.
SEE SECTION 6.3 FOR THEIR USE.

6. ERRORS

6.1 ERROR HALTS

THE ERROR MESSAGE FORMAT FOR ALL ERROR TYPEOUTS
IS AS FOLLOWS

PC+2 MESSAGE
HEADER (IF APPLICABLE)
DATA (IF APPLICABLE)

WHERE

PC+2 IS THE ADDRESS OF THE CALL TO THE ERROR HANDLER + 2
MESSAGE IS AN ASCII MESSAGE DESCRIBING (BRIEFLY) THE FAILURE
HEADER IS A DESCRIPTION OF THE DATA TO FOLLOW
DATA IS OCTAL INFORMATION RELATING TO THE CAUSE OF THE FAILURE
IF THE SAME ERROR OCCURS IN A GIVEN TEST ON THE SAME
PASS, AND IF DATA IS ASSOCIATED WITH THAT ERROR, ONLY
DATA IS TYPED ON SUCCEEDING ERROR TYPEOUTS

IF NO DATA IS ASSOCIATED WITH THE ERROR
THE COMPLETE ERROR MESSAGE IS TYPED.

6.1.1 ERROR DESCRIPTIONS

SEE LISTING FOR DETAILS OF ERRORS

6.2 ERROR RECOVERY

6.2.1 SW15=0

IF THE PROGRAM IS RUN WITH SW15=0, NO OPERATOR ACTION IS
REQUIRED TO CONTINUE TESTING

6.2.2 SW15=1

IF THE PROGRAM IS RUN WITH SW15=1, TO CONTINUE TESTING
AFTER THE PROGRAM HAS HALTED, PRESS THE PROCESSOR
CONSOLE CONTINUE SWITCH

6.2.3 ILLEGAL INTERRUPTS

IF AN INTERRUPT OCCURS TO A VECTOR ADDRESS NOT
SELECTED DURING PROGRAM INITIALIZATION, THE PROGRAM WILL
HALT IN THE TRAPCATCHER. THE ADDRESS AT WHICH
THE PROGRAM HALTS IS 2 GREATER THAN THE ADDRESS
TO WHICH THE INTERRUPT OCCURED. THE PROGRAM MUST BE
RESTARTED AT 200 TO RECOVER FROM THIS ERROR.

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- 6.3 SCOPE LOOPING
- 6.3.1 TO SCOPE ON A SPECIFIC TEST, SET SW14=1 AND SW13=1
THIS WILL CAUSE THE PROGRAM TO CONTINUOUSLY LOOP ON THE
SAME TEST, AND WILL CAUSE ALL ERROR TYPEOUTS TO BE INHIBITED
- 6.3.2 TO SCOPE ON A SPECIFIC VALUE OF A PARAMETER WITHIN
A TEST, SET SW09=1 TO FREEZE THE DATA
(SEE LISTING FOR THOSE TESTS THAT INCORPORATE THIS FEATURE)

6. (CONT'D)

- 6.3.3 PROGRAM START TO SCOPE LOOP ON SELECTED TEST
PERFORM SECTION 4.3.4 WITH SW14=1

7. RESTRICTIONS

- 7.1 STARTING
THE DH11 TEST CARD MUST BE INSTALLED

- 7.2 RUNNING
NONE

8. MISCELLANEOUS

- 8.1 EXECUTION TIME
THE TIME FOR ONE PASS OF THE PROGRAM (END OF
TYPEOUT OF DZDHX TO END OF TYPEOUT OF DZDHX)
IS GIVEN FOR VARIOUS PROCESSORS IN THE TABLE BELOW

PROCESSOR	TIME
PDP-11/05,10	
PDP-11/20	
PDP-11/40	
PDP-11/45	

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9. PROGRAM DESCRIPTION

THE FIRST GROUP OF TESTS VERIFIES THAT NO INTERRUPTS OCCUR WITH INTERRUPT ENABLES SET FOR EACH INTERRUPTING FUNCTION AND THE ASSOCIATED DONE BIT OR FLAG FOR THAT FUNCTION CLEARED.

THE NEXT GROUP OF TESTS VERIFIES THAT AN INTERRUPT DOES OCCUR IF A SPECIFIC DONE BIT OR FLAG IS SET, ALONG WITH ITS CORRESPONDING INTERRUPT ENABLE.
AT THIS TIME, INTERRUPTS TO THE CORRECT VECTOR ARE TESTED. IF AN INTERRUPT OCCURS TO ANY VECTOR OTHER THAN THOSE SELECTED AT PROGRAM START, THE PROGRAM WILL HALT IN THE TRAPCATCHER IN A LOCATION 2 GREATER THAN THE ADDRESS OF THE VECTOR TO WHICH THE INTERRUPT OCCURED.

THE NEXT GROUP OF TESTS CHECKS TRANSMITTER NPR AND INTERRUPT LOGIC OPERATION FOR EACH LINE, IN AN INDIVIDUAL TEST FOR EACH LINE. THE BYTE COUNT FOR THE SELECTED LINE IS SET TO -1 (FOR 1 CHARACTER TRANSMISSION) AND THE BUS ADDRESS MEMORY LOCATION FOR THAT LIN IS SET TO 0. THE BAR BIT FOR THE SELECTED LINE IS SET, TRANSMITTER INTERRUPT ENABLE IS SET, AND THE PROCESSOR STATUS WORD IS CLEARED TO ALLOW INTERRUPTS TO OCCUR. A DELAY LOOP IS THEN ENTERED, AND IF THE DELAY TIMES OUT BEFORE AN INTERRUPT OCCURS, AN ERROR MESSAGE IS TYPED. IF AN INTERRUPT DOES OCCUR, THE CONTROL REGISTER IS TESTED TO SEE IF THE TRANSMITTER DONE BIT HAS BEEN SET, THE BAR REGISTER IS CHECKED TO SEE THAT THE BAR BIT FOR THE SELECTED LIN HAS CLEARED, BYTE COUNT IS CHECKED TO SEE THAT IT WENT TO 0 AND THE BUS ADDRESS REGISTER FOR THE SELECTED LINE IS CHECKED TO SEE THAT IT INCREMENTED TO 1.

THE NEXT GROUP OF TESTS VERIFIES THAT A SINGLE SELECTED LINE WILL PERFORM TRANSMIT FUNCTIONS WITHOUT AFFECTING ANY OTHER LINE. THIS IS DONE BY SETTING ALL BYTE COUNTS TO -1, AND VERIFYING THAT ONLY THE LINE SELECTED FOR TRANSMISSION HAD CHANGES MADE IN BYTE COUNT AND BUS ADDRESS WHEN TRANSMISSION HAS BEEN COMPLETED.

THE NEXT TEST VERIFIES THAT A SINGLE CHARACTER CAN BE LOADED INTO THE SILO (IN MAINTENANCE MODE). THE TEST IS MADE WITH INTERRUPTS ENABLED AND CHECKS ARE MADE TO DETERMINE IF RECEIVER DONE WAS SET, IF THE SILO FILL LEVEL REGISTER WAS INCREMENTED, AND IF THE DATA RECEIVED IN MAINTENANCE MODE WAS CORRECT.

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9. (CONT'D)

THE NEXT TEST VERIFIES THAT FROM 1 TO 63 CHARACTERS CAN BE LOADED INTO THE SILO, AND THAT THE SILO FILL LEVEL REGISTER INDICATES THE CORRECT NUMBER OF CHARACTERS IN THE SILO.

THE NEXT TEST VERIFIES THAT 64 CHARACTERS CAN BE LOADED INTO THE SILO, FROM 1 TO 64 CHARACTERS CAN BE READ OUT OF THE SILO, AND THAT THE SILO FILL REGISTER INDICATES THE NUMBER OF CHARACTERS REMAINING IN THE SILO.

THE FINAL TEST VERIFIES THAT THE CHARACTER AVAILABLE FLAG WILL NOT BE SET UNTIL THE SILO FILL LEVEL EXCEEDS THE SILO ALARM LEVEL, FOR ALL ALARM LEVELS 0-63.

10. LISTING

!

:DH11 TRANSMITTER AND RECEIVER BASIC LOGIC TEST
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:STARTING PROCEDURE
:LOAD PROGRAM
:LOAD ADDRESS 000200
:PRESS START
:PROGRAM WILL TYPE DH11 TRANSMITTER AND RECEIVER BASIC LOGIC TEST
:PROGRAM WILL TYPE "VECTOR ADDRESS-"
:TYPE IN THE ADDRESS OF THE RECEIVER INTERRUPT VECTOR
:FOR THE DH11 TO BE TESTED, FOLLOWED BY <CARRIAGE RETURN>
:PROGRAM WILL TYPE "CONTROL REGISTER ADDRESS-"
:TYPE IN THE ADDRESS OF THE SYSTEM CONTROL REGISTER
:FOR THE DH11 TO BE TESTED, FOLLOWED BY <CARRIAGE RETURN>
:PROGRAM WILL TYPE "R" TO INDICATE THAT TESTING HAS STARTED
:AT THE END OF A PASS, PROGRAM WILL TYPE " DZDHC "
:AND THEN RESUM TESTING

:SWITCH REGISTER OPTIONS

100000
040000
020000
010000
004000
002000
001000
000400
000100
000040
000020

SW15=100000 :=1,HALT ON ERROR
SW14=40000 :=1,LOOP ON CURRENT TEST
SW13=20000 :=1,INHIBIT ERROR TYPEOUT
SW12=10000
SW11=4000 :=1,INHIBIT ITERATIONS
SW10=2000 :=1,ESCAPE TO NEXT TEST ON ERROR
SW09=1000 :=1,LOOP WITH CURRENT DATA
SW08=400
SW06=100
SW05=40
SW04=20

NO1

553 000010
554 000004
555 000002
556 000001
557

SW03=10
SW02=4
SW01=2
SW00=1

:RESTART PROGRAM AT SELECTED TEST
:RESELECT VECTOR AND CONTROL REGISTER
:ADDRESS AFTER PROGRAM RESTART

717	000334	000336	.+2	:UNEXPECTED TRAP TO THIS LOCATION
718	000336	000000	HALT	:EXAMINE STACK TO FIND CAUSE
719	000340	000342	.+2	:UNEXPECTED TRAP TO THIS LOCATION
720	000342	000000	HALT	:EXAMINE STACK TO FIND CAUSE
721	000344	000346	.+2	:UNEXPECTED TRAP TO THIS LOCATION
722	000346	000000	HALT	:EXAMINE STACK TO FIND CAUSE
723	000350	000352	.+2	:UNEXPECTED TRAP TO THIS LOCATION
724	000352	000000	HALT	:EXAMINE STACK TO FIND CAUSE
725	000354	000356	.+2	:UNEXPECTED TRAP TO THIS LOCATION
726	000356	000000	HALT	:EXAMINE STACK TO FIND CAUSE
727	000360	000362	.+2	:UNEXPECTED TRAP TO THIS LOCATION
728	000362	000000	HALT	:EXAMINE STACK TO FIND CAUSE
729	000364	000366	.+2	:UNEXPECTED TRAP TO THIS LOCATION
730	000366	000000	HALT	:EXAMINE STACK TO FIND CAUSE
731	000370	000372	.+2	:UNEXPECTED TRAP TO THIS LOCATION
732	000372	000000	HALT	:EXAMINE STACK TO FIND CAUSE
733	000374	000376	.+2	:UNEXPECTED TRAP TO THIS LOCATION
734	000376	000000	HALT	:EXAMINE STACK TO FIND CAUSE
735	000400	000402	.+2	:UNEXPECTED TRAP TO THIS LOCATION
736	000402	000000	HALT	:EXAMINE STACK TO FIND CAUSE
737	000404	000406	.+2	:UNEXPECTED TRAP TO THIS LOCATION
738	000406	000000	HALT	:EXAMINE STACK TO FIND CAUSE
739	000410	000412	.+2	:UNEXPECTED TRAP TO THIS LOCATION
740	000412	000000	HALT	:EXAMINE STACK TO FIND CAUSE
741	000414	000416	.+2	:UNEXPECTED TRAP TO THIS LOCATION
742	000416	000000	HALT	:EXAMINE STACK TO FIND CAUSE
743	000420	000422	.+2	:UNEXPECTED TRAP TO THIS LOCATION
744	000422	000000	HALT	:EXAMINE STACK TO FIND CAUSE
745	000424	000426	.+2	:UNEXPECTED TRAP TO THIS LOCATION
746	000426	000000	HALT	:EXAMINE STACK TO FIND CAUSE
747	000430	000432	.+2	:UNEXPECTED TRAP TO THIS LOCATION
748	000432	000000	HALT	:EXAMINE STACK TO FIND CAUSE
749	000434	000436	.+2	:UNEXPECTED TRAP TO THIS LOCATION
750	000436	000000	HALT	:EXAMINE STACK TO FIND CAUSE
751	000440	000442	.+2	:UNEXPECTED TRAP TO THIS LOCATION
752	000442	000000	HALT	:EXAMINE STACK TO FIND CAUSE
753	000444	000446	.+2	:UNEXPECTED TRAP TO THIS LOCATION
754	000446	000000	HALT	:EXAMINE STACK TO FIND CAUSE
755	000450	000452	.+2	:UNEXPECTED TRAP TO THIS LOCATION
756	000452	000000	HALT	:EXAMINE STACK TO FIND CAUSE
757	000454	000456	.+2	:UNEXPECTED TRAP TO THIS LOCATION
758	000456	000000	HALT	:EXAMINE STACK TO FIND CAUSE
759	000460	000462	.+2	:UNEXPECTED TRAP TO THIS LOCATION
760	000462	000000	HALT	:EXAMINE STACK TO FIND CAUSE
761	000464	000466	.+2	:UNEXPECTED TRAP TO THIS LOCATION
762	000466	000000	HALT	:EXAMINE STACK TO FIND CAUSE
763	000470	000472	.+2	:UNEXPECTED TRAP TO THIS LOCATION
764	000472	000000	HALT	:EXAMINE STACK TO FIND CAUSE
765	000474	000476	.+2	:UNEXPECTED TRAP TO THIS LOCATION
766	000476	000000	HALT	:EXAMINE STACK TO FIND CAUSE
767	000500	000502	.+2	:UNEXPECTED TRAP TO THIS LOCATION
768	000502	000000	HALT	:EXAMINE STACK TO FIND CAUSE
769	000504	000506	.+2	:UNEXPECTED TRAP TO THIS LOCATION
770	000506	000000	HALT	:EXAMINE STACK TO FIND CAUSE
771	000510	000512	.+2	:UNEXPECTED TRAP TO THIS LOCATION
772	000512	000000	HALT	:EXAMINE STACK TO FIND CAUSE

773	000514	000516	.+2	:UNEXPECTED TRAP TO THIS LOCATION
774	000516	000000	HALT	:EXAMINE STACK TO FIND CAUSE
775	000520	000522	.+2	:UNEXPECTED TRAP TO THIS LOCATION
776	000522	000000	HALT	:EXAMINE STACK TO FIND CAUSE
777	000524	000526	.+2	:UNEXPECTED TRAP TO THIS LOCATION
778	000526	000000	HALT	:EXAMINE STACK TO FIND CAUSE
779	000530	000532	.+2	:UNEXPECTED TRAP TO THIS LOCATION
780	000532	000000	HALT	:EXAMINE STACK TO FIND CAUSE
781	000534	000536	.+2	:UNEXPECTED TRAP TO THIS LOCATION
782	000536	000000	HALT	:EXAMINE STACK TO FIND CAUSE
783	000540	000542	.+2	:UNEXPECTED TRAP TO THIS LOCATION
784	000542	000000	HALT	:EXAMINE STACK TO FIND CAUSE
785	000544	000546	.+2	:UNEXPECTED TRAP TO THIS LOCATION
786	000546	000000	HALT	:EXAMINE STACK TO FIND CAUSE
787	000550	000552	.+2	:UNEXPECTED TRAP TO THIS LOCATION
788	000552	000000	HALT	:EXAMINE STACK TO FIND CAUSE
789	000554	000556	.+2	:UNEXPECTED TRAP TO THIS LOCATION
790	000556	000000	HALT	:EXAMINE STACK TO FIND CAUSE
791	000560	000562	.+2	:UNEXPECTED TRAP TO THIS LOCATION
792	000562	000000	HALT	:EXAMINE STACK TO FIND CAUSE
793	000564	000566	.+2	:UNEXPECTED TRAP TO THIS LOCATION
794	000566	000000	HALT	:EXAMINE STACK TO FIND CAUSE
795	000570	000572	.+2	:UNEXPECTED TRAP TO THIS LOCATION
796	000572	000000	HALT	:EXAMINE STACK TO FIND CAUSE
797	000574	000576	.+2	:UNEXPECTED TRAP TO THIS LOCATION
798	000576	000000	HALT	:EXAMINE STACK TO FIND CAUSE
799	000600	000602	.+2	:UNEXPECTED TRAP TO THIS LOCATION
800	000602	000000	HALT	:EXAMINE STACK TO FIND CAUSE
801	000604	000606	.+2	:UNEXPECTED TRAP TO THIS LOCATION
802	000606	000000	HALT	:EXAMINE STACK TO FIND CAUSE
803	000610	000612	.+2	:UNEXPECTED TRAP TO THIS LOCATION
804	000612	000000	HALT	:EXAMINE STACK TO FIND CAUSE
805	000614	000616	.+2	:UNEXPECTED TRAP TO THIS LOCATION
806	000616	000000	HALT	:EXAMINE STACK TO FIND CAUSE
807	000620	000622	.+2	:UNEXPECTED TRAP TO THIS LOCATION
808	000622	000000	HALT	:EXAMINE STACK TO FIND CAUSE
809	000624	000626	.+2	:UNEXPECTED TRAP TO THIS LOCATION
810	000626	000000	HALT	:EXAMINE STACK TO FIND CAUSE
811	000630	000632	.+2	:UNEXPECTED TRAP TO THIS LOCATION
812	000632	000000	HALT	:EXAMINE STACK TO FIND CAUSE
813	000634	000636	.+2	:UNEXPECTED TRAP TO THIS LOCATION
814	000636	000000	HALT	:EXAMINE STACK TO FIND CAUSE
815	000640	000642	.+2	:UNEXPECTED TRAP TO THIS LOCATION
816	000642	000000	HALT	:EXAMINE STACK TO FIND CAUSE
817	000644	000646	.+2	:UNEXPECTED TRAP TO THIS LOCATION
818	000646	000000	HALT	:EXAMINE STACK TO FIND CAUSE
819	000650	000652	.+2	:UNEXPECTED TRAP TO THIS LOCATION
820	000652	000000	HALT	:EXAMINE STACK TO FIND CAUSE
821	000654	000656	.+2	:UNEXPECTED TRAP TO THIS LOCATION
822	000656	000000	HALT	:EXAMINE STACK TO FIND CAUSE
823	000660	000662	.+2	:UNEXPECTED TRAP TO THIS LOCATION
824	000662	000000	HALT	:EXAMINE STACK TO FIND CAUSE
825	000664	000666	.+2	:UNEXPECTED TRAP TO THIS LOCATION
826	000666	000000	HALT	:EXAMINE STACK TO FIND CAUSE
827	000670	000672	.+2	:UNEXPECTED TRAP TO THIS LOCATION
828	000672	000000	HALT	:EXAMINE STACK TO FIND CAUSE

829	000674	000676	.+2	:UNEXPECTED TRAP TO THIS LOCATION
830	000676	000000	HALT	:EXAMINE STACK TO FIND CAUSE
831	000700	000702	.+2	:UNEXPECTED TRAP TO THIS LOCATION
832	000702	000000	HALT	:EXAMINE STACK TO FIND CAUSE
833	000704	000706	.+2	:UNEXPECTED TRAP TO THIS LOCATION
834	000706	000000	HALT	:EXAMINE STACK TO FIND CAUSE
835	000710	000712	.+2	:UNEXPECTED TRAP TO THIS LOCATION
836	000712	000000	HALT	:EXAMINE STACK TO FIND CAUSE
837	000714	000716	.+2	:UNEXPECTED TRAP TO THIS LOCATION
838	000716	000000	HALT	:EXAMINE STACK TO FIND CAUSE
839	000720	000722	.+2	:UNEXPECTED TRAP TO THIS LOCATION
840	000722	000000	HALT	:EXAMINE STACK TO FIND CAUSE
841	000724	000726	.+2	:UNEXPECTED TRAP TO THIS LOCATION
842	000726	000000	HALT	:EXAMINE STACK TO FIND CAUSE
843	000730	000732	.+2	:UNEXPECTED TRAP TO THIS LOCATION
844	000732	000000	HALT	:EXAMINE STACK TO FIND CAUSE
845	000734	000736	.+2	:UNEXPECTED TRAP TO THIS LOCATION
846	000736	000000	HALT	:EXAMINE STACK TO FIND CAUSE
847	000740	000742	.+2	:UNEXPECTED TRAP TO THIS LOCATION
848	000742	000000	HALT	:EXAMINE STACK TO FIND CAUSE
849	000744	000746	.+2	:UNEXPECTED TRAP TO THIS LOCATION
850	000746	000000	HALT	:EXAMINE STACK TO FIND CAUSE
851	000750	000752	.+2	:UNEXPECTED TRAP TO THIS LOCATION
852	000752	000000	HALT	:EXAMINE STACK TO FIND CAUSE
853	000754	000756	.+2	:UNEXPECTED TRAP TO THIS LOCATION
854	000756	000000	HALT	:EXAMINE STACK TO FIND CAUSE
855	000750	000762	.+2	:UNEXPECTED TRAP TO THIS LOCATION
856	000762	000000	HALT	:EXAMINE STACK TO FIND CAUSE
857	000764	000766	.+2	:UNEXPECTED TRAP TO THIS LOCATION
858	000766	000000	HALT	:EXAMINE STACK TO FIND CAUSE
859	000770	000772	.+2	:UNEXPECTED TRAP TO THIS LOCATION
860	000772	000000	HALT	:EXAMINE STACK TO FIND CAUSE
861	000774	000776	.+2	:UNEXPECTED TRAP TO THIS LOCATION
862	000776	000000	HALT	:EXAMINE STACK TO FIND CAUSE

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863                                     :STANDARD INTERUPT VECTORS
864
865
866                                     . =24
867 000024 015460 PFAIL ;POWER FAIL HANDLER
868 000026 000340 340 ;SERVICE AT LEVEL 7
869 000030 014240 ERRORS ;ERROR HANDLER
870 000032 000340 340 ;SERVICE AT LEVEL 7
871 000034 014442 TRPSRV ;GENERAL HANDLER DISPATCH SERVICE
872 000036 000340 340 ;SERVICE AT LEVEL 7
873
874 000200 000167 000574 . =200 JMP START ;GO TO START OF PROGRAM
875
876
877
878                                     :DEFINITIONS FOR TRAP SUBROUTINE CALLS
879                                     :POINTERS TO SUBROUTINES CAN BE FOUND STARTING
880                                     :AT LOCATION "TRPTAB"
881
882 104400 SCOPE=TRAP+Y ;SCOPE LOOP AND ITERATION HANDLER
883 104401 TYPE=TRAP+Y ;TELETYPE OUTPUT ROUTINE
884 104402 OCTASC=TRAP+Y ;OCTAL TO ASCII CONVERSION
885 104403 INSTR=TRAP+Y ;INPUT ASCII STRING
886 104404 INSTER=TRAP+Y ;STRING INPUT ERROR
887 104405 PARAM=TRAP+Y ;CONVERT STRING TO OCTAL, CHECK LIMITS
888 104406 SAVOSP=TRAP+Y ;SAVE R0-R5, PC
889 104407 RESDS=TRAP+Y ;RESTORE R0-R5
890 104410 SCOPE1=TRAP+Y ;CHECK FOR FREEZE ON CURRENT DATA
891
892 000046 . =46 LOGICAL
893 000052 . =52
894 000052 040000 40000

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001000      . = 1000
:PROGRAM INITIALIZATION
:LOCK OUT INTERRUPTS
:SET UP PROCESSOR STACK
:SET UP POWER FAIL VECTOR
:CLEAR PROGRAM FLAGS AND COUNTS
:TYPE TITLE MESSAGE
:DETERMINE MEMORY SIZE

001000 012767 000340 176770 START: MOV #340,PS      :LOCK OUT INTERRUPTS
001006 012706 017102      MOV #STACK,SP    :SET UP PROCESSOR STACK
001012 012737 015460 000024 MOV #PFAIL,2#24  :SET UP POWER FAIL TRAP
001020 005067 014426      CLR STFLG       :CLEAR TEST START FLAG
001024 005067 014362      CLR PASCNT      :CLEAR PASS COUNT
001030 005067 014360      CLR ERRCNT      :CLEAR ERROR COUNT
001034 005067 014350      CLR ERRFLG      :CLEAR ERROR FLAG
001040 005067 014344      CLR ERRFLG      :CLEAR LAST ERROR PC
001044 104401 015624      TYPE MTITLE      :TYPE TITLE MESSAGE
001050 005767 014374      TST INIFLG      :CHECK INITIALIZATION FLAG
001054 001021      BNE VEC1      :IF NOT 0, CHECK SWITCHES
:FOR REINITIALIZATION

001056 005000      CLR R0              :SET UP TIME OUT RETURN
001060 012737 001072 000004 MOV #25,2#4      :WILL TRAP WHEN NO MEMORY
15: TST (R0)+      :LOCATION RESPONDED, CONTINUE
920 001070 000776      BR 15              :R0 CONTAINS ADDRESS OF
921 001072 010067 014360 25: MOV R0,HCORE      :NON EXISTANT MEMORY
922 001076 162767 000002 014352 SUB #2,HCORE      :RESTORE TRAPCATCHER
923 001104 012737 000006 000004 MOV #6,2#4

925 001112 005767 014332      TST INIFLG      :IF INITIALIZE FLAG=0
926 001116 001404      BEQ VEC2      :GET VECTOR AND CSR ADDRESS
927 001120 032767 000001 176442 VEC1: BIT #SW00,SWR   :IF SW00=1, GET NEW VECTOR
928 001126 001475      BEG BEGIN      :AND CSR
929 001130 012701 000300      VEC2: MOV #300,R1
930 001134 012702 000302      MOV #302,R2
931 001140 012703 000004      MOV #4,R3
932 001144 010211      15: MOV R2,(R1)      :RESTORE TRAPCATCHER
933 001146 005012      CLR (R2)      :IN FLOATING VECTOR AREA
934 001150 060301      ADD R3,R1
935 001152 060302      ADD R3,R2
936 001154 020127 001000      CMP R1,#1000
937 001160 001371      BNE 15
938 001162 104403      INSTR          :INPUT ADDRESS OF DEVICE VECTOR
939 001164 015703      MVECTOR       :MESSAGE "VECTOR ADDRESS--"
940 001166 104405      LDRM          :CONVERT STRING TO OCTAL
941 001170 000300      300          :LOW LIMIT
942 001172 000770      770          :HIGH LIMIT
943 001174 015400      DHRVEC       :LOCATIONS TO BE FILLED
944 001176      003      .BYTE 3      :NUMBER OF LOCATIONS
945 001177      004      .BYTE 4      :LSB MASK
946 001200 104403      INSTR          :INPUT ADDRESS OF DEVICE CSR
947 001202 015725      MREGADR      :MESSAGE "CONTROL REGISTER ADDRESS--"
948 001204 104405      PARAM       :CONVERT STRING TO OCTAL
949 001206 000000      0          :LOW LIMIT
950 001210 177776      177776      :HIGH LIMIT

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951	001212	015356				DHSCR			:LOCATIONS TO BE FILLED
952	001214	007				7			:NUMBER OF LOCATIONS
953	001215	010			.BYTE	10			:LSB MASK
954	001216	016767	014152	014152	.BYTE	MOV	DHSSR,DHSLR		:SET UP ADDRESS OF SILO
955	001224	005267	014146			INC	DHSLR		:STATUS REGISTER HIGH BYTE
956	001230	005767	014214			TST	INIFLG		:IF INITIALIZATION FLAG
957	001234	001002				BNE	BEGIN		:IS CLEARED
958	001236	005167	014206			COM	INIFLG		:SET IT
959									
960									:PROGRAM START
961									:CHECK FOR PROGRAM START AT SELECTED ADDRESS
962									
963	001242	012767	000340	176526	BEGIN:	MOV	#340,PS		:LOCK OUT INTERRUPTS
964	001250	012706	017102			MOV	#STACK,SP		:SET UP PROCESSOR STACK
965	001254	032767	000002	176306		BIT	#SW01,SWR		:IF SW01=1
966	001262	001410				BEQ	1\$:GET PC FOR PROGRAM START
967	001264	104403				INSTR			:GET PC
968	001266	016071				MTSTPC			:MESSAGE "TEST PC"
969	001270	104405				PARAM			:CONVERT STRING TO OCTAL
970	001272	000000				0			
971	001274	017500				17500			
972	001276	000207				RETURN			
973	001300	001			.BYTE	1			
974	001301	001			.BYTE	1			
975	001302	000410				BR	2\$		
976	001304	012767	001334	014104	1\$:	MOV	#T1,RETURN		:NORMAL START, TEST 1
977	001312	005767	014134			TST	STFLG		:IF LOOPING, BYPASS TIMEOUT
978	001316	001004				BNE	3\$		
979	001320	005167	014126			COM	STFLG		
980	001324	104401	016065		2\$:	TYPE	MR		:TYPE "R" TO INDICATE START
981	001330	000177	014062		3\$:	JMP	2RETURN		:START TESTING

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982
983
984
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986
987 001334 012767 000340 175434 T1:  MOV    #340,PS           ;DISABLE ALL INTERRUPTS
988 001342 012767 004000 014054      MOV    #4000,ICOUNT      ;SET UP FOR 4000 ITERATIONS
989 001350 012767 001470 014042      MOV    #3$,ESCAPE       ;SET UP TO ESCAPE TO NEXT TEST
990 001356 012777 004000 013772      MOV    #BIT11,ADHSCR    ;MASTER CLEAR INTERFACE
991 001364 012777 001440 014006      MOV    #1$,ADHRVEC     ;SET UP FOR POSSIBLE
992                                     ;RECEIVER INTERRUPT
993 001372 012777 000340 014002      MOV    #340,ADHRLVL    ;
994 001400 012777 001454 013776      MOV    #2$,ADHTVEC     ;SET UP FOR POSSIBLE
995                                     ;TRANSMITTER INTERRUPT
996 001406 012777 000340 013772      MOV    #340,ADHTLVL    ;
997 001414 012777 000100 013734      MOV    #BIT6,ADHSCR    ;SET CHARACTER AVAILABLE
998                                     ;INTERRUPT ENABLE
999 001422 005067 175350                CLR    PS              ;ALLOW INTERRUPTS
1000 001426 000240                        NOP                    ;WINDOW FOR INTERRUPTS
1001 001430 012767 000340 176340      MOV    #340,PS         ;NO INTERRUPT OCCURED
1002 001436 000414                        BR     3$              ;CONTINUE
1003 001440 017705 013712              1$:  MOV    ADHSCR,R5     ;GET CONTENTS OF SYSTEM CONTROL REGISTER
1004 001444 104000                        HLT    0               ;UNEXPECTED INTERRUPT
1005 001446 012716 001470              MOV    #3$, (SP)      ;SET UP TO
1006 001452 000002                        RTI                    ;RETURN FROM INTERRUPT
1007 001454 017705 013676              2$:  MOV    ADHSCR,R5     ;GET CONTENTS OF SYSTEM CONTROL REGISTER
1008 001460 104000                        HLT    0               ;UNEXPECTED INTERRUPT
1009 001462 012716 001470              MOV    #3$, (SP)      ;SET UP TO
1010 001466 000002                        RTI                    ;RETURN FROM INTERRUPT
1011 001470 016777 013706 013702  3$:  MOV    DHRLVL,ADHRVEC  ;RESTORE TRAPCATCHER
1012 001476 005077 013700              CLR    ADHRLVL
1013 001502 016777 013700 013674      MOV    ADHTLVL,ADHTVEC
1014 001510 005077 013672              CLR    ADHTLVL
1015 001514 104400                        SCOPE                  ;CHECK FOR ITERATIONS, LOOP
1016
1017
1018
1019
1020
1021 001516 012767 000340 176252 T2:  MOV    #340,PS           ;DISABLE ALL INTERRUPTS
1022 001524 012767 004000 013672      MOV    #4000,ICOUNT      ;SET UP FOR 4000 ITERATIONS
1023 001532 012767 001652 013660      MOV    #3$,ESCAPE       ;SET UP TO ESCAPE TO NEXT TEST
1024 001540 012777 004000 013610      MOV    #BIT11,ADHSCR    ;MASTER CLEAR INTERFACE
1025 001546 012777 001622 013624      MOV    #1$,ADHRVEC     ;SET UP FOR POSSIBLE
1026                                     ;RECEIVER INTERRUPT
1027 001554 012777 000340 013620      MOV    #340,ADHRLVL    ;
1028 001562 012777 001636 013614      MOV    #2$,ADHTVEC     ;SET UP FOR POSSIBLE
1029                                     ;TRANSMITTER INTERRUPT
1030 001570 012777 000340 013610      MOV    #340,ADHTLVL    ;
1031 001576 012777 010000 013552      MOV    #BIT12,ADHSCR    ;SET SILO OVERFLOW
1032                                     ;INTERRUPT ENABLE
1033 001604 005067 176166                CLR    PS              ;ALLOW INTERRUPTS
1034 001610 000240                        NOP                    ;WINDOW FOR INTERRUPTS
1035 001612 012767 000340 176156      MOV    #340,PS         ;NO INTERRUPT OCCURED
1036 001620 000414                        BR     3$              ;CONTINUE
1037 001622 017705 013530              1$:  MOV    ADHSCR,R5     ;GET CONTENTS OF SYSTEM CONTROL REGISTER

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1038 001626 104000 HLT 0 ;UNEXPECTED INTERRUPT
1039 001630 012716 001652 MOV #3$, (SP) ;SET UP TO
1040 001634 000002 RTI ;RETURN FROM INTERRUPT
1041 001636 017705 013514 2$: MOV @DHSCR, R5 ;GET CONTENTS OF SYSTEM CONTROL REGISTER
1042 001642 104000 HLT 0 ;UNEXPECTED INTERRUPT
1043 001644 012716 001652 MOV #3$, (SP) ;SET UP TO
1044 001650 000002 RTI ;RETURN FROM INTERRUPT
1045 001652 016777 013524 013520 3$: MOV DHRLVL, @DHRVEC ;RESTORE TRAPCATCHER
1046 001660 005077 013516 CLR @DHRLVL
1047 001664 016777 013516 013512 MOV DHTLVL, @DHTVEC
1048 001672 005077 013510 CLR @DHTLVL
1049 001676 104400 SCOPE ;CHECK FOR ITERATIONS, LOOP
1050
1051 ;INTERRUPT LOGIC TEST
1052 ;SET TRANSMITTER DONE INTERRUPT ENABLE
1053 ;VERIFY THAT NO INTERRUPTS OCCUR
1054
1055 001700 012767 000340 176070 T3: MOV #340, PS ;DISABLE ALL INTERRUPTS
1056 001706 012767 004000 013510 MOV #4000, ICOUNT ;SET UP FOR 4000 ITERATIONS
1057 001714 012767 002034 013476 MOV #3$, ESCAPE ;SET UP TO ESCAPE TO NEXT TEST
1058 001722 012777 004000 013426 MOV #BIT11, @DHSCR ;MASTER CLEAR INTERFACE
1059 001730 012777 002004 013442 MOV #13, @DHRVEC ;SET UP FOR POSSIBLE
1060 ;RECEIVER INTERRUPT
1061 001736 012777 000340 013436 MOV #340, @DHRLVL
1062 001744 012777 002020 013432 MOV #2$, @DHTVEC ;SET UP FOR POSSIBLE
1063 ;TRANSMITTER INTERRUPT
1064 001752 012777 000340 013426 MOV #340, @DHTLVL
1065 001760 012777 020000 013370 MOV #BIT13, @DHSCR ;SET TRANSMITTER DONE
1066 ;INTERRUPT ENABLE
1067 001766 005067 176004 CLR PS ;ALLOW INTERRUPTS
1068 001772 000240 NOP ;WINDOW FOR INTERRUPTS
1069 001774 012767 000340 175774 MOV #340, PS ;NO INTERRUPT OCCURED
1070 002002 000414 BR 3$ ;CONTINUE
1071 002004 017705 013346 1$: MOV @DHSCR, R5 ;GET CONTENTS OF SYSTEM CONTROL REGISTER
1072 002010 104000 HLT 0 ;UNEXPECTED INTERRUPT
1073 002012 012716 002034 MOV #3$, (SP) ;SET UP TO
1074 002016 000002 RTI ;RETURN FROM INTERRUPT
1075 002020 017705 013332 2$: MOV @DHSCR, R5 ;GET CONTENTS OF SYSTEM CONTROL REGISTER
1076 002024 104000 HLT 0 ;UNEXPECTED INTERRUPT
1077 002026 012716 002034 MOV #3$, (SP) ;SET UP TO
1078 002032 000002 RTI ;RETURN FROM INTERRUPT
1079 002034 016777 013342 013336 3$: MOV DHRLVL, @DHRVEC ;RESTORE TRAPCATCHER
1080 002042 005077 013334 CLR @DHRLVL
1081 002046 016777 013334 013330 MOV DHTLVL, @DHTVEC
1082 002054 005077 013326 CLR @DHTLVL
1083 002060 104400 SCOPE ;CHECK FOR ITERATIONS, LOOP
1084
1085 ;INTERRUPT LOGIC TEST
1086 ;SET CHARACTER AVAILABLE INTERRUPT ENABLE
1087 ;SET CHARACTER AVAILABLE (MAINTENANCE MODE IS ENABLED)
1088 ;VERIFY THAT AN INTERRUPT OCCURS
1089
1090 002062 012767 000340 175706 T4: MOV #340, PS ;DISABLE ALL INTERRUPTS
1091 002070 012767 004000 013326 MOV #4000, ICOUNT ;SET UP FOR 4000 ITERATIONS
1092 002076 012767 002226 013314 MOV #3$, ESCAPE ;SET UP TO ESCAPE TO NEXT TEST
1093 002104 012777 004000 013244 MOV #BIT11, @DHSCR ;MASTER CLEAR INTERFACE

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1094 002112 012777 002204 013260      MOV      #1$,ADHRVEC      ;SET UP FOR RECEIVER INTERRUPT
1095 002120 012777 000340 013254      MOV      #3$,ADHRLVL
1096 002126 012777 002212 013250      MOV      #2$,ADHTVEC      ;SET UP FOR TRANSMITTER INTERRUPT
1097 002134 012777 000340 013244      MOV      #340,ADHTLVL
1098 002142 012777 001000 013206      MOV      #BIT09,ADHSCR      ;SET MAINTENANCE MODE
1099 002150 052777 000100 013200      BIS      #BIT06,ADHSCR      ;SET CHARACTER AVAILABLE
1100                                     ;INTERRUPT ENABLE
1101 002156 052777 000200 013172      BIS      #BIT07,ADHSCR      ;FORCE INTERRUPT BY
1102                                     ;SETTING CHARACTER AVAILABLE
1103 002164 005067 175606      CLR      PS                ;ALLOW INTERRUPTS
1104 002170 000240                                     NOP                        ;WINDOW FOR INTERRUPTS
1105 002172 012767 000340 175576      MOV      #340,PS          ;NO INTERRUPT OCCURED
1106 002200 104001                                     HLT                        ;WITH CHARACTER AVAILABLE INTERRUPT
1107                                     ;ENABLE AND CHARACTER AVAILABLE SET
1108                                     ;ERROR
1109 002202 000411      BR      3$
1110 002204 012716 002226      1$: MOV      #3$, (SP)      ;SET UP TO RETURN
1111 002210 000002      RTI                                     ;FROM VALID INTERRUPT
1112 002212 017705 013140      2$: MOV      ADHSCR,R5      ;GET CONTENTS OF SYSTEM CONTROL REGISTER
1113 002216 104000      HLT      0                ;UNEXPECTED INTERRUPT
1114 002220 012716 002226      MOV      #3$, (SP)      ;SET UP TO RETURN
1115 002224 000002      RTI                                     ;FROM UNEXPECTED INTERRUPT
1116 002226 016777 013150 013144      3$: MOV      DHRLVL,ADHRVEC ;RESTORE TRAPCATCHER
1117 002234 005077 013142      CLR      ADHRLVL
1118 002240 016777 013142 013136      MOV      DHTLVL,ADHTVEC
1119 002246 005077 013134      CLR      ADHTLVL
1120 002252 104400      SCOPE
1121
1122                                     ; INTERRUPT LOGIC TEST
1123                                     ; SET SILO OVERFLOW INTERRUPT ENABLE
1124                                     ; SET SILO OVERFLOW (MAINTENANCE MODE IS ENABLED)
1125                                     ; VERIFY THAT AN INTERRUPT OCCURS
1126
1127 002254 012767 000340 175514      T5: MOV      #340,PS        ;DISABLE ALL INTERRUPTS
1128 002262 012767 004000 013134      MOV      #4000,ICOUNT     ;SET UP FOR 4000 ITERATIONS
1129 002270 012767 002420 013122      MOV      #3$,ESCAPE      ;SET UP TO ESCAPE TO NEXT TEST
1130 002276 012777 004000 013052      MOV      #BIT11,ADHSCR    ;MASTER CLEAR INTERFACE
1131 002304 012777 002376 013066      MOV      #1$,ADHRVEC      ;SET UP FOR RECEIVER INTERRUPT
1132 002312 012777 000340 013062      MOV      #340,ADHRLVL
1133 002320 012777 002404 013056      MOV      #2$,ADHTVEC      ;SET UP FOR TRANSMITTER INTERRUPT
1134 002326 012777 000340 013052      MOV      #340,ADHTLVL
1135 002334 012777 001000 013014      MOV      #BIT09,ADHSCR    ;SET MAINTENANCE MODE
1136 002342 052777 040000 013006      BIS      #BIT14,ADHSCR    ;SET SILO OVERFLOW
1137                                     ;INTERRUPT ENABLE
1138 002350 052777 010000 013000      BIS      #BIT12,ADHSCR    ;FORCE INTERRUPT BY
1139                                     ;SETTING SILO OVERFLOW
1140 002356 005067 175414      CLR      PS                ;ALLOW INTERRUPTS
1141 002362 000240                                     NOP                        ;WINDOW FOR INTERRUPTS
1142 002364 012767 000340 175404      MOV      #340,PS          ;NO INTERRUPT OCCURED
1143 002372 104001                                     HLT                        ;WITH SILO OVERFLOW INTERRUPT
1144                                     ;ENABLE AND SILO OVERFLOW SET
1145                                     ;ERROR
1146 002374 000411      BR      3$
1147 002376 012716 002420      1$: MOV      #3$, (SP)      ;SET UP TO RETURN
1148 002402 000002      RTI                                     ;FROM VALID INTERRUPT
1149 002404 017705 012746      2$: MOV      ADHSCR,R5      ;GET CONTENTS OF SYSTEM CONTROL REGISTER

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1150 002410 104000          HLT      0          ;UNEXPECTED INTERRUPT
1151 002412 012716 002420  MOV      #3$, (SP)      ;SET UP TO RETURN
1152 002416 000002          RTI          ;FROM UNEXPECTED INTERRUPT
1153 002420 016777 012756 012752 3$:  MOV      DHRLVL, @DHRVEC ;RESTORE TRAPCATCHER
1154 002426 005077 012750          CLR      @DHRLVL
1155 002432 016777 012750 012744  MOV      DHTLVL, @DHTVEC
1156 002440 005077 012742          CLR      @DHTLVL
1157 002444 104400          SCOPE
1158
1159          ; INTERRUPT LOGIC TEST
1160          ; SET TRANSMITTER INTERRUPT ENABLE
1161          ; SET NON EXISTATN MEMORY (MAINTENANCE MODE IS ENABLED)
1162          ; VERIFY THAT AN INTERRUPT OCCURS
1163
1164 002446 012767 000340 175322 T6:  MOV      #340, PS      ;DISABLE ALL INTERRUPTS
1165 002454 012767 004000 012742  MOV      #4000, ICOUNT ;SET UP FOR 4000 ITERATIONS
1166 002462 012767 002612 012730  MOV      #3$, ESCAPE   ;SET UP TO ESCAPE TO NEXT TEST
1167 002470 012777 004000 012660  MOV      #BIT11, @DHSCR ;MASTER CLEAR INTERFACE
1168 002476 012777 002576 012674  MOV      #2$, @DHRVEC  ;SET UP FOR RECEIVER INTERRUPT
1169 002504 012777 000340 012670  MOV      #340, @DHRLVL
1170 002512 012777 002570 012664  MOV      #1$, @DHTVEC  ;SET UP FOR TRANSMITTER INTERRUPT
1171 002520 012777 000340 012660  MOV      #340, @DHTLVL
1172 002526 012777 001000 012622  MOV      #BIT09, @DHSCR ;SET MAINTENANCE MODE
1173 002534 052777 020000 012614  BIS      #BIT13, @DHSCR ;SET TRANSMITTER
1174          ; INTERRUPT ENABLE
1175 002542 052777 002000 012606  BIS      #BIT10, @DHSCR ;FORCE INTERRUPT BY
1176          ; SETTING NON EXISTATN MEMORY
1177 002550 005067 175222          CLR      PS          ;ALLOW INTERRUPTS
1178 002554 000240          NOP          ;WINDOW FOR INTERRUPTS
1179 002556 012767 000340 175212  MOV      #340, PS      ;NO INTERRUPT OCCURED
1180 002564 104001          HLT      1          ;WITH TRANSMITTER INTERRUPT
1181          ; ENABLE AND NON EXISTATN MEMORY SET
1182          ; ERROR
1183 002566 000411          BR      3$
1184 002570 012716 002612          1$:  MOV      #3$, (SP)      ;SET UP TO RETURN
1185 002574 000002          RTI          ;FROM VALID INTERRUPT
1186 002576 017705 012554          2$:  MOV      @DHSCR, R5    ;GET CONTENTS OF SYSTEM CONTROL REGISTER
1187 002602 104000          HLT      0          ;UNEXPECTED INTERRUPT
1188 002604 012716 002612          MOV      #3$, (SP)      ;SET UP TO RETURN
1189 002610 000002          RTI          ;FROM UNEXPECTED INTERRUPT
1190 002612 016777 012564 012560 3$:  MOV      DHRLVL, @DHRVEC ;RESTORE TRAPCATCHER
1191 002620 005077 012556          CLR      @DHRLVL
1192 002624 016777 012556 012552  MOV      DHTLVL, @DHTVEC
1193 002632 005077 012550          CLR      @DHTLVL
1194 002636 104400          SCOPE
1195
1196          ; INTERRUPT LOGIC TEST
1197          ; SET TRANSMITTER DONE INTERRUPT ENABLE
1198          ; SET TRANSMITTER DONE (MAINTENANCE MODE IS ENABLED)
1199          ; VERIFY THAT AN INTERRUPT OCCURS
1200
1201 002640 012767 000340 175130 T7:  MOV      #340, PS      ;DISABLE ALL INTERRUPTS
1202 002646 012767 004000 012550  MOV      #4000, ICOUNT ;SET UP FOR 4000 ITERATIONS
1203 002654 012767 003004 012536  MOV      #3$, ESCAPE   ;SET UP TO ESCAPE TO NEXT TEST
1204 002662 012777 004000 012466  MOV      #BIT11, @DHSCR ;MASTER CLEAR INTERFACE
1205 002670 012777 002770 012502  MOV      #2$, @DHRVEC  ;SET UP FOR RECEIVER INTERRUPT
  
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003:63 005777 012204 35: TST 2D4BAR ;WAS BAR BIT CLEARED FOR LINE 0
003:64 001404 BEQ 45
003:66 005005 CLR R5 ;(R5)=EXPECTED DATA IN
;BUFFER ACTIVE REGISTER, 0
003:70 017704 012174 MOV 2DHBA,R4 ;(R4)=ACTUAL CONTENTS OF
;BUFFER ACTIVE REGISTER
003:72 104000 HLT 0 ;BUS ACTIVE BIT NOT CLEARED, ERROR
003:74 002777 000001 012120 45: CMP #1,2DHBA ;WAS BUS ADDRESS INCREMENTED
003:76 001405 BEQ 55
003:78 017704 012152 MOV 2DHBA,R4 ;(R4)=ACTUAL CONTENTS
;OF BUS ADDRESS MEMORY FOR
;LINE 0
003212 012705 000001 MOV #1,R5 ;(R5)=EXPECTED VALUE OF
;BUS ADDRESS MEMORY FOR
;LINE 0, 1
003216 104003 HLT 3 ;BUS ADDRESS NOT UPDATED
;CORRECTLY, ERROR
003220 005777 012142 55: TST 2DHBC ;DID BYTE COUNT DECREMENT TO 0
003224 001416 BEQ 65
003226 017704 012134 MOV 2DHBC,R4 ;(R4)=ACTUAL VALUE OF BYTE
;COUNT FOR LINE 0
003232 005005 CLR R5 ;(R5)=EXPECTED VALUE OF BYTE
;COUNT FOR LINE 0, 0
003234 104004 HLT 4 ;BYTE COUNT DID NOT DECREMENT TO 0, ERROR
003236 016777 012142 012134 MOV 2DHRLVL,2DHVEC ;RESTORE TRAPCATCHER
003238 005077 012132 CLR 2DHRLVL
003240 001677 012132 012126 MOV 2DHTVL,2DHTVEC
003242 005077 012124 CLR 2DHTLVL
003244 012700 017120 55: MOV #STACK,SP ;RESTORE STACK
003246 104100 SCOPE ;CHECK FOR ITERATIONS, LOOP

;NPR LOGIC TEST
;SET BYTE COUNT TO 1 FOR LINE 1
;SET BAR BIT FOR LINE 1
;DELAY FOR NPR
;VERIFY THAT BAR BIT FOR LINE 1 CLEARS
;VERIFY THAT TRANSMITTER DONE IS SET

003270 012767 000340 174500 T11: MOV #340,PS ;DISABLE ALL INTERRUPTS
003276 012767 000020 012120 MOV #20,ICOUNT ;SET UP FOR 20 ITERATIONS
003304 012767 003520 012105 MOV #65,ESCAPE ;SET UP TO ESCAPE TO NEXT TEST
003312 012777 004000 012036 MOV #BIT11,2DHSCR ;ISSUE MASTER CLEAR
003320 004767 011740 JSR PC,CLEAR ;CLEAR ALL BUS ADDRESS
;AND BYTE COUNT MEMORY LOCATIONS
003324 012777 003406 012052 MOV #25,2DHTVEC ;SET UP TRANSMITTER
003332 012777 000340 012046 MOV #340,2DHTLVL ;INTERRUPT VECTOR
003340 012777 000001 012010 MOV #1,2DHSCR ;SELECT LINE 1
003346 012777 177777 0120.2 MOV #-1,2DHBC ;SET BYTE COUNT TO 1
003354 012700 001000 MOV #1000,R0
003360 012777 000002 012002 MOV #2,2DHBA ;SET BAR BIT FOR
;LINE 1
003366 052777 020000 011762 BIS #BIT13,2DHSCR ;SET TRANSMITTER INTERRUPT ENABLE
003374 005067 174376 CLR PS ;ALLOW INTERRUPTS
003400 005300 15: DEC R0 ;DELAY FOR NPR
003402 001376 BNE 15
003404 104001 HLT 1 ;NO INTERRUPT OCCURED, ERROR

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1330 003406 005777 011744 25: TST 2DHSCR ;VERIFY THAT TRANSMITTER
1331 ;DONE IS SET
1332 003412 100401 BMI 35
1333 003414 104002 HLT 2 ;TRANSMITTER DONE NOT SET, ERROR
1334 003416 005777 011746 35: TST 2DHBAR ;WAS BAR BIT CLEARED FOR LINE 1
1335 003422 001404 BEQ 45
1336 003424 005005 CLR R5 ;(R5)=EXPECTED DATA IN
1337 ;BUFFER ACTIVE REGISTER, 0
1338 003426 011704 011736 MOV 2DHBAR,R4 ;(R4)=ACTUAL CONTENTS OF
1339 ;BUFFER ACTIVE REGISTER
1340 003432 104000 HLT 0 ;BUS ACTIVE BIT NOT CLEARED, ERROR
1341 003434 022777 000001 011722 45: CMP #1,2DHBA ;WAS BUS ADDRESS INCREMENTED
1342 003442 001405 BEQ 55
1343 003444 011704 011714 MOV 2DHBA,R4 ;(R4)=ACTUAL CONTENTS
1344 ;OF BUS ADDRESS MEMORY FOR
1345 ;LINE 1
1346 003450 012705 000001 MOV #1,R5 ;(R5)=EXPECTED VALUE OF
1347 ;BUS ADDRESS MEMORY FOR
1348 ;LINE 1
1349 003454 104003 HLT 3 ;BUS ADDRESS NOT UPDATED
1350 ;CORRECTLY, ERROR
1351 003456 005777 011704 55: TST 2DHBC ;DID BYTE COUNT DECREMENT TO 0
1352 003462 001416 BEQ 65
1353 003464 011704 011676 MOV 2DHBC,R4 ;(R4)=ACTUAL VALUE OF BYTE
1354 ;COUNT FOR LINE 1
1355 003470 005005 CLR R5 ;(R5)=EXPECTED VALUE OF BYTE
1356 ;COUNT FOR LINE 1, 0
1357 003472 104004 HLT 4 ;BYTE COUNT DID NOT DECREMENT TO 0, ERROR
1358 003474 016777 011702 011676 MOV DHRVLV,2DHRVEC ;RESTORE TRAPCATCHER
1359 003502 005077 011674 CLR 2DHRVLV
1360 003506 016777 011674 011670 MOV DHTLVL,2DHTVEC
1361 003514 005077 011656 CLR 2DHTLVL
1362 003520 012706 011702 65: MOV #STACK,SP ;RESTORE STACK
1363 003524 104000 SCOPE ;CHECK FOR ITERATIONS, LOOP
1364 ;NPR LOGIC TEST
1365 ;SET BYTE COUNT TO 1 FOR LINE 2
1366 ;SET BAR BIT FOR LINE 2
1367 ;DELAY FOR NPR
1368 ;VERIFY THAT BAR BIT FOR LINE 2 CLEARS
1369 ;VERIFY THAT TRANSMITTER DONE IS SET
1370 003526 012767 000340 174242 712: MOV #340,FS ;DISABLE ALL INTERRUPTS
1371 003534 012767 000020 011662 MOV #20,ICOUNT ;SET UP FOR 20 ITERATIONS
1372 003542 012767 003756 011650 MOV #65,ESCAPE ;SET UP TO ESCAPE TO NEXT TEST
1373 003550 012777 004000 011600 MOV #BIT11,2DHSCR ;ISSUE MASTER CLEAR
1374 003556 004767 011502 JSR PC,CLEAR ;CLEAR ALL BUS ADDRESS
1375 ;AND BYTE COUNT MEMORY LOCATIONS
1376 003562 012777 003644 011614 MOV #25,2DHTVEC ;SET UP TRANSMITTER
1377 003570 012777 000340 011610 MOV #340,2DHTLVL ;INTERRUPT VECTOR
1378 003576 012777 000002 011552 MOV #2,2DHSCR ;SELECT LINE 2
1379 003604 012777 177777 011554 MOV #-1,2DHBC ;SET BYTE COUNT TO 1
1380 003612 012700 001000 MOV #1000,R0
1381 003616 012777 000004 011544 MOV #4,2DHBAR ;SET BAR BIT FOR
1382 ;LINE 2
1383 003624 052777 020000 011524 BIS #BIT13,2DHSCR ;SET TRANSMITTER INTERRUPT ENABLE

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E03

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13:01 003632 005067 174140          CLR      PS          ;ALLOW INTERRUPTS
13:02 003636 005300          DEC      RC          ;DELAY FOR NPR
13:03 003640 001376          BNE     1$          .
13:04 003642 104001          HLT     1           ;NO INTERRUPT OCCURED, ERROR
13:05 003644 005777 011506          TST     @DHSCR     ;VERIFY THAT TRANSMITTER
13:06 003650 100401          SMI     3$          ;DONE IS SET
13:07 003652 104002          HLT     2           ;TRANSMITTER DONE NOT SET, EPROR
13:08 003654 005777 011510          TST     @CHBAR     ;WAS BAR BIT CLEARED FOR LINE 2
13:09 003660 001404          BEQ     4$          .
13:10 003662 005005          CLR     R5          ;(R5)=EXPECTED DATA IN
13:11 003664 017704 011500          MOV     @DHBAR,R4  ;BUFFER ACTIVE REGISTER, 0
13:12 003670 104000          HLT     0           ;(R4)=ACTUAL CONTENTS OF
13:13 003672 022777 000001 011464 4$:      CMP     #1,@DHBA   ;BUFFER ACTIVE REGISTER
13:14 003700 001405          BEQ     5$          ;BUS ACTIVE BIT NOT CLEARED, ERROR
13:15 003702 017704 011456          MOV     @DHBA,R4   ;WAS BUS ADDRESS INCREMENTED
13:16 003706 012705 000001          MOV     #1,R5      ;(R4)=ACTUAL CONTENTS
13:17 003712 104003          HLT     3           ;OF BUS ADDRESS MEMORY FOR
13:18 003714 005777 011446          TST     @DHBC      ;LINE 2
13:19 003720 001416          BEQ     6$          ;(R5)=EXPECTED VALUE OF
13:20 003722 017704 011440          MOV     @DHBC,R4   ;BUS ADDRESS MEMORY FOR
13:21 003726 005005          CLR     R5          ;LINE 2, 1
13:22 003730 104004          HLT     4           ;BUS ADDRESS NOT UPDATED
13:23 003732 016777 011444 011440          MOV     @DHRLVL,@DHAVEC ;CORRECTLY, ERROR
13:24 003740 005077 011436          CLR     @DHRLVL    ;DID BYTE COUNT DECREMENT TO 0
13:25 003744 016777 011436 011432          MOV     @DHTLVL,@DHTVEC ;
13:26 003752 005077 011430          CLR     @DHTLVL    ;
13:27 003756 012706 017102          MOV     #STACK,SP  ;(R4)=ACTUAL VALUE OF BYTE
13:28 003762 104400          SCOPE             ;COUNT FOR LINE 2
13:29 003764 012767 000340 174004 T13:      MOV     #340,PS    ;(R5)=EXPECTED VALUE OF BYTE
13:30 003772 012767 000020 011424          MOV     #20,COUNT  ;COUNT FOR LINE 2, 0
13:31 004000 012767 004214 011412          MOV     #65,ESCAPE ;BYTE COUNT DID NOT DECREMENT TO 0, ERROR
13:32 004006 012777 004000 011342          MOV     #BIT11,@DHSCR ;RESTORE TRAPCATCHER
13:33 004014 004767 011244          JSR     PC,CLEAR   ;
13:34 004020 012777 004102 011356          MOV     #25,@DHTVEC ;RESTORE STACK
13:35 004026 012777 000340 011352          MOV     #340,@DHTLVL ;CHECK FOR ITERATIONS, LOOP
13:36 004034 012777 000003 011314          MOV     #3,@DHSCR  ;
13:37 004042 012777 177777 011316          MOV     #-1,@DHBC  ;NPR LOGIC TEST
13:38 004044 012777 177777 011316          MOV     #-1,@DHBC  ;SET BYTE COUNT TO 1 FOR LINE 3
13:39 004046 012777 177777 011316          MOV     #-1,@DHBC  ;SET BAR BIT FOR LINE 3
13:40 004048 012777 177777 011316          MOV     #-1,@DHBC  ;DELAY FOR NPR
13:41 004050 012777 177777 011316          MOV     #-1,@DHBC  ;VERIFY THAT BAR BIT FOR LINE 3 CLEARS
13:42 004052 012777 177777 011316          MOV     #-1,@DHBC  ;VERIFY THAT TRANSMITTER DONE IS SET
13:43 004054 012777 177777 011316          MOV     #-1,@DHBC  ;
13:44 004056 012777 177777 011316          MOV     #-1,@DHBC  ;DISABLE ALL INTERRUPTS
13:45 004058 012777 177777 011316          MOV     #-1,@DHBC  ;SET UP FOR 20 ITERATIONS
13:46 004060 012777 177777 011316          MOV     #-1,@DHBC  ;SET UP TO ESCAPE TO NEXT TEST
13:47 004062 012777 177777 011316          MOV     #-1,@DHBC  ;ISSUE MASTER CLEAR
13:48 004064 012777 177777 011316          MOV     #-1,@DHBC  ;CLEAR ALL BUS ADDRESS
13:49 004066 012777 177777 011316          MOV     #-1,@DHBC  ;AND BYTE COUNT MEMORY LOCATIONS
13:50 004068 012777 177777 011316          MOV     #-1,@DHBC  ;SET UP TRANSMITTER
13:51 004070 012777 177777 011316          MOV     #-1,@DHBC  ;INTERRUPT VECTOR
13:52 004072 012777 177777 011316          MOV     #-1,@DHBC  ;SELECT LINE 3
13:53 004074 012777 177777 011316          MOV     #-1,@DHBC  ;SET BYTE COUNT TO 1

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1486 004256 012777 004340 011120      MOV      #2$,DHTVEC      ;SET UP TRANSMITTER
1487 004264 012777 000340 011114      MOV      #340,DHTLVL    ;INTERRUPT VECTOR
1488 004272 012777 000004 011056      MOV      #4,DHSCR       ;SELECT LINE 4
1489 004300 012777 177777 011060      MOV      #-1,DHBC       ;SET BYTE COUNT TO 1
1490 004306 012700 001000      MOV      #1000,R0
1491 004312 012777 000020 011050      MOV      #20,DHBAR      ;SET BAR BIT FOR
1492                                     ;LINE 4
1493 004320 052777 020000 011030      BIS      #BIT13,DHSCR    ;SET TRANSMITTER INTERRUPT ENABLE
1494 004326 005067 173444      CLR      PS              ;ALLOW INTERRUPTS
1495 004332 005300      1$:      DEC      R0              ;DELAY FOR NPR
1496 004334 001376      BNE     1$
1497 004336 104001      HLT     1$
1498 004340 005777 011012      2$:      TST     DHSCR          ;NO INTERRUPT OCCURED, ERROR
1499                                     ;VERIFY THAT TRANSMITTER
1500                                     ;DONE IS SET
1501 004344 100401      BMI     3$
1502 004346 104002      HLT     2$
1503 004350 005777 011014      3$:      TST     DHBAR          ;TRANSMITTER DONE NOT SET, ERROR
1504 004354 001404      BEQ     4$              ;WAS BAR BIT CLEARED FOR LINE 4
1505 004356 005005      CLR     R5
1506                                     ;(R5)=EXPECTED DATA IN
1507 004360 017704 011004      MOV     DHBAR,R4        ;BUFFER ACTIVE REGISTER, 0
1508                                     ;(R4)=ACTUAL CONTENTS OF
1509 004364 104000      HLT     0$              ;BUFFER ACTIVE REGISTER
1510 004366 022777 000001 010770      4$:      CMP     #1,DHBA        ;BUS ACTIVE BIT NOT CLEARED, ERROR
1511 004374 001405      BEQ     5$              ;WAS BUS ADDRESS INCREMENTED
1512 004376 017704 010762      MOV     DHBA,R4
1513                                     ;(R4)=ACTUAL CONTENTS
1514                                     ;OF BUS ADDRESS MEMORY FOR
1515 004402 012705 000001      MOV     #1,R5          ;LINE 4
1516                                     ;(R5)=EXPECTED VALUE OF
1517 004406 104003      HLT     3$              ;BUS ADDRESS MEMORY FOR
1518                                     ;LINE 4, 1
1519 004410 005777 010752      5$:      TST     DHBC          ;BUS ADDRESS NOT UPDATED
1520 004414 001416      BEQ     6$              ;CORRECTLY, ERROR
1521 004416 017704 010744      MOV     DHBC,R4        ;DID BYTE COUNT DECREMENT TO 0
1522                                     ;(R4)=ACTUAL VALUE OF BYTE
1523 004422 005005      CLR     R5              ;COUNT FOR LINE 4
1524                                     ;(R5)=EXPECTED VALUE OF BYTE
1525 004424 104004      HLT     4$              ;COUNT FOR LINE 4, 0
1526 004426 016777 010750 010744      MOV     DHRLVL,DHVEC    ;BYTE COUNT DID NOT DECREMENT TO 0, ERROR
1527 004434 005077 010742      CLR     DHRLVL          ;RESTORE TRAPCATCHER
1528 004440 016777 010742 010736      MOV     DHTLVL,DHTVEC
1529 004446 005077 010734      CLR     DHHTLVL
1530 004452 012706 017102      6$:      MOV     #STACK,SP      ;RESTORE STACK
1531 004456 104400      SCOPE    ;CHECK FOR ITERATIONS, LOOP
1532
1533      ;NPR LOGIC TEST
1534      ;SET BYTE COUNT TO 1 FOR LINE 5
1535      ;SET BAR BIT FOR LINE 5
1536      ;DELAY FOR NPR
1537      ;VERIFY THAT BAR BIT FOR LINE 5 CLEARS
1538      ;VERIFY THAT TRANSMITTER DONE IS SET
1539
1540 004460 012767 000340 173310      7$:      MOV     #340,PS        ;DISABLE ALL INTERRUPTS
1541 004466 012767 000020 010730      MOV     #20,ICOUNT     ;SET UP FOR 20 ITERATIONS

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H03

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1542	004474	012767	004710	010716	MOV	#6\$, ESCAPE	:SET UP TO ESCAPE TO NEXT TEST
1543	004502	012777	004000	010646	MOV	#BIT11, @DHSCR	:ISSUE MASTER CLEAR
1544	004510	004767	010550		JSR	PC.CLEAR	:CLEAR ALL BUS ADDRESS
1545							:AND BYTE COUNT MEMORY LOCATIONS
1546	004514	012777	004576	010662	MOV	#2\$, @DHTVEC	:SET UP TRANSMITTER
1547	004522	012777	000340	010656	MOV	#340, @DHTLVL	: INTERRUPT VECTOR
1548	004530	012777	000005	010620	MOV	#5, @DHSCR	:SELECT LINE 5
1549	004536	012777	177777	010622	MOV	#-1, @DHBC	:SET BYTE COUNT TO 1
1550	004544	012700	001000		MOV	#1000, R0	
1551	004550	012777	000040	010612	MOV	#40, @DHBAR	:SET BAR BIT FOR
1552							:LINE 5
1553	004556	052777	020000	010572	BIS	#BIT13, @DHSCR	:SET TRANSMITTER INTERRUPT ENABLE
1554	004554	005067	173206		CLR	PS	:ALLOW INTERRUPTS
1555	004570	005300			15:	DEC	R0
1556	004572	001376				BNE	1\$
1557	004574	104001				HLT	1
1558	004576	005777	010554		2\$:	TST	@DHSCR
1559							:NO INTERRUPT OCCURED, ERROR
1560	004602	100401					:VERIFY THAT TRANSMITTER
1561	004604	104002					:DONE IS SET
1562	004606	005777	010556		3\$:	TST	@DHBAR
1563	004612	001404					:TRANSMITTER DONE NOT SET, ERROR
1564	004614	005005					:WAS BAR BIT CLEARED FOR LINE 5
1565							
1566	004616	017704	010546			MOV	@DHBAR, R4
1567							: (R5)=EXPECTED DATA IN
1568	004622	104000				HLT	0
1569	004624	022777	000001	010532	4\$:	CMP	#1, @DHBA
1570	004632	001405					:BUFFER ACTIVE REGISTER, 0
1571	004634	017704	010524			BEQ	5\$
1572						MOV	@DHBA, R4
1573							: (R4)=ACTUAL CONTENTS OF
1574	004640	012705	000001			MOV	#1, R5
1575							:BUFFER ACTIVE REGISTER
1576							:BUS ACTIVE BIT NOT CLEARED, ERROR
1577	004644	104003				HLT	3
1578							:WAS BUS ADDRESS INCREMENTED
1579	004646	005777	010514		5\$:	TST	@DHBC
1580	004652	001416				BEQ	6\$
1581	004654	017704	010506			MOV	@DHBC, R4
1582							: (R4)=ACTUAL VALUE OF BYTE
1583	004660	005005				CLR	R5
1584							:COUNT FOR LINE 5
1585	004662	104004				HLT	4
1586	004664	016777	010512	010506		MOV	@DHLVL, @DHVEC ;RESTORE TRAPCATCHER
1587	004672	005077	010504			CLR	@DHLVL
1588	004676	016777	010504	010500		MOV	@DHTLVL, @DHTVEC
1589	004704	005077	010476			CLR	@DHTLVL
1590	004710	012706	017102		6\$:	MOV	#STACK, SP
1591	004714	104400				SCOPE	:RESTORE STACK
1592							:CHECK FOR ITERATIONS, LOOP
1593							:NPR LOGIC TEST
1594							:SET BYTE COUNT TO 1 FOR LINE 6
1595							:SET BAR BIT FOR LINE 6
1596							:DELAY FOR NPR
1597							:VERIFY THAT BAR BIT FOR LINE 6 CLEARS


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1654                                     :SET BYTE COUNT TO 1 FOR LINE 7
1655                                     :SET BAR BIT FOR LINE 7
1656                                     :DELAY FOR NPR
1657                                     :VERIFY THAT BAR BIT FOR LINE 7 CLEARS
1658                                     :VERIFY THAT TRANSMITTER DONE IS SET
1659
1660 005154 012767 000340 172614 T17: MOV #340,PS ;DISABLE ALL INTERRUPTS
1661 005162 012767 000020 010234 MOV #20,COUNT ;SET UP FOR 20 ITERATIONS
1662 005170 012767 005404 010222 MOV #6$,ESCAPE ;SET UP TO ESCAPE TO NEXT TEST
1663 005176 012777 004000 010152 MOV #BIT11,ADHSCR ;ISSUE MASTER CLEAR
1664 005204 004767 010054 JSR PC,CLEAR ;CLEAR ALL BUS ADDRESS
1665 ;AND BYTE COUNT MEMORY LOCATIONS
1666 005210 012777 005272 010166 MOV #2$,ADHTVEC ;SET UP TRANSMITTER
1667 005216 012777 000340 010162 MOV #340,ADHTLVL ;INTERRUPT VECTOR
1668 005224 012777 000007 010124 MOV #7,ADHSCR ;SELECT LINE 7
1669 005232 012777 177777 010126 MOV #-1,ADHBC ;SET BYTE COUNT TO 1
1670 005240 012700 001000 MOV #1000,R0
1671 005244 012777 000200 010116 MOV #200,ADHBAR ;SET BAR BIT FOR
1672 ;LINE 7
1673 005252 052777 020000 010076 BIS #BIT13,ADHSCR ;SET TRANSMITTER INTERRUPT ENABLE
1674 005260 005067 172512 CLR PS ;ALLOW INTERRUPTS
1675 005264 005300 1$: DEC R0 ;DELAY FOR NPR
1676 005266 001376 BNE 1$
1677 005270 104001 HLT 1 ;NO INTERRUPT OCCURED, ERROR
1678 005272 005777 010060 2$: TST ADHSCR ;VERIFY THAT TRANSMITTER
1679 ;DONE IS SET
1680 005276 100401 BMI 3$
1681 005300 104002 HLT 2 ;TRANSMITTER DONE NOT SET, ERROR
1682 005302 005777 010062 3$: TST ADHBAR ;WAS BAR BIT CLEARED FOR LINE 7
1683 005306 001404 BEQ 4$
1684 005310 005005 CLR R5 ;(R5)=EXPECTED DATA IN
1685 ;BUFFER ACTIVE REGISTER, 0
1686 005312 017704 010052 MOV ADHBAR,R4 ;(R4)=ACTUAL CONTENTS OF
1687 ;BUFFER ACTIVE REGISTER
1688 005316 104000 HLT 0 ;BUS ACTIVE BIT NOT CLEARED, ERROR
1689 005320 022777 000001 010036 4$: CMP #1,ADHBA ;WAS BUS ADDRESS INCREMENTED
1690 005326 001405 BEQ 5$
1691 005330 017704 010030 MOV ADHBA,R4 ;(R4)=ACTUAL CONTENTS
1692 ;OF BUS ADDRESS MEMORY FOR
1693 ;LINE 7
1694 005334 012705 000001 MOV #1,R5 ;(R5)=EXPECTED VALUE OF
1695 ;BUS ADDRESS MEMORY FOR
1696 ;LINE 7, 1
1697 005340 104003 HLT 3 ;BUS ADDRESS NOT UPDATED
1698 ;CORRECTLY, ERROR
1699 005342 005777 010020 5$: TST ADHBC ;DID BYTE COUNT DECREMENT TO 0
1700 005346 001416 BEQ 6$
1701 005350 017704 010012 MOV ADHBC,R4 ;(R4)=ACTUAL VALUE OF BYTE
1702 ;COUNT FOR LINE 7
1703 005354 005005 CLR R5 ;(R5)=EXPECTED VALUE OF BYTE
1704 ;COUNT FOR LINE 7, 0
1705 005356 104004 HLT 4 ;BYTE COUNT DID NOT DECREMENT TO 0, ERROR
1706 005360 016777 010016 010012 MOV DHRLVL,ADHRVEC ;RESTORE TRAPCATCHER
1707 005366 005077 010010 CLR ADHRLVL
1708 005372 016777 010010 010004 MOV DHTLVL,ADHTVEC
1709 005400 005077 010002 CLR ADHTLVL
    
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1710	005404	012706	017102	6\$:	MOV	#STACK,SP		;RESTORE STACK
1711	005410	104400			SCOPE			;CHECK FOR ITERATIONS, LOOP
1712								
1713								;NPR LOGIC TEST
1714								;SET BYTE COUNT TO 1 FOR LINE 10
1715								;SET BAR BIT FOR LINE 10
1716								;DELAY FOR NPR
1717								;VERIFY THAT BAR BIT FOR LINE 10 CLEARS
1718								;VERIFY THAT TRANSMITTER DONE IS SET
1719								
1720	005412	012767	000340	172356	T20:	MOV	#340,PS	;DISABLE ALL INTERRUPTS
1721	005420	012767	000020	007776		MOV	#20,ICOUNT	;SET UP FOR 20 ITERATIONS
1722	005426	012767	005642	007764		MOV	#6\$,ESCAPE	;SET UP TO ESCAPE TO NEXT TEST
1723	005434	012777	004000	007714		MOV	#BIT11,ADHSCR	;ISSUE MASTER CLEAR
1724	005442	004767	007616			JSR	PC,CLEAR	;CLEAR ALL BUS ADDRESS
1725								;AND BYTE COUNT MEMORY LOCATIONS
1726	005446	012777	005530	007730		MOV	#2\$,ADHTVEC	;SET UP TRANSMITTER
1727	005454	012777	000340	007724		MOV	#340,ADHTLVL	;INTERRUPT VECTOR
1728	005462	012777	000010	007666		MOV	#10,ADHSCR	;SELECT LINE 10
1729	005470	012777	177777	007670		MOV	#-1,ADHBC	;SET BYTE COUNT TO 1
1730	005476	012700	001000			MOV	#1000,R0	
1731	005502	012777	000400	007660		MOV	#400,ADHBAR	;SET BAR BIT FOR
1732								;LINE 10
1733	005510	052777	020000	007640		BIS	#BIT13,ADHSCR	;SET TRANSMITTER INTERRUPT ENABLE
1734	005516	005067	172254			CLR	PS	;ALLOW INTERRUPTS
1735	005522	005300			1\$:	DEC	R0	;DELAY FOR NPR
1736	005524	001376				BNE	1\$	
1737	005526	104001				HLT	1	;NO INTERRUPT OCCURED, ERROR
1738	005530	005777	007622		2\$:	TST	ADHSCR	;VERIFY THAT TRANSMITTER
1739								;DONE IS SET
1740	005534	100401				BMI	3\$	
1741	005536	104002				HLT	2	;TRANSMITTER DONE NOT SET, ERROR
1742	005540	005777	007624		3\$:	TST	ADHBAR	;WAS BAR BIT CLEARED FOR LINE 10
1743	005544	001404				BEG	4\$	
1744	005546	005005				CLR	R5	
1745								; (R5)=EXPECTED DATA IN
1746	005550	017704	007614			MOV	ADHBAR,R4	;BUFFER ACTIVE REGISTER, 0
1747								; (R4)=ACTUAL CONTENTS OF
1748	005554	104000				HLT	0	;BUFFER ACTIVE REGISTER
1749	005556	022777	000001	007600	4\$:	CMP	#1,ADHBA	;BUS ACTIVE BIT NOT CLEARED, ERROR
1750	005564	001405				BEG	5\$;WAS BUS ADDRESS INCREMENTED
1751	005566	017704	007572			MOV	ADHBA,R4	
1752								; (R4)=ACTUAL CONTENTS
1753								; OF BUS ADDRESS MEMORY FOR
1754	005572	012705	000001			MOV	#1,R5	;LINE 10
1755								; (R5)=EXPECTED VALUE OF
1756								;BUS ADDRESS MEMORY FOR
1757	005576	104003				HLT	3	;LINE 10, 1
1758								;BUS ADDRESS NOT UPDATED
1759	005600	005777	007562		5\$:	TST	ADHBC	;CORRECTLY, ERROR
1760	005604	001416				BEG	6\$;DID BYTE COUNT DECREMENT TO 0
1761	005606	017704	007554			MOV	ADHBC,R4	
1762								; (R4)=ACTUAL VALUE OF BYTE
1763	005612	005005				CLR	R5	;COUNT FOR LINE 10
1764								; (R5)=EXPECTED VALUE OF BYTE
1765	005614	104004				HLT	4	;COUNT FOR LINE 10, 0
								;BYTE COUNT DID NOT DECREMENT TO 0, ERROR

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1766 005616 016777 007560 007554      MOV    DHRLVL, @DHVEC ;RESTORE TRAPCATCHER
1767 005624 005077 007552              CLR    @DHRLVL
1768 005630 016777 007552 007546      MOV    DHTLVL, @DHVEC
1769 005636 005077 007544              CLR    @DHTLVL
1770 005642 012706 017102      6$:   MOV    *STACK, SP ;RESTORE STACK
1771 005646 104400              SCOPE ;CHECK FOR ITERATIONS, LOOP
1772
1773              :NPR LOGIC TEST
1774              :SET BYTE COUNT TO 1 FOR LINE 11
1775              :SET BAR BIT FOR LINE 11
1776              :DELAY FOR NPR
1777              :VERIFY THAT BAR BIT FOR LINE 11 CLEARS
1778              :VERIFY THAT TRANSMITTER DONE IS SET
1779
1780 005650 012767 000340 172120 T21:  MOV    #340, PS ;DISABLE ALL INTERRUPTS
1781 005656 012767 000020 007540      MOV    #20, ICOUNT ;SET UP FOR 20 ITERATIONS
1782 005664 012767 006100 007526      MOV    #6$, ESCAPE ;SET UP TO ESCAPE TO NEXT TEST
1783 005672 012777 004000 007456      MOV    #BIT11, @DHSCR ;ISSUE MASTER CLEAR
1784 005700 004767 007360      JSR    PC, CLEAR ;CLEAR ALL BUS ADDRESS
1785 ;AND BYTE COUNT MEMORY LOCATIONS
1786 005704 012777 005766 007472      MOV    #2$, @DHVEC ;SET UP TRANSMITTER
1787 005712 012777 000340 007466      MOV    #340, @DHTLVL ;INTERRUPT VECTOR
1788 005720 012777 000011 007430      MOV    #11, @DHSCR ;SELECT LINE 11
1789 005726 012777 177777 007432      MOV    #-1, @DHBC ;SET BYTE COUNT TO 1
1790 005734 012700 001000      MOV    #1000, R0
1791 005740 012777 001000 007422      MOV    #1000, @DHBAR ;SET BAR BIT FOR
1792 ;LINE 11
1793 005746 052777 020000 007402      BIS    #BIT13, @DHSCR ;SET TRANSMITTER INTERRUPT ENABLE
1794 005754 005067 172016      CLR    PS ;ALLOW INTERRUPTS
1795 005760 005300      1$:   DEC    R0 ;DELAY FOR NPR
1796 005762 001376      BNE   1$
1797 005764 104001      HLT   1 ;NO INTERRUPT OCCURED, ERROR
1798 005766 005777 007364      2$:   TST   @DHSCR ;VERIFY THAT TRANSMITTER
1799 ;DONE IS SET
1800 005772 100401      BMI   3$
1801 005774 104002      HLT   2 ;TRANSMITTER DONE NOT SET, ERROR
1802 005776 005777 007366      3$:   TST   @DHBAR ;WAS BAR BIT CLEARED FOR LINE 11
1803 006002 001404      BEQ   4$
1804 006004 005005      CLR   R5 ;(R5)=EXPECTED DATA IN
1805 ;BUFFER ACTIVE REGISTER, 0
1806 006006 017704 007356      MOV    @DHBAR, R4 ;(R4)=ACTUAL CONTENTS OF
1807 ;BUFFER ACTIVE REGISTER
1808 006012 104000      HLT   0 ;BUS ACTIVE BIT NOT CLEARED, ERROR
1809 006014 022777 000001 007342 4$:   CMP    #1, @DHBA ;WAS BUS ADDRESS INCREMENTED
1810 006022 001405      BEQ   5$
1811 006024 017704 007334      MOV    @DHBA, R4 ;(R4)=ACTUAL CONTENTS
1812 ;OF BUS ADDRESS MEMORY FOR
1813 ;LINE 11
1814 006030 012705 000001      MOV    #1, R5 ;(R5)=EXPECTED VALUE OF
1815 ;BUS ADDRESS MEMORY FOR
1816 ;LINE 11, 1
1817 006034 104003      HLT   3 ;BUS ADDRESS NOT UPDATED
1818 ;CORRECTLY, ERROR
1819 006036 005777 007324      5$:   TST   @DHBC ;DID BYTE COUNT DECREMENT TO 0
1820 006042 001416      BEQ   6$
1821 006044 017704 007316      MOV    @DHBC, R4 ;(R4)=ACTUAL VALUE OF BYTE

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1822                                     ;COUNT FOR LINE 11
1823 006050 005005 CLR R5 ;(R5)=EXPECTED VALUE OF BYTE
1824                                     ;COUNT FOR LINE 11, 0
1825 006052 104004 HLT 4 ;BYTE COUNT DID NOT DECREMENT TO 0, ERROR
1826 006054 016777 007322 007316 MOV DHRLVL,ADHRVEC ;RESTORE TRAPCATCHER
1827 006062 005077 007314 CLR ADHRLVL
1828 006056 016777 007314 007310 MOV DHTLVL,ADHTVEC
1829 006074 005077 007306 CLR ADHTLVL
1830 006100 012706 017102 6$: MOV #STACK,SP ;RESTORE STACK
1831 006104 104400 SCOPE ;CHECK FOR ITERATIONS, LOOP
1832
1833 ;NPR LOGIC TEST
1834 ;SET BYTE COUNT TO 1 FOR LINE 12
1835 ;SET BAR BIT FOR LINE 12
1836 ;DELAY FOR NPR
1837 ;VERIFY THAT BAR BIT FOR LINE 12 CLEARS
1838 ;VERIFY THAT TRANSMITTER DONE IS SET
1839
1840 006106 012767 000340 171662 T22: MOV #340,PS ;DISABLE ALL INTERRUPTS
1841 006114 012767 000020 007302 MOV #20,COUNT ;SET UP FOR 20 ITERATIONS
1842 006122 012767 006336 007270 MOV #6$,ESCAPE ;SET UP TO ESCAPE TO NEXT TEST
1843 006130 012777 004C00 007220 MOV #BIT11,ADHSCR ;ISSUE MASTER CLEAR
1844 006136 004767 007122 JSR PC,CLEAR ;CLEAR ALL BUS ADDRESS
1845 ;AND BYTE COUNT MEMORY LOCATIONS
1846 006142 012777 006224 007234 MOV #2$,ADHTVEC ;SET UP TRANSMITTER
1847 006150 012777 000340 007230 MOV #340,ADHTLVL ;INTERRUPT VECTOR
1848 006156 012777 000012 007172 MOV #12,ADHSCR ;SELECT LINE 12
1849 006164 012777 177777 007174 MOV #-1,ADHBC ;SET BYTE COUNT TO 1
1850 006172 012700 001000 MOV #1000,RO
1851 006176 012777 002000 007164 MOV #2000,ADHBAR ;SET BAR BIT FOR
1852 ;LINE 12
1853 006204 052777 020000 007144 BIS #BIT13,ADHSCR ;SET TRANSMITTER INTERRUPT ENABLE
1854 006212 005067 171560 CLR PS ;ALLOW INTERRUPTS
1855 006216 005300 1$: DEC RO ;DELAY FOR NPR
1856 006220 001376 BNE 1$
1857 006222 104001 HLT 1 ;NO INTERRUPT OCCURED, ERROR
1858 006224 005777 007126 2$: TST ADHSCR ;VERIFY THAT TRANSMITTER
1859 ;DONE IS SET
1860 006230 100401 BMI 3$
1861 006232 104002 HLT 2 ;TRANSMITTER DONE NOT SET, ERROR
1862 006234 005777 007130 3$: TST ADHBAR ;WAS BAR BIT CLEARED FOR LINE 12
1863 006240 001404 BEQ 4$
1864 006242 005005 CLR R5 ;(R5)=EXPECTED DATA IN
1865 ;BUFFER ACTIVE REGISTER, J
1866 006244 017704 007120 MOV ADHBAR,R4 ;(R4)=ACTUAL CONTENTS OF
1867 ;BUFFER ACTIVE REGISTER
1868 006250 104000 HLT 0 ;BUS ACTIVE BIT NOT CLEARED, ERROR
1869 006252 022777 000001 007104 4$: CMP #1,ADHBA ;WAS BUS ADDRESS INCREMENTED
1870 006250 001405 BEQ 5$
1871 006262 017704 007076 MOV ADHBA,R4 ;(R4)=ACTUAL CONTENTS
1872 ;OF BUS ADDRESS MEMORY FOR
1873 ;LINE 12
1874 006266 012705 000001 MOV #1,R5 ;(R5)=EXPECTED VALUE OF
1875 ;BUS ADDRESS MEMORY FOR
1876 ;LINE 12, 1
1877 006272 104003 HLT 3 ;BUS ADDRESS NOT UPDATED
    
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1878                                     ;CORRECTLY, ERROR
1879 006274 005777 007066          5$:  TST   @DHBC          ;DID BYTE COUNT DECREMENT TO 0
1880 005300 001416                                     BEQ   6$
1881 006302 017704 007060          MOV   @DHBC,R4          ;(R4)=ACTUAL VALUE OF BYTE
1882                                     ;COUNT FOR LINE 12
1883 006306 005005          CLR   R5          ;(R5)=EXPECTED VALUE OF BYTE
1884                                     ;COUNT FOR LINE 12, 0
1885 006310 104004          HLT   4          ;BYTE COUNT DID NOT DECREMENT TO 0, ERROR
1886 006312 016777 007064 007060    MOV   DHRVLV,@DHVEC ;RESTORE TRAPCATCHER
1887 006320 005077 007056          CLR   @DHRVLV
1888 006324 016777 007056 007052    MOV   DHTVLV,@DHTVEC
1889 006332 005077 007050          CLR   @DHTVLV
1890 006336 012706 017102          6$:  MOV   *STACK,SP      ;RESTORE STACK
1891 006342 104400          SCOPE          ;CHECK FOR ITERATIONS, LOOP
1892
1893                                     ;NPR LOGIC TEST
1894                                     ;SET BYTE COUNT TO 1 FOR LINE 13
1895                                     ;SET BAR BIT FOR LINE 13
1896                                     ;DELAY FOR NPR
1897                                     ;VERIFY THAT BAR BIT FOR LINE 13 CLEARS
1898                                     ;VERIFY THAT TRANSMITTER DONE IS SET
1899
1900 006344 012767 000340 171424    T23: MOV   #340,PS          ;DISABLE ALL INTERRUPTS
1901 006352 012767 000020 007044    MOV   #20,ICOUNT      ;SET UP FOR 20 ITERATIONS
1902 006360 012767 006574 007032    MOV   #6$,ESCAPE      ;SET UP TO ESCAPE TO NEXT TEST
1903 006366 012777 004000 006762    MOV   #BIT11,@DHSCR   ;ISSUE MASTER CLEAR
1904 006374 004767 006664          JSR   PC,CLEAR        ;CLEAR ALL BUS ADDRESS
1905                                     ;AND BYTE COUNT MEMORY LOCATIONS
1906 006400 012777 006462 006776    MOV   #2$,@DHTVEC     ;SET UP TRANSMITTER
1907 006406 012777 000340 006772    MOV   #340,@DHTVLV   ;INTERRUPT VECTOR
1908 006414 012777 000013 006734    MOV   #13,@DHSCR     ;SELECT LINE 13
1909 006422 012777 177777 006736    MOV   #-1,@DHBC      ;SET BYTE COUNT TO 1
1910 006430 012700 001000          MOV   #1000,R0
1911 006434 012777 004000 006726    MOV   #4000,@DHBAR   ;SET BAR BIT FOR
1912                                     ;LINE 13
1913 006442 052777 020000 006706    BIS   #BIT13,@DHSCR  ;SET TRANSMITTER INTERRUPT ENABLE
1914 006450 005067 171322          CLR   PS             ;ALLOW INTERRUPTS
1915 006454 005300          1$:  DEC   R0             ;DELAY FOR NPR
1916 006456 001376          BNE   1$
1917 006460 104001          HLT   1             ;NO INTERRUPT OCCURED, ERROR
1918 006462 005777 006670          2$:  TST   @DHSCR     ;VERIFY THAT TRANSMITTER
1919                                     ;DONE IS SET
1920 006466 100401          BMI   3$
1921 006470 104002          HLT   2             ;TRANSMITTER DONE NOT SET, ERROR
1922 006472 005777 006672          3$:  TST   @DHBAR     ;WAS BAR BIT CLEARED FOR LINE 13
1923 006476 001404          BEQ   4$
1924 006500 005005          CLR   R5             ;(R5)=EXPECTED DATA IN
1925                                     ;BUFFER ACTIVE REGISTER, 0
1926 006502 017704 006662          MOV   @DHBAR,R4      ;(R4)=ACTUAL CONTENTS OF
1927                                     ;BUFFER ACTIVE REGISTER
1928 006506 104000          HLT   0             ;BUS ACTIVE BIT NOT CLEARED, ERROR
1929 006510 022777 000001 006646    4$:  CMP   #1,@DHBA     ;WAS BUS ADDRESS INCREMENTED
1930 006516 001405          BEQ   5$
1931 006520 017704 006640          MOV   @DHBA,R4      ;(R4)=ACTUAL CONTENTS
1932                                     ;OF BUS ADDRESS MEMORY FOR
1933                                     ;LINE 13

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006524 012705 000001      MOV      #1,R5      ; R5=EXPECTED VALUE OF
                                ; BUS ADDRESS MEMORY FOR
                                ; LINE 13, 1
006530 104003      HLT      3          ; BUS ADDRESS NOT UPDATED
                                ; CORRECTLY, ERROR
006532 005777 006630      55:     TST      2DHBC  ; DID BYTE COUNT DECREMENT TO 0
006536 001416      BEQ      55
006540 017704 006622      MOV      2DHBC,R4  ; R4=ACTUAL VALUE OF BYTE
                                ; COUNT FOR LINE 13
006544 005005      CLR      R5        ; R5=EXPECTED VALUE OF BYTE
                                ; COUNT FOR LINE 13, 0
006546 104004      HLT      4          ; BYTE COUNT DID NOT DECREMENT TO 0, ERROR
006550 016777 006626 006622      MOV      2DHRLVL,2DHRVEC ; RESTORE TRAPCATCHER
006552 005005      CLR      2DHRLVL
006554 016777 006620 006614      MOV      2DHTLVL,2DHTVEC
006556 005005      CLR      2DHTLVL
006558 012706 006612 006612      MOV      #STACK,SP ; RESTORE STACK
006560 104400      SCOPE           ; CHECK FOR ITERATIONS, LOOP

                                ; NPR LOGIC TEST
                                ; SET BYTE COUNT TO 1 FOR LINE 14
                                ; SET BAR BIT FOR LINE 14
                                ; DELAY FOR NPR
                                ; VERIFY THAT BAR BIT FOR LINE 14 CLEARS
                                ; VERIFY THAT TRANSMITTER DONE IS SET

006600 012767 000340 171166  T24:   MOV      #240,PS   ; DISABLE ALL INTERRUPTS
006602 012767 000020 006606      MOV      #20,ICOUNT ; SET UP FOR 20 ITERATIONS
006604 012767 007032 006574      MOV      #65,ESCAPE ; SET UP TO ESCAPE TO NEXT TEST
006606 012777 004000 006524      MOV      #BIT11,2DHSCR ; ISSUE MASTER CLEAR
006608 004767 006426      JSR      PC,CLEAR  ; CLEAR ALL BUS ADDRESS
                                ; AND BYTE COUNT MEMORY LOCATIONS
006610 012777 006720 006540      MOV      #25,2DHTVEC ; SET UP TRANSMITTER
006612 012777 000340 006534      MOV      #340,2DHTLVL ; INTERRUPT VECTOR
006614 012777 000014 006476      MOV      #14,2DHSCR  ; SELECT LINE 14
006616 012777 177777 006500      MOV      #-1,2DHBC  ; SET BYTE COUNT TO 1
006618 012700 001000      MOV      #1000,R0
006620 012777 010000 006470      MOV      #10000,2DHBAR ; SET BAR BIT FOR
                                ; LINE 14
006700 052777 020000 006450      BIS      #BIT13,2DHSCR ; SET TRANSMITTER INTERRUPT ENABLE
006702 005067 171064      CLR      PS        ; ALLOW INTERRUPTS
006704 005000      15:     DEC      R0        ; DELAY FOR NPR
006706 001376      BNE     15
006708 104001      HLT     !          ; NO INTERRUPT OCCURED, ERROR
006710 005777 006432      25:     TST      2DHSCR  ; VERIFY THAT TRANSMITTER
                                ; DONE IS SET
006712 100401      BMI     35
006714 104002      HLT     2
006716 005777 006434      35:     TST      2DHBAR  ; TRANSMITTER DONE NOT SET, ERROR
                                ; WAS BAR BIT CLEARED FOR LINE 14
006718 001404      BEQ     45
006720 005005      CLR     R5
                                ; (R5)=EXPECTED DATA IN
                                ; BUFFER ACTIVE REGISTER, 0
006722 017704 006424      MOV     2DHBAR,R4 ; (R4)=ACTUAL CONTENTS OF
                                ; BUFFER ACTIVE REGISTER
006724 104000      HLT     0          ; BUS ACTIVE BIT NOT CLEARED, ERROR
006726 022777 000001 006410  45:     CMP     #1,2DHBA  ; WAS BUS ADDRESS INCREMENTED

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00000000 006754 001405 BEQ 55
00000001 006756 017704 006402 MOV 2D4BA,R4 ;(R4)=ACTUAL CONTENTS
00000002 006762 012705 000001 MOV #1,R5 ;OF BUS ADDRESS MEMORY FOR
00000003 006766 104003 HLT 3 ;LINE 14
00000004 006770 005777 006372 55: TST 2DHBC ;(R5)=EXPECTED VALUE OF
00000005 006774 001416 BEQ 65 ;BUS ADDRESS MEMOR. FOR
00000006 006776 017704 006364 MOV 2DHBC,R4 ;LINE 14
00000007 007002 005005 CLR R5 ;BUS ADDRESS NOT UPDATED
00000008 007004 104004 HLT 4 ;CORRECTLY ERROR
00000009 007006 016777 006370 006364 MOV DHRVLV,2DHRVEC ;DID BYTE COUNT DECREMENT TO 0
00000010 007014 005077 006362 CLR 2DHRVLV ;RESTORE TRAPCATCHER
00000011 007020 016777 006362 006356 MOV DHTLVL,2DHTVEC
00000012 007026 005077 006354 CLR 2DHTLVL
00000013 007032 012706 017102 65: MOV #STACK,SP ;RESTORE STACK
00000014 007036 :04400 SCOPE ;CHECK FOR ITERATIONS. LOOP

;NPR LOGIC TEST
;SET BYTE COUNT TO 1 FOR LINE 15
;SET BAR BIT FOR LINE 15
;DELAY FOR NPR
;VERIFY THAT BAR BIT FOR LINE 15 CLEARS
;VERIFY THAT TRANSMITTER DONE IS SET

00000015 007040 012767 000340 170730 725: MOV #340,PS ;DISABLE ALL INTERRUPTS
00000016 007046 012767 000020 006350 MOV #20,COUNT ;SET UP FOR 20 ITERATIONS
00000017 007054 012767 007270 006336 MOV #65,ESCAPE ;SET UP TO ESCAPE TO NEXT TEST
00000018 007062 012777 004000 006266 MOV #BIT11,2DHSCR ;ISSUE MASTER CLEAR
00000019 007070 004767 006170 JSR PC,CLEAR ;CLEAR ALL BUS ADDRESS
;AND BYTE COUNT MEMORY LOCATIONS
00000020 007074 012777 007156 006302 MOV #25,2DHTVEC ;SET UP TRANSMITTER
00000021 007102 012777 000340 006276 MOV #340,2DHTLVL ;INTERRUPT VECTOR
00000022 007110 012777 000015 006240 MOV #15,2DHSCR ;SELECT LINE 15
00000023 007116 012777 177777 006242 MOV #-1,2DHBC ;SET BYTE COUNT TO 1
00000024 007124 012700 001000 MOV #1000,R0
00000025 007130 012777 020000 006232 MOV #20000,2DH3AR ;SET BAR BIT FOR
;LINE 15
00000026 007136 052777 020000 006212 BIS #BIT13,2DHSCR ;SET TRANSMITTER INTERRUPT ENABLE
00000027 007144 005067 170626 CLR PS ;ALLOW INTERRUPTS
00000028 007150 005300 1S: DEC R0 ;DELAY FOR NPR
00000029 007152 001376 BNE 15
00000030 007154 10400! HLT 1 ;NO INTERRUPT OCCURED. ERROR
00000031 007156 005777 006174 25: TST 2DHSCR ;VERIFY THAT TRANSMITTER
;DONE IS SET
00000032 007162 100401 BMI 35
00000033 007164 104002 HLT 2 ;TRANSMITTER DONE NOT SET. ERROR
00000034 007166 005777 006176 35: TST 2DHBAR ;WAS BAR BIT CLEARED FOR LINE 15
00000035 007172 001404 BEQ 45
00000036 007174 005005 CLR R5 ;(R5)=EXPECTED DATA IN
;BLUFFER ACTIVE REGISTER. 0

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007176 017704 006166      MOV      2DHBAR,R4      ;(R4)=ACTUAL CONTENTS OF
007202 104000      HLT      0              ;BUFFER ACTIVE REGISTER
007204 022777 000001 006152 45:      CMP      #1,2DHBA      ;BUS ACTIVE BIT NOT CLEARED, ERROR
007212 001405      BEQ      55            ;WAS BUS ADDRESS INCREMENTED
007214 017704 006144      MOV      2DHBA,R4      ;(R4)=ACTUAL CONTENTS
                                ;OF BUS ADDRESS MEMORY FOR
                                ;LINE 15
007220 012705 000001      MOV      #1,R5         ;(R5)=EXPECTED VALUE OF
                                ;BUS ADDRESS MEMORY FOR
                                ;LINE 15, 1
007224 104003      HLT      3              ;BUS ADDRESS NOT UPDATED
                                ;CORRECTLY, ERROR
007226 005777 006134      55:      TST      2DHBC         ;DID BYTE COUNT DECREMENT TO 0
007232 001416      BEQ      55
007234 017704 006126      MOV      2DHBC,R4      ;(R4)=ACTUAL VALUE OF BYTE
                                ;COUNT FOR LINE 15
007240 005005      CLR      R5            ;(R5)=EXPECTED VALUE OF BYTE
                                ;COUNT FOR LINE 15, 0
007242 104004      HLT      4              ;BYTE COUNT DID NOT DECREMENT TO 0, ERROR
007244 016777 006132 006126      MOV      2DHRLVL,2DHRVEC ;RESTORE TRAPCATCHER
007252 005077 006124      CLR      2DHRLVL
007256 016777 006124 006120      MOV      2DHTLVL,2DHTVEC
007264 005077 006116      CLR      2DHTLVL
007270 012706 017102 55:      MOV      #STACK,SP    ;RESTORE STACK
007274 104400      SCOPE                ;CHECK FOR ITERATIONS, LOOP

;NPR LOGIC TEST
;SET BYTE COUNT TO 1 FOR LINE 16
;SET BAR BIT FOR LINE 16
;DELAY FOR NPR
;VERIFY THAT BAR BIT FOR LINE 16 CLEARS
;VERIFY THAT TRANSMITTER DONE IS SET

007276 012767 000340 170472 T26:      MOV      #340,PS      ;DISABLE ALL INTERRUPTS
007284 012767 000020 006112      MOV      #20,ICOUNT   ;SET UP FOR 20 ITERATIONS
007312 012767 007526 006100      MOV      #65,ESCAPE   ;SET UP TO ESCAPE TO NEXT TEST
007320 012777 004000 006030      MOV      #BIT11,2DHSCR ;ISSUE MASTER CLEAR
007326 004767 005732      JSR      PC,CLEAR     ;CLEAR ALL BUS ADDRESS
                                ;AND BYTE COUNT MEMORY LOCATIONS
007332 012777 007414 006044      MOV      #25,2DHTVEC  ;SET UP TRANSMITTER
007340 012777 000340 006040      MOV      #340,2DHTLVL ;INTERRUPT VECTOR
007346 012777 000016 006002      MOV      #16,2DHSCR   ;SELECT LINE 16
007354 012777 177777 006004      MOV      #-1,2DHBC    ;SET BYTE COUNT TO 1
007362 012700 001000      MOV      #1000,R0
007366 012777 040000 005774      MOV      #40000,2DHBAR ;SET BAR BIT FOR
                                ;LINE 16
007374 052777 020000 005754      BIS      #BIT13,2DHSCR ;SET TRANSMITTER INTERRUPT ENABLE
007402 005067 170370      CLR      PS           ;ALLOW INTERRUPTS
007406 005300      15:      DEC      R0           ;DELAY FOR NPR
007410 001376      BNE     15
007412 104001      HLT     1
007414 005777 005736 25:      TST     2DHSCR        ;NO INTERRUPT OCCURED, ERROR
                                ;VERIFY THAT TRANSMITTER
                                ;DONE IS SET
007420 100401      BMI     35
007422 104002      HLT     2              ;TRANSMITTER DONE NOT SET, ERROR

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2158 007652 005777 005500 2$: TST 3DHSCR ;VERIFY THAT TRANSMITTER
2159 ;DONE IS SET
2160 007656 100401 BMI 3$
2161 007660 104002 HLT 2 ;TRANSMITTER DONE NOT SET, ERROR
2162 007662 005777 005502 3$: TST 3DHBAR ;WAS BAR BIT CLEARED FOR LINE 17
2163 007666 001404 BEQ 4$
2164 007670 005005 CLR R5 ;(R5)=EXPECTED DATA IN
2165 ;BUFFER ACTIVE REGISTER, 0
2166 007672 017704 005472 MOV 3DHBAR,R4 ;(R4)=ACTUAL CONTENTS OF
2167 ;BUFFER ACTIVE REGISTER
2168 007676 104000 HLT 0 ;BUS ACTIVE BIT NOT CLEARED, ERROR
2169 007700 022777 000001 005456 4$: CMP #1,3DHBA ;WAS BUS ADDRESS INCREMENTED
2170 007706 001405 BEQ 5$
2171 007710 017704 005450 MOV 3DHBA,R4 ;(R4)=ACTUAL CONTENTS
2172 ;OF BUS ADDRESS MEMORY FOR
2173 ;LINE 17
2174 007714 012705 000001 MOV #1,R5 ;(R5)=EXPECTED VALUE OF
2175 ;BUS ADDRESS MEMORY FOR
2176 ;LINE 17, 1
2177 007720 104003 HLT 3 ;BUS ADDRESS NOT UPDATED
2178 ;CORRECTLY, ERROR
2179 007722 005777 005440 5$: TST 3DHBC ;DID BYTE COUNT DECREMENT TO 0
2180 007726 001416 BEQ 6$
2181 007730 017704 005432 MOV 3DHBC,R4 ;(R4)=ACTUAL VALUE OF BYTE
2182 ;COUNT FOR LINE 17
2183 007734 005005 CLR R5 ;(R5)=EXPECTED VALUE OF BYTE
2184 ;COUNT FOR LINE 17, 0
2185 007736 104004 HLT 4 ;BYTE COUNT DID NOT DECREMENT TO 0, ERROR
2186 007740 016777 005436 005432 MOV DHRVLV,3DHVEC ;RESTORE TRAPCATCHER
2187 007746 005077 005430 CLR 3DHRVLV
2188 007752 016777 005430 005424 MOV DHTLVL,3DHTVEC
2189 007760 005077 005422 CLR 3DHTLVL
2190 007764 012706 017102 6$: MOV #STACK,SP ;RESTORE STACK
2191 007770 104400 SSCOPE ;CHECK FOR ITERATIONS, LOOP
2192
2193 ;NPR LOGIC TEST
2194 ;SET BYTE COUNT ON ALL LINES TO 1
2195 ;SET BAR BIT FOR LINE 0
2196 ;VERIFY THAT BYTE COUNT FOR LINE 0 GOES TO 0
2197 ;VERIFY THAT BUS ADDRESS FOR LINE 0 IS INCREMENTED
2198 ;VERIFY THAT BYTE COUNTS AND BUS ADDRESSES FOR ALL OTHER LINES
2199 ;ARE UNCHANGED
2200
2201 007772 012767 000340 167776 T30: MOV #340,PS ;DISABLE ALL INTERRUPTS
2202 010000 012767 000010 005416 MOV #10,ICOUNT ;SET UP FOR 10 ITERATIONS
2203 010006 012767 010140 005404 MOV #8$,ESCAPE ;SET UP TO ESCAPE TO NEXT TEST
2204 010014 012777 004000 005334 MOV #BIT11,3DHSCR ;MASTER CLEAR INTERFACE
2205 ;TO SET ALL TBMT BITS
2206 010022 004767 005236 JSR PC,CLEAR ;CLEAR ALL BYTE COUNT AND
2207 ;BUS ADDRESS MEMORY LOCATIONS
2208 010026 004767 005264 JSR PC,LOAD ;SET ALL BYTE COUNT LOCATIONS TO -1
2209 010032 012777 000001 005330 MOV #1,3DHBAR ;SET BAR BIT FOR LINE 0
2210 010040 005777 005312 3$: TST 3DHSCR ;WAIT FOR TRANSMITTER DONE
2211 010044 100375 BPL 3$
2212 010046 012700 000020 MOV #20,R0 ;SET UP TO CHECK ALL 16 LINES
2213 010052 005077 005300 CLR 3DHSCR ;START AT LINE 0
    
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2214 010056 005001          CLR      R1          ;KEEP TRACK OF LINE NUMBER
2215 010060 012705 177777 4$:  MOV      #-1,R5    ;(R5)=EXPECTED BYTE COUNT,
2216                                ;IF LINE NUMBER NOT = 0
2217 010064 005003          CLR      R3          ;(R3)=EXPECTED BUS ADDRESS,
2218                                ;IF LINE NUMBER NOT = 0
2219 010066 017704 005274    MOV      @DHBC,R4    ;(R4)=ACTUAL BYTE ACCOUNT
2220 010072 017702 005266    MOV      @DHBA,R2    ;(R5)=ACTUAL BUS ADDRESS
2221 010076 027727 005254 000000  CMP      @DHSCR,#0    ;IF LINE BEING COMPARED IS LINE 0
2222 010104 001002          BNE     5$
2223 010106 005005          CLR      R5          ;EXPECTED BYTE COUNT=0
2224 010110 005203          INC     R3          ;EXPECTED BUS ADDRESS = 1
2225 010112 020504          5$:  CMP      R5,R4    ;IS BYTE COUNT CORRECT
2226 010114 001401          SEQ     6$
2227 010116 104004          HLT     4           ;BYTE COUNT ERROR
2228 010120 020302          5$:  CMP      R3,R2    ;IS BUS ADDRESS CORRECT
2229 010122 001401          BEQ     7$
2230 010124 104003          HLT     3           ;BUS ADDRESS ERROR
2231 010126 005277 005224 7$:  INC     @DHSCR    ;PREPARE TO CHECK NEXT LINE
2232 010132 005201          INC     R1
2233 010134 005300          DEC     R0          ;CONTINUE IF ALL NOT DONE
2234 010136 001350          BNE     4$
2235 010140 104400          5$:  SCOPE          ;CHECK FOR ITERATIONS, LOOP
2236
2237                                ;NPP LOGIC TEST
2238                                ;SET BYTE COUNT ON ALL LINES TO 1
2239                                ;SET BAR BIT FOR LINE 1
2240                                ;VERIFY THAT BYTE COUNT FOR LINE 1 GOES TO 0
2241                                ;VERIFY THAT BUS ADDRESS FOR LINE 1 IS INCREMENTED
2242                                ;VERIFY THAT BYTE COUNTS AND BUS ADDRESSES FOR ALL OTHER LINES
2243                                ;ARE UNCHANGED
2244
2245 010142 012767 000340 167626 T31: MOV      #340,PS    ;DISABLE ALL INTERRUPTS
2246 010150 012767 000010 005246    MOV      #10,ICOUNT ;SET UP FOR 10 ITERATIONS
2247 010156 012767 010310 005234    MOV      #8$,ESCAPE ;SET UP TO ESCAPE TO NEXT TEST
2248 010164 012777 004000 005164    MOV      #BIT11,@DHSCR ;MASTER CLEAR INTERFACE
2249                                ;TO SET ALL TBMT BITS
2250 010172 004767 005066          JSR     PC,CLEAR    ;CLEAR ALL BYTE COUNT AND
2251                                ;BUS ADDRESS MEMORY LOCATIONS
2252 010176 004767 005114          JSR     PC,LOAD     ;SET ALL BYTE COUNT LOCATIONS TO -1
2253 010202 012777 000002 005160    MOV      #2,@DHBAR  ;SET BAR BIT FOR LINE 1
2254 010210 005777 005142          3$:  TST     @DHSCR    ;WAIT FOR TRANSMITTER DONE
2255 010214 100375          BPL     3$
2256 010216 012700 000020          MOV      #20,R0    ;SET UP TO CHECK ALL 16 LINES
2257 010222 005077 005130          CLR     @DHSCR    ;START AT LINE 0
2258 010226 005001          CLR     R1          ;KEEP TRACK OF LINE NUMBER
2259 010230 012705 177777 4$:  MOV      #-1,R5    ;(R5)=EXPECTED BYTE COUNT,
2260                                ;IF LINE NUMBER NOT = 1
2261 010234 005003          CLR     R3          ;(R3)=EXPECTED BUS ADDRESS,
2262                                ;IF LINE NUMBER NOT = 1
2263 010236 017704 005124    MOV      @DHBC,R4    ;(R4)=ACTUAL BYTE ACCOUNT
2264 010242 017702 005116    MOV      @DHBA,R2    ;(R5)=ACTUAL BUS ADDRESS
2265 010246 027727 005104 000001  CMP      @DHSCR,#1    ;IF LINE BEING COMPARED IS LINE 1
2266 010254 001002          BNE     5$
2267 010256 005005          CLR     R5          ;EXPECTED BYTE COUNT=0
2268 010260 005203          INC     R3          ;EXPECTED BUS ADDRESS = 1
2269 010262 020504          5$:  CMP      R5,R4    ;IS BYTE COUNT CORRECT
    
```

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2270 010264 001401      BEQ      6$
2271 010266 104004      HLT      4          ;BYTE COUNT ERROR
2272 010270 020302      6$: CMP    R3,R2    ;IS BUS ADDRESS CORRECT
2273 010272 001401      BEQ      7$
2274 010274 104003      HLT      3          ;BUS ADDRESS ERROR
2275 010276 005277 005054      7$: INC    2DHSCR   ;PREPARE TO CHECK NEXT LINE
2276 010302 005201      INC     R1
2277 010304 005300      DEC     R0          ;CONTINUE IF ALL NOT DONE
2278 010306 001350      BNE     4$
2279 010310 104400      8$: SCOPE          ;CHECK FOR ITERATIONS, LOOP
2280
2281      ;NPR LOGIC TEST
2282      ;SET BYTE COUNT ON ALL LINES TO 1
2283      ;SET BAR BIT FOR LINE 2
2284      ;VERIFY THAT BYTE COUNT FOR LINE 2 GOES TO 0
2285      ;VERIFY THAT BUS ADDRESS FOR LINE 2 IS INCREMENTED
2286      ;VERIFY THAT BYTE COUNTS AND BUS ADDRESSES FOR ALL OTHER LINES
2287      ;ARE UNCHANGED
2288
2289 010312 012767 000340 167456 T32: MOV     #340,R5    ;DISABLE ALL INTERRUPTS
2290 010320 012767 000010 005076   MOV     #10,R1    ;SET UP FOR 10 ITERATIONS
2291 010326 012767 010460 005064   MOV     #8$,R2    ;SET UP TO ESCAPE TO NEXT TEST
2292 010334 012777 004300 005014   MOV     #BIT11,2DHSCR ;MASTER CLEAR INTERFACE
2293
2294 010342 004767 004716      JSR     PC,CLEAR  ;TO SET ALL TBMT BITS
2295
2296 010346 004767 004744      JSR     PC,LOAD   ;CLEAR ALL BYTE COUNT AND
2297 010352 012777 000004 005010   MOV     #4,2DHBAR ;BUS ADDRESS MEMORY LOCATIONS
2298 010360 005777 004772      3$: TST    2DHSCR  ;SET ALL BYTE COUNT LOCATIONS TO -1
2299 010364 100375      BPL     3$        ;SET BAR BIT FOR LINE 2
2300 010366 012700 000020      MOV     #20,R0    ;WAIT FOR TRANSMITTER DONE
2301 010372 005077 004760      CLR     2DHSCR
2302 010376 005001      CLR     R1
2303 010400 012705 177777      4$: MOV     #-1,R5  ;SET UP TO CHECK ALL 16 LINES
2304
2305 010404 005003      CLR     R3        ;START AT LINE 0
2306
2307 010406 017704 004754      MOV     2DHBC,R4  ;KEEP TRACK OF LINE NUMBER
2308 010412 017702 004746      MOV     2DHBA,R2  ;(R5)=EXPECTED BYTE COUNT,
2309 010416 027727 004734 000002   CMP     2DHSCR,#2 ;IF LINE NUMBER NOT = 2
2310 010424 001002      BNE     5$        ;(R3)=EXPECTED BUS ADDRESS,
2311 010426 005005      CLR     R5        ;IF LINE NUMBER NOT = 2
2312 010430 005203      INC     R3        ;(R4)=ACTUAL BYTE COUNT
2313 010432 020504      5$: CMP     R5,R4   ;(R5)=ACTUAL BUS ADDRESS
2314 010434 001401      BEQ     6$        ;IF LINE BEING COMPARED IS LINE 2
2315 010436 104004      HLT     4          ;EXPECTED BYTE COUNT=0
2316 010440 020302      6$: CMP     R3,R2  ;EXPECTED BUS ADDRESS = 1
2317 010442 001401      BEQ     7$        ;IS BYTE COUNT CORRECT
2318 010444 104003      HLT     3          ;BYTE COUNT ERROR
2319 010446 005277 004704      7$: INC     2DHSCR  ;IS BUS ADDRESS CORRECT
2320 010452 005201      INC     R1
2321 010454 005300      DEC     R0        ;BUS ADDRESS ERROR
2322 010456 001350      BNE     4$        ;PREPARE TO CHECK NEXT LINE
2323 010460 104400      8$: SCOPE          ;CONTINUE IF ALL NOT DONE
2324
2325      ;NPR LOGIC TEST
  
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2326 ;SET BYTE COUNT ON ALL LINES TO 1
2327 ;SET BAR BIT FOR LINE 3
2328 ;VERIFY THAT BYTE COUNT FOR LINE 3 GOES TO 0
2329 ;VERIFY THAT BUS ADDRESS FOR LINE 3 IS INCREMENTED
2330 ;VERIFY THAT BYTE COUNTS AND BUS ADDRESSES FOR ALL OTHER LINES
2331 ;ARE UNCHANGED
2332
2333 010462 012767 000340 167306 T33: MOV #340,PS ;DISABLE ALL INTERRUPTS
2334 010470 012767 000010 004726 MOV #10,ICOUNT ;SET UP FOR 10 ITERATIONS
2335 01047E 012767 010630 004714 MOV #8$,ESCAPE ;SET UP TO ESCAPE TO NEXT TEST
2336 010504 012777 004000 004644 MOV #BIT11,JDHSCR ;MASTER CLEAR INTERFACE
2337 ;TO SET ALL TBMT BITS
2338 010512 004767 004546 JSR PC,CLEAR ;CLEAR ALL BYTE COUNT AND
2339 ;BUS ADDRESS MEMORY LOCATIONS
2340 010516 004767 004574 JSR PC,LOAD ;SET ALL BYTE COUNT LOCATIONS TO -1
2341 010522 012777 000010 004640 MOV #10,JDHBAR ;SET BAR BIT FOR LINE 3
2342 010530 005777 004622 3$: TST JDHSCR ;WAIT FOR TRANSMITTER DONE
2343 010534 100375 SP, 3$
2344 010536 012700 000020 MOV #20,R0 ;SET UP TO CHECK ALL 16 LINES
2345 010542 005077 004610 CLR JDHSCR ;START AT LINE 0
2346 010546 005001 CLR R1 ;KEEP TRACK OF LINE NUMBER
2347 010550 012705 177777 4$: MOV #-1,R5 ;(R5)=EXPECTED BYTE COUNT,
2348 ;IF LINE NUMBER NOT = 3
2349 010554 005003 CLR R3 ;(R3)=EXPECTED BUS ADDRESS.
2350 ;IF LINE NUMBER NOT = 3
2351 010556 017704 004604 MOV JDHBC,R4 ;(R4)=ACTUAL BYTE ACOUNT
2352 010562 017702 004576 MOV JDHBA,R2 ;(R5)=ACTUAL BUS ADDRESS
2353 010566 027727 004564 000003 CMP JDHSCR,#3 ;IF LINE BEING COMPARED IS LINE 3
2354 010574 001002 BNE 5$
2355 010576 005005 CLR R5 ;EXPECTED BYTE COUNT=0
2356 010600 005203 INC R3 ;EXPECTED BUS ADDRESS = 1
2357 010602 020504 5$: CMP R5,R4 ;IS BYTE COUNT CORRECT
2358 010604 001401 BEQ 6$
2359 010606 104004 HLT 4 ;BYTE COUNT ERROR
2360 010610 020302 6$: CMP R3,R2 ;IS BUS ADDRESS CORRECT
2361 010612 001401 BEQ 7$
2362 010614 104003 HLT 3 ;BUS ADDRESS ERROR
2363 010616 005277 004534 7$: INC JDHSCR ;PREPARE TO CHECK NEXT LINE
2364 010622 005201 INC R1
2365 010624 005300 DEC R0 ;CONTINUE IF ALL NOT DONE
2366 010626 001350 BNE 4$
2367 010630 104400 8$: SCOPE ;CHECK FOR ITERATIONS, LOOP
2368
2369 ;NPR LOGIC TEST
2370 ;SET BYTE COUNT ON ALL LINES TO 1
2371 ;SET BAR BIT FOR LINE 4
2372 ;VERIFY THAT BYTE COUNT FOR LINE 4 GOES TO 0
2373 ;VERIFY THAT BUS ADDRESS FOR LINE 4 IS INCREMENTED
2374 ;VERIFY THAT BYTE COUNTS AND BUS ADDRESSES FOR ALL OTHER LINES
2375 ;ARE UNCHANGED
2376
2377 010632 012767 000340 167136 T34: MOV #340,PS ;DISABLE ALL INTERRUPTS
2378 010640 012767 000010 004556 MOV #10,ICOUNT ;SET UP FOR 10 ITERATIONS
2379 010646 012767 011000 004544 MOV #8$,ESCAPE ;SET UP TO ESCAPE TO NEXT TEST
2380 010654 012777 004000 004474 MOV #BIT11,JDHSCR ;MASTER CLEAR INTERFACE
2381 ;TO SET ALL TBMT BITS
  
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2382 010662 004767 004376 JSR PC,CLEAR ;CLEAR ALL BYTE COUNT AND
2383 ;BUS ADDRESS MEMORY LOCATIONS
2384 010666 004767 004424 JSR PC,LOAD ;SET ALL BYTE COUNT LOCATIONS TO -1
2385 010672 012777 000020 004470 MOV #20,JDHBAR ;SET BAR BIT FOR LINE 4
2386 010700 005777 004452 3$: TST JDHSCR ;WAIT FOR TRANSMITTER DONE
2387 010704 100375 BPL 3$
2388 010706 012700 000020 MOV #20,R0 ;SET UP TO CHECK ALL 16 LINES
2389 010712 005077 004440 CLR JDHSCR ;START AT LINE 0
2390 010716 005001 CLR R1 ;KEEP TRACK OF LINE NUMBER
2391 010720 012705 177777 4$: MOV #-1,R5 ;(R5)=EXPECTED BYTE COUNT,
2392 ;IF LINE NUMBER NOT = 4
2393 010724 005003 CLR R3 ;(R3)=EXPECTED BUS ADDRESS,
2394 ;IF LINE NUMBER NOT = 4
2395 010726 017704 004434 MOV JDHBC,R4 ;(R4)=ACTUAL BYTE ACOUNT
2396 010732 017702 004426 MOV JDHBA,R2 ;(R5)=ACTUAL BUS ADDRESS
2397 010736 027727 004414 000004 CMP JDHSCR,#4 ;IF LINE BEING COMPARED IS LINE 4
2398 010744 001002 BNE 5$
2399 010746 005005 CLR R5 ;EXPECTED BYTE COUNT=0
2400 010750 005203 INC R3 ;EXPECTED BUS ADDRESS = 1
2401 010752 020504 5$: CMP R5,R4 ;IS BYTE COUNT CORRECT
2402 010754 001401 BEQ 6$
2403 010756 104004 HLT 4 ;BYTE COUNT ERROR
2404 010760 020302 6$: CMP R3,R2 ;IS BUS ADDRESS CORRECT
2405 010762 001401 BEQ 7$
2406 010764 104003 HLT 3 ;BUS ADDRESS ERROR
2407 010766 005277 004364 7$: INC JDHSCR ;PREPARE TO CHECK NEXT LINE
2408 010772 005201 INC R1
2409 010774 005300 DEC R0
2410 010776 001350 BNE 4$ ;CONTINUE IF ALL NOT DONE
2411 011000 104400 8$: SCOPE ;CHECK FOR ITERATIONS, LOOP
2412
2413 ;NPR LOGIC TEST
2414 ;SET BYTE COUNT ON ALL LINES TO 1
2415 ;SET BAR BIT FOR LINE 5
2416 ;VERIFY THAT BYTE COUNT FOR LINE 5 GOES TO 0
2417 ;VERIFY THAT BUS ADDRESS FOR LINE 5 IS INCREMENTED
2418 ;VERIFY THAT BYTE COUNTS AND BUS ADDRESSES FOR ALL OTHER LINES
2419 ;ARE UNCHANGED
2420
2421 011002 012767 000340 166766 T35: MOV #340,PS ;DISABLE ALL INTERRUPTS
2422 011010 012767 000010 004406 MOV #10,ICOUNT ;SET UP FOR 10 ITERATIONS
2423 011016 012767 011150 004374 MOV #8$,ESCAPE ;SET UP TO ESCAPE TO NEXT TEST
2424 011024 012777 004000 004324 MOV #BIT11,JDHSCR ;MASTER CLEAR INTERFACE
2425 ;TO SET ALL TBMT BITS
2426 011032 004767 004226 JSR PC,CLEAR ;CLEAR ALL BYTE COUNT AND
2427 ;BUS ADDRESS MEMORY LOCATIONS
2428 011036 004767 004254 JSR PC,LOAD ;SET ALL BYTE COUNT LOCATIONS TO -1
2429 011042 012777 000040 004320 MOV #40,JDHBAR ;SET BAR BIT FOR LINE 5
2430 011050 005777 004302 3$: TST JDHSCR ;WAIT FOR TRANSMITTER DONE
2431 011054 100375 BPL 3$
2432 011056 012700 000020 MOV #20,R0 ;SET UP TO CHECK ALL 16 LINES
2433 011062 005077 004270 CLR JDHSCR ;START AT LINE 0
2434 011066 005001 CLR R1 ;KEEP TRACK OF LINE NUMBER
2435 011070 012705 177777 4$: MOV #-1,R5 ;(R5)=EXPECTED BYTE COUNT,
2436 ;IF LINE NUMBER NOT = 5
2437 011074 005003 CLR R3 ;(R3)=EXPECTED BUS ADDRESS.

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2438
2439 011076 017704 004264      MOV      @DHC,R4      ; IF LINE NUMBER NOT = 5
2440 011102 017702 004256      MOV      @DHBA,R2    ; (R4)=ACTUAL BYTE ACOUNT
2441 011106 027727 004244 000005    CMP      @DHSCR,#5   ; (R5)=ACTUAL BUS ADDRESS
2442 011114 001002      BNE      5$          ; IF LINE BEING COMPARED IS LINE 5
2443 011116 005005      CLR      R5          ; EXPECTED BYTE COUNT=0
2444 011120 005203      INC      R3          ; EXPECTED BUS ADDRESS = 1
2445 011122 020504      5$:     CMP      R5,R4  ; IS BYTE COUNT CORRECT
2446 011124 001401      BEQ      6$
2447 011126 104004      HLT      4           ; BYTE COUNT ERROR
2448 011130 020302      5$:     CMP      R3,R2  ; IS BUS ADDRESS CORRECT
2449 011132 001401      BEQ      7$
2450 011134 104003      HLT      3           ; BUS ADDRESS ERROR
2451 011136 005277 004214    7$:     INC      @DHSCR ; PREPARE TO CHECK NEXT LINE
2452 011142 005201      INC      R1
2453 011144 005300      DEC      R0          ; CONTINUE IF ALL NOT DONE
2454 011146 001350      BNE      4$
2455 011150 104400      8$:     SCOPE        ; CHECK FOR ITERATIONS. LOOP
2456
2457
2458      ; NPR LOGIC TEST
2459      ; SET BYTE COUNT ON ALL LINES TO 1
2460      ; SET BAR BIT FOR LINE 6
2461      ; VERIFY THAT BYTE COUNT FOR LINE 6 GOES TO 0
2462      ; VERIFY THAT BUS ADDRESS FOR LINE 6 IS INCREMENTED
2463      ; VERIFY THAT BYTE COUNTS AND BUS ADDRESSES FOR ALL OTHER LINES
2464      ; ARE UNCHANGED
2465 011152 012767 000340 166616 736:   MOV      #340,PS    ; DISABLE ALL INTERRUPTS
2466 011160 012767 000010 004232    MOV      #10,ICOUNT ; SET UP FOR 10 ITERATIONS
2467 011166 012767 011320 004224    MOV      #8$,ESCAPE ; SET UP TO ESCAPE TO NEXT TEST
2468 011174 012777 004000 004154    MOV      #BIT11,@DHSCR ; MASTER CLEAR INTERFACE
2469
2470 011202 004767 004056      JSR      PC,CLEAR   ; TO SET ALL TBMT BITS
2471
2472 011206 004767 004104      JSR      PC,LOAD    ; CLEAR ALL BYTE COUNT AND
2473 011212 012777 000100 004150    MOV      #100,@DHBAR ; BUS ADDRESS MEMORY LOCATIONS
2474 011220 005777 004132      3$:     TST      @DHSCR  ; SET ALL BYTE COUNT LOCATIONS TO -1
2475 011224 100375      BPL      3$
2476 011226 012700 000020      MOV      #20,R0    ; SET UP TO CHECK ALL 16 LINES
2477 011232 005077 004120      CLR      @DHSCR    ; START AT LINE 0
2478 011236 005001      CLR      R1        ; KEEP TRACK OF LINE NUMBER
2479 011240 012705 177777      4$:     MOV      #-1,R5   ; (R5)=EXPECTED BYTE COUNT.
2480
2481 011244 005003      CLR      R3        ; IF LINE NUMBER NOT = 6
2482
2483 011246 017704 004114      MOV      @DHC,R4   ; (R3)=EXPECTED BUS ADDRESS.
2484 011252 017702 004106      MOV      @DHBA,R2 ; IF LINE NUMBER NOT = 6
2485 011256 027727 004074 000006    CMP      @DHSCR,#6 ; (R4)=ACTUAL BYTE ACOUNT
2486 011264 001002      BNE      5$          ; (R5)=ACTUAL BUS ADDRESS
2487 011266 005005      CLR      R5          ; IF LINE BEING COMPARED IS LINE 6
2488 011270 005203      INC      R3          ; EXPECTED BYTE COUNT=0
2489 011272 020504      5$:     CMP      R5,R4  ; EXPECTED BUS ADDRESS = 1
2490 011274 001401      BEQ      6$
2491 011276 104004      HLT      4           ; IS BYTE COUNT CORRECT
2492 011300 020302      6$:     CMP      R3,R2  ; BYTE COUNT ERROR
2493 011302 001401      BEQ      7$          ; IS BUS ADDRESS CORRECT

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2494	011304	104003				HLT	3		;BUS ADDRESS ERROR
2495	011306	005277	004044		7\$:	INC	2DHSCR		;PREPARE TO CHECK NEXT LINE
2496	011312	005201				INC	R1		
2497	011314	005300				DEC	R0		;CONTINUE IF ALL NOT DONE
2498	011316	001350				BNE	4\$		
2499	011320	104400			9\$:	SCOPE			;CHECK FOR ITERATIONS, LOOP
2500									
2501									;NPR LOGIC TEST
2502									;SET BYTE COUNT ON ALL LINES TO 1
2503									;SET BAR BIT FOR LINE 7
2504									;VERIFY THAT BYTE COUNT FOR LINE 7 GOES TO 0
2505									;VERIFY THAT BUS ADDRESS FOR LINE 7 IS INCREMENTED
2506									;VERIFY THAT BYTE COUNTS AND BUS ADDRESSES FOR ALL OTHER LINES
2507									;ARE UNCHANGED
2508									
2509	011322	012767	000340	166446	T37:	MOV	#340,PS		;DISABLE ALL INTERRUPTS
2510	011330	012767	000010	004066		MOV	#10,ICOUNT		;SET UP FOR 10 ITERATIONS
2511	011336	012767	011470	004054		MOV	#8\$,ESCAPE		;SET UP TO ESCAPE TO NEXT TEST
2512	011344	012777	004000	004004		MOV	#BIT11,2DHSCR		;MASTER CLEAR INTERFACE
2513									;TO SET ALL TBMT BITS
2514	011352	004767	003706			JSR	PC,CLEAR		;CLEAR ALL BYTE COUNT AND
2515									;BUS ADDRESS MEMORY LOCATIONS
2516	011356	004767	003734			JSR	PC,LOAD		;SET ALL BYTE COUNT LOCATIONS TO -1
2517	011362	012777	000200	004000		MOV	#200,2DHBAR		;SET BAR BIT FOR LINE 7
2518	011370	005777	003762		3\$:	TST	2DHSCR		;WAIT FOR TRANSMITTER DONE
2519	011374	100375				BPL	3\$		
2520	011376	012700	000020			MOV	#20,R0		;SET UP TO CHECK ALL 16 LINES
2521	011402	005077	003750			CLR	2DHSCR		;START AT LINE 0
2522	011406	005001				CLR	R1		;KEEP TRACK OF LINE NUMBER
2523	011410	012705	177777		4\$:	MOV	#-1,R5		; (R5)=EXPECTED BYTE COUNT,
2524									; IF LINE NUMBER NOT = 7
2525	011414	005003				CLR	R3		; (R3)=EXPECTED BUS ADDRESS,
2526									; IF LINE NUMBER NOT = 7
2527	011416	017704	003744			MOV	2DHBC,R4		; (R4)=ACTUAL BYTE ACOUNT
2528	011422	017702	003736			MOV	2DHBA,R2		; (R5)=ACTUAL BUS ADDRESS
2529	011426	027727	003724	000007		CMP	2DHSCR,#7		; IF LINE BEING COMPARED IS LINE 7
2530	011434	001002				BNE	5\$		
2531	011436	005005				CLR	R5		;EXPECTED BYTE COUNT=0
2532	011440	005203				INC	R3		;EXPECTED BUS ADDRESS = 1
2533	011442	020504			5\$:	CMP	R5,R4		;IS BYTE COUNT CORRECT
2534	011444	001401				BEQ	6\$		
2535	011446	104004				HLT	4		;BYTE COUNT ERROR
2536	011450	020302			6\$:	CMP	R3,R2		;IS BUS ADDRESS CORRECT
2537	011452	001401				BEQ	7\$		
2538	011454	104003				HLT	3		;BUS ADDRESS ERROR
2539	011456	005277	003674		7\$:	INC	2DHSCR		;PREPARE TO CHECK NEXT LINE
2540	011462	005201				INC	R1		
2541	011464	005300				DEC	R0		;CONTINUE IF ALL NOT DONE
2542	011466	001350				BNE	4\$		
2543	011470	104400			8\$:	SCOPE			;CHECK FOR ITERATIONS, LOOP
2544									
2545									;NPR LOGIC TEST
2546									;SET BYTE COUNT ON ALL LINES TO 1
2547									;SET BAR BIT FOR LINE 10
2548									;VERIFY THAT BYTE COUNT FOR LINE 10 GOES TO 0
2549									;VERIFY THAT BUS ADDRESS FOR LINE 10 IS INCREMENTED

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2550                                     :VERIFY THAT BYTE COUNTS AND BUS ADDRESSES FOR ALL OTHER LINES
2551                                     :ARE UNCHANGED
2552
2553 011472 012767 002340 166276 T40: MOV #340,PS ;DISABLE ALL INTERRUPTS
2554 011500 012767 000010 003716 MOV #10,ICOUNT ;SET UP FOR 10 ITERATIONS
2555 011506 012767 011640 003704 MOV #8$,ESCAPE ;SET UP TO ESCAPE TO NEXT TEST
2556 011514 012777 004000 003634 MOV #BIT11,ADHSCR ;MASTER CLEAR INTERFACE
2557                                     ;TO SET ALL TBMT BITS
2558 011522 004767 003536 JSR PC,CLEAR ;CLEAR ALL BYTE COUNT AND
2559                                     ;BUS ADDRESS MEMORY LOCATIONS
2560 011526 004767 003564 JSR PC,LOAD ;SET ALL BYTE COUNT LOCATIONS TO -1
2561 011532 012777 000400 003630 MOV #400,ADHBAR ;SET BAR BIT FOR LINE 10
2562 011540 005777 003612 3$: TST ADHSCR ;WAIT FOR TRANSMITTER DONE
2563 011544 100375 BPL 3$
2564 011546 012700 000020 MOV #20,R0 ;SET UP TO CHECK ALL 16 LINES
2565 011552 005077 003600 CLR ADHSCR ;START AT LINE 0
2566 011556 005001 CLR R1 ;KEEP TRACK OF LINE NUMBER
2567 011560 012705 177777 4$: MOV #-1,R5 ;(R5)=EXPECTED BYTE COUNT,
2568                                     ;IF LINE NUMBER NOT = 10
2569 011564 005003 CLR R3 ;(R3)=EXPECTED BUS ADDRESS,
2570                                     ;IF LINE NUMBER NOT = 10
2571 011566 017704 003574 MOV ADHBC,R4 ;(R4)=ACTUAL BYTE ACOUNT
2572 011572 017702 003566 MOV ADHBA,R2 ;(R5)=ACTUAL BUS ADDRESS
2573 011576 027727 003554 000010 CMP ADHSCR,#10 ;IF LINE BEING COMPARED IS LINE 10
2574 011604 000002 BNE 5$
2575 011606 005305 CLR R5 ;EXPECTED BYTE COUNT=0
2576 011610 005203 INC R3 ;EXPECTED BUS ADDRESS =
2577 011612 020504 5$: CMP R5,R4 ;IS BYTE COUNT CORRECT
2578 011614 001401 BEQ 6$
2579 011616 104004 HLT 4 ;BYTE COUNT ERROR
2580 011620 020302 6$: CMP R3,R2 ;IS BUS ADDRESS CORRECT
2581 011622 001401 BEQ 7$
2582 011624 104003 HLT 3 ;BUS ADDRESS ERROR
2583 011626 005277 003524 7$: INC ADHSCR ;PREPARE TO CHECK NEXT LINE
2584 011632 005201 INC R1
2585 011634 005300 DEC R0 ;CONTINUE IF ALL NOT DONE
2586 011636 001350 BNE 4$
2587 011640 104400 8$: SCOPE ;CHECK FOR ITERATIONS, LOOP
2588
2589                                     ;NPR LOGIC TEST
2590                                     ;SET BYTE COUNT ON ALL LINES TO 1
2591                                     ;SET BAR BIT FOR LINE 11
2592                                     ;VERIFY THAT BYTE COUNT FOR LINE 11 GOES TO 0
2593                                     ;VERIFY THAT BUS ADDRESS FOR LINE 11 IS INCREMENTED
2594                                     ;VERIFY THAT BYTE COUNTS AND BUS ADDRESSES FOR ALL OTHER LINES
2595                                     ;ARE UNCHANGED
2596
2597 011642 012767 000340 166126 T41: MOV #340,PS ;DISABLE ALL INTERRUPTS
2598 011650 012767 000010 003546 MOV #10,ICOUNT ;SET UP FOR 10 ITERATIONS
2599 011656 012767 012010 003534 MOV #8$,ESCAPE ;SET UP TO ESCAPE TO NEXT TEST
2600 011664 012777 004000 003464 MOV #BIT11,ADHSCR ;MASTER CLEAR INTERFACE
2601                                     ;TO SET ALL TBMT BITS
2602 011672 004767 003366 JSR PC,CLEAR ;CLEAR ALL BYTE COUNT AND
2603                                     ;BUS ADDRESS MEMORY LOCATIONS
2604 011676 004767 003414 JSR PC,LOAD ;SET ALL BYTE COUNT LOCATIONS TO -1
2605 011702 012777 001000 003460 MOV #1000,ADHBAR ;SET BAR BIT FOR LINE 11
  
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2606 011710 005777 003442      3$:  TST      @DHSCR          ;WAIT FOR TRANSMITTER DONE
2607 011714 100375                BPL      3$
2608 011716 012700 000020      MOV      #20,R0          ;SET UP TO CHECK ALL 16 LINES
2609 011722 005077 003430      CLR      @DHSCR        ;START AT LINE 0
2610 011726 005001                CLR      R1             ;KEEP TRACK OF LINE NUMBER
2611 011730 C12705 177777      4$:  MOV      #-1,R5        ;(R5)=EXPECTED BYTE COUNT,
2612                                ;IF LINE NUMBER NOT = 11
2613 011734 005003                CLR      R3             ;(R3)=EXPECTED BUS ADDRESS,
2614                                ;IF LINE NUMBER NOT = 11
2615 011736 017704 003424      MOV      @DHBC,R4        ;(R4)=ACTUAL BYTE ACOUNT
2616 011742 017702 003416      MOV      @DHBA,R2        ;(R5)=ACTUAL BUS ADDRESS
2617 011746 027727 003404 000011  CMP      @DHSCR,#11      ;IF LINE BEING COMPARED IS LINE 11
2618 011754 001002                SNE     5$
2619 011756 005005                CLR      R5             ;EXPECTED BYTE COUNT=0
2620 011760 005203                INC      R3             ;EXPECTED BUS ADDRESS = 1
2621 011762 020504                5$:  CMP      R5,R4          ;IS BYTE COUNT CORRECT
2622 011764 001401                BEQ     6$
2623 011766 104004                HLT     4
2624 011770 020302                6$:  CMP      R3,R2          ;BYTE COUNT ERROR
2625 011772 001401                BEQ     7$             ;IS BUS ADDRESS CORRECT
2626 011774 104003                HLT     3
2627 011776 005277 003354      7$:  INC      @DHSCR        ;BUS ADDRESS ERROR
2628 012002 005201                INC     R1             ;PREPARE TO CHECK NEXT LINE
2629 012004 005300                DEC     R0
2630 012006 001350                BNE     4$            ;CONTINUE IF ALL NOT DONE
2631 012010 104400                8$:  SCOPE              ;CHECK FOR ITERATIONS. LOOP
2632
2633                                ;NPR LOGIC TEST
2634                                ;SET BYTE COUNT ON ALL LINES TO 1
2635                                ;SET BAR BIT FOR LINE 12
2636                                ;VERIFY THAT BYTE COUNT FOR LINE 12 GOES TO 0
2637                                ;VERIFY THAT BUS ADDRESS FOR LINE 12 IS INCREMENTED
2638                                ;VERIFY THAT BYTE COUNTS AND BUS ADDRESSES FOR ALL OTHER LINES
2639                                ;ARE UNCHANGED
2640
2641 012012 012767 000340 165756 T42:  MOV      #340,PS        ;DISABLE ALL INTERRUPTS
2642 012020 012767 000010 003376      MOV      #10,ICOUNT     ;SET UP FOR 10 ITERATIONS
2643 012026 012767 012160 003364      MOV      #8$,ESCAPE     ;SET UP TO ESCAPE TO NEXT TEST
2644 012034 012777 004000 003314      MOV      #BIT11,@DHSCR  ;MASTER CLEAR INTERFACE
2645                                ;TO SET ALL TBMT BITS
2646 012042 004767 003216                JSR     PC,CLEAR        ;CLEAR ALL BYTE COUNT AND
2647                                ;BUS ADDRESS MEMORY LOCATIONS
2648 012046 004767 003244                JSR     PC,LOAD         ;SET ALL BYTE COUNT LOCATIONS TO -1
2649 012052 012777 002000 003310      MOV      #2000,@DHBAR   ;SET BAR BIT FOR LINE 12
2650 012060 005777 003272                3$:  TST      @DHSCR        ;WAIT FOR TRANSMITTER DONE
2651 012064 100375                BPL     3$
2652 012066 012700 000020      MOV      #20,R0          ;SET UP TO CHECK ALL 16 LINES
2653 012072 005077 003260      CLR      @DHSCR        ;START AT LINE 0
2654 012076 005001                CLR     R1             ;KEEP TRACK OF LINE NUMBER
2655 012100 012705 177777      4$:  MOV      #-1,R5        ;(R5)=EXPECTED BYTE COUNT,
2656                                ;IF LINE NUMBER NOT = 12
2657 012104 005003                CLR     R3             ;(R3)=EXPECTED BUS ADDRESS,
2658                                ;IF LINE NUMBER NOT = 12
2659 012106 017704 003254      MOV      @DHBC,R4        ;(R4)=ACTUAL BYTE ACOUNT
2660 012112 017702 003246      MOV      @DHBA,R2        ;(R5)=ACTUAL BUS ADDRESS
2661 012116 027727 003234 000012  CMP      @DHSCR,#12      ;IF LINE BEING COMPARED IS LINE 12
  
```



```

012736 005001          CLR      R1          :KEEP TRACK OF LINE NUMBER
012740 012705 177777 45:  MOV      #-1,R5      : (R5)=EXPECTED BYTE COUNT,
                                : IF LINE NUMBER NOT = 16
012744 005003          CLR      R3          : (R3)=EXPECTED BUS ADDRESS,
                                : IF LINE NUMBER NOT = 16
012746 017704 002414          MOV      2DHBC,R4      : (R4)=ACTUAL BYTE COUNT
012750 017702 002406          MOV      2DHBA,R2      : (R5)=ACTUAL BUS ADDRESS
012752 027727 002374 000016  CMP      2DHSCR,#16    : IF LINE BEING COMPARED IS LINE 16
012756 001002          BNE      55          :EXPECTED BYTE COUNT=0
012760 005005          CLR      R5          :EXPECTED BUS ADDRESS = 1
012764 005203          INC      R3          :IS BYTE COUNT CORRECT
012768 020504 55:  CMP      R5,R4
012772 001401          BEQ      65          :BYTE COUNT ERROR
012776 004004          HLT     4           :IS BUS ADDRESS CORRECT
013000 020302 55:  CMP      R3,R2
013002 001401          BEQ      75          :BUS ADDRESS ERROR
013004 104003          HLT     3           :PREPARE TO CHECK NEXT LINE
013006 005277 002344 75:  INC      2DHSCR
013012 005201          INC      R1
013014 005300          DEC      R0          :CONTINUE IF ALL NOT DONE
013016 001350          BNE      45
013020 104400 55:  SCOPE          :CHECK FOR ITERATIONS, LOOP

:NPR LOGIC TEST
:SET BYTE COUNT ON ALL LINES TO 1
:SET BAR BIT FOR LINE 17
:VERIFY THAT BYTE COUNT FOR LINE 17 GOES TO 0
:VERIFY THAT BUS ADDRESS FOR LINE 17 IS INCREMENTED
:VERIFY THAT BYTE COUNTS AND BUS ADDRESSES FOR ALL OTHER LINES
:ARE UNCHANGED

013022 012767 000340 164746 T47: MOV      #340,PS      :DISABLE ALL INTERRUPTS
013030 012767 000010 002366  MOV      #10,COUNT    :SET UP FOR 10 ITERATIONS
013036 012767 013170 002354  MOV      #85,ESCAPE   :SET UP TO ESCAPE TO NEXT TEST
013044 012777 004000 002304  MOV      #BIT11,2DHSCR :MASTER CLEAR INTERFACE
                                :TO SET ALL TBMT BITS
013052 004767 002206          JSR     PC,CLEAR      :CLEAR ALL BYTE COUNT AND
                                :BUS ADDRESS MEMORY LOCATIONS
013056 004767 002234          JSR     PC,LOAD       :SET ALL BYTE COUNT LOCATIONS TO -1
013062 012777 100000 002300  MOV      #10000,2DH-BAR :SET BAR BIT FOR LINE 17
013070 005777 002262 35:  TST     2DHSCR        :WAIT FOR TRANSMITTER DONE
013074 100375          BPL     35
013076 012700 000020          MOV      #20,R0      :SET UP TO CHECK ALL 16 LINES
013102 005077 002250          CLR     2DHSCR       :START AT LINE 0
013106 005001          CLR     R1          :KEEP TRACK OF LINE NUMBER
013110 012705 177777 45:  MOV      #-1,R5      : (R5)=EXPECTED BYTE COUNT,
                                : IF LINE NUMBER NOT = 17
013114 005003          CLR     R3          : (R3)=EXPECTED BUS ADDRESS,
                                : IF LINE NUMBER NOT = 17
013116 017704 002244          MOV      2DHBC,R4      : (R4)=ACTUAL BYTE COUNT
013122 017702 002236          MOV      2DHBA,R2      : (R5)=ACTUAL BUS ADDRESS
013126 027727 002224 000017  CMP      2DHSCR,#17    : IF LINE BEING COMPARED IS LINE 17
013134 001002          BNE     55
013136 005005          CLR     R5          :EXPECTED BYTE COUNT=0
013140 005203          INC     R3          :EXPECTED BUS ADDRESS = 1
013142 020504 55:  CMP      R5,R4      :IS BYTE COUNT CORRECT

```

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0013144 001401
0013145 104004
0013150 020302
0013151 001401
0013152 104004
0013153 005277
0013154 005201
0013155 005301
0013156 005301
0013157 005301
0013158 005301
0013159 005301
0013160 104400

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002:74

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65: BEQ 65
    HLT 4
    CMP R3,R2
75: BEQ 65
    HLT 4
    INC 20HSCR
    INC R1
    DEC R2
85: BNE 48
    SCOPE

```

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:BYTE COUNT ERROR
:IS BUS ADDRESS CORRECT
:BUS ADDRESS ERROR
:PREPARE TO CHECK NEXT LINE
:CONTINUE IF ALL NOT DONE
:CHECK FOR ITERATIONS, LOOP

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013172	012767	000340	164576	T50:	MOV	#340,PS	:DISABLE ALL INTERRUPTS
013200	012767	000010	002216		MOV	#10,ICOUNT	:SET UP FOR 10 ITERATIONS
013206	012767	013350	002204		MOV	#5\$,ESCAPE	:SET UP TO ESCAPE TO NEXT TEST
013214	012777	004000	002134		MOV	#BIT11,JDHSCR	:MASTER CLEAR INTERFACE
013222	012777	013270	002150		MOV	#2\$,JDHARVEC	:SET UP RECEIVER INTERRUPT
013230	012777	000340	002144		MOV	#340,JDHPLVL	:VECTOR AND STATUS
013236	052777	100000	002130		BIS	#BIT15,JDHSSR	:SET SILO MAINTENANCE
013244	012777	000100	002104		MOV	#BIT06,JDHSCR	:SET RECEIVER INTERRUPT ENABLE
013252	005067	164520			CLR	PS	:ALLOW INTERRUPTS
013256	012700	001000			MOV	#1000,R0	:SET UP DELAY FOR SILO LOAD
013262	005300			1\$:	DEC	RC	:DELAY FOR SILO LOAD
013264	001376				BNE	1\$	
013266	104001				HLT	1	:NO CHARACTER AVAILABLE INTERRUPT OCCURED
013270	042777	100000	002076	2\$:	BIC	#BIT15,JDHSSR	:CLEAR SILO MAINTENANCE BIT
013276	105777	002054			TSTB	JDHSCR	:IS CHARACTER AVAILABLE BIT SET
013302	100401				BMI	3\$	
013304	104005				HLT	5	:CHARACTER AVAILABLE NOT, ERROR
013306	017703	002062		3\$:	MOV	JDHSSR,R3	:READ SILO STATUS REGISTER
013312	017704	002042			MOV	JDHNR,R4	: (R4)=ACTUAL DATA IN NEXT
							:RECEIVED CHARACTER REGISTER
013316	012705	125252			MOV	#125252,R5	: (R5)=EXPECTED DATA IN
							:NEXT RECEIVED CHARACTER REGISTER
013322	020504				CMP	R5,R4	:IS DATA IN SILO CORRECT
013324	001401				BEQ	4\$	
013326	104006				HLT	6	:SILO DATA ERROR
013330	010304			4\$:	MOV	R3,R4	:GET SILO STATUS REGISTER
013332	042704	000300			BIC	#300,R4	:CLEAR UNWANTED BITS
013336	012705	000400			MOV	#400,R5	: (R5)=EXPECTED DATA
							:IN SILO STATUS REGISTER
013342	020504				CMP	R5,R4	:CHECK RESULTS
013344	001401				BEQ	5\$	
013346	104007				HLT	7	:SILO STATUS ERROR
013350	012706	017102		5\$:	MOV	#STACK,SP	:RESTORE STACK
013354	104400				SCOPE		:CHECK FOR ITERATIONS, LOOP

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013356	012767	000340	164412	T51:	MOV	#340,PS	:DISABLE ALL INTERRUPTS
013364	012767	000001	002032		MOV	#1,ICOUNT	:SET UP FOR 1 ITERATIONS
013372	012767	013510	002020		MOV	#5\$,ESCAPE	:SET UP TO ESCAPE TO NEXT TEST
013400	012767	013412	002014		MOV	#13,FREEZ1	:SET UP TO LOOP WITH DATA
013406	012701	000001			MOV	#1,R1	:SET UP TO LOAD SILO WITH 1 CHARACTER

```

;SILO LOGIC TEST (MAINTENANCE MODE)
;FORCE 1 CHARACTER INTO SILO USING SILO
;MAINTENANCE BIT
;VERIFY THAT CHARACTER AVAILABLE INTERRUPT OCCURS
;VERIFY THAT CHARACTER AVAILABLE BIT IS
;SET IN SYSTEM CONTROL REGISTER
;VERIFY THAT SILO FILL REGISTER INCREMENTS TO 1
;VERIFY THAT NEXT RECEIVED CHARACTER REGISTER
;VALID DATA BIT IS SET
;VERIFY THAT CORRECT DATA PATTERN WAS RECEIVED
    
```

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2952 013412 012777 004000 001736 1$: MOV #BIT11,2DHSCR ;MASTER CLEAR INTERFACE
2953 013420 010100 MOV R1,R0 ;SAVE COUNT
2954 013422 005005 CLR R5 ;WILL BE COUNT OF CHARACTERS LOADED
2955 013424 052777 100000 001742 2$: BIS #BIT15,2DHSSR ;LOAD A CHARACTER
2956 013432 012702 001000 MOV #1000,R2 ;STALL FOR SILO
2957 013436 005302 3$: DEC R2
2958 013440 001376 SNE 3$
2959 013442 042777 100000 001724 BIC #BIT15,2DHSSR ;CLEAR LOAD BIT
2960 013450 005205 INC R5 ;UPDATE COUNT OF CHARACTERS LOADED
2961 013452 005300 DEC R0 ;IF ALL CHARACTERS NOT LOADED
2962 013454 001363 BNE 2$ ;LOAD ANOTHER
2963 013456 017704 001712 MOV 2DHSSR,R4 ;READ SILO STATUS REGISTER
2964 013462 042704 000300 BIC #300,R4 ;CLEAR UNWANTED BITS
2965 013466 000304 SWAB R4 ;GET DATA INTO LOW BYTE
2966 013470 020504 CMP R5,R4 ;COMPARE
2967 013472 001401 BEQ 4$
2968 013474 104007 HLT 7 ;SILO STATUS ERROR
2969 013476 104410 4$: SCOPE1 ;CHECK FOR LOOP WITH CURRENT
2970 ;LOAD COUNT (R5)
2971 013500 005201 INC R1 ;ADD 1 TO NUMBER OF CHARACTERS
2972 ;TO BE LOADED INTO SILO
2973 013502 022701 000100 CMP #100,R1 ;CONTINUE UNTIL SILO IS FULL
2974 013506 001341 BNE 1$
2975 013510 104400 5$: SCOPE
2976
2977 ;SILO LOGIC TEST (MAINTENANCE MODE)
2978 ;LOAD 64 (DECIMAL CHARACTERS INTO SILO)
2979 ;READ CHARACTERS OUT OF SILO
2980 ;VERIFY THAT SILO STATUS REGISTER COUNTS DOWN CORRECTLY
2981
2982 013512 012767 000340 164256 T52: MOV #340,PS ;DISABLE ALL INTERRUPTS
2983 013520 012767 000001 001676 MOV #1,ICOUNT ;SET UP FOR 1 ITERATIONS
2984 013526 012767 013670 001664 MOV #7$,ESCAPE ;SET UP TO ESCAPE TO NEXT TEST
2985 013534 012767 013546 001660 MOV #1$,FREEZI ;SET UP TO LOOP WITH DATA
2986 013542 012701 000001 MOV #1,R1 ;SET UP TO READ 1 CHARACTER
2987 013546 012777 004000 001602 1$: MOV #BIT11,2DHSCR ;MASTER CLEAR INTERFACE
2988 013554 012705 000100 MOV #100,R5 ;SILO STATUS COUNT SHOULD BE
2989 013560 160105 SUB R1,R5 ;100(OCTAL)-NUMBER
2990 ;OF CHARACTERS READ
2991 013562 012700 000100 MOV #100,R0 ;SET UP TO LOAD SILO
2992 013566 012702 001000 2$: MCV #1000,R2 ;SET UP DELAY
2993 013572 052777 100000 001574 BIS #BIT15,2DHSSR ;LOAD 1 CHARACTER
2994 013600 005302 3$: DEC R2 ;DELAY
2995 013602 001376 BNE 3$
2996 013604 042777 100000 001562 BIC #BIT15,2DHSSR ;CLEAR SILO LOAD BIT
2997 013612 005300 DEC R0 ;CONTINUE IF SILO NOT FULL
2998 013614 001364 BNE 2$
2999 013616 010100 MOV R1,R0 ;SET UP TO READ SILO
3000 013620 012702 001000 4$: MOV #1000,R2 ;SET UP DELAY FOR SILO
3001 013624 005777 001530 TST 2DHNR0 ;READ SILO
3002 013630 005302 5$: DEC R2 ;DELAY FOR SILO
3003 013632 001376 BNE 5$
3004 013634 005300 DEC R0 ;UPDATE NUMBER OF CHARACTER S TO BE READ
3005 013636 001370 BNE 4$ ;CONTINUE READING
3006 013640 117704 001532 MOVB 2DHSLR,R4 ;READ SILO STATUS REGISER
3007 013644 042704 000300 BIC #300,R4 ;CLEAR UNWANTED BITS
    
```

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3010
3011
3012 013650 020504
3013 013652 001401
3014 013654 104007
3015 013656 104410
3016 013660 005201
3017 013662 020127 000101
3018 013666 001327
3019 013670 104400

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```

        CMP      R5,R4
        BEQ      65
        HLT      7
65:     SCOPE1
        INC      R1
        CMP      R1,#101
        BNE     15
75:     SCOPE

```

```

;(R5)=EXPECTED SILO STATUS
;(IN UPPER BYTE)
;(R4)=ACTUAL SILO STATUS
;(IN UPPER BYTE)
;COMPARE EXPECTED AND RECEIVED DATA

;SILO STATUS ERROR
;CHECK FOR LOOP WITH SAME READ COUNT
;UPDATE COUNT OF CHARACTERS TO BE READ
;CONTINUE IF NOT DONE

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3020
3021      :SILO LOGIC TEST (MAINTENANCE MODE)
3022      :SET SILO ALARM LEVEL TO ALL VALUFS 0-77
3023      :VERIFY THAT CHARACTER AVAILABLE FLAG
3024      :DOES NOT SET UNTIL SILO FILL LEVEL IS GREATER THAN
3025      :SILO ALARM LEVEL
3026
3027 013672 012767 000340 164076 T53:  MOV    #340,PS      ;DISABLE ALL INTERRUPTS
3028 013700 012767 000040 001516      MOV    #40,ICOUNT  ;SET UP FOR 40 ITERATIONS
3029 013706 012767 014046 001504      MOV    #5$,ESCAPE ;SET UP TO ESCAPE TO NEXT TEST
3030 013714 012767 013724 001500      MOV    #1$,FREEZ1 ;SET UP TO LOOP WITH DATA
3031 013722 005005                CLR    R5          ;START AT ALARM LEVEL 0
3032 013724 012777 004000 001424 1$:  MOV    #BIT11,JDHSCR ;MASTERCLEAR INTERFACE
3033 013732 010577 001436                MOV    R5,JDHSSR  ;SET ALARM LEVEL
3034 013736 010501                MOV    R5,R1      ;SET FILL COUNT
3035 013740 005201                INC    R1          ;ONE MORE THAN ALARM LEVEL
3036 013742 052777 100000 001424 2$:  BIS    #BIT15,JDHSSR ;LOAD A CHARACTER
3037 013750 012700 001000                MOV    #1000,R0   ;WAIT FOR SILO TO SETTLE
3038 013754 005300                DEC    R0
3039 013756 001376                BNE    .-2
3040 013760 042777 100000 001406      BIC    #BIT15,JDHSSR ;CLEAR MAINTENANCE BIT
3041 013766 005301                DEC    R1          ;UPDATE FILL COUNT
3042 013770 105777 001362                TSTB   JDHSCR     ;IS CHARACTER AVAILABLE FLAG SET
3043 013774 100406                BMI    3$         ;YES
3044 013776 005701                TST   R1          ;CHARACTER AVAILALBE FLAG NOT SET
3045 014000 001360                BNE    2$         ;SHOULD IT BE
3046 014002 117703 001370                MOVB  JDHSLR,R3   ;READ SILO FILL LEVEL
3047 014006 104010                HLT   10          ;SILO ALARM ERPOP
3048                                ;NO CHARACTER AVAILABLE WHEN EXPECTED
3049 014010 000406                BR    4$
3050 014012 020127 000001 3$:      CMP    R1,#1
3051 014016 003403                BLE   4$
3052 014020 117703 001352                MOVB  JDHSLR,R3   ;READ SILO FILL LEVEL
3053 014024 104010                HLT   10          ;SILO ALARM ERROR
3054 014026 104410                4$:  SCOPE1          ;CHECK FOR FREEZE AT CURRENT ALARM LEVEL
3055 014030 005705                TST   R5
3056 014032 001001                BNE   10$
3057 014034 000261                SEC
3058 014036 006105                10$: ROL    R5      ;GO TO NEXT ALARM LEVEL
3059 014040 022705 000100                CMP    #100,R5   ;CONTINUE IF NOT DONE
3060 014044 001327                BNE   1$
3061 014046 104430                5$:  SCOPE

```

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3062
3063
3064 ;END OF PASS
3065 ;TYPE NAME OF TEST
3066 ;UPDATE PASS COUNT
3067 ;CHECK FOR EXIT TO ACT-11
3068 ;RESTART TEST
3069
3070 014050 104401 EOP: TYPE ;TYPE NAME OF TEST
3071 014052 016055 MEPASS
3072 014054 005067 001374 CLR LAST ;CLEAR LAST ERROR PC
3073 014060 005067 001324 CLR ERRFLG ;CLEAR ERROR FLAG
3074 014064 005267 001322 INC PASCNT ;UPDATE PASS COUNT
3075 014070 016767 001316 163472 MOV PASCNT,LIGHTS ;DISPLAY PASS COUNT
3076 014076 013701 000042 MOV #42,R1 ;CHECK FOR ACT-11 OR DDP
3077 014102 001405 BEQ RESTRT ;IF NOT, CONTINUE TESTING
3078 014104 000005 RESET
3079 014106 004711 LOGICAL: JSR PC,(R1)
3080 014110 000240 NOP
3081 014112 000240 NOP
3082 014114 000240 NOP
3083 014116 000167 165120 RESTRT: JMP BEGIN
3084
3085 ;CHECK FOR LOOP ON CURRENT TEST
3086 ;CHECK FOR ITERATION SUPPRESSION
3087
3088 014122 032767 002000 163440 SCOPER: BIT #SW10,SWR
3089 014130 001030 BNE 4$
3090 014132 032767 040000 163430 1$: BIT #SW14,SWR
3091 014140 001021 BNE 3$
3092 014142 032767 004000 163420 BIT #SW11,SWR
3093 014150 001006 BNE 2$
3094 014152 005267 001250 INC LPCNT
3095 014156 026767 001244 001240 CMP LPCNT,ICOUNT
3096 014164 001007 BNE 3$
3097 014166 005067 001234 2$: CLR LPCNT
3098 014172 005067 001212 CLR ERRFLG
3099 014176 011667 001214 MOV (SP),RETURN
3100 014202 000002 RTI
3101 014204 016716 001206 3$: MOV RETURN,(SP)
3102 014210 000002 RTI
3103 014212 005767 001172 4$: TST ERRFLG
3104 014216 001745 BEQ 1$
3105 014220 000762 BR 2$
3106
3107 ;CHECK FOR FREEZE ON CURRENT DATA
3108
3109 014222 032767 001000 163340 SCOP1R: BIT #SW09,SWR
3110 014230 001402 BEQ 1$
3111 014232 016716 001164 MOV FREEZ1,(SP)
3112 014236 000002 1$: RTI
3113
3114 ;ERROR HANDLER
3115
3116 014240 032767 020000 163322 ERRORS: BIT #SW13,SWR
3117 014246 001051 BNE HALTS

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3118	014250	021567	001200		CMP	(SP),LAST	
3119	014254	001404			BEQ	1\$	
3120	014256	011667	001172		MOV	(SP),LAST	
3121	014262	005067	001122		CLR	ERRFLG	
3122	014266	104406		1\$:	SAVOSP		
3123	014270	011605			MOV	(SP),R5	
3124	014272	162705	000002		SUB	#2,R5	
3125	014276	011504			MOV	(R5),R4	
3126	014300	006304			ASL	R4	
3127	014302	006304			ASL	R4	
3128	014304	042704	177001		BIC	#177001,R4	
3129	014310	062704	016164		ADD	#ERRTAB,R4	
3130	014314	012467	000034		MOV	(R4)+,ERRMSG	
3131	014320	011467	000042		MOV	(R4),DATABP	
3132	014324	005767	001060		TST	ERRFLG	
3133	014330	001403			BEQ	TYPMSG	
3134	014332	005767	000030		TST	DATABP	
3135	014335	001007			BNE	TYPDAT	
3136	014340	104402		TYPMSG:	OCTASC		
3137	014342	014434			ERTABO		
3138	014344	012767	000001	001036	MOV	#1,ERRFLG	
3139	014352	104401			TYPE		
3140	014354	000000		ERRMSG:	0		
3141	014356	005767	000004		TYPDAT:	TST	DATABP
3142	014362	001402			BEQ	RESREG	
3143	014364	104402			OCTASC		
3144	014366	000000		DATABP:	0		
3145	014370	104407		RESREG:	RES05		
3146	014372	005767	163172	HALTS:	TST	SWR	
3147	014376	100005			BPL	EXITER	
3148	014400	010046			PUSHRO		
3149	014402	016600	000002		MOV	2(SP),RO	
3150	014406	000000			HALT		
3151	014410	012600			POPRO		
3152	014412	005267	000776	EXITER:	INC	ERPCNT	
3153	014416	032767	002000	163144	BIT	#SW10,SWR	
3154	014424	001402			BEQ	1\$	
3155	014426	016716	000766		MOV	ESCAPE,(SP)	
3156	014432	000002		1\$:	RTI		
3157	014434	000001		ERTABO:	1		
3158	014436	006	002		.BYTE	6,2	
3159	014440	015446			SAVPC		
3160					;TRAP DISPATCH SERVICE		
3161					;ARGUMENT OF TRAP IS EXTRACTED		
3162					;AND USED AS OFFSET TO OBTAIN POINTER		
3163					;TO SELECTED SUBROUTINE		
3164							
3165	014442	011646		TRPSRV:	MOV	(SP),-(SP)	;GET PC OF RETURN
3166	014444	162716	000002		SUB	#2,(SP)	;=PC OF TRAP
3167	014450	017616	000000		MOV	2(SP),(SP)	;GET TRP
3168	014454	006316		TRPOK:	ASL	(SP)	;MULTIPLY TRAP ARG BY 2
3169	014456	042716	177001		BIC	#177001,(SP)	;CLEAR UNWANTED BITS
3170	014462	062716	016104		ADD	#TRPTAB,(SP)	;POINTER TO SUBROUTINE ADDRESS
3171	014466	017616	000000		MOV	2(SP),(SP)	;SUBROUTINE ADDRESS
3172	014472	000136			JMP	2(SP)+	;GO TO SUBROUTINE
3173							

```

3174                                     ; TELETYPE OUTPUT ROUTINE
3175
3176 014474 017605 000000          TYPBR:  MOV    2(SP),R5
3177 014500 062716 000002          ADD    #2,(SP)
3178 014504 105777 000642          1$:   TSTB  2TPCSR
3179 014510 100375                   BPL    1$
3180 014512 105715                   TSTB  (R5)
3181 014514 001001                   BNE   2$
3182 014516 000002                   RTI
3183 014520 112577 000630          2$:   MOVB  (R5)+,2TPDBR
3184 014524 000767                   BR    1$
  
```

```

3185                                     ; ASCII STRING INPUT ROUTINE
3186
3187
3188 014526 017667 000000 000006  INSTRG: MOV    2(SP),MSG
3189 014534 062716 000002          ADD    #2,(SP)
3190 014540 104401          INSTR1: TYPE
3191 014542 000000          MSG:   0
3192 014544 012704 016126          MOV    #INBUF,R4
3193 014550 012703 000007          MOV    #7,R3
3194 014554 105777 000566          1$:   TSTB  2TKCSR
3195 014560 100375                   BPL    1$
3196 014562 117714 000562          MOVB  2TKDBR,(R4)
3197 014566 142714 000200          BICB  #200,(R4)
3198 014572 122427 000015          CMPB  (R4)+,#15
3199 014576 001413          BEQ   INSTR2
3200 014600 117777 000544 000546  MOVB  2TKDBR,2TPDBR
3201 014606 105777 000540          2$:   TSTB  2TPCSR
3202 014612 100375                   BPL    2$
3203 014614 005303                   DEC    R3
3204 014616 001356                   BNE   1$
3205 014620 104401          INSTRE: TYPE
3206 014622 015761          MQM
3207 014624 000745          BR    INSTR1
3208 014626 000002          INSTR2: RTI
  
```

```

3209                                     ; CONVERT ASCII STRING TO OCTAL
3210
3211
3212 014630 011605          PARAMS: MOV    (SP),R5
3213 014632 012567 000146          MOV    (R5)+,LOLIM
3214 014636 012567 000144          MOV    (R5)+,HILIM
3215 014642 012567 000142          MOV    (R5)+,DEVADR
3216 014646 112567 000140          MOVB  (R5)+,LOBITS
3217 014652 112567 000135          MOVB  (R5)+,ADRCNT
3218 014656 010516          MOV    R5,(SP)
3219 014660 005005          PARAM1: CLR   R5
3220 014662 012704 016126          MOV    #INBUF,R4
3221 014666 122714 000015          CMPB  #15,(R4)
3222 014672 001420          BEQ   PARERR
3223 014674 121427 000060          1$:   CMPB  (R4),#60
3224 014700 002415          BLT   PARERR
3225 014702 121427 000067          CMPB  (R4),#67
3226 014706 003012          BGT   PARERR
3227 014710 142714 000060          BICB  #60,(R4)
3228 014714 152405          BISB  (R4)+,R5
3229 014716 122714 000015          CMPB  #15,(R4)
  
```

3230	014722	001406		BEQ	LIMITS
3231	014724	006305		ASL	R5
3232	014726	006305		ASL	R5
3233	014730	006305		ASL	R5
3234	014732	000760		BR	1\$
3235	014734	104404		PARERR: INSTER	
3236	014736	000750		BR	PARAM1
3237					
3238					;TEST TO SEE IF NUMBER IS WITHIN LIMITS
3239					
3240	014740	020567	000042	LIMITS: CMP	R5, HILIM
3241	014744	101373		BHI	PARERR
3242	014746	020567	000032	CMP	R5, LOLIM
3243	014752	103770		BLO	PARERR
3244	014754	136705	000032	BITB	LOBITS, R5
3245	014760	001365		BNE	PARERR
3246					
3247					:STORE NUMBER AT SPECIFIED ADDRESS
3248					
3249	014762	016704	000022	1\$: MOV	DEVADR, R4
3250	014766	010524		MOV	R5, (R4)+
3251	014770	062705	000002	ADD	#2, R5
3252	014774	105367	000013	DECB	ADRCNT
3253	015000	001372		BNE	1\$
3254	015002	000902		RTI	
3255	015004	000900		LOLIM: 0	
3256	015006	000900		HILIM: 0	
3257	015010	000900		DEVADR: 0	
3258	015012	000900		LOBITS: 0	
3259		015013		ADRCNT=LOBITS+1	
3260					
3261					;CONVERT OCTAL NUMBER TO ASCII AND OUTPUT TO TELEPRINTER
3262					
3263	015014	104401		OCTASN: TYPE	
3264	015016	015765		MCRLF	
3265	015020	017601	000000	MOV	@(SP), R1
3266	015024	062716	000002	ADD	#2, (SP)
3267	015030	012167	000130	MOV	(R1)+, WRDCNT
3268	015034	112167	000126	1\$: MOVB	(R1)+, CHRCNT
3269	015040	112167	000123	MOVB	(R1)+, SPACNT
3270	015044	013167	000120	MOV	@(R1)+, BINWRD
3271	015050	016704	000114	2\$: MOV	BINWRD, R4
3272	015054	116705	000106	MOVB	CHRCNT, R5
3273	015060	012700	01614C	MOV	#TEMP, R0
3274	015064	010403		3\$: MOV	R4, R3
3275	015066	042703	177770	BIC	#177770, R3
3276	015072	062703	000260	ADD	#260, R3
3277	015076	110320		MOVB	R3, (R0)+
3278	015100	006204		ASR	R4
3279	015102	006204		ASR	R4
3280	015104	006204		ASR	R4
3281	015106	005305		DEC	R5
3282	015110	001365		BNE	3\$
3283	015112	012703	016152	4\$: MOV	#MDATA, R3
3284	015116	114023		MOVB	-(R0), (R3)+
3285	015120	105367	000042	DECB	CHRCNT

015511 PFC

```

015508 012767 015516 1623.2 MOV #RESTART,24 ;SET UP FOR POWER UP TRAP
015512 000000 HALT ;HALT ON POWER DOWN NORMAL
015514 000000 BR .

;PROCESSOR WILL TRAP HERE WHEN POWER IS RESTORED

015516 016706 177722 RESTAR: MOV SAVSP,SP ;RESTORE STACK POINTER
015518 012605 MOV (SP)+,R5 ;RESTORE R0-R5
015520 012604 MOV (SP)+,R4
015522 012603 MOV (SP)+,R3
015524 012602 MOV (SP)+,R2
015526 012601 MOV (SP)+,R1
015528 012600 MOV (SP)+,R0
015530 012767 015460 162250 MOV #PFAIL,24 ;SET UP FOR POWER FAILURE
015532 012767 000340 MOV #340,R5
015534 012767 017102 MOV #STACK,SP
015536 005067 000356 CLR TEMP
015538 005267 000352 INC TEMP
015540 001375 BNE .-4
015542 104402 OCTASC
015544 015614 PFTAB
015546 104401 TYPE
015548 015770 MPFAIL
015550 005067 177604 CLR ERRFLG
015552 005067 177644 CLR LAST
015554 000177 177602 JMP #RETURN
015556 000001 PFTAB: 1
015558 000006 6
015560 000207 2
015562 005015 042012 030510 MTITLE: .ASCIZ <15><12><12>/CH11 TRANSMITTER AND RECEIVER LOGIC TEST <15><12>
015564 020061 051124 047101
015566 046523 052111 042524
015568 020122 047101 020104
015570 042522 042503 053111
015572 051105 046040 043517
015574 041511 052040 051505
015576 020124 005015 000
015578 015 053012 041505 MVECT0: .ASCIZ <15><12>/VECTOR ADDRESS-
015580 047524 020122 042101
015582 051104 051505 026523
015584 000
015586 015 041412 047117 MREGAD: .ASCIZ <15><12>/CONTROL REGISTER ADDRESS-
015588 051124 046117 051040
015590 043505 051511 042524
015592 020122 042101 051104
015594 051505 026523 000
015596 040 037440 000
015598 015 000012
015600 020040 047520 042527 MQM: .ASCIZ / ?
015602 020122 040506 046111 MCRLF: .ASCIZ <15><12>
015604 051125 026105 050040 MPFAIL: .ASCIZ / POWER FAILURE, PROGRAM RESTART AT TEST IN PROGRESS
015606 047522 051107 046501
015608 051040 051505 040524
015610 052122 040440 020124
015612 042524 052123 044440
015614 020122 051120 043517

```

016050	042522	051523	000
016055	015	042012	042132
016060	041510	000	
016065	000	051010	000
016070	000	052010	051505
016075	020124	041520	000055

```

MEPASS: .ASCIZ  <15><12>/DZDHC/
MR: .ASCIZ  <15><12>/R/
MTSTPC: .ASCIZ  <15><12>/TEST PC-

```

:TABLE OF POINTERS FOR TRAP DECODING

016104	014122
016106	014474
016110	015014
016112	014526
016114	014620
016116	014630
016118	015122
016120	015222
016124	014222

```

TRPTAB: SCOPER
        TYPER
        OCTASN
        INSTAG
        INSTRE
        PARAMS
        SVOSP
        RSOS
        SCOPR

```

:BUFFERS FOR INPUT-OUTPUT

016126	000000
	016140
016140	000000
	016152
016152	000000
	016164

```

INBUF: 0
        =.+10
TEMP: 0
        =.+10
MDATA: 0
        =.+10

```

:TABLE OF POINTERS TO ERROR MESSAGES AND DATA

016164			
016164	016230		
016166	016656		
016170	016310		
016172	000000		
016174	015325		
016176	000000		
016200	016256		
016202	016656		
016204	016415		
016206	016656		
016210	016453		
016212	000000		
016214	016507		
016216	016656		
016220	016544		
016222	016656		
016224	016603		
016226	016670		
016230	047125	054105	042520
016236	052103	042105	044440
016244	052116	051105	052522
016252	052120		
016254	005015	047503	052116
016262	047522	020114	042522
016270	044507	052123	051105

```

ERRTAB:
        EMO
        DT1
        EM1
        0
        EM2
        0
        EM3
        DT1
        EM4
        DT1
        EM5
        0
        EM6
        DT1
        EM7
        DT1
        EM10
        DT2
EMO: .ASCII  /UNEXPECTED INTERRUPT/

.ASCIZ  <15><12>/CONTROL REGISTER CONTENTS

```

F06

00000000 .PFC

016276	041440	047117	042524		
016304	052116	000123			
016310	047516	044440	052116	EM1:	.ASCIZ /NO INTERRUPT/
016316	051105	052522	052120		
016324	000				
016325	124	040522	051516	EM2:	.ASCIZ /TRANSMITTER DONE NOT SET/
016332	044515	052124	051105		
016340	042040	047117	020105		
016346	047516	020124	042523		
016354	000124				
016356	052502	020123	042101	EM3:	.ASCII /BUS ADDRESS ERROR/
016364	051104	051505	020123		
016372	051105	047522	122		
016377	015	042412	050130		.ASCIZ <15><12>/EXP REC/
016404	020040	020040	051040		
016412	041505	000			
016415	102	052131	020105	EM4:	.ASCII /BYTE COUNT ERROR/
016422	047503	047125	020124		
016430	051105	047522	122		
016435	015	042412	050130		.ASCIZ <15><12>/EXP REC/
016442	020040	020040	051040		
016450	041505	000			
016453	103	040510	040522	EM5:	.ASCIZ /CHARACTER AVAILABLE NOT SET/
016460	052103	051105	040440		
016466	040526	046111	041101		
016474	042514	047040	052117		
016502	051440	052105	000		
016507	123	046111	020117	EM6:	.ASCII /SILO DATA ERROR/
016514	040504	040524	042440		
016522	051122	051117			
016526	005015	054105	020120		.ASCIZ <15><12>/EXP REC/
016534	020040	020040	042522		
016542	000103				
016544	044523	047514	051440	EM7:	.ASCII /SILO STATUS ERROR/
016552	040524	052524	020123		
016560	051105	047522	122		
016565	015	042412	050130		.ASCIZ <15><12>/EXP REC/
016572	020040	020040	051040		
016600	041505	000			
016603	123	046111	020117	EM10:	.ASCII /SILO ALARM ERROR/
016610	046111	051101	020115		
016616	051105	047522	122		
016623	015	040412	040514		.ASCIZ <15><12>/ALARM LEVEL FILL LEVEL/
016630	046522	046040	053105		
016636	046105	020040	044506		
016644	046114	046040	053105		
016652	046105	000			
016656	016656				.EVEN
					;DATA TABLES FOR ERROR OUTPUT
016656	000002			DT1:	2
016660	006	002		.BYTE	6,2
016662	015442				SAVR5
016664	006	000		.BYTE	6,0
016666	015440				SAVR4

3566	016670	000002
3567	016672	002
3568	016674	015442
3569	016676	002
3570	016700	015438
3571	016702	000000
3572		000001

014
000

DT2: 2
 .BYTE 2 14
 SAVR5
 .BYTE 2 0
 SAVR3
 ENDCOD: 0
 .END

H06

ADRCNT = 015013	321*	3252*	3259*											
ADRCNT = 001242	528	957	963*	3083										
ADRCNT = 015170	3270*	3271	3301*											
ADRCNT = 000001	1232*	1292*	1352*	1412*	1472*	1532*	1592*	1652*	1712*	1772*	1832*	1892*	1952*	
	2013*	2072*	2132*	2192*	2236*	2280*	2324*	2368*	2412*	2456*	2500*	2544*	2588*	
	2632*	2676*	2720*	2764*	2808*	2852*	2896*							
BIT00 = 000001	604*													
BIT01 = 000002	603*													
BIT02 = 000004	602*													
BIT03 = 000010	601*													
BIT04 = 000020	600*													
BIT05 = 000040	599*													
BIT06 = 000100	598*	997	1099	2915										
BIT07 = 000200	597*	1101												
BIT08 = 000400	596*													
BIT09 = 001000	595*	1099	1135	1172	1209									
BIT10 = 002000	594*	1175												
BIT11 = 004000	593*	990	1024	1058	1093	1130	1167	1204	1243	1303	1363	1423	1483	
	1543	1603	1663	1723	1783	1843	1903	1963	2023	2093	2143	2204	2248	
	2292	2336	2380	2424	2466	2512	2556	2600	2644	2698	2732	2776	2920	
	2864	2911	2952	2987	3032									
BIT12 = 010000	592*	1031	1138											
BIT13 = 020000	591*	1065	1173	1210	1253	1313	1373	1433	1493	1553	1613	1673	1733	
	1793	1853	1913	1973	2033	2093	2153							
BIT14 = 040000	590*	1136												
BIT15 = 100000	589*	1212	2914	2921	2955	2959	2993	2996	3036	3040				
CHRCNT 015166	3268*	3272	3285*	3299*	3300									
CLEAR 015264	1244	1304	1364	1424	1484	1544	1604	1664	1724	1784	1844	1904	1964	
	2024	2084	2144	2206	2250	2294	2338	2382	2426	2470	2514	2558	2602	
	2646	2690	2734	2778	2822	2866	3328*							
CATABP 014366	3131*	3134	3141	3144*										
DEVADR 015010	3215*	3249	3257*											
CHBA 015364	1269	1271	1329	1331	1389	1391	1449	1451	1509	1511	1569	1571	1629	
	1631	1689	1691	1749	1751	1809	1811	1869	1871	1929	1931	1989	1991	
	2049	2051	2109	2111	2169	2171	2220	2264	2308	2352	2396	2440	2484	
	2528	2572	2616	2660	2704	2748	2792	2836	2880	3331*	3355*			
DHBAR 015370	1251*	1262	1266	1311*	1322	1326	1371*	1382	1396	1431*	1442	1446	1491*	
	1502	1506	1551*	1562	1566	1611*	1622	1626	1671*	1682	1686	1731*	1742	
	1746	1791*	1802	1806	1851*	1862	1866	1911*	1922	1926	1971*	1982	1986	
	2031*	2042	2046	2091*	2102	2106	2151*	2162	2166	2209*	2253*	2297*	2341*	
	2385*	2429*	2473*	2517*	2561*	2605*	2649*	2693*	2737*	2781*	2825*	2869*	3357*	
DHBC 015366	1249*	1279	1281	1309*	1339	1341	1369*	1399	1401	1429*	1459	1461	1489*	
	1519	1521	1549*	1579	1581	1609*	1639	1641	1669*	1699	1701	1729*	1759	
	1761	1789*	1819	1821	1849*	1879	1891	1909*	1939	1941	1969*	1999	2001	
	2029*	2059	2061	2089*	2119	2121	2149*	2179	2181	2219	2253	2307	2351	
	2395	2439	2483	2527	2571	2615	2659	2703	2747	2791	2835	2879	3330*	
	3341*	3356*												
DHBCR 015372	3358*													
DHLPR 015362	3354*													
DHNRC 015360	2926	3001	3353*											
DHRLVL 015402	993*	1011	1012*	1027*	1045	1046*	1061*	1079	1090*	1095*	1116	1117*	1132*	
	1153	1154*	1169*	1190	1191*	1206*	1227	1228*	1286	1287*	1346	1347*	1406	
	1407*	1466	1467*	1526	1527*	1586	1587*	1646	1647*	1706	1707*	1766	1767*	
	1826	1827*	1886	1887*	1946	1947*	2006	2007*	2066	2067*	2126	2127*	2186	
	2187*	2913*	3362*											
DHVEC 015400	943	991*	1011*	1025*	1045*	1059*	1079*	1094*	1116*	1131*	1153*	1169*	1190*	

HILIM	015006	3214*	3240	3256*										
ICOUNT	015424	989*	1022*	1056*	1091*	1128*	1165*	1202*	1241*	1301*	1361*	1421*	1491*	1541*
		1601*	1661*	1721*	1781*	1841*	1901*	1961*	2021*	2081*	2141*	2202*	2246*	2290*
		2334*	2378*	2422*	2466*	2510*	2554*	2598*	2642*	2686*	2730*	2774*	2818*	2862*
		2909*	2948*	2993*	3028*	3095	3373*							
INBUF	016126	3192	3220	3475*										
INIFLG	015450	914	925	956	958*	3383*								
INSTER=	104404	886*	3235											
INSTR =	104403	885*	938	946	967									
INSTRE	014620	3205*	3467											
INSTRG	014526	3188*	3465											
INSTR1	014540	3190*	3207											
INSTR2	014626	3199	3208*											
LAST	015454	3072*	3118	3120*	3385*	3422*								
LIGHTS=	177570	574*	3075*											
LIMITS	014740	3230	3240*											
LINE =	000000	1232*	1292*	1352*	1412*	1472*	1532*	1592*	1652*	1712*	1772*	1832*	1892*	1952*
		2012*	2072*	2132*	2192*	2235*	2280*	2324*	2368*	2412*	2456*	2500*	2544*	2588*
		2632*	2676*	2720*	2764*	2808*	2352*	2896*						
LOAD	015316	2208	2252	2296	2340	2384	2428	2472	2516	2560	2604	2648	2692	2736
		2780	2824	2868	3339*									
LOBITS	015012	3216*	3244	3258*	3259									
LOGICA	014106	892	3079*											
LOLIM	015004	3213*	3242	3255*										
LPCNT	015426	3094*	3095	3097*	3374*									
MCRLF	015765	3264	3445*											
MDATA	016152	3283	3294	3479*										
MEPASS	016055	3071	3455*											
MFFAIL	015770	3420	3446*											
MGM	015761	3206	3444*											
MR	016063	980	3457*											
MREGAD	015725	947	3439*											
MSG	014542	3188*	3191*											
MTITLE	015624	913	3427*											
MTSTPC	016071	968	3458*											
MVECTO	015703	939	3435*											
N =	000001	1*												
OCTASC=	104402	884*	3136	3143	3417									
OCTASN	015014	3263*	3465											
PARAM =	104405	887*	940	948	969									
PARAMS	014630	3212*	3468											
PARAM1	014660	3213*	3236											
PAPERR	014734	3222	3224	3226	3235*	3241	3243	3245						
PASCNT	015412	909*	3074*	3075	3368*									
PC =	%000007	569*	1244*	1304*	1364*	1424*	1484*	1544*	1604*	1664*	1724*	1784*	1844*	1904*
		1964*	2024*	2084*	2144*	2206*	2208*	2250*	2252*	2294*	2296*	2338*	2340*	2382*
		2384*	2426*	2428*	2470*	2472*	2514*	2516*	2558*	2560*	2602*	2604*	2646*	2688*
		2690*	2692*	2734*	2736*	2778*	2780*	2822*	2824*	2866*	2868*	3079*	3335*	3345*
PFAIL	015460	867	907	3390*	3411									
PFTAB	015614	3418	3424*											
POPPO =	012600	583*	3151											
POP1SP=	005726	581*												
POP2SP=	022626	585*												
FS =	177776	575*	905*	963*	987*	999*	1001*	1021*	1033*	1035*	1055*	1067*	1069*	1090*
		1103*	1105*	1127*	1140*	1142*	1164*	1177*	1179*	1201*	1214*	1216*	1240*	1254*
		1300*	1314*	1360*	1374*	1420*	1434*	1490*	1494*	1540*	1554*	1600*	1614*	1650*

K06

		1674*	1720*	1734*	1790*	1794*	1840*	1854*	1900*	1914*	1950*	1974*	2020*	2034*
		2080*	2094*	2140*	2154*	2201*	2245*	2283*	2333*	2377*	2421*	2465*	2503*	2552*
		2597*	2641*	2685*	2729*	2773*	2817*	2861*	2908*	2916*	2947*	2982*	3027*	3412*
PUSHRO=	010046	582*	3148											
PUSH1S=	005746	580*												
PUSH2S=	024646	584*												
RESREG	014370	3142	3145*											
RESTAR	015516	3398	3404*											
RESTRY	014116	3077	3083*											
RESOS =	104407	889*	3145											
RETURN	015416	976*	981	3099*	3101	3370*	3423							
RSCS	015232	3318*	3470											
R0	=:000000	562*	917*	919	921	1250*	1255*	1310*	1315*	1370*	1375*	1430*	1435*	1490*
		1495*	1550*	1555*	1610*	1615*	1670*	1675*	1730*	1735*	1790*	1795*	1850*	1855*
		1910*	1915*	1970*	1975*	2030*	2035*	2090*	2095*	2150*	2155*	2212*	2233*	2255*
		2277*	2300*	2321*	2344*	2365*	2388*	2409*	2432*	2453*	2476*	2497*	2520*	2541*
		2564*	2585*	2608*	2629*	2652*	2673*	2696*	2717*	2740*	2761*	2784*	2805*	2828*
		2849*	2872*	2893*	2917*	2919*	2953*	2961*	2991*	2997*	2999*	3004*	3037*	3038*
R1	=:000001	3149*	3273*	3277*	3284	3314	3318*	3328*	3333*	3339*	3343*	3390	3410*	3038*
		563*	929*	932*	934*	936	2214*	2232*	2258*	2276*	2302*	2320*	2346*	2364*
		2390*	2408*	2434*	2452*	2478*	2496*	2522*	2540*	2566*	2584*	2610*	2628*	2654*
		2672*	2698*	2716*	2742*	2760*	2786*	2804*	2830*	2848*	2874*	2892*	2951*	2953
		2971*	2973	2986*	2389	2999	3016*	3017	3034*	3035*	3041*	3044	3050	3076*
		3079	3265*	3267	3268	3269	3270	3313	3319*	3391	3409*			
R2	=:000002	564*	930*	932	933*	935*	2220*	2228	2264*	2272	2308*	2316	2352*	2360
		2396*	2404	2440*	2448	2484*	2492	2528*	2536	2572*	2580	2616*	2624	2660*
		2668	2704*	2712	2748*	2756	2792*	2800	2836*	2844	2880*	2888	2956*	2957*
		2992*	2994*	3000*	3002*	3312	3320*	3392	3408*					
R3	=:000003	565*	931*	934	935	2217*	2224*	2228	2261*	2268*	2272	2305*	2312*	2316
		2349*	2356*	2360	2393*	2400*	2404	2437*	2444*	2448	2481*	2488*	2492	2525*
		2532*	2536	2569*	2576*	2580	2613*	2620*	2624	2657*	2664*	2668	2701*	2709*
		2712	2745*	2752*	2756	2789*	2796*	2800	2833*	2840*	2844	2877*	2884*	2888
		2925*	2933	3046*	3052*	3193*	3203*	3274*	3275*	3276*	3277	3283*	3284*	3289*
		3292*	3311	3321*	3393	3407*								
R4	=:000004	566*	1266*	1271*	1281*	1326*	1331*	1341*	1386*	1391*	1401*	1446*	1451*	1461*
		1506*	1511*	1521*	1566*	1571*	1581*	1626*	1631*	1641*	1686*	1691*	1701*	1745*
		1751*	1761*	1806*	1811*	1821*	1866*	1871*	1891*	1926*	1931*	1941*	1986*	1991*
		2001*	2046*	2051*	2061*	2106*	2111*	2121*	2166*	2171*	2181*	2219*	2225	2263*
		2269	2307*	2313	2351*	2357	2395*	2401	2439*	2445	2483*	2489	2527*	2533
		2571*	2577	2615*	2621	2659*	2665	2703*	2709	2747*	2753	2791*	2797	2835*
		2841	2879*	2885	2926*	2930	2933*	2934*	2937	2963*	2964*	2965*	2966	3006*
		3007*	3012	3125*	3126*	3127*	3128*	3129*	3130	3131	3192*	3196*	3197*	3199
		3220*	3221	3223	3225	3227*	3228	3229	3249*	3250*	3271*	3274	3278*	3279*
		3280*	3310	3322*	3394	3406*								
R5	=:000005	567*	1003*	1007*	1037*	1041*	1071*	1075*	1112*	1149*	1186*	1223*	1264*	1274*
		1283*	1324*	1334*	1343*	1384*	1394*	1402*	1444*	1454*	1463*	1504*	1514*	1523*
		1564*	1574*	1583*	1624*	1634*	1643*	1684*	1694*	1703*	1744*	1754*	1763*	1804*
		1814*	1823*	1864*	1874*	1883*	1924*	1934*	1943*	1984*	1994*	2003*	2044*	2054*
		2063*	2104*	2114*	2123*	2164*	2174*	2183*	2215*	2223*	2225	2259*	2267*	2269
		2303*	2311*	2313	2347*	2355*	2357	2391*	2399*	2401	2435*	2443*	2445	2479*
		2487*	2489	2523*	2531*	2533	2567*	2575*	2577	2611*	2613*	2621	2655*	2663*
		2665	2699*	2707*	2709	2743*	2751*	2753	2787*	2795*	2797	2831*	2839*	2841
		2875*	2883*	2885	2928*	2930	2935*	2937	2954*	2960*	2966	2998*	2989*	3012
		3031*	3033	3034	3055	3058*	3059	3123*	3124*	3125	3176*	3180	3183	3212*
		3213	3214	3215	3216	3217	3218	3219*	3228*	3231*	3232*	3233*	3240	3242
		3244	3250	3251*	3272*	3281*	3309	3323*	3395	3405*				

SAVPC	015446	3159	3305*	3382#										
SAVRO	015430	3314*	3318	3375#										
SAVR1	015432	3313*	3319	3376#										
SAVR2	015434	3312*	3320	3377#										
SAVR3	015436	3311*	3321	3378#	3570									
SAVR4	015440	3310*	3322	3379#	3565									
SAVR5	015442	3309*	3323	3380#	3563	3568								
SAVSP	015444	3381#	3397*	3404										
SAVOSP =	104406	888#	3122											
SCOPE =	10440C	882#	1015	1049	1083	1120	1157	1194	1231	1291	1351	1411	1471	1531
		1591	1651	1711	1771	1831	1891	1951	2011	2071	2131	2191	2235	2279
		2323	2367	2411	2455	2499	2543	2587	2631	2675	2719	2763	2907	2951
		2895	2941	2975	3019	3061								
SCOPER	014122	3088#	3463											
SCOPE1 =	104410	990#	2969	3015	3054									
SCOPIR	014222	3109#	3471											
SIZE	001056	917#												
SP =	0000006	568#	906*	964*	1005*	1009*	1039*	1043*	1073*	1077*	1110*	1114*	1147*	1151*
		1184*	1188*	1221*	1225*	1290*	1350*	1410*	1470*	1530*	1590*	1650*	1710*	1770*
		1830*	1890*	1950*	2010*	2070*	2130*	2190*	2940#	3099	3101*	3111*	3118	3120
		3123	3149	3155*	3165*	3166*	3167*	3168*	3169*	3170*	3171*	3172	3176	3177*
		3188	3189*	3212	3218*	3265	3266*	3305	3390*	3391*	3392*	3393*	3394*	3395*
		3396*	3397	3404*	3405	3406	3407	3408	3409	3410	3413*			
SPACNT =	015167	3269*	3287	3290*	3300#									
STACK =	017102	576#	906	964	1290	1350	1410	1470	1530	1590	1650	1710	1770	1830
		1890	1950	2010	2070	2130	2190	2940	3413					
START	001000	874	905#											
STFLG	015452	908*	977	979*	3384#									
SV05	015200	3309#												
SV05P	015172	3305#	3469											
SWR =	177570	573#	927	965	3088	3090	3092	3109	3116	3146	3153			
SW00 =	000001	556#	927											
SW01 =	000002	555#	965											
SW02 =	000004	554#												
SW03 =	000010	553#												
SW04 =	000020	552#												
SW05 =	000040	551#												
SW06 =	000100	550#												
SW08 =	000400	549#												
SW09 =	001000	548#	3109											
SW10 =	002000	547#	3088	3153										
SW11 =	004000	546#	3092											
SW12 =	010000	545#												
SW13 =	020000	544#	3116											
SW14 =	040000	543#	3090											
SW15 =	100000	542#												
TEMP	016140	3273	3414*	3415*	3477#									
TKCSR	015346	3194	3348#											
TKDBR	015350	3196	3200	3349#										
TPCSR	015352	3178	3201	3350#										
TPCDBR	015354	3183*	3200*	3351#										
TRPOK	014454	3168#												
TRFSRV	014442	871	3165#											
TRPTAB	016104	3170	3463#											
TYPDAT	014356	3135	3141#											
TYPE =	104401	883#	913	980	3070	3139	3190	3205	3263	3293	3419			

TYPFR	014474	3176#	3464												
TYPMSG	014340	3133	3136#												
T1	001334	976	987#												
T10	003032	1240#													
T11	003270	1300#													
T12	003526	1360#													
T13	003764	1420#													
T14	004222	1480#													
T15	004460	1540#													
T16	004716	1600#													
T17	005154	1660#													
T2	001516	1021#													
T20	005412	1720#													
T21	005650	1780#													
T22	006106	1840#													
T23	006344	1900#													
T24	006602	1960#													
T25	007040	2020#													
T26	007276	2080#													
T27	007534	2140#													
T3	001700	1055#													
T30	007772	2201#													
T31	010142	2245#													
T32	010312	2289#													
T33	010462	2333#													
T34	010632	2377#													
T35	011002	2421#													
T36	011152	2465#													
T37	011322	2509#													
T4	002062	1090#													
T40	011472	2553#													
T41	011642	2597#													
T42	012012	2641#													
T43	012162	2685#													
T44	012332	2729#													
T45	012502	2773#													
T46	012652	2817#													
T47	013022	2861#													
T5	002254	1127#													
T50	013172	2908#													
T51	013356	2947#													
T52	013512	2982#													
T53	013672	3027#													
T6	002446	1164#													
T7	002640	1201#													
VEC1	001120	915	927#												
VEC2	001130	926	929#												
WRDCNT	015164	3267*	3295*	3298#											
X =	000000	1#													
XBIT =	000001	1232#	2192#	2896#											
XLIN =	000000	1232#	2192#	2896#											
XN =	000054	1#	987	990#	1021	1024#	1055	1058#	1090	1093#	1127	1130#	1164	1167#	
		1201	1204#	1240	1243#	1300	1303#	1360	1363#	1420	1423#	1490	1483#	1540	
		1543#	1600	1603#	1660	1663#	1720	1723#	1780	1783#	1840	1843#	1900	1903#	
		1960	1963#	2020	2023#	2080	2083#	2140	2143#	2201	2204#	2245	2248#	2299	
		2292#	2333	2336#	2377	2380#	2421	2424#	2465	2468#	2509	2512#	2553	2556#	

		2597	2600*	2641	2644*	2685	2688*	2729	2732*	2773	2776*	2817	2820*	2861
Y	= 000011	2864*	2908	2911*	2947	2951*	2982	2986*	3027	3031*				
.	= 016704	1*	882	883*	884*	885*	886*	887*	888*	889*	890*	891*		
		606*	607	609	611	613	615	617	619	621	623	625	627	629
		631	633	635	637	639	641	643	645	647	649	651	653	655
		657	659	661	663	665	667	669	671	673	675	677	679	691
		683	685	687	689	691	693	695	697	699	701	703	705	707
		709	711	713	715	717	719	721	723	725	727	729	731	733
		735	737	739	741	743	745	747	749	751	753	755	757	759
		761	763	765	767	769	771	773	775	777	779	781	783	785
		787	789	791	793	795	797	799	801	803	805	807	809	911
		813	815	817	819	821	823	825	827	829	831	833	835	837
		839	841	843	845	847	849	851	853	855	857	859	861	865*
		873*	891*	893*	895*	3039	3400	3416	3476*	3478*	3480*	3557*		

DZDHC MACY11 27.732 16-MAR-76 09:17 PAGE 87
DZDHC.PFC CROSS REFERENCE TABLE -- PERMANENT SYMBOLS

..PAGE	1955	15095	99	883	884	885	886	887	888	889	890	891	892	893	894
..PAGE	558	605	863	895											
..PAGE	607	1232	2192												
..TITLE	539														

ERRORS DETECTED: 0
DEFAULT GLOBALS GENERATED: 0

*DZDHC.DZDHC.SEQ/CRF.SOL/PAGNUM=DSK2:UTIL2.P11.DZDHC.PFC
RUN-TIME: 14 26 4 SECONDS
RUN-TIME RATIO: 107 45=2.3
CORE USED: 12K (23 PAGES)

