

**DH11**

LOGIC TEST  
**MD-11-DZDHC-B**

EP-DZDHC-B-DL-A

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IDENTIFICATION

PRODUCT CODE: PRINCEC-11-C2C-C-B-D  
PRODUCT #: D411 TRANSMITTER AND RECEIVER  
TEST:  
MANUFACTURER: DIAGNOSTIC GROUP  
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100-1127732 16-205-76 09:17 PAGE 3

INSTRUMENTATION

ABSTRACT

THE D411 TRANSMITTER AND RECEIVER LOGIC TEST CHECKS THE BASIC TRANSMITTER AND RECEIVER FUNCTIONS. FUNCTIONS TESTED INCLUDE INTERRUPTS, OPERATION OF TRANSMITTER MFR LOGIC, AND OPERATION OF RECEIVER SILO LOGIC.

## 3. REQUIREMENTS

## 2.1 EQUIPMENT

PDP-11 FAMILY STANDARD COMPUTER WITH 4KW OF MEMORY  
ASR-33 TELETYPE OR EQUIVALENT  
DH11 ASYNCHRONOUS MULTIPLEXER  
CM11 MAINTENANCE CARD INSTALLED

## 2.2 STORAGE

THE PROGRAM LOADS INTO 4KW OF MEMORY

## 3. LOADING PROCEDURE

THE STANDART PROCEDURE FOR LOADING ABSOLUTE BINARY TAPES  
IS TO BE USED

## 4. STARTING PROCEDURE

## 4.1 CONTROL SWITCH SETTINGS

## 4.1.1 AFTER PROGRAM LOAD (INITIAL PROGRAM START)

ALL CONSOLE SWITCHES DOWN

4.1.2 TO MODIFY DEVICE VECTOR AND CONTROL REGISTER ADDRESSES  
AFTER PROGRAM RESTART

SW00=1

## 4.1.3 TO START PROGRAM AT SELECTED TEST AFTER PROGRAM RESTART

SW01=1

## 4.2 STARTING ADDRESS

THE STARTING ADDRESS FOR ALL TESTS IS 000200

THE RESTART ADDRESS FOR ALL TESTS IS 0002000

THE STARTING ADDRESS TO ENTER A SELECTED TEST IS 000200

## 4.3 PROGRAM AND/OR OPERATOR ACTION

## 4.3.1 INITIAL PROGRAM START

## 4.3.1.1 LOAD PROGRAM INTO MEMORY

## 4.3.1.2 LOAD ADDRESS 000200

## 4.3.1.3 CLEAR CONSOLE SWITCHES

## 4.3.1.4 PRESS START

4.3.1.5 THE PROGRAM WILL TYPE "DH11 XXXX"  
AND WILL THEN TYPE "VECTOR ADDRESS--" AND WAIT FOR AN  
INPUT FROM THE TELETYPE KEYBOARD.

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## 4.3 (CONT'D)

4.3.1.6 TYPE IN THE ADDRESS OF THE RECEIVER INTERRUPT VECTOR FOR THE DH11 TO BE TESTED FOLLOWED BY <CARRIAGE RETURN>

NOTE: WORDS IN ANGLE BRACKETS, I.E. <CARRIAGE RETURN> MEAN THAT THE TELETYPE KEY WITH THE NAMED FUNCTION SHOULD BE PRESSED

IF AN INCORRECT ADDRESS IS ENTERED, THE PROGRAM

WILL TYPE "?" AND WILL REPEAT THE SECOND MESSAGE OF 4.3.1.5  
4.3.1.7 THE PROGRAM WILL TYPE "CONTROL REGISTER ADDRESS-" AND WAIT FOR AN INPUT FROM THE TELETYPE KEYBOARD

4.3.1.8 TYPE IN THE ADDRESS OF THE SYSTEM CONTROL REGISTER OF THE DH11 TO BE TESTED FOLLOWED BY <CARRIAGE RETURN>

IF AN INCORRECT ADDRESS IS TYPED, THE PROGRAM WILL TYPE "?" AND WILL THEN REPEAT THE MESSAGE OF 4.3.1.7

4.3.1.9 THE PROGRAM WILL TYPE "R" TO INDICATE THAT IT IS ABOUT TO START TESTING, AND THEN TESTING WILL BEGIN

## 4.3.2 PROGRAM RESTART WITH ALL SWITCHES DOWN

4.3.2.1 PERFORM 4.3.1.2 TO 4.3.1.5

4.3.2.2 THE PROGRAM WILL TYPE "DH11 XXXX" AND WILL THEN CONTINUE AS DESCRIBED IN 4.3.1.9

## 4.3.3 PROGRAM RESTART WITH SW00=1

4.3.3.1 LOAD ADDRESS 000200

4.3.3.2 SET SW01=1

4.3.3.3 PRESS START

4.3.3.4 THE PROGRAM WILL PERFORM AS DESCRIBED IN 4.3.1.5 TO 4.3.1.9

## 4.3.4 PROGRAM RESTART WITH SW01=1

4.3.4.1 LOAD ADDRESS 000200

4.3.4.2 SET SW01=1

4.3.4.3 PRESS START

4.3.4.4 THE PROGRAM WILL TYPE "DH11 XXXX" AND WILL THEN TYPE "TEST FC-" AND WILL WAIT FOR AN INPUT FROM THE TELETYPE KEYBOARD

4.3.4.5 TYPE IN THE ADDRESS OF THE TEST AT WHICH THE PROGRAM IS TO BE STARTED FOLLOWED BY <CARRIAGE RETURN>

4.3.4.6 THE PROGRAM WILL TYPE R TO INDICATE THAT IT HAS STARTED AND WILL START TESTING AT THE SELECTED TEST.

NOTE: CARE MUST BE TAKEN WHEN THIS FEATURE IS USED, SINCE THERE IS NO PROTECTION AGAINST SELECTING AN ADDRESS THAT IS IN THE MIDDLE OF A TEST

NOTE: IF IT IS DESIRED TO LOOP ON THE TEST THAT IS SELECTED SET SW14=1 BEFORE ENTERING THE TEST ADDRESS

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## 5. OPERATING PROCEDURE

## 5.1 OPERATIONAL SWITCH SETTINGS

SW15=1. HALT ON ERROR  
SW14=1, LOOP ON CURRENT TEST  
SW13=1, SUPPRESS ERROR TYPEOUT  
SW11=1, INHIBIT ITERATIONS  
SW10=1, ESCAPE TO NEXT TEST ON ERROR  
SW09=1, FREEZE VARIABLE PARAMETER IN CURRENT TEST  
SW01=1, START PROGRAM AT SELECTED TEST  
SW00=1, CHANGE PARAMETERS AT PROGRAM RESTART

## 5.2 SUBROUTINE ABSTRACTS

## 5.2.1 TRAPCATCHER (LOCATIONS 000000-000776)

THIS ROUTINE IS USED TO INTERCEPT UNEXPECTED INTERRUPTS AND TRAPS. THE AREA FROM 000000-000776 IS LOADED WITH THE FOLLOWING SEQUENCE

2  
0  
4  
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:  
772  
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776  
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IF AN UNEXPECTED INTERRUPT OR TRAP OCCURS, THE PROGRAM WILL HALT WITH THE PC 2 GREATER THAN THE ADDRESS TO WHICH THE PROGRAM TRAPPED. THE PROCESSOR STACK MAY BE EXAMINED TO DETERMINE WHERE THE PROGRAM WAS WHEN THE TRAP OR INTERRUPT OCCURED.

## 5.2.2 START (PROGRAM INITIALIZATION)

THIS ROUTINE INITIALIZES ALL PROGRAM FLAGS AND COUNTERS, TYPES THE PROGRAM TITLE MESSAGE, AND INPUTS THE VECTOR AND CONTROL REGISTER ADDRESSES OF THE DH11 TO BE TESTED.

## 5.2.3 BEGIN (PROGRAM START AND RESTART)

THIS ROUTINE IS ENTERED IMMEDIATELY AFTER "START" AND EACH TIME A PROGRAM PASS HAS BEEN COMPLETED. THE ROUTINE SETS UP THE PROCESSOR STACK AND STATUS WORD AND THEN TRANSFERS CONTROL TO THE TEST AT WHICH TESTING WILL BEGIN. IF SW01=0 WHEN THIS ROUTINE IS ENTERED TESTING WILL START AT T1 (TEST 1). IF SW01=1 WHEN THIS ROUTINE IS ENTERED, TESTING WILL START AT THE PC ENTERED FROM THE TELETYPE KEYBOARD.

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## 5.2.4 EOP (END OF PASS)

THIS ROUTINE IS ENTERED ONCE PER PASS AFTER ALL TESTS HAVE BEEN COMPLETED. THIS ROUTINE TYPES THE MAINDEC IDENTIFICATION CODE OF THE PROGRAM, CLEARS ERROR FLAGS AND UPDATES THE PASS COUNT. IF THE PROGRAM WAS LOADED UNDER ACT11 OR DDP, THE ROUTINE CHECKS FOR RETURN TO THE ACT11 OR DDP MONITOR. IF THE PROGRAM IS NOT UNDER MONITOR CONTROL, THE ROUTINE TRANSFERS TO BEGIN.

## 5.2.5 SCOPER (SCOPE LOOP AND ITERATION HANDLER)

THIS ROUTINE IS ENTERED EACH TIME A TEST IS COMPLETED. THE ROUTINE CHECKS FOR THE FOLLOWING UPON ENTRY  
A) IF SW1G=1, THE ROUTINE WILL TRANSFER TO THE NEXT TEST IN SEQUENCE, AFTER CLEARING ERROR FLAGS.  
B) IF SW1I=1, THE ROUTINE WILL TRANSFER TO THE NEXT TEST SEQUENCE, AFTER CLEARING ERROR FLAGS.  
C) IF SW14=1, THE ROUTINE WILL LOOP ON THE CURRENT TEST REGARDLESS OF THE ITERATION COUNT.

IF NONE OF THE ABOVE IS TRUE, THE ROUTINE WILL ADD 1 TO THE COUNT OF TEST ITERATIONS, AND COMPARE THIS VALUE TO THE NUMBER OF ITERATIONS THAT SHOULD BE PERFORMED. IF THESE NUMBERS ARE EQUAL, THE ROUTINE WILL TRANSFER TO THE NEXT TEST IN SEQUENCE. IF THE NUMBERS ARE NOT EQUAL, THE TEST CURRENTLY IN PROGRESS WILL BE REPEATED.

## 5.2.6 SCOP1R (FREEZE ON CURRENT DATA)

THE CALL TO THIS ROUTINE FOLLOWS IMMEDIATELY AFTER THE CALL TO THE ERROR HANDLER IN THOSE TESTS THAT HAVE VARIABLE PARAMETERS. THIS ROUTINE IS ALWAYS ENTERED IN THOSE TESTS, WHETHER OR NOT AN ERROR OCCURS.  
IF SWC9=1, THE ROUTINE WILL TRANSFER CONTROL BACK TO THE TEST AT A POINT WHICH WILL ALLOW REPEATING THE FUNCTION UNDER TEST CONTINUOUSLY WITH THE SAME DATA. IF THIS OPTION IS SELECTED, THE ROUTINE "SCOPER" IS NEVER ENTERED AND ITERATION COUNTS WILL NOT BE UPDATED.

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### 5.2.7 ERRORS (ERROR HANDLER)

THIS ROUTINE IS ENTERED UPON ERROR DETECTION ONLY.  
WITH ALL CONSOLE SWITCHES DOWN, THE ROUTINE PROCEEDS AS FOLLOWS:  
A) THE PC OF THE INSTRUCTION THAT CALLED THE ERROR HANDLER  
IS ACCESSED THRU THE STACK, AND THEN THE EMT INSTRUCTION  
ITSELF IS FETCHED. THE 8 LSB OF THE EMT  
INSTRUCTION ARE THE ERROR CODE. THIS CODE IS  
USED TO ACCESS A TABLE OF ERROR MESSAGES AND ERROR  
DATA STORAGE LOCATIONS.  
B) IF THE TEST THAT FAILED DID NOT FAIL PREVIOUSLY  
DURING THIS PASS, A COMPLETE ERROR REPORT IS MADE  
IF THE TEST THAT FAILED FAILED MORE THAN ONCE DURING  
THE CURRENT PASS, ONLY THE DATA RELATING TO THE FAILURE  
IS TYPED. IF SW13=1, NO ERROR TYPEOUT IS MADE.  
C) THE ROUTINE NOW CHECKS FOR HALT ON ERROR. IF SW15=1  
THE PROGRAM WILL HALT WITH THE PC OF THE CALL TO  
THE ERROR ROUTINE IN R0. IF SW15=0, THE PROGRAM WILL  
NOT HALT, BUT WILL CHECK FOR ESCAPE TO NEXT TEST.  
D) IF SW10=1, THE ROUTINE WILL RETURN  
TO THE TEST IN PROGRESS. IF SW10=1, THE ROUTINE WILL  
ABORT THE CURRENT TEST, AND TRANSFER TO THE NEXT  
TEST IN SEQUENCE, THRU THE ROUTINE "SCOOPER".

### 5.2.8 TRPSRV (TRAP DECODE AND DISPATCH)

THIS ROUTINE DECODES THE 8 LSB OF THE TRAP INSTRUCTION  
THAT CAUSED THE PROGRAM INTERRUPT, AND TRANSFERS CONTROL  
TO THE ROUTINE THRU THE TABLE "RPTAB" USING THE 8 LSB  
OF THE TRAP INSTRUCTION AS AN OFFSET TO THE POINTER TO  
THE ROUTINE TO BE ENTERED.

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- 5.3 PROGRAM AND OR OPERATOR ACTION
    - 5.3.1 PROGRAM START WITH ALL SWITCHES DOWN
      - 5.3.1.1 REFER TO SECTIONS 4.3.1 AND 4.3.2 FOR INITIAL PROGRAM BEHAVIOR.
      - 5.3.1.2 AFTER "R" HAS BEEN TYPED BY THE PROGRAM, TEST EXECUTION WILL BEGIN. EACH TEST WILL BE REPEATED A SELECTED NUMBER OF ITERATIONS (SEE LISTING FOR EXACT NUMBER FOR EACH TEST) AND THEN THE PROGRAM WILL PROCEED TO THE NEXT TEST.
      - 5.3.1.3 WHEN ALL ITERATIONS HAVE BEEN COMPLETED, THE PROGRAM WILL TYPE "DZDHX" AND THEN RESTART TESTING AT TEST 1 (LOCATION T1 IN THE PROGRAM).
      - 5.3.1.4 IF AN ERROR OCCURS, THE PROGRAM WILL TYPE AN APPROPRIATE ERROR MESSAGE, AND THEN CONTINUE THE TEST IN PROGRESS.
    - 5.3.2 PROGRAM START WITH SW00=1
      - THE PROGRAM WILL PERFORM AS DESCRIBED IN 4.3.1 AND 5.3.1
    - 5.3.3 PROGRAM START WITH SW01=1
      - 5.3.3.1 REFER TO SECTION 4.3.4 FOR INITIAL PROGRAM BEHAVIOR
      - 5.3.3.2 TEST EXECUTION WILL START AT THE ADDRESS SPECIFIED AND WILL CONTINUE AS DESCRIBED IN 5.3.1.2
      - 5.3.3.3 AFTER "DZDHX" HAS BEEN TYPED, THE PROGRAM WILL RESUME TESTING AT TEST 1
    - 5.3.4 PROGRAM OPERATION WITH SW15=1
      - SAME AS 5.3.1, EXCEPT THAT IN THE CASE OF AN ERROR, THE PROGRAM WILL HALT AFTER THE ERROR TYPEOUT, AND THE PC+2 OF THE CALL TO THE ERROR ROUTINE WILL BE DISPLAYED IN R0.
    - 5.3.5 PROGRAM OPERATION WITH SW13=1
      - SAME AS 5.3.1 EXCEPT THAT NO ERROR TYPEOUTS WILL OCCUR
    - 5.3.6 PROGRAM OPERATION WITH SW11=1
      - SAME AS 5.3.1 EXCEPT THAT EACH TEST WILL BE REPEATED ONCE ONLY
    - 5.3.7 PROGRAM OPERATION WITH SW10=1
      - SAME AS 5.3.1, EXCEPT THAT IN THE CASE OF AN ERROR THE CURRENT TEST WILL BE ABORTED, AND THE PROGRAM WILL PROCEED TO THE NEXT TEST IN SEQUENCE.

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## 5. (CONT'D)

## 5.3.8 PROGRAM OPERATION WITH SW14=1, OR SW09=1

THESE FUNCTIONS ARE NORMALLY USED FOR TROUBLE SHOOTING.  
SEE SECTION 6.3 FOR THEIR USE.

## 6. ERRORS

## 6.1 ERROR HALTS

THE ERROR MESSAGE FORMAT FOR ALL ERROR TYPEOUTS  
IS AS FOLLOWS

PC+2      MESSAGE  
              HEADER (IF APPLICABLE)  
              DATA    (IF APPLICABLE)

WHERE

PC+2 IS THE ADDRESS OF THE CALL TO THE ERROR HANDLER + 2  
MESSAGE IS AN ASCII MESSAGE DESCRIBING (BRIEFLY) THE FAILURE  
HEADER IS A DESCRIPTION OF THE DATA TO FOLLOW  
DATA IS OCTAL INFORMATION RELATING TO THE CAUSE OF THE FAILURE  
IF THE SAME ERROR OCCURS IN A GIVEN TEST ON THE SAME  
PASS, AND IF DATA IS ASSOCIATED WITH THAT ERROR, ONLY  
DATA IS TYPE ON SUCCEEDING ERROR TYPEOUTS

IF NO DATA IS ASSOCIATED WITH THE ERROR  
THE COMPLETE ERROR MESSAGE IS TYPED.

## 6.1.1 ERROR DESCRIPTIONS

SEE LISTING FOR DETAILS OF ERRORS

## 6.2 ERROR RECOVERY

## 6.2.1 SW15=0

IF THE PROGRAM IS RUN WITH SW15=0, NO OPERATOR ACTION IS  
REQUIRED TO CONTINUE TESTING

## 6.2.2 SW15=1

IF THE PROGRAM IS RUN WITH SW15=1, TO CONTINUE TESTING  
AFTER THE PROGRAM HAS HALTED, PRESS THE PROCESSOR  
CONSOLE CONTINUE SWITCH

## 6.2.3 ILLEGAL INTERRUPTS

IF AN INTERRUPT OCCURS TO A VECTOR ADDRESS NOT  
SELECTED DURING PROGRAM INITIALIZATION, THE PROGRAM WILL  
HALT IN THE TRAPCATCHER. THE ADDRESS AT WHICH  
THE PROGRAM HALTS IS 2 GREATER THAN THE ADDRESS  
TO WHICH THE INTERRUPT OCCURRED. THE PROGRAM MUST BE  
RESTARTED AT 200 TO RECOVER FROM THIS ERROR.

DZDHC MACY11 27(732) 16-MAR-76 09:17 PAGE 11  
DZDHCB.PFC

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405           6.3     SCOPE LOOPING  
406  
407           6.3.1   TO SCOPE ON A SPECIFIC TEST, SET SW14=1 AND SW13=1  
408           THIS WILL CAUSE THE PROGRAM TO CONTINUOUSLY LOOP ON THE  
409           SAME TEST, AND WILL CAUSE ALL ERROR TYPEOUTS TO BE INHIBITED  
410  
411           6.3.2   TO SCOPE ON A SPECIFIC VALUE OF A PARAMETER WITHIN  
412           A TEST, SET SW09=1 TO FREEZE THE DATA  
413           (SEE LISTING FOR THOSE TESTS THAT INCORPORATE THIS FEATURE)  
414  
415           6.       (CONT'D)  
416  
417           6.3.3   PROGRAM START TO SCOPE LOOP ON SELECTED TEST  
418           PERFORM SECTION 4.3.4 WITH SW14=1  
419  
420           7.       RESTRICTIONS  
421  
422           7.1      STARTING  
423           THE DH11 TEST CARD MUST BE INSTALLED  
424  
425           7.2      RUNNING  
426           NONE  
427  
428           8.       MISCELLANEOUS  
429  
430           8.1      EXECUTION TIME  
431           THE TIME FOR ONE PASS OF THE PROGRAM (END OF  
432           TYPEOUT OF DZDHX TO END OF TYPEOUT OF DZDHX)  
433           IS GIVEN FOR VARIOUS PROCESSORS IN THE TABLE BELOW  
434  
435           TIME  
436           PROCESSOR  
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438           PDP-11/05,10  
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440           PDP-11/20  
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442           PDP-11/40  
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444           PDP-11/45  
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## 9. PROGRAM DESCRIPTION

THE FIRST GROUP OF TESTS VERIFIES THAT NO INTERRUPTS OCCUR WITH INTERRUPT ENABLES SET FOR EACH INTERRUPTING FUNCTION AND THE ASSOCIATED DONE BIT OR FLAG FOR THAT FUNCTION CLEARED.

THE NEXT GROUP OF TESTS VERIFIES THAT AN INTERRUPT DOES OCCUR IF A SPECIFIC DONE BIT OR FLAG IS SET, ALONG WITH ITS CORRESPONDING INTERRUPT ENABLE. AT THIS TIME, INTERRUPTS TO THE CORRECT VECTOR ARE TESTED. IF AN INTERRUPT OCCURS TO ANY VECTOR OTHER THAN THOSE SELECTED AT PROGRAM START, THE PROGRAM WILL HALT IN THE TRAPCATCHER IN A LOCATION 2 GREATER THAN THE ADDRESS OF THE VECTOR TO WHICH THE INTERRUPT OCCURED.

THE NEXT GROUP OF TESTS CHECKS TRANSMITTER NPR AND INTERRUPT LOGIC OPERATION FOR EACH LINE. IN AN INDIVIDUAL TEST FOR EACH LINE, THE BYTE COUNT FOR THE SELECTED LINE IS SET TO -1 (FOR 1 CHARACTER TRANSMISSION) AND THE BUS ADDRESS MEMORY LOCATION FOR THAT LIN IS SET TO 0. THE BAR BIT FOR THE SELECTED LINE IS SET. TRANSMITTER INTERRUPT ENABLE IS SET, AND THE PROCESSOR STATUS WORD IS CLEARED TO ALLOW INTERRUPTS TO OCCUR. A DELAY LOOP IS THEN ENTERED, AND IF THE DELAY TIMES OUT BEFORE AN INTERRUPT OCCURS, AN ERROR MESSAGE IS TYPED. IF AN INTERRUPT DOES OCCUR, THE CONTROL REGISTER IS TESTED TO SEE IF THE TRANSMITTER DONE BIT HAS BEEN SET, THE BAR REGISTER IS CHECKED TO SEE THAT THE BAR BIT FOR THE SELECTED LIN HAS CLEARED, BYTE COUNT IS CHECKED TO SEE THAT IT WENT TO 0 AND THE BUS ADDRESS REGISTER FOR THE SELECTED LINE IS CHECKED TO SEE THAT IT INCREMENTED TO 1.

THE NEXT GROUP OF TESTS VERIFIES THAT A SINGLE SELECTED LINE WILL PERFORM TRANSMIT FUNCTIONS WITHOUT AFFECTING ANY OTHER LINE. THIS IS DONE BY SETTING ALL BYTE COUNTS TO -1, AND VERIFYING THAT ONLY THE LINE SELECTED FOR TRANSMISSION HAD CHANGES MADE IN BYTE COUNT AND BUS ADDRESS WHEN TRANSMISSION HAS BEEN COMPLETED.

THE NEXT TEST VERIFIES THAT A SINGLE CHARACTER CAN BE LOADED INTO THE SILO (IN MAINTENANCE MODE). THE TEST IS MADE WITH INTERRUPTS ENABLED AND CHECKS ARE MADE TO DETERMINE IF RECEIVER DONE WAS SET, IF THE SILO FILL LEVEL REGISTER WAS INCREMENTED, AND IF THE DATA RECEIVED IN MAINTENANCE MODE WAS CORRECT.

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## 9. (CONT'D)

THE NEXT TEST VERIFIES THAT FROM 1 TO 63 CHARACTERS CAN BE LOADED INTO THE SILO, AND THAT THE SILO FILL LEVEL REGISTER INDICATES THE CORRECT NUMBER OF CHARACTERS IN THE SILO.

THE NEXT TEST VERIFIES THAT 64 CHARACTERS CAN BE LOADED INTO THE SILO, FROM 1 TO 64 CHARACTERS CAN BE READ OUT OF THE SILO, AND THAT THE SILO FILL REGISTER INDICATES THE NUMBER OF CHARACTERS REMAINING IN THE SILO.

THE FINAL TEST VERIFIES THAT THE CHARACTER AVAILABLE FLAG WILL NOT BE SET UNTIL THE SILO FILL LEVEL EXCEEDS THE SILO ALARM LEVEL, FOR ALL ALARM LEVELS 0-63.

## 10. LISTING

!

:DH11 TRANSMITTER AND RECEIVER BASIC LOGIC TEST  
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;STARTING PROCEDURE  
;LOAD PROGRAM  
;LOAD ADDRESS 000200  
;PRESS START  
;PROGRAM WILL TYPE DH11 TRANSMITTER AND RECEIVER BASIC LOGIC TEST  
;PROGRAM WILL TYPE "VECTOR ADDRESS-"  
;TYPE IN THE ADDRESS OF THE RECEIVER INTERRUPT VECTOR  
;FOR THE DH11 TO BE TESTED, FOLLOWED BY <CARRIAGE RETURN>  
;PROGRAM WILL TYPE "CONTROL REGISTER ADDRESS-"  
;TYPE IN THE ADDRESS OF THE SYSTEM CONTROL REGISTER  
;FOR THE DH11 TO BE TESTED, FOLLOWED BY <CARRIAGE RETURN>  
;PROGRAM WILL TYPE "R" TO INDICATE THAT TESTING HAS STARTED  
;AT THE END OF A PASS, PROGRAM WILL TYPE " DZDHC "  
;AND THEN RESUM TESTING

## :SWITCH REGISTER OPTIONS

100000	SW15=100000	:=1,HALT ON ERROR
040000	SW14=40000	:=1,LOOP ON CURRENT TEST
020000	SW13=20000	:=1,INHIBIT ERROR TYPEOUT
010000	SW12=10000	
004000	SW11=4000	:=1,INHIBIT ITERATIONS
002000	SW10=2000	:=1,ESCAPE TO NEXT TEST ON ERROR
001000	SW09=1000	:=1,LOOP WITH CURRENT DATA
000400	SW08=400	
000100	SW06=100	
000040	SW05=40	
000020	SW04=20	

NO1

DZDHC MACY11 27(732) 16-MAR-76 09:17 PAGE 14  
DZDHCB.PFC

553	000010	SW03=10
554	000004	SW02=4
555	000002	SW01=2
556	000001	SW00=1
557		

:RESTART PROGRAM AT SELECTED TEST  
:RESELECT VECTOR AND CONTROL REGISTER  
:ADDRESS AFTER PROGRAM RESTART

## :REGISTER DEFINITIONS

000000	R0=1.0	:GENERAL REGISTER
000001	R1=1.1	:GENERAL REGISTER
000002	R2=1.2	:GENERAL REGISTER
000003	R3=1.3	:GENERAL REGISTER
000004	R4=1.4	:GENERAL REGISTER
000005	R5=1.5	:GENERAL REGISTER
000006	SP=1.6	:PROCESSOR STACK POINTER
000007	P=1.7	:PROGRAM COUNTER

## :LOCATION EQUIVALENCIES

177570	SWR=177570	:CONSOLE SWITCH REGISTER
177570	IGHTS=177570	:POP-11.45 DISPLAY REGISTER
177776	PS=177776	:PROCESSOR STATUS WORD
171200	STACK=ENCODE+200	:START OF PROCESSOR STACK

## :INSTRUCTION DEFINITIONS

005746	PUSHISP=5746	:DECREMENT PROCESSOR STACK 1 WORD
005746	POPISP=5726	:INCREMENT PROCESSOR STACK 1 WORD
005746	PUSHRO=10046	:SAVE RO ON STACK
005746	POPRO=12600	:RESTORE RO FROM STACK
005746	PUSH2SP=24646	:DECREMENT STACK TWICE
022626	POP2SP=22626	:INCREMENT STACK TWICE
022626	.EQUIV EMT,HLT	:BASIC DEFINITION OF ERROR CALL

100000	BIT15=100000
100000	BIT14=40000
100000	BIT13=20000
100000	BIT12=10000
100000	BIT11=4000
100000	BIT10=2000
100000	BIT09=1000
100000	BIT08=400
100000	BIT07=200
100000	BIT06=100
100000	BIT05=40
100000	BIT04=20
100000	BIT03=10
100000	BIT02=4
100000	BIT01=2
100000	BIT00=1

C02

•

## TRAPCATCHER FOR ILLEGAL INTERRUPTS

56:	000154	000156	.+2	:UNEXPECTED TRAP TO THIS LOCATION
56:	000156	000000	HALT	:EXAMINE STACK TO FIND CAUSE
56:	000160	000162	.+2	:UNEXPECTED TRAP TO THIS LOCATION
56:	000162	000000	HALT	:EXAMINE STACK TO FIND CAUSE
56:	000164	000156	.+2	:UNEXPECTED TRAP TO THIS LOCATION
56:	000166	000000	HALT	:EXAMINE STACK TO FIND CAUSE
56:	000170	000172	.+2	:UNEXPECTED TRAP TO THIS LOCATION
56:	000172	000000	HALT	:EXAMINE STACK TO FIND CAUSE
56:	000174	000176	.+2	:UNEXPECTED TRAP TO THIS LOCATION
56:	000176	000000	HALT	:EXAMINE STACK TO FIND CAUSE
56:	000200	000202	.+2	:UNEXPECTED TRAP TO THIS LOCATION
56:	000202	000000	HALT	:EXAMINE STACK TO FIND CAUSE
56:	000204	000206	.+2	:UNEXPECTED TRAP TO THIS LOCATION
56:	000206	000000	HALT	:EXAMINE STACK TO FIND CAUSE
56:	000210	000212	.+2	:UNEXPECTED TRAP TO THIS LOCATION
56:	000212	000000	HALT	:EXAMINE STACK TO FIND CAUSE
56:	000214	000216	.+2	:UNEXPECTED TRAP TO THIS LOCATION
56:	000216	000000	HALT	:EXAMINE STACK TO FIND CAUSE
56:	000220	000222	.+2	:UNEXPECTED TRAP TO THIS LOCATION
56:	000222	000000	HALT	:EXAMINE STACK TO FIND CAUSE
56:	000224	000226	.+2	:UNEXPECTED TRAP TO THIS LOCATION
56:	000226	000000	HALT	:EXAMINE STACK TO FIND CAUSE
56:	000230	000232	.+2	:UNEXPECTED TRAP TO THIS LOCATION
56:	000232	000000	HALT	:EXAMINE STACK TO FIND CAUSE
56:	000234	000236	.+2	:UNEXPECTED TRAP TO THIS LOCATION
56:	000236	000000	HALT	:EXAMINE STACK TO FIND CAUSE
56:	000240	000242	.+2	:UNEXPECTED TRAP TO THIS LOCATION
56:	000242	000000	HALT	:EXAMINE STACK TO FIND CAUSE
56:	000244	000246	.+2	:UNEXPECTED TRAP TO THIS LOCATION
56:	000246	000000	HALT	:EXAMINE STACK TO FIND CAUSE
56:	000250	000252	.+2	:UNEXPECTED TRAP TO THIS LOCATION
56:	000252	000000	HALT	:EXAMINE STACK TO FIND CAUSE
56:	000254	000256	.+2	:UNEXPECTED TRAP TO THIS LOCATION
56:	000256	000000	HALT	:EXAMINE STACK TO FIND CAUSE
56:	000260	000262	.+2	:UNEXPECTED TRAP TO THIS LOCATION
56:	000262	000000	HALT	:EXAMINE STACK TO FIND CAUSE
56:	000264	000266	.+2	:UNEXPECTED TRAP TO THIS LOCATION
56:	000266	000000	HALT	:EXAMINE STACK TO FIND CAUSE
56:	000270	000272	.+2	:UNEXPECTED TRAP TO THIS LOCATION
56:	000272	000000	HALT	:EXAMINE STACK TO FIND CAUSE
56:	000274	000276	.+2	:UNEXPECTED TRAP TO THIS LOCATION
56:	000276	000000	HALT	:EXAMINE STACK TO FIND CAUSE
56:	000300	000302	.+2	:UNEXPECTED TRAP TO THIS LOCATION
56:	000302	000000	HALT	:EXAMINE STACK TO FIND CAUSE
56:	000304	000306	.+2	:UNEXPECTED TRAP TO THIS LOCATION
56:	000306	000000	HALT	:EXAMINE STACK TO FIND CAUSE
56:	000310	000312	.+2	:UNEXPECTED TRAP TO THIS LOCATION
56:	000312	000000	HALT	:EXAMINE STACK TO FIND CAUSE
56:	000314	000316	.+2	:UNEXPECTED TRAP TO THIS LOCATION
56:	000316	000000	HALT	:EXAMINE STACK TO FIND CAUSE
56:	000320	000322	.+2	:UNEXPECTED TRAP TO THIS LOCATION
56:	000322	000000	HALT	:EXAMINE STACK TO FIND CAUSE
56:	000324	000326	.+2	:UNEXPECTED TRAP TO THIS LOCATION
56:	000326	000000	HALT	:EXAMINE STACK TO FIND CAUSE
56:	000330	000332	.+2	:UNEXPECTED TRAP TO THIS LOCATION
56:	000332	000000	HALT	:EXAMINE STACK TO FIND CAUSE

717	000334	000336	.+2	:UNEXPECTED TRAP TO THIS LOCATION
718	000336	000000	HALT	:EXAMINE STACK TO FIND CAUSE
719	000340	000342	.+2	:UNEXPECTED TRAP TO THIS LOCATION
720	000342	000000	HALT	:EXAMINE STACK TO FIND CAUSE
721	000344	000346	.+2	:UNEXPECTED TRAP TO THIS LOCATION
722	000346	000000	HALT	:EXAMINE STACK TO FIND CAUSE
723	000350	000352	.+2	:UNEXPECTED TRAP TO THIS LOCATION
724	000352	000000	HALT	:EXAMINE STACK TO FIND CAUSE
725	000354	000356	.+2	:UNEXPECTED TRAP TO THIS LOCATION
726	000356	000000	HALT	:EXAMINE STACK TO FIND CAUSE
727	000360	000362	.+2	:UNEXPECTED TRAP TO THIS LOCATION
728	000362	000000	HALT	:EXAMINE STACK TO FIND CAUSE
729	000364	000366	.+2	:UNEXPECTED TRAP TO THIS LOCATION
730	000366	000000	HALT	:EXAMINE STACK TO FIND CAUSE
731	000370	000372	.+2	:UNEXPECTED TRAP TO THIS LOCATION
732	000372	000000	HALT	:EXAMINE STACK TO FIND CAUSE
733	000374	000376	.+2	:UNEXPECTED TRAP TO THIS LOCATION
734	000376	000000	HALT	:EXAMINE STACK TO FIND CAUSE
735	000400	000402	.+2	:UNEXPECTED TRAP TO THIS LOCATION
736	000402	000000	HALT	:EXAMINE STACK TO FIND CAUSE
737	000404	000406	.+2	:UNEXPECTED TRAP TO THIS LOCATION
738	000406	000000	HALT	:EXAMINE STACK TO FIND CAUSE
739	000410	000412	.+2	:UNEXPECTED TRAP TO THIS LOCATION
740	000412	000000	HALT	:EXAMINE STACK TO FIND CAUSE
741	000414	000416	.+2	:UNEXPECTED TRAP TO THIS LOCATION
742	000416	000000	HALT	:EXAMINE STACK TO FIND CAUSE
743	000420	000422	.+2	:UNEXPECTED TRAP TO THIS LOCATION
744	000422	000000	HALT	:EXAMINE STACK TO FIND CAUSE
745	000424	000426	.+2	:UNEXPECTED TRAP TO THIS LOCATION
746	000426	000000	HALT	:EXAMINE STACK TO FIND CAUSE
747	000430	000432	.+2	:UNEXPECTED TRAP TO THIS LOCATION
748	000432	000000	HALT	:EXAMINE STACK TO FIND CAUSE
749	000434	000436	.+2	:UNEXPECTED TRAP TO THIS LOCATION
750	000436	000000	HALT	:EXAMINE STACK TO FIND CAUSE
751	000440	000442	.+2	:UNEXPECTED TRAP TO THIS LOCATION
752	000442	000000	HALT	:EXAMINE STACK TO FIND CAUSE
753	000444	000446	.+2	:UNEXPECTED TRAP TO THIS LOCATION
754	000446	000000	HALT	:EXAMINE STACK TO FIND CAUSE
755	000450	000452	.+2	:UNEXPECTED TRAP TO THIS LOCATION
756	000452	000000	HALT	:EXAMINE STACK TO FIND CAUSE
757	000454	000456	.+2	:UNEXPECTED TRAP TO THIS LOCATION
758	000456	000000	HALT	:EXAMINE STACK TO FIND CAUSE
759	000460	000462	.+2	:UNEXPECTED TRAP TO THIS LOCATION
760	000462	000000	HALT	:EXAMINE STACK TO FIND CAUSE
761	000464	000466	.+2	:UNEXPECTED TRAP TO THIS LOCATION
762	000466	000000	HALT	:EXAMINE STACK TO FIND CAUSE
763	000470	000472	.+2	:UNEXPECTED TRAP TO THIS LOCATION
764	000472	000000	HALT	:EXAMINE STACK TO FIND CAUSE
765	000474	000476	.+2	:UNEXPECTED TRAP TO THIS LOCATION
766	000476	000000	HALT	:EXAMINE STACK TO FIND CAUSE
767	000500	000502	.+2	:UNEXPECTED TRAP TO THIS LOCATION
768	000502	000000	HALT	:EXAMINE STACK TO FIND CAUSE
769	000504	000506	.+2	:UNEXPECTED TRAP TO THIS LOCATION
770	000506	000000	HALT	:EXAMINE STACK TO FIND CAUSE
771	000510	000512	.+2	:UNEXPECTED TRAP TO THIS LOCATION
772	000512	000000	HALT	:EXAMINE STACK TO FIND CAUSE

773	000514	000516	.+2	;UNEXPECTED TRAP TO THIS LOCATION
774	000516	000000	HALT	;EXAMINE STACK TO FIND CAUSE
775	000520	000522	.+2	;UNEXPECTED TRAP TO THIS LOCATION
776	000522	000000	HALT	;EXAMINE STACK TO FIND CAUSE
777	000524	000526	.+2	;UNEXPECTED TRAP TO THIS LOCATION
778	000526	000000	HALT	;EXAMINE STACK TO FIND CAUSE
779	000530	000532	.+2	;UNEXPECTED TRAP TO THIS LOCATION
780	000532	000000	HALT	;EXAMINE STACK TO FIND CAUSE
781	000534	000536	.+2	;UNEXPECTED TRAP TO THIS LOCATION
782	000536	000000	HALT	;EXAMINE STACK TO FIND CAUSE
783	000540	000542	.+2	;UNEXPECTED TRAP TO THIS LOCATION
784	000542	000000	HALT	;EXAMINE STACK TO FIND CAUSE
785	000544	000546	.+2	;UNEXPECTED TRAP TO THIS LOCATION
786	000546	000000	HALT	;EXAMINE STACK TO FIND CAUSE
787	000550	000552	.+2	;UNEXPECTED TRAP TO THIS LOCATION
788	000552	000000	HALT	;EXAMINE STACK TO FIND CAUSE
789	000554	000556	.+2	;UNEXPECTED TRAP TO THIS LOCATION
790	000556	000000	HALT	;EXAMINE STACK TO FIND CAUSE
791	000560	000562	.+2	;UNEXPECTED TRAP TO THIS LOCATION
792	000562	000000	HALT	;EXAMINE STACK TO FIND CAUSE
793	000564	000566	.+2	;UNEXPECTED TRAP TO THIS LOCATION
794	000566	000000	HALT	;EXAMINE STACK TO FIND CAUSE
795	000570	000572	.+2	;UNEXPECTED TRAP TO THIS LOCATION
796	000572	000000	HALT	;EXAMINE STACK TO FIND CAUSE
797	000574	000576	.+2	;UNEXPECTED TRAP TO THIS LOCATION
798	000576	000000	HALT	;EXAMINE STACK TO FIND CAUSE
799	000600	000602	.+2	;UNEXPECTED TRAP TO THIS LOCATION
800	000602	000000	HALT	;EXAMINE STACK TO FIND CAUSE
801	000604	000606	.+2	;UNEXPECTED TRAP TO THIS LOCATION
802	000606	000000	HALT	;EXAMINE STACK TO FIND CAUSE
803	000610	000612	.+2	;UNEXPECTED TRAP TO THIS LOCATION
804	000612	000000	HALT	;EXAMINE STACK TO FIND CAUSE
805	000614	000616	.+2	;UNEXPECTED TRAP TO THIS LOCATION
806	000616	000000	HALT	;EXAMINE STACK TO FIND CAUSE
807	000620	000622	.+2	;UNEXPECTED TRAP TO THIS LOCATION
808	000622	000000	HALT	;EXAMINE STACK TO FIND CAUSE
809	000624	000626	.+2	;UNEXPECTED TRAP TO THIS LOCATION
810	000626	000000	HALT	;EXAMINE STACK TO FIND CAUSE
811	000630	000632	.+2	;UNEXPECTED TRAP TO THIS LOCATION
812	000632	000000	HALT	;EXAMINE STACK TO FIND CAUSE
813	000634	000536	.+2	;UNEXPECTED TRAP TO THIS LOCATION
814	000636	000000	HALT	;EXAMINE STACK TO FIND CAUSE
815	000640	000642	.+2	;UNEXPECTED TRAP TO THIS LOCATION
816	000642	000000	HALT	;EXAMINE STACK TO FIND CAUSE
817	000644	000646	.+2	;UNEXPECTED TRAP TO THIS LOCATION
818	000646	000000	HALT	;EXAMINE STACK TO FIND CAUSE
819	000650	000652	.+2	;UNEXPECTED TRAP TO THIS LOCATION
820	000652	000000	HALT	;EXAMINE STACK TO FIND CAUSE
821	000654	000656	.+2	;UNEXPECTED TRAP TO THIS LOCATION
822	000656	000000	HALT	;EXAMINE STACK TO FIND CAUSE
823	000660	000662	.+2	;UNEXPECTED TRAP TO THIS LOCATION
824	000662	000000	HALT	;EXAMINE STACK TO FIND CAUSE
825	000664	000666	.+2	;UNEXPECTED TRAP TO THIS LOCATION
826	000666	000000	HALT	;EXAMINE STACK TO FIND CAUSE
827	000670	000672	.+2	;UNEXPECTED TRAP TO THIS LOCATION
828	000672	000000	HALT	;EXAMINE STACK TO FIND CAUSE

## GO2

DZDHC MACY11 271732 16-MAR-76 09:17 PAGE 20  
DZDHC8.PFC

929	000674	000676	.+2	:UNEXPECTED TRAP TO THIS LOCATION
930	000676	000000	HALT	;EXAMINE STACK TO FIND CAUSE
931	000700	000702	.+2	:UNEXPECTED TRAP TO THIS LOCATION
932	000702	000000	HALT	;EXAMINE STACK TO FIND CAUSE
933	000704	000706	.+2	:UNEXPECTED TRAP TO THIS LOCATION
934	000706	000000	HALT	;EXAMINE STACK TO FIND CAUSE
935	000710	000712	.+2	:UNEXPECTED TRAP TO THIS LOCATION
936	000712	000000	HALT	;EXAMINE STACK TO FIND CAUSE
937	000714	000716	.+2	:UNEXPECTED TRAP TO THIS LOCATION
938	000716	000000	HALT	;EXAMINE STACK TO FIND CAUSE
939	000720	000722	.+2	:UNEXPECTED TRAP TO THIS LOCATION
940	000722	000000	HALT	;EXAMINE STACK TO FIND CAUSE
941	000724	000726	.+2	:UNEXPECTED TRAP TO THIS LOCATION
942	000726	000000	HALT	;EXAMINE STACK TO FIND CAUSE
943	000730	000732	.+2	:UNEXPECTED TRAP TO THIS LOCATION
944	000732	000000	HALT	;EXAMINE STACK TO FIND CAUSE
945	000734	000736	.+2	:UNEXPECTED TRAP TO THIS LOCATION
946	000736	000000	HALT	;EXAMINE STACK TO FIND CAUSE
947	000740	000742	.+2	:UNEXPECTED TRAP TO THIS LOCATION
948	000742	000000	HALT	;EXAMINE STACK TO FIND CAUSE
949	000744	000746	.+2	:UNEXPECTED TRAP TO THIS LOCATION
950	000746	000000	HALT	;EXAMINE STACK TO FIND CAUSE
951	000750	000752	.+2	:UNEXPECTED TRAP TO THIS LOCATION
952	000752	000000	HALT	;EXAMINE STACK TO FIND CAUSE
953	000754	000756	.+2	:UNEXPECTED TRAP TO THIS LOCATION
954	000756	000000	HALT	;EXAMINE STACK TO FIND CAUSE
955	000760	000762	.+2	:UNEXPECTED TRAP TO THIS LOCATION
956	000762	000000	HALT	;EXAMINE STACK TO FIND CAUSE
957	000764	000766	.+2	:UNEXPECTED TRAP TO THIS LOCATION
958	000766	000000	HALT	;EXAMINE STACK TO FIND CAUSE
959	000770	000772	.+2	:UNEXPECTED TRAP TO THIS LOCATION
960	000772	000000	HALT	;EXAMINE STACK TO FIND CAUSE
961	000774	000776	.+2	:UNEXPECTED TRAP TO THIS LOCATION
962	000776	000000	HALT	;EXAMINE STACK TO FIND CAUSE

863 :STANDARD INTERRUPT VECTORS

864

865

866 .=24

867 000024 015460 PFAIL ;POWER FAIL HANDLER

868 000026 000340 340 ;SERVICE AT LEVEL 7

869 000030 014240 ERRORS ;ERROR HANDLER

870 000032 000340 340 ;SERVICE AT LEVEL 7

871 000034 014442 TRPSRV ;GENERAL HANDLER DISPATCH SERVICE

872 000036 000340 340 ;SERVICE AT LEVEL 7

873 000200 000200 .=200 JMP START ;GO TO START OF PROGRAM

874 000200 000167 000574

875

876

877

878 :DEFINITIONS FOR TRAP SUBROUTINE CALLS

879 ;POINTERS TO SUBROUTINES CAN BE FOUND STARTING

880 ;AT LOCATION "TRPTAB"

881

882 104400 SCOPE=TRAP+Y ;SCOPE LOOP AND ITERATION HANDLER

883 104401 TYPE=TRAP+Y ;TELETYPE OUTPUT ROUTINE

884 104402 OCTASC=TRAP+Y ;OCTAL TO ASCII CONVERSION

885 104403 INSTR=TRAP+Y ;INPUT ASCII STRING

886 104404 INSTER=TRAP+Y ;STRING INPUT ERROR

887 104405 PARAM=TRAP+Y ;CONVERT STRING TO OCTAL, CHECK LIMITS

888 104406 SAVNSP=TRAP+Y ;SAVE R0-R5, PC

889 104407 RESOE=TRAP+Y ;RESTORE R0-R5

890 104410 SCOPE1=TRAP+Y ;CHECK FOR FREEZE ON CURRENT DATA

891 000046 .=46

892 000046 014106 LOGICAL

893 000052 000052 .=52

894 000052 040000 40000

DZDHC MACY11 27(732) 16-MAR-76 09:17 PAGE 22  
DZDHC8.PFC

895	001000	.=1000				
896						
897					:PROGRAM INITIALIZATION	
898					:LOCK OUT INTERRUPTS	
899					:SET UP PROCESSOR STACK	
900					:SET UP POWER FAIL VECTOR	
901					:CLEAR PROGRAM FLAGS AND COUNTS	
902					:TYPE TITLE MESSAGE	
903					:DETERMINE MEMORY SIZE	
904						
905	001000	012767	000340	176770	START: MOV \$340,PS	:LOCK OUT INTERRUPTS
906	001006	012706	017102		MOV \$STACK,SP	:SET UP PROCESSOR STACK
907	001012	012737	015460	000024	MOV #PFAIL,0#24	:SET UP POWER FAIL TRAP
908	001020	005067	014426		CLR STFLG	:CLEAR TEST START FLAG
909	001024	005067	014362		CLR PASCNT	:CLEAR PASS COUNT
910	001030	005067	014360		CLR ERRCNT	:CLEAR ERROR COUNT
911	001034	005067	014350		CLR ERRFLG	:CLEAR ERROR FLAG
912	001040	005067	014344		CLR ERRFLG	:CLEAR LAST ERROR PC
913	001044	104401	C15624		TYPE ,MTITLE	:TYPE TITLE MESSAGE
914	001050	005767	014374		TST INIFLG	:CHECK INITIALIZATION FLAG
915	001054	001021			BNE VEC1	:IF NOT 0, CHECK SWITCHES FOR REINITIALIZATION
916						
917	001056	005000			CLR R0	
918	001060	012737	001072	000004	MOV #25,0#4	:SET UP TIME OUT RETURN
919	001066	005720			TST (R0)+	:WILL TRAP WHEN NO MEMORY
920	001070	000776			BR 1\$	:LOCATION RESPONDED, CONTINUE
921	001072	010067	014360		MOV R0,HCORE	:R0 CONTAINS ADDRESS OF
922	001076	162767	000002	014352	SUB #2,HCORE	:NON EXISTANT MEMORY
923	001104	012737	000006	000004	MOV #6,0#4	:RESTORE TRAPCATCHER
924						
925	001112	005767	014332		TST INIFLG	:IF INITIALIZE FLAG=0
926	001116	001104			BEQ VEC2	:GET VECTOR AND CSR ADDRESS
927	001120	0327E7	000001	176442	BIT #SWOO,SWR	:IF SWOO=1, GET NEW VECTOR
928	001126	001445			BEG BEGIN	:AND CSR
929	001130	012701	000300		MOV #300,R1	
930	001134	012702	000302		MOV #302,R2	
931	001140	012703	000004		MOV #4,R3	
932	001144	010211			MOV R2,(R1)	:RESTORE TRAPCATCHER
933	001146	005012			CLR (R2)	:IN FLOATING VECTOR AREA
934	001150	060301			ADD R3,R1	
935	001152	060302			ADD R3,R2	
936	001154	020127	001000		CMP R1,#1000	
937	001160	001371			BNE 1\$	
938	001162	104403			INSTR	:INPUT ADDRESS OF DEVICE VECTOR
939	001164	015703			MVECTOR	:MESSAGE "VECTOR ADDRESS-"
940	001166	104405			104405	:CONVERT STRING TO OCTAL
941	001170	000300			300	:LOW LIMIT
942	001172	000770			770	:HIGH LIMIT
943	001174	015400			DHRVEC	:LOCATIONS TO BE FILLED
944	001176	003			3	:NUMBER OF LOCATIONS
945	001177	004			4	:LSB MASK
946	001200	104403			INSTR	:INPUT ADDRESS OF DEVICE CSR
947	001202	015725			MREGAD	:MESSAGE "CONTROL REGISTER ADDRESS-"
948	001204	104405			PARAM	:CONVERT STRING TO OCTAL
949	001206	000000			O	:LOW LIMIT
950	001210	177778			177778	:HIGH LIMIT

## J02

DODMC MACY11 27(732) 16-MAR-75 09:17 PAGE 23  
DODHCB.PFC

951	001212	015356			DHSCR	:LOCATIONS TO BE FILLED
952	001214	007		.BYTE	7	:NUMBER OF LOCATIONS
953	001215	010		.BYTE	10	:LSB MASK
954	001216	016767	014152	014152	MOV DHSSR,DHSLR	:SET UP ADDRESS OF SILO
955	001224	005267	014146		INC DHSLR	:STATUS REGISTER HIGH BYTE
956	001230	005767	014214		TST INIFLG	:IF INITIALIZATION FLAG
957	001234	001002			BNE BEGIN	:IS CLEARED
958	001236	005167	014206		COM INIFLG	:SET IT
959						
960						:PROGRAM START
961						:CHECK FOR PROGRAM START AT SELECTED ADDRESS
962						
963	001242	012767	000340	176526	BEGIN: MOV #340,PS	:LOCK OUT INTERRUPTS
964	001250	012706	017102		MOV #STACK,SP	:SET UP PROCESSOR STACK
965	001254	032767	000002	176306	BIT #SW01,SWR	:IF SW01=1
966	001262	001410			BEQ 1\$	:GET PC FOR PROGRAM START
967	001264	104403			INSTR	:GET PC
968	001266	016071			MTSTPC	:MESSAGE "TEST PC"
969	001270	104405			PARAM	:CONVERT STRING TO OCTAL
970	001272	000000			O	
971	001274	017500			17500	
972	001276	000207			RETURN	
973	001300	001		.BYTE	1	
974	001301	001		.BYTE	1	
975	001302	000410			BR 2\$	
976	001304	012767	001334	014104	1\$: MOV #T1,RETURN	:NORMAL START, TEST 1
977	001312	005767	014134		TST STFLG	:IF LOOPING, BYPASS TYPEOUT
978	001316	001004			BNE 3\$	
979	001320	005167	014126		COM STFLG	
980	001324	104401	016065		TYPE MR	:TYPE "R" TO INDICATE START
981	001330	000177	014062	2\$:	JMP \$RETURN	:START TESTING

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982
983
984 ;INTERRUPT LOGIC TEST
985 ;SET CHARACTER AVAILABLE INTERRUPT ENABLE
986 ;VERIFY THAT NO INTERRUPTS OCCUR
987 001334 012767 000340 176434 T1: MOV #340,PS ;DISABLE ALL INTERRUPTS
988 001342 012767 004000 014054 MOV #4000,ICOUNT ;SET UP FOR 4000 ITERATIONS
989 001350 012767 001470 014042 MOV #3$,ESCAPE ;SET UP TO ESCAPE TO NEXT TEST
990 001356 012777 004000 013772 MOV #BIT11,JDHSCR ;MASTER CLEAR INTERFACE
991 001364 012777 001440 014006 MOV #1$,JDHRVEC ;SET UP FOR POSSIBLE
992 ;RECEIVER INTERRUPT
993 001372 012777 000340 014002 MOV #340,JDHRLVL ;SET UP FOR POSSIBLE
994 001400 012777 001454 013776 MOV #2$,JDHTVEC ;TRANSMITTER INTERRUPT
995
996 001405 012777 000340 013772 MOV #340,JCHTLVL ;SET CHARACTER AVAILABLE
997 001414 012777 000100 013734 MOV #BITC6,JDHSCR ;INTERRUPT ENABLE
998
999 001422 005067 176350 CLR PS ;ALLOW INTERRUPTS
1000 001426 000240 NOP ;WINDOW FOR INTERRUPTS
1001 001430 012767 000340 176340 MOV #340,PS ;NO INTERRUPT OCCURED
1002 001436 000414 BR 3$ ;CONTINUE
1003 001440 017705 013712 1$: MOV JDHSCR,RS ;GET CONTENTS OF SYSTEM CONTROL REGISTER
1004 001444 104000 HLT 0 ;UNEXPECTED INTERRUPT
1005 001446 012716 001470 MOV #3$, (SP) ;SET UP TO
1006 001452 000002 RTI ;RETURN FROM INTERRUPT
1007 001454 017705 013676 2$: MOV JDHSCR,RS ;GET CONTENTS OF SYSTEM CONTROL REGISTER
1008 001460 104000 HLT 0 ;UNEXPECTED INTERRUPT
1009 001462 012716 001470 MOV #3$, (SP) ;SET UPT TO
1010 001466 000002 RTI ;RETURN FROM INTERRUPT
1011 001470 016777 013706 3$: MOV JDHRLVL,JDHRVEC ;RESTORE TRAPCATCHER
1012 001476 005077 013700 MOV JDHRLVL
1013 C01502 016777 013700 013674 MOV JCHTLVL,JDHTVEC
1014 001510 005077 013672 CLR JDHTLVL
1015 C01514 104400 SCOPE ;CHECK FOR ITERATIONS, LOOP

1016
1017 ;INTERRUPT LOGIC TEST
1018 ;SET SILO OVERFLOW INTERRUPT ENABLE
1019 ;VERIFY THAT NO INTERRUPTS OCCUR
1020
1021 001516 012767 000340 176252 T2: MOV #340,PS ;DISABLE ALL INTERRUPTS
1022 001524 012767 004000 013672 MOV #4000,ICOUNT ;SET UP FOR 4000 ITERATIONS
1023 001532 012767 001652 013660 MOV #3$,ESCAPE ;SET UP TO ESCAPE TO NEXT TEST
1024 001540 012777 004000 013610 MO: #BIT11,JDHSCR ;MASTER CLEAR INTERFACE
1025 001546 012777 001622 013624 MOV #1$,JDHRVEC ;SET UP FOR POSSIBLE
1026 ;RECEIVER INTERRUPT
1027 001554 012777 000340 013620 MOV #340,JDHRLVL ;SET UP FOR POSSIBLE
1028 001562 012777 001636 013614 MOV #2$,JDHTVEC ;TRANSMITTER INTERRUPT
1029
1030 001570 012777 000340 013610 MOV #340,JCHTLVL ;SET SILO OVERFLOW
1031 001576 012777 010000 013552 MOV #BIT12,JDHSCR ;INTERRUPT ENABLE
1032
1033 001604 005067 176166 CLR PS ;ALLOW INTERRUPTS
1034 001610 000240 NOP ;WINDOW FOR INTERRUPTS
1035 001612 012767 000340 176156 MOV #340,PS ;NO INTERRUPT OCCURED
1036 001620 000414 BR 3$ ;CONTINUE
1037 001622 017705 013530 1$: MOV JDHSCR,RS ;GET CONTENTS OF SYSTEM CONTROL REGISTER

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DZDHC MACY11 27.7321 0-MAR-76 09:17 PAGE 25  
DZDHCB.PFC

1038	001626	J4000			HLT	0	;UNEXPECTED INTERRUPT	
1039	001626	012716	001652		MOV	#3\$, (SP)	;SET UP TO	
1040	001634	000002			RTI		;RETURN FROM INTERRUPT	
1041	001636	017705	013514	2\$:	MOV	#DHSCR, RS	;GET CONTENTS OF SYSTEM CONTROL REGISTER	
1042	001642	104000			HLT	0	;UNEXPECTED INTERRUPT	
1043	001644	012716	001652		MOV	#3\$, (SP)	;SET UPT TO	
1044	001650	000002			RTI		;RETURN FROM INTERRUPT	
1045	001652	016777	013524	013520	3\$:	MOV	#DHLVL, #DHRVEC	;RESTORE TRAPCATCHER
1046	001660	005077	013516		CLR	#DHLVL		
1047	001664	016777	013516	013512	MOV	#HTLVL, #DHTVEC		
1048	001672	005077	013510		CLR	#DHTLVL		
1049	001676	104400			SCOPE		;CHECK FOR ITERATIONS, LOOP	
1050								
1051							;INTERRUPT LOGIC TEST	
1052							;SET TRANSMITTER DONE INTERRUPT ENABLE	
1053							;VERIFY THAT NO INTERRUPTS OCCUR	
1054								
1055	001700	012767	000340	176070	T3:	MOV	#340, PS	;DISABLE ALL INTERRUPTS
1056	001706	012767	004000	013510		MOV	#4000, ICOUNT	;SET UP FOR 4000 ITERATIONS
1057	001714	012767	002034	013476		MOV	#3\$, ESCAPE	;SET UP TO ESCAPE TO NEXT TEST
1058	001722	012777	004000	013426		MOV	#BIT11, #DHSCR	;MASTER CLEAR INTERFACE
1059	001730	012777	002004	013442		MOV	#1\$, #DHRVEC	;SET UP FOR POSSIBLE
1060								;RECEIVER INTERRUPT
1061	001736	012777	000340	013436		MOV	#340, #DHLVL	
1062	001744	012777	002020	013432		MOV	#2\$, #DHTVEC	;SET UP FOR POSSIBLE
1063								;TRANSMITTER INTERRUPT
1064	001752	012777	000340	013426		MOV	#340, #DHTLVL	
1065	001760	012777	020000	013370		MOV	#BIT13, #DHSCR	;SET TRANSMITTER DONE
1066								;INTERRUPT ENABLE
1067	001766	005067	176004			CLR	PS	;ALLOW INTERRUPTS
1068	001772	000240				NOP		;WINDOW FOR INTERRUPTS
1069	001774	012767	000340	175774		MOV	#340, PS	;NO INTERRUPT OCCURED
1070	002002	000414				BR	3\$	;CONTINUE
1071	002004	017705	013346		1\$:	MOV	#DHSCR, RS	;GET CONTENTS OF SYSTEM CONTROL REGISTER
1072	002010	104000				HLT	0	;UNEXPECTED INTERRUPT
1073	002012	012716	002034			MOV	#3\$, (SP)	;SET UP TO
1074	002016	000002				RTI		;RETURN FROM INTERRUPT
1075	002020	017705	013332		2\$:	MOV	#DHSCR, RS	;GET CONTENTS OF SYSTEM CONTROL REGISTER
1076	002024	104000				HLT	C	;UNEXPECTED INTERRUPT
1077	002026	012716	002034			MOV	#3\$, (SP)	;SET JPT TO
1078	002032	000002				RTI		;RETURN FROM INTERRUPT
1079	002034	016777	013342	013336	3\$:	MOV	#DHLVL, #DHRVEC	;RESTORE TRAPCATCHER
1080	002042	005077	013334			CLR	#DHLVL	
1081	002046	016777	013334	013330		MOV	#HTLVL, #DHTVEC	
1082	002054	005077	013326			CLR	#DHTLVL	
1083	002060	104400				SCOPE		;CHECK FOR ITERATIONS, LOOP
1084								
1085								;INTERRUPT LOGIC TEST
1086								;SET CHARACTER AVAILABLE INTERRUPT ENABLE
1087								;SET CHARACTER AVAILABLE (MAINTENANCE MODE IS ENABLED)
1088								;VERIFY THAT AN INTERRUPT OCCURS
1089								
1090	002062	012767	000340	175706	T4:	MOV	#340, PS	;DISABLE ALL INTERRUPTS
1091	002070	012767	004000	013326		MOV	#4000, ICOUNT	;SET UP FOR 4000 ITERATIONS
1092	002076	012767	002226	013314		MOV	#3\$, ESCAPE	;SET UP TO ESCAPE TO NEXT TEST
1093	002104	012777	004000	013244		MOV	#BIT11, #DHSCR	;MASTER CLEAR INTERFACE

## M02

DZDHC MACY11 27(732) 16-MAR-76 09:17 PAGE 26  
DZDHC8.PFC

1094	002112	012777	002204	013260		MOV	#1\$, @DHRVEC	;SET UP FOR RECEIVER INTERRUPT
1095	002120	012777	000340	013254		MOV	#3\$, @DHLVL	;SET UP FOR TRANSMITTER INTERRUPT
1096	002126	012777	002212	013250		MOV	#2\$, @DHTVEC	
1097	002134	012777	000340	013244		MOV	#340, @DHTLVL	
1098	002142	012777	001000	013205		MOV	#BIT09, @DHSCR	;SET MAINTENANCE MODE
1099	002150	052777	000100	013200		BIS	#BIT06, @DHSCR	;SET CHARACTER AVAILABLE
1100								;INTERRUPT ENABLE
1101	002156	052777	000200	013172		BIS	#BIT07, @DHSCR	;FORCE INTERRUPT BY
1102								;SETTING CHARACTER AVAILABLE
1103	002164	005067	175606			CLR	PS	;ALLOW INTERRUPTS
1104	002170	000240				NOP		;WINDOW FOR INTERRUPTS
1105	002172	012767	000340	175576		MOV	#340, PS	;NO INTERRUPT OCCURED
1106	002200	104001				HLT	1	;WITH CHARACTER AVAILABLE INTERRUPT
1107								;ENABLE AND CHARACTER AVAILABLE SET
1108								;ERROR
1109	002202	000411				BR	3\$	
1110	002204	012716	002226		1\$:	MOV	#3\$, (SP)	;SET UP TO RETURN
1111	002210	000002				RTI		;FROM VALID INTERRUPT
1112	002212	017705	013140		2\$:	MOV	@DHSCR.RS	;GET CONTENTS OF SYSTEM CONTROL REGISTER
1113	002216	104000				HLT	0	;UNEXPECTED INTERRUPT
1114	002220	012716	002226			MOV	#3\$, (SP)	;SET UP TO RETURN
1115	002224	000002				RTI		;FROM UNEXPECTED INTERRUPT
1116	002226	016777	013150	013144	3\$:	MOV	DHRLVL, @DHRVEC	;RESTORE TRAPCATCHER
1117	002234	005077	013142			CLR	@DHLVL	
1118	002240	016777	013142	013136		MOV	DHTLVL, @DHTVEC	
1119	00224E	005077	013134			CLR	@DHTLVL	
1120	002252	104400				SCOPE		
1121								
1122								:INTERRUPT LOGIC TEST
1123								:SET SILO OVERFLOW INTERRUPT ENABLE
1124								:SET SILO OVERFLOW (MAINTENANCE MODE IS ENABLED)
1125								:VERIFY THAT AN INTERRUPT OCCURS
1126								
1127	002254	012767	000340	175514	T5:	MOV	#340, PS	:DISABLE ALL INTERRUPTS
1128	002262	012767	004000	013134		MOV	#4000, ICOUNT	;SET UP FOR 4000 ITERATIONS
1129	002270	012767	002420	013122		MOV	#3\$, ESCAPE	;SET UP TO ESCAPE TO NEXT TEST
1130	002276	012777	004000	013052		MOV	#BIT11, @DHSCR	;MASTER CLEAR INTERFACE
1131	002304	012777	002376	013066		MOV	#1\$, @DHRVEC	;SET UP FOR RECEIVER INTERRUPT
1132	002312	012777	000340	013062		MOV	#340, @DHLVL	
1133	002320	012777	002404	013056		MOV	#2\$, @DHTVEC	;SET UP FOR TRANSMITTER INTERRUPT
1134	002326	012777	000340	013052		MOV	#340, @DHTLVL	
1135	002334	012777	001000	013014		MOV	#BIT09, @DHSCR	;SET MAINTENANCE MODE
1136	002342	052777	040000	013006		BIS	#BIT14, @DHSCR	;SET SILO OVERFLOW
1137								;INTERRUPT ENABLE
1138	002350	052777	010000	013000		BIS	#BIT12, @DHSCR	;FORCE INTERRUPT BY
1139								;SETTING SILO OVERFLOW
1140	002356	005067	175414			CLR	PS	;ALLOW INTERRUPTS
1141	002362	000240				NOP		;WINDOW FOR INTERRUPTS
1142	002364	012767	000340	175404		MOV	#340, PS	;NO INTERRUPT OCCURED
1143	002372	104001				HLT	1	;WITH SILO OVERFLOW INTERRUPT
1144								;ENABLE AND SILO OVERFLOW SET
1145								;ERROR
1146	002374	000411				BR	3\$	
1147	002376	012716	002420		1\$:	MOV	#3\$, (SP)	;SET UP TO RETURN
1148	002402	000002			2\$:	RTI		;FROM VALID INTERRUPT
1149	002404	017735	012746			MOV	@DHSCR, RS	;GET CONTENTS OF SYSTEM CONTROL REGISTER

## NO2

DZDHC MACY11 27(732) 16-MAR-76 09:17 PAGE 27  
DZDHCB.PFC

1150	002410	104000			HLT	0	;	UNEXPECTED INTERRUPT	
1151	002412	012716	002420		MOV	*3\$, (SP)	;	SET UP TO RETURN	
1152	002416	000002			RTI		;	FROM UNEXPECTED INTERRUPT	
1153	002420	016777	012756	012752	3\$:	MOV	DHRLVL, JDHRVEC	;	RESTORE TRAPCATCHER
1154	002426	005077	012750		CLR	JDHRLVL			
1155	002432	016777	012750	012744	MOV	DHTLVL, JDHTVEC			
1156	002440	005077	012742		CLR	JDHTLVL			
1157	002444	104400			SCOPE				
1158									
1159							:	INTERRUPT LOGIC TEST	
1160							:	SET TRANSMITTER INTERRUPT ENABLE	
1161							:	SET NON EXISTATN MEMORY (MAINTENANCE MODE IS ENABLED)	
1162							:	VERIFY THAT AN INTERRUPT OCCURS	
1163									
1164	002446	012767	000340	175322	T6:	MOV	#340, PS	;	DISABLE ALL INTERRUPTS
1165	002454	012767	004000	012742		MOV	#4000, ICOUNT	;	SET UP FOR 4000 ITERATIONS
1166	002462	012767	002612	012730		MOV	#3\$, ESCAPE	;	SET UP TO ESCAPE TO NEXT TEST
1167	002470	012777	004000	012660		MOV	#BIT11, JDHSCR	;	MASTER CLEAR INTERFACE
1168	002476	012777	002576	012674		MOV	#2\$, JDHRVEC	;	SET UP FOR RECEIVER INTERRUPT
1169	002504	012777	000340	012670		MOV	#340, JDHRLVL		
1170	002512	012777	002570	012664		MOV	#1\$, JDHTVEC	;	SET UP FOR TRANSMITTER INTERRUPT
1171	002520	012777	000340	012660		MOV	#340, JDHTLVL		
1172	002526	012777	001000	012622		MOV	#8BIT9, JDHSCR	;	SET MAINTENANCE MODE
1173	002534	052777	020000	012614		BIS	#8BIT13, JDHSCR	;	SET TRANSMITTER
1174								;	INTERRUPT ENABLE
1175	002542	052777	002000	012606		BIS	#BIT10, JDHSCR	;	FORCE INTERRUPT BY
1176								;	SETTING NON EXISTATN MEMORY
1177	002550	005067	175222			CLR	PS	;	ALLOW INTERRUPTS
1178	002554	000240				NOP		;	WINDOW FOR INTERRUPTS
1179	002556	012767	000340	175212		MOV	#340, PS	;	NO INTERRUPT OCCURED
1180	002564	104001				HLT	1	;	WITH TRANSMITTER INTERRUPT
1181								;	ENABLE AND NON EXISTATN MEMORY SET
1182								;	ERROR
1183	002566	000411				BR	3\$		
1184	002570	012716	002612	. 1\$:		MOV	*3\$, (SP)	;	SET UP TO RETURN
1185	002574	000002				RTI		;	FROM VALID INTERRUPT
1186	002576	017705	012554	. 2\$:		MOV	JDHSCR, RS	;	GET CONTENTS OF SYSTEM CONTROL REGISTER
1187	002602	104000				HLT	0	;	UNEXPECTED INTERRUPT
1188	002604	012716	002612			MOV	*3\$, (SP)	;	SET UP TO RETURN
1189	002610	000002				RTI		;	FROM UNEXPECTED INTERRUPT
1190	002612	016777	012564	012560	3\$:	MOV	DHRLVL, JDHRVEC	;	RESTORE TRAPCATCHER
1191	002620	005077	012556			CLR	JDHRLVL		
1192	002624	016777	012556	012552		MOV	DHTLVL, JDHTVEC		
1193	002632	005077	012550			CLR	JDHTLVL		
1194	002636	104400				SCOPE			
1195									
1196							:	INTERRUPT LOGIC TEST	
1197							:	SET TRANSMITTER DONE INTERRUPT ENABLE	
1198							:	SET TRANSMITTER DONE (MAINTENANCE MODE IS ENABLED)	
1199							:	VERIFY THAT AN INTERRUPT OCCURS	
1200									
1201	002640	012767	000340	175130	T7:	MOV	#340, PS	;	DISABLE ALL INTERRUPTS
1202	002646	012767	004000	012550		MOV	#4000, ICOUNT	;	SET UP FOR 4000 ITERATIONS
1203	002654	012767	003004	012536		MOV	#3\$, ESCAPE	;	SET UP TO ESCAPE TO NEXT TEST
1204	002662	012777	004000	012466		MOV	#BIT11, JDHSCR	;	MASTER CLEAR INTERFACE
1205	002670	012777	002770	012502		MOV	#2\$, JDHRVEC	;	SET UP FOR RECEIVER INTERRUPT

30246 MAR211 27.732 16-MAR-75 09:17 PAGE 29  
30248.PRC

226	00276	012777	000340	012476		MOV	#340, SDHRLVL	:SET UP FOR TRANSMITTER INTERRUPT
227	00274	012777	002762	012472		MOV	#340, SDHTVEC	
228	00272	012777	000340	012466		MOV	#340, SDHTLVL	:SET MAINTENANCE MODE
229	00270	012777	001000	012430		MOV	#BIT09, SDHSCR	:SET TRANSMITTER DONE
230	00276	052777	020000	012422		BIS	#BIT13, SDHSCR	:INTERRUPT ENABLE
231	00274	052777	100000	012414		BIS	#BIT15, SDHSCR	:FORCE INTERRUPT BY
232	002742	005067	175030			CLR	PS	:SETTING TRANSMITTER DONE
233	002748	005067	175030			NOP		:ALLOW INTERRUPTS
234	002750	012767	000340	175020		MOV	#340, PS	:WINDOW FOR INTERRUPTS
235	002756	104001				HLT	:	:NO INTERRUPT OCCUPIED
236								:WITH TRANSMITTER DONE INTERRUPT
237								:ENABLE AND TRANSMITTER DONE SET
238								:ERROR
239	002760	000411				BR	3S	
240	002762	012716	003004		1S:	MOV	#3S, (SP)	:SET UP TO RETURN
241	002756	000002				RTI		:FROM VALID INTERRUPT
242	002770	017705	012362		2S:	MOV	SDHSCR, RS	:GET CONTENTS OF SYSTEM CONTROL REGISTER
243	002774	104000				HLT	0	:UNEXPECTED INTERRUPT
244	002776	012716	003004			MOV	#3S, (SP)	:SET UP TO RETURN
245	003002	000002				RTI		:FROM UNEXPECTED INTERRUPT
246	003004	016777	012372	012365	3S:	MOV	SDHRLVL, SDHRTVEC	:RESTORE TRAPCATCHER
247	003012	005077	012364	012364		CLR	SDHRLVL	
248	003016	016777	012364	012360		MOV	SDHTLVL, SDHTVEC	
249	003024	005077	012356	012356		CLR	SDHTLVL	
250	003030	104400				SCOPE		
251								
252								:NPR LOGIC TEST
253								:SET BYTE COUNT TO 1 FOR LINE 0
254								:SET BAR BIT FOR LINE 0
255								:DELAY FOR NPR
256								:VERIFY THAT BAR BIT FOR LINE 0 CLEARS
257								:VERIFY THAT TRANSMITTER DONE IS SET
258								
259	003032	012767	000340	174736	T10:	MOV	#340, PS	:DISABLE ALL INTERRUPTS
260	003040	012767	000020	012356		MOV	#20, ICOUNT	:SET UP FOR 20 ITERATIONS
261	003046	012767	003262	012344		MOV	#65, ESCAPE	:SET UP TO ESCAPE TO NEXT TEST
262	003054	012777	004000	012274		MOV	#BIT11, SDHSCR	:ISSUE MASTER CLEAR
263	003062	004767	012176			JSR	PC, CLEAR	:CLEAR ALL BUS ADDRESS
264								:AND BYTE COUNT MEMORY LOCATIONS
265	003066	012777	003150	012310		MOV	#2S, SDHTVEC	:SET UP TRANSMITTER
266	003074	012777	000340	012304		MOV	#340, SDHTLVL	:INTERRUPT VECTOR
267	003074	012777	000000	012246		MOV	#0, SDHSCR	:SELECT LINE 0
268	003102	012777	177777	012250		MOV	#-1, SDHBC	:SET BYTE COUNT TO 1
269	003110	012777	177777	012250		MOV	#1000, RD	
270	003116	012700	001000	012240		MOV	#1, SDHBAR	
271	003122	012777	000001	012240		MOV	#1, SDHBAR	:SET BAR BIT FOR
272								:LINE 0
273	003130	052777	020000	012220		BIS	#BIT13, SDHSCR	:SET TRANSMITTER INTERRUPT ENABLE
274	003136	005067	174634			CLR	PS	:ALLOW INTERRUPTS
275	003142	005067	174634		1S:	DEC	RD	:DELAY FOR NPR
276	003144	001376				BNE	1S	
277	003146	104001				HLT	1	:NO INTERRUPT OCCURED, ERROR
278	003150	005077	012202		2S:	TST	SDHSCR	:VERIFY THAT TRANSMITTER
279								:DONE IS SET
280	003154	100401				BMI	3S	
281	003156	104002				HLT	2	:TRANSMITTER DONE NOT SET, ERROR

C03

MAC 11 27.732 16-MAR-76 09:17 PAGE 29  
229.PFC

1353	003163	005777	012204	38:	TST BEQ CLR	DDHBAR 45 RE	: WAS BAR BIT CLEARED FOR LINE 0	
1354	003164	001404			MOV	DDHBAR,R4	: (RS)=EXPECTED DATA IN BUFFER ACTIVE REGISTER, 0	
1355	003166	005005			HLT	0	: (R4)=ACTUAL CONTENTS OF BUFFER ACTIVE REGISTER	
1356	003170	017704	012174		CMP BEQ	\$1, DDHBA	: BUS ACTIVE BIT NOT CLEARED, ERROR	
1357	003176	104000			MOV	DDHBAR,R4	: WAS BUS ADDRESS INCREMENTED	
1358	003204	022777	000001	45:	HLT	0	: (R4)=ACTUAL CONTENTS	
1359	003205	001405	012160		CMP BEQ	\$5	: OF BUS ADDRESS MEMORY FOR	
1360	003206	017704	012152		MOV	DDHBAR,R4	: LINE 0	
1361	003212	012705	000001		MOV	\$1, RS	: (RS)=EXPECTED VALUE OF	
1362	003216	104003			HLT	3	: BUS ADDRESS MEMORY FOR	
1363	003220	005777	012142	55:	TST BEQ	DDHBC 65	: LINE 0 1	
1364	003224	001416			MOV	DDHBC,R4	: BUS ADDRESS NOT UPDATED	
1365	003226	017704	012134		CLR	RS	: CORRECTLY, ERROR	
1366	003232	005005			HLT	4	: DID BYTE COUNT DECREMENT TO 0	
1367	003234	104004			MOV	DDHBL, DDHVEC	: (R4)=ACTUAL VALUE OF BYTE	
1368	003236	016777	012140	012134	CLR	DDHBL	: COUNT FOR LINE 0	
1369	003244	005077	012132		MOV	DDHTVL, DDHTVEC	: (RS)=EXPECTED VALUE OF BYTE	
1370	003250	016777	012132	012125	CLR	DDHTVL	: COUNT FOR LINE 0 0	
1371	003255	005077	012124		MOV	DDHTVL	: BYTE COUNT DID NOT DECREMENT TO 0, ERROR	
1372	003256	012706	001702		CLR	\$STACK, SP	: RESTORE TRAPCATCHER	
1373	003256	104000			MOV	SCOPE	: RESTORE STACK	
1374							: CHECK FOR ITERATIONS, LOOP	
1375							: NPR LOGIC TEST	
1376							: SET BYTE COUNT TO 1 FOR LINE 1	
1377							: SET BAR BIT FOR LINE 1	
1378							: DELAY FOR NPR	
1379							: VERIFY THAT BAR BIT FOR LINE 1 CLEARS	
1380							: VERIFY THAT TRANSMITTER DONE IS SET	
1381	003270	012767	000340	174500	711:	MOV	\$340, PS	: DISABLE ALL INTERRUPTS
1382	003276	012767	000020	012120		MOV	\$20, ICOUNT	: SET JP FOR 20 ITERATIONS
1383	003304	012767	003520	012105		MOV	\$65, ESCAPE	: SET UP TO ESCAPE TO NEXT TEST
1384	003312	012777	004000	012036		MOV	\$BIT11, DDHSCR	: ISSUE MASTER CLEAR
1385	003320	004767	011740		JSR	PC, CLEAR	: CLEAR ALL BUS ADDRESS	
1386							: AND BYTE COUNT MEMORY LOCATIONS	
1387	003324	012777	003406	012052		MOV	\$25, DDHTVEC	: SET UP TRANSMITTER
1388	003332	012777	000340	012045		MOV	\$340, DDHTVL	: INTERRUPT VECTOR
1389	003340	012777	000001	012010		MOV	\$1, DDHSCR	: SELECT LINE 1
1390	003346	012777	177777	01202		MOV	\$-1, DDHBC	: SET BYTE COUNT TO 1
1391	003354	012700	001000			MOV	\$1000, R0	
1392	003360	012777	000002	012002		MOV	\$2, DDHBAR	: SET BAR BIT FOR
1393	003366	052777	020000	011762		BIS	\$BIT13, DDHSCR	: LINE 1
1394	003374	005067	174376			CLR	PS	: SET TRANSMITTER INTERRUPT ENABLE
1395	003400	005300				DEC	RO	: ALLOW INTERRUPTS
1396	003402	001376				BNE	1\$	: DELAY FOR NPR
1397	003404	104001				HLT	1	: NO INTERRUPT OCCURED, ERROR

## D03

MACYII 27.7321 16-MAR-75 09:17 PAGE 30  
2225.S.PFC

1359	003406	005777	011744	2S:	TST	JDHSCR	:VERIFY THAT TRANSMITTER :DONE IS SET	
1360	003412	100401			BMI	3S		
1361	003414	104002			HLT	2		
1362	003416	005777	011746	3S:	TST	JDHBAR	:TRANSMITTER DONE NOT SET, ERROR :WAS BAR BIT CLEARED FOR LINE 1	
1363	003422	00-404			BEQ	4S		
1364	003424	005005			CLR	R5	:RS)=EXPECTED DATA IN :BUFFER ACTIVE REGISTER, 0	
1365	003426	011704	011736		MOV	JDHBAR,R4	:R4)=ACTUAL CONTENTS OF :BUFFER ACTIVE REGISTER	
1366	003428	104000			HLT	0	:BUS ACTIVE BIT NOT CLEARED, ERROR	
1367	003432	022777	000001	011722 4S:	CMP	*1,JDHBA	:WAS BUS ADDRESS INCREMENTED	
1368	003434	001405			BEQ	5S		
1369	003442	017704	011714		MOV	JDHBA,R4	:R4)=ACTUAL CONTENTS :OF BUS ADDRESS MEMORY FOR :LINE 1	
1370	003450	012705	000001		MOV	*1,R5	:RS)=EXPECTED VALUE OF :BUS ADDRESS MEMORY FOR :LINE 1	
1371	003454	104003			HLT	3	:BUS ADDRESS NOT UPDATED :CORRECTLY, ERROR	
1372	003456	005777	011704	5S:	TST	JDHBC	:DID BYTE COUNT DECREMENT TO 0	
1373	003462	001416			BEQ	6S		
1374	003464	017704	011676		MOV	JDHBC,R4	:R4)=ACTUAL VALUE OF BYTE :COUNT FOR LINE 1	
1375	003470	005005			CLR	R5	:RS)=EXPECTED VALUE OF BYTE :COUNT FOR LINE 1, 0	
1376	003472	104004			HLT	4	:BYTE COUNT DID NOT DECREMENT TO 0, ERROR	
1377	003474	016777	011702	011676	MOV	DHRLVL,JDHRVEC	;RESTORE TRAPCATCHER	
1378	003502	005077	011674		CLR	DHRLVL		
1379	003506	016777	011674	011670	MOV	DHTLVL,JDHTVEC		
1380	003514	005077	011656		CLR	DHTLVL		
1381	003520	012706	017102		MOV	*STACK,SP	:RESTORE STACK	
1382	003524	104400			SCPPE		:CHECK FOR ITERATIONS, LOOP	
1383							:NPR LOGIC TEST	
1384							:SET BYTE COUNT TO 1 FOR LINE 2	
1385							:SET BAR BIT FOR LINE 2	
1386							:DELAY FOR NPR	
1387							:VERIFY THAT BAR BIT FOR LINE 2 CLEARS	
1388							:VERIFY THAT TRANSMITTER DONE IS SET	
1389	003526	012767	000340	174242	712:	MOV	*340,FS	:DISABLE ALL INTERRUPTS
1390	003534	012767	C00020	011662	MOV	*20,1COUNT	:SET UP FOR 20 ITERATIONS	
1391	003542	012767	003756	011650	MOV	*6S,ESCAPE	:SET UP TO ESCAPE TO NEXT TEST	
1392	003550	012777	004000	011600	MOV	*BIT11,JDHSCR	:ISSUE MASTER CLEAR	
1393	003556	004767	011502		JSR	PC,CLEAR	:CLEAR ALL BUS ADDRESS :AND BYTE COUNT MEMORY LOCATIONS	
1394	003562	012777	003644	011614	MOV	*2S,JDHTVEC	:SET UP TRANSMITTER	
1395	003570	012777	000340	011610	MOV	*340,JDHTLVL	:INTERRUPT VECTOR	
1396	003576	012777	000002	011552	MOV	*2,JDHSCR	:SELECT LINE 2	
1397	003604	012777	177777	011554	MOV	*-1,JDHBC	:SET BYTE COUNT TO 1	
1398	003612	012700	001000		MOV	*1000,R0		
1399	003616	012777	000004	011544	MOV	*4,JDHBAR	:SET BAR BIT FOR :LINE 2	
1400	003624	05E777	020000	011524	BIS	*BIT13,JDHSCR	:SET TRANSMITTER INTERRUPT ENABLE	

E03

DECDC MACY11 27,732' 16-MAR-75 09:17 PAGE 31  
222405.PFC

1374	003632	005067	174140					: ALLOW INTERRUPTS
1375	003636	005300			13:	CLR	PS	; DELAY FOR NPR
1376	003640	001376				BNE	R5	
1377	003642	104001				HLT	1S	
1378	003644	005777	011505		25:	TST	JDHSCR	: NO INTERRUPT OCCUPIED, ERROR
1379								; VERIFY THAT TRANSMITTER
1380	003650	100401				BMI	3S	; DONE IS SET
1381	003652	104002				HLT	2	
1382	003654	005777	011510		25:	TST	JDHBAR	: TRANSMITTER DONE NOT SET, ERROR
1383	003660	001404				BEQ	4S	; WAS BAR BIT CLEARED FOR LINE 2
1384	003662	005005				CLR	R5	
1385	003664	017704	011500			MOV	JDHBAR, R4	: (R5)=EXPECTED DATA IN
1386								; BUFFER ACTIVE REGISTER, 0
1387								: (R4)=ACTUAL CONTENTS OF
1388	003670	104000				HLT	0	; BUFFER ACTIVE REGISTER
1389	003672	022777	000001	011464	45:	CMP	*1, JDHBA	; BUS ACTIVE BIT NOT CLEARED, ERROR
1390	003700	001405				BEQ	5S	; WAS BUS ADDRESS INCREMENTED
1391	003702	017704	011456			MOV	JDHBA, R4	
1392								: (R4)=ACTUAL CONTENTS
1393								; OF BUS ADDRESS MEMORY FOR
1394	003706	012705	000001			HLT	3	; LINE 2
1395						MOV	*1, R5	: (R5)=EXPECTED VALUE OF
1396								; BUS ADDRESS MEMORY FOR
1397	003712	104003				HLT	3	; LINE 2, 1
1398						MOV		; BUS ADDRESS NOT UPDATED
1399	003714	005777	011446		55:	TST	JDHBC	; CORRECTLY, ERROR
1400	003720	001416				BEQ	6S	; DID BYTE COUNT DECREMENT TO 0
1401	003722	017704	011440			MOV	JDHBC, R4	
1402								: (R4)=ACTUAL VALUE OF BYTE
1403	003726	005005				CLR	R5	; COUNT FOR LINE 2
1404						HLT	4	: (R5)=EXPECTED VALUE OF BYTE
1405	003730	104004				MOV	DHRLVL, JDHRVEC	; COUNT FOR LINE 2, 0
1406	003732	016777	011444	011440				; BYTE COUNT DID NOT DECREMENT TO 0, ERROR
1407	003740	005077	011436			CLR	JDHRLVL	
1408	003744	016777	011436	011432		MOV	DHTLVL, JDHTVEC	
1409	003752	005077	011430			CLR	JDHTLVL	
1410	003756	012706	017102		65:	MOV	*STACK, SP	
1411	003762	104400				SCOPE		: RESTORE STACK
1412								; CHECK FOR ITERATIONS, LOOP
1413								
1414								: NPR LOGIC TEST
1415								; SET BYTE COUNT TO 1 FOR LINE 3
1416								; SET BAR BIT FOR LINE 3
1417								; DELAY FOR NPR
1418								; VERIFY THAT BAR BIT FOR LINE 3 CLEARS
1419								; VERIFY THAT TRANSMITTER DONE IS SET
1420	003764	012767	000340	174004	T13:	MOV	*340, PS	
1421	003772	012767	000020	011424		MOV	*20, *COUNT	: DISABLE ALL INTERRUPTS
1422	004000	012767	004214	011412		MOV	*6S, *ESCAPE	; SET UP FOR 20 ITERATIONS
1423	004006	012777	004000	011342		MOV	*BIT11, JDHSCR	; SET UP TO ESCAPE TO NEXT TEST
1424	004014	004757	011244			JSR	PC, CLEAR	: ISSUE MASTER CLEAR
1425								; CLEAR ALL BUS ADDRESS
1426								; AND BYTE COUNT MEMORY LOCATIONS
1427	004020	012777	004102	011356		MOV	*25, JDHTVEC	
1428	004026	012777	000340	011352		MOV	*340, JDHRLVL	: SET UP TRANSMITTER
1429	004034	012777	000003	011314		MOV	*3, JDHSCR	; INTERRUPT VECTOR
1430	004042	012777	177777	011316		MOV	*-1, JDHBC	; SELECT LINE 3
1431								; SET BYTE COUNT TO 1

DECDC MACY11 27(732) 16-MAR-76 09:17 PAGE 32  
DDCHOB.PFC

1430	004050	012700	001000		MUV	#1000, R0		
1431	004054	012777	000010	011306	MOV	#10, DDHBAR	:SET BAR BIT FOR	
1432							:LINE 3	
1433	004062	052777	020000	011265	BIS	#BIT13, DDHSCR	:SET TRANSMITTER INTERRUPT ENABLE	
1434	004070	005067	173702		CLR	PS	:ALLOW INTERRUPTS	
1435	004074	005300			DEC	R0	:DELAY FOR NPR	
1436	004076	001376			SNE	1\$		
1437	004100	104001			HLT	1	:NO INTERRUPT OCCURED, ERROR	
1438	004102	005777	011250		2\$:	TST	:VERIFY THAT TRANSMITTER	
1439						DDHSCR	:DONE IS SET	
1440	004106	100401			BMI	3\$		
1441	004110	104002			HLT	2	:TRANSMITTER DONE NOT SET, ERROR	
1442	004112	005777	011252		TST	DDHBAR	:WAS BAR BIT CLEARED FOR LINE 3	
1443	004116	001404			BEQ	4\$		
1444	004120	005005			CLR	RS	: (RS)=EXPECTED DATA IN	
1445							: BUFFER ACTIVE REGISTER, 0	
1446	004122	017704	011242		MOV	DDHBAR,R4	: (R4)=ACTUAL CONTENTS OF	
1447							: BUFFER ACTIVE REGISTER	
1448	004126	104000			HLT	0	: BUS ACTIVE BIT NOT CLEARED, ERROR	
1449	004130	022777	000001	011226	CMP	*1, DDHBA	: WAS BUS ADDRESS INCREMENTED	
1450	004136	001405			BEQ	5\$		
1451	004140	017704	011220		MOV	DDHBA,R4	: (R4)=ACTUAL CONTENTS	
1452							: OF BUS ADDRESS MEMORY FOR	
1453							: LINE 3	
1454	004144	012705	000001		MOV	*1, RS	: (RS)=EXPECTED VALUE OF	
1455							: BUS ADDRESS MEMORY FOR	
1456							: LINE 3	
1457	004150	104003			HLT	3	: BUS ADDRESS NOT UPDATED	
1458							: CORRECTLY, ERROR	
1459	004152	005777	011210		5\$:	TST	: DID BYTE COUNT DECREMENT TO 0	
1460	004156	001416				BEQ	6\$	
1461	004160	017704	011202			MOV	DDHBC	
1462							: (R4)=ACTUAL VALUE OF BYTE	
1463	004164	005005					: COUNT FOR LINE 3	
1464						CLR	: (RS)=EXPECTED VALUE OF BY E	
1465	004166	104004					: COUNT FOR LINE 3, 0	
1466	004170	016777	011206	011202		HLT	: BYTE COUNT DID NOT DECREMENT TO 0, ERROR	
1467	004176	005077	011200			MOV	CHRLVL, DDHRVEC : RESTORE TRAPCATCHER	
1468	004202	016777	011200	011174		CLR	DDHRLVL	
1469	004210	005077	011172			MOV	DHTLVL, DDHTVEC	
1470	004214	012705	017102			CLR	DDHTLVL	
1471	004220	104400			6\$:	MOV	*STACK, SP : RESTORE STACK	
1472						SCOPE	: CHECK FOR ITERATIONS, LOOP	
1473							: NPR LOGIC TEST	
1474							: SET BYTE COUNT TO 1 FOR LINE 4	
1475							: SET BAR BIT FOR LINE 4	
1476							: DELAY FOR NPR	
1477							: VERIFY THAT BAR BIT FOR LINE 4 CLEARS	
1478							: VERIFY THAT TRANSMITTER DONE IS SET	
1479								
1480	004222	012767	000340	173546	T14:	MOV	#340, PS	: DISABLE ALL INTERRUPTS
1481	004230	012767	000020	011166		MOV	#20, ICOUNT	: SET UP FOR 20 ITERATIONS
1482	004236	012767	004452	011154		MOV	#6\$, ESCAPE	: SET UP TO ESCAPE TO NEXT TEST
1483	004244	012777	004000	011104		MOV	#BIT11, DDHSCR	: ISSUE MASTER CLEAR
1484	004252	004767	011006			JSR	PC, CLEAR	: CLEAR ALL BUS ADDRESS
1485								: AND BYTE COUNT MEMORY LOCATIONS

DDHCB MACYII 27(732) 16-MAR-76 09:17 PAGE 33  
DDHCB.PFC

1486	004256	016777	004340	011120	MOV	#2\$, DDHTVEC	;SET UP TRANSMITTER	
1487	004264	012777	000340	011114	MOV	#340, DDHTLVL	;INTERRUPT VECTOR	
1489	004272	012777	000004	011056	MOV	#4, DDHSCR	;SELECT LINE 4	
1490	004300	012777	177777	011060	MOV	#-1, DDHBC	;SET BYTE COUNT TO 1	
1491	004306	012700	001000		MOV	#1000, R0		
1492	004312	012777	000020	011050	MOV	#20, DDHBAR	;SET BAR BIT FOR	
1493	004320	052777	020000	011030	BIS	#BIT13, DDHSCR	;LINE 4	
1494	004326	005067	173-44		CLR	PS	;SET TRANSMITTER INTERRUPT ENABLE	
1495	004332	005300			PS	RO	;ALLOW INTERRUPTS	
1496	004334	001376			DEC	1\$	;DELAY FOR NPR	
1497	004336	104001			BNE	!		
1498	004340	005777	011012		HLT	!	;NO INTERRUPT OCCURED, ERROR	
1499					TST	DDHSCR	;VERIFY THAT TRANSMITTER	
1500	004344	100401			BMI	3\$	;DONE IS SET	
1501	004346	104002			HLT	2		
1502	004350	005777	011014		TST	DDHBAR	;TRANSMITTER DONE NOT SET, ERROR	
1503	004354	001404			BEQ	4\$	;WAS BAR BIT CLEARED FOR LINE 4	
1504	004356	005005			CLR	RS		
1505							; (RS)=EXPECTED DATA IN	
1506	004360	017704	011004		MOV	DDHBAR, R4	;BUFFER ACTIVE REGISTER, 0	
1507							; (R4)=ACTUAL CONTENTS OF	
1508	004364	104000			HLT	0	;BUFFER ACTIVE REGISTER	
1509	004366	022777	000001	010770	CMP	#1, DDHBA	;BUS ACTIVE BIT NOT CLEARED, ERROR	
1510	004374	001405			BEQ	5\$	;WAS BUS ADDRESS INCREMENTED	
1511	004376	017704	010762		MOV	DDHBA, R4		
1512							; (R4)=ACTUAL CONTENTS	
1513							;OF BUS ADDRESS MEMORY FOR	
1514	004402	012705	000001		MOV	#1, RS	;LINE 4	
1515							; (RS)=EXPECTED VALUE OF	
1516							;BUS ADDRESS MEMORY FOR	
1517	004406	104003			HLT	3	;LINE 4, 1	
1518							;BUS ADDRESS NOT UPDATED	
1519	004410	005777	010752		TST	DDHBC	;CORRECTLY, ERROR	
1520	004414	001416			BEQ	6\$	;DID BYTE COUNT DECREMENT TO 0	
1521	004416	017704	010744		MOV	DDHBC, R4		
1522							; (R4)=ACTUAL VALUE OF BYTE	
1523	004422	005005			CLR	RS	;COUNT FOR LINE 4	
1524							; (RS)=EXPECTED VALUE OF BYTE	
1525	004424	104004			HLT	4	;COUNT FOR LINE 4, 0	
1526	004426	016777	010750	010744	MOV	DDHRLVL, DDHRVEC	;BYTE COUNT DID NOT DECREMENT TO 0, ERROR	
1527	004434	005077	010742		CLR	DDHRLVL	;RESTORE TRAPCATHER	
1528	004440	016777	010742	010736	MOV	DDTLVL, DDHTVEC		
1529	004446	005077	010734		CLR	DDHTLV		
1530	004452	012706	017102		MOV	#STACK, SP		
1531	004456	104400			SCOPE		:RESTORE STACK	
1532							;CHECK FOR ITERATIONS, LOOP	
1533								
1534							;NPR LOGIC TEST	
1535							;SET BYTE COUNT TO 1 FOR LINE 5	
1536							;SET BAR BIT FOR LINE 5	
1537							;DELAY FOR NPR	
1538							;VERIFY THAT BAR BIT FOR LINE 5 CLEARS	
1539							;VERIFY THAT TRANSMITTER DONE IS SET	
1540	004460	012767	000340	173310	T15:	MOV	#340, PS	;DISABLE ALL INTERRUPTS
1541	004466	012767	000020	010730		MOV	#20, ICOUNT	;SET UP FOR 20 ITERATIONS

DDHC MACY11 27.7321 16-MAR-75 09:17 PAGE 34  
0224C8.PFC

1542	004474	012767	004710	010716	MUV	#6\$, ESCAPE	:SET UP TO ESCAPE TO NEXT TEST
1543	004502	012777	004000	010646	MOV	#81 <sup>1</sup> , 0DHSCR	:ISSUE MASTER CLEAR
1544	004510	004767	010550		JSR	PC,CLEAR	:CLEAR ALL BUS ADDRESS
1545							:AND BYTE COUNT MEMORY LOCATIONS
1546	004514	012777	004576	010662	MOV	#25, 0DHTVEC	:SET UP TRANSMITTER
1547	004522	012777	000340	010656	MOV	#340, 0DHTLVL	:INTERRUPT VECTOR
1548	004530	012777	000005	010620	MOV	#5, 0DHSCR	:SELECT LINE 5
1549	004535	012777	177777	010622	MOV	#-1, 0DHBC	:SET BYTE COUNT TO 1
1550	004544	012700	001000		MOV	#1000, R0	
1551	004550	012777	000040	010612	MOV	#40, 0DHBAR	:SET BAR BIT FOR
1552							:LINE 5
1553	004556	052777	020000	010572	BIS	#BIT13, 0DHSCR	:SET TRANSMITTER INTERRUPT ENABLE
1554	004554	005067	173206		CLR	PS	:ALLOW INTERRUPTS
1555	004570	005300			DEC	R0	:DELAY FOR NPR
1556	004572	001376			BNE	1\$	
1557	004574	104001			HLT	1	:NO INTERRUPT OCCURED, ERROR
1558	004576	005777	010554		TST	0DHSCR	:VERIFY THAT TRANSMITTER
1559							:DONE IS SET
1560	004602	100401			BMI	3\$	
1561	004604	104002			HLT	2	:TRANSMITTER DONE NOT SET, ERROR
1562	004606	005777	010556		TST	0DHBAR	:WAS BAR BIT CLEARED FOR LINE 5
1563	004612	001404			BEQ	4\$	
1564	004614	005005			CLR	R5	: (RS)=EXPECTED DATA IN
1565							: BUFFER ACTIVE REGISTER, 0
1566	004616	017704	010546		MOV	0DHBAR,R4	: (R4)=ACTUAL CONTENTS OF
1567							: BUFFER ACTIVE REGISTER
1568	004622	104000			HLT	0	: BUS ACTIVE BIT NOT CLEARED, ERROR
1569	004624	022777	000001	010532	CMP	#1, 0DHBA	: WAS BUS ADDRESS INCREMENTED
1570	004532	001405			BEQ	5\$	
1571	004634	017704	010524		MOV	0DHBA,R4	: (R4)=ACTUAL CONTENTS
1572							: OF BUS ADDRESS MEMORY FOR
1573							: LINE 5
1574	004640	012705	000001		MOV	#1,R5	: (RS)=EXPECTED VALUE OF
1575							: BUS ADDRESS MEMORY FOR
1576							: LINE 5, 1
1577	004644	104003			HLT	3	: BUS ADDRESS NOT UPDATED
1578							: CORRECTLY, ERROR
1579	004546	005777	010514		TST	0DHBC	: DID BYTE COUNT DECREMENT TO 0
1580	004652	001416			BEQ	6\$	
1581	004654	017704	010506		MOV	0DHBC,R4	: (R4)=ACTUAL VALUE OF BYTE
1582							: COUNT FOR LINE 5
1583	004660	005005			CLR	R5	: (RS)=EXPECTED VALUE OF BYTE
1584							: COUNT FOR LINE 5, 0
1585	004662	104004			HLT	4	: BYTE COUNT DID NOT DECREMENT TO 0, ERROR
1586	004664	016777	010512	010506	MOV	DHRLVL, 0DHRVEC	: RESTORE TRAPCATHER
1587	004672	005077	010504		CLR	0DHLVL	
1588	004676	016777	010504	010500	MOV	DHTLVL, 0DHTVEC	
1589	004704	005077	010476		CLR	0DHTLVL	
1590	004710	012706	017102		MOV	#STACK, SP	: RESTORE STACK
1591	004714	104400			SCOPE		: CHECK FOR ITERATIONS, LOOP
1592							
1593							: NPR LOGIC TEST
1594							: SET BYTE COUNT TO 1 FOR LINE 6
1595							: SET BAR BIT FOR LINE 6
1596							: DELAY FOR NPR
1597							: VERIFY THAT BAR BIT FOR LINE 6 CLEARS

1598 :VERIFY THAT TRANSMITTER DONE IS SET

1599

1600 004716 012767 000340 173052 T16: MOV #340,PS ;DISABLE ALL INTERRUPTS  
 1601 004724 012767 000020 010472 MOV #20,ICOUNT ;SET UP FOR 20 ITERATIONS  
 1602 004732 012767 005146 010460 MOV #65,ESCAPE ;SET UP TO ESCAPE TO NEXT TEST  
 1603 004740 012777 004000 010410 MOV #BIT11,JDHSCR ;ISSUE MASTER CLEAR  
 1604 004746 004767 010312 JSR PC,CLEAR ;CLEAR ALL BUS ADDRESS  
 1605 ;AND BYTE COUNT MEMORY LOCATIONS  
 1606 004752 012777 005034 010424 MOV #25,JDHTVEC ;SET UP TRANSMITTER  
 1607 004760 012777 000340 010420 MOV #340,JDHTLVL ;INTERRUPT VECTOR  
 1608 004766 012777 000006 010352 MOV #6,JDHSCR ;SELECT LINE 6  
 1609 004774 012777 177777 010364 MOV #-1,JDHBC ;SET BYTE COUNT TO 1  
 1610 005002 012700 001000 010364 MOV #1000,RO ;  
 1611 005006 012777 000100 010354 MOV #100,JDHBAR ;SET BAR BIT FOR  
 1612 ;LINE 6  
 1613 005014 052777 020000 010334 BIS #BIT13,JDHSCR ;SET TRANSMITTER INTERRUPT ENABLE  
 1614 005022 005067 172750 CLR PS ;ALLOW INTERRUPTS  
 1615 005026 005300 DEC RO ;DELAY FOR NPR  
 1616 005030 001376 BNE 1S ;  
 1617 005032 104001 HLT I ;NO INTERRUPT OCCURED, ERROR  
 1618 005034 005777 010316 2S: TST JD4SCR ;VERIFY THAT TRANSMITTER  
 1619 ;DONE IS SET  
 1620 005040 100401 BMI 3S ;  
 1621 005042 104002 HLT 2 ;TRANSMITTER DONE NOT SET. ERROR  
 1622 005044 005777 010320 3S: TST JDHBAR ;WAS BAR' BIT CLEARED FOR LINE 6  
 1623 005050 001404 BEQ 4S ;  
 1624 005052 005005 CLR R5 ;(RS)=EXPECTED DATA IN  
 1625 ;BUFFER ACTIVE REGISTER. 0  
 1626 005054 017704 010310 MOV JDHBAR,R4 ;(R4)=ACTUAL CONTENTS OF  
 1627 ;BUFFER ACTIVE REGISTER  
 1628 005060 104000 HLT 0 ;BUS ACTIVE BIT NOT CLEARED, ERROR  
 1629 005062 022777 000001 010274 4S: CMP #1.JDHBA ;WAS BUS ADDRESS INCREMENTED  
 1630 005070 001405 BEQ 5S ;  
 1631 005072 017704 010266 MOV JDHBA,R4 ;(R4)=ACTUAL CONTENTS  
 1632 ;OF BUS ADDRESS MEMORY FOR  
 1633 ;LINE 6  
 1634 005076 012705 000001 MOV #1.R5 ;(RS)=EXPECTED VALUE OF  
 1635 ;BUS ADDRESS MEMORY FOR  
 1636 ;LINE 6, 1  
 1637 005102 104003 HLT 3 ;BUS ADDRESS NOT UPDATED  
 1638 ;CORRECTLY, ERROR  
 1639 005104 005777 010256 5S: TST JDHBC ;DID BYTE COUNT DECREMENT TO 0  
 1640 005110 001416 BEQ 6S ;  
 1641 005112 017704 010250 MOV JDHBC,R4 ;(R4)=ACTUAL VALUE OF BYTE  
 1642 ;COUNT FOR LINE 6  
 1643 005116 005005 CLR R5 ;(RS)=EXPECTED VALUE OF BYTE  
 1644 ;COUNT FOR LINE 6, 0  
 1645 005120 104004 HLT 4 ;BYTE COUNT DID NOT DECREMENT TO 0. ERROR  
 1646 005122 016777 010254 010250 MOV DHRLVL,JDHRVEC ;RESTORE TRAPCATCHER  
 1647 005130 005077 010246 CLR JDHRLVL ;  
 1648 005134 016777 010246 010242 MOV DHTLVL,JDHTVEC ;  
 1649 005142 005077 010240 CLR JDHTLVL ;  
 1650 005146 012706 017102 MOV #STACK,SP ;RESTORE STACK  
 1651 005152 104400 SCOPE ;CHECK FOR ITERATIONS, LOOP  
 1652 ;  
 1653 ;NPR LOGIC TEST

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1654          :SET BYTE COUNT TO 1 FOR LINE 7
1655          :SET BAR BIT FOR LINE 7
1656          :DELAY FOR NPR
1657          :VERIFY THAT BAR BIT FOR LINE 7 CLEARS
1658          :VERIFY THAT TRANSMITTER DONE IS SET
1659

1660 005154 012767 000340 172614 T17: MOV #340,PS      :DISABLE ALL INTERRUPTS
1661 005162 012767 000020 010234    MOV #20,ICOUNT   :SET UP FOR 20 ITERATIONS
1662 005170 012767 005404 010222    MOV #65,ESCAPE   :SET UP TO ESCAPE TO NEXT TEST
1663 005176 012777 004000 010152    MOV #BIT11,JDHSCR :ISSUE MASTER CLEAR
1664 005204 004767 010054          JSR PC,CLEAR     :CLEAR ALL BUS ADDRESS
1665                      AND BYTE COUNT MEMORY LOCATIONS
1666 005210 012777 005272 010166    MOV #25,JDHTVEC   :SET UP TRANSMITTER
1667 005216 012777 000340 010162    MOV #340,JDHTLVL :INTERRUPT VECTOR
1668 005224 012777 000007 010124    MOV #7,JDHSCR    :SELECT LINE 7
1669 005232 012777 177777 010126    MOV #-1,JDHBC    :SET BYTE COUNT TO 1
1670 005240 012700 001000          MOV #1000,R0
1671 005244 012777 000200 010116    MOV #200,JDHBAR   :SET BAR BIT FOR
1672                      LINE 7
1673 005252 052777 020000 010076    BIS #BIT13,JDHSCR :SET TRANSMITTER INTERRUPT ENABLE
1674 005260 005067 172512          CLR PS
1675 005264 005300          1$: DEC RO
1676 005266 001376          BNE 1$      :DELAY FOR NPR
1677 005270 104001          HLT 1
1678 005272 005777 010060          2$: TST JDHSCR    :NO INTERRUPT OCCURRED, ERROR
1679                      VERIFY THAT TRANSMITTER
1680 005276 100401          BMI 3$      :DONE IS SET
1681 005300 104002          HLT 2
1682 005302 005777 010062          3$: TST JDHBAR   :TRANSMITTER DONE NOT SET, ERROR
1683 005306 001404          BEQ 4$      :WAS BAR BIT CLEARED FOR LINE 7
1684 005310 005005          CLR R5
1685 005312 017704 010052          MOV JDHBAR,R4   :(R5)=EXPECTED DATA IN
1686                      BUFFER ACTIVE REGISTER, 0
1687                      :ACTUAL CONTENTS OF
1688 005316 104000          HLT 0
1689 005320 022777 000001 010036 4$: CMP #1,JDHBA   :BUFFER ACTIVE REGISTER
1690 005326 001405          BEQ 5$      :BUS ACTIVE BIT NOT CLEARED, ERROR
1691 005330 017704 010030          MOV JDHBA,R4   :WAS BUS ADDRESS INCREMENTED
1692                      :(R4)=ACTUAL CONTENTS
1693                      :OF BUS ADDRESS MEMORY FOR
1694 005334 012705 000001          MOV #1,R5      :LINE 7, 1
1695                      :(R5)=EXPECTED VALUE OF
1696                      :BUS ADDRESS MEMORY FOR
1697 005340 104003          HLT 3      :LINE 7, 1
1698                      :BUS ADDRESS NOT UPDATED
1699 005342 005777 010020          5$: TST JDHBC   :CORRECTLY, ERROR
1700 005346 001416          BEQ 6$      :DID BYTE COUNT DECREMENT TO 0
1701 005350 017704 010012          MOV JDHBC,R4   :(R4)=ACTUAL VALUE OF BYTE
1702                      :COUNT FOR LINE 7
1703 005354 005005          CLR R5      :(R5)=EXPECTED VALUE OF BYTE
1704                      :COUNT FOR LINE 7, 0
1705 005356 104004          HLT 4      :BYTE COUNT DID NOT DECREMENT TO 0, ERROR
1706 005360 016777 010016 010012    MOV DHLVL,JDHRVEC :RESTORE TRAPCATCHER
1707 005366 005077 010010          CLR JDHRLVL
1708 005372 016777 010010 010004    MOV DHTLVL,JDHTVEC
1709 005400 005077 010002          CLR JDHTLVL

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## K03

DZDHC MACY11 27(732) 16-MAR-76 09:17 PAGE 37  
DZDHCB.PFC

1710	005404	012706	017102		5\$:	MOV SCOPE	*STACK,SP	:RESTORE STACK ;CHECK FOR ITERATIONS, LOOP
1711	005410	104400						
1712								
1713								:NPR LOGIC TEST
1714								:SET BYTE COUNT TO 1 FOR LINE 10
1715								:SET BAR BIT FOR LINE 10
1716								:DELAY FOR NPR
1717								:VERIFY THAT BAR BIT FOR LINE 10 CLEARS
1718								:VERIFY THAT TRANSMITTER DONE IS SET
1719								
1720	005412	012767	000340	172356	T20:	MOV	#340,PS	:DISABLE ALL INTERRUPTS
1721	005420	012767	000020	007776		MOV	#20,ICOUNT	:SET UP FOR 20 ITERATIONS
1722	005426	012767	005642	007764		MOV	#5\$,ESCAPE	:SET UP TO ESCAPE TO NEXT TEST
1723	005434	012777	004000	007714		MOV	#BIT11,JDHSCR	:ISSUE MASTER CLEAR
1724	005442	004767	007616			JSR	PC,CLEAR	:CLEAR ALL BUS ADDRESS
1725								:AND BYTE COUNT MEMORY LOCATIONS
1726	005446	012777	005530	007730		MOV	#2\$,JDHTVEC	:SET UP TRANSMITTER
1727	005454	012777	000340	007724		MOV	#340,JDHTLVL	:INTERRUPT VECTOR
1728	005462	012777	000010	007666		MOV	#10,JDHSCR	:SELECT LINE 10
1729	005470	012777	177777	007670		MOV	#-1,JDHBC	:SET BYTE COUNT TO 1
1730	005476	012700	001000			MOV	#1000,RO	
1731	005502	012777	000400	007660		MOV	#400,JDHBAR	:SET BAR BIT FOR
1732								:LINE 10
1733	005510	052777	020000	007640		BIS	#BIT13,JDHSCR	:SET TRANSMITTER INTERRUPT ENABLE
1734	005516	005067	172254			CLR	PS	:ALLOW INTERRUPTS
1735	005522	005300				DEC	RO	:DELAY FOR NPR
1736	005524	001376				BNE	1\$	
1737	005526	104001				HLT	1	:NO INTERRUPT OCCURED, ERROR
1738	005530	005777	007622		2\$:	TST	JDHSCR	:VERIFY THAT TRANSMITTER
1739								:DONE IS SET
1740	005534	100401				BMI	3\$	
1741	005536	104002				HLT	2	
1742	005540	005777	007624		3\$:	TST	JDHBAR	:TRANSMITTER DONE NOT SET, ERROR
1743	005544	001404				BEG	4\$	:WAS BAR BIT CLEARED FOR LINE 10
1744	005546	005005				CLR	R5	
1745								: (R5)=EXPECTED DATA IN
1746	005550	017704	007614			MOV	JDHBAR,R4	: BUFFER ACTIVE REGISTER, 0
1747								: (R4)=ACTUAL CONTENTS OF
1748	005554	104000				HLT	0	: BUFFER ACTIVE REGISTER
1749	005556	022777	000001	007600	4\$:	CMP	#1,JDHBA	: BUS ACTIVE BIT NOT CLEARED, ERROR
1750	005564	001405				BEQ	5\$	: WAS BUS ADDRESS INCREMENTED
1751	005566	017704	007572			MOV	JDHBA,R4	
1752								: (R4)=ACTUAL CONTENTS
1753								: OF BUS ADDRESS MEMORY FOR
1754	005572	012705	000001			MOV	#1,R5	: LINE 10
1755								: (R5)=EXPECTED VALUE OF
1756								: BUS ADDRESS MEMORY FOR
1757	005576	104003				HLT	3	: LINE 10, 1
1758								: BUS ADDRESS NOT UPDATED
1759	005600	005777	007562		5\$:	TST	JDHBC	: CORRECTLY, ERROR
1760	005604	001416				BEQ	6\$	: DID BYTE COUNT DECREMENT TO 0
1761	005606	017704	007554			MOV	JDHBC,R4	
1762								: (R4)=ACTUAL VALUE OF BYTE
1763	005612	005005				CLR	R5	: COUNT FOR LINE 10
1764								: (R5)=EXPECTED VALUE OF BYTE
1765	005614	104004				HLT	4	: COUNT FOR LINE 10, 0
								: BYTE COUNT DID NOT DECREMENT TO 0, ERROR

DZDHOC MACY11 27(732) .16-MAR-76 09:17 PAGE 38  
DZDHOCB.PFC

## M03

DZDHC MACY11 27(732) 16-MAR-76 09:17 PAGE 39  
DZDHCB.PFC

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1822
1823 006050 005005           CLR   R5      ;COUNT FOR LINE 11
1824                               ;(R5)=EXPECTED VALUE OF BYTE
1825 006052 104004           HLT   4      ;COUNT FOR LINE 11 0
1826 006054 016777 007322 007316    MOV   DHRLVL, JDHRVEC ;RESTORE TRAPCATCHER
1827 006062 005077 007314           CLR   JDHRLVL
1828 006056 016777 007314 007310    MOV   DHTLVL, JDHTVEC
1829 006074 005077 007306           CLR   JDHTLVL
1830 006100 012706 017102           MOV   #STACK,SP      ;RESTORE STACK
1831 006104 104400             SCOPE            ;CHECK FOR ITERATIONS, LOOP
1832
1833
1834
1835
1836
1837
1838
1839
1840 006106 012767 000340 171662 T22:  MOV   #340,PS      ;DISABLE ALL INTERRUPTS
1841 006114 012767 000020 007302     MOV   #20,ICOUNT   ;SET UP FOR 20 ITERATIONS
1842 006122 012767 006336 007270     MOV   #6$,ESCAPE   ;SET UP TO ESCAPE TO NEXT TEST
1843 006130 012777 004C00 007220     MOV   #BIT11,JDHSCR ;ISSUE MASTER CLEAR
1844 006136 004767 007122           JSR   PC,CLEAR    ;CLEAR ALL BUS ADDRESS
1845                               ;AND BYTE COUNT MEMORY LOCATIONS
1846 005142 012777 006224 007234     MOV   #25,JDHTVEC  ;SET UP TRANSMITTER
1847 006150 012777 000340 007230     MOV   #340,JDHTLVL ;INTERRUPT VECTOR
1848 006156 012777 000012 007172     MOV   #12,JDHSCR   ;SELECT LINE 12
1849 006164 012777 177777 007174     MOV   #-1,JDHBC    ;SET BYTE COUNT TO 1
1850 006172 012700 001000           MOV   #1000,RO      ;SET BAR BIT FOR
1851 006176 012777 002000 007164     MOV   #2000,JDHBAR ;LINE 12
1852                               ;SET TRANSMITTER INTERRUPT ENABLE
1853 006204 052777 020000 007144     BIS   #BIT13,JDHSCR ;ALLOW INTERRUPTS
1854 006212 0050E7 171560           CLR   PS          ;DELAY FOR NPR
1855 006216 005300             1$:   DEC   RO          ;NO INTERRUPT OCCURED, ERROR
1856 006220 00137E             1$:   BNE   1$          ;VERIFY THAT TRANSMITTER
1857 006222 104001             2$:   HLT   1          ;DONE IS SET
1858 006224 005777 007126           TST   JDHSCR    ;TRANSMITTER DONE NOT SET, ERROR
1859                               ;WAS BAR BIT CLEARED FOR LINE 12
1860 006230 100401             3$:   BMI   3$          ;(RS)=EXPECTED DATA IN
1861 006232 104002             HLT   2          ;BUFFER ACTIVE REGISTER, J
1862 006234 005777 007130           TST   JDHBAR    ;(R4)=ACTUAL CONTENTS OF
1863 006240 001404             BEQ   4$          ;BUFFER ACTIVE REGISTER
1864 006242 005005             CLR   RS          ;BUS ACTIVE BIT NOT CLEARED, ERROR
1865                               ;WAS BUS ADDRESS INCREMENTED
1866 003244 017704 007120           MOV   JDHBAR,R4 ;(R4)=ACTUAL CONTENTS
1867                               ;OF BUS ADDRESS MEMORY FOR
1868 006250 104000             HLT   0          ;LINE 12
1869 006252 022777 000001 007104 4$:   CMP   #1,JDHBA ;(R5)=EXPECTED VALUE OF
1870 006260 001405             BEQ   5$          ;BUS ADDRESS MEMORY FOR
1871 006262 017704 007076           MOV   JDHBA,R4 ;LINE 12, 1
1872                               ;BUS ADDRESS NOT UPDATED
1873
1874 006266 012705 000001           MOV   #1,RS
1875
1876
1877 006272 104003             HLT   3

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## NO3

DZDHC MACY11 27(732) 16-MAR-76 09:17 PAGE 40  
DZDHC.PFC

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1878
1879 006274 005777 007066      5$:    TST     @DHBC          ;CORRECTLY, ERROR
1880 005300 001416
1881 006302 017704 007060      BEQ     6$          ;DID BYTE COUNT DECREMENT TO 0
1882
1883 006306 005005      MOV     @DHBC,R4        ;(R4)=ACTUAL VALUE OF BYTE
1884
1885 006310 104004      CLR     R5          ;COUNT FOR LINE 12
1886 006312 016777 007064 007060      HLT     4          ;(R5)=EXPECTED VALUE OF BYTE
1887 006320 005077 007056      MOV     DHRLVL, @DHRVEC ;COUNT FOR LINE 12, 0
1888 006324 016777 007056 007052      CLR     @DHRLVL        ;BYTE COUNT DID NOT DECREMENT TO 0, ERROR
1889 006332 005077 007050      MOV     DHTLVL, @DHTVEC ;RESTORE TRAPCATCHER
1890 006336 012706 017102      CLR     @DHTLVL        ;RESTORE STACK
1891 006342 104400      MOV     *STACK,SP      ;CHECK FOR ITERATIONS, LOOP
1892
1893
1894
1895
1896
1897
1898
1899
1900 006344 012767 000340 171424  T23:   MOV     #340,PS          ;NPR LOGIC TEST
1901 006352 012767 000020 007044      MOV     #20,ICOUNT       ;SET BYTE COUNT TO 1 FOR LINE 13
1902 006360 012767 006574 007032      MOV     #6$,ESCAPE        ;SET BAR BIT FOR LINE 13
1903 006366 012777 004000 006762      MOV     #BIT11,@DHSCR      ;DELAY FOR NPR
1904 006374 004767 006664      JSR     PC,CLEAR        ;VERIFY THAT BAR BIT FOR LINE 13 CLEARS
1905
1906 006400 012777 006462 006776      MOV     #2$,@DHTVEC      ;VERIFY THAT TRANSMITTER DONE IS SET
1907 006406 012777 000340 006772      MOV     #340,@DHTLVL      ;DISABLE ALL INTERRUPTS
1908 006414 012777 000013 006734      MOV     #13,@DHSCR        ;SET UP FOR 20 ITERATIONS
1909 006422 012777 177777 006736      MOV     #-1,@DHBC         ;SET UP TO ESCAPE TO NEXT TEST
1910 006430 012700 001000      MOV     #1000,RO          ;ISSUE MASTER CLEAR
1911 006434 012777 004000 006726      MOV     #4000,@DHBAR        ;CLEAR ALL BUS ADDRESS
1912
1913 006442 052777 020000 006706      BIS     #BIT13,@DHSCR      ;AND BYTE COUNT MEMORY LOCATIONS
1914 006450 005067 171322      CLR     PS              ;SET UP TRANSMITTER
1915 006454 005300      DEC     RO              ;INTERRUPT VECTOR
1916 006456 001376      BNE     1$              ;SELECT LINE 13
1917 006460 104001      HLT     1              ;SET BYTE COUNT TO 1
1918 006462 005777 006670      1$:    TST     @DHSCR        ;SET BAR BIT FOR
1919
1920 006466 100401      BMI     3$              ;LINE 13
1921 006470 104002      HLT     2              ;SET TRANSMITTER INTERRUPT ENABLE
1922 006472 005777 006672      3$:    TST     @DHBAR        ;ALLOW INTERRUPTS
1923 006476 001404      BEQ     4$              ;DELAY FOR NPR
1924 006500 005005      CLR     R5              ;NO INTERRUPT OCCURED, ERROR
1925
1926
1927
1928 006502 017704 006662      MOV     @DHBAR,R4        ;VERIFY THAT TRANSMITTER
1929 006506 104000      HLT     0              ;DONE IS SET
1930 006510 022777 000001 006646  4$:    CMP     #1,@DHBA        ;TRANSMITTER DONE NOT SET, ERROR
1931 006516 001405      BEQ     5$              ;WAS BAR BIT CLEARED FOR LINE 13
1932 006520 017704 006640      MOV     @DHBA,R4        ;(R5)=EXPECTED DATA IN
1933

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MAC111 27732 16-MAR-76 09:17 PAGE 41  
22929.PFC

934	005524	012705	000001		MOV	\$1,RS	:RS1=EXPECTED VALUE OF
935							:BUS ADDRESS MEMORY FOR
936							:LINE 13.1
937	006530	104003			HLT	3	:BUS ADDRESS NOT UPDATED
938					TST	3DHBC	:CORRECTLY ERROR
939	006532	005777	005630	5S:	BEO	5S	:DID BYTE COUNT DECREMENT TO 0
940	006536	001416			MOV	3DHBC,R4	
941	006540	017704	006622		CLR	RS	:R4)=ACTUAL VALUE OF BYTE
942							:COUNT FOR LINE 13
943	006544	005005					:RS5)=EXPECTED VALUE OF BYTE
944							:COUNT FOR LINE 13.0
945	006546	104004			HLT	4	:BYTE COUNT DID NOT DECREMENT TO 0. ERROR
946	006550	016777	006626	006622	MOV	DHRLVL,3DHRCVEC	:RESTORE TRAPCATCHER
947	006556	005077	006620		CLR	3DHRLVL	
948	006560	016777	006620	006614	MOV	3HTLVL,3CHT,EC	
949	006565	005077	006612		CLR	3CHTLVL	
950	006570	012706	017102	6S:	MOV	3STACK,SP	:RESTORE STACK
951	006600	104400			SCOPE		:CHECK FOR ITERATIONS. LOOP
952							:NPR LOGIC TEST
953							:SET BYTE COUNT TO 1 FOR LINE 14
954							:SET BAR BIT FOR LINE 14
955							:DELAY FOR NPR
956							:VERIFY THAT BAR BIT FOR LINE 14 CLEARS
957							:VERIFY THAT TRANSMITTER DONE IS SET
958	006622	012767	000340	171166	T24:	MOV	0340,PS
959	006623	012767	000020	006606		MOV	020,1,COUNT
960	006626	012767	007032	006574		MOV	065,ESCAPE
961	006624	012777	004000	006524		MOV	0BIT1,3DHSCR
962	006632	004767	006426		JSR	PC,CLEAR	
963							:CLEAR ALL BUS ADDRESS
964							:AND BYTE COUNT MEMORY LOCATIONS
965	006636	012777	006720	006540		MOV	025,3DHTEVC
966	006644	012777	000340	006534		MOV	0340,3DHTLVL
967	006652	012777	000014	006476		MOV	014,3DHSCR
968	006660	012777	177777	006500		MOV	0-1,3DHBC
969	006666	012700	001000			MOV	01000,RS
970	006672	012777	010000	006470		MOV	010000,3DHBAR
971							:SET BAR BIT FOR
972							:LINE 14
973	006700	052777	020000	006450		BIS	0BIT13,3DHSCR
974	006706	005067	171064			CLR	PS
975	006712	005300				DEC	RS
976	006714	001376				BNE	1S
977	006716	104001				HLT	
978	006720	005777	006432		2S:	TST	:NO INTERRUPT OCCURED. ERROR
979							:VERIFY THAT TRANSMITTER
980							:DONE IS SET
981	006724	100401				BMI	3S
982	006726	104002				HLT	2
983	006730	005777	006434	3S:	TST	3DHBAR	:TRANSMITTER DONE NOT SET. ERROR
984	006734	001404				BEO	4S
985	006736	005005				CLR	RS
986	006740	017704	006424			MOV	3DHBAR,R4
987							:R5)=EXPECTED DATA IN
988	006744	104000					:BUFFER ACTIVE REGISTER. 0
989	006746	022777	000001	006410	4S:	HLT	:R4)=ACTUAL CONTENTS OF
						CMP	:BUFFER ACTIVE REGISTER
							:BUS ACTIVE BIT NOT CLEARED. ERROR
							:WAS BUS ADDRESS INCREMENTED

DECNC MAC111 27.732: 16-MAR-76 09:17 PAGE 42  
DDHCB.PFC

1990	006754	001405				BEQ	55		
1991	006756	011704	006402			MOV	3048A,R4	: (R4)=ACTUAL CONTENTS	
1992								: OF BUS ADDRESS MEMORY FOR	
1993								: LINE 14	
1994	006762	012705	000001			MOV	\$1,RS	: (RS)=EXPECTED VALUE OF	
1995								: BUS ADDRESS MEMOR. FOR	
1996								: LINE 14	
1997	006766	104003				HLT	3	: BUS ADDRESS NOT UPDATED	
1998								: CORRECTLY ERROR	
1999	006770	005777	006372		55:	TST	30HBC	: DID BYTE COUNT DECREMENT TO 0	
2000	006774	001416				BEQ	65		
2001	006776	017704	006364			MOV	30HBC,R4	: (R4)=ACTUAL VALUE OF BYTE	
2002								: COUNT FOR LINE 14	
2003	007002	005005				CLR	RS	: (RS)=EXPECTED VALUE OF BYTE	
2004								: COUNT FOR LINE 14	0
2005	007004	104004				HLT	4	: BYTE COUNT DID NOT DECREMENT TO 0. ERROR	
2006	007006	016777	006370	006364		MOV	DHRLVL,30HRVEC	: RESTORE TRAPCATCHER	
2007	007014	005077	006362			CLR	30HRLVL		
2008	007020	016777	006362	006356		MOV	DHTLVL,30HTVEC		
2009	007026	005077	006354			CLR	30HTLVL		
2010	007032	012706	017102		65:	MOV	*STACK,SP	: RESTORE STACK	
2011	007036	004400				SCOPE		: CHECK FOR ITERATIONS. LOOP	
2012									
2013									
2014									
2015									
2016									
2017									
2018									
2019									
2020									
2021	007040	012767	000340	170730	T25:	MOV	#340,PS	: DISABLE ALL INTERRUPTS	
2022	007046	012767	000020	006350		MOV	#20,ICOUNT	: SET UP FOR 20 ITERATIONS	
2023	007054	012767	007270	006336		MOV	#65,ESCAPE	: SET UP TO ESCAPE TO NEXT TEST	
2024	007062	012777	004000	006266		MOV	#BIT11,30HSCR	: ISSUE MASTER CLEAR	
2025	007070	004767	006170			JSR	PC,CLEAR	: CLEAR ALL BUS ADDRESS	
2026								: AND BYTE COUNT MEMORY LOCATIONS	
2027									
2028	007074	012777	007156	006302		MOV	#25,30HTVEC	: SET UP TRANSMITTER	
2029	007102	012777	000340	006276		MOV	#340,30HTLVL	: INTERRUPT VECTOR	
2030	007110	012777	000015	006240		MOV	#1E,30HSCR	: SELECT LINE 15	
2031	007116	012777	177777	005242		MOV	#-1,30HBC	: SET BYTE COUNT TO 1	
2032	007124	012700	001000			MOV	#1000,90		
2033	007130	012777	020000	006232		MOV	#20000,30H3BAR	: SET BAR BIT FOR	
2034								: LINE 15	
2035	007136	052777	020000	006212		BIS	#BIT13,30HSCR	: SET TRANSMITTER INTERRUPT ENABLE	
2036	007144	005067	170626			CLR	PC	: ALLOW INTERRUPTS	
2037	007150	005300				DEC	R0	: DELAY FOR NPR	
2038	007152	001376				BNE	1		
2039	007154	104001				HLT	1	: NO INTERRUPT OCCURED. ERROR	
2040	007156	005777	006174		25:	TST	30HSCR	: VERIFY THAT TRANSMITTER	
2041								: DONE IS SET	
2042	007162	100401				BMI	35		
2043	007164	104002				HLT	2	: TRANSMITTER DONE NOT SET. ERROR	
2044	007166	005777	006176		35:	TST	30HBAR	: WAS BAR BIT CLEARED FOR LINE 15	
2045	007172	001404				BEQ	45		
	007174	005005				CLR	RS	: (RS)=EXPECTED DATA IN	
								: BUFFER ACTIVE REGISTER. 3	

J22HC MACY11 27:7321 16-MAR-76 09:17 PAGE 43  
J22HCB.PFC

2046	007176	017704	006166		MUV	JDHBR,R4	: (R4)=ACTUAL CONTENTS OF : BUFFER ACTIVE REGISTER	
2047	007202	104000			HLT	0	: BUS ACTIVE BIT NOT CLEARED, ERROR	
2048	007204	02277	000001	006152	4S:	CMP	: WAS BUS ADDRESS INCREMENTED	
2049	007212	001405			BEQ	5S		
2050	007214	017704	006144		MOV	JDHBA,R4	: (R4)=ACTUAL CONTENTS : OF BUS ADDRESS MEMORY FOR	
2051							: LINE 15	
2052							: (RS)=EXPECTED VALUE OF : BUS ADDRESS MEMORY FOR	
2053							: LINE 15, 1	
2054	007220	012705	000001		MOV	\$1,RS	: BUS ADDRESS NOT UPDATED	
2055							: CORRECTLY, ERROR	
2056					HLT	3	: DID BYTE COUNT DECREMENT TO 0	
2057	007224	104003			TST	JDHBC		
2058					BEQ	ES		
2059	007226	005777	006134		MOV	JDHBC,R4	: (R4)=ACTUAL VALUE OF BYTE : COUNT FOR LINE 15	
2060	007232	001416			CLR	RS	: (RS)=EXPECTED VALUE OF BYTE : COUNT FOR LINE 15, 0	
2061	007234	017704	006126		HLT	4	: BYTE COUNT DID NOT DECREMENT TO 0, ERROR	
2062					MOV	CHRLVL,JDHRVEC	: RESTORE TRAPCATCHER	
2063	007240	005005			CLR	JD4RLVL		
2064					MOV	DHTLVL,JDHTVEC		
2065	007242	104004			CLR	JDHTLVL		
2066	007244	016777	006132	006126	MOV	*STACK,SP	: RESTORE STACK	
2067	007252	005077	006124		SCOPE		: CHECK FOR ITERATIONS, LOOP	
2068	007256	016777	006124	006120				
2069	007264	005077	006116					
2070	007270	012706	017102					
2071	007274	104400						
2072								
2073								
2074								
2075								
2076								
2077								
2078								
2079								
2080	007276	012767	000340	170472	T26:	MOV	*340,PS	: DISABLE ALL INTERRUPTS
2081	007304	012767	000020	006112		MOV	*20,ICOUNT	: SET UP FOR 20 ITERATIONS
2082	007312	012767	007526	006100		MOV	*65,ESCAPE	: SET UP TO ESCAPE TO NEXT TEST
2083	007320	012777	004000	006030		MOV	*BIT11,JDHSCR	: ISSUE MASTER CLEAR
2084	007326	004767	005732		JSR	PC,CLEAR	: CLEAR ALL BUS ADDRESS : AND BYTE COUNT MEMORY LOCATIONS	
2085								
2086	007332	012777	007414	006044		MOV	*25,JDHTVEC	: SET UP TRANSMITTER
2087	007340	012777	000340	006040		MOV	*340,JDHTLVL	: INTERRUPT VECTOR
2088	007348	012777	000016	006002		MOV	*16,JDHSCR	: SELECT LINE 16
2089	007354	012777	177777	006004		MOV	*-1,JDHBC	: SET BYTE COUNT TO 1
2090	007362	012700	001000			MOV	*1000,RO	
2091	007366	012777	040000	005774		MOV	*40000,JDHBR	: SET BAR BIT FOR
2092							: LINE 16	
2093	007374	052777	020000	005754		BIS	*BIT13,JDHSCR	: SET TRANSMITTER INTERRUPT ENABLE
2094	007402	005067	170370			CLR	PS	: ALLOW INTERRUPTS
2095	007406	005300				DEC	RO	: DELAY FOR NPR
2096	007410	001376				BNE	1S	
2097	007412	104001				HLT	1	: NO INTERRUPT OCCURRED, ERROR
2098	007414	005777	005736		2S:	TST	JDHSCR	: VERIFY THAT TRANSMITTER
2099								: DONE IS SET
2100	007420	100401				BMI	3S	
2101	007422	104002				HLT	2	: TRANSMITTER DONE NOT SET, ERROR

022408 MACYII 27.732 16-MAR-76 09:17 PAGE 44  
022408.PFC

2102	007424	005777	005740		35:	TST	JDHBAR	; WAS BAR BIT CLEARED FOR LINE 16
2103	007430	001404				BEQ	RS	
2104	007432	005005				CLR	RS	; (RS)=EXPECTED DATA IN
2105								; BUFFER ACTIVE REGISTER, 0
2106	007434	017704	005730			MOV	JDHBAR,R4	; (R4)=ACTUAL CONTENTS OF
2107								; BUFFER ACTIVE REGISTER
2108	007440	104000				HLT	0	; BUS ACTIVE BIT NOT CLEARED, ERROR
2109	007442	022777	000001	005714	45:	CMP	#1, JDHBA	; WAS BUS ADDRESS INCREMENTED
2110	007450	001405				BEQ	RS	
2111	007452	017704	005706			MOV	JDHBA,R4	; (R4)=ACTUAL CONTENTS
2112								; OF BUS ADDRESS MEMORY FOR
2113	007456	012705	000001			MOV	#1, RS	; LINE 16
2114								; (RS)=EXPECTED VALUE OF
2115								; BUS ADDRESS MEMORY FOR
2116	007462	104003				HLT	3	; LINE 15
2117								; BUS ADDRESS NOT UPDATED
2118	007464	005777	005676		55:	TST	JDHBC	; CORRECTLY, ERROR
2119	007470	001416				BEQ	RS	; DID BYTE COUNT DECREMENT TO 0
2120	007472	017704	005670			MOV	JDHBC,R4	
2121								; (R4)=ACTUAL VALUE OF BYTE
2122	007476	005005				CLR	RS	; COUNT FOR LINE 16
2123								; (RS)=EXPECTED VALUE OF BYTE
2124	007500	104004				HLT	4	; COUNT FOR LINE 16, 0
2125	007502	016777	005674	005670		MOV	DHRLVL, JDHRVEC	; BYTE COUNT DID NOT DECREMENT TO 0, ERROR
2126						CLR	DCHRLVL	; RESTORE TRAPCATCHER
2127	007510	005077	005666			MOV	DHTLVL, JDHTVEC	
2128	007514	016777	005666	005662		CLR	JDHTLVL	
2129	007522	005077	005660			MOV	#STACK, SP	
2130	007526	012706	017102		65:	SCOPE		; RESTORE STACK
2131	007532	104400						; CHECK FOR ITERATIONS, LOOP
2132								
2133								; NPR LOGIC TEST
2134								; SET BYTE COUNT TO 1 FOR LINE 17
2135								; SET BAR BIT FOR LINE 17
2136								; DELAY FOR NPR
2137								; VERIFY THAT BAR BIT FOR LINE 17 CLEARS
2138								; VERIFY THAT TRANSMITTER DONE IS SET
2139								
2140	007534	012767	000340	170234	727:	MOV	#340, PS	; DISABLE ALL INTERRUPTS
2141	007542	012767	000020	005654		MOV	#20, ICOUNT	; SET UP FOR 20 ITERATIONS
2142	007550	012767	007764	005642		MOV	#65, ESCAPE	; SET UP TO ESCAPE TO NEXT TEST
2143	007556	012777	004000	005572		MOV	#BIT11, JDHSCR	; ISSUE MASTER CLEAR
2144	007564	004767	005474			JSR	PC,CLEAR	; CLEAR ALL BUS ADDRESS
2145								; AND BYTE COUNT MEMORY LOCATIONS
2146	007570	012777	007652	005606		MOV	#25, JDHTVEC	; SET UP TRANSMITTER
2147	007576	012777	000340	005602		MOV	#340, JDHTLVL	; INTERRUPT VECTOR
2148	007604	012777	000017	005544		MOV	#17, JDHSCR	; SELECT LINE 17
2149	007612	012777	177777	005546		MOV	#-1, JDHBC	; SET BYTE COUNT TO 1
2150	007620	012700	001000			MOV	#1000, R0	
2151	007624	012777	100000	005536		MOV	#100000, JDHBAR	; SET BAR BIT FOR
2152								; LINE 17
2153	007632	052777	020000	005516		BIS	#BIT13, JDHSCR	; SET TRANSMITTER INTERRUPT ENABLE
2154	007640	005067	170132			CLR	PS	; ALLOW INTERRUPTS
2155	007644	005300				DEC	R0	; DELAY FOR NPR
2156	007646	001376				BNE	1\$	
2157	007650	104001				HLT	1	; NO INTERRUPT OCCURED, ERROR

22040 MACY11 27.732 16-MAR-76 09:17 PAGE 45  
22040B.PRG

2158	007652	005777	005500		2\$:	TST	JDHSCR	:VERIFY THAT TRANSMITTER ;DONE IS SET
2159	007656	100401				BMI	3S	
2160	007660	104002				HLT	2	
2161	007662	005777	005502		3\$:	TST	JDHBAR	;TRANSMITTER DONE NOT SET. ERROR ;WAS BAR BIT CLEARED FOR LINE 17
2162	007666	001404				BEQ	4S	
2163	007670	005005				CLR	R5	:RS)=EXPECTED DATA IN ;BUFFER ACTIVE REGISTER, 0
2164	007672	017704	005472			MOV	JDHBAR, R4	:R4)=ACTUAL CONTENTS OF ;BUFFER ACTIVE REGISTER
2165	007676	104000				HLT	0	:BUS ACTIVE BIT NOT CLEARED, ERROR
2166	007700	022777	000001	005456	4\$:	CMP	#1.JDHBA	;WAS BUS ADDRESS INCREMENTED
2167	007706	001405				BEQ	5S	
2168	007710	017704	005450			MOV	JDHBA, R4	:R4)=ACTUAL CONTENTS ;OF BUS ADDRESS MEMORY FOR
2169	007714	012705	000001			MOV	#1.R5	:LINE 17
2170	007720	104003				HLT	3	:RS)=EXPECTED VALUE OF ;BUS ADDRESS MEMORY FOR
2171	007722	005777	005440		5\$:	TST	JDHBC	:LINE 17, 1
2172	007726	001416				BEQ	6S	:BUS ADDRESS NOT UPDATED ;CORRECTLY, ERROR
2173	007730	017704	005432			MOV	JDHBC, R4	;DID BYTE COUNT DECREMENT TO 0
2174	007734	005005				CLR	R5	:R4)=ACTUAL VALUE OF BYTE
2175	007736	104004				HLT	4	:COUNT FOR LINE 17
2176	007740	016777	005436	005432		MOV	DHRLVL, JDHRVEC	:EXPECTED VALUE OF BYTE
2177	007746	005077	005430			CLR	JDHRLVL	:COUNT FOR LINE 17, 0
2178	007752	016777	005430	005424		MOV	DHTLVL, JDHTVEC	:BYTE COUNT DID NOT DECREMENT TO 0. ERROR
2179	007760	005077	005422			CLR	JDHTLVL	;RESTORE TRAPCATCHER
2180	007764	012706	017102		6\$:	MOV	#STACK, SP	:RESTORE STACK
2181	007770	104400				SCOPE		:CHECK FOR ITERATIONS, LOOP
2182								
2183								
2184								
2185								
2186								
2187								
2188								
2189								
2190								
2191								
2192								
2193								
2194								
2195								
2196								
2197								
2198								
2199								
2200								
2201	007772	012767	000340	167776	T30:	MOV	#340, PS	:DISABLE ALL INTERRUPTS
2202	010000	C12767	000010	005416		MOV	#10, COUNT	:SET UP FOR 10 ITERATIONS
2203	010006	012767	010140	005404		MOV	#85, ESCAPE	:SET UP TO ESCAPE TO NEXT TEST
2204	010014	012777	004000	005334		MOV	#BIT11, JDHSCR	:MASTER CLEAR INTERFACE
2205								:TO SET ALL TBMT BITS
2206	010022	004767	005236			JSR	PC,CLEAR	:CLEAR ALL BYTE COUNT AND
2207								:BUS ADDRESS MEMORY LOCATIONS
2208	010026	004757	005264			JSR	PC,LOAD	:SET ALL BYTE COUNT LOCATIONS TO -1
2209	010032	012777	000001	005330		MOV	#1, JDHBAR	:SET BAR BIT FOR LINE 0
2210	010040	005777	005312		3\$:	TST	JDHSCR	:WAIT FOR TRANSMITTER DONE
2211	010044	100375				BPL	3S	
2212	010046	012700	000020			MOV	#20, R0	:SET UP TO CHECK ALL 16 LINES
2213	010052	005077	005300			CLR	JDHSCR	:START AT LINE 0

DZDHC MACY11 27(732) 16-MAR-76 09:17 PAGE 46  
DZDHCB.PFC

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2214 010056 005001      CLR   R1           ;KEEP TRACK OF LINE NUMBER
2215 010060 012705 177777    MOV   #-1,R5      ;(RS)=EXPECTED BYTE COUNT,
2216                                     ;IF LINE NUMBER NOT = 0
2217 010064 005003      CLR   R3           ;(R3)=EXPECTED BUS ADDRESS,
2218                                     ;IF LINE NUMBER NOT = 0
2219 010066 017704 005274      MOV   ADHBC,R4     ;(P4)=ACTUAL BYTE ACCOUNT
2220 010072 017702 005266      MOV   ADHBA,R2     ;(RS)=ACTUAL BJS ADDRESS
2221 010076 027727 005254 000000  CMP   ADHSCR,#0  ;IF LINE BEING COMPARED IS LINE 0
2222 010104 001002      BNE   SS          ;EXPECTED BYTE COUNT=0
2223 010106 005005      CLR   RS          ;EXPECTED BUS ADDRESS = 1
2224 010110 005203      INC   R3          ;IS BYTE COUNT CORRECT
2225 010112 020504      CMP   R5,R4
2226 010114 001401      BEQ   SS          ;BYTE COUNT ERROR
2227 010116 104004      HLT   4           ;IS BUS ADDRESS CORRECT
2228 010120 020302      SS:   CMP   R3,R2
2229 010122 001401      BEQ   7S          ;BUS ADDRESS ERROR
2230 010124 104003      HLT   3           ;PREPARE TO CHECK NEXT LINE
2231 010126 005277 005224  T3:   INC   ADHSCR
2232 010132 005201      INC   R1          ;CONTINUE IF ALL NOT DONE
2233 010134 005300      DEC   R0          ;CHECK FOR ITERATIONS, LOOP
2234 010136 001350      BNE   4S
2235 010140 104400      SS:   SCOPE
2236
2237
2238
2239
2240
2241
2242
2243
2244
2245 010142 012767 000340 167626  T31:  MOV   #340,PS      ;DISABLE ALL INTERRUPTS
2246 010150 012767 000010 005246      MOV   #10,ICOUNT    ;SET UP FOR 10 ITERATIONS
2247 010156 012767 010310 005234      MOV   #8$,ESCAPE    ;SET UP TO ESCAPE TO NEXT TEST
2248 010164 012777 004000 005164      MOV   #BIT11,ADHSCR  ;MASTER CLEAR INTERFACE
2249                                     ;TO SET ALL TBMT BITS
2250 010172 004767 005066      JSR   PC,CLEAR    ;CLEAR ALL BYTE COUNT AND
2251                                     ;BUS ADDRESS MEMORY LOCATIONS
2252 010176 004767 005114      JSR   PC,LOAD     ;SET ALL BYTE COUNT LOCATIONS TO -1
2253 010202 012777 000002 005160  3S:   MOV   #2,ADHBAR    ;SET BAR BIT FOR LINE 1
2254 010210 005777 005142      TST   ADHSCR     ;WAIT FOR TRANSMITTER DONE
2255 010214 100375      BPL   3S          ;SET UP TO CHECK ALL 16 LINES
2256 010216 012700 000020      MOV   #20,R0      ;START AT LINE 0
2257 010222 005077 005130      CLR   ADHSCR    ;KEEP TRACK OF LINE NUMBER
2258 010226 005001      CLR   R1          ;(RS)=EXPECTED BYTE COUNT.
2259 010230 012705 177777      4S:   MOV   #-1,R5      ;IF LINE NUMBER NOT = 1
2260                                     ;(R3)=EXPECTED BUS ADDRESS.
2261 010234 005003      CLR   R3          ;IF LINE NUMBER NOT = 1
2262                                     ;(R3)=EXPECTED BUS ADDRESS.
2263 010236 017704 005124      MOV   ADHBC,R4     ;(R4)=ACTUAL BYTE ACCOUNT
2264 010242 017702 005116      MOV   ADHBA,R2     ;(RS)=ACTUAL BJS ADDRESS
2265 010246 027727 005104 000001  CMP   ADHSCR,#1  ;IF LINE BEING COMPARED IS LINE 1
2266 010254 001002      BNE   SS          ;EXPECTED BYTE COUNT=0
2267 010256 005005      CLR   RS          ;EXPECTED BUS ADDRESS = 1
2268 010260 005203      INC   R3          ;IS BYTE COUNT CORRECT
2269 010262 020504      SS:   CMP   RS,R4

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DZDHC MACY11 27.7321 16-MAR-75 09:17 PAGE 47  
DZDHB.PFC

2270	010264	001401				BEQ	6\$		
2271	010266	104004				HLT	4	:BYTE COUNT ERROR	
2272	010270	020302				CMP	R3,R2	:IS BUS ADDRESS CORRECT	
2273	010272	001401				BEQ	7\$		
2274	010274	104003				HLT	3	:BUS ADDRESS ERROR	
2275	010276	005277	005054			INC	ADHSCR	:PREPARE TO CHECK NEXT LINE	
2276	010302	005201				INC	R1		
2277	010304	005300				DEC	R0	:CONTINUE IF ALL NOT DONE	
2278	010306	001350				BNE	4\$		
2279	010310	104400				SCOPE		:CHECK FOR ITERATIONS. LOOP	
2280									
2281								:NPR LOGIC TEST	
2282								:SET BYTE COUNT ON ALL LINES TO 1	
2283								:SET BAR BIT FOR LINE 2	
2284								:VERIFY THAT BYTE COUNT FOR LINE 2 GOES TO 0	
2285								:VERIFY THAT BUS ADDRESS FOR LINE 2 IS INCREMENTED	
2286								:VERIFY THAT BYTE COUNTS AND BUS ADDRESSES FOR ALL OTHER LINES	
2287								:ARE UNCHANGED	
2288									
2289	010312	012767	000340	167456	T32:	MOV	#340,PS	:DISABLE ALL INTERRUPTS	
2290	010320	012767	000010	005076		MOV	#10,ICOUNT	:SET UP FOR 10 ITERATIONS	
2291	010326	012767	010460	005064		MOV	#8\$,ESCAPE	:SET UP TO ESCAPE TO NEXT TEST	
2292	010334	012777	004300	005014		MOV	#8111,ADHSCR	:MASTER CLEAR INTERFACE	
2293								:TO SET ALL TBMT BITS	
2294	010342	004767	004716			JSR	PC,CLEAR	:CLEAR ALL BYTE COUNT AND	
2295								:BUS ADDRESS MEMORY LOCATIONS	
2296	010346	004767	004744			JSR	PC,LOAD	:SET ALL BYTE COUNT LOCATIONS TO -1	
2297	010352	012777	000004	005010		MOV	#4,ADHBAR	:SET BAR BIT FOR LINE 2	
2298	010360	005777	004772		3\$:	TST	ADHSCR	:WAIT FOR TRANSMITTER DONE	
2299	010364	100375				BPL	3\$		
2300	010366	012700	000020			MOV	#20,R0		
2301	010372	005077	004760			CLR	ADHSCR		
2302	010376	005001				CLR	R1		
2303	010400	012705	177777		4\$:	MOV	#-1,RS		
2304						CLR	R3		
2305	010404	005003							
2306								:IF LINE NUMBER NOT = 2	
2307	010406	017704	004754			MOV	ADHBC,R4		
2308	010412	017702	004746			MOV	ADHBA,R2		
2309	010416	027727	004734	000002		CMP	ADHSCR,#2	:IF LINE BEING COMPARED IS LINE 2	
2310	010424	001002				BNE	5\$		
2311	010426	005005				CLR	R5		
2312	010430	005203				INC	R3		
2313	010432	020504			5\$:	CMP	R5,R4		
2314	010434	001401				BEQ	6\$		
2315	010436	104004				HLT	4	:BYTE COUNT ERROR	
2316	010440	020302			6\$:	CMP	R3,R2	:IS BUS ADDRESS CORRECT	
2317	010442	0C1401				BEQ	7\$		
2318	010444	104003				HLT	3	:BUS ADDRESS ERROR	
2319	010446	005277	004704		7\$:	INC	ADHSCR	:PREPARE TO CHECK NEXT LINE	
2320	010452	005201				INC	R1		
2321	010454	005300				DEC	R0		
2322	010456	001350				BNE	4\$		
2323	010460	104400			8\$:	SCOPE			
2324								:CHECK FOR ITERATIONS. LOOP	
2325									

:NPR LOGIC TEST

DDHC MACYII 27.732 16-MAR-76 09:17 PAGE 49  
DDHCB.PFC

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2326      :SET BYTE COUNT ON ALL LINES TO 1
2327      :SET BAR BIT FOR LINE 3
2328      :VERIFY THAT BYTE COUNT FOR LINE 3 GOES TO 0
2329      :VERIFY THAT BUS ADDRESS FOR LINE 3 IS INCREMENTED
2330      :VERIFY THAT BYTE COUNTS AND BUS ADDRESSES FOR ALL OTHER LINES
2331      :ARE UNCHANGED
2332
2333 010462 012767 000340 167306 T33: MOV #340,PS      ;DISABLE ALL INTERRUPTS
2334 010470 012767 000010 004726   MOV #10,ICOUNT    ;SET UP FOR 10 ITERATIONS
2335 01047E 012767 010630 004714   MOV #85,ESCAPE    ;SET UP TO ESCAPE TO NEXT TEST
2336 010504 012777 004000 004644   MOV #BIT11,DDHSCR ;MASTER CLEAR INTERFACE
2337                               ;TO SET ALL TBMT BITS
2338 010512 004767 004546      JSR PC,CLEAR      ;CLEAR ALL BYTE COUNT AND
2339                               ;BUS ADDRESS MEMORY LOCATIONS
2340 010516 004767 004574      JSR PC,LOAD       ;SET ALL BYTE COUNT LOCATIONS TO -1
2341 010522 012777 000010 004640   MOV #10,DDHSBAR   ;SET BAR BIT FOR LINE 3
2342 010530 005777 004622      TST DDHSCR        ;WAIT FOR TRANSMITTER DONE
2343 010534 100375          BP_ 3$           ;SET UP TO CHECK ALL 16 LINES
2344 010536 012700 000020      MOV #20,R0        ;START AT LINE 0
2345 010542 005077 004610      CLR DDHSCR        ;KEEP TRACK OF LINE NUMBER
2346 010546 005001          CLR R1           ;(R5)=EXPECTED BYTE COUNT,
2347 010550 012705 177777      MOV #-1,R5        ;IF LINE NUMBER NOT = 3
2348                               ;(R3)=EXPECTED BUS ADDRESS.
2349 010554 005003          CLR R3           ;IF LINE NUMBER NOT = 3
2350                               ;(R4)=ACTUAL BYTE ACCOUNT
2351 010556 017704 004604      MOV DDHBC,R4     ;(R5)=ACTUAL BUS ADDRESS
2352 010562 017702 004576      MOV DDHBA,R2     ;:IF LINE BEING COMPARED IS LINE 3
2353 010566 027727 004564 000003  CMP DDHSCR,#3
2354 010574 001002          BNE 5$           ;EXPECTED BYTE COUNT=0
2355 010576 005005          CLR R5           ;EXPECTED BUS ADDRESS = 1
2356 010600 005203          INC R3           ;IS BYTE COUNT CORRECT
2357 010602 020504          CMP R5,R4        ;IS BUS ADDRESS CORRECT
2358 010604 001401          BEQ 6$           ;BYTE COUNT ERROR
2359 010606 104004          HLT 4            ;IS BUS ADDRESS CORRECT
2360 010610 020302          CMP R3,R2        ;BUS ADDRESS ERROR
2361 010612 001401          BEQ 7$           ;PREPARE TO CHECK NEXT LINE
2362 010614 104003          HLT 3            ;CONTINUE IF ALL NOT DONE
2363 010616 005277 004534 7$: INC DDHSCR      ;CHECK FOR ITERATIONS, LOOP
2364 010622 005201          INC R1           ;NPR LOGIC TEST
2365 010624 005300          DEC R0           ;SET BYTE COUNT ON ALL LINES TO 1
2366 010626 001350          BNE 4$           ;SET BAR BIT FOR LINE 4
2367 010630 104400          SCOPE          ;VERIFY THAT BYTE COUNT FOR LINE 4 GOES TO 0
2368                               ;VERIFY THAT BUS ADDRESS FOR LINE 4 IS INCREMENTED
2369                               ;VERIFY THAT BYTE COUNTS AND BUS ADDRESSES FOR ALL OTHER LINES
2370                               ;ARE UNCHANGED
2371
2372      :SET BYTE COUNT ON ALL LINES TO 1
2373      :SET BAR BIT FOR LINE 4
2374      :VERIFY THAT BYTE COUNT FOR LINE 4 GOES TO 0
2375      :VERIFY THAT BUS ADDRESS FOR LINE 4 IS INCREMENTED
2376      :VERIFY THAT BYTE COUNTS AND BUS ADDRESSES FOR ALL OTHER LINES
2377      :ARE UNCHANGED
2377 010632 012767 000340 167136 T34: MOV #340,PS      ;DISABLE ALL INTERRUPTS
2378 010640 012767 000010 004556   MOV #10,ICOUNT    ;SET UP FOR 10 ITERATIONS
2379 010646 012767 011000 004544   MOV #85,ESCAPE    ;SET UP TO ESCAPE TO NEXT TEST
2380 010654 012777 004000 004474   MOV #BIT11,DDHSCR ;MASTER CLEAR INTERFACE
2381                               ;TO SET ALL TBMT BITS

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DZDHOC MACY11 27(732) 16-MAR-76 09:17 PAGE 49  
DZDHOB.PFC

2382	010662	004767	004376			JSR	PC,CLEAR	:CLEAR ALL BYTE COUNT AND :BUS ADDRESS MEMORY LOCATIONS
2383								:SET ALL BYTE COUNT LOCATIONS TO -1
2384	010666	004767	004424			JSR	PC LOAD	:SET BAR BIT FOR LINE 4
2385	010672	012777	000020	004470		MOV	#20, ZDHBAR	:WAIT FOR TRANSMITTER DONE
2386	010700	005777	004452		3\$:	TST	ZDHSCR	
2387	010704	100375				BPL	3\$	
2388	010706	012700	000020			MOV	#20, R0	:SET UP TO CHECK ALL 16 LINES
2389	010712	005077	004440			CLR	ZDHSCR	:START AT LINE 0
2390	010716	005001				CLR	R1	:KEEP TRACK OF LINE NUMBER
2391	010720	012705	177777		4\$::	MOV	#-1, RS	:(RS)=EXPECTED BYTE COUNT,
2392								:IF LINE NUMBER NOT = 4
2393	010724	005003				CLR	R3	:(R3)=EXPECTED BUS ADDRESS,
2394								:IF LINE NUMBER NOT = 4
2395	010726	017704	004434			MOV	ZDHBC,R4	:(R4)=ACTUAL BYTE ACCOUNT
2396	010732	017702	004426			MOV	ZDHBA,R2	:(R5)=ACTUAL BUS ADDRESS
2397	010736	027727	004414	000004		CMP	ZDHSCR,\$4	:IF LINE BEING COMPARED IS LINE 4
2398	010744	001002				BNE	5\$	
2399	010746	005005				CLR	R5	:EXPECTED BYTE COUNT=0
2400	010750	005203				INC	R3	:EXPECTED BUS ADDRESS = 1
2401	010752	020504			5\$::	CMP	R5,R4	:IS BYTE COUNT CORRECT
2402	010754	001401				BEQ	6\$	
2403	010756	104004				HLT	4	:BYTE COUNT ERROR
2404	010760	020302			6\$::	CMP	R3,R2	:IS E/S ADDRESS CORRECT
2405	010762	001401				BEQ	7\$	
2406	010764	104003				HLT	3	:BUS ADDRESS ERROR
2407	010766	005277	004364		7\$::	INC	ZDHSCR	:PREPARE TO CHECK NEXT LINE
2408	010772	005201				INC	R1	
2409	010774	005300				DEC	R0	:CONTINUE IF ALL NOT DONE
2410	010776	001350				BNE	4\$	
2411	011000	104400			8\$::	SCOPE		:CHECK FOR ITERATIONS, LOOP
2412								
2413								:NPR LOGIC TEST
2414								:SET BYTE COUNT ON ALL LINES TO 1
2415								:SET BAR BIT FOR LINE 5
2416								:VERIFY THAT BYTE COUNT FOR LINE 5 GOES TO 0
2417								:VERIFY THAT BUS ADDRESS FOR LINE 5 IS INCREMENTED
2418								:VERIFY THAT BYTE COUNTS AND BUS ADDRESSES FOR ALL OTHER LINES
2419								:ARE UNCHANGED
2420								
2421	011002	012767	000340	166766	T35:	MOV	#340, PS	:DISABLE ALL INTERRUPTS
2422	011010	012767	000010	004406		MOV	#10, ICOUNT	:SET UP FOR 10 ITERATIONS
2423	011016	012767	011150	004374		MOV	#8\$, ESCAPE	:SET UP TO ESCAPE TO NEXT TEST
2424	011024	012777	004000	004324		MOV	#BIT11,ZDHSCR	:MASTER CLEAR INTERFACE
2425								:TO SET ALL TBMT BITS
2426	011032	004767	004226			JSR	PC,CLEAR	:CLEAR ALL BYTE COUNT AND
2427								:BUS ADDRESS MEMORY LOCATIONS
2428	011036	004767	004254			JSR	PC LOAD	:SET ALL BYTE COUNT LOCATIONS TO -1
2429	011042	012777	000040	004320		MOV	#40, ZDHBAR	:SET BAR BIT FOR LINE 5
2430	011050	005777	004302		3\$::	TST	ZDHSCR	:WAIT FOR TRANSMITTER DONE
2431	011054	100375				BPL	3\$	
2432	011056	012700	000020			MOV	#20, R0	:SET UP TO CHECK ALL 16 LINES
2433	011062	005077	004270			CLR	ZDHSCR	:START AT LINE 0
2434	011066	005001				CLR	R1	:KEEP TRACK OF LINE NUMBER
2435	011070	012705	177777		4\$::	MOV	#-1, RS	:(RS)=EXPECTED BYTE COUNT.
2436								:IF LINE NUMBER NOT = 5
2437	011074	005003				CLR	R3	:(R3)=EXPECTED BUS ADDRESS.

DZDHC MACY11 27(732) 16-MAR-76 09:17 PAGE 50  
DZDHCB.PFC

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2438          ;IF LINE NUMBER NOT = 5
2439 011076 017704 004264      MOV 3DHBC,R4      ;(R4)=ACTUAL BYTE ACCOUNT
2440 011102 017702 004256      MOV 3DHBA,R2      ;(RS)=ACTUAL BUS ADDRESS
2441 011106 027727 004244 000005  CMP 3DHSCR,$5    ;IF LINE BEING COMPARED IS LINE 5
2442 011114 001002      BNE 5$                   ;EXPECTED BYTE COUNT=0
2443 011116 005005      CLR R5                   ;EXPECTED BUS ADDRESS = 1
2444 011120 005203      INC R3                   ;IS BYTE COUNT CORRECT
2445 011122 020504      CMP R5,R4      ;BYTE COUNT ERROR
2446 011124 001401      BEQ 6$                   ;IS BUS ADDRESS CORRECT
2447 011126 104004      HLT 4$                   ;BUS ADDRESS ERROR
2448 011130 020302      5$: CMP R3,R2      ;PREPARE TO CHECK NEXT LINE
2449 011132 001401      BEQ 7$                   ;CONTINUE IF ALL NOT DONE
2450 011134 104003      HLT 3$                   ;CHECK FOR ITERATIONS. LOOP
2451 011136 005277 004214 7$: INC 3DHSCR      ;NPR LOGIC TEST
2452 011142 005201      INC R1                   ;SET BYTE COUNT ON ALL LINES TO 1
2453 011144 005300      DEC R0                   ;SET BAR BIT FOR LINE 6
2454 011146 001350      BNE 4$                   ;VERIFY THAT BYTE COUNT FOR LINE 6 GOES TO 0
2455 011150 104400      SCOPE                  ;VERIFY THAT BUS ADDRESS FOR LINE 6 IS INCREMENTED
2456          ;VERIFY THAT BYTE COUNTS AND BUS ADDRESSES FOR ALL OTHER LINES
2457          ;ARE UNCHANGED
2458          ;DISABLE ALL INTERRUPTS
2459          ;SET UP FOR 10 ITERATIONS
2460          ;SET UP TO ESCAPE TO NEXT TEST
2461          ;MASTER CLEAR INTERFACE
2462          ;TO SET ALL TBMT BITS
2463          ;CLEAR ALL BYTE COUNT AND
2464          ;BUS ADDRESS MEMORY LOCATIONS
2465 011152 012767 000340 166616 T36: MOV #340,PS      ;SET ALL BYTE COUNT LOCATIONS TO -1
2466 011160 012767 000010 C0423E      MOV #10,ICOUNT
2467 011166 012767 011320 004224      MOV #8$,ESCAPE
2468 011174 012777 004000 004154      MOV #BIT11,3DHSCR
2469          ;SET BAR BIT FOR LINE 6
2470 011202 004767 004056      JSR PC,CLEAR      ;WAIT FOR TRANSMITTER DONE
2471          ;SET UP TO CHECK ALL 16 LINES
2472 011206 004767 004104      JSR PC,LOAD      ;START AT LINE 0
2473 011212 012777 000100 004150      MOV #100,3DHBAR
2474 011220 005777 004132      3$: TST 3DHSCR      ;KEEP TRACK OF LINE NUMBER
2475 011224 100375      BPL 3$                   ;(RS)=EXPECTED BYTE COUNT.
2476 011226 012700 000020      MOV #20,R0      ;IF LINE NUMBER NOT = 6
2477 011232 005077 004120      CLR 3DHSCR      ;(R3)=EXPECTED BUS ADDRESS.
2478 011236 005001      CLR R1                   ;IF LINE NUMBER NOT = 6
2479 011240 012705 177777      4$: MOV #-1,RS      ;(R4)=ACTUAL BYTE ACCOUNT
2480          ;(RS)=ACTUAL BUS ADDRESS
2481 011244 005003      CLR R3                   ;IF LINE BEING COMPARED IS LINE 6
2482          ;EXPECTED BYTE COUNT=0
2483 011246 017704 004114      MOV 3DHBC,R4      ;EXPECTED BUS ADDRESS = 1
2484 011252 017702 004106      MOV 3DHBA,R2      ;IS BYTE COUNT CORRECT
2485 011256 027727 004074 000006  CMP 3DHSCR,$6    ;BYTE COUNT ERROR
2486 011264 001002      BNE 5$                   ;IS BUS ADDRESS CORRECT
2487 011266 005005      CLR R5                   ;NPR LOGIC TEST
2488 011270 005203      INC R3                   ;SET BYTE COUNT ON ALL LINES TO 1
2489 011272 020504      5$: CMP R5,R4      ;SET BAR BIT FOR LINE 6
2490 011274 001401      BEQ 6$                   ;VERIFY THAT BYTE COUNT FOR LINE 6 GOES TO 0
2491 011276 104004      HLT 4$                   ;VERIFY THAT BUS ADDRESS FOR LINE 6 IS INCREMENTED
2492 011300 020302      6$: CMP R3,R2      ;VERIFY THAT BYTE COUNTS AND BUS ADDRESSES FOR ALL OTHER LINES
2493 011302 001401      BEQ 7$                   ;ARE UNCHANGED

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2494 011304 104003  
 2495 011306 005277 004044 7\$: HLT 3 ;BUS ADDRESS ERROR  
 2496 011312 005201 INC #D4SCR ;PREPARE TO CHECK NEXT LINE  
 2497 011314 005300 INC R1 ;CONTINUE IF ALL NOT DONE  
 2498 011316 001350 DEC R0  
 2499 011320 104400 BNE 4\$ BNE SCOPE ;CHECK FOR ITERATIONS, LOOP  
 2500  
 2501 ;NPR LOGIC TEST  
 2502 ;SET BYTE COUNT ON ALL LINES TO 1  
 2503 ;SET BAR BIT FOR LINE 7  
 2504 ;VERIFY THAT BYTE COUNT FOR LINE 7 GOES TO 0  
 2505 ;VERIFY THAT BUS ADDRESS FOR LINE 7 IS INCREMENTED  
 2506 ;VERIFY THAT BYTE COUNTS AND BUS ADDRESSES FOR ALL OTHER LINES  
 2507 ;ARE UNCHANGED  
 2508  
 2509 011322 012767 000340 166446 T37: MOV #340, PS ;DISABLE ALL INTERRUPTS  
 2510 011330 012767 000010 004066 MOV #10, ICOUNT ;SET UP FOR 10 ITERATIONS  
 2511 011336 012767 011470 004054 MOV #8\$, ESCAPE ;SET UP TO ESCAPE TO NEXT TEST  
 2512 011344 012777 004000 004004 MOV #BIT11, #DHSCR ;MASTER CLEAR INTERFACE  
 2513  
 2514 011352 004767 003706 JSR PC.CLEAR ;TO SET ALL TBMT BITS  
 2515  
 2516 011356 004767 003734 JSR PC.LOAD ;CLEAR ALL BYTE COUNT AND  
 2517 011362 012777 000200 004000 MOV #200, #DHBAR ;BUS ADDRESS MEMORY LOCATIONS  
 2518 011370 005777 003762 T3\$: TST #DHSCR ;SET ALL BYTE COUNT LOCATIONS TO -1  
 2519 011374 100375 BPL 3\$ ;SET BAR BIT FOR LINE 7  
 2520 011376 012700 000020 CLR #DHSCR ;WAIT FOR TRANSMITTER DONE  
 2521 011402 005077 003750 CLR R1  
 2522 011406 005001 CLR R1 ;KEEP TRACK OF LINE NUMBER  
 2523 011410 012705 177777 4\$: MOV #-1, R5 ;(R5)=EXPECTED BYTE COUNT.  
 2524  
 2525 011414 005003 CLR R3 ;IF LINE NUMBER NOT = 7  
 2526  
 2527 011416 017704 003744 MOV #DHBC, R4 ;(R3)=EXPECTED BUS ADDRESS.  
 2528 011422 017702 003736 MOV #DHBA, R2 ;(R4)=ACTUAL BYTE ACCOUNT  
 2529 011426 027727 003724 000007 CMP #DHSCR, #7 ;(R5)=ACTUAL BUS ADDRESS  
 2530 011434 001002 BNE 5\$ ;IF LINE BEING COMPARED IS LINE 7  
 2531 011436 005005 CLR R5 ;EXPECTED BYTE COUNT=0  
 2532 011440 005203 INC R3 ;EXPECTED BUS ADDRESS = 1  
 2533 011442 020504 CMP R5, R4 ;IS BYTE COUNT CORRECT  
 2534 011444 001401 BEQ 6\$  
 2535 011446 104004 HLT 4 ;BYTE COUNT ERROR  
 2536 011450 020302 CMP R3, R2 ;IS BUS ADDRESS CORRECT  
 2537 011452 001401 BEQ 7\$  
 2538 011454 104003 HLT 3 ;BUS ADDRESS ERROR  
 2539 011456 005277 003674 7\$: INC #DHSCR ;PREPARE TO CHECK NEXT LINE  
 2540 011462 005201 INC R1 ;CONTINUE IF ALL NOT DONE  
 2541 011464 005300 DEC R0  
 2542 011466 001350 BNE 4\$ BNE SCOPE ;CHECK FOR ITERATIONS, LOOP  
 2543 011470 104400  
 2544  
 2545 ;NPR LOGIC TEST  
 2546 ;SET BYTE COUNT ON ALL LINES TO 1  
 2547 ;SET BAR BIT FOR LINE 10  
 2548 ;VERIFY THAT BYTE COUNT FOR LINE 10 GOES TO 0  
 2549 ;VERIFY THAT BJS ADDRESS FOR LINE 10 IS INCREMENTED

2550 :VERIFY THAT BYTE COUNTS AND BUS ADDRESSES FOR ALL OTHER LINES  
 2551 :ARE UNCHANGED  
 2552  
 2553 011472 012767 000340 166276 T40: MOV #340,PS :DISABLE ALL INTERRUPTS  
 2554 011500 012767 000010 003716 MOV #10,ICOUNT :SET UP FOR 10 ITERATIONS  
 2555 011506 012767 011640 003704 MOV #8\$,ESCAPE :SET UP TO ESCAPE TO NEXT TEST  
 2556 011514 012777 004000 003634 MOV #BIT11,ADHSCR :MASTER CLEAR INTERFACE  
 2557  
 2558 011522 004767 003536 JSR PC,CLEAR :TO SET ALL TBMT BITS  
 2559  
 2560 011526 004767 003564 JSR PC,LOAD :CLEAR ALL BYTE COUNT AND  
 2561 011532 012777 000400 003630 MOV #400,ADHBAR :BUS ADDRESS MEMORY LOCATIONS  
 2562 011540 005777 003612 TST ADHSCR :SET ALL BYTE COUNT LOCATIONS TO -1  
 2563 011544 100375 BPL 3\$ :SET BAR BIT FOR LINE 10  
 2564 011546 012700 000020 CLR ADHSCR :WAIT FOR TRANSMITTER DONE  
 2565 011552 005077 003600 CLR RI :SET UP TO CHECK ALL 16 LINES  
 2566 011556 005001 CLR R1 :START AT LINE 0  
 2567 011560 012705 177777 4\$: MOV #-1,R5 :KEEP TRACK OF LINE NUMBER  
 2568  
 2569 011564 005003 CLR R3 :(R5)=EXPECTED BYTE COUNT,  
 2570  
 2571 011566 017704 003574 MOV ADHBC,R4 :(R3)=EXPECTED BUS ADDRESS,  
 2572 011572 017702 003566 MOV ADHBA,R2 :(R4)=ACTUAL BYTE ACOUNT  
 2573 011576 027727 003554 000010 CMP ADHSCR,#10 ;IF LINE BEING COMPARED IS LINE 10  
 2574 011604 00002 BNE 5\$  
 2575 011606 005005 CLR R5 :EXPECTED BYTE COUNT=0  
 2576 011610 005203 INC R3 :EXPECTED BUS ADDRESS = :  
 2577 011612 020504 CMP R5,R4 :IS BYTE COUNT CORRECT  
 2578 011614 001401 BEQ 6\$  
 2579 011616 104004 HLT 4 :BYTE COUNT ERROR  
 2580 011620 020302 CMP R3,R2 :IS BUS ADDRESS CORRECT  
 2581 011622 001401 BEQ 7\$  
 2582 011624 104003 HLT 3 :BUS ADDRESS ERROR  
 2583 011626 005277 003524 7\$: INC ADHSCR :PREPARE TO CHECK NEXT LINE  
 2584 011632 005201 INC R1 :CONTINUE IF ALL NOT DONE  
 2585 011634 005300 DEC R0 :  
 2586 011636 001350 BNE 4\$  
 2587 011640 104400 SCOPE :CHECK FOR ITERATIONS, LOOP  
 2588  
 2589 ;NPR LOGIC TEST  
 2590 ;SET BYTE COUNT ON ALL LINES TO 1  
 2591 ;SET BAR BIT FOR LINE 11  
 2592 ;VERIFY THAT BYTE COUNT FOR LINE 11 GOES TO 0  
 2593 ;VERIFY THAT BUS ADDRESS FOR LINE 11 IS INCREMENTED  
 2594 ;VERIFY THAT BYTE COUNTS AND BUS ADDRESSES FOR ALL OTHER LINES  
 2595 ;ARE UNCHANGED  
 2596  
 2597 011642 012767 000340 166126 T41: MOV #340,PS :DISABLE ALL INTERRUPTS  
 2598 011650 012767 000010 003546 MOV #10,ICOUNT :SET UP FOR 10 ITERATIONS  
 2599 011656 012767 012010 003534 MOV #8\$,ESCAPE :SET UP TO ESCAPE TO NEXT TEST  
 2600 011664 012777 004000 003464 MOV #BIT11,ADHSCR :MASTER CLEAR INTERFACE  
 2601  
 2602 011672 004767 003366 JSR PC,CLEAR :TO SET ALL TBMT BITS  
 2603  
 2604 011676 004767 003414 JSR PC,LOAD :CLEAR ALL BYTE COUNT AND  
 2605 011702 012777 001000 003460 MOV #1000,ADHBAR :BUS ADDRESS MEMORY LOCATIONS  
 :SET ALL BYTE COUNT LOCATIONS TO -1  
 :SET BAR BIT FOR LINE 11

DZHC MACY11 27.732) 16-MAR-76 09:17 PAGE 53  
DZDHCB.PFC

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2606 011710 005777 003442      3$:    TST    @DHSCR          ;WAIT FOR TRANSMITTER DONE
2607 011714 100375              BPL    3$                ;SET UP TO CHECK ALL 16 LINES
2608 011716 012700 000020      MOV    #20,R0           ;START AT LINE 0
2609 011722 005077 003430      CLR    @DHSCR          ;KEEP TRACK OF LINE NUMBER
2610 011726 005001              CLR    R1                ;(RS)=EXPECTED BYTE COUNT.
2611 011730 C12705 177777      MOV    #-1,R5           ;IF LINE NUMBER NOT = 11
2612                               CLR    R3                ;(R3)=EXPECTED BJS ADDRESS,
2613 011734 005003              CLR    R3                ;IF LINE NUMBER NOT = 11
2614                               MOV    @DHBC,R4          ;(R4)=ACTUAL BYTE ACOUNT
2615 011736 017704 003424      MOV    @DHBA,R2          ;(RS)=ACTUAL BUS ADDRESS
2616 011742 017702 003416      CMP    @DHSCR,#11        ;IF LINE BEING COMPARED IS LINE 11
2617 011746 027727 003404 000011  CMP    5$                ;EXPECTED BYTE COUNT=0
2618 011754 001002              BNE    5$                ;EXPECTED BUS ADDRESS = 1
2619 011756 005005              CLR    R5                ;IS BYTE COUNT CORRECT
2620 011760 005203              INC    R3                ;BYTE COUNT ERROR
2621 011762 020504              CMP    R5,R4           ;IS BUS ADDRESS CORRECT
2622 011764 001401              BEQ    6$                ;BUS ADDRESS ERROR
2623 011766 104004              HLT    4$                ;PREPARE TO CHECK NEXT LINE
2624 011770 020302              CMP    R3,R2           ;CONTINUE IF ALL NOT DONE
2625 011772 001401              BEQ    ?$                ;CHECK FOR ITERATIONS. LOOP
2626 011774 104003              HLT    3$                ;NPR LOGIC TEST
2627 011776 005277 003354      7$:    INC    @DHSCR          ;SET BYTE COUNT ON ALL LINES TO 1
2628 012002 005201              INC    R1                ;SET BAR BIT FOR LINE 12
2629 012004 005300              DEC    R0                ;VERIFY THAT BYTE COUNT FOR LINE 12 GOES TO 0
2630 012006 001350              BNE    4$                ;VERIFY THAT BUS ADDRESS FOR LINE 12 IS INCREMENTED
2631 012010 104400              SCOPE            ;VERIFY THAT BYTE COUNTS AND BUS ADDRESSES FOR ALL OTHER LINES
2632                               ;ARE UNCHANGED
2633                               ;DISABLE ALL INTERRUPTS
2634                               ;SET UP FOR 10 ITERATIONS
2635                               ;SET UP TO ESCAPE TO NEXT TEST
2636                               ;MASTER CLEAR INTERFACE
2637                               ;TO SET ALL TBMT BITS
2638                               ;CLEAR ALL BYTE COUNT AND
2639                               ;BUS ADDRESS MEMORY LOCATIONS
2640                               ;SET ALL BYTE COUNT LOCATIONS TO -1
2641 012012 012767 000340 165756 T42:  MOV    #340,PS          ;SET BAR BIT FOR LINE 12
2642 012020 012767 000010 003376  MOV    #10,ICOUNT        ;WAIT FOR TRANSMITTER DONE
2643 012026 012767 012160 003364  MOV    #8$,ESCAPE         ;SET UP TO CHECK ALL 16 LINES
2644 012034 012777 004000 003314  MOV    #BIT11,@DHSCR       ;START AT LINE 0
2645                               JSR    PC,CLEAR         ;KEEP TRACK OF LINE NUMBER
2646 012042 004767 003216              JSR    PC,LOAD          ;(RS)=EXPECTED BYTE COUNT.
2647                               TST    @DHSCR          ;IF LINE NUMBER NOT = 12
2648 012046 004767 003244              MOV    #2000,@DHBAR        ;(R3)=EXPECTED BJS ADDRESS.
2649 012052 012777 002000 003310  3$:    TST    @DHSCR          ;IF LINE NUMBER NOT = 12
2650 012060 005777 003272              CLR    R1                ;(R4)=ACTUAL BYTE ACOUNT
2651 012064 100375              CLR    R3                ;(RS)=ACTUAL BUS ADDRESS
2652 012066 012700 000020              MOV    #20,R0           ;IF LINE BEING COMPARED IS LINE 12
2653 012072 005077 003260              CLR    @DHSCR          ;EXPECTED BYTE COUNT.
2654 012076 005001              CLR    R1                ;EXPECTED BUS ADDRESS,
2655 012100 012705 177777      4$:    MOV    #-1,R5           ;IF LINE NUMBER NOT = 12
2656                               CLR    R3                ;(R4)=ACTUAL BYTE ACOUNT
2657 012104 005003              CLR    R3                ;(RS)=ACTUAL BUS ADDRESS
2658                               MOV    @DHBC,R4          ;IF LINE NUMBER NOT = 12
2659 012106 017704 003254              MOV    @DHBA,R2          ;(R4)=ACTUAL BYTE ACOUNT
2660 012112 017702 003246              CMP    @DHSCR,#12        ;(RS)=ACTUAL BUS ADDRESS
2661 012116 027727 003234 000012

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003204 5S: SNE CLR INC CMP BEQ HLT CMP BEQ HLT INC INC DEC BNE SCOPE :EXPECTED BYTE COUNT=0 :EXPECTED BUS ADDRESS = ! :IS BYTE COUNT CORRECT

6S: R1 R2 R3, R2 R3, R4 :BYTE COUNT ERROR :IS BUS ADDRESS CORRECT

7S: R1 R2 R3, R4 :BUS ADDRESS ERROR :PREPARE TO CHECK NEXT LINE

8S: R1 R2 R3, R4 :CONTINUE IF ALL NOT DONE

:CHECK FOR ITERATIONS. LOOP

:NPR LOGIC TEST  
:SET BYTE COUNT ON ALL LINES TO 1  
:SET BAR BIT FOR LINE 13  
:VERIFY THAT BYTE COUNT FOR LINE 13 GOES TO 0  
:VERIFY THAT BUS ADDRESS FOR LINE 13 IS INCREMENTED  
:VERIFY THAT BYTE COUNTS AND BUS ADDRESSES FOR ALL OTHER LINES  
:ARE UNCHANGED

012767 012767 000340 165606 T43: MOV #340, PS :DISABLE ALL INTERRUPTS  
012767 000010 003226 MOV \$10, COUNT :SET UP FOR 10 ITERATIONS  
012777 012330 004000 003144 MOV #85, ESCAPE :SET UP TO ESCAPE TO NEXT TEST  
MOV #9111, DDHSCR :MASTER CLEAR INTERFACE  
012212 004767 003046 JSR PC,CLEAR :TO SET ALL TBMT BITS  
012216 004767 003074 JSR PC,LOAD :CLEAR ALL BYTE COUNT AND  
012222 012777 004000 003140 3S: TST DDHSCR :BUS ADDRESS MEMORY LOCATIONS  
MOV #4000, DDHBAR :SET ALL BYTE COUNT LOCATIONS TO -1  
005777 003122 BPL 3S :SET BAR BIT FOR LINE 13  
012236 100375 TST DDHSCR :WAIT FOR TRANSMITTER DONE  
012236 012700 003020 MOV #20, RD :SET UP TO CHECK ALL 16 LINES  
012242 005077 003110 CLR DDHSCR :START AT LINE 0  
012246 005001 CLR R1 :KEEP TRACK OF LINE NUMBER  
012250 012705 177777 4S: MOV #-1, RS :RS1)=EXPECTED BYTE COUNT,  
CLR R3 :IF LINE NUMBER NOT = 13  
012254 005003 CLR R3 :RS3)=EXPECTED BUS ADDRESS.  
012256 017704 003104 MOV DDHBC, R4 :IF LINE NUMBER NOT = 13  
012262 017702 003076 MOV DDHBA, R2 :R4)=ACTUAL BYTE COUNT  
012266 027727 003064 000013 CMP DDHSCR, #13 :R5)=ACTUAL BUS ADDRESS  
012274 001002 BNE SS :IF LINE BEING COMPARED IS LINE 13  
012276 005005 CLR R5 :EXPECTED BYTE COUNT=0  
012300 005203 INC R3 :EXPECTED BUS ADDRESS = !  
012302 020504 CMP R5, R4 :IS BYTE COUNT CORRECT  
012304 001401 BEQ 6S :BYTE COUNT ERROR  
012306 104004 HLT 4 :IS BUS ADDRESS CORRECT  
012310 020302 CMP R3, R2  
012312 001401 BEQ 7S :BUS ADDRESS ERROR  
012314 104003 HLT 3 :PREPARE TO CHECK NEXT LINE  
012316 005277 003034 INC DDHSCR :CONTINUE IF ALL NOT DONE  
012322 005201 INC R1  
012324 005300 DEC RC

22240 MAR 11 1973 16-MAR-75 09:17 PAGE 55

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## DOS

02240 MACYII ZT..32' 16-MAR-76 09:17 PAGE 56  
022HCB.PFC

2774	012510	012767	000010	002706		MOV	\$10, ICOUNT	:SET UP FOR 10 ITERATIONS
2775	012516	012767	012650	002674		MOV	\$85, ESCAPE	:SET UP TO ESCAPE TO NEXT TEST
2776	012524	012777	004000	002624		MOV	\$BIT11, JDHSCR	:MASTER CLEAR INTERFACE
2777								:TO SET ALL TBMT BITS
2778	012532	004767	002526			JSR	PC,CLEAR	:CLEAR ALL BYTE COUNT AND
2779								:BUS ADDRESS MEMORY LOCATIONS
2780	012536	004767	002554			JSR	PC,LOAD	:SET ALL BYTE COUNT LOCATIONS TO -1
2781	012542	012777	020000	002620	33:	MOV	\$20000, JDHBAR	:SET BAR BIT FOR LINE 15
2782	012550	005777	002602			TST	JDHSCR	:WAIT FOR TRANSMITTER DONE
2783	012554	100375				BPL	35	
2784	012556	012700	000020			MOV	\$20, R0	:SET UP TO CHECK ALL 16 LINES
2785	012552	005077	002570			CLR	JDHSCR	:START AT LINE 0
2786	012556	005001				CLR	R1	:KEEP TRACK OF LINE NUMBER
2787	012570	012705	177777		45:	MOV	\$-1, R5	:R5)=EXPECTED BYTE COUNT.
2788						CLR	R3	:IF LINE NUMBER NOT = 15
2789	012574	005003						:R3)=EXPECTED BUS ADDRESS.
2790								:IF LINE NUMBER NOT = 15
2791	012576	017734	002554			MOV	JDHBC,R4	:R4)=ACTUAL BYTE ACOUNT
2792	012602	017702	002556			MOV	JDHBA,R2	:R5)=ACTUAL BUS ADDRESS
2793	012606	027727	002544	000015		CMP	JDHSCR,\$15	:IF LINE BEING COMPARED IS LINE 15
2794	012614	001002				BNE	SS	
2795	012616	005005				CLR	R5	:EXPECTED BYTE COUNT=0
2796	012620	005203				INC	R3	:EXPECTED BUS ADDRESS = 1
2797	012622	020524			55:	CMP	R5,R4	:IS BYTE COUNT CORRECT
2798	012624	001401				BEQ	65	
2799	012626	104004				HLT	4	:BYTE COUNT ERROR
2800	012630	020392			65:	CMP	R3,R2	:IS BUS ADDRESS CORRECT
2801	012632	001401				BEQ	75	
2802	012634	104003				HLT	3	:BUS ADDRESS ERROR
2803	012636	005277	002514		75:	INC	JDHSCR	:PREPARE TO CHECK NEXT LINE
2804	012642	005201				INC	R1	
2805	012644	005300				DEC	R0	:CONTINUE IF ALL NOT DONE
2806	012546	001350				BNE	45	
2807	012650	104400			95:	SC0PE		:CHECK FOR ITERATIONS, LOOP
2808								
2809								:NPR LOGIC TEST
2810								:SET BYTE COUNT ON ALL LINES TO 1
2811								:SET BAR BIT FOR LINE 16
2812								:VERIFY THAT BYTE COUNT FOR LINE 16 GOES TO 0
2813								:VERIFY THAT BUS ADDRESS FOR LINE 16 IS INCREMENTED
2814								:VERIFY THAT BYTE COUNTS AND BUS ADDRESSES FOR ALL OTHER LINES
2815								:ARE UNCHANGED
2816								
2817	012652	012767	000340	165116	T46:	MOV	\$340, PS	:DISABLE ALL INTERRUPTS
2818	012660	012767	000010	002536		MOV	\$10, ICOUNT	:SET UP FOR 10 ITERATIONS
2819	012666	012767	013020	002524		MOV	\$85, ESCAPE	:SET UP TO ESCAPE TO NEXT TEST
2820	012674	012777	004000	002454		MOV	\$BIT11, JDHSCR	:MASTER CLEAR INTERFACE
2821								:TO SET ALL TBMT BITS
2822	012702	004767	002356			JSR	PC,CLEAR	:CLEAR ALL BYTE COUNT AND
2823								:BUS ADDRESS MEMORY LOCATIONS
2824	012706	004767	002404			JSR	PC,LOAD	:SET ALL BYTE COUNT LOCATIONS TO -1
2825	012712	012777	049000	002450	35:	MOV	\$40000, JDHBAR	:SET BAR BIT FOR LINE 15
2826	012720	005777	002432			TST	JDHSCR	:WAIT FOR TRANSMITTER DONE
2827	012724	100375				BPL	35	
2828	012726	012700	000020			MOV	\$20, R0	:SET UP TO CHECK ALL 16 LINES
2829	012732	005077	002420			CLR	JDHSCR	:START AT LINE 0

22240 MACY11 27(732) 16-MAR-76 09:17 PAGE 57  
222408.PFC

2930	012736	005001				CLR	R1		:KEEP TRACK OF LINE NUMBER
2931	012740	012705	177777		4S:	MOV	*-1,RS		: (RS)=EXPECTED BYTE COUNT.
2932									: IF LINE NUMBER NOT = 16
2933	012744	005003				CLR	R3		: (R3)=EXPECTED BUS ADDRESS.
2934									: IF LINE NUMBER NOT = 16
2935	012746	017704	002414			MOV	ADHBC,R4		: (R4)=ACTUAL BYTE ACCOUNT
2936	012752	017702	002406			MOV	ADHBA,R2		: (RS)=ACTUAL BUS ADDRESS
2937	012756	027727	002374	000016		CMP	ADHSCR,*16		: IF LINE BEING COMPARED IS LINE 16
2938	012764	001002				BNE	SS		
2939	012766	005005				CLR	RS		: EXPECTED BYTE COUNT=0
2940	012770	005203				INC	R3		: EXPECTED BUS ADDRESS = 1
2941	012772	020504				CMP	RS,R4		: IS BYTE COUNT CORRECT
2942	012774	001401				BEQ	SS		
2943	012776	104004				HLT	4		: BYTE COUNT ERROR
2944	013000	020302				CMP	R3,R2		: IS BUS ADDRESS CORRECT
2945	013002	001401				BEQ	SS		
2946	013004	104003				HLT	3		: BUS ADDRESS ERROR
2947	013006	005277	002344			INC	ADHSCR		: PREPARE TO CHECK NEXT LINE
2948	013012	005201				INC	R1		
2949	013014	025300				DEC	RS		: CONTINUE IF ALL NOT DONE
2950	013016	001350				BNE	4S		
2951	013020	104400				SCOPE			: CHECK FOR ITERATIONS, LOOP
2952									
2953									
2954									:NPR LOGIC TEST
2955									:SET BYTE COUNT ON ALL LINES TO 1
2956									:SET BAR BIT FOR LINE 17
2957									:VERIFY THAT BYTE COUNT FOR LINE 17 GOES TO 0
2958									:VERIFY THAT BUS ADDRESS FOR LINE 17 IS INCREMENTED
2959									:VERIFY THAT BYTE COUNTS AND BUS ADDRESSES FOR ALL OTHER LINES
2960									:ARE UNCHANGED
2961	013022	012767	000340	164746	T47:	MOV	*340,PS		:DISABLE ALL INTERRUPTS
2962	013030	012767	000010	002366		MOV	*10,ICOUNT		:SET UP FOR 10 ITERATIONS
2963	013036	012767	013170	002354		MOV	*85,ESCAPE		:SET UP TO ESCAPE TO NEXT TEST
2964	013044	012777	004000	002304		MOV	*8111,ADHSCR		:MASTER CLEAR INTERFACE
2965									:TO SET ALL TBMT BITS
2966	013052	004767	002206			JSR	PC,CLEAR		:CLEAR ALL BYTE COUNT AND
2967									:BUS ADDRESS MEMORY LOCATIONS
2968	013056	004767	002234			JSR	PC,LOAD		:SET ALL BYTE COUNT LOCATIONS TO -1
2969	013062	012777	100000	002300		MOV	*100000,ADHBAR		:SET BAR BIT FOR LINE 17
2970	013070	005777	002262		3S:	TST	ADHSCR		:WAIT FOR TRANSMITTER DONE
2971	013074	100375				BPL	SS		
2972	013076	012700	000020			MOV	*20,RS		:SET UP TO CHECK ALL 16 LINES
2973	013102	005077	002250			CLR	ADHSCR		:START AT LINE 0
2974	013106	005001				CLR	R1		:KEEP TRACK OF LINE NUMBER
2975	013110	012705	177777		4S:	MOV	*-1,RS		: (RS)=EXPECTED BYTE COUNT.
2976									: IF LINE NUMBER NOT = 17
2977	013114	005003				CLR	R3		: (R3)=EXPECTED BUS ADDRESS.
2978									: IF LINE NUMBER NOT = 17
2979	013116	017704	002244			MOV	ADHBC,R4		: (R4)=ACTUAL BYTE ACCOUNT
2980	013122	017702	002236			MOV	ADHBA,R2		: (RS)=ACTUAL BUS ADDRESS
2981	013128	027727	002224	000017		CMP	ADHSCR,*17		: IF LINE BEING COMPARED IS LINE 17
2982	013134	001002				BNE	SS		
2983	013136	005005				CLR	RS		: EXPECTED BYTE COUNT=0
2984	013140	005203				INC	R3		: EXPECTED BUS ADDRESS = 1
2985	013142	020504				CMP	RS,R4		: IS BYTE COUNT CORRECT

F05

DDMHC MACY11 27(732) 16-MAR-75 09:17 PAGE 59  
DDMHCB.PFC

2996 013144 001401  
2997 013146 104004  
2998 013150 C20302  
2999 013152 001401  
3000 013154 104003  
3001 013156 005277  
3002 013158 005201  
3003 013164 005300  
3004 013166 001350  
3005 013170 104403

6S: BEQ 6S  
      HLT 4  
      CMP R3,R2  
      BEQ S  
7S: INC 7S  
      HLT  
      INC 7OHSCR  
      INC R1  
      DEC R2  
      BEQ 4S  
9S: SCOPE

:BYTE COUNT ERROR  
:IS BUS ADDRESS CORRECT  
:BUS ADDRESS ERROR  
:PREPARE TO CHECK NEXT LINE  
:CONTINUE IF ALL NOT DONE  
:CHECK FOR ITERATIONS, LOOP

2996 :SILO LOGIC TEST (MAINTENANCE MODE)  
 2997 :FORCE 1 CHARACTER INTO SILO USING SILO  
 2998 :MAINTENANCE BIT  
 2999 :VERIFY THAT CHARACTER AVAILABLE INTERRUPT OCCURS  
 3000 :VERIFY THAT CHARACTER AVAILABLE BIT IS  
 3001 :SET IN SYSTEM CONTROL REGISTER  
 3002 :VERIFY THAT SILO FILL REGISTER INCREMENTS TO 1  
 3003 :VERIFY THAT NEXT RECEIVED CHARACTER REGISTER  
 3004 :VALID DATA BIT IS SET  
 3005 :VERIFY THAT CORRECT DATA PATTERN WAS RECEIVED  
 3006  
 3007  
 2909 013172 012767 000340 164576 T50: MOV #340,PS :DISABLE ALL INTERRUPTS  
 2910 013200 012767 000010 002216 MOV #10,ICOUNT :SET UP FOR 10 ITERATIONS  
 2911 013205 012767 013350 002204 MOV #5\$,ESCAPE :SET UP TO ESCAPE TO NEXT TEST  
 2912 013214 012777 004009 002134 MOV #BIT11,DDHSCR :MASTER CLEAR INTERFACE  
 2913 013222 012777 013270 002150 MOV #2\$,DDHRVEC :SET UP RECEIVER INTERRUPT  
 2914 013230 012777 000340 002144 MOV #340,DDHPLVL :VECTOR AND STATUS  
 2915 013236 052777 100000 002130 BIS #BIT15,DDHSSR :SET SILO MAINTENANCE  
 2916 013244 012777 000100 002104 MOV #BIT06,DDHSCR :SET RECEIVER INTERRUPT ENABLE  
 2917 013252 005067 164520 CLR PS :ALLOW INTERRUPTS  
 2918 013256 012700 001000 MOV #1000,RO :SET UP DELAY FOR SILO LOAD  
 2919 013262 005300 1S: DEC RO :SET UP DELAY FOR SILO LOAD  
 2920 013264 001376 BNE 1S :DELAY FOR SILO LOAD  
 2921 013266 104001 HLT ! :NO CHARACTER AVAILABLE INTERRUPT OCCURED  
 2922 013270 042777 100000 002076 2S: BIC #BIT15,DDHSSR :CLEAR SILO MAINTENANCE BIT  
 2923 013276 105777 002054 TSTB DDHSCR :IS CHARACTER AVAILABLE BIT SET  
 2924 013302 100401 BMI 3S :CHARACTER AVAILABLE NOT, ERROR  
 2925 013304 104005 HLT E :READ SILO STATUS REGISTER  
 2926 013306 017703 002052 MOV #DDHSSR,R3 :(R4)=ACTUAL DATA IN NEXT  
 2927 013312 017704 002042 MOV #DDHNRC,R4 :RECEIVED CHARACTER REGISTER  
 2928 013316 012705 125252 3S: MOV #125252,R5 :(R5)=EXPECTED DATA IN  
 2929 013322 020504 CMP R5,R4 :NEXT RECEIVED CHARACTER REGISTER  
 2930 013324 001401 BEQ 4S :IS DATA IN SILO CORRECT  
 2931 013326 104006 HLT 6 :SILO DATA ERROR  
 2932 013330 010304 MOV R3,R4 :GET SILO STATUS REGISTER  
 2933 013332 042704 000300 BIC #300,R4 :CLEAR UNWANTED BITS  
 2934 013336 012705 000400 MOV #400,R5 :;(R5)=EXPECTED DATA  
 2935 013342 020504 CMP R5,R4 :IN SILO STATUS REGISTER  
 2936 013344 001401 BEQ 5S :CHECK RESULTS  
 2937 013346 104007 HLT 7 :SILO STATUS ERROR  
 2938 013350 012706 017102 5S: MOV #STACK,SP :RESTORE STACK  
 2939 013354 104400 SCOPE :CHECK FOR ITERATIONS, LOOP  
 2940  
 2941  
 2942  
 2943 :SILO LOGIC TEST (MAINTENANCE MODE)  
 2944 :LOAD 63(DECIMAL) CHARACTERS INTO SILO  
 2945 :VERIFY THAT SILO STATUS REGISTER COUNTS UP CORRECTLY  
 2946  
 2947 013356 012767 000340 164412 T51: MOV #340,PS :DISABLE ALL INTERRUPTS  
 2948 013364 012767 000001 002032 MOV #1,ICOUNT :SET UP FOR 1 ITERATIONS  
 2949 013372 012767 013510 002020 MOV #5\$,ESCAPE :SET UP TO ESCAPE TO NEXT TEST  
 2950 013400 012767 013412 002014 MOV #13,FREEZ1 :SET UP TO LOOP WITH DATA  
 2951 01340E C12701 000001 MOV #1,R1 :SET UP TO LOAD SILO WITH 1 CHARACTER

DDHC MACY11 27(732) 16-MAR-76 09:17 PAGE 60  
DDHCB.PFC

2952	013412	012777	004000	001736	1\$:	MOV	#BIT11, DDHSCR	:MASTER CLEAR INTERFACE
2953	013420	010100				MOV	R1, R0	:SAVE COUNT
2954	013422	005005				CLR	R5	:WILL BE COUNT OF CHARACTERS LOADED
2955	013424	05277	100000	001742	2\$:	BIS	#BIT15, DDHSSR	:LOAD A CHARACTER
2956	013432	012702	001000			MOV	#1000, R2	:STALL FOR SILO
2957	013436	005302			3\$:	DEC	R2	
2958	013440	001376				BNE	3\$	
2959	013442	042777	100000	001724		BIC	#BIT15, DDHSSR	:CLEAR LOAD BIT
2960	013450	005205				INC	R5	:UPDATE COUNT OF CHARACTERS LOADED
2961	013452	005300				DEC	R0	:IF ALL CHARACTERS NOT LOADED
2962	013454	001363				BNE	2\$	:LOAD ANOTHER
2963	013456	017704	001712			MOV	DDHSSR, R4	:READ SILO STATUS REGISTER
2964	013462	042704	000300			BIC	#300, R4	:CLEAR UNWANTED BITS
2965	013466	000304				SWAB	R4	:GET DATA INTO LOW BYTE
2966	013470	020504				CMP	R5, R4	:COMPARE
2967	013472	001401				BEQ	4\$	
2968	013474	104007				HLT	7	
2969	013476	104410			4\$:	SCOPE1		:SILO STATUS ERROR
2970								:CHECK FOR LOOP WITH CURRENT
2971	013500	005201				INC	R1	:LOAD COUNT (RS)
2972								:ADD 1 TO NUMBER OF CHARACTERS
2973	013502	022701	000100			CMP	#100, R1	:TO BE LOADED INTO SILO
2974	013506	001341				BNE	1\$	:CONTINUE UNTIL SILO IS FULL
2975	013510	104400			5\$:	SCOPE		
2976								
2977								:SILO LOGIC TEST (MAINTENANCE MODE)
2978								:LOAD S4 (DECIMAL CHARACTERS INTO SILO)
2979								:READ CHARACTERS OUT OF SILO
2980								:VERIFY THAT SILO STATUS REGISTER COUNTS DOWN CORRECTLY
2981								
2982	013512	012767	000340	164256	T52:	MOV	#340, PS	:DISABLE ALL INTERRUPTS
2983	013520	012767	000001	001576		MOV	#1, ICOUNT	:SET UP FOR 1 ITERATIONS
2984	013526	012767	013670	001664		MOV	#7\$, ESCAPE	:SET UP TO ESCAPE TO NEXT TEST
2985	013534	012767	013546	001660		MOV	#1\$, FREEZ1	:SET UP TO LOOP WITH DATA
2986	013542	012701	000001			MOV	#1, R1	:SET UP TO READ 1 CHARACTER
2987	013546	012777	004000	001602	1\$:	MOV	#BIT11, DDHSCR	:MASTER CLEAR INTERFACE
2988	013554	012705	000100			MOV	#100, RS	:SILO STATUS COUNT SHOULD BE
2989	013560	160105				SUB	R1, RS	:100(OCTAL)-NUMBER
2990								:OF CHARACTERS READ
2991	013562	012700	000100			MOV	#100, R0	:SET UP TO LOAD SILO
2992	013566	012702	001000		2\$:	MCY	#1000, R2	:SET UP DELAY
2993	013572	052777	100000	001574		BIS	#BIT15, DDHSSR	:LOAD 1 CHARACTER
2994	013600	005302			3\$:	DEC	R2	:DELAY
2995	013602	001376				BNE	3\$	
2996	013604	042777	100000	001562		BIC	#BIT15, DDHSSR	:CLEAR SILO LOAD BIT
2997	013612	005300				DEC	R0	:CONTINUE IF SILO NOT FULL
2998	013614	001364				BNE	2\$	
2999	013616	010100				MOV	R1, R0	
3000	013620	012702	001000		4\$:	MOV	#1000, R2	:SET UP TO READ SILO
3001	013624	005777	0C1530			TST	DDHNRC	:SET UP DELAY FOR SILO
3002	013630	005302			5\$:	DEC	R2	:READ SILO
3003	013632	001376				BNE	5\$	:DELAY FOR SILO
3004	013634	005300				DEC	R0	
3005	013636	001370				BNE	4\$	:UPDATE NUMBER OF CHARACTERS TO BE READ
3006	013640	117704	001532			MOVB	DDHSLR, R4	:CONTINUE READING
3007	013644	042704	000300			BIC	#300, R4	:READ SILO STATUS REGISER
								:CLEAR UNWANTED BITS

DZDHC MACY11 27732 16-MAR-75 09:17 PAGE 61  
DZDHCB.PFC

3008  
3009  
3010  
3011  
3012 013650 020504  
3013 013652 001401  
3014 013654 104007  
3015 013656 104410  
3016 013660 005201  
3017 013662 020127  
3018 013666 001327  
3019 013670 104400

CMP R5,R4 ;(R5)=EXPECTED SILO STATUS  
BEQ 6S ;(IN UPPER BYTE)  
HLT ? ;(R4)=ACTUAL SILO STATUS  
;IN UPPER BYTE  
;COMPARE EXPECTED AND RECEIVED DATA  
6S: SCOPE1 ;SILO STATUS ERROR.  
INC R1 ;CHECK FOR LOOP WITH SAME READ COUNT  
CMP R1,\*101 ;UPDATE COUNT OF CHARACTERS TO BE READ  
BNE 1S ;CONTINUE IF NOT DONE  
7S: SCOPE

## J05

DZDMC MACY11 27.732 16-MAR-75 09:17 PAGE 62  
DZDMC9.PFC

3020								
3021								:SILO LOGIC TEST (MAINTENANCE MODE)
3022								:SET SILO ALARM LEVEL TO ALL VALUES 0-77
3023								:VERIFY THAT CHARACTER AVAILABLE FLAG
3024								:DOES NOT SET UNTIL SILO FILL LEVEL IS GREATER THAN
3025								:SILO ALARM LEVEL
3026								
3027	013672	012767	000340	164076	T53:	MOV	\$340,PS	:DISABLE ALL INTERRUPTS
3028	013700	012767	000040	001516		MOV	\$40,1COUNT	:SET UP FOR 40 ITERATIONS
3029	013706	012767	014046	001504		MOV	\$5\$,ESCAPE	:SET UP TO ESCAPE TO NEXT TEST
3030	013714	012767	013724	001500		MOV	\$1\$,FREEZ1	:SET UP TO LOOP WITH DATA
3031	013722	J05005				CLR	R5	:START AT ALARM LEVEL 0
3032	013724	012777	004000	001424	I\$:	MOV	#BIT11,JDHSCR	:MASTERCLEAR INTERFACE
3033	013732	010577	001436			MOV	R5,JDHSSR	:SET ALARM LEVEL
3034	013736	010501				MOV	R5,R1	:SET FILL COUNT
3035	013740	005201				INC	R1	:ONE MORE THAN ALARM LEVEL
3036	013742	052777	100000	001424	2\$:	BIS	#BIT15,JDHSSR	:LOAD A CHARACTER
3037	013750	012700	001000			MOV	*1000,R0	:WAIT FOR SILO TO SETTLE
3038	013754	005300				DEC	R0	
3039	013756	001376				BNE	.-2	
3040	013760	042777	100000	001406		BIC	#BIT15,JDHSSR	:CLEAR MAINTENANCE BIT
3041	013766	005301				DEC	R1	:UPDATE FILL COUNT
3042	013770	105777	001362			TSTB	JDHSCR	:IS CHARACTER AVAILABLE FLAG SET
3043	013774	100406				BMI	35	:YES
3044	013776	005701				TST	R1	:CHARACTER AVAILABLE FLAG NOT SET
3045	014000	001360				BNE	2\$	:SHOULD IT BE
3046	014002	117703	001370			MOV	JDHSLR,R3	:READ SILO FILL LEVEL
3047	014006	104010				HLT	10	:SILO ALARM ERROR
3048								:NO CHARACTER AVAILABLE WHEN EXPECTED
3049	014010	000406				BR	4\$	
3050	014012	020127	000001		3\$:	CMP	R1,#1	
3051	014016	003403				BLE	4\$	
3052	014020	117703	001352			MOV	JDHSLR,R3	:READ SILO FILL LEVEL
3053	014024	104010				HLT	10	:SILO ALARM ERROR
3054	014026	104410			4\$:	SCOPE1		:CHECK FOR FREEZE AT CURRENT ALARM LEVEL
3055	014030	005705				TST	R5	
3056	014032	001001				BNE	10\$	
3057	014034	000261				SEC		
3058	014036	006105			10\$:	ROL	R5	:GO TO NEXT ALARM LEVEL
3059	014040	J22705	000100			CMP	*100,R5	:CONTINUE IF NOT DONE
3060	014044	001327				BNE	1\$	
3061	014046	104400			5\$:	SCOPE		:CHECK FOR ITERATIONS, LOOP

DZDHC MACY11 27.732) 15-MAR-76 09:17 PAGE 63  
DZDHCB.PFC

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3062
3063
3064 :END OF PASS
3065 :TYPE NAME OF TEST
3066 :UPDATE PASS COUNT
3067 :CHECK FOR EXIT TO ACT-11
3068 :RESTART TEST
3069

3070 014050 104401           EOP: TYPE               ;TYPE NAME OF TEST
3071 014052 016055          MEPASS
3072 014054 005067          CLR    LAST
3073 014060 005067          CLR    ERRFLG
3074 014064 005267          INC    PASCNT
3075 014070 016767          MOV    PASCNT,LIGHTS
3076 014076 013701          MOV    @#42,R1
3077 014102 001409          BEQ    RESTRT
3078 014104 000005          RESET
3079 014106 004711          LOGICAL: JSR    PC,(R1)
3080 014110 000240          NOP
3081 014112 000240          NOP
3082 014114 000240          NOP
3083 014116 000167          165120          RESTRT: JMP   BEGIN
3084
3085
3086
3087
3088 014122 032767          SCOPER: BIT    #SW10,SWR
3089 014130 001030          BNE    4S
3090 014132 032767          1$:    BIT    #SW14,SWR
3091 014140 001021          BNE    3S
3092 014142 032767          004000 163420      BIT    #SW11,SWR
3093 014150 001006          BNE    2S
3094 014152 005267          001250          INC    LPCNT
3095 014156 026767          001244 001240      CMP    LPCNT,ICOUNT
3096 014164 001007          BNE    3S
3097 014166 005067          001234          2$:    CLR    LPCNT
3098 014172 005067          001212          CLR    ERRFLG
3099 014176 011667          001214          MOV    (SP),RETURN
3100 014202 000002          001206          3$:    RTI    RETURN,(SP)
3101 014204 016716          001206          4$:    MOV    RETURN,(SP)
3102 014210 000002          RTI
3103 014212 005767          001172          TST    ERRFLG
3104 014216 001745          BEQ    1S
3105 014220 000762          BR    2S
3106
3107
3108
3109 014222 032767          SCOPIR: BIT    #SW09,SWR
3110 014230 001402          BEQ    1S
3111 014232 016716          001164          1$:    MOV    FREEZ1,(SP)
3112 014236 000002          RTI
3113
3114
3115
3116 014240 032767          020000 163322      ERRORS: BIT    #SW13,SWR
3117 014246 001051          BNE    HALTS

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DZDHC MACY11 27(732) 16-MAR-76 09:17 PAGE 64  
DZDHCB.PFC

3118	014250	021567	001200		CMP	(SP),LAST	
3119	014254	001404			BEQ	1\$	
3120	014256	011667	001172		MOV	(SP),LAST	
3121	014262	005067	001122		CLR	ERRFLG	
3122	014266	104406		1\$: SAVOSP			
3123	014270	011605			MOV	(SP),R5	
3124	014272	162705	000002		SUB	*2 R5	
3125	014276	011504			MOV	(R5),R4	
3126	014300	006304			ASL	R4	
3127	014302	006304			ASL	R4	
3128	014304	042704	177001		BIC	#177001,R4	
3129	014310	062704	016164		ADD	#ERRTAB,R4	
3130	014314	C12467	000034		MOV	(R4)+ERRMSG	
3131	014320	011467	000042		MOV	(R4),DATABP	
3132	014324	005767	001060		TST	ERRFLG	
3133	014330	001403			BEQ	TYPMSG	
3134	014332	005767	000030		TST	DATABP	
3135	014335	001007			BNE	TYPDAT	
3136	014340	104402		TYPMSG:	OCTASC		
3137	014342	014434			ERTABO		
3138	014344	012767	000001 001036		MOV	*1,ERRFLG	
3139	014352	104401			TYPE		
3140	014354	000000		ERRMSG:	0		
3141	014356	005767	000004		TYPDAT:	TST	
3142	014362	001402			BEQ	DATABP	
3143	014364	104402				RESREG	
3144	014366	000000		DATAFP:	0		
3145	014370	104407			RESREG:	RES05	
3146	014372	005767	163172		HALTS:	TST	
3147	014376	100005			BPL	SWR	
3148	014400	010046			PUSHRO	EXITER	
3149	014402	016600	000002		MOV	2(SP),R0	
3150	014406	000000			HALT		
3151	014410	012600			POPRO		
3152	014412	005267	000776	EXITER:	INC	ERPCNT	
3153	014416	032767	002000 163144		BIT	*SW10,SWR	
3154	014424	001402			BEQ	1\$	
3155	014426	016716	000766		MOV	ESCAPE,(SP)	
3156	014432	000002		1\$:	RTI		
3157	014434	000001			ERTABO:	1	
3158	014436	006	002		BYTE	6.2	
3159	014440	015446			SAVPC		
3160						:TRAP DISPATCH SERVICE	
3161						:ARGUMENT OF TRAP IS EXTRACTED	
3162						:AND USED AS OFFSET TO OBTAIN POINTER	
3163						:TO SELECTED SUBROUTINE	
3164							
3165	014442	011646		TRPSRV:	MOV	(SP),-(SP)	:GET PC OF RETURN
3166	014444	162716	000002		SUB	*2 (SP)	:=PC OF TRAP
3167	014450	017616	000000		MOV	2(SP),(SP)	:GET TRP
3168	014454	006316		TRPOK:	ASL	(SP)	:MULTIPLY TRAP ARG BY 2
3169	014456	042716	177001		BIC	#177001,(SP)	:CLEAR UNWANTED BITS
3170	014462	062716	016104		ADD	*TRPTAB,(SP)	:POINTER TO SUBROUTINE ADDRESS
3171	014466	017616	000000		MOV	2(SP),(SP)	:SUBROUTINE ADDRESS
3172	014472	000136			JMP	2(SP)+	:GO TO SUBROUTINE
3173							

DZDHC MACY11 27(732) 16-MAR-76 09:17 PAGE 65  
DZDHC.B.PFC

3174 ;TELETYPE OUTPUT ROUTINE  
 3175  
 3176 014474 017605 000000  
 3177 014500 062716 000002  
 3178 014504 105777 000642  
 3179 014510 100375  
 3180 014512 105715  
 3181 014514 001001  
 3182 014516 000002  
 3183 014520 112577 000630  
 3184 014524 000767  
 3185 ;ASCII STRING INPUT ROUTINE  
 3186  
 3187  
 3188 014526 017667 000000 000006  
 3189 014534 062716 000002  
 3190 014540 104401  
 3191 014542 000000  
 3192 014544 012704 016126  
 3193 014550 012703 000007  
 3194 014554 105777 000566  
 3195 014560 100375  
 3196 014562 117714 000562  
 3197 014566 142714 000200  
 3198 014572 122427 000015  
 3199 014576 001413  
 3200 014600 117777 000544 000546  
 3201 014606 105777 000540  
 3202 014612 100375  
 3203 014614 005303  
 3204 014616 001356  
 3205 014620 104401  
 3206 014622 015761  
 3207 014624 000745  
 3208 014626 000002  
 3209 ;CONVERT ASCII STRING TO OCTAL  
 3210  
 3211  
 3212 014630 011605  
 3213 014632 012567 000146  
 3214 014636 012567 000144  
 3215 014642 012567 000142  
 3216 014646 112567 000140  
 3217 014652 112567 000135  
 3218 014656 010516  
 3219 014660 005005  
 3220 014662 012704 016126  
 3221 014666 122714 000015  
 3222 014672 001420  
 3223 014674 121427 000060  
 3224 014700 002415  
 3225 014702 121427 000067  
 3226 014706 003012  
 3227 014710 142714 000060  
 3228 014714 152405  
 3229 014716 122714 000015  
 3176 TYPER: MOV J(SP), R5  
 ADD #2, (SP)  
 3177 TSTB @TPCSR  
 BPL 1\$  
 3178 TSTB (R5)  
 BNE 2\$  
 3179 RTI  
 3180 MOVB (R5)+, @TPD8R  
 BR 1\$  
 3181 ;ASCII STRING INPUT ROUTINE  
 3182 INSTRG: MOV J(SP), MSG  
 ADD #2, (SP)  
 3183 INSTR1: TYPE  
 MSG: 0  
 3184 TSTB @TKCSR  
 BPL 1\$  
 3185 MOVB @TKD8R, (R4)  
 3186 MOV #7, R3  
 3187 BICB #200, (R4)  
 3188 CMPB (R4)+, #15  
 3189 BEQ INSTR2  
 3190 MOVB @TKD8R, @TPD8R  
 3191 TSTB @TPCSR  
 3192 FPL 2\$  
 3193 DEC R3  
 3194 BNE 1\$  
 3195 INSTR2: TYPE  
 3196 MQM  
 3197 BR INSTR1  
 3198 INSTR2: RTI  
 3199 ;CONVERT ASCII STRING TO OCTAL  
 3200 PARAMS: MOV (SP), RS  
 3201 MOV (RS)+, LOLIM  
 3202 MOV (RS)+, HILIM  
 3203 MOV (RS)+, DEVADR  
 3204 MOVB (RS)+, LOBITS  
 3205 MOVB (RS)+, ADRCNT  
 3206 MOV R5, (SP)  
 3207 PARAM1: CLR R5  
 3208 MOV #INBUF, R4  
 3209 CMPB #15, (R4)  
 3210 BEQ PARERR  
 3211 CMPB (R4), #60  
 3212 BLT PARERR  
 3213 CMPB (R4), #67  
 3214 BGT PARERR  
 3215 BICB #60, (R4)  
 3216 BISB (R4)+, R5  
 3217 CMPB #15, (R4)

DZDHC MACY11 27(732) 16-MAR-76 09:17 PAGE 66  
DZDHC8.PFC

3230	014722	001406		BEQ	LIMIT3
3231	014724	006305		ASL	R5
3232	014726	006305		ASL	R5
3233	014730	006305		ASL	R5
3234	014732	000760		BR	IS
3235	014734	104404		PARERR:	INSTER
3236	014736	000750		BR	PARAM1
3237				; TEST TO SEE IF NUMBER IS WITHIN LIMITS	
3238					
3239	014740	020567	000042	LIMITS:	CMP R5,HILIM
3240	014744	101373			BHI PARERR
3241	014746	020567	000032		CMP R5,LOLIM
3242	014752	103770			BLO PARERR
3243	014754	136705	000032		BITB LOBITS,R5
3244	014760	001365			BNE PARERR
3245				; STORE NUMBER AT SPECIFIED ADDRESS	
3246					
3247	014762	016704	000022		MOV DEVADR,R4
3248	014766	010524		1\$:	MOV R5,(R4)+
3249	014770	062705	000002		ADD #2,R5
3250	014774	105367	000013		DEC8 ADRCNT
3251	015000	001372			BNE 1\$
3252	015002	000002			RTI
3253	015004	000000		LOLIM:	0
3254	015006	000000		HILIM:	0
3255	015010	000000		DEVADR:	0
3256	015012	000000		LOBITS:	0
3257					ADRCNT=LOBITS+1
3258				; CONVERT OCTAL NUMBER TO ASCII AND OUTPUT TO TELEPRINTER	
3259					
3260				OCTASN:	TYPE
3261	015014	104401			MCRLF
3262	015016	015765			MOV a(SP),R1
3263	015020	017601	000000		ADD #2,(SP)
3264	015024	062716	000002	1\$:	MOV (R1)+,WRDCNT
3265	015030	012167	000130		MOVB (R1)+,CHRCNT
3266	015034	112167	000126		MOVB (R1)+,SPACNT
3267	015040	112167	000123	2\$:	MOV a(R1)+,BINWRD
3268	015044	013167	000120		MOVB BINWRD,R4
3269	015050	016704	000114		MOVB CHRCNT,R5
3270	015054	116705	000106	3\$:	MOV #TEMP,R0
3271	015060	012700	01614C		MOV R4,R3
3272	015064	010403			BIC #177770,R3
3273	015066	042703	177770		ADD #260,R3
3274	015072	062703	000260		MOVB R3,(R0)+
3275	015076	110320			ASR R4
3276	015100	006204			ASR R4
3277	015102	006204			DEC R5
3278	015104	006204			BNE 2\$
3279	015106	005305			MOV #MDATA,R3
3280	015110	001365			MOVB -(R0),(R3)+
3281	015112	012703	016152	4\$:	DEC8 CHRCNT
3282	015116	114023			
3283	015120	105367	000042		

153111 37.732 15-MAR-76 09:17 PAGE 67  
000008.PRC

015170	015170	000000	000035		BNE	15	SPACNT
			000240	ES:	MOV	15	SS
			000023		DEC	SS	SPACNT
				ES:	BYE	SS	
					TYPE	(R3)	
					MCATA		
					DEC	WRCNT	
					BNE	15	
			000034		RTI		
					WRCNT:	0	
					CHRCNT:	0	
					SPACNT=CHRCNT+1		
					SINWRD:	0	
							:SAVE PC OF TEST THAT FAILED ANC RD-RS
015172	016667	000004	000246	SVCSP:	MOV	4(SP),SAVPC	
							:SAVE RD-RS
015200	010567	000236		SVCS:	MOV	RS,SAVRS	
015201	010467	000230			MOV	R4,SAVR4	
015202	010367	000222			MOV	R3,SAVR3	
015203	010267	000214			MOV	R2,SAVR2	
015204	010167	000206			MOV	R1,SAVR1	
015205	010067	000200			MOV	RO,SAVRO	
015230	000002				RTI		:RESTORE RD-RS
015232	016700	000172		RSOS:	MOV	SAVRO,RO	
015236	016701	000173			MOV	SAVR1,R1	
015242	016702	000196			MOV	SAVR2,R2	
015246	016703	000164			MOV	SAVR3,R3	
015252	016704	000162			MOV	SAVR4,R4	
015256	016705	000160			MOV	SAVRS,RS	
015262	000002				RTI		
							:CLEAR BYTE COUNT AND BUS ADDRESS MEMORIES
015264	012700	000020		CLEAR:	MOV	\$20,RO	
015265	005077	000062			CLR	ADHSCR	:SET UPT TO CLEAR 16 (DECIMAL) LOCATIONS
015274	005077	000066			CLR	ADHBC	:START AT LOCATION 0
015279	005077	000060			CLR	ADHBA	:CLEAR BYTE COUNT
015284	005277	000046			INC	ADHSCR	:CLEAR BUS ADDRESS
015290	005300				DEC	RO	:ADVANCE LINE NUMBER
015294	005277				BNE	15	:CONTINUE IF NOT DONE
015310	005300				RTS	PC	
015312	001370						:RETURN
015314	000207						
							:LOAD ALL BYTE COUNT MEMORY LOCATIONS WITH -1
015316	012700	000020		LOAD:	MOV	\$20,RO	
015322	005077	000030			CLR	ADHSCR	:SET UP TO LOAD 16 (DECIMAL) LOCATIONS
015326	C12777	177777	000032		MOV	\$-1,ADHBC	:START WITH LINE 0
				2\$:			:SET BYTE COUNT TO -1

3342	015334	005277	000016	INC	20HSCR	:ADVANCE LINE NUMBER
3343	015340	005300		DEC	R0	:CONTINUE IF NOT DONE
3344	015342	001371		BNE	28	
3345	015344	000200		RTS	PC	:RETURN TO CALLING ROUTINE
3346				:INDIRECT POINTERS		
3347				TKCSR:	177560	
3348				TKD8R:	177562	
3349				TPCSR:	177564	
3350				TPD8R:	177566	
3351				DHSR:	0	
3352				CHNRC:	0	
3353				DHLPR:	0	
3354				CHBRA:	0	
3355				CHBC:	0	
3356				CHBAR:	0	
3357				DHBCR:	0	
3358				CHSSR:	0	
3359				DHSLR:	0	
3360				CHRVEC:	0	
3361				CHRRLV:	0	
3362				DHTVEC:	0	
3363				DHTLVL:	0	
3364				DT'LVL:	0	
3365				:PROGRAM VARIABLES		
3366				ERRFLG:	0	:ERROR FLAG
3367	015410	000000		PASCNT:	0	:PASS COUNT
3368	015412	000000		ERRCNT:	0	:ERROR COUNT
3369	015414	000000		RETURN:	0	:SCOPE RETURN ADDRESS FOR TEST LOOPING
3370	015416	000000		ESCAPE:	0	:ADDRESS FOR ERROR ESCAPE
3371	015420	000000		FREEZ1:	0	:DATA LOOPING RETURN ADDRESS
3372	015422	000000		ICOUNT:	0	:ITERATION COUNT FOR TEST IN PROGRESS
3373	015424	000000		LPCNT:	0	:NUMBER OF ITERATIONS THIS TEST
3374	015426	000000		SAVRC:	0	:R0 SAVE AREA
3375	015430	000000		SAVR1:	0	:R1 SAVE AREA
3376	015432	000000		SAVR2:	0	:R2 SAVE AREA
3377	015434	000000		SAVR3:	0	:R3 SAVE AREA
3378	015436	000000		SAVR4:	0	:R4 SAVE AREA
3379	015440	000000		SAVR5:	0	:R5 SAVE AREA
3380	015442	000000		SAVSP:	0	:STACK POINTER SAVE AREA
3381	015444	000000		SAVPC:	0	:CALLING ROUTINE SAVE AREA
3382	015446	000000		INIFLG:	0	:PROGRAM INITIALIZATION FLAG
3383	015448	000000		STFLG:	0	:PROGRAM START FLAG
3384	015450	000000		LAST:	0	:LAST ERROR PC
3385	015452	000000		HCore:	0	
3386	015454	000000		:ENTER HERE ON POWER FAILURE		
3387	015456	000000		PFAIL:	MOV R0,-(SP)	:SAVE R0-R5 ON PROCESSOR STACK
3388	015460	010046		MOV R1,-(SP)		
3389	015462	010146		MOV R2,-(SP)		
3390	015464	010246		MOV R3,-(SP)		
3391	015466	010346		MOV R4,-(SP)		
3392	015470	010446		MOV R5,-(SP)		
3393	015472	010546	1E2324	MOV 24,-(SP)		
3394	015474	010646	177740	MOV SP,SAVSP		:SAVE STACK POINTER
3395	015500	010687				

2224C 222111 27:732) 16-MAR-76 09:17 PAGE 69  
2224CB.PFC

3398	015504	012767	015516	1623.2	MUV HALT BR	BRESTART,24 . .	:SET UP FOR POWER UP TRAP :HALT ON POWER DOWN NORMAL
:PROCESSOR WILL TRAP HERE WHEN POWER IS RESTORED							
3400	015514	000777					
3401	015516	016706	177722		RESTAR:	MOV MOV MOV MOV MOV MOV MOV MOV MOV MOV MOV MOV MOV MOV MOV MOV CLR INC BNE	SAXSP,SP (SP)+,R5 (SP)+,R4 (SP)+,R3 (SP)+,R2 (SP)+,R1 (SP)+,R0 #PFAIL,24 #340,PS #STACK,SP TEMP TEMP .4
3402	015522	012605					:RESTORE STACK POINTER :RESTORE R0-R5
3403	015524	012604					
3404	015526	012603					
3405	015530	012602					
3406	015532	012601					
3407	015534	012600					
3408	015536	012767	015460	152250			:SET UP FOR POWER FAILURE
3409	015544	012767	000340	162224			
3410	015552	012706	017102				
3411	015556	005067	000356				
3412	015562	005267	000352				
3413	015566	001375			OCTASC		
3414	015570	104402			PFTAB		
3415	015572	015614			TYPE		
3416	015574	104401			MPFAIL		
3417	015576	015770			CLR	ERRFLG	
3418	015600	005067	177604		PFTAB:	CLR	LAST
3419	015604	005067	177644			JMP	RETURN
3420	015610	000177	177602				
3421	015614	000001	000002				
3422	015616	000006					
3423	015622	000207					
3424	015624	005015	042012	030510	MTITLE:	.ASCIZ	<15><12><12>/CH11 TRANSMITTER AND RECEIVER LOGIC TEST <>15<>12>
3425	015632	020061	051124	047101			
3426	015640	045523	052111	042524			
3427	015646	020122	047101	020104			
3428	015654	042522	042503	053111			
3429	015662	051105	046040	043517			
3430	015670	041511	052040	051505			
3431	015676	020124	005015	000			
3432	015703	015	053012	041505	MVECT0:	.ASCIZ	<15><12>/VECTOR ADDRESS-
3433	015710	047524	020122	042101			
3434	015716	051104	051505	026523			
3435	015724	000					
3436	015725	015	041412	047117	MREGAD:	.ASCIZ	<15><12>/CONTROL REGISTER ADDRESS-
3437	015732	051124	046117	051040			
3438	015740	043505	051511	042524			
3439	015746	020122	042101	051104			
3440	015754	051505	026523	000			
3441	015761	040	037440	000	MQM:	.ASCIZ	/ ? /
3442	015765	015	000012		MCRLF:	.ASCIZ	<15><12>
3443	015770	020040	047520	042527	MPFAIL:	.ASCIZ	/ POWER FAILURE, PROGRAM RESTART AT TEST IN PROGRESS
3444	015776	020122	040506	046111			
3445	016004	051125	026105	050040			
3446	016012	047522	051107	046501			
3447	016020	051040	051505	040524			
3448	016026	052122	040440	020124			
3449	016034	042524	052123	044440			
3450	016042	020116	051120	043517			

EO6

DDMC MACY11 27.732 16-MAR-75 09:17 PAGE 70  
DDMCB.PFC

3454	016050	042522	051523	000
3455	016055	015	042012	042132 NEPASS: .ASCIZ <15><12>/DDMC/
3456	016060	041510	051000	
3457	016065	015	051012	000 MR: .ASCIZ <15><12>/R/
3458	016071	015	052012	051000 MT\$TPC: .ASCIZ <15><12>/TEST PC-1
3459	016076	020124	041520	000055

:TABLE OF POINTERS FOR TRAP DECODING

3460	016104	014122
3461	016106	014414
3462	016110	015014
3463	016112	014526
3464	016114	014620
3465	016116	014630
3466	016120	015112
3467	016122	015232
3468	016124	014222

TRPTAB: SCOPER  
TYPER  
OCTASN  
INSTRG  
INSTRE  
PARAMS  
SVOSP  
RSOS  
SCOP1R

:BUFFERS FOR INPUT-OUTPUT

3475	016126	000000
3476	016140	.=.+10
3477	016140	000000
3478	016152	.=.+10
3479	016152	000000
3480	016164	016164

INBUF: 0  
TEMP: 0  
MDATA: 0  
.=.+10

:TABLE OF POINTERS TO ERROR MESSAGES AND DATA

3484	016164	016164
3485	016164	016230
3486	016166	016656
3487	016170	016310
3488	016172	000000
3489	016174	016325
3490	016176	000000
3491	016200	016356
3492	016202	016656
3493	016204	016415
3494	016206	016656
3495	016210	016453
3496	016212	000000
3497	016214	016507
3498	016216	016656
3499	016220	016544
3500	016222	016656
3501	016224	016603
3502	016226	016670
3503	016230	047125 054105 042520 EMO: .ASCII /UNEXPECTED INTERRUPT/
3504	016236	052103 042105 044440
3505	016244	052116 051105 052522
3506	016252	052120

ERRTAB: EMO  
DT1  
EM1  
0  
EM2  
0  
EM3  
DT1  
EM4  
DT1  
EM5  
0  
EM6  
DT1  
EM7  
DT1  
EM10  
DT2

3507	016254	005015 047503 052116 .ASCIZ <15><12>/CONTROL REGISTER CONTENTS
3508	016262	047522 020114 042522
3509	016270	044507 052123 051105

## F06

022405 MACY11 27:7321 16-MAR-76 09:17 PAGE 71  
022405.PFC

3510	016276	041440	047117	042524	
3511	016304	052116	000123		
3512	016310	047516	044440	052116	EM1: .ASCIIZ /NO INTERRUPT/
3513	016316	051105	052522	052120	
3514	016324	000			
3515	016325	124	040522	051516	EM2: .ASCIIZ /TRANSMITTER DONE NOT SET/
3516	016332	044515	052124	051105	
3517	016340	042040	047117	020105	
3518	016346	047516	020124	042523	
3519	016354	000124			
3520	016356	052502	020123	042101	EM3: .ASCII /BUS ADDRESS ERROR/
3521	016354	051104	051505	020123	
3522	016372	051105	047522	122	
3523	016377	015	042412	050130	.ASCIIZ <15><12>/EXP REC/
3524	016404	020040	020040	051040	
3525	016412	041505	000		
3526	016415	102	052131	020105	EM4: .ASCII /BYTE COUNT ERROR/
3527	016422	047503	047125	020124	
3528	016430	051105	047522	122	
3529	016435	015	042412	050130	.ASCIIZ <15><12>/EXP REC/
3530	016442	020040	020040	051040	
3531	016450	041505	000		
3532	016453	103	040510	040522	EM5: .ASCII /CHARACTER AVAILABLE NOT SET/
3533	016460	052103	051105	040440	
3534	016466	040526	046111	041101	
3535	016474	042514	047040	052117	
3536	016502	051440	052105	000	
3537	016507	123	046111	020117	EM6: .ASCII /SILO DATA ERROR/
3538	016514	040504	040524	042440	
3539	016522	051122	051117		
3540	016526	005015	054105	020120	.ASCIIZ <15><12>/EXP REC/
3541	016534	020040	020040	042522	
3542	016542	000103			
3543	016544	044523	047514	051440	EM7: .ASCII /SILO STATUS ERROR/
3544	016552	040524	052524	020123	
3545	016560	051105	047522	122	
3546	016565	015	042412	050130	.ASCIIZ <15><12>/EXP REC/
3547	016572	020040	020040	051040	
3548	016600	041505	000		
3549	016603	123	046111	020117	EM10: .ASCII /SILO ALARM ERROR/
3550	016610	046111	051101	020115	
3551	016616	051105	047522	122	
3552	016623	015	040412	040514	.ASCIIZ <15><12>/ALARM LEVEL FILL LEVEL/
3553	016630	046522	046040	053105	
3554	016636	046105	020040	044506	
3555	016644	046114	046040	053105	
3556	016652	046105	000		
3557		016656			.EVEN
3558					;DATA TABLES FOR ERROR OUTPUT
3559					
3560					
3561	016656	000002			DT1: 2
3562	016660	006	002		.BYTE 6,2
3563	016662	015442			.BYTE SAVR5
3564	016664	006	000		.BYTE 6,0
3565	016666	015440			.BYTE SAVR4

G06

DDHIC MACYII 27(732) 16-MAR-76 09:17 PAGE 72  
DDHICB.PFC

3566	016670	000002		DT2:	2
3567	016672	002	014	.BYTE	2,14
3569	016674	015442			SAVR5
3570	016676	002	000	.BYTE	2,0
3570	016700	015436			SAVR3
3571	016702	000000		ENDOD:	0
3572		000001		.END	



DZDHC MACY11 27(732) 16-MAR-76 09:17 PAGE 75  
DZDHC8.PFC CROSS REFERENCE TABLE -- USER SYMBOLS

DZDHC MACY11 27(732) 16-MAR-76 09:17 PAGE 76  
 DZDHC8.PFC CROSS REFERENCE TABLE -- USER SYMBOLS

HILIM	015006	3214*	3240	3256*											
ICOUNT	015424	989*	1022*	1056*	1091*	1128*	1165*	1202*	1241*	1301*	1361*	1421*	1491*	1541*	
		1601*	1661*	1721*	1781*	1841*	1901*	1961*	2021*	2081*	2141*	2202*	2246*	2290*	
		2334*	2378*	2422*	2466*	2510*	2554*	2598*	2642*	2686*	2730*	2774*	2818*	2862*	
		2909*	2949*	2993*	3028*	3095	3373*								
INBUF	016126	3192	3220	3475*											
INIFLG	015450	914	925	956	958*	3383*									
INSTER=	104404	886*	3235												
INSTR =	104403	885*	938	946	967										
INSTRE	014620	3205*	3467												
INSTRG	014526	3188*	3465												
INSTRI	014540	3190*	3207												
INSTR2	014626	3199	3208*												
LAST	015454	3072*	3118	3120*	3385*	3422*									
LIGHTS=	177570	574*	3075*												
LIMITS	014740	3230	3240*												
LINE =	000000	1232*	1292*	1352*	1412*	1472*	1532*	1592*	1652*	1712*	1772*	1832*	1892*	1952*	
		2012*	2072*	2132*	2192*	2235*	2280*	2324*	2368*	2412*	2456*	2500*	2544*	2589*	
		2632*	2676*	2720*	2764*	2808*	2852*	2896*							
LOAD	015316	2208	2252	2296	2340	2384	2428	2472	2516	2560	2604	2648	2692	2736	
		2780	2824	2868	3339*										
LOBITS	015012	3216*	3244	3258*	3259										
LOGICA	014106	892	3079*												
LOLIM	015004	3213*	3242	3255*											
LPCNT	015426	3094*	3095	3097*	3374*										
MCRLF	015765	3264	3445*												
MDATA	016152	3283	3294	3479*											
MEPASS	016055	3071	3455*												
MFFAIL	015770	3420	3446*												
MGM	015761	3206	3444*												
MR	016065	980	3457*												
MREGAD	015725	947	3439*												
MSG	014542	3188*	3191*												
MTITLE	015624	913	3427*												
MTSTPC	016071	968	3458*												
MVECTO	015703	939	3435*												
N =	000001	1*													
OCTASC=	104402	884*	3136	3143	3417										
OCTASN	015014	3263*	3465												
PARAM =	104405	887*	940	948	969										
PARAMS	014630	3212*	3468												
PARAM1	014660	3219*	3236												
PAPERR	014734	3222	3224	3226	3235*	3241	3243	3245							
PASCNT	015412	909*	3074*	3075	3368*										
PC =%000007		569*	1244*	1304*	1364*	1424*	1484*	1544*	1604*	1664*	1724*	1784*	1844*	1904*	
		1964*	2024*	2084*	2144*	2206*	2268*	2250*	2252*	2294*	2295*	2339*	2370*	2393*	
		2384*	2426*	2428*	2470*	2472*	2514*	2516*	2558*	2560*	2602*	2604*	2646*	2675*	
		2690*	2692*	2734*	2736*	2778*	2780*	2822*	2824*	2866*	2868*	3079*	3335*	3375*	
PFAIL	015460	867	907	3390*	3411										
PFTAB	015614	3418	3424*												
POPRO =	012600	583*	3151												
POP1SP=	005726	581*													
PCP2SP=	022626	585*													
PS =	177776	575*	905*	963*	987*	999*	1001*	1021*	1033*	1035*	1055*	1067*	1069*	1093*	
		1103*	1105*	1127*	1140*	1142*	1164*	1177*	1179*	1201*	1214*	1216*	1240*	1251*	
		1300*	1314*	1360*	1374*	1420*	1434*	1480*	1494*	1540*	1554*	1600*	1617*	1663*	



## LOG

DODMC MACY11 27.732) 16-MAR-76 09:17 PAGE 78  
DODMCR.PFC CROSS REFERENCE TABLE -- USER SYMBOLS

SAVPC	015446	3159	3305*	3382*													
SAVRO	015430	3314*	3318	3375*													
SAVR1	015432	3313*	3319	3376*													
SAVR2	015434	3312*	3320	3377*													
SAVR3	015436	3311*	3321	3378*	3570												
SAVR4	015440	3310*	3322	3379*	3565												
SAVR5	015442	3309*	3323	3380*	3563	3568											
SAVSP	015444	3381*	3397*	3404													
SAVSP=	104406	888*	3122														
SCOPE	= 104400	882*	1015	1049	1083	1120	1157	1194	1231	1291	1351	1411	1471	1531			
		1591	1651	1711	1771	1831	1891	1951	2011	2071	2131	2191	2235	2279			
		2323	2367	2411	2455	2499	2543	2587	2631	2675	2719	2763	2907	2951			
		2895	2941	2975	3019	3061											
SCOPER	014122	3088*	3453														
SCOPE1	= 104410	990*	2969	3015	3054												
SCOPIR	014222	3109*	3471														
SIZE	001056	917*															
SP	= .0000006	568*	906*	964*	1005*	1009*	1039*	1043*	1073*	1077*	1110*	1114*	1147*	1151*			
		1184*	1188*	1221*	1225*	1290*	1350*	1410*	1470*	1530*	1590*	1650*	1710*	1770*			
		1830*	1890*	1950*	2010*	2070*	2130*	2190*	2940*	3099	3101*	3111*	3118	3120			
		3123	3149	3155*	3165*	3166*	3167*	3168*	3169*	3170*	3171*	3172	3176	3177*			
		3188	3189*	3212	3218*	3265	3266*	3305	3390*	3391*	3392*	3393*	3394*	3395*			
		3396*	3397	3404*	3405	3406	3407	3408	3409	3410	3413*						
SPACNT	= 015167	3269*	3287	3290*	3300*												
STACK	= 017102	576*	906	964	1290	1350	1410	1470	1530	1590	1650	1710	1770	1830			
START	001000	874	905*														
STFLG	015452	908*	977	979*	3384*												
SV05	015200	3309*															
SV05P	015172	3305*	3469														
SWR	= 177570	573*	927	965	3088	3090	3092	3109	3115	3146	3153						
SWO0	= 000001	556*	927														
SW01	= 000002	555*	965														
SW02	= 000004	554*															
SW03	= 000010	553*															
SW04	= 000020	552*															
SW05	= 000040	551*															
SW06	= 000100	550*															
SW08	= 000400	549*															
SW09	= 001000	548*	3109														
SW10	= 002000	547*	3088														
SW11	= 004000	546*	3092		3153												
SW12	= 010000	545*															
SW13	= 020000	544*	3116														
SW14	= 040000	543*	3090														
SW15	= 100000	542*															
TEMP	016140	3273	3414*	3415*	3477*												
TKCSR	015346	3194	3348*														
TKDBR	015350	3196	3200	3349*													
TPCSR	015352	3178	3201	3350*													
TPCBR	015354	3183*	3200*	3351*													
TRPOK	014454	3168*															
TRFSRV	014442	871	3165*														
TRPTAB	016104	3170	3463*														
TYPDAT	014356	3135	3141*														
TYPE	= 104401	883*	913	980	3070	3139	3190	3205	3263	3293	3419						

## MO6

DZDHC MACY11 27(732) 16-MAR-76 09:17 PAGE 79  
 DZDHC.PFC CROSS REFERENCE TABLE -- USER SYMBOLS

TYPER	014474	3176*	3464											
TYPMSC	014340	3133	3136*											
T1	001334	976	987*											
T10	003032	1240*												
T11	003270	1300*												
T12	003526	1360*												
T13	003764	1420*												
T14	004222	1480*												
T15	004460	1540*												
T16	004716	1600*												
T17	005154	1660*												
T2	001516	1021*												
T20	005412	1720*												
T21	005650	1780*												
T22	006106	1840*												
T23	006344	1900*												
T24	006602	1960*												
T25	007040	2020*												
T26	007276	2080*												
T27	007534	2140*												
T3	001700	1055*												
T30	007772	2201*												
T31	010142	2245*												
T32	010312	2289*												
T33	010462	2333*												
T34	010632	2377*												
T35	011002	2421*												
T36	011152	2465*												
T37	011322	2509*												
T4	002062	1090*												
T40	011472	2553*												
T41	011642	2597*												
T42	012012	2641*												
T43	012162	2685*												
T44	012332	2729*												
T45	012502	2773*												
T46	012552	2817*												
T47	013022	2861*												
T5	002254	1127*												
T50	013172	2908*												
T51	013356	2947*												
T52	013512	2982*												
T53	013672	3027*												
T6	002446	1164*												
T7	002640	1201*												
VEC1	001120	915	927*											
VEC2	001130	926	929*											
WRDCNT	015164	3267*	3295*	3298*										
X	= 000000	1*												
XBIT	= 000001	1232*	2192*	2896*										
XLINE	= 000000	1232*	2192*	2896*										
XN	= 000054	1*	987	990*	1021	1024*	1055	1058*	1090	1093*	1127	1130*	1164	1167*
		1201	1204*	1240	1243*	1300	1303*	1360	1363*	1420	1423*	1490	1483*	1540
		1543*	1600	1603*	1660	1663*	1720	1723*	1780	1783*	1840	1843*	1900	1903*
		1960	1963*	2020	2023*	2080	2083*	2140	2143*	2201	2204*	2245	2248*	2299
		2292*	2333	2336*	2377	2380*	2421	2424*	2465	2468*	2509	2512*	2553	2556*

## NO6

DZDHC MACY11 27(732) 16-MAR-76 09:17 PAGE 80  
 DZDHC8.PFC CROSS REFERENCE TABLE -- USER SYMBOLS

	2597	2600*	2641	2644*	2685	2688*	2729	2732*	2773	2776*	2817	2820*	2851
Y	2864*	2908	2911*	2947	2951*	2982	2986*	3027	3031*	889*	890*	891*	
.	= 000011	1*	882	883*	884*	985*	886*	887*	888*	889*	890*	891*	
.	= 016704	606*	607	609	611	613	615	617	619	621	623	625	627
	631	633	635	637	639	641	643	645	647	649	651	653	655
	657	659	661	663	665	667	669	671	673	675	677	679	681
	683	685	687	689	691	693	695	697	699	701	703	705	707
	709	711	713	715	717	719	721	723	725	727	729	731	733
	735	737	739	741	743	745	747	749	751	753	755	757	759
	761	763	765	767	769	771	773	775	777	779	781	783	785
	787	789	791	793	795	797	799	801	803	805	807	809	911
	813	815	817	819	821	823	825	827	829	831	833	835	837
	839	841	843	845	847	849	851	853	855	857	859	861	966*
	873*	891*	893*	895*	3039	3400	3416	3476*	3478*	3480*	3557*		

MACROS.PRC 16-MAR-76 09:17 PAGE 82  
CROSS REFERENCE TABLE -- MACROS NAMES

1180	1197	1217	1224
1198	1201	1237	1237
1200	1204	1243	1243
1201	1207	1257	1257
1202	1208	1267	1267
1203	1209	1274	1274
1204	1210	1287	1287
1205	1211	1297	1297
1206	1212	1307	1307
1207	1213	1317	1317
1208	1214	1327	1327
1209	1215	1337	1337
1210	1216	1347	1347
1211	1217	1357	1357
1212	1218	1367	1367
1213	1219	1377	1377
1214	1220	1387	1387
1215	1221	1397	1397
1216	1222	1407	1407
1217	1223	1417	1417
1218	1224	1427	1427
1219	1225	1437	1437
1220	1226	1447	1447
1221	1227	1457	1457
1222	1228	1467	1467
1223	1229	1477	1477
1224	1230	1487	1487
1225	1231	1497	1497
1226	1232	1507	1507
1227	1233	1517	1517
1228	1234	1527	1527
1229	1235	1537	1537
1230	1236	1547	1547
1231	1237	1557	1557
1232	1238	1567	1567
1233	1239	1577	1577
1234	1240	1587	1587



REF ID: A671112773321  
 1965-66 REFERENCE TABLE -- PERMANENT SYMBOLS  
 PAGE 95

235	1315 3295	1325 2290	1435 295.	1435 2961	1555 2994	1675 3002	1735 3034	1795 3039	1855 3041	1915 3203	1975 3281	2035 3299	2095 3345	2364 3347	2364 3348	2364 3349	2364 3350	2364 3351	2364 3352	2364 3353	2364 3354	2364 3355	2364 3356	2364 3357	2364 3358	2364 3359	
236	1316 3296	1326 2291	1436 2962	1436 2963	1556 2995	1676 3003	1736 3035	1796 3036	1856 3042	1916 3204	1976 3282	2036 3297	2096 3346	2365 3349	2365 3350	2365 3351	2365 3352	2365 3353	2365 3354	2365 3355	2365 3356	2365 3357	2365 3358	2365 3359	2365 3360	2365 3361	
237	1317 3297	1327 2292	1437 2964	1437 2965	1557 2996	1677 3004	1737 3037	1797 3038	1857 3043	1917 3205	1977 3283	2037 3298	2097 3347	2366 3351	2366 3352	2366 3353	2366 3354	2366 3355	2366 3356	2366 3357	2366 3358	2366 3359	2366 3360	2366 3361	2366 3362	2366 3363	
238	1318 3298	1328 2293	1438 2966	1438 2967	1558 2997	1678 3005	1738 3039	1798 3039	1858 3044	1918 3206	1978 3284	2038 3299	2098 3348	2367 3353	2367 3354	2367 3355	2367 3356	2367 3357	2367 3358	2367 3359	2367 3360	2367 3361	2367 3362	2367 3363	2367 3364	2367 3365	
239	1319 3299	1329 2294	1439 2968	1439 2969	1559 2998	1679 3006	1739 3040	1799 3040	1859 3045	1919 3207	1979 3285	2039 3300	2099 3349	2368 3355	2368 3356	2368 3357	2368 3358	2368 3359	2368 3360	2368 3361	2368 3362	2368 3363	2368 3364	2368 3365	2368 3366	2368 3367	2368 3368

215

44  
46  
48

CCCAC 080:11 27.732) 16-MAR-76 09:17 PAGE 86  
CCCAC.PFC CROSS REFERENCE TABLE -- PERMANENT SYMBOLS

!@#;	2611	2615	2616	2641	2642	2643	2644	2649	2652	2655	2659	2660	2685	2695	
@<>	2689	2693	2694	2696	2697	2698	2699	2700	2701	2702	2703	2704	2740	2747	
@<>	2831	2845	2851	2861	2862	2863	2864	2865	2866	2867	2868	2870	2880	2895	
@<>	2951	2953	2956	2961	2962	2963	2964	2965	2966	2967	2968	2969	2970	2974	
@<>	3021	3025	3028	3029	3030	3032	3033	3034	3037	3075	3076	3099	3101	3111	
@<>	3125	3214	3215	3218	3220	3249	3250	3265	3267	3270	3271	3273	3274	3279	
@<>	3219	3310	3311	3312	3313	3314	3315	3318	3319	3320	3321	3322	3323	3329	
@<>	3390	3411	3412	3413	3416	3418	3419	3420	3421	3422	3423	3424	3425	3429	
@<>	3446	3056	3183	1034	1068	1154	1141	1178	1215	3080	3081	3092	3272	3277	
@<>	3078	3426											3284	3289	
@<>	3058	1010	1040	1044	1074	1078	1111	1115	1148	1152	1185	1189	1222	1226	
@<>	3056	3110	3156	3182	3208	3254	3297	3315	3324					3100	
@<>	3055	2989	3124	3166											
.1399	882	883	884	885	975	995	996	987	988	989	990	1322	1339	1379	
.1739	944	945	946	947	1459	1498	1502	1519	1559	1562	1579	1618	1639	1678	
.2038	3146	2562	2606	2650	2694	2738	2782	2826	2862	2879	2919	2922	1922	1939	
.2430	3503	3520	3526	3537	3543	3544	3545	3549	3555	3557	3564	3567	3570	3572	
.2734	3427	3435	3439	3444	3445	3446	3446	3446	3457	3458	3458	3507	3512	3515	
.3134	3540	3546	3552	952	953	973	974	3158	3562	3564	3567	3569	3523	3529	
.3532	539	945	952	953	973	974	3158	3562	3564	3567	3569				
.3846	3572	924	927	954	956	990	1024	1058	1093	1130	1157	1204	1243	1303	
.4248	1423	1483	1543	1603	1663	1723	1783	1843	1903	1963	2023	2093	2143	2204	
.4656	2292	2296	2336	2380	2424	2468	2512	2556	2600	2644	2688	2732	2776	2920	
.5011	2951	2986	3031	3031	2424	2468	2512	2556	2600	2644	2688	2732	2776	2920	
.5398	3557	915	917	924	954	990	1024	1058	1093	1130	1167	1204	1243	1303	
.5755	1423	1483	1543	1603	1663	1723	1783	1843	1903	1963	2023	2093	2143	2204	
.6153	2296	2336	2380	2424	2468	2512	2556	2600	2644	2688	2732	2776	2920	2954	
.6559	2952	3357	3386	539	893	884	885	886	887	988	889	990	891	992	
.6956	3036	3036	3036	1167	1204	1204	1232	1243	1292	1303	1352	1363	1412	1472	
.7357	2297	2336	2380	2424	2468	2512	2556	2600	2644	2688	2732	2776	2920	2954	
.7755	2953	3352	3386	539	893	884	885	886	887	988	889	990	891	992	
.8154	3427	3435	3439	3444	3445	3446	3446	3446	3457	3458	3458	3507	3512	3515	
.8553	2336	2380	2424	2468	2512	2556	2600	2644	2688	2732	2776	2920	2954	2994	
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F07

DZDHC8 MAC111 371732 16-MAR-76 09:17 PAGE 87  
DZDHC8.PFC CROSS REFERENCE TABLE -- PERMANENT SYMBOLS

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	1532	1953	2012	2025	2072	2093	2132	2143	2192	2204	2236	2248	1973	1892	1903		
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.REM																	
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CORE USED: 12K (23 PAGES)

