

# CR11/CM11F

DIAGNOSTIC  
MD-11-DZCRB-C

EP-DZCRB-C-DL-A

NOV 1976

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FICHE 1 OF 1

MADE IN U.S.A.

This microfiche card contains a grid of frames, each displaying diagnostic data for an MD-11 aircraft. The data is organized into columns and rows, with each frame containing a specific set of information, likely related to engine performance, system status, or fault codes. The frames are arranged in a regular grid pattern, with some frames appearing to contain text and others containing graphical representations or data tables. The overall layout is dense and structured, typical of diagnostic data storage on microfiche.

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DZCRB-C CR11/CM11F DIAGNOSTIC TEST  
DZCRB.SRC

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IDENTIFICATION

PRODUCT CODE: MAINDEC-11-DZCRB-C  
PRODUCT NAME: CR11/CM11F DIAGNOSTIC TEST  
PROGRAM DATE: APRIL 1976  
MAINTAINER: DIAGNOSTIC GROUP

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1. ABSTRACT

THIS TEST IS TO BE USED AS A CARD READER DIAGNOSTIC FOR THE PDP-11 WITH THE CR11 CARD READER. IT TESTS ALL LOGIC FUNCTIONS OF THE CARD READER, AND INCLUDES AN EXERCISER FOR ALPHANUMERIC AND BINARY TEST DECKS. A SEPARATE STARTING ADDRESS ALLOWS THE ERROR SENSING FUNCTIONS OF THE G.D.I. OR DOCUMENTATION READER TO BE CHECKED. ANOTHER STARTING ADDRESS TESTS SPECIAL DECKS WHICH HAVE ALL COLUMNS AND CARDS PUNCHED IDENTICALLY, TO AID IN DIAGNOSING SPECIAL PROBLEMS.

2. REQUIREMENTS

2.1 EQUIPMENT

PDP-11 STANDARD COMPUTER  
CR11 CARD READER OR  
CM11F CARD READER

2.2 TEST DECKS

MAINDEC-00-DZCRA-A-CA ALPHANUMERIC TEST DECK (ROTATING PATTERN)  
WITH CLOCK MARKS.  
MAINDEC-00-DZCRA-A-CB BINARY TEST DECK (ROTATING PATTERN)  
WITH CLOCK MARKS.  
MAINDEC-00-DZCMA-A-CA ALPHANUMERIC TEST DECK (SAME PATTERN)  
MAINDEC-00-DZCMA-A-CB BINARY TEST DECK (SAME PATTERN)  
MAINDEC-00-DZCMB-A-CO MARK SENSE BINARY (SAME PATTERN)

EXTRA CARDS (FOR ERROR FUNCTION TEST)

2.3 STORAGE

THE PROGRAM RUNS IN BK MEMORY.

3. LOADING PROCEDURE

PROCEDURE FOR NORMAL ABSOLUTE TAPES SHOULD BE FOLLOWED.

4. STARTING PROCEDURE

THIS PROGRAM HAS BEEN MODIFIED TO RUN ON A PROCESSOR WITH OR WITHOUT A HARDWARE SWITCH REGISTER. WHEN FIRST EXECUTED THE PROGRAM TESTS THE EXISTENCE OF A HARDWARE SWITCH REGISTER. IF NOT FOUND A SOFTWARE SWITCH REGISTER LOCATION (SWREG=LOC. 176 ) IS DEFAULTED TO. IF THIS IS THE CASE, UPON EXECUTION THE CONTENTS OF THE SWREG ARE DUMPED IN OCTAL ON THE CONSOLE TTY AND ANY CHANGES ARE REQUESTED

(IE) SWR=XXXXXX NEW=

POSSIBLE RESPONSES ARE:

1. (CR) IF NO CHANGES ARE TO BE MADE
2. 6 DIGITS 0-7 TO REPRESENT IN OCTAL THE NEW SWITCH REGISTER

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VALUE ;LAST DIGIT FOLLOWED BY <CR>.  
TO ALLOW REENTERING VALUE IF ERROR IS COMMITTED  
KEYING IN SWREG VALUE.

BUILT INTO THE PROGRAM IS THE ABILITY TO DYNAMICALLY CHANGE THE CONTENTS OF SWREG DURING PROGRAM EXECUTION. BY STRIKING 1G (CNTRL G) ON CONSOLE TTY THE OPERATOR SETS A REQUEST FLAG TO CHANGE THE CONTENTS OF SWREG, WHICH IS PROCESSED IN KEY AREAS OF THE PROGRAM CODE (IE) ERROR ROUTINES, AFTER HALTS END OF PASS, AND OTHER APPLICABLE AREAS.

4.1 CONTROL SWITCH SETTINGS

BASIC SWITCH REGISTER SETTINGS ARE:

- SW15=1 OR UP---HALT ON ERROR
- SW14=1 OR UP---SCOPE LOOP
- SW13=1 OR UP---INHIBIT PRINT OUT
- SW12=1 OR UP---INHIBIT TRACE TRAPPING
- SW11=1 OR UP---INHIBIT SUB-PROGRAM ITERATION  
(NOTE THAT IF SW11 IS SET, THE CARD COUNT WILL BE ALTERED, CAUSING FAILURES IN THE DATA TEST SECTION.)
- SW10=1 OR UP---CR11 CONTROLLER USES THE M829 MODULE  
(IF SW10 & SW09 IS DOWN, ASSUMES THE M8291 MODULE)
- SW09=1 OR UP---THE M8290 CR11 CONTROL BOARD IS BEING USED  
(IF SW10 & SW09 IS DOWN, ASSUMES THE M8291 MODULE)
- SW08=1 OR UP---LOOP ON THE MAINTENANCE TEST PORTION OF THIS DIAGNOSTIC (MUST BE M8291 CONTROL MODULE FOR CR11/CM11F).
- SW07=1 OR UP---LOOP THRU THE INSTRUCTION TEST PORTION  
NOTE: DATA ERRORS MAY OCCUR IF SW7 IS SET, THEN CLEARED.  
ALSO THE TEST MAY HANG WHEN THE INPUT HOPPER GOES EMPTY IF SW7 WAS SET.
- SW06=1 OR UP---RETURN TO THE BEGINNING OF THE INSTRUCTION TEST WHEN CONTINUING FROM ONE DECK TO ANOTHER
- SW05=1 OR UP---HALT BETWEEN TEST DECKS  
(SEE 5.2.1 FOR EXPLANATION OF SW5=0)
- SW04=1 & SW02=0 --- RUN BINARY TEST DECK M-00-DZCRA-A-CB
- SW04=0 & SW02=0 --- RUN ALPHA TEST DECK M-00-DZCRA-A-CA
- SW04=1 & SW02=1 --- RUN BINARY TEST DECK M-00-DZCMA-A-CB
- SW04=0 & SW02=1 --- RUN ALPHA TEST DECK M-00-DZCMA-A-CA
- SW03=1 OR UP---MARK SENSE BINARY TEST DECK M-00-DZCMB-A-CO
- SW00=1 OR UP---DISABLE TEST TESTG(DARK-LIGHT TEST)

4.2 STARTING ADDRESSES

- 200 = INSTRUCTION AND DATA TEST
- 204 = ERROR FUNCTION TEST (WITH G.D.I. READER)
- 210 = ERROR FUNCTION TEST (WITH DOCUMENTATION READER)
- 214 = SINGLE SUBTEST LOOP
- 220 = READ SINGLE DATA PATTERN TEST

4.3 PROGRAM AND/OR OPERATOR ACTION

4.3.1 INSTRUCTION AND DATA RELIABILITY TEST (SA 200)

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LOAD PROGRAM INTO MEMORY.  
LOAD ONE TEST DECK IN THE CARD READER INPUT HOPPER.  
PRESS MOTOR START AND READ START ("RESET" ON DOCUMENTATION READER).  
SET SWITCH REGISTER TO STARTING ADDRESS.  
LOAD ADDRESS.  
IF HARDWARE SWITCH REGISTER IS AVAILABLE SET SWITCH SETTINGS BEFORE PRESSING START. IF SWITCH-LESS MACHINE SIMPLY PRESS START.  
WHEN THE INPUT HOPPER IS EMPTY THE PROGRAM WILL HANG WAITING FOR AN INTERRUPT FROM THE CARD READER. LOAD ONE OR MORE TEST DECKS INTO THE INPUT HOPPER. PRESSING "MOTOR START" AND "READ START" ("RESET" ON DOCUMENTATION READER) ON THE CARD READER SHOULD CAUSE PROGRAM EXECUTION TO RESUME.  
THIS ENTIRE SEQUENCE IS NECESSARY TO RUN THE FULL TEST ON THE CARD READER.  
ALL PRINTOUTS INDICATE FAILURE, INCLUDING THOSE SAYING THAT BIT 8 OR BIT 15 WAS SET.

4.3.2 ERROR FUNCTION TEST (SA 204 OR 210)

LOAD A FEW SPARE CARDS INTO THE INPUT HOPPER (DO NOT LOAD A TEST DECK-THIS TEST IS DESTRUCTIVE!)  
PRESS "MOTOR START" AND "READ START" ("RESET" ON DOCUMENTATION READER) ON THE CARD READER.  
LOAD THE STARTING ADDRESS.  
IF HARDWARE SWITCH REGISTER IS AVAILABLE SET SWITCH SETTINGS BEFORE PRESSING START. IF SWITCH-LESS MACHINE SIMPLY PRESS START.  
FOLLOW THE INSTRUCTIONS AS THEY ARE PRINTED OUT.

4.3.3 SINGLE SUBTEST LOOP (SA 214)

LOAD CARDS (SPARE CARDS OR A TEST DECK) INTO THE INPUT HOPPER.  
PRESS "MOTOR START" AND "READ START" ("RESET" ON DOCUMENTATION READER) ON THE CARD READER.  
LOAD THE STARTING ADDRESS.  
IF HARDWARE SWITCH REGISTER IS AVAILABLE SET SWITCH SETTINGS BEFORE PRESSING START. IF SWITCH-LESS MACHINE SIMPLY PRESS START.  
WHEN ASKED ENTER THE STARTING ADDRESS OF THE DESIRED TEST (ADDRESS OF THE TESTXX TAG, WHERE XX MAY BE 1 THRU 24 OR A THRU G OR TSTMD0-22).

4.3.4 SINGLE DATA PATTERN TEST (SA 220)

A SPECIAL DECK (1 OR MORE CARDS) MUST BE PUNCHED TO RUN THIS TEST. ANY DATA PATTERN MAY BE USED, BUT IT MUST BE IDENTICAL IN ALL 80 COLUMNS OF ALL THE CARDS (I.E. ONLY ONE PIECE OF DATA).  
LOAD THIS PREPARED DECK INTO THE INPUT HOPPER.  
PRESS CARD READER "MOTOR START" AND "READ START" ("RESET" ON DOCUMENTATION READER).  
LOAD SA 220.  
IF HARDWARE SWITCH REGISTER IS AVAILABLE SET SWITCH SETTINGS BEFORE PRESSING START. IF SWITCH-LESS MACHINE SIMPLY

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PRESS START.  
WHEN THE CARD READER RUNS OUT OF CARDS IT WILL RING THE BELL.  
RELOADING THE DECK AND PRESSING "READ START" ("RESET") ON THE CARD  
READER WILL CONTINUE THE TEST.

5. OPERATING PROCEDURE

5.1 OPERATIONAL SWITCH SETTINGS

5.1.1 AT SA 200 (INSTRUCTION AND DATA RELIABILITY TEST)

SEE 4.1

5.1.2 AT SA 204 OR 210 (ERROR FUNCTION TEST FOR CR11/CM11)

SM00=1 TO INHIBIT TESTING THE DARK-LIGHT ERROR.  
SM14=1 TO LOOP THRU THE CURRENT SUBTEST  
SM15=1 TO HALT ON ERROR

5.1.3 AT SA 220 (SINGLE SUBTEST LOOP)

SEE 4.1 FOR SR OPTIONS

5.1.4 AT SA 220 (SINGLE DATA PATTERN TEST)

SM15=1 TO HALT ON ERROR  
SM13=1 TO INHIBIT PRINTOUT

5.2 SUBROUTINE ABSTRACTS

5.2.1 BEGIN SA 200

THE INSTRUCTION TESTS ARE RUN FIRST, FOLLOWED BY THE DATA  
RELIABILITY TESTS ON THE REMAINING CARDS IN THE FIRST TEST DECK.  
AT THE END OF THE DECK THE BELL WILL RING, AND IF SM5=1 THE  
PROGRAM HALTS. IF SM5=0, PROGRAM ACTION DEPENDS ON THE NUMBER  
OF TEST DECKS LOADED. IF THERE ARE STILL CARDS IN THE INPUT HOPPER,  
THE PROGRAM WILL RUN THE DATA RELIABILITY TEST ON THE ENTIRE NEXT DECK.  
IF THE INPUT HOPPER IS EMPTY AT THE END OF A DECK, THE PROGRAM  
WILL RUN A SET OF TESTS OF OFF-LINE OPERATIONS. AT THE END OF  
THESE TESTS, IT WAITS FOR THE CARD READER TO BE PUT BACK ON-LINE.  
FURTHER CHECKS ARE MADE OF THE OFF-LINE TO ON-LINE OPERATIONS,  
AND THEN THE DATA RELIABILITY TEST IS RUN ON THE ENTIRE DECK.  
IF SM5=1, HITTING CONTINUE WILL RESUME PROGRAM OPERATION AFTER  
THE HALT. IF ALL OTHER SWITCHES WERE DOWN, FOR EXAMPLE, THE  
DATA RELIABILITY TEST WOULD THEN BE RUN ON THE NEXT DECK. THE  
OTHER SWITCHES AFFECT PROGRAM FLOW AS NOTED IN 4.1.

5.2.2 SCOPE

THIS SUBROUTINE CALL IS PLACED BETWEEN EACH SUBTEST IN THE  
INSTRUCTION SECTION. IT RECORDS THE STARTING ADDRESS OF EACH  
SUB-TEST AS IT IS BEING ENTERED. IF A SCOPE LOOP IS REQUESTED,  
IT WILL JUMP TO THE START OF THE SUBTEST THAT THE SCOPE LOOP  
IS REQUESTED FOR. IF SCOPE LOOP IS NOT REQUESTED, THERE WILL

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BE 1 ITERATION ON THAT SUBTEST BEFORE THE NEXT SUBTEST IS ENTERED. SWITCH 11 ON A 1 INHIBITS ITERATION OF SUBTESTS.

5.2.3 HLT

THIS SUBROUTINE PRINTS OUT THE LOCATION COUNTER AT THE TIME OF FAILURE, AND THE CONTENTS OF THE PROCESSOR STATUS REGISTER. NOTE THAT THE LOCATION COUNTER WILL BE THE ADDRESS OF THE HLT.

5.2.4 TTRAP

THIS ROUTINE ALLOWS THE TRACE BIT TO BE SET AFTER THE FIRST LOOP OF THE PROGRAM. THE TRACE BIT WILL BE SET ON ALTERNATE LOOPS OF THE INSTRUCTION TEST, AND ON ALL LOOPS OF THE CHANNEL TEST UNLESS SW12 IS SET. THE FIRST INSTRUCTION EXECUTED UPON TRAPPING IS AN "RTI" WHICH RETURNS TO THE INTERRUPTED SEQUENCE. THIS CONTINUES UNTIL THE END OF THE PROGRAM LOOP IS REACHED.

5.2.5 TRAPCATCHER

THIS IS A SERIES OF INSTRUCTIONS STARTING AT LOCATION 0 DESIGNED TO DETECT AND ISOLATE UNEXPECTED TRAPS AND INTERRUPTS TO THE TRAP AND INTERRUPT VECTOR AREA OF MEMORY.

EACH VECTOR ENTRANCE ADDRESS IS LOADED WITH THE ADDRESS OF THE NEXT LOCATION. THE NEXT LOCATION IS LOADED WITH A HALT (000000). THUS AN ILLEGAL TRAP OR INTERRUPT WILL CAUSE A HALT AT THE TRAP LOCATION PLUS TWO.

IF A HALT OCCURS IN THE TRAP OR INTERRUPT AREA, EXAMINE REGISTER SIX. IT WILL CONTAIN THE CURRENT STACK ADDRESS. THE CONTENTS OF THE CURRENT STACK ADDRESS IS THE VALUE OF THE PROGRAM COUNTER WHEN THE TRAP OR INTERRUPT OCCURRED.

5.2.6 ERCR11 (ERROR FUNCTION TEST)

THIS TEST CHECKS OPERATION OF THE VARIOUS ERROR SENSING FEATURES OF THE G.D.I. OR THE DOCUMENTATION CARD READER. CARD READER OFF-LINE, INPUT HOPPER EMPTY, OUTPUT STACKER FULL, FEED ERROR, MOTION ERROR, STACK FAIL, AND DARK-LIGHT ERROR ARE ALL CHECKED.

5.2.7 TESTX (SINGLE TEST LOOP)

THIS ROUTINE ALLOWS A SINGLE SUBTEST TO BE RUN CONTINUOUSLY FOR SCOPE LOOP PURPOSES. WHILE A SCOPE LOOP SWITCH OPTION EXISTS, IT REQUIRES THAT YOU ARE WITHIN THE TEST IN WHICH YOU WISH TO LOOP. IN SOME CASES (SUCH AS WITH INTERMITTENT FAILURES) THAT'S NOT EASY TO DO. THIS SUBROUTINE ALLOWS YOU TO LOAD THE ADDRESS OF ANY TEST FROM TEST0 THRU TEST24 AND TESTA THRU TESTG AND THEN GO DIRECTLY TO THAT TEST.

5.2.8 CKSAME (SINGLE DATA PATTERN TEST)

THIS TEST IS DESIGNED TO AID IN THE DIAGNOSIS OF DIFFICULT DATA ERROR PROBLEMS AND FACILITATE SOME CARD READER ADJUSTMENTS.

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IT CONTINUOUSLY READS CARDS WHICH HAVE ALL COLUMNS PUNCHED IDENTICALLY (AND ALL CARDS MUST BE IDENTICAL), CHECKING THE DATA AGAINST A PATTERN SET UP ON THE SWITCHES INITIALLY. ANY ERRORS ARE PRINTED OUT, ALONG WITH A COUNT OF THE TOTAL NUMBER OF CARDS READ AND THE TOTAL NUMBER OF DATA ERRORS WHICH HAVE OCCURRED SINCE THE TEST WAS STARTED.

5.3 PROGRAM AND/OR OPERATOR ACTION

5.3.1 LOADING AND STARTING AT 200 WITH ALL SWITCHES DOWN IS WORST CASE TESTING. A SINGLE ALPHANUMERIC DECK SHOULD BE RUN. THIS EXECUTES AN INSTRUCTION TEST FOLLOWED BY A DATA RELIABILITY TEST. AT THE END OF THE DECK CHECKS ARE MADE OF THE FLAG SETTINGS WHICH SHOULD BE AFFECTED, AND THE PROGRAM WAITS FOR AN INTERRUPT FROM THE READER COMING BACK ON-LINE. AT THE END OF THE FIRST DECK THE OPERATOR SHOULD LOAD ONE OR MORE DECKS IN THE INPUT HOPPER AND PRESS MOTOR START AND READ START (RESET ON THE DOCUMENTATION READER). IF THE CARD READER IS WORKING PROPERLY, THE BELL WILL RING ONCE WHEN READ START IS PRESSED AND THE ENTIRE DECK WILL BE RUN THRU THE DATA RELIABILITY PORTION OF THE TEST. IF, AFTER READING 80 CARDS, THE INPUT HOPPER IS NOT EMPTY, THE PROGRAM WILL CONTINUE TO THE NEXT DECK. SWITCH OPTIONS MAY BE USED TO ALTER THIS FLOW AS NOTED IN SECTION 4.1.

5.3.2 TO GO DIRECTLY TO A SINGLE SUBTEST AND RUN IT CONTINUOUSLY, USE SA 240. SEE 4.3.3 FOR DETAILS. THE PROGRAM WILL CONTINUOUSLY LOOP THRU THE DESIRED SUBTEST.

6. ERRORS

6.1 ERROR PRINTOUT

6.1.1 STANDARD PRINTOUT

PRINTOUTS ARE IN A TWO-WORD FORMAT. THE FIRST IS THE PC OF THE DETECTED ERROR. THE SECOND IS THE CONTENTS OF THE PROCESSOR STATUS REGISTER WHEN THE ERROR WAS DETECTED.

6.1.2 DATA ERROR PRINTOUT

THE HEADING IS PRINTED OUT ONCE PER TEST DECK. THE COLUMNS HAVE THE FOLLOWING SIGNIFICANCE:

- DECK -EITHER ALPHANUMERIC OR BINARY, DEPENDING ON SW. SETTING
- CARD -THE CARD NUMBER WHERE THE FAILURE OCCURRED
- COLUMN -THE COLUMN NUMBER WHERE THE FAILURE OCCURRED
- PATTERN -THE CORRECT CARD IMAGE DATA THAT SHOULD HAVE BEEN READ
- READ1 -THE CARD IMAGE DATA IS READ TWICE. THIS IS WHAT WAS READ THE FIRST TIME FROM CR01
- READ2 -THIS IS WHAT WAS IN CR01 AFTER A BRIEF TIMING LOOP. IT SHOULD BE THE SAME AS THE PREVIOUS READING.
- CODED -THIS IS WHAT THE DATA SHOULD BE IN ENCODED FORM
- READ -THIS IS WHAT WAS READ BY ADDRESSING THE ENCODED BUFFER

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DATA ERRORS NOT TRACED TO CARD READER HARDWARE INCLUDE:

- A. SW04 NOT SET TO TYPE OF DECK USED
- B. CARD MISSING
- C. CARD DECK OUT OF PROPER SEQUENCE
- D. DAMAGED CARD

6.1.3 SINGLE DATA PATTERN PRINTOUT

THE SINGLE DATA PATTERN TEST PRINTS OUT A HEADING WITH EACH ERROR PRINTOUT. THE COLUMNS HAVE THE FOLLOWING SIGNIFICANCE:

- COLUMN -THE COLUMN NUMBER WHERE THE FAILURE OCCURRED.
- READ1 -DATA IS READ TWICE. THIS IS THE FIRST READING.
- READ2 -THIS IS WHAT WAS READ THE SECOND TIME.
- CARDS -THE TOTAL NUMBER OF CARDS (IN OCTAL) THAT HAVE BEEN RUN SINCE THE TEST WAS STARTED.
- ERRORS -THE TOTAL NUMBER OF ERRORS DETECTED (IN OCTAL) SINCE THE TEST WAS STARTED.

6.1.4 "BIT 8 WAS SET"

AT THE BEGINNING OF MOST SUBTESTS, BIT 8 (OFF-LINE) IS CHECKED TO MAKE SURE THAT THE READER IS NOT OFF-LINE. IT IS ALSO CHECKED IN THE DATA TEST WHEN AN INTERRUPT OCCURS DUE TO BIT 15 BEING SET. IF BIT 8 IS SET WHEN IT WAS NOT SUPPOSED TO BE, THE ERROR MESSAGE "BIT 8 WAS SET. REMEDY THE ERROR CONDITION AND PRESS 'CONTINUE'." IS PRINTED OUT. THE PROCESSOR THEN HALTS. SINCE THE CARD READER GOES OFF-LINE WHEN A CARD READER FUNCTION ERROR OCCURS (CARD JAM, PICK FAIL, ETC.), THE CARD READER ERROR MUST BE FIXED AND THE READER MUST BE PUT BACK ON-LINE BEFORE THE PROGRAM CAN BE CONTINUED.

6.2 ERROR RECOVERY

IN GENERAL, TEST FAILURES WILL PRINTOUT AN ERROR MESSAGE AND CONTINUE. IF THE "HALT ON ERROR" SWITCH IS SET, HITTING CONTINUE WILL RECOVER. IF THE PROGRAM HANGS UP IN A LOOP, THE ERROR IS LIKELY TO BE A SIGNAL WHICH WAS NEVER RECEIVED. IF A HALT OCCURS IN THE TRAP AND VECTOR AREA THE PROGRAM MUST BE RESTARTED. IF THE PROGRAM HALTS IN THE MAIN FLOW, CONSULT THE LISTING IF NO MESSAGE IS TYPED OUT.

7. RESTRICTIONS

7.1 STARTING PROCEDURE

NONE

7.2 OPERATIONAL RESTRICTIONS

7.2.1 COMBINED INSTRUCTION AND DATA RELIABILITY TEST (SA200)

IF A STANDARD TEST DECK IS NOT BEING USED, SW7 MUST BE SET TO INHIBIT RUNNING THE DATA RELIABILITY PORTION OF THE TEST.

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WHEN USING THE STANDARD TEST DECKS, THEY MUST BE IN PROPER SEQUENCE AND IN GOOD CONDITION. IT IS A GOOD IDEA TO NUMBER THE CARDS IN EACH DECK AS SOON AS THE DECK IS RECEIVED.

IF THE CR11 USES AN M829 MODULE SW10 MUST BE SET IN THE SWITCH REGISTER.

7.2.2 ERROR FUNCTION TEST (SA 204 FOR G.D.I. READER - SA 210 FOR DOCUMENTATION READER)

THE ERROR FUNCTION TEST REQUIRES SPARE CARDS, AS IT BENDS SEVERAL. ALSO, TO RUN THE DARK-LIGHT CHECK 2 CARDS MUST BE SPECIALLY PREPARED. THE TEST WILL TYPE OUT A REQUEST FOR THESE CARDS WHEN THEY ARE NEEDED. TO MAKE THEM:

1. TEAR A SMALL PIECE FROM THE LEADING EDGE OF ONE CARD.
2. TAPE 2 OTHER CARDS TOGETHER TO MAKE ONE "LONG" CARD - IT ONLY NEEDS TO BE ABOUT 1/2 INCH LONGER THAN A REGULAR CARD

7.2.3 SINGLE DATA PATTERN TEST (SA 220)

A SPECIAL DECK (ONE OR MORE CARDS) MUST BE PREPARED. ALL COLUMNS OF ALL CARDS ARE PUNCHED IDENTICALLY, USING A DATA PATTERN WHICH WILL TEST THE PROBLEM BEING DIAGNOSED.

8. MISCELLANEOUS

8.1 EXECUTION TIME

NOT APPLICABLE

8.2 CARD DECK DESCRIPTION

8.2.1 ALPHANUMERIC

REFERENCE THE ALPHANUMERIC TABLE BEGINNING AT THE TAG ALPCD IN THE LISTING FOR THE CODES PUNCHED FOR EACH OF 80 COLUMNS OF THE FIRST CARD. THE FIRST VALUE GIVEN FOR A COLUMN IS THE CARD IMAGE OF THAT COLUMN, WHILE THE SECOND VALUE IS THE ENCODED FORM OF THE SAME PATTERN. EACH SUCCESSIVE CARD IN THE DECK USES THE SAME SEQUENCE OF CODES ROTATED ONE COLUMN TO THE LEFT. THIS PROGRAM WILL SUPPORT CARD DECKS THAT HAVE THE SAME PATTERN ON EACH CARD.

8.2.2 BINARY

REFERENCE THE BINARY DATA TABLE BEGINNING AT THE TAG BINCD IN THE LISTING FOR THE CODES PUNCHED FOR EACH OF THE 80 COLUMNS OF THE 1ST CARD. AS WITH THE ALPHANUMERIC DECK EACH SUCCESSIVE CARD HAS THE SAME SEQUENCE OF CODES ROTATED ONE COLUMN TO THE LEFT. THIS PROGRAM WILL SUPPORT CARD DECKS THAT HAVE THE SAME PATTERN ON EACH CARD.

8.3 SPECIAL NOTES

IF THE CARD READER GOES OFF-LINE BEFORE THE END OF A CARD,

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BUSY REMAINS SET UNTIL THE CARD ACTUALLY CLEARS THE READER.

THE CARD READER GOES OFF-LINE DUE TO "INPUT HOPPER EMPTY" AFTER THE BOTH COLUMN OF THE LAST CARD IS READ, BUT BEFORE CARD DONE OCCURS. THUS, THE SPECIAL CONDITION BIT IN THE CSR WILL BE SET BEFORE CARD DONE ON THE LAST CARD.

IF THE CARD READER USES AN MB29 MODULE, SW10 MUST BE SET IN THE SWITCH REGISTER. WITH THE MB29 MODULE, CARD DONE NEVER OCCURS AFTER THE LAST CARD IN THE INPUT HOPPER IS READ. IF THE CARD READER USES AN MB290 MODULE, SW09 MUST BE SET. WITH THE MB290 MODULE, CARD DONE IS ISSUED AFTER THE LAST CARD IN THE INPUT HOPPER IS READ.

IF BIT 0 OF THE CRS IS CLEARED IMMEDIATELY AFTER BEING SET, THE READING OF A CARD MAY NOT OCCUR. SINCE THIS BIT IS WRITE ONLY, A BIS OR BIC DONE AFTER SETTING BIT 0 MAY CLEAR THE BIT AND PREVENT THE READ FROM OCCURRING.

#### 8.4 TESTING CR11/CH11'S WITH NON-STANDARD ADDRESSES

BY SUBSTITUTING INTO THE LOCATIONS KCRS, KCRB1, KCRB2, AND KCRM THE ADDRESSES OF THE CRS, CRB1, AND CRB2 OF A CARD READER ASSIGNED A NON-STANDARD ADDRESS, AND SUBSTITUTING ITS INTERRUPT VECTOR ADDRESS INTO INTVC & INPRI, A CR11 MAY BE TESTED AT ANY ADDRESS ASSIGNED TO IT.

#### 9. PROGRAM DESCRIPTION

THIS SET OF TESTS IS DESIGNED TO CHECK ALL OPERATIONS OF THE CR11 CARD READER, WITH THE NECESSARY EXCEPTION THAT TIMING IN MOST CASES IS ONLY PARTIALLY TESTED. A SPECIAL TEST IS INCLUDED TO CHECK OUT THE ERROR FUNCTIONS OF THE G.D.I. 100 READER, WHICH PRINTS OUT DIRECTIONS AS IT GOES ALONG. A TEST IS ALSO INCLUDED TO ISOLATE DIFFICULT DATA ERRORS USING A SPECIAL TEST DECK FUNCHED BY THE USER.

#### 10. MAINTENANCE TEST

1. THE MB291 CR11 CONTROL MODULE (MB291) HAS BEEN ADDED TO THE CR11 CONTROL BOARDS. THIS MODULE (MB291) HAS AN ADDITIONAL REGISTER (THE MAINTENANCE REG.). THE FIRST TWENTY TWO TEST (TSTND1-22) ADDED TO THE CR11 DIAGNOSTIC HAVE BEEN DESIGNED TO CHECK OUT THE NEW REGISTER ON A BIT RESPONSE & TO EXERCISE THE WHOLE CR11/CH11F CONTROL BOARD (MB291).

THIS ADDITIONAL CODE WILL RUN ON AN AUTOMATIC COMPUTER TESTING (ACT-11) SYSTEM, BUT ONLY THE MAINTENANCE PORTION.

THE SELECTION FOR TESTING OF THE MB291 STAND ALONE

DIAGNOSTIC IS SW09 & SW10 = ZERO 0.

THE M8291 MAINTENANCE REGISTER IS A WRITE ONLY REGISTER, THEREFORE CREATING DIFFICULT TESTING CODE.

2. MAINTENANCE SUB TITLES OF EACH ROUTINES

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- TSTM01: SCOPE  
THIS TEST MAINTENANCE REGISTERS ADDRESS
- TSTM02: SCOPE  
THIS TEST WILL CHECK OUT THE CSR INTERRUPT ENABLE BIT SETTING & CLEARING OF THAT BIT.  
AT THE TIME OF TEST IT WILL PROTECT AGAINST FALSE INTR.
- TSTM03: SCOPE  
THIS TEST WILL CHECK THE EJECT BIT IN THE CSR  
THIS IS REQUIRE FOR TIMING ERROR, COLUMN READY TO TEST IN THE MAINT MODE & NORMAL MODE
- TSTM04: SCOPE  
THIS PROGRAM WILL VERIFY BIT 13 OF THE CR11 MAINTENANCE REGISTER MAINT 3 TEST AND MAINT 4 TEST WILL INDICATE TRUE FAULT
- TSTM05: SCOPE  
THIS TEST WILL BIT BANG BIT 14 IN CR11 MAINTENANCE REGISTER
- TSTM06: SCOPE  
THIS TEST WILL BIT BANG BIT 13 IN THE CR11 MAINT. REG.  
ON LINE TRANSITION
- TSTM07: SCOPE  
THIS TEST WILL EXERCISE (BIT BANG) BIT 12 MOT/HOP IN THE CR11 MAINTENANCE REGISTER.
- TSTM08: SCOPE  
THIS TEST WILL PASS DATA PATTERNS THRU ZONE BIT(S) OF THE MAINTENANCE REGISTER & CHECK COMPARE WITH CRB1 REG.
- TSTM09: SCOPE  
THIS TEST WILL CHECKOUT DATA PATHS FROM THE MAINTENANCE BUFFER REGISTER THRU TO CRB2 (COMPRESSED CODE)
- TSTM10: SCOPE  
TEST WILL CHECK THE SETTING & CLEARING OF TRANSITION ON LINE BIT IN THE CSR.  
THIS TEST IS REQ'S BEFORE WE CAN PROCED & CHECK SOME OF THE MAINT. FUNCTIONS
- TSTM11: SCOPE  
THIS TEST WILL CHECK THE MAINT. FUNCTION CAUSE AN OFF-LINE & ERROR CONDITION
- TSTM12: SCOPE  
THIS TEST WILL SET CONDITIONS TO SET CARD DONE BIT THRU THE MAINT. REG. FOR TEST.
- TSTM13: SCOPE  
COLUMN READY TEST THRU MAINT. REG., SETTING READY, 0 BUSY WILL GIVE AN INDEX MARK WHICH SET COLUMN READY.
- TSTM14: SCOPE  
TEST WILL CHECK OUT CONDITIONS THAT SET TIMING ERROR BIT
- TSTM15: SCOPE  
TEST ON LINE FUNCTION TO CREATE AN INTERRUPT

# MO1

DZCRB-C CR11/CN11F DIAGNOSTIC TEST  
DZCRB.SRC

MACY11 27(732) 02-NOV-76 15:51 PAGE 13

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TSTM16: SCOPE  
TEST OF LINE FUNCTION TO INTERRUPT

TSTM17: SCOPE  
TEST CARD DONE FUNCTION TO CAUSE AN INTERRUPT

TSTM18: SCOPE  
TEST COLUMN READY FUNCTION TO CAUSE AN INTERRUPT

TSTM19: SCOPE  
THIS TEST WILL CAUSE A TIMING ERROR WHICH SHOULD  
CREATE AN INTERRUPT. A CHECK FOR THE RIGHT  
INTERRUPT FUNCTIONS WILL BE MADE.

TSTM20: SCOPE  
SET ALL CONTROL BITS IN CR11'S CONTROL & STATUS  
REGISTER PERFORM A RESET COMMAND VERIFY  
THAT RESET DID CLEAR FUNCTION IN CSR.

TSTM21: SCOPE  
THIS TEST WILL LOOK FOR INTERACTION BETWEEN  
MOTION CHECK BIT 12 & HOPPER CHECK BIT 13

TSTM22: SCOPE  
THIS TEST WILL PASS SIMULATED DATA OF AN  
ALPHANUMERIC CARD DECK & ALSO A BINARY CARD  
DECK IN THE INTERRUPT MODE

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DIAGNOSTIC FOR CR11 CARD READER  
BY RICK FADDEN  
(MODIFIED MAY 75 TO ACCOMIDATE THE M8291 MODULE (AL. COSSETTE))  
(MODIFIED APRIL-72 FOR HARDWARE ECO)  
MODIFIED APRIL 1976 FOR SWITCH REGISTER-LESS PROCESSORS  
BY RON PLATUKIS

STARTING ADDRESSES ARE.  
200=INSTRUCTION AND DATA TEST FOR THE CR11  
204=ERROR FUNCTION TEST OF CR11 (GDI)  
210=ERROR FUNCTION TEST OF CR11/CM11F USING DOCUMENTATION READER.  
214=SINGLE TEST LOOP  
220=READ SINGLE DATA PATTERN TEST

SWITCH REGISTER SETTINGS FOR THE INSTRUCTION AND DATA TEST ARE:  
SW00=1 FOR DISABLE OF TEST TESTG(DARK-LIGHT TEST)  
SW03=1 RUN MARK SENSE BINARY TEST DECK M-00-DZCMB-A-CO  
SW04=0 & SW02=1 RUN ALPH TEST DECK M-11-DZCMA-A-CA(FIX PAT)  
SW04=1 & SW02=1 RUN BINARY TEST DECK M-11-DZCMA-A-CB(FIX PAT)  
SW04=0 & SW02=0 RUN ALPHA TEST DECK M-00-DZCRA-A-CA(ROT PAT)  
SW04=1 & SW02=0 RUN BINARY TEST DECK M-00-DZCRA-A-CB(ROT PAT)  
SW05=1 TO HALT AT THE END OF A STANDARD 80 CARD  
TEST DECK.  
=0 TO CONTINUE FROM ONE DECK TO THE NEXT.  
AFTER THE LAST DECK IN THE HOPPER IS  
RUN, THE PROGRAM WAITS FOR THE CARD READER  
TO COME BACK ON-LINE AND RUNS THRU  
A SERIES OF CHECKS OF OFF-LINE AND  
COMING ON-LINE OPERATIONS OF THE READER.  
WHEN THE READER IS BACK ON-LINE AND THE  
CHECKS ARE COMPLETE, THE DATA TEST IS RESUMED.  
SW06=1 TO RUN THE COMBINED INSTRUCTION AND DATA TEST  
WHEN CONTINUING FROM ONE DECK TO THE NEXT  
=0 TO RUN ONLY THE DATA TEST ON EVERY DECK AFTER THE FIRST  
SW07=1 TO RUN ONLY THE INSTRUCTION TEST CONTINUALLY  
SETTING SW06 AND SW07 AT THE END OF A DECK WILL  
CAUSE THE INSTRUCTION TEST TO BE RUN CONTINUOUSLY FROM THEN ON  
NOTE: IF SW7 IS SET, CHECKED BY PROGRAM, AND THEN  
CLEARED, THE DATA TEST WILL BE INCORRECT. THIS IS  
TRUE BECAUSE THE FIRST CARD IN THE DATA TEST WILL NOT  
BE THE ONE EXPECTED. WITH SW7 SET THE TEST MAY HANG  
WHEN THE INPUT HOPPER RUNS OUT OF CARDS.  
SW08=1 OR UP---LOOP ON THE MAINTENANCE TEST PORTION OF  
THIS DIAGNOSTIC (MUST BE M8291 CONTROL  
MODULE FOR CR11/CM11F).  
SW09=1 CR11/CM11 UNDER TEST IS NOT MODULE M8290.  
SW10=1 TO INDICATE THAT THE CR11 BEING TESTED USES THE  
M829 MODULE  
SW10 & SW09 BOTH = ZERO TO INDICATE THAT THE CR11/CM11 BEING TESTED USES  
M8291 MODULE  
SW11=1 TO INHIBIT SUBPROGRAM ITERATION  
(NOTE THAT IF PROGRAM FLOW IS ALLOWED TO ENTER THE



730	000054	000056	.+2
731	000056	000060	HALT
732	000060	000062	.+2
733	000062	000000	HALT
734	000064	000066	.+2
735	000066	000000	HALT
736	000070	000072	.+2
737	000072	000000	HALT
738	000074	000076	.+2
739	000076	000000	HALT
740	000100	000102	.+2
741	000102	000000	HALT
742	000104	000106	.+2
743	000106	000000	HALT
744	000110	000112	.+2
745	000112	000000	HALT
746	000114	000116	.+2
747	000116	000000	HALT
748	000120	000122	.+2
749	000122	000000	HALT
750	000124	000126	.+2
751	000126	000000	HALT
752	000130	000132	.+2
753	000132	000000	HALT
754	000134	000136	.+2
755	000136	000000	HALT
756	000140	000142	.+2
757	000142	000000	HALT
758	000144	000146	.+2
759	000146	000000	HALT
760	000150	000152	.+2
761	000152	000000	HALT
762	000154	000156	.+2
763	000156	000000	HALT
764	000160	000162	.+2
765	000162	000000	HALT
766	000164	000166	.+2
767	000166	000000	HALT
768	000170	000172	.+2
769	000172	000000	HALT
770	000174	000176	.+2
771	000176	000000	HALT
772	000200	000202	.+2
773	000202	000000	HALT
774	000204	000206	.+2
775	000206	000000	HALT
776	000210	000212	.+2
777	000212	000000	HALT
778	000214	000216	.+2
779	000216	000000	HALT
780	000220	000222	.+2
781	000222	000000	HALT
782	000224	000226	.+2
783	000226	000000	HALT
784	000230	000232	.+2
785	000232	000000	HALT









```

1010 001142 000000
1011 001144 000000
1012 001146 000002
1013 001150 000000
1014 001152 000000
1015
1016 001154 000000
1017
1018
1019
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1021
1022 001156 012706 001100
1023 001162 004767 000064
1024 001166 000167 003732
1025
1026 001172 012706 001100
1027 001176 004767 000050
1028 001202 000167 012234
1029
1030 001206 012706 001100
1031 001212 004767 000034
1032 001216 000167 012226
1033
1034 001222 012706 001100
1035 001226 004767 000020
1036 001232 000167 013704
1037
1038 001236 012706 001100
1039 001242 004767 000004
1040 001246 000167 014010
1041
1042
1043
1044 001252 104007
1045 001254 013746 000004
1046 001260 012737 001300 000004
1047 001266 005777 177616
1048 001272 012637 000004
1049 001276 000405
1050 001300 022626
1051 001302 012637 000004
1052 001306 104000
1053 001310 000760
1054 001312 013746 000004
1055 001316 012737 001336 000004
1056 001324 005777 177562
1057 001330 012637 000004
1058 001334 000405
1059 001336 022626
1060 001340 012637 000004
1061 001344 104000
1062 001346 000761
1063 001350 013746 000004
1064 001354 012737 001374 000004
1065 001362 005777 177526

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```

TIB: 0
FLAG: 0 ;SET TO ONE FOR MARK-SENSE CARD READER
TRTRAP: RTI ;RETURN FROM TRACE LOOP
TRFLG: 0 ;TOGGLED TO SWITCH BETWEEN TRACE TRAPPING AND NORMAL FLO
PROC: 0 ;STORES PROCESSOR STATUS WHEN TRACE TRAP MUST BE CLEARED
ERFLG: 0 ;IN A SUBTEST
;SET TO ZERO TO OUTPUT DATA ERROR HEADING

```

```

;THIS ROUTINE WILL CHECK FOR THE PRESENCE OF THE NEW CR11
;MODULE M8291 BOARD

```

```

START1: MOV #STACK, SP ;SET STACK POINTER
        JSR PC, BOARD
        JMP BEGIN ;INSTRUCTION AND DATA TEST

START2: MOV #STACK, SP ;SET STACK POINTER
        JSR PC, BOARD
        JMP ERCR11 ;ERROR FUNCTION TEST (G.D.I. READER)

START3: MOV #STACK, SP ;SET STACK POINTER
        JSR PC, BOARD
        JMP ERCH11 ;ERROR FUNCTIO TEST (DUCUMATIOON READER)

START4: MOV #STACK, SP ;SET STACK POINTER
        JSR PC, BOARD
        JMP TESTX ;SINGLE SUB TEST LOOP

START5: MOV #STACK, SP ;SET STACK POINTER
        JSR PC, BOARD
        JMP CKSAME ;READ SINGLE PATTERN TEST

```

```

;TEST CR11 REGISTERS RESPOND TO ADDRESS REQUEST

```

```

BOARD: TIT
        MOV #4, -(SP) ;SAVE RETURN INFO
        MOV #25, #4 ;RESET RETURN CALL
        TST #KCRB1 ;TEST ADDRESS
        MOV (SP)+, #4 ;ADDRESS GOOD RESTORE RETURN ADDR.
        BR 3S ;CONT. TEST

2S: CMP (SP)+, (SP)+ ;UPDATE STACK
     MOV (SP)+, #4 ;UPDATE TRAP RETURN ADDR.
     HLT ;ERROR IN ADDRESSING THIS REGISTER
     BR BOARD ;CONT. ERROR REPORT

3S: MOV #4, -(SP) ;SAVE RETURN INFO
     MOV #45, #4 ;RESET RETURN CALL
     TST #KCRB1 ;TEST ADDRESS
     MOV (SP)+, #4 ;ADDRESS GOOD RESTORE RETURN ADDR.
     BR 5S ;CONT. TEST

4S: CMP (SP)+, (SP)+ ;UPDATE STACK
     MOV (SP)+, #4 ;UPDATE TRAP RETURN ADDR.
     HLT ;ERROR IN ADDRESSING THIS REGISTER
     BR 3S ;CONT. ERROR REPORT

5S: MOV #4, -(SP) ;SAVE RETURN INFO
     MOV #65, #4 ;RESET RETURN CALL
     TST #KCRB2 ;TEST ADDRESS

```

1066	001366	012637	000004		MOV	(SP)+,2#4	: ADDRESS GOOD RESTORE RETURN ADDR.
1067	001372	000405			BR	MBRD	: CONT. TEST
1068	001374	022626		6S:	CMP	(SP)+, (SP)+	: UPDATE STACK
1069	001376	012637	000004		MOV	(SP)+,2#4	: UPDATE TRAP RETURN ADDR.
1070	001402	104000			HLT		: ERROR IN ADDRESSING THIS REGISTER
1071	001404	000761			BR	5S	: CONT. ERROR REPORT
1072							
1073	001406	104005			MBRD:	SUSWRR	
1074	001410	104002				CNTLU	
1075	001412	104006				CKU	
1076	001414	032777	002000	177500		BIT	#2000,2SWR
1077	001422	001401				BEQ	4S
1078	001424	000207				RTS	PC
1079	001426	032777	001000	177466	4S:	BIT	#1000,2SWR
1080	001434	001401				BEQ	1S
1081	001436	000207				RTS	PC
1082	001440	012767	177777	003410	1S:	MOV	#-1,MFLG
1083	001446	005767	003404		2S:	TST	MFLG
1084	001452	001001				BNE	3S
1085	001454	000207				RTS	PC
1086	001456	012767	001472	014740	3S:	MOV	#TSTM1A,RETURN
1087	001464	004767	003372			JSR	PC,SETUP
1088							



```

1145
1146 001676 104001
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1149
1150 001700 004767 003130 JSR PC,MINIT ;INIT. MAINT. TEST
1151 001704 052777 110000 177204 BIS #110000,AKCRM ;SET MAINT & MOT/HOP(BIT 12)
1152 001712 032777 020000 177170 BIT #20000,AKCRS ;TEST BIT 13 IN CSR REG.
1153 001720 001001 BNE 25 ;TEST GOOD BRANCH
1154 001722 104000 HLT ;INDICATE ERROR
1155 001724 012777 000000 177156 2S: MOV #0,AKCRS ;CLEAR CONTROL STATUS
1156 001732 012777 100000 177156 MOV #100000,AKCRM ;CLEAR MAINTENANCE REG.
1157 001740 032777 020000 177142 BIT #20000,AKCRS ;DID BIT 13 CLEAR
1158 001746 001401 BEQ 3S ;YES BRANCH & DO ANOTHER TEST CYCLE
1159 001750 104000 HLT ;INDICATE ERROR
1160 001752 005077 177140 3S: CLR AKCRM ;CLEAR MAINT. REG.
1161
1162
1163 001756 104001
1164
1165
1166 001760 004767 003050 JSR PC,MINIT ;INIT. MAINT. TEST
1167 001764 052777 140000 177124 BIS #140000,AKCRM ;SET MAINT. MODE & BUSY BIT (MAINT.)
1168 001772 032777 001000 177110 BIT #1000,AKCRS ;DID BUSY MAINT. BIT SET BUSY CSR BIT
1169 002000 001001 BNE 25 ;TEST GOOD CONTINUE.
1170 002002 104000 HLT ;ERROR CONDITION
1171 002004 012777 000000 177076 2S: MOV #0,AKCRS ;CLEAR BUSY BIT (CSR)
1172 002012 012777 100000 177076 MOV #100000,AKCRM ;CLEAR MAINT. REG.
1173 002020 032777 001000 177062 BIT #1000,AKCRS ;DID WE CLEAR BIT 09
1174 002026 001401 BEQ 3S ;BIT 09 DID CLEAR
1175 002030 104000 HLT ;ERROR
1176 002032 052777 140000 177056 3S: BIS #140000,AKCRM ;SET MAINT. MODE & BUSY BIT (MAINT.)
1177 002040 032777 001000 177042 BIT #1000,AKCRS ;DID BUSY MAINT. BIT SET BUSY CSR BIT
1178 002046 001001 BNE 4S ;TEST GOOD CONTINUE.
1179 002050 104000 HLT ;ERROR CONDITION
1180 002052 000005 4S: RESET ;INIT.
1181 002054 032777 001000 177026 BIT #1000,AKCRS ;TEST BUSY BIT
1182 002062 001401 BEQ 5S ;BUSY = 0, YES BRANCH
1183 002064 104000 HLT ;NO, ERROR
1184 002066 005077 177024 5S: CLR AKCRM ;CLEAR MAINT. REG.
1185
1186 002072 104001
1187
1188
1189
1190
1191 002074 004767 002734 JSR PC,MINIT ;INIT. MAINT. TEST
1192 002100 052777 120000 177010 BIS #120000,AKCRM ;SET MAINT. AND READY BIT
1193 002106 032777 002000 176774 BIT #2000,AKCRS ;TEST TRANSITION ON LINE
1194 002114 001001 BNE 25 ;TEST GOOD BRANCH
1195 002116 104000 HLT ;ERROR CONDITION
1196 002120 012777 000000 176762 2S: MOV #0,AKCRS ;CLEAR STATUS REG.
1197 002126 012777 100000 176762 MOV #100000,AKCRM ;CLEAR MAINT. REG.
1198 002134 032777 002000 176746 BIT #2000,AKCRS ;DID WE CLEAR BIT 10
1199 002142 001401 BEQ 3S ;BRANCH IF CLEAR
1200 002144 104000 HLT ;ERROR DID NOT CLEAR BIT 10

```

TSTM04: SCOPE  
;THIS PROGRAM WILL VERIFY BIT 12(MOT/HOP) OF THE CR11 MAINTENANCE REGISTER.

TSTM05: SCOPE  
;THIS TEST WILL BIT BANG BIT 14(BUSY) IN CR11 MAINTENANCE REGISTER

TSTM06: SCOPE  
;THIS TEST WILL BIT BANG BIT 13 IN THE CR11 MAINT. REG.  
;ON LINE TRANSITION

```

1201 002146 005077 176744      3S:   CLR      2KCRM      ;CLEAR MAINT. REG.
1202
1203 002152 104001
1204
1205
1206
1207 002154 004767 002654      JSR      PC,MINIT      ;INIT. MAINT. TEST
1208 002160 052777 110000 176730  BIS      2(110000),2KCRM ;SET MAINT & MOT/HOP(BIT 12)
1209 002166 032777 010000 176714  BIT      2(10000),2KCRS ;TEST BIT 12
1210 002174 001001
1211 002176 104000
1212 002200 012777 000000 176702 2S:   MOV      2(0),2KCRS    ;CLEAR CONTROL STATUS
1213 002206 012777 100000 176702  MOV      2(100000),2KCRM ;CLEAR MAINT. REG.
1214 002214 032777 010000 176666  BIT      2(10000),2KCRS ;DID BIT 12 CLEAR
1215 002222 001401
1216 002224 104000
1217 002226 005077 176664      3S:   CLR      2KCRM      ;CLEAR MAINT. REG.
1218
1219 002232 104001
1220
1221
1222
1223
1224 002234 004767 002574      JSR      PC,MINIT      ;INIT. MAINT. TEST
1225 002240 012702 017300      MOV      2(8ALPCD),R2    ;GET BUF STARTING ADDRESS
1226 002244 012705 017776      MOV      2(8ALPEND),R5  ;GET BUF ENDING ADDRESS
1227 002250 162705 000002      SUB      2(2),R5        ;UPDATE R5
1228 002254 012767 160000 002576 2S:   MOV      2(160000),TSTM  ;SET MAINT. CMD. FUNC.
1229 002262 051267 002572      BIS      2(R2),TSTM     ;GET DATA TO PASS
1230 002266 016777 002566 176622  MOV      2(TSTM),2KCRM  ;PASS WORD TO MAINT REG
1231 002274 022277 176612      CMP      2(R2)+,2KCRB1  ;CHECK DATA WORD
1232 002300 001401
1233 002302 104000
1234 002304 005722      3S:   TST      2(R2)+    ;GOOD WORD
1235 002306 020205      CMP      2(R2),R5      ;BAD WORD. ERROR
1236 002310 001361
1237 002312 005077 176600      BNE     2(2)          ;UPDATE REG. #2
1238
1239
1240 002316 104001
1241
1242
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1244
1245 002320 004767 002510      JSR      PC,MINIT      ;INIT. MAINT. TEST
1246 002324 012702 017300      MOV      2(8ALPCD),R2    ;GET BUF STARTING ADDRESS
1247 002330 012705 017776      MOV      2(8ALPEND),R5  ;GET BUF ENDING ADDRESS
1248 002334 062705 000002      ADD     2(2),R5        ;UPDATE R5
1249 002340 012767 160000 002512 2S:   MOV      2(160000),TSTM  ;GET DATA TO PASS
1250 002346 052267 002506      BIS      2(R2)+,TSTM    ;SET MAINT. FUNCTION
1251 002352 016777 002502 176536  MOV      2(TSTM),2KCRM  ;PASS WORD TO MAINT REG
1252 002360 022277 176530      CMP      2(R2)+,2KCRB2  ;CHECK DATA WORD COMPRESSED DATA
1253 002364 001401
1254 002366 104000
1255 002370 020205      3S:   CMP      2(R2),R5    ;GOOD WORD
1256 002372 001362      BNE     2(2)          ;BAD WORD. ERROR
                        ;PATTERN DONE
                        ;BRANCH IF NOT

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1257 002374 005077 176516          CLR      2KCRM          ;CLEAR MAINT. REG.
1258
1259 002400 104001          TSTM10: SCOPE
1260          ;TEST WILL CHECK THE SETTING & CLEARING OF
1261          ;TRANSITION TO ON LINE BIT IN THE CSR.
1262          ;THIS TEST IS REQ'D BEFORE WE CAN PROCEED & CHECK
1263          ;SOME OF THE MAINT. FUNCTIONS
1264
1265 002402 004767 002426          JSR      PC,MINIT      ;SET MAINT. CONDITION
1266 002406 012777 100000 176502      MOV      #100000,2KCRM ;CLR READY MAINT. REG.
1267 002414 052777 120000 176474      BIS      #120000,2KCRM ;SET READY MAINT. REG.
1268 002422 000240          NOP                      ;TEMP PAUSE
1269 002424 032777 002000 176456      BIT      #2000,2KCRS   ;TEST ON LINE TRANSITION BIT ON
1270 002432 001001          BNE     1$              ;TRANSITION ON LINE BIT TEST GOOD
1271 002434 104000          HLT                      ;TRANSITION ON LINE BIT TEST BAD
1272 002436 012777 000000 176444 1$:  MOV      #0,2KCRS      ;CLEAR ON LINE TRANSITION BIT
1273 002444 032777 002000 176436      BIT      #2000,2KCRS   ;TEST ON LINE TRANSITION BIT OFF
1274 002452 001401          BEQ     2$              ;GOOD TEST PROCEED TO NEXT ONE
1275 002454 104000          HLT                      ;ON LINE TRANSITION BIT DID NOT CLEAR
1276 002456 005077 176434 2$:  CLR      2KCRM          ;CLEAR MAINT.
1277
1278 002462 104001          TSTM11: SCOPE
1279          ;THIS TEST WILL CHECK THAT THE MAINT. FUNCTION CAUSES
1280          ;AN OFF-LINE & ERROR CONDITION
1281
1282 002464 004767 002344          JSR      PC,MINIT      ;SET UP MAINT. CONDITION
1283 002470 052777 120000 176420      BIS      #120000,2KCRM ;SET READY MAINT. BIT
1284 002476 012777 100000 176412      MOV      #100000,2KCRM ;CLR READY MAINT. REG.
1285 002504 000240          NOP                      ;TIME PAUSE
1286 002506 032777 100000 176374      BIT      #100000,2KCRS ;TEST FOR ERROR BIT
1287 002514 001001          BNE     1$              ;BRANCH IF BIT IS SET
1288 002516 104000          HLT                      ;ERROR & OFFLINE BIT SHOULD BE ON
1289 002520 032777 000400 176362 1$:  BIT      #400,2KCRS    ;OFF LINE BIT SHOULD BE ON
1290 002526 001001          BNE     2$              ;GOOD TEST
1291 002530 104000          HLT                      ;ERROR OFF LINE BIT ABSENT
1292 002532 012777 000000 176350 2$:  MOV      #0,2KCRS      ;CLEAR CR11'S CONTROL REG.
1293 002540 032777 100000 176342      BIT      #100000,2KCRS ;ERROR BITS OFF
1294 002546 001401          BEQ     3$              ;BITS CLEAR GO TO NEXT TEST
1295 002550 104000          HLT                      ;ERROR ON ERROR & OFF LINE BIT
1296 002552 032777 000400 176330 3$:  BIT      #400,2KCRS    ;OFFLINE SHOULD BE SET
1297 002560 001001          BNE     4$              ;YES, BRANCH
1298 002562 104000          HLT                      ;NO ERROR
1299 002564 005077 176326 4$:  CLR      2KCRM          ;CLEAR MAINT.
1300
1301 002570 104001          TSTM12: SCOPE
1302          ;THIS TEST WILL SET CONDITIONS TO SET CARD DONE BIT
1303          ;THRU THE MAINT. REG. FOR TEST.
1304
1305 002572 004767 002236          JSR      PC,MINIT      ;GO SET UP MAINT. CONDITION
1306 002576 052777 160000 176312      BIS      #160000,2KCRM ;SET BUSY & READY BIT
1307 002604 000240          NOP                      ;TIME PAUSE
1308 002606 012777 100000 176302      MOV      #100000,2KCRM ;CLR READY MAINT. REG.
1309 002614 000240          NOP                      ;TIME PAUSE
1310 002616 032777 040000 176264      BIT      #40000,2KCRS  ;TEST CARD DONE BIT
1311 002624 001001          BNE     1$              ;BRANCH IF CARD DONE SET
1312 002626 104000          HLT                      ;ERROR CARD DONE BIT NOT SET

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1313	002630	012777	000000	176252	1S:	MOV	#0,AKCRS	:CLEAR CONTROL REG.
1314	002636	032777	040000	176244		BIT	#40000,AKCRS	:TEST IF CARD DONE BIT CLEARED
1315	002644	001401				BEQ	2S	:YES BRANCH TO NEXT TEST
1316	002646	104000				HLT		:ERROR CARD DONE DIDN'T CLEAR.
1317	002650	005077	176242		2S:	CLR	AKCRM	:CLEAR MAINT.
1318								
1319	002654	104001						
1320								
1321								
1322								
1323	002656	004767	002152			JSR	PC,MINIT	:SET UP MAINT. CONDITION
1324	002662	052777	160000	176226		BIS	#160000,AKCRM	:SET BUSY & READY MAINT BIT
1325	002670	032777	000200	176212		BIT	#200,AKCRS	:TEST COLUMN READY BIT SET
1326	002676	001001				BNE	1S	:COLUMN READY DID SET BRANCH
1327	002700	104000				HLT		:ERROR COLUMN READY DID NOT SET
1328	002702	017767	176204	002150	1S:	MOV	AKCRB1,TSTM	:READ BUF #1
1329	002710	032777	000200	176172		BIT	#200,AKCRS	:TEST COLUMN READY BIT CLEARED
1330	002716	001401				BEQ	2S	:COLUMN READY WAS CLEARED
1331	002720	104000				HLT		:COLUMN READY SHOULD HAVE CLEARED
1332	002722	052777	160000	176166	2S:	BIS	#160000,AKCRM	:SET BUSY & READY MAINT BITS
1333	002730	032777	000200	176152		BIT	#200,AKCRS	:TEST COLUMN READY SET
1334	002736	001001				BNE	3S	:COLUMN READY DID SET
1335	002740	104000				HLT		:COLUMN READY DIDN'T SET
1336	002742	017767	176146	002110	3S:	MOV	AKCRB2,TSTM	:READY BUF #2
1337	002750	032777	000200	176132		BIT	#200,AKCRS	:TEST COLUMN READY BIT CLEAR
1338	002756	001401				BEQ	4S	:COLUMN READY DID CLR BRANCH
1339	002760	104000				HLT		:ERROR ON COLUMN READ BIT
1340	002762	052777	160000	176126	4S:	BIS	#160000,AKCRM	:SET BUSY & READY MAINT BIT
1341	002770	032777	000200	176112		BIT	#200,AKCRS	:COLUMN READY
1342	002776	001001				BNE	5S	:COLUMN READY DID SET BRANCH
1343	003000	104000				HLT		:ERROR COLUMN READY DID NOT SET
1344	003002	000005			5S:	RESET		:INIT.
1345	003004	032777	000200	176076		BIT	#200,AKCRS	:COL. READY SHOULD = ZERO
1346	003012	001401				BEQ	6S	:YES, BRANCH
1347	003014	104000				HLT		:NO, ERROR
1348	003016	005077	176074		6S:	CLR	AKCRM	:CLEAR MAINT.
1349								
1350	003022	104001						
1351								
1352								
1353								
1354	003024	004767	002004			JSR	PC,MINIT	:SET UP MAINT. CONDITION
1355	003030	052777	160000	176060		BIS	#160000,AKCRM	:MAINT. SET BUSY, READY & INDEX MARK
1356	003036	032777	000200	176044		BIT	#200,AKCRS	:TEST FOR COLUMN READY
1357	003044	001001				BNE	1S	:COLUMN RDY SET BRANCH
1358	003046	104000				HLT		:ERROR ON COLUMN READY
1359	003050	032777	004000	176032	1S:	BIT	#4000,AKCRS	:TEST TIMING ERROR (T.E.)
1360	003056	001401				BEQ	2S	:T.E. SHOULD BE CLEARED
1361	003060	104000				HLT		:T.E. IS SET & SHOULDN'T BE
1362	003062	052777	160000	176026	2S:	BIS	#160000,AKCRM	:SECOND INDEX MARK
1363	003070	032777	000200	176012		BIT	#200,AKCRS	:IS COLUMN READY SET
1364	003076	001401				BEQ	3S	:COLUMN READY SHOULD NOT BE SET
1365	003100	104000				HLT		:WASN'T SET ERROR
1366	003102	032777	004000	176000	3S:	BIT	#4000,AKCRS	:TEST TIMING ERROR
1367	003110	001001				BNE	4S	:TIMING ERROR SHOULD BE SET
1368	003112	104000				HLT		:TIMING WASN'T SET

TSTM13: SCOPE  
:COLUMN READY TEST THRU MAINT. REG., SETTING READY 0  
:BUSY WILL GIVE AN INDEX MARK WHICH SETS COLUMN READY.

TSTM14: SCOPE  
:TEST WILL CHECK OUT CONDITIONS THAT SET TIMING ERROR  
:BIT

1369	003114	052777	160000	175774	4S:	BIS	#160000,2KCRM	:THIRD INDEX MARK
1370	003122	032777	000200	175760		BIT	#200,2KCRS	:TEST COLUMN READY
1371	003130	001401				BEQ	5S	:COLUMN READY NOT SET BRANCH
1372	003132	104000				HLT		:COLUMN READY SHOULD BE OFF
1373	003134	032777	004000	175746	5S:	BIT	#4000,2KCRS	:TEST TIMING ERROR
1374	003142	001001				BNE	6S	:BRANCH IF T.E. SET
1375	003144	104000				HLT		:T.E. SHOULD NOT BE ZERO
1376	003146	052777	000002	175734	6S:	BIS	#2,2KCRS	:SET EJECT BIT
1377	003154	052777	160000	175734		BIS	#160000,2KCRM	:FOURTH INDEX MARK.
1378	003162	032777	000200	175720		BIT	#200,2KCRS	:COLUMN READY SET?
1379	003170	001401				BEQ	7S	:COLUMN READY NOT SET
1380	003172	104000				HLT		:COLUMN READY IS NOT CLEAR ERROR
1381	003174	032777	004000	175706	7S:	BIT	#4000,2KCRS	:TEST TIMING ERROR
1382	003202	001401				BEQ	8S	:TIMING ERROR SET BRANCH
1383	003204	104000				HLT		:TIMING ERROR CLEARED ERROR
1384	003206	012777	100000	175702	8S:	MOV	#100000,2KCRM	:CLR READY MAINT. REG.
1385	003214	032777	100000	175666		BIT	#100000,2KCRS	:TIMING ERROR SET?
1386	003222	001001				BNE	91S	:TIMING ERROR IN ERROR ?
1387	003224	104000				HLT		:TIMING ERROR IN ERROR
1388	003226	032777	040000	175654	81S:	BIT	#40000,2KCRS	:CARD DONE SET ?
1389	003234	001001				BNE	9S	:CARD DONE IN ERROR ?
1390	003236	104000				HLT		:CARD DONE ERROR
1391	003240	005077	175644		9S:	CLR	2KCRS	:CLEAR CONTROL REG.
1392	003244	032777	044202	175636		BIT	#44202,2KCRS	:DID THIS CLEAR ALL
1393	003252	001401				BEQ	10S	:GO DO NEXT TEST
1394	003254	104000				HLT		:ALL CONDITION WHERE NOT
1395	003256	005077	175634		10S:	CLR	2KCRM	:CLEAR MAINT.
1396								:RIGHT.

TSTM15: SCOPE  
 ;TEST ON LINE FUNCTION TO CREATE AN INTERRUPT

1401	003264	004767	001544			JSR	PC,MINIT	:SET UP MAINT. FUNCTION
1402	003270	012767	000340	174500		MOV	#340,PSR	:SET PRIORITY LOCK OUT
1403	003276	012777	000100	175604		MOV	#100,2KCRS	:SET INTERRUPT ENABLE (I.E)
1404	003304	052777	120000	175604		BIS	#120000,2KCRM	:SET READY EQUALS TRANSITION
1405								:TO ON LINE
1406	003312	017702	175566			MOV	2INTVC,R2	:SAVE OLD INTVC
1407	003316	012777	003366	175560		MOV	#1S,2INTVC	:SET UP NEW SERVICE ROUTINE
1408	003324	012777	000300	175554		MOV	#300,2INPRI	:SET UP PRIORITY INTERRUPT
1409	003332	005067	174440			CLR	PSR	:ALLOW INTERRUPT
1410	003336	000240				NOP		:TIME
1411	003340	000240				NOP		:TIME
1412	003342	000240				NOP		:TIME
1413	003344	104000				HLT		:NO INTERRUPT HAPPENED
1414	003346	012767	000340	174422	2S:	MOV	#340,PSR	:SET PROC. PRIORITY
1415	003354	005077	175530			CLR	2KCRS	:CLR I.E. & TRANSITION ON LINE
1416	003360	010277	175520			MOV	R2,2INTVC	:RESTORE OLD SERVICE ROUTINE
1417	003364	000402				BR	3S	:CONTINUE TO NEXT TEST
1418	003366	022626			1S:	CMP	(R6)+,(R6)+	:RESTORE STACK FROM INTR.
1419	003370	000766				BR	2S	:GOOD INTR RETURN TO CONT.
1420	003372	005077	175520		3S:	CLR	2KCRM	:CLEAR MAINT.

TSTM16: SCOPE  
 ;TEST OFF LINE FUNCTION TO INTERRUPT

1421  
 1422 003376 104001  
 1423  
 1424

1425	003400	004767	001430			JSR	PC,MINIT	:GO SET UP MAINT. CONDITION
1426	003404	012767	000340	174364		MOV	#340,PSR	:SET PROC. PRIORITY
1427	003412	052777	120000	175476		BIS	#120000,#KCRM	:SET READY
1428	003420	012777	000100	175462		MOV	#100,#KCRS	:SET I.E.
1429	003426	012777	100000	175462		MOV	#100000,#KCRM	:CLR READY MAINT. REG.
1430	003434	017702	175444			MOV	#INTVC,R2	:SAVE OLD SERVICE ROUTINE
1431	003440	012777	003510	175436		MOV	#18,#INTVC	:SET NEW SERVICE ROUTINE
1432	003446	012777	000300	175432		MOV	#300,#INPRI	:SET INTR PRIORITY
1433	003454	005067	174316			CLR	PSR	:DROP PROC. PRIORITY
1434	003460	000240				NOP		:TIME
1435	003462	000240				NOP		:TIME
1436	003464	000240				NOP		:TIME
1437	003466	104000				HLT		:ERROR NO INTERRUPT
1438	003470	012767	000340	174300	2S:	MOV	#340,PSR	:SET PROC. PRIORITY
1439	003476	005077	175406			CLR	#KCRS	:CLEAR INTR. ENA & OFF LINE
1440	003502	010277	175376			MOV	R2,#INTVC	:RESTORE INTERRUPT VECTOR
1441	003506	000402				BR	3S	:CONTINUE TESTING
1442	003510	022626			1S:	CMP	(R6)+,(R6)+	:RESTORE STACK
1443	003512	000766				BR	2S	:GOOD TEST CONTINUE
1444	003514	005077	175376		3S:	CLR	#KCRM	:CLEAR MAINT.
1445								
1446	003520	104001						
1447								
1448								
1449	003522	004767	001306			JSR	PC,MINIT	:SET MAINT. CONDITION
1450	003526	012767	000340	174242		MOV	#340,PSR	:SET PRIORITY
1451	003534	052777	160000	175354		BIS	#160000,#KCRM	:SET READY & BUSY
1452	003542	012777	000100	175340		MOV	#100,#KCRS	:SET I.E.
1453	003550	000240				NOP		:TIME
1454	003552	012777	120000	175336		MOV	#120000,#KCRM	:CLR READY MAINT. REG.
1455	003560	017702	175320			MOV	#INTVC,R2	:SAVE INTR. SERV (OLD)
1456	003564	012777	003634	175312		MOV	#18,#INTVC	:SET NEW SERVICE ROUTINE
1457	003572	012777	000300	175306		MOV	#300,#INPRI	:SET BR 6 FOR CARD READER
1458	003600	005067	174172			CLR	PSR	:LOWER PROC. PRIORITY
1459	003604	000240				NOP		:TIME
1460	003606	000240				NOP		:TIME
1461	003610	000240				NOP		:TIME
1462	003612	104000				HLT		:ERROR NO INTER. HAPPENED.
1463	003614	012767	000340	174154	2S:	MOV	#340,PSR	:RESTORE PROC. STATUS
1464	003622	005077	175262			CLR	#KCRS	:CLEAR CONTROL REG.
1465	003626	010277	175252			MOV	R2,#INTVC	:RESTORE OLD SERV. ROUTINE
1466	003632	000402				BR	3S	:CONT. TEST
1467	003634	022626			1S:	CMP	(R6)+,(R6)+	:RESTORE STACK
1468	003636	000766				BR	2S	:CONTINUE TEST
1469	003640	005077	175252		3S:	CLR	#KCRM	:CLEAR MAINT.
1470								
1471	003644	104001						
1472								
1473								
1474	003646	004767	001162			JSR	PC,MINIT	:SET UP MAINT.
1475	003652	012767	000340	174116		MOV	#340,PSR	:SET PROC. PRIORITY
1476	003660	012777	000100	175222		MOV	#100,#KCRS	:SET I.E.
1477	003666	052777	160000	175222		BIS	#160000,#KCRM	:SET BUSY, READY CAUSE IND. MARK
1478	003674	017702	175204			MOV	#INTVC,R2	:SAVE OLD SERV. ROUTINE
1479	003700	012777	003750	175176		MOV	#18,#INTVC	:SET NEW SERV. ROUTINE
1480	003706	012777	000300	175172		MOV	#300,#INPRI	:SET BR 6 FOR CARD READER

TSTM17: SCOPE  
;TEST CARD DONE FUNCTION TO CAUSE AN INTERRUPT

TSTM18: SCOPE  
;TEST COLUMN READY FUNCTION TO CAUSE AN INTERRUPT

1481	003714	005067	174056			CLR	PSR	:LOWER PROC. PRIORITY
1482	003720	000240				NOP		:TIME
1483	003722	000240				NOP		:TIME
1484	003724	000240				NOP		:TIME
1485	003726	104000				HLT		:ERROR COLUMN READY SHOULD INTR.
1486	003730	012767	000340	174040	2S:	MOV	#340,PSR	:RESTORE PROC PRIORITY
1487	003736	005077	175146			CLR	AKCRS	:CLEAR CONTROL REG.
1488	003742	010277	175136			MOV	R2,AINVC	:RESTORE OLD SERV. ROUTINE
1489	003746	000402				BR	3S	:GO TO NEXT TEST
1490	003750	022626			1S:	CMP	(R6)+,(R6)+	:RESTORE STACK
1491	003752	000766				BR	2S	:CONT. TEST
1492	003754	005077	175136		3S:	CLR	AKCRM	:CLEAR MAINT.
1493								
1494	003760	104001						
1495								
1496								
1497								
1498	003762	004767	001046			JSR	PC,MINIT	:SET MAINT. CONDITION
1499	003766	012767	000340	174002		MOV	#340,PSR	:SET CPU PRIORITY
1500	003774	017702	175104			MOV	AINVC,R2	:SAVE OLD SERVICE ROUTINE
1501	004000	012777	004072	175076		MOV	#1S,AINVC	:SET NEW SERVICE ROUTINE
1502	004006	012777	000300	175072		MOV	#300,AINPRI	:SET BR 6 FOR CARD READER
1503	004014	052777	160000	175074		BIS	#160000,AKCRM	:SET FIRST INDEX MARK
1504	004022	012777	000100	175060		MOV	#100,AKCRS	:SET INTR. ENABLE
1505	004030	052777	120000	175060		BIS	#120000,AKCRM	:SET SECOND INDEX MARK
1506	004036	005067	173734			CLR	PSR	:LOWER CPU PRIORITY
1507	004042	000240				NOP		
1508	004044	000240				NOP		
1509	004046	000240				NOP		
1510	004050	104000				HLT		:ERROR NO INTERRUPT
1511	004052	012767	000340	173716	2S:	MOV	#340,PSR	:RESTORE CPU PRIORITY
1512	004060	005077	175024			CLR	AKCRS	:CLEAR CR11 CONTROL & STATUS
1513	004064	010277	175014			MOV	R2,AINVC	:RESTORE INTR. VECTOR
1514	004070	000402				BR	3S	:GO DO NEXT TEST
1515	004072	022626			1S:	CMP	(R6)+,(R6)+	:RESTORE STACK
1516	004074	000766				BR	2S	:CONTINUE TEST
1517	004076	005077	175014		3S:	CLR	AKCRM	:INIT. MAINT. REG.
1518								
1519								
1520	004102	104001						
1521								
1522								
1523								
1524								
1525	004104	004767	000724			JSR	PC,MINIT	:SET MAINT. CONDITION
1526	004110	052777	160000	175000		BIS	#160000,AKCRM	:SET MAINT BUSY & READY = 1
1527	004116	032777	000200	174764		BIT	#200,AKCRS	:COLUMN READY (BIT 07)
1528	004124	001001				BNE	1S	:COLUMN READY SET BRANCH
1529	004126	104000				HLT		:COLUMN READY SHOULD HAVE BEEN SET
1530	004130	052777	120000	174760	1S:	BIS	#120000,AKCRM	:SET READY & MAINT.
1531	004136	032777	002000	174744		BIT	#2000,AKCRS	:TEST BIT 10 ON LINE TRANS.
1532	004144	001001				BNE	2S	:BRANCH IF SET
1533	004146	104000				HLT		:ERROR BIT 10 WAS ZERO
1534	004150	052777	160000	174740	2S:	BIS	#160000,AKCRM	:SET MAINT BUSY READY, CAUSE INDEX MARK
1535	004156	052777	160000	174732		BIS	#160000,AKCRM	:SECOND INDEX MARK
1536	004164	032777	004000	174716		BIT	#4000,AKCRS	:BIT 11 SET

TSTM19: SCOPE  
 :THIS TEST WILL CAUSE A TIMING ERROR WHICH SHOULD  
 :CREATE AN INTERRUPT AT CARD DONE.

TSTM20: SCOPE  
 :SET ALL CONTROL BITS IN CR11'S CONTROL & STATUS  
 :REGISTER PERFORM A RESET COMMAND VERIFY  
 :THAT RESET DID CLEAR FUNCTION IN CSR.

# E03

1537	004172	001001				BNE	35		: YES BRANCH
1538	004174	104000				HLT			: NO ERROR
1539	004176	052777	110000	174712	35:	BIS	#110000,2KCRM		: SET MAINT & MOT/HOP
1540	004204	032777	010000	174676		BIT	#10000,2KCRS		: BIT 12 SET
1541	004212	001001				BNE	45		: YES BRANCH
1542	004214	104000				HLT			: NO ERROR
1543	004216	052777	110000	174672	45:	BIS	#110000,2KCRM		: SET MAINT & MOT/HOP
1544	004224	032777	020000	174656		BIT	#20000,2KCRS		: BIT 13 SET
1545	004232	001001				BNE	55		: YES BRANCH
1546	004234	104000				HLT			: NO ERROR
1547	004236	052777	160000	174652	55:	BIS	#160000,2KCRM		: MAINT BUSY READY
1548	004244	000240				NOP			: TIME?
1549	004246	042777	140000	174642		BIC	#140000,2KCRM		: CLEAR BUSY
1550	004254	000240				NOP			: TIME?
1551	004256	032777	040000	174624		BIT	#40000,2KCRS		: BIT 14 SET
1552	004264	001001				BNE	65		: YES BRANCH
1553	004266	104000				HLT			: NO ERROR
1554	004270	052777	120000	174620	65:	BIS	#120000,2KCRM		: MAINT & READY
1555	004276	042777	120000	174612		BIC	#120000,2KCRM		: CLEAR MAINT & READY
1556	004304	000240				NOP			
1557	004306	032777	100000	174574		BIT	#100000,2KCRS		: BIT 15 SET
1558	004314	001001				BNE	75		: YES BRANCH
1559	004316	104000				HLT			: NO ERROR
1560	004320	052777	000100	174562	75:	BIS	#100,2KCRS		: SET INTR. ENABLE
1561	004326	032777	000100	174554		BIT	#100,2KCRS		: TEST FOR INTR. ENABLE SET
1562	004334	001001				BNE	85		: BRANCH IF I.E. SET
1563	004336	104000				HLT			
1564	004340	052777	000002	174542	85:	BIS	#2,2KCRS		: SET EJECT BIT
1565	004346	032777	000002	174534		BIT	#2,2KCRS		: TEST EJECT BIT SET
1566	004354	001001				BNE	95		: EJECT BIT IS SET BRANCH
1567	004356	104000				HLT			: EJECT BIT NOT SET ERROR
1568	004360	000005			95:	RESET			: INIT. THE SYSTEM
1569	004362	032777	000002	174520		BIT	#,2KCRS		: TEST BIT SHOULD = ZERO
1570	004370	001401				BEQ	105		: YES, BRANCH
1571	004372	104000				HLT			: NO, ERROR
1572	004374	032777	000100	174506	105:	BIT	#100,2KCRS		: TEST BIT SHOULD = ZERO
1573	004402	001401				BEQ	125		: YES, BRANCH
1574	004404	104000				HLT			: NO, ERROR
1575	004406	032777	002000	174474	125:	BIT	#2000,2KCRS		: TEST BIT SHOULD = ZERO
1576	004414	001401				BEQ	135		: YES, BRANCH
1577	004416	104000				HLT			: NO, ERROR
1578	004420	032777	004000	174462	135:	BIT	#4000,2KCRS		: TEST BIT SHOULD = ZERO
1579	004426	001401				BEQ	145		: YES, BRANCH
1580	004430	104000				HLT			: NO, ERROR
1581	004432	032777	040000	174450	145:	BIT	#40000,2KCRS		: TEST BIT SHOULD = ZERO
1582	004440	001401				BEQ	155		: YES, BRANCH
1583	004442	104000				HLT			: NO, ERROR
1584	004444	032777	100000	174436	155:	BIT	#100000,2KCRS		: TEST BIT SHOULD = ZERO
1585	004452	001401				BEQ	165		: YES, BRANCH
1586	004454	104000				HLT			: NO, ERROR
1587	004456	005077	174434		165:	CLR	2KCRM		: CONTINUE TO NEXT TEST

1588  
1589  
1590 004462 104001  
1591  
1592

TSTM21: SCOPE  
: THIS TEST WILL LOOK FOR INTERACTION BETWEEN  
: MOTION CHECK BIT 12 & HOPPER CHECK BIT 13

1593										
1594	004464	004767	000344			JSR	PC,MINIT		:	SET UP MAINT. FUNCTION
1595	004470	052777	150000	174420		BIS	#150000,2KCRM		:	SET MAINT BUSY MOT/HOP
1596	004476	032777	010000	174404		BIT	#10000,2KCRS		:	MOTION CHCK. SHOULD BE SET
1597	004504	001001				BNE	15		:	YES BRANCH
1598	004506	104000				HLT			:	NO ERROR
1599	004510	032777	020000	174400	15:	BIT	#20000,2KCRM		:	HOPPER CHCK. SHOULD BE CLEARED
1600	004516	001401				BEQ	25		:	YES BRANCH
1601	004520	104000				HLT			:	NO ERROR
1602	004522	012777	100000	174366	25:	MOV	#100000,2KCRM		:	CLR BUSY MOT/HOP MAINT. REG.
1603	004530	032777	010000	174352		BIT	#10000,2KCRS		:	MOTION CHCK. SHOULD BE CLEARED
1604	004536	001401				BEQ	35		:	YES BRANCH
1605	004540	104000				HLT			:	NO ERROR
1606	004542	032777	020000	174340	35:	BIT	#20000,2KCRS		:	HOPPER CHCK. SHOULD BE CLEARED
1607	004550	001401				BEQ	45		:	YES BRANCH
1608	004552	104000				HLT			:	NO. ERROR
1609	004554	005077	174336		45:	CLR	2KCRM		:	
1610									:	
1611									:	
1612	004560	104001							:	
1613									:	
1614									:	
1615									:	
1616									:	
1617	004562	004767	000246			JSR	PC,MINIT		:	SETUP MAINT. CONDITION
1618	004566	012767	000340	173202		MOV	#340,PSR		:	SET CPU PRIORITY
1619	004574	012702	017300			MOV	#ALPCD,R2		:	GET STARTING ADDRESS INTO R2
1620	004600	012705	020476			MOV	#BINEND,R5		:	GET END ADDRESS INTO R5
1621	004604	062705	000002			ADD	#2,R5		:	UPDATE END ADDRESS
1622	004610	017767	174270	000234		MOV	2JINTVC,MCNT		:	SAVE
1623	004616	017767	174264	000230		MOV	2JINPRI,MTST		:	SAVE
1624	004624	012777	004702	174252		MOV	#25,2JINTVC		:	NEW SERVICE ROUTINE
1625	004632	012777	000300	174246		MOV	#300,2JINPRI		:	SET BR6 FOR SERVICE
1626	004640	012767	160000	000212	15:	MOV	#160000,TSTM		:	SET CONTROL FUNCTIONS
1627	004646	051267	000206			BIS	(R2),TSTM		:	COMPLETE TEST WORD
1628	004652	012777	000100	174230		MOV	#100,2KCRS		:	SET INTERRUPT ENABLE
1629	004660	016777	000174	174230		MOV	TSTM,2KCRM		:	PASS CONTROL & DATA
1630	004666	005067	173104			CLR	PSR		:	LOWER CPU PRIORITY
1631	004672	000240				NOP			:	
1632	004674	000240				NOP			:	
1633	004676	000240				NOP			:	
1634	004700	104000				HLT			:	ERROR NO INTR. RESPONSE
1635	004702	022626			25:	CMP	(R6)+,(R6)+		:	UPDATE STACK
1636	004704	000257				CCC			:	CLEAR CONDITION CODE
1637	004706	022277	174200			CMP	(R2)+,2KCRB1		:	CHECK DATA
1638	004712	001401				BEQ	35		:	YES GOOD DATA BRANCH
1639	004714	104000				HLT			:	DATA ERROR
1640	004716	022277	174172		35:	CMP	(R2)+,2KCRB2		:	CHECK COMPRESSED DATA
1641	004722	001401				BEQ	45		:	YES GOOD DATA BRANCH
1642	004724	104000				HLT			:	DATA ERROR
1643	004726	020205			45:	CMP	R2,R5		:	ARE WE DONE
1644	004730	001343				BNE	15		:	CONTINUE TEST
1645	004732	005077	174160			CLR	2KCRM		:	INIT. MAINT. REG.
1646	004736	005077	174146			CLR	2KCRS		:	INIT. CONTROL REG.
1647	004742	016777	000104	174134		MOV	MCNT,2JINTVC		:	RESTORE
1648	004750	016777	000100	174130		MOV	MTST,2JINPRI		:	RESTORE

TSTM22: SCOPE  
 : THIS TEST WILL PASS SIMULATED DATA OF AN  
 : ALPHANUMERIC CARD DECK & ALSO A BINARY CARD  
 : DECK IN THE INTERRUPT MODE

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1649 004756 032777 000400 174136      BIT      #400, @SWR      ;DO YOU WANT TO LOOP ON MAINT. MODE TEST
1650 004764 001010                      BNE      MAINTL      ;YES-BRANCH TO MAINT. LOOP
1651 004766 013702 000042      MOV      @R4, R2
1652 004772 001411                      BEQ      CONT
1653 004774 000005                      RESET
1654 004776 004712      LOGICAL: JSR      PC, (R2)
1655 005000                      NOP
1656 005002                      NOP
1657 005004                      NOP
1658 005006 005726      MAINTL: TST      (SP)+
1659 005010                      CCC
1660 005012 000167 174140      JMP      START1
1661 005016 012702 023506      CONT:  MOV      @MSG20, R2      ;GO TELL A STORY ABOUT
1662 005022 004767 011400      JSR      PC, TOUT      ;WHAT WILL BE WRONG
1663 005026 004767 011516      JSR      PC, CRLF4      ;ADVANCE MESSAGE
1664
1665
1666
1667      ;*****
1668
1669 005032 000207                      RTS      PC      ;RETURN TO STARTING ADDRESS CALL
1670
1671      ;*****
1672
1673
1674
1675
1676
1677 005034 012777 100000 174054  MINIT: MOV      #100000, @KCRM      ;SET MAINT. CONTROL BIT
1678 005042 005777 174044                      TST      @KCRB1      ;STROBE BUFFER FOR CLEARING
1679 005046 005013                      CLR      @CRS      ;CLEAR CONTROL STATUS REG.
1680 005050 000207                      RTS      PC      ;RETURN TO CALLER
1681
1682
1683 005052 000000                      MCNT:   0      ;COUNT REGISTER
1684 005054 000000                      MTST:   0      ;MAINT. TEST WORD
1685 005056 000000                      MFLG:   0      ;FLAG INDICATING M8291 MODULE WITH MAINT REG
1686 005060 000000                      TSTW:   0      ;WORD USED FOR DATA TEST PATTERN
1687
1688
1689
1690

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1691      ;*****
1692      ;*****      CARD READER TEST
1693      ;*****
1694      ;*****      INITIALIZE CSR AND DBR POINTERS
1695      005062 012767 000001 011330 SETUP:  MOV    #1,ITMAX      ;SET ITERATION MAXIMUM TO 1 ITERATION
1696      005070 016703 174014          MOV    KCAS,CRS      ;SET UP REGISTER POINTERS
1697      005074 016704 174012          MOV    KCRB1,CRB1
1698      005100 016700 174000          MOV    INTVC,ADINT   ;LOAD ADDRESS OF INTERRUPT VECTOR
1699      005104 005067 173772          CLR    INTFLG        ;INITIALIZE INTERRUPT FLAG
1700      005110 005067 174034          CLR    TRFLG         ;INITIALIZE TRACE FLAG
1701      005114 012767 000340 172654 MOV    #340,PSR      ;SETUP PROCESSOR STATUS
1702      005122 000207          RTS     #7           ;RETURN
1703
1704      005124 004767 177732          BEGIN: JSR    #7,SETUP ;INITIALIZE POINTERS AND FLAGS
1705      005130 000424          BR     TEST         ;GO TO INSTRUCTION TESTS
1706      005132 022767 000176 173762 RESTRT: CMP    #SMREG,SMR
1707      005140 001002          BNE   IS
1708      005142 104002          CNTLU
1709      005144 104006          CKU
1710      005146 005767 173776          IS:   TST    TRFLG      ;CHECK FOR TRACE TRAPPING
1711      005152 001004          BNE   TRAPX        ;IF SET, TRACE TRAP
1712      005154 012767 000340 172614 NOTRP: MOV    #340,PSR   ;IF ZERO, CLEAR TRACE BIT
1713      005162 000407          BR     TEST         ;GO TO INSTRUCTION TESTS
1714      005164 032777 010000 173730 TRAPX: BIT    #10000,SMR ;CHECK SM12
1715      005172 001370          BNE   NOTRP        ;BRANCH IF SET TO CLEAR TRACE BIT
1716      005174 012767 000360 172574 MOV    #360,PSR     ;SET TRACE BIT
1717
1718      ;TEST FOR CORRECT INITIALIZATION OF STATUS REGISTER
1719      005202 012767 005212 011214 TEST:  MOV    #TEST1A,RETURN ;SETUP SCOPE LOOP RETURN ADDRESS
1720      005210 104001          TEST1: SCOPE
1721      005212 004767 010540          TEST1A: JSR    #7,CKBITB   ;CHECK FOR OFF. LINE SET
1722      005216 016767 172554 173726 MOV    PSR,PROC     ;STORE PROCESSOR STATUS
1723      005224 005067 172546          CLR    PSR         ;CLEAR TRACE BIT
1724      005230 005001          CLR    COUNT       ;INITIALIZE COUNTER
1725      005232 005201          INC    COUNT       ;WAIT TO BE CERTAIN
1726      005234 001376          BNE   .-2          ;THAT ALL CARDS ARE
1727      005236 005201          INC    COUNT       ;THRU BEFORE ISSUING
1728      005240 001376          BNE   .-2          ;INIT
1729      005242 016767 173704 172526 MOV    PROC,PSR     ;RESTORE PROCESSOR STATUS
1730      005250 000005          RESET
1731      005252 005713          TST   #CRS         ;CHECK FOR STATUS REGISTER ALL ZERO
1732      005254 001401          BEQ   .+4          ;BRANCH IF OK
1733      005256 104000          HLT
1734      ;ONLY BITS 1 AND 6 OF THE STATUS REGISTER SHOULD BE ABLE TO BE SET TO ONE
1735      ;AND READ BACK AS ONE
1736      005260 052713 177776          BIS   #177776,#CRS ;SET ALL BITS BUT 0
1737      005264 022713 000102          CMP   #102,#CRS   ;ONLY BITS 1 AND 6 SHOULD BE SET
1738      005270 001402          BEQ   .+6          ;BRANCH IF OK
1739      005272 104000          HLT                ;STATUS REGISTER DIDN'T CONTAIN 102
1740      005274 000404          BR    TEST2        ;BRANCH AFTER FAILURE
1741      ;CLEARING STATUS REGISTER SHOULD CLEAR BITS 1 AND 6
1742      005276 005013          CLR   #CRS         ;CLEAR BITS 1 AND 6
1743      005300 005713          TST   #CRS         ;CHECK FOR ALL BITS CLEAR
1744      005302 001401          BEQ   .+4          ;BRANCH IF OK
1745      005304 104000          HLT                ;BIT 1 AND/OR BIT 6 DIDN'T CLEAR
1746

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1747 005306 104001
1748
1749
1750 005310 004767 010442
1751 005314 016767 172456 173630
1752 005322 005067 172450
1753 005326 005213
1754 005330 032713 000001
1755 005334 001401
1756 005336 104000
1757 005340 005227 000000
1758 005344 001375
1759 005346 005227 000000
1760 005352 001375
1761 005354 005227 000000
1762 005360 001375
1763 005362 005227 000000
1764 005366 001375
1765 005370 005227 000000
1766 005374 001375
1767 005376 016767 173550 172372
1768 005404 032713 040000
1769 005410 001002
1770 005412 104000
1771 005414 000406
1772
1773 005416 052713 040000
1774 005422 032713 040000
1775 005426 001401
1776 005430 104000
1777
1778 005432 104001
1779
1780
1781 005434 004767 010316
1782 005440 005013
1783 005442 005213
1784 005444 032713 001000
1785 005450 001002
1786 005452 104000
1787 005454 000417
1788 005456 032713 040000
1789 005462 001010
1790 005464 032713 001000
1791 005470 001372
1792 005472 032713 040000
1793 005476 001006
1794 005500 104000
1795 005502 000404
1796 005504 032713 001000
1797 005510 001401
1798 005512 104000
1799
1800 005514 104001
1801
1802

TEST2: SCOPE
;START SHOULD CAUSE CARD DONE WITHIN 1 SECOND
;BIT 0 SHOULD ALWAYS READ AS BEING EQUAL TO ZERO
JSR X7,CKBIT8 ;CHECK FOR OFF-LINE SET
MOV PSR,PROC ;STORE CURRENT PROCESSOR STATUS
CLR PSR ;CLEAR TRACE BIT
INC @CRS ;START READING A CARD
BIT #1,@CRS ;CHECK BIT 0
BEQ .+4 ;BRANCH IF NOT SET
HLT ;BIT 0 READ AS A ONE
INC #0 ;WAIT
BNE .+1
INC #0
BNE .+1
INC #0
BNE .+1
INC #0
BNE .+1
INC #0
BNE .+1
MOV PROC,PSR ;RESTORE PROCESSOR STATUS
BIT #40000,@CRS ;CHECK CARD DONE
BNE CONT2 ;CONTINUE IF SET
HLT ;CARD DONE DIDN'T SET WITHIN 400 MS
BR TEST3 ;NOTE THAT FAILURE COULD BE DUE TO READ
;NOT BEING RESET

CONT2: BIS #40000,@CRS ;DATO TO STATUS REGISTER SHOULD CLEAR
BIT #40000,@CRS ;CARD DONE
BEQ .+4 ;BRANCH IF IT DID
HLT ;DATO DIDN'T CLEAR CARD DONE

TEST3: SCOPE
;BUSY (BIT 9) SHOULD BE SET BY READING A CARD
;IT SHOULD REMAIN SET UNTIL CARD DONE SETS, WHICH SHOULD CLEAR IT
JSR X7,CKBIT8 ;CHECK FOR OFF-LINE SET
CLR @CRS ;INITIALIZE STATUS REGISTER
INC @CRS ;READ A CARD
BIT #1000,@CRS ;CHECK BUSY
BNE LOOP3 ;BRANCH IF SET
HLT ;READING A CARD DIDN'T SET BUSY
BR TEST4

LOOP3: BIT #40000,@CRS ;CHECK CARD DONE
BNE DONE3 ;BRANCH IF SET
BIT #1000,@CRS ;CHECK BUSY
BNE LOOP3 ;BRANCH IF STILL SET
BIT #40000,@CRS ;CHECK CARD DONE
BNE TEST4 ;GO TO NEXT TEST IF SET
BR ;BUSY CLEARED BEFORE CARD DONE SET

DONE3: BIT #1000,@CRS ;CHECK BUSY
BEQ TEST4 ;GO ON TO NEXT TEST IF CLEAR
HLT ;CARD DONE DIDN'T CLEAR BUSY

TEST4: SCOPE
;A TIMING ERROR SHOULD OCCUR IF DATA IS NOT READ AND NEW DATA COMES IN
;A TIMING ERROR SHOULD SET THE SPECIAL CONDITION BIT WHEN CARD DONE OCCURS

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1803 ;COLUMN READY SHOULD BE CLEARED BY THE TIMING ERROR AND PREVENTED FROM RESETTING
1804 ;BITS 11, 14, AND 15 SHOULD BE CLEARED BY A DATO TO THE STATUS REGISTER
1805 005516 004767 010162 JSR %7, INIT ;INITIALIZE STATUS REGISTER
1806 005522 005001 CLR COUNT ;INITIALIZE COUNTER
1807 005524 005213 INC %CRS ;INITIATE READ
1808 005526 032713 140200 LOOP4: BIT #140200, %CRS ;WAIT FOR SPECIAL CONDITION, CARD DONE,
1809 ;OR COLUMN READY
1810 005532 001775 BEQ LOOP4 ;LOOP IF NONE OCCURRED
1811 005534 032713 140000 BIT #140000, %CRS ;SPECIAL CONDITION OR CARD DONE
1812 005540 001007 BNE CK4 ;YES, BRANCH
1813 005542 005201 INC COUNT ;NO, COUNT COLUMN READYS
1814 005544 105713 LOOP4B: TSTB %CRS ;WAIT FOR COLUMN READY TO CLEAR
1815 005546 100367 BPL LOOP4 ;IF CLEAR, RETURN TO LOOP4
1816 005550 032713 140000 BIT #140000, %CRS ;CHECK FOR SPECIAL CONDITION OR CARD DONE
1817 005554 001001 BNE CK4 ;BRANCH IF EITHER SET
1818 005556 000772 BR LOOP4B ;OTHERWISE, CHECK AGAIN
1819 005560 032713 040000 CK4: BIT #40000, %CRS ;CHECK CARD DONE
1820 005564 001002 BNE .+6 ;BRANCH IF SET
1821 005566 104000 HLT ;SPECIAL CONDITION SET BEFORE CARD DONE
1822 005570 000403 BR CONT4
1823 005572 005713 TST %CRS ;CHECK SPECIAL CONDITION
1824 005574 100401 BMI .+4 ;BRANCH IF SET
1825 005576 104000 HLT ;SPECIAL CONDITION WASN'T SET
1826 005600 032713 004000 CONT4: BIT #4000, %CRS ;CHECK TIMING ERROR
1827 005604 001001 BNE .+4 ;BRANCH IF SET
1828 005606 104000 HLT ;TIMING ERROR WASN'T SET
1829 005610 005301 DEC COUNT ;CHECK NUMBER OF COLUMN READYS
1830 005612 100002 BPL .+6 ;BRANCH IF ANY OCCURRED
1831 005614 104000 HLT ;COLUMN READY NEVER OCCURRED
1832 005616 000402 BR .+6
1833 005620 001401 BEQ .+4 ;BRANCH IF ONLY ONE OCCURRED
1834 005622 104000 HLT ;COLUMN READY OCCURRED MORE THAN ONCE
1835 005624 105713 TSTB %CRS ;CHECK COLUMN READY
1836 005626 100001 BPL .+4 ;BRANCH IF NOT SET
1837 005630 104000 HLT ;COLUMN READY WASN'T CLEARED
1838 005632 005013 CLR %CRS ;CLEAR BITS 11, 14, AND 15 VIA DATO
1839 005634 032713 144000 BIT #144000, %CRS ;CHECK
1840 005640 001401 BEQ .+4
1841 005642 104000 HLT ;BITS 11, 14, AND 15 WEREN'T ALL CLEARED
1842
1843
1844 005644 104001 TEST5: SCOPE
1845 ;SETTING READ SHOULD CAUSE COLUMN READY TO SET 80 TIMES BEFORE CARD DONE SETS
1846 ;READING THE DATA BUFFER SHOULD CLEAR COLUMN READY AND PREVENT A TIMING ERROR
1847 005646 004767 010032 JSR %7, INIT ;INITIALIZE STATUS REGISTER
1848 005652 005001 CLR COUNT ;INITIALIZE COUNTER
1849 005654 005213 INC %CRS ;INITIATE READ
1850 005656 032713 140200 LOOPS: BIT #140200, %CRS ;WAIT FOR COLUMN READY, CARD DONE
1851 005662 001775 BEQ .-4 ;OR SPECIAL CONDITION
1852 005664 032713 040000 BIT #40000, %CRS ;CARD DONE
1853 005670 001015 BNE CK5 ;YES, BRANCH
1854 005672 005713 TST %CRS ;CHECK BIT 15
1855 005674 100002 BPL .+6 ;SKIP ERROR HALT IF NOT SET
1856 005676 104000 HLT ;BIT 15 WAS SET
1857 005700 000437 BR TEST6 ;GO TO NEXT TEST
1858 005702 020127 000117 CMP COUNT, #79 ;CHECK FOR 80

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1859 005706 100363      BPL      LOOPS      ;BRANCH IF 80 OR MORE WITHOUT CLEARING READY
1860 005710 005201      INC      COUNT      ;INCREMENT COUNTER
1861 005712 005714      TST     @CRB1      ;CLEAR READY
1862 005714 105713      TSTB    @CRS       ;MAKE SURE IT CLEARED
1863 005716 100001      BPL     .+4        ;BRANCH IF IT DID
1864 005720 104000      HLT     ;READING DATA BUFFER DIDN'T CLEAR READY
1865 005722 000755      BR      LOOPS      ;LOOP
1866 005724 032713 004000      CK5:    BIT     @4000, @CRS ;CHECK TIMING ERROR BIT
1867 005730 001401      BEQ     .+4        ;BRANCH IF NOT SET
1868 005732 104000      HLT     ;TIMING ERROR WAS SET
1869                                     ;NOTE THAT IF COLUMN READY SET MORE THAN 80 TIMES
1870                                     ;A TIMING ERROR WILL OCCUR AND THE COUNT WILL BE 79 (=117 OCTAL)
1871 005734 000421      BR      TEST6     ;BRANCH AFTER ERROR
1872 005736 020127 000117      CMP     COUNT, #79 ;CHECK COUNT
1873 005742 001401      BEQ     .+4        ;BRANCH IF 80 COLUMN READYS OCCURRED
1874 005744 104000      HLT     ;COLUMN READY DIDN'T OCCUR 80 TIMES
1875                                     ;BEFORE CARD DONE
1876 005746 021327 040200      CMP     @CRS, #40200 ;ONLY CARD DONE AND COLUMN READY SHOULD BE SET
1877 005752 001401      BEQ     .+4
1878 005754 104000      HLT     ;STATUS REGISTER IN WRONG STATE
1879 005756 005013      CLR     @CRS      ;SHOULD CLEAR DONE BUT NOT READY
1880 005760 021327 000200      CMP     @CRS, #200 ;CHECK FOR ONLY READY SET
1881 005764 001401      BEQ     .+4        ;BRANCH IF OK
1882 005766 104000      HLT     ;STATUS REGISTER IN WRONG STATE
1883 005770 005714      TST     @CRB1     ;READING DATA BUFFER SHOULD CLEAR COLUMN READY
1884 005772 005713      TST     @CRS      ;CHECK STATUS REGISTER
1885 005774 001401      BEQ     .+4        ;BRANCH IF ALL BITS ZERO
1886 005776 104000      HLT     ;STATUS REGISTER NOT EQUAL TO ZERO
1887
1888 006000 104001      TEST6: SCOPE
1889                                     ;TIMING ERROR SHOULD SET BIT 11 BEFORE CARD DONE OCCURS, EVEN IF IT OCCURS AT COLUMN 80
1890                                     ;DATOB TO THE LOW BYTE OF THE CRS SHOULD CLEAR BITS 15,14, AND 11
1891 006002 004767 007676      JSR     X7, INIT   ;INITIALIZE
1892 006006 012701 000115      MOV     #77, COUNT ;SETUP COUNTER
1893 006012 005213      INC     @CRS      ;START READING A CARD
1894 006014 105713      LOOP6: TSTB    @CRS ;WAIT FOR COLUMN READY
1895 006016 100376      BPL     .-2
1896 006020 005714      TST     @CRB1     ;CLEAR COLUMN READY
1897 006022 005301      DEC     COUNT     ;GO THRU LOOP FOR 1ST 78 COLUMN READY'S
1898 006024 100373      BPL     LOOP6
1899 006026 032713 144000      BIT     #144000, @CRS ;WAIT FOR CARD DONE OR TIMING ERROR
1900 006032 001775      BEQ     .-4        ;OR SPECIAL CONDITION
1901 006034 032713 040000      BIT     #40000, @CRS ;CARD DONE SET
1902 006040 001026      BNE     ERR6      ;YES, 2 POSSIBLE TEST FAILURES
1903 006042 032713 004000      BIT     #4000, @CRS ;CHECK TIMING ERROR
1904 006046 001416      BEQ     OFF6      ;IF NOT SET, READER IS PROBABLY OFF-LINE
1905 006050 105713      TSTB    @CRS      ;CHECK COLUMN READY
1906 006052 100001      BPL     .+4        ;BRANCH IF CLEAR
1907 006054 104000      HLT     ;TIMING ERROR DIDN'T CLEAR READY
1908 006056 005713      TST     @CRS      ;WAIT FOR SPECIAL CONDITION
1909 006060 100376      BPL     .-2
1910 006062 032713 040000      BIT     #40000, @CRS ;CHECK CARD DONE
1911 006066 001406      BEQ     OFF6      ;IF NOT SET, READER IS PROBABLY OFF-LINE
1912 006070 105013      CLRB   @CRS      ;DATOB TO LOW BYTE OF CRS
1913 006072 032713 144000      BIT     #144000, @CRS ;CHECK BITS 15,14,11
1914 006076 001415      BEQ     TEST7     ;BRANCH IF CLEAR TO NEXT TEST

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1915 006100 104000
1916
1917 006102 000413
1918 006104 032713 000400
1919 006110 001010
1920 006112 104000
1921 006114 000406
1922 006116 032713 004000
1923 006122 001402
1924 006124 104000
1925 006126 000401
1926 006130 104000
1927
1928 006132 104001
1929
1930
1931
1932
1933
1934 006134 004767 007544
1935 006140 005213
1936 006142 012701 000120
1937 006146 032713 140200
1938 006152 001775
1939 006154 005713
1940 006156 100002
1941 006160 104000
1942 006162 000455
1943 006164 032713 040000
1944 006170 001013
1945 006172 005301
1946 006174 001402
1947 006176 005714
1948 006200 000762
1949 006202 032713 140000
1950 006206 001775
1951 006210 005713
1952 006212 100002
1953 006214 104000
1954 006216 000437
1955 006220 005701
1956 006222 001402
1957 006224 104000
1958 006226 000433
1959 006230 105213
1960 006232 105713
1961 006234 100401
1962 006236 104000
1963 006240 032713 004000
1964 006244 001775
1965 006246 105713
1966 006250 100002
1967 006252 104000
1968 006254 000420
1969 006256 112713 000002
1970 006262 032713 004000

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      HLT                                ;DATOB TO LOW BYTE OF CRS DIDN'T CLEAR
OFF6: BR      TEST7                      ;BITS 15,14 AND/OR 11
      BIT      #400,CRS                   ;GO TO NEXT TEST
      BNE     TEST7                       ;CHECK BIT 8
      HLT                                ;BRANCH IF SET
ERR6: BR      TEST7                      ;BIT 15 WAS SET, 8 WASN'T
      BIT      #4000,CRS                  ;GO TO NEXT TEST
      BEQ     .+6                          ;TIMING ERROR SET
      HLT                                ;NO BRANCH
      BR      TEST7                      ;TIMING ERROR DIDN'T SET BEFORE CARD DONE
      HLT                                ;GO TO NEXT TEST AFTER ERROR
      HLT                                ;TIMING ERROR WASN'T SET

TEST7: SCOPE
;NOT READING THE EIGHTIETH COLUMN OF DATA FROM THE BUFFER
;SHOULD CAUSE A TIMING ERROR ON THE FIRST COLUMN OF THE NEXT CARD
;SETTING EJECT SHOULD CLEAR TIMING ERROR, AND BIT 15 SHOULDN'T SET
;INCB SHOULD START A READ

      JSR     %7,INIT                     ;INITIALIZE
      INC     CRCS                         ;START READ
      MOV     #80,COUNT                    ;INITIALIZE COUNTER
LOOP7: BIT      #140200,CRS                ;TEST FOR ERROR, DONE OR READY
      BEQ     LOOP7                       ;LOOP IF NONE SET
      TST     CRCS                         ;CHECK ERROR
      BPL     .+6                          ;BRANCH IF NOT SET
      HLT                                ;BIT 15 WAS SET
      BR      TEST8                       ;GO TO NEXT TEST AFTER ERROR
      BIT      #40000,CRS                  ;CHECK FOR CARD DONE
      BNE     DONE7                       ;BRANCH IF SET
      DEC     COUNT                       ;COUNT
      BEQ     .+6                          ;IF BOTH COLUMN READY, BRANCH
      TST     @CRB1                       ;CLEAR DONE
      BR      LOOP7                       ;LOOP
      BIT      #140000,CRS                  ;WAIT FOR DONE OR SPECIAL CONDITION
      BEQ     -4                            ;CHECK SPECIAL CONDITION
      TST     CRCS                         ;BRANCH IF NOT SET
      BPL     DONE7                       ;SPECIAL CONDITION WAS SET
      HLT                                ;GO TO NEXT TEST AFTER ERROR
DONE7: TST     COUNT                       ;TEST FOR 80 COLUMN READY'S
      BEQ     .+6                          ;BRANCH IF OK
      HLT                                ;COLUMN READY DID NOT OCCUR 80 TIMES
      BR      TEST8                       ;GO TO NEXT TEST AFTER ERROR
      INCB    CRCS                         ;START READ
      TSTB   CRCS                         ;CHECK COLUMN READY
      BMI     .+4                          ;BRANCH IF STILL SET
      HLT                                ;READY DID NOT REMAIN SET
      BIT      #4000,CRS                   ;TEST FOR TIMING ERROR
      BEQ     -4                            ;LOOP IF NOT SET
      TSTB   CRCS                         ;CHECK COLUMN READY
      BPL     .+6                          ;BRANCH IF NOT SET
      HLT                                ;TIMING ERROR DIDN'T CLEAR READY
      BR      TEST8                       ;SET EJECT
      MOVB   #2,CRCS                      ;CHECK TIMING ERROR
      BIT      #4000,CRS

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1971 006266 001402          BEQ      .+6          ;BRANCH IF CLEARED
1972 006270 104000          HLT                      ;TIMING ERROR NOT CLEARED BY DATOB
1973 006272 000411          BR       TEST8          ;GO TO NEXT TEST AFTER ERROR
1974 006274 032713 140000   BIT      #140000,DCRS   ;WAIT FOR DONE OR SPECIAL CONDITION
1975 006300 001775          BEQ      .-4
1976 006302 032713 000400   BIT      #400,DCRS     ;CHECK BIT 8
1977 006306 001003          BNE     TEST8          ;BRANCH IF READER OFF-LINE
1978 006310 005713          TST     DCRS           ;SPECIAL CONDITION SHOULDN'T SET
1979 006312 100001          BPL     .+4           ;SINCE DATOB CLEARED TIMING ERROR
1980 006314 104000          HLT                      ;BIT 15 WAS SET, 8 WASN'T
1981
1982
1983 006316 104001          TEST8:  SCOPE
;DATA SHOULD BE AVAILABLE IN THE DATA BUFFER FOR AT LEAST 1.0 MILLISECOND
1984
1985 006320 004767 007360          JSR     %7 INIT        ;INITIALIZE STATUS REGISTER
1986 006324 016767 171446 172620   MOV     PSR,PROC       ;STORE CURRENT PROCESSOR STATUS
1987 006332 005067 171440          CLR     PSR            ;CLEAR TRACE BIT
1988 006336 005213          INC     DCRS           ;START READ
1989 006340 032713 140200   LOOP8:  BIT      #140200,DCRS ;WAIT FOR COLUMN READY OR CARD DONE
1990 006344 001775          BEQ     .-4           ;OR SPECIAL CONDITION
1991 006346 032713 040000   BIT      #40000,DCRS  ;CARD DONE
1992 006352 001023          BNE     DBRCK8        ;YES, GO TO CHECK STROBING OF DBR
1993 006354 005713          TST     DCRS           ;NO, CHECK BIT 15
1994 006356 100002          BPL     .+6           ;BRANCH IF NOT SET
1995 006360 104000          HLT                      ;BIT 15 WAS SET
1996 006362 000441          BR      TEST9          ;GO TO NEXT TEST AFTER ERROR
1997 006364 005013          CLR     DCRS           ;DATO TO CRS - SHOULDN'T CLEAR BUSY OR READY
1998 006366 022713 001200   CMP     #1200,DCRS     ;CHECK FOR BUSY AND READY
1999 006372 001402          BEQ     .+6           ;BRANCH IF STILL SET
2000 006374 104000          HLT                      ;CRS IN WRONG STATE
2001 006376 000433          BR      TEST9          ;GO TO NEXT TEST AFTER ERROR
2002 006400 011405          MOV     @CRB1,R5       ;STORE DATA
2003 006402 012701 000300   MOV     #300,COUNT     ;INITIALIZE COUNTER
2004 006406 005301          DEC     COUNT          ;WAIT FOR 1 MILLISECOND (APPROX.)
2005 006410 001376          BNE     .-2
2006 006412 021405          CMP     @CRB1,R5       ;DATA UNCHANGED
2007 006414 001751          BEQ     LOOP8          ;OK, CONTINUE
2008 006416 104000          HLT                      ;DATA NOT AVAILABLE FOR 1.0 MILLISECONDS
2009 006420 000422          BR      TEST9          ;GO TO NEXT TEST AFTER FAILURE
2010 006422 017702 172466   DBRCK8: MOV     @KCRB2,R2 ;STORE ENCODED DATA IN REGISTER 2
2011 006426 012701 000100   MOV     #100,COUNT    ;SET UP COUNTER
2012 006432 021405          CONT8:  CMP     @CRB1,R5 ;READ CARD-IMAGE DATA BUFFER
2013 006434 001402          BEQ     .+6           ;BRANCH IF UNCHANGED
2014 006436 104000          HLT                      ;CRB1 READ INCORRECTLY
2015 006440 000407          BR      REST8         ;BRANCH TO RESTORE PROCESSOR STATUS AND EXIT
2016 006442 027702 172446   CMP     @KCRB2,R2     ;READ ENCODED DATA BUFFER
2017 006446 001402          BEQ     .+6           ;BRANCH IF UNCHANGED
2018 006450 104000          HLT                      ;KCRB2 READ INCORRECTLY
2019 006452 000402          BR      REST8         ;BRANCH AFTER FAILURE
2020 006454 005301          DEC     COUNT          ;COUNT DOWN
2021 006456 001365          BNE     CONT8         ;LOOP IF NOT DONE
2022 006460 016767 172466 171310 REST8:  MOV     PROC,PSR      ;RESTORE PROCESSOR STATUS
2023
2024
2025 006466 104001          TEST9:  SCOPE
;EJECT SHOULD PREVENT FURTHER COLUMN READY'S
2026

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2027                                     ;CARD DONE SHOULD STILL OCCUR, AND TIMING ERRORS SHOULD BE
2028                                     ;PREVENTED IF THE CURRENT COLUMN READY IS CLEARED
2029 006470 004767 007210                JSR    %7,INIT          ;INITIALIZE STATUS REGISTER
2030 006474 016757 171276 172450        MOV    PSR,PROC        ;SAVE PROCESSOR STATUS
2031 006502 005067 171270                CLR    PSR             ;CLEAR TRACE BIT
2032 006506 005213                        INC    %CRS            ;START READ
2033 006510 105713                        TSTB   %CRS            ;WAIT FOR COLUMN READY
2034 006512 001776                        BEQ    -2              ;
2035 006514 052713 000002                BIS    #2,%CRS        ;SET EJECT
2036 006520 005714                        TST    %CRB1          ;CLEAR COLUMN READY
2037 006522 005001                        CLR    COUNT          ;LOOP TAKES 11.4 MICROSECONDS ONCE THRU
2038 006524 032713 044200                WAIT9: BIT  #44200,%CRS ;WAIT FOR CARD DONE, TIMING ERROR, OR
2039 006530 001004                        BNE    CK9            ;COLUMN READY
2040 006532 005201                        INC    COUNT          ;TIME FOR ABOUT 3/4 SECOND
2041 006534 001373                        BNE    WAIT9          ;CONTINUE WAITING
2042 006536 104000                        HLT                                ;NO CARD DONE OCCURRED WITHIN 3/4 SECOND
2043 006540 000411                        BR                                ;CONTINUE AFTER FAILURE
2044 006542 032713 040000                CK9:  BIT  #40000,%CRS ;CHECK FOR CARD DONE
2045 006546 001006                        BNE    REST9          ;
2046 006550 032713 000200                BIT    #200,%CRS      ;CHECK COLUMN READY
2047 006554 001402                        BEQ    +6              ;BRANCH IF NOT SET
2048 006556 104000                        HLT                                ;COLUMN READY WAS SET
2049 006560 000401                        BR                                ;
2050 006562 104000                        HLT                                ;EJECT DID NOT PREVENT A TIMING ERROR
2051 006564 016767 172362 171204        REST9: MOV   PROC,PSR  ;RESTORE PROCESSOR STATUS
2052
2053
2054 006572 104001                TEST10: SCOPE
2055                                     ;CARD DONE SHOULD CAUSE AN INTERRUPT
2056 006574 004767 007104                JSR    %7,INIT          ;INITIALIZE
2057 006600 012710 006654                MOV    #TINT10,%ADINT ;LOAD RETURN POINTER
2058 006604 052767 000340 171164        BIS    #340,PSR        ;SET PROCESSOR TO LEVEL 7
2059 006612 016760 171160 000002        MOV    PSR,2(%ADINT)  ;LOAD RETURN PROCESSOR STATUS
2060 006620 042767 000340 171150        BIC    #340,PSR        ;SET PROCESSOR PRIORITY TO 0
2061 006626 012713 000103                MOV    #103,%CRS      ;SET EJECT, INTERRUPT ENABLE, AND READ
2062 006632 032713 040000                BIT    #40000,%CRS    ;WAIT FOR CARD DONE
2063 006636 001775                        BEQ    -4              ;
2064 006640 016067 000002 171130        MOV    2(%ADINT),PSR  ;RESTORE PROCESSOR TO HIGHEST PRIORITY
2065 006646 105013                        CLRB   %CRS            ;CLEAR INTERRUPT ENABLE
2066 006650 104000                        HLT                                ;NO INTERRUPT OCCURRED
2067 006652 000414                        BR                                ;
2068 006654 032713 040000                TINT10: BIT #40000,%CRS ;CHECK CARD DONE
2069 006660 001001                        BNE    +4              ;BRANCH IF SET
2070 006662 104000                        HLT                                ;CARD DONE NOT SET
2071 006664 022626                        CMP    (SP)+,(SP)+    ;RESTORE STACK POINTER
2072 006666 005713                        TST    %CRS            ;MAKE SURE NO ERROR OCCURRED
2073 006670 100001                        BPL    +4              ;
2074 006672 104000                        HLT                                ;BIT 15 WAS SET
2075 006674 105713                        TSTB   %CRS            ;CHECK COLUMN READY
2076 006676 100001                        BPL    +4              ;BRANCH IF NOT SET
2077 006700 104000                        HLT                                ;COLUMN READY WAS SET
2078 006702 005013                        CLR    %CRS            ;DISABLE INTERRUPTS
2079 006704 012710 000232                CONT10: MOV #232,%ADINT ;CHANGE INTERRUPT RETURN ADDRESS
2080 006710 005037 000232                CLR    %232            ;TO CAUSE A HALT IF AN INTERRUPT OCCURS
2081
2082 006714 104001                TEST11: SCOPE

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2083 ;COLUMN READY SHOULD CAUSE AN INTERRUPT
2084 006716 004767 006762 JSR X7,INIT ;INITIALIZE
2085 006722 012710 006774 MOV #TINT11,ADINT ;LOAD RETURN POINTER
2086 006726 052767 000340 171042 BIS #340,PSR ;SET PROCESSOR STATUS TO LEVEL 7
2087 006734 016760 171036 000002 MOV PSR,2(ADINT) ;LOAD RETURN PROCESSOR STATUS
2088 006742 042767 000340 171026 BIC #340,PSR ;SET PROCESSOR PRIORITY TO 0
2089 006750 012713 000101 MOV #101,ACRS ;SET READ AND INTERRUPT ENABLE
2090 006754 105713 TSTB ACRS ;WAIT FOR COLUMN READY
2091 006756 100376 BPL -2
2092 006760 016067 000002 171010 MOV 2(ADINT),PSR ;RESTORE PROCESSOR TO HIGHEST PRIORITY
2093 006766 005013 CLR ACRS ;CLEAR INTERRUPT ENABLE
2094 006770 104000 HLT ;COLUMN READY DID NOT INTERRUPT
2095 006772 000405 BR CONT11
2096 006774 005013 TINT11: CLR ACRS ;CLEAR INTERRUPT ENABLE
2097 006776 105713 TSTB ACRS ;MAKE SURE COLUMN READY IS SET
2098 007000 100401 BMI +4 ;BRANCH IF SET
2099 007002 104000 HLT ;COLUMN READY WASN'T SET
2100 007004 022626 CMP (SP)+,(SP)+ ;RESTORE STACK POINTER
2101 007006 012710 000232 CONT11: MOV #232,ADINT ;CHANGE INTERRUPT RETURN ADDRESS
2102 007012 005037 000232 CLR #232 ;TO CAUSE A HALT IF ANOTHER INTERRUPT OCCURS
2103
2104 007016 104001 TEST12: SCOPE
2105 ;CARD DONE SHOULDN'T CAUSE AN INTERRUPT IF THE PROCESSOR IS AT LEVEL 7 PRIORITY
2106 007020 004767 006660 JSR X7,INIT ;INITIALIZE
2107 007024 012710 007060 MOV #TINT12,ADINT ;SETUP RETURN
2108 007030 052767 000340 170740 BIS #340,PSR ;SET PROCESSOR TO LEVEL 7 PRIORITY
2109 007036 016760 170734 000002 MOV PSR,2(ADINT) ;LOAD RETURN PROCESSOR STATUS
2110 007044 012713 000103 MOV #103,ACRS ;SET EJECT, INTERRUPT ENABLE, AND READ
2111 007050 032713 040000 BIT #40000,ACRS ;WAIT FOR CARD DONE
2112 007054 001775 BEQ -4
2113 007056 000402 BR +6 ;CONTINUE IF NO INTERRUPT OCCURRED
2114 007060 104000 TINT12: HLT ;AN INTERRUPT OCCURRED
2115 007062 022626 CMP (SP)+,(SP)+ ;RESTORE STACK POINTER
2116 007064 005013 CLR ACRS ;CLEAR INTERRUPT ENABLE AND EJECT
2117 007066 012710 000232 MOV #232,ADINT ;CHANGE INTERRUPT RETURN ADDRESS
2118 007072 005037 000232 CLR #232 ;TO CAUSE A HALT IF AN INTERRUPT OCCURS
2119
2120 ;FIND THE LEVEL AT WHICH AN INTERRUPT OCCURS
2121 ;PRINT OUT A MESSAGE STATING THIS LEVEL IF IT IS OTHER THAN THE STANDARD (LEVEL 6)
2122 ;MAKE CERTAIN THAT IT ALWAYS OCCURS AT THIS LEVEL
2123 ;THE MESSAGE STATING THE LEVEL IS PRINTED ONLY ONCE, AND THE PROGRAM MUST
2124 ;BE STARTED OVER AT LOCATION 200 FOR IT TO BE PRINTED AGAIN
2125
2126
2127 ;TEST FOR AN INTERRUPT ON LEVEL 7
2128 TEST13: SCOPE
2129 007076 104001 JSR X7,INIT ;INITIALIZE
2130 007100 004767 006600 MOV #TINT13,ADINT ;SETUP RETURN ADDRESS
2131 007104 012710 007214 BIS #340,PSR ;SET PROCESSOR PRIORITY TO 7
2132 007110 052767 000340 170660 MOV PSR,2(ADINT) ;SETUP RETURN PROCESSOR STATUS
2133 007116 016760 170654 000002 BIC #340,PSR ;SET PROCESSOR PRIORITY TO 0
2134 007124 042767 000340 170644 BIS #300,PSR ;SET PROCESSOR TO LEVEL 6 PRIORITY
2135 007132 052767 000300 170636 MOV #103,ACRS ;SET EJECT INTERRUPT ENABLE, AND READ
2136 007140 012713 000103 BIT #40000,ACRS ;WAIT FOR CARD DONE
2137 007144 032713 040000 BEQ -4
2138 007152 016067 000002 170616 MOV 2(ADINT),PSR ;RESTORE PROCESSOR TO HIGHEST PRIORITY

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2139 007160 005013          CLR      @CRS      ;DISABLE INTERRUPTS
2140 007167 012710 000232  MOV      @232,@ADINT ;CHANGE INTERRUPT RETURN ADDRESS
2141 007166 005037 000232  CLR      @232      ;TO CAUSE A HALT IF AN INTERRUPT OCCURS
2142 007172 005767 171704  TST     INTFLG    ;CHECK TO SEE IF LEVEL ALREADY RECORDED
2143 007176 100044          BPL     TEST14    ;IF NO, GO TO NEXT TEST
2144 007200 026727 171676 100007  CMP     INTFLG,@100007 ;IF SO, CHECK TO SEE
2145 007206 100440          BMI     TEST14    ;THAT THE INTERRUPT LEVEL RECORDED
2146                                     ;IS BELOW THE CURRENT LEVEL
2147 007210 104000          HLT                                     ;INTERRUPT DIDN'T OCCUR WITH STATUS
2148                                     ;AT LEVEL 7, BUT PREVIOUSLY OCCURRED
2149                                     ;AT OR ABOVE THIS LEVEL
2150 007212 000436          BR      TEST14
2151 007214 032713 040000  TINT13: BIT     @40000,@CRS ;MAKE SURE CARD DONE IS SET
2152 007220 001001          BNE     .+4       ;BRANCH IF SET
2153 007222 104000          HLT                                     ;CARD DONE WASN'T SET
2154 007224 005013          CLR      @CRS      ;DISABLE FURTHER INTERRUPTS
2155 007226 012710 000232  MOV      @232,@ADINT ;CHANGE INTERRUPT RETURN ADDRESS
2156 007232 005037 000232  CLR      @232      ;TO CAUSE A HALT IF AN INTERRUPT OCCURS
2157 007236 022626          CMP     (SP)+,(SP)+ ;RESTORE STACK POINTER
2158 007240 005767 171630  TST     INTFLG    ;CHECK FOR PREVIOUS FLAG
2159 007244 100414          BMI     SET7      ;BRANCH IF FLAG SET
2160 007246 012767 100007 171626  MOV     @100007,INTFLG ;SET FLAG AND LEVEL
2161 007254 012702 022163  MOV     @MSG4,R2   ;SETUP FOR PRINTOUT
2162 007260 004767 007142  JSR     X7,TOUT    ;PRINT MESSAGE "THE INTERRUPT LEVEL WAS"
2163 007264 012702 000007  MOV     @7,R2
2164 007270 004767 006714  JSR     X7,PROCT  ;PRINT LEVEL NUMBER
2165 007274 000405          BR      TEST14
2166 007276 026727 171600 100007  SET7:  CMP     INTFLG,@100007 ;CHECK PREVIOUS LEVEL
2167 007304 100001          BPL     TEST14
2168 007306 104000          HLT                                     ;INTERRUPT PREVIOUSLY OCCURRED ONLY AT A LOWER LEVEL
2169
2170
2171
2172                                     ;TEST FOR AN INTERRUPT ON LEVEL 6
2173                                     ;SINCE THIS IS WHERE THE CARD READER NORMALLY IS, DON'T PRINT OUT A MESSAGE
2174                                     ;IF IT IS FOUND HERE
2175 007310 104001          TEST14: SCOPE
2176 007312 004767 006366  JSR     X7,INIT   ;INITIALIZE
2177 007316 012710 007406  MOV     @TINT14,@ADINT ;SETUP RETURN ADDRESS
2178 007322 052767 000340 170446  BIS     @340,PSR  ;SET PROCESSOR PRIORITY TO 7
2179 007330 016760 170442 000002  MOV     PSR,2(ADINT) ;SETUP RETURN PROCESSOR STATUS
2180 007336 042767 000340 170432  BIC     @340,PSR  ;SET PROCESSOR PRIORITY TO 0
2181 007344 052767 000240 170424  BIS     @240,PSR  ;SET PROCESSOR TO LEVEL 5 PRIORITY
2182 007352 012710 000103  MOV     @103,@CRS ;SET EJECT, INTERRUPT ENABLE, AND READ
2183 007356 032713 040000  BIT     @40000,@CRS ;WAIT FOR CARD DONE
2184 007362 001775          BEQ     .-4
2185 007364 016067 000002 170404  MOV     2(ADINT),PSR ;RESTORE PROCESSOR TO HIGHEST PRIORITY
2186 007372 005013          CLR     @CRS      ;DISABLE INTERRUPTS
2187 007374 012710 000232  MOV     @232,@ADINT ;CHANGE INTERRUPT RETURN ADDRESS
2188 007400 005037 000232  CLR     @232      ;TO CAUSE A HALT IF AN INTERRUPT OCCURS
2189 007404 000426          BR      TEST15
2190 007406 032713 040000  TINT14: BIT     @40000,@CRS ;MAKE SURE CARD DONE IS SET
2191 007412 001001          BNE     .+4       ;BRANCH IF SET
2192 007414 104000          HLT                                     ;CARD DONE WASN'T SET
2193 007416 005013          CLR     @CRS      ;DISABLE FURTHER INTERRUPTS
2194 007420 012710 000232  MOV     @232,@ADINT ;CHANGE INTERRUPT RETURN ADDRESS

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2195 007424 005037 000232 CLR @#232 ;TO CAUSE A HALT IF AN INTERRUPT OCCURS
2196 007430 022626 CMP (SP)+,(SP)+ ;RESTORE STACK POINTER
2197 007432 005767 171444 TST INTFLG ;CHECK FOR PREVIOUS FLAG
2198 007436 100404 BMI SET14 ;BRANCH IF FLAG SET
2199 007440 012767 100006 171434 MOV #100006,INTFLG ;SET FLAG AND LEVEL
2200 007446 000405 BR TEST15
2201 007450 026727 171426 100006 SET14: CMP INTFLG,#100006 ;CHECK PREVIOUS LEVEL
2202 007456 100001 BPL TEST15
2203 007460 104000 HLT ;INTERRUPT PREVIOUSLY OCCURRED ONLY AT A LOWER LEVEL
2204
2205 ;TEST FOR AN INTERRUPT ON LEVEL 5
2206 007462 104001 TEST15: SCOPE
2207 007464 004767 006214 JSR X7,INIT ;INITIALIZE
2208 007470 012710 007600 MOV #TINT15,@ADINT ;SETUP RETURN ADDRESS
2209 007474 052767 000340 170274 BIS #340,PSR ;SET PROCESSOR PRIORITY TO 7
2210 007502 016760 170270 000002 MOV PSR,2(ADINT) ;SETUP RETURN PROCESSOR STATUS
2211 007510 042767 000340 170260 BIC #340,PSR ;SET PROCESSOR PRIORITY TO 0
2212 007516 052767 000200 170252 BIS #200,PSR ;SET PROCESSOR TO LEVEL 4 PRIORITY
2213 007524 012713 000103 MOV #103,@CRS ;SET EJECT INTERRUPT ENABLE, AND READ
2214 007530 032713 040000 BIT #40000,@CRS ;WAIT FOR CARD DONE
2215 007534 001775 BEQ -4
2216 007536 016067 000002 170232 MOV 2(ADINT),PSR ;RESTORE PROCESSOR TO HIGHEST PRIORITY
2217 007544 005013 CLR @CRS ;DISABLE INTERRUPTS
2218 007546 012710 000232 MOV #232,@ADINT ;CHANGE INTERRUPT RETURN ADDRESS
2219 007552 005037 000232 CLR @#232 ;TO CAUSE A HALT IF AN INTERRUPT OCCURS
2220 007556 005767 171320 TST INTFLG ;CHECK TO SEE IF LEVEL ALREADY RECORDED
2221 007562 100044 BPL TEST16 ;IF NO, GO TO NEXT TEST
2222 007564 026727 171312 100005 CMP INTFLG,#100005 ;IF SO, CHECK TO SEE
2223 007572 100440 BMI TEST16 ;THAT THE INTERRUPT LEVEL RECORDED
2224 ;IS BELOW THE CURRENT LEVEL
2225 007574 104000 HLT ;INTERRUPT DIDN'T OCCUR WITH STATUS
2226 ;AT LEVEL 5, BUT PREVIOUSLY OCCURRED
2227 ;AT OR ABOVE THIS LEVEL
2228 007576 000436 BR TEST16
2229 007600 032713 040000 TINT15: BIT #40000,@CRS ;MAKE SURE CARD DONE IS SET
2230 007604 001001 BNE .+4 ;BRANCH IF SET
2231 007606 104000 HLT ;CARD DONE WASN'T SET
2232 007610 005013 CLR @CRS ;DISABLE FURTHER INTERRUPTS
2233 007612 012710 000232 MOV #232,@ADINT ;CHANGE INTERRUPT RETURN ADDRESS
2234 007616 005037 000232 CLR @#232 ;TO CAUSE A HALT IF AN INTERRUPT OCCURS
2235 007622 022626 CMP (SP)+,(SP)+ ;RESTORE STACK POINTER
2236 007624 005767 171252 TST INTFLG ;CHECK FOR PREVIOUS FLAG
2237 007630 100414 BMI SET5 ;BRANCH IF FLAG SET
2238 007632 012767 100005 171242 MOV #100005,INTFLG ;SET FLAG AND LEVEL
2239 007640 012702 022163 MOV #MSG4,R2 ;SETUP FOR PRINTOUT
2240 007644 004767 006556 JSR X7,TOUT ;PRINT MESSAGE "THE INTERRUPT LEVEL WAS"
2241 007650 012702 000005 MOV #5,R2
2242 007654 004767 006330 JSR X7,PROCT ;PRINT LEVEL NUMBER
2243 007660 000405 BR TEST16
2244 007662 026727 171214 100005 SET5: CMP INTFLG,#100005 ;CHECK PREVIOUS LEVEL
2245 007670 100001 BPL TEST16
2246 007672 104000 HLT ;INTERRUPT PREVIOUSLY OCCURRED ONLY AT A LOWER LEVEL
2247
2248 ;TEST FOR AN INTERRUPT ON LEVEL 4
2249 007674 104001 TEST16: SCOPE
2250 007676 004767 006002 JSR X7,INIT ;INITIALIZE

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2251 007702 012710 010012      MOV      #TINT16, @ADINT      ; SETUP RETURN ADDRESS
2252 007706 052767 000340 170062  BIS      #340, PSR           ; SET PROCESSOR PRIORITY TO 7
2253 007714 016760 170056 000002  MOV      PSR, 2(ADINT)       ; SETUP RETURN PROCESSOR STATUS
2254 007722 042767 000340 170046  BIC      #340, PSR           ; SET PROCESSOR PRIORITY TO 0
2255 007730 052767 000140 170040  BIS      #140, PSR           ; SET PROCESSOR TO LEVEL 3 PRIORITY
2256 007736 012713 000103      MOV      #103, @CRS         ; SET EJECT INTERRUPT ENABLE, AND READ
2257 007742 032713 040000      BIT      #40000, @CRS       ; WAIT FOR CARD DONE
2258 007746 001775      BEQ      -4
2259 007750 016067 000002 170020  MOV      2(ADINT), PSR       ; RESTORE PROCESSOR TO HIGHEST PRIORITY
2260 007756 005013      CLR      @CRS               ; DISABLE INTERRUPTS
2261 007760 012710 000232      MOV      #232, @ADINT       ; CHANGE INTERRUPT RETURN ADDRESS
2262 007764 005037 000232      CLR      @232               ; TO CAUSE A HALT IF AN INTERRUPT OCCURS
2263 007770 005767 171106      TST      INTFLG             ; CHECK TO SEE IF LEVEL ALREADY RECORDED
2264 007774 100044      BPL      TEST17             ; IF NO, GO TO NEXT TEST
2265 007776 026727 171100 100004  CMP      INTFLG, #100004    ; IF SO, CHECK TO SEE
2266 010004 100440      BMI      TEST17             ; THAT THE INTERRUPT LEVEL RECORDED
2267                                ; IS BELOW THE CURRENT LEVEL
2268 010006 104000      HLT
2269                                ; INTERRUPT DIDN'T OCCUR WITH STATUS
2270                                ; AT LEVEL 4, BUT PREVIOUSLY OCCURRED
2271                                ; AT OR ABOVE THIS LEVEL
2271 010010 000436      BR      TEST17
2272 010012 032713 040000  TINT16: BIT      #40000, @CRS  ; MAKE SURE CARD DONE IS SET
2273 010016 001001      BNE      .+4
2274 010020 104000      HLT
2275 010022 005013      CLR      @CRS               ; BRANCH IF SET
2276 010024 012710 000232      MOV      #232, @ADINT       ; CARD DONE WASN'T SET
2277 010030 005037 000232      CLR      @232               ; DISABLE FURTHER INTERRUPTS
2278 010034 022626      CMP      (SP)+, (SP)+       ; CHANGE INTERRUPT RETURN ADDRESS
2279 010036 005767 171040      TST      INTFLG             ; TO CAUSE A HALT IF AN INTERRUPT OCCURS
2280 010042 100414      BMI      SET4 ; BRANCH     ; RESTORE STACK POINTER
2281 010044 012767 100004 171030  MOV      #100004, INTFLG    ; CHECK FOR PREVIOUS FLAG
2282 010052 012702 022163      MOV      @MSG4, R2          ; IF FLAG SET
2283 010056 004767 006344      JSR      X7, TOUT           ; SET FLAG AND LEVEL
2284 010062 012702 000004      MOV      #4, R2            ; SETUP FOR PRINTOUT
2285 010066 004767 006116      JSR      X7, PROCT         ; PRINT MESSAGE "THE INTERRUPT LEVEL WAS"
2286 010072 000405      BR      TEST17
2287 010074 026727 171002 100004  SET4: CMP      INTFLG, #100004 ; PRINT LEVEL NUMBER
2288 010102 100001      BPL      TEST17            ; CHECK PREVIOUS LEVEL
2289 010104 104000      HLT
2290                                ; INTERRUPT PREVIOUSLY OCCURRED ONLY AT A LOWER LEVEL
2291                                ; TEST FOR AN INTERRUPT ON LEVEL 3
2292 TEST17: SCOPE
2293 010106 104001      JSR      X7, INIT           ; INITIALIZE
2294 010110 004767 005570      MOV      #TINT17, @ADINT    ; SETUP RETURN ADDRESS
2295 010114 012710 010224      BIS      #340, PSR           ; SET PROCESSOR PRIORITY TO 7
2296 010120 052767 000340 167650  MOV      PSR, 2(ADINT)       ; SETUP RETURN PROCESSOR STATUS
2297 010126 016760 167644 000002  BIC      #340, PSR           ; SET PROCESSOR PRIORITY TO 0
2298 010134 042767 000340 167634  BIS      #100, PSR          ; SET PROCESSOR TO LEVEL 2 PRIORITY
2299 010142 052767 000100 167626  MOV      #103, @CRS         ; SET EJECT INTERRUPT ENABLE, AND READ
2300 010154 032713 040000      BIT      #40000, @CRS       ; WAIT FOR CARD DONE
2301 010160 001775      BEQ      -4
2302 010162 016067 000002 167606  MOV      2(ADINT), PSR       ; RESTORE PROCESSOR TO HIGHEST PRIORITY
2303 010170 005013      CLR      @CRS               ; DISABLE INTERRUPTS
2304 010172 012710 000232      MOV      #232, @ADINT       ; CHANGE INTERRUPT RETURN ADDRESS
2305 010176 005037 000232      CLR      @232               ; TO CAUSE A HALT IF AN INTERRUPT OCCURS
2306 010202 005767 170674      TST      INTFLG             ; CHECK TO SEE IF LEVEL ALREADY RECORDED

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2307 010206 100044          BPL      TEST18      ; IF NO, GO TO NEXT TEST
2308 010210 026727 170666 100003  CMP      INTFLG, #100003 ; IF SO, CHECK TO SEE
2309 010216 100440          BMI      TEST18      ; THAT THE INTERRUPT LEVEL RECORDED
2310                                ; IS BELOW THE CURRENT LEVEL
2311 010220 104000          HLT      ; INTERRUPT DIDN'T OCCUR WITH STATUS
2312                                ; AT LEVEL 3, BUT PREVIOUSLY OCCURRED
2313                                ; AT OR ABOVE THIS LEVEL
2314 010222 000436          BR       TEST18
2315 010224 032713 040000  TINT17: BIT    #40000, @CRS ; MAKE SURE CARD DONE IS SET
2316 010230 001001          BNE     .+4          ; BRANCH IF SET
2317 010232 104000          HLT      ; CARD DONE WASN'T SET
2318 010234 005013          CLR     @CRS        ; DISABLE FURTHER INTERRUPTS
2319 010236 012710 000232  MOV     @232, @ADINT ; CHANGE INTERRUPT RETURN ADDRESS
2320 010242 005037 000232  CLR     @#232      ; TO CAUSE A HALT IF AN INTERRUPT OCCURS
2321 010246 022626          CMP     (SP)+, (SP)+ ; RESTORE STACK POINTER
2322 010250 005767 170626  TST     INTFLG      ; CHECK FOR PREVIOUS FLAG
2323 010254 100414          BMI     SET3        ; BRANCH IF FLAG SET
2324 010256 012767 100003 170616  MOV     #100003, INTFLG ; SET FLAG AND LEVEL
2325 010264 012702 022163  MOV     @MSG4, R2   ; SETUP FOR PRINTOUT
2326 010270 004767 006132  JSR     X7, TOUT    ; PRINT MESSAGE "THE INTERRUPT LEVEL WAS"
2327 010274 012702 000003  MOV     #3, R2
2328 010300 004767 005704  JSR     X7, PROCT   ; PRINT LEVEL NUMBER
2329 010304 000405          BR
2330 010306 026727 170570 100003 SET3: CMP   INTFLG, #100003 ; CHECK PREVIOUS LEVEL
2331 010314 100001          BPL
2332 010316 104000          HLT      ; INTERRUPT PREVIOUSLY OCCURRED ONLY AT A LOWER LEVEL
2333
2334                                ; TEST FOR AN INTERRUPT ON LEVEL 2
2335                                TEST18: SCOPE
2336 010320 104001          JSR     X7, INIT    ; INITIALIZE
2337 010322 004767 005356  JSR     @TINT18, @ADINT ; SETUP RETURN ADDRESS
2338 010326 012710 010436  MOV     #340, PSR   ; SET PROCESSOR PRIORITY TO 7
2339 010332 052767 000340 167436  BIS     PSR, 2(@ADINT) ; SETUP RETURN PROCESSOR STATUS
2340 010340 016760 167432 000002  MOV     #340, PSR   ; SET PROCESSOR PRIORITY TO 0
2341 010346 042767 000340 167422  BIS     #040, PSR   ; SET PROCESSOR TO LEVEL 1 PRIORITY
2342 010354 052767 000040 167414  BIS     #103, @CRS  ; SET EJECT INTERRUPT ENABLE, AND READ
2343 010362 012713 000103  MOV     #40000, @CRS ; WAIT FOR CARD DONE
2344 010366 032713 040000  BIT     #40000, @CRS
2345 010372 001775          BEQ     .-4
2346 010374 016067 000002 167374  MOV     2(@ADINT), PSR ; RESTORE PROCESSOR TO HIGHEST PRIORITY
2347 010402 005013          CLR     @CRS        ; DISABLE INTERRUPTS
2348 010404 012710 000232  MOV     @232, @ADINT ; CHANGE INTERRUPT RETURN ADDRESS
2349 010410 005037 000232  CLR     @#232      ; TO CAUSE A HALT IF AN INTERRUPT OCCURS
2350 010414 005767 170462  TST     INTFLG      ; CHECK TO SEE IF LEVEL ALREADY RECORDED
2351 010420 100044          BPL     TEST19      ; IF NO, GO TO NEXT TEST
2352 010422 026727 170454 100002  CMP     INTFLG, #100002 ; IF SO, CHECK TO SEE
2353 010430 100440          BMI     TEST19      ; THAT THE INTERRUPT LEVEL RECORDED
2354                                ; IS BELOW THE CURRENT LEVEL
2355                                ; INTERRUPT DIDN'T OCCUR WITH STATUS
2356                                ; AT LEVEL 2, BUT PREVIOUSLY OCCURRED
2357                                ; AT OR ABOVE THIS LEVEL
2358 010432 104000          HLT
2359 010434 000436          BR       TEST19
2360 010436 032713 040000  TINT18: BIT    #40000, @CRS ; MAKE SURE CARD DONE IS SET
2361 010442 001001          BNE     .+4          ; BRANCH IF SET
2362 010444 104000          HLT      ; CARD DONE WASN'T SET
2363 010446 005013          CLR     @CRS        ; DISABLE FURTHER INTERRUPTS
2364 010450 012710 000232  MOV     @232, @ADINT ; CHANGE INTERRUPT RETURN ADDRESS

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2363 010454 005037 000232          CLR      @#232          ;TO CAUSE A HALT IF AN INTERRUPT OCCURS
2364 010460 022626          CMP      (SP)+,(SP)+  ;RESTORE STACK POINTER
2365 010462 005767 170414          TST     INTFLG        ;CHECK FOR PREVIOUS FLAG
2366 010466 100414          BMI     SET2          ;BRANCH IF FLAG SET
2367 010470 012767 100002 170404    MOV     @100002,INTFLG ;SET FLAG AND LEVEL
2368 010476 012702 022163          MOV     @MSG4,R2      ;SETUP FOR PRINTOUT
2369 010502 004767 005720          JSR     X7,TOUT       ;PRINT MESSAGE "THE INTERRUPT LEVEL WAS"
2370 010506 012702 000002          MOV     @2,R2         ;
2371 010512 004767 005472          JSR     X7,PROCT      ;PRINT LEVEL NUMBER
2372 010516 000405          BR      TEST19        ;
2373 010520 026727 170356 100002    SET2:  CMP     INTFLG,@100002 ;CHECK PREVIOUS LEVEL
2374 010526 100001          BPL     TEST19        ;
2375 010530 104000          HLT                    ;INTERRUPT PREVIOUSLY OCCURRED ONLY AT A LOWER LEVEL
2376
2377          ;TEST FOR AN INTERRUPT ON LEVEL 1
2378 010532 104001          TEST19: SCOPE
2379 010534 004767 005144          JSR     X7,INIT       ;INITIALIZE
2380 010540 012710 010650          MOV     @TINT19,@ADINT ;SETUP RETURN ADDRESS
2381 010544 052767 000340 167224    BIS     @340,PSR      ;SET PROCESSOR PRIORITY TO 7
2382 010552 016760 167220 000002    MOV     PSR,2(ADINT)  ;SETUP RETURN PROCESSOR STATUS
2383 010560 042767 000340 167210    BIC     @340,PSR      ;SET PROCESSOR PRIORITY TO 0
2384 010566 052767 000000 167202    BIS     @000,PSR     ;SET PROCESSOR TO LEVEL 0 PRIORITY
2385 010574 012713 000103          MOV     @103,@CRS    ;SET EJECT INTERRUPT ENABLE, AND READ
2386 010600 032713 040000          BIT     @40000,@CRS  ;WAIT FOR CARD DONE
2387 010604 001775          BEQ     -4            ;
2388 010606 016067 000002 167162    MOV     2(ADINT),PSR ;RESTORE PROCESSOR TO HIGHEST PRIORITY
2389 010614 005013          CLR     @CRS         ;DISABLE INTERRUPTS
2390 010616 012710 000232          MOV     @232,@ADINT  ;CHANGE INTERRUPT RETURN ADDRESS
2391 010622 005037 000232          CLR     @#232        ;TO CAUSE A HALT IF AN INTERRUPT OCCURS
2392 010626 005767 170250          TST     INTFLG        ;CHECK TO SEE IF LEVEL ALREADY RECORDED
2393 010632 100044          BPL     TEST20        ;IF NO, GO TO NEXT TEST
2394 010634 026727 170242 100001    CMP     INTFLG,@100001 ;IF SO, CHECK TO SEE
2395 010642 100440          BMI     TEST20        ;THAT THE INTERRUPT LEVEL RECORDED
2396          ;IS BELOW THE CURRENT LEVEL
2397 010644 104000          HLT                    ;INTERRUPT DIDN'T OCCUR WITH STATUS
2398          ;AT LEVEL 1, BUT PREVIOUSLY OCCURRED
2399          ;AT OR ABOVE THIS LEVEL
2400
2401 010646 000436          BR      TEST20        ;
2402 010650 032713 040000          TINT19: BIT     @40000,@CRS ;MAKE SURE CARD DONE IS SET
2403 010654 001001          BNE     .+4          ;BRANCH IF SET
2404 010656 104000          HLT                    ;CARD DONE WASN'T SET
2405 010660 005013          CLR     @CRS         ;DISABLE FURTHER INTERRUPTS
2406 010662 012710 000232          MOV     @232,@ADINT  ;CHANGE INTERRUPT RETURN ADDRESS
2407 010666 005037 000232          CLR     @#232        ;TO CAUSE A HALT IF AN INTERRUPT OCCURS
2408 010672 022626          CMP     (SP)+,(SP)+  ;RESTORE STACK POINTER
2409 010674 005767 170202          TST     INTFLG        ;CHECK FOR PREVIOUS FLAG
2410 010700 100414          BMI     SET1          ;BRANCH IF FLAG SET
2411 010702 012767 100001 170172    MOV     @100001,INTFLG ;SET FLAG AND LEVEL
2412 010710 012702 022163          MOV     @MSG4,R2      ;SETUP FOR PRINTOUT
2413 010714 004767 005506          JSR     X7,TOUT       ;PRINT MESSAGE "THE INTERRUPT LEVEL WAS"
2414 010720 012702 000001          MOV     @1,R2         ;
2415 010724 004767 005260          JSR     X7,PROCT      ;PRINT LEVEL NUMBER
2416 010730 000405          BR      TEST20        ;
2417 010732 026727 170144 100001    SET1:  CMP     INTFLG,@100001 ;CHECK PREVIOUS LEVEL
2418 010740 100001          BPL     TEST20        ;
2419 010742 104000          HLT                    ;INTERRUPT PREVIOUSLY OCCURRED ONLY AT A LOWER LEVEL

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010744 104001 004732 167012 000002 166764 166754 104001 004626 166706 166674 000000 166654 104001 004532 166612 000002 166576 000001 000776 011210 011212 011216 011222 011224

010744 104001 004732 167012 000002 166764 166754 104001 004626 166706 166674 000000 166654 104001 004532 166612 000002 166576 000001 000776 011210 011212 011216 011222 011224

;A TIMING ERROR SHOULDN'T CAUSE AN INTERRUPT

```
TEST20: SCOPE
JSR X7,INIT ;INITIALIZE
MOV #TINT20,ADINT ;LOAD RETURN POINTER
BIS #340,PSR ;SET PROCESSOR TO HIGHEST PRIORITY
MOV PSR,2(ADINT) ;LOAD RETURN PROCESSOR STATUS
MOV #101,ACRS ;SET INTERRUPT ENABLE AND READ
BIT #4000,ACRS ;WAIT FOR TIMING ERROR TO SET
BEQ -4
BIC #340,PSR ;MOVE PROCESSOR TO LOWEST PRIORITY
NOP ;CLOCK INTERRUPT IF IT OCCURRED
MOV 2(ADINT),PSR ;MOVE PROCESSOR BACK TO HIGHEST PRIORITY
BR .+6
TINT20: HLT ;TIMING ERROR CAUSED AN INTERRUPT
CMP (SP)+,(SP)+ ;RESTORE STACK POINTER
MOV #232,ADINT ;CHANGE INTERRUPT ADDRESS TO CAUSE A
CLR #232 ;HALT IF AN INTERRUPT OCCURS
BIT #40000,ACRS ;WAIT FOR CARD DONE
BEQ -4
CLR ACRS ;CLEAR INTERRUPT ENABLE
```

TEST21: SCOPE ;TEST FOR NO INTERRUPT OCCURING WITH INTERRUPT ENABLE SET AND REST CLEARED

```
JSR X7,INIT ;INITIALIZE CSR TO ZERO
MOV #TNINT,ADINT ;SETUP RETURN ADDRESS
BIS #340,PSR ;SET PROCESSOR TO LEVEL 7
MOV PSR,2(ADINT) ;STORE PROCESSOR STATUS
CLR PSR ;SET PROCESSOR TO LEVEL 0
MOV #100,ACRS ;ENABLE INTERRUPTS
INC #0 ;WAIT AWHILE
BNE -4
MOV 2(ADINT),PSR ;RESTORE PROCESSOR TO LEVEL 7
CLR ACRS ;DISABLE FURTHER INTERRUPTS
BR CONT21
TNINT: HLT ;AN INTERRUPT OCCURRED
CMP (SP)+,(SP)+ ;RESTORE STACK
CLR ACRS ;DISABLE FURTHER INTERRUPTS
CONT21: CLR #232 ;CHANGE INTERRUPT RETURN ADDRESS TO
MOV #232,ADINT ;CAUSE A HALT IF AN INTERRUPT OCCURS
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TEST22: SCOPE ;CHECK FOR SIMULTANEOUS INTERRUPTS ON MORE THAN ONE LEVEL

```
JSR X7,INIT ;INITIALIZE CSR TO ZERO
MOV #T2INT,ADINT ;SETUP RETURN ADDRESS
BIS #340,PSR ;SET PROCESSOR TO LEVEL 7
MOV PSR,2(ADINT) ;STORE PROCESSOR STATUS
BIC #340,PSR ;SET PROCESSOR TO LEVEL 0
MOV #103,ACRS ;SET INTERRUPT ENABLE AND EJECT A CARD
WAIT ;WAIT FOR INTERRUPT
BR -2 ;SIT IF TRACE BIT IS SET
T2INT: CMP (6)+,(6)+ ;RESTORE STACK POINTER
MOV #T2INTA,ADINT ;CHANGE RETURN ADDRESS
CLR PSR ;SET PROCESSOR TO LEVEL 0
NOP ;WAIT
MOV 2(ADINT),PSR ;RESTORE PROCESSOR TO LEVEL 7
```

011232	000402		BR	CONT22	
011234	022626		T2INTA: CMP	(6)+,(6)+	:RESTORE STACK
011236	104000		HLT		:THE INTERRUPT OCCURRED AT 2 LEVELS
011240	005013		CONT22: CLR	@CRS	:DISABLE INTERRUPTS
011242	005037	000232	CLR	@#232	:CHANGE INTERRUPT RETURN ADDRESS TO
011246	012710	000232	MOV	#232,@ADINT	:CAUSE A HALT IF AN INTERRUPT OCCURS
011252	104001		TEST23: SCOPE		
			:ALL MODES OF ADDRESSING KCRB1 OR KCRB2 (DATO,DATOB,DATI) SHOULD CLEAR		
			:COLUMN READY		
011254	004767	004424	JSR	X7,INIT	:INITIALIZE
011260	005213		INC	@CRS	:START READING A CARD
011262	105713		TSTB	@CRS	:WAIT FOR COLUMN READY
011264	100376		BPL	.-2	
011266	005014		CLR	@CRB1	:DATO TO CRB1
011270	105713		TSTB	@CRS	:CHECK COLUMN READY
011272	100002		BPL	CNT23A	:BRANCH IF CLEARED
011274	104000		HLT		:DATO TO CRB1 DIDN'T CLEAR READY
011276	000467		BR	TEST24	:GO TO NEXT TEST
011300	105713		CNT23A: TSTB	@CRS	:WAIT FOR COLUMN READY
011302	100376		BPL	.-2	
011304	105014		CLRB	@CRB1	:DATOB TO LOW BYTE OF CRB1
011306	105713		TSTB	@CRS	:CHECK COLUMN READY
011310	100002		BPL	CNT23B	:BRANCH IF CLEARED
011312	104000		HLT		:DATOB TO CRB1 LOW BYTE DIDN'T CLEAR READY
011314	000460		BR	TEST24	:GO TO NEXT TEST
011316	105713		CNT23B: TSTB	@CRS	:WAIT FOR COLUMN READY
011320	100376		BPL	.-2	
011322	105064	000001	CLRB	1(CR#1)	:DATOB TO HIGH BYTE OF CRB1
011326	105713		TSTB	@CRS	:CHECK COLUMN READY
011330	100002		BPL	CNT23C	:BRANCH IF CLEARED
011332	104000		HLT		:DATOB TO CRB1 HIGH BYTE DIDN'T CLEAR READY
011334	000450		BR	TEST24	:GO TO NEXT TEST
011336	105713		CNT23C: TSTB	@CRS	:WAIT FOR COLUMN READY
011340	100376		BPL	.-2	
011342	005714		TST	@CRB1	:DATI TO CRB1
011344	105713		TSTB	@CRS	:CHECK COLUMN READY
011346	100002		BPL	CNT23D	:BRANCH IF CLEARED
011350	104000		HLT		:DATI TO CRB1 DIDN'T CLEAR READY
011352	000441		BR	TEST24	:GO TO NEXT TEST
011354	105713		CNT23D: TSTB	@CRS	:WAIT FOR COLUMN READY
011356	100376		BPL	.-2	
011360	005077	167530	CLR	@KCRB2	:DATO TO CRB2
011364	105713		TSTB	@CRS	:CHECK COLUMN READY
011366	100002		BPL	CNT23E	:BRANCH IF CLEARED
011370	104000		HLT		:DATO TO KCRB2 DIDN'T CLEAR READY
011372	000431		BR	TEST24	:GO TO NEXT TEST
011374	105713		CNT23E: TSTB	@CRS	:WAIT FOR COLUMN READY
011376	100376		BPL	.-2	
011400	105077	167510	CLRB	@KCRB2	:DATOB TO LOW BYTE OF CRB2
011404	105713		TSTB	@CRS	:CHECK COLUMN READY
011406	100002		BPL	CNT23F	:BRANCH IF CLEARED
011410	104000		HLT		:DATOB TO CRB2 LOW BYTE DIDN'T CLEAR READY
011412	000421		BR	TEST24	:GO TO NEXT TEST
011414	105713		CNT23F: TSTB	@CRS	:WAIT FOR COLUMN READY
011416	100376		BPL	.-2	

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011420 012702 177164      MOV      #177164,R2      ;LOAD POINTER
011424 105063 000001      CLR      1(R2)         ;DATOB TO HIGH BYTE OF CRB2
011430 105713          TSTB     @CRS          ;CHECK COLUMN READY
011432 100002          BPL      CNT23G        ;BRANCH IF CLEARED
011434 104000          HLT                     ;DATOB TO CRB2 HIGH BYTE DIDN'T CLEAR READY
011436 000407          BR       TEST24        ;GO TO NEXT TEST

011440 105713          CNT23G: TSTB     @CRS          ;WAIT FOR COLUMN READY
011442 100376          BPL      -2            ;
011444 005777 167444      TST      @KCRB2        ;DATI TO CRB2
011450 105713          TSTB     @CRS          ;CHECK COLUMN READY
011452 100001          BPL      TEST24        ;BRANCH IF CLEARED
011454 104000          HLT                     ;DATI TO CRB2 DIDN'T CLEAR READY

011456 104001          TEST24: SCOPE
;SETTING EJECT AFTER A COLUMN READY WITHOUT CLEARING THE COLUMN READY
;SHOULD SET TIMING ERROR (WHICH IN TURN SHOULD CLEAR COLUMN READY)
011460 004767 004220      JSR      %7,INIT        ;INITIALIZE
011464 005213          INC      @CRS          ;START READING A CARD
011466 105713          TSTB     @CRS          ;CHECK COLUMN READY - WAIT
011470 100376          BPL      -2            ;
011472 052713 000002      BIS      #2,@CRS        ;SET EJECT
011476 105713          TSTB     @CRS          ;CHECK COLUMN READY
011500 100402          BMI      CNT24A        ;BRANCH IF STILL SET
011502 104000          HLT                     ;SETTING EJECT CLEARED COLUMN READY
011504 000421          BR       END24          ;BRANCH TO WAIT FOR DONE AFTER ERROR
011506 032713 004000      CNT24A: BIT      #4000,@CRS ;CHECK TIMING ERROR
011512 001013          BNE      TIM24          ;BRANCH IF SET
011514 032713 040400      BIT      #40400,@CRS   ;CHECK CARD DONE AND OFF-LINE
011520 001772          BEQ      CNT24A        ;LOOP IF NONE SET
011522 032713 040000      BIT      #40000,@CRS   ;CARD DONE SET
011526 001003          BNE      CNT24B        ;YES - BRANCH TO ERROR PRINTOUT
011530 004767 004222      JSR      %7,CKBIT8     ;NO - BIT 8 WAS SET SO OUTPUT MESSAGE
011534 000415          BR       ENDCK         ;BRANCH AFTER COMING BACK ON-LINE
011536 104000          CNT24B: HLT                     ;CARD DONE SET BUT TIMING ERROR DIDN'T
011540 000413          BR       ENDCK         ;BRANCH TO NEXT SECTION
011542 105713          TIM24:  TSTB     @CRS          ;CHECK COLUMN READY
011544 100001          BPL      +4            ;BRANCH IF NOT SET
011546 104000          HLT                     ;TIMING ERROR DIDN'T CLEAR READY
011550 032713 040400      END24:  BIT      #40400,@CRS ;WAIT FOR CARD DONE OR OFF-LINE
011554 001775          BEQ      END24          ;
011556 032713 000400      BIT      #400,@CRS     ;CHECK OFF LINE
011562 001402          BEQ      ENDCK         ;BRANCH IF NOT SET
011564 004767 004166      JSR      %7,CKBIT8     ;OUTPUT ERROR MESSAGE

;CHECK SW7 AND RETURN TO TEST1 IF SET, AFTER RINGING BELL
;OTHERWISE GO INTO THE DATA TEST
011570 104001          ENDCK:  SCOPE
011572 032777 000200 167322  BIT      #200,@SWR      ;
011600 001406          BEQ      DATST         ;
011602 004767 004124      JSR      %7,BELL       ;
011606 005167 167336      COM      TRFLG         ;TOGGLE TRACE FLAG
011612 000167 173314      JMP      RESTAT        ;

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011616 012767 000056 001264  
011624 000410  
011626 022767 000176 167266  
011634 001002  
011636 104002  
011640 104006  
011642 005067 001242  
011646 005067 167302  
011652 032777 000010 167242  
011660 001412  
011662 012767 021200 001214  
011670 012767 021702 001210  
011676 012767 023307 001176  
011704 000442  
011706 032777 000020 167206  
011714 001425  
011716 032777 000004 167176  
011724 001407  
011726 012767 020500 001150  
011734 012767 021176 001144  
011742 000406  
011744 012767 020000 001132  
011752 012767 020476 001126  
011760 012767 023307 001114  
011766 000411  
011770 012767 017300 001106  
011776 012767 017776 001102  
012004 012767 023276 001070  
012012 005767 167132  
012016 001004  
012020 012767 000340 165750  
012026 000407  
012030 032777 010000 167064  
012036 001370  
012040 012767 000360 165730  
012046 004767 003632  
012052 012710 012106  
012056 042767 000340 165712  
012064 016760 165706 000102  
012072 004767 000674  
012076 052713 000101  
012102 000001  
012104 000776  
012106 005713  
012110 100460  
012112 105713

\*\*\*\*\*  
DATA RELIABILITY TEST FOR CR11  
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:CHECK SR FOR TYPE OF DECK BEING TESTED, AND INITIALIZE POINTERS
DATST:  MOV    #56, CDCNT      ;SETUP CARD COUNT TO ENTER TABLE CORRESPONDING TO NEXT C
        BR     DATST2         ;SKIP NEXT INSTRUCTION
DATST1: CMP    #SWREG, SWR
        BNE   IS
        CMTLU
        CKU
1$:     CLR    CDCNT          ;SETUP CARD COUNT TO ENTER DATA TABLE AT BEGINNING
DATST2: CLR    ERFLG         ;FLAG SET PREVENTS PRINTING OUT ERROR HEADING
        BIT   #10, JSWR      ;CHECK FOR TYPE OF DECK-MARK SENSE
        BEQ  DATST3
        MOV  #MRKCD, TSTART
        MOV  #MRKEND, TEND
        MOV  #MSG15, DECK
        BR   CONTD
DATST3: BIT   #20, JSWR      ;CHECK BIT 4 OF JSRPTR FOR TYPE OF DECK
        BEQ  ALP1           ;BRANCH IF NOT SET TO LOAD ALPHANUMERIC POINTERS
        BIT   #4, JSWR      ;TEST FOR TYPE OFF DECK-BINARY FIXED PATTERN
        BEQ  IS            ;NO-BRANCH TO ROTATING PATTERN
        MOV  #BINCD, TSTART ;LOAD TABLE POINTER
        MOV  #BINEND, TEND ;END OF TABLE
        BR   2$           ;CONT.
1$:     MOV  #BINCD, TSTART ;BIT 2 SET, LOAD BINARY TABLE POINTERS
        MOV  #BINEND, TEND
2$:     MOV  #MSG15, DECK
        BR   CONTD        ;BRANCH AROUND ALPHANUMERIC POINTERS
ALP1:   MOV  #ALPCD, TSTART ;LOAD ALPHANUMERIC TABLE POINTERS
        MOV  #ALPEND, TEND
        MOV  #MSG14, DECK
CONTD:  TST  TRFLG          ;CHECK TRACE TRAP FLAG
        BNE  TRP1          ;BRANCH IF FLAG WAS SET
        MOV  #340, PSR     ;CLEAR TRACE BIT
        BR   DCNT1
TRP1:   BIT   #10000, JSWR  ;CHECK SW12 TO INHIBIT TRACE TRAPPING
        BNE  NOTRP1       ;BRANCH IF SET
        MOV  #360, PSR     ;SET TRACE BIT
        JSR  %7, INIT      ;INITIALIZE CARD READER STATUS REGISTER
        ;SET UP INTERRUPT SERVICING, AND START READING
        MOV  #SRVC, ADINT  ;SETUP RETURN POINTER
        BIC  #340, PSR     ;SET PROCESSOR TO LEVEL 0
        MOV  PSR, 2(ADINT) ;STORE CURRENT STATUS
        JSR  %7, (XCRD)    ;ADJUST POINTER AND START READING
        BIS  #101, JCRS    ;ENABLE INTERRUPTS
        BR   -2           ;WAIT FOR INTERRUPTS

: INTERRUPT SERVICE ROUTINE WHICH RUNS DATA RELIABILITY TEST
SRVC:   TST   JCRS         ;CHECK SPECIAL CONDITION (BIT 15)
        BMI  ERSET        ;BRANCH IF SET
        TSTB JCRS         ;CHECK COLUMN READY
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2640 012114 100402          BMI      .+6          ;BRANCH IF SET
2641 012116 000167 000542    JMP      NOTCOL      ;JUMP IF NOT SET
2642 012122 005267 000764    INC      CLCNT       ;KEEP TRACK OF COLUMN NUMBER
2643 012128 011467 000762    MOV      @CRB1,DAT1  ;STORE DATA OF FIRST READ
2644 012132 105713          TSTB     @CRS        ;MAKE SURE COLUMN READY CLEARED
2645 012134 100006          BPL      SCONT1      ;BRANCH IF IT DID
2646 012136 052767 000340 165632  BIS      #340,PSR    ;SET PROCESSOR TO LEVEL 7
2647 012144 104000          HLT      ;READING DATA DIDN'T CLEAR COLUMN READY
2648 012146 000167 000532    JMP      LASTCK      ;GO TO NEXT CARD AFTER ERROR PRINTOUT
2649 012152 017767 166736 000740 SCONT1: MOV      @KCRB2,DATENC ;STORE ENCODED DATA
2650 012160 012701 000010    MOV      #10,COUNT  ;WAIT AWHILE
2651 012164 005301          DEC      COUNT
2652 012166 001376          BNE      .-2
2653 012170 011467 000722    MOV      @CRB1,DAT2  ;STORE DATA OF SECOND READ
2654 012174 005067 000722    CLR      PTOFF       ;CLEAR POINTER OFFSET
2655 012200 026715 000710    CMP      DAT1,@RS    ;CHECK FIRST DATA READ
2656 012204 001053          BNE      FAIL        ;PRINTOUT IF WRONG
2657 012206 012767 000002 000706  MOV      #2,PTOFF    ;SET POINTER OFFSET
2658 012214 026725 000676    CMP      DAT2,(RS)+  ;CHECK SECOND READING OF SAME DATA
2659 012220 001045          BNE      FAIL        ;BRANCH IF WRONG
2660 012222 012767 000004 000672  MOV      #4,PTOFF    ;SET POINTER OFFSET
2661 012230 026725 000664    CMP      DATENC,(RS)+ ;CHECK ENCODED DATA
2662 012234 001037          BNE      FAIL        ;BRANCH IF WRONG
2663 012236 020567 000644    CMP      RS,TEND     ;CHECK FOR END OF TABLE
2664 012242 100402          BMI      .+6          ;IF NOT THERE, RTI
2665 012244 016705 000634    MOV      TSTART,RS  ;MOVE POINTER TO LOOP THRU TABLE
2666 012250 000002          RTI
2667          ;SPECIAL CONDITION BIT 15 WAS SET WHEN THE INTERRUPT SERVICE ROUTINE
2668          ;WAS ENTERED
2669          ;OUTPUT A MESSAGE AND HALT
2670 012252 052767 000340 165516  ERSET:  BIS      #340,PSR    ;LOCK OUT INTERRUPTS
2671 012260 104003          KBINTT
2672 012262 022767 000120 000620    CMP      #80.,CDCNT ;CHECK FOR LAST CARD
2673 012270 001006          BNE      ER1         ;IF NOT, PRINT OUT MESSAGE
2674 012272 022767 000120 000612    CMP      #80.,CLCNT ;IF LAST CARD, CHECK FOR LAST COLUMN
2675 012300 001002          BNE      ER1         ;IF NOT, PRINT MESSAGE
2676 012302 000167 000616          JMP      ALLDON      ;IF END OF DECK, JUMP
2677 012306 012702 023320          ER1:   MOV      #MSG16,R2 ;"BIT 15 WAS SET."
2678 012312 004767 004110          JSR      %7,TOUT
2679 012316 012702 023341          MOV      #MSG17,R2  ;"REMEDY THE ERROR CONDITION
2680 012322 004767 004100          JSR      %7,TOUT    ;AND PRESS CONTINUE"
2681 012326 000000          HALT
2682 012330 000167 000350          JMP      LASTCK      ;SET UP FOR NEXT CARD AND GO ON
2683 012334 052767 000340 165434  FAIL:   BIS      #340,PSR    ;LOCK OUT INTERRUPTS
2684 012342 052713 000002          BIS      #2,@CRS    ;SET EJECT TO PREVENT TIMING ERROR
2685 012346 005714          TST      @CRB1      ;MAKE SURE COLUMN READY IS CLEARED
2686 012350 032777 020000 166544    BIT      #20000,@SWR ;CK SW13
2687 012356 001431          BEQ      FAILCN     ;CONTINUE IF NOT SET
2688 012360 005777 166536          TST      @SWR      ;IF SET, CHECK FOR HALT ON ERROR
2689 012364 100003          BPL      FAILC      ;BRANCH IF HALT ON ERROR NOT SET
2690 012366 000000          HALT
2691 012370 000167 000310          JMP      LASTCK      ;CONTINUE AFTER HALT
2692 012374 032713 040000          FAILC: BIT      #40000,@CRS ;CHECK FOR CARD DONE
2693 012400 001402          BEQ      .+6
2694 012402 000167 000276          JMP      LASTCK     ;INHIBIT PRINTOUT AFTER CARD DONE SET
2695 012406 032713 000400          BIT      #400,@CRS ;CHECK FOR OFF-LINE

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2696	012412	001770			BEG	FAILC		: BRANCH IF NOT
2697	012414	022767	000120	000466	CMP	#80., CDCNT		: CHECK FOR LAST CARD
2698	012422	001002			BNE	.+6		
2699	012424	000167	000474		JMP	ALLDON		: IF LAST CARD, WAIT FOR NEXT DECK
2700	012430	004767	003322		JSR	%7, CKBIT8		: IF NOT LAST CARD, PRINT MESSAGE
2701	012434	004767	000332		JSR	%7, NXC RD		: START NEXT CARD THRU READER
2702	012440	000002			RTI			
2703	012442	005767	166506		FAILCN: TST	ERFLG		: TEST FLAG FOR PREVIOUS PRINTOUT
2704	012446	001006			BNE	NOHD		: IF SET, DON'T OUTPUT HEADING
2705	012450	005267	166500		INC	ERFLG		: SET FLAG
2706	012454	012702	023206		MOV	#MSG13, R2		: OUTPUT HEADING FOR DATA ERROR PRINTOUT
2707	012460	004767	003742		JSR	%7, TOUT		
2708	012464	016702	000412		NOHD: MOV	DECK, R2		: OUTPUT TYPE OF DECK
2709	012470	004767	003732		JSR	%7, TOUT		
2710	012474	004767	003312		JSR	%7, SPACE		
2711	012500	016702	000404		MOV	CDCNT, R2		: OUTPUT CARD NUMBER WHERE ERROR OCCURRED
2712	012504	004767	003500		JSR	%7, PROCT		
2713	012510	004767	003276		JSR	%7, SPACE		
2714	012514	016702	000372		MOV	CLCNT, R2		: OUTPUT COLUMN NUMBER WHERE ERROR OCCURRED
2715	012520	004767	003464		JSR	%7, PROCT		
2716	012524	004767	003262		JSR	%7, SPACE		
2717	012530	166705	000366		SUB	PTOFF, R5		: SUBTRACT OFFSET FROM POINTER TO POINT TO
2718								: ADDRESS OF DESIRED PATTERN
2719	012534	012502			MOV	(R5)+, R2		: OUTPUT CORRECT DATA PATTERN (NOT ENCODED)
2720	012536	004767	003446		JSR	%7, PROCT		
2721	012542	004767	003244		JSR	%7, SPACE		
2722	012546	016702	000342		MOV	DAT1, R2		: OUTPUT DATA READ ON FIRST READING OF BUFFER
2723	012552	004767	003432		JSR	%7, PROCT		
2724	012556	004767	003230		JSR	%7, SPACE		
2725	012562	016702	000330		MOV	DAT2, R2		: OUTPUT DATA READ ONE MILLISECOND LATER
2726	012566	004767	003416		JSR	%7, PROCT		
2727	012572	004767	003214		JSR	%7, SPACE		
2728	012576	011502			MOV	DR5, R2		: OUTPUT CORRECT DATA PATTERN (ENCODED FORM)
2729	012600	004767	003404		JSR	%7, PROCT		
2730	012604	004767	003202		JSR	%7, SPACE		
2731	012610	016702	000304		MOV	DATENC, R2		: OUTPUT DATA READ (ENCODED)
2732	012614	004767	003370		JSR	%7, PROCT		
2733	012620	104003			KBINTT			
2734	012622	005777	166274		TST	DSMR		: CHECK "HALT ON ERROR" SWITCH
2735	012626	100001			BPL	.+4		: BRANCH IF NOT SET
2736	012630	000000			HALT			: HALT AFTER AN ERROR
2737	012632	005713			TST	DCRS		: CHECK ERROR
2738	012634	100023			BPL	LASTCK		: BRANCH IF NOT SET
2739	012636	022767	000120	000244	CMP	#80., CDCNT		: CHECK FOR LAST CARD
2740	012644	001005			BNE	FAILC1		
2741	012646	032713	000400		BIT	#400, DCRS		
2742	012652	001423			BEG	LASTCD		
2743	012654	000167	000244		JMP	ALLDON		
2744	012660	000167	177366		FAILC1: JMP	ERSET		: OUTPUT ERROR MESSAGE
2745								
2746								: INTERRUPT NOT DUE TO ERROR OR COLUMN READY
2747	012664	032713	040000		NOTCOL: BIT	#40000, DCRS		: CHECK FOR CARD DONE
2748	012670	001470			BEG	NOTCD		: BRANCH IF NOT SET
2749	012672	022767	000120	000212	CMP	#80., CLCNT		: CHECK COLUMN COUNT
2750	012700	001401			BEG	.+4		: SKIP ERROR HALT IF 80 COLUMNS WERE READ
2751	012702	104000			HLT			: LESS THAN EIGHTY COLUMNS WERE READ

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2752 012704 022767 000120 000176 LASTCK: CMP #80, CDCNT ;CHECK FOR LAST CARD
2753 012712 001403 BEQ LASTCD ;BRANCH IF LAST CARD
2754 012714 004767 000052 JSR %7, NXC RD ;IF NOT LAST CARD
2755 012720 000002 RTI ;GO ON
2756 012722 022626 LASTCD: CMP (SP)+, (SP)+ ;IF LAST CARD, RESTORE STACK POINTER
2757 012724 004767 003002 JSR %7, BELL ;RING BELL TO SIGNIFY "PASS COMPLETE"
2758 012730 032777 000040 166164 END: BIT #40, %SWR ;CHECK %SRPTR FOR CONTINUATION TO ANOTHER DECK
2759 012736 001002 BNE +6 ;BRANCH TO HALT IF SW5 SET
2760 012740 000167 000002 JMP DECKCK ;CONTINUE TO ANOTHER DECK
2761 012744 000000 HALT ;DATA TEST DONE
2762
2763 ;WHEN CONTINUING FROM ONE DECK TO ANOTHER, CHECK SW6 FOR TYPE
2764 ;OF TESTING TO BE PERFORMED
2765 012746 005167 166176 DECKCK: COM TRFLG ;TOGGLE TRACE FLAG
2766 012752 032777 000100 166142 BIT #100, %SWR ;CHECK SW6
2767 012760 001402 BEQ +6 ;BRANCH IF NOT SET
2768 012762 000167 172144 JMP RESTR ;RERUN COMBINED INSTRUCTION AND DATA TEST
2769 012766 000167 176634 JMP DATST1
2770
2771 012772 016705 000106 NXC RD: MOV TSTART, R5 ;LOAD R5 WITH TABLE STARTING ADDRESS
2772 012776 032777 000014 166116 BIT #14, %SWR ;
2773 013004 001012 BNE 1$ ;
2774 013006 006367 000076 ASL CDCNT ;MULTIPLY CARD COUNT BY FOUR
2775 013012 006367 000072 ASL CDCNT
2776 013016 066705 000066 ADD CDCNT, R5 ;ADD OFFSET TO R5 TO POINT TO NEXT DATUM
2777 013022 006267 000062 ASR CDCNT ;RESTORE CARD COUNT
2778 013026 006267 000056 ASR CDCNT
2779 013032 042713 000002 1$: BIC #2, %CRS ;CLEAR EJECT IF SET
2780 013036 005213 INC %CRS ;READ ANOTHER CARD
2781 013040 005267 000044 INC CDCNT ;KEEP TRACK OF CARD NUMBER
2782 013044 005067 000042 CLR CLCNT ;INITIALIZE COLUMN COUNT
2783 013050 000207 RTS ;RETURN
2784 ;INTERRUPT NOT CAUSED BY ERROR COLUMN READY OR CARD DONE
2785 013052 052767 000340 164716 NOTCD: BIS #340, %PSR ;LOCK OUT FURTHER INTERRUPTS
2786 013060 032713 002000 BIT #2000, %CRS ;TEST ON-LINE TRANSITION BIT
2787 013064 001003 BNE NOTCD1 ;BRANCH IF SET
2788 013066 104000 HLT ;NO BITS SET TO CAUSE AN INTERRUPT
2789 013070 000167 177610 JMP LASTCK ;START NEXT CARD
2790 013074 104000 NOTCD1: HLT ;ON-LINE TRANSITION CAUSED AN INTERRUPT
2791 013076 000167 177602 JMP LASTCK ;START NEXT CARD
2792 013102 000000 DECK: 0 ;POINTER TO LITERAL "ALPHA" OR "BINARY"
2793 013104 000000 TSTART: 0 ;STARTING ADDRESS OF DATA TABLE
2794 013106 000000 TEND: 0 ;END ADDRESS OF DATA TABLE
2795 013110 000000 CDCNT: 0 ;NUMBER OF CARD BEING READ
2796 013112 000000 CLCNT: 0 ;NUMBER OF COLUMN BEING CHECKED
2797 013114 000000 DAT1: 0 ;DATA ON FIRST READ FROM CRB1
2798 013116 000000 DAT2: 0 ;DATA ON SECOND READ OF CRB1
2799 013120 000000 DATENC: 0 ;DATA READ FROM CRB2
2800 013122 000000 PTOFF: 0 ;OFFSET TO POINTER FOR DATA PRINTOUT
2801 013124 004767 002602 JSR %7, BELL ;RING BELL
2802 013130 032713 000400 BIT #400, %CRS ;CHECK OFF-LINE BIT
2803 013134 001001 BNE +4 ;BRANCH IF SET
2804 013136 104000 HLT ;OFF-LINE NOT SET, BUT SPECIAL CONDITION
2805 ;WAS SET AFTER 80 COLUMNS OF THE BOTH CARD WERE READ
2806 013140 032777 000040 165754 BIT #40, %SWR ;CHECK %SRPTR FOR HALT AT END OF DECK
2807 013146 001403 BEQ ALCNT ;CONTINUE IF NOT SET

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2808	013150	000000				HALT			:END OF DECK, SMS SET
2809	013152	000167	177570			JMP	DECKCK		:CHECK FOR TYPE OF TESTING
2810	013156	032777	002000	165736	ALCNT:	BIT	#2000, @SWR		:DOES THIS CR11 USE THE M829 MODULE
2811	013164	001025				BNE	ALCNT1		:YES- BRANCH
2812	013166	005027	000000			CLR	#0		:NO-STALL TO ALLOW CARD DONE TO SET
2813	013172	005367	177772			DEC	.-2		
2814	013176	001375				BNE	.-4		
2815	013200	005327	000000			DEC	#0		
2816	013204	001375				BNE	.-4		
2817	013206	005327	000000			DEC	#0		
2818	013212	001375				BNE	.-4		
2819	013214	032713	040000			BIT	#40000, @CRS		:CHECK CARD DONE
2820	013220	001001				BNE	.-4		
2821	013222	104000				HLT			:CARD DONE DIDN'T SET- THIS ERROR COULD BE
2822	013224	005013				CLR	@CRS		:CAUSED BY RUNNING A CR11 WHICH HAS THE
2823									:M829 MODULE AND NOT SETTING SWITCH REGISTER
2824									:SWITCH 10
2825									
2826	013226	032713	157377			BIT	#157377, @CRS		:ONLY BIT 8 & 13 MAY STILL BE SET
2827	013232	001401				BEQ	.-4		:BRANCH IF OK
2828	013234	104000				HLT			:STATUS REGISTER INCORRECT
2829	013236	000405				BR	ALCNT2		
2830	013240	005013			ALCNT1:	CLR	@CRS		:CLEAR ERROR
2831	013242	032713	156377			BIT	#156377, @CRS		:ONLY BITS 8 AND 9 & 13 MAY STILL BE SET
2832									:BIT 9 MAY BE SET SINCE CARD MAY NOT
2833									:YET HAVE CLEARED THE READER TO CAUSE
2834									:CARD DONE
2835	013246	001401				BEQ	.-4		
2836	013250	104000				HLT			:STATUS REGISTER INCORRECT
2837	013252	052767	000340	164516	ALCNT2:	BIS	#340, PSR		:SET PROCESSOR TO LEVEL 7
2838	013260	016760	164512	000002		MOV	PSR, 2(ADINT)		:SETUP RETURN STATUS
2839	013266	105213				INCB	@CRS		:ATTEMPT TO READ- SHOULD RESET ERROR
2840	013270	005713				TST	@CRS		:CHECK BIT 15
2841	013272	100402				BMI	ALLOK		:BRANCH IF OK
2842	013274	104000				HLT			:SETTING READ DIDN'T RESET ERROR
2843	013276	000416				BR	ALWAIT		:BRANCH TO WAIT FOR ON-LINE
2844	013300	012710	013332		ALLOK:	MOV	#SRVC1, @ADINT		:LOAD INTERRUPT RETURN ADDRESS
2845	013304	005067	164466			CLR	PSR		:SET PROCESSOR TO LEVEL 0
2846	013310	012713	000101			MOV	#101, @CRS		:ENABLE INTERRUPTS, KEEP ERROR SET BY SETTING READ
2847	013314	000240				NOP			:CLOCK IN INTERRUPT
2848	013316	016067	000002	164452		MOV	2(ADINT), PSR		:SET PROCESSOR TO LEVEL 7
2849	013324	005013				CLR	@CRS		:CLEAR INTERRUPT ENABLE AND ERROR
2850	013326	104000				HLT			:BIT 15 DIDN'T CAUSE AN INTERRUPT
2851	013330	000402				BR	.-6		
2852	013332	022626			SRVC1:	CMP	(SP)+, (SP)+		:RESTORE STACK POINTER
2853	013334	005013			ALWAIT:	CLR	@CRS		:CLEAR INTERRUPT ENABLE AND ERROR
2854	013336	012710	013374			MOV	#SRVC2, @ADINT		:CHANGE INTERRUPT RETURN ADDRESS
2855	013342	112713	000100			MOV	#100, @CRS		:ENABLE INTERRUPTS
2856	013346	042767	000340	164422		BIC	#340, PSR		:SET PROCESSOR TO LEVEL 0
2857	013354	032713	000400			BIT	#400, @CRS		:CHECK OFF-LINE BIT
2858	013360	001375				BNE	.-4		:LOOP UNTIL CLEAR
2859	013362	016067	000002	164406		MOV	2(ADINT), PSR		:SET PROCESSOR TO LEVEL 7
2860	013370	104000				HLT			:NO INTERRUPT OCCURRED
2861	013372	000403				BR	SRVC2A		:BRANCH AROUND
2862	013374	004767	002332		SRVC2:	JSR	X7 BELL		:RING BELL
2863	013400	022626				CMP	(SP)+, (SP)+		:RESTORE STACK POINTER

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2864 013402 032713 002000 SRVC2A: BIT      #2000, @CRS      ;CHECK BIT 10
2865 013406 001001          BNE          .+4          ;BRANCH IF SET
2866 013410 104000          HLT          ;BIT 10 NOT SET
2867 013412 032713 000400          BIT      #400, @CRS      ;CHECK BIT 8
2868 013416 001401          BEQ          .+4          ;BRANCH IF NOT SET
2869 013420 104000          HLT          ;BIT 8 WAS SET
2870 013422 005013          CLR          @CRS        ;DATO TO CRS
2871 013424 032713 002000          BIT      #2000, @CRS      ;CHECK BIT 10
2872 013430 001401          BEQ          .+4          ;BRANCH IF NOT SET
2873 013432 104000          HLT          ;DATO DIDN'T CLEAR ON-LINE BIT
2874 013434 022626          CMP      (SP)+, (SP)+    ;RESTORE STACK FROM INITIAL INTERRUPT
2875 013436 000167 177304          JNP      DECKCK         ;RESTART
2876
2877 013442 005067 165476          ERCR11: CLR      FLAG
2878 013446 000403          BR      TSTA
2879 013450 012767 000001 165466          ERCM11: MOV     #1, FLAG
2880 013456 012702 024203          TSTA:  MOV     @SUBT2, R2
2881 013462 004767 002740          JSR     PC, TOUT
2882 013466 004767 171370          JSR     %7, SETUP
2883 013472 012767 013502 002724          MOV     @TESTA+2, RETURN ;INITIALIZE REGISTERS
2884
2885 013500 104001          ;THE CARD READER GOING OFF-LINE SHOULD SET SPECIAL CONDITION (BIT 15) AND OFF-LINE (BIT
2886 013502 005067 002712          TESTA: SCOPE
2887 013506 004767 002172          CLR      ITMAX          ;RUN EACH ERROR TEST ONCE ONLY
2888 013512 012702 022070          JSR     %7, INIT        ;INITIALIZE STATUS REGISTER
2889 013516 005767 165422          MOV     @MSG3, R2       ;"PRESS CARD READER 'READ STOP'"
2890 013522 001402          TST     FLAG           ;CHANGE MESSAGE FOR DOCUMENTATION READER
2891 013524 012702 022130          BEQ     .+6            ;NO
2892 013530 004767 002672          MOV     @MSG3A, R2      ;"PRESS CARD READER 'STOP'"
2893 013534 012702 022023          JSR     %7, TOUT
2894 013540 004767 002662          MOV     @MSG2, R2
2895 013544 004767 003000          JSR     %7, TOUT
2896 013550 000000          JSR     %7, CRLF4
2897 013552 032713 000400          HALT
2898 013556 001001          BIT      #400, @CRS      ;CHECK BIT 8
2899 013560 104000          BNE     .+4            ;BRANCH IF SET
2900 013562 005713          HLT          ;OFF-LINE (BIT 8) WASN'T SET
2901 013564 100401          TST     @CRS           ;CHECK BIT 15
2902 013566 104000          BMI     .+4            ;BRANCH IF SET
2903 013570 012702 021704          HLT          ;BIT 15 WASN'T SET
2904 013574 005767 165344          MOV     @MSG1, R2       ;"PRESS CARD READER 'MOTOR START' AND 'READ START'";
2905 013600 001402          TST     FLAG           ;CHANGE MESSAGE FOR DOCUMENTATION READER
2906 013602 012702 021767          BEQ     .+6            ;NO
2907 013606 004767 002614          MOV     @MSG1A, R2      ;"PRESS CARD READER 'RESET'"
2908 013612 012702 022023          JSR     %7, TOUT
2909 013616 004767 002604          MOV     @MSG2, R2
2910 013622 004767 002722          JSR     %7, TOUT
2911 013626 000000          JSR     %7, CRLF4
2912 013630 032713 000400          HALT
2913 013634 001375          BIT      #400, @CRS      ;WAIT FOR OFF-LINE TO CLEAR
2914
2915          BNE     .-4
2916          ; INPUT HOPPER EMPTY SHOULD SET SPECIAL CONDITION
2917          TESTB: SCOPE
2918          JSR     %7, INIT        ;INITIALIZE STATUS REGISTER
2919          MOV     @MSG5, R2       ;"REMOVE ALL CARDS FROM THE INPUT HOPPER"
2919          JSR     %7, TOUT

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2920 013654 012702 022023      MOV      @MSG2,R2      ;"THEN HIT 'CONTINUE' ON THE CONSOLE"
2921 013660 004767 002542      JSR      X7,TOUT
2922 013664 004767 002660      JSR      X7,CRLF4     ;MOVE MESSAGE UP ON TTY
2923 013670 000000          HALT
2924 013672 032713 000400      BIT      @400,@CRS    ;CHECK BIT 8
2925 013676 001001          BNE      .+4          ;BRANCH IF SET
2926 013700 104000          HLT
2927 013702 005713          TST      @CRS         ;OFF-LINE (BIT 8) WASN'T SET
2928 013704 100401          BMI     .+4          ;CHECK SPECIAL CONDITION BIT
2929 013706 104000          HLT
2930 013710 012702 022267      MOV      @MSG6,R2     ;"RESTORE CARDS IN INPUT HOPPER"
2931 013714 004767 002506      JSR      X7,TOUT
2932 013720 012702 021704      MOV      @MSG1,R2
2933 013724 005767 165214      TST      FLAG        ;"PRESS CARD READER 'MOTOR START' AND 'READ START'"
2934 013730 001402          BEQ      .+6          ;CHANGE MESSAGE FOR DOCUMENTATION READER
2935 013732 012702 021767      MOV      @MSG1A,R2    ;NO
2936 013736 004767 002464      JSR      X7,TOUT     ;"PRESS CARD READER 'RESET'"
2937 013742 012702 022023      MOV      @MSG2,R2
2938 013746 004767 002454      JSR      X7,TOUT     ;"THEN HIT 'CONTINUE' ON THE CONSOLE"
2939 013752 004767 002572      JSR      X7,CRLF4     ;MOVE MESSAGE UP ON TTY
2940 013756 000000          HALT
2941 013760 032713 000400      BIT      @400,@CRS    ;WAIT FOR OFF-LINE TO CLEAR
2942 013764 001375          BNE      .-4
;OUTPUT STACKER FULL SHOULD SET BIT 15
2943 013766 104001          TESTC: SCOPE
2944 013770 004767 001710      JSR      X7,INIT      ;INITIALIZE STATUS REGISTER
2945 013774 012702 022333      MOV      @MSG7,R2     ;"RAISE OUTPUT STACKER PRESSURE ARM ABOVE HORIZONTAL THE
2946 014000 005767 165140      TST      FLAG        ;CHANGE MESSAGE FOR DOCUMENTATION READER
2947 014004 001402          BEQ      .+6          ;NO
2948 014006 012702 022451      MOV      @MSG7A,R2    ;"LOWER OUTPUT STACKER PLATE TO BOTTOM"
2949 014012 004767 002410      JSR      X7,TOUT
2950 014016 012702 022023      MOV      @MSG2,R2     ;"THEN HIT 'CONTINUE' ON THE CONSOLE"
2951 014022 004767 002400      JSR      X7,TOUT
2952 014026 004767 002516      JSR      X7,CRLF4     ;MOVE MESSAGE UP ON TTY
2953 014032 000000          HALT
2954 014034 032713 000400      BIT      @400,@CRS    ;CHECK BIT 8
2955 014040 001001          BNE      .+4          ;BRANCH IF SET
2956 014042 104000          HLT
2957 014044 005713          TST      @CRS         ;OFF-LINE (BIT 8) WASN'T SET
2958 014046 100401          BMI     .+4          ;CHECK SPECIAL CONDITION BIT
2959 014050 104000          HLT
2960 014052 012702 021704      MOV      @MSG1,R2     ;SPECIAL CONDITION NOT SET
2961 014056 005767 165062      TST      FLAG        ;"PRESS CARD READER 'MOTOR START' AND 'READ START'"
2962 014062 001402          BEQ      .+6          ;CHANGE MESSAGE FOR DOCUMENTATION READER
2963 014064 012702 021767      MOV      @MSG1A,R2    ;NO
2964 014070 004767 002332      JSR      X7,TOUT     ;"PRESS CARD READER 'RESET'"
2965 014074 012702 022023      MOV      @MSG2,R2
2966 014100 004767 002322      JSR      X7,TOUT     ;"THEN HIT 'CONTINUE' ON THE CONSOLE"
2967 014104 004767 002440      JSR      X7,CRLF4     ;MOVE MESSAGE UP ON TTY
2968 014110 000000          HALT
2969 014112 032713 000400      BIT      @400,@CRS    ;WAIT FOR OFF-LINE TO CLEAR
2970 014116 001375          BNE      .-4
;A FEED ERROR SHOULD SET BIT 15
;THIS ERROR OCCURS WHEN THE FEED MECHANISM FAILS TO DELIVER A CARD TO THE READ STATION
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30076	014120	104001		TESTD:	SCOPE	
30077	014122	004767	001556		JSR	X7, INIT
30078	014126	012702	022216		MOV	#MSG5, R2
30079	014130	004767	002270		JSR	X7, TOUT
30080	014136	012702	022023		MOV	#MSG2, R2
30081	014140	004767	002260		JSR	X7, TOUT
30082	014146	012702	022520		MOV	#MSG8, R2
30083	014150	005767	164766		TST	FLAG
30084	014156	001402			BEQ	.+6
30085	014160	012702	022611		MOV	#MSG8A, R2
30086	014164	004767	002236		JSR	X7, TOUT
30087	014170	012702	021704		MOV	#MSG1, R2
30088	014174	005767	164744		TST	FLAG
30089	014200	001402			BEQ	.+6
30090	014202	012702	021767		MOV	#MSG1A, R2
30091	014206	004767	002214		JSR	X7, TOUT
30092	014212	004767	002332		JSR	X7, CRLF4
30093	014216	000000			HALT	
30094	014220	032713	002000		BIT	#2000, @CRS
30095	014224	001775			BEQ	.+4
30096	014226	004767	001452		JSR	X7, INIT
30097	014230	012713	000003		MOV	#3, @CRS
30098	014236	005227	000000		INC	#0, T
30099	014240	001375			BNE	#0, T
30100	014244	005227	000000		INC	#0, T
30101	014250	001375			BNE	#0, T
30102	014252	005227	000000		INC	#0, T
30103	014256	001375			BNE	#0, T
30104	014260	005227	000000		INC	#0, T
30105	014264	001375			BNE	#0, T
30106	014266	032713	000400		BIT	#400, @CRS
30107	014272	001001			BNE	.+4
30108	014274	104000			HLT	
30109	014276	005713			TST	@CRS
30110	014300	100401			BMI	.+4
30111	014302	104000			HLT	
30112	014304	012702	022267		MOV	#MSG6, R2
30113	014310	004767	002112		JSR	X7, TOUT
30114	014314	012702	021704		MOV	#MSG1, R2
30115	014320	005767	164620		TST	FLAG
30116	014324	001402			BEQ	.+6
30117	014326	012702	021767		MOV	#MSG1A, R2
30118	014332	004767	002070		JSR	X7, TOUT
30119	014336	012702	022023		MOV	#MSG2, R2
30120	014342	004767	002060		JSR	X7, TOUT
30121	014346	004767	002176		JSR	X7, CRLF4
30122	014352	000000			HALT	
30123	014354	032713	000400		BIT	#400, @CRS
30124	014360	001375			BNE	.+4
30125	014362	005767	164556		TST	FLAG
30126	014366	001402			BEQ	.+6
30127	014370	000167	000314		JMP	TESTG
30128						
30129						
30130						
30131	014374	104001				

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; "REMOVE ALL CARDS FROM THE INPUT HOPPER"
; "THEN HIT 'CONTINUE' ON THE CONSOLE"
; "HOLD DOWN THE SWITCH AT THE BOTTOM OF INPUT HOPPER
; CHANGE MESSAGE FOR DOCUMENTATION READER
; NO
; "LIFT SWITCH UNDER RIFFLE CAP
; "PRESS CARD READER 'MOTOR START' AND 'READ START'
; CHANGE MESSAGE FOR DOCUMENTATION READER
; NO
; "PRESS CARD READER 'RESET'"
; MOVE MESSAGE UP ON TTY
; WAIT FOR CARD READER TO COME ON-LINE
; INITIALIZE STATUS REGISTER
; SET EJECT AND READ
; WAIT AMHILE
; TEST OFF-LINE BIT
; BRANCH IF SET
; BIT 8 WAS NOT SET
; CHECK BIT 15
; BRANCH IF SET
; BIT 15 WAS NOT SET
; "RESTORE CARDS IN THE INPUT HOPPER"
; "PRESS CARD READER 'MOTOR START' AND 'READ START'"
; CHANGE MESSAGE FOR DOCUMENTATION READER
; NO
; "PRESS CARD READER 'RESET'"
; "THEN HIT 'CONTINUE' ON THE CONSOLE"
; MOVE MESSAGE UP ON TTY
; WAIT FOR OFF-LINE TO CLEAR
; SKIP NEXT TEST IF DOCUMENTATION READER

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: A NOTION ERROR SHOULD SET BIT 15  
: THIS ERROR OCCURS WHEN A CARD JAM OCCURS AT THE READ STATION  
TESTE: SCOPE

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3032 014376 004767 001302 JSR X7,INIT ;INITIALIZE STATUS REGISTER
3033 014402 012702 022070 MOV #MSG3,R2 ;"PRESS CARD READER 'READ STOP'"
3034 014406 004767 002014 JSR X7,TOUT ;"THEN HIT 'CONTINUE' ON THE CONSOLE"
3035 014412 012702 022023 MOV #MSG2,R2 ;"BLOCK THE CARD READER STATION TO
3036 014416 004767 002004 JSR X7,TOUT ;PREVENT A CARD GOING THRU, AND"
3037 014422 012702 022650 MOV #MSG9,R2 ;"PRESS CARD READER 'MOTOR START' AND 'READ START'"
3038 014426 004767 001774 JSR X7,TOUT ;"PRESS CARD READER 'MOTOR START' AND 'READ START'"
3039 014432 012702 021704 MOV #MSG1,R2 ;"PRESS CARD READER 'MOTOR START' AND 'READ START'"
3040 014436 004767 001764 JSR X7,TOUT ;"PRESS CARD READER 'MOTOR START' AND 'READ START'"
3041 014442 004767 002102 JSR X7,CRLF4 ;MOVE MESSAGE UP ON TTY
3042 014446 000000 HALT
3043 014450 032713 002000 BIT #2000,ACRS ;MONITOR ON-LINE TRANSITION (BIT 10)
3044 014454 001775 BEQ .-4 ;CONTINUE WHEN CARD READER COMES ON-LINE
3045 014456 012713 000003 MOV #3,ACRS ;READ A CARD AND SET EJECT
3046 014462 032713 140000 BIT #140000,ACRS ;CHECK DONE AND SPECIAL CONDITION BITS
3047 014466 001775 BEQ .-4 ;WAIT
3048 014470 005713 TST ACRS ;CHECK SPECIAL CONDITION BIT
3049 014472 100401 BMI .+4 ;CONTINUE IF SET
3050 014474 104000 HLT ;SPECIAL CONDITION NOT SET
3051 014476 012702 022752 MOV #MSG10,R2 ;"REMOVE JAMMED CARD"
3052 014502 004767 001720 JSR X7,TOUT
3053 014506 012702 021704 MOV #MSG1,R2 ;"PRESS CARD READER 'MOTOR START' AND 'READ START'"
3054 014512 004767 001710 JSR X7,TOUT
3055 014516 012702 022023 MOV #MSG2,R2 ;"THEN HIT 'CONTINUE' ON THE CONSOLE"
3056 014522 004767 001700 JSR X7,TOUT
3057 014526 004767 002016 JSR X7,CRLF4 ;MOVE MESSAGE UP ON TTY
3058 014532 000000 HALT
3059 014534 032713 000400 BIT #400,ACRS ;WAIT FOR OFF-LINE TO CLEAR
3060 014540 001375 BNE .-4

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:A STACK FAIL ERROR SHOULD SET BIT 15  
:ERROR OCCURS WHEN 3 CARDS IN A ROW HAVE NOT BEEN DELIVERED PROPERLY TO THE OUTPUT STACK  
TESTF: SCOPE

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3064 014542 104001 JSR X7,INIT ;INITIALIZE STATUS REGISTER
3065 014544 004767 001134 MOV #MSG3,R2 ;"PRESS CARD READER 'READ STOP'"
3066 014550 012702 022070 JSR X7,TOUT ;"THEN HIT 'CONTINUE' ON THE CONSOLE"
3067 014554 004767 001646 MOV #MSG2,R2 ;"HOLD THE OUTPUT STACKER GATE OPEN. THEN"
3068 014560 012702 022023 JSR X7,TOUT ;"HOLD THE OUTPUT STACKER GATE OPEN. THEN"
3069 014564 004767 001636 MOV #MSG11,R2 ;"PRESS CARD READER 'MOTOR START' AND
3070 014570 012702 022777 JSR X7,TOUT ;"READ START,"
3071 014574 004767 071626 MOV #MSG1,R2 ;MOVE MESSAGE UP ON TTY
3072 014600 012702 021704 JSR X7,CRLF4 ;MOVE MESSAGE UP ON TTY
3073 014604 004767 001616 HALT
3074 014610 004767 001734 BIT #2000,ACRS ;WAIT FOR CARD READER TO COME ON-LINE
3075 014614 000000 BEQ .-4 ;INITIALIZE COUNTER TO READ 3 CARDS
3076 014616 032713 002000 MOV #3,COUNT ;EJECT A CARD
3077 014622 001775 MOV #3,ACRS ;WAIT FOR CARD DONE OR SPECIAL CONDITION
3078 014624 012701 000003 BIT #140000,ACRS ;COUNT DOWN
3079 014630 012713 000003 DEC COUNT ;READ 3 CARDS ALL TOGETHER
3080 014634 032713 140000 BNE LOOPF ;CHECK SPECIAL CONDITION BIT 15
3081 014640 001775 BEQ .-4 ;BRANCH IF SET
3082 014642 005301 DEC COUNT ;SPECIAL CONDITION NOT SET
3083 014644 001371 BNE LOOPF ;"PRESS CARD READER 'MOTOR START' AND 'READ START'"
3084 014646 005713 TST ACRS
3085 014650 100401 BMI .+4
3086 014652 104000 HLT
3087 014654 012702 021704 MOV #MSG1,R2

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3088 014660 004767 001542 JSR X7,TOUT
3089 014664 012702 022023 MOV #MSG2,R2 ;"THEN HIT 'CONTINUE' ON THE CONSOLE"
3090 014670 004767 001532 JSR X7,TOUT
3091 014674 004767 001650 JSR X7,CRLF4 ;MOVE MESSAGE UP ON TTY
3092 014700 000000 HALT
3093 014702 032713 000400 BIT #400,ACRS ;WAIT FOR OFF-LINE TO CLEAR
3094 014706 001375 BNE .-4
3095
3096
3097 ;DARK-LIGHT ERROR SHOULD SET BIT 15
3098 ;THIS OCCURS WHEN DATA IS SENSED BEFORE COLUMN ONE OR AFTER COLUMN EIGHTY
3099 ;OR WHEN THE SENSORS ARE NOT ALL SENSING A HOLE AFTER THE CARD HAS PASSED
3100 ;THIS TEST IS SKIPPED IF BIT 0 OF THE SWITCH REGISTER EQUALS ONE
3101 ;TO MAKE THE 2 DARK-LIGHT CHECK CARDS:
3102 ; 1. TEAR A SMALL PIECE FROM THE LEADING EDGE OF ONE CARD
3103 ; 2. TAPE 2 CARDS TOGETHER TO MAKE ONE "LONG" CARD-IT ONLY NEEDS TO BE
3104 ; ABOUT 1/2 INCH LONGER THAN A REGULAR CARD
3104 014710 104001 TESTG: SCOPE
3105 014712 032777 000001 164202 BIT #1,ASMR ;CHECK SMD
3106 014720 001410 BEQ CONTG ;RUN TEST IF NOT SET
3107 014722 004767 001004 JSR X7,BELL ;IF SET, RING BELL AND
3108 014726 000000 HALT ;HALT
3109 014730 012767 013502 001466 MOV #TESTA+2,RETURN ;SETUP SCOPE LOOP RETURN ADDRESS TO LOOP THRU TESTS
3110 014736 000167 176536 JMP TESTA ;START ERROR TESTS OVER ON CONTINUING
3111 014742 004767 000736 CONTG: JSR X7,INIT ;INITIALIZE STATUS REGISTER
3112 014746 005001 CLR COUNT ;INITIALIZE COUNTER
3113 014750 005201 INC COUNT ;SET TO INDICATE FIRST PASS
3114 014752 012702 023051 MOV #MSG12,R2 ;"PLACE SPECIAL DARK-LIGHT CHECK CARDS (SEE LISTING, TES
3115 014756 004767 001444 JSR X7,TOUT ;AT THE BOTTOM OF THE INPUT STACK"
3116 014762 012702 021704 LOOPG: MOV #MSG1,R2 ;"PRESS CARD READER 'MOTOR START' AND 'READ START'"
3117 014766 005767 164152 TST FLAG ;CHANGE MESSAGE FOR DOCUMENTATION READER
3118 014772 001402 BEQ .+6 ;NO
3119 014774 012702 021767 MOV #MSG1A,R2 ;"PRESS CARD READER 'RESET'"
3120 015000 004767 001422 JSR X7,TOUT
3121 015004 012702 022023 MOV #MSG2,R2
3122 015010 004767 001412 JSR X7,TOUT ;"THEN HIT 'CONTINUE' ON THE CONSOLE"
3123 015014 004767 001530 JSR X7,CRLF4 ;MOVE MESSAGE UP ON TTY
3124 015020 000000 HALT
3125 015022 032713 000400 BIT #400,ACRS ;WAIT FOR OFF-LINE TO CLEAR
3126 015026 001375 BNE .-4
3127 015030 012713 000003 MOV #3,ACRS ;EJECT THE CARD
3128 015034 032713 140000 BIT #140000,ACRS ;WAIT FOR ERROR OR CARD DONE
3129 015040 001775 BEQ .-4
3130 015042 005713 TST ACRS ;CHECK SPECIAL CONDITION
3131 015044 100401 BMI .+4 ;CONTINUE IF SET
3132 015046 104000 HLT ;SPECIAL CONDITION NOT SET
3133 015050 005301 DEC COUNT ;COUNT DOWN
3134 015052 001743 BEQ LOOPG ;IF FIRST PASS, LOOP
3135 015054 004767 000652 JSR X7,BELL ;RING BELL
3136 015060 000000 HALT
3137 015062 012702 021704 MOV #MSG1,R2 ;"PRESS CARD READER 'MOTOR START' AND 'READ START'"
3138 015066 005767 164052 TST FLAG ;CHANGE MESSAGE FOR DOCUMENTATION READER
3139 015072 001402 BEQ .+6 ;NO
3140 015074 012702 021767 MOV #MSG1A,R2 ;"PRESS CARD READER 'RESET'"
3141 015100 004767 001322 JSR X7,TOUT
3142 015104 012702 022023 MOV #MSG2,R2 ;"THEN HIT 'CONTINUE' ON THE CONSOLE"
3143 015110 004767 001312 JSR X7,TOUT

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3144 015114 004767 001430      JSR      X7,CRLF4      ;MOVE MESSAGE UP ON TTY
3145 015120 000000                HALT
3146 015122 032713 000400      BIT      #400,BCRS     ;WAIT FOR OFF-LINE TO CLEAR
3147 015126 001375                BNE
3148 015130 012767 013502 001266  MOV      #TESTA+2,RETURN ;SETUP SCOPE LOOP RETURN ADDRESS
3149 015136 000167 176336      JMP      TESTA         ;LOOP THRU TEST ON CONTINUING
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3154 015142 012702 024236      ;ROUTINE TO LOOP THRU A SINGLE INSTRUCTION TEST
3155 015146 004767 001254      ;NOTE THAT SW11 MUST BE DOWN AFTER 2ND HALT
3156 015152 004767 167704      TESTX:  MOV      #SUBT4,R2
3157 015156 012702 024077      JSR      PC,TOUT
3158 015162 004767 001240      JSR      X7,SETUP     ;SETUP POINTERS AND FLAGS
3159 015166 104004                MOV      #STADD,R2
3160 015170 016767 163740 000062  JSR      PC,TOUT
3161 015176 062767 000002 000054  MOV      TMP1,RETRNX
3162 015204 032777 010000 163710 2S:  ADD      #2,RETRNX     ;CHANGE TO FIRST ADDRESS AFTER SCOPE INSTRUCTION
3163 015212 001404                BIT      #10000,BSHR  ;CHECK SW12
3164 015214 042767 000020 162554  BEQ      .+12         ;BRANCH IF NOT SET
3165 015222 000403                BIC      #20,PSR     ;CLEAR TRACE BIT
3166 015224 052767 000020 162544  BR       .+10         ;SKIP NEXT INSTRUCTION
3167 015232 005067 001164                BIS      #20,PSR     ;SET TRACE BIT
3168 015236 012767 015250 001160  CLR      ITCNT       ;CLEAR ITERATION COUNTER
3169 015244 000177 000010                MOV      #XLOOP,RETURN ;LOAD RETURN ADDRESS
3170 015250 005067 001146                JMP      @RETRNX     ;JUMP TO TEST
3171 015254 000177 000000      XLOOP:  CLR      ITCNT ;KEEP ITERATION COUNTER AT ZERO
3172 015260 000000                JMP      @RETRNX     ;JUMP TO TEST
RETRNX: 0

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3186 015262 012702 024261
3187 015266 004767 001134
3188 015272 004767 167564
3189 015276 012702 024050
3190 015302 004767 001120
3191 015306 104004
3192 015310 016767 163620 000364
3193 015316 042767 170000 000356
3194 015324 005067 000350
3195 015330 005067 000342
3196 015334 005067 163614
3197 015340 005067 175546
3198 015344 104003
3199 015346 032713 000400
3200 015352 001017
3201 015354 005213
3202 015356 005267 000316
3203 015362 105713
3204 015364 100426
3205 015366 032713 040000
3206 015372 001015
3207 015374 005713
3208 015376 100371
3209 015400 032713 000400
3210 015404 001002
3211 015406 104000
3212 015410 000753
3213
3214 015412 004767 000314
3215 015416 032713 000400
3216 015422 001375
3217 015424 000745
3218 015426 022767 000120 175456
3219 015434 001741
3220 015436 104000
3221 015440 000737
3222 015442 011467 175446
3223 015446 005267 175440
3224 015452 105713
3225 015454 100002
3226 015456 104000
3227 015460 000727
3228 015462 012701 000200
    
```

```

:ROUTINE TO CHECK CARDS WHICH HAVE ALL COLUMNS IDENTICALLY PUNCHED.
:THIS ROUTINE ALLOWS SPECIFIC TYPES OF DATA FAILURES TO BE STUDIED
:EASILY. THE PATTERN IS STORED, AND THEN
:EACH COLUMN OF EACH CARD IS READ TWICE AND COMPARED WITH IT. IF A
:DISCREPANCY OCCURS, THE ERROR IS PRINTED OUT ALONG WITH THE TOTAL
:NUMBER OF CARDS READ AND THE TOTAL NUMBER OF DATA ERRORS DISCOVERED
:UP TO THAT POINT (ALL PRINTOUTS ARE IN OCTAL). WHEN THE INPUT HOPPER
:IS EMPTY, THE ROUTINE RINGS THE BELL AND WAITS FOR MORE CARDS TO BE
:LOADED AND THE CARD READER TO BE PUT BACK ON-LINE.
:SW15=1 CAUSES A HALT AFTER AN ERROR, AND SW13=1 INHIBITS ERROR PRINTOUTS.
    
```

```

CKSAME: MOV #SUBTS,R2
        JSR PC,TOUT
        JSR X7,SETUP ;INITIALIZE POINTERS
        MOV #CIMPAT,R2
        JSR PC,TOUT
        READC
        MOV TMP1,CARDIN
        BIC #170000,CARDIN ;CLEAR UPPER BITS OF PATTERN
        CLR TOTCRD ;INITIALIZE CARD COUNT
        CLR TOTERR ;INITIALIZE ERROR COUNT
        CLR ERFLG ;CLEAR FLAG FOR PRINTING ERROR HEADING
        CLR CLCNT ;INITIALIZE COLUMN COUNT
CKLOOP: CLR KBINTT
        BIT #400,ACRS ;CHECK BIT 8
        BNE CKSIT ;BRANCH IF SET TO WAIT FOR READER TO COME ON-LINE.
        INC ACRS ;START READING CARD
        INC TOTCRD ;INCREMENT CARD COUNT
CKLP1: TSTB ACRS ;CHECK COLUMN READY
        BMI CKCOL ;BRANCH IF SET
        BIT #40000,ACRS ;CHECK CARD DONE
        BNE CKCRD ;BRANCH IF SET
        TST ACRS ;CHECK SPECIAL CONDITION
        BPL CKLP1 ;LOOP IF NOT SET
        BIT #400,ACRS ;CHECK BIT 8
        BNE CKSIT ;BRANCH IF SET TO WAIT FOR READER ON-LINE.
        BR CKLOOP ;SPECIAL CONDITION SET, BIT 8 CLEAR
CKSIT: JSR X7,BELL ;RING BELL TO SIGNIFY READER OFF-LINE
CKSIT1: BIT #400,ACRS ;CHECK BIT 8
        BNE CKSIT1 ;LOOP IF STILL SET
        BR CKLOOP ;START NEXT CARD
CKCRD: CMP #80,CLCNT ;CHECK FOR 80 COLUMNS READ
        BEQ CKLOOP ;START NEXT CARD IF OK
        HLT ;FINAL COLUMN COUNT WASN'T 80
        BR CKLOOP ;START NEXT CARD
CKCOL: MOV ACRB1,DAT1 ;READ DATA BUFFER
        INC CLCNT ;COUNT COLUMNS
        TSTB ACRS ;CHECK COLUMN READY
        BPL .+6 ;BRANCH IF OK
        HLT ;READING DAB DIDN'T CLEAR READY
        BR CKLOOP ;START NEXT CARD AFTER ERROR
        MOV #200,COUNT ;WAIT AWHILE
    
```

```

3229 015466 005301          CKLP2: DEC      COUNT
3230 015470 001376          BNE      CKLP2
3231 015472 011467 175420    MOV      @CRB1, DAT2      ; READ CRB1 AGAIN
3232 015476 026767 175412 000176  CMP      DAT1, CARDIM    ; COMPARE FIRST DATA TO PATTERN
3233 015504 001005          BNE      CKFAIL          ; BRANCH IF FAILURE
3234 015506 026767 175404 000166  CMP      DAT2, CARDIM    ; COMPARE SECOND READING TO PATTERN
3235 015514 001001          BNE      CKFAIL          ; BRANCH IF FAILURE
3236 015516 000721          BR       CKLP1           ; WAIT FOR NEXT COLUMN OR END OF CARD
3237 015520 005267 000152    CKFAIL: INC      TOTERR  ; COUNT ERRORS
3238 015524 104003          KBINTT
3239 015526 032777 020000 163366  BIT      #20000, @SWR    ; CHECK FOR INHIBITING PRINTOUT
3240 015534 001047          BNE      CKHLT           ; BRANCH AROUND PRINTOUT IF SET
3241 015536 005767 163412    TST      ERFLG           ; TEST FLAG TO PRINT HEADING
3242 015542 001006          BNE      CKNOHD          ; BRANCH IF ALREADY DONE
3243 015544 005267 163404    INC      ERFLG           ; PRINT HEADING ONCE ONLY
3244 015550 012702 023444    MOV      @MSG19, R2      ; OUTPUT HEADING
3245 015554 004767 000646    JSR      X7, TOUT
3246 015560 004767 000732    CKNOHD: JSR      X7, CRLF  ; OUTPUT CARRIAGE RETURN, LINEFEED
3247 015564 016702 175322    MOV      CLCNT, R2      ; PRINT COLUMN NUMBER
3248 015570 004767 000414    JSR      X7, PROCT
3249 015574 004767 000212    JSR      X7, SPACE
3250 015600 016702 175310    MOV      DAT1, R2      ; PRINT FIRST READING
3251 015604 004767 000400    JSR      X7, PROCT
3252 015610 004767 000176    JSR      X7, SPACE
3253 015614 016702 175276    MOV      DAT2, R2      ; PRINT SECOND READING
3254 015620 004767 000364    JSR      X7, PROCT
3255 015624 004767 000162    JSR      X7, SPACE
3256 015630 016702 000044    MOV      TOTCRD, R2    ; PRINT TOTAL NUMBER OF CARDS READ
3257 015634 004767 000350    JSR      X7, PROCT
3258 015640 004767 000146    JSR      X7, SPACE
3259 015644 016702 000026    MOV      TOTERR, R2    ; PRINT TOTAL NUMBER OF DATA ERRORS
3260 015650 004767 000334    JSR      X7, PROCT
3261 015654 005777 163242    CKHLT: TST      @SWR    ; CHECK SW15 TO HALT ON ERROR
3262 015660 100002          BPL      CKDONE         ; BRANCH IF NOT SET
3263 015662 000000          HALT
3264 015664 000625          BR       CKLOOP         ; CONTINUE
3265 015666 032713 140000    CKDONE: BIT      #140000, @CRS ; WAIT FOR SPECIAL CONDITION OR DONE
3266 015672 001775          BEQ      CKDONE
3267 015674 000621          BR       CKLOOP
3268 015676 000000    TOTERR: 0
3269 015700 000000    TOTCRD: 0
3270 015702 000000    CARDIM: 0
3271
3272
3273          ; ISSUE MESSAGE IF CARD READER IS OFF-LINE
3274          ; WAIT FOR BUSY TO CLEAR IN CASE CARD READER IS STILL READING A CARD
3275          ; INITIALIZE STATUS REGISTER AND USE ERROR HALT IF IT DOESN'T CLEAR PROPERLY
3276          ; NOTE THAT PROGRAM WILL HANG HERE IF BUSY REMAINS SET
3277 015704 004767 000046    INIT: JSR      X7, CKBIT8 ; SEE IF OFF-LINE BIT IS SET
3278 015710 032713 001000    BIT      #1000, @CRS    ; WAIT FOR BUSY TO CLEAR, IN CASE
3279 015714 001375          BNE      .-4            ; A CARD IS STILL BEING READ
3280 015716 005013          CLR      @CRS           ; INITIALIZE STATUS REGISTER
3281 015720 005714          TST      @CRB1         ; READ DATA BUFFER TO CLEAR COLUMN READY
3282 015722 005713          TST      @CRS           ; MAKE SURE INITIALIZATION OK
3283 015724 001401          BEQ      .+4            ; BRANCH IF ALL BITS ZERO
3284 015726 104000          HLT                    ; NOT ALL BITS OF STATUS REGISTER ARE ZERO

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3285 015730 000207          RTS      X7          ;RETURN
3286
3287          ;BELL ON PASS COMPLETE
3288 015732 105777 163172  BELL:  TSTB   @TCSR          ;WAIT FOR TTY READY
3289 015736 100375          BPL     -4
3290 015740 012777 000207 163164  MOV     @207,@TDBR        ;RING BELL
3291 015746 012767 000001 000444  MOV     @1,@ITMAX        ;MAKE CERTAIN ITERATION MAXIMUM IS CORRECT
3292 015754 000207          RTS      X7          ;RETURN
3293
3294          ;SUBROUTINE TO CHECK FOR BIT B (OFF-LINE) BEING SET IN CARD
3295          ;READER CSR, AND PRINT OUT A MESSAGE IF IT IS
3296 015756 032713 000400  CKBITB: BIT     @400,@CRS    ;CHECK BIT B
3297 015762 001001          BNE     +4             ;BRANCH IF SET
3298 015764 000207          RTS      X7             ;RETURN IF NOT SET
3299 015766 012702 023424  MOV     @MSG18,R2        ;OUTPUT MESSAGE
3300 015772 004767 000430  JSR     X7,TOUT          ;"BIT B WAS SET"
3301 015776 012702 023341  MOV     @MSG17,R2        ;"REMEDY THE ERROR CONDITION
3302 016002 004767 000420  JSR     X7,TOUT          ;AND PRESS 'CONTINUE'"
3303 016006 000000          HALT
3304 016010 000762          BR      CKBITB         ;CHECK AGAIN
3305
3306          ;SUBROUTINE TO ISSUE N SPACES
3307          ;N IS ONE PLUS VALUE CONTAINED IN SPACEX
3308          ;SPACEX IS CLEARED WITHIN THE SUBROUTINE, SO THAT A CALL ON
3309          ;SPACE WITHOUT LOADING SPACEX ISSUES ONLY ONE SPACE
3310 016012 105777 163112  SPACE: TSTB   @TCSR          ;WAIT FOR TTY READY
3311 016016 100375          BPL     -4
3312 016020 012777 000240 163104  MOV     @240,@TDBR        ;OUTPUT A SPACE
3313 016026 005367 000010  DEC     SPACEX          ;DECREMENT COUNT
3314 016032 100367          BPL     SPACE          ;LOOP IF NOT DONE
3315 016034 005067 000002  CLR     SPACEX          ;RESET COUNT TO ZERO
3316 016040 000207          RTS      X7          ;RETURN
3317 016042 000000  SPACEX: 0
3318
3319
3320
3321
3322          ;ENTERED WITH SYSTEM TRAP CALL (HLT)
3323          ;PRINT OUT THE ERROR PC AND STATUS REGISTER
3324 016044 104003          PRINT: KBINTT
3325 016046 037727 163050 020000  BIT     @SWR, @20000    ;TEST FOR INHIBIT PRINT OUT
3326 016054 001401          BEQ     +4             ;BRANCH TO PRINT
3327 016056 000441          BR      @.CK          ;INHIBIT, CHECK FOR HALT
3328 016060 012667 000120  MOV     (6)+, SAVPC      ;PC OF FAILING ROUTINE
3329 016064 012667 000116  MOV     (6)+, SAVPSR     ;PSR OR ERROR CONDITION
3330 016070 024646          CMP     -(6), -(6)     ;RESTORE STACK
3331 016072 004767 000420  JSR     X7,CRLF         ;OUTPUT CARRIAGE RETURN, LINEFEED
3332 016076 010267 000074  MOV     X2, SAVR2       ;SAVE R2
3333 016102 016702 000076  MOV     SAVPC, X2
3334 016106 162702 000002  SUB     @2,R2           ;UPDATE ADDRESS POINTER
3335 016112 004767 000072  JSR     X7,PROCT        ;PRINT PC IN OCTAL
3336 016116 105777 163006  TSTB   @TCSR          ;WAIT FOR TTY READY
3337 016122 100375          BPL     -4
3338 016124 012777 000240 163000  MOV     @240,@TDBR        ;OUTPUT A SPACE
3339 016132 016702 000050  MOV     SAVPSR, X2
3340 016136 004767 000046  JSR     X7,PROCT        ;PRINT PROCESSOR STATUS AT TIME OF FAILURE

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3341 016142 016702 000030      MOV      SAVR2, %2      ;RESTORE REGISTER 2
3342 016146 105777 162756      TSTB    @TCSR          ;WAIT FOR TTY READY
3343 016152 100375                BPL     .-4
3344 016154 012777 000240 162750      MOV     @240,@TDBR
3345 016162 005777 162734      B.CK:   TST     @SWR          ;CHECK @SRPTR FOR HALT SWITCH
3346 016166 100001                BPL     .+4            ;BRANCH IF NOT SET
3347 016170 000000                HALT
3348 016172 104003                KBINTT
3349 016174 000002                RTI                    ;RETURN TO MAIN LINE
3350 016176 000000      SAVR2:  0
3351 016200 000000      SAVR3:  0
3352 016202 000000      SAVR4:  0
3353 016204 000000      SAVPC:  0
3354 016206 000000      SAVPSR: 0
3355
3356 016210 010367 177764      PROCT:  MOV     %3,SAVR3    ;SAVE R3
3357 016214 010467 177762      MOV     %4,SAVR4    ;SAVE R4
3358 016220 005004                CLR     %4            ;CLEAR R4 TO USE AS COUNTER
3359 016222 005001                CLR     COUNT        ;CLEAR COUNT TO USE AS CARRY FLAG
3360 016224 012703 000260      MOV     @260,%3     ;SETUP ASCII ZERO IN R3
3361 016230 005702                TST     %2            ;CHECK BIT 15 OF DESIRED NUMBER
3362 016232 100001                BPL     .+4            ;BRANCH IF NOT SET
3363 016234 005203                INC     %3            ;CHANGE TO ASCII ONE
3364 016236 006102                ROL     %2            ;ROTATE INTO RIGHTMOST BIT
3365 016240 006102                ROL     %2            ;TO PREPARE FOR LOOP
3366 016242 005501                ADC     COUNT        ;STORE CARRY
3367 016244 105777 162660      C.WAIT: TSTB    @TCSR          ;WAIT FOR TTY READY
3368 016250 100375                BPL     C.WAIT
3369 016252 010377 162654      MOV     %3,@TDBR    ;OUTPUT ASCII
3370 016256 005204                INC     %4            ;COUNT CHARACTERS OUTPUT
3371 016260 020427 000006      CMP     %4,%6        ;CHECK FOR DONE
3372 016264 001005                BNE     C.CONT       ;BRANCH IF NOT DONE
3373 016266 016703 177706      MOV     SAVR3,%3     ;RESTORE REGISTER 3
3374 016272 016704 177704      MOV     SAVR4,%4     ;RESTORE REGISTER 4
3375 016276 000207                RTS
3376 016300 000241      C.CONT: CLC                    ;CLEAR CARRY
3377 016302 005701                TST     COUNT        ;TEST CARRY FLAG
3378 016304 001402                BEQ     .+6            ;BRANCH IF NOT SET
3379 016306 005001                CLR     COUNT        ;CLEAR FLAG
3380 016310 000261                SEC
3381 016312 006102                ROL     %2            ;SET CARRY
3382 016314 006102                ROL     %2            ;ROTATE NEXT 3 BITS INTO RIGHTMOST 3
3383 016316 006102                ROL     %2
3384 016320 005501                ADC     COUNT        ;STORE CARRY
3385 016322 010203                MOV     %2,%3        ;MOVE DATA FOR OUTPUT
3386 016324 042703 177770      BIC     @177770,%3   ;CLEAR ALL BUT RIGHTMOST 3 BITS
3387 016330 052703 000260      BIS     @260,%3      ;SET TO ASCII EQUIVALENT
3388 016334 000743                BR     C.WAIT        ;LOOP
3389
3390 016336 104003                ;SCOPE AND/OR ITERATION LOOP FOR EACH TEST 2 TIMES
3391 016340 032777 040000 162554      SCOPEC: KBINTT
3392 016346 001012                BIT     @40000,@SWR   ;TEST @SRPTR FOR SCOPE
3393 016350 032777 004000 162544      BIT     @4000,@SWR   ;YES,SCOPE
3394 016356 001013                BNE     D.1
3395 016360 026767 000036 000032      CMP     ITCNT,ITMAX  ;NO- TEST FOR ITERATION
3396 016366 100007                BPL     D.2          ;INHIBIT ITERATION
                                ;CHECK FOR ITERATIONS COMPLETE
                                ;EXIT-DONE

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3397 016370 005267 000026
3398 016374 022606
3399 016376 012667 161374
3400 016402 000177 000016
3401 016406 005067 000010
3402 016412 011667 000006
3403 016416 000002
3404 016420 000000
3405 016422 000000
3406 016424 005212
3407
3408
3409
3410 016426 142777 000177 162474
3411 016434 111267 000054
3412 016440 005202
3413 016442 121267 000046
3414 016446 001006
3415 016450 105777 162454
3416 016454 100375
3417 016456 005077 162450
3418 016462 000207
3419 016464 121227 000100
3420 016470 001003
3421 016472 004767 000020
3422 016476 000760
3423 016500 105777 162424
3424 016504 100375
3425 016506 112277 162420
3426 016512 000753
3427 016514 000000
3428
3429
3430 016516 105777 162406
3431 016522 100375
3432 016524 112777 000215 162400
3433 016532 105777 162372
3434 016536 100375
3435 016540 112777 000212 162364
3436 016546 000207
3437
3438
3439
3440 016550 004767 177742
3441 016554 004767 177736
3442 016560 004767 177732
3443 016564 004767 177726
3444 016570 000207
3445
3446
3447 016572 022767 000176 162322
3448 016600 001403
3449 016602 062716 000002
3450 016606 000504
3451 016610 012702 024037
3452 016614 004767 177606

```

```

D.1: INC ITCNT ; INCREMENT COUNT
      CMP (6)+, %6 ; REPOSITION STACK POINTER
      MOV (6)+, PSR ; RESTORE PROCESSOR STATUS
      JMP @RETURN ; RETURN TO RERUN TEST
D.2: CLR ITCNT ; CLEAR COUNTER
      MOV @%6, RETURN ; SAVE SCOPE RETURN POINTER
      RTI ; RETURN INLINE-NEXT TEST
ITMAX: 0 ; MAX NUMBER OF ITERATIONS
ITCNT: 0 ; COUNT LOCATION FOR ITERATION LOOP
RETURN: TEST1+2 ; ADDRESS OF LAST TEST

; MOV ADDRESS OF MESSAGE TO REGISTER 2
; THEN JSR %7, TOUT
TOUT: BICB #177, @TCSR ; CLEAR INT FLAG
      MOVB @%2, L.EOMK ; MOVE IN EOM MARKER
L.INC: INC %2 ; MOVE DATA POINTER TO NEXT BYTE
L.TOUT: CMPB @%2, L.EOMK ; COMPARE FOR EOM
      BNE L.CNT ; BRANCH IF NOT END OF MESSAGE
      TSTB @TCSR ; WAIT FOR TTY READY
      BPL -4
      CLR @TDBR ; OUTPUT NULL
      RTS %7 ; RETURN IF EOM
L.CNT: CMPB @%2, #'@ ; CHECK FOR CR, LF REQUEST
      BNE .+10 ; BRANCH IF NOT
      JSR %7, CRLF ; OUTPUT CARRIAGE RETURN, LINEFEED
      BR L.INC ; LOOP
      TSTB @TCSR ; WAIT FOR TTY
      BPL -4
      MOVB (2)+, @TDBR ; OUTPUT NEXT CHARACTER
      BR L.TOUT ; CONTINUE
L.EOMK: 0

; SUBROUTINE TO ISSUE CARRIAGE RETURN AND LINEFEED
CRLF: TSTB @TCSR ; WAIT FOR TTY READY
      BPL -4
      MOVB #215, @TDBR ; SEND CARRIAGE RETURN
      TSTB @TCSR ; WAIT FOR TTY
      BPL -4
      MOVB #212, @TDBR ; SEND LINE FEED
      RTS %7 ; RETURN

; DO 4 CRLF'S TO MOVE MESSAGES ON TELETYPE
CRLF4: JSR %7, CRLF
      JSR %7, CRLF
      JSR %7, CRLF
      JSR %7, CRLF
      RTS %7

CNTLUU: CMP #SWREG, SWR
        BEQ 1$
        ADD #2, (SP)
        BR OUT
1$: MOV #SWREQ, R2
     JSR PC, TOUT

```

3453	016620	016702	161352			MOV	SWREG,R2
3454	016624	004767	177360			JSR	PC,PROCT
3455	016630	012702	024022			MOV	#NEWIS,R2
3456	016634	004767	177566			JSR	PC,TOUT
3457	016640	005067	162270			CLR	TMP1
3458	016644	012767	000007	162266		MOV	#7,CSNT
3459	016652	105777	162246		AGN:	TSTB	#KBCSR
3460	016656	100375			READ:	BPL	READ
3461	016660	117767	162242	162254		MOVB	#KBOBR,TIB
3462	016666	116777	162250	162236		MOVB	TIB,#TDBR
3463	016674	142767	000200	162240		BICB	#200,TIB
3464	016702	122767	000025	162232		CMPB	#25,TIB
3465	016710	001005				BNE	2\$
3466	016712	012702	024174			MOV	#CTLU,R2
3467	016716	004767	177504			JSR	PC,TOUT
3468	016722	000746				BR	AGN
3469	016724	122767	000015	162210	2\$:	CMPB	#15,TIB
3470	016732	001430				BEQ	1\$
3471	016734	122767	000060	162200		CMPB	#60,TIB
3472	016742	003027				BGT	INERRR
3473	016744	122767	000067	162170		CMPB	#67,TIB
3474	016752	002423				BLT	INERRR
3475	016754	142767	000060	162160		BICB	#60,TIB
3476	016762	006367	162146			ASL	TMP1
3477	016766	006367	162142			ASL	TMP1
3478	016772	006367	162136			ASL	TMP1
3479	016776	156767	162140	162130		BISB	TIB,TMP1
3480	017004	005367	162130			DEC	CSNT
3481	017010	001404				BEQ	INERRR
3482	017012	000717				BR	READ
3483	017014	004767	177476		1\$:	JSR	#7,CRLF
3484	017020	000002			OUT:	RTI	
3485	017022	012702	024011		INERRR:	MOV	#QEST,R2
3486	017026	004767	177374			JSR	PC,TOUT
3487	017032	000702				BR	AGN
3488							
3489							
3490							
3491	017034	016746	160746		SUSWR:	MOV	6,-(SP)
3492	017040	016746	160740			MOV	4,-(SP)
3493	017044	012767	017064	160732		MOV	#1\$ ,4
3494	017052	022777	177777	162042		CMP	#-1,#SWR
3495	017060	001402				BEQ	2\$
3496	017062	000407				BR	3\$
3497	017064	022626			1\$:	CMP	(SP)+,(SP)+
3498	017066	012767	000176	162026	2\$:	MOV	#SWREG,SWR
3499	017074	012767	000174	162016		MOV	#DISPREG,DISPLAY
3500	017102	012667	160676		3\$:	MOV	(SP)+,4
3501	017106	012667	160674			MOV	(SP)+,6
3502	017112	000002				RTI	
3503							
3504	017114	022767	000176	162000	KBINT:	CMP	#SWREG,SWR
3505	017122	001016				BNE	1\$
3506	017124	005067	162004			CLR	TMP1
3507	017130	117767	161772	161776		MOVB	#KBOBR,TMP1
3508	017136	142767	000200	161770		BICB	#200,TMP1

;ROUTINE TO CHECK EXISTANCE OF SWREG

DZCRB.SRC

```

009 017144 122767 000007 161762      CMPB      #7,TMP1
010 017152 001002                      BNE      IS
011 017154 104002                      CNTLU
012 017156 104006                      CKU
013 017160 000002                      IS:      RTI
014
015 017162 011646                      ENTSRV:  MOV      (SP) -(SP)
016 017164 162716 000002                      SUB      #2,(SP)
017 017170 017616 000000                      MOV      #2(SP),(SP)
018 017174 006316                      ASL      (SP)
019 017176 042716 177001                      BIC      #177001,(SP)
020 017202 062716 017214                      ADD      @ENTTAB,(SP)
021 017206 017616 000000                      MOV      #2(SP),(SP)
022 017212 000136                      JMP
023
024 017214 016044                      ENTTAB:  PRINT
025 017216 016336                      SCOPEC
026 017220 016572                      CNTLUU
027 017222 017114                      KBINT
028 017224 016652                      READ
029 017226 017034                      SUSWR
030 017230 017234                      CKUU
031 017232 017254                      TITTYP
032
033 017234 122767 000007 161676  CKUU:  CMPB      #7,CSNT
034 017242 001403                      BEQ      IS
035 017244 016777 161664 161650  MOV      TMP1,@SWR
036 017252 000002                      IS:      RTI
037
038 017254 005767 161656                      TITTYP:  TST      TIFLG
039 017260 001406                      BEQ      IS
040 017262 012702 024125                      MOV      @TITL,R2
041 017266 004767 177134                      JSR      X7,TOUT
042 017272 005067 161640                      CLR      TIFLG
043 017276 000002                      IS:      RTI

```

```

:CALLED BY EMT HLT
:CALLED BY EMT SCOPE
:CALLED BY EMT CNTLU
:CALLED BY EMT KBINTT
:CALLED BY EMT READC
:CALLED BY EMT SUSWR
:CALLED BY EMT CKU
:CALLED BY EMT TIT

```

;DATA TABLES FOR DATA RELIABILITY TESTS

;ALPHANUMERIC DECK DATA TABLE

;FIRST VALUE FOR A COLUMN IS THE DIRECT  
;CARD IMAGE FOR THAT COLUMN ON CARD 1  
;THE SECOND VALUE IS THE ENCODED FORM OF THAT DATA

;COLUMN CHAR HOLLERITH

3560  
3561  
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3596  
3597  
3598  
3599  
3600  
3601  
3602  
3603

ALPCD:	4000	;	1	8	12
	200				
	4400	;	2	A	12 1
	201				
	4200	;	3	B	12 2
	202				
	4100	;	4	C	12 3
	203				
	4040	;	5	D	12 4
	204				
	4020	;	6	E	12 5
	205				
	4010	;	7	F	12 6
	206				
	4004	;	8	G	12 7
	207				
	4002	;	9	H	12 8
	210				
	4001	;	10	I	12 9
	220				
	4202	;	11	CENT	12 8 2
	212				
	4102	;	12	.	12 8 3
	213				
	4042	;	13	<	12 8 4
	214				
	4022	;	14	(	12 8 5
	215				
	4012	;	15	+	12 8 6
	216				
	4006	;	16	1	12 8 7
	217				
	2000	;	17	-	11
	100				
	2400	;	18	J	11 1
	101				
	2200	;	19	K	11 2
	102				
	2100	;	20	L	11 3
	103				
	2040	;	21	M	11 4
	104				
	2020	;	22	N	11 5
	105				
	2010	;	23	O	11 6
	106				
	2004	;	24	P	11 7
	107				

3652	017440	002002	2002	;25	Q	11 8
3653	017442	000110	110			
3654	017444	002001	2001	;26	R	11 9
3655	017446	000120	120			
3656	017450	002202	2202	;27	:	11 8 2
3657	017452	000112	112			
3658	017454	002102	2102	;28	S	11 8 3
3659	017456	000113	113			
3660	017460	002042	2042	;29	*	11 8 4
3661	017462	000114	114			
3662	017464	002022	2022	;30	)	11 8 5
3663	017466	000115	115			
3664	017470	002012	2012	;31	;	11 8 6
3665	017472	000116	116			
3666	017474	002006	2006	;32	BLANK	11 8 7
3667	017476	000117	117			
3668	017500	001000	1000	;33	0	0
3669	017502	000040	40			
3670	017504	001400	1400	;34	/	0 1
3671	017506	000041	41			
3672	017510	001200	1200	;35	S	0 2
3673	017512	000042	42			
3674	017514	001100	1100	;36	T	0 3
3675	017516	000043	43			
3676	017520	001040	1040	;37	U	0 4
3677	017522	000044	44			
3678	017524	001020	1020	;38	V	0 5
3679	017526	000045	45			
3680	017530	001010	1010	;39	W	0 6
3681	017532	000046	46			
3682	017534	001004	1004	;40	X	0 7
3683	017536	000047	47			
3684	017540	001002	1002	;41	Y	0 8
3685	017542	000050	50			
3686	017544	001001	1001	;42	Z	0 9
3687	017546	000060	60			
3688	017550	001202	1202	;43		0 8 2
3689	017552	000052	52			
3690	017554	001102	1102	;44	,	0 8 3
3691	017556	000053	53			
3692	017560	001042	1042	;45	x	0 8 4
3693	017562	000054	54			
3694	017564	001022	1022	;46	-	0 8 5
3695	017566	000055	55			
3696	017570	001012	1012	;47	>	0 8 6
3697	017572	000056	56			
3698	017574	001006	1006	;48		0 8 7
3699	017576	000057	57			
3700	017600	000000	0000	;49		BLANK
3701	017602	002000	0			
3702	017604	000400	0400	;50	1	1
3703	017606	000001	0			
3704	017610	000200	0200	;51	2	2
3705	017612	000002	0			
3706	017614	000100	0100	;52	3	3
3707	017616	000003	0			

3666	017630	000040
3667	017632	000004
3668	017634	000020
3669	017636	000005
3670	017638	000010
3671	017640	000006
3672	017642	000004
3673	017644	000007
3674	017646	000002
3675	017648	000010
3676	017650	000001
3677	017652	000020
3678	017654	000202
3679	017656	000012
3680	017658	000102
3681	017660	000013
3682	017662	000042
3683	017664	000014
3684	017666	000022
3685	017668	000015
3686	017670	000012
3687	017672	000016
3688	017674	000006
3689	017676	000017
3690	017700	004000
3691	017702	000200
3692	017704	004400
3693	017706	000201
3694	017710	004200
3695	017712	000202
3696	017714	004100
3697	017716	000203
3698	017720	004040
3699	017722	000204
3700	017724	004020
3701	017726	000205
3702	017730	004010
3703	017732	000206
3704	017734	004004
3705	017736	000207
3706	017740	004002
3707	017742	000210
3708	017744	004001
3709	017746	000220
3710	017750	004202
3711	017752	000212
3712	017754	004102
3713	017756	000213
3714	017760	004042
3715	017762	000214

0040
4
0020
5
0010
6
0004
7
0002
10
0001
20
0202
12
0102
13
0042
14
0022
15
0012
16
0006
17
4000
200
4400
201
4200
202
4100
203
4040
204
4020
205
4010
206
4004
207
4002
210
4001
220
4202
212
4102
213
4042
214
4022
215
4012
216
4006
217

ALPEND:

;53	4	4
;54	5	5
;55	6	6
;56	7	7
;57	8	8
;58	9	9
;59	:	8 2
;60	#	8 3
;61	A	8 4
;62	'	8 5
;63	=	8 6
;64	"	8 7
;65	&	12
;66	A	12 1
;67	B	12 2
;68	C	12 3
;69	D	12 4
;70	E	12 5
;71	F	12 6
;72	G	12 7
;73	H	12 8
;74	I	12 9
;75	CENT	12 8 2
;76	.	12 8 3
;77	<	12 8 4
;78	(	12 8 5
;79	+	12 8 6
;80	1	12 8 7

```

3716
3717
3718
3719
3720
3721
3722
3723
3724
3725
3726 020000 000000
3727 020002 000000
3728 020004 000001
3729 020006 000020
3730 020010 000002
3731 020012 000010
3732 020014 000004
3733 020016 000007
3734 020020 000010
3735 020022 000006
3736 020024 000020
3737 020026 000005
3738 020030 000040
3739 020032 000004
3740 020034 000100
3741 020036 000003
3742 020040 000200
3743 020042 000002
3744 020044 000400
3745 020046 000001
3746 020050 001000
3747 020052 000040
3748 020054 002000
3749 020056 000100
3750 020060 004000
3751 020062 000200
3752 020064 001111
3753 020066 000067
3754 020070 002222
3755 020072 000117
3756 020074 003333
3757 020076 000177
3758 020100 004444
3759 020102 000207
3760 020104 005555
3761 020106 000267
3762 020110 006666
3763 020112 000317
3764 020114 007777
3765 020116 000377
3766 020120 001010
3767 020122 000046
3768 020124 001212
3769 020126 000056
3770 020130 001313
3771 020132 000077

```

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: BINARY DECK DATA TABLE
: FIRST VALUE FOR A COLUMN IS THE DIRECT CARD IMAGE OF THAT COLUMN ON CARD1
: THE SECOND VALUE IS THE ENCODED VALUE, WHICH ORS THE OCTAL REPRESENTATION OF
: ROWS ONE THRU SEVEN
: MAINDEC-89-02A2-C
BINCD:

```

```

0 ; CARD COLUMN 1
1 ;2
20 ;3
10 ;4
4 ;5
7 ;6
10 ;7
6 ;8
20 ;9
5 ;10
40 ;11
4 ;12
100 ;13
200 ;14
400 ;15
1 ;16
1000 ;17
40 ;18
2000 ;19
100 ;20
4000 ;21
200 ;22
1111 ;23
67
2222
117
3333
177
4444
207
5555
267
6666
317
7777
377
1010
46
1212
56
1313
77

```

3772	020134	001414	1414	;24
3773	020136	000047	47	
3774	020140	001515	1515	;25
3775	020142	000067	67	
3776	020144	001616	1616	;26
3777	020146	000057	57	
3778	020150	001717	1717	;27
3779	020152	000077	77	
3780	020154	002020	2020	;28
3781	020156	000105	105	
3782	020160	002121	2121	;29
3783	020162	000127	127	
3784	020164	002323	2323	;30
3785	020166	000137	137	
3786	020170	002424	2424	;31
3787	020172	000107	107	
3788	020174	002525	2525	;32
3789	020176	000127	127	
3790	020200	002626	2626	;33
3791	020202	000117	117	
3792	020204	002727	2727	;34
3793	020206	000137	137	
3794	020210	003030	3030	;35
3795	020212	000147	147	
3796	020214	003131	3131	;36
3797	020216	000167	167	
3798	020220	003232	3232	;37
3799	020222	000157	157	
3800	020224	003434	3434	;38
3801	020226	000147	147	
3802	020230	003535	3535	;39
3803	020232	000167	167	
3804	020234	003636	3636	;40
3805	020236	000157	157	
3806	020240	003737	3737	;41
3807	020242	000177	177	
3808	020244	004040	4040	;42
3809	020246	000204	204	
3810	020250	004141	4141	;43
3811	020252	000227	227	
3812	020254	004242	4242	;44
3813	020256	000216	216	
3814	020260	004343	4343	;45
3815	020262	000237	237	
3816	020264	004545	4545	;46
3817	020266	000227	227	
3818	020270	004646	4646	;47
3819	020272	000217	217	
3820	020274	004747	4747	;48
3821	020276	000237	237	
3822	020300	005050	5050	;49
3823	020302	000246	246	
3824	020304	005151	5151	;50
3825	020306	000267	267	
3826	020310	005252	5252	;51
3827	020312	000256	256	

3828	020314	005353	5353	;52
3829	020316	000277	277	
3830	020320	005454	5454	;53
3831	020322	000247	247	
3832	020324	005656	5656	;54
3833	020326	000257	257	
3834	020330	005757	5757	;55
3835	020332	000277	277	
3836	020334	006060	6060	;56
3837	020336	000305	305	
3838	020340	006161	6161	;57
3839	020342	000327	327	
3840	020344	006262	6262	;58
3841	020346	000317	317	
3842	020350	006363	6363	;59
3843	020352	000337	337	
3844	020354	006464	6464	;60
3845	020356	000307	307	
3846	020360	006565	6565	;61
3847	020362	000327	327	
3848	020364	006767	6767	;62
3849	020366	000337	337	
3850	020370	007070	7070	;63
3851	020372	000347	347	
3852	020374	007171	7171	;64
3853	020376	000367	367	
3854	020400	007272	7272	;65
3855	020402	000357	357	
3856	020404	007373	7373	;66
3857	020406	000377	377	
3858	020410	007474	7474	;67
3859	020412	000347	347	
3860	020414	007575	7575	;68
3861	020416	000367	367	
3862	020420	007676	7676	;69
3863	020422	000357	357	
3864	020424	000101	0101	;70
3865	020426	000023	23	
3866	020430	000202	0202	;71
3867	020432	000012	12	
3868	020434	000303	0303	;72
3869	020436	000033	33	
3870	020440	000404	0404	;73
3871	020442	000007	7	
3872	020444	000505	0505	;74
3873	020446	000027	27	
3874	020450	000606	0606	;75
3875	020452	000017	17	
3876	020454	000707	0707	;76
3877	020456	000037	37	
3878	020460	003210	3210	;77
3879	020462	000146	146	
3880	020464	000123	0123	;78
3881	020466	000037	37	
3882	020470	007654	7654	;79
3883	020472	000347	347	

3884 020474 004567  
 3885 020476 000237  
 3886  
 3887  
 3888  
 3889  
 3890  
 3891  
 3892 020500 002577  
 3893 020502 000137  
 3894 020504 007252  
 3895 020506 000356  
 3896 020510 005777  
 3897 020512 000277  
 3898 020514 006777  
 3899 020516 000337  
 3900 020520 000000  
 3901 020522 000000  
 3902 020524 003777  
 3903 020526 000177  
 3904 020530 005777  
 3905 020532 000277  
 3906 020534 007737  
 3907 020536 000377  
 3908 020540 007757  
 3909 020542 000377  
 3910 020544 007767  
 3911 020546 000377  
 3912 020550 003773  
 3913 020552 000177  
 3914 020554 006775  
 3915 020556 000327  
 3916 020560 007776  
 3917 020562 000357  
 3918 020564 002001  
 3919 020566 000120  
 3920 020570 003002  
 3921 020572 000150  
 3922 020574 004404  
 3923 020576 000207  
 3924 020600 004210  
 3925 020602 000206  
 3926 020604 002120  
 3927 020606 000107  
 3928 020610 002040  
 3929 020612 000104  
 3930 020614 004120  
 3931 020616 000207  
 3932 020620 004210  
 3933 020622 000206  
 3934 020624 002404  
 3935 020626 000107  
 3936 020630 003002  
 3937 020632 000150  
 3938 020634 007777  
 3939 020636 000377

BINEND: 4567 ;80  
237

:MAINDEC-00-DZCMA-A-CB  
 BINCD: 2577 ;1 CARD COLUMN  
 137 ;2  
 7252 ;3  
 356 ;4  
 5777 ;5  
 277 ;6  
 6777 ;7  
 337 ;8  
 0000 ;9  
 0 ;10  
 3777 ;11  
 177 ;12  
 5777 ;13  
 277 ;14  
 7737 ;15  
 377 ;16  
 7757 ;17  
 377 ;18  
 7767 ;19  
 377 ;20  
 3773 ;21  
 177 ;22  
 6775 ;23  
 327 ;24  
 7776  
 357  
 2001  
 120  
 3002  
 150  
 4404  
 207  
 4210  
 206  
 2120  
 107  
 2040  
 104  
 4120  
 207  
 4210  
 206  
 2404  
 107  
 3002  
 150  
 7777  
 377

3940	020640	000000	0000	;25
3941	020642	000000	0	
3942	020644	006000	6000	;26
3943	020646	000300	300	
3944	020650	003001	3001	;27
3945	020652	000160	160	
3946	020654	004402	4402	;28
3947	020656	000211	211	
3948	020660	004204	4204	;29
3949	020662	000207	207	
3950	020664	002110	2110	;30
3951	020666	000107	107	
3952	020670	002060	2060	;31
3953	020672	000105	105	
3954	020674	004060	4060	;32
3955	020676	000205	205	
3956	020700	004110	4110	;33
3957	020702	000207	207	
3958	020704	002204	2204	;34
3959	020706	000107	107	
3960	020710	002402	2402	;35
3961	020712	000111	111	
3962	020714	005001	5001	;36
3963	020716	000260	260	
3964	020720	007777	7777	;37
3965	020722	000377	377	
3966	020724	007777	7777	;38
3967	020726	000377	377	
3968	020730	000000	0000	;39
3969	020732	000000	0	
3970	020734	000577	0577	;40
3971	020736	000037	037	
3972	020740	007252	7252	;41
3973	020742	000356	356	
3974	020744	000777	0777	;42
3975	020746	000037	37	
3976	020750	001000	1000	;43
3977	020752	000040	40	
3978	020754	006000	6000	;44
3979	020756	000300	300	
3980	020760	002477	2477	;45
3981	020762	000137	137	
3982	020764	001777	1777	;46
3983	020766	000077	77	
3984	020770	006537	6537	;47
3985	020772	000337	337	
3986	020774	005757	5757	;48
3987	020776	000277	277	
3988	021000	002767	2767	;49
3989	021002	000137	137	
3990	021004	005773	5773	;50
3991	021006	000277	277	
3992	021010	002775	2775	;51
3993	021012	000127	127	
3994	021014	005776	5776	;52
3995	021016	000257	257	

3996	021020	002001	2001	;53
3997	021022	000120	120	
3998	021024	005002	5002	;54
3999	021026	000250	250	
4000	021030	002404	2404	;55
4001	021032	000107	107	
4002	021034	005210	5210	;56
4003	021036	000246	246	
4004	021040	002120	2120	;57
4005	021042	000107	107	
4006	021044	005040	5040	;58
4007	021046	000244	244	
4008	021050	002120	2120	;59
4009	021052	000107	107	
4010	021054	005210	5210	;60
4011	021056	000246	246	
4012	021060	002404	2404	;61
4013	021062	000107	107	
4014	021064	003002	3002	;62
4015	021066	000150	150	
4016	021070	007777	7777	;63
4017	021072	000377	377	
4018	021074	000000	0000	;64
4019	021076	000000	0	
4020	021100	006000	6000	;65
4021	021102	000300	300	
4022	021104	003001	3001	;66
4023	021106	000160	160	
4024	021110	004402	4402	;67
4025	021112	000211	211	
4026	021114	004204	4204	;68
4027	021116	000207	207	
4028	021120	002110	2110	;69
4029	021122	000107	107	
4030	021124	002060	2060	;70
4031	021126	000105	105	
4032	021130	004060	4060	;71
4033	021132	000205	205	
4034	021134	004110	4110	;72
4035	021136	000207	207	
4036	021140	002204	2204	;73
4037	021142	000107	107	
4038	021144	002402	2402	;74
4039	021146	000111	111	
4040	021150	005001	5001	;75
4041	021152	000260	260	
4042	021154	007777	7777	;76
4043	021156	000377	377	
4044	021160	007777	7777	;77
4045	021162	000377	377	
4046	021164	002525	2525	;78
4047	021166	000127	127	
4048	021170	005252	5252	;79
4049	021172	000256	256	
4050	021174	007777	7777	;80
4051	021176	000377		

BINEND: 377

4053		
4054		
4055		
4056		
4057		
4058	021200	007777
4059	021202	000377
4060	021204	007777
4061	021206	000377
4062	021210	004000
4063	021212	000200
4064	021214	002000
4065	021216	000100
4066	021220	001000
4067	021222	000040
4068	021224	000400
4069	021226	000001
4070	021230	000200
4071	021232	000002
4072	021234	000100
4073	021236	000003
4074	021240	000040
4075	021242	000004
4076	021244	000020
4077	021246	000005
4078	021250	000010
4079	021252	000006
4080	021254	000004
4081	021256	000007
4082	021260	000002
4083	021262	000010
4084	021264	000001
4085	021266	000020
4086	021270	003777
4087	021272	000177
4088	021274	005777
4089	021276	000277
4090	021300	006777
4091	021302	000337
4092	021304	007377
4093	021306	000377
4094	021310	007577
4095	021312	000377
4096	021314	007677
4097	021316	000377
4098	021320	007737
4099	021322	000377
4100	021324	007757
4101	021326	000377
4102	021330	007767
4103	021332	000377
4104	021334	007773
4105	021336	000377
4106	021340	007775
4107	021342	000367

; MARK SENSE CARD TABLE  
; MAINDEC-00-DZCMB-A-CD  
MRKCD:

7777  
377  
7777  
377  
4000  
200  
2000  
100  
1000  
40  
400  
1  
200  
2  
100  
3  
40  
4  
20  
5  
10  
6  
4  
7  
2  
10  
1  
20  
3777  
177  
5777  
277  
6777  
337  
7377  
377  
7577  
377  
7677  
377  
7737  
377  
7757  
377  
7767  
377  
7773  
377  
7775  
367

4108	021344	007776	7776
4109	021346	000357	357
4110	021350	005252	5252
4111	021352	000256	256
4112	021354	002525	2525
4113	021356	000127	127
4114	021360	005252	5252
4115	021362	000256	256
4116	021364	002525	2525
4117	021366	000127	127
4118	021370	005252	5252
4119	021372	000256	256
4120	021374	002525	2525
4121	021376	000127	127
4122	021400	005252	5252
4123	021402	000256	256
4124	021404	002525	2525
4125	021406	000127	127
4126	021410	005252	5252
4127	021412	000256	256
4128	021414	002525	2525
4129	021416	000127	127
4130	021420	005252	5252
4131	021422	000256	256
4132	021424	002525	2525
4133	021426	000127	127
4134	021430	005252	5252
4135	021432	000256	256
4136	021434	002525	2525
4137	021436	000127	127
4138	021440	007777	7777
4139	021442	000377	377
4140	021444	007777	7777
4141	021446	000377	377
4142	021450	004000	4000
4143	021452	000200	200
4144	021454	002000	2000
4145	021456	000100	100
4146	021460	001000	1000
4147	021462	000040	40
4148	021464	000400	400
4149	021466	000001	1
4150	021470	000200	200
4151	021472	000002	2
4152	021474	000100	100
4153	021476	000003	3
4154	021500	000040	40
4155	021502	000004	4
4156	021504	000020	20
4157	021506	000005	5
4158	021510	000010	10
4159	021512	000006	6
4160	021514	000004	4
4161	021516	000007	7
4162	021520	000002	2
4163	021522	000010	10

4164	021524	000001	1
4165	021526	000020	20
4166	021530	003777	3777
4167	021532	000177	177
4168	021534	005777	5777
4169	021536	000277	277
4170	021540	006777	6777
4171	021542	000337	337
4172	021544	007377	7377
4173	021546	000377	377
4174	021550	007577	7577
4175	021552	000377	377
4176	021554	007677	7677
4177	021556	000377	377
4178	021560	007737	7737
4179	021562	000377	377
4180	021564	007757	7757
4181	021566	000377	377
4182	021570	007767	7767
4183	021572	000377	377
4184	021574	007773	7773
4185	021576	000377	377
4186	021600	007775	7775
4187	021602	000367	367
4188	021604	007776	7776
4189	021606	000357	357
4190	021610	005252	5252
4191	021612	000256	256
4192	021614	002525	2525
4193	021616	000127	127
4194	021620	005252	5252
4195	021622	000256	256
4196	021624	002525	2525
4197	021626	000127	127
4198	021630	005252	5252
4199	021632	000256	256
4200	021634	002525	2525
4201	021636	000127	127
4202	021640	005252	5252
4203	021642	000256	256
4204	021644	002525	2525
4205	021646	000127	127
4206	021650	005252	5252
4207	021652	000256	256
4208	021654	002525	2525
4209	021656	000127	127
4210	021660	005252	5252
4211	021662	000256	256
4212	021664	002525	2525
4213	021666	000127	127
4214	021670	005252	5252
4215	021672	000256	256
4216	021674	002525	2525
4217	021676	000127	127
4218	021700	000000	0
4219	021702	000000	0

MRKEND: 0

;END MARK SENSE DIAG TABLE

4220					
4221					
4222					
4223	021704	040057	051120	051505	MSG1: .ASCII ;/PRESS CARD READER 'MOTOR START' AND 'READ START'/;
4224	021712	020123	040503	042122	
4225	021720	051040	040505	042504	
4226	021726	020122	046447	052117	
4227	021734	051117	051440	040524	
4228	021742	052122	020047	047101	
4229	021750	020104	051047	040505	
4230	021756	020104	052123	051101	
4231	021764	023524	057		
4232	021767	057	050100	042522	MSG1A: .ASCII ;/PRESS CARD READER 'RESET'/;
4233	021774	051523	041440	051101	
4234	022002	020104	042522	042101	
4235	022010	051105	023440	042522	
4236	022016	042523	023524	057	
4237	022023	057	052100	042510	MSG2: .ASCII ;/ATTN HIT 'CONTINUE' ON THE CONSOLE/;
4238	022030	020116	044510	020124	
4239	022036	041447	047117	044524	
4240	022044	052516	023505	047440	
4241	022052	020116	044124	020105	
4242	022060	047503	051516	046117	
4243	022066	027505			
4244	022070	040057	051120	051505	MSG3: .ASCII ;/PRESS CARD READER 'READ STOP'/;
4245	022076	020123	040503	042122	
4246	022104	051040	040505	042504	
4247	022112	020122	051047	040505	
4248	022120	020104	052123	050117	
4249	022126	027447			
4250	022130	040057	051120	051505	MSG3A: .ASCII ;/PRESS CARD READER 'STOP'/;
4251	022136	020123	040503	042122	
4252	022144	051040	040505	042504	
4253	022152	020122	051447	047524	
4254	022160	023520	057		
4255	022163	057	052100	042510	MSG4: .ASCII ;/THE INTERRUPT LEVEL WAS /;
4256	022170	044440	052116	051105	
4257	022176	052523	052120	046040	
4258	022204	053105	046105	053440	
4259	022212	051501	027440		
4260	022216	040057	042522	047515	MSG5: .ASCII ;/REMOVE ALL CARDS FROM THE INPUT HOPPER/;
4261	022224	042526	040440	046114	
4262	022232	041440	051101	051504	
4263	022240	043040	047522	020115	
4264	022246	044124	020105	047111	
4265	022254	052520	020124	047510	
4266	022262	050120	051105	057	
4267	022267	057	051100	051505	MSG6: .ASCII ;/RESTORE CARDS IN THE INPUT HOPPER/;
4268	022274	047524	042522	041440	
4269	022302	051101	051504	044440	
4270	022310	020116	044124	020105	
4271	022316	047111	052520	020124	
4272	022324	047510	050120	051105	
4273	022332	057			
4274	022333	057	051100	044501	MSG7: .ASCII ;/RAISE OUTPUT STACKER PRESSURE ARM SLIGHTLY ABOVE HORIZONTAL & THEN LO
4275	022340	042523	047440	052125	
4276	022346	052520	020124	052123	

4276	022354	041501	042513	020122	
4277	022362	051120	051505	052523	
4278	022370	042522	040440	046522	
4279	022376	051440	044514	044107	
4280	022404	046124	020131	041101	
4281	022412	053117	020105	047510	
4282	022420	044522	047532	052116	
4283	022426	046101	040040	052040	
4284	022434	042510	020116	047514	
4285	022442	042527	020122	052111	
4286	022450	057			
4287	022451	057	046100	053517	MSG7A: .ASCII ;/2LOWER OUTPUT STACKER PLATE TO BOTTOM/;
4288	022456	051105	047440	052125	
4289	022464	052520	020124	052123	
4290	022472	041501	042513	020122	
4291	022500	046120	052101	020105	
4292	022506	047524	041040	052117	
4293	022514	047524	027515		
4294	022520	040057	047510	042114	MSG8: .ASCII ;/2HOLD DOWN THE SWITCH AT THE BOTTOM OF THE INPUT HOPPER/;
4295	022526	042040	053517	020116	
4296	022534	044124	020105	053523	
4297	022542	052111	044103	040440	
4298	022550	020124	044124	020105	
4299	022556	047502	052124	046517	
4300	022564	047440	020106	044124	
4301	022572	020105	047111	052520	
4302	022600	020124	047510	050120	
4303	022606	051105	057		
4304	022611	057	046100	043111	MSG8A: .ASCII ;/2LIFT SWITCH UNDER RIFFLE CAP/;
4305	022616	020124	053523	052111	
4306	022624	044103	052440	042116	
4307	022632	051105	051040	043111	
4308	022640	046106	020105	040503	
4309	022646	027520			
4310	022650	040057	046102	041517	MSG9: .ASCII ;/2BLOCK THE CARD READER STATION TO PREVENT A CARD GOING THRU, AND/;
4311	022656	020113	044124	020105	
4312	022664	040503	042122	051040	
4313	022672	040505	042504	020122	
4314	022700	052123	052101	047511	
4315	022706	020116	047524	050040	
4316	022714	042522	042526	052116	
4317	022722	040440	041440	051101	
4318	022730	020104	047507	047111	
4319	022736	020107	044124	052522	
4320	022744	020054	047101	027504	
4321	022752	040057	042522	047515	MSG10: .ASCII ;/2REMOVE JAMMED CARD/;
4322	022760	042526	045040	046501	
4323	022766	042515	020104	040503	
4324	022774	042122	057		
4325	022777	057	044100	046117	MSG11: .ASCII ;/2HOLD THE OUTPUT STACKER GATE OPEN. THEN/;
4326	023004	020104	044124	020105	
4327	023012	052517	050124	052125	
4328	023020	051440	040524	045503	
4329	023026	051105	043440	052101	
4330	023034	020105	050117	047105	
4331	023042	020056	044124	047105	

4332	023050	057				
4333	023051	057	050100	040514	MSG12: .ASCII ;/2PLACE SPECIAL DARK-LIGHT CHECK CARDS (SEE LISTING, TESTG);	
4334	023056	042503	051440	042520		
4335	023064	044503	046101	042040		
4336	023072	051101	026513	044514		
4337	023100	044107	020124	044103		
4338	023106	041505	020113	040503		
4339	023114	042122	020123	051450		
4340	023122	042505	046040	051511		
4341	023130	044524	043516	020054		
4342	023136	042524	052123	024507		
4343	023144	040500	020124	044124	.ASCII ;2AT THE BOTTOM OF THE INPUT STACK/;	
4344	023152	020105	047502	052124		
4345	023160	046517	047440	020106		
4346	023166	044124	020105	047111		
4347	023174	052520	020124	052123		
4348	023202	041501	027513			
4349	023206	040057	042504	045503	MSG13: .ASCII ;/2DECK CARD COLUMN PATTERN READ1 READ2 CODED READ/;	
4350	023214	020040	020040	040503		
4351	023222	042122	020040	047503		
4352	023230	052514	047115	050040		
4353	023236	052101	042524	047122		
4354	023244	051040	040505	030504		
4355	023252	051040	040505	031104		
4356	023260	020040	047503	042504		
4357	023266	020104	051040	040505		
4358	023274	027504				
4359	023276	040057	046101	044120	MSG14: .ASCII ;/2ALPHA /;	
4360	023304	020101	057			
4361	023307	057	041100	047111	MSG15: .ASCII ;/2BINARY/;	
4362	023314	051101	027531			
4363	023320	040057	044502	020124	MSG16: .ASCII ;/2BIT 15 WAS SET/;	
4364	023326	032461	053440	051501		
4365	023334	051440	052105	057		
4366	023341	057	051100	046505	MSG17: .ASCII ;/2REMEDY THE ERROR CONDITION AND PRESS 'CONTINUE'2/;	
4367	023346	042105	020131	044124		
4368	023354	020105	051105	047522		
4369	023362	020122	047503	042116		
4370	023370	052111	047511	020116		
4371	023376	047101	020104	051120		
4372	023404	051505	020123	041447		
4373	023412	047117	044524	052516		
4374	023420	023505	027500			
4375	023424	040057	044502	020124	MSG18: .ASCII ;/2BIT 8 WAS SET/;	
4376	023432	020070	040527	020123		
4377	023440	042523	027524			
4378	023444	040057	047503	052514	MSG19: .ASCII ;/2COLUMN READ1 READ2 CARDS ERRORS/;	
4379	023452	047115	051040	040505		
4380	023460	030504	051040	040505		
4381	023466	031104	041440	051101		
4382	023474	051504	042440	051122		
4383	023502	051117	027523			
4384	023506	040057	046101	020114	MSG20: .ASCII ;/2ALL OF THE CR11 CONTROL BOARD HAS;	
4385	023514	043117	052040	042510		
4386	023522	041440	030522	020061		
4387	023530	047503	052116	047522		

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4388 023536 020114 047502 051101
4389 023544 020104 040510 123
4390 023551 100 042502 047105
4391 023556 041440 042510 045503
4392 023564 042105 047440 052123
4393 023572 052040 051110 020125
4394 023600 044124 020105 040515
4395 023606 047111 042524 040516
4396 023614 041516 105
4397 023617 100 042523 044507
4398 023624 052123 051105 020056
4399 023630 051120 041117 042514
4400 023640 051515 047040 053517
4401 023646 053440 046111 020114
4402 023654 042502 044440 116
4403 023661 100 051104 053111
4404 023666 051105 026123 051040
4405 023674 041505 044505 042526
4406 023702 051522 023040 041440
4407 023710 041101 042514 041040
4408 023716 052105 042527 047105
4409 023724 041500 047117 051124
4410 023732 046117 023040 042040
4411 023740 044522 042526 047440
4412 023746 020122 044124 020105
4413 023754 051104 053111 020105
4414 023762 052111 042523 043114
4415 023770 057
4416
4417 023771 057 041500 042510 MSG21: .ASCII ;/CHECKER BOARD/;
4418 023776 045503 051105 041040
4419 024004 040517 042123 057
4420 024011 057 037500 020040 QUEST: .ASCII ;/a? = a/;
4421 024016 020075 027500
4422 024022 020057 020040 020040 NEWIS: .ASCII ;/ NEW = /;
4423 024030 042516 020127 020075
4424 024036 057
4425 024037 057 051500 051127 SMREQ: .ASCII ;/SMR = /;
4426 024044 036440 027440
4427 024050 040057 040503 042122 CIMPAT: .ASCII ;/CARD IMAGE PATTERN= /;
4428 024056 044440 040515 042507
4429 024064 050040 052101 042524
4430 024072 047123 020075 057
4431 024077 057 051500 040524
4432 024104 052123 047111 020107
4433 024112 042101 051104 051505
4434 024120 020123 020075 057
4435 024126 057 040100 055104 TITL: .ASCII ;/DZCRB-C CR11-CH11F DIAGNOSTIC TEST/;
4436 024132 051103 026502 020103
4437 024140 041440 030522 026461
4438 024146 046503 030461 020106
4439 024154 044504 043501 047516
4440 024162 052123 041511 052040
4441 024170 051505 027524
4442 024174 057057 040125 020075 CTLU: .ASCII ;/Ua= /;
4443 024202 057

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.ASCII ;/BEEN CHECKED OUT THRU THE MAINTENANCE/;

.ASCII ;/REGISTER. PROBLEMS NOW WILL BE IN/;

.ASCII ;/DRIVERS, RECEIVERS & CABLE BETWEEN/;

.ASCII ;/CONTROL & DRIVE OR THE DRIVE ITSELF/;

MSG21: .ASCII ;/CHECKER BOARD/;

QUEST: .ASCII ;/a? = a/;

NEWIS: .ASCII ;/ NEW = /;

SMREQ: .ASCII ;/SMR = /;

CIMPAT: .ASCII ;/CARD IMAGE PATTERN= /;

STADD: .ASCII ;/STARTING ADDRESS = /;

TITL: .ASCII ;/DZCRB-C CR11-CH11F DIAGNOSTIC TEST/;

CTLU: .ASCII ;/Ua= /;

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000001 051505 047522 041500 030522 SUBT2: .ASCII ;/@CR11 ERROR FUNCTION TEST/;
000002 051505 047522 051105 047522
000003 051505 047522 052506 041516
000004 051505 047522 047117 052040
000005 051505 047522 027524
000006 040057 044523 043516 SUBT4: .ASCII ;/@SINGLE TEST LOOP/;
000007 042514 052040 051505
000008 020124 047514 050117
000009 051500 047111 SUBT5: .ASCII ;/@SINGLE DATA PATTERN TEST/;
000010 046107 020105 040504
000011 040524 050040 052101
000012 042524 047122 052040
000013 051505 027524
000014 000001

```

.END

















3416 3420 3424 3431 3434

COMMEN	10						
ENDCOM	10						
ESCAPE	10						
GETPRI	10						
GETSAR	10						
INT	2126	2127	2205	2248	2291	2334	2377
MULT	10						
NEWTST	10						
POP	10						
PUSH	10						
REPORT	10						
SETPRI	10						
SETUP	10						
SKIP	10						
SLASH	10						
STARS	10						
SARSU	10						
TYPBIN	10						
TYPDEC	10						
TYPNAM	10						
TYPNUM	10						
TYPPCS	10						
TYPCT	10						
TYPTXT	10						
SSSCA	10						
SSNEMT	10						
SSSKIP	10						
.EQUAT	10						
.HEADE	10						
.KTLI	10						
.SETUP	10						
.SARHI	10						
.SACTI	10						
.SAPT8	10						
.SAPTH	10						
.SAPTY	10						
.SASTA	10						
.SCATC	10						
.SCHTA	10						
.SDB20	10						
.SDB20	10						
.SDIV	10						
.SEOP	10						
.SERRO	10						
.SERRT	10						
.SMULT	10						
.SPOWE	10						
.SRAND	10						
.SRODE	10						
.SRODC	10						
.SREAD	10						
.SR2RZ	10						
.SSAVE	10						
.SSB20	10						
.SSB20	10						
.SSCOP	10						

..SIZE	10
..SUPR	10
..STRAP	10
..STYPB	10
..STYPD	10
..STYPE	10
..STYPO	10
..S40CA	10
..1170	10

ADC	3366	3384													
ADG	1248	1621	2776	3161	3449	3520									
ASL	2774	2775	3476	3477	3478	3518									
ASR	2777	2778													
BEG	1077	1080	1123	1143	1158	1174	1182	1199	1215	1232	1253	1274	1294	1315	1330
	1338	1346	1360	1364	1371	1379	1382	1393	1570	1573	1576	1579	1582	1585	1600
	1604	1607	1638	1641	1652	1732	1738	1744	1755	1775	1797	1810	1833	1840	1851
	1867	1873	1877	1881	1885	1900	1904	1911	1914	1923	1938	1946	1950	1956	1964
	1971	1975	1990	1999	2007	2013	2017	2034	2047	2063	2112	2137	2184	2215	2258
	2301	2344	2387	2428	2438	2560	2571	2573	2580	2600	2606	2608	2687	2693	2696
	2742	2748	2750	2753	2767	2807	2827	2835	2868	2872	2890	2905	2934	2949	2964
	2984	2989	2995	3016	3026	3044	3047	3077	3081	3106	3118	3129	3134	3139	3163
	3219	3266	3283	3326	3378	3448	3470	3481	3495	3535	3541				
BGT	3472														
BIC	1121	1141	1549	1555	2060	2088	2133	2180	2211	2254	2297	2340	2383	2429	2466
BICB	2639	2779	2856	3164	3193	3386	3519								
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	1547	1554	1560	1564	1595	1627	1736	1773	2035	2058	2086	2108	2131	2134	2178
	2181	2209	2212	2252	2255	2295	2298	2338	2341	2381	2384	2424	2445	2464	2552
	2632	2646	2670	2683	2684	2785	2837	3166	3387						
BISB	3479														
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	1970	1974	1976	1989	1991	2038	2044	2046	2052	2068	2111	2136	2151	2183	2190
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	3162	3199	3205	3209	3215	3239	3265	3278	3296	3325	3391	3393			
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H08

DZCRB-C CR11/CH11F DIAGNOSTIC TEST MACY11 27(732) 02-NOV-76 15:51 PAGE 102  
DZCRB.SRC CROSS REFERENCE TABLE -- PERMANENT SYMBOLS

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.REPT	708		
.TITLE	685		

ERRORS DETECTED: 0  
DEFAULT GLOBALS GENERATED: 0

\*.NON.SEQ/SOL/CRF/PAGNUM/NL:TOC=SYSMAC.CO,DZCRB.SRC  
RUN-TIME: 31 46 4 SECONDS  
RUN-TIME RATIO: 260/82=3.1  
CORE USED: 33K (65 PAGES)

