

PDP11/04

CPU TEST
MD-11-DGKAA-A

EP-DGKAA-A-DL-A
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This microfiche card contains a grid of frames. The first 10 columns of frames contain data, likely test results or program output, with some frames showing vertical bar patterns. The remaining 10 columns of frames are mostly blank, with some faint vertical lines visible. The card is oriented vertically on the page.

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2.0 OPERATING INSTRUCTIONS

2.1 LOADING AND STARTING PROCEDURES

2.1.1 LOADING

USE NORMAL PROCEDURES FOR LOADING ABSOLUTE BINARY TAPES.

2.1.2 NORMAL START

THIS IS THE PROCEDURE FOR NORMAL PROGRAM RUNNING (I.E., STARTING WITH TEST 1 AND EXECUTING ENTIRE DIAGNOSTIC).

LOAD ADDRESS = 200
START

2.1.3 SUBTEST START

THIS IS THE PROCEDURE FOR STARTING AT A SUBTEST OTHER THAN 1.

1. LOAD \$TESTN (IN MAILBOX SECTION) WITH THE NUMBER OF SUBTEST MINUS ONE (IN OCTAL) FOR EXAMPLE, TO START AT SUBTEST 100, \$TESTN=77.
2. LOAD STARTING ADDRESS OF SUBTEST IN LOC. 216
3. LOAD ADDRESS = ADDRESS OF SUBTEST
START

2.2 SPECIAL ENVIRONMENTS

THIS PROGRAM IS WRITTEN TO COMPLY WITH ALL THE REQUIREMENTS OF THE APT INTERFACE SPECIFICATION. IT WILL RUN UNDER APT IN EITHER QUICK VERIFY, PROGRAM OR RUN-TIME MODES.

THIS PROGRAM IS WRITTEN TO COMPLY WITH ALL OF THE REQUIREMENTS OF PROGRAMS TO RUN UNDER THE ACT11 MONITOR.

2.3 PROGRAM OPTIONS

THIS PROGRAM IS INTENDED TO BE A BASIC PROCESSOR TEST. IT IS INTENDED TO BE THE LOWEST LEVEL DIAGNOSTIC RUN. IT PROVIDES FOR NO SELECTABLE OPTIONS.

IN ORDER THAT THE TEST BE RUNNABLE ON A PROCESSOR WITHOUT A TELETYPE, IT IS POSSIBLE TO SUPPRESS THE END OF PASS MESSAGE. IF NO TELETYPE IS AVAILABLE, ALTER THE BYTE, SENVM, WHICH IS LOCATED IN THE APT MAILBOX. SETTING SENVM TO 40(8) WILL

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THIS LOCATION IS INCREMENTED FROM ZERO TO ONE BEFORE THE PROGRAM COMES TO A PROGRAMMED HALT. IF THIS LOCATION IS NOT ONE, THEN THE DIAGNOSTIC HAS COME TO AN UNPROGRAMMED HALT. CHECK THE STACK AND PC FOR A CLUE TO THE CAUSE. SUSPECT A TRAP.

3.2.2 \$FATAL

THIS LOCATION IS LOADED WITH A NUMBER BEFORE A HALT IS EXECUTED. EACH PROGRAMMED HALT HAS A UNIQUE NUMBER ASSOCIATED WITH IT WHICH CAN BE USED TO IDENTIFY THE ERROR WHICH HAS BEEN DETECTED.

3.2.3 \$PASS

THIS LOCATION IS INCREMENTED FOR EVERY COMPLETE PASS OF THE DIAGNOSTIC. MONITORING THIS LOCATION WILL INDICATE WHETHER OR NOT THE PROGRAM IS HUNG. IT WILL ALSO INDICATE THE NUMBER OF SUCCESSFUL PASSES COMPLETED BEFORE THE ERROR HALT. A HIGH PASS COUNT MIGHT INDICATE THAT THE ERROR HALT IS ASSOCIATED WITH AN INTERMITTANT FAULT.

3.2.4 \$TESTN

THIS LOCATION IS INCREMENTED IN EACH NEW SUBTEST. THIS SHOULD INDICATE THE TEST BEING EXECUTED WHEN THE ERROR WAS DETECTED. THIS LOCATION IS ALSO USED TO DETECT A SEQUENCE ERROR.

3.4 ERROR IDENTIFICATION

BECAUSE OF THE OVERHEAD ASSOCIATED WITH EACH HALT IN AN APT COMPATIBLE PROGRAM THE SEQUENCE CHECK CODE WILL SHARE THE ERROR HALT OF FUNCTIONAL ERROR WITHIN EACH SUBTEST. TO DETERMINE WHICH ERROR IS BEING REPORTED, LOCATIONS \$FATAL AND \$TESTN ARE USED TOGETHER. WHEN AN ERROR HALT OCCURS, CHECK \$FATAL TO DETERMINE THE NUMBER OF THE ERROR DETECTED. NOW, CHECK THAT THE TEST NUMBER WHERE THIS ERROR IS DETECTED CORRESPONDS TO THE VALUE IN \$TESTN. IF THESE AGREE THE ERROR WAS A FUNCTIONAL ERROR AS DESCRIBED IN THE LISTINGS. IF THESE NUMBERS DO NOT AGREE, THEN A SEQUENCE ERROR WAS DETECTED. IN THIS CASE \$TESTN WILL CONTAIN ONE MORE THAN THE NUMBER OF THE LAST TEST SUCCESSFULLY COMPLETED. SEQUENCE ERRORS WHICH SHARE THE ERROR HALTS OF FUNCTIONAL ERRORS WILL ALWAYS BE REPORTED BY THE LAST HALT IN THE SUBTEST IN WHICH THEY WERE DISCOVERED.

4.0 PROGRESS REPORT

AT THE END OF EACH SUCCESSFUL PASS THE PROGRAM INCREMENTS THE LOCATION \$PASS WHICH IS IN THE APT MAILBOX. THIS LOCATION WILL

ALWAYS CONTAIN THE NUMBER OF SUCCESSFUL PASSES COMPLETED.
\$PASS IS RESET WITH EVERY RETART FROM LOC. 200.

ADDITIONALLY, THE MESSAGE END OF DGKAA IS PRINTED ON THE CONSOLE
TELETYPE AFTER THE FIRST PASS AND FOLLOWING EVERY 400TH PASS
THEREAFTER.

IF NO TELETYPE IS AVAILABLE, THE CONSOLE OUTPUT MUST BE SUPPRESSED.
(SEE SECTION 2.3).

5.0 TROUBLE SHOOTING

WHEN THE PROGRAM DISCOVERS A FAULT IT WILL HALT. TO DETERMINE
THE CAUSE OF THE HALT, THE DIAGNOSTIC PROVIDES ERROR INFORMATION.
THIS INFORMATION IS STORED IN THE APT MAILBOX AND IS THE PRIMARY
SOURCE OF ERROR IDENTIFICATION.

UPON FINDING AN ERROR, THE FOLLOWING PROCEDURE SHOULD AID IN ISOLATING
THE FAULT.

5.1 CHECK THE MAILBOX

1. \$MSGTY THIS LOCATION SHOULD CONTAIN A 1. IF THE PROCESSOR
HALTS AND THIS LOCATION IS ZERO, THEN THE PROCESSOR HAS COME
TO AN UNEXPECTED HALT. FIRST SUSPECT A TRAP. CHECK THE
PC AND IF A TRAP CHECK R6 AND THE STACK FOR THE LOCATION OF
THE FAILING INSTRUCTION.
2. \$FATAL THIS LOCATION IS USED TO HOLD THE NUMBER OF THE ERROR WHICH HAS
DETECTED. EACH ERROR BEING CHECKED BY THE DIAGNOSTIC IS ASSIGNED
A UNIQUE NUMBER WHICH IS STORED IN \$FATAL WHEN THAT ERROR IS DETECTED.

WHEN AN ERROR IS DETECTED, CHECK THE LISTING TO SEE THAT THE ERROR
NUMBER STORED IN \$FATAL IS ONE WHICH IS DETECTED IN THE
TEST WHOSE NUMBER IS IN \$TESTN. IF THERE IS A DISAGREEMENT THEN
THE ERROR BEING REPORTED IS A SEQUENCE ERROR. \$TESTN CONTAINS
ONE MORE THAN THE LAST TEST WHICH WAS SUCCESSFULLY COMPLETED.

3. \$TESTN THIS LOCATION IS USED TO INDICATE THE NUMBER OF THE
TEST WHICH WAS BEING EXECUTED WHEN THE FAULT WAS DETECTED.
\$TESTN IS USED IN CONJUNCTION WITH \$FATAL TO DISTINGUISH
BETWEEN SEQUENCE AND FUNCTIONAL ERRORS. (SEE 2. THIS SECTION)
4. \$PASS THIS LOCATION IS USED TO INDICATE THE NUMBER OF SUCCESSFUL
PASSES WHICH THE DIAGNOSTIC HAS COMPLETED. THIS WILL GIVE AN
INDICATION THAT THE DIAGNOSTIC HAS NOT JUST BEEN HUNG IN A LOOP
IF NOT TELETYPE IS AVAILABLE TO REPORT THE PRINTED PROGRESS
REPORTS.

IF AN ERROR HAS BEEN DETECTED \$PASS WILL SHOW WHETHER IT
WAS A HARD ERROR DISCOVERED DURING THE FIRST TRY OR WHETHER
IT WAS INTERMITTANT OR DEVELOPED DURING THE RUNNING OF THE
DIAGNOSTIC.

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5.2 SCOPING

WHILE THIS DIAGNOSTIC IS PRIMARILY INTENDED TO BE A FAULT DETECTION PROGRAM, PROVISIONS ARE MADE TO ASSIST A TECHNICIAN WHO MIGHT WANT TO USE THE PROGRAM AS A TROUBLE SHOOTING TEST.

THE PROCEDURE FOR SCOPING A SUBTEST INVOLVES MODIFYING SEVERAL MEMORY LOCATIONS IN THE TEST ITSELF. THE PHILOSOPHY IS TO PROVIDE A SCOPING LOOP WHICH WILL INCLUDE THE CODE WHERE THE ERROR WAS DETECTED. THE LOOP IS SET UP SO THAT THE LOOP WILL NOT BE TERMINATED SHOULD THE ERROR INTERMITTANTLY DISAPPEAR.

THE PROCEDURE IS AS FOLLOWS:

1. DETERMINE WHICH ERROR IS TO BE SCOPED. USE \$FATAL AND \$TESTN FOR THIS (SEE ABOVE)
2. LOCATE THE ERROR ROUTINE IN THE LISTING.
3. CLEAR THE RIGHT BYTE OF THE CONDITIONAL BRANCH INSTRUCTION ASSOCIATED WITH THE ERROR. (THIS IS MARKED WITH <===='S IN THE LISTING.)
4. REPLACE THE INSTRUCTION FOLLOWING <MOV #XXX, -(R2)> WITH THE SCOPING BRANCH PROVIDED IN THE LISTING COMMENTS.
5. RESTART THE PROGRAM. THE PROGRAM MAY BE RESTARTED FROM THE BEGINNING OR FROM THE SUBTEST (SEE 2.0).

6.0 LISTING

000500

000240
000007
000006
177776
177564
177566

000400

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%
.TITLE MAINDEC-11-DGKAA 11/04 CPU TEST
.ENABLE ABS
STBOT=500
.NLIST CND,MC,MD
.LIST ME
SCOPE=NOP
R7=%7
R6=%6
PS=177776
TPS=177564
TPB=177566
.MCALL .SAPTHDR, .SAPTBL, .SACT11
.SBTTL ACT11 HOOKS
;*****
;HOOKS REQUIRED BY ACT11
$SVPC=. ;SAVE PC

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415
416 000046
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418 000052
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421
422
423
424
425 000300
426 000300 000000
427 000302 000000
428 000304 000000
429 000306 000000
430 000310 000000
431 000312 000000
432 000314 000000
433 000316 000000
434 000320
435 000320 000
436 000321 000
437 000322 000000
438 000324 000000
439 000326 000000
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446 000330
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453 000330
454 000024 000024
455 000024 000200
456 000044 000044
457 000044 000330
458 000330
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463 000330
464 000330 000000
465 000332 000300
466 000334 000002
467 000336 000002
468 000340 000000
469 000342 000014
470 000370

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.=46
$ENDAD ;;1)SET LOC.46 TO ADDRESS OF $ENDAD IN .SEOP
.=52
.WORD 0 ;;2)SET LOC.52 TO ZERO
.=$$VPC ;; RESTORE PC
.=300
.SBTTL APT MAILBOX-ETABLE

;*****
;EVEN
$MAIL: ;; APT MAILBOX
$MSGTY: .WORD AMSGTY ;; MESSAGE TYPE CODE
$FATAL: .WORD AFATAL ;; FATAL ERROR NUMBER
$TESTN: .WORD ATESTN ;; TEST NUMBER
$PASS: .WORD APASS ;; PASS COUNT
$DEVCT: .WORD ADEVCT ;; DEVICE COUNT
$UNIT: .WORD AUNIT ;; I/O UNIT NUMBER
$MSGAD: .WORD AMSGAD ;; MESSAGE ADDRESS
$MSGLG: .WORD AMSGLG ;; MESSAGE LENGTH
$ETABLE: ;; APT ENVIRONMENT TABLE
$ENV: .BYTE AENV ;; ENVIRONMENT BYTE
$ENVM: .BYTE AENVM ;; ENVIRONMENT MODE BITS
$SWREG: .WORD ASWREG ;; APT SWITCH REGISTER
$USWR: .WORD AUSWR ;; USER SWITCHES
$CPUOP: .WORD ACPUOP ;; CPU TYPE, OPTIONS
;*
;* BIT 15-11=CPU TYPE
;* 11/04=01,11/05=02,11/20=03,11/40=04,11/45=05
;* 11/70=06,PDQ=07,Q=10
;* BIT 10=REAL TIME CLOCK
;* BIT 9=FLOATING POINT PROCESSOR
;* BIT 8=MEMORY MANAGEMENT
$ETEND:
.MEXIT
.SBTTL APT PARAMETER BLOCK

;*****
;SET LOCATIONS 24 AND 44 AS REQUIRED FOR APT
;*****
.$X=.; ;SAVE CURRENT LOCATION
.=24 ;SET POWER FAIL TO POINT TO START OF PROGRAM
200 ;FOR APT START UP
.=44 ;POINT TO APT INDIRECT ADDRESS PNTR.
$APTHDR ;POINT TO APT HEADER BLOCK
.=.$X ;RESET LOCATION COUNTER
;*****
;SETUP APT PARAMETER BLOCK AS DEFINED IN THE APT-PDP11 DIAGNOSTIC
;INTERFACE SPEC.

$APTHD:
$HIBTS: .WORD 0 ;; TWO HIGH BITS OF 18 BIT MAILBOX ADDR.
$MBADR: .WORD $MAIL ;; ADDRESS OF APT MAILBOX (BITS 0-15)
$STMT: .WORD 2 ;; RUN TIM OF LONGEST TEST
$PASTM: .WORD 2 ;; RUN TIME IN SECS. OF 1ST PASS ON 1 UNIT (QUICK VERIFY)
$UNITM: .WORD 0 ;; ADDITIONAL RUN TIME (SECS) OF A PASS FOR EACH ADDITIONAL UNIT
.WORD $ETEND-$MAIL/2 ;; LENGTH MAILBOX-ETABLE(WORDS)
.=370

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471 000370 000000 000000 000000      0,0,0,0,0,0
472 000376 000000 000000 000000
473 000404 000001 000001 177777      1,1,-1
474      000500      =500
475      ;*****
476      ;SET UP STARTING ADDRESS
477      .SX=
478      =200
479 000200 000167 000274      JMP      START
480
481 000204 012706 000500      MOV      #STBOT,R6      ;SET STACK POINTER
482 000210 012702 000304      MOV      #STSTN,R2     ;SET MAILBOX POINTER
483 000214 000137      JMP      @PC+          ;JUMP TO SUBTEST
484 000216 000000      0      ;ADDR. OF SUBTEST GOES HERE
485
486      000500      =.SX
487      000302      $ERROR=$FATAL
488      000304      $STSTNM=$STSTN
489 000500 012737 015426 000024      START: MOV      #PWRDN,@#24      ;SET UP FOR POWER FAIL
490 000506 012737 000000 000306      MOV      #0,@#SPASS     ;CLEAR PASS COUNT
491 000514 012737 177777 015310      MOV      #-1,@#PASSPT  ;SET PRINT COUNTER
492 000522 012706 000500      RESTRT: MOV     #STBOT,R6 ;INITIALIZE STACK POINTER
493 000526 012702 000304      MOV      #STSTN,R2     ;SET UP POINTER TO MESSAGE TYPE
494 000532 012737 000000 000304      MOV      #0,@#STSTNM  ;CLEAR TEST NUMBER
495 000540 012737 000000 000302      MOV      #0,@#$ERROR  ;CLEAR ERROR NUMBER
496 000546 012737 000000 000300      MOV      #0,@#MSGTY   ;CLEAR MESSAGE TYPE(FOR APT)

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500 000554 005212
501 000556 022712 000001
502 000562 001024
503 000564 000257
504 000566 001401
505 000570 000404
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510 000572
511 000572 012742 000001
512 000576 005242
513 000600 000000
514 000602
515 000602 001004
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520 000604 012742 000002
521 000610 005242
522 000612 000000
523 000614 000264
524 000616 001001
525 000620 000404
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530 000622
531 000622 012742 000003
532 000626 005242
533 000630 000000
534 000632
535 000632 001404
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540 000634 012742 000004
541 000640 005242
542 000642 000000
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*****
;TEST 1 CHECK BRANCHES ON Z BIT
*****
TST1: INC (R2) ;UPDATE TEST NUMBER
      CMP #1,(R2) ;SEQUENCE ERROR?
      BNE TST2-10 ;BR TO ERROR HALT ON SEQ ERROR
      CCC ;CLEAR ALL CONDITION CODES
      BEQ BR1 ;SHOULD BRANCH
      BR BR2 ;BAD BRANCH OF Z-BIT
      ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
      ; BRANCH INSTRUCTION AND <====
      ; REPLACE THE MOVE INSTRUCTION <====
      ; FOLLOWING W/ 774 <====
      ;
BR1: MOV #1,-(R2) ;MOVE TO MAILBOX # ***** 1 *****
      INC -(R2) ;SET MSGTYP TO FATAL ERROR
      HALT ;SHOULD HAVE BRANCHED: Z=0
      ;
BR2: BNE BR3
      ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
      ; CONDITIONAL BRANCH INST. AND <====
      ; REPLACE THE MOVE INSTRUCTION <====
      ; WHICH FOLLOWS W/ 770 <====
      ;
      ; MOVE TO MAILBOX # ***** 2 *****
      ; SET MSGTYP TO FATAL ERROR
      ;
      ;
      ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
      ; BRANCH INSTRUCTION AND <====
      ; REPLACE THE MOVE INSTRUCTION <====
      ; FOLLOWING W/ 760 <====
      ;
BR4: MOV #3,-(R2) ;MOVE TO MAILBOX # ***** 3 *****
      INC -(R2) ;SET MSGTYP TO FATAL ERROR
      HALT ;SHOULD NOT HAVE BRANCHED HERE ON Z=1
      ;
BR5: BEQ TST2
      ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
      ; CONDITIONAL BRANCH INST. AND <====
      ; REPLACE THE MOVE INSTRUCTION <====
      ; WHICH FOLLOWS W/ 754 <====
      ;
      ; MOVE TO MAILBOX # ***** 4 *****
      ; SET MSGTYP TO FATAL ERROR
      ; SHOULD HAVE BRANCHED ON Z=1
      ; OR SEQUENCE ERROR

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:SBTTL DATA PATH TESTS

THE DATA PATH TESTS ARE USED TO VERIFY THAT VARIOUS
DATA PATTERNS CAN BE SUCCESSFULLY MOVED THROUGH THE DATA PATHS
MOVE AND COMPARE MODE 2,3 INSTRUCTIONS ARE USED TO PASS AND
TEST VARIOUS DATA PATTERNS IN THE DATA PATHS.
THE TEST EXERCISES THE INTERNAL DATA PATHS, THE UNIBUS
DATA TRANSCIEVERS, AND AMUX CONTROL FOR ALU AND UBUS INPUTS.
IF THESE TESTS FAIL, EXAMINE THE TARGET LOCATION (LOC. 0)
TO SEE WHICH BITS OF THE DATA PATH ARE FAILING. IF THIS PROVIDES
INCONCLUSIVE DATA, TRY TO CHECK MODE 3 IR DECODE BY RUNNING
JUST THE MICROCODE AND IR DECODE TESTS FOR THE MOVE AND COMPARE
INSTRUCTIONS.

:TEST 2 TEST OF ZEROES IN THE DATA PATH

TST2: INC (R2) ;UPDATE TEST NUMBER
CMP #2,(R2) ;SEQUENCE ERROR?
BNE TST3-10 ;BR TO ERROR HALT ON SEQ ERROR
MOV #0,a#0 ;MOVE ZEROES THRU ADDRESS LINES, DATA
;LINES AND INTERNAL PATHS
TST a#0 ;SUCCESSFUL?
BEQ TST3
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 772 <====
MOV #5,-(R2) ;MOVE TO MAILBOX # ***** 5 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;DATA INCORRECT
; OR SEQUENCE ERROR

:TEST 3 TEST OF PATTERN 125252 IN DATA PATH

TST3: INC (R2) ;UPDATE TEST NUMBER
CMP #3,(R2) ;SEQUENCE ERROR?
BNE TST4-10 ;BR TO ERROR HALT ON SEQ ERROR
MOV #125252,a#0 ;MOVE ALTERNATING ONES AND ZEROES
;THRU DATA PATHS
CMP #125252,a#0 ;SUCCESSFUL
BEQ TST4
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 771 <====
MOV #6,-(R2) ;MOVE TO MAILBOX # ***** 6 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;DATA INCORRECT
; OR SEQUENCE ERROR

:TEST 4 TEST OF PATTERN 052525 IN DATA PATH

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600 000736 005212          TST4:  INC      (R2)          ;UPDATE TEST NUMBER
601 000740 022712 000004    CMP      #4,(R2)        ;SEQUENCE ERROR?
602 000744 001007          BNE     TST5-10        ;BR TO ERROR HALT ON SEQ ERROR
603 000746 012737 052525 000000  MOV     #052525,0#0    ;MOVE ALTERNATING ZEROES AND ONES
604                                     ;THRU DATA PATH
605 000754 022737 052525 000000  CMP     #052525,0#0    ;SUCCESSFUL?
606 000762 001404          BEQ     TST5
607                                     ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
608                                     ;          CONDITIONAL BRANCH INST. AND <====
609                                     ;          REPLACE THE MOVE INSTRUCTION <====
610                                     ;          WHICH FOLLOWS W/ 771 <====
611 000764 012742 000007    MOV     #7,-(R2)       ;MOVE TO MAILBOX # ***** 7 *****
612 000770 005242          INC     -(R2)         ;SET MSGTYP TO FATAL ERROR
613 000772 000000          HALT                    ;DATA INCORRECT
614                                     ; OR SEQUENCE ERROR
615
616 ;*****
617 ;TEST 5 TEST OF ALL ONES IN DATA PATH
618 ;*****
619 000774 005212          TST5:  INC      (R2)          ;UPDATE TEST NUMBER
620 000776 022712 000005    CMP     #5,(R2)        ;SEQUENCE ERROR?
621 001002 001007          BNE     TST6-10        ;BR TO ERROR HALT ON SEQ ERROR
622 001004 012737 177777 000000  MOV     #177777,0#0    ;MOVE ONES THRU DATA PATH
623 001012 022737 177777 000000  CMP     #177777,0#0    ;SUCCESSFUL
624 001020 001404          BEQ     TST6
625                                     ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
626                                     ;          CONDITIONAL BRANCH INST. AND <====
627                                     ;          REPLACE THE MOVE INSTRUCTION <====
628                                     ;          WHICH FOLLOWS W/ 771 <====
629 001022 012742 000010    MOV     #10,-(R2)     ;MOVE TO MAILBOX # ***** 10 *****
630 001026 005242          INC     -(R2)         ;SET MSGTYP TO FATAL ERROR
631 001030 000000          HALT                    ;DATA INCORRECT
632                                     ; OR SEQUENCE ERROR

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:SBTTL SCRATCH PAD TESTS

: THE SCRATCH PAD TESTS ARE USED TO VERIFY THAT VARIOUS
: DATA PATTERNS CAN BE SUCCESSFULLY HELD IN THE SCRATCH PAD
: CIRCUITRY. MOVE AND COMPARE INSTRUCTIONS ARE USED TO TEST THAT
: RO CAN HOLD VARIOUS DATA PATTERNS. EACH DATA PATTERN IS
: MOVED AND TESTED IN A SMALL LOOP CONVENIENT FOR SCOPING. THE
: SUCCESSFUL COMPLETION OF THESE TESTS SHOULD VERIFY THE CIRCUITRY EXTERNAL
: TO THE SCRATCH PAD ITSELF.

: THE REMAINDER OF THE GENERAL REGISTERS ARE TESTED BY MOVING
: A BIT INTO BIT 0 OF THE REGISTER AND SHIFTING IT LEFT ONE
: BIT AT A TIME INTO THE CARRY BIT. THE RESULT IS THEN CHECKED TO INSURE THAT
: NO BITS WERE PICKED.

: AT THIS POINT ALL OF THE GENERAL REGISTERS HAVE BEEN EXERCISED
: AS WELL AS REGISTER 11. REGISTERS 10 AND 12 HAVE BEEN ACCESSED BY
: THE INSTRUCTIONS. REGISTERS 13,14,AND 17 WILL BE TESTED LATER IN THE
: MICROCODE TESTS.

: IF THE PATTERN TESTS WITH REGISTER 0 FAIL CHECK THE RESULTANT
: DATA FOR A CLUE TO A FAULT IN THE EXTERNAL CIRCUITRY. IF THE
: PATTERN TESTS WITH RO ARE SUCCESSFUL BUT THE TESTS WITH THE OTHER
: REGISTERS FAIL, SUSPECT THE REGISTER SELECT LINES AND THEN THE SCRATCH
: PAD ITSELF.

:TEST 6 TEST IF RO CAN HOLD ALL ZEROES

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TST6:  INC      (R2)          ;UPDATE TEST NUMBER
        CMP      #6,(R2)    ;SEQUENCE ERROR?
        BNE     TST7-10    ;BR TO ERROR HALT ON SEQ ERROR
        MOV      #0,RO      ;MOVE ZEROES TO RO
        TST     RO         ;SUCCESSFUL?
        BEQ     TST7
        ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
        ;           CONDITIONAL BRANCH INST. AND <====
        ;           REPLACE THE MOVE INSTRUCTION <====
        ;           WHICH FOLLOWS W/ 774 <====
        MOV      #11,-(R2)  ;MOVE TO MAILBOX # ***** 11 *****
        INC     -(R2)      ;SET MSGTYP TO FATAL ERROR
        HALT    ;RO NOT 0
        ; OR SEQUENCE ERROR
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:TEST 7 TEST IF RO CAN HOLD ONES AND ZEROES

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TST7:  INC      (R2)          ;UPDATE TEST NUMBER
        CMP      #7,(R2)    ;SEQUENCE ERROR?
        BNE     TST10-10   ;BR TO ERROR HALT ON SEQ ERROR
        MOV      #125252,RO ;MOVE ALTERNATING ONES AND ZEROES TO RO
        CMP     RO,#125252  ;SUCCESSFUL?
        BEQ     TST10
        ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
        ;           CONDITIONAL BRANCH INST. AND <====
        ;           REPLACE THE MOVE INSTRUCTION <====
```

```

689
690 001104 012742 000012      MOV      #12,-(R2)      ; WHICH FOLLOWS W/ 773      <====
691 001110 005242      INC      -(R2)          ; MOVE TO MAILBOX # ***** 12 *****
692 001112 000000      HALT                    ; SET MSGTYP TO FATAL ERROR
693                                     ; RO NOT 125252
694                                     ; OR SEQUENCE ERROR

```

```

;*****
;TEST 10      TEST IF RO CAN HOLD ZEROES AND ONES
;*****

```

```

697
698 001114 005212      TST10: INC      (R2)          ; UPDATE TEST NUMBER
699 001116 022712 000010      CMP      #10,(R2)      ; SEQUENCE ERROR?
700 001122 001005      BNE     TST11-10      ; BR TO ERROR HALT ON SEQ ERROR
701 001124 012700 052525      MOV     #052525,RO     ; MOVE ALTERNATING ZEROES AND ONES TO RO
702 001130 020027 052525      CMP     RO,#052525     ; SUCCESSFUL?
703 001134 001404      BEQ     TST11

```

```

704                                     ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS      <====
705                                     ; CONDITIONAL BRANCH INST. AND                <====
706                                     ; REPLACE THE MOVE INSTRUCTION                <====
707                                     ; WHICH FOLLOWS W/ 773                        <====

```

```

708 001136 012742 000013      MOV     #13,-(R2)      ; MOVE TO MAILBOX # ***** 13 *****
709 001142 005242      INC     -(R2)          ; SET MSGTYP TO FATAL ERROR
710 001144 000000      HALT                    ; RO NOT 52525
711                                     ; OR SEQUENCE ERROR

```

```

;*****
;TEST 11      TEST IF RO CAN HOLD ALL ONES
;*****

```

```

714
715
716 001146 005212      TST11: INC      (R2)          ; UPDATE TEST NUMBER
717 001150 022712 000011      CMP     #11,(R2)      ; SEQUENCE ERROR?
718 001154 001005      BNE     TST12-10      ; BR TO ERROR HALT ON SEQ ERROR
719 001156 012700 177777      MOV     #177777,RO    ; MOVE ALL ONES TO RO
720 001162 020027 177777      CMP     RO,#177777    ; SUCCESSFUL?
721 001166 001404      BEQ     TST12

```

```

722                                     ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS      <====
723                                     ; CONDITIONAL BRANCH INST. AND                <====
724                                     ; REPLACE THE MOVE INSTRUCTION                <====
725                                     ; WHICH FOLLOWS W/ 773                        <====

```

```

726 001170 012742 000014      MOV     #14,-(R2)      ; MOVE TO MAILBOX # ***** 14 *****
727 001174 005242      INC     -(R2)          ; SET MSGTYP TO FATAL ERROR
728 001176 000000      HALT                    ; RO NOT 177777
729                                     ; OR SEQUENCE ERROR

```

```

;*****
;TEST 12      TEST IF R1 CAN HOLD A ONE IN ALL BITS
;*****

```

```

731
732
733
734 001200 005212      TST12: INC      (R2)          ; UPDATE TEST NUMBER
735 001202 022712 000012      CMP     #12,(R2)      ; SEQUENCE ERROR?
736 001206 001006      BNE     TST13-10      ; BR TO ERROR HALT ON SEQ ERROR
737 001210 012701 000001      MOV     #1,R1          ; SET BIT 0
738 001214 000241      CLC                    ; CLEAR C-BIT
739 001216 006101      REG1: ROL     R1        ; ROTATE 1 POSITION
740 001220 103376      BCC     REG1           ; ALL DONE
741 001222 001404      BEQ     TST13

```

```

742                                     ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS      <====
743                                     ; CONDITIONAL BRANCH INST. AND                <====
744                                     ; REPLACE THE MOVE INSTRUCTION                <====

```

```

745
746 001224 012742 000015      MOV    #15,-(R2)      ; MOVE TO MAILBOX # ***** 15 *****
747 001230 005242              INC    -(R2)          ; SET MSGTYP TO FATAL ERROR
748 001232 000000              HALT                  ; FAILURE WITH R1
749                                     ; OR SEQUENCE ERROR
750
751 ;*****
752 ;TEST 13      TEST IF R2 CAN HOLD A ONE IN ALL BITS
753 ;*****
754 001234 005212              TST13: INC    (R2)          ; UPDATE TEST NUMBER
755 001236 022712 000013      CMP    #13,(R2)      ; SEQUENCE ERROR?
756 001242 001006              BNE   REG2A-14      ; BR TO ERROR HALT ON SEQ ERROR
757 001244 012702 000001      MOV    #1,R2         ; SET BIT 0
758 001250 000241              CLC                    ; CLEAR C-BIT
759 001252 006102              REG2: ROL    R2         ; ROTATE 1 POSITION
760 001254 103376              BCC   REG2          ; ALL DONE
761 001256 001406              BEQ   REG2A
762                                     ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
763                                     ; BRANCH INSTRUCTION AND
764                                     ; REPLACE THE MOVE INSTRUCTION
765                                     ; FOLLOWING W/ 771
766 001260 012702 000304      MOV    #$TESTN,R2    ; RESTORE POINTER
767 001264 012742 000016      MOV    #16,-(R2)     ; MOVE TO MAILBOX # ***** 16 *****
768 001270 005242              INC    -(R2)          ; SET MSGTYP TO FATAL ERROR
769 001272 000000              HALT                  ; FAILURE WITH R2
770 001274 012702 000304      REG2A: MOV    #$TESTN,R2 ; RESTORE POINTER
771 ;*****
772 ;TEST 14      TEST IF R3 CAN HOLD A ONE IN ALL BITS
773 ;*****
774 001300 005212              TST14: INC    (R2)          ; UPDATE TEST NUMBER
775 001302 022712 000014      CMP    #14,(R2)      ; SEQUENCE ERROR?
776 001306 001006              BNE   TST15-10      ; BR TO ERROR HALT ON SEQ ERROR
777 001310 012703 000001      MOV    #1,R3         ; SET BIT 0
778 001314 000241              CLC                    ; CLEAR C-BIT
779 001316 006103              REG3: ROL    R3         ; ROTATE 1 POSITION
780 001320 103376              BCC   REG3          ; ALL DONE
781 001322 001404              BEQ   TST15
782                                     ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
783                                     ; CONDITIONAL BRANCH INST. AND
784                                     ; REPLACE THE MOVE INSTRUCTION
785                                     ; WHICH FOLLOWS W/ 772
786 001324 012742 000017      MOV    #17,-(R2)     ; MOVE TO MAILBOX # ***** 17 *****
787 001330 005242              INC    -(R2)          ; SET MSGTYP TO FATAL ERROR
788 001332 000000              HALT                  ; FAILURE WITH R3
789                                     ; OR SEQUENCE ERROR
790
791 ;*****
792 ;TEST 15      TEST IF R4 CAN HOLD A ONE IN ALL BITS
793 ;*****
794 001334 005212              TST15: INC    (R2)          ; UPDATE TEST NUMBER
795 001336 022712 000015      CMP    #15,(R2)      ; SEQUENCE ERROR?
796 001342 001006              BNE   TST16-10      ; BR TO ERROR HALT ON SEQ ERROR
797 001344 012704 000001      MOV    #1,R4         ; SET BIT 0
798 001350 000241              CLC                    ; CLEAR C-BIT
799 001352 006104              REG4: ROL    R4         ; ROTATE 1 POSITION
800 001354 103376              BCC   REG4          ; ALL DONE

```

```

801 001356 001404 BEQ TST16
802
803
804
805
806 001360 012742 000020 MOV #20, -(R2)
807 001364 005242 INC -(R2)
808 001366 000000 HALT
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825
826 001414 012742 000021 MOV #21, -(R2)
827 001420 005242 INC -(R2)
828 001422 000000 HALT
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846 001450 012742 000022 MOV #22, -(R2)
847 001454 005242 INC -(R2)
848 001456 000000 HALT
849
850

```

```

: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
: CONDITIONAL BRANCH INST. AND <====
: REPLACE THE MOVE INSTRUCTION <====
: WHICH FOLLOWS W/ 772 <====
: MOVE TO MAILBOX # ***** 20 *****
: SET MSGTYP TO FATAL ERROR
: FAILURE WITH R4
: OR SEQUENCE ERROR

```

```

;*****
;TEST 16 TEST IF R5 CAN HOLD A ONE IN ALL BITS
;*****

```

```

†TST16: INC (R2) ;UPDATE TEST NUMBER
CMP #16, (R2) ;SEQUENCE ERROR?
BNE TST17-10 ;BR TO ERROR HALT ON SEQ ERROR
MOV #1, R5 ;SET BIT 0
CLC ;CLEAR C-BIT
REG5: ROL R5 ;ROTATE 1 POSITION
BCC REG5 ;ALL DONE
BEQ TST17

```

```

: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
: CONDITIONAL BRANCH INST. AND <====
: REPLACE THE MOVE INSTRUCTION <====
: WHICH FOLLOWS W/ 772 <====
: MOVE TO MAILBOX # ***** 21 *****
: SET MSGTYP TO FATAL ERROR
: FAILURE WITH R5
: OR SEQUENCE ERROR

```

```

;*****
;TEST 17 TEST IF R6 CAN HOLD A ONE IN ALL BITS
;*****

```

```

†TST17: INC (R2) ;UPDATE TEST NUMBER
CMP #17, (R2) ;SEQUENCE ERROR?
BNE TST20-10 ;BR TO ERROR HALT ON SEQ ERROR
MOV #1, R6 ;SET BIT 0
CLC ;CLEAR C-BIT
REG6: ROL R6 ;ROTATE 1 POSITION
BCC REG6 ;ALL DONE
BEQ TST20

```

```

: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
: CONDITIONAL BRANCH INST. AND <====
: REPLACE THE MOVE INSTRUCTION <====
: WHICH FOLLOWS W/ 772 <====
: MOVE TO MAILBOX # ***** 22 *****
: SET MSGTYP TO FATAL ERROR
: FAILURE WITH R6
: OR SEQUENCE ERROR

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001460	005212		
001462	022712	000020	
001466	001010		
001470	012706	000500	
001474	012737	000000	177776
001502	005737	177776	
001506	001404		
001510	012742	000023	
001514	005242		
001516	000000		
001520	005212		
001522	022712	000021	
001526	001007		
001530	012737	000252	177776
001536	023727	177776	000252
001544	001404		
001546	012742	000024	
001552	005242		
001554	000000		

```
*****
:SBTTL PSW TESTS
:
: THE PSW TESTS ARE USED TO VERIFY THAT VARIOUS DATA
: PATTERNS CAN BE SUCCESSFULLY HELD IN THE PSE AND THAT THE
: PSW ADDRESSING LOGIC IS FUNCTIONING. MOVE AND COMPARE INSTRUCTIONS
: ARE USED TO TEST THAT THE PSE CAN HOLD VARIOUS DATA PATTERNS.
: EACH DATA PATTERN IS MOVED AND TESTED IN A SMALL LOOP CONVENIENT FOR
: SCOPING.
: THE PSW REGISTER ITSELF IS TESTED AS WELL AS THE ADDRESS
: SELECT CIRCUITRY. THE AMUX INPUTS TO THE PSW MUX ARE TESTED. THE
: CC INPUTS ARE TESTED LATER IN THE MICROCODE TESTS. SETTING OF
: THE T-BIT BY THE TEST PATTERNS IS PURPOSELY AVOIDED; TESTING OF THE
: T-BIT TRAP CIRCUITRY IS LEFT FOR THE TRAP TEST.
:
:*****
:TEST 20 TEST IF PSW WILL HOLD ZEROES
:*****
TST20: INC (R2) ;UPDATE TEST NUMBER
: CMP #20,(R2) ;SEQUENCE ERROR?
: BNE TST21-10 ;BR TO ERROR HALT ON SEQ ERROR
: MOV #STBOT,R6
: MOV #0,#PS ;SET PSW TO ZERO
: TST #PS ;SUCCESSFUL
: BEQ TST21
:
: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
: CONDITIONAL BRANCH INST. AND <====
: REPLACE THE MOVE INSTRUCTION <====
: WHICH FOLLOWS W/ 770 <====
: MOV #23,-(R2) ;MOVE TO MAILBOX # ***** 23 *****
: INC -(R2) ;SET MSGTYP TO FATAL ERROR
: HALT ;PSW NOT 0
: ; OR SEQUENCE ERROR
:
:*****
:TEST 21 TEST IF PSW WILL HOLD ONES AND ZEROES
:*****
TST21: INC (R2) ;UPDATE TEST NUMBER
: CMP #21,(R2) ;SEQUENCE ERROR?
: BNE TST22-10 ;BR TO ERROR HALT ON SEQ ERROR
: MOV #252,#PS ;MOVE ALT. ONES AND ZEROES TO PSW
: CMP #PS,#252 ;SUCCESSFUL?
: BEQ TST22
:
: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
: CONDITIONAL BRANCH INST. AND <====
: REPLACE THE MOVE INSTRUCTION <====
: WHICH FOLLOWS W/ 771 <====
: MOV #24,-(R2) ;MOVE TO MAILBOX # ***** 24 *****
: INC -(R2) ;SET MSGTYP TO FATAL ERROR
: HALT ;PSW NOT 252
: ; OR SEQUENCE ERROR
:
:*****
:TEST 22 TEST IF PSW (EXCEPT T-BIT) WILL HOLD ZEROES AND ONES
:*****
```

```

907 001556 005212          TST22: INC      (R2)          ;UPDATE TEST NUMBER
908 001560 022712 000022    CMP      #22,(R2)        ;SEQUENCE ERROR?
909 001564 001007          BNE     TST23-10        ;BR TO ERROR HALT ON SEQ ERROR
910 001566 012737 000105 177776  MOV     #105,2#PS      ;MOVE ALT. ONES AND ZEROES TO PSW
911 001574 023727 177776 000105  CMP     2#PS,#105      ;SUCCESSFUL?
912 001602 001404          BEQ     TST23
913
914
915
916
917 001604 012742 000025    MOV     #25,-(R2)      ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
918 001610 005242          INC     -(R2)          ; CONDITIONAL BRANCH INST. AND <====
919 001612 000000          HALT                    ; REPLACE THE MOVE INSTRUCTION <====
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934
935 001642 012742 000026    MOV     #26,-(R2)      ; MOVE TO MAILBOX # ***** 26 *****
936 001646 005242          INC     -(R2)          ; SET MSGTYP TO FATAL ERROR
937 001650 000000          HALT                    ; PSW NOT 105
938

```

```

;*****
;TEST 23 TEST IF PSW (EXCEPT T-BIT) WILL HOLD ALL ONES
;*****

```

```

925 001614 005212          TST23: INC      (R2)          ;UPDATE TEST NUMBER
926 001616 022712 000023    CMP     #23,(R2)        ;SEQUENCE ERROR?
927 001622 001007          BNE     TST24-10        ;BR TO ERROR HALT ON SEQ ERROR
928 001624 012737 000357 177776  MOV     #357,2#PS      ;MOVE ONES TO PSW
929 001632 023727 177776 000357  CMP     2#PS,#357      ;SUCCESSFUL
930 001640 001404          BEQ     TST24
931
932
933
934
935 001642 012742 000026    MOV     #26,-(R2)      ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
936 001646 005242          INC     -(R2)          ; CONDITIONAL BRANCH INST. AND <====
937 001650 000000          HALT                    ; REPLACE THE MOVE INSTRUCTION <====
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:SBTTL B-REGISTER TEST

: THE B-REGISTER SHIFTING LOGIC TESTS ARE USED TO TEST THAT THE
: B-REGISTER CAN HOLD VARIOUS DATA PATTERNS AND THAT THE ASSOCIATED
: LOGIC SUPPORTS THE SHIFTING FUNCTIONS WITHIN THE B-REGISTER AND C-BIT.
: A ONE IS SHIFTED THROUGH EVERY BIT IN THE B-REGISTER AND C-BIT IN
: BOTH DIRECTIONS.

: THE B-REGISTER ITSELF IS TESTED IN ITS ABILITY AS A BUFFER AND AS
: A SHIFT REGISTER. DATA IS ALSO PASSED THROUGH THE DATA PATH AND ALU.
: IF THESE TESTS FAIL, EXAMINE THE TARGET LOCATION (LOC. 0) TO SEE
: WHICH BITS OF THE B-REGISTER MAY BE FAILING. IF THIS PROVIDES
: INCONCLUSIVE DATA TRY TO CHECK THE MODE 3 IR DECODE BY RUNNING JUST
: THE MICROCODE AND IR DECODE TESTS FOR THE PARTICULAR INSTRUCTIONS.

:TEST 24 SHIFT BIT 0 TO BIT 1

TST24: INC (R2) ;UPDATE TEST NUMBER
CMP #24,(R2) ;SEQUENCE ERROR?
BNE TST25-10 ;BR TO ERROR HALT ON SEQ ERROR
CLC ;CLEAR CARRY BIT
MOV #1,A#0 ;LOAD A 1
ROL A#0 ;SHIFT LEFT
CMP #2,A#0 ;SUCCESSFUL
BEQ TST25
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 766 <====
MOV #27,-(R2) ;MOVE TO MAILBOX # ***** 27 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;BIT 1 NOT SET
; OR SEQUENCE ERROR

:TEST 25 SHIFT CARRY INTO BIT 0

TST25: INC (R2) ;UPDATE TEST NUMBER
CMP #25,(R2) ;SEQUENCE ERROR?
BNE TST26-10 ;BR TO ERROR HALT ON SEQ ERROR
MOV #0,A#0 ;CLEAR LOCATION
SEC ;SET CARRY
ROL A#0 ;ROTATE CARRY BIT TO BIT 0
BCC TST26
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 771 <====
MOV #30,-(R2) ;MOVE TO MAILBOX # ***** 30 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;CARRY CLEAR
; OR SEQUENCE ERROR
CMP #1,A#0 ;BIT 0 SET
BEQ TST26

```

995
996
997
998
999 001764 012742 000031      MOV    #31,-(R2)      ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
1000 001770 005242      INC    -(R2)         ; CONDITIONAL BRANCH INST. AND
1001 001772 000000      HALT                ; REPLACE THE MOVE INSTRUCTION
                                ; WHICH FOLLOWS W/ 761
                                ; MOVE TO MAILBOX # ***** 31 *****
                                ; SET MSGTYP TO FATAL ERROR
                                ; BIT 0 NOT SET
                                ; OR SEQUENCE ERROR

```

```

1002
1003
1004
1005 ;*****
;TEST 26      LEFT SHIFT FROM BIT 0 TO C-BIT
;*****

```

```

1006
1007 001774 005212      TST26: INC    (R2)      ; UPDATE TEST NUMBER
1008 001776 022712 000026      CMP    #26,(R2)     ; SEQUENCE ERROR?
1009 002002 001010      BNE    TST27-10     ; BR TO ERROR HALT ON SEQ ERROR
1010 002004 012737 000001 000000      MOV    #1,#0        ; SET BIT 0
1011 002012 000241      CLC                    ; CLEAR C-BIT
1012 002014 006137 000000      SHL:  ROL    #0      ; SHIFT LEFT ONE POSITION
1013 002020 103375      BCC    SHL           ; BRANCH IF C-BIT NOT SET
1014 002022 001404      BEQ    TST27

```

```

1015
1016 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
1017 ; CONDITIONAL BRANCH INST. AND
1018 ; REPLACE THE MOVE INSTRUCTION
1019 ; WHICH FOLLOWS W/ 770
1019 002024 012742 000032      MOV    #32,-(R2)     ; MOVE TO MAILBOX # ***** 32 *****
1020 002030 005242      INC    -(R2)         ; SET MSGTYP TO FATAL ERROR
1021 002032 000000      HALT                ; LEFT SHIFTING LOGIC FAILED
                                ; OR SEQUENCE ERROR

```

```

1022
1023 ;*****
;TEST 27      SHIFT BIT 15 TO BIT 14
;*****

```

```

1024
1025
1026
1027 002034 005212      TST27: INC    (R2)      ; UPDATE TEST NUMBER
1028 002036 022712 000027      CMP    #27,(R2)     ; SEQUENCE ERROR?
1029 002042 001012      BNE    TST30-10     ; BR TO ERROR HALT ON SEQ ERROR
1030 002044 012737 100000 000000      MOV    #100000,#0   ; SET BIT 15
1031 002052 000241      CLC                    ; CLEAR CARRY
1032 002054 006037 000000      ROR    #0            ; SHIFT BIT 15 TO BIT 14
1033 002060 022737 040000 000000      CMP    #40000,#0    ; SUCCESSFUL
1034 002066 001404      BEQ    TST30

```

```

1035
1036 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
1037 ; CONDITIONAL BRANCH INST. AND
1038 ; REPLACE THE MOVE INSTRUCTION
1039 ; WHICH FOLLOWS W/ 766
1039 002070 012742 000033      MOV    #33,-(R2)     ; MOVE TO MAILBOX # ***** 33 *****
1040 002074 005242      INC    -(R2)         ; SET MSGTYP TO FATAL ERROR
1041 002076 000000      HALT                ; BIT 14 NOT SET
                                ; OR SEQUENCE ERROR

```

```

1042
1043 ;*****
;TEST 30      RIGHT SHIFT FROM BIT 15 TO C-BIT
;*****

```

```

1044
1045
1046
1047 002100 005212      TST30: INC    (R2)      ; UPDATE TEST NUMBER
1048 002102 022712 000030      CMP    #30,(R2)     ; SEQUENCE ERROR?
1049 002106 001010      BNE    TST31-10     ; BR TO ERROR HALT ON SEQ ERROR
1050 002110 012737 100000 000000      MOV    #100000,#0   ; SET BIT 15

```

1051	002116	000241	
1052	002120	006037	000000
1053	002124	103375	
1054	002126	001404	
1055			
1056			
1057			
1058			
1059	002130	012742	000034
1060	002134	005242	
1061	002136	000000	
1062			

SHR: CLC
ROR
BCC
BEQ

0#0
SHR
TST31

```

;CLEAR C-BIT
;ROTATE RIGHT ONE POSITION
;BRANCH IF C-BIT CLEAR

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
;              CONDITIONAL BRANCH INST. AND
;              REPLACE THE MOVE INSTRUCTION
;              WHICH FOLLOWS W/ 770
;MOVE TO MAILBOX # ***** 34 *****
;SET MSGTYP TO FATAL ERROR
;RIGHT SHIFT LOGIC FAILED
; OR SEQUENCE ERROR
  
```

.SBTTL CONDITION CODE TEST

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1080
1081 002140 005212
1082 002142 022712 000031
1083 002146 001014
1084
1085 002150 000257
1086 002152 000264
1087 002154 001001
1088 002156 001404
1089
1090
1091
1092
1093 002160
1094 002160 012742 000035
1095 002164 005242
1096 002166 000000
1097
1098 002170 000277
1099 002172 000244
1100 002174 001401
1101 002176 001004
1102
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1104
1105
1106 002200
1107 002200 012742 000036
1108 002204 005242
1109 002206 000000
1110

```

*****
THIS TEST CHECKS THE CONDITIONAL BRANCHES INVOLVING THE Z-BIT.
THE Z-BIT IS SET WITH ALL OTHER CC BITS ZERO AND BOTH CONDITIONS
BEQ AND BNE ARE TESTED FOR PROPER EXECUTION. THEN THE Z-BIT IS
SET WITH ALL OTHER CC BITS CLEAR AND BOTH CONDITIONS ARE TESTED
AGAIN FOR PROPER OPERATION.
THIS TEST CHECKS THE OPERATION OF THE SET AND CLEAR CONDITION
CODE INSTRUCTIONS AND CHECKS THE CIRCUITRY EXTERNAL TO THE CONDITIONAL
BRANCH ROM. THE BRANCH MICROCODE FOR ALTERING THE PC AND FOR
LEAVING THE PC UNALTERED IS TESTED. ONLY THOSE ROM ADDRESSES SPECIFICALLY
USED IN THE TEST ARE VERIFIED HERE.
*****
TEST 31 TEST BRANCHES AROUND Z-BIT
*****
TST31: INC (R2) ;UPDATE TEST NUMBER
CMP #31,(R2) ;SEQUENCE ERROR?
BNE TST32-10 ;BR TO ERROR HALT ON SEQ ERROR
;FIRST WITH Z-BIT ON
CCC ;CC=0100: JUST Z-BIT
SEZ
BNE BRZ1 ;CHECK OPPOSITE CONDITION
BEQ BRZ2
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 774 <====

BRZ1: MOV #35,-(R2) ;MOVE TO MAILBOX # ***** 35 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;IMPROPER BR W/ Z=1
;CHECK WITH Z-BIT OFF

BRZ2: SCC ;CC=1011: ALL BUT Z-BIT
CLZ
BEQ BRZ3
BNE TST32
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 764 <====

BRZ3: MOV #36,-(R2) ;MOVE TO MAILBOX # ***** 36 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;IMPROPER BR W/ Z=0
; OR SEQUENCE ERROR

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1128 002210 005212
1129 002212 022712 000032
1130 002216 001014
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1132 002220 000257
1133 002222 000270
1134 002224 100001
1135 002226 100404
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1140 002230
1141 002230 012742 000037
1142 002234 005242
1143 002236 000000
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1145 002240 000277
1146 002242 000250
1147 002244 100401
1148 002246 100004
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1153 002250
1154 002250 012742 000040
1155 002254 005242
1156 002256 000000
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:*****
:
:   THIS TEST CHECKS THE CONDITIONAL BRANCHES INVOLVING THE N-BIT.
: THE N-BIT IS SET WITH ALL OTHER CC BITS ZERO AND BOTH CONDITIONS
: BMI AND BPL ARE TESTED FOR PROPER EXECUTION. THEN THE N-BIT IS
: SET WITH ALL OTHER CC BITS CLEAR AND BOTH CONDITIONS ARE TESTED
: AGAIN FOR PROPER OPERATION.
:   THIS TEST CHECKS THE OPERATION OF THE SET AND CLEAR CONDITION
: CODE INSTRUCTIONS AND CHECKS THE CIRCUITRY EXTERNAL TO THE CONDITIONAL
: BRANCH ROM. THE BRANCH MICROCODE FOR ALTERING THE PC AND FOR
: LEAVING THE PC UNALTERED IS TESTED. ONLY THOSE ROM ADDRESSES SPECIFICALLY
: USED IN THE TEST ARE VERIFIED HERE.
:*****
:TEST 32      TEST BRANCHES AROUND N-BIT
:*****
TST32:  INC      (R2)          ;UPDATE TEST NUMBER
        CMP      #32,(R2)    ;SEQUENCE ERROR?
        BNE     TST33-10    ;BR TO ERROR HALT ON SEQ ERROR
        ;FIRST WITH N-BIT ON
        CCC
        SEN
        BPL     BRN1        ;CHECK OPPOSITE CONDITION
        BMI     BRN2
        ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
        ;          CONDITIONAL BRANCH INST. AND <====
        ;          REPLACE THE MOVE INSTRUCTION <====
        ;          WHICH FOLLOWS W/ 774 <====
BRN1:  MOV      #37,-(R2)    ;MOVE TO MAILBOX # ***** 37 *****
        INC      -(R2)      ;SET MSGTYP TO FATAL ERROR
        HALT
        ;CHECK WITH N-BIT OFF
        ;IMPROPER BR W/ N=1
BRN2:  SCC
        CLN
        BMI     BRN3        ;CHECK OPPOSITE CONDITION
        BPL     TST33
        ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
        ;          CONDITIONAL BRANCH INST. AND <====
        ;          REPLACE THE MOVE INSTRUCTION <====
        ;          WHICH FOLLOWS W/ 764 <====
BRN3:  MOV      #40,-(R2)    ;MOVE TO MAILBOX # ***** 40 *****
        INC      -(R2)      ;SET MSGTYP TO FATAL ERROR
        HALT
        ;IMPROPER BR W/ N=0
        ; OR SEQUENCE ERROR

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002260 005212
002262 022712 000033
002266 001014
002270 000257
002272 000262
002274 102001
002276 102404
002300
002300 012742 000041
002304 005242
002306 000000
002310 000277
002312 000242
002314 102401
002316 102004
002320
002320 012742 000042
002324 005242
002326 000000

```
*****
THIS TEST CHECKS THE CONDITIONAL BRANCHES INVOLVING THE V-BIT.
THE V-BIT IS SET WITH ALL OTHER CC BITS ZERO AND BOTH CONDITIONS
BVS AND BVC ARE TESTED FOR PROPER EXECUTION. THEN THE V-BIT IS
SET WITH ALL OTHER CC BITS CLEAR AND BOTH CONDITIONS ARE TESTED
AGAIN FOR PROPER OPERATION.
THIS TEST CHECKS THE OPERATION OF THE SET AND CLEAR CONDITION
CODE INSTRUCTIONS AND CHECKS THE CIRCUITRY EXTERNAL TO THE CONDITIONAL
BRANCH ROM. THE BRANCH MICROCODE FOR ALTERING THE PC AND FOR
LEAVING THE PC UNALTERED IS TESTED. ONLY THOSE ROM ADDRESSES SPECIFICALLY
USED IN THE TEST ARE VERIFIED HERE.
*****
TEST 33 TEST BRANCHES AROUND V-BIT
*****
TST33: INC (R2) ;UPDATE TEST NUMBER
CMP #33,(R2) ;SEQUENCE ERROR?
BNE TST34-10 ;BR TO ERROR HALT ON SEQ ERROR
;FIRST WITH V-BIT ON
CCC ;CC=0010: JUST V-BIT
SEV
BVC BRV1 ;CHECK OPPOSITE CONDITION
BVS BRV2
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 774 <====
BRV1: MOV #41,-(R2) ;MOVE TO MAILBOX # ***** 41 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;IMPROPER BR W/ V=1
;CHECK WITH V-BIT OFF
BRV2: SCC ;CC=1101: ALL BVT V-BIT
CLV
BVS BRV3 ;CHECK OPPOSITE CONDITION
BVC TST34
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 764 <====
BRV3: MOV #42,-(R2) ;MOVE TO MAILBOX # ***** 42 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;IMPROPER BR W/ V=0
; OR SEQUENCE ERROR
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002330 005212
002332 022712 000034
002336 001014
002340 000257
002342 000261
002344 103001
002346 103404
002350
002350 012742 000043
002354 005242
002356 000000
002360 000277
002362 000242
002364 102401
002366 100404
002370
002370 012742 000044
002374 005242
002376 000000

```
*****
THIS TEST CHECKS THE CONDITIONAL BRANCHES INVOLVING THE C-BIT.
THE C-BIT IS SET WITH ALL OTHER CC BITS ZERO AND BOTH CONDITIONS
BCS AND BCC ARE TESTED FOR PROPER EXECUTION. THEN THE C-BIT IS
SET WITH ALL OTHER CC BITS CLEAR AND BOTH CONDITIONS ARE TESTED
AGAIN FOR PROPER OPERATION.
THIS TEST CHECKS THE OPERATION OF THE SET AND CLEAR CONDITION
CODE INSTRUCTIONS AND CHECKS THE CIRCUITRY EXTERNAL TO THE CONDITIONAL
BRANCH ROM. THE BRANCH MICROCODE FOR ALTERING THE PC AND FOR
LEAVING THE PC UNALTERED IS TESTED. ONLY THOSE ROM ADDRESSES SPECIFICALLY
USED IN THE TEST ARE VERIFIED HERE.
*****
TEST 34 TEST BRANCHES AROUND C-BIT
*****
TST34: INC (R2) ;UPDATE TEST NUMBER
CMP #34,(R2) ;SEQUENCE ERROR?
BNE TST35-10 ;BR TO ERROR HALT ON SEQ ERROR
;FIRST WITH C-BIT ON
CCC ;CC=0001: JUST C-BIT
SEC
BCC BRC1 ;CHECK OPPOSITE CONDITION
BCS BRC2
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 774 <====
BRC1: MOV #43,-(R2) ;MOVE TO MAILBOX # ***** 43 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;IMPROPER BR W/ C=1
;CHECK WITH V-BIT OFF
BRC2: SCC ;CC=1110
CLV
BVS BRC3 ;CHECK OPPOSITE CONDITION
BMI TST35
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 764 <====
BRC3: MOV #44,-(R2) ;MOVE TO MAILBOX # ***** 44 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;IMPROPER BR W/ C=0
; OR SEQUENCE ERROR
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*****  
:SBTTL MICROCODE TESTS  
:  
: THE MICROCODE TESTS ARE USED TO VERIFY THE MICROPROGRAMM  
: FLOW. THE GOAL OF THESE TESTS IS TO EXERCISE EVERY POSSIBLE  
: BRANCH IN THE MICROPROGRAM FLOW.  
: THE TEST EXERCISES EVERY BRANCH IN THE MICROCODE BY  
: TESTING AT LEAST ONE INSTRUCTION FROM EVERY CLASS OF INSTRUCTION IN  
: ALL POSSIBLE MODES. FOR EXAMPLE, TO TEST THE SINGLE OPERAND INSTRUCTIONS,  
: AT LEAST ONE SINGLE OPERAND INSTRUCTION IS VERIFIED IN ALL UNIQUE  
: ADDRESSING MODES. BYTE MODES ARE ALSO TESTED. AS EACH NEW  
: MODE IS INTRODUCED THE SAME INSTRUCTION IS TRIED AND TESTED IN  
: A SMALL LOOP CONVENIENT FOR SCOPING. THE TEST IS SET UP USING  
: ONLY INSTRUCTIONS AND ADDRESSING MODES WHICH HAVE BEEN PREVIOUSLY  
: VERIFIED.  
: IF THESE TESTS FAIL, CHECK THE RESULTS FOR A CLUE TO THE  
: FAULT.  
:*****
```

```
*****  
: THE CLR INSTRUCTION IS USED TO INTRODUCE EACH ADDRESSING  
: MODE WITH THE SINGLE OPERAND INSTRUCTION. FOLLOWING THE SEQUENCE CHECK,  
: THE CLR INSTRUCTION IS EXECUTED AND A BRANCH TEST IS EXECUTED WHICH  
: CHECKS THAT THE Z-BIT WAS PROPERLY SET. THIS SMALL TEST IS SELF-SUFFICIENT  
: AND CAN BE SCOPED TO TROUBLE SHOOT ALL OF THE IR DECODE LOGIC AND  
: MICROCODE FOR SOP INSTRUCTIONS WITH MODE 0. FOLLOWING THIS TEST  
: SEVERAL OTHER SOP INSTRUCTIONS ARE INTRODUCED WITH MODE 0. THESE  
: INSTRUCTIONS MAINPULATE DATA AND SERVE TO CHECK THE DATA RESULTS  
: OF THE SOP INSTRUCTIONS IN THIS TEST. THE DATA IN THIS TEST IS  
: OPERATED ON BY EACH INSTRUCTION WITHOUT REINITIALIZING.  
:*****
```

```
*****  
:TEST 35 TEST MODE 0 USING SOP INST.  
:*****
```

1291 002400 005212
1292 002402 022712 000035
1293 002406 001017
1294 002410 005000
1295 002412 001404
1296
1297
1298
1299
1300 002414 012742 000045
1301 002420 005242
1302 002422 000000
1303 002424 005200
1304 002426 005400
1305 002430 100404
1306
1307

```
TST35: INC (R2) ;UPDATE TEST NUMBER  
: CMP #35,(R2) ;SEQUENCE ERROR?  
: BNE TST36-10 ;BR TO ERROR HALT ON SEQ ERROR  
: CLR R0 ;TRY THE CLEAR INST.  
: BEQ SOP0A  
: ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====  
: ; CONDITIONAL BRANCH INST. AND <====  
: ; REPLACE THE MOVE INSTRUCTION <====  
: ; WHICH FOLLOWS W/ 776 <====  
: ; MOVE TO MAILBOX # ***** 45 *****  
: ; SET MSGTYP TO FATAL ERROR  
: ; CLR DID NOT SET Z-BIT  
SOP0A: INC R0 ;TRY THE INCREMENT INST.  
: NEG R0 ;TRY THE NEGATE INST.  
: BMI SOP0B  
: ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====  
: ; CONDITIONAL BRANCH INST. AND <====
```

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1308                                     ; REPLACE THE MOVE INSTRUCTION <====
1309                                     ; WHICH FOLLOWS W/ 767 <====
1310 002432 012742 000046                MOV #46, -(R2) ; MOVE TO MAILBOX # ***** 46 *****
1311 002436 005242                       INC -(R2) ; SET MSGTYP TO FATAL ERROR
1312 002440 000000                       HALT ; NEGATE DID NOT SET N-BIT
1313 002442 005100                SOPOB: COM R0 ; TRY COMPLEMENT INST.
1314 002444 001404                BEQ TST36
1315                                     ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
1316                                     ; CONDITIONAL BRANCH INST. AND <====
1317                                     ; REPLACE THE MOVE INSTRUCTION <====
1318                                     ; WHICH FOLLOWS W/ 761 <====
1319 002446 012742 000047                MOV #47, -(R2) ; MOVE TO MAILBOX # ***** 47 *****
1320 002452 005242                       INC -(R2) ; SET MSGTYP TO FATAL ERROR
1321 002454 000000                       HALT ; CUMMULATIVE RESULT OF CLR, INC, NEG AND COM INSTS. FAILED
1322                                     ; OR SEQUENCE ERROR
1323
1324
1325 *****
1326
1327                                     ; THIS TEST INTRODUCES THE REMAINING SOP INSTRUCTIONS AND TESTS
1328 ; THEM IN MODE 0. THE PURPOSE IS TO PROVIDE A BASELINE OF
1329 ; INSTRUCTIONS FOR USE IN THE SUBSEQUENT TESTS. SINCE THE MICROCODE FOR
1330 ; THESE INSTRUCTIONS IS IDENTICAL TO THAT ALREADY TESTED, ANY TROUBLE
1331 ; SHOOTING EFFORTS SHOULD BE AIMED AT THE ACTUAL IR DECODE AND ALU
1332 ; FUNCTIONING.
1333 *****
1334
1335 ; TEST 36 TEST REMAINDER OF SOP INSTS IN MODE 0
1336 *****
1337 002456 005212 000036                TST36: INC (R2) ; UPDATE TEST NUMBER
1338 002460 022712                       CMP #36, (R2) ; SEQUENCE ERROR?
1339 002464 001020                       BNE TST37-10 ; BR TO ERROR HALT ON SEQ ERROR
1340 002466 005000                       CLR R0 ; INITIALIZE
1341 002470 005300                       DEC R0 ; TRY DECREMENT INST.
1342 002472 100404                       BMI SOPDC
1343                                     ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
1344                                     ; CONDITIONAL BRANCH INST. AND <====
1345                                     ; REPLACE THE MOVE INSTRUCTION <====
1346                                     ; WHICH FOLLOWS W/ 775 <====
1347 002474 012742 000050                MOV #50, -(R2) ; MOVE TO MAILBOX # ***** 50 *****
1348 002500 005242                       INC -(R2) ; SET MSGTYP TO FATAL ERROR
1349 002502 000000                       HALT ; N-BIT NOT SET ON DEC
1350 002504 000261                SOPOC: SEC ; INITIALIZE CARRY
1351 002506 005500                       ADC R0 ; TRY ADD CARRY INST
1352 002510 001006                       BNE SOPDC
1353 002512 000261                       SEC ; INITIALIZE CARRY
1354 002514 005600                       SBC R0 ; TRY SUBTRACT-CARRY INST
1355 002516 100003                       BPL SOPDC
1356 002520 005400                       NEG R0
1357 002522 005300                       DEC R0
1358 002524 001404                       BEQ TST37
1359                                     ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
1360                                     ; CONDITIONAL BRANCH INST. AND <====
1361                                     ; REPLACE THE MOVE INSTRUCTION <====
1362                                     ; WHICH FOLLOWS W/ 760 <====
1363 002526                SOPOD:

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1364 002526 012742 000051
1365 002532 005242
1366 002534 000000
1367

MOV #51, -(R2)
INC -(R2)
HALT

; MOVE TO MAILBOX # ***** 51 *****
; SET MSGTYP TO FATAL ERROR
; CUMMULATIVE RESULT OF ADC, SBC, NEG AND DEC INSTS. FAILE
; OR SEQUENCE ERROR

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1378 002536 005212
1379 002540 022712 000037
1380 002544 001012
1381 002546 105000
1382 002550 001404
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1387 002552 012742 000052
1388 002556 005242
1389 002560 000000
1390 002562 105100
1391 002564 100002
1392 002566 105200
1393 002570 001404
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1398 002572
1399 002572 012742 000053
1400 002576 005242
1401 002600 000000
1402

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```

:*****
:
:   THIS TEST INTRODUCES THE BYTE CONTROL LOGIC OF THE PROCESSOR.
: THE MODE 0 BYTE MICROCODE IS TESTED.  THE METHOD AND SEQUENCE
: OF TESTING IS THE SAME AS THAT USED IN THE SOP MODE 0 TESTS.
:
:*****
: TEST 37          TEST MODE 0 EVEN BYTE USING SOP INST
:*****
TST37:  INC      (R2)          ;UPDATE TEST NUMBER
        CMP      #37,(R2)     ;SEQUENCE ERROR?
        BNE     TST40-10     ;BR TO ERROR HALT ON SEQ ERROR
        CLRB    R0           ;TRY CLEARING EVEN BYTE OF REGISTER
        BEQ     SOPB0A
:
:   TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
:             CONDITIONAL BRANCH INST. AND <====
:             REPLACE THE MOVE INSTRUCTION <====
:             WHICH FOLLOWS W/ 776 <====
:
:             MOV      #52,-(R2) ;MOVE TO MAILBOX # ***** 52 *****
:             INC      -(R2)     ;SET MSGTYP TO FATAL ERROR
:             HALT
SOPB0A: COMB     R0           ;CLRB DID NOT SET Z-BIT
        BPL     SOPB0B
        INCB    R0           ;TRY SETTING EVEN BYTE OF REGISTER
        BEQ     TST40
:
:   TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
:             CONDITIONAL BRANCH INST. AND <====
:             REPLACE THE MOVE INSTRUCTION <====
:             WHICH FOLLOWS W/ 766 <====
:
:             MOV      #53,-(R2) ;MOVE TO MAILBOX # ***** 53 *****
:             INC      -(R2)     ;SET MSGTYP TO FATAL ERROR
:             HALT
SOPB0B:          ;TEST CUMMULATIVE RESULT OF ABOVE BYTE INST.
:             OR SEQUENCE ERROR
:

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002602 005212
 002604 022712 000040
 002610 001014
 002612 005000
 002614 005010
 002616 001404
 012742 000054
 002624 005242
 002626 000000
 002630 005310
 002632 100003
 002634 000261
 002636 005510
 002640 001404
 002642
 002642 012742 000055
 002646 005242
 002650 000000

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*****
: THIS TEST USES THE CLR INSTRUCTION TO INTRODUCE AND TEST
: SINGLE OPERAND MODE 1 INSTRUCTIONS. AGAIN, THE CLR INSTRUCTION
: IS USED TO INTRODUCE THE MICROCODE AND TO TEST THAT THE PROPER
: CONDITION CODES ARE SET. OTHER SOP INSTRUCTIONS ARE USED TO MANIPULATE
: COMMON DATA TO VERIFY THAT THE CORRECT DATA IS PRODUCED.
*****
: TEST 40 TEST MODE 1 USING SOP INST.
*****
TST40: INC (R2) ; UPDATE TEST NUMBER
      CMP #40,(R2) ; SEQUENCE ERROR?
      BNE TST41-10 ; BR TO ERROR HALT ON SEQ ERROR
      CLR R0 ; INITIALIZE R0
      CLR (R0) ; TRY CLEAR INST W/MODE 1
      BEQ SOP1A
      ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
      ; CONDITIONAL BRANCH INST. AND <====
      ; REPLACE THE MOVE INSTRUCTION <====
      ; WHICH FOLLOWS W/ 775 <====
      MOV #54,-(R2) ; MOVE TO MAILBOX # ***** 54 *****
      INC -(R2) ; SET MSGTYP TO FATAL ERROR
      HALT ; CLR DID NOT SET Z-BIT
SOP1A: DEC (R0) ; TRY DECREMENT INST W/MODE 1
      BPL SOP1B
      SEC ; INITIALIZE CARRY
      ADC (R0) ; TRY ADD-CARRY W/MODE 1
      BEQ TST41
      ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
      ; CONDITIONAL BRANCH INST. AND <====
      ; REPLACE THE MOVE INSTRUCTION <====
      ; WHICH FOLLOWS W/ 764 <====
SOP1B: MOV #55,-(R2) ; MOVE TO MAILBOX # ***** 55 *****
      INC -(R2) ; SET MSGTYP TO FATAL ERROR
      HALT ; TEST CUMMULATIVE RESULT OF ABOVE INST
      ; OR SEQUENCE ERROR
    
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*****
THIS TEST VERIFIES THE BYTE INSTRUCTION MICROCODE FOR MODE 1
SINGLE OPERAND INSTRUCTIONS.
THIS IS THE FIRST PLACE THE SIGN EXTEND LOGIC IS EXERCISED
AND VERIFIED.
*****
    
```

```

*****
TEST 41 TEST MODE 1 EVEN BYTE USING SOP INST
*****
    
```

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002652 005212 000041
002654 022712
002660 001017
002662 005000
002664 005010
002666 005110
002670 105010
002672 001404
    
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TST41: INC (R2)
        CMP #41,(R2)
        BNE TST42-10
        CLR R0
        CLR (R0)
        COM (R0)
        CLRB (R0)
        BEQ SOPB1A
    
```

```

;UPDATE TEST NUMBER
;SEQUENCE ERROR?
;BR TO ERROR HALT ON SEQ ERROR
;INITIALIZE R0
;INITIALIZE LOC. 0
;TRY TO CLEAR BYTE 0
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 773 <====
    
```

```

002674 012742 000056
002700 005242
002702 000000
002704 005210
002706 100004
002710 105410
002712 100002
002714 105210
002716 001404
    
```

```

MOV #56,-(R2)
INC -(R2)
HALT
SOPB1A: INC (R0)
        BPL SOPB1B
        NEGB (R0)
        BPL SOPB1B
        INCB (R0)
        BEQ TST42
    
```

```

;MOVE TO MAILBOX # ***** 56 *****
;SET MSGTYP TO FATAL ERROR
;CLRB DID NOT SET Z-BIT
;INCREMENT TO TEST WORD
;NEGATE: ODD BYTE=377
;INCREMENT ODD BYTE=0
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 761 <====
    
```

```

002720 012742 000057
002720 005242
002724 000000
    
```

```

SOPB1B: MOV #57,-(R2)
        INC -(R2)
        HALT
    
```

```

;MOVE TO MAILBOX # ***** 57 *****
;SET MSGTYP TO FATAL ERROR
;CHECK CUMMULATIVE RESULT OF ABOVE INST
; OR SEQUENCE ERROR
    
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002730 005212
002732 022712 000042
002736 001021
002740 005000
002742 005010
002744 005110
002746 005200
002750 105010
002752 001404

012742 000060
005242
000000
005300
005210
005200
105410
100002
105210
001404

003002 012742 000061
003006 005242
003010 000000

```
*****
: THIS TEST VERIFIES THAT SINGLE OPERAND BYTE INSTRUCTIONS WILL
: FUNCTION CORRECTLY FOR ODD BYTES.
: THIS IS THE FIRST TIME THAT ADDRESS LINE 0 HAS BEEN
: EXERCISED. CHECKS ARE MADE THAT THE PROPER BYTE IS MODIFIED AND
: THE CONDITION CODES ARE CHECKED. IT IS ALSO VERIFIED THAT THE UNADDRESSED
: BYTE IS NOT ALTERED BY THE INSTRUCTION.
*****
: TEST 42 TEST MODE 1 ODD BYTE USING SOP INST
*****
TST42: INC (R2) ;UPDATE TEST NUMBER
CMP #42,(R2) ;SEQUENCE ERROR?
BNE TST43-10 ;BR TO ERROR HALT ON SEQ ERROR
CLR R0 ;INITIALIZE R0
CLR (R0) ;INITIALIZE LOC. 0
COM (R0)
INC R0 ;R0=ODD BYTE
CLRB (R0) ;TRY TO CLEAR BYTE 1
BEQ SOPB1C
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 772 <====
MOV #60,-(R2) ;MOVE TO MAILBOX # ***** 60 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;CLRB DID NOT SET Z-BIT
SOPB1C: DEC R0 ;R0=WORD ADDR.
INC (R0) ;INCREMENT TO TEST WORD
INC R0 ;R0=ODD BYTE
NEGB (R0) ;TRY TO NEGATE BYTE 1
BPL SOPB1D
INCB (R0) ;TRY TO INCREMENT BYTE 1
BEQ TST43
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 757 <====
SOPB1D: MOV #61,-(R2) ;MOVE TO MAILBOX # ***** 61 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;TEST CUMMULATIVE RESULT OF ABOVE INST.
; OR SEQUENCE ERROR
```

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1543 003012 005212 000043
1544 003014 022712
1545 003020 001023
1546 003022 005000
1547 003024 105100
1548 003026 005200
1549 003030 005010
1550 003032 005110
1551 003034 005020
1552 003036 001404
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1557 003040 012742 000062
1558 003044 005242
1559 003046 000000
1560 003050 005300
1561 003052 005300
1562 003054 005120
1563 003056 100004
1564 003060 005300
1565 003062 005300
1566 003064 005220
1567 003066 001404
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1572 003070
1573 003070 012742 000063
1574 003074 005242
1575 003076 000000
1576

: THIS TEST VERIFIES MODE 2 SINGLE-OPERAND INSTRUCTIONS. PREVIOUSLY
: TESTED INSTRUCTIONS ARE USED TO SET A POINTER IN R0 TO LOC. 400.
: LOC. 400 IS INITIALIZED TO -1 BEFORE A CLR MODE 2 IS EXECUTED.
: THEN R0 IS DECREMENTED BY TWO TO AGAIN POINT TO 400 BEFORE EACH
: OF SEVERAL MODE 2 INSTRUCTIONS ARE USED TO VERIFY THE DATA RESULTS OF
: THE TEST. THIS PROCEDURE ALSO VERIFIES THE PROPER INCREMENTING OF THE
: REGISTER.

: TEST 43 TEST MODE 2 USING SOP INST.

TST43: INC (R2) ;UPDATE TEST NUMBER
CMP #43,(R2) ;SEQUENCE ERROR?
BNE TST44-10 ;BR TO ERROR HALT ON SEQ ERROR
CLR R0 ;SET R0=400
COMB R0
INC R0
CLR (R0) ;CLEAR 400
COM (R0) ;INITIALIZE: 400=-1
CLR (R0)+ ;TRY CLEARING WITH MODE 2
BEQ SOPZA

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 771 <====

MOV #62,-(R2) ;MOVE TO MAILBOX # ***** 62 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;CLR INST DID NOT SET Z-BIT
SOPZA: DEC R0 ;RESET R0
DEC R0
COM (R0)+ ;TRY COMPLEMENTING WITH MODE 2
BPL SOP2B
DEC R0 ;RESET R0
DEC R0
INC (R0)+ ;TRY INCREMENTING WITH MODE 2
BEQ TST44

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 755 <====

SOP2B: MOV #63,-(R2) ;MOVE TO MAILBOX # ***** 63 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;CHECK CUMMULATIVE RESULT OF ABOVE INST
; OR SEQUENCE ERROR

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003100 005212
003102 022712 000044
003106 001022
003110 005000
003112 105100
003114 005200
003116 005010
003120 005110
003122 105020
003124 001404

003126 012742 000064
003132 005242
003134 000000
003136 005300
003140 005210
003142 105420
003144 100003
003146 005300
003150 105220
003152 001404

003154 012742 000065
003154 005242
003162 000000

```
*****
THIS TEST VERIFIES MODE 2 SINGLE OPERAND INSTRUCTIONS WHICH
ADDRESS EVEN BYTES.  RO IS SET TO 400 AND USED TO INITIALIZE LOCATION
400 TO -1.  CLRB INSTRUCTION IS THEN EXECUTED ON BYTE 400 WITH
MODE 2.
RO IS THEN DECREMENTED BEFORE EACH OF SEVERAL MODE 2 INSTRUCTIONS
WHICH ARE USED TO VERIFY THE DATA RESULTS OF THE TEST.  THIS PROCEDURE ALSO
VERIFIES THE PROPER INCREMENTING OF THE REGISTER.
*****
TEST 44          TEST MODE 2 EVEN BYTE USING SOP INST.
*****
TST44:  INC      (R2)          ;UPDATE TEST NUMBER
        CMP      #44,(R2)     ;SEQUENCE ERROR?
        BNE     TST45-10     ;BR TO ERROR HALT ON SEQ ERROR
        CLR     RO           ;SET RO=400
        COMB    RO
        INC     RO
        CLR     (RO)         ;CLEAR 400
        COM     (RO)         ;INITIALIZE: 400=-1
        CLRB   (RO)+        ;TRY TO CLEAT 400 W/MODE 2
        BEQ    SOPB2A
        ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
        ;          CONDITIONAL BRANCH INST. AND <====
        ;          REPLACE THE MOVE INSTRUCTION <====
        ;          WHICH FOLLOWS W/ 771 <====
        MOV     #64, -(R2)   ;MOVE TO MAILBOX # ***** 64 *****
        INC     -(R2)       ;SET MSGTYP TO FATAL ERROR
        HALT                    ;CLR DID NOT SET Z-BIT
SOPB2A: DEC     RO           ;RESULT RO=400
        INC     (RO)        ;INC 400 TO TEST WORD
        NEGB   (RO)+       ;TRY TO NEGATE EVEN BYTE
        BPL    SOPB2B
        DEC     RO         ;RESET RO=400
        INCB   (RO)+       ;TRY INCREMENT OF EVEN BYTE
        BEQ    TST45
        ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
        ;          CONDITIONAL BRANCH INST. AND <====
        ;          REPLACE THE MOVE INSTRUCTION <====
        ;          WHICH FOLLOWS W/ 756 <====
SOPB2B: MOV     #65, -(R2)   ;MOVE TO MAILBOX # ***** 65 *****
        INC     -(R2)       ;SET MSGTYP TO FATAL ERROR
        HALT                    ;TEST CUMMULATIVE RESULT OF ABOVE INST.
        ; OR SEQUENCE ERROR
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003164 005212
003166 022712 000045
003172 001025
003174 005000
003176 105100
003200 005200
003202 005010
003204 005110
003206 005200
003210 105020
003212 001404

003214 012742 000066
003220 005242
003222 000000
003224 005300
003226 005300
003230 005220
003232 005300
003234 105420
003236 100003
003240 005300
003242 105220
003244 001404

003246 012742 000067
003246 005242
003252 000000

```

:*****
: THIS TEST FOLLOWS THE SAME PROCEDURE DESCRIBED IN THE PREVIOUS
: TEST.  HERE, THE BYTE INSTRUCTION IS USED TO ADDRESS AN ODD BYTE.
:*****
: TEST 45      TEST MODE 2 ODD BYTE USING SOP INST.
:*****
†ST45:  INC      (R2)          ;UPDATE TEST NUMBER
        CMP      #45,(R2)     ;SEQUENCE ERROR?
        BNE     TST46-10     ;BR TO ERROR HALT ON SEQ ERROR
        CLR     RO           ;SET RO=400
        COMB    RO
        INC     RO
        CLR     (RO)         ;CLEAR LOC 400
        COM     (RO)         ;INITIALIZE: 400=-1
        INC     RO           ;RO=ODD BYTE
        CLRB   (RO)+        ;TRY TO CLEAR ODD BYTE
        BEQ    SOPB2C
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
;           CONDITIONAL BRANCH INST. AND <====
;           REPLACE THE MOVE INSTRUCTION <====
;           WHICH FOLLOWS W/ 770 <====
        MOV     #66,-(R2)    ;MOVE TO MAILBOX # ***** 66 *****
        INC     -(R2)
        HALT
SOPB2C: DEC     RO
        DEC     RO
        INC     (RO)+
        DEC     RO
        NEGB   (RO)+
        BPL    SOPB2D
        DEC     RO
        INCB   (RO)+
        BEQ    TST46
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
;           CONDITIONAL BRANCH INST. AND <====
;           REPLACE THE MOVE INSTRUCTION <====
;           WHICH FOLLOWS W/ 753 <====
SOPB2D: MOV     #67,-(R2)    ;MOVE TO MAILBOX # ***** 67 *****
        INC     -(R2)
        HALT
; TEST CUMMULATIVE RESULT OF ABOVE INST.
; OR SEQUENCE ERROR
    
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003256 005212
003260 022712 000046
003264 001020
003266 005000
003270 105100
003272 005200
003274 005010
003276 005030
003300 001404

003302 012742 000070
003306 005242
003310 000000
003312 005300
003314 005300
003316 005130
003320 100002
003322 005230
003324 001404

003326 012742 000071
003326 005242
003332 000000
003334 000000

```
*****
THIS TEST VERIFIES MODE 3 SINGLE OPERAND INSTRUCTIONS. IT
USES LOCATION 0 AS ITS TARGET DATA. A TABLE LOCATED AT LOC. 400
THRU 402 IS USED TO SUPPLY THE ADDRESS OF LOCATION 0 TO THE
INSTRUCTIONS UNDER TEST.
RO IS SET TO 400, THE START OF THE ADDRESS TABLE, AND A CLR
INSTRUCTION IS EXECUTED WITH MODE 3 TO CLEAR LOC. 0. THEN RO
IS DECREMENTED BY TWO AND TWO OTHER MODE 3 INSTRUCTIONS OPERATE ON
LOC. 0 TO VERIFY THE DATA RESULTS OF THE TEST. THE PROPER INCREMENTING
OF THE REGISTER IS ALSO VERIFIED IN THIS MANNER.
IF A FAILURE IS DETECTED BE SURE TO VERIFY THAT THE TABLE
(LOC. 400-402) HAS THE PROPER VALUES (0).
*****
TEST 46 TEST MODE 3 USING SOP INST.
*****
TST46: INC (R2) ;UPDATE TEST NUMBER
CMP #46,(R2) ;SEQUENCE ERROR?
BNE TST47-10 ;BR TO ERROR HALT ON SEQ ERROR
CLR RO ;SET RO=400
COMB RO
INC RO
CLR (RO) ;CLEAR LOC 400
CLR @ (RO)+ ;TRY TO CLEAR LOC 0 USING MODE 3
BEQ SOP3A
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 772 ***** <====
; MOVE TO MAILBOX # ***** 70 *****
; SET MSGTYP TO FATAL ERROR
; CLR DID NOT SET Z-BIT
; RESET RO=400
SOP3A: DEC RO
DEC RO
COM @ (RO)+ ;TRY TO COMPLEMENT LOC 0 OF MODE 3
BPL SOP3B
INC @ (RO)+ ;TRY TO INCREMENT LOC 0 W/MODE 3
BEQ TST47
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 760 ***** <====
SOP3B: MOV #71,-(R2) ;MOVE TO MAILBOX # ***** 71 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;CUMMULATIVE RESULT OF ABOVE INST FAILED
; OR SEQUENCE ERROR
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003336 005212
003340 022712 000047
003344 001026
003346 005004
003350 105104
003352 005204
003354 005000
003356 005010
003360 005110
003362 105034
003364 001404

003366 012742 000072
003372 005242
003374 000000
003376 005304
003400 005304
003402 005234
003404 100006
003406 105434
003410 100004
003412 005304
003414 005304
003416 105234
003420 001404

003422 012742 000073
003426 005242
003430 000000

```
*****
THIS TEST VERIFIES MODE 3 SINGLE OPERAND BYTE INSTRUCTIONS
WHICH ADDRESS EVEN BYTES. AGAIN, THE TARGET LOCATION 0 IS USED
AND THE SAME TABLE AT 400 IS EMPLOYED.
AFTER POINTING R4 TO THE TABLE (400) AND SETTING LOCATION
0 TO -1, A CLRB INSTRUCTION IS USED TO CLEAR BYTE 0.
SEVERAL OTHER MODE 3 INSTRUCTIONS ARE THEN USED WITH THE TABLE
TO VERIFY THE DATA RESULTS AND THE PROPER INCREMENTING OF THE REGISTER.
IF A FAILURE IS DETECTED, BE SURE THAT THE TABLE (LOCATION 400-402) HAS
THE PROPER VALUES (0).
*****
TEST 47 TEST MODE 3 EVEN BYTE USING SOP INST.
*****
TST47: INC (R2) ;UPDATE TEST NUMBER
CMP #47,(R2) ;SEQUENCE ERROR?
BNE TST50-10 ;BR TO ERROR HALT ON SEQ ERROR
CLR R4 ;SET R4=400
COMB R4
INC R4
CLR R0 ;INITIALIZE LOC. 0=-1
CLR (R0)
COM (R0)
CLRB @R4+ ;TRY TO CLEAR EVEN BYTE
BEQ SOPB3A
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 770 <====
MOV #72,-(R2) ;MOVE TO MAILBOX # ***** 72 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;CLRB DID NOT SET Z-BIT
SOPB3A: DEC R4 ;RESET POINTER
DEC R4
INC @R4+ ;TRY INCREMENTING WORD
BPL SOPB3B ;TRY TO NEGATE EVEN BYTE
NEGB @R4+
BPL SOPB3B
DEC R4
DEC R4
INCB @R4+ ;TRY TO INCREMENT EVEN BYTE
BEQ TST50
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 752 <====
SOPB3B: MOV #73,-(R2) ;MOVE TO MAILBOX # ***** 73 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;CUMMULATIVE RESULT OF ABOVE INST FAILED
; OR SEQUENCE ERROR
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1788 003432 005212 000050
1789 003434 022712
1790 003440 001024
1791 003442 005000
1792 003444 105100
1793 003446 005200
1794 003450 005030
1795 003452 005130
1796 003454 105030
1797 003456 001404
1798
1799
1800
1801
1802 003460 012742 000074
1803 003464 005242
1804 003466 000000
1805 003470 005300
1806 003472 005300
1807 003474 005300
1808 003476 005300
1809 003500 005230
1810 003502 105430
1811 003504 100002
1812 003506 105230
1813 003510 001404
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1818 003512 012742 000075
1819 003512 005242
1820 003516 000000
1821 003520
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```
*****
; THIS TEST VERIFIES MODE 3 SINGLE OPERAND BYTE INSTRUCTIONS
; WHICH ADDRESS ODD BYTES. THE TARGET IS BYTE 1. A TABLE AT
; LOC. 400-406 IS USED. R0 SERVES AS THE TABLE POINTER.
; R0 IS INITIALIZED TO 400. LOC. 0 IS SET TO -1 USING THE
; FIRST TWO TABLE ENTRIES. A CLRB MODE 3 IS EXECUTED ON BYTE 1 USING
; TABLE ADDRESS AT 404. R0 IS DECREMENTED TO 402 AND SEVERAL SOP
; MODE 3 INSTRUCTIONS ARE USED TO VERIFY DATA RESULTS AND PROPER
; REGISTER INCREMENTING.
; THE TABLE (400-406) SHOULD CONTAIN 0,0,1,1 BEFORE AND
; AFTER THE TEST IS RUN.
*****
```

```
*****
TEST 50 TEST MODE 3 ODD BYTE USING SOP INST.
*****
```

```
TST50: INC (R2) ; UPDATE TEST NUMBER
; SEQUENCE ERROR?
CMP #50,(R2) ; BR TO ERROR HALT ON SEQ ERROR
BNE TST51-10 ; SET R0=400
CLR R0
COMB R0
INC R0
CLR @ (R0)+ ; INITIALIZE
COM @ (R0)+ ; LOC 0=-1 R0=404
CLRB @ (R0)+ ; TRY TO CLEAR ODD BYTE
BEQ SOPB3C
```

```
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 771 <====
```

```
MOV #74,-(R2) ; MOVE TO MAILBOX # ***** 74 *****
INC -(R2) ; SET MSGTYP TO FATAL ERROR
HALT ; CLRB DID NOT SET Z-BIT
SOPB3C: DEC R0 ; RESET R0
DEC R0 ; POINT TO EVEN BYTE ADDR.
DEC R0 ; INCREMENT WORD
DEC R0 ; TRY TO NEGATE ODD BYTE
INC @ (R0)+ ; TRY TO INCREMENT ODD BYTE
NEGB @ (R0)+
BPL SOPB3D
INCB @ (R0)+
BEQ TST51
```

```
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 754 <====
```

```
SOPB3D: MOV #75,-(R2) ; MOVE TO MAILBOX # ***** 75 *****
INC -(R2) ; SET MSGTYP TO FATAL ERROR
HALT ; CUMMULATIVE RESULT OF ABOVE INSTS FAILED
; OR SEQUENCE ERROR
```

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1827 003522 005212
1828 003524 022712 000051
1829 003530 001021
1830 003532 005000
1831 003534 105100
1832 003536 005200
1833 003540 005040
1834 003542 001404
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1839 003544 012742 000076
1840 003550 005242
1841 003552 000000
1842 003554 005200
1843 003556 005200
1844 003560 005140
1845 003562 100004
1846 003564 005200
1847 003566 005200
1848 003570 005240
1849 003572 001404
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1854 003574
1855 003574 012742 000077
1856 003600 005242
1857 003602 000000
1858

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```

;*****
;TEST 51 TEST MODE 4 USING SOP INSTS
;*****
↑ST51: INC (R2) ;UPDATE TEST NUMBER
      CMP #51,(R2) ;SEQUENCE ERROR?
      BNE TST52-10 ;BR TO ERROR HALT ON SEQ ERROR
      CLR RO ;SET RO=400
      COMB RO
      INC RO
      CLR -(RO) ;TRY TO CLEAR USING MODE 4
      BEQ SOP4A
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 773 <====
      MOV #76,-(R2) ;MOVE TO MAILBOX # ***** 76 *****
      INC -(R2) ;SET MSGTYP TO FATAL ERROR
      HALT ;CLR DID NOT SET Z-BIT
SOP4A: INC RO ;RESET RO
      INC RO
      COM -(RO) ;TRY TO COMPLEMENT USING MODE 4
      BPL SOP4B
      INC RO ;MOVE POINTER
      INC -(RO)
      BEQ TST52
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 757 <====
SOP4B: MOV #77,-(R2) ;MOVE TO MAILBOX # ***** 77 *****
      INC -(R2) ;SET MSGTYP TO FATAL ERROR
      HALT ;CHECK CUMMULATIVE RESULT OF ABOVE INST.
; OR SEQUENCE ERROR

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003604 005212
003606 022712 000052
003612 001017
003614 005000
003616 005020
003620 105400
003622 005050
003624 001404

003626 012742 000100
003632 005242
003634 000000
003636 005200
003640 005200
003642 005150
003644 100002
003646 005250
003650 001404

003652
003652 012742 000101
003656 005242
003660 000000

```

*****
      THIS TEST VERIFIES MODE 5 SINGLE OPERAND INSTRUCTIONS.  IT
      USES LOCATION 0 AS ITS TARGET DATA.  A TABLE LOCATED AT LOC. 372
      THRU 374 IS USED TO SUPPLY THE ADDRESS OF LOCATION 0 TO THE
      INSTRUCTIONS UNDER TEST.
      RO IS SET TO 376, (THE START OF THE ADDRESS TABLE) +2,
      AND A CLR INSTRUCTION IS EXECUTED WITH MODE 3 TO CLEAR
      LOC. 0.  THEN RO IS INCREMENTED BY TWO AND TWO OTHER MODE 3
      INSTRUCTIONS OPERATE ON LOC. 0 TO VERIFY THE DATA RESULTS OF
      THE TEST.  THE PROPER DECREMENTING OF THE REGISTER IS ALSO
      VERIFIED IN THIS MANNER.
      IF A FAILURE IS DETECTED BE SURE TO VERIFY THAT THE TABLE
      (LOC. 372 THRU 374) HAS THE PROPER VALUES (0).
*****
TEST 52      TEST MODE 5 USING SOP INSTS
*****
TST52:  INC      (R2)          ;UPDATE TEST NUMBER
        CMP      #52,(R2)     ;SEQUENCE ERROR?
        BNE     TST53-10     ;BR TO ERROR HALT ON SEQ ERROR
        CLR     RO           ;SET RO=376
        CLR     (RO)+
        NEGB   RO
        CLR     2-(RO)      ;TRY TO CLEAR LOC 0 W/MODE 5
        BEQ    SOP5A
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
;          CONDITIONAL BRANCH INST. AND <====
;          REPLACE THE MOVE INSTRUCTION <====
;          WHICH FOLLOWS W/ 773 <====
        MOV     #100,-(R2)   ;MOVE TO MAILBOX # ***** 100 *****
        INC     -(R2)
        HALT
SOP5A:  INC     RO
        INC     RO
        COM     2-(RO)      ;TRY TO COMPLEMENT LOC. 0 W/MODE 5
        BPL    SOP5B
        INC     2-(RO)      ;TRY TO INCREMENT LOC. 0 W/MODE 5
        BEQ    TST53
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
;          CONDITIONAL BRANCH INST. AND <====
;          REPLACE THE MOVE INSTRUCTION <====
;          WHICH FOLLOWS W/ 761 <====
SOP5B:  MOV     #101,-(R2)   ;MOVE TO MAILBOX # ***** 101 *****
        INC     -(R2)
        HALT
;TEST CUMMULATIVE RESULT OF ABOVE INSTS
; OR SEQUENCE ERROR

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1908
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1920 003662 005212
1921 003664 022712 000053
1922 003670 001020
1923 003672 005000
1924 003674 105100
1925 003676 005200
1926 003700 005060 177400
1927 003704 001404
1928
1929
1930
1931
1932 003706 012742 000102
1933 003712 005242
1934 003714 000000
1935 003716 005160 177400
1936 003722 100003
1937 003724 005260 177400
1938 003730 001404
1939
1940
1941
1942
1943 003732
1944 003732 012742 000103
1945 003736 005242
1946 003740 000000
1947

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*****
: THIS TEST VERIFIES MODE 6 SINGLE OPERAND INSTRUCTIONS. IT
: USES LOCATION 0 AS ITS TARGET DATA. RO IS SET TO 400 USING
: PREVIOUSLY TESTED INSTRUCTIONS AND A MODE 6 CLR INSTRUCTION IS
: EXECUTED ON LOC. 0 USING RO AND A -400 OFFSET. COM AND INC
: INSTRUCTIONS ARE THEN USED TO VERIFY THE DATA.
*****
: TEST 53 TEST MODE 6 USING SOP INSTS
*****
TST53: INC (R2) ;UPDATE TEST NUMBER
CMP #53,(R2) ;SEQUENCE ERROR?
BNE TST54-10 ;BR TO ERROR HALT ON SEQ ERROR
CLR RO ;SET RO=400
COMB RO
INC RO
CLR -400(RO) ;TRY TO CLEAR LOCATION 0 W/MODE 6
BEQ SOP6A
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 772 <====
MOV #102,-(R2) ;MOVE TO MAILBOX # ***** 102 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;CLR DID NOT SET Z-BIT
SOP6A: COM -400(RO) ;TRY TO COMPLEMENT LOCATION 0 W/MODE 6
BPL SOP6B
INC -400(RO) ;TRY TO INCREMENT LOCATION 0 W/MODE 6
BEQ TST54
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 760 <====
SOP6B: MOV #103,-(R2) ;MOVE TO MAILBOX # ***** 103 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;TEST CUMMULATIVE RESULT OF ABOVE INSTS
; OR SEQUENCE ERROR

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003742 005212
003744 022712 000054
003750 001020
003752 005000
003754 105100
003756 005200
003760 005070 000002
003764 001404

012742 000104
005242
000000
005170 000002
100003
005270 000002
001404

004012
004012 012742 000105
004016 005242
004020 000000

```
*****
THIS TEST VERIFIES MODE 7 SINGLE OPERAND INSTRUCTIONS. IT USES
THE POINTER TO LOC. 0 WHICH IS STORED AT LOC. 402.
RD IS SET TO 400 AND A MODE 7 CLR INSTRUCTION IS
EXECUTED WITH A +2 OFFSET TO CLEAR LOC. 0.
SEVERAL OTHER MODE 7 INSTRUCTIONS ARE THEN USED ON THE COMMON
LOCATION TO VERIFY THE DATA RESULTS.
*****
TEST 54 TEST MODE 7 USING SOP INST.
*****
TST54: INC (R2) ;UPDATE TEST NUMBER
CMP #54,(R2) ;SEQUENCE ERROR?
BNE TST55-10 ;BR TO ERROR HALT ON SEQ ERROR
CLR RO ;SET RO=400
COMB RO
INC RO
CLR @2(RO) ;TRY TO CLEAR LOC. 0 W/MODE 7
BEQ SOP7A
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 772 <====
MOV #104,-(R2) ;MOVE TO MAILBOX # ***** 104 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;CLR DID NOT SET Z-BIT
SOP7A: COM @2(RO) ;TRY TO COMPLEMENT LOC. 0 W/MODE 7
BPL SOP7B
INC @2(RO) ;TRY TO INCREMENT LOC. 0 W/MODE 7
BEQ TST55
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 750 <====
SOP7B: MOV #105,-(R2) ;MOVE TO MAILBOX # ***** 105 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;TEST CUMMULATIVE RESULT OF ABOVE INSTS.
; OR SEQUENCE ERROR
```

1989
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004022 005212
004024 022712 000055
004030 001017
004032 005027
004034 177777
004036 001404

012742 000106
004044 005242
004046 000000
004050 005237 004034
004054 005467 177754
004060 100003
004062 005277 000012
004066 001405

012742 000107
004074 000000
004076 000000
004100 004034

```

*****
THIS TEST VERIFIES PROGRAM COUNTER ADDRESSING WITH SOP
INSTRUCTIONS. CLR MODE 77 IS USED TO CLEAR THE LOCATION FOLLOWING THE
INSTRUCTION (SOPX). THEN SINGLE OPERAND INSTRUCTIONS WITH MODES 37, 67, AND
77, USING INDIRECT POINTER SOPXAD ARE USED TO VERIFY THE DATA RESULTS
OF THESE INSTRUCTIONS.
*****
TEST 55 TEST SOP INSTRUCTIONS MODES 2,3,6,7 WITH REGISTER 7
*****
TST55: INC (R2) ; UPDATE TEST NUMBER
        CMP #55, (R2) ; SEQUENCE ERROR?
        BNE SOPB ; BR TO ERROR HALT ON SEQ ERROR
        CLR (R7)+ ; CLEAR NEXT LOCATION: (SOPX)
SOPX: -1 ; USE MODE 27
        BEQ SOPA
        ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
        ; CONDITIONAL BRANCH INST. AND <====
        ; REPLACE THE MOVE INSTRUCTION <====
        ; WHICH FOLLOWS W/ 775 <====
        MOV #106, -(R2) ; MOVE TO MAILBOX # ***** 106 *****
        INC -(R2) ; SET MSGTYP TO FATAL ERROR
        HALT ; CLR DID NOT SET Z-BIT
SOPA: INC #SOPX ; INC SOPX W/MODE 37
        NEG SOPX ; NEGATE SOPX W/MODE 67
        BPL SOPB
        INC #SOPXAD ; INC SOPX W/MODE 77
        BEQ TST56
        ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
        ; CONDITIONAL BRANCH INST. AND <====
        ; REPLACE THE MOVE INSTRUCTION <====
        ; WHICH FOLLOWS W/ 761 <====
SOPB: MOV #107, -(R2) ; MOVE TO MAILBOX # ***** 107 *****
        INC -(R2) ; SET MSGTYP TO FATAL ERROR
        HALT ; INC DID NOT SET Z-BIT
        ; OR SEQUENCE ERROR
SOPXAD: SOPX ; INDIRECT ADDRESS OF SOPX
    
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004102 005212
004104 022712 000056
004110 001010
004112 005000
004114 000277
004116 000244
004120 005700
004122 102403
004124 100402
004126 103401
004130 001404

004132 012742 000110
004132 005242
004136 000000

```
*****
THIS TEST VERIFIES SINGLE OPERAND NON-MODIFYING INSTRUCTIONS
USING MODE 0.  R0 IS SET TO ZERO AND THE CONDITION CODES ARE SET
TO THE COMPLEMENT OF THAT EXPECTED BY THE INSTRUCTION.  A TST INSTRUCTION
IS EXECUTED AND CONDITIONAL BRANCHES ARE USED TO TEST THE CONDITION
CODES.
*****
TEST 56      TEST MODE 0 SOP NON-MODIFYING
*****
TST56:  INC      (R2)          ;UPDATE TEST NUMBER
        CMP      #56,(R2)     ;SEQUENCE ERROR?
        BNE     TST57-10      ;BR TO ERROR HALT ON SEQ ERROR
        CLR     R0            ;INITIALIZE R0=0
        SCC     ;SET CC=1011
        CLZ
        TST     R0            ;TRY TST W/ MODE 0
        BVS     SNMOA         ;CHECK THAT CC=0100
        BMI     SNMOA
        BCS     SNMOA
        BEQ     TST57
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 770 <====
SNMOA:  MOV     #110,-(R2)    ;MOVE TO MAILBOX # ***** 110 *****
        INC     -(R2)        ;SET MSGTYP TO FATAL ERROR
        HALT                ;CONDITION CODES NOT SET PROPERLY
; OR SEQUENCE ERROR
*****
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2092

004142 005212
004144 022712 000057
004150 001010
004152 005000
004154 105100
004156 000277
004160 000250
004152 105700
004164 102402
004166 101401
004170 100404

004172
004172 012742 000111
004176 005242
004200 000000

```
*****
: THIS TEST VERIFIES SINGLE OPERAND NON-MODIFYING BYTE INSTRUCTIONS WITH MODE 0.
: RO IS SET TO 377 AND COMPLEMENT OF THE EXPECTED CONDITION CODES
: IS LOADED IN PSW. A TSTB INSTRUCTION IS EXECUTED AND THE RESULTS
: ARE CHECKED WITH SEVERAL CONDITIONAL BRANCH INSTRUCTIONS.
: THIS VERIFIES THAT THE PROPER BYTE WAS TESTED.
*****
: TEST 57 TEST MODE 0 EVEN BYTE W/ SOP NON-MODIFYING
*****
TST57: INC (R2) ;UPDATE TEST NUMBER
CMP #57,(R2) ;SEQUENCE ERROR?
BNE TST60-10 ;BR TO ERROR HALT ON SEQ ERROR
CLR RO ;INITIALIZE
COMB RO ;RO=377
SCC ;SET CC=0111
CLN
TSTB RO ;TRY TST EVEN BYTE
BVS SNMBOA ;CHECK CC=1000
BLOS SNMBOA
BMI TST60

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 770 <====

SNMBOA: MOV #111,-(R2) ;MOVE TO MAILBOX # ***** 111 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;CONDITION CODES NOT SET PROPERLY
; OR SEQUENCE ERROR
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2110
2111
2112
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2114
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2116
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2118
2119
2120
2121
2122
2123
2124
2125

004202 005212
004204 022712 000060
004210 001011
004212 005000
004214 005010
004216 000277
004220 000244
004222 005710
004224 102403
004226 103402
004230 100401
004232 001404

004234 012742 000112
004234 005242
004242 000000

THIS TEST VERIFIES SINGLE OPERAND INSTRUCTIONS WITH MODE 1.
RO IS USED TO POINT TO AND CLEAR LOC. 0. THE COMPLEMENT OF THE
EXPECTED CONDITION CODES ARE LOADED IN THE PSW. A TST INSTRUCTION
IS THEN EXECUTED ON LOC. 0 USING RO AND CONDITIONAL BRANCHES TEST
THE RESULTS.

TEST 60 TEST MODE 1 SOP NON-MODIFYING

TST60: INC (R2) ;UPDATE TEST NUMBER
CMP #60,(R2) ;SEQUENCE ERROR?
BNE TST61-10 ;BR TO ERROR HALT ON SEQ ERROR
CLR RO ;POINT TO LOC 0
CLR (RO) ;CLEAR LOC 0
SCC ;INITIALIZE
CLZ ;CC=1011
TST (RO) ;TRY TST W/ MODE 1
BVS SNM1A ;CHECK CC=0100
BCS SNM1A
BMI SNM1A
BEQ TST61

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 767 <====

SNM1A: MOV #112,-(R2) ;MOVE TO MAILBOX # ***** 112 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;CC'S NOT SET PROPERLY
; OR SEQUENCE ERROR

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2161
2162
2163
2164
2165
2166
2167
2168
2169
2170
2171
2172
2173
2174

004244 005212
004246 022712 000061
004252 001026
004254 005000
004256 005010
004260 105110
004262 000277
004264 000250
004266 105710
004270 102402
004272 101401
004274 100404

004276 012742 000113
004276 005242
004302 000000
004306 005000
004310 005200
004312 000277
004314 000244
004316 105710
004320 102403
004322 103402
004324 100401
004326 001404

004330 012742 000114
004330 005242
004334 000000
004336 000000

```
*****
: THIS TEST SETS LOCATION 0 TO 377 AND THEN USES R0 TO TEST
: THE EVEN BYTE AND THE ODD BYTE USING SOP BYTE INSTRUCTIONS WITH MODE 1.
: AGAIN, CONDITIONAL BRANCHES ARE USED TO VERIFY THE SETTING OF THE
: PROPER CONDITION CODE BITS.
*****
: TEST 61 TEST MODE 1 BYTE INST. NON-MODIFYING
*****
TST61: INC (R2) ; UPDATE TEST NUMBER
      CMP #61,(R2) ; SEQUENCE ERROR?
      BNE TST62-10 ; BR TO ERROR HALT ON SEQ ERROR
      CLR R0 ; POINT TO LOC 0
      CLR (R0) ; CLEAR LOC 0
      COMB (R0) ; COMPLEMENT BYTE 0
      SCC ; SET CC=0111
      CLN
      TSTB (R0) ; TRY TST ON EVEN BYTE
      BVS SNMB1A
      BLOS SNMB1A
      BMI SNMB1B

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 767 <====

SNMB1A: MOV #113,-(R2) ; MOVE TO MAILBOX # ***** 113 *****
        INC -(R2) ; SET MSGTYP TO FATAL ERROR
        HALT ; CC'S NOT CORRECT

SNMB1B: CLR R0
        INC R0
        SCC ; SET CC=1011
        CLZ
        TSTB (R0) ; TRY TO TST AN ODD BYTE
        BVS SNMB1C ; CHECK CC=0100
        BCS SNMB1C
        BMI SNMB1C
        BEQ TST62

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 752 <====

SNMB1C: MOV #114,-(R2) ; MOVE TO MAILBOX # ***** 114 *****
        INC -(R2) ; SET MSGTYP TO FATAL ERROR
        HALT ; CC'S NOT CORRECT
        OR SEQUENCE ERROR
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2200
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2203
2204
2205
2206
2207
2208
2209
2210
2211
2212
2213
2214
2215
2216

004340 005212
004342 022712 000062
004346 001020
004350 005000
004352 005010
004354 000277
004356 000244
004360 005720
004362 102403
004364 103402
004366 100401
004370 001404

004372
004372 012742 000115
004376 005242
004400 000000
004402 005300
004404 005300
004406 001404

004410 012742 000116
004414 005242
004416 000000

```
*****
: THIS TEST VERIFIES THE SINGLE-OPERAND NON-MODIFYING INSTRUCTIONS
: USING MODE 2. IT USES THE IDENTICAL PROCEDURE EMPLOYED IN THE
: MODE 1 TESTS. ADDITIONALLY, THE REGISTER IS CHECKED TO ASSURE THAT
: IT IS INCREMENTED PROPERLY.
*****
: TEST 62 TEST MODE 2 WITH SOP NON-MODIFYING
*****
TST62: INC (R2) ;UPDATE TEST NUMBER
CMP #62,(R2) ;SEQUENCE ERROR?
BNE TST63-10 ;BR TO ERROR HALT ON SEQ ERROR
CLR RO ;INITIALIZE RO=0
CLR (RO) ;CLEAR LOC 0
SCC ;SET CC=1011
CLZ
TST (RO)+ ;TRY TST W/ MODE 2
BVS SNM2A ;CHECK CC=0100
BCS SNM2A
BMI SNM2A
BEQ SNM2B

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 767 <====

SNM2A: MOV #115,-(R2) ;MOVE TO MAILBOX # ***** 115 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;CC'S NOT CORRECT
SNM2B: DEC RO ;RESET RO
DEC RO
BEQ TST63

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 760 <====

MOV #116,-(R2) ;MOVE TO MAILBOX # ***** 116 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;MODE 2 DID NOT INC REG CORRECTLY
; OR SEQUENCE ERROR
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2217
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2222
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004420 005212
004422 022712 000063
004426 001042
004430 005000
004432 005010
004434 105110
004436 000277
004440 000250
004442 105720
004444 102402
004446 101401
004450 100404

004452 012742 000117
004456 005242
004460 000000
004462 005300
004464 001404

004466 012742 000120
004472 005242
004474 000000
004476 005200
004500 000277
004502 000244
004504 105720
004506 102403
004510 103402
004512 100401
004514 001404

004516 012742 000121
004522 005242

```
*****  
: THIS TEST VERIFIES MODE 2 SINGLE OPERAND NON-MODIFYING BYTE  
: INSTRUCTIONS IT USES R0 TO POINT TO LOC. 0. WITH LOCATION 0  
: SET TO 377, THE EVEN AND ODD BYTE IS TESTED WITH TSTB INSTRUCTIONS  
: TO VERIFY THE CORRECT CC ARE SET. THE REGISTER IS CHECKED FOR  
: PROPER INCREMENTING.  
*****  
: TEST 63 TEST MODE 2 - BYTE W/ SOP NON-MODIFYING  
*****  
TST63: INC (R2) ; UPDATE TEST NUMBER  
CMP #63,(R2) ; SEQUENCE ERROR?  
BNE TST64-10 ; BR TO ERROR HALT ON SEQ ERROR  
CLR R0 ; CLEAR R0  
CLR (R0) ; CLEAR LOC 0  
COMB (R0) ; SET LOC 0=377  
SCC ; SET CC=0111  
CLN ;  
TSTB (R0)+ ; TRY TST OF EVEN BYTE  
BVS SNMB2A  
BLOS SNMB2A  
BMI SNMB2B  
  
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====  
; CONDITIONAL BRANCH INST. AND <====  
; REPLACE THE MOVE INSTRUCTION <====  
; WHICH FOLLOWS W/ 767 <====  
  
SNMB2A: MOV #117, -(R2) ; MOVE TO MAILBOX # ***** 117 *****  
INC -(R2) ; SET MSGTYP TO FATAL ERROR  
HALT ; CC'S NOT SET CORRECTLY  
SNMB2B: DEC R0 ; DECREMENT R0  
BEQ SNMB2C  
  
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====  
; CONDITIONAL BRANCH INST. AND <====  
; REPLACE THE MOVE INSTRUCTION <====  
; WHICH FOLLOWS W/ 761 <====  
  
SNMB2C: MOV #120, -(R2) ; MOVE TO MAILBOX # ***** 120 *****  
INC -(R2) ; SET MSGTYP TO FATAL ERROR  
HALT ; MODE 2 DID NOT INC REG CORRECTLY  
SNMB2C: INC R0 ; POINT TO ODD BYTE  
SCC ; SET CC=1011  
CLZ  
TSTB (R0)+ ; TRY TST OF ODD BYTE  
BVS SNMB2D  
BCS SNMB2D  
BMI SNMB2D  
BEQ SNMB2E  
  
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====  
; CONDITIONAL BRANCH INST. AND <====  
; REPLACE THE MOVE INSTRUCTION <====  
; WHICH FOLLOWS W/ 745 <====  
  
SNMB2D: MOV #121, -(R2) ; MOVE TO MAILBOX # ***** 121 *****  
INC -(R2) ; SET MSGTYP TO FATAL ERROR
```

J04

2273	004524	000000		HALT					
2274	004526	005300		DEC	RO				
2275	004530	005300		DEC	RO				
2276	004532	001404		BEG	TST64				
2277									
2278									
2279									
2280									
2281	004534	012742	000122	MOV	#122, -(R2)				
2282	004540	005242		INC	-(R2)				
2283	004542	000000		HALT					
2284									

;CC'S NOT CORRECT

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 736 <====
; MOVE TO MAILBOX # ***** 122 *****
; SET MSGTYP TO FATAL ERROR
; RO DID NOT INCREMENT PROPERLY
; OR SEQUENCE ERROR

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004544 005212
004546 022712 000064
004552 001022
004554 005000
004556 005010
004560 105100
004562 005300
004564 000277
004566 000244
004570 005730
004572 102403
004574 103402
004576 100401
004600 001404

004602 012742 000123
004606 005242
004610 000000
004612 005300
004614 105100
004616 001404

004620 012742 000124
004624 005242
004626 000000

```
*****
: THIS TEST VERIFIES MODE 3 SINGLE OPERAND NON-MODIFYING INSTRUCTIONS.
: A POINTER IN A TABLE AT LOC. 376 IS USED TO TEST LOCATION 0.
: THE CC'S AND THE REGISTER ARE CHECKED FOLLOWING THE
: TST MODE 3 INSTRUCTION.
*****
: TEST 64 TEST MODE 3 W/ SOP NON-MODIFYING INSTS
*****
TST64: INC (R2) ; UPDATE TEST NUMBER
      CMP #64,(R2) ; SEQUENCE ERROR?
      BNE TST65-10 ; BR TO ERROR HALT ON SEQ ERROR
      CLR RO ; RO=0
      CLR (RO) ; CLEAR LOC 0
      COMB RO ; RO=376
      DEC RO
      SCC ; SET CC=1011
      CLZ
      TST 2(RO)+ ; TRY TST W/ MODE 3
      BVS SNM3A ; CHECK CC=0100
      BCS SNM3A
      BMI SNM3A
      BEQ SNM3B
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 765 <====
SNM3A: MOV #123,-(R2) ; MOVE TO MAILBOX # ***** 123 *****
      INC -(R2) ; SET MSGTYP TO FATAL ERROR
      HALT ; CC'S NOT CORRECT
SNM3B: DEC RO ; RO=377
      COMB RO ; RO=0
      BEQ TST65
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 756 <====
      MOV #124,-(R2) ; MOVE TO MAILBOX # ***** 124 *****
      INC -(R2) ; SET MSGTYP TO FATAL ERROR
      HALT ; MODE 3 DID NOT INC REG CORRECTLY
; OR SEQUENCE ERROR
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004630 005212
004632 022712 000065
004636 001036
004640 005000
004642 005010
004644 105110
004646 105100
004650 005200
004652 005720
004654 000277
004656 000250
004660 105730
004662 102402
004664 101401
004666 100404

004670
004670 012742 000125
004674 005242
004676 000000
004700 000277
004702 000244
004704 105730
004706 102403
004710 103402
004712 100401
004714 001404

004716
004716 012742 000126
004722 005242
004724 000000
004726 005720
004730 005710
004732 100404

```
*****
;
; THIS TEST VERIFIES SOP NON-MODIFYING BYTE INSTRUCTIONS MODE 3
; LOC. 0 IS SET TO 377. TABLE AT LOC. 402-404 IS USED TO TEST
; BYTE 0 AND BYTE 1. THE REGISTER IS CHECKED FOR PROPER INCREMENTING AND
; THE CC'S ARE VERIFIED.
; THE TABLE AT LOC. 402-404 SHOULD CONTAIN 0 AND 1 BEFORE AND
; AFTER THE TEST IS RUN.
;
*****
; TEST 65 TEST MODE 3 - BYTES W/ SOP NON-MODIFYING INSTS.
*****
TST65: INC (R2) ; UPDATE TEST NUMBER
; CMP #65, (R2) ; SEQUENCE ERROR?
; BNE TST66-10 ; BR TO ERROR HALT ON SEQ ERROR
; CLR RO ; RO=0
; CLR (RO) ; CLEAR LOC 0
; COMB (RO) ; LOC. 0 =377
; COMB RO
; INC RO
; TST (RO)+ ; RO=402
; SCC ; CC=0111
; CLN
; TSTB @ (RO)+ ; TRY TST OF EVEN BYTE
; BVS SNMB3A ; CHECK CC=1000
; BLOS SNMB3A
; BMI SNMB3B
;
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 764 <====
;
SNMB3A: MOV #125, -(R2) ; MOVE TO MAILBOX # ***** 125 *****
; INC -(R2) ; SET MSGTYP TO FATAL ERROR
; HALT ; CC'S NOT CORRECT
SNMB3B: SCC ; SET CC=1011
; CLZ
; TSTB @ (RO)+ ; TRY TST OF ODD BYTE
; BVS SNMB3C ; CHECK CC=0100
; BCS SNMB3C
; BMI SNMB3C
; BEQ SNMB3D
;
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 751 <====
;
SNMB3C: MOV #126, -(R2) ; MOVE TO MAILBOX # ***** 126 *****
; INC -(R2) ; SET MSGTYP TO FATAL ERROR
; HALT ; CC'S NOT CORRECT
SNMB3D: TST (RO)+ ; RO=410
; TST (RO)
; BMI TST66
;
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
```

2385										REPLACE THE MOVE INSTRUCTION	<====
2386										WHICH FOLLOWS W/ 742	<====
2387	004734	012742	000127	MOV	#127, -(R2)					MOVE TO MAILBOX # ***** 127 *****	
2388	004740	005242		INC	-(R2)					SET MSGTYP TO FATAL ERROR	
2389	004742	000000		HALT						TSTB DID NOT INCREMENT RO CORRECTLY	
2390										OR SEQUENCE ERROR	
2391										*****	
2392										THIS TEST VERIFIES MODE 4 SOP NON-MODIFYING INSTRUCTIONS.	
2393										LOC. 0 IS SET TO -1 AND THE CC'S ARE SET TO THE COMPLEMENT OF THE	
2394										EXPECTED RESULTS. RO AND SET TO 2 AND A TST MODE 4 IS EXECUTED.	
2395										THE CC'S ARE CHECKED WITH CONDITIONAL BRANCH INSTRUCTIONS AND THE REGISTER	
2396										IS CHECKED FOR PROPER DECREMENTING.	
2397										*****	
2398										TEST 66 TEST MODE 4 W/ SOP NON-MODIFYING INSTS	
2399										*****	
2400										TST66: INC (R2)	UPDATE TEST NUMBER
2401										CMP #66, (R2)	SEQUENCE ERROR?
2402	004744	005212	000066							BNE TST67-10	BR TO ERROR HALT ON SEQ ERROR
2403	004746	022712								CLR RO	RO=0
2404	004752	001017								CLR (R0)	LOC 0=0
2405	004754	005000								COM (R0)+	LOC 0=-1
2406	004756	005010								SCC	SET CC=1011
2407	004760	005120								CLZ	
2408	004762	000277								TST -(R0)	TRY TST W/ MODE 4
2409	004764	000244								BVS SNM4A	CHECK CC=0100
2410	004766	005740								BLOS SNM4A	
2411	004770	102402								BMI SNM4B	
2412	004772	101401									
2413	004774	100404									
2414										TO SCOPE: CLEAR THE RIGHT BYTE OF THIS	<====
2415										CONDITIONAL BRANCH INST. AND	<====
2416										REPLACE THE MOVE INSTRUCTION	<====
2417										WHICH FOLLOWS W/ 767	<====
2418	004776			SNM4A:							
2419	004776	012742	000130		MOV #130, -(R2)					MOVE TO MAILBOX # ***** 130 *****	
2420	005002	005242			INC -(R2)					SET MSGTYP TO FATAL ERROR	
2421	005004	000000			HALT					CC'S NOT CORRECT	
2422	005006	005700		SNM4B:							
2423	005010	001404			TST RO						
2424					BEQ TST67						
2425										TO SCOPE: CLEAR THE RIGHT BYTE OF THIS	<====
2426										CONDITIONAL BRANCH INST. AND	<====
2427										REPLACE THE MOVE INSTRUCTION	<====
2428	005012	012742	000131							WHICH FOLLOWS W/ 761	<====
2429	005016	005242			MOV #131, -(R2)					MOVE TO MAILBOX # ***** 131 *****	
2430	005020	000000			INC -(R2)					SET MSGTYP TO FATAL ERROR	
2431					HALT					TST MODE 4 DID NOT DEC RO CORRECTLY	
										OR SEQUENCE ERROR	

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005022 005212
005024 022712 000067
005030 001022
005032 005000
005034 005010
005036 005110
005040 105100
005042 005200
005044 000277
005046 000250
005050 005750
005052 102402
005054 101401
005056 100404

005060
005060 012742 000132
005064 005242
005066 000000
005070 005200
005072 105100
005074 001404

005076 012742 000133
005102 005242
005104 000000

```
*****
;
; THIS TEST VERIFIES MODE 5 SOP NON-MODIFYING INSTRUCTIONS.
; IT USES A POINTER AT LOC. 376 TO TEST LOC. 0. RO IS SET
; TO 400, A TST MODE 5 INSTRUCTION IS EXECUTED AND THE CC'S CHECKED.
; RO IS CHECKED TO INSURE PROPER DECREMENTING.
;
*****
; TEST 67 TEST MODE 5 W/ SOP NON-MODIFYING INSTS
*****
TST67: INC (R2) ; UPDATE TEST NUMBER
; CMP #67,(R2) ; SEQUENCE ERROR?
; BNE TST70-10 ; BR TO ERROR HALT ON SEQ ERROR
; CLR RO ; RO=0
; CLR (RO) ; LOC 0=0
; COM (RO) ; LOC 0=-1
; COMB RO ; RO=377
; INC RO ; RO=400
; SCC ; SET CC=0111
; CLN
; TST 2-(RO) ; TRY TST W/ MODE 5
; BVS SNM5A ; CHECK CC=1000
; BLOS SNM5A
; BMI SNM5B
;
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 765 <====
;
SNM5A: MOV #132,-(R2) ; MOVE TO MAILBOX # ***** 132 *****
; INC -(R2) ; SET MSGTYP TO FATAL ERROR
; HALT ; CC'S NOT SET PROPERLY
SNM5B: INC RO ; RO=377
; COMB RO ; RO=0
; BEQ TST70
;
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 756 <====
;
; MOVE TO MAILBOX # ***** 133 *****
; INC -(R2) ; SET MSGTYP TO FATAL ERROR
; HALT ; MODE 5 DID NOT DEC RO CORRECTLY
; OR SEQUENCE ERROR
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005198
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005170 005212
005172 022712 000071
005176 001021
005200 005000
005202 005010
005204 005110
005206 105100
005210 000277
005212 000250
005214 005770 000001
005220 102402
005222 101401
005224 100404

005226 012742 000136
005226 005242
005232 000000
005234 105100
005236 001404

005242 012742 000137
005246 005242
005250 000000

```
*****
: THIS TEST VERIFIES MODE 7 SOP NON-MODIFYING INSTRUCTIONS.
: IT USES A POINTER TO LOC. 0 STORED AT LOC. 400 TO TST LOC. 0.
: RO IS SET TO 377 AND LOC. 0 IS TESTED THRU THE POINTER AT 400 USING
: RO AND AN OFFSET OF 1.
*****
: TEST 71 TEST MODE 7 W/ SOP NON-MODIFYING INSTS.
*****
TST71: INC (R2) ;UPDATE TEST NUMBER
CMP #71,(R2) ;SEQUENCE ERROR?
BNE TST72-10 ;BR TO ERROR HALT ON SEQ ERROR
CLR RO ;RO=0
CLR (RO) ;LOC 0=0
COM (RO) ;LOC 0=-1
COMB RO ;RO=377
SCC ;CC=0111
CLN
TST #1(RO) ;TRY TST W/ MODE 7
BVS SNM7A ;CHECK CC=1000
BLOS SNM7A
BMI SNM7B

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 765 <====

SNM7A: MOV #136,-(R2) ;MOVE TO MAILBOX # ***** 136 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;CC'S NOT CORRECT
BEG RO ;RO=0
TST72

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 757 <====

SNM7B: MOV #137,-(R2) ;MOVE TO MAILBOX # ***** 137 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;TST MODE 7 INCORRECTLY CHANGED RC
; OR SEQUENCE ERROR
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005252 005212
005254 022712 000072
005260 001006
005262 005000
005264 005100
005266 005004
005270 060004
005272 005204
005274 001404

005276 012742 000140
005302 005242
005304 000000

 : THIS TEST VERIFIES MODE 0 DOUBLE OPERAND INSTRUCTIONS. IT SETS
 : DATA IN R0 AND R4 AND USES THE ADD INSTRUCTION TO TEST THE DOP
 : MICROCODE.

TEST 72 TEST MODE 0 DOUBLE-OPERAND (DOP) INSTS.

```
TST72: INC (R2) ; UPDATE TEST NUMBER
        CMP #72,(R2) ; SEQUENCE ERROR?
        BNE TST73-10 ; BR TO ERROR HALT ON SEQ ERROR
        CLR R0 ; R0=0
        COM R0 ; R0=-1
        CLR R4 ; R4=0
        ADD R0,R4 ; TRY ADD: R4=-1
        INC R4 ; R4=0
        BEQ TST73

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 772 <====
        MOV #140,-(R2) ; MOVE TO MAILBOX # ***** 140 *****
        INC -(R2) ; SET MSGTYP TO FATAL ERROR
        HALT ; ADD INST. FAILED W/ MODE 0
; OR SEQUENCE ERROR
```

 : THIS TEST VERIFIES THE MOVE INSTRUCTION WITH MODE 0 TO MODE 0.
 : THIS TEST IS NECESSARY BECAUSE THIS PARTICULAR INSTRUCTION UTILIZES UNIQUE
 : MICROCODE.

TEST 73 MOV MODE 0 TO MODE 0

```
TST73: INC (R2) ; UPDATE TEST NUMBER
        CMP #73,(R2) ; SEQUENCE ERROR?
        BNE TST74-10 ; BR TO ERROR HALT ON SEQ ERROR
        CLR R0 ; R0=0
        CLR R4 ; R4=0
        COM R0 ; R0=-1
        MOV R0,R4 ; TRY MOVE -1 TO R4
        INC R4 ; INC R4
        BEQ TST74

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 772 <====
        MOV #141,-(R2) ; MOVE TO MAILBOX # ***** 141 *****
        INC -(R2) ; SET MSGTYP TO FATAL ERROR
        HALT ; MOVE FAILED MODE 0 TO MODE 0
; OR SEQUENCE ERROR
```

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2626 005342 005212
2627 005344 022712 000074
2628 005350 001051
2629 005352 005000
2630 005354 010004
2631 005356 001404
2632
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2636 005360 012742 000142
2637 005364 005242
2638 005366 000000
2639 005370 005200
2640 005372 005100
2641 005374 005104
2642 005376 040004
2643 005400 005304
2644 005402 001404
2645
2646
2647
2648
2649 005404 012742 000143
2650 005410 005242
2651 005412 000000
2652 005414 050004
2653 005416 005204
2654 005420 005204
2655 005422 001404
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2660 005424 012742 000144
2661 005430 005242
2662 005432 000000
2663 005434 005000
2664 005436 105100
2665 005440 005004
2666 005442 005104
2667 005444 040004
2668 005446 060004
2669 005450 005204

```

```

*****
THIS TEST QUICKLY VERIFIES THE REMAINING DOP MODIFYING INSTRUCTIONS
WITH MODE 0 TO PROVIDE A BASELINE FOR SUBSEQUENT TESTS.
SINGLE OPERAND INSTRUCTIONS ARE USED TO SET UP DATA IN R0 AND R4
BEFORE EACH OF THE SEVERAL DOP MODIFYING INSTRUCTIONS ARE USED AND
VERIFIED.
*****
TEST 74 TEST ALL THE DOP INSTRUCTIONS W/ SOURCE MODE 0
*****
TST74: INC (R2) ;UPDATE TEST NUMBER
CMP #74,(R2) ;SEQUENCE ERROR?
BNE TST75-10 ;BR TO ERROR HALT ON SEQ ERROR
CLR R0 ;R0=0
MOV R0,R4 ;TRY MOVE MODE 0,0
BEQ DOP0A

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 775 <====

MOV #142,-(R2) ;MOVE TO MAILBOX # ***** 142 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;Z-BIT NOT SET
DOP0A: INC R0 ;R0=1
COM R0 ;R0=177776
COM R4 ;R4=177777
BIC R0,R4 ;TRY BIC: R4=1
DEC R4 ;R4=0
BEQ DOP0B

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 763 <====

MOV #143,-(R2) ;MOVE TO MAILBOX # ***** 143 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;BIC CLEAR RESULT INCORRECT
DOP0B: BIS R0,R4 ;TRY BIS: R4=177777
INC R4 ;R4=0
INC R4
BEQ DOP0C

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 753 <====

MOV #144,-(R2) ;MOVE TO MAILBOX # ***** 144 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;RESULT OF BIS INCORRECT
DOP0C: CLR R0 ;R0=0
COMB R0 ;R0=377
CLR R4 ;R4=0
COM R4 ;R4=177777
BIC R0,R4 ;R4=177400
ADD R0,R4 ;TRY ADD: R4=177777
INC R4 ;R4=0

```

2670	005452	001404		BEQ	DOP0D		
2671							
2672							
2673							
2674							
2675	005454	012742	000145	MOV	#145, -(R2)		
2676	005460	005242		INC	-(R2)		
2677	005462	000000		HALT			
2678	005464	160004					
2679	005466	105404					
2680	005470	005204					
2681	005472	001404		BEQ	TST75		
2682							
2683							
2684							
2685							
2686	005474	012742	000146	MOV	#146, -(R2)		
2687	005500	005242		INC	-(R2)		
2688	005502	000000		HALT			
2689							

			DOP0D:	SUB	R0, R4		
				NEGB	R4		
				INC	R4		
				BEQ	TST75		

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
 ; CONDITIONAL BRANCH INST. AND <====
 ; REPLACE THE MOVE INSTRUCTION <====
 ; WHICH FOLLOWS W/ 737 <====
 ; MOVE TO MAILBOX # ***** 145 *****
 ; SET MSGTYP TO FATAL ERROR
 ; RESULT OF ADD INCORRECT
 ; 177401=R4
 ; R4=177777
 ; RD=0

 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
 ; CONDITIONAL BRANCH INST. AND <====
 ; REPLACE THE MOVE INSTRUCTION <====
 ; WHICH FOLLOWS W/ 727 <====
 ; MOVE TO MAILBOX # ***** 146 *****
 ; SET MSGTYP TO FATAL ERROR
 ; RESULT OF SUB INCORRECT
 ; OR SEQUENCE ERROR

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2700 005504 005212
2701 005506 022712 000075
2702 005512 001042
2703 005514 005000
2704 005516 005004
2705 005520 005204
2706 005522 020400
2707 005524 003004
2708
2709
2710
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2712 005526 012742 000147
2713 005532 005242
2714 005534 000000
2715 005536 020004
2716 005540 002404
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2721 005542 012742 000150
2722 005546 005242
2723 005550 000000
2724 005552 005200
2725 005554 020400
2726 005556 001404
2727
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2729
2730
2731 005560 012742 000151
2732 005564 005242
2733 005566 000000
2734 005570 005000
2735 005572 005100
2736 005574 005004
2737 005576 030004
2738 005600 001404
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2743 005602 012742 000152
2744 005606 005242
2745 005610 000000

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*****
THIS TEST VERIFIES MODE 0 DOP NON-MODIFYING INSTRUCTIONS.
RO AND R4 ARE PRESET TO 0 AND 1 RESPECTIVELY. COMPARE INSTRUCTIONS ARE
THEN EXECUTED AND CHECKED. FIRST R4 IS COMPARED TO RO THEN RO TO R4.
*****
TEST 75 TEST DOP NON-MODIFYING INST. W/ SOURCE MODE 0
*****
TST75: INC (R2) ;UPDATE TEST NUMBER
CMP #75,(R2) ;SEQUENCE ERROR?
BNE TST76-10 ;BR TO ERROR HALT ON SEQ ERROR
CLR RO ;RO=0
CLR R4 ;R4=0
INC R4 ;R4=1
CMP R4,RO ;TRY COMPARE R4 TO RO
BGT DNM1
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 773 <====
; MOVE TO MAILBOX # ***** 147 *****
; SET MSGTYP TO FATAL ERROR
; CC'S NOT CORRECT FOR CMP
; TRY COMPARE RO TO R4
DNM1: CMP RO,R4
BLT DNM2
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 765 <====
; MOVE TO MAILBOX # ***** 150 *****
; SET MSGTYP TO FATAL ERROR
; CC'S NOT CORRECT FOR CMP
; R4=0
; TRY COMPARE R4=1 TO RO=1
DNM2: INC RO
CMP R4,RO
BEQ DNM3
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 756 <====
; MOVE TO MAILBOX # ***** 151 *****
; SET MSGTYP TO FATAL ERROR
; CC'S NOT CORRECT (Z=1) FOR CMP
; RO=0
; RO=177777
; R4=0
; TRY BIT RO TO R4
DNM3: MOV #151,-(R2)
INC -(R2)
HALT
CLR RO
COM RO
CLR R4
BIT RO,R4
BEQ DNM4
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 745 <====
; MOVE TO MAILBOX # ***** 152 *****
; SET MSGTYP TO FATAL ERROR
; CC'S NOT CORRECT FOR BIT

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2796 005666 005212
2797 005670 022712 000077
2798 005674 001007
2799 005676 005000
2800 005700 005010
2801 005702 005110
2802 005704 005004
2803 005706 151004
2804 005710 105104
2805 005712 001404
2806
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2810 005714 012742 000155
2811 005720 005242
2812 005722 000000
2813

```

```

:*****
:
:      THIS TEST VERIFIES MODE 1 DOP BYTE INSTRUCTIONS WHICH ADDRESS
:      EVEN BYTES.  LOC. 0 IS SET TO -1 AND R4 IS CLEARED.  THEN R4 IS
:      SET TO -1 USING A BISB THRU R0 WITH MODE 1.
:*****
:TEST 77      TEST MODE 1 - EVEN BYTE W/ DOP INSTS.
:*****
TST77:  INC      (R2)          ;UPDATE TEST NUMBER
        CMP      #77,(R2)    ;SEQUENCE ERROR?
        BNE     TST100-10   ;BR TO ERROR HALT ON SEQ ERROR
        CLR     R0          ;R0=0
        CLR     (R0)        ;LOC. 0=0
        COM     (R0)        ;LOC. 0=177777
        CLR     R4          ;R4=0
        BISB   (R0),R4     ;TRY MODE 1- EVEN BYTE W/ DOP
        COMB   R4          ;R4=0
        BEQ    TST100
:
:      TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
:      CONDITIONAL BRANCH INST. AND <====
:      REPLACE THE MOVE INSTRUCTION <====
:      WHICH FOLLOWS W/ 771 <====
:      MOVE TO MAILBOX # ***** 155 *****
:      SET MSGTYP TO FATAL ERROR
:      RESULT OF BISB IS INCORRECT
:      OR SEQUENCE ERROR

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2825 005724 005212
2826 005726 022712 000100
2827 005732 001007
2828 005734 005000
2829 005736 005010
2830 005740 005110
2831 005742 005004
2832 005744 105104
2833 005746 121004
2834 005750 001404
2835
2836
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2838
2839 005752 012742 000156
2840 005756 005242
2841 005760 000000
2842

```

```

;*****
; THIS TEST VERIFIES MODE 1 DOP NON-MODIFYING INSTRUCTIONS
; WHICH ADDRESS EVEN BYTES. LOC 0 IS SET TO -1 AND R0 IS CLEARED
; AND USED AS THE ADDRESSING REGISTER. R4 IS SET TO 377 AND A
; MODE 1,0 CMPB INSTRUCTION IS USED THE RESULTS VERIFIED.
;*****
;TEST 100 TEST MODE 1 - EVEN BYTE W/ DOP NON-MODIFYING INST.
;*****
TST100: INC (R2) ;UPDATE TEST NUMBER
; SEQUENCE ERROR?
CMP #100,(R2) ;BR TO ERROR HALT ON SEQ ERROR
BNE TST101-10 ;R0=0
CLR R0 ;LOC 0=0
CLR (R0) ;LOC 0=177777
COM (R0) ;R4=0
CLR R4 ;R4=377
COMB R4 ;TRY MODE 1 - EVEN BYTE W/ DOP NON-MODIFYING
CMPB (R0),R4 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
BEQ TST101 ; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 771 <====
MOV #156, -(R2) ;MOVE TO MAILBOX # ***** 156 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;RESULT OF CMPB INCORRECT
; OR SEQUENCE ERROR

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005762 005212
005764 022712 000101
005770 001020
005772 005000
005774 005010
005776 105110
006000 005110
006002 005004
006004 005104
006006 111004
006010 005704
006012 001404

006014 012742 000157
006020 005242
006022 000000
006024 005110
006026 111004
006030 100404

006032 012742 000160
006036 005242
006040 000000

```
*****
:
: THIS TEST VERIFIES MODE 1,0 MOVB INSTRUCTIONS
: WHICH ADDRESS EVEN BYTES. LOC. 0 IS SET TO 177400, R0 IS CLEARED AND
: R4 IS SET TO -1. MOVB ARE USED TO MOVE BYTE 0 TO R4. THIS
: VERIFIES THAT THE PROPER BYTE WAS SELECTED AND THAT THE SIGN-X-TEND
: FUNCTION WITH MODE 0.
: THEN LOC. 0 IS COMPLEMENTED AND THE SAME PROCEDURE EXERCISES
: THE LOGIC FOR COMPLEMENTARY DATA.
: THIS TEST EXERCISES UNIQUE MICROCODE.
:
: *****
: TEST 101 TEST MOV INSTRUCTION MODE 1,0 EVEN BYTE
: *****
TST101: INC (R2) ;UPDATE TEST NUMBER
CMP #101,(R2) ;SEQUENCE ERROR?
BNE TST102-10 ;BR TO ERROR HALT ON SEQ ERROR
CLR R0 ;R0=0
CLR (R0) ;LOC 0=0
COMB (R0) ;LOC 0=177400
COM (R0)
CLR R4 ;R4=0
COM R4 ;R4=177777
MOVB (R0),R4 ;R4=0
TST R4 ;CHECK SIGN OF WORD
BEQ DOP1
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 767 <====
; MOVE TO MAILBOX # ***** 157 *****
; SET MSGTYP TO FATAL ERROR
; MOVB SHOULD SIGN X-TEND
; LOC 0=177777
; DO MOVB W/ EVEN BYTE
;
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 760 <====
; MOVE TO MAILBOX # ***** 160 *****
; SET MSGTYP TO FATAL ERROR
; MOVB SHOULD SIGN X-TEND
; OR SEQUENCE ERROR

```

DOP1:

MOV #157,-(R2)
INC -(R2)
HALT
DOP1: COM (R0)
MOVB (R0),R4
BMI TST102

MOV #160,-(R2)
INC -(R2)
HALT

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2917

006042 005212
006044 022712 000102
006050 001010
006052 005000
006054 005010
006056 005004
006060 005204
006062 105114
006064 151410
006066 005210
006070 001404

006072 012742 000161
006076 005242
006100 000000

```
*****
: THIS TEST VERIFIES MODE 1 DOP INSTRUCTIONS WHICH REFERENCE
: ODD BYTES. LOC. 0 IS SET TO 177400. R0 IS SET TO 0 AND R4 IS
: SET TO 1. THE BISB INSTRUCTION USES THE DATA IN BYTE 1 TO SET BYTE 0.
: THE RESULT IS CHECKED BY INCREMENTING THE WORD (LOC. 0) TO ZERO.
*****
: TEST 102 TEST MODE 1-ODD BYTE W/ DOP INSTS.
*****
TST102: INC (R2) ; UPDATE TEST NUMBER
: CMP #102,(R2) ; SEQUENCE ERROR?
: BNE TST103-10 ; BR TO ERROR HALT ON SEQ ERROR
: CLR R0 ; R0=0
: CLR (R0) ; LOC. 0=0
: CLR R4 ; R4=0
: INC R4 ; R4=1
: COMB (R4) ; LOC. 0=177400
: BISB (R4),(R0) ; TRY TO BIS LOW ORDER BITS W/ MODE 1
: INC (R0) ; CHECK RESULT
: BEQ TST103
:
: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
: CONDITIONAL BRANCH INST. AND <====
: REPLACE THE MOVE INSTRUCTION <====
: WHICH FOLLOWS W/ 770 <====
: MOVE TO MAILBOX # ***** 161 *****
: SET MSGTYP TO FATAL ERROR
: RESULT OF BISB INCORRECT
: OR SEQUENCE ERROR
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2954
2955

006102 005212
006104 022712 000103
006110 001015
006112 005000
006114 005010
006116 005110
006120 012004
006122 005204
006124 001404

006126 012742 000162
006132 005242
006134 000000
006136 005300
006140 005300
006142 001404

006144 012742 000163
006150 005242
006152 000000

TST103: INC (R2)
CMP #103,(R2)
BNE TST104-10
CLR R0
CLR (R0)
COM (R0)
MOV (R0)+,R4
INC R4
BEQ DOP2

DOP2: MOV #162,-(R2)
INC -(R2)
HALT
DEC R0
DEC R0
BEQ TST104

MOV #163,-(R2)
INC -(R2)
HALT

```
*****
;
; THIS TEST VERIFIES MODE 2 DOP INSTRUCTIONS. LOC. 0 IS SET TO -1.
; R0 IS CLEARED AND USED AS THE MODE 2 ADDRESSING REGISTER TO MOVE LOC. 0
; TO R7. THE DATA RESULTS ARE VERIFIED AND THE INCREMENTING OF THE REGISTER
; IS CHECKED.
;
;*****
; TEST 103 TEST MODE 2 W/ DOP INSTS.
;*****
TST103: INC (R2) ; UPDATE TEST NUMBER
        CMP #103,(R2) ; SEQUENCE ERROR?
        BNE TST104-10 ; BR TO ERROR HALT ON SEQ ERROR
        CLR R0 ; R0=0
        CLR (R0) ; LOC. 0=0
        COM (R0) ; LOC. 0=177777
        MOV (R0)+,R4 ; TRY MOVE MODE 2,0
        INC R4 ; CHECK R4
        BEQ DOP2
;
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 772 <====
; MOVE TO MAILBOX # ***** 162 *****
; SET MSGTYP TO FATAL ERROR
; RESULT OF MOV INST INCORRECT
; TEST R0 AFTER MODE 2
;
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 763 <====
; MOVE TO MAILBOX # ***** 163 *****
; SET MSGTYP TO FATAL ERROR
; REGISTER NOT INCREMENTED IN MODE 2
; OR SEQUENCE ERROR
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2969 006154 005212
2970 006156 022712 000104
2971 006162 001016
2972 006164 005000
2973 006166 010010
2974 006170 005110
2975 006172 142010
2976 006174 105737 000001
2977 006200 001404
2978
2979
2980
2981
2982 006202 012742 000164
2983 006206 005242
2984 006210 000000
2985 006212 105137 000000
2986 006216 001404
2987
2988
2989
2990
2991 006220 012742 000165
2992 006224 005242
2993 006226 000000
2994
    
```

```

;*****
;
;   THIS TEST VERIFIES MODE 2 DOP BYTE INSTRUCTIONS WHICH ADDRESS
;EVEN BYTES. LOC. 0 IS SET TO -1. R0 IS CLEARED AND USED AS THE
;ADDRESSING REGISTER IN A TEST WHICH TRIES TO CLEAR BYTE 1 USING
;BYTE 0 DATA AND A BICB. UNIQUE IN THIS TEST IS USE OF THE
;SAME ADDRESSING REGISTER FOR BOTH SOURCE AND DESTINATION. THE SOURCE AND
;DESTINATION IS CHECKED TO INSURE PROPER FUNCTIONING.
;*****
;TEST 104 TEST MODE 2 - EVEN BYTE W/ DOP INST.
;*****
TST104: INC (R2) ;UPDATE TEST NUMBER
        CMP #104,(R2) ;SEQUENCE ERROR?
        BNE TST105-10 ;BR TO ERROR HALT ON SEQ ERROR
        CLR R0 ;R0=0
        MOV R0,(R0) ;LOC. 0=0
        COM (R0) ;LOC. 0=177777
        BICB (R0)+,(R0) ;TRY TO CLEAR BYTE 1 FROM BYTE 0 W/ BICB
        TSTB @#1 ;CHECK RESULT
        BEQ DOPB2A
;
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 771 <====
; MOVE TO MAILBOX # ***** 164 *****
; SET MSGTYP TO FATAL ERROR
; BICB DESTINATION INCORRECT
; CHECK BICB SOURCE
;
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 762 <====
; MOVE TO MAILBOX # ***** 165 *****
; SET MSGTYP TO FATAL ERROR
; BICB SOURCE INCORRECTLY CHANGED
; OR SEQUENCE ERROR
    
```

```

TST104: INC (R2)
        CMP #104,(R2)
        BNE TST105-10
        CLR R0
        MOV R0,(R0)
        COM (R0)
        BICB (R0)+,(R0)
        TSTB @#1
        BEQ DOPB2A

DOPB2A: COMB @#0
        BEQ TST105
    
```

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2995
2996
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2999
3000
3001
3002
3003
3004
3005 006230 005212
3006 006232 022712 000105
3007 006236 001017
3008 006240 005000
3009 006242 005004
3010 006244 005010
3011 006246 005110
3012 006250 105120
3013 006252 112004
3014 006254 005204
3015 006256 001404
3016
3017
3018
3019
3020 006260 012742 000166
3021 006264 005242
3022 006266 000000
3023 006270 005740
3024 006272 005700
3025 006274 001404
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3030 006276 012742 000167
3031 006302 005242
3032 006304 000000
3033

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:*****
:
:   THIS TEST VERIFIES MODE 2 DOP BYTE INSTRUCTIONS WHICH REFERENCE
: ODD BYTES.  R0 IS SET TO 1, LOC. 0 IS SET TO 177400, AND R4 IS CLEARED.
: A MODE 2 MOV B USES R0 TO MOVE BYTE 1 TO R4.  AN INCREMENT
: IS USED TO CHECK THAT THE PROPER BYTE WAS MOVED AND SIGN X-TENDED.
:*****
:TEST 105      TEST MODE 2 - ODD BYTE W/ DOP INST.
:*****
TST105: INC      (R2)          ;UPDATE TEST NUMBER
        CMP      #105,(R2)   ;SEQUENCE ERROR?
        BNE     TST106-10   ;BR TO ERROR HALT ON SEQ ERROR
        CLR     R0          ;R0=0
        CLR     R4          ;R4=0
        CLR     (R0)        ;LOC. 0=0
        COM     (R0)        ;LOC. 0=177777
        COMB    (R0)+       ;LOC 0=177400; R0=1
        MOV B   (R0)+,R4    ;TRY DOP MODE 2 W/ ODD BYTE
        INC     R4          ;CHECK RESULT OF MOV B
        BEQ     DOPB2B
;
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
;           CONDITIONAL BRANCH INST. AND <====
;           REPLACE THE MOVE INSTRUCTION <====
;           WHICH FOLLOWS W/ 770 <====
; MOVE TO MAILBOX # ***** 166 *****
; SET MSGTYP TO FATAL ERROR
; RESULT OF MOV B INCORRECT
; BUMP R0 DOWN BY 2
; CHECK R0
;
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
;           CONDITIONAL BRANCH INST. AND <====
;           REPLACE THE MOVE INSTRUCTION <====
;           WHICH FOLLOWS W/ 761 <====
; MOVE TO MAILBOX # ***** 167 *****
; SET MSGTYP TO FATAL ERROR
; MODE 2 BYTE DID NOT INCREMENT REG. CORRECTLY
; OR SEQUENCE ERROR

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3006
3005
3004
3003
3002
3001
3000

006412 005212
006414 022712 000110
006420 001011
006422 012737 052652 000000
006430 005000
006432 153700 000001
006436 022700 000125
006442 001404

006444 012742 000172
006450 005242
006452 000000

006454 005212
006456 022712 000111
006462 001015
006464 012700 006536
006470 014037 006536
006474 064037 006536
006500 144037 006536
006504 154037 006537
006510 024037 006536
006514 001411

THIS TEST VERIFIES MODE 3 DOUBLE OPERAND BYTE INSTRUCTIONS WHICH ADDRESS ODD BYTES. THE SAME PROCEDURE USED IN PREVIOUS TEST IS USED HERE. THIS TIME BYTE 1 IS USED AS THE SOURCE BYTE. THE EXPECTED RESULT IS: RO = 125.

TEST 110 TEST MODE 3 - ODD BYTE W/ DOP INSTS.

TST110: INC (R2) ; UPDATE TEST NUMBER
CMP #110, (R2) ; SEQUENCE ERROR?
BNE TST111-10 ; BR TO ERROR HALT ON SEQ ERROR
MOV #52652, @#0 ; MOVE 1'S AND 0'S PATTERN TO LOC 0
CLR RO ; RO=0
BISB @#1, RO ; TRY RO=152 W/ MODE 3 - ODD BYTE
CMP #125, RO ; RO=125?
BEQ TST111

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS (====
; CONDITIONAL BRANCH INST. AND (====
; REPLACE THE MOVE INSTRUCTION (====
; WHICH FOLLOWS W/ 767 (====
MOV #172, -(R2) ; MOVE TO MAILBOX # ***** 172 *****
INC -(R2) ; SET MSGTYP TO FATAL ERROR
HALT ; BISB W/ MODE 3 - ODD BYTE FAILED
; OR SEQUENCE ERROR

THIS TEST VERIFIES MODE 4 DOUBLE OPERAND INSTRUCTIONS. THE TEST USES MODE 4 ADDRESSING WITH REGISTER 0 TO MOVE THRU A TABLE OF OPERANDS. THE TABLE OF OPERANDS AND THE WORK LOCATION IS STORED FOLLOWING THE TEST CODE. A SERIES OF 5 DOP INSTRUCTIONS UTILIZES THE DATA IN THE TABLE TO CYCLE THE WORK LOCATION THRU A SET OF VALUE. THE DATA HAS BEEN CHOSEN TO INSURE THAT NO SINGLE ERROR WILL GO UNDETECTED. WORD AND BYTE INSTRUCTION ACCESSING BOTH EVEN AND ODD ADDRESSES ARE USED IN THE TEST. THE LISTING SHOWS THE EXPECTED INTERMEDIATE RESULT AS EACH INSTRUCTION IS EXECUTED.

TEST 111 TEST MODE 4 W/ DOP INSTS.

TST111: INC (R2) ; UPDATE TEST NUMBER
CMP #111, (R2) ; SEQUENCE ERROR?
BNE DOP4 ; BR TO ERROR HALT ON SEQ ERROR
MOV #TBL1, RO ; INITIALIZE RO
MOV -(RO), @#TBL1 ; TBL1=125252
ADD -(RO), @#TBL1 ; TBL1=000377
BICB -(RO), @#TBL1 ; TBL1=000252
BISB -(RO), @#TBL1+1 ; TBL1=125252
CMP -(RO), @#TBL1 ; CHECK RESULT
BEQ TST112

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS (====
; CONDITIONAL BRANCH INST. AND (====
; REPLACE THE MOVE INSTRUCTION (====

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3145
3146 006516
3147 006516 012742 000173
3148 006522 005242
3149 006524 000000
3150
3151
3152 006526 125252
3153 006530 052652
3154 006532 053125
3155 006534 125252
3156 006536 000000
3157
3158
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3162
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3166
3167
3168
3169
3170 006540 005212
3171 006542 022712 000112
3172 006546 001015
3173 006550 012700 006624
3174 006554 015037 006536
3175 006560 065037 006536
3176 006564 145037 006536
3177 006570 155037 006537
3178 006574 025037 006536
3179 006600 001411
3180
3181
3182
3183
3184 006602
3185 006602 012742 000174
3186 006606 005242
3187 006610 000000
3188
3189 006612 006526
3190 006614 006530
3191 006616 006531
3192 006620 006532
3193 006622 006534

```

```

DOP4:
MOV #173, -(R2) ; MOVE TO MAILBOX # ***** 173 *****
INC -(R2) ; SET MSGTYP TO FATAL ERROR
HALT ; RESULT OF MODE 4 INSTS. INCORRECT
; OR SEQUENCE ERROR

```

```

125252
52652
53125
125252
TBL1: 0

```

```

*****
: THIS TEST VERIFIES MODE 5 DOUBLE OPERAND INSTRUCTIONS.
: THE TEST USES AN ADDRESS TABLE STORED FOLLOWING THE TEST CODE.
: THIS TABLE IS SIMPLY A TABLE OF ADDRESS POINTERS WHICH ADDRESS
: THE DATA TABLE USED IN THE PREVIOUS TEST. THE TEST IS IDENTICAL TO
: THE PREVIOUS TEST EXCEPT THE DATA IS REFERENCED USING THIS ADDRESS
: TABLE AND MODE 5 ADDRESSING. (SEE PREVIOUS TEST).
*****

```

```

*****
: TEST 112 TEST MODE 5 W/ DOP INSTS.
*****

```

```

TST112: INC (R2) ; UPDATE TEST NUMBER
CMP #112, (R2) ; SEQUENCE ERROR?
BNE DOP5 ; BR TO ERROR HALT ON SEQ ERROR
MOV #TBL2+2, R0 ; INITIALIZE R0
MOV @-(R0), @#TBL1 ; TBL1=125252
ADD @-(R0), @#TBL1 ; TBL1=000377
BICB @-(R0), @#TBL1 ; TBL1=000252
BISB @-(R0), @#TBL1+1 ; TBL1=125252
CMP @-(R0), @#TBL1 ; CHECK RESULT
BEQ TST113

```

```

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
; CONDITIONAL BRANCH INST. AND
; REPLACE THE MOVE INSTRUCTION
; WHICH FOLLOWS W/ 763

```

```

DOP5:
MOV #174, -(R2) ; MOVE TO MAILBOX # ***** 174 *****
INC -(R2) ; SET MSGTYP TO FATAL ERROR
HALT ; RESULT OF MODE 5 INSTS. INCORRECT
; OR SEQUENCE ERROR

```

```

TBL1-10
TBL1-6
TBL1-5
TBL1-4
TBL2: TBL1-2

```

3194
3195
3196
3197
3198
3199
3200
3201
3202
3203
3204
3205
3206
3207
3208 006624 005212
3209 006626 022712 000113
3210 006632 001022
3211 006634 012700 006532
3212 006640 016037 000002 006536
3213 006646 066037 000000 006536
3214 006654 146037 177777 006536
3215 006662 156037 177776 006537
3216 006670 026037 177774 006536
3217 006676 001404

```

*****
: THIS TEST VERIFIES MODE 6 DOUBLE OPERAND INSTRUCTIONS.
: IT USES THE SAME DATA AS THAT USED IN THE MODE 4 TESTS.
: THIS TIME THE DATA IS ACCESSED USING MODE 6.  RO IS SET
: TO POINT TO THE MIDDLE OF THE TABLE.  THE TABLE IS ACCESSED FROM
: BOTTOM TO TOP BY VARYING THE OFFSET IN THE MODE 6 INSTRUCTIONS.
: THE DATA RESULTS ARE IDENTICAL TO THOSE EXPECTED IN THE MODE 4
: TESTS.
*****

```

```

*****
: TEST 113 TEST MODE 6 W/ DOP INSTS.
*****

```

```

TST113: INC (R2) ;UPDATE TEST NUMBER
        CMP #113,(R2) ;SEQUENCE ERROR?
        BNE TST114-10 ;BR TO ERROR HALT ON SEQ ERROR
        MOV #TBL1-4,RO ;INITIALIZE RO
        MOV 2(RO),@#TBL1 ;TBL1=125252
        ADD 0(RO),@#TBL1 ;TBL1=000377
        BICB -1(RO),@#TBL1 ;TBL1=000252
        BISB -2(RO),@#TBL1+1 ;TBL1=125252
        CMP -4(RO),@#TBL1 ;CHECK RESULT
        BEQ TST114

```

```

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 756 <====
; MOVE TO MAILBOX # ***** 175 *****
; SET MSGTYP TO FATAL ERROR
; RESULT OF MODE 6 INSTS. INCORRECT
; OR SEQUENCE ERROR

```

3218
3219
3220
3221
3222 006700 012742 000175
3223 006704 005242
3224 006706 000000
3225
3226
3227
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3235
3236
3237
3238
3239

```

*****
: THIS TEST VERIFIES MODE 7 DOUBLE OPERAND INSTRUCTIONS.
: THIS TEST USES THE SAME ADDRESS TABLE AND DATA TABLE USED BY
: THE MODE 5 TESTS.  THIS TIME THE DATA IS ACCESSED USING MODE 7.
: RO IS SET TO POINT TO THE MIDDLE OF THE ADDRESS TABLE IN THE MODE 5
: TEST.  THE TABLE IS ACCESSED FROM BOTTOM TO TOP BY VARYING THE OFFSET
: IN THE MODE 7 INSTRUCTIONS.  THE DATA RESULTS ARE IDENTICAL TO
: THOSE EXPECTED IN THE MODE 5 TESTS.
*****

```

```

*****
: TEST 114 TEST MODE 7 W/ DOP INSTS.
*****

```

```

TST114: INC (R2) ;UPDATE TEST NUMBER
        CMP #114,(R2) ;SEQUENCE ERROR?
        BNE TST115-10 ;BR TO ERROR HALT ON SEQ ERROR
        MOV #TBL2-4,RO ;INITIALIZE RO
        MOV @4(RO),@#TBL1 ;TBL1=125252
        ADD @2(RO),@#TBL1 ;TBL1=000377
        BICB @0(RO),@#TBL1 ;TBL1=000252
        BISB @-2(RO),@#TBL1+1 ;TBL1=125252
        CMP @-4(RO),@#TBL1 ;CHECK RESULT
        BEQ TST115

```

3240 006710 005212
3241 006712 022712 000114
3242 006716 001022
3243 006720 012700 006616
3244 006724 017037 000004 006536
3245 006732 067037 000002 006536
3246 006740 147037 000000 006536
3247 006746 157037 177776 006537
3248 006754 027037 177774 006536
3249 006762 001404

```

3250      : TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
3251      :          CONDITIONAL BRANCH INST. AND <====
3252      :          REPLACE THE MOVE INSTRUCTION <====
3253      :          WHICH FOLLOWS W/ 756 <====
3254 006764 012742 000176      MOV #176,-(R2) ;MOVE TO MAILBOX # ***** 176 *****
3255 006770 005242      INC -(R2) ;SET MSGTYP TO FATAL ERROR
3256 006772 000000      HALT ;RESULT OF MODE 7 INSTS INCORRECT
3257      : OR SEQUENCE ERROR

```

```

3260      :
3261      : THIS TEST VERIFIES THE ROTATE MODE 0 INSTRUCTIONS.
3262      : R0 IS LOADED WITH A DATA PATTERN, THE C-BIT IS LOADED, AND
3263      : AN ROL INSTRUCTION IS EXECUTED WITH MODE 0. THE OPERATION IS CHECKED
3264      : BY TESTING THE RESULTING DATA AND THE STATE OF THE C AND V BITS.
3265      : NEXT, THE SAME PROCEDURE IS EXECUTED TO TEST MODE 0 BYTE INSTRUCTIONS.
3266      :

```

```

3267      : TEST 115 TEST ROTATE INSTRUCTIONS OF MODE 0
3268      : *****

```

```

3269 TST115: INC (R2) ;UPDATE TEST NUMBER
3270 006774 005212      CMP #115,(R2) ;SEQUENCE ERROR?
3271 006776 022712 000115      BNE TST116-10 ;BR TO ERROR HALT ON SEQ ERROR
3272 007002 001026      MOV #125252,R0 ;INITIALIZE DATA
3273 007004 012700 125252      SEC ;SET C-BIT
3274 007010 000261      ROL R0 ;TRY ROL W/ MODE 0
3275 007012 006100      BVC ROT0A ;CC=0011
3276 007014 102004      BCC ROT0A
3277 007016 103003      CMP #052525,R0 ;CHECK DATA
3278 007020 022700 052525      BEQ ROT0B
3279 007024 001404

```

```

3280      : TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
3281      :          CONDITIONAL BRANCH INST. AND <====
3282      :          REPLACE THE MOVE INSTRUCTION <====
3283      :          WHICH FOLLOWS W/ 767 <====

```

```

3284 007026      ROT0A: MOV #177,-(R2) ;MOVE TO MAILBOX # ***** 177 *****
3285 007026 012742 000177      INC -(R2) ;SET MSGTYP TO FATAL ERROR
3286 007032 005242      HALT ;ROL MODE 0 FAILED
3287 007034 000000      ROT0B: MOV #125252,R0 ;INITIALIZE DATA
3288 007036 012700 125252      SEC ;SET C-BIT
3289 007042 000261      ROLB R0 ;TRY ROL W/ MODE 0 EVEN BYTE
3290 007044 106100      BVC ROT0C ;CC=0011
3291 007046 102004      BCC ROT0C
3292 007050 103003      CMP #125125,R0 ;CHECK DATA
3293 007052 022700 125125      BEQ TST116
3294 007056 001404

```

```

3295      : TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
3296      :          CONDITIONAL BRANCH INST. AND <====
3297      :          REPLACE THE MOVE INSTRUCTION <====
3298      :          WHICH FOLLOWS W/ 752 <====

```

```

3299 007060      ROT0C: MOV #200,-(R2) ;MOVE TO MAILBOX # ***** 200 *****
3300 007060 012742 000200      INC -(R2) ;SET MSGTYP TO FATAL ERROR
3301 007064 005242      HALT ;ROLB MODE 0 FAILED
3302 007066 000000      ; OR SEQUENCE ERROR
3303

```

```

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3310
3311
3312
3313
3314
3315
3316
3317 007070 005212
3318 007072 022712 000116
3319 007076 001051
3320 007100 005000
3321 007102 012710 052525
3322 007106 000241
3323 007110 006110
3324 007112 102005
3325 007114 103404
3326 007116 023727 000000 125252
3327 007124 001404
3328
3329
3330
3331
3332 007126
3333 007126 012742 000201
3334 007132 005242
3335 007134 000000
3336 007136 000261
3337 007140 012710 125252
3338 007144 106110
3339 007146 102005
3340 007150 103004
3341 007152 022737 125125 000000
3342 007160 001404
3343
3344
3345
3346
3347 007162
3348 007162 012742 000202
3349 007166 005242
3350 007170 000000
3351 007172 012710 125252
3352 007176 005000
3353 007200 005200
3354 007202 000261
3355 007204 106110
3356 007206 102005
3357 007210 103004
3358 007212 022737 052652 000000
3359 007220 001404

```

```

*****
: THIS TEST VERIFIES THE ROTATE MODE 1 INSTRUCTIONS.
: THE DATA TO BE ROTATED IS IN LOC 0. R0 IS USED AS THE
: ADDRESSING REGISTER. THE C-BIT IS LOADED AND AN ROL IS EXECUTED.
: THE RESULTS ARE CHECKED BY COMPARING THE DATA RESULTS AND TESTING
: THE C AND V BITS. THIS PROCEDURE IS THEN REPEATED TWICE MORE
: TO TEST THE BYTE ROTATES. FIRST ON BYTE 0, THEN ON BYTE 1.
*****
: TEST 116 TEST ROTATE INSTRUCTIONS W/ MODE 1
*****
TST116: INC (R2) ;UPDATE TEST NUMBER
: CMP #116,(R2) ;SEQUENCE ERROR?
: BNE TST117-10 ;BR TO ERROR HALT ON SEQ ERROR
: CLR R0 ;POINT TO LOC. 0
: MOV #52525,(R0) ;INITIALIZE DATA
: CLC ;CLEAR C-BIT
: ROL (R0) ;TRY ROL W/ MODE 1
: BVC ROT1A ;CC=1010
: BCS ROT1A
: CMP #0,#125252 ;CHECK RESULT
: BEQ ROT1B
: ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
: ; CONDITIONAL BRANCH INST. AND <====
: ; REPLACE THE MOVE INSTRUCTION <====
: ; WHICH FOLLOWS W/ 765 <====
:
ROT1A: MOV #201,-(R2) ;MOVE TO MAILBOX # ***** 201 *****
: INC -(R2) ;SET MSGTYP TO FATAL ERROR
: HALT ;ROL MODE 1 FAILED
:
ROT1B: SEC
: MOV #125252,(R0) ;INITIALIZE DATA
: ROLB (R0) ;TRY ROLB W/ MODE 1 EVEN BYTE
: BVC ROT1C ;CC=1011
: BCC ROT1C
: CMP #125125,#0 ;TEST RESULT
: BEQ ROT1D
: ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
: ; CONDITIONAL BRANCH INST. AND <====
: ; REPLACE THE MOVE INSTRUCTION <====
: ; WHICH FOLLOWS W/ 747 <====
:
ROT1C: MOV #202,-(R2) ;MOVE TO MAILBOX # ***** 202 *****
: INC -(R2) ;SET MSGTYP TO FATAL ERROR
: HALT ;ROLB W/ MODE 1 EVEN BYTE FAILED
:
ROT1D: MOV #125252,(R0)
: CLR R0 ;POINT TO ODD BYTE
: INC R0
: SEC ;SET C-BIT
: ROLB (R0) ;TRY ROLB W/ MODE 1 ODD BYTE
: BVC ROT1E ;CC=0011
: BCC ROT1E
: CMP #052652,#0 ;CHECK DATA
: BEQ TST117

```

```

3360                                     ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
3361                                     ; CONDITIONAL BRANCH INST. AND <====
3362                                     ; REPLACE THE MOVE INSTRUCTION <====
3363                                     ; WHICH FOLLOWS W/ 727 <====
3364 007222                                ROT1E:
3365 007222 012742 000203                 MOV #203,-(R2) ;MOVE TO MAILBOX # ***** 203 *****
3366 007226 005242                       INC -(R2)      ;SET MSGTYP TO FATAL ERROR
3367 007230 000000                       HALT          ;ROLB W/ MODE 1 ODD BYTE FAILED
3368                                     ; OR SEQUENCE ERROR
3369
3370
3371
3372
3373                                     ;*****
3374                                     ; THIS TEST VERIFIES MODE 2 ROTATE INSTRUCTIONS.
3375                                     ; THE SAME PROCEDURE AS IN THE OTHER ROTATE TESTS ARE USED. RO
3376                                     ; IS USED AS THE ADDRESSING REGISTER AND IS CHECKED FOR PROPER
3377                                     ; INCREMENTING. BYTE INSTRUCTIONS ARE ALSO CHECKED.
3378                                     ;*****
3379 TEST 117 TEST ROTATE INSTRUCTIONS W/ MODE 2
3380 007232 005212                                TST117: INC (R2) ;UPDATE TEST NUMBER
3381 007234 022712 000117                   CMP #117,(R2) ;SEQUENCE ERROR?
3382 007240 001057                               BNE TST120-10 ;BR TO ERROR HALT ON SEQ ERROR
3383 007242 005000                               CLR RO ;POINT TO LOC 0
3384 007244 012710 173737                   MOV #173737,(RO) ;INITIALIZE DATA
3385 007250 000241                               CLC ;CLEAR C-BIT
3386 007252 006120                               ROL (RO)+ ;TRY ROL W/ MODE 2
3387 007254 103007                               BCC ROT2A ;CHECK C-BIT
3388 007256 022737 167676 000000          CMP #167676,#0 ;CHECK DATA
3389 007264 001003                               BNE ROT2A ;BRANCH IF RESULT INCORRECT
3390 007266 005300                               DEC RO ;TEST RO
3391 007270 005300                               DEC RO
3392 007272 001404                               BEQ ROT2B
3393
3394                                     ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
3395                                     ; CONDITIONAL BRANCH INST. AND <====
3396                                     ; REPLACE THE MOVE INSTRUCTION <====
3397                                     ; WHICH FOLLOWS W/ 763 <====
3398 007274                                ROT2A:
3399 007274 012742 000204                 MOV #204,-(R2) ;MOVE TO MAILBOX # ***** 204 *****
3400 007300 005242                       INC -(R2)      ;SET MSGTYP TO FATAL ERROR
3401 007302 000000                       HALT          ;ROL W/ MODE 2 FAILED
3402 007304 005000                                ROT2B: CLR RO ;POINT TO LOC 0
3403 007306 012710 004040                   MOV #4040,(RO) ;INITIALIZE DATA
3404 007312 000241                               CLC ;CLEAR C-BIT
3405 007314 106120                               ROLB (RO)+ ;TRY ROLB W/ MODE 2 EVEN BYTE
3406 007316 103406                               BCS ROT2C ;CHECK C-BIT
3407 007320 022737 004100 000000          CMP #4100,#0 ;CHECK DATA
3408 007326 001002                               BNE ROT2C ;BRANCH IF DATA INCORRECT
3409 007330 005300                               DEC RO ;CHECK RO
3410 007332 001404                               BEQ ROT2D
3411
3412                                     ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
3413                                     ; CONDITIONAL BRANCH INST. AND <====
3414                                     ; REPLACE THE MOVE INSTRUCTION <====
3415                                     ; WHICH FOLLOWS W/ 743 <====
3416 007334                                ROT2C:
3417 007334 012742 000205                 MOV #205,-(R2) ;MOVE TO MAILBOX # ***** 205 *****
    
```

```

3416 007340 005242      INC      -(R2)      ; SET MSGTYP TO FATAL ERROR
3417 007342 000000      HALT                    ; ROLB W/ MODE 2 EVEN BYTE FAILED
3418 007344 005000      ROT2D:  CLR      R0      ; POINT TO LOC 0
3419 007346 012710 004040  MOV      #4040,(R0)    ; INITIALIZE DATA
3420 007352 005200      INC      R0           ; POINT TO ODD BYTE OF DATA
3421 007354 000261      SEC                    ; SET C-BIT
3422 007356 106120      ROLB     (R0)+         ; TRY ROL W/ MODE 2 ODD BYTE
3423 007360 103407      BCS     ROT2E         ; CHECK C-BIT
3424 007362 022737 010440 000000  CMP      #10440,#0     ; CHECK DATA
3425 007370 001003      BNE     ROT2E         ; BRANCH IF DATA INCORRECT
3426 007372 005300      DEC     R0           ; CHECK R0
3427 007374 005300      DEC     R0
3428 007376 001404      SEQ     TST120
3429
3430
3431
3432
3433 007400      ROT2E:  MOV      #206,-(R2) ; MOVE TO MAILBOX # ***** 206 *****
3434 007400 012742 000206      INC      -(R2)         ; SET MSGTYP TO FATAL ERROR
3435 007404 005242      HALT                    ; ROLB W/ MODE 2 ODD BYTE FAILED
3436 007406 000000
3437
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 721 <====

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007410 005212
007412 022712 000120
007416 001051
007420 012737 052525 000000
007426 000261
007430 006137 000000
007434 103404
007436 022737 125253 000000
007444 001404

007446
007446 012742 000207
007452 005242
007454 000000
007456 012737 125252 000000
007464 000241
007466 006137 000000
007472 103004
007474 023727 000000 125124
007502 001404

007504
007504 012742 000210
007510 005242
007512 000000
007514 012737 125252 000000
007522 000261
007524 106137 000001
007530 103004
007532 022737 052652 000000
007540 001404

007542
007542 012742 000211
007546 005242
007550 000000

```
*****
: THIS TEST VERIFIES MODE 3 ROTATE INSTRUCTIONS.
: THIS TEST USES THE SAME PROCEDURES AS IN THE OTHER ROTATE
: TESTS. THE DATA IS STORED IN LOC. 0 AND IS ADDRESSED USING
: MODE 37. BYTE ADDRESSING IS ALSO CHECKED FOR EVEN AND ODD BYTES.
*****
: TEST 120 TEST ROTATE INSTRUCTIONS /W MODE 3
*****
TST120: INC (R2) ; UPDATE TEST NUMBER
: CMP #120,(R2) ; SEQUENCE ERROR?
: BNE TST121-10 ; BR TO ERROR HALT ON SEQ ERROR
: MOV #52525,a#0 ; INITIALIZE DATA IN LOC 0
: SEC ; SET C-BIT
: ROL a#0 ; TRO ROL W/ MODE 3
: BCS ROT3A ; CHECK C-BIT
: CMP #125253,a#0 ; CHECK DATA
: BEQ ROT3B
:
: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
: CONDITIONAL BRANCH INST. AND <====
: REPLACE THE MOVE INSTRUCTION <====
: WHICH FOLLOWS W/ 765 <====
:
ROT3A: MOV #207,-(R2) ; MOVE TO MAILBOX # ***** 207 *****
: INC -(R2) ; SET MSGTYP TO FATAL ERROR
: HALT ; ROL W/ MODE 3 FAILED
:
ROT3B: MOV #125252,a#0 ; INITIALIZE DATA
: CLC ; CLEAR C-BIT
: ROLB a#0 ; TRY ROL W/ MODE 3 EVEN BYTE
: BCC ROT3C ; CHECK C-BIT
:
45: CMP a#0,#125124 ; CHECK DATA
: BEQ ROT3D
:
: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
: CONDITIONAL BRANCH INST. AND <====
: REPLACE THE MOVE INSTRUCTION <====
: WHICH FOLLOWS W/ 746 <====
:
ROT3C: MOV #210,-(R2) ; MOVE TO MAILBOX # ***** 210 *****
: INC -(R2) ; SET MSGTYP TO FATAL ERROR
: HALT ; ROL W/ MODE 3 EVEN BYTE FAILED
:
ROT3D: MOV #125252,a#0 ; INITIALIZE DATA IN LOC. 0
: SEC ; SET C-BIT
: ROLB a#1 ; TRY ROL W/ MODE 3 ODD BYTE
: BCC ROT3E ; CHECK C-BIT
:
CMP #052652,a#0 ; CHECK DATA
: BEQ TST121
:
: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
: CONDITIONAL BRANCH INST. AND <====
: REPLACE THE MOVE INSTRUCTION <====
: WHICH FOLLOWS W/ 727 <====
:
ROT3E: MOV #211,-(R2) ; MOVE TO MAILBOX # ***** 211 *****
: INC -(R2) ; SET MSGTYP TO FATAL ERROR
: HALT ; ROL W/ MODE 3 ODD BYTE FAILED
```

L06

3494

; OR SEQUENCE ERROR

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3496
3497
3498
3499
3500
3501
3502
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3507
3508
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007552 005212
007554 022712 000121
007560 001016
007562 012737 070707 000000
007570 012700 000002
007574 000261
007576 006140
007600 103406
007602 022737 161617 000000
007610 001002
007612 005700
007614 001404

007616
007616 012742 000212
007622 005242
007624 000000

007626 005212
007630 022712 000122
007634 001021
007636 012737 007710 000000
007644 012700 000002
007650 012767 107070 000032
007656 000241
007660 006150
007662 103006

```
*****
;
; THIS TEST VERIFIES MODE 4 ROTATE INSTRUCTIONS. THE DATA IS
; STORED IN LOC. 0. RO IS SET TO 2 AND THE CARRY IS SET. AN ROL MODE 4
; IS USED TO ROTATE LOCATION 0 USING RO. THE DATA IS CHECKED
; AND THE C AND V BITS ARE TESTED. THE PROPER DECREMENTING OF
; RO IS VERIFIED.
;
;*****
; TEST 121 TEST MODE 4 W/ ROTATE INSTRUCTIONS
;*****
TST121: INC (R2) ; UPDATE TEST NUMBER
; CMP #121,(R2) ; SEQUENCE ERROR?
; BNE TST122-10 ; BR TO ERROR HALT ON SEQ ERROR
; MOV #070707,R0 ; INITIALIZE DATA IN LOC. 0
; MOV #2,RO ; INITIALIZE RO AS POINTER
; SEC ; SET C-BIT
; ROL -(RO) ; TRY ROL W/ MODE 4
; BCS ROT4 ; CHECK C-BIT
; CMP #161617,R0 ; CHECK DATA
; BNE ROT4 ; BRANCH IF DATA INCORRECT
; TST RO ; CHECK MODE 4 REGISTER
; BEQ TST122
```

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 762 <====

```
ROT4: MOV #212,-(R2) ; MOVE TO MAILBOX # ***** 212 *****
; INC -(R2) ; SET MSGTYP TO FATAL ERROR
; HALT ; ROL MODE 4 FAILED
; ; OR SEQUENCE ERROR
```

```
*****
;
; THIS TEST VERIFIES MODE 5 ROTATE INSTRUCTIONS.
; THE DATA IS STORED IN A WORK LOCATION (ROTX) AT THE END OF THE
; TEST CODE. LOC. 0 IS LOADED WITH THE ADDRESS OF THE DATA (ROTX).
; RO IS SET TO 2. THE CARRY IS CLEARED AND A MODE 5 ROL
; IS EXECUTED USING RO AS AN ADDRESSING REGISTER. THE DATA IS
; CHECKED, THE C AND V BITS TESTED, AND RO CHECKED FOR PROPER
; DECREMENTING.
;
;*****
```

```
*****
; TEST 122 TEST MODE 5 W/ ROTATE INSTRUCTIONS
;*****
TST122: INC (R2) ; UPDATE TEST NUMBER
; CMP #122,(R2) ; SEQUENCE ERROR?
; BNE ROT5 ; BR TO ERROR HALT ON SEQ ERROR
; MOV #ROTX,R0 ; MOVE POINTER TO LOC. 0
; MOV #2,RO ; SET MODE 5 REG. TO LOC. 0
; MOV #107070,ROTX ; INITIALIZE DATA
; CLC ; CLEAR C-BIT
; ROL R0-(R0) ; TRY ROL W/ MODE 5
; BCC ROT5 ; CHECK C-BIT
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007760 005212
007762 022712 000124
007766 001016
007770 012737 052525 007710
007776 012737 007710 010034
010004 000241
010006 006177 000022
010012 103404
010014 023727 007710 125252
010022 001405

010024
010024 012742 000215
010030 005242
010032 000000

010034 000000

010036 005212
010040 022712 000125
010044 001013
010046 012700 177400
010052 000300
010054 100404

010056 012742 000216
010062 005242
010064 000000

```
*****
: THIS TEST VERIFIES MODE 7 ROTATE INSTRUCTIONS.
: THE DATA IS SET IN LOC. ROTX, (SEE PREVIOUS TEST). THE ROL INSTRUCTION
: ADDRESSES IT INDIRECTLY USING MODE 7 AND INDIRECT ADDRESS LOCATION
: (ROTXAD) FOLLOWING THE TEST CODE.
*****
: TEST 124 TEST MODE 7 W/ ROTATE INSTRUCTIONS
*****
TST124: INC (R2) ; UPDATE TEST NUMBER
: CMP #124,(R2) ; SEQUENCE ERROR?
: BNE ROT7 ; BR TO ERROR HALT ON SEQ ERROR
: MOV #52525,2#ROTX ; INITIALIZE DATA
: MOV #ROTX,2#ROTXAD ; INITIALIZE ADDRESS POINTER
: CLC ; CLEAR C-BIT
: ROL 2ROTXAD ; TRY ROL W/ MODE 7
: BCS ROT7 ; CHECK C-BIT
: CMP 2#ROTX,#125252 ; CHECK DATA
: BEQ TST125
:
: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
: CONDITIONAL BRANCH INST. AND <====
: REPLACE THE MOVE INSTRUCTION <====
: WHICH FOLLOWS W/ 762 <====
:
ROT7: MOV #215,-(R2) ; MOVE TO MAILBOX # ***** 215 *****
: INC -(R2) ; SET MSGTYP TO FATAL ERROR
: HALT ; ROL W/ MODE 7 FAILED
: ; OR SEQUENCE ERROR
ROTXAD: 0
*****
: THIS TEST VERIFIES MODE 0 SWAB INSTRUCTION. RO IS SET TO
: 177400. A SWAB MODE 0 IS EXECUTED AND THE CONDITIONAL BRANCH
: IS USED TO CHECK THE SIGN OF THE RESULT. ALSO, A COMPARISON
: IS MADE TO CHECK THE DATA RESULTS.
*****
: TEST 125 TEST MODE 0 W/ SWAB INST.
*****
TST125: INC (R2) ; UPDATE TEST NUMBER
: CMP #125,(R2) ; SEQUENCE ERROR?
: BNE TST126-10 ; BR TO ERROR HALT ON SEQ ERROR
: MOV #177400,RO ; MOVE TEST PATTERN TO RO
: SWAB RO ; TRY SWAB MODE 0
: BMI 580
:
: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
: CONDITIONAL BRANCH INST. AND <====
: REPLACE THE MOVE INSTRUCTION <====
: WHICH FOLLOWS W/ 774 <====
:
: MOVE TO MAILBOX # ***** 216 *****
: SET MSGTYP TO FATAL ERROR
: SWAB DID NOT SET CC'S CORRECT
```

3650	010066	022700	000377	SBO:	CMP	#377, RD	;CHECK RESULT	
3651	010072	001404			BEO	TST126		
3652							: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS	<====
3653							: CONDITIONAL BRANCH INST. AND	<====
3654							: REPLACE THE MOVE INSTRUCTION	<====
3655							: WHICH FOLLOWS W/ 765	<====
3656	010074	012742	000217		MOV	#217, -(R2)	: MOVE TO MAILBOX # ***** 217 *****	
3657	010100	005242			INC	-(R2)	: SET MSGTYP TO FATAL ERROR	
3658	010102	000000			HALT		: RESULT OF SWAB MODE 0 FAILED	
3659							: OR SEQUENCE ERROR	

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3671 010104 005212
3672 010106 022712 000126
3673 010112 001011
3674 010114 012737 125652 000000
3675 010122 005000
3676 010124 000310
3677 010126 022737 125253 000000
3678 010134 001404
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3683 010136 012742 000220
3684 010142 005242
3685 010144 000000
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3699 010146 005212
3700 010150 022712 000127
3701 010154 001020
3702 010156 012737 125152 000000
3703 010164 005000
3704 010166 000320
3705 010170 022737 065252 000000
3706 010176 001404
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3711 010200 012742 000221
3712 010204 005242
3713 010206 000000
3714 010210 162700 000002
3715 010214 001404

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*****
: THIS TEST VERIFIES MODE 1 SWAB INSTRUCTION. THE TEST
: PATTERN IS MOVED TO LOC 0. R0 IS CLEARED AND USED AS THE ADDRESSING
: REGISTER IN THE MODE 1 SWAB. THE DATA RESULTS ARE CHECKED WITH
: A COMPARE.
*****

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*****
: TEST 126 TEST MODE 1 W/ SWAB INST
*****

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```

TST126: INC (R2) ;UPDATE TEST NUMBER
: CMP #126,(R2) ;SEQUENCE ERROR?
: BNE TST127-10 ;BR TO ERROR HALT ON SEQ ERROR
: MOV #125652,R#0 ;MOVE TEST PATTERN TO LOC. 0
: CLR R0 ;R0=0
: SWAB (R0) ;TRY SWAB MODE 1
: CMP #125253,R#0 ;CHECK RESULT
: BEQ TST127
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS (=====
: CONDITIONAL BRANCH INST. AND (=====
: REPLACE THE MOVE INSTRUCTION (=====
: WHICH FOLLOWS W/ 767 (=====
: MOVE TO MAILBOX # ***** 220 *****
: SET MSGTYP TO FATAL ERROR
: RESULT OF SWAB MODE 1 FAILED
: OR SEQUENCE ERROR

```

```

*****
: THIS TEST VERIFIES MODE 2 SWAB INSTRUCTION. THE TEST
: PATTERN IS MOVED TO LOC 0. R0 IS CLEARED AND USED AS THE MODE
: 2 ADDRESSING REGISTER. THE RESULTS ARE CHECKED WITH A COMPARE.
: R0 IS CHECKED FOR PROPER DECREMENTING.
*****

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*****
: TEST 127 TEST MODE 2 W/ SWAB INST
*****

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TST127: INC (R2) ;UPDATE TEST NUMBER
: CMP #127,(R2) ;SEQUENCE ERROR?
: BNE TST130-10 ;BR TO ERROR HALT ON SEQ ERROR
: MOV #125152,R#0 ;MOVE TEST PATTERN TO LOC. 0
: CLR R0 ;R0=0
: SWAB (R0)+ ;TRY SWAB MODE 2
: CMP #65252,R#0 ;CHECK RESULT
: BEQ SB2
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS (=====
: CONDITIONAL BRANCH INST. AND (=====
: REPLACE THE MOVE INSTRUCTION (=====
: WHICH FOLLOWS W/ 767 (=====
: MOVE TO MAILBOX # ***** 221 *****
: SET MSGTYP TO FATAL ERROR
: RESULT OF SWAB MODE 0 FAILED
: CHECK EFFECT OF REG.
SB2: SUB #2,R0
: BEQ TST130

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010270 005212
010272 022712 000131
010276 001020
010300 012737 125652 000000
010306 012700 000002
010312 000340
010314 022737 125253 000000
010322 001404

010324 012742 000224
010330 005242
010332 000000
010334 005700
010336 001404

010340 012742 000225
010344 005242
010346 000000

```
*****
THIS TEST VERIFIES MODE 4 SWAB INSTRUCTIONS. THE DATA
IS MOVED TO LOC 0. R0 IS SET TO 2 AND USED AS THE MODE 4 ADDRESSING
REGISTER. THE DATA IS CHECKED WITH A COMPARE AND R0 IS CHECKED
FOR PROPER DECREMENTING.
*****
TEST 131 TEST MODE 4 W/ SWAB INST
*****
TST131: INC (R2) ;UPDATE TEST NUMBER
CMP #131,(R2) ;SEQUENCE ERROR?
BNE TST132-10 ;BR TO ERROR HALT ON SEQ ERROR
MOV #125652,2#0 ;MOVE TEST PATTERN TO LOC. 0
MOV #2,R0 ;SET UP REGISTER POINTER
SWAB -(R0) ;TRY SWAB MODE 4
CMP #125253,2#0 ;CHECK RESULT
BEQ SB4

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 766 <====
; MOVE TO MAILBOX # ***** 224 *****
; SET MSGTYP TO FATAL ERROR
; RESULT OF SWAB INCORRECT
; CHECK EFFECT ON REG.

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 760 <====
; MOVE TO MAILBOX # ***** 225 *****
; SET MSGTYP TO FATAL ERROR
; REGISTER VALUE INCORRECT
; OR SEQUENCE ERROR

SB4: TST R0
BEQ TST132
MOV #224, -(R2)
INC -(R2)
HALT
TST R0
BEQ TST132
MOV #225, -(R2)
INC -(R2)
HALT
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010350 005212
010352 022712 000132
010356 001021
010360 012700 010436
010364 012767 125125 000040
010372 000350
010374 022767 052652 000030
010402 001404

010404 012742 000226
010410 005242
010412 000000
010414 020027 010434
010420 001406

010422
010422 012742 000227
010426 005242
010430 000000

010432 000000
010434 010432

TST132: INC (R2)
CMP #132,(R2)
BNE SB5
MOV #SB5XAD+2,R0
MOV #125125,SB5X
SWAB @-(R0)
CMP #52652,SB5X
BEQ SB5A

MOV #226,-(R2)
INC -(R2)
HALT
SBSA: CMP R0,#SB5XAD
BEQ TST133

SBS: MOV #227,-(R2)
INC -(R2)
HALT

SBSX: 0
SB5XAD: SB5X

THIS TEST VERIFIES MODE 5 SWAB INSTRUCTION. THE TEST USES
TWO LOCATIONS FOLLOWING THE TEST CODE. SB5X HOLDS THE DATA;
SB5XAD IS A POINTER TO THE DATA LOCATION. THE DATA IS MOVED TO
SB5X AND R0 IS SET TO TWO PLUS THE ADDRESS OF SB5XAD. FOLLOWING
THE MODE 5 SWAB SB5X IS CHECKED FOR THE PROPER DATA. R0 IS
CHECKED TO SEE THAT IT WAS DECREMENTED PROPERLY.

TEST 132 TEST MODE 5 W/ SWAB INST.

;UPDATE TEST NUMBER
;SEQUENCE ERROR?
;BR TO ERROR HALT ON SEQ ERROR
;SET UP POINTER TO WORK LOCATION
;MOVE PATTERN TO WORK LOCATION
;TRY SWAB MODE 5
;CHECK RESULT

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 766 <====
;MOVE TO MAILBOX # ***** 226 *****
;SET MSGTYP TO FATAL ERROR
;RESULT OF SWAB INCORRECT
;CHECK RESULT OF REG.

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 757 <====
;MOVE TO MAILBOX # ***** 227 *****
;SET MSGTYP TO FATAL ERROR
;REGISTER VALUE INCORRECT
; OR SEQUENCE ERROR
;WORK LOCATION

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 3862

010436	005212		
010440	022712	000133	
010444	001013		
010446	012767	125125	000030
010454	012700	010476	
010460	000360	000006	
010464	022760	052652	000006
010472	001405		
010474			
010474	012742	000230	
010500	005242		
010502	000000		
010504	000000		

```

*****
THIS TEST VERIFIES MODE 6 SWAB INSTRUCTION. THIS TEST
USES A WORK LOCATION (SB6X) FOLLOWING THE TEST CODE. TEST DATA
IS LOADED INTO THE WORK LOCATION. R0, THE ADDRESSING REGISTER
IS LOADED WITH 6 LESS THEN THE ADDRESS OF THE WORK LOCATION.
THE MODE 6 SWAB IS EXECUTED WITH A +6 OFFSET. THE DATA IS
VERIFIED WITH A COMPARE.
*****
TEST 133 TEST MODE 6 W/ SWAB INST.
*****
TST133: INC (R2) ;UPDATE TEST NUMBER
CMP #133,(R2) ;SEQUENCE ERROR?
BNE SB6 ;BR TO ERROR HALT ON SEQ ERROR
MOV #125125,SB6X ;MOVE PATTERN TO WORK LOCATION
MOV #SB6X-6,R0 ;MOVE OFFSET POINTER TO R0
SWAB 6(R0) ;TRY SWAB W/ MODE 6
CMP #52652,6(R0) ;CHECK RESULT
BEQ TST134

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 765 <====

SB6: MOV #230,-(R2) ;MOVE TO MAILBOX # ***** 230 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;RESULT OF SWAB INCORRECT
; OR SEQUENCE ERROR
SB6X: 0 ;WORK LOCATION
  
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010506 005212
010510 022712 000134
010514 001013
010516 012767 177400 000030
010524 012700 010464
010530 000370 000072
010534 027027 000072 000377
010542 001406

010544
010544 012742 000231
010550 005242
010552 000000

010554 000000
010556 010554

```
*****
:
:   THIS TEST VERIFIES MODE 7 SWAB INSTRUCTION.  THIS TEST
:   USES TWO LOCATIONS FOLLOWING THE TEST CODE:  A WORK LOCATION
:   (SB7X) AND A POINTER TO THE WORK LOCATION (SB7XAD).  DATA IS MOVED
:   TO THE WORK LOCATION.  RO IS LOADED WITH 72 LESS THAN THE ADDRESS
:   OF THE ADDRESS POINTER.  THE DATA IS SWAB'ED USING A MODE 7
:   INSTRUCTION WITH AN OFFSET OF +72.  THE DATA IS VERIFIED WITH A
:   COMPARE.
:
:*****
:TEST 134      TEST MODE 7 W/ SWAB INST.
:*****
TST134: INC      (R2)           ;UPDATE TEST NUMBER
        CMP      #134,(R2)    ;SEQUENCE ERROR?
        BNE     SB7          ;BR TO ERROR HALT ON SEQ ERROR
        MOV     #177400,SB7X  ;MOVE PATTERN TO WORK LOCATION
        MOV     #SB7XAD-72,RO ;MOVE OFFSET POINTER TO RO
        SWAB   @72(RO)       ;TRY SWAB MODE 7
        CMP     @72(RO),#377  ;CHECK RESULTS
        BEQ    TST135

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  <====
; CONDITIONAL BRANCH INST. AND          <====
; REPLACE THE MOVE INSTRUCTION         <====
; WHICH FOLLOWS W/ 765                  <====

SB7:    MOV     #231,-(R2)    ;MOVE TO MAILBOX # ***** 231 *****
        INC     -(R2)        ;SET MSGTYP TO FATAL ERROR
        HALT                    ;RESULT OF SWAB INCORRECT
; OR SEQUENCE ERROR
SB7X:   0                    ;WORK LOCATION
SB7XAD: SB7X                ;POINTER TO WORK LOCATION
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THIS TEST VERIFIES ALL LEGAL MODES OF THE JMP INSTRUCTION.
BECAUSE OF THE NATURE OF THE INSTRUCTION UNDER TEST, THIS TEST
UTILIZES SEVERAL DIFFERENT TECHNIQUES. THE CODE IS NOT EXECUTED
IN A LINEAR FASHION. THE DIFFERENT MODES ARE EXECUTED IN ORDER
FROM 1-7; HOWEVER, THE CODE IS ARRANGED SO THAT CONTROL LEAP
FROGS THRU THE TEST CODE. THE ORDER OF APPEARANCE OF THE CODE
IS:

- JMP MODE 1
- JMP MODE 3
- JMP MODE 2
- JMP MODE 4
- JMP MODE 6
- JMP MODE 5
- JMP MODE 7

AN INTERNAL SEQUENCE TEST (JMPSEQ) IS USED TO INSURE THAT THE
JUMPS ARE OCCURRING IN THE PROGRAMMED SEQUENCE.

THE TEST IS MADE UP OF SEVERAL BLOCKS OF CODE. EACH CODE
BEGINS WITH A LABEL WHICH INDICATES THE MODE BEING EXECUTED IN
THAT BLOCK. A SIMPLE PROCEDURE IS FOLLOWED IN EACH BLOCK. FOR
EXAMPLE THE CODE BEGINNING AT JMP3 WILL FIRST COMPARE THE RESULTS
OF THE PREVIOUS MODE 2 JUMP. (ANY REGISTER CHANGES ARE VERIFIED
AND THE SEQUENCE CHECK IS MADE). THEN THE REGISTERS ARE SETUP
FOR A MODE 3 JUMP TO THE NEXT TEST BLOCK (HERE, JMP4), THE SEQUENCE
CHECKER IS UPDATED AND THE JUMP IS EXECUTED.

IF A FAILURE OCCURS, THE SEQUENCE CHECKER WILL ASSIST IN
DETERMINING JUST WHICH MODE FAILED. IF THE SEQUENCE IS CORRECT
THEN THE ERROR DETECTED WAS A MODE FAILURE (E.G. FAILURE OF THE
REGISTER TO BE INCREMENTED IN MODE 2 JUMP.)

TEST 135 TEST THE JMP INSTRUCTION IN ALL MODES

```

TST135: INC      (R2)          ;UPDATE TEST NUMBER
        CMP      #135, (R2)   ;SEQUENCE ERROR?
        BNE     JMPCK+6      ;BR TO ERROR HALT ON SEQ ERROR
        CLR     JMPSEQ       ;ESTABLISH A SEQUENCE CHECKER
        MOV     #JMP2, R0     ;SET R0=JUMP TARGET
        JMP     (R0)         ;TRY JMP MODE 1
JMP3:   CMP     #.+2, R0      ;CHECK RESULT OF MODE 2 JUMP
        BEQ     JMP3A

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
;           CONDITIONAL BRANCH INST. AND <====
;           REPLACE THE MOVE INSTRUCTION <====
;           WHICH FOLLOWS W/ 770 <====
        MOV     #232, -(R2)   ;MOVE TO MAILBOX # ***** 232 *****
        INC     -(R2)        ;SET MSGTYP TO FATAL ERROR
        HALT    .            ;REGISTER VALUE AFTER JMP MODE 2 INCORRECT
JMP3A:  CMP     JMPSEQ, #1    ;MAKE SURE JUMPS ARE IN SEQUENCE: JMPSEQ=1?
        BEQ     JMP3B

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
;           CONDITIONAL BRANCH INST. AND <====
;           REPLACE THE MOVE INSTRUCTION <====
;           WHICH FOLLOWS W/ 760 <====

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010560	005212		
010562	022712	000135	
010566	001150		
010570	005067	000326	
010574	012700	010654	
010600	000110		
010602	022700	010604	
010606	001404		
010610	012742	000232	
010614	005242		
010616	000000		
010620	026727	000276	000001
010626	001404		

3953	010630	012742	000233		MOV	#233, -(R2)	; MOVE TO MAILBOX # ***** 233 *****
3954	010634	005242			INC	-(R2)	; SET MSGTYP TO FATAL ERROR
3955	010636	000000			HALT		; SHOULD BE HERE FROM JMP MODE 2 ONLY
3956	010640	012700	010652	JMP3B:	MOV	#IIMP4, R0	; POINT R0 TO INDIRECT JMP ADDR.
3957	010644	005267	000252		INC	JMPSEQ	; UPDATE SEQUENCE CHECKER
3958	010650	000130			JMP	2(R0)+	; TRY JMP MODE 3
3959	010652	010704		IIMP4:	JMP4		; ADDRESS INDIRECT JUMP
3960							
3961	010654	005767	000242	JMP2:	TST	JMPSEQ	; CHECK THAT JMPs ARE IN SEQUENCE: JMPSEQ=0?
3962	010660	001404			BEQ	JMP2A	
3963							; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
3964							; CONDITIONAL BRANCH INST. AND <====
3965							; REPLACE THE MOVE INSTRUCTION <====
3966							; WHICH FOLLOWS W/ 743 <====
3967	010662	012742	000234		MOV	#234, -(R2)	; MOVE TO MAILBOX # ***** 234 *****
3968	010666	005242			INC	-(R2)	; SET MSGTYP TO FATAL ERROR
3969	010670	000000			HALT		; SHOULD BE HERE FROM JMP MODE 1 ONLY
3970	010672	005267	000224	JMP2A:	INC	JMPSEQ	; UPDATE SEQUENCE CHECKER
3971	010676	012700	010602		MOV	#JMP3, R0	; SET R0=JUMP TARGET
3972	010702	000120			JMP	(R0)+	; TRY A JUMP MODE 2 TO "JMP3"
3973	010704	022700	010654	JMP4:	CMP	#IIMP4+2, R0	; CHECK RESULT OF REGISTER IN MODE 3 JUMP
3974	010710	001404			BEQ	JMP4A	
3975							; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
3976							; CONDITIONAL BRANCH INST. AND <====
3977							; REPLACE THE MOVE INSTRUCTION <====
3978							; WHICH FOLLOWS W/ 727 <====
3979	010712	012742	000235		MOV	#235, -(R2)	; MOVE TO MAILBOX # ***** 235 *****
3980	010716	005242			INC	-(R2)	; SET MSGTYP TO FATAL ERROR
3981	010720	000000			HALT		; REGISTER VALUE AFTER MODE 3 JUMP INCORRECT
3982	010722	022767	000002	000172	JMP4A:	CMP	#2, JMPSEQ
3983	010730	001404			BEQ	JMP4B	; CHECK JUMP SEQUENCE: JMPSEQ=2?
3984							; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
3985							; CONDITIONAL BRANCH INST. AND <====
3986							; REPLACE THE MOVE INSTRUCTION <====
3987							; WHICH FOLLOWS W/ 717 <====
3988	010732	012742	000236		MOV	#236, -(R2)	; MOVE TO MAILBOX # ***** 236 *****
3989	010736	005242			INC	-(R2)	; SET MSGTYP TO FATAL ERROR
3990	010740	000000			HALT		; SHOULD BE ONLY FROM MODE 3 JUMP
3991	010742	012700	011012	JMP4B:	MOV	#JMP5+2, R0	; SET UP POINTER TO JUMP TARGET
3992	010746	005267	000150		INC	JMPSEQ	; UPDATE SEQUENCE CHECKER
3993	010752	000140			JMP	-(R0)	; TRY JUMP MODE 4 TO "JMP4"
3994							
3995	010754	022767	000004	000140	JMP6:	CMP	#4, JMPSEQ
3996	010762	001404			BEQ	JMP6A	; CHECK THAT JUMPS ARE IN SEQUENCE: JMPSEQ=4?
3997							; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
3998							; CONDITIONAL BRANCH INST. AND <====
3999							; REPLACE THE MOVE INSTRUCTION <====
4000							; WHICH FOLLOWS W/ 702 <====
4001	010764	012742	000237		MOV	#237, -(R2)	; MOVE TO MAILBOX # ***** 237 *****
4002	010770	005242			INC	-(R2)	; SET MSGTYP TO FATAL ERROR
4003	010772	000000			HALT		; SHOULD BE HERE ONLY FROM MODE 5 JUMP
4004	010774	012700	011442	JMP6A:	MOV	#JMP7+376, R0	; SET UP OFFSET POINTER TO JUMP TARGET
4005	011000	005267	000116		INC	JMPSEQ	; UPDATE JUMP SEQUENCE
4006	011004	000160	177402		JMP	-376(R0)	; TRY MODE 6 JUMP
4007							
4008	011010	022767	000003	000104	JMP5:	CMP	#3, JMPSEQ
							; CHECK THAT JUMPS ARE IN SEQUENCE: JMPSEQ=3?

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4009 011016 001404          BEQ      JMP5A
4010                                     ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
4011                                     ; CONDITIONAL BRANCH INST. AND <====
4012                                     ; REPLACE THE MOVE INSTRUCTION <====
4013                                     ; WHICH FOLLOWS W/ 664 <====
4014 011020 012742 000240      MOV      #240, -(R2)
4015 011024 005242              INC      -(R2)
4016 011026 000000              HALT
4017 011030 012700 011044      JMP5A:  MOV      #IIMP5+2, R0
4018 011034 005267 000062      INC      JMPSEQ
4019 011040 000150              JMP      @-(R0)
4020 011042 010754              IIMP5:  JMP6
4021
4022 011044 022767 000005 000050 JMP7:   CMP      #5, JMPSEQ
4023 011052 001404              BEQ      JMP7A
4024                                     ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
4025                                     ; CONDITIONAL BRANCH INST. AND <====
4026                                     ; REPLACE THE MOVE INSTRUCTION <====
4027                                     ; WHICH FOLLOWS W/ 646 <====
4028 011054 012742 000241      MOV      #241, -(R2)
4029 011060 005242              INC      -(R2)
4030 011062 000000              HALT
4031 011064 012700 011110      JMP7A:  MOV      #IIMP+10, R0
4032 011070 005267 000026      INC      JMPSEQ
4033 011074 000170 177770      JMP      @-10(R0)
4034 011100 011102              IIMP:   JMPCK
4035
4036 011102 026727 000014 000006 JMPCK:  CMP      JMPSEQ, #6
4037 011110 001405              BEQ      TST136
4038                                     ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
4039                                     ; CONDITIONAL BRANCH INST. AND <====
4040                                     ; REPLACE THE MOVE INSTRUCTION <====
4041                                     ; WHICH FOLLOWS W/ 627 <====
4042 011112 012742 000242      MOV      #242, -(R2)
4043 011116 005242              INC      -(R2)
4044 011120 000000              HALT
4045
4046 011122 000000              JMPSEQ: 0

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4067 011124 005212
4068 011126 022712 000136
4069 011132 001001
4070 011134 000402
4071 011136 000137 011572
4072
4073 011142 012706 000500
4074 011146 012700 011254
4075 011152 005037 011552
4076 011156 005001
4077 011160 005101
4078 011162 004110
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4081 011164
4082 011164 012742 000243
4083 011170 005242
4084 011172 000000
4085
4086 011174 022737 000001 011552
4087 011202 001014
4088 011204 020127 011336
4089 011210 001011
4090 011212 022706 000476
4091 011216 001006
4092 011220 022716 125252
4093 011224 001003
4094 011226 022700 011176
4095 011232 001404
4096
4097
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4100 011234
4101 011234 012742 000244
4102 011240 005242

```

;*****
; THIS TEST VERIFIES ALL LEGAL MODES OF THE JSR INSTRUCTION.
; THE CONCEPT OF LEAP FROGGING AND SEQUENCE CHECKING (JSRSEQ) IS
; IDENTICAL TO THAT USED IN JMP TEST (SEE PREVIOUS TEST). EACH
; BLOCK OF CODE VERIFIES THE PREVIOUS JSR BY CHECKING THE SEQUENCE,
; CHECKING THAT THE PC WAS SAVED IN THE SPECIFIED REGISTER, CHECKING
; THAT THE SP WAS DECREMENTED, CHECKING THAT THE REGISTER WAS
; SAVED ON THE STACK, AND FINALLY CHECKING THAT ANY MODE ADDRESS
; REGISTER ALTERATIONS (E.G. INCREMENT REGISTER IN MODE 2) WERE
; SUCCESSFUL. R1 IS USED AS THE REGISTER IN ALL JSR INSTRUCTIONS.
; IF A FAILURE OCCURS, THE SEQUENCE CHECKER WILL ASSIST IN
; DETERMINING JUST WHICH MODE FAILED. IF THE SEQUENCE IS CORRECT
; THEN THE ERROR DETECTED WAS A FUNCTIONAL FAILURE (E.G., INCORRECT
; REGISTER SAVED).
;*****
; TEST 136 TEST JSR INSTRUCTION W/ ALL MODES
;*****
TST136: INC (R2) ;UPDATE TEST NUMBER
CMP #136,(R2) ;SEQUENCE ERROR?
BNE JSR0 ;BR TO ERROR HALT ON SEQ ERROR
BR JSR1
JSR0: JMP @#JSRCK1

JSR1: MOV #STBOT,R6 ;SET STACK POINTER
MOV #JSR2,R0 ;SET TARGET ADDRESS
CLR @#JSRSEQ ;INITIALIZE SEQUENCE CHECKER
CLR R1 ;INITIALIZE R1
COM R1
JSR R1,(R0) ;TRY JSR MODE 1
; TO SCOPE: REPLACE THE MOVE INSTRUCTION <====
; FOLLOWING W/ 774 <====

JSR1A: MOV #243,-(R2) ;MOVE TO MAILBOX # ***** 243 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;JSR MODE 1 FAILED

JSR3: CMP #1,@#JSRSEQ ;CHECK SEQUENCE: JSRSEQ=1?
BNE JSR3A ;BRANCH IF OUT OF SEQUENCE
CMP R1,#JSR4 ;PROPER PC SAVED?
BNE JSR3A ;BRANCH IF PC WRONG
CMP #STBOT-2,R6 ;STACK POINTER DECREMENTED?
BNE JSR3A ;BRANCH IF SP WRONG
CMP #125252,(R6) ;REG SAVED ON STACK?
BNE JSR3A ;BRANCH IF REG. NOT SAVED
CMP #JSR3+2,R0 ;MODE 2 INCREMENT CORRECT?
BEQ JSR3B
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 740 <====

JSR3A: MOV #244,-(R2) ;MOVE TO MAILBOX # ***** 244 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR


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4159 011432 005237 011552 JSR6B: INC 2#JSRSEQ ;UPDATE SEQUENCE CHECKER
4160 011436 004167 00J046 JSR R1,JSR7 ;TRY JSR MODE 6
4161 011442 022767 000003 000102 JSR5: CMP 3#JSRSEQ ;CHECK SEQUENCE: JSRSEQ=3?
4162 011450 001006 BNE JSR5A ;BRANCH IF OUT OF SEQUENCE
4163 011452 022701 011376 CMP 2#JSR6,R1 ;PROPER PC SAVED?
4164 011456 001003 BNE JSR5A ;BRANCH IF PC WRONG
4165 011460 022700 011442 CMP 2#JSR5,R0 ;CHECK MODE 4 REGISTER
4166 011464 001404 BEQ JSR5B
4167 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====
4168 ; CONDITIONAL BRANCH INST. AND <=====
4169 ; REPLACE THE MOVE INSTRUCTION <=====
4170 ; WHICH FOLLOWS W/ 623 <=====
4171 011466 JSR5A:
4172 011466 012742 000250 MOV 250,-(R2) ;MOVE TO MAILBOX # ***** 250 *****
4173 011472 005242 INC -(R2) ;SET MSGTYP TO FATAL ERROR
4174 011474 000000 HALT ;JSR MODE 4 MALFUNCTIONED
4175 011476 005237 011552 JSR5B: INC 2#JSRSEQ ;UPDATE SEQUENCE CHECKER
4176 011502 012700 011550 MOV 2#JSR6AD+2,R0 ;POINT R0 TO TARGET ADDRESS
4177 011506 004150 JSR R1,2-(R0) ;TRY JSR MODE 5
4178
4179 011510 022737 000005 011552 JSR7: CMP 5,2#JSRSEQ ;CHECK SEQUENCE: JSRSEQ=5?
4180 011516 001003 BNE JSR7A ;BRANCH IF OUT OF SEQUENCE
4181 011520 022701 011442 CMP 2#JSR5,R1 ;PROPER PC SAVED?
4182 011524 001404 BEQ JSR7B
4183 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====
4184 ; CONDITIONAL BRANCH INST. AND <=====
4185 ; REPLACE THE MOVE INSTRUCTION <=====
4186 ; WHICH FOLLOWS W/ 603 <=====
4187 011526 JSR7A:
4188 011526 012742 000251 MOV 251,-(R2) ;MOVE TO MAILBOX # ***** 251 *****
4189 011532 005242 INC -(R2) ;SET MSGTYP TO FATAL ERROR
4190 011534 000000 HALT ;JSR MODE 6 FAILED
4191 011536 005237 011552 JSR7B: INC 2#JSRSEQ ;UPDATE SEQUENCE CHECKER
4192 011542 004177 000002 JSR R1,2JSRCKAD ;TRY JSR MODE 7
4193
4194 JSR6AD: JSR6 ;MODE 5 TARGET ADDRESS
4195 011550 011554 JSRCKAD: JSRCK ;MODE 7 TARGET ADDRESS
4196 011552 000000 JSRSEQ: 0 ;SEQUENCE CHECKER
4197
4198 011554 022767 000006 177770 JSRCK: CMP 6,JSRSEQ ;CHECK SEQUENCE: JSRSEQ=6?
4199 011562 001003 BNE JSRCK1 ;BRANCH IF OUT OF SEQUENCE
4200 011564 022701 011546 CMP 2#JSR6AD,R1 ;PROPER PC SAVED?
4201 011570 001404 BEQ TST137
4202 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====
4203 ; CONDITIONAL BRANCH INST. AND <=====
4204 ; REPLACE THE MOVE INSTRUCTION <=====
4205 ; WHICH FOLLOWS W/ 561 <=====
4206 011572 JSRCK1:
4207 011572 012742 000252 MOV 252,-(R2) ;MOVE TO MAILBOX # ***** 252 *****
4208 011576 005242 INC -(R2) ;SET MSGTYP TO FATAL ERROR
4209 011600 000000 HALT ;JSR MODE 7 MALFUNCTIONED
4210 ; OR SEQUENCE ERROR
4211
4212
4213 ;*****
4214 ;

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4215 : THIS TEST VERIFIES THE RTS INSTRUCTION. THE STACK POINTER
4216 : IS INITIALIZED AND A TEST PATTERN STORED ON STACK. R0 IS LOADED
4217 : WITH RETURN ADDRESS. AN RTS IS EXECUTED, AND, AT THE TARGET
4218 : ADDRESS, A CHECK IS MADE THAT R0 WAS PROPERLY RESTORED FROM THE
4219 : STACK.
4220 : *****
4221 : TEST 137 TEST RTS INSTRUCTION
4222 : *****
4223 011602 005212 TST137: INC (R2) ;UPDATE TEST NUMBER
4224 011604 022712 000137 CMP #137,(R2) ;SEQUENCE ERROR?
4225 011610 001016 BNE TST140-10 ;BR TO ERROR HALT ON SEQ ERROR
4226 011612 012706 000500 MOV #STBOT,R6 ;INITIALIZE STACK POINTER
4227 011616 012746 052525 MOV #52525,-(R6) ;INITIALIZE TOP OF STACK
4228 011622 012700 011640 MOV #RTS1,R0 ;INITIALIZE RETURN REGISTER
4229 011626 000200 RTS R0 ;TRY RTS THROUGH R0
4230 : TO SCOPE: REPLACE THE MOVE INSTRUCTION <====
4231 : FOLLOWING W/ 770 <====
4232 011630 012742 000253 MOV #253,-(R2) ;MOVE TO MAILBOX # ***** 253 *****
4233 011634 005242 INC -(R2) ;SET MSGTYP TO FATAL ERROR
4234 011636 000000 HALT ;RTS FAILED
4235 011640 022700 052525 RTS1: CMP #52525,R0 ;CHECK THAT R0 RESTORED FROM STACK
4236 011644 001404 BEQ TST140
4237 : TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
4238 : CONDITIONAL BRANCH INST. AND <====
4239 : REPLACE THE MOVE INSTRUCTION <====
4240 : WHICH FOLLOWS W/ 762 <====
4241 011646 012742 000254 MOV #254,-(R2) ;MOVE TO MAILBOX # ***** 254 *****
4242 011652 005242 INC -(R2) ;SET MSGTYP TO FATAL ERROR
4243 011654 000000 HALT ;RTS MALFUNCTIONED
4244 : OR SEQUENCE ERROR
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4263 011656 005212
4264 011660 022712 000140
4265 011664 001022
4266 011666 000277
4267 011670 000251
4268 011672 012700 100000
4269 011676 101402
4270 011700 102401
4271 011702 100404
4272
4273
4274
4275
4276 011704
4277 011704 012742 000255
4278 011710 005242
4279 011712 000000
4280
4281 011714 000277
4282 011716 000244
4283 011720 012700 000000
4284 011724 101002
4285 011726 102401
4286 011730 100004
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4291 011732
4292 011732 012742 000256
4293 011736 005242
4294 011740 000000
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4300 011742 005212

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:*****
:
:   THESE NEXT FOUR TESTS VERIFY THE FUNCTIONING OF A GROUP
: OF FOUR INSTRUCTIONS.  THE GROUP CONSISTS OF THE INSTRUCTIONS:
: MOV, BIC, BIT, AND BIS.  THESE INSTRUCTIONS ARE SIMILAR IN THE
: WAY THEY EFFECT THE C AND V BITS.  THEY ALL LEAVE THE V-BIT
: CLEAR AND THE C-BIT UNAFFECTED.
:   THE TEST PROCEDURE IS AS FOLLOWS:  THE N, Z, AND V BITS
: ARE LOADED WITH THE COMPLEMENT OF THE EXPECTED RESULTS, THE C-BIT
: IS LOADED WITH THE DESIRED RESULT.  THE INSTRUCTION IS EXECUTED
: WITH DIFFERENT DATA PATTERNS AND THE RESULTS ARE VERIFIED WITH
: A SERIES OF CONDITIONAL BRANCH INSTRUCTIONS.  THE DATA IS CHOSEN
: TO PRODUCT ALL POSSIBLE COMBINATIONS OF THE C AND V BITS.
:*****
:TEST 140      TEST MOV INSTRUCTION
:*****
TST140: INC      (R2)          ;UPDATE TEST NUMBER
        CMP      #140,(R2)   ;SEQUENCE ERROR?
        BNE     TST141-10    ;BR TO ERROR HALT ON SEQ ERROR
        SCC
        +CLN!CLC           ;CC=0110
        MOV     #100000,RO    ;CC=1000
        BLOS   MOV1
        BVS    MOV1
        BMI    MOV2
:
:   TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
:              CONDITIONAL BRANCH INST. AND <====
:              REPLACE THE MOVE INSTRUCTION <====
:              WHICH FOLLOWS W/ 771 <====
:
MOV1:   MOV     #255,-(R2)    ;MOVE TO MAILBOX # ***** 255 *****
        INC     -(R2)
        HALT   ;SET MSGTYP TO FATAL ERROR
:              ;MOV DID NOT SET CC'S CORRECTLY
:
MOV2:   SCC
        CLZ
        MOV     #0,RO        ;CC=1011
        BHI    MOV3         ;CC=0101
        BVS    MOV3         ;C OR Z = 0?
        BPL    TST141       ;V=1?
:
:   TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
:              CONDITIONAL BRANCH INST. AND <====
:              REPLACE THE MOVE INSTRUCTION <====
:              WHICH FOLLOWS W/ 756 <====
:
MOV3:   MOV     #256,-(R2)    ;MOVE TO MAILBOX # ***** 256 *****
        INC     -(R2)
        HALT   ;SET MSGTYP TO FATAL ERROR
:              ;MOV DID NOT SET CC'S CORRECTLY
:              ;OR SEQUENCE ERROR
:*****
:TEST 141      TEST BIT INSTRUCTION
:*****
TST141: INC      (R2)          ;UPDATE TEST NUMBER

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4301 011744 022712 000141      CMP      #141,(R2)      ;SEQUENCE ERROR?
4302 011750 001024      BNE      TST142-10     ;BR TO ERROR HALT ON SEQ ERROR
4303 011752 012700 100001      MOV      #100001,R0
4304 011756 000277      SCC
4305 011760 000251      +CLN!CLC              ;CC=0110
4306 011762 032700 100000      BIT      #100000,R0    ;CC=1000
4307 011766 101402      BLOS    BIT1
4308 011770 102401      BVS     BIT1
4309 011772 100404      BMI     BIT2
4310
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4314 011774      BIT1:
4315 011774 012742 000257      MOV      #257,-(R2)    ;MOVE TO MAILBOX # ***** 257 *****
4316 012000 005242      INC      -(R2)         ;SET MSGTYP TO FATAL ERROR
4317 012002 000000      HALT
4318
4319 012004 000277      BIT2:  SCC              ;CC=1011
4320 012006 000244      CLZ
4321 012010 032700 077776      BIT      #77776,R0    ;CC=0101
4322 012014 101002      BHI     BIT3
4323 012016 102401      BVS     BIT3
4324 012020 100004      BPL     TST142
4325
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4328
4329 012022      BIT3:
4330 012022 012742 000260      MOV      #260,-(R2)    ;MOVE TO MAILBOX # ***** 260 *****
4331 012026 005242      INC      -(R2)         ;SET MSGTYP TO FATAL ERROR
4332 012030 000000      HALT
4333
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4335
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4338 012032 005212      ;*****
4339 012034 022712 000142      ;TEST 142      TEST BIC INSTRUCTION
4340 012040 001024      ;*****
4341 012042 012700 177777      †TST142: INC      (R2)      ;UPDATE TEST NUMBER
4342 012046 000277      CMP      #142,(R2)    ;SEQUENCE ERROR?
4343 012050 000251      BNE      TST143-10     ;BR TO ERROR HALT ON SEQ ERROR
4344 012052 042700 077777      MOV      #177777,R0
4345 012056 101402      SCC
4346 012060 102401      +CLN!CLC              ;CC=0110
4347 012062 100404      BIC      #77777,R0    ;CC=1000
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4352 012064      BIC1:
4353 012064 012742 000261      MOV      #261,-(R2)    ;MOVE TO MAILBOX # ***** 261 *****
4354 012070 005242      INC      -(R2)         ;SET MSGTYP TO FATAL ERROR
4355 012072 000000      HALT
4356 012074 000277      BIC2:  SCC              ;BIC DID NOT SET CC'S CORRECTLY
                                        ;CC=1011

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; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
; CONDITIONAL BRANCH INST. AND
; REPLACE THE MOVE INSTRUCTION
; WHICH FOLLOWS W/ 767
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; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
; CONDITIONAL BRANCH INST. AND
; REPLACE THE MOVE INSTRUCTION
; WHICH FOLLOWS W/ 754
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; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
; CONDITIONAL BRANCH INST. AND
; REPLACE THE MOVE INSTRUCTION
; WHICH FOLLOWS W/ 767
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012214 005212
012216 022712 000144
012222 001037
012224 012700 077777
012230 000257
012232 000264
012234 005200
012236 101402
012240 100001
012242 102404

012244
012244 012742 000265
012250 005242
012252 000000
012254 052700 077777
012260 000261
012262 000244
012264 005200
012266 100403
012270 102402
012272 103001
012274 001404

012276
012276 012742 000266
012302 005242
012304 000000

012306 000277
012310 000241
012312 005200
012314 101402
012316 100401
012320 100004

THESE NEXT TWO TESTS VERIFY THE FUNCTIONING OF THE INC AND
DEC INSTRUCTIONS. THESE INSTRUCTIONS BOTH EFFECT THE C AND V
BITS THE SAME; THE C-BIT IS LEFT UNCHANGED AND THE V-BIT IS DEPENDENT
UPON THE DATA RESULTS. THE SAME PROCEDURE IS USED. THE CONDITION
CODE BITS ARE INITIALIZED, THE INSTRUCTION IS EXECUTED AND THE
RESULTS ARE VERIFIED WITH A SERIES OF CONDITIONAL BRANCH INSTRUCTIONS.
THIS PROCEDURE IS REPEATED WITH SEVERAL DATA PATTERNS TO PRODUCE
DIFFERENT COMBINATIONS OF THE C AND V BITS.

TEST 144 TEST INC INSTRUCTION

TST144: INC (R2) ;UPDATE TEST NUMBER
CMP #144,(R2) ;SEQUENCE ERROR?
BNE TST145-10 ;BR TO ERROR HALT ON SEQ ERROR
MOV #077777,R0 ;RO=077777
CCC ;CC=0100
SEZ
INC R0 ;CC=1010 RO=10000
BLOS INC1
BPL INC1
BVS INC2

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
CONDITIONAL BRANCH INST. AND <====
REPLACE THE MOVE INSTRUCTION <====
WHICH FOLLOWS W/ 770 <====

INC1: MOV #265,-(R2) ;MOVE TO MAILBOX # ***** 265 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;INC DID NOT SET CC'S CORRECTLY
INC2: BIS #77777,R0 ;RO=177777
SEC ;CC=1011
CLZ
INC R0 ;CC=0101 RO=0
BMI INC3
BVS INC3
BCC INC3
BEQ INC4

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
CONDITIONAL BRANCH INST. AND <====
REPLACE THE MOVE INSTRUCTION <====
WHICH FOLLOWS W/ 753 <====

INC3: MOV #266,-(R2) ;MOVE TO MAILBOX # ***** 266 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;INC DID NOT SET CC'S CORRECTLY
INC4: SCC ;CC=1110
CLC
INC R0 ;CC=0000 RO=1
BLOS INC5
BMI INC5
BPL TST145

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4471 012322
4472 012322 012742 000267
4473 012326 005242
4474 012330 000000
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4480 012332 005212
4481 012334 022712 000145
4482 012340 001051
4483 012342 012700 000002
4484 012346 000277
4485 012350 005300
4486 012352 100403
4487 012354 001402
4488 012356 102401
4489 012360 103404
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4494 012362
4495 012362 012742 000270
4496 012366 005242
4497 012370 000000
4498 012372 000261
4499 012374 000244
4500 012376 005300
4501 012400 101002
4502 012402 100401
4503 012404 102004
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4508 012406
4509 012406 012742 000271
4510 012412 005242
4511 012414 000000
4512 012416 000277
4513 012420 000251
4514 012422 005300
4515 012424 101402
4516 012426 102401
4517 012430 100404
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4522 012432

```

INC5: MOV #267, -(R2) ; MOVE TO MAILBOX # ***** 267 *****
INC INC -(R2) ; SET MSGTYP TO FATAL ERROR
HALT ; INC DID NOT SET CC'S CORRECTLY
; OR SEQUENCE ERROR

;*****
;TEST 145 TEST DEC INSTRUCTION
;*****
†ST145: INC (R2) ; UPDATE TEST NUMBER
CMP #145, (R2) ; SEQUENCE ERROR?
BNE TST146-10 ; BR TO ERROR HALT ON SEQ ERROR
MOV #2, R0 ; R0=2
SCC ; CC=1111
DEC R0 ; CC=0001 R0=1
BMI DEC1
BEQ DEC1
BVS DEC1
BCS DEC2

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 741 <====

DEC1: MOV #270, -(R2) ; MOVE TO MAILBOX # ***** 270 *****
INC INC -(R2) ; SET MSGTYP TO FATAL ERROR
HALT ; DEC DID NOT SET CC'S CORRECTLY
DEC2: SEC ; CC=1011
CLZ ; CC=0101 R0=0
DEC R0
BHI DEC3
BMI DEC3
BVC DEC4

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 770 <====

DEC3: MOV #271, -(R2) ; MOVE TO MAILBOX # ***** 271 *****
INC INC -(R2) ; SET MSGTYP TO FATAL ERROR
HALT ; DEC DID NOT SET CC'S CORRECTLY
DEC4: SCC ; CC=0110
+CLN!CLC ; CC=1000 R0=17777
DEC R0
BLOS DEC5
BVS DEC5
BMI DEC6

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 744 <====

DEC5:

4523	012432	012742	000272		MOV	#272, -(R2)	; MOVE TO MAILBOX # ***** 272 *****	
4524	012436	005242			INC	-(R2)	; SET MSGTYP TO FATAL ERROR	
4525	012440	000000			HALT		; DEC DID NOT SET CC'S CORRECTLY	
4526	012442	042700	077777	DEC6:	BIC	#77777, R0	; R0=100000	
4527	012446	000277			SCC		; CC=0101	
4528	012450	000252			+CLN!CLV			
4529	012452	005300			DEC	R0	; CC=1011 R0=77777	
4530	012454	100403			BMI	DEC7	; CC=0011	
4531	012456	001402			BEQ	DEC7		
4532	012460	102001			BVC	DEC7		
4533	012462	103404			BOS	TST146		
4534							; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS	<====
4535							; CONDITIONAL BRANCH INST. AND	<====
4536							; REPLACE THE MOVE INSTRUCTION	<====
4537							; WHICH FOLLOWS W/ 727	<====
4538	012464			DEC7:				
4539	012464	012742	000273		MOV	#273, -(R2)	; MOVE TO MAILBOX # ***** 273 *****	
4540	012470	005242			INC	-(R2)	; SET MSGTYP TO FATAL ERROR	
4541	012472	000000			HALT		; DEC DID NOT SET CC'S CORRECTLY	
4542							; OR SEQUENCE ERROR	
4543								

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4557 012474 005212
4558 012476 022712 000146
4559 012502 001007
4560 012504 000277
4561 012506 000244
4562 012510 005000
4563 012512 100403
4564 012514 102402
4565 012516 103401
4566 012520 001404
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4571 012522
4572 012522 012742 000274
4573 012526 005242
4574 012530 000000
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4580 012532 005212
4581 012534 022712 000147
4582 012540 001022
4583 012542 000277
4584 012544 000244
4585 012546 005700
4586 012550 100403
4587 012552 102402
4588 012554 103401
4589 012556 001404
4590
4591
4592
4593
4594 012560
4595 012560 012742 000275
4596 012564 005242
4597 012566 000000
4598 012570 005300
4599 012572 000277

```

```

THESE NEXT THREE TESTS VERIFY THE FUNCTIONING OF THE CLR,
TST, AND SWAB INSTRUCTIONS. THESE THREE INSTRUCTIONS ALL LEAVE
THE C AND V BITS CLEARED. AGAIN, THE CONDITION CODES ARE PRESET,
THE INSTRUCTION EXECUTED AND THE RESULTS CHECKED WITH CONDITIONAL
BRANCH INSTRUCTIONS. THE PROCEDURE IS REPEATED TO PRODUCE OTHER
COMBINATIONS OF CONDITION CODES.

```

TEST 146 TEST CLR INSTRUCTION

```

TST146: INC (R2) ;UPDATE TEST NUMBER
        CMP #146,(R2) ;SEQUENCE ERROR?
        BNE TST147-10 ;BR TO ERROR HALT ON SEQ ERROR
        SCC ;CC=1011
        CLZ
        CLR RO ;CC=0100 RO=0
        BMI CLR1
        BVS CLR1
        BCS CLR1
        BEQ TST147

```

```

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 771 <====

```

```

CLR1: MOV #274,-(R2) ;MOVE TO MAILBOX # ***** 274 *****
      INC -(R2) ;SET MSGTYP TO FATAL ERROR
      HALT ;CLR DID NOT SET CC'S CORRECTLY
          ; OR SEQUENCE ERROR

```

TEST 147 TEST TST INSTRUCTION

```

TST147: INC (R2) ;UPDATE TEST NUMBER
        CMP #147,(R2) ;SEQUENCE ERROR?
        BNE TST150-10 ;BR TO ERROR HALT ON SEQ ERROR
        SCC ;CC=1011
        CLZ
        TST RO ;CC=0100
        BMI TEST1
        BVS TEST1
        BCS TEST1
        BEQ TEST2

```

```

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 771 <====

```

```

TEST1: MOV #275,-(R2) ;MOVE TO MAILBOX # ***** 275 *****
      INC -(R2) ;SET MSGTYP TO FATAL ERROR
      HALT ;TEST DID NOT SET CC'S CORRECTLY
TEST2: DEC RO ;MAKE RO NEGATIVE
      SCC ;CC=0111

```

```

4600 012574 000250          CLN
4601 012576 005700          TST          RO          ;CC=1000
4602 012600 101402          BLOS        TEST3
4603 012602 102401          BVS        TEST3
4604 012604 100404          BMI        TST150
4605                                     ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
4606                                     ;          CONDITIONAL BRANCH INST. AND <====
4607                                     ;          REPLACE THE MOVE INSTRUCTION <====
4608                                     ;          WHICH FOLLOWS W/ 756 <====
4609 012606          TEST3:
4610 012606 012742 000276      MOV        #276, -(R2)    ;MOVE TO MAILBOX # ***** 276 *****
4611 012612 005242          INC        -(R2)        ;SET MSGTYP TO FATAL ERROR
4612 012614 000000          HALT          ;TEST DID NOT SET CC'S CORRECTLY
4613                                     ;          OR SEQUENCE ERROR
4614
4615 ;*****
4616 ;TEST 150          TEST SWAB INSTRUCTION
4617 ;*****
4618 012616 005212          TST150: INC        (R2)          ;UPDATE TEST NUMBER
4619 012620 022712 000150      CMP        #150, (R2)    ;SEQUENCE ERROR?
4620 012624 001023          BNE        TST151-10    ;BR TO ERROR HALT ON SEQ ERROR
4621 012626 012700 170000      MOV        #170000, RO  ;RO=170000
4622 012632 000277          SCC          ;CC=0111
4623 012634 000250          CLN
4624 012636 000300          SWAB       RO          ;CC=1000  RO=360
4625 012640 101402          BLOS       SWB1
4626 012642 102401          BVS       SWB1
4627 012644 100404          BMI       SWB2
4628                                     ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
4629                                     ;          CONDITIONAL BRANCH INST. AND <====
4630                                     ;          REPLACE THE MOVE INSTRUCTION <====
4631                                     ;          WHICH FOLLOWS W/ 77C <====
4632 012646          SWB1:
4633 012646 012742 000277      MOV        #277, -(R2)    ;MOVE TO MAILBOX # ***** 277 *****
4634 012652 005242          INC        -(R2)        ;SET MSGTYP TO FATAL ERROR
4635 012654 000000          HALT          ;SWAB DID NOT SET CC'S CORRECTLY
4636 012656 000277          SWB2: SCC          ;CC=1011
4637 012660 000244          CLZ
4638 012662 000300          SWAB       RO          ;CC=0100  RO=170000
4639 012664 102403          BVS       SWB3
4640 012666 103402          BCS       SWB3
4641 012670 100401          BMI       SWB3
4642 012672 001404          BEQ       TST151
4643                                     ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
4644                                     ;          CONDITIONAL BRANCH INST. AND <====
4645                                     ;          REPLACE THE MOVE INSTRUCTION <====
4646                                     ;          WHICH FOLLOWS W/ 755 <====
4647 012674          SWB3:
4648 012674 012742 000300      MOV        #300, -(R2)    ;MOVE TO MAILBOX # ***** 300 *****
4649 012700 005242          INC        -(R2)        ;SET MSGTYP TO FATAL ERROR
4650 012702 000000          HALT
4651

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4666 012704 005212
4667 012706 022712 000151
4668 012712 001062
4669 012714 012700 040000
4670 012720 000277
4671 012722 062700 030000
4672 012726 101402
4673 012730 102401
4674 012732 100004
4675
4676
4677
4678
4679 012734
4680 012734 012742 000301
4681 012740 005242
4682 012742 000000
4683 012744 000264
4684
4685 012746 062700 010000
4686 012752 101402
4687 012754 102001
4688 012756 100404
4689
4690
4691
4692
4693 012760
4694 012760 012742 000302
4695 012764 005242
4696 012766 000000
4697 012770 000257
4698 012772 000270
4699 012774 062700 100000
4700 013000 101002
4701 013002 102001
4702 013004 100004
4703
4704
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4707 013006

THESE NEXT TWO TESTS VERIFY THE FUNCTIONING OF THE ADD AND
ADC INSTRUCTIONS. BOTH OF THESE INSTRUCTIONS HANDLE THE C AND
V BITS IDENTICALLY. THE PROCEDURE IS TO PRESET THE CONDITION
CODES, EXECUTE THE INSTRUCTION WITH A PARTICULAR SET OF DATA, AND
THEN CHECK THE RESULTS BY EXECUTING A SERIES OF CONDITIONAL
BRANCHES. THIS PROCEDURE IS REPEATED SEVERAL TIMES WITH DIFFERENT
DATA TO PRODUCE EVERY COMBINATION OF C AND V BITS.

TEST 151 TEST ADD INSTRUCTION

TST151: INC (R2) ;UPDATE TEST NUMBER
CMP #151,(R2) ;SEQUENCE ERROR?
BNE TST152-10 ;BR TO ERROR HALT ON SEQ ERROR
MOV #40000,R0 ;RO=40000
SCC ;CC=1111
ADD #30000,R0 ;CC=0000 RO=70000
BLOS ADD1
BVS ADD1
BPL ADD2

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 770 <====

ADD1: MOV #301,-(R2) ;MOVE TO MAILBOX # ***** 301 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;ADD DID NOT SET CC'S CORRECTLY
ADD2: SEZ ;CC=0100

ADD #10000,R0 ;CC=1010 40=100000
BLOS ADD3
BVC ADD3
BMI ADD4

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 756 <====

ADD3: MOV #302,-(R2) ;MOVE TO MAILBOX # ***** 302 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;ADD DID NOT SET CC'S CORRECTLY
ADD4: CCC ;CC=1000
SEN

ADD #100000,R0 ;CC=0111 RO=0
BHI ADD5
BVC ADD5
BPL ADD6

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 743 <====

ADD5:

```

4708 013006 012742 000303      MOV      #303,-(R2)      ;MOVE TO MAILBOX # ***** 303 *****
4709 013012 005242              INC      -(R2)          ;SET MSGTYP TO FATAL ERROR
4710 013014 000000              HALT                    ;ADD DID NOT SET CC'S CORRECTLY
4711 013016 062700 177777      ADD6:   ADD      #177777,R0 ;CC=1000  RO=177777
4712 013022 101402              BLOS    ADD7
4713 013024 102401              BVS     ADD7
4714 013026 100404              BMI     ADD8
4715                                ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
4716                                ;                                     <====
4717                                ;                                     <====
4718                                ;                                     <====
4719 013030                                ADD7:
4720 013030 012742 000304      MOV      #304,-(R2)      ;MOVE TO MAILBOX # ***** 304 *****
4721 013034 005242              INC      -(R2)          ;SET MSGTYP TO FATAL ERROR
4722 013036 000000              HALT                    ;ADD DID NOT SET CC'S CORRECTLY
4723 013040 000277      ADD8:   SCC
4724 013042 000245              +CLC!CLZ                ;CC=1010
4725 013044 062700 000001      ADD      #1,R0          ;CC=0101  R=0
4726 013050 102403              BVS     ADD9
4727 013052 103002              BCC     ADD9
4728 013054 100401              BMI     ADD9
4729 013056 001404              BEQ     TST152
4730                                ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
4731                                ;                                     <====
4732                                ;                                     <====
4733                                ;                                     <====
4734 013060                                ADD9:
4735 013060 012742 000305      MOV      #305,-(R2)      ;MOVE TO MAILBOX # ***** 305 *****
4736 013064 005242              INC      -(R2)          ;SET MSGTYP TO FATAL ERROR
4737 013066 000000              HALT                    ;ADD DID NOT SET CC'S CORRECTLY
4738                                ; OR SEQUENCE ERROR
4739
4740 ;*****
4741 ;TEST 152 TEST ADC INSTRUCTION
4742 ;*****
4743 013070 005212      TST152: INC      (R2)          ;UPDATE TEST NUMBER
4744 013072 022712 000152      CMP      #152,(R2)      ;SEQUENCE ERROR?
4745 013076 001037              BNE     TST153-10      ;BR TO ERROR HALT ON SEQ ERROR
4746 013100 012700 077777      MOV      #077777,R0
4747 013104 000277              SCC
4748 013106 000252              +CLN!CLV                ;CC=0101
4749 013110 005500              ADC      R0              ;CC=1010
4750 013112 101402              BLOS    ADC1
4751 013114 102001              BVC     ADC1
4752 013116 100404              BMI     ADC2
4753                                ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
4754                                ;                                     <====
4755                                ;                                     <====
4756                                ;                                     <====
4757 013120                                ADC1:
4758 013120 012742 000306      MOV      #306,-(R2)      ;MOVE TO MAILBOX # ***** 306 *****
4759 013124 005242              INC      -(R2)          ;SET MSGTYP TO FATAL ERROR
4760 013126 000000              HALT                    ;ADC DID NOT SET CC'S CORRECTLY
4761 013130 052700 077777      ADC2:   BIS      #77777,R0
4762 013134 000277              SCC
4763 013136 000244              CLZ

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4764 013140 005500          ADC      RO          ;CC=0101  RO=0
4765 013142 101002          BHI      ADC3
4766 013144 102401          BVS      ADC3
4767 013146 100004          BPL      ADC4
4768
4769
4770
4771
4772 013150          ADC3:
4773 013150 012742 000307          MOV      #307,-(R2)
4774 013154 005242          INC      -(R2)
4775 013156 000000          HALT
4776 013160 000277          ADC4:  SCC
4777 013162 000245          +CLZ!CLC
4778 013164 005500          ADC      RO          ;CC=0100 ;CC=1010
4779 013166 102403          BVS      ADC5
4780 013170 103402          BCS      ADC5
4781 013172 100401          BMI      ADC5
4782 013174 001404          BEQ      TST153
4783
4784
4785
4786
4787 013176          ADC5:
4788 013176 012742 000310          MOV      #310,-(R2)
4789 013202 005242          INC      -(R2)
4790 013204 000000          HALT
4791

```

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 754 <====

; MOVE TO MAILBOX # ***** 307 *****
; SET MSGTYP TO FATAL ERROR
; ADC DID NOT SET CC'S CORRECTLY

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 741 <====

; MOVE TO MAILBOX # ***** 310 *****
; SET MSGTYP TO FATAL ERROR
; ADC DID NOT SET CC'S CORRECTLY
; OR SEQUENCE ERROR

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4792
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4800
4801
4802
4803
4804
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4806 013206 005212
4807 013210 022712 000153
4808 013214 001042
4809 013216 012700 000001
4810 013222 000277
4811 013224 000251
4812 013226 005400
4813 013230 103003
4814 013232 102402
4815 013234 001401
4816 013236 100404
4817
4818
4819
4820
4821 013240
4822 013240 012742 000311
4823 013244 005242
4824 013246 000000
4825 013250 042700 077777
4826 013254 000257
4827 013256 000264
4828 013260 005400
4829 013262 102003
4830 013264 103002
4831 013266 001401
4832 013270 100404
4833
4834
4835
4836
4837 013272
4838 013272 012742 000312
4839 013276 005242
4840 013300 000000
4841 013302 005000
4842 013304 000277
4843 013306 000244
4844 013310 005400
4845 013312 102403
4846 013314 103402
4847 013316 001001

```

```

*****
: THESE NEXT THREE TESTS VERIFY THE FUNCTIONING OF THE NEG,
: CMP, AND COM INSTRUCTIONS. EACH OF THESE INSTRUCTIONS GENERATE
: THE C AND V BITS IDENTICALLY. THE CONDITION CODES ARE PRESET,
: THE INSTRUCTIONS EXECUTED, AND THE RESULTS CHECKED WITH A SERIES
: OF CONDITIONAL BRANCH INSTRUCTIONS. THIS PROCEDURE IS REPEATED
: SEVERAL TIMES WITH DIFFERENT DATA IN ORDER TO GENERATE DIFFERENT
: COMBINATIONS OF THE C AND V BITS.
*****

```

```

*****
: TEST 153 TEST NEG INSTRUCTION
*****

```

```

↑ST153: INC (R2) ;UPDATE TEST NUMBER
: CMP #153,(R2) ;SEQUENCE ERROR?
: BNE TST154-10 ;BR TO ERROR HALT ON SEQ ERROR
: MOV #1,R0
: SCC ;CC=0110
: +CLN!CLC
: NEG R0 ;CC=1001 RO=177777
: BCC NEG1
: BVS NEG1
: BEQ NEG1
: BMI NEG2

```

```

: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
: CONDITIONAL BRANCH INST. AND <====
: REPLACE THE MOVE INSTRUCTION <====
: WHICH FOLLOWS W/ 767 <====

```

```

NEG1: MOV #311,-(R2) ;MOVE TO MAILBOX # ***** 311 *****
: INC -(R2) ;SET MSGTYP TO FATAL ERROR
: HALT ;NEG DID NOT SET CC'S CORRECTLY

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NEG2: BIC #77777,R0
: CCC ;CC=0100
: SEZ
: NEG R0 ;CC=1011 RO=100000
: BVC NEG3
: BCC NEG3
: BEQ NEG3
: BMI NEG4

```

```

: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
: CONDITIONAL BRANCH INST. AND <====
: REPLACE THE MOVE INSTRUCTION <====
: WHICH FOLLOWS W/ 752 <====

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NEG3: MOV #312,-(R2) ;MOVE TO MAILBOX # ***** 312 *****
: INC -(R2) ;SET MSGTYP TO FATAL ERROR
: HALT ;NEG DID NOT SET CC'S CORRECTLY

```

```

NEG4: CLR R0
: SCC ;CC=1011
: CLZ
: NEG R0 ;CC=0100 RO=0
: BVS NEG5
: BCS NEG5
: BNE NEG5

```

```

4848 013320 100004          BPL      TST154
4849
4850
4851
4852
4853 013322          NEGS:
4854 013322 012742 000313      MOV      #313, -(R2)
4855 013326 005242          INC      -(R2)
4856 013330 000000          HALT
4857
4858
4859
4860
4861
4862 013332 005212          ST154: INC      (R2)
4863 013334 022712 000154      CMP      #154, (R2)
4864 013340 001060          BNE     TST155-10
4865 013342 012700 000005      MOV      #5, R0
4866 013346 000257          CCC
4867 013350 000271          +SEN!SEC
4868 013352 022700 000005      CMP      #5, R0
4869 013356 101002          BHI     CMP1
4870 013360 102401          BVS     CMP1
4871 013362 100004          BPL     CMP2
4872
4873
4874
4875
4876 013364          CMP1:
4877 013364 012742 000314      MOV      #314, -(R2)
4878 013370 005242          INC      -(R2)
4879 013372 000000          HALT
4880 013374 012700 100000      CMP2: MOV      #100000, R0
4881 013400 000277          SCC
4882 013402 000242          CLV
4883 013404 020027 077777      CMP      R0, #77777
4884 013410 101402          BLOS   CMP3
4885 013412 102001          BVC     CMP3
4886 013414 100004          BPL     CMP4
4887
4888
4889
4890
4891 013416          CMP3:
4892 013416 012742 000315      MOV      #315, -(R2)
4893 013422 005242          INC      -(R2)
4894 013424 000000          HALT
4895 013426 052700 040000      CMP4: BIS      #40000, R0
4896 013432 000257          CCC
4897 013434 000264          SEZ
4898 013436 022700 040000      CMP      #40000, R0
4899 013442 102003          BVC     CMP5
4900 013444 103002          BCC     CMP5
4901 013446 001401          BEQ     CMP5
4902 013450 100404          BMI     CMP6
4903

```

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
 ; CONDITIONAL BRANCH INST. AND <====
 ; REPLACE THE MOVE INSTRUCTION <====
 ; WHICH FOLLOWS W/ 736 <====
 ; MOVE TO MAILBOX # ***** 313 *****
 ; SET MSGTYP TO FATAL ERROR
 ; NEG DID NOT SET CC'S CORRECTLY
 ; OR SEQUENCE ERROR
 ;*****
 ;TEST 154 TEST CMP INSTRUCTION
 ;*****
 ; UPDATE TEST NUMBER
 ; SEQUENCE ERROR?
 ; BR TO ERROR HALT ON SEQ ERROR
 ; CC=1010
 ; CC=0101
 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
 ; CONDITIONAL BRANCH INST. AND <====
 ; REPLACE THE MOVE INSTRUCTION <====
 ; WHICH FOLLOWS W/ 767 <====
 ; MOVE TO MAILBOX # ***** 314 *****
 ; SET MSGTYP TO FATAL ERROR
 ; CMP DID NOT SET CC'S CORRECTLY
 ; CC=1101
 ; CC=0010
 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
 ; CONDITIONAL BRANCH INST. AND <====
 ; REPLACE THE MOVE INSTRUCTION <====
 ; WHICH FOLLOWS W/ 752 <====
 ; MOVE TO MAILBOX # ***** 315 *****
 ; SET MSGTYP TO FATAL ERROR
 ; CMP DID NOT SET CC'S CORRECTLY
 ; R0=140000
 ; CC=0100
 ; CC=1011
 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====


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4964 013552 005212
4965 013554 022712 000156
4966 013560 001055
4967 013562 012700 125252
4968 013566 000257
4969 013570 000271
4970 013572 162700 125252
4971 013576 101002
4972 013600 102401
4973 013602 100004
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4978 013604
4979 013604 012742 000321
4980 013610 005242
4981 013612 000000
4982 013614 052700 100000
4983 013620 000277
4984 013622 000242
4985 013624 162700 077777
4986 013630 101402
4987 013632 102001
4988 013634 100004
4989
4990
4991
4992
4993 013636
4994 013636 012742 000322
4995 013642 005242
4996 013644 000000
4997 013646 005100
4998 013650 000277
4999
5000 013652 162700 100000
5001 013656 101402
5002 013660 102401
5003 013662 100004
5004
5005

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*****
: THESE NEXT TWO TESTS VERIFY THE FUNCTIONING OF THE SUB
: AND SBC INSTRUCTIONS. BOTH OF THESE INSTRUCTIONS HANDLE THE
: C AND V BITS IDENTICALLY. THE PROCEDURE IS TO PRESET THE CONDITION
: CODES, EXECUTE THE INSTRUCTION WITH A PARTICULAR SET OF DATA, AND
: THEN CHECK THE RESULTS BY EXECUTING A SERIES OF CONDITIONAL
: BRANCHES. THIS PROCEDURE IS REPEATED SEVERAL TIMES WITH DIFFERENT
: DATA PATTERNS TO PROVIDE EVERY COMBINATION OF THE C AND V BITS.
*****
: TEST 156 TEST SUB INSTRUCTION
*****
TST156: INC (R2) ;UPDATE TEST NUMBER
: CMP #156,(R2) ;SEQUENCE ERROR?
: BNE TST157-10 ;BR TO ERROR HALT ON SEQ ERROR
: MOV #125252,R0
: CCC ;CC=1010
: +SEN!SEC
: SUB #125252,R0 ;CC=0101 R0=0
: BHI SUB1
: BVS SUB1
: BPL SUB2
: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
: CONDITIONAL BRANCH INST. AND <====
: REPLACE THE MOVE INSTRUCTION <====
: WHICH FOLLOWS W/ 767 <====
SUB1: MOV #321,-(R2) ;MOVE TO MAILBOX # ***** 321 *****
: INC -(R2) ;SET MSGTYP TO FATAL ERROR
: HALT ;SUB DID NOT SET CC'S CORRECTLY
SUB2: BIS #100000,R0
: SCC ;CC=1101
: CLV
: SUB #77777,R0 ;CC=0010 R0=1
: BLOS SUB3
: BVC SUB3
: BPL SUB4
: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
: CONDITIONAL BRANCH INST. AND <====
: REPLACE THE MOVE INSTRUCTION <====
: WHICH FOLLOWS W/ 752 <====
SUB3: MOV #322,-(R2) ;MOVE TO MAILBOX # ***** 322 *****
: INC -(R2) ;SET MSGTYP TO FATAL ERROR
: HALT
SUB4: COM R0 ;R0=177777
: SCC ;CC=11111
: SUB #100000,R0 ;CC=0000 R0=77777
: BLOS SUB5
: BVS SUB5
: BPL SUB6
: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
: CONDITIONAL BRANCH INST. AND <====

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5006                                     ;                                     <====
5007                                     ;                                     <====
5008 013664                               SUB5:                               ;
5009 013664 012742 000323                MOV      #323, -(R2)                ; MOVE TO MAILBOX # ***** 323 *****
5010 013670 005242                        INC      -(R2)                    ; SET MSGTYP TO FATAL ERROR
5011 013672 000000                        HALT                                     ; SUB DID NOT SET CC'S CORRECTLY
5012 013674 000257                               SUB6:                               ; CC=0100
5013 013676 000264                               SEZ                                     ;
5014 013700 162700 140000                SUB      #140000, R0                ; CC=1011
5015 013704 102003                               BVC      SUB7
5016 013706 103002                               BCC      SUB7
5017 013710 001401                               BEQ      SUB7
5018 013712 100404                               BMI      TST157
5019                                     ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
5020                                     ; CONDITIONAL BRANCH INST. AND <====
5021                                     ; REPLACE THE MOVE INSTRUCTION <====
5022                                     ; WHICH FOLLOWS W/ 737 <====
5023 013714                               SUB7:                               ;
5024 013714 012742 000324                MOV      #324, -(R2)                ; MOVE TO MAILBOX # ***** 324 *****
5025 013720 005242                        INC      -(R2)                    ; SET MSGTYP TO FATAL ERROR
5026 013722 000000                        HALT                                     ;
5027
5028 ;*****
5029 ;TEST 157 TEST SBC INSTRUCTION
5030 ;*****
5031 013724 005212                               †TST157: INC      (R2)                ; UPDATE TEST NUMBER
5032 013726 022712 000157                CMP      #157, (R2)                ; SEQUENCE ERROR?
5033 013732 001053                        BNE      TST160-10                ; BR TO ERROR HALT ON SEQ ERROR
5034 013734 012700 000001                MOV      #1, R0
5035 013740 000277                               SCC                                     ; CC=1011
5036 013742 000244                               CLZ
5037 013744 005600                               SBC      R0                        ; CC=0100 R=0
5038 013746 103403                               BCS      SBC1
5039 013750 102402                               BVS      SBC1
5040 013752 100401                               BMI      SBC1
5041 013754 001404                               BEQ      SBC2
5042                                     ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
5043                                     ; CONDITIONAL BRANCH INST. AND <====
5044                                     ; REPLACE THE MOVE INSTRUCTION <====
5045                                     ; WHICH FOLLOWS W/ 767 <====
5046 013756                               SBC1:                               ;
5047 013756 012742 000325                MOV      #325, -(R2)                ; MOVE TO MAILBOX # ***** 325 *****
5048 013762 005242                        INC      -(R2)                    ; SET MSGTYP TO FATAL ERROR
5049 013764 000000                        HALT                                     ; SBC DID NOT SET CC'S CORRECTLY
5050 013766 000277                               SBC2:                               ; CC=1010
5051 013770 000245                               +CLZ!CLC
5052 013772 005600                               SBC      R0                        ; CC=0100 R=0
5053 013774 103403                               BCS      SBC3
5054 013776 102402                               BVS      SBC3
5055 014000 100401                               BMI      SBC3
5056 014002 001404                               BEQ      SBC4
5057                                     ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
5058                                     ; CONDITIONAL BRANCH INST. AND <====
5059                                     ; REPLACE THE MOVE INSTRUCTION <====
5060                                     ; WHICH FOLLOWS W/ 754 <====
5061 014004                               SBC3:

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5062	014004	012742	000326		MOV	#326, -(R2)	; MOVE TO MAILBOX # ***** 326 *****	
5063	014010	005242			INC	-(R2)	; SET MSGTYP TO FATAL ERROR	
5064	014012	000000			HALT		; SBC DID NOT SET CC'S CORRECTLY	
5065	014014	000277		SBC4:	SCC		; CC=0111	
5066	014016	000250			CLN			
5067	014020	005600			SBC	RO	; CC=1001 RO=177777	
5068	014022	103003			BCC	SBC5		
5069	014024	102402			BVS	SBC5		
5070	014026	001401			BEQ	SBC5		
5071	014030	100404			BMI	SBC6		
5072							; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS	<====
5073							; CONDITIONAL BRANCH INST. AND	<====
5074							; REPLACE THE MOVE INSTRUCTION	<====
5075							; WHICH FOLLOWS W/ 741	<====
5076	014032			SBC5:				
5077	014032	012742	000327		MOV	#327, -(R2)	; MOVE TO MAILBOX # ***** 327 *****	
5078	014036	005242			INC	-(R2)	; SET MSGTYP TO FATAL ERROR	
5079	014040	000000			HALT		; SBC DID NOT SET CC'S CORRECTLY	
5080	014042	042700	077777	SBC6:	BIC	#77777, RO	; RO=100000	
5081	014046	000277			SCC		; CC=1101	
5082	014050	000242			CLV			
5083	014052	005600			SBC	RO	; CC=0010	
5084	014054	101402			BLOS	SBC7		
5085	014056	102001			BVC	SBC7		
5086	014060	100004			BPL	TST160		
5087							; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS	<====
5088							; CONDITIONAL BRANCH INST. AND	<====
5089							; REPLACE THE MOVE INSTRUCTION	<====
5090							; WHICH FOLLOWS W/ 725	<====
5091	014062			SBC7:				
5092	014062	012742	000330		MOV	#330, -(R2)	; MOVE TO MAILBOX # ***** 330 *****	
5093	014066	005242			INC	-(R2)	; SET MSGTYP TO FATAL ERROR	
5094	014070	000000			HALT		; SBC DID NOT SET CC'S CORRECTLY	
5095							; OR SEQUENCE ERROR	
5096								

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014072 005212
014074 022712 000160
014100 001053
014102 012700 144000
014106 000257
014110 000266
014112 006100
014114 103003
014116 102402
014120 001401
014122 100404

014124
014124 012742 000331
014130 005242
014132 000000
014134 000277
014136 000243
014140 006100
014142 103003
014144 102002
014146 001401
014150 100004

014152
014152 012742 000332
014156 005242
014160 000000
014162 000277
014164 000250
014166 006100
014170 101402
014172 102401
014174 100004

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*****
:
: THESE NEXT FOUR TESTS VERIFY THE FUNCTIONING OF THE ROL,
: ROR, ASL AND ASR INSTRUCTIONS. SPECIAL DATA PATTERNS ARE LOADED
: AND ROTATED SEVERAL TIMES FOR EACH TEST. THE CONDITION CODES
: ARE PRESET BEFORE EACH ROTATION AND THE CONDITION CODES ARE
: CHECKED AFTER EACH ROTATION. THE FINAL CHECK IN EACH TEST IS
: TO VERIFY THE COMMULATIVE DATA RESULT. THE DATA PATTERNS HAVE
: BEEN SELECTED TO PRODUCE ALL COMBINATIONS OF THE C AND V BITS.
:
: *****
: TEST 160 TEST ROL INSTRUCTION
: *****
: ST160: INC (R2) ; UPDATE TEST NUMBER
: CMP #160, (R2) ; SEQUENCE ERROR?
: BNE TST161-10 ; BR TO ERROR HALT ON SEQ ERROR
: MOV #144000, R0 ; RO=144000
: CCC ; CC=0110
: +SEZ!SEV
: ROL R0 ; CC=1001 RO=110000
: BCC ROL1
: BVS ROL1
: BEQ ROL1
: BMI ROL2
:
: ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
: ; CONDITIONAL BRANCH INST. AND <====
: ; REPLACE THE MOVE INSTRUCTION <====
: ; WHICH FOLLOWS W/ 767 <====
:
: ROL1: MOV #331, -(R2) ; MOVE TO MAILBOX # ***** 331 *****
: INC -(R2) ; SET MSGTYP TO FATAL ERROR
: HALT
: ROL2: SCC ; CC=1100
: +CLV!CLC
: ROL R0 ; CC=0011 RO=020000
: BCC ROL3
: BVC ROL3
: BEQ ROL3
: BPL ROL4
:
: ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
: ; CONDITIONAL BRANCH INST. AND <====
: ; REPLACE THE MOVE INSTRUCTION <====
: ; WHICH FOLLOWS W/ 754 <====
:
: ROL3: MOV #332, -(R2) ; MOVE TO MAILBOX # ***** 332 *****
: INC -(R2) ; SET MSGTYP TO FATAL ERROR
: HALT ; ROL DID NOT SET CC'S CORRECTLY
: ROL4: SCC ; CC=0111
: CLN
: ROL R0 ; CC=0000 RO=040001
: BLOS ROL5
: BVS ROL5
: BPL ROL6
:
: ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
: ; CONDITIONAL BRANCH INST. AND <====
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5153                                     ; REPLACE THE MOVE INSTRUCTION <====
5154                                     ; WHICH FOLLOWS W/ 742 <====
5155 014176                                ROL5:
5156 014176 012742 000333                MOV #333, -(R2) ; MOVE TO MAILBOX # ***** 333 *****
5157 014202 005242                        INC -(R2) ; SET MSGTYP TO FATAL ERROR
5158 014204 000000                        HALT ; ROL DID NOT SET CC'S CORRECTLY
5159 014206 000257                                ROL6: ; CC=0101
5160 014210 000265                        CCC
5161 014212 006100                        +SEZ!SEC ; CC=1010 RO=100003
5162 014214 101405                        ROL RO
5163 014216 102004                        BLOS ROL7
5164 014220 100003                        BVC ROL7
5165 014222 022700 100003                BPL ROL7
5166 014226 001404                        CMP #100003, RO
5167                                     BEQ TST161
5168                                     ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
5169                                     ; CONDITIONAL BRANCH INST. AND <====
5170                                     ; REPLACE THE MOVE INSTRUCTION <====
5171                                     ; WHICH FOLLOWS W/ 725 <====
5172 014230                                ROL7:
5173 014230 012742 000334                MOV #334, -(R2) ; MOVE TO MAILBOX # ***** 334 *****
5174 014234 005242                        INC -(R2) ; SET MSGTYP TO FATAL ERROR
5175 014236 000000                        HALT ; ROL MALFUNCTIONED
5176                                     ; OR SEQUENCE ERROR
5177 ;*****
5178 ;TEST 161 TEST ROR INSTRUCTION
5179 ;*****
5180 014240 005212                                TST161: INC (R2) ; UPDATE TEST NUMBER
5181 014242 022712 000161                CMP #161, (R2) ; SEQUENCE ERROR?
5182 014246 001051                                BNE TST162-10 ; BR TO ERROR HALT ON SEQ ERROR
5183 014250 012700 000023                MOV #23, RO ; RO=23
5184 014254 000277                                SCC ; CC=0111
5185 014256 000250                                CLN
5186 014260 006000                                ROR RO ; CC=1001 RO=100011
5187 014262 102403                        BVS ROR1
5188 014264 103002                        BCC ROR1
5189 014266 001401                        BEQ ROR1
5190 014270 100404                        BMI ROR2
5191                                     ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
5192                                     ; CONDITIONAL BRANCH INST. AND <====
5193                                     ; REPLACE THE MOVE INSTRUCTION <====
5194                                     ; WHICH FOLLOWS W/ 767 <====
5195 014272                                ROR1:
5196 014272 012742 000335                MOV #335, -(R2) ; MOVE TO MAILBOX # ***** 335 *****
5197 014276 005242                        INC -(R2) ; SET MSGTYP TO FATAL ERROR
5198 014300 000000                        HALT ; ROR DID NOT SET CC'S CORRECTLY
5199 014302 000257                                ROR2: ; CC=1100
5200 014304 000274                        CCC
5201 014306 006000                        +SEN!SEZ ; CC=0011 RO=040004
5202 014310 102003                        ROR RO
5203 014312 103002                        BVC ROR3
5204 014314 001401                        BCC ROR3
5205 014316 100004                        BEQ ROR3
5206                                     BPL ROR4
5207                                     ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
5208                                     ; CONDITIONAL BRANCH INST. AND <====
                                     ; REPLACE THE MOVE INSTRUCTION <====

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5209                                     ;          WHICH FOLLOWS W/ 754          <====
5210 014320                                ROR3:                                     ;
5211 014320 012742 000336                MOV      #336, -(R2)                ; MOVE TO MAILBOX # ***** 336 *****
5212 014324 005242                        INC      -(R2)                ; SET MSGTYP TO FATAL ERROR
5213 014326 000000                        HALT                                     ; ROR DID NOT SET CC'S CORRECTLY
5214 014330 000277                                ROR4:                ; CC=1110
5215 014332 000241                        SCC                                     ;
5216 014334 006000                        CLC                                     ;
5217 014336 101403                        ROR      RO                ; CC=0000  RO=020002
5218 014340 102402                        BLOS    ROR5               ;
5219 014342 001401                        BVS     ROR5               ;
5220 014344 100004                        BEQ     ROR5               ;
5221                                     ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  <====
5222                                     ; CONDITIONAL BRANCH INST. AND           <====
5223                                     ; REPLACE THE MOVE INSTRUCTION         <====
5224                                     ; WHICH FOLLOWS W/ 741                  <====
5225 014346                                ROR5:                                     ;
5226 014346 012742 000337                MOV      #337, -(R2)                ; MOVE TO MAILBOX # ***** 337 *****
5227 014352 005242                        INC      -(R2)                ; SET MSGTYP TO FATAL ERROR
5228 014354 000000                        HALT                                     ; ROR DID NOT SET CC'S CORRECTLY
5229 014356 000257                                ROR6:                ; CC=0101
5230 014360 000265                        CCC                                     ;
5231 014362 006000                        +SEC!SEZ                            ;
5232 014364 101402                        ROR      RO                ; CC=1010  RO=110001
5233 014366 102001                        BLOS    ROR7               ;
5234 014370 100404                        BVC     ROR7               ;
5235                                     ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  <====
5236                                     ; CONDITIONAL BRANCH INST. AND           <====
5237                                     ; REPLACE THE MOVE INSTRUCTION         <====
5238                                     ; WHICH FOLLOWS W/ 727                  <====
5239 014372                                ROR7:                                     ;
5240 014372 012742 000340                MOV      #340, -(R2)                ; MOVE TO MAILBOX # ***** 340 *****
5241 014376 005242                        INC      -(R2)                ; SET MSGTYP TO FATAL ERROR
5242 014400 000000                        HALT                                     ; ROR DID NOT PRODUCE CORRECT RESULTS
5243                                     ; OR SEQUENCE ERROR
5244
5245 ;*****
5246 ;TEST 162 TEST ASL INSTRUCTION
5247 ;*****
5248 014402 005212                                TST162: INC      (R2)                ; UPDATE TEST NUMBER
5249 014404 022712 000162                CMP      #162, (R2)                ; SEQUENCE ERROR?
5250 014410 001054                        BNE     TST163-10                ; BR TO ERROR HALT ON SEQ ERROR
5251 014412 012700 144000                MOV      #144000, RO                ; RO=14000
5252 014416 000257                        CCC                                     ; CC=0110
5253 014420 000271                        +SEN!SEC                            ;
5254 014422 006300                        ASL      RO                ; CC=1001  RO=110000
5255 014424 103003                        BCC     ASL1                   ;
5256 014426 102402                        BVS     ASL1                   ;
5257 014430 001401                        BEQ     ASL1                   ;
5258 014432 100404                        BMI     ASL2                   ;
5259                                     ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  <====
5260                                     ; CONDITIONAL BRANCH INST. AND           <====
5261                                     ; REPLACE THE MOVE INSTRUCTION         <====
5262                                     ; WHICH FOLLOWS W/ 767                  <====
5263 014434                                ASL1:                                     ;
5264 014434 012742 000341                MOV      #341, -(R2)                ; MOVE TO MAILBOX # ***** 341 *****

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5265 014440 005242          INC      -(R2)          ;SET MSGTYP TO FATAL ERROR
5266 014442 000000          HALT
5267 014444 000277          ASL2:  SCC              ;CC=1100
5268 014446 000243          +CLV!CLC
5269 014450 006300          ASL      R0              ;CC=0011  R0=020000
5270 014452 103003          BCC      ASL3
5271 014454 102002          BVC      ASL3
5272 014456 001401          BEQ      ASL3
5273 014460 100004          BPL      ASL4
5274
5275
5276
5277
5278 014462
5279 014462 012742 000342          ASL3:  MOV      #342, -(R2) ;MOVE TO MAILBOX # ***** 342 *****
5280 014466 005242          INC      -(R2)          ;SET MSGTYP TO FATAL ERROR
5281 014470 000000          HALT
5282 014472 000277          ASL4:  SCC              ;ASL DID NOT SET CC'S CORRECTLY
5283 014474 000250          CLN
5284 014476 006300          ASL      R0              ;CC=0000  R0=040000
5285 014500 101402          BLOS     ASL5
5286 014502 102401          BVS      ASL5
5287 014504 100004          BPL      ASL6
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5292 014506
5293 014506 012742 000343          ASL5:  MOV      #343, -(R2) ;MOVE TO MAILBOX # ***** 343 *****
5294 014512 005242          INC      -(R2)          ;SET MSGTYP TO FATAL ERROR
5295 014514 000000          HALT
5296 014516 000257          ASL6:  CCC              ;ASL DID NOT SET CC'S CORRECTLY
5297 014520 000265          +SEZ!SEC ;CC=0101
5298 014522 006300          ASL      R0              ;CC=1010  R0=100000
5299 014524 103406          BCS      ASL7
5300 014526 001405          BEQ      ASL7
5301 014530 102004          BVC      ASL7
5302 014532 100003          BPL      ASL7
5303 014534 022700 100000          CMP      #100000, R0
5304 014540 001404          BEQ      TST163
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5309 014542
5310 014542 012742 000344          ASL7:  MOV      #344, -(R2) ;MOVE TO MAILBOX # ***** 344 *****
5311 014546 005242          INC      -(R2)          ;SET MSGTYP TO FATAL ERROR
5312 014550 000000          HALT
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5318 014552 005212          TST163: INC      (R2)          ;UPDATE TEST NUMBER
5319 014554 022712 000163          CMP      #163, (R2)      ;SEQUENCE ERROR?
5320 014560 001060          BNE      TST164-10      ;BR TO ERROR HALT ON SEQ ERROR

;*****
;TEST 163 TEST ASR INSTRUCTION
;*****
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 754 <====

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 742 <====

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 724 <====

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5321	014562	012700	100023		MOV	#100023,RO		;RO=100023	
5322	014566	000277			SCC			;CC=0110	
5323	014570	000250			CLN				
5324	014572	006200			ASR	RO		;CC=1001	RP=140011
5325	014574	102403			BVS	ASR1			
5326	014576	103002			BCC	ASR1			
5327	014600	001401			BEQ	ASR1			
5328	014602	100404			BMI	ASR2			
5329								; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS	<=====
5330								CONDITIONAL BRANCH INST. AND	<=====
5331								REPLACE THE MOVE INSTRUCTION	<=====
5332								WHICH FOLLOWS W/ 767	<=====
5333	014604			ASR1:					
5334	014604	012742	000345		MOV	#345,-(R2)		;MOVE TO MAILBOX # ***** 345 *****	
5335	014610	005242			INC	-(R2)		;SET MSGTYP TO FATAL ERROR	
5336	014612	000000			HALT			;ASR DID NOT SET CC'S CORRECTLY	
5337	014614	042700	100000	ASR2:	BIC	#100000,RO		;RO=40011	
5338	014620	000277			SCC			;CC=1100	
5339	014622	000243			+CLV!CLC				
5340	014624	006200			ASR	RO		;CC=0011	RO=020004
5341	014626	102003			BVC	ASR3			
5342	014630	103002			BCC	ASR3			
5343	014632	001401			BEQ	ASR3			
5344	014634	100004			BPL	ASR4			
5345								; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS	<=====
5346								CONDITIONAL BRANCH INST. AND	<=====
5347								REPLACE THE MOVE INSTRUCTION	<=====
5348								WHICH FOLLOWS W/ 752	<=====
5349	014636			ASR3:					
5350	014636	012742	000346		MOV	#346,-(R2)		;MOVE TO MAILBOX # ***** 346 *****	
5351	014642	005242			INC	-(R2)		;SET MSGTYP TO FATAL ERROR	
5352	014644	000000			HALT			;ASR DID NOT SET CC'S CORRECTLY	
5353	014646	000277		ASR4:	SCC			;CC=1111	
5354									
5355	014650	006200			ASR	RO		;CC=0000	RO=010002
5356	014652	101403			BLOS	ASR5			
5357	014654	102402			BVS	ASR5			
5358	014656	001401			BEQ	ASR5			
5359	014660	100004			BPL	ASR6			
5360								; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS	<=====
5361								CONDITIONAL BRANCH INST. AND	<=====
5362								REPLACE THE MOVE INSTRUCTION	<=====
5363								WHICH FOLLOWS W/ 740	<=====
5364	014662			ASR5:					
5365	014662	012742	000347		MOV	#347,-(R2)		;MOVE TO MAILBOX # ***** 347 *****	
5366	014666	005242			INC	-(R2)		;SET MSGTYP TO FATAL ERROR	
5367	014670	000000			HALT			;ASR DID NOT SET CC'S CORRECTLY	
5368	014672	052700	100000	ASR6:	BIS	#100000,RO		;RO=110002	
5369	014676	000257			CCC			;CC=0101	
5370	014700	000265			+SEZ!SEC				
5371	014702	006200			ASR	RO		;C=1010	RO=144001
5372	014704	101406			BLOS	ASR7			
5373	014706	102005			BVC	ASR7			
5374	014710	100004			BPL	ASR7			
5375	014712	001403			BEQ	ASR7			
5376	014714	022700	144001		CMP	#144001,RO		;CHECK RESULT OF ASR'S	

5377 014720 001404 BEQ TST164

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014722
014722 012742 000350
014726 005242
014730 000000

ASR7:

MOV #350, -(R2)
INC -(R2)
HALT

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 720 <====
; MOVE TO MAILBOX # ***** 350 *****
; SET MSGTYP TO FATAL ERROR
; ASR DID NOT FUNCTION CORRECTLY
; OR SEQUENCE ERROR

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5416 014732 005212
5417 014734 022712 000164
5418 014740 001062
5419 014742 012700 015332
5420 014746 012704 015370
5421 014752 012767 000015 000142
5422 014760 012067 000110
5423 014764 012401
5424 014766 012767 177777 000074
5425 014774 012703 000016
5426 015000 005267 000064
5427 015004 032701 100000
5428 015010 013705 177776
5429 015014 042705 177773
5430 015020 000165 015024
5431 015024 000167 000020
5432 015030 012767 015124 000042
5433 015036 012767 015106 000040
5434 015044 000167 000014
5435 015050 012767 015106 000022
5436 015056 012767 015124 000020
5437 015064 006101
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5439 015066 012737
5440 015070 000000
5441 015072 177776
5442 015074 000000
5443 015076 000137
5444 015100 000000

```

;*****
;
;   THIS TEST VERIFIES THE CONTENTS OF THE BRANCH ROM.  THE TEST
; EXECUTES EVERY POSSIBLE BRANCH WITH EVERY POSSIBLE CONDITION
; CODE COMBINATION.
;   THE ROUTINE USES TWO TABLES.  THE BRANCH TABLE HOLDS ALL THE
; POSSIBLE BRANCH INSTRUCTIONS.  THE OTHER TABLE (YNTAB) HOLDS BIT MAPS FOR
; EACH BRANCH.  A ONE IN THE BIT MAP INDICATES THAT THE CORRESPONDING
; BRANCH INSTRUCTION SHOULD BRANCH FOR THE CONDITION CODE SETTING WHICH
; CORRESPONDS TO THE BIT POSITION WITHIN THE MAP.  FOR EXAMPLE IF THE LEFT
; MOST BIT IS A ONE THEN THE CORRESPONDING BRANCH INSTRUCTION SHOULD BRANCH
; WHEN THE CONDITION CODES ARE 0.
;   THE ROUTINE CONSISTS OF NESTED LOOPS.  THE OUTER LOOP SETS UP
; ALL THE POSSIBLE BRANCH INSTRUCTIONS.  THE INNER LOOP SETS UP EVERY POSSIBLE
; CONDITION CODE FOR EACH BRANCH.
;   THE BIT MAP IS USED TO SET THE ADDRESS LOCATION IN TWO
; JUMP MODE 3 INSTRUCTIONS.  THE ADDRESSES ARE CHANGED TO ALLOW THE
; PROGRAM TO CONTINUE OR JUMP TO AN ERROR ROUTINE DEPENDING UPON
; WHETHER IT HANDLED THE BRANCH INSTRUCTION CORRECTLY.
;   AT ANY ERROR HALT, LOCATION, BRH, HOLDS THE BRANCH INSTRUCTION
; UNDER TEST AND LOCATION, CC, HOLDS THE VALUE OF THE CONDITION CODES
; AT THE TIME THE BRANCH WAS EXECUTED.
;*****

```

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;*****
; TEST 164      TEST THE BRANCH ROM
;*****
TST164: INC      (R2)          ;UPDATE TEST NUMBER
        CMP      #164,(R2)    ;SEQUENCE ERROR?
        BNE     ER           ;BR TO ERROR HALT ON SEQ ERROR
SETUP:  MOV      #BRTAB,R0    ;INITIALIZE BRANCH TABLE POINTER
        MOV      #YNTAB,R4    ;INITIALIZE YES/NO BRANCH MAP POINTER
        MOV      #15,BRCT     ;INITIALIZE BRANCH TABLE COUNT
SETBR:  MOV      (R0)+,BRH    ;GET NEXT BRANCH INST.
        MOV      (R4)+,R1     ;GET NEXT BRANCH MAP
        MOV      #-1,CC       ;INITIALIZE CONDITION CODE VALUE
        MOV      #16,R3       ;INITIALIZE CONDITION CODE COUNT
SETCC:  INC      CC           ;SET FOR NEXT CC VALUE
        BIT      #100000,R1    ;SEE IF SHOULD BR W/ THESE CC'S
        MOV      @#177776,R5   ;SIMULATE A JNE
        BIC     #177773,R5
        JMP     .+4(R5)
        JMP     SET2BR
        MOV      #CONT,NBR    ;SET TO CONTINUE IF NO BRANCH
        MOV      #ER,YBR      ;SET TO REPORT ERROR IF BRANCH
        JMP     AROUND        ;GO AROUNDND OPPOSITE CONDITION
        MOV      #ER,NBR      ;SET TO REPORT ERROR IF NO BRANCH
        MOV      #CONT,YBR    ;SET TO CONTINUE IF BRANCH
AROUND: ROL      R1           ;UPDATE BIT MAP
        MOV      (PC)+,@(PC)+ ;SET CONDITION CODE
CC:     0                    ;NEW CC VALUE GOES HERE
        177776
BRH:    0                    ;BRANCH INST. GOES HERE
        JMP     @ (PC)+       ;THIS JUMP IF NO BRANCH
NBR:    0                    ;WHERE TO GO IF NO BRANCH OCCURS

```

5445	015102	000137		JMP	@(PC)+	: THIS JUMP IF BRANCH OCCURS
5446	015104	000000		0		: WHERE TO GO IF BRANCH OCCURS
5447	015106	012702	000304	YBR: MOV	#\$TESTN,R2	: RESTORE POINTER
5448	015112	012742	000351	ER: MOV	#\$351,-(R2)	: MOVE TO MAILBOX # ***** 351 *****
5449	015116	005242		INC	-(R2)	: SET MSGTYP TO FATAL ERROR
5450	015120	000000		HALT		:
5451	015122	000000		BRCT: 0		:
5452	015124	005303		CONT: DEC	R3	: CC'S DONE?
5453	015126	013705	177776	MOV	@#177776,R5	: SIMULATE A JNE
5454	015132	042705	177773	BIC	##177773,R5	: (JUMP NOT EQUAL)
5455	015136	000165	015142	JMP	#+4(R5)	: TO SETCC
5456	015142	000167	177632	JMP	SETCC	:
5457	015146	005367	177750	DEC	BRCT	: BR'S DONE?
5458	015152	013705	177776	MOV	@#177776,R5	: SIMULATE A JNE
5459	015156	042705	177773	BIC	##177773,R5	: (JUMP NOT EQUAL)
5460	015162	000165	015166	JMP	#+4(R5)	: TO SETBR
5461	015166	000167	177566	JMP	SETBR	:

```

5462 :*****
5463 :TEST 165      END OF PASS SEQUENCE
5464 :*****
5465 015172 005212          TST165: INC      (R2)          ;UPDATE TEST NUMBER
5466 015174 022712 000165    CMP      #165,(R2)      ;SEQUENCE ERROR?
5467 015200 001037          BNE      EOP1          ;BR TO ERROR HALT ON SEQ ERROR
5468 015202 005237 000306    INC      @SPASS
5469 015206 105267 000076    INCB    PASSPT        ;SHOULD PRINT THIS PASS?
5470 015212 001020          BNE      ACT          ;NO
5471 015214 132767 000040 163077 BITB    #40,$ENVM      ;WILL APT ALLOW PRINTING?
5472 015222 001014          BNE      ACT          ;NO
5473 015224 023727 000042 015264    CMP      @42,$SENDAD  ;UNDER ACT AUTO ACCEPT?
5474 015232 001410          BEQ      ACT          ;IF SO SKIP PRINTOUT
5475 015234 012700 015312    MOV      #MSG,RO      ;GET MSG ADDR.
5476 015240 105737 177564    WAIT:  TSTB    @TPS     ;TTY READY
5477 015244 100375          BPL      WAIT         ;NO WAIT
5478 015246 112037 177566    MOVB    (RO)+,@TPB    ;PRINT CHARACTER
5479 015252 001372          BNE      WAIT         ;NEXT IF NOT DONE.
5480 015254 013700 000042    ACT:   MOV      @42,RO  ;CHECK ACT
5481 015260 001405          BEQ      GOAGIN       ;KEEP GOING
5482 015262 000005          RESET
5483 015264 004710          SENDAD: JSR     PC,(RO) ;ACT HOOKS
5484 015266 000240          NOP
5485 015270 000240          NOP
5486 015272 000240          NOP
5487 015274 000167 163222    GOAGIN: JMP     RESTRT   ;DO NEXT PASS
5488 015300          EOP1:
5489 015300 012742 000352    MOV      #352,-(R2)   ;MOVE TO MAILBOX # ***** 352 *****
5490 015304 005242          INC      -(R2)        ;SET MSGTYP TO FATAL ERROR
5491 015306 000000          HALT      ;SEQUENCE ERROR
5492 015310 177777          PASSPT: -1
5493 015312 047105 020104 043117    MSG:   .ASCIZ .END OF DGKAA.<15><12>
5494 015320 042040 045507 040501
5495 015326 005015          000
    
```

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5496          015332          .EVEN
5497
5498 015332 000402      BRTAB: BR      .+6
5499 015334 001002      BNE      .+6
5500 015336 001402      BEQ      .+6
5501 015340 002002      BGE      .+6
5502 015342 002402      BLT      .+6
5503 015344 003002      BGT      .+6
5504 015346 003402      BLE      .+6
5505 015350 100002      BPL      .+6
5506 015352 100402      BMI      .+6
5507 015354 101002      BHI      .+6
5508 015356 101402      BLOS     .+6
5509 015360 102002      BVC      .+6
5510 015362 102402      BVS      .+6
5511 015364 103002      BCC      .+6
5512 015366 103402      BCS      .+6

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5513
5514          000002      .RADIX 2
5515 015370 177777      YNTAB: 1111111111111111
5516 015372 170360      1111000011110000
5517 015374 007417      0000111100001111
5518 015376 146063      1100110000110011
5519 015400 031714      0011001111001100
5520 015402 140060      1100000000110000
5521 015404 037717      0011111111001111
5522
5523 015406 177400      1111111100000000
5524 015410 000377      0000000011111111
5525 015412 120240      1010000010100000
5526 015414 057537      0101111101011111
5527 015416 146314      1100110011001100
5528 015420 031463      0011001100110011
5529 015422 125252      1010101010101010
5530 015424 052525      0101010101010101
5531

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;BR
;BNE: Z=0
;BEQ: Z=1
;BGE: N XOR V =0
;BLT: N XOR V =1
;BGT: Z+(N XOR V) =0
;BLE: Z+(N XOR V) =1
;BPL: N=0
;BMI: N=1
;BHI: C+Z=0
;BLOS: C+Z=1
;BVC: V=0
;BVS: V=1
;BCC: C=0
;BCS: C=1

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5532          000010      .RADIX 8
5533 015426 012737 015436 000024 PWRDN: MOV      #PWRUP, @#24      ;SET UP FOR A POWER UP
5534 015434 000000      HALT
5535
5536 015436 012737 015426 000024 PWRUP: MOV      #PWRDN, @#24      ;SET UP FOR A POWER FAIL
5537 015444 012706 000500      MOV      #STBOT, R6      ;SET UP STACK POINTER
5538 015450 132767 000040 162643 BITB     #40, $ENVM      ;SHOULD PRINT?
5539 015456 001010      BNE      PWR2           ;IF NOT: BR
5540 015460 012700 015504      MOV      #PFMES, R0      ;GET POWER FAIL MESSG.
5541 015464 105737 177564      WATE:   TSTB    @#TPS     ;TTY READY?
5542 015470 100375      BPL      WATE           ;IF NOT: BR
5543 015472 112037 177566      MOVB    (R0)+, @#TPB    ;PRINT NEXT CHAR.
5544 015476 001372      BNE      WATE           ;IF NOT DONE: BR
5545 015500 000137 000500      PWR2:   JMP      @#START  ;START PROGRAM AGAIN
5546
5547 015504 006412 047520 042527 PFMES: .ASCIZ <12><15>.POWER FAILURE.<12><15>
5548 015512 020122 040506 046111
5549 015520 051125 005105 000015
5550
5551          000001      .END

```

ABASE =	000000	424			
ACDW1 =	000000	424			
ACDW2 =	000000	424			
ACPUOP =	000000	424	439		
ACT	015254	5470	5472	5474	5480#
ADC1	013120	4750	4751	4757#	
ADC2	013130	4752	4761#		
ADC3	013150	4765	4766	4772#	
ADC4	013160	4767	4776#		
ADC5	013176	4779	4780	4781	4787#
ADDW0 =	000000	424			
ADDW1 =	000000	424			
ADDW10 =	000000	424			
ADDW11 =	000000	424			
ADDW12 =	000000	424			
ADDW13 =	000000	424			
ADDW14 =	000000	424			
ADDW15 =	000000	424			
ADDW2 =	000000	424			
ADDW3 =	000000	424			
ADDW4 =	000000	424			
ADDW5 =	000000	424			
ADDW6 =	000000	424			
ADDW7 =	000000	424			
ADDW8 =	000000	424			
ADDW9 =	000000	424			
ADD1	012734	4672	4673	4679#	
ADD2	012744	4674	4683#		
ADD3	012760	4686	4687	4693#	
ADD4	012770	4688	4697#		
ADD5	013006	4700	4701	4707#	
ADD6	013016	4702	4711#		
ADD7	013030	4712	4713	4719#	
ADD8	013040	4714	4723#		
ADD9	013060	4726	4727	4728	4734#
ADEVCT =	000000	424	430		
ADEVN =	000000	424			
RENV	000000	424	435		
RENVN	000000	424	436		
RFATAL =	000000	424	427		
AMADR1 =	000000	424			
AMADR2 =	000000	424			
AMADR3 =	000000	424			
AMADR4 =	000000	424			
AMAMS1 =	000000	424			
AMAMS2 =	000000	424			
AMAMS3 =	000000	424			
AMAMS4 =	000000	424			
AMSGAD =	000000	424	432		
AMSGLG =	000000	424	433		
AMSGTY =	000000	424	426		
AMTYP1 =	000000	424			
AMTYP2 =	000000	424			
AMTYP3 =	000000	424			
AMTYP4 =	000000	424			
RPASS =	000000	424	429		

APRIOR=	000000	424				
AROUND	015064	5434	5437#			
ASL1	014434	5255	5256	5257	5263#	
ASL2	014444	5258	5267#			
ASL3	014462	5270	5271	5272	5278#	
ASL4	014472	5273	5282#			
ASL5	014506	5285	5286	5292#		
ASL6	014516	5287	5296#			
ASL7	014542	5299	5300	5301	5302	5309#
ASR1	014604	5325	5326	5327	5333#	
ASR2	014614	5328	5337#			
ASR3	014636	5341	5342	5343	5349#	
ASR4	014646	5344	5353#			
ASR5	014662	5356	5357	5358	5364#	
ASR6	014672	5359	5368#			
ASR7	014722	5372	5373	5374	5375	5382#
ASWREG=	000000	424	437			
ATESTN=	000000	424	428			
AUNIT =	000000	424	431			
AUSWR =	000000	424	438			
AVECT1=	000000	424				
AVECT2=	000000	424				
BIC1	012064	4345	4346	4352#		
BIC2	012074	4347	4356#			
BIC3	012112	4359	4360	4366#		
BIS1	012154	4382	4383	4384	4390#	
BIS2	012164	4385	4394#			
BIS3	012204	4397	4398	4399	4405#	
BIT1	011774	4307	4308	4314#		
BIT2	012004	4309	4319#			
BIT3	012022	4322	4323	4329#		
BACT	015122	5421*	5451#	5457*		
BRC1	002350	1228	1234#			
BRC2	002360	1229	1239#			
BRC3	002370	1241	1247#			
BRH	015074	5422*	5442#			
BRN1	002230	1134	1140#			
BRN2	002240	1135	1145#			
BRN3	002250	1147	1153#			
BRTAB	015332	5419	5498#			
BRV1	002300	1181	1187#			
BRV2	002310	1182	1192#			
BRV3	002320	1194	1200#			
BRZ1	002160	1087	1093#			
BRZ2	002170	1088	1098#			
BRZ3	002200	1100	1106#			
BR1	000572	504	510#			
BR2	000602	505	514#			
BR3	000614	515	523#			
BR4	000622	524	530#			
BRS	000632	525	534#			
CC	015070	5424*	5426*	5440#		
CLR1	012522	4563	4564	4565	4571#	
CMP1	013364	4869	4870	4876#		
CMP2	013374	4871	4880#			
CMP3	013416	4884	4885	4891#		

3174	3175	3176	3177	3178	3211*	3212	3213	3214	3215	3216	3243*	3244
3245	3246	3247	3248	3273*	3275*	3278	3288*	3290*	3293	3320*	3321*	3323*
3337*	3338*	3351*	3352*	3353*	3355*	3383*	3384*	3386*	3390*	3391*	3401*	3402*
3404*	3408*	3418*	3419*	3420*	3422*	3426*	3427*	3511*	3513*	3517	3546*	3549*
3553	3640*	3641*	3650	3675*	3676*	3703*	3704*	3714*	3767*	3768*	3778	3805*
3807*	3817	3848*	3849*	3850	3881*	3882*	3883	3936*	3937	3938	3956*	3958
3971*	3972	3973	3991*	3993	4004*	4006	4017*	4019	4031*	4033	4074*	4078
4094	4126*	4127	4142*	4143	4149	4165	4176*	4177	4228*	4229*	4235	4268*
4283*	4303*	4306	4321	4341*	4344*	4358*	4378*	4381*	4396*	4429*	4432*	4444*
4447*	4463*	4483*	4485*	4500*	4514*	4526*	4529*	4562*	4585	4598*	4601	4621*
4624*	4638*	4669*	4671*	4685*	4699*	4711*	4725*	4746*	4749*	4761*	4764*	4778*
4809*	4812*	4825*	4828*	4841*	4844*	4865*	4868	4880*	4883	4895*	4898	4911*
4913	4933*	4936*	4967*	4970*	4982*	4985*	4997*	5000*	5014*	5034*	5037*	5052*
5067*	5080*	5083*	5114*	5117*	5132*	5147*	5161*	5165	5183*	5186*	5201*	5216*
5231*	5251*	5254*	5269*	5284*	5298*	5303	5321*	5324*	5337*	5340*	5355*	5368*
5371*	5376	5419*	5422	5475*	5478	5480*	5483	5540*	5543			
737*	739*	4076*	4077*	4078*	4088	4105*	4109	4124*	4127*	4131	4143*	4147
4160*	4163	4177*	4181	4192*	4200	5423*	5427	5437*				
482*	493*	500*	501	511*	512*	520*	521*	531*	532*	540*	541*	562*
563	573*	574*	581*	582	592*	593*	600*	601	611*	612*	619*	620
629*	630*	661*	662	672*	673*	680*	681	690*	691*	698*	699	708*
709*	716*	717	726*	727*	734*	735	746*	747*	754*	755	757*	759*
766*	767*	768*	770*	774*	775	786*	787*	794*	795	806*	807*	814*
815	826*	827*	834*	835	846*	847*	870*	871	881*	882*	889*	890
899*	900*	907*	908	917*	918*	925*	926	935*	936*	958*	959	970*
971*	978*	979	989*	990*	999*	1000*	1007*	1008	1019*	1020*	1027*	1028
1039*	1040*	1047*	1048	1059*	1060*	1081*	1082	1094*	1095*	1107*	1108*	1128*
1129	1141*	1142*	1154*	1155*	1175*	1176	1188*	1189*	1201*	1202*	1222*	1223
1235*	1236*	1248*	1249*	1291*	1292	1300*	1301*	1310*	1311*	1319*	1320*	1337*
1338	1347*	1348*	1364*	1365*	1378*	1379	1387*	1388*	1399*	1400*	1415*	1416
1425*	1426*	1438*	1439*	1453*	1454	1465*	1466*	1479*	1480*	1497*	1498	1510*
1511*	1525*	1526*	1543*	1544	1557*	1558*	1573*	1574*	1591*	1592	1605*	1606*
1620*	1621*	1633*	1634	1648*	1649*	1665*	1666*	1687*	1688	1700*	1701*	1714*
1715*	1734*	1735	1749*	1750*	1767*	1768*	1788*	1789	1802*	1803*	1819*	1820*
1827*	1828	1839*	1840*	1855*	1856*	1878*	1879	1890*	1891*	1904*	1905*	1920*
1921	1932*	1933*	1944*	1945*	1961*	1962	1973*	1974*	1985*	1986*	2001*	2002
2011*	2012*	2024*	2025*	2041*	2042	2057*	2058*	2073*	2074	2089*	2090*	2105*
2106	2122*	2123*	2137*	2138	2154*	2155*	2171*	2172*	2186*	2187	2203*	2204*
2213*	2214*	2229*	2230	2246*	2247*	2255*	2256*	2271*	2272*	2281*	2282*	2296*
2297	2315*	2316*	2325*	2326*	2342*	2343	2362*	2363*	2377*	2378*	2387*	2388*
2402*	2403	2419*	2420*	2428*	2429*	2443*	2444	2462*	2463*	2472*	2473*	2487*
2488	2505*	2506*	2514*	2515*	2529*	2530	2547*	2548*	2556*	2557*	2570*	2571
2583*	2584*	2597*	2598	2610*	2611*	2626*	2627	2636*	2637*	2649*	2650*	2660*
2661*	2675*	2676*	2686*	2687*	2700*	2701	2712*	2713*	2721*	2722*	2731*	2732*
2743*	2744*	2753*	2754*	2768*	2769	2782*	2783*	2796*	2797	2810*	2811*	2825*
2826	2839*	2840*	2858*	2859	2874*	2875*	2884*	2885*	2899*	2900	2914*	2915*
2929*	2930	2942*	2943*	2952*	2953*	2969*	2970	2982*	2983*	2991*	2992*	3005*
3006	3020*	3021*	3030*	3031*	3046*	3047	3058*	3059*	3073*	3074	3085*	3086*
3100*	3101	3112*	3113*	3132*	3133	3147*	3148*	3170*	3171	3185*	3186*	3208*
3209	3222*	3223*	3240*	3241	3254*	3255*	3270*	3271	3285*	3286*	3300*	3301*
3317*	3318	3333*	3334*	3348*	3349*	3365*	3366*	3380*	3381	3398*	3399*	3415*
3416*	3434*	3435*	3449*	3450	3463*	3464*	3477*	3478*	3491*	3492*	3507*	3508
3524*	3525*	3542*	3543	3560*	3561*	3576*	3577	3590*	3591*	3605*	3606	3620*
3621*	3637*	3638	3647*	3648*	3656*	3657*	3671*	3672	3683*	3684*	3699*	3700
3711*	3712*	3720*	3721*	3736*	3737	3747*	3748*	3763*	3764	3775*	3776*	3784*
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R2 =%000002

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SNMB2B	004462	2240	2249#		
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SNM2A	004372	2194	2195	2196	2202#
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SOPB1A	002704	1460	1468#		
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SOPX	004034	2005#	2014*	2015*	2028
SOPXAD	004100	2017*	2028#		
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SOP1A	002630	1420	1428#		
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SOP5A	003636	1885	1893#		

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4082	4083#	4101	4102#	4120	4121#	4138	4139#	4156	4157#	4172	4173#	4188
4189#	4207	4208#	4232	4233#	4241	4242#	4277	4278#	4292	4293#	4315	4316#
4330	4331#	4353	4354#	4367	4368#	4391	4392#	4406	4407#	4441	4442#	4457
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4595	4596#	4610	4611#	4633	4634#	4648	4649#	4680	4681#	4694	4695#	4708
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		616	622#	624	658	664#	667	677	683#	685	695	701#
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		811	817#	821	831	837#	841	867	873#	876	886	892#
		910#	912	922	928#	930	955	961#	965	975	981#	984
		1010#	1014	1024	1030#	1034	1044	1050#	1054	1078	1084#	1101
		1148	1172	1178#	1195	1219	1225#	1242	1288	1294#	1314	1334
		1375	1381#	1393	1412	1418#	1432	1450	1456#	1473	1494	1500#
		1546#	1567	1588	1594#	1614	1630	1636#	1659	1684	1690#	1708
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		1958	1964#	1979	1998	2004#	2018	2038	2044#	2051	2070	2076#
		2108#	2116	2134	2140#	2165	2183	2189#	2208	2226	2232#	2276
		2320	2339	2345#	2382	2399	2405#	2423	2440	2446#	2467	2484
		2526	2532#	2551	2567	2573#	2578	2594	2600#	2605	2623	2629#
		2703#	2748	2765	2771#	2777	2793	2799#	2805	2822	2828#	2834
		2879	2896	2902#	2909	2926	2932#	2947	2966	2972#	2986	3002
		3043	3049#	3053	3070	3076#	3080	3097	3103#	3107	3129	3135#
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3851	3874	3880#	3884	3929	3935#	4037	4064	4070#	4201	4220	4226#	4236
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488#	494*											
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503#	518	538	565#	571	584#	590	603#	609	622#	627	664#	670
683#	688	701#	706	719#	724	737#	744	757#	777#	784	797#	804
817#	824	837#	844	873#	879	892#	897	910#	915	928#	933	961#
968	981#	987	997	1010#	1017	1030#	1037	1050#	1057	1084#	1091	1104
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797	804	817	824	837	844	873	879	892	897	910	915	928
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3173	3182	3211	3220	3243	3252	3273	3282	3297	3320	3330	3345	3362
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TYPNAM
TYPNUM
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TYPTXT
SSERCD

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ASL	5254	5269	5284	5298										
ASR	5324	5340	5355	5371										
BCC	740	760	780	800	820	840	984	1013	1053	1228	3277	3292	3340	3357
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	5203	5255	5270	5326	5342	5511								
BOS	1229	2050	2114	2163	2195	2263	2307	2369	3325	3405	3423	3455	3514	3612
	4489	4533	4565	4588	4640	4780	4846	5038	5053	5299	5512			4382
BEQ	504	535	568	587	606	624	667	685	703	721	741	761	781	801
	841	876	894	912	930	965	994	1014	1034	1054	1088	1100	1295	1314
	1382	1393	1420	1432	1460	1473	1505	1519	1552	1567	1600	1614	1643	1659
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	2051	2116	2165	2197	2208	2250	2265	2276	2309	2320	2371	2423	2467	2509
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	4023	4037	4095	4114	4132	4150	4166	4182	4201	4236	4385	4399	4451	4487
	4566	4589	4642	4729	4782	4815	4831	4901	5017	5041	5056	5070	5120	5135
	5189	5204	5219	5257	5272	5300	5304	5327	5343	5358	5375	5377	5474	5481
	5501													5500
BGE	2707	5503												
BGT	4284	4322	4359	4501	4700	4765	4869	4937	4971	5507				
BHI	2642	2667	4344	4358	4526	4825	4911	5080	5337	5429	5454	5459		
BIC	2975	3138	3176	3214	3246									
BICB	2652	3051	4381	4396	4444	4761	4895	4982	5368					
BIS	2803	2907	3078	3105	3139	3177	3215	3247						
BISB	2737	2747	4306	4321	5427									
BIT	5471	5538												
BITB	5504													
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BLOS	4625	4672	4686	4712	4750	4884	4914	4986	5001	5084	5148	5162	5217	5232
	5356	5372	5508											4602
	2716	5502												5285
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	4816	4832	4902	5018	5040	5055	5071	5121	5190	5234	5258	5328	5506	4781
BNE	502	515	524	564	583	602	621	663	682	700	718	736	756	776
	816	836	872	891	909	927	960	980	1009	1029	1049	1083	1087	1101
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	1845	1896	1936	1977	2016	4286	4324	4361	4434	4466	4674	4702	4767	4848
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	5344	5359	5374	5477	5505	5542								5302
BR	505	525	4070	5498										
BVC	1181	1195	3276	3291	3324	3339	3356	4503	4532	4687	4701	4751	4829	4885
	4987	5015	5085	5134	5163	5202	5233	5271	5301	5341	5373	5509		4899

BVS	1182	1194	1241	2048	2081	2113	2146	2162	2194	2238	2262	2306	2354	2368	2411
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	4564	4587	4603	4626	4639	4673	4713	4726	4766	4779	4814	4845	4870	4915	4938
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	5199	5229	5252	5296	5369										
CLC	738	758	778	798	818	838	961	1011	1031	1051	3322	3385	3403	3467	3548
	3610	4267	4305	4343	4380	4462	4513	4724	4777	4811	5051	5131	5215	5268	5339
CLN	1146	2079	2144	2236	2352	2452	2495	2537	4267	4305	4343	4380	4395	4513	4528
	4600	4623	4748	4811	5066	5146	5185	5283	5323						
CLR	1294	1340	1418	1419	1456	1457	1500	1501	1546	1549	1551	1594	1597	1636	1639
	1690	1693	1694	1737	1740	1741	1791	1794	1830	1833	1881	1882	1884	1923	1926
	1964	1967	2004	2044	2076	2108	2109	2140	2141	2157	2189	2190	2232	2233	2299
	2300	2345	2346	2405	2406	2446	2447	2490	2491	2532	2533	2573	2575	2600	2601
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CLRB	1381	1459	1504	1599	1642	1743	1796								
CLV	1193	1240	4528	4748	4882	4984	5082	5131	5268	5339					
CLZ	1099	2046	2111	2160	2192	2260	2304	2366	2409	4282	4320	4357	4446	4499	4561
	4584	4637	4724	4763	4777	4843	5036	5051							
CMP	501	563	582	586	601	605	620	623	662	681	684	699	702	717	720
	735	755	775	795	815	835	871	890	893	908	911	926	929	959	964
	979	993	1008	1028	1033	1048	1082	1129	1176	1223	1292	1338	1379	1416	1454
	1498	1544	1592	1634	1688	1735	1789	1828	1879	1921	1962	2002	2042	2074	2106
	2138	2187	2230	2297	2343	2403	2444	2488	2530	2571	2598	2627	2701	2706	2715
	2725	2769	2797	2826	2859	2900	2930	2970	3006	3047	3074	3079	3101	3106	3133
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	5376	5417	5466	5473											
CMPB	2833														
COM	1313	1458	1502	1550	1562	1598	1640	1705	1742	1795	1844	1895	1935	1976	2407
	2448	2492	2534	2574	2602	2640	2641	2666	2735	2772	2801	2830	2864	2866	2877
	2934	2974	3011	4077	4936	4997									
COMB	1390	1547	1595	1637	1691	1738	1792	1831	1924	1965	2077	2142	2234	2301	2319
	2347	2348	2449	2466	2493	2508	2535	2550	2664	2804	2832	2863	2906	2985	3012
DEC	1341	1357	1428	1513	1560	1561	1564	1565	1608	1612	1651	1652	1654	1657	1703
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	5452	5457													
HALT	409	513	522	533	542	575	594	613	631	674	692	710	728	748	769
	788	808	828	848	883	901	919	937	972	991	1001	1021	1041	1061	1096
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	1804	1821	1841	1857	1892	1906	1934	1946	1975	1987	2013	2026	2059	2091	2124
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INC	4122	4140	4158	4174	4190	4209	4234	4243	4279	4294	4317	4332	4355	4369	4393
	4408	4443	4459	4474	4497	4511	4525	4541	4574	4597	4612	4635	4650	4682	4696
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	5266	5281	5295	5312	5336	5352	5367	5385	5450	5491	5534				
	500	512	521	532	541	562	574	581	593	600	612	619	630	661	673
	680	691	698	709	716	727	734	747	754	768	774	787	794	807	814
	827	834	847	870	882	889	900	907	918	925	936	958	971	978	990
	1000	1007	1020	1027	1040	1047	1060	1081	1095	1108	1128	1142	1155	1175	1183
	1202	1222	1236	1249	1291	1301	1303	1311	1320	1337	1348	1365	1378	1388	1400
	1415	1426	1439	1453	1466	1468	1480	1497	1503	1511	1514	1515	1526	1543	1548
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	1925	1933	1937	1945	1961	1966	1974	1978	1986	2001	2012	2014	2017	2025	2041
	2058	2073	2090	2105	2123	2137	2155	2158	2172	2186	2204	2214	2229	2247	2256
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INCB	1392	1472	1518	1613	1658	1760	1812	5469							
JMP	479	483	3937	3958	3972	3993	4006	4019	4033	4071	5430	5431	5434	5443	5445
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MOV	481	482	489	490	491	492	493	494	495	496	511	520	531	540	565
	573	584	592	603	611	622	629	665	672	683	690	701	708	719	726
	737	746	757	766	767	770	777	786	797	806	817	826	837	846	873
	874	881	892	899	910	917	928	935	962	970	981	989	999	1010	1019
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	2011	2024	2057	2089	2122	2154	2171	2203	2213	2246	2255	2271	2281	2315	2325
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MOVB	2867	2878	3013	5478	5543										
NEG	1304	1356	2015	4812	4828	4844									
NEGB	1470	1516	1610	1655	1756	1810	1883	2679							
NOP	403	5484	5485	5486											
RESET	5482														
ROL	739	759	779	799	819	839	963	983	1012	3275	3323	3386	3454	3513	3549
	3581	3611	5117	5132	5147	5161	5437								
ROLB	3290	3338	3355	3404	3422	3468	3482								
ROR	1032	1052	5186	5201	5216	5231									
RTS	4229														
SBC	1354	5037	5052	5067	5083										
SCC	1098	1145	1192	1239	2045	2078	2110	2143	2159	2191	2235	2259	2303	2351	2365
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	4527	4560	4583	4599	4622	4636	4670	4723	4747	4762	4776	4810	4842	4881	4912
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SEC	982	1227	1350	1353	1430	3274	3289	3336	3354	3421	3453	3481	3512	3580	4445
	4498	4867	4935	4969	5160	5230	5253	5297	5370						
SEN	1133	4698	4867	4969	5200	5253									
SEV	1180	5116													
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SUB	2678	3714	4970	4985	5000	5014									
SWAB	3641	3676	3704	3740	3768	3807	3849	3882	4624	4638					
TST	567	666	875	2047	2112	2193	2305	2350	2380	2381	2410	2422	2453	2496	2538
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TSTB	2080	2145	2161	2237	2261	2353	2367	2976	5476	5541					
.ASCIZ	5493	5547													
.BYTE	435	436													
.ENABL	1	399													
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	750	770	790	810	830	850	885	903	921	939	974	993	1003	1023	1043
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	2093	2126	2157	2175	2206	2217	2249	2258	2274	2285	2318	2329	2365	2380	2391
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.EVEN	424	5496													
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	667	676	685	694	703	712	721	730	741	750	767	781	790	801	810
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MACRO	1														
MCALL	409														
MEXIT	447														
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ERRORS DETECTED: 0
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