AA11

DAC CALIBRATION
MD-11-D6B-A

EP-D6B-A-DL

FICHE 1 OF 1

FEB 1978
digital
MADE IN USA

IDENTIFICATION

PRODUCT CODE: MAINDEC-11-D6BA-D

PRODUCT NAME: AA11 DAC CALIBRATION

DATE CREATED: NOVEMBER 20, 1978

MAINTAINER: DIAGNOSTIC GROUP

AUTHOR: JOHN RODENHISER

1. ABSTRACT

THIS PROGRAM ASSISTS IN THE TESTING AND CALIBRATION OF THE AA11 DIGITAL TO ANALOG CONVERTER. PROVISIONS ARE INCLUDED FOR A PDP-11 SYSTEM WITH UP TO 4 AA-11 DAC'S. THE PROGRAM IS DIVIDED INTO FOUR SECTIONS: DAC TEST, RAMP, SQUARE WAVE, AND CALIBRATE.

2. REQUIREMENTS

2.1 EQUIPMENT

PDP-11/20
AA11 DIGITAL TO ANALOG CONVERTER SUBSYSTEM WITH UP TO 4 CONVERTER MODULES.

2.2 STORAGE

THE PROGRAM OCCUPIES MEMORY FROM 0 TO 1510.

3. LOADING PROCEDURE

3.1 METHOD

PROCEDURE FOR NORMAL BINARY TAPES SHOULD BE FOLLOWED.

1. ABSOLUTE LOADER MUST BE IN MEMORY.
2. PLACE BINARY TAPE IN READER
3. LOAD ADDRESS #7500 (# DETERMINED BY ADDRESS OF LOADER).
4. PRESS "START" (PROGRAM WILL LOAD).

4. STARTING PROCEDURE

4.1 CONTROL SWITCH SETTINGS

4.1.1 ALL SECTIONS

SWITCH REGISTER BITS 14, 13, 12 SELECTS DAC TO BE TESTED.

14	13	12		ADDRESS ASSIGNMENT	
0	0	0	DAC0	176760	(REFERENCE 8.3)
0	0	1	DAC1	176762	
0	1	0	DAC2	176764	
1	0	0	DAC3	176766	

4.1.2 RAMP, SQUARE WAVE, AND CALIBRATE

SWITCH REGISTER BIT 11 CONTROLS DAC POLARITY

11=0 POSITIVE
11=1 NEGATIVE

4.1.3 RAMP TEST

SWITCH REGISTER BITS 6 THRU 0 CONTOL RAMP SLOPE

```
6  5 4 3  2 1 0

0  0 0 0  0 0 0 = MINIMUM RAMP TIME
0  0 0 0  0 0 1
0  0 0 0  0 1 0
0  0 0 0  0 1 1
          .
          .
          .
1  1 1 1  1 1 1 = MAXIMUM RAMP TIME
```

4.1.4 SQUARE WAVE

SWITCH REGISTER BITS 6 THRU 0 CONTROL SQUARE WAVE FREQUENCY

```
6  5 4 3  2 1 0

0  0 0 0  0 0 0 = MAXIMUM FREQUENCY
0  0 0 0  0 0 1
0  0 0 0  0 1 0
0  0 0 0  0 1 1
          .
          .
          .
1  1 1 1  1 1 1 = MINIMUM FREQUENCY
```

4.1.5 CALIBRATE

SWITCH REGISTER BITS 10 THRU 0 CONTROL 11 BIT DAC VALUE.

```
10 9  8 7 6  5 4 3  2 1 0

0  0  0 0 0  0 0 0  0 0 0 = MINIMUM VALUE (0 VOLTS)
             .
             .
             .
1  1  1 1 1  1 1 1  1 1 1 = MAXIMUM VALUE (+ OR - FULL SCALE)
```

4.2 STARTING ADDRESS

4.2.1 200 DAC TEST

4.2.2 204 RAMP

4.2.3 210 SQUARE WAVE

4.2.4 214 CALIBRATE

4.3 PROGRAM AND/OR OPERATOR ACTION

LOAD PROGRAM INTO MEMORY
SELECT TEST.
LOAD STARTING ADDRESS.
SET APPROPRIATE CONTROL SWITCHES.
PRESS "START"

5. OPERATING PROCEDURE

5.1 DAC TEST

LOAD ADDRESS 200
SELECT ONE DAC WITH SWITCHES 14, 13, 12 (REFERENCE 4.1.1).
PRESS START.
PROGRAM WILL BEGIN TESTING THE SELECTED DAC.
ONLY ONE DAC WILL BE TESTED AT A TIME, HOWEVER, DAC SELECTION
CAN BE CHANGED AT ANY TIME WHILE THE PROGRAM IS RUNNING.

5.2 RAMP TEST

LOAD ADDRESS 204.
SELECT ONE DAC WITH SWITCHES 14, 13, 12 (REFERENCE 4.1.1).
SELECT POLARITY WITH SWITCH 11 (REFERENCE 4.1.2).
SELECT RAMP SLOPE WITH SWITCHES 6 THRU 0 (REFERENCE 4.1.3).
PRESS START.
PROGRAM WILL EXECUTE RAMP.
ONLY ONE DAC AND POLARITY MAY BE SELECTED AT A TIME. TO
SELECT ANOTHER DAC OR CHANGE POLARITY RESTART TEST AT 210.
SWITCHES CONTROLLING RAMP SLOPE MAY BE CHANGED WHILE PROGRAM
IS RUNNING.

5.3 SQUARE WAVE

LOAD ADDRESS 210.
SELECT ONE DAC WITH SWITCHES 14, 13, 12 (REFERENCE 4.1.1).
SELECT POLARITY WITH SWITCH 11 (REFERENCE 4.1.2)
SELECT SQUARE WAVE FREQUENCY WITH SWITCHES 6 THRU 0 (REFERENCE 4.1.4)
PRESS START.
PROGRAM WILL EXECUTE SQUARE WAVE.
ONLY ONE DAC AND MAY BE SELECTED AT A TIME. TO SELECT ANOTHER
DAC RESTART TEST. SWITCHES CONTROLLING SQUARE WAVE POLARITY OR
FREQUENCY MAY BE CHANGED WHILE PROGRAM IS RUNNING.

5.4 CALIBRATE TEST

LOAD ADDRESS 214.
SELECT UP TO FOUR DACS WITH SWITCHES 14, 13, 12 (REFERENCE 4.1.1).
SELECT POLARITY WITH SWITCH 11 (REFERENCE 4.1.2).
SELECT DAC VALUE WITH SWITCHES 10 THRU 0 (REFERENCE 4.1.5).
PRESS START.
PROGRAM WILL LOAD DACS WITH SELECTED VALUES.
SWITCHES SELECTING DACS, POLARITY OR VALUES CAN BE CHANGED
WHILE PROGRAM IS RUNNING.

6. ERRORS

6.1 ERROR REPORTING

IF AN ERROR OCCURS DURING DAC TEST THE PROGRAM WILL HALT.
REGISTER Ø WILL CONTAIN EXPECTED VALUE OF DAC. TO RESUME
TESTING PRESS "CONTINUE". IF IT IS DESIRED TO LOOP ON
THE TEST THAT FAILS REPLACE THE HALT INSTRUCTION WITH A
240 (NOP).

NO ERROR INDICATIONS ARE GIVEN DURING OTHER TESTS.

7. RESTRICTIONS

NONE

8. MISCELLANEOUS

8.1 EXECUTION TIME

N/A

8.2 PROGRAMMING TECHNIQUE

THIS PROGRAM MAKES EXTENSIVE USE OF GENERAL REGISTERS FOR THE
PURPOSE OF GAINING MAXIMUM OPERATING SPEED.

8.3 DAC SELECTION

THE PROGRAM CAN TEST UP TO FOUR DAC'S AT ONE TIME. IN IT'S STANDARD FORM IT WILL TEST DAC0, DAC1, DAC2 AND DAC3. MEMORY ADDRESSES 100, 102, 104 AND 106 CONTAIN THE POINTERS FOR THESE DACS. IF IT IS DESIRED TO TEST ANY OF THE OTHER 16 DACS, THE OPERATOR MUST CHANGE THE CONTENTS OF THE POINTER ADDRESSES TO SELECT THE DESIRED DAC.

EXAMPLE: 100/ 176760
102/ 176520
104/ 176542
106/ 176566

DACS 0, 8, 13 AND 19 COULD NOW BE SELECTED.

DAC	ADDRESS
0	176760
1	176762
2	176764
3	176766
4	176500
5	176502
6	176504
7	176506
8	176520
9	176522
10	176524
11	176526
12	176540
13	176542
14	176544
15	176546
16	176560
17	176562
18	176564
19	176566

9. PROGRAM DESCRIPTION

9.1 DAC TEST

THIS TEST MAKES CERTAIN THAT ALL BITS OF THE DAC MAY BE SET, CLEARED AND READ BACK. FIRST THE DAC IS CLEARED AND CHECKED TO BE CLEAR, THEN SET TO ALL ONES AND CHECKED TO BE SET TO ALL ONES, NEXT THE DAC IS SET WITH AN INCREMENTING PATTERN AND CHECKED. ALSO CHECKED ARE THE CONDITIONS WITH BIT 11 SET TO MAKE SURE THAT BIT 11 IS REFLECTED IN BITS 15 THRU 12.

9.2 RAMP TEST

THE DAC SELECTED BY SWITCHES 14, 13, 12 IS CLEARED (SET TO ZERO VOLTS) AND THEN INCREMENTED (OR DECREMENTED) AT A RATE THAT MAY BE CONTROLLED BY SWITCHES 6 THRU 0 UNTIL THE MAXIMUM VALUE (+ OR - FULL SCALE) IS REACHED.

9.3 SQUARE WAVE

THE DAC SELECTED BY SWITCHES 14, 13, 12 IS SET TO ZERO AND FULL SCALE (IF POLARITY NEGATIVE) AT A RATE THAT MAY BE CONTROLLED BY SWITCHES 6 THRU 0.

9.4 CALIBRATION

THE VALUE CONTAINED IN SWITCHES 11 THRU 0 IS LOADED INTO THE DAC SELECTED BY SWITCHES 14, 13, 12. THE OPERATOR MUST DETERMINE WITH A DVM OR SCOPE IF THE DAC OUTPUT IS ACCURATE.

```
                                ;AA11 DAC CALIBRATION
                                ;COPYRIGHT 1970, DIGITAL EQUIPMENT CORP., MAYNARD, MASS.
                                ;JOHN RODENHISER
            000000                      .=0
            000020                      .REPT   20
                                        .+2
                                        HALT
                                        .ENDR
000000  000002                         .+2
000002  000000                         HALT
000004  000006                         .+2
000006  000000                         HALT
000010  000012                         .+2
000012  000000                         HALT
000014  000016                         .+2
000016  000000                         HALT
000020  000022                         .+2
000022  000000                         HALT
000024  000026                         .+2
000026  000000                         HALT
000030  000032                         .+2
000032  000000                         HALT
000034  000036                         .+2
000036  000000                         HAL
000040  000042                         .+2
000042  000000                         HALT
000044  000046                         .+2
000046  000000                         HALT
000050  000052                         .+2
000052  000020                         HALT
000054  000056                         .+2
000056  000000                         HALT
000060  000062                         .+2
000062  000000                         HALT
000064  000066                         .+2
000066  000000                         HALT
000070  000072                         .+2
000072  000000                         HALT
000074  000076                         .+2
000076  000000                         HALT
                                ;THE FOLLOWING 4 ADDRESSES MAY BE MODIFIED TO POINT TO OTHER DACS
000100  176760                  DAC0:   176760                  ;CONTAINS ADDRESS OF DAC 0
000102  176762                  DAC1:   176762                  ;CONTAINS ADDRESS OF DAC 1
000104  176764                  DAC2:   176764                  ;CONTAINS ADDRESS OF DAC 2
000106  176766                  DAC3:   176766                  ;CONTAINS ADDRESS OF DAC 3
            177570              SR=177570
            000240              NOP=240
            000776              STACK=776

            000200                      .=200
000200  000167  000574                  JMP     DACTST          ;DAC TEST
000204  000167  001006                  JMP     RAMP            ;RAMP TEST
000210  000167  001106                  JMP     SQUARE          ;SQUARE WAVE TEST
000214  000167  000704                  JMP     CALIB           ;CALIBRATE
```

```
001000                          .=1000
                        ;TEST DAC BITS 12-0 TO SET AND CLEAR
                        ;SW 14, 13, 12 SELECT DACS
001000  012706  000776  DACTST: MOV     #STACK,%6
001004  004767  000422          JSR     %7,DACSEL       ;GET DAC SELECTED
                        ;TEST DAC CAN BE CLEARED
001010  005010          DT0:    CLR     (0)
001012  011001                  MOV     (0),%1
001014  001402                  BEQ     DT1
001016  000000                  HALT                    ;ERROR DAC NOT CLEARED
001020  000773                  BR      DT0
                        ;TEST DAC CAN BE SET TO ALL 1'S
001022  012710  177777  DT1:    MOV     #-1,(0)
001026  011001                  MOV     (0),%1
001030  022701  177777          CMP     #-1,%1
001034  001402                  BEQ     DT2
001036  000000                  HALT                    ;ERROR DAC NOT = ALL 1'S
001040  000770                  BR      DT1
                        ;TEST DAC WILL ACCEPT A COUNT PATTERN (0 TO 3777)
001042  005001          DT2:    CLR     %1
001044  005010                  CLR     (0)
001046  005201          DT2A:   INC     %1
001050  005210                  INC     (0)
001052  020110                  CMP     %1,(0)
001054  001402                  BEQ     DT2B
001056  000000                  HALT                    ;ERROR DAC NOT = %1
001060  000770                  BR      DT2
001062  022701  003777  DT2B:   CMP     #3777,%1
001066  001367                  BNE     DT2A
                        ;TEST THAT DAC WILL ACCEPT A COUNT PATTERN (4000-7777)
001070  012701  173777  DT3:    MOV     #173777,%1
001074  012710  003777          MOV     #3777,(0)
001100  005210          DT3A:   INC     (0)
001102  005201                  INC     %1
001104  020110                  CMP     %1,(0)
001106  001402                  BEQ     DT3B
001110  000000                  HALT                    ;ERROR DAC NOT = %1
001112  000766                  BR      DT3
001114  022710  177777  DT3B:   CMP     #-1,(0)
001120  001367                  BNE     DT3A
001122  000726                  BR      DACTST          ;REPEAT TEST LOOP
```

```
                                        ;CALIBRATION ROUTINE FOR UP TO 4 DACS
                                        ;SW 14, 13, 12 SELECT DACS
                                        ;SW 11 SELECTS POLARITY
                                        ;SW 10-0 SELECTS DIGITAL VALUE
001124  032767  070000  176436  CALIB:  BIT     #70000,SR       ;TEST SW 12, 13, 14 = 0 TO LOAD DAC 0
001132  001003                          BNE     C1
001134  016777  176430  176736          MOV     SR,@DAC0
001142  032767  010000  176420  C1:     BIT     #10000,SR       ;TEST SW 12 TO LOAD DAC 1
001150  001403                          BEQ     C2
001152  016777  176412  176722          MOV     SR,@DAC1
001160  032767  020000  176402  C2:     BIT     #20000,SR       ;TEST SW 13 TO LOAD DAC 2
001166  001403                          BEQ     C3
001170  016777  176374  176706          MOV     SR,@DAC2
001176  032767  040000  176364  C3:     BIT     #40000,SR       ;TEST SW 14 TO LOAD DAC 3
001204  001747                          BEQ     CALIB
001206  016777  176356  176672          MOV     SR,@DAC3
001214  000743                          BR      CALIB
                                        ;RAMP TEST
                                        ;SW 14, 13, 12 SELECTS DACS
                                        ;SW 11 SELECTS POLARITY
                                        ;SW 7-0 CONTROLS RAMP SLOPE
001216  012706  000776          RAMP:   MOV     #STACK,%6
001222  004767  000204                  JSR     %7,DACSEL
001226  032767  004000  176334          BIT     #4000,SR
001234  001015                          BNE     RN
                                        ;POSITIVE RAMP
                                        ;%0 CONTAINS DAC POINTER
001236  005010          RP:     CLR     (0)             ;CLEAR DAC
001240  012702  177570                  MOV     #SR,%2          ;%2 IS SWITCH REGISTER POINTER
001244  012703  003777                  MOV     #3777,%3        ;%3 IS DAC VALUE COMPARITOR
001250  005210          RP1:    INC     (0)             ;+1 TO DAC VALUE
001252  111201          RP2:    MOVB    (2),%1          ;GET DELAY FROM SWITCHES
001254  105301                  DECB    %1
001256  100376                  BPL     .-2             ;DELAY COUNT
001260  020310                  CMP     %3,(0)          ;IS DAC=37777
001262  001372                  BNE     RP1             ;NO
001264  005010                  CLR     (0)             ;YES, CLEAR DAC
001266  000771                  BR      RP2
                                        ;NEGATIVE RAMP
                                        ;%0 CONTAINS DAC POINTER
001270  005010          RN:     CLR     (0)             ;CLEAR DAC
001272  012702  177570                  MOV     #SR,%2          ;%2 IS SWITCH REGISTER POINTER
001276  012703  174000                  MOV     #174000,%3      ;%3 IS DAC VALUE COMPARITOR
001302  005310          RN1:    DEC     (0)             ;-1 TO DAC VALUE
001304  111201          RN2:    MOVB    (2),%1          ;GET DELAY FROM SWITCHES
001306  105301                  DECB    %1
001310  100376                  BPL     .-2             ;DELAY COUNT
001312  020310                  CMP     %3,(0)          ;IS DAC=174000
001314  001372                  BNE     RN1             ;NO
001316  005010                  CLR     (0)             ;YES, CLEAR DAC
001320  000771                  BR      RN2
```

```
                                ;SQUARE WAVE TEST
                                ;SW 14, 13, 12 SELECTS DACS
                                ;SW 11 SELECTS POLARITY
                                ;SW 7-0 CONTROLS FREQUENCY
001322  012706  000776          SQUARE: MOV     #STACK,%6
001326  004767  000100                  JSR     %7,DACSEL
001332  032767  004000  176230  SQ:     BIT     #4000,SR
001340  001016                          BNE     SN
                                ;POSITIVE SQUARE WAVE
                                ;%0 CONTAINS DAC POINTER
001342  012710  000000          SP:     MOV     #0,(0)          ;SET DAC AT 0 VOLTS
001346  000400                          BR      .+2             ;BALANCE TIME BETWEEN + AND GND
001350  116701  176214                  MOVB    SR,%1
001354  105301                          DECB            %1
001356  100376                          BPL     .-2             ;DELAY
001360  012710  003777                  MOV     #3777,(0)       ;SET DAC AT +10 VOLTS
001364  116701  176200                  MOVB    SR,%1
001370  105301                          DECB    %1
001372  100376                          BPL     .-2             ;DELAY
001374  000756                          BR      SQ
                                ;NEGATIVE SQUARE WAVE
                                ;%0 CONTAINS DAC POINTER
001376  012710  000000          SN:     MOV     #0,(0)          ;SET DAC AT 0 VOLTS
001402  000400                          BR      .+2             ;BALANCE TIME BETWEEN - AND GND
001404  116701  176160                  MOVB    SR,%1
001410  105301                          DECB    %1
001412  100376                          BPL     .-2             ;DELAY
001414  012710  004000                  MOV     #4000,(0)       ;SET DAC AT -10 VOLTS
001420  116701  176144                  MOVB    SR,%1
001424  105301                          DECB    %1
001426  100376                          BPL     .-2             ;DELAY
001430  000740                          BR      SQ
```

```
                                ;DAC SELECT SUBROUTINE
                                ;SWITCH REGISTER BITS 14, 13, 12 SELECT DACS
                                ;REGISTER 0 WILL CONTAIN POINTER FOR DAC SELECTED
                                ;
001432  132767  000160  176131  DACSEL: BITB    #160,SR+1       ;IS DAC 0 SELECTED?
001440  001003                          BNE     DS1             ;NO
001442  016700  176432                  MOV     DAC0,%0 ;YES
001446  000207                          RTS     %7
001450  132767  000020  176113  DS1:    BITB    #20,SR+1        ;IS DAC 1 SELECTED
001456  001403                          BEQ     DS2             ;NO
001460  016700  176416                  MOV     DAC1,%0 ;YES
001464  000207                          RTS     %7
001466  132767  000040  176075  DS2:    BITB    #40,SR+1        ;IS DAC2 SELECTED
001474  001403                          BEQ     DS3             ;NO
001476  016700  176402                  MOV     DAC2,%0 ;YES
001502  000207                          RTS     %7
001504  016700  176376          DS3:    MOV     DAC3,%0 ;MUST BE DAC3 - NO OTHERS SELECTED
001510  000207                          RTS     %7
        000001                          .END
```

```
C1          001142
C2          001160
C3          001176
CALIB       001124
DAC0        000100
DAC1        000102
DAC2        000104
DAC3        000106
DACSEL      001432
DACTST      001000
DS1         001450
DS2         001466
DS3         001504
DT0         001010
DT1         001022
DT2         001042
DT2A        001046
DT2B        001062
DT3         001070
DT3A        001100
DT3B        001114
NOP         000240
RAMP        001216
RN          001270
RN1         001302
RN2         001304
RP          001236
RP1         001250
RP2         001252
SN          001376
SP          001342
SQ          001332
SQUARE      001322
SR          177570
STACK       000776

ERRORS DETECTED: 0

RUN-TIME:  1 SECONDS

4K CORE USED
```