EK-CI780-UG-001

CI780 USER'S GUIDE

Prepared by Educational Services
of
Digital Equipment Corporation

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TABLES

CHAPTER 1
INTRODUCTION

1.1 THE COMPUTER INTERCONNECT

The Computer Interconnect (CI) is a high-speed, serial data bus used to link computer subsystems (nodes) to form a CI cluster. Typically, the cluster is confined to a computer room environment. Nodes may consist of CPUs, memory, and intelligent mass storage, communication, and data acquisition subsystems. Features of the CI include:

- Dual signal paths capable of simultaneous operation
- 70 megabit/sec path bandwidth
- Low error rates
- Packet-oriented transmission
- Immediately acknowledges successful packet receipt
- Contention arbitration (light loading)
- Round-robin arbitration (heavy loading)

Each node within a CI cluster connects to the CI via an interface that provides two separate signal paths (Figure 1-1). Dual paths provide a high degree of data availability between nodes. One pair of nodes can communicate over one path (path A), while another pair of nodes communicates over the second path (path B).

A single CI path consists of a pair of bus cables (one for transmit, one for receive). These cables connect a node and the signal distribution coupler for that path. For each path, a central Star Coupler (SC008) receives the data transmitted by a node and distributes this data to the other nodes within the cluster.

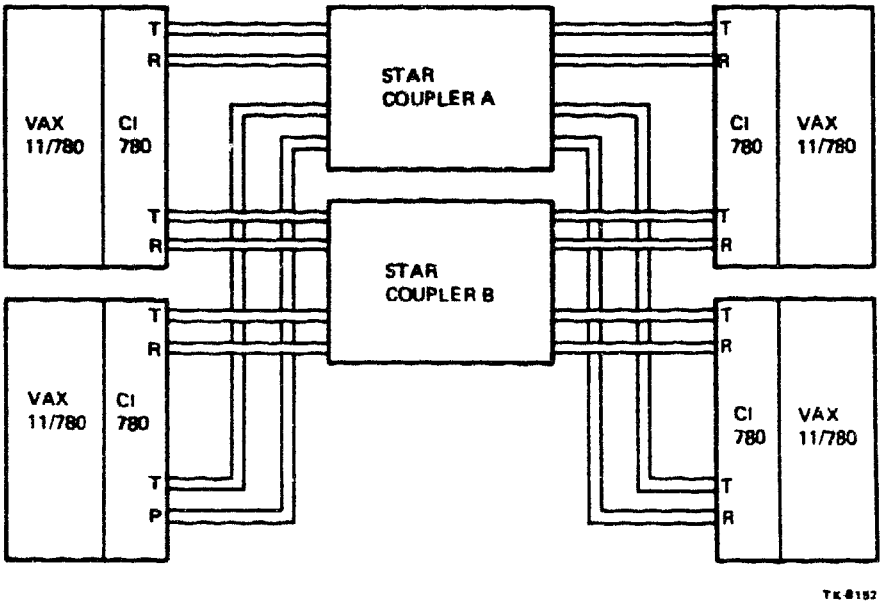

Figure 1-1 4-Node CI Cluster

1.2 THE CI780 INTERFACE

The CI780 interface connects the Synchronous Backplane Interface (SBI) of a host VAX-11/780 system to the CI (Figure 1-2).

NOTE
References to VAX-11/780 imply the VAX-11/782 Primary Processor.

The CI780 is an intelligent interface that functions as a buffered communications port. It uses the queue structures provided under the VAX/VMS operating system to transfer messages and blocks of data between the host system's memory and other nodes within the CI cluster. By providing the necessary data buffering, address translation, and serial encoding/decoding, the CI780 reduces the amount of overhead software processing required to complete typical high-level intercomputer communications.

The CI780 may be installed in any 4 inch option slot in either the standard CPU cabinet or H9602-H SBI expansion cabinet of the host system. It consists of the following major components:

- Four extended hex "L" series modules

  1. Link Interface Module (ILI) L0100
  2. Packet Buffer Module (IPB) L0101
  3. Data Path Module (IDP) L0102
  4. SBI Interface Module (ISI) L0104

- Pressed pin backplane (P/N 70 17654)

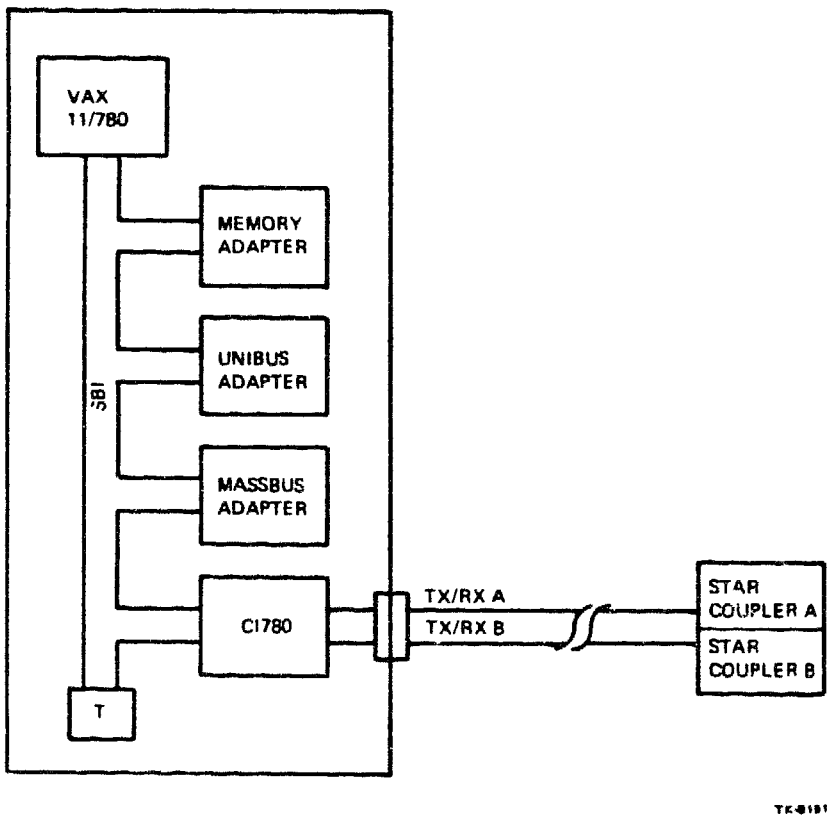

Figure 1-2 Typical CI780 Connection

- H7100 power supply with H7101 −5 V regulator (P/N 70 14956)
- TX/RX cable sets (2) with attached bulkhead connectors (P/N 70 18527)

NOTE

CI bus cables and SC008 Star Couplers are separate options. They are not a part of the CI780 Interface option.

Figure 1-3 shows the module-level block diagram of the CI780.

For the CI780 to operate correctly, the host VAX-11/780 system must have:

1. Hardware at revision level 4 or higher.
2. Two (2) MBytes or more of memory installed.
3. VAX/VMS software version 3.1 or higher installed.

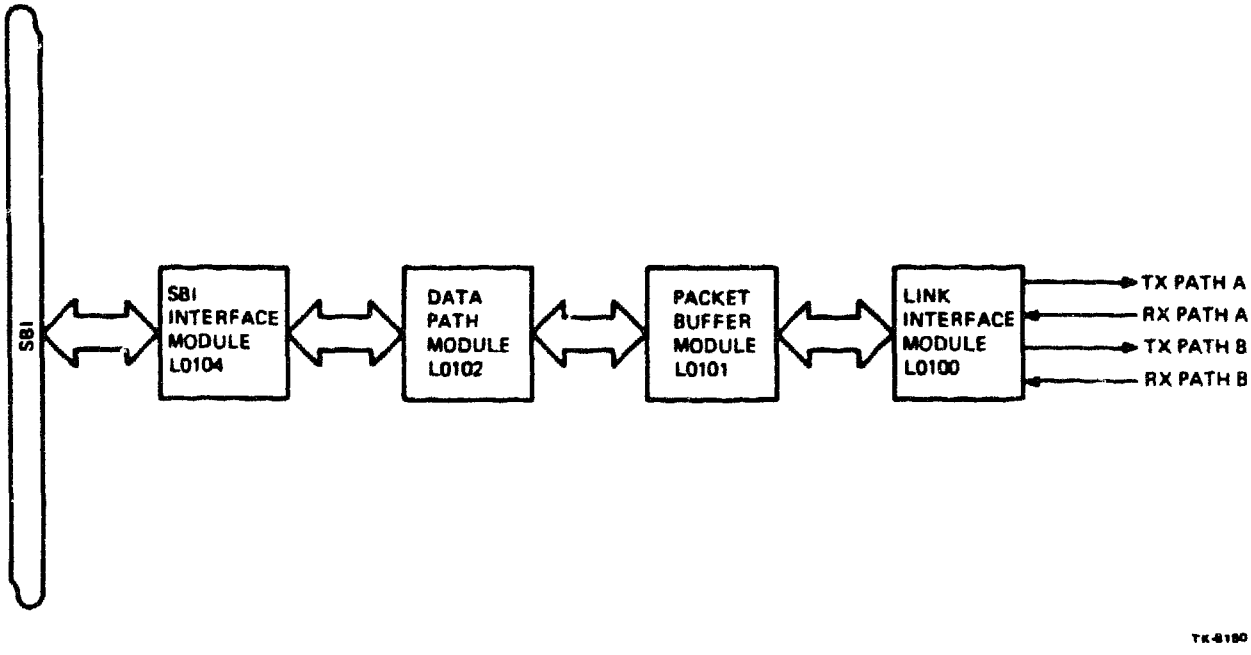

Figure 1-3 CI780 Block Diagram

1.3 CI780 SPECIFICATIONS

The CI780 specifications are outlined in Table 1-1.

Table 1-1 CI780 Specifications

Specification	Description
Data Format	Manchester encoded serial packets
Data Transfer Rate	5 MB/Sec maximum
Data Throughput	3 MB/Sec sustained
Modes	Uninitialized Uninitialized/Maintenance Disabled Disabled/Maintenance Enabled Enabled/Maintenance
SBI Priority Level	TR14 BR4
CI Cluster Cabling	Half-duplex - BNCIA-XX shielded coaxial cables, 45 meters (148 feet) maximum radius from coupler
Power	+5 V at 48.3A nominal −5.2 V at 10A nominal
Operating Temperature Range	10° C to 40° C (50° F to 104° F) with a temperature gradient of 20° C/hour (36° F/hour)
Operating Relative Humidity Range	10% to 90% with a wet bulb temperature of 28° C (82° F), and a minimum dew point of 2° C (36° F)
Operating Altitude Range	Sea level to 2400 meters (8000 ft) Derate the maximum allowable operating temperature by 1.8° C/1000 meters (1° F/1000 feet) for operation above sea level

1.4 RELATED DOCUMENTS

Table 1-2 lists the documents related to this guide.

Table 1-2 Related Hardware and Software Documents

Title	Document Numbers
CI780 Technical Description	EK-CI780-TD-001
SC008 Star Coupler User's Guide	EK-SC008-UG-001
VAX-11/780 System Installation Manual	EK-SI780-IN-002

DIGITAL personnel may order hardcopy documents from:

Digital Equipment Corporation
444 Whitney Street
Northboro, MA. 01532

Attn: Publishing and Circulation Services (NRO3/W3)
Order Processing Section

Customers may order hardware documents from:

Digital Equipment Corporation
Accessories and Supplies Group
Cotton Road
Nashua, New Hampshire 03060

For information call: 1-800-257-1710

CHAPTER 2
INSTALLATION

2.1 INTRODUCTION

The installation procedure for the CI780 requires:

1. Unpacking and inspecting the components
2. Mounting the components in either of the following cabinets:
   - The standard VAX-11/780 CPU cabinet
   - The H9602-H SBI expansion cabinet
3. Connecting the components
4. Configuring the jumpers and switches

2.2 UNPACKING AND INSPECTING THE CI780

The CI780 is packaged for shipment in two cardboard containers placed on a wooden pallet and covered with a single outer carton (see Figure 2-1). The outer carton is secured to the pallet with two shipping straps.

1. Cut the shipping straps and remove the outer carton.
2. Check each of the two inner containers for external damage such as dents, holes, or crushed corners.
3. Notify your DIGITAL Representative of any damage and list it on the appropriate installation report form. Clarify the extent of the damage.
4. Make sure the containers are sealed.

NOTE

Any opened containers should be called to the attention of the customer and documented on the appropriate installation report form.

5. Open the two containers and check their contents against the packing list (Figure 2-2).

NOTE

Packing materials such as foam fillers and plastic inserts should be retained if reshipment is contemplated.

Notify your DIGITAL Representative of any missing or incorrect items.

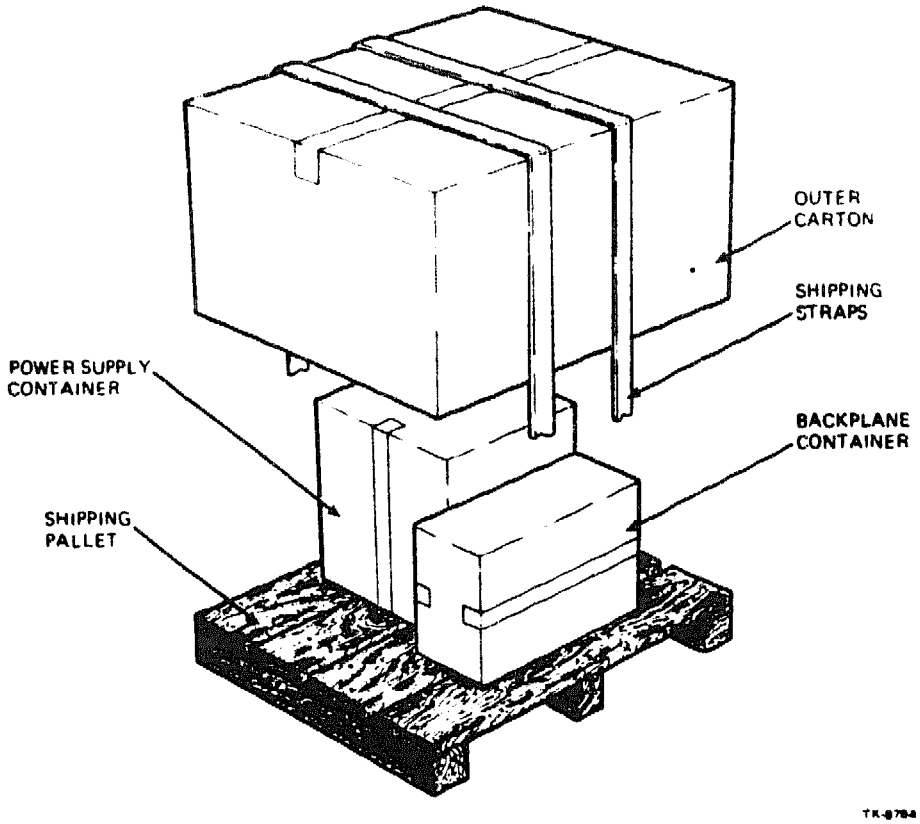

Figure 2-1 CI780 Outer Packaging

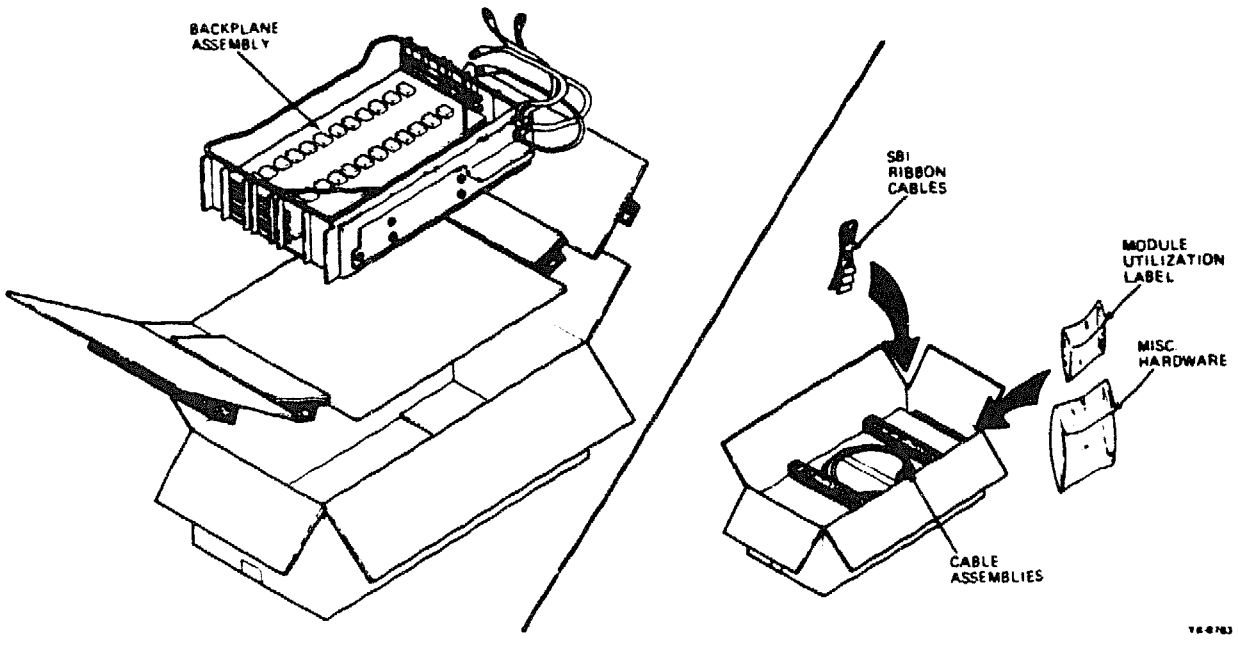

Figure 2-2 CI780 Backplane Container Arrangement

6. Inspect each component for damage such as scratches, dents, or breaks. Report any damage to shipping and record it on the appropriate installation report form. Notify your DIGITAL Representative of any damaged components that require immediate replacement.

2.3 MOUNTING THE CI780 IN THE CPU CABINET

The following paragraphs describe the procedure for mounting the CI780 components in the standard VAX-11/780 CPU cabinet. Connecting the CI780 components is described in Section 2.5.

2.3.1 Turning Off the System and Removing AC Power

NOTE
Check with the system manager before shutting the system down.

To turn off the system, and remove power, perform the following (Figure 2-3):

1. Shut down the system from the console terminal.
   a. Log in to the "SYSTEM" account.
   b. Type @SYS$SYSTEM:SHUTDOWN.
   c. Answer any questions asked by the program.
2. Set the front panel keyswitch to the OFF position.

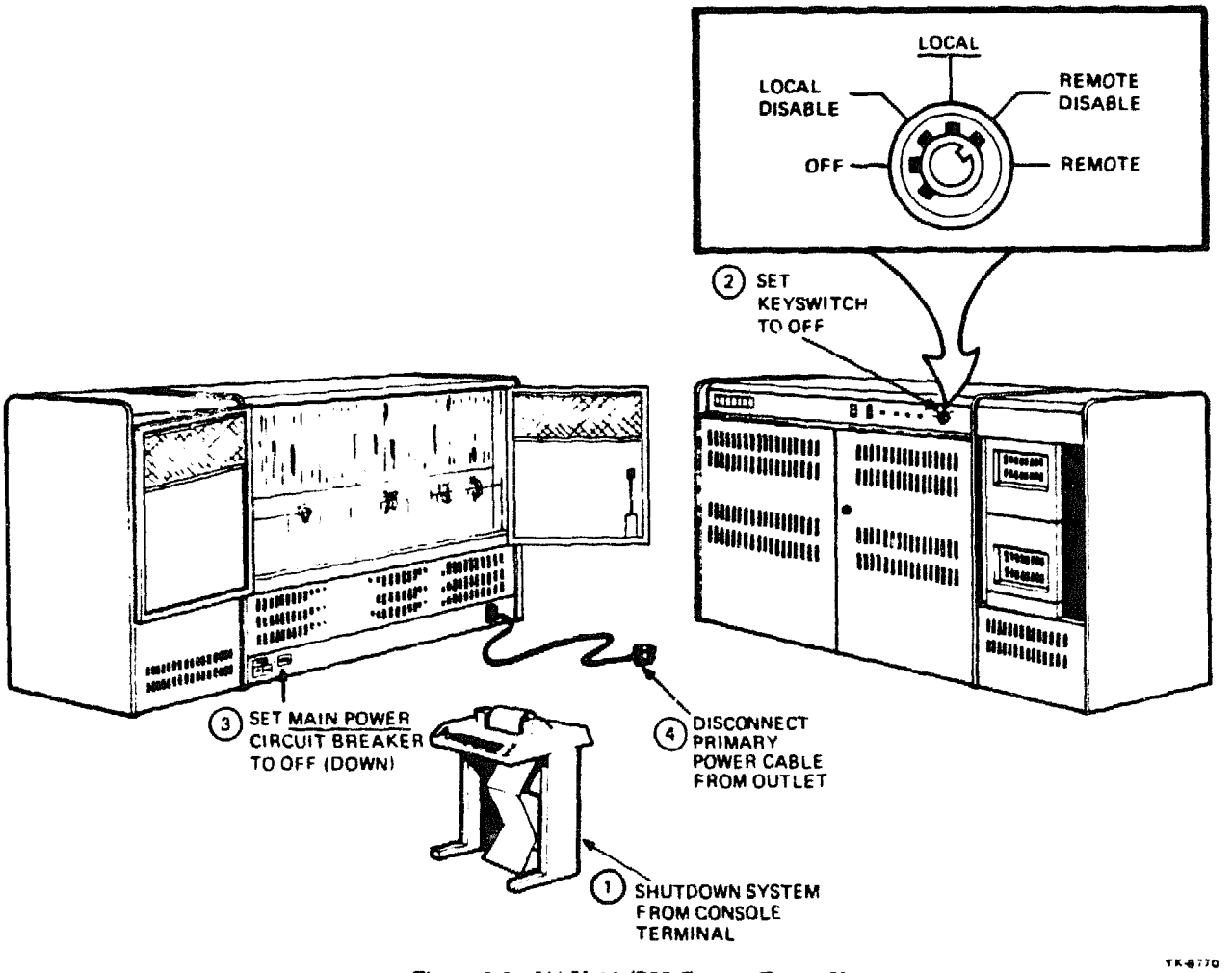

Figure 2-3 VAX-11/780 System Turn-off

3. Set the main power circuit breaker to the OFF (down) position.

4. Disconnect the primary power cable from its outlet.

2.3.2 Mounting The CI780 Power Supply (H7100 with H7101 -5 V Regulator)

NOTE

If the CI780 will share a power supply with another VAX-11/780 option, then the H7100 with the H7101 -5 V regulator (P/N 7014956) MUST be the power supply used. Remove the existing option power supply in step 2 below.

To mount the CI780 Power Supply (Figure 2-4):

1. Open the front and back CPU cabinet covers.

2. Remove the option power supply blank panel.

   a. From the front, remove the screw at the top center of the blank power supply panel.

   b. From the back, release the mounting chassis slide lock from the locking pin at the bottom of the blank power supply panel.

   c. From the front, slide the blank power supply panel out of the mounting chassis.

3. Carefully slide the H7100 power supply (P/N 7014956) into the empty slot from the front. Be sure to align the rear locking pin of the power supply with the hole at the back of the mounting chassis.

4. Secure the back of the power supply to the chassis by engaging the mounting chassis slide lock over the power supply locking pin.

5. Secure the front of the power supply to the chassis with an 8 × 32 screw supplied.

2.3.3 Mounting The CI780 Backplane Assembly

To mount the CI780 Backplane Assembly:

1. From the back, remove and save the six 12" SBI jumper cables (P/N 1700087-01) connecting J1 through J6 of the System Far End Terminator (SFT) to J1 through J6 of the adjacent backplane to the right of the SFT.

NOTE

These cables will be used to connect the CI780 backplane assembly to the SFT in Section 2.5.

2. Remove the blank panel from the next empty 4" option slot (Figure 2-4).

   a. From the front, remove the four screws holding the blank panel to the bottom of the chassis.

   b. From the back, remove the two screws holding the blank panel to the top of the chassis.

   c. From the back, slide the blank panel out of the chassis.

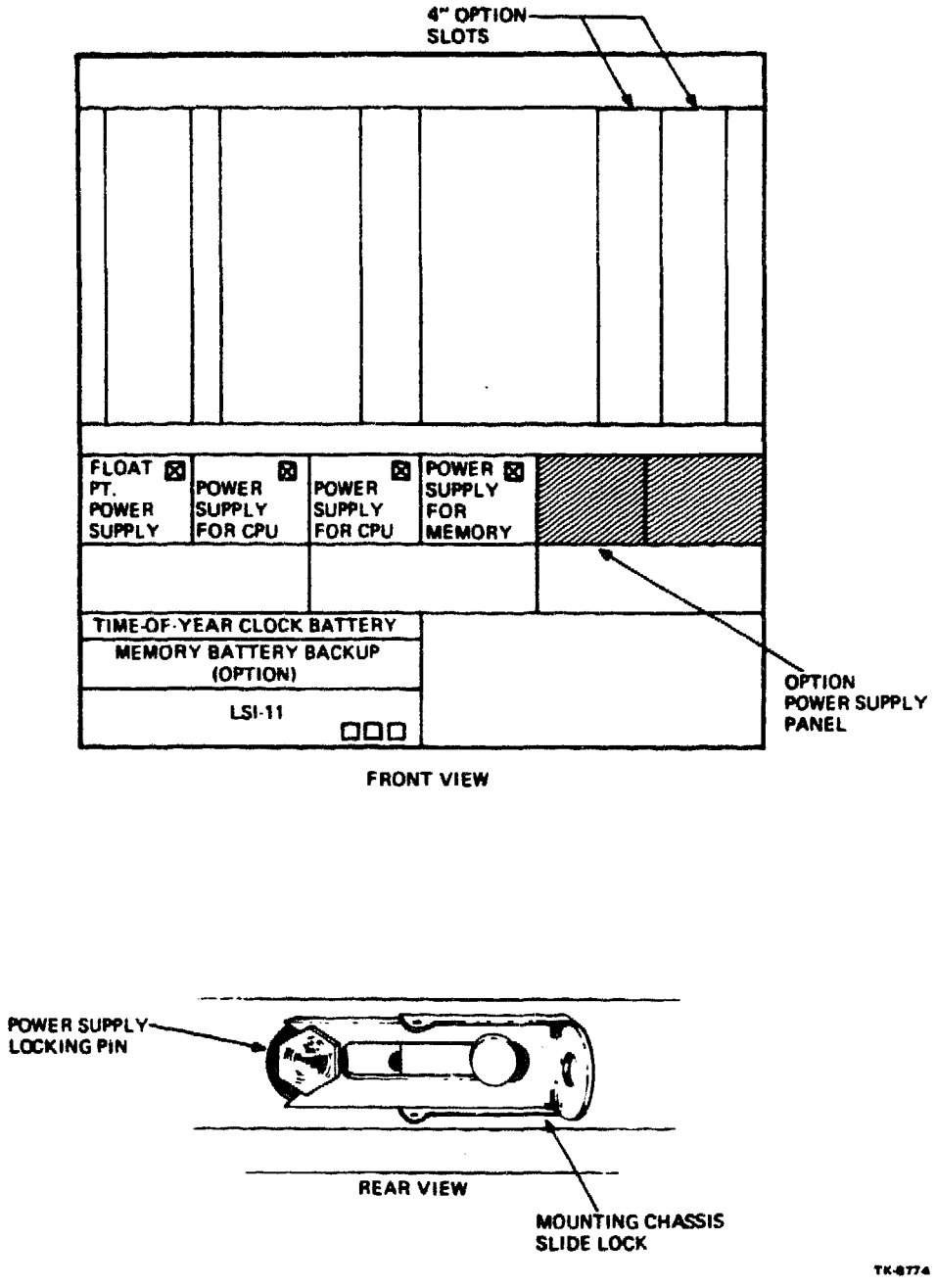

Figure 2-4 CPU Cabinet Option Mounting Details

3. Carefully slide the CI780 backplane assembly (P/N 7017654) into the empty slot from the back of the cabinet.

4. Secure the backplane assembly to the front and back of the chassis using four 8 × 2 screws.

5. Locate the CI780 Module Utilization Label (P/N 3618809-01) and remove its paper backing.

6. From the front, place the label on the inside of the left vertical cabinet channel (Figure 2-11).

2.4 MOUNTING THE CI780 IN THE H9602-H SBI EXPANSION CABINET

The following paragraphs describe the procedure for mounting the CI780 components in the H9602-H SBI expansion cabinet. The procedure for connecting the CI780 components is described in Section 2.5.

2.4.1 Turning Off the System and Removing AC Power

NOTE
Check with the system manager before shutting down the system.

To turn off the system and remove power (Figure 2-3):

1. Shut down the system from the console terminal.
   a. Log in to the "SYSTEM" account.
   b. Type @SYS$SYSTEM:SHUTDOWN.
   c. Answer any questions asked by the program.
2. Set the front panel keyswitch to the OFF position.
3. Set the main power circuit breaker to the OFF (down) position.
4. Disconnect the primary power cable from the outlet.

2.4.2 Mounting the CI780 Power Supply (H7100 with H7101 -5 V Regulator)

NOTE
If the CI780 is to share a power supply with another VAX 11/780 option, then the H7100 with the H7101 -5V regulator (P/N 7014956) MUST be the power supply used. Remove the existing option power supply in step 2 below.

To mount the CI780 Power Supply:

1. Open the front and back expansion cabinet covers.
2. Remove the blank power supply panel from the next empty power supply slot (Figure 2-5).
   a. From the front, remove the screw at the top center of the blank power supply panel.
   b. From the back, release the mounting chassis slide lock from the locking pin at the bottom of the blank power supply panel.
   c. From the front, slide the blank power supply panel out of the mounting chassis.
3. Carefully slide the H7100 power supply (P/N 7014956) into the empty slot from the front. Be sure to align the rear locking pin of the power supply with the hole at the back of the mounting chassis.
4. Secure the back of the power supply to the chassis by engaging the mounting chassis slide lock over the power supply locking pin.
5. Secure the front of the power supply to the chassis with an 8 × 32 screw.

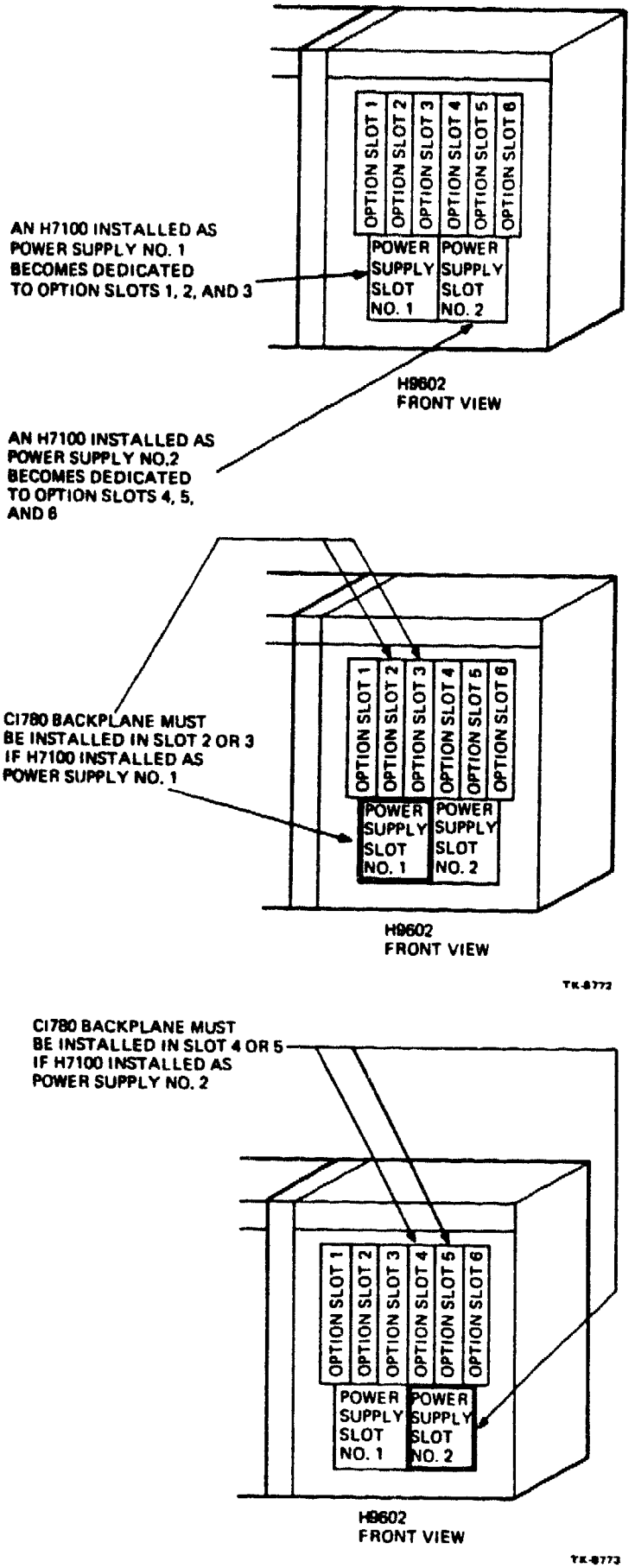

Figure 2-5 Expansion Cabinet Option Mounting Details

2.4.3 Relocating the System Far End Terminator (SFT)

From the back of the cabinet:

1. Remove and save the six 12" SBI jumper cables (P/N 1700087-01) connecting J1 through J6 of the System Far End Terminator (SFT) to J1 through J6 of the adjacent backplane to the right of the SFT.

NOTE
These cables will be used to connect the CI780 backplane assembly to the SFT in Section 2.5.

2. Disconnect the cable harness plugs from J7, J8, and J9 on the lower portion of the SFT.

3. Remove and save the ten screws that hold the SFT to the blank panel.

4. Remove the SFT from the blank panel.

5. Mount the SFT on a blank panel to the left of the 4" option slot that will contain the CI780 backplane assembly (Figure 2-5).

6. Secure the relocated SFT to the blank panel using the ten screws saved in step 3.

7. Connect plugs P7, P8, and P9 from the cabinet cable harness to J7, J8, and J9 on the SFT.

2.4.4 Mounting the CI780 Backplane Assembly

To mount the CI780 Backplane Assembly:

1. Remove the blank panel from the 4 inch option slot that will contain the backplane assembly (Figure 2-5).

   a. From the front, remove the four screws holding the blank panel to the bottom of the chassis.

   b. From the back, remove the two screws holding the blank panel to the top of the chassis.

   c. From the back, slide the blank panel out of the chassis.

2. Carefully slide the CI780 backplane assembly (P/N 7017654) into the empty slot from the back of the cabinet.

3. Secure the backplane assembly to the front and back of the chassis using four 8 × 32.

4. Locate the CI780 module utilization label (P/N 3618809-01) and remove its paper backing.

5. From the front, place the label on the inside of the left vertical cabinet channel (Figure 2-12).

2.5 CONNECTING THE CI780

Connect the CI780 components using the procedures in the following paragraphs. The procedure for configuring the CI780 jumpers and switches is described in Section 2.6.

2.5.1 Connecting the H7100 Power Supply

To connect the H7100 Power Supply:

1. Remove the exhaust plenum from the lower rear portion of the cabinet.

   a. At the upper corners of the plenum, loosen the two captive thumb screws holding the plenum mounting brackets to the cabinet braces.

   b. Lift the plenum up and toward the rear to release the pins holding it to the lower cabinet braces.

2. Locate the male end of the power supply AC power cable, and check that it is plugged into a switched outlet on the power controller (Figure 2-6).

3. Locate and connect the female end of the power cable into J1 on the front of the power supply (Figure 2-7).

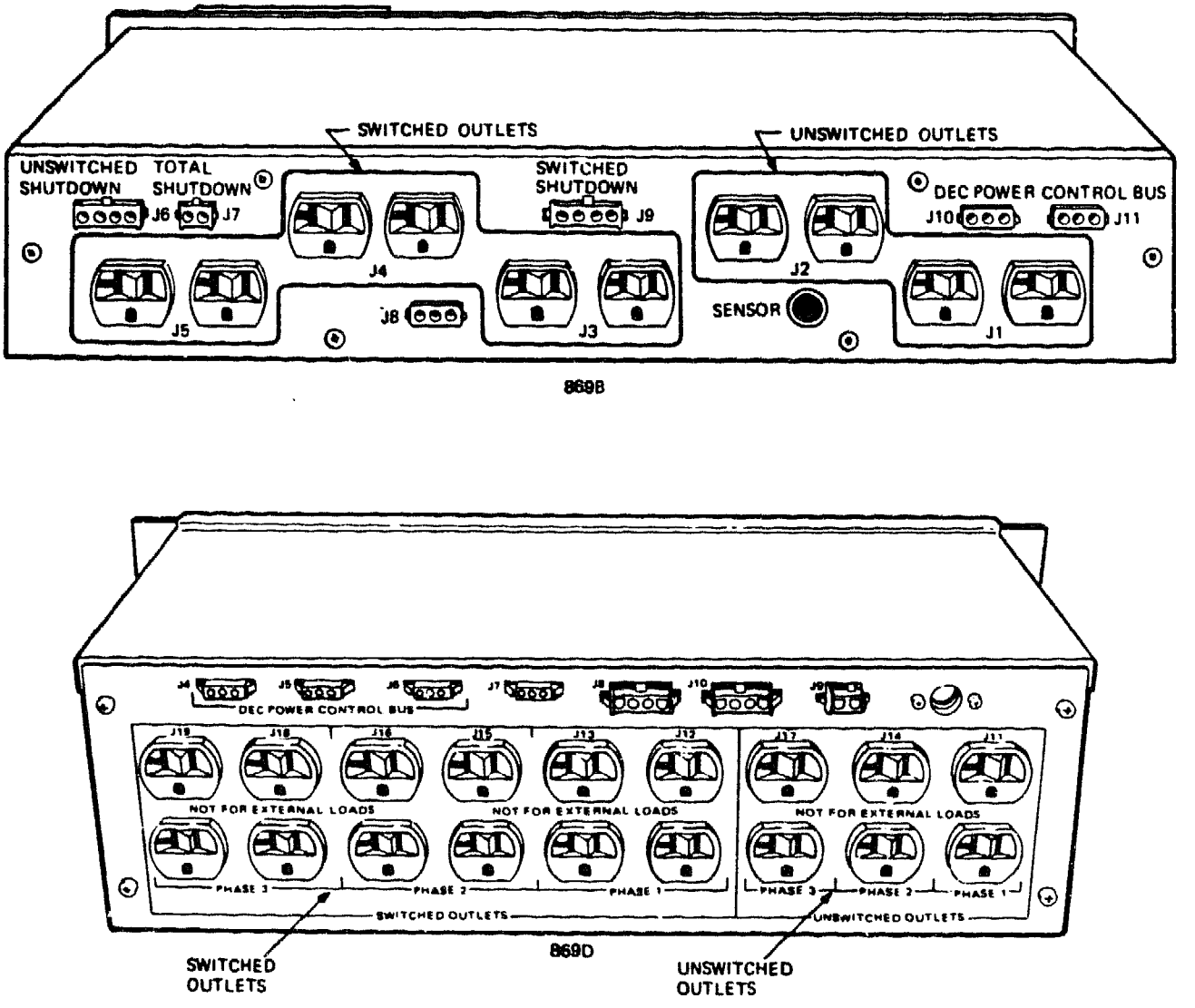

Figure 2-6 869B/869D Power Controllers (Rear Views)

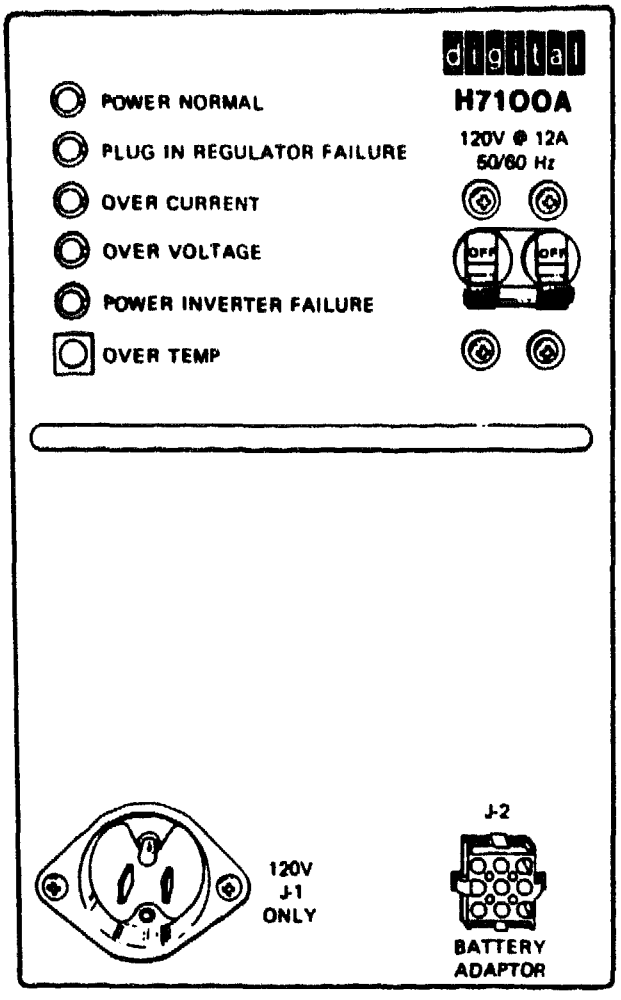

Figure 2-7 H7100 Power Supply (Front View)

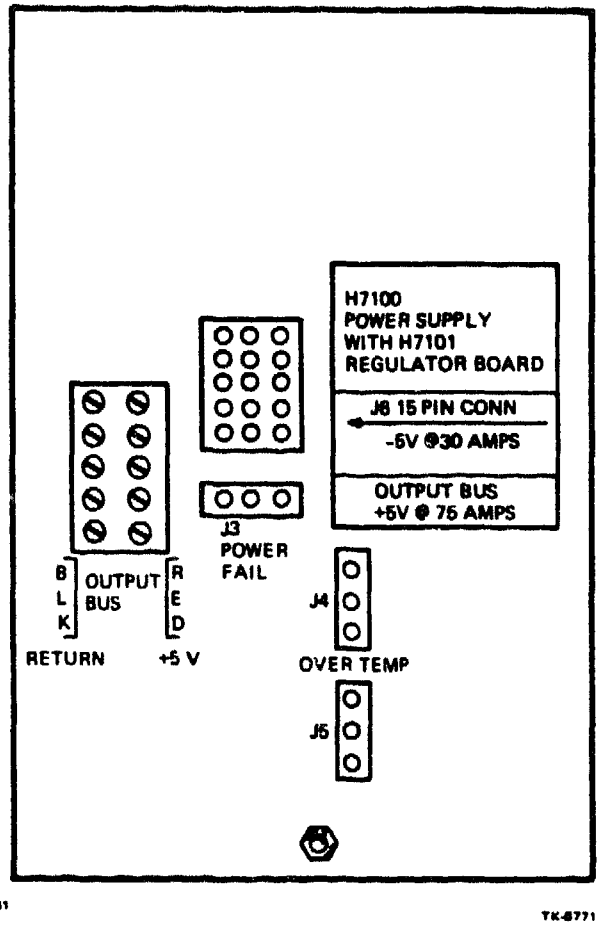

Figure 2-8 H7100 Power Supply (Rear View)

4. Perform the following cable connections at the back of the power supply (Figure 2-8).

   a. Secure the two BLACK cables (P/N 7014249-0L) from the backplane assembly to the RETURN terminals on the left side of the power supply output bus using two 10 × 32 screws and lock washers.

   b. Secure the two RED cables (P/N 7014530-0L) from the backplane assembly to the +5V terminals on the RIGHT side of the power supply output bus using two 10 × 32 screws and lock washers.

CAUTION

Incorrect connection of the +5V (red) and return (black) power cables will cause serious damage to the components on the CI780 modules.

   c. Connect P6 on the −5V cable (P/N 7018524-1F) to J6 (15-pin connector) on the power supply.

   d. Connect P1 on the AC LOW/DC LOW cable (P/N 7014212-0M) to J3 on the power supply.

e. Connect the OVER TEMP cable (P/N 7014213-0K) from J4 on the CI780 power supply to J4 on the next option power supply (if present).

f. Locate and connect the cabinet harness OVER TEMP cable (P/N 7014213-4A in CPU cabinet, P/N 7016001-4A in H9602-H expansion cabinet) to J5 on the power supply.

2.5.2 Connecting the CI780 Backplane Assembly

NOTE

All cable connections are made at the rear of the backplane.

To connect the CI780 Backplane Assembly (Figures 2-9 and 2-10):

1. Connect P16 on the −5 V cable (P/N 7018524-1F) from the power supply to J16 on the backplane.

2. Connect P2 on the AC LOW/DC LOW cable (P/N 7014212-0M) from the power supply to J13 on the backplane.

3. Locate and connect P3 (plug number may vary depending on the option slot) on the −5 V cabinet cable harness (P/N 7015073-00 in CPU cabinet, P/N 7015630-00 in H9602-H cabinet) to J15 on the backplane.

4. Connect six 4 inch SBI jumper cables (P/N 1700087-00) from J7 through J12 on the CI780 backplane to J1 through J6 on the adjacent backplane to the right of the CI780.

CAUTION

Always connect SBI jumper cables with the "SIGNAL" label on the outside of the loop.

NOTE

If the CI780 is the first option installed in an H9602-H cabinet, use the 18" SBI jumper cables (P/N 1700087-03) supplied with the H9602-H cabinet when performing step 4.

5. Connect the six 12 inch SBI jumper cables (P/N 1700087-01) removed in paragraphs 2.3.3 or 2.4.3, from J1 through J6 on the CI780 backplane to J1 through J6 on the SFT.

2.5.3 Connecting the CI780 TX/RX Bulkhead Cable Assemblies

Two sets of TX/RX bulkhead cable assemblies are supplied with the CI780: one set for signal path A (P/N 7018527-00), and the other for signal path B (P/N 7017527-01). These cables should be routed and connected from the back of the cabinet.

1. Mount the bulkhead connector plate of each cable assembly, from the inside, to the MASSBUS cutouts on the I/O panel at the bottom of the cabinet. Refer to Figure 2-11 (CPU cabinet) or Figure 2-12 (H9602-H expansion cabinet) for details.

   a. Secure the TX/RX B bulkhead connector plate to the first available cutout on the right side of the panel using four 6 × 32 screws.

   b. Secure the TX/RX A bulkhead connector plate to the next adjacent cutout on the left using four 6 × 32 screws.

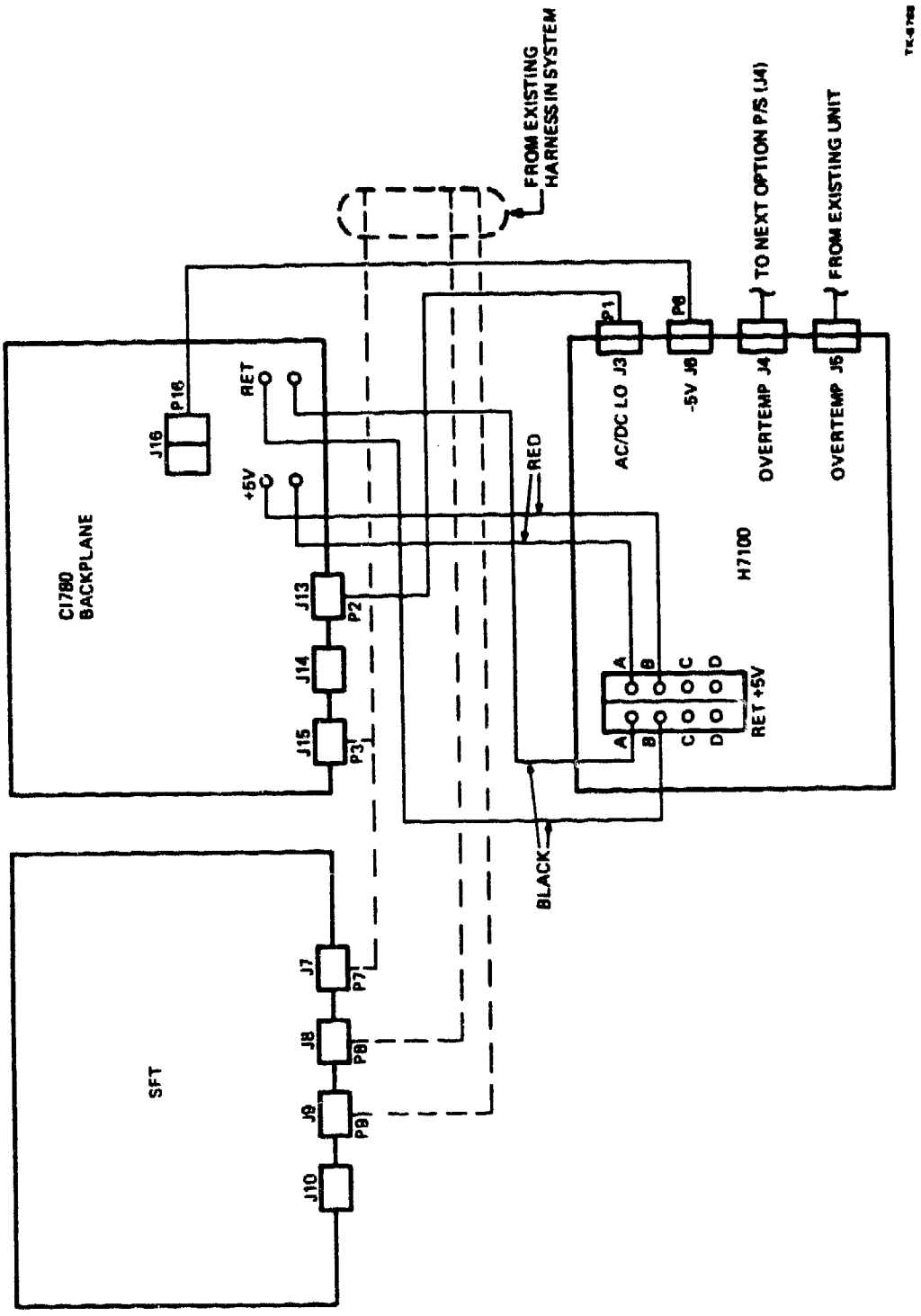

Figure 2-9 C1780 Power Connection Details

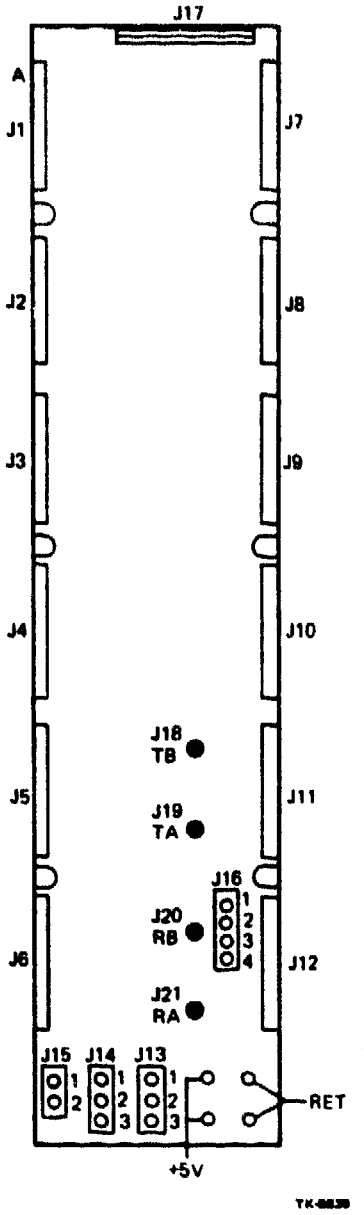

Figure 2-10 CI780 Backplane Connectors

2. Route the four coaxial cables up through the cabinet cable ways to the backplane. Take care to avoid any sharp bends, kinks, or twists in the cables (Figure 2-11 or 2-12).

3. Place a P-clamp over each cable, just behind the pin plug on the end, and carefully insert the plug into the proper jack on the backplane (Figure 2-10). Gradually push the cable plug into the jack until it is secured by the detent lock.

   a. Transmit B (TB) to J18 on the backplane.
   b. Transmit A (TA) to J19 on the backplane.
   c. Receive B (RB) to J20 on the backplane.
   d. Receive A (RA) to J21 on the backplane.

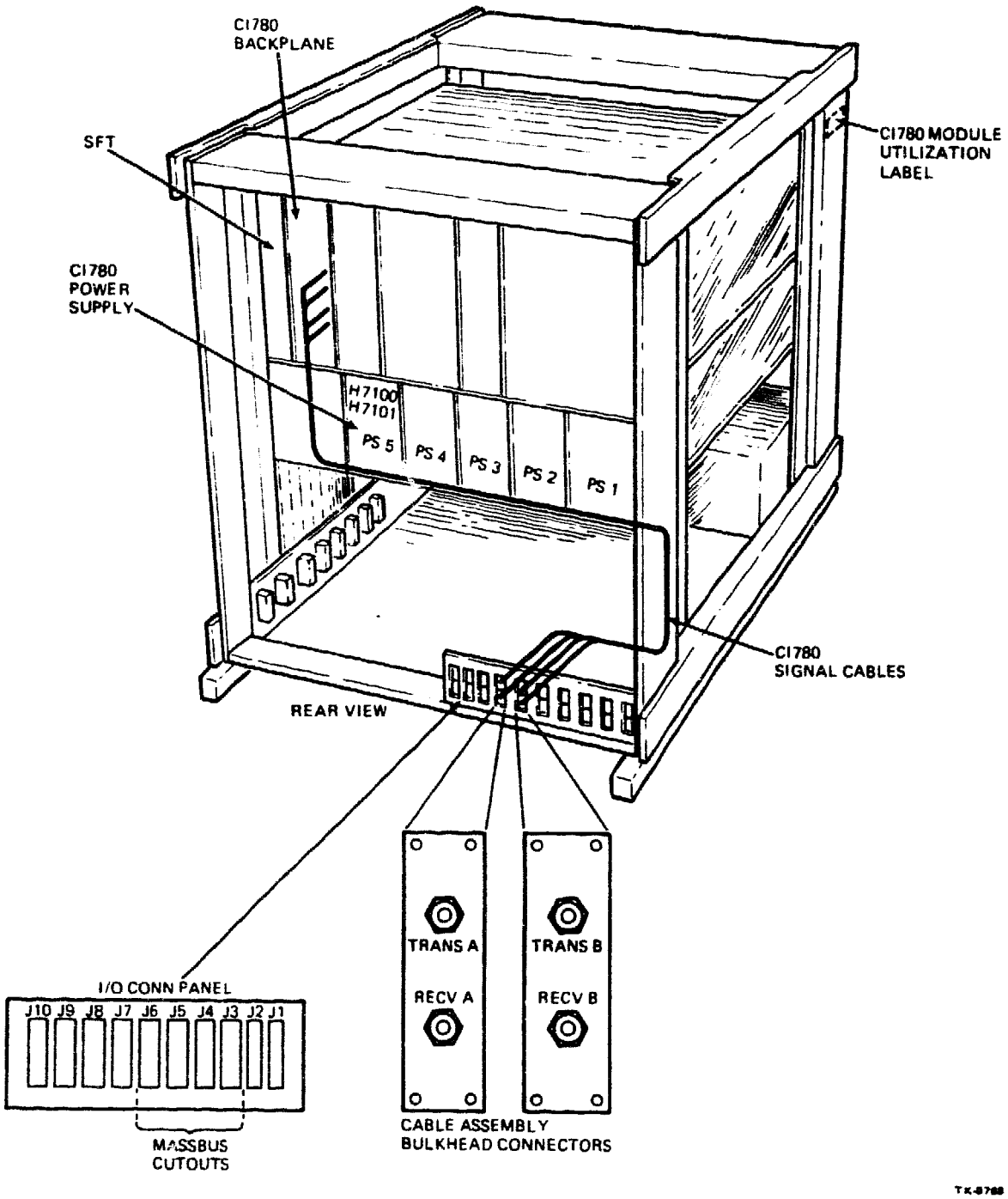

Figure 2-11 CPU Cabinet Cable Assembly Connection Details

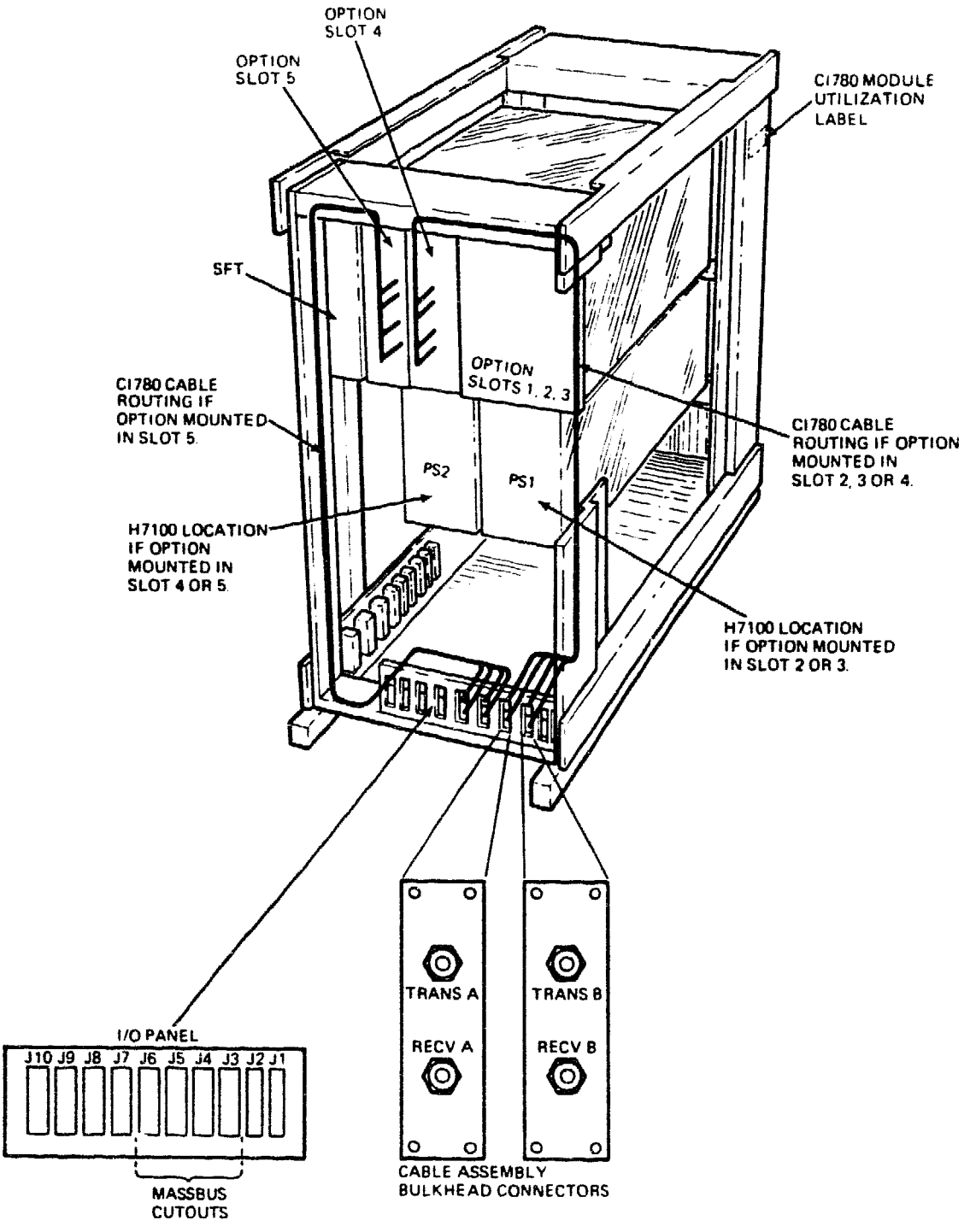

Figure 2-12 Expansion Cabinet Cable Assembly Connection Details

4. Secure the P-clamp on each cable to the plastic cable support with a 10 × 32 screw, washer, and nut (Figure 2-13).

5. Attach the exhaust plenum removed in paragraph 2.5.1 to the back of the cabinet.

2.6 CONFIGURING THE CI780 JUMPERS AND SWITCHES

There are two types of jumpers on the CI780 backplane:

- A row of seventeen jumpers on header jack J17 that are used to select various hardware options via jumper plugs
- An additional wirewrap jumper located on slot 1, row C to connect the SBI interface logic to the desired TR arbitration level

The CI780 is shipped with the backplane jumpers installed and slot C01 pins wirewrapped for a single cluster configuration. This consists of one CI780 installed per VAX-11/780 system, set-up as follows:

- SBI TR Arbitration Level - 14
- SBI BR Priority Level - 4

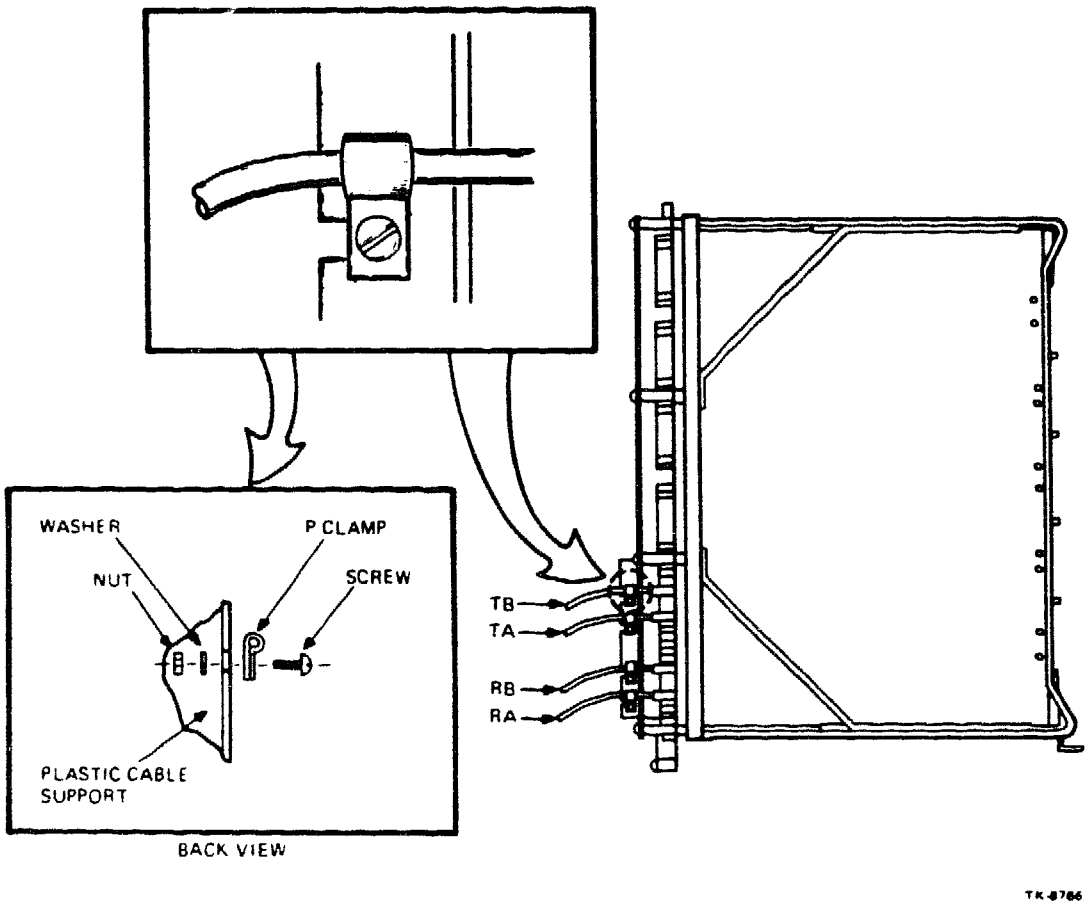

Figure 2-13 CI780 Backplane Cable Assembly Connection Details

2.6.1 Verifying the Backplane Jumper Configuration

To verify the Backplane Jumper Configuration (Figure 2-14):

1. Jumpers W2, W3, and W4 on J17 should be IN. All others should be OUT.
2. Pin C01-53 should be wirewrapped to pin C01-87.

NOTE

For additional information on the backplane jumpers, refer to Appendix A.

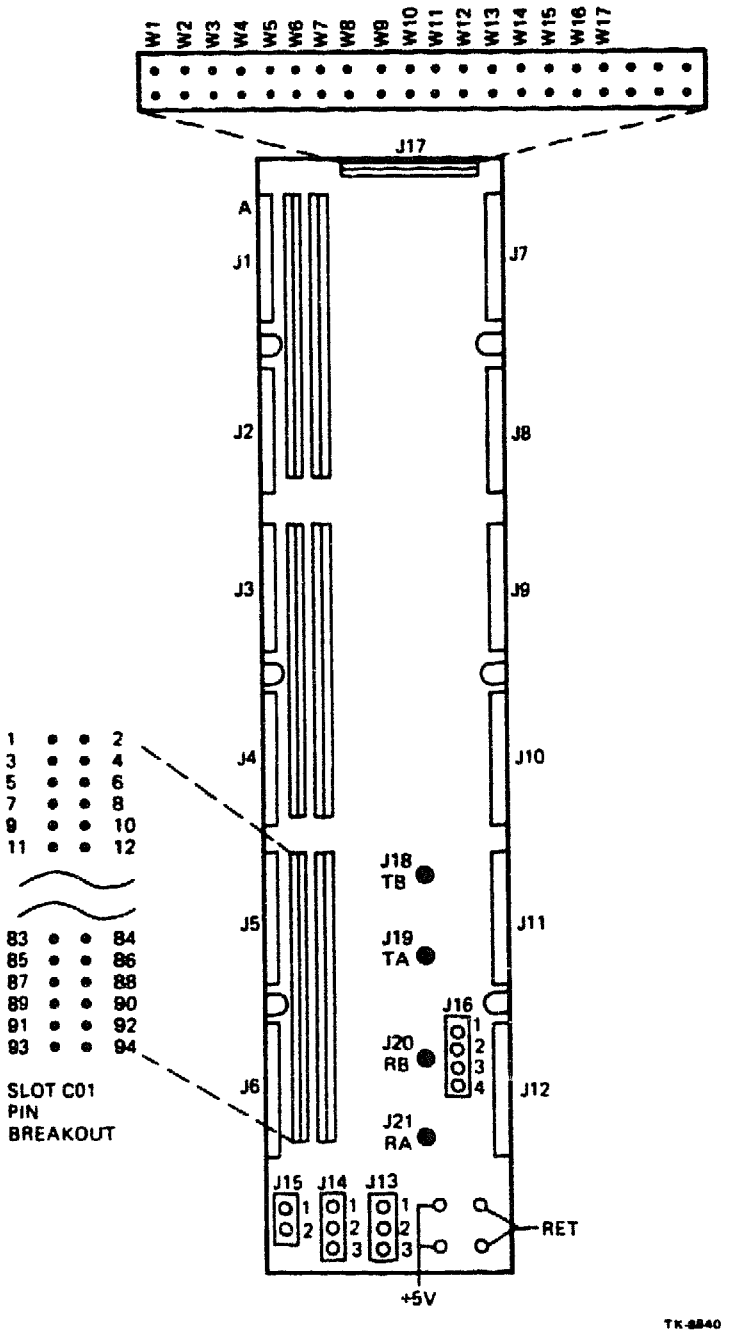

Figure 2-14 CI780 Backplane Jumper Pin Breakout

2.6.2 Configuring the Link Module Switches

The switches on the Link Interface Module (L0100) provide the system with a unique node address within a CI cluster. This address is typically a number from 0 to 15. To assign a node address, each of the two switch packs (S1 and S2) on the link module must be set to the binary value of the assigned number (Figure 2-15).

1. Assign the system a node address.

   a. For CI780 installations that create a new CI cluster, assign a node address within the range of the number of CI780s being installed.

   b. For CI780 installations that add a node to an existing CI cluster, determine the highest node address currently in use and assign the next higher sequential number.

CAUTION

Difficult to diagnose software failures will occur if two nodes in a cluster are assigned the same address.

2. Without removing the link module from the CI780 backplane, set S1 and S2 to the assigned address. The ON position of each switch represents a logic zero, and the OFF position a logic one (Table 2-1).

   a. Set S1-1 through S1-8 to the logic value of the assigned address.
   b. Set S2-1 through S2-8 to the logic value of the assigned address.

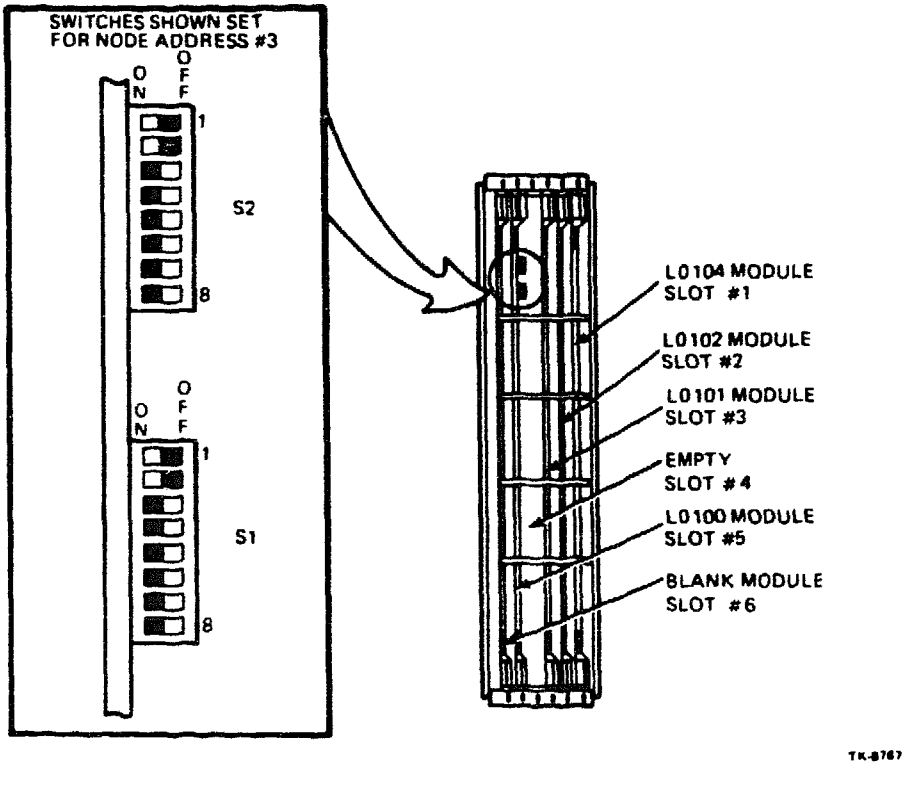

Figure 2-15 Link Module Switch Details

3. Locate the correct node address identification label and remove its paper backing. This label is part of a set (P/N 3619264-17) shipped with the SC008 Star Coupler.

NOTE
Refer to the SC008 Star Coupler User's Guide (EK-SC008-UG-001) for additional information.

4. Place the label at eye level on the outside of the rear door of the cabinet which houses the CI780.

Table 2-1 Node Address Switch Settings

	Node Address							
Node Number	**S8**	**S7**	**S6**	**S5**	**S4**	**S3**	**S2**	**S1**
0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
6	0	0	0	0	0	1	1	0
7	0	0	0	0	0	1	1	1
8	0	0	0	0	1	0	0	0
9	0	0	0	0	1	0	0	1
10	0	0	0	0	1	0	1	0
11	0	0	0	0	1	0	1	1
12	0	0	0	0	1	1	0	0
13	0	0	0	0	1	1	0	1
14	0	0	0	0	1	1	1	0
15	0	0	0	0	1	1	1	1

0 = ON
1 = OFF

CHAPTER 3
ACCEPTANCE TESTING

3.1 INTRODUCTION

Acceptance testing of the CI780 is basically a two-step procedure:

1. The newly installed CI780 is operationally verified stand-alone (not connected to the CI).

2. The system is connected to the Computer Interconnect and operationally verified as a node within the CI cluster.

Stand-alone verification consists of running the system microdiagnostics, which contain CI780 support, followed by the CI780 Level 3 diagnostics.

Operational verification of the system within the CI Cluster consists of:

1. Connecting the node to the CI and verifying the connection by running the CI Exerciser (CIE) program (EVXCI).

2. Running a copy of the User Environmental Test Package (UETP) on the node under test.

NOTE
If all VAX nodes within a CI cluster are being tested, UETP must be run on each node.

3.2 CI780 CHECK-OUT PROCEDURE (STAND-ALONE)

To verify the CI780 installation:

1. Power-up the system.
2. Run the VAX-11/780 microdiagnostics.

To determine if the CI780 is functioning properly, the following Level 3 diagnostic programs must be run.

- ESCGA - CI780 Repair Level Diagnostic 1
- ESCGB - CI780 Repair Level Diagnostic 2
- ESCGC - CI780 Repair Level Diagnostic 3
- ESCGD - CI780 Repair Level Diagnostic 4

Before loading the diagnostics, make the following connections to the I/O connector panel at the back of the cabinet:

1. Using one of the attenuator pads (P/N 1219907-01) and two of the SC008 modularity cables (P/N 7018530-00) supplied in the CI780 CD Kit, connect the TRANSMIT A bulkhead connection to the RECEIVE A bulkhead connection.

2. Perform the same connection for path B using the other attenuator pad and two SC008 modularity cables from the CI780 CD Kit to connect TRANSMIT B to RECEIVE B.

Use the following procedure to load the diagnostic programs into the system.

1. Put the VAX-11/780 in a stable, halted condition.

2. Initialize and unjam the SBI via the console commands:

   ))) INIT
   ))) UNJAM

3. Load the Diagnostic Supervisor, ESSAA.EXE, via the command BOOT (or LOAD ESSAA.EXE/ST:FE00), from the diskette, or BOOT it from the system disk.

4. Load the diagnostic program using LOAD ESCGA.

5. Attach the device to be tested:

   DS) ATTACH CI780 SBI UNIT# (PAA0) TR (14) BR (4) NODE (0)

6. Select the unit to be tested via the command SELECT (UNIT #).

7. Set any desired supervisor flags.

8. Start the diagnostic program.

NOTE

Diagnostics ESCGB and ESCGD contain manual intervention test sections. To run them once the diagnostic is loaded, type

DS) START/SECTION:MANUAL

and perform the required manual actions listed by the diagnostic printout.

When running the diagnostics for the first time after installing the CI780, run them in ascending order from ESCGA to ESCGD and include the manual intervention test sections.

9. After successfully running the four diagnostics, remove the attenuator pads and modularity cables from the I/O panel bulkhead connectors.

10. Locate the CI bus cables (BNCIA-XX) and connect one end of each cable to the appropriate bulkhead connector.

NOTE

DO NOT unroll or route the CI bus cables at this time.

11. Connect the two attenuator pads to the free ends of the CI cables. Be sure to connect TRANSMIT A to RECEIVE A and TRANSMIT B to RECEIVE B.

12. Run the EXTLOOP section of diagnostic ESCGD five times to test the CI cables prior to routing and connecting them to the SC008 by typing:

    DS) START/SECTION:MANUAL/PASS:5

13. Disconnect the CI bus cables from the bulkhead and remove the two attenuators.

14. Carefully unroll, route, and connect the CI bus cables to the SC008 and the CI780 bulkhead. Refer to Section 2.4 of the *SC008 Star Coupler User's Guide* for the cable routing procedure.

15. Rerun the EXTLOOP section of diagnostic ESCGD five times to verify the cable connections.

3.3 ON-LINE TESTING OF THE CI780 AND THE CI CLUSTER

1. Use the procedure described in Appendix C to update SYE with the SYE update kit supplied in the CI780 software box (BX-Q3113-TE) and the console floppy diskette with the CI780 microcode.

2. Run the CI Exerciser program, EVXCI. Refer to the procedure Installing and Running the CI Exerciser Software (AV-T311A-TE) supplied in the CI780 software box for operating instructions.

3. Run UETP on each VAX node where a CI780 has been installed. Refer to the *VAX/VMS UETP User's Guide* (AA-D643C-TE) for operating instructions.

APPENDIX A
BACKPLANE JUMPERS

A.1 LONG TIMEOUT (W1)

IN= 2048 SBI cycles
OUT= 512 SBI cycles

A.2 TR ARBITRATION LEVEL (W2, W3, W4, W7 and C01-53 Wirewrap)

TR No.	W2	W3	W7	W4	C01-53 TO
1	OUT	OUT	OUT	OUT	C01-57
2	OUT	OUT	OUT	IN	C01-63
3	OUT	OUT	IN	OUT	C01-62
4	OUT	OUT	IN	IN	C01-65
5	OUT	IN	OUT	OUT	C01-69
6	OUT	IN	OUT	IN	C01-71
7	OUT	IN	IN	OUT	C01-73
8	OUT	IN	IN	IN	C01-75
9	IN	OUT	OUT	OUT	C01-77
10	IN	OUT	OUT	IN	C01-81
11	IN	OUT	IN	OUT	C01-83
12	IN	OUT	IN	IN	C01-85
13	IN	IN	OUT	OUT	C01-86
14	IN	IN	OUT	IN	C01-87
15	IN	IN	IN	OUT	C01-88

NOTE
TR No. 0 is reserved as the HOLD line

A.3 BR INTERRUPT PRIORITY LEVEL (W5 and W6)

BR No.	W6	W5
4	OUT	OUT
5	OUT	IN
6	IN	OUT
7	IN	IN

A.4 PANIC MODE (W8)

IN = Panic Mode Disabled
OUT = Panic Mode Enabled

A.5 BOOT TIMER (W9, W10, W12, W13)

Time (Sec)	W9	W13	W10	W12
1500	OUT	OUT	OUT	OUT
0000	OUT	OUT	OUT	IN
0100	OUT	OUT	IN	OUT
0200	OUT	OUT	IN	IN
0300	OUT	IN	OUT	OUT
0400	OUT	IN	OUT	IN
0500	OUT	IN	IN	OUT
0600	OUT	IN	IN	IN
0700	IN	OUT	OUT	OUT
0800	IN	OUT	OUT	IN
0900	IN	OUT	IN	OUT
1000	IN	OUT	IN	IN
1100	IN	IN	OUT	OUT
1200	IN	IN	OUT	IN
1300	IN	IN	IN	OUT
1400	IN	IN	IN	IN

A.6 RESERVED (W11)

A.7 DISABLE ARBITRATION (W14)

IN= Disable Normal Arbitration
OUT= Allow Normal Arbitration

A.8 EXTEND HEADER/TRAILER (W15)

IN= Extended Header/Trailer
OUT= Normal Header/Trailer

A.9 ALTER DELTA TIME (W16)

IN= Long Delta Time
OUT= Short Delta Time

A.10 EXTEND ACKNOWLEDGEMENT TIMEOUT (W17)

IN= Long Timeout
OUT= Short Timeout

APPENDIX B
CI780 REGISTER SUMMARY

B.1 SBI REGISTER ADDRESS ASSIGNMENT

The TR number selected for the CI780 determines which SBI addresses are assigned to the registers. To find the actual address of a register, add the byte offset specified for the desired register to the base address specified by TR number in Table B-1. The normal configuration for the CI780 is TR14.

Table B-1 SBI Address Assignment

TR Number (Base 10)	30-Bit Physical Address (Hex)	28-Bit SBI Address (Hex)
1	2000 2000	800 0800
2	2000 4000	800 1000
3	2000 6000	800 1800
4	2000 8000	800 2000
5	2000 A000	800 2800
6	2000 C000	800 3000
7	2000 E000	800 3800
8	2001 0000	800 4000
9	2001 2000	800 4800
10	2001 4000	800 5000
11	2001 6000	800 5800
12	2001 8000	800 6000
13	2001 A000	800 6800
14	2001 C000	800 7000
15	2001 E000	800 7800

B.1.1 SBI Configuration Register (CNFGR)
Byte offset = 0 Hex

The CNFGR contains the SBI fault bits, port status bits, error bits, and the adaptor code for the CI780. This register is writable by longword only. It can be read by byte, word or longword reference. Any other mode of access results in error confirmation by the CI780. Figure B-1 illustrates the register format. Each bit is described in Table B-2.

B.1.2 Port Maintenance Control and Status Register (PMCSR)
Byte offset = 4 or 10 Hex

The PMCSR contains the port hardware error flags, interrupt and port initialization control bits. Figure B-2 illustrates the register format. Each bit is described in Table B-3.

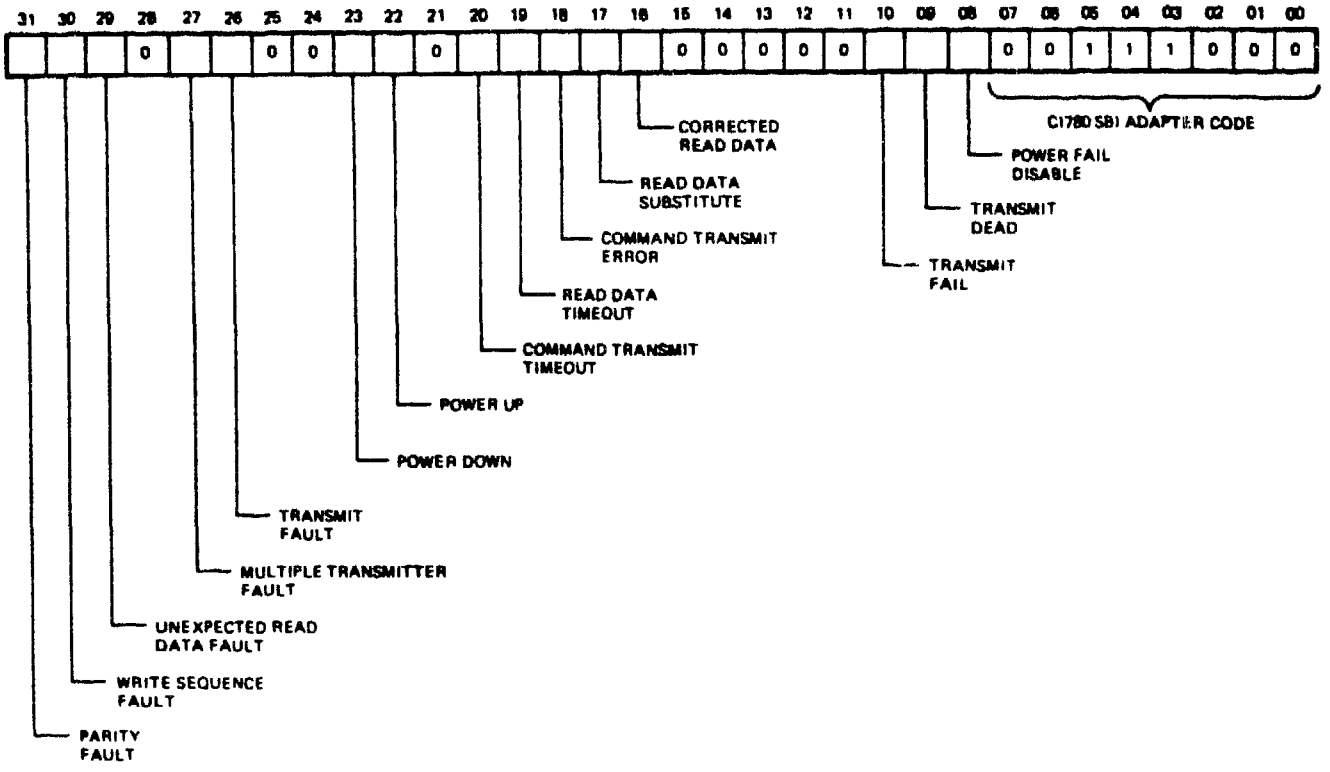

Figure B-1 SBI Configuration Register

Table B-2 SBI Configuration Register

Bit	Function	Description
31	Parity Fault (PAR FLT)	Set when the port has detected an SBI parity error.
30	Write Sequence Fault (WSQ FLT)	Set when the port receives a Write Mask or Interlock Write Mask command that is not immediately followed by the expected write data.
29	Unexpected Read Data (URD FLT)	Set when the port received read data and had not issued a Read Mask, Extended Read or Interlock Read Mask command.
28	Reserved	Read as zero.
27	Multiple Transmitter Fault (MXT FLT)	Set when port is transmitting information on the SBI and the ID bits transmitted do not match the ID bits received.
26	Transmit Fault (XMT FLT)	Set when the CI780 is the transmitter that asserts the SBI Fault line.
25:24	Reserved	Read as zero.
23	Power Down (PDN)	Indicates that the port is powering down. 1. Set by assertion of ACLO when the port is in the uninitialized state. 2. Set by microcode control when the port is in the initialized state. 3. Cleared by writing a 1 to it, or when the Power Up bit sets.

Table B-2 SBI Configuration Register (Cont)

Bit	Function	Description
22	Power Up (PUP)	Indicates that the port has powered up. 1. Set by the negation of AC LO. 2. Cleared by writing a 1 to it, or when the Power Down bit sets.
21	Reserved	Read as zero.
20	Command Transmit Timeout (CXTMO)	Set when no confirmation is received for a port-initiated SBI command transfer within 512 or 2048 SBI cycles (102.4 or 409.6 μs). This count is jumper selectable on the CI780 backplane.
19	Read Data Timeout (RDTO)	Set when the port initiates a SBI read command and receives no data within 512 SBI cycles (102.4 μs).
18	Command Transmit Error (CXTER)	Set when the port receives an SBI error confirmation for a port-initiated SBI command.
17	Read Data Substitute (RDS)	Set when the response to a port-initiated read command contains a read data substitute tag.
16	Corrected Read Data (CRD)	Set when the response to a port-initiated read command contains a corrected read data tag.
15:11	Reserved	Read as zero.
10	Transmit Fail (T FAIL)	This bit is the input to the SBI FAIL driver and is set by the microcode.
09	Transmit Dead (T DEAD)	This bit is the input to the SBI DEAD driver and is set by the microcode.
08	Power Fail Disable (PFD)	When set disables gateing Fail or Dead to the SBI. This enables the diagnostic to test the ability to generate these signals without affecting the SBI.
07:00	Adapter Code	The CI780 adapter code equals 38 hex.

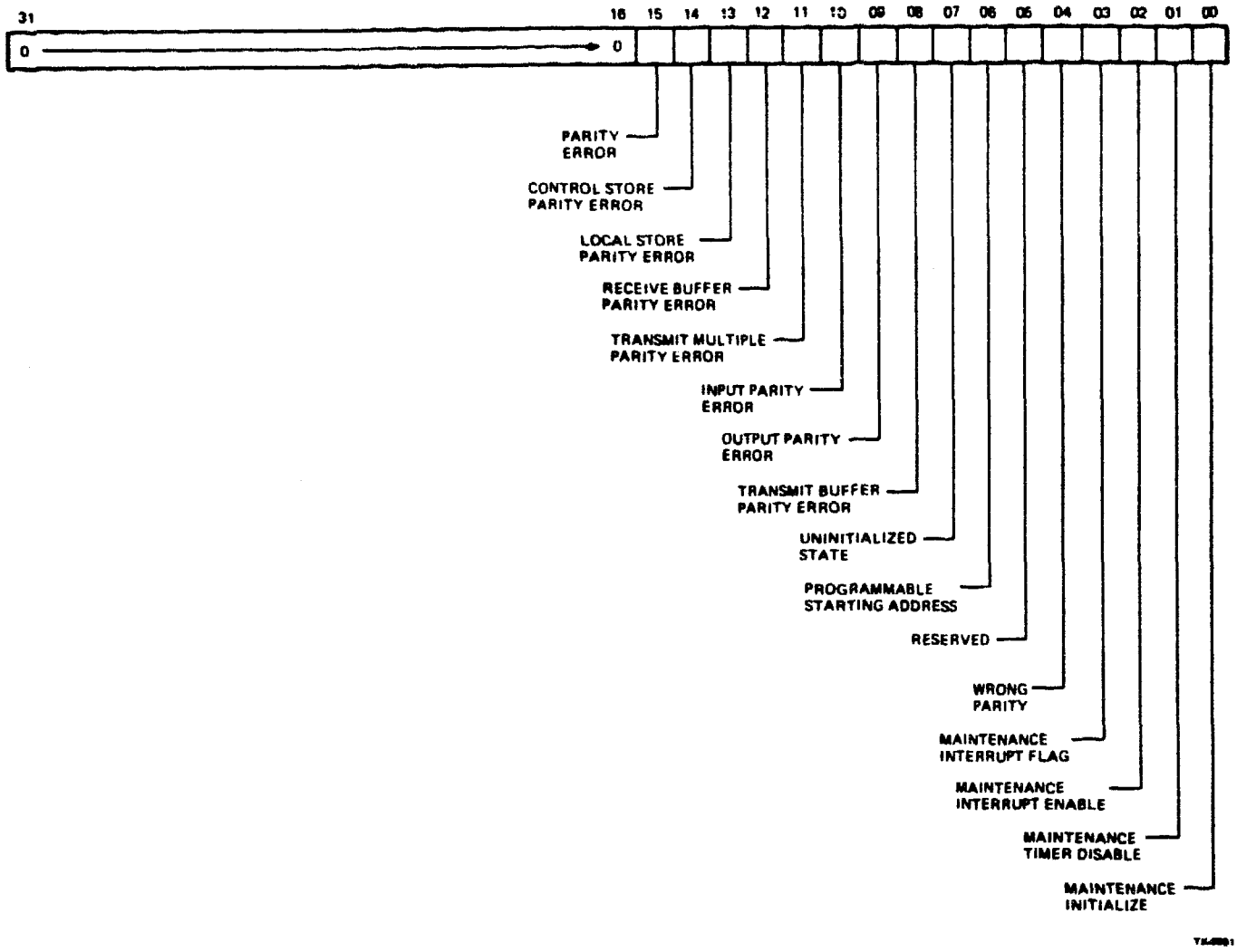

Figure B-2 Port Maintenance Control and Status Register

Table B-3 Port Maintenance Control and Status Register

Bit	Function	Description
31:16	Reserved	Read as zero.
15	Parity Error (PE)	Set if any one or more of bits 8 through 14 are set.
14	Control Store Parity Error (CSPE)	Set by microcode when a parity error is detected in the control store RAM or PROM. Not used when the control store is accessed from the SBI.
13	Local Store Parity Error (LSPE)	Set by microcode when a parity error is detected in the local store or VCDT. Not used when the local store is accessed from the SBI.
12	Receive Buffer Parity Error (RBPE)	Set when a parity error is detected on the data path board while reading a receive buffer or transmit buffer (for loopback test) located on the packet buffer board.

Table B-3 Port Maintenance Control and Status Register (Cont)

Bit	Function	Description
11	Transmit Multiple Parity Error (XMPE)	Set when the link module detects a parity error in the data being transmitted.
10	Input Parity Error (IPE)	Set when a parity error is detected on a data transfer from the SBI transceivers to the Data Path board.
09	Output Parity Error (OPE)	Set when a parity error is detected on a data transfer from the Data Path Board to the SBI transceivers.
08	Transmit Buffer Parity Error (XBPE)	Set when a parity error is detected while the link board is unloading the transmit buffer.
07	Unitialized State (UNIN)	Set when the port is in the Uninitialized state. The microcode is stopped and the port will not respond to CI traffic. This bit is read-only and is set by DEAD, PMCSR MIN, or PSR MTE.
06	Programmable Starting Address (PSA)	When set, the microcode will start at the address loaded in MADR when PICR is written with a "1" or a boot timeout occurs. When clear, the microcode will start at address 000 (in the PROM area). PSA is read/write and is cleared by DEAD or setting the MIN bit.
05	Reserved	
04	Wrong Parity (WP)	Set to generate and check for even parity on the Data Path board IBUS.
03	Maintenance Interrupt Flag (MIF)	When set, an interrupt has occurred and the PSR register is valid. This bit allows the diagnostic to operate the port with interrupts to the SBI disabled.
02	Maintenance Interrupt Enable (MIE)	Interrupts are enabled when this bit is set. This bit is set by DC LO or by writing MIE with a one. It is cleared by setting the PMCSR MIN bit, SBI UNJAM, or by writing MIE with 0.
01	Maintenance Timer Disable (MTD)	When set, the boot and sanity timers are disabled and cannot cause an interrupt. When clear, the timers are enabled.
00	Maintenance Initialize (MIN)	When set, an initialize signal is generated that clears all port errors and leaves the port in the uninitialized state. Setting this bit clears the PMCSR MIE bit. MIN is write-only and always reads as a zero.

B.1.3 Maintenance Address Register (MADR) Byte Offset = 14 Hex

The MADR is loaded with the address to be referenced in the port control store when initially loading the microcode or specifying the microcode starting address. Figure B-3 illustrates the register format. Each bit is described in Table B-4.

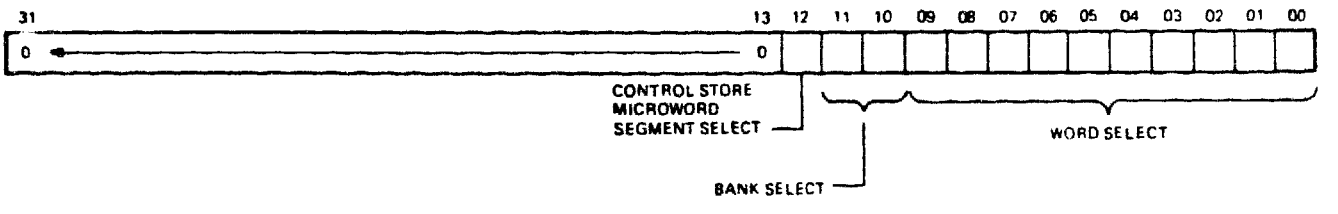

Figure B-3 Maintenance Address Register

Table B-4 Maintenance Address Register

Bit	Function	Description
31:13	Reserved	Read as zero.
12	A12	Selects a segment of the control store word. 0 = control store bits (31:00) 1 = control store bits (47:32)
11:10	A11:A10	Selects a bank within the control store.
9:0	A9:A0	Selects a word within the selected bank.

A11	A10	Bank Selected
0	0	0 (000-3FF PROM)
0	1	1 (400-7FF RAM)
1	0	2 (800-BFF RAM)
1	1	3 (C00-FFF Reserved)

B.1.4 Maintenance Data Register (MDATR) Byte Offset = 18 Hex

The MDATR is used to access the contents of the control store location pointed to by the Maintenance Address Register. This register is used to initially load the port microcode. The MDATR register is both read and write accessible, bit is valid only when the port is in the uninitialized state. Figure B-4 illustrates the register format.

B.1.5 Port Status Register (PSR) Byte Offset = 900 Hex

NOTE

The PSR is used by the port driver software and is only valid when the operational port microcode is loaded and running.

Figure B-4 Maintenance Data Register

The PSR displays the cause of interrupts from the CI780. The PSR is read-only and writing to it can cause false interrupt indications to the Port Driver. Figure B-5 illustrates the register format; each bit is described in Table B-5.

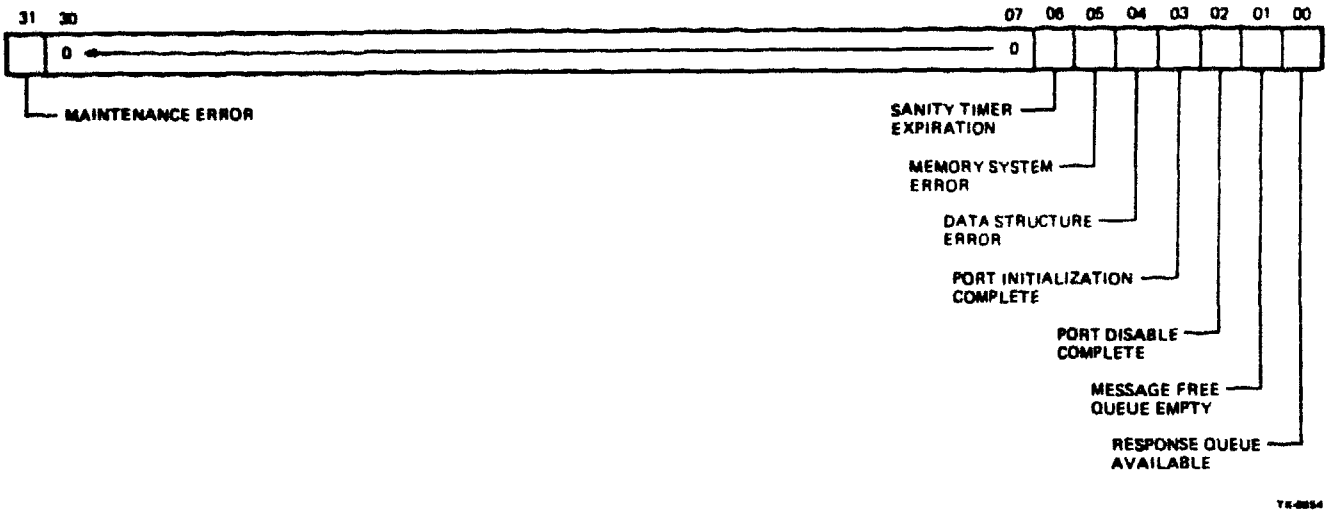

Figure B-5 Port Status Register

Table B-5 Port Status Register

Bit	Function	Description
31	Maintenance Error (MTE)	Set when the Port has detected an internal hardware failure. The exact error can be determined by reading the PMCSR and CNFGR. When set: 1. Port enters uninitialized state 2. Microcode is halted 3. An interrupt is generated (PSR ⟨0:7⟩ are invalid)
30:07	Reserved	Read as zero
06	Sanity Timer Expiration (SE)	Set when the Sanity or Boot timer has expired and the Port has entered the Uninitialized/Maintenance state.
05	Memory System Error (MSE)	Set when the Port has detected an uncorrectable data or non-existent memory error while accessing SBI memory. MSE can set as a result of CXTMO, RDTO, CXTER or RDS in the CNFGR register. The PFAR register displays further information.
04	Data Structure Error (DSE)	Set when the port encounters an error in a port data structure. Further information can be found in the PFAR register.
03	Port Initialization Complete (PIC)	When set indicates that the port has completed internal initialization and is in the Disabled or Disabled/Maintenance state.
02	Port Disable Complete (PDC)	When set the Port is disabled and ceases to process the command queues. The port will also cease to respond to incoming CI transmissions (except maintenance class if enabled). The port is in the Disabled or Disabled/Maintenance state.
01	Message Free Queue Empty (MFQE)	Set when Port attempted to remove an entry from the Message Free Queue and found it empty.
00	Response Queue Available (RQA)	Set when port has inserted an entry onto an empty response queue.

B.1.6 Port Failing Address Register (PFAR)
Byte Offset = 938 Hex

NOTE

This register is used by the port driver software and is only valid when the operational port microcode is loaded and running.

The PFAR register contains the memory address at which a failure occured after a MSE or DSE interrupt, or, after a response with buffer memory system error status. This address may be the exact address, an address in the same page as the failing address, or, in the case or DSE interrupts, and address in some part to the data structure. For DSE interrupts, PFAR contains a virtual address or offset; for MSE interrupts and buffer memory system errors, the PFAR contains a physical address. PESR may contain further information about the contents of PFAR for DSE interrupts. Figure B-6 illustrates the register format.

Figure B-6 Port Failing Address Register

B.1.7 Port Error Status Register (PESR)
Byte Offset = 93C Hex

NOTE

This register is used by the port driver software and is only valid when the operational port microcode is loaded and running.

The PESR register indicates which type of error resulted in a DSE interrupt. This register is read only by the port driver and is valid after a DSE interrupt. Table B-6 describes the contents of this register.

Table B-6 Port Error Status Register

Error	Description	Hex Code	PFAR Contents
SYS_VA_FRM	Illegal system virtual address format (Bits (31:30) ⟨⟩ 10)	1	Virtual address
NX_SYS_VA	Nonexistent system virtual address (VA(29:9))= SPT_LEN)	2	Virtual address
INV_SYS_PTE	Invalid system PTE (Bits (31,26,22) ⟨⟩ 1XX,000, or 001)	3	Virtual address (being mapped)
INV_BUF_PTE	Invalid buffer PTE (Bits (31,26,22) ⟨⟩ 1XX,000,001)	4	PTE virtual address
NX_GLBL_SVA	Nonexistent system global virtual address (GPXT)= GPT_LEN)	5	Virtual address

Table B-6 Port Error Status Register (Cont)

Error	Description	Hex Code	PFAR Contents
NX_GLBL_VA	Nonexistent buffer global virtual address (GPTX)= GPT_LEN)	6	PTE virtual address
INV_SGLBL_PTE	Invalid system global PTE PTE ((31,26,22) () 1XX or 000)	7	Virtual address
INV_BGLBL_PTE	Invalid buffer global PTE PTE ((31,26,22) () 1XX or 000)	8	PTE virtual address
INV_SGPTE_MAP	Invalid system global PTE mapping. System virtual address of system global PTE is globally mapped.	9	Virtual address
INV_BGPTE_MAP	Invalid buffer global PTE mapping. System virtual address of buffer global PTE is globally mapped.	A	PTE virtual address
Q_INTL_FAIL	Queue interlock retry failure. Interlock was tested and found locked.	B	Queue head
ILL_Q_ALIGN	Illegal queue offset alignment (FLINK (2:1) () 0 or BLINK (2:1) () 0)	C	Queue head virtual address
ILL_PQB_FRM	Illegal PQB format. A field of the PQB specified to be MBZ was found to be non-zero.	D	Field offset in PQB in bytes
REG_PROT_VIOL	Register protocol violation. Register was written with wrong value or under wrong conditions.	E	Register byte offset from device base address

B.1.8 Port Parameter Register (PPR)
Byte Offset = 940 Hex

NOTE

This register is used by the port driver software and is only valid when the operational port microcode is loaded and running.

The PPR is set up by microcode during the port initialization process and is valid in any state except the uninitialized state. This register displays the port number. Figure B-7 illustrates the register and Table B-7 describes the contents.

B.1.9 Port Initialize Control Register (PICR)
Byte Offset = 924 Hex

The driver initializes the port and starts execution of the microcode by writing a 1 into bit (0) of the PICR. Figure B-8 illustrates the register format.

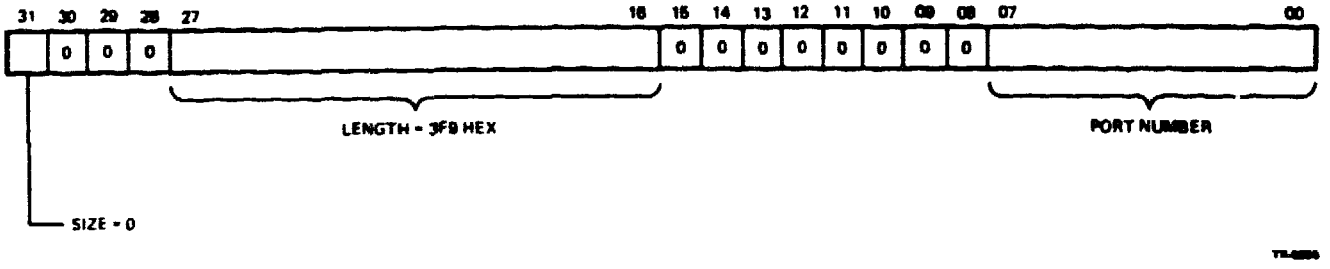

Figure B-7 Port Parameter Register

Table B-7 Port Parameter Register

Bit	Function	Description
31	Size	Initialized to zero, indicates 16 nodes maximum on the CI.
30:28	Reserved	Read as zero.
27:16	Length	Indicates size of internal buffers and is preset to 3F9 hex.
15:8	Reserved	Read as 0.
07:0	Port Number	Indicates the CI node number selected by the switches on the ILI board.

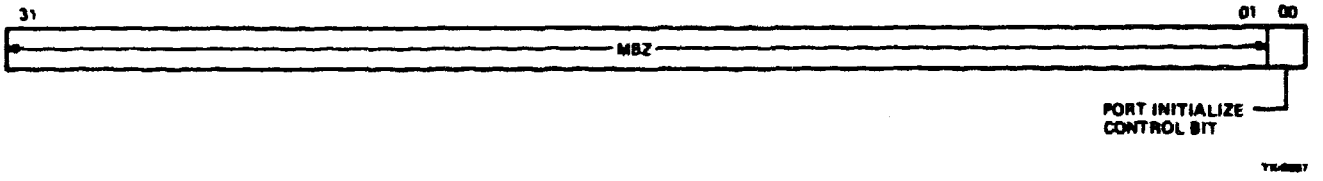

Figure B-8 Port Initialize Control Register