

BA11-L mounting box technical manual

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# BA11-L mounting box technical manual

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# CONTENTS

CHAPTER 1	CHARACTERISTICS AND SPECIFICATIONS
1.1	GENERAL1-1
1.2	PHYSICAL CHARACTERISTICS OF THE BA11-L1-2
1.3	H777 POWER SUPPLY1-6
1.4	H775A BATTERY BACKUP UNIT1-11
1.5	REMOTE POWER CONTROL
CILL DTED A	
CHAPTER 2	BACKPLANE CONFIGURATIONS AND INSTALLATION INFORMATION
2.1	GENERAL
2.2	PHYSICAL DESCRIPTION
2.3	ELECTRICAL DESCRIPTION
2.3.1	Non-Processor Grant (NPG) Line2-7
2.3.2	Bus Grant (BG) Lines2-7
2.4	POWER HARNESŚ2-8
2.5	INSTALLATION
2.5.1	Backplane Installation
2.5.2	Electrical Requirements
CHAPTER 3	H777 POWER SUPPLY
3.1	GENERAL
3.2	H777 PHYSICAL DESCRIPTION
3.3	H777 FUNCTIONAL DESCRIPTION
3.4	DETAILED DISCUSSION
3.4.1	Raw DC Circuit
3.4.2	MOS Regulator (Part 5411601)3-5
3.4.2.1	Functional Description
3.4.2.2	Master Clock
3.4.2.3	±15B Circuit Detailed Description
3.4.2.4	+5B Circuit Detailed Description
3.4.3	Core Regulator (Part 5411599)
3.4.3.1	Functional Description
3.4.3.2	+20 V Circuit Detailed Description
3.4.3.3	-5 V Circuit Detailed Description
3.4.4	+5 V Regulator (Parts 7011073 and 7012909)3-32
3.4.4.1	Functional Description
3.4.4.2	+5 V Circuit Detailed Description
3.4.4.3	Power Sequence Control Circuit Detailed Discussion
3.4.4.4	Battery Monitor Circuit
3.4.4.5	Boot Enable Circuit
3.4.4.6	Line Time Clock (LTC) Circuit (Print Set Drawing 35411597-0-1)3-49

# **CONTENTS (CONT)**

#### CHAPTER 4 H775A BATTERY BACKUP UNIT

•

4.1	GENERAL	4-1
4.2	PHYSICAL DESCRIPTION	4-1
4.3	FUNCTIONAL DESCRIPTION	4-3
4.4	DETAILED CIRCUIT DESCRIPTION	4-5
4.4.1	Voltage Boost Circuit	4-5
4.4.2	Regulator Circuit	4-5
4.4.3	Battery Charge Rate Status and Control	
4.4.4	Battery Discharge Switch and Control	
4.4.5	Battery Discharge Limit Circuit	

# CHAPTER 5 MAINTENANCE

5.1	GENERAL	5-1
5.2	PREVENTIVE MAINTENANCE PHYSICAL INSPECTION	5-1
5.3	CORRECTIVE MAINTENANCE	5-2
5.3.1	Introduction	5-2
5.3.2	Power Supply (H777) Output Voltage Check	5-2
5.3.3	Major Power Supply Failure	
5.3.3.1	Raw DC Voltage Check	
5.3.3.2	MOS Regulator Pico Fuse Check	
5.3.3.3	CLOCK OFF Signal Test	5-5
5.3.3.4	Clock Output Check	5-5
5.3.3.5	+5 V Regulator Fuse Check	
5.3.4	Raw DC Voltage Failure	
5.3.4.1	EMI Line Filter Test	
5.3.4.2	Transformer Input Check	5-9
5.3.4.3	Fuse Check	
5.3.5	AC LO and DC LO Corrective Maintenance	5-10
5.3.6	Removal of Power Supply and Assemblies	5-10
5.3.6.1	Power Supply Cover Removal	5-10
5.3.6.2	Power Supply Removal	
5.3.6.3	AC Control Assembly Removal	
5.3.6.4	Core Regulator Removal	5-12
5.3.6.5	MOS Regulator Removal	
5.3.6.6	Removal of the +5 V Regulator (7011073 or 7012909)	5-14
5.3.7	H775A Battery Backup Maintenance	5-15
5.3.7.1	Input/Output Check	5-15
5.3.7.2	Battery Check	
5.3.7.3	Shut-Off Relay Circuit Check	5-21
5.3.7.4	Fuse Check	
5.3.7.5	Discharge Circuit Check	
5.3.7.6	Charging Circuit Check	5-21
5.3.8	Battery Backup Component Replacement	5-24

# APPENDIX A H777 INTERCONNECTION DIAGRAM

Page

# **FIGURES**

# Figure No.

## Title

# Page

1-1	BA11-L Mounting Box	.1-3
1-2	Consoles	
1-3	H777 Power Supply	
1-4	Power Distribution Board	
1-5	H775A Battery Backup Option (Front View)	<b>I-11</b>
1-6	Remote Power Control	
2-1	Double System Unit Backplane	
2-2	Backplane Size	
2-3	Module Contact Designations	
2-4	Backplane Map	
2-5	Standard and Modified Unibus Pin Designations	
2-6	SPC Pin Designations	
2-7	NPG Signal Path	
2-8	BG Signal Path (BG4 Line)	
2-9	Backplane Power Harness	
2-10	Mate-N-Lok Connector Pin Locations (Viewed from Wire Side)	
2-11	Power Distribution Board	
2-12	Connector Specifications for BA11-L	2-13
2-12	Connector Specifications for 861-B and 861-C Power Controllers	2-14
3-1	H777 Power Supply	.3-1
3-2	H777 Block Diagram.	
3-3	Raw DC Circuit	
3-4	115 V and 230 V Transformer Configurations	
3-5	AC Control Assembly Mechanical Configuration (7011075)	
3-6	MOS Regulator Board	
3-7	MOS Regulator Block Diagram	
3-8	555 Timer	
3-9	Master Clock	
3-10	±15B Circuit	
3-11	±15B Pass Switch and Filter	
3-12	±15B Controller	
3-13	Reset-Trigger Sequence Exaggerated Waveform	
3-14	Overcurrent Limiting Waveforms	
3-15	+5B Circuit	
3-16	Current Foldback	
3-17	Core Regulator Board	
3-18	Core Regulator Block Diagram	
3-19	+20 V Circuit	
3-20	–5 V Circuit	
3-21	+5 V Regulator (7011073)	
3-22	+5 V Regulator Block Diagram	
3-23	+5 V Circuit	
3-24	+5 V Controller Waveforms	
3-25	Power Sequence Control Circuit	
3-26	Power Up/Down Sequence	

# FIGURES (CONT)

#### Title Page **Figure No** Power Up/Down Control of Core and +5 V Regulators......3-45 3-27 3-28 3-29 3-30 H775A Battery Backup Unit (Rear View).....4-2 4-1 Input/Output Circuit Breaker ......4-2 4-2 H775A Input/Output Cable.....4-3 4-3 H775A Block Diagram......4-4 4-4 4-5 Voltage Boost Circuit ......4-6 4-6 Battery Charge Rate Status and Control......4-9 4-7 Battery Discharge and Control Circuit......4-10 4-8 4-9 Battery Discharge Limit Circuit......4-11 5-1 5-2 5-3 5-4 AC Control Assembly Mechanical Configuration (7011075)......5-8 5-5 5-6 5-7 5-8 5-9 5-10 H775A Battery Backup Board ......5-19 5-11 5-12 5 - 13

# TABLES

#### Table No.

#### Title

#### Page

1-1	BA11-L Option Designations	1-1
1-2	BA11-L Physical Specifications	
1-3	H777 Major Assemblies	
1-4	H777 Input Specifications	1-9
1-5	H777 Output Specifications	1-10
1-6	H775A Battery Backup Specifications	
1-7	Power Control Operation	
2-1	Power Connector Signal Assignments for DD11-DK	
2-2	Power Connector Signal Assignments for DD11-CK	

# **TABLES** (CONT)

# Table No.TitlePage3-1AC Control Assemblies3-53-2Battery Monitor Operation in 25 A Regulator3-473-3Battery Monitor Operation in 32 A Regulator3-495-1Regulator Specifications5-45-2H775A Input/Output Connector Voltages5-175-3Troubleshooting Voltages for Charge Rate Switch and Control5-24

# CHAPTER 1 CHARACTERISTICS AND SPECIFICATIONS

#### **1.1 GENERAL**

This manual describes the BA11-L mounting box. The BA11-L comes in 12 versions as listed in Table 1-1. The BA11-L can be used to house a PDP-11/04, PDP-11/34 or PDP-11/34A. It can also be used as an expander box containing various devices or options compatible with the PDP-11 family (i.e., peripheral controls).

Mounting Box Designation	Usage	AC Input Voltage (Vac)	Backplane Supplied	Power Supply	Regulators Contained in Power Supply
BA11-LA	PDP-11/04 or 11/34	115	DD11-CK or PK	H777-AA	25 A, +5 V, MOS and Core
BA11-LB	PDP-11/04 or 11/34	230	DD11-CK or DD11-PK	H777-AB	25 A, +5 V, MOS and Core
BA11-LC	PDP-11/04 or 11/34	115	DD11-CK or DD11-PK	H777-BA	25 A, +5 V and MOS
BA11-LD	PDP-11/04 or 11/34	230	DD11-CK or DD11-PK	H777-BB	25 A, +5 V and MOS
BA11-LE	Expander Box	115	Not Supplied	H777-CA	32 A, +5 V MOS and Core
BA11-LF	Expander Box	230	Not Supplied	Н777-СВ	32 A, +5 V MOS and Core
BA11-LH	Expander Box	115	Not Supplied	H777-DA	32 A, +5 V and MOS
BA11-LJ	Expander Box	230	Not Supplied	H777-DB	32 A, +5 V and MOS
BA11-LK	PDP-11/04 or 11/34A	115	DD11-CK or DD11-PK	H777-CA	32 A, +5 V MOS and Core

 Table 1-1
 BA11-L Option Designations

Mounting Box Designation	Usage	AC Input Voltage (Vac)	Backplane Supplied	Power Supply	Regulators Contained In Power Supply
BA11-LL	PDP-11/04 or 11/34A	230	DD11-CK or DD11-PK	Н777-СВ	32 A, +5 V, MOS and Core
BA11-LM	PDP-11/04 or 11/34A	115	DD11-CK or DD11-PK	H777-DA	32 A, +5 V and MOS
BA11-LN	PDP-11/04 or 11/34A	230	DD11-CK or DD11-PK	H777-DB	32 A, +5 V and MOS

 Table 1-1
 BA11-L Option Designations (Cont)

#### NOTES

1.	The DD11-PK or DD11-CK is supplied in a PDP-11/04 processor box. Only the DD11-PK is supplied in a PDP-11/34 or PDP-11/34A processor box.
2.	An expander box can use a DD11-DK, DD11- CK or special purpose backplane
3.	A PDP-11/04 housed in a BA11-LK, -LL,

3. A PDP-11/04 housed in a BAI1-LK, -LL, -LM or -LN is assigned serial #10000 or higher.

The BA11-L contains a power supply (H777) and mounting space for a backplane. A 9-slot backplane (DD11-DK) or up to two 4-slot backplanes (DD11-CK) can be placed in the BA11-L.

There are eight versions of the H777. These versions are combinations of the following: 115 Vac or 230 Vac input power source and a 25 A or 32 A + 5 V regulator (with an MOS or MOS and core regulator).

A self-contained battery backup unit (H775A) is offered as an option for use with any version of the BA11-L.

#### **1.2** PHYSICAL CHARACTERISTICS OF THE BA11-L (Figure 1-1)

The BA11-L components fit into a mounting frame designed to provide a strong enclosure with maximum accessibility. The mounting frame is divided into two major sections with the modules in one section and the H777 power supply in the other section.

There are two fans in the BA11-L. One fan cools the power supply and the other fan cools the module section. Both fans circulate air toward the back of the mounting frame. A single fan filter goes across the width of the mounting frame in the front of the box.

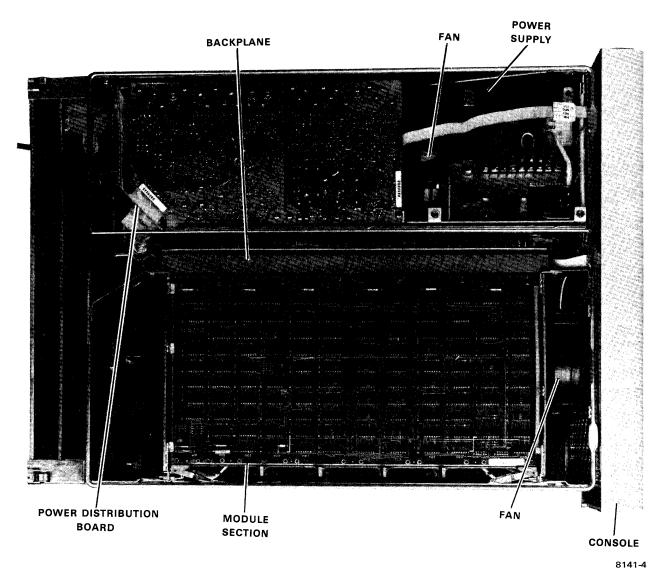
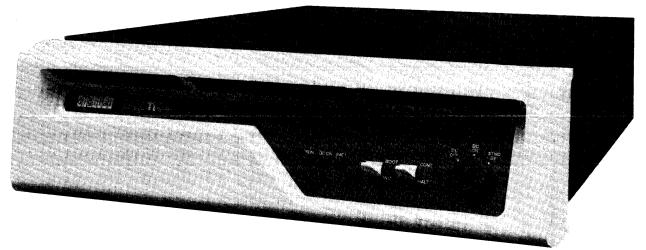


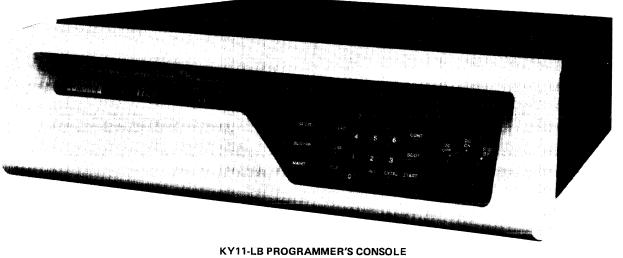
Figure 1-1 BA11-L Mounting Box

A console mounts to the front of the mounting frame. There are three consoles available with the BA11-L; the operator's console (KY11-LA), the programmer's console (KY11-LB) and the expander console (70-12540-00). The expander console comes with the BA11-LE, BA11-LF, BA11-LH and BA11-LJ; the KY11-LA and KY11-LB are used with the other versions of the BA11-L. Figure 1-2 illustrates the three consoles. Only the expander console is discussed here. For information concerning the KY11-LB, refer to the KY11-LB Programmer's Console Maintenance Manual, (EK-KY1LB-MM-001); for information concerning the KY11-LA, refer to the PDP-11/04 System User's Manual (EK-11004-0P-002).

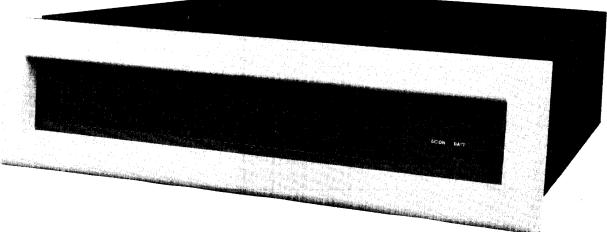


KY11-LA OPERATOR'S CONSOLE

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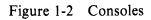


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EXPANDER CONSOLE

8141-5



The expander console is a metal plate with a louvered grill for airflow. A power light (DC ON) and a battery monitor light (BATT) are displayed on the panel. The indicator lights are light-emitting diodes (LEDs) mounted to a printed circuit (PC) board attached to the console behind the grill.

A ribbon cable from the +5 V regulator in the H777 plugs into a connector on the PC board to power the display lights. (The ribbon cable also contains control lines for a power switch that is used on the KY11-LA and KY11-LB.)

The mounting frame slides into a wraparound envelope that completely encloses four sides of the mounting frame. The front and back of the envelope are open for airflow. The envelope is easily mounted and functions as a slide mechanism for withdrawing the frame and its contents. Refer to Table 1-2.

Parameter	Specification		
Chassis size (with expansion console)	13.5 cm H × 48 cm W × 64 cm D (5-1/4 in H × 19 in W × 25 in D)		
Chassis weight (without logic modules)	20 kg (45 lb)		
H777 power supply size	12.7 cm H $\times$ 15.3 cm W $\times$ 50.8 cm D (5 in H $\times$ 6 in W $\times$ 20 in D)		
Slide extension	57.15 cm (22.5 in)		
Slideweight capacity	18.14 kg (40 lb)		
(BA11-L fully extended) Mounting capacity	1 double system unit backplane or 2 single system unit back- planes		
Fan air movement direction	Front to back		
Shock and vibration character- istics Operating Nonoperating	10G for 10 ms – 1/2 sine pulse 40G for 30 ms – 1/2 sine pulse		
Temperature Operating Nonoperating	0° to 50° C (32° to 122° F) -55° to 85° C (-67° to 185° F)		
Humidity	0 to 90% (no condensation)		

 Table 1-2
 BA11-L
 Physical
 Specifications

The H777 provides two green wires which are chassis ground. The green wire in the back is used to ground the rack; the green wire in the front is used to ground the console.

#### 1.3 H777 POWER SUPPLY

The H777 (Figure 1-3), a multivoltage power supply designed for use within the BA11-L, provides 240 W of dc power. The power supply has at last three and a maximum of four assemblies which are listed in Table 1-3.

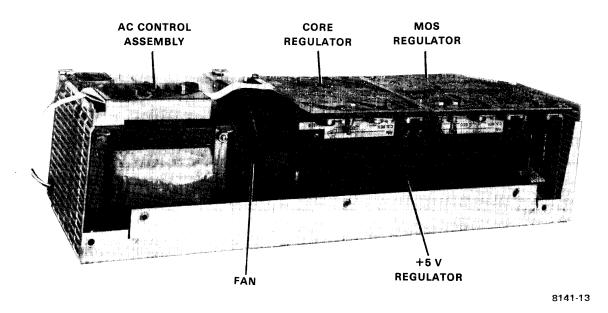


Figure 1-3 H777 Power Supply

Assembly	Function		
AC Input Assembly	Contains a transformer, line filter, and other ac utility interface equipment		
+5 V Regulator (7011073 or 7012909)	Produces +5 V power for the logic modules Provides AC LO and DC LO power fail signals Provides an ac line clock signal (LTC) Contains battery monitoring circuitry for the H775A battery backup unit Provides a BOOT ENABLE signal		
MOS Regulator (5411601)	Produces $\pm 15$ V and $+5$ V power for use by MOS memory (designated $\pm 15B$ and $+5B$ ) Provides $\pm 15$ V power to the logic modules via solid state switches		

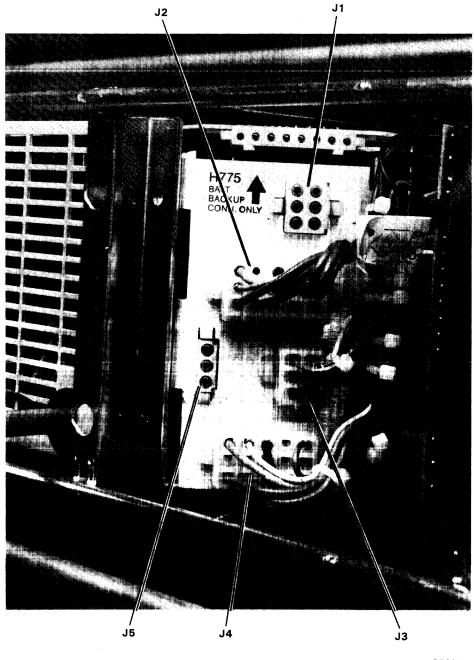
Table 1-3	H777	Major	Assemblies
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Assembly		Function
Core Regulator (5411599)		Produces $+20$ V and $-5$ V power for use by core memory
	1.	NOTES Regulator 7011073 provides up to 25 A of +5 V power to the load and regulator 7012909 pro- vides up to 32 A of +5 V power to the load.
	2.	In the STANDBY mode, only the $\pm 15B$ and $\pm 5B$ outputs are operational. During an ac power failure, the $\pm 15B$ and $\pm 5B$ outputs are battery supported if the H775A is present. If the H777 is in the STANDBY mode and ac input power is present, the batteries in the H755A are not discharged.
	3.	The core regulator is optional.

#### Table 1-3 H777 Major Assemblies (Cont)

Power from the regulators is routed to the backplane via the power distribution board (Figure 1-4) on the H777. The dc voltage outputs of the H777 are available at J2 and J4 which are wired in parallel. Signals AC LO, DC LO and LTC are available at J1 and J3 which are also wired in parallel. Connector J5 is the power control (PC) connector discussed in Paragraph 1.5.

The input specifications for the H777 are listed in Table 1-4 and the output specifications are listed in Table 1-5.



8141-17

Figure 1-4 Power Distribution Board

104–127 Vrms
208–254 Vrms
90–132 Vrms
180–264 Vrms
47–63 Hz
5 A (rms)
2.5 Å
4 A
2 A
480* W
480 W
340 W
340 W
20 A peak
40 A peak
180/360 Vrms 0.1 second
0.1 second
Time interval between the start of an ac power failure and the
assertion (grounding) of AC LO.
Time interval between the start of an ap newer failure and a lass
Time interval between the start of an ac power failure and a loss
of regulated dc output.
Internal Magnetic Circuit Breaker
115 V – 10 A for H777-AA and -BA, 5 A for H777-CA and -DA
230  V - 5  A
100° C (212° F) NC mounted on +5 V REG heat sink. Provides
electronic shutdown of that regulator and 5411599.

# Table 1-4 H777 Input Specifications

#### Table 1-4 H777 Input Specifications (Cont)

#### Hi Potential

1500 Vdc for 60 seconds from input to output or input to chassis.

#### \*Transformer limit.

NOTE

Except for the circuit breakers, the input specifications for the H777-CA, -CB, -DA, and -DB are the same as for the H777-AA, -AB, -BA, and -BB, respectively.

Regulator Assembly	Output Designation	Output Voltage	Tolerance	Regulation Line	Reg Load	Current Output
MOS Regulator (5411601)	+15B	+15.3 V	±450 mV	0.5%	0.5%	0–2 A
(3411001)	–15 B	–15.3 V	$\pm 450 \mathrm{mV}$	1%	1%	0–2 A
	+15 V	+15.3 V	-200  mV max at $+15B$ Output	1%	1.5%	0–1A
	-15 V	-15.3 V	-200 mV max at -15B Output	1%	1.5%	0–1 A
	+5B	+5.1 V	+100 mV -150	1%	1%	0–4 A
Core Regulator (5411599)	+20 V	+20.0 V	$\pm 500 \text{ mV}$	1%	0.5%	0-6 A
(5411577)	-5 V	-5.1 V	+100 mV -150	1%	1%	0–4 A
5 V Regulator (7011073)	+5 V	+5.1 V	+100 mV -150	1%	1%	0–25 A
or +5 V Regulator (7012909)	+5 V	+5.1 V	+100 mV -150	1%	1%	0-32 A

Table 1-5 H777 Output Specifications

Ripple – 2% peak to peak all outputs Temp Coefficient – +0.5 mV/°C Output Noise – 2% max peak

#### **NOTES:**

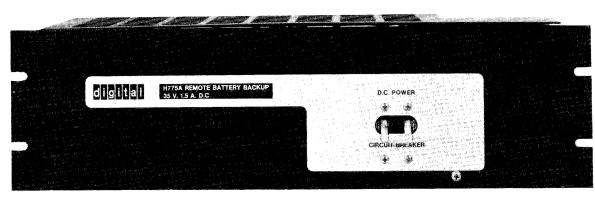
- 1. The total current output of +15 V, -15 V, +15B, and -15B cannot exceed 4 A. The +15 V and -15 V outputs can provide a maximum of 1 A each. Refer to Paragraph 3.6.3.4.
- 2. The line regulation specifies the variation in output voltage during power supply operation with a constant load. This load regulation specifies the variation in output voltage caused by varying the load from an open circuit to max load.

#### 1.4 H775A BATTERY BACKUP UNIT

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A self-contained battery backup unit, the H775A, is offered as an option for use with the H777 power supply. During an ac power failure, the H775A provides a battery input voltage to the MOS regulator only allowing the  $\pm 15B$  and  $\pm 5B$  outputs to remain operational. Therefore, the MOS regulator can provide refresh power for a limited time after an ac power failure has occurred.

The H775A contains two batteries and charging circuitry. Figure 1-5 shows the H775A and Table 1-6 lists the specifications for the H775A.



7883-3

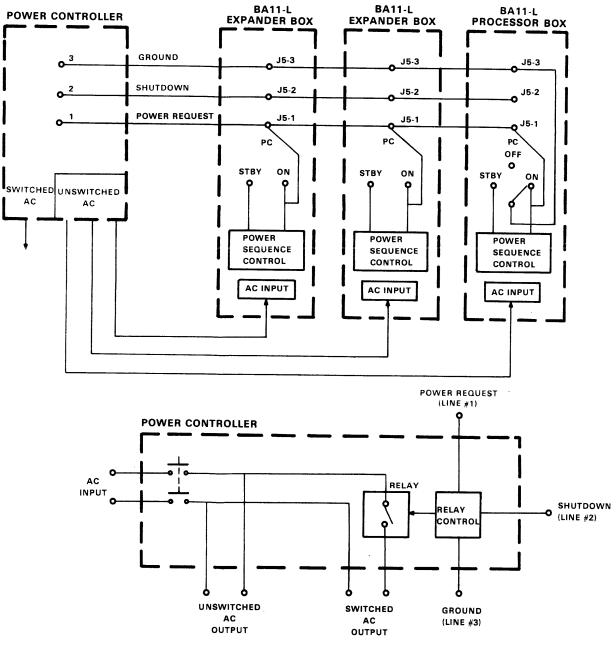
Figure 1-5 H775A Battery Backup Option (Front View)

Parameter	Specification
Size	13.3 cm H $\times$ 48.25 cm W $\times$ 10.8 cm D (5-1/4 in H $\times$ 19 in W $\times$ 4-1/4 in D)
Weight	6.8 kg (15 lb)
Input/Output	25-48 Vdc/24 Vdc
Capacity	120 wh at 2.5 A and 50° C (122° F)
Cell Type	Sealed lead acid
Charger	Constant current, dual rate

Table 1-6 H775A Battery Backup Specifications

# **1.5 REMOTE POWER CONTROL (Figure 1-6)**

The power control is a power distribution system which simultaneously turns on all the power supplies in a PDP-11 system (processor box and expander boxes). The power control consists of a power controller and three power control lines: power request (line 1), emergency shutdown (line 2), and system ground (line 3).



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Figure 1-6 Remote Power Control

The power controller routes ac power to the system via unswitched and switched outputs. The unswitched outputs are live as long as ac power is applied to the power controller via its circuit breaker. The switched outputs are controlled by a relay which, in turn, is controlled by the power request and emergency shutdown lines. These lines are either open or grounded. The operation of the power controller is summarized in Table 1-7.

Line Status		Power Controller Status		
Power Request (Line 1)	Emergency Shutdown (Line 2)	State of Relay	Switched Outputs	
open open grounded grounded	open grounded grounded open	open open open closed	dead dead dead live	

 Table 1-7
 Power Control Operation

The power control lines plug into connector J5 at the H777 power distribution board of all the BA11-L boxes in the PDP-11 system. The emergency shutdown line is not used by the H777.

Only the processor box has a power switch on the console. When the power switch is placed in the ON position, the power request line is grounded which, in turn, grounds the ON input of the power supplies in the expander boxes. Therefore, when the power switch in the processor box is turned on, all the power supplies connected to the power control lines initiate a power-up sequence.

Standby operation of an expander box is selectable via a jumper plug on the expander console. The jumper plug grounds the STBY input of the H777. If the power request line is not grounded, the power supply is in the STANDBY mode. If the STBY input is not grounded, the power supply turns off when the power request line is not grounded.

# CHAPTER 2 BACKPLANE CONFIGURATIONS AND INSTALLATION INFORMATION

#### 2.1 GENERAL

Three types of backplanes can be used in the BA11-L: a processor backplane (DD11-PK), an expander backplane (DD11-DK), or a special purpose backplane.

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The DD11-CK can be used as an expander backplane or a processor backplane for the PDP-11/04. Only the expander backplanes, DD11-CK and DD11-DK, are discussed in this chapter.

A backplane is also classified as a double system unit with nine slots or a single system unit with four slots. The DD11-DK and DD11-PK are double system units and the DD11-CK is a single system unit. The BA11-L can house any double system unit or up to two single system units.

#### 2.2 PHYSICAL DESCRIPTION

A double system unit backplane is shown in Figure 2-1. It is a grid of connectors with each connector specified by a slot (1-9) and a section (A-F). Logic modules plug into the module side of the backplane. The pin side is wired to provide power and signal interconnections to the modules.

Any pin on the backplane can be specified as shown in the following example.

Designation A01B2

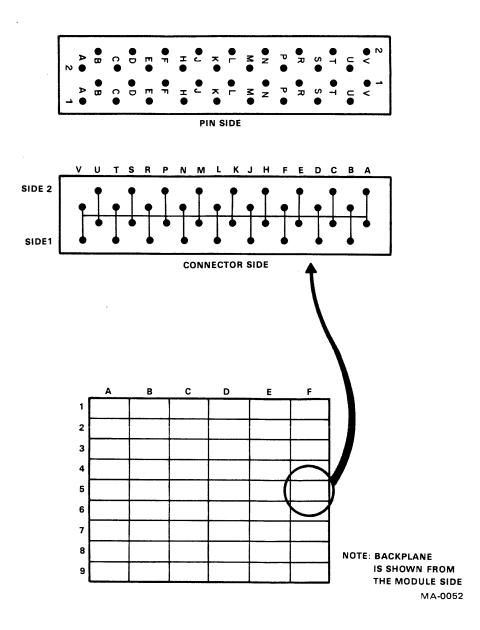
- A Section letter (A–F)
- 01 Slot number (01–09)
- B Pin letter (A–V)
- 2 Connector side (1 or 2)

Figure 2-2 shows a double system unit and a single system unit. Note that the single system unit has only four slots.

A module can connect with one or more sections of a slot.

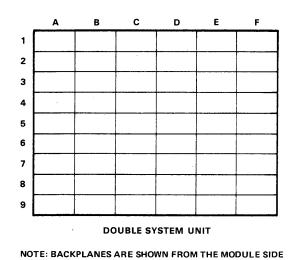
Single height module – 1 section Dual height module – 2 sections Quad height modules – 4 sections Hex height modules – 6 sections (1 full slot)

Figure 2-3 shows the connecting edge of a hex module.



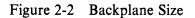
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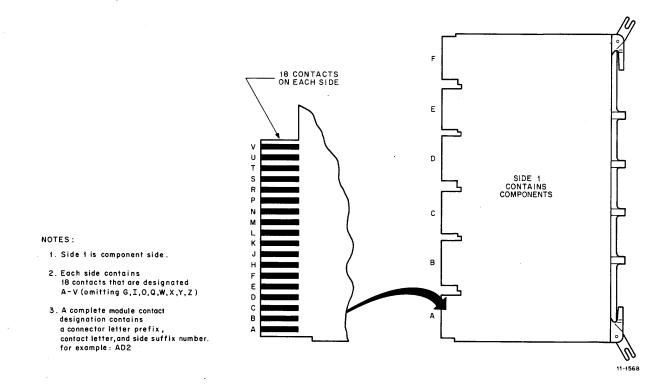
Figure 2-1 Double System Unit Backplane



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#### 2.3 ELECTRICAL DESCRIPTION

In accordance with their pin designations, the connectors in the backplane are classified into three categories: standard Unibus, modified Unibus and small peripheral control (SPC) connectors. Particular areas of the backplane are reserved for the different types of connectors as shown in Figure 2-4.

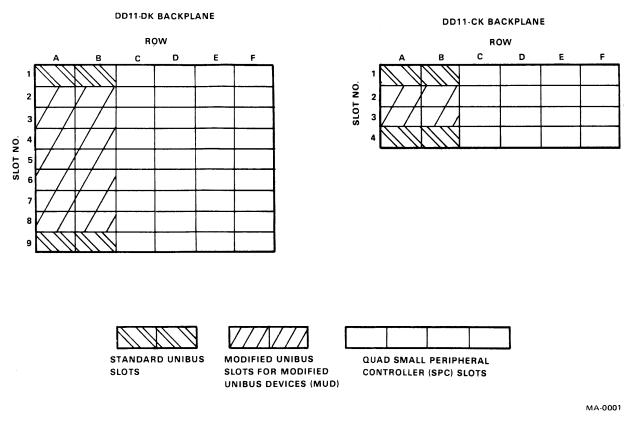


Figure 2-4 Backplane Map

The standard Unibus connectors contain all the Unibus connections. Sections A and B of slot 1 are the beginning of the Unibus in the DD11-CK and DD11-DK and should be occupied by the BC11-A Unibus cable since they are expander backplanes. Sections A and B of slot 9 in the DD11-DK or of slot 4 in the DD11-CK are the end of the Unibus on the backplane. These sections should be occupied by the BC11-A Unibus cable or a terminator module.

Slots 2 through 8 (sections A and B) are the modified Unibus in the DD11-DK and slots 2 and 3 (sections A and B) are the modified Unibus in the DD11-CK.

Figure 2-5 shows the pin designations of the standard and modified Unibus connectors. The modified Unibus differs from the standard Unibus in that certain pins have been redesignated. Some ground connections, BUS GRANT signals and the NPG signal have been removed from the standard Unibus and have been redesignated with core memory voltage pins, battery backup voltage pins for MOS memory, parity signal pins, several reserve pins and test point pins.

#### STANDARD UNIBUS PIN DESIGNATIONS

		COLI	JMN		COLL	IN	1N	
		4	A B		В			
\$	ide							
P	in	1	2		1		2	
F		INIT	+5V		G6	1	+5V	
<u>_</u>		L		+	н	_		ļ
E	2		GND	Γ.	G5	0	GND	
		L			н			
(		D00	GND		R5	'	GND	l
		L			L			ļ
	þ	D02	D01	G	ND		BR4	l
		L	L			Ĺ	L	
	E	D04	D03	G	ND		BG4	l
		L	L				H DC	
	F	D06	D05	1	C .			
L		L	L		.0 L	╞	LO L A00	4
	н	D08	D07	1	.01		L	
L		L	L		L 103	╀	L A02	
	J	D10	D09	1	103 L		L L	
ŀ			L D11	+	L 405	╀	A04	┥
	к	D12		ſ			L	
┞		L D14	L D13	_	L 407	+	A06	-
l	L	L L		ľ	L.		L	
ŀ			L	+	A09	╀	A08	4
I	м	PA	D15	ľ			L	
ŀ		L	L	+	L A11	+	A10	-
I	N	GND		ľ			L	
ł			L BBS	<u>_</u>	L A13	╉	A12	-
	P	GNE		1	L		L	
ł		GNE		/	A15	+	A14	-
	R	GNL		1	L		L	
		GNE		,	A17	+	A16	_
	s	GN		`	L		L	
		GNI	4	,	GND	-	C1	-
	т			' I	5110		L	
		NPC		6	SSYN	-	- C0	
	υ	H	ן ( ה	-	L		L	
		BG	7 GN	D	MSYN	1	GND	
	v	so		_	L			
							L	

#### MODIFIED UNIBUS PIN DESIGNATIONS

	COLL		COLU	MN
	A			
Side				
Pin	1	2	1	2
А	INIT	+5V	RESV PIN	+5V
	L			
в	INTR	ТР	RESV	тр
• •	L		PIN	
с	D00	GND	BR5	GND
	L		L	
D	D02	D01	+5	BR4
	L	L	ВАТ	L
Е	D04	D03	INT	PAR
E	L	L	SSYN	DET
-	D06	D05	AC	DC
F	L	L	LOL	LOL
	D08	D07	A01	A00
н	L	L	L	L
	D10	D09	A03	A02
J	L	L	L	L
	D12	D11	A05	A04
к	L	L	L	L
	D14	D13	A07	A06
L	L	L	L	L
	РА	D15	A09	A08
м	L	L	L	L
<u> </u>	PAR	PB	A11	A10
N	P1	L	L	L
<u> </u>	PAR	BBSY		A12
Р	P0	L	L	L
<u> </u>	+15	SAC	( A15	A14
R	ВАТ	L	L	L
<u> </u>	-15	NPR	A17	A16
s	ВАТ	L	L	L
<b>—</b>	GND	BR7	GND	C1
т	1	L		L
	+20	BR6	SSYN	CO
U	(CORE)	L	L	L
$\square$	+20	+20	MSYN	
v	(CORE)			(CORE)
L				

11-4631



Figure 2-5 Standard and Modified Unibus Pin Designations

Dual height modules that are standard Unibus compatible should not be placed in the modified Unibus sections. To do so would destroy the modules.

The small peripheral control sections (C, D, E, and F) collectively contain all the Unibus connections (including grant lines) as well as power voltages (+5 V, +15 V, -15 V). These sections can be occupied by hex height or SPC modules containing control logic for peripheral devices. Figure 2-6 shows the pin designations for the SPC connectors.

NIDE PIN121212121ANPG (IN)+5VTP+5VGND A+5VABG OUT+5VBNPG (OUT)-15VTP-15VASSYN-15VABG OUT-15VBNPG (OUT)-15VTP-15VASSYN-15VABG OUT-15VCPA LGNDA SELGNDA12GNDSSYNGNDLPAGNDA SELGNDA12GNDSSYNGNDDLTCD15A OUTBR7A17A15BBSYF01LLOWLLLLN1N1ETPD13A SELBR6MSYNA16F01D02FTPD13A SELBR5A02C1D05D06LLLLLLHLLQQUTLLLENB BAINTLENB BAINTAINTBG7A14A13D08AINTJBL2OUTLLLLLZAINTKTPD09A OUTBG7A14A13D08AINTAINTLLBCQUTLLLZAINTLD07AINTBG6A11A13D08AINTAINTLAINTBG7 <th></th> <th>COLU</th> <th></th> <th>COLL</th> <th></th> <th>COLL</th> <th>MN</th> <th>COLL</th> <th></th>		COLU		COLL		COLL	MN	COLL	
A A (IN)NPG (IN)+5VTP+5VGND (GND+5VABG (OUT)+5VABG (OUT)+5VBNPG (OUT)15VTP-15VASSYN-15VABG-15VBNPG (OUT)15VTP-15VASSYN-15VABG-15VCLGNDASELGNDA12GNDSSYNGNDCL015A OUTBR7A17A15BBSYFO1DLTCD15A OUTBR7A17A16FO1D02LLLOWLLLLN1ETPD14ASELBR6MSYNA16FO1D02LL4LLLLLLFD13ASELBR5A02C1D05D06L0LLLLLLHD11D12A INBR4A01A00D07A INTJBL2OUTLLLLAJA INTD09A OUTBG7A14A13D08A INTJA INTD09A OUTBG7A14A13D08A INTJCD09A OUTBG7A14A13D08A INTKLLCUULLLKD09A OUTBG7 <td< td=""><td>SIDE</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></td<>	SIDE								
A     (IIN)     INP     INP <td>PIN</td> <td>1</td> <td>2</td> <td>1</td> <td>2</td> <td>1</td> <td>2</td> <td>1</td> <td>2</td>	PIN	1	2	1	2	1	2	1	2
(IN)(IN)(IN)(IN)(IN)(IN)(IN)(IN)(IN)(IN)BNPG15VTP.15VASSYN.15VABG.15V.15V(IU)(IU)(II)IINIINIINIINIINIINCPAGNDASELGNDA12GNDSSYNGNDLICD15A OUTBR7A17A15BBSYF01DICUOWICICICICN1TD15A OUTBR7A17A15BBSYF01DIASELBR6MSYNA16F01D02FD14ASELBR6MSYNA16F01D02CIA SELBR5A02C1D05D06FI013A SELBR5A02C1D05D06JBI2OUTILILIRNJD11D12A INBR4A01A00D07A INTJBI2OUTILILIAJD10A SELABRSSYNC0NPRGNDJA INTD08INITBG7A14A13D08A INTKIIOUTILILILILILMID09AOUTBG7A11TPD03F01M		NPG	+5V	тр	+5V	GND	+5V	ABG	+5V
B         IOU         IOU         IOU         IN         IN         IN         IN           C         L         GND         A SEL         GND         A12         GND         SSYN         GND           D         L         GND         A SEL         GND         L         L         L         IN           D         L         LOW         L         L         L         NI         SSYN         GND           P         ITC         D15         A OUT         BR7         A17         A15         BBSY         F01           E         TP         D14         A SEL         BR6         MSYN         A16         F01         D02           F         TP         D13         A SEL         BR5         A02         C1         D05         D06           L         0         L         L         L         L         L         L         K           M         D11         D12         A IN         BR4         A01         A00         D07         A INT           J         D11         D12         A IN         BR4         SYN         C0         NPR         GND           J	A	(IN)				A		ουτ	
IOUT)IOUT)IOUT)ININPAGNDA SELGNDA12GNDSSYNGNDLGNDBR7A17A15BBSYF01DLLOWLLLLN1PD15A OUTBR7A17A15BBSYF01DLLOWLLLLN1PD14A SELBR6MSYNA16F01D02FTPD13A SELBR5A02C1D05D06L0LLLLLLLHD11D12A INBR4A01A00D07A INTHD11D12A INBR4A01A00D07A INTJA INTD10A SELA BRSSYNC0NPRGNDJA INTD10A SELA BRSSYNC0NPRGNDJA INTD10A SELA BRSSYNC0NPRGNDKTPD09A OUTBG7A114A13D08A117KLSOLLLLLMCSOAA11TPD03F01LENBASOLLLLLMLSOA11TPD33F01D04MLGNDAINTBG6 <t< td=""><td></td><td>NPG</td><td>-15V</td><td>тр</td><td>-15V</td><td>ASSYN</td><td>-15V</td><td>ABG</td><td>-15V</td></t<>		NPG	-15V	тр	-15V	ASSYN	-15V	ABG	-15V
CLIndicationIndicationIndicationIndicationIndicationDLIC0LLLIN1DLLOWLLLLN1ETPD14A SELBR6MSYNA16FO1D02LL4LLLV2LFTPD13A SELBR5A02C1D05D06L0LLLLLLHD11D12A INBR4A01A00D07A INTLLLLLLLENBBJAINTD10A SELA BRSSYNC0NPRGNDJBL2OUTLLLBJRD09A OUTBG7A14A13D08A INTKTDD08INITBG7A11TPD03F01LENBBLLOUTLLLL2MTPD07AINTBG6AINAOUTINTRF01LENBASOLLN1L2N1L2MDCD04AINTBG6AOUTA08F01D04LENBASOLLN1L2N1L2MDCD04AINTBG5A09ASELF01 <td>в</td> <td>(OUT)</td> <td></td> <td></td> <td></td> <td>IN H</td> <td></td> <td>IN</td> <td></td>	в	(OUT)				IN H		IN	
LGGLLLLDLLBR7A17A15BBSYF01LLOWLLLLN1ETPD14ASELBR6MSYNA16F01D02CL4LLLV2LFTPD13ASELBR5A02C1D05D06L0LLLLLLPD13ASELBR5A02C1D05D06L0LLLLLLPD11D12AINBR4A01A00D07AINTHD11D12AINBR4SSYNC0NPRGNDJBL2OUTLLLAINTMD10ASELABRSSYNC0NPRGNDJBL2OUTLLLAINTMD09AOUTBG7AI14A13D08AINTKLSOLLLLLLMD09AOUTBG7AI11TPD03F01LLSOLAINTBG6AUNAUUNITMDCD04AINTBG6AUUA08F01D04MLOLAOUTLOAINTBG5		PA	GND	A SEL	GND	A12	GND	SSYN	GND
DLLLLLLLLLN1ETPD14A SELBR6MSYNA16FO1D02L4LLLV2LFTPD13A SELBR5A02C1D05D06L0LLLLLLLHD11D12A INBR4A01A00D07A INTHLLLLLLENB BJA INTD10A SELA BRSSYNC0NPRGNDJBL2OUTLLLAKTPD09A OUTBG7A14A13D08A INTKTPD09A OUTBG7A11TPD03F01LSOLLLLLLMD07AINTBG7A11TPD03F01LENBBLUOUTLLLLMDCD04AINTBG6AUTA08F01D04NDCD04AINTBG6AOUTA08F01D04NLOLAOUTLON1LLPBC0LSOLUN1LPBC0LSOLLN1LPGR1 <td>Ľ</td> <td>L</td> <td></td> <td>6</td> <td></td> <td>L</td> <td></td> <td>L</td> <td></td>	Ľ	L		6		L		L	
Image: border		LTC	D15	A OUT	BR7	A17	A15	BBSY	F01
ELALLLV2LFTPD13A SELBR5A02C1D05D06L0LLLLLLHD11D12A INBR4A01A00D07A INTLLLLLLLENBBJA INTD10A SELA BRSSYNC0NPRGNDJBL2OUTLLLAMTPD09A OUTBG7A14A13D08A INTKTPD09A OUTBG7A11TPD03F01LLOUTLLLLLMTPD08INITBG7A11TPD03F01LENBBLLOUTLLLLMTPD07AINTBG6AINAOUTINTRF01MDCD04A INTBG6A OUTA08F01D04NLOLAOUTLOWLN1LPREQLAOUTLOWLN1LPREQLAOUTLOWLN1LPREQLAOUTLAQUTP2REQLAOUTSOGQUP2N1 <t< td=""><td>Ū</td><td></td><td>L</td><td>LOW</td><td>L</td><td>L</td><td>L</td><td>L</td><td>N1</td></t<>	Ū		L	LOW	L	L	L	L	N1
Image: big	_	тр	D14	A SEL	BR6	MSYN	A16	F01	D02
FL0LLLLLLHL1D11D12A INBR4A01A00D07A INTHLLLLLLENB BJA INTD10A SELA BRSSYNCONPRGNDJBL2OUTLLLAMNTD09A OUTBG7A14A13D08A INTKTPD09A OUTBG7A14A13D08A INTLLOUTLLLBLRNBLOUTLLLBLBINITBG7A11TPD03FO1LENBBLUOUTLLLLMPPD07AINTBG6AINAOUTINTRFO1MDCD04A INTBG6A OUTA08FO1D04NLENBASOLLN1LM2NDCD04A INTBG6A OUTA08FO1D04NLOLAOUTLOWLN1LPHALTD05TPBG5A10A07ABRFO1RGRTLOUSOLLQUTP2N1SFBD00TPBG4ASELASEL	E		L	4	L	L	L	V2	L
Image: big		ТР	D13	A SEL	BR5	A02	C1	D05	D06
HLLLLLLLENBBJA INTD10A SELA BRSSYNCONPRGNDBL2OUTLLLARTPD09A OUTBG7A14A13D08A INTKTPD09A OUTBG7A14A13D08A INTKLSOLLLBTPD09A INTBG7A11TPD03FO1LENBBLLOUTLLL2MTPD07AINTBG6AINAOUTINTRFO1MD07AINTBG6AINAOUTINTRFO1MDCD04A INTBG6AOUTA08FO1D04NDCD04A INTBG5A10A07ABRFO1PREQLGNS0LLOUTP2N1RAALTD05TPBG5A09ASELF01F01RGRTLGNS0GGM2P2N1SFBD00TPBG4ASELASELFO1F01SGNDGNDBG4GNDASELGNDSACKLLLTGNDGNDBG4GNDASELAGAAINTABROUTLLA			L	0	L	L	L	L	L
LLLLLLLLENB BJAINTD10A SELA BRSSYNCONPRGNDJBL2OUTLLLAKD09A OUTBG7A14A13D08A INTKLCSOLLLBLLSOLLLBLD09A OUTBG7A11TPD03FO1LENBBLLOUTLLLPD07AINTBG7A11TPD03FO1MDCDALOUTLAOUTINTRFO1MDCD04AINTBG6AINAOUTINTRFO1MDCD04AINTBG6AOUTA08FO1D04NDCD04AINTBG6AOUTA08FO1D04NDCD04AINTBG5A10A07ABRFO1PREQLSOLLQUTP2N1RD01TPBG5A09ASELFO1FO1SRRTLOUTLASELFO1FO1SRRTLOUTLASELASELFO1SD00TPBG4ASELASELFO1FO1SCCOUT <t< td=""><td></td><td>D11</td><td>D12</td><td>A IN</td><td>BR4</td><td>A01</td><td>A00</td><td>D07</td><td>A INT</td></t<>		D11	D12	A IN	BR4	A01	A00	D07	A INT
JBL2OUTLLLARTPD09A OUTBG7A14A13D08A INTKLCSOLLLBLLSOLLLBLA INTD08INITBG7A11TPD03FO1LENBBLLOUTLLL2MTPD07AINTBG6AINAOUTINTRFO1MLENBASO-HIGHLM2NDCD04A INTBG6A OUTA08FO1D04LOLAOUTLOWLN1LPREQLANBG5A10A07ABRFO1REQLOUTSOLLOUTP2REQLOUTBG5A09ASELFO1FO1SRALTD01TPBG5A09ASELFO1FO1SRALTD01TPBG4ASELASELFO1FO1SGNDGNDGNDBG4GNDASELGNDSACKTLOUTIIIIIIIIIMLIOUTABGA06A04AINTABRMLIIIIIIIIIIIIIIIR<	н	L	L		L	L	L	L	ENB B
$ \begin{array}{ c c c c c c } \hline \begin{tabular}{ c c c } \hline \begin{tabular}{ c c c } \hline \begin{tabular}{ c c } \hline \hline \begin{tabular}{ c c } \hline \begin{tabular}{ c$		A INT	D10	A SEL	A BR	SSYN	C0	NPR	GND
K         L         L         SO         L         L         L         B           A INT         D08         INIT         BG7         A11         TP         D03         FO1           L         BRB         L         L         OUT         L         TP         D03         FO1           M         TP         D07         AINT         BG6         AIN         AOUT         INTR         FO1           M         TP         D07         AINT         BG6         AOUT         AOUT         INTR         FO1           M         L         ENBA         SO         -         HIGH         L         M2           M         DC         D04         AINT         BG6         AOUT         A08         FO1         D04           N         DC         D04         AINT         BG6         AOUT         A08         FO1         D04           N         DC         D04         AINT         BG6         AOUT         A08         FO1         D04           P         RCQ         L          SO         L         L         N1         E           REQ         L         O00	J	В	L	2	OUT	L	L	L	A
Image: Constraint of the section of		тр	D09	A OUT	BG7	A14	A13	D08	AINT
LENBBLLOUTLLLLMTPD07AINTBG6AINAOUTINTRFO1MLENBASO-HIGHLM2NDCD04A INTBG6A OUTA08FO1D04NDCD04A INTBG6A OUTA08FO1D04NLOLAAOUTLOWLN1LPHALTD05TPBG5A10A07ABRFO1REQLSOLLOUTP2N1RGRTLOUDULASELFO1FO1SPBD00TPBG4ASELASELFO1FO1SGNDD3GNDBG4GNDASELGNDSACKTH15/+8D02TPABGA06A04A INTABRVACD06ASSYNABGA05A03A INTFO1	к		L		so	L	L	L	в
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $		A INT	D08	INIT	BG7	A11	ТР	D03	F01
	L	ENBB	L	L	ουτ	L		L	L2
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$		ТР	D07	AINT	BG6	AIN	AOUT	INTR	F01
	м		L	ENBA	so		HIGH	L	M2
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $		DC	D04	A INT	BG6	A OUT	A08	F01	D04
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	N	LO	L	А	оυт	LOW	L	N1	L
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $		HALT	D05	ТР	BG5	A10	A07	ABR	F01
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	ľ	REQ	L		S0	L	L	ουτ	P2
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	<b> </b>	HALT	D01	тр	BG5	A09	ASEL	FO1	F01
S         L         L         L         S0         6         0         M2         P2           T         GND         D03         GND         BG4         GND         ASEL         GND         SACK           T         L         OUT         2         L <td>R</td> <td>GRT</td> <td>L</td> <td></td> <td>оит</td> <td>L</td> <td>4</td> <td>L2</td> <td>N1</td>	R	GRT	L		оит	L	4	L2	N1
L         L         L         S0         6         0         M2         P2           T         GND         D03         GND         BG4         GND         ASEL         GND         SACK           L         L         OUT         2         L <td></td> <td>РВ</td> <td>D00</td> <td>TP</td> <td>BG4</td> <td>ASEL</td> <td>ASEL</td> <td>FO1</td> <td>F01</td>		РВ	D00	TP	BG4	ASEL	ASEL	FO1	F01
T         L         OUT         2         L           H15/H8         D02         TP         ABG         A06         A04         A INT         ABR           L         L         IN         L         L         A         OUT         OUT           V         AC         D06         ASSYN         ABG         A05         A03         A INT         F01	s	L	L		SO	6	0	M2	P2
L         OUT         2         L           U         +15/+8         D02         TP         ABG         A06         A04         A INT         ABR           U         L         IN         L         L         A         OUT           V         AC         D06         ASSYN         ABG         A05         A03         A INT         F01		GND	D03	GND	BG4	GND	ASEL	GND	SACK
U         L         IN         L         L         A         OUT           V         AC         D06         ASSYN         ABG         A05         A03         A INT         F01	Т		L		ουτ		2		L
AC DO6 ASSYN ABG A05 A03 A INT FO1		+15/+8	D02	ТР	ABG	A06	A04	AINT	ABR
V	U		L		IN	L	L	А	оυт
V LO L IN H OUT L L ENBA FOI		AC		ASSYN	ABG	A05	A03	AINT	FO1
	v	LO	L	IN H	оυт	L	L	ENB A	FO1

11-4630

Figure 2-6 SPC Pin Designations

#### 2.3.1 Non-Processor Grant (NPG) Line

The NPG line is the Unibus grant line for devices that perform data transfers without processor intervention. The NPG line grant continuity is provided by wire wrap jumpers on the backplane. When an NPR device is placed in a slot, the corresponding jumper wire from pin CA1 to pin CB1 of that slot must be removed. The routing of the NPG signal through the backplane is shown in Figure 2-7. Grant priority decreases from slot 1 to slot 9 in the DD11-DK (i.e., slot 1 has the highest priority and slot 9 the lowest).

NOTE If an NPR device is removed from a slot, the jumper wire from CA1 to CB1 must be reconnected.

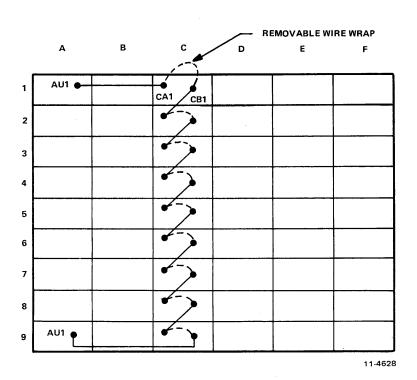


Figure 2-7 NPG Signal Path

#### 2.3.2 Bus Grant (BG) Lines

The bus grant lines (BG4:BG7) for devices requiring processor intervention during data transfers are routed through each small peripheral control section in connector D. Each of the four GRANT signals is routed on a separate line. Figure 2-8 shows the routing of one of the grant lines; the other three follow a similar path. Grant priority for each level decreases from slot 1 to slot 9.

#### NOTE

A bus grant jumper card (G727) must be placed in connector D of any unoccupied SPC section. If an SPC section is left open, bus grant continuity will be lost.

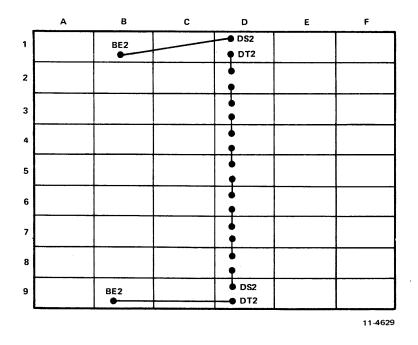
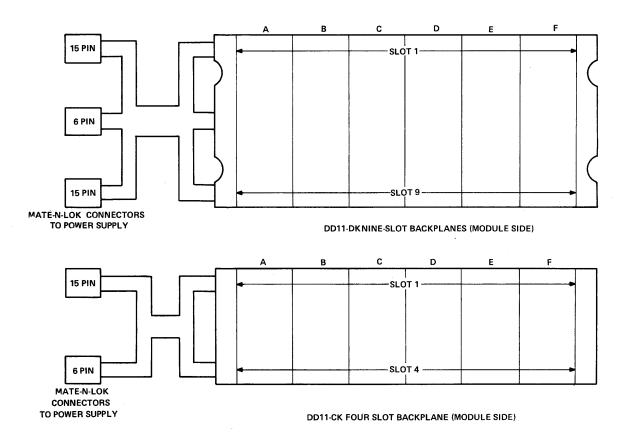


Figure 2-8 BG Signal Path (BG4 Line)

#### 2.4 POWER HARNESS

Power is supplied to the backplane via a wire harness that connects to the power distribution board of the power supply. The wires run from the backplane to a set of Mate-N-Lok connectors that plug directly into the distribution board (Figure 2-9).

The power harness from the DD11-DK contains two large connectors (15-pin Mate-N-Lok) and one small connector (6-pin Mate-N-Lok). The DD11-CK backplane has only one 15-pin connector and one 6-pin connector. The connector pin locations are shown in Figure 2-10 and the signal assignments for each pin are listed in Table 2-1 (DD11-DK) and Table 2-2 (DD11-CK).



11-4624

Figure 2-9 Backplane Power Harness

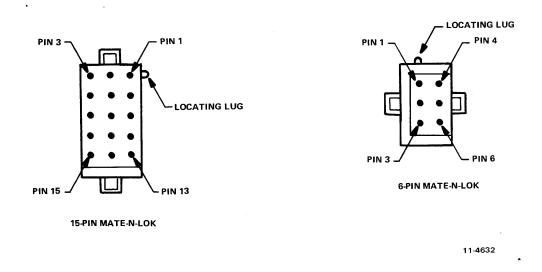


Figure 2-10 Mate-N-Lok Connector Pin Locations (Viewed from Wire Side)

	15-Pin Mate-N-Lok Connector 1					
Pin	Signal	Wire	Color			
1	+5 V	No. 14	Red			
2	+15 V	No. 18	Gray			
3	+20 V	No. 14	Orange			
4	+5 V	-	Red			
5	Spare (not connected)	-	-			
6	Spare (not connected)	No. 14	-			
7	Ground	No. 14	Black			
8	Ground	-	Black			
9	Ground	No. 14	Black			
10	Spare (not connected)	-	-			
11	Spare (not connected)	No. 14	-			
12	+5B	-	Red			
13	Spare (not connected)	No. 14	-			
14	-5 V	No. 18	Brown			
	Spare (not connected)	-	-			

 Table 2-1
 Power Connector Signal Assignments for DD11-DK

#### 15-Pin Mate-N-Lok Connector 2

Pin	Signal	Wire	Color
1	+5 V	No. 14	Red
2	Spare (not connected)	-	-
3	+20 V	No. 14	Orange
4	+5 V	No. 14	Red
5	Spare (not connected)	_	_
6	+15B	No. 18	White
7	Spare (not connected)	-	_
8	Ground	No. 14	Black
9	Ground	No. 14	Black
10	Spare (not connected)	-	_
11	Spare (not connected)	_	-
12	Spare (not connected)	_	_
13	-15 V	No. 18	Blue
14	Spare (not connected)	_	_ ·
15	-15B	No. 18	Green

#### 6-Pin Mate-N-Lok Connector

Pin	Signal	Wire	Color
1	LO GND	No. 14	Black
2	LTC (line clock)	No. 18	Brown
3	DC LO	No. 18	Violet
4	AC LO	No. 18	Yellow
5	Spare (not connected)	_	-
6	Spare (not connected)	-	_

15-Pin Mate-N-Lok Connector					
Pin	Signal	Wire	Color		
1	+5 V	No. 14	Red		
2	+15 V	No. 18	Gray		
3	+20 V	No. 18	Orange		
4	+5 V	No. 14	Red		
5	Spare (not connected)	-	-		
6	+15B	No. 18	Green		
7	Ground	No. 14	Black		
8	Ground	No. 14	Black		
9	Spare (not connected)	-	-		
10	Spare (not connected	-	_		
11	Spare (not connected)	-	- 1		
12	+5B	No. 14	Red		
13	-15 V	No. 18	Blue		
14	-5 V	No. 18	Brown		
15	-15B	No. 18	White		

 Table 2-2
 Power Connector Signal Assignments for DD11-CK

#### 6-Pin Mate-N-Lok

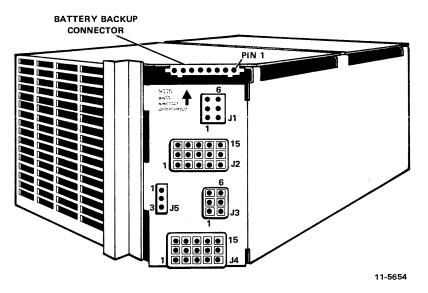
Pin	Signal	Wire	Color	
1 2 3 4 5	LO GND LTC (line clock) DC LO AC LO Spare (not connected) Spare (not connected)	No. 14 No. 18 No. 18 No. 18 -	Black Brown Violet Yellow -	

#### 2.5 INSTALLATION

#### 2.5.1 Backplane Installation

The BA11-L can house a double system unit backplane (DD11-DK) or up to two single system unit backplanes (DD11-CK). The DD11-DK is mounted into the BA11-L by four bolts, two at each edge of the backplane. Two bolts mount the DD11-CK, one bolt at each edge (Figure 2-1).

The power harness from the backplane(s) plugs into the power distribution board of the H777 (Figure 2-11). With a double system unit backplane, connectors J2, J3, and J4 are used; with a single system unit, J3 and J4 are used. If two single system units are mounted into the BA11-L, one power harness plugs into J3 and J4 and the other plugs into J1 and J2. The two 6-pin connectors (J1 and J3) are wired in parallel as are the two 15-pin connectors (J2 and J4). Connector J5 is the power control (PC) plug discussed in Paragraph 1.5.



H777 POWER SUPPLY

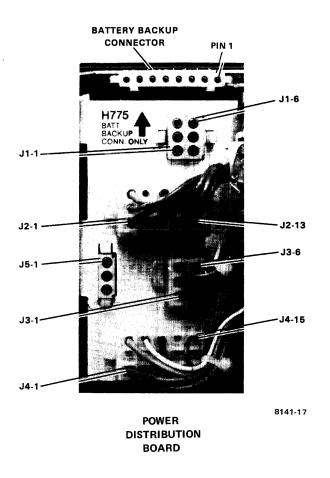
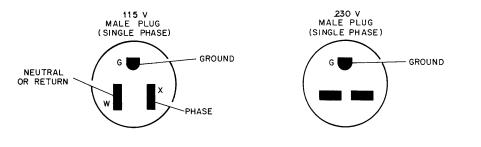


Figure 2-11 Power Distribution Board

#### **2.5.2** Electrical Requirements

The BA11-L can be operated from a 115/230 Vac  $\pm$  10 percent, 47 to 63 Hz power source. The primary power outlets at the installation site must be compatible with the BA11-L primary power input connectors or compatible with the primary input connectors of the 861 power controller if the system is cabinet mounted.

Two types of connectors are used with the BA11-L depending on whether the power supply is configured for 115 Vac or 230 Vac operation (Table 1-1). Figure 2-12 shows the plug portion of each connector and a table provides specifications for both plugs and receptacles.



CONNECTOR SPECIFICATIONS

DESCRIPTION	NEMA * CONFIGURATION	POLES	WIDES	PLUG	RECEPTACLE
			Intes	DEC PART NO.	DEC PART NO.
115V, 15 AMP	5-15	2	3	90-08938	12 - 0535 1
230V, 15 AMP	6-15	2	3	90-08853	12- 11204

\* ADD P SUFFIX FOR PLUG ADD R SUFFIX FOR RECEPTACLE

11-2572

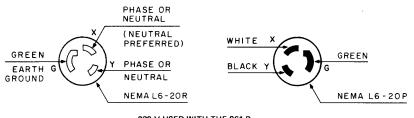
Figure 2-12 Connector Specifications for BA11-L

If the BA11-L is used as an expander box, the 861 power controller is used. The power control requires different primary connections from those used with the BA11-L. The 861-C power controller is used for 115 Vac operation and the 861-B is used for 230 Vac operation. Figure 2-13 illustrates these connectors and the associated table provides connector specifications.

The BA11-L 3-prong power connector, when inserted in a properly wired receptacle, should ground the BA11-L mounting frame. If the integrity of the ground is questionable, the user is advised to measure the potential between the mounting frame and a known ground with a voltmeter.

#### WARNING

The H777 power supply in the BA11-L provides two green wires which are chassis ground. The green wire in the front should be used to ground the console and the green wire in the back should be used to ground the rack in which the BA11-L is installed.



230 V USED WITH THE 861-B



115 V USED WITH THE 861-C

CONNECTOR	SPECIFICATIONS

MODEL			PLUG	RECEPTACLE (SUPPLIED BY CUSTOMER)	
NUMBER	POWER	RATING	NEMA CODE	NEMA CODE	DEC PART NO.
861-C	115 V SINGLE PHASE	30 A	L5-30P	L5-30R	12-11191
861-B	230 V SINGLE PHASE	20 A	L6-20P	L6-20R	12-11194

Figure 2-13 Connector Specifications for 861-B and 861-C Power Controllers

# CHAPTER 3 H777 POWER SUPPLY

#### 3.1 GENERAL

This chapter contains mechanical and functional descriptions of the H777 power supply as well as detailed descriptions of its major assemblies (Table 1-3). An electrical interconnection diagram of the major assemblies in the H777 is shown in Appendix A.

#### **3.2 H777 PHYSICAL DESCRIPTION**

Figure 3-1 shows the H777 as it applies to versions CA, CB, DA, and DB. The AA, AB, BA, and BB versions are similar. The versions of the BA11-L are listed in Table 1-1.

The ac control assembly rests in the front of the H777 and is separated from the core, MOS, and +5 V regulators by the fan. The core and MOS regulators are positioned above the heat sink (etched side up) with the core regulator board placed closer to the fan. The +5 V regulator rests underneath the core and MOS regulators and acts as a motherboard, channeling signals to the core and MOS boards.

The regulated outputs of the +5 V and MOS regulators are routed directly to the power distribution board while the core regulator outputs are routed through the +5 V regulator. A ribbon cable which comes out of the +5 V regulator plugs into a connector in the front panel assembly of the BA11-L.

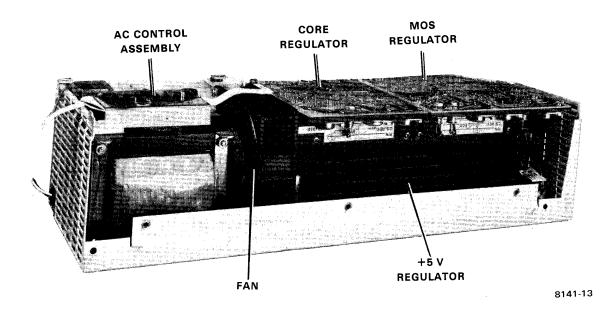


Figure 3-1 H777 Power Supply

### 3.3 H777 FUNCTIONAL DESCRIPTION

Figure 3-2 is a functional block diagram of the H777 which contains the ac control assembly, +5 V regulator, MOS regulator, and a core regulator.

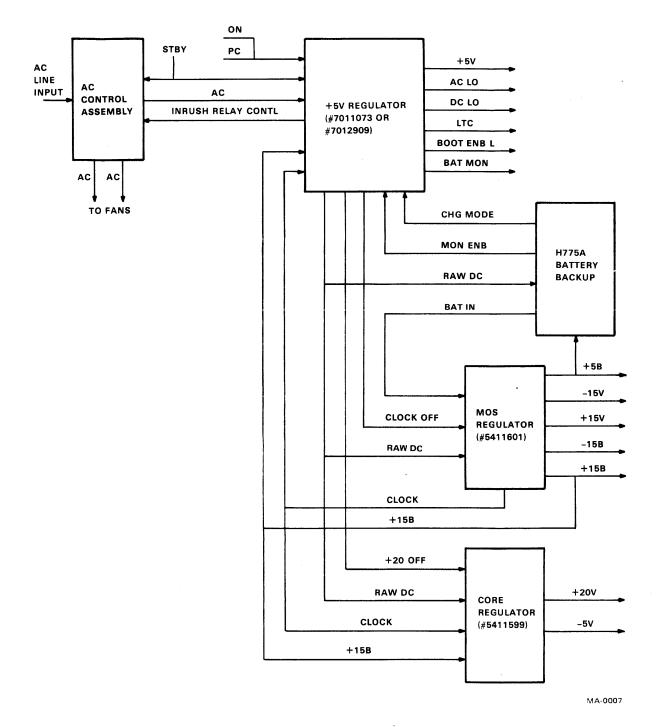


Figure 3-2 H777 Block Diagram

The core regulator is an optional assembly in the H777 that generates +20 V and -5 V which are used by core memory.

The MOS regulator produces +5 V power designated as +5B, and  $\pm 15$  V power designated as  $\pm 15B$ and  $\pm 15$  V. The  $\pm 15B$  and +5B outputs are used to refresh MOS memory in the BA11-L and the  $\pm 15$ V outputs supply power to non-MOS loads. The  $\pm 15B$  outputs also provide the power required by the H777 regulators for internal use. Note that the MOS regulator also generates the clock signal which is a squarewave used to synchronize all the regulators in the H777. The +5 V regulator supplies +5 V power to all the BA11-L loads except the MOS memory refresh circuitry.

The ac line voltage is applied to the ac control assembly which contains a circuit breaker and transformer as well as other ac interface circuitry. The ac control assembly steps down the ac line input to a lower amplitude which is routed to the +5 V regulator and 115 Vac power is provided to the fans.

The +5 V regulator rectifies and filters its ac input yielding an unregulated raw dc output which is used as the source voltage to generate the regulated outputs of the H777. Note that raw dc is generated as long as the ac line voltage is present and the circuit breaker is on.

The +5 V regulator controls Unibus signals AC LO and DC LO, and the CLOCK OFF and +20 OFF lines which enable the MOS and core regulators, respectively. Assume that the raw dc is present. The H777 regulators are turned on when the power control (PC) input is grounded. The STANDBY mode is specified when the PC input is open and the STBY input is grounded (Paragraph 1.5).

A self-contained battery backup unit (H775A) is offered as an option for use with the H777 power supply. During an ac power failure, the H775A provides a battery input voltage to the MOS regulator only, allowing the  $\pm 15B$  and  $\pm 5B$  outputs to stay operational. (The  $\pm 15$  V outputs are cut off.) The status of the battery in the H775A is indicated by BAT MON which controls an LED on the front console of the BA11-L.

### 3.4 DETAILED DISCUSSION

The assemblies in the H777 are discussed in detail in Paragraphs 3.4.1 to 3.4.4. The raw dc circuit, which includes the ac control assembly and part of the +5 V regulator, is discussed in Paragraph 3.4.1.

### 3.4.1 Raw DC Circuit

The circuit shown in Figure 3-3 converts 115 Vac into an unregulated dc voltage, referred to as raw dc (25–48 V). The raw dc is the source voltage used to generate all the regulated voltage outputs in the H777.

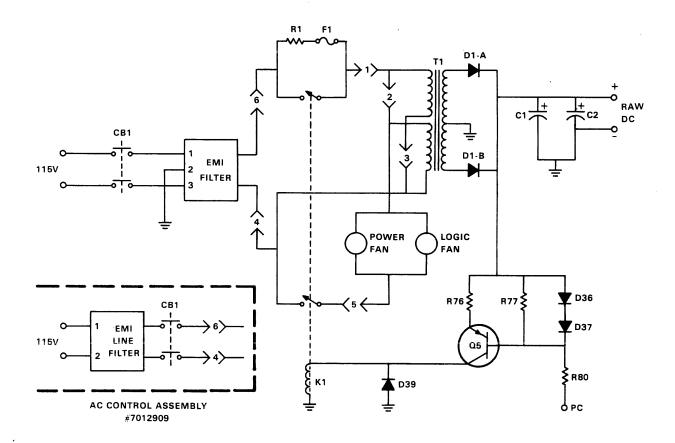
During an ac power turn-on, the ac voltage is applied to transformer T1 via components CB1, the EMI line filter, R1, and F1. The ac line voltage is stepped down by T1 and rectified by D1-A and D1-B and the raw dc voltage appears across C1 and C2.

The remote power control or a power switch on the front panel grounds the PC input. Once raw dc is present, Q5 turns on and K1 is energized, which bypasses R1 and F1 and turns on the 115 V fans.

Resistor R1 prevents the accidental tripping of CB1 during turn on by limiting the inrush current. A 1 A slow blow fuse (F1) protects R1 if K1 malfunctions (opens) while the H777 regulators are operational.

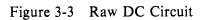
The rectifier diodes (D1-A, D1-B) and the control circuitry for K1 are located on the +5 V regulator board. Capacitors C1 and C2 are located underneath the +5 V regulator board due to their large size. Components CB1, K1, R1, F1, T1, and the EMI line filter are part of the ac control assembly.

The ac control assembly is available in four versions which are listed in Table 3-1.



NOTE: CONNECTIONS SHOWN ARE TO TB2 IN THE AC CONTROL ASSEMBLY

MA-0011



AC Control Assembly	5 V Reg	AC Input (Vac)	Circuit Breaker (CB1)	AC Line Cord	Transformer Jumper Configu- rations on TB2
7011075-00	7011073 (5 V, 25 A Reg)	115	1210191-00 (10 A)	7010131-00	1 and 2 jumpered 3 and 4 jumpered (parallel)
7011075-01	7011073 (5 V, 25 A Reg)	230	1210191-01 (5 A)	7010131-01	2 and 3 jumpered (series)
7012910-00	7012909 (5 V, 32 A Reg)	115	1210191-01 (5 A)	701230-00	1 and 2 jumpered 3 and 4 jumpered (parallel)
7012910-01	7012909 (5 V, 32 A Reg)	230	1210191-01 (5 A)	701230-01	2 and 3 jumpered (series)

 Table 3-1
 AC Control Assemblies

The coils of the transformer primary are connected to the other ac control circuitry via terminal board TB2. In the 115 V versions, the transformer windings are connected in parallel. In the 230 V versions, the transformer windings are connected in series (Figure 3-4).

Figure 3-5 shows the mechanical configuration of ac control assemblies 7011075-00 and 7011075-01. The mechanical configuration of the other two ac assemblies is similar to that shown in Figure 3-5; however, the EMI filter is mounted toward the back of the BA11-L.

### 3.4.2 MOS Regulator (Part 5411601)

The succeeding paragraphs contain functional and detailed circuit descriptions of the MOS regulator which produces  $\pm 15$  V,  $\pm 15B$  and  $\pm 5B$  power. Figure 3-6 is a photograph of the MOS regulator.

**3.4.2.1** Functional Description – Figure 3-7 is a functional block diagram of the MOS regulator. For purposes of discussion only, the MOS regulator is divided into three parts: the  $\pm 15B$  circuit, the +5B circuit, and the clock.

In the  $\pm 15B$  circuit, the pass switch, filter, and controller form a closed loop regulating circuit that produces  $\pm 15$  Vdc and  $\pm 15$  Vdc from an unregulated raw dc voltage (25-48 V). The current limiting circuit protects the  $\pm 15B$  circuit from a current overload. The  $\pm 15B$  outputs supply power to the H777 regulators and the MOS memory in the BA11-L, while the  $\pm 15$  V power for the non-MOS load is supplied via the transistor switches. The start-up circuit supplies  $\pm 12$  V which is used to power the clock and the  $\pm 15B$  circuit during a power-up sequence.

The +5B circuit is similar to the  $\pm 15B$  circuit. The overvoltage crowbar protects the +5B load from excessively high voltage at the filter output due to a +5B circuit malfunction. The +5B output supplies power to MOS memory, the battery monitor circuit in the +5 V regulator, and the optional H775A battery backup.

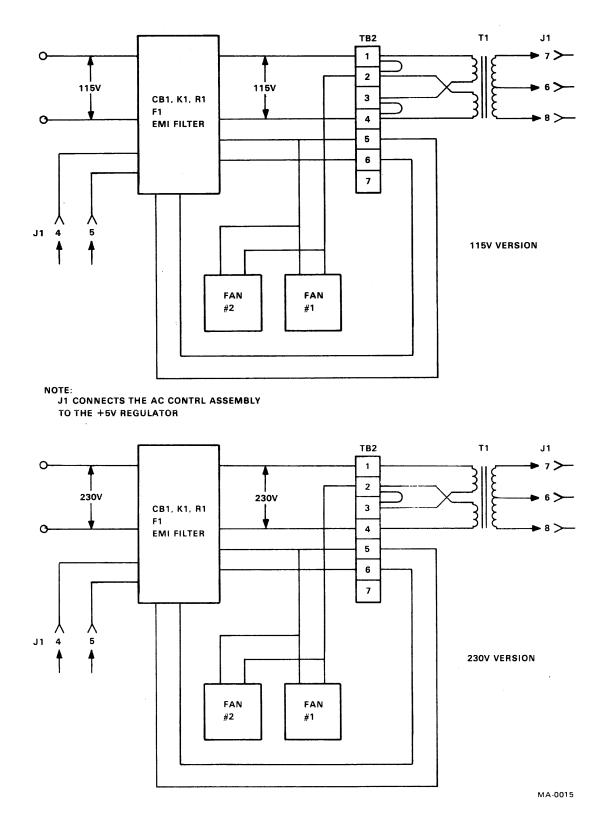


Figure 3-4 115 V and 230 V Transformer Configurations

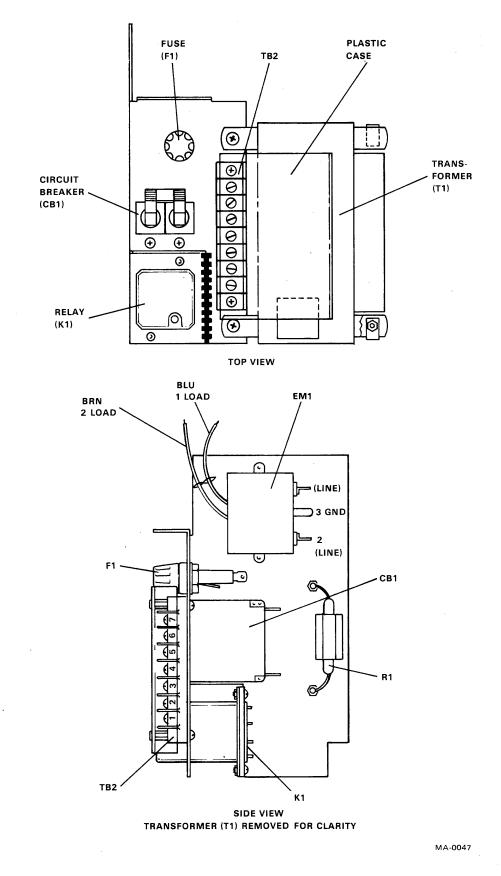
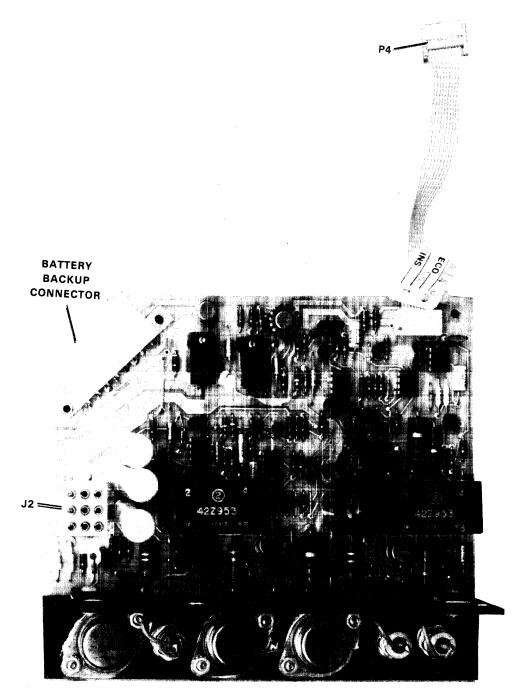
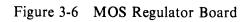


Figure 3-5 AC Control Assembly Mechanical Configuration (7011075)



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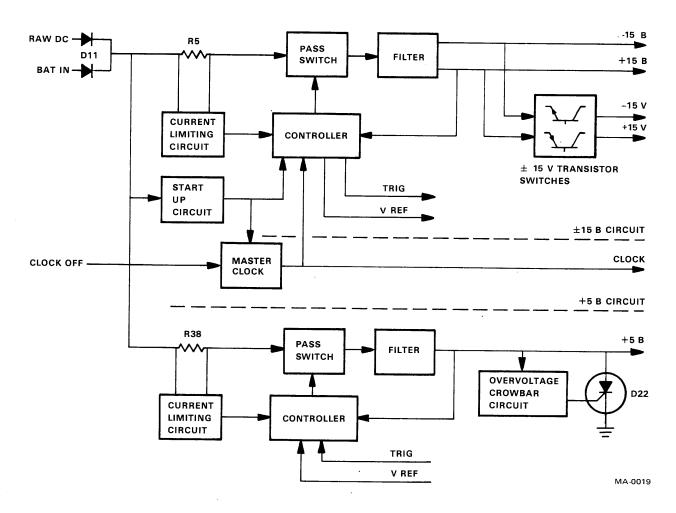


Figure 3-7 MOS Regulator Block Diagram

The clock produces a 0 to +12 V squarewave with a period of 50  $\mu$ s, which is used to synchronize all the switching regulators in the H777.

During an ac power failure, the optional H775A battery backup provides input power to the MOS regulator only. Therefore, only the MOS regulator is operational while the +5 V and core regulators are disabled. However, the  $\pm 15$  V transistor switches are open, cutting off power to the non-MOS loads in the BA11-L during an ac power failure.

**3.4.2.2** Master Clock – The 555 timer, E3, is the major component of the master clock; since the timer is used frequently in the H777, a discussion of its internal operation is presented in the following paragraph.

**555 Timer** (Figure 3-8) – The 555 timer contains two voltage comparators which are used to set and reset a flip-flop. The reference for the comparators is determined by the bias voltage (Vcc) or the control voltage at pin 5. The timer has an open collector output at pin 7 and a buffered output at pin 3 which can source or sink up to 100 mA.

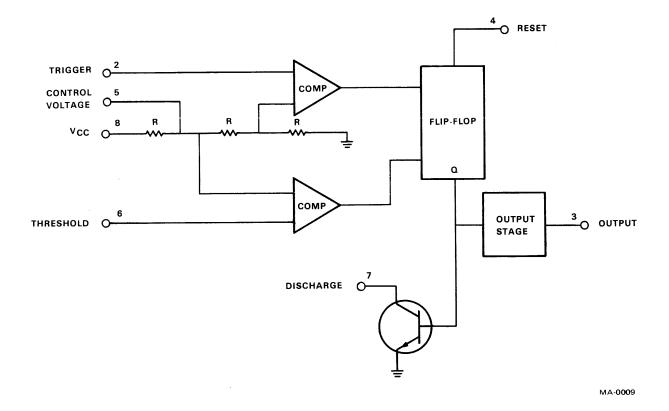


Figure 3-8 555 Timer

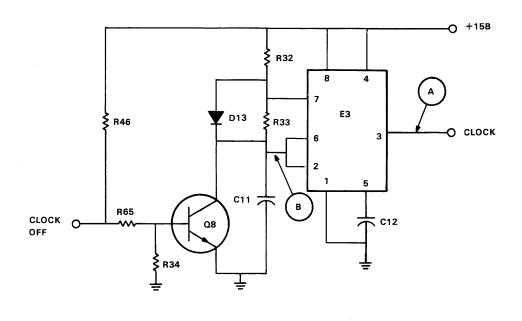
When the trigger input at pin 2 goes below 1/3 of Vcc or 1/2 of the control voltage, the flip-flop is set (pin 3 goes high and the discharge transistor turns on). The flip-flop is reset when the voltage at pin 6 exceeds either the control voltage or 2/3 of Vcc. The timer is also reset by a low voltage level at pin 4. The timer ignores the trigger input if pin 4 is held low.

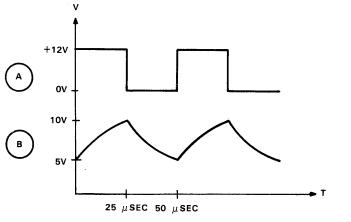
Master Clock Description (Figure 3-9) – A 555 timer (E3), set up as a free running oscillator, generates the master clock output which is a 20 kHz squarewave with an amplitude of 12 V.

In operation, when the timer output (at E3 pin 3) is high, C11 is charged via R32 and D13. The timer is reset when the voltage across C11 equals 10 V (E3 pin 3, goes low and C11 discharges via R33 and the internal discharge transistor at E3 pin 7). When the voltage across C11 equals 5 V, the timer is triggered (E3 pin 3, goes high) and the cycle repeats.

Transistor Q8 is controlled by circuitry in the +5 V regulator via the CLOCK OFF line. If Q8 is turned on, C11 discharges, and the clock output is latched high. All the regulators in the H777 are disabled due to the absence of a squarewave clock output.

3.4.2.3  $\pm 15B$  Circuit Detailed Description – The  $\pm 15B$  circuit shown in Figure 3-10 is discussed in the succeeding paragraphs.





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Figure 3-9 Master Clock

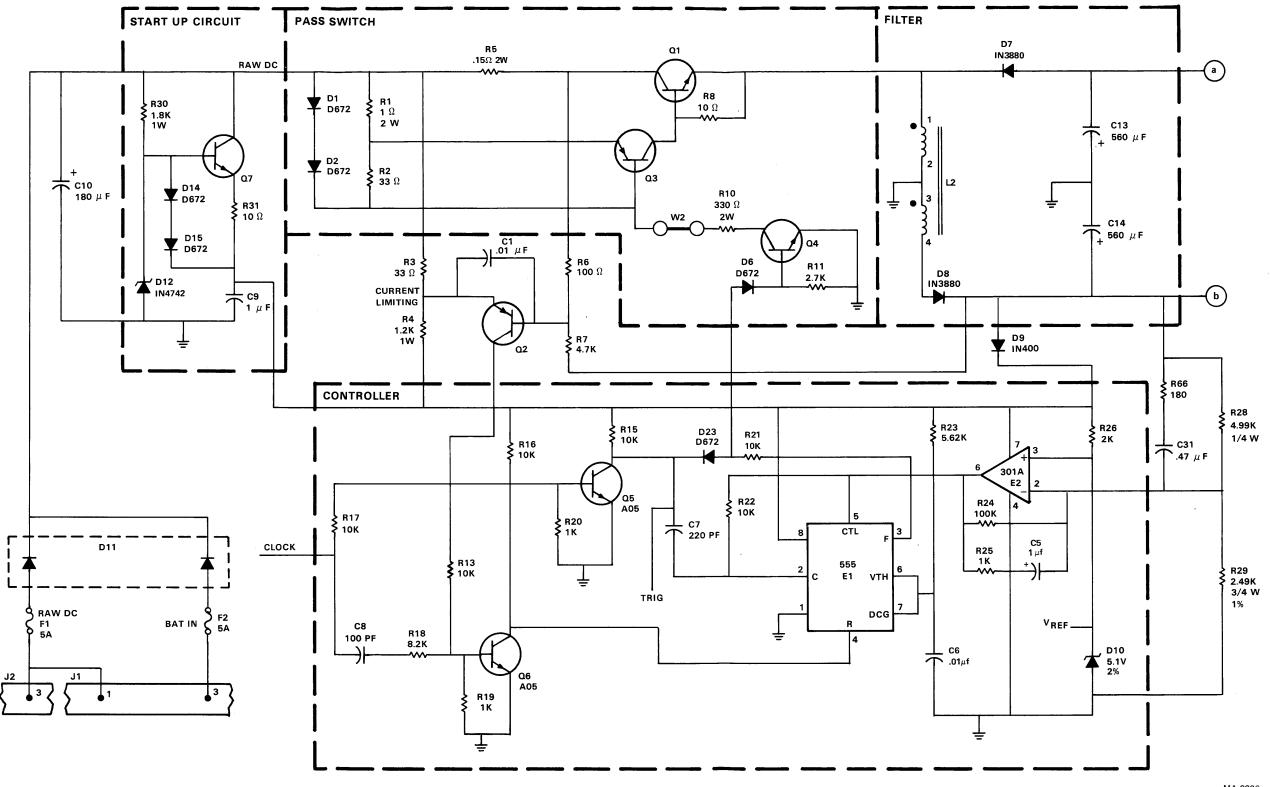


Figure 3-10  $\pm 15B$  Circuit (Sheet 1 of 2)

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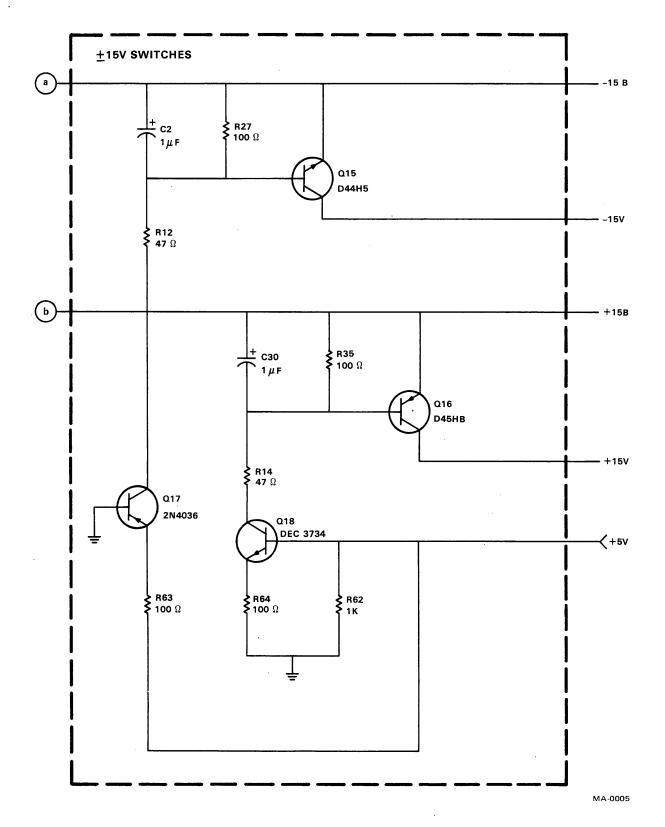


Figure 3-10  $\pm 15B$  Circuit (Sheet 2 of 2)

 $\pm 15B$  Pass Switch and Filter (Figure 3-11) – The pass switch (Q1) is repeatedly turned on and off generating a pulse train across L2. Note that the center tap of L2 is grounded. When current flows through D6, the pass switch is turned on and the raw dc voltage appears across one half of L2 and is reflected across the other half. Diodes D7 and D8 are reverse biased, the inductor current (IL) increases, and current is provided to the load by C13 and C14. Once the pass switch is turned off, D7 and D8 are forward biased and the inductor current (IL) flows into C13, C14, and the load.

The voltage magnitude at both filter outputs (+15B and -15B) is determined by the magnitude of the raw dc voltage and the conduction time of the pass switch. For example, assume that raw dc equals 35 V and that the pass switch conduction time is 21  $\mu$ s during a 50  $\mu$ s period. The voltage magnitude of both filter outputs is approximated as follows.

 $\pm 15B$  voltage magnitude = [35 (21)] / (50) = 14.7 Vdc

In this example, the +15B output is 14.7 Vdc and the -15B output is -14.7 Vdc.

 $\pm 15B$  Controller (Figure 3-12) – The  $\pm 15B$  output is fed back to the controller which regulates the  $\pm 15B$  outputs at  $\pm 15$  V by varying the conduction time of the pass switch. the major components of the controller are the operational amplifier E2 and the 555 timer E1.

Amplifier E2 compares approximately 1/3 of the +15B output to a 5.1 V zener reference voltage and amplifies the difference. The output of E2 is an error voltage which increases (decreases) as the +15B output decreases (increases).

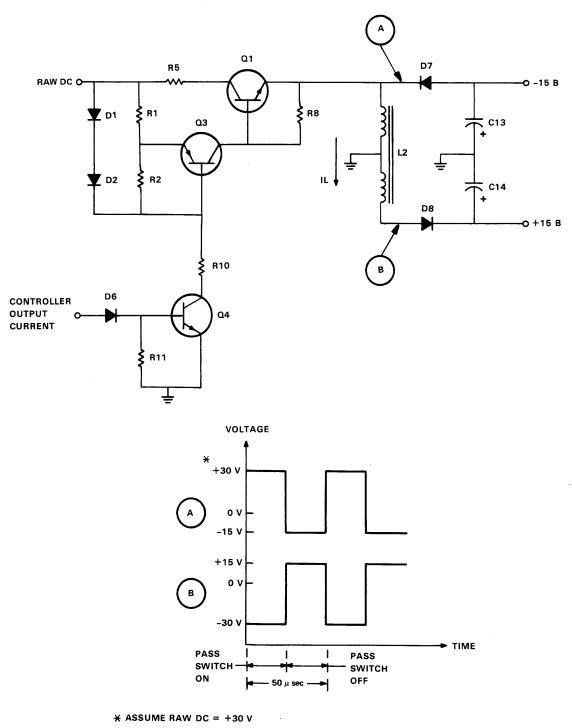
The output of the controller is generated by E1 and is synchronized to the clock signal which is a 0 to +12 V squarewave with a period of 50  $\mu$ s. E1 (the 555 timer) was discussed earlier.

When the clock signal goes high, Q5 is turned on and a negative pulse appears at E1 pin 2, triggering the timer. The timer output at E1 pin 3, is latched to +12 V producing a current in R21 which is bypassed to ground via D23 and Q5 during the time that the clock signal is high. Triggering E1 also turns off the internal discharge transistor at E1 pin 7, and C6 charges toward +15 V along a fixed exponential curve. When the voltage at E1 pin 6, equals the error voltage at E1 pin 5, the timer is reset. (E1 pin 3, goes low and C6 is clamped to approximately 0.6 V because the discharge transistor is on.) Diode D6, shown in Figure 3-10, conducts current and the pass switch is turned on from the time the clock signal goes low until E1 is reset. The conduction time of the pass switch increases (decreases) as the error voltage increases (decreases).

Note that the timer is also reset when Q6 is turned on at the leading (rising) edge of the clock signal. The timer does not react to the trigger pulse at E1 pin 2, until the trailing (rising) edge of the reset pulse at E1 pin 4. Therefore, when the clock goes high, the timer is first reset (ensuring an end to the previous timer cycle) and then triggered (starting a new timer cycle). Refer to Figure 3-13.

During each 50  $\mu$ s clock period, the conduction time of the pass switch is between 0 and 25  $\mu$ s; the exact time is dependent on the error voltage.

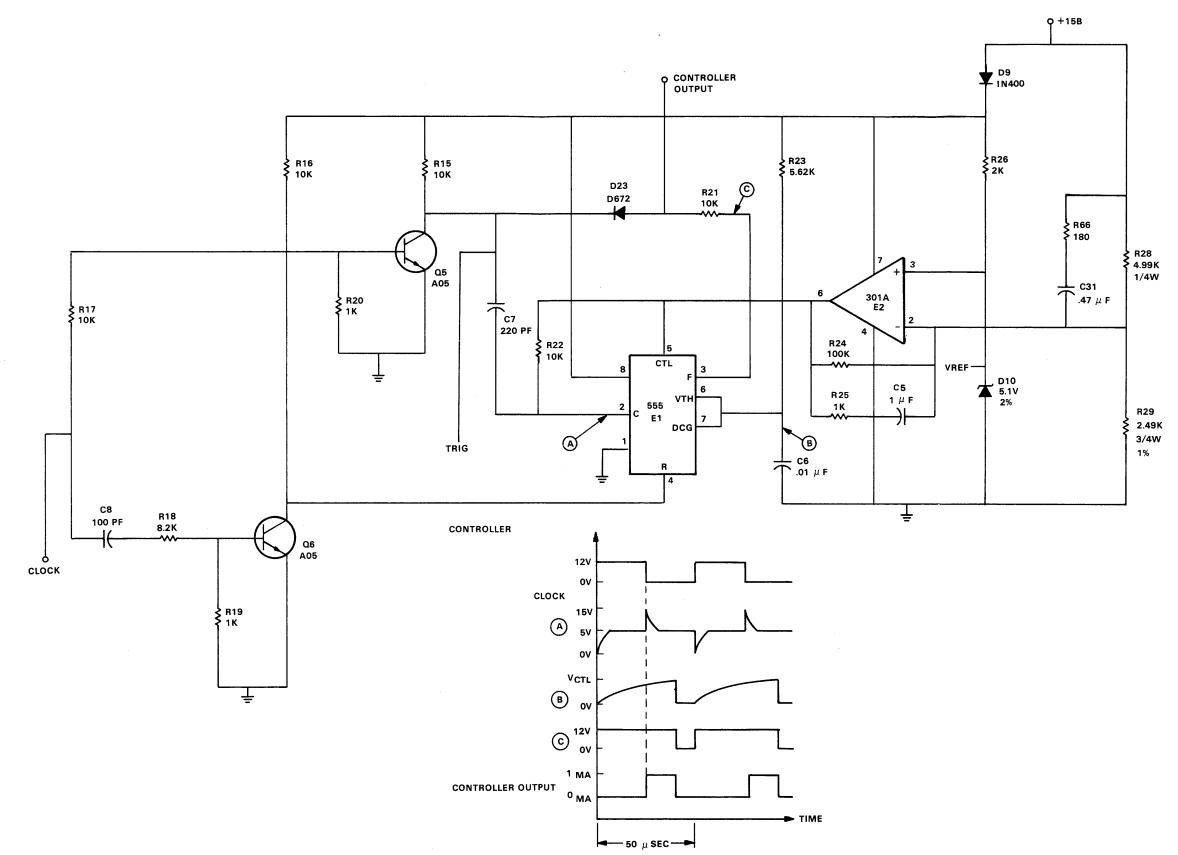
 $\pm 15B$  Current Limiting Circuit (Figure 3-10) – Transistor Q2 is the major component of the current limiting circuit which protects the  $\pm 15B$  circuitry from a current overload. When the pass switch (Q1) is turned on, the inductor current and the voltage drop across R5 increase. If the inductor current reaches approximately 5 A, the voltage drop across R5 is sufficient to turn on Q2. Subsequently, Q6 turns on, resetting the timer (E1). The pass switch turns off and the inductor current decreases; thus, the *peak inductor* current is limited to approximately 5 A. The conduction time of the pass switch is decreased as the overload increases toward 5 A and the voltage decreases (Figure 3-14).



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Figure 3-11 ±15B Pass Switch and Filter

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# Figure 3-12 ±15B Controller

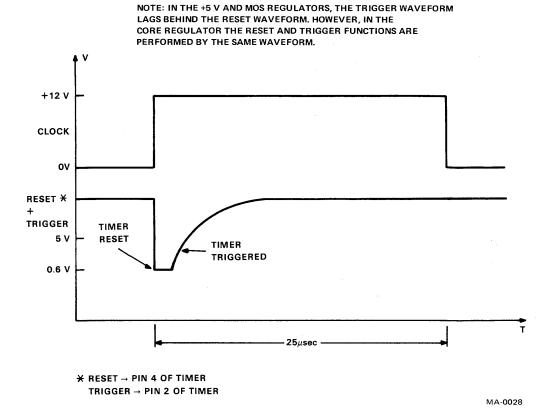
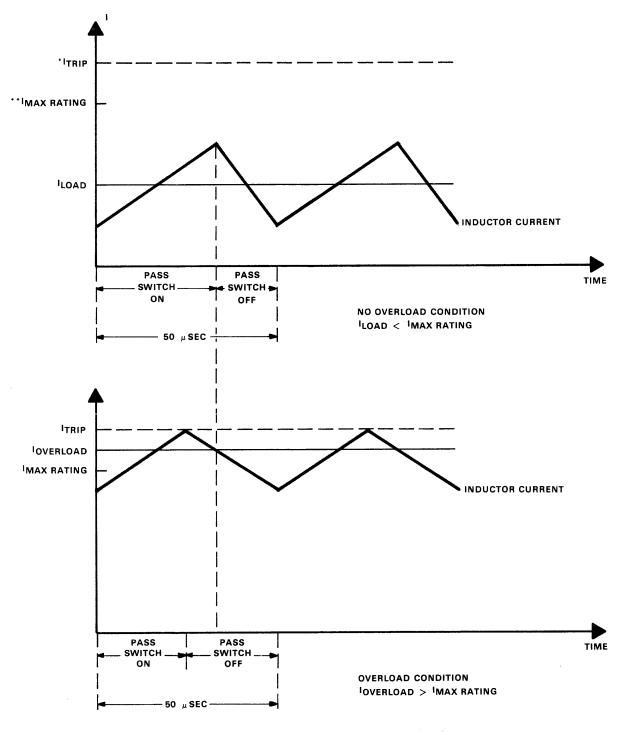


Figure 3-13 Reset-Trigger Sequence Exaggerated Waveform



**'ITRIP IS THE VALUE OF THE INDUCTOR CURRENT AT WHICH THE CURRENT LIMITING CIRCUIT TURNS OFF THE PASS SWITCH** 

\*\*IMAX RATING IS THE MAXIMUM CURRENT THAT CAN BE SUPPLIED TO THE LOAD WITHOUT CAUSING THE PASS SWITCH TO TURN OFF PREMATURELY.

MA-0017

Figure 3-14 Overcurrent Limiting Waveforms

 $\pm 15$  V Transistor Switches (Figure 3-10) – The MOS regulator provides  $\pm 15$  V and  $\pm 15$  V and  $\pm 15$  V power to all BA11-L loads, except MOS memory, via Q15 and Q16. The main  $\pm 5$  V regulator provides  $\pm 5$  V power to Q17 and Q18, which provide the base drive to Q15 and Q16.

When the H777 is in the STANDBY mode, the +5 V regulator is inactive, and Q15 and Q16 turn off, cutting off power to the non-MOS loads. However, the MOS regulator is operational and MOS memory receives refresh power via the  $\pm 15B$  outputs (and +5B output). Therefore, it is possible to service other modules in the BA11-L without losing the contents of MOS memory.

During an ac power failure, the optional H775A battery backup provides input power to the MOS regulator only for a limited time. Therefore, the operation of the H777 is the same as it is in the STANDBY mode. Since the non-MOS loads no longer draw current from the MOS regulator, the battery backup time is maximized.

**Start-Up Circuit** (Figure 3-10) – Zener diode D12 and Q7 are the major components of the start-up circuit. The raw dc voltage is present as long as ac power is supplied to the H777 via its circuit breaker.

The start-up circuit uses the raw dc voltage to produce a regulated  $\pm 12$  V across C9 when the voltage regulators are inactive. The regulated  $\pm 12$  V supplies the power necessary to activate the clock and  $\pm 15B$  circuit during a power-up sequence. The clock and  $\pm 15B$  outputs are needed to power-up the  $\pm 5B$  circuit, the  $\pm 5$  V regulator and the core regulator.

Note that once +15B power has come up, D9 is forward biased and Q7 turns off. The start-up circuit is disabled and power to the clock is provided by the +15B output.

**3.4.2.4** +5B Circuit Detailed Description (Figure 3-15) – The pass switch, filter and controller form a closed loop circuit that produces a regulated +5 V from an unregulated raw dc voltage (25-48 V).

The pass switch (Q9) is repeatedly turned on and off generating a pulse train across D21 at the LC filter input (L1 and C17). When current flows through D19, the pass switch is turned on and the raw dc voltage appears across D21. Diode D21 is forward biased when the pass switch is off, clamping the filter input to approximately -1 V. The output voltage of the filter is equal to the time averaged (dc) value of the voltage across D21.

The conduction time of the pass switch and the magnitude of the raw dc voltage determine the filter output voltage which is the +5B output. For example, assume that raw dc equals 35 V and that the conduction time of the pass switch is 8  $\mu$ s during a 50  $\mu$ s period. The +5B output voltage is approximated as follows.

 $+5B \text{ output} = [(35)(8/50)] + \{(-1)[(50 - 8)/50]\} = 4.76 \text{ Vdc}$ 

The +5B output is fed back to the controller which regulates the +5B output at +5 V by varying the conduction time of the pass switch. The major components of the controller are the operational amplifier E5, and the 555 timer, E4.

Amplifier E5 compares the +5B output to a 5.1 V reference voltage (VREF) and amplifies the difference. (The reference voltage is generated by D10 in the  $\pm 15B$  circuit.) The amplifier output is an error voltage which increases (decreases) as the +5B output decreases (increases).

The output of the controller is generated by E4 and is synchronized to the clock signal which is a 0 to  $\pm 12$  V squarewave with a period of 50  $\mu$ s. E4 (the 555 timer) was discussed previously. The TRIG signal is generated at the collector of Q5 in the  $\pm 15B$  circuit and is  $\pm 15$  V when Q5 is turned off.

When the clock signal goes high, the TRIG signal is clamped to approximately 0.6 V (Q5 on) and a negative pulse appears at E4 pin 2 triggering the timer. The timer output at E4 pin 3 is latched to +12 V, producing a current in R51 which is bypassed to ground via D20 and Q5 during the time that the clock signal is high. Triggering E4 also turns off the internal discharge transistor at E4 pin 7 and C21 charges towards +15 V along a fixed exponential curve. When the voltage at E4 pin 6 equals the error voltage at E4 pin 5, the timer is reset. (E4 pin 3 goes low and C21 is clamped to approximately 0.6 V because the discharge transistor is on.) Diode D19 conducts current and the pass switch is turned on from the time the clock signal goes low until E4 is reset. The conduction time of the pass switch increases (decreases) as the error voltage increases (decreases).

Note that the timer is reset when Q14 is turned on at the leading (rising) edge of the clock signal. The timer does not react to the trigger pulse at E4 pin 2 until the trailing (rising) edge of the reset pulse at E4 pin 4. Therefore, when the clock signal goes high the timer is first reset (ensuring the end of the previous timer cycle) and then triggered (starting a new timer cycle).

During each 50  $\mu$ s clock period, the conduction time of the pass switch is between 0 and 25  $\mu$ s; the exact time is dependent on the error voltage. Waveforms that apply to the +5B controller are shown in Figure 3-12.

Transistors Q10 and Q13 are the major components of the current limiting circuit which protects the +5B circuitry from a current overload. When the pass switch is turned on, the inductor current and the voltage drop across R38 increase. If the inductor current reaches approximately 5 A, the voltage drop across R38 is sufficient to turn on Q10 and, subsequently, Q14 turns on, resetting the timer (E4). The pass switch turns off and the inductor current decreases; thus, the *peak inductor* current is limited to approximately 5 A. The conduction time of the pass switch is decreased as the overload increases toward 5 A. The current supplied to the load is limited to approximately 4 A and the +5B output voltage decreases. Waveforms that apply to the +5B current limiting circuit are shown in Figure 3-14.

As the +5B output voltage decreases below VREF (5.1 V), the current flow through Q13 and R39 increases and therefore, the voltage drop across R38 required to turn on Q10 decreases. The peak inductor current level and thus the current available to the load decreases as the +5B output voltage decreases. Refer to Figure 3-16.

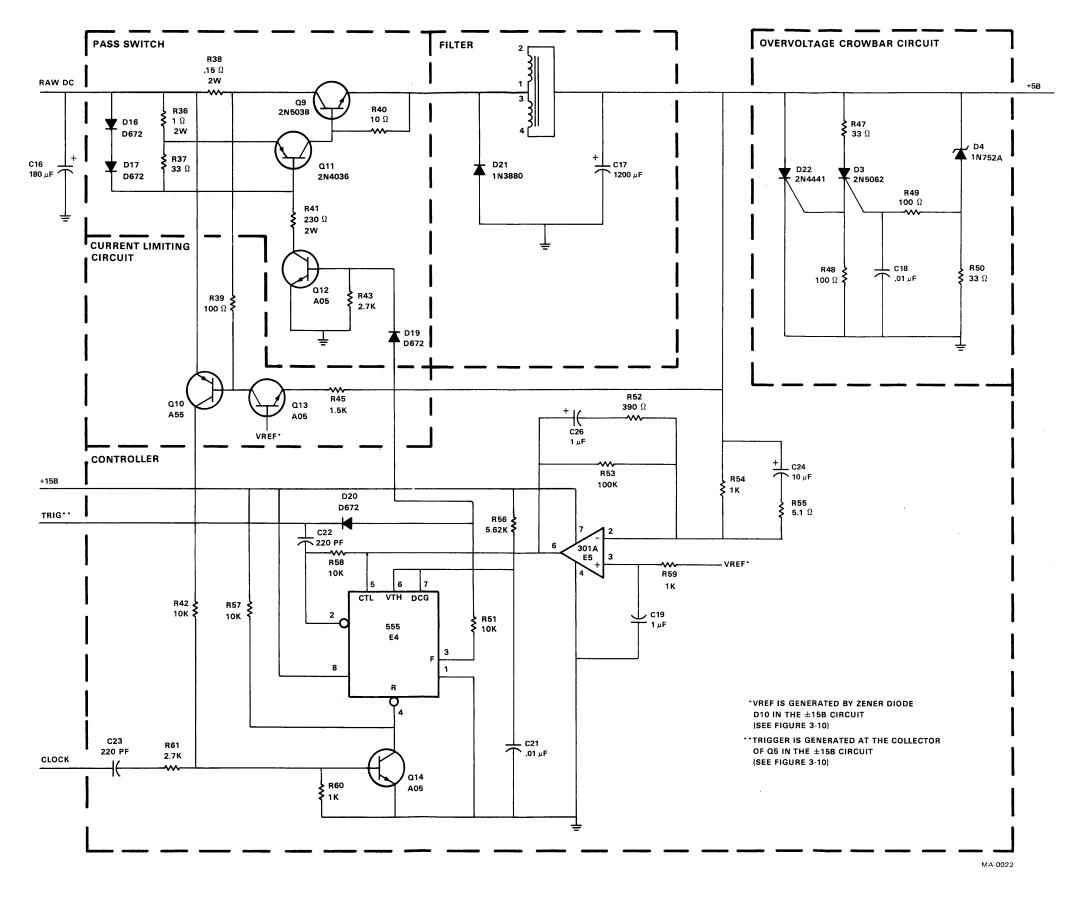
+5B Overvoltage Crowbar Circuit (Figure 3-15) – Zener diode D4 and silicon controlled rectifiers (SCR) D22 and D3 are the major components of the overvoltage crowbar circuit which protects the +5B load from excessively high voltage at the fliter output (i.e., raw dc appears at the filter output due to a pass switch failure).

With the +5B filter output in the 5.6–6.5 V range, D4 conducts and the voltage difference between the output and the zener voltage (5.6 V) appears across R50. Current flows into the gate of D3 so that D3 and, subsequently, D22 are fired. Once fired, D22 bypasses the output current to ground and clamps the output voltage to approximately 1 V.

The SCR (D22) will keep conducting until its anode current falls below approximately 75 mA for approximately 50  $\mu$ s.

#### 3.4.3 Core Regulator (Part 5411599)

The core regulator (Figure 3-17) produces two voltages, +20 V and -5 V, that are used by core memory. The succeeding paragraphs contain functional and detailed descriptions of the core regulator circuitry.



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Figure 3-15 +5B Circuit

3-23

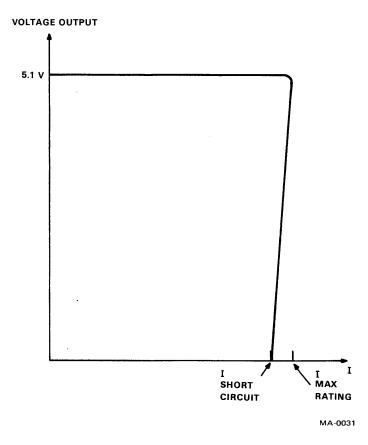
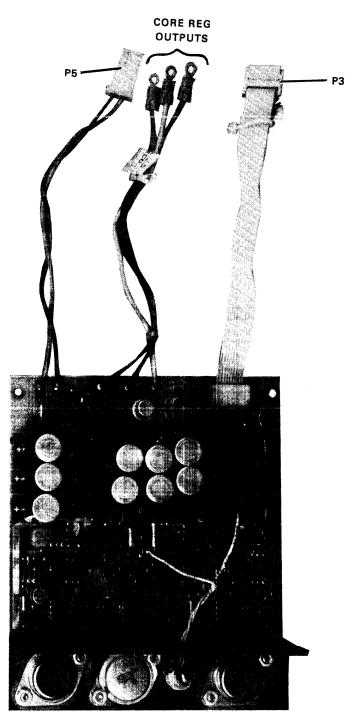


Figure 3-16 Current Foldback



8141-18

Figure 3-17 Core Regulator Board

**3.4.3.1** Functional Description – Figure 3-18 is a functional block diagram of the core regulator. For purposes of discussion, the core regulator is divided into two parts: the +20 V circuit and the -5 V circuit.

In the +20 V circuit, the pass switch, filter and controller form a closed loop circuit that produces +20 V from an unregulated raw dc voltage (25–48 V). The current limiting circuit protects the +20 V circuit from a current overload, and the overvoltage crowbar circuit protects the +20 V *load* from excessively high voltage at the filter output due to a +20 V circuit malfunction.

The -5 V circuit is similar to the +20 V circuit.

**3.4.3.2** +20 V Circuit Detailed Description (Figure 3-19) – The pass switch (Q2) is repeatedly turned on and off generating a pulse train across D8 at the LC filter input (L1, C4, C20, C21 and C22). When current flows through D5 and D6, the pass switch is turned on and the raw dc voltage appears across D8. Diode D8 is forward biased when the pass switch is turned off, clamping the filter input to approximately -1 V. The output voltage of the filter is equal to the time averaged (dc) value of the voltage across D8.

The magnitude of the raw dc voltage and the conduction time of the pass switch determine the filter output voltage. For example, assume that raw dc equals 35 V and that the conduction time of the pass switch is 29  $\mu$ s during a 50  $\mu$ s period. The filter output voltage is approximated as follows.

Filter output voltage =  $[(35)(29/50)] + \{(-1)[(50 - 29)/50]\} = 19.88$  Vdc

The filter output voltage is fed back to the controller that regulates the filter output at +20 V by varying the conduction time of the pass switch. The major components of the controller are operational amplifier, E1, and the 555 timer E2.

Amplifier E1 compares approximately 1/4 of the filter output voltage to a 5.1 V zener reference and amplifies the difference. The amplifier output is an error voltage which increases (decreases) as the filter output decreases (increases).

The output of the controller is generated by E2 and is synchronized to the clock signal which is a 0 to +12 V squarewave with a period of 50  $\mu$ s. E2 (the 555 timer) was discussing previously.

When the clock signal goes high, Q6 is momentarily turned on and the timer is first reset and then triggered. Once triggered, the timer output at E2 pin 3 is latched to +12 V producing a current in R14, D5 and D6, and the pass switch turns on. Triggering E2 also turns off the internal discharge transistor at E2 pin 7 and C8 charges towards +15 V along a fixed exponential curve. When the voltage at E2 pin 6 equals the error voltage at E2 pin 5, the timer is reset. (E2 pin 3 goes low, the pass switch turns off, and the voltage across C8 is clamped to approximately 0.6 V, because the discharge transistor is on.) The conduction time of the pass switch increases (decreases) as the error voltage increases (decreases).

Note that if the error voltage is very high, the timer is not reset until Q6 turns on. The timer does not react to a trigger input at E2 pin 2 until the trailing (rising) edge of the reset input at E2 pin 4. Therefore, when the clock goes high the timer is first reset (ensuring an end to the previous timer cycle) and then triggered (starting a new timer cycle).

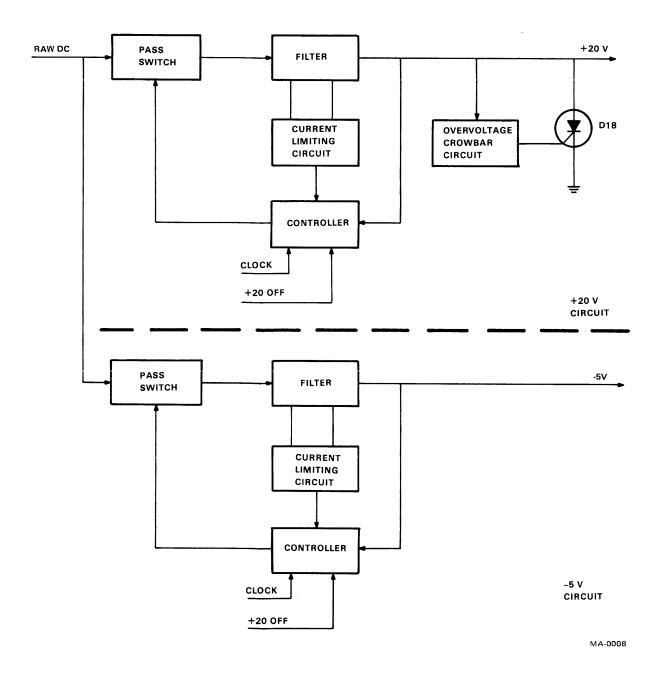
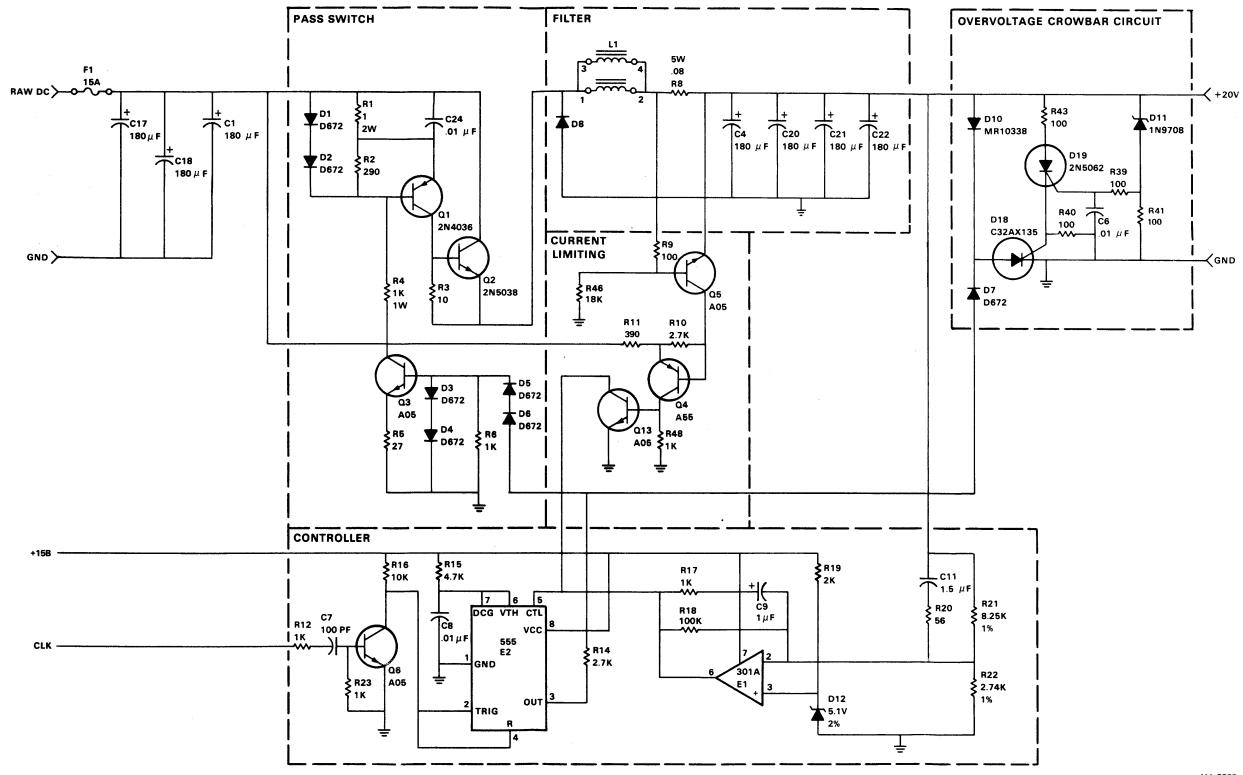


Figure 3-18 Core Regulator Block Diagram



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Figure 3-19 +20 V Circuit

Transistors Q5, Q4, and Q13 are the major components of the current limiting circuit that protects the +20 V circuitry from a current overload. The inductor current and the voltage drop across R8 increase when the pass switch is on and decrease when the pass switch is off. If the inductor current reaches approximately 8.8 A during pass switch on time, the voltage drop across R8 is sufficient to turn on Q5; subsequently Q4 and Q13 also turn on. The error voltage at E2 pin 5 is clamped to approximately 0.6 V and is lower than the voltage at E2 pin 6, so the timer is reset. The pass switch is turned off and the *peak inductor* current is limited to approximately 8.8 A. The conduction time of the pass switch is decreased as the overload increases toward 8.8 A. The current output available to the load is limited to approximately 6 A and the output voltage decreases. Waveforms that apply to the +20 V current limiting circuit are shown in Figure 3-14.

Zener diode D11 and SCRs D18 and D19 are the major components of the overvoltage crowbar circuit which protects the +20 V load from an excessively high voltage at the filter output (i.e., raw dc appears at the filter output due to a pass switch failure).

If the filter output voltage becomes higher than approximately 24 V, D11 conducts and the voltage difference between the output voltage and the zener voltage (24 V) appears across R41. Current flows to the gate of D19 so that D19 and, subsequently, D18 are fired. Once D18 is fired, the output load current is bypassed to ground and the output voltage is clamped to approximately 1.6 V.

The SCR (D18) conducts until its anode current falls below approximately 75 mA for approximately 50  $\mu$ s.

**3.4.3.3** -5 V Circuit Detailed Description (Figure 3-20) – The pass switch, filter and controller form a closed loop circuit that produces a regulated –5 V from an unregulated raw dc voltage (25–48 V).

The pass switch (Q10) is repeatedly turned on and off, generating a pulse train across L2. When current flows into the base of Q9, the pass switch is turned on and the raw dc voltage appears across L2. Diode D17 is reverse biased, the inductor current increases, and current to the load is provided by C5 and C16. When the pass switch is turned off, D17 is forward biased and the inductor current flows into the load.

The voltage magnitude at the filter output is determined by the magnitude of the raw dc voltage and the conduction time of the pass switch. For example, assume that raw dc equals 35 V and that the pass switch conduction time is 7  $\mu$ s during a 50  $\mu$ s period. The voltage magnitude at the filter output is approximated as follows.

Voltage magnitude at filter output = (35)(7/50) = 4.9 Vdc

In this example the filter output voltage is -4.9 Vdc.

The filter output voltage is fed back to the controller which regulates the filter output at -5 V by varying the conduction time of the pass switch. The major components of the controller are operational amplifier E3 and the 555 timer E4.

Amplifier E3 compares the filter output voltage to a -5.1 V reference generated across D13, and amplifies the difference. Zener diode D22 (Vz = 12 V) acts as a level shifter. The control voltage at E4 pin 5 has a positive polarity, while the op amp output varies around the -5 V level. The control voltage increases (decreases) as the filter output voltage becomes less (more) negative.

The controller output is generated by E4 and is synchronized to the clock signal which is a 0 to +12 V squarewave with a period of 50  $\mu$ s. E4 (the 555 timer) was discussed previously.

When the clock signal goes high, Q6 is momentarily turned on and the timer is first reset and then triggered. Once triggered, the timer output at E4 pin 3 is latched to +12 V producing a current in R29 which is bypassed to ground via Q7 during the time that the clock signal is high (Q7 turned on). Triggering E4 also turns off the internal discharge transistor at E4 pin 7 and C14 charges towards +15 V along a fixed exponential curve. When the voltage at E4 pin 6 equals the control voltage at E4 pin 5, the timer is reset. (E3 pin 3 goes low and C14 is clamped to approximately 0.6 V because the discharge transistor is on.) Current flows into the base of Q9, and the pass switch is turned on from the time the clock signal goes low until E4 is reset. The conduction time of the pass switch increases (decreases) as the control voltage increases (decreases). Note that if the control voltage is very high, the timer is not reset until Q6 is turned on. The timer does not react to a trigger input at E4 pin 2 until the trailing (rising) edge of the reset input at E4 pin 4. Therefore, when the clock goes high, the timer is first reset (ensuring an end to the previous timer cycle) and then triggered (starting a new timer cycle).

During each 50  $\mu$ s clock cycle, the conduction time of the pass switch is between 0 and 25  $\mu$ s; the exact time is dependent on the control voltage. Waveforms that apply to the -5 V controller are shown in Figures 3-12 and 3-13.

Transistor Q12 is the major component of the current limiting circuit which protects the -5 V circuitry from a current overload. The inductor current and the voltage across R37 increase when the pass switch is on and decrease when the pass switch is off. If the inductor current reaches approximately 7.5 A during pass switch on time, the voltage across R37 is sufficient to turn on Q12. The control voltage at E4 pin 5 is clamped to approximately 0.6 V and is lower than the voltage at E4 pin 6, so the timer is reset. The pass switch is turned off and the *peak inductor* current is limited to approximately 7.5 A. As the overload increases towards 7.5 A, the conduction time of the pass switch is decreased and the filter output voltage becomes less negative. Waveforms that apply to the -6 V current limiting circuit are shown in Figure 3-14.

### 3.4.4 +5 V Regulator (Parts 7011073 and 7012909)

The following paragraphs contain functional and detailed circuit descriptions of the +5 V regulator. The +5 V regulator exists in two versions; part 7011073 provides 25 A of +5 V power and part 7012909 provides 32 A of +5 V power. Figure 3-21 shows the 25 A version of the +5 V regulator. The circuit descriptions apply to both the 25 A and 32 A regulators.

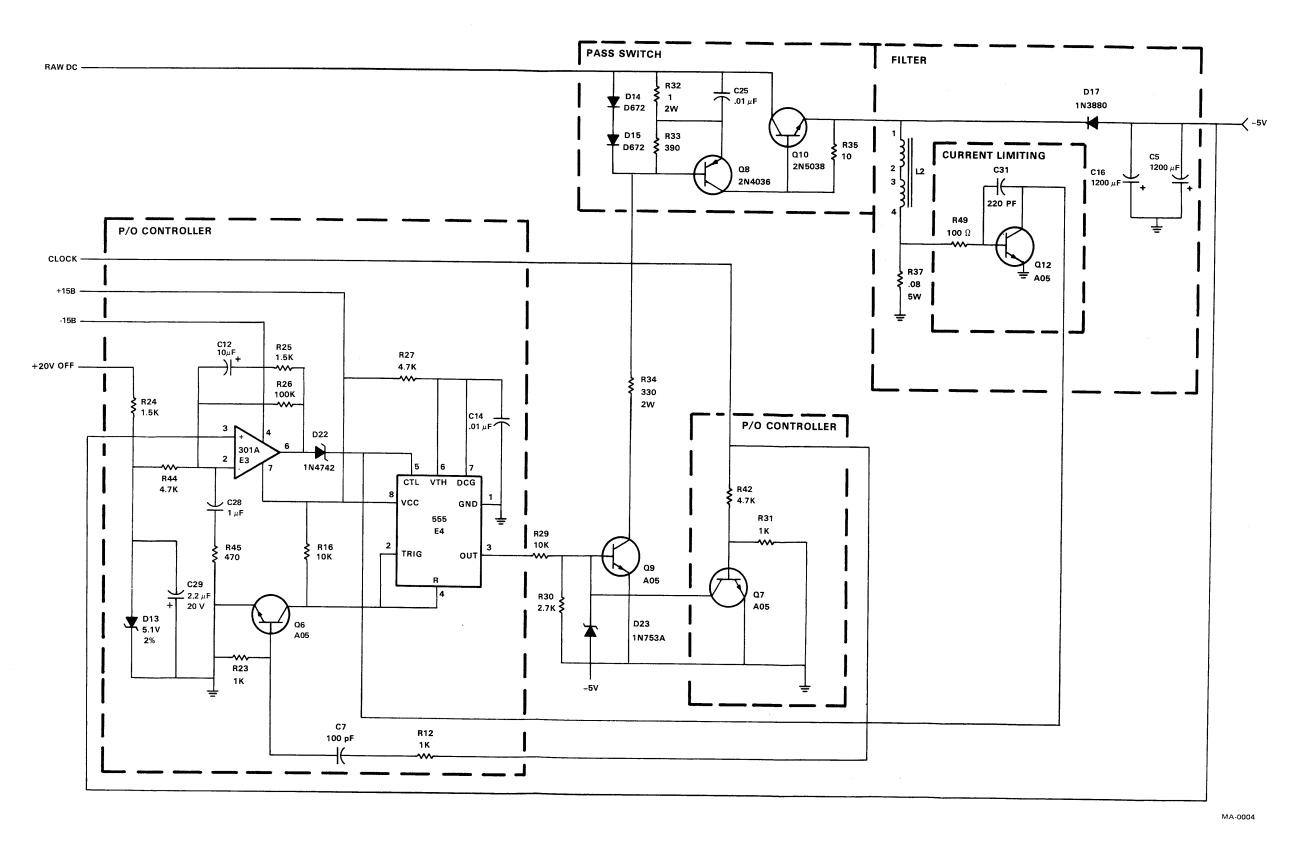
**3.4.4.1 Functional Description** – Figure 3-22 is a functional block diagram that applies to the 25 A and 32 A versions of the +5 V regulator.

The input to the +5 V regulator is a stepped down ac voltage which is rectified and filtered, producing an unregulated raw dc voltage which is used by all the regulators in the H777. The pass switch, filter and controller form a closed loop circuit that produces a regulated +5 V from the unregulated raw dc voltage (25-48 V). The current limiting circuit protects the +5 V regulator from a current overload, and the overvoltage crowbar circuit protects the 5 V *load* from excessively high voltage at the filter output due to a regulator malfunction.

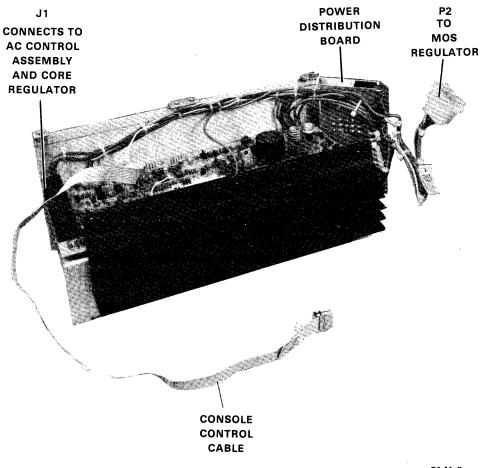
Control signals used to power-up (or power-down) the voltage regulators in the H777 are provided by the power sequence control circuit, which also controls Unibus signals AC LO and DC LO.

The status of the battery in the H775A is interpreted by the battery monitor circuit in the +5 V regulator. An LED on the front console of the BA11-L indicates the battery status by flashing at different rates.

The +15B output of the MOS regulator is monitored by the boot enable circuit which signals the system to reboot by asserting BOOT ENB L if the +15B output drops below +13 V. Due to the  $\pm$ 15B power drop, the MOS memory may have lost its contents and therefore it is necessary to reboot the system during the next power-up sequence.

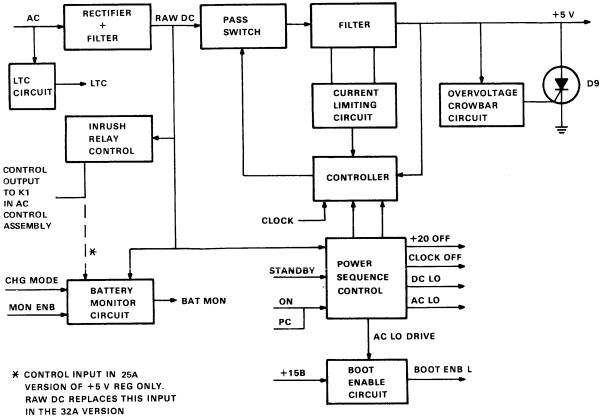


## Figure 3-20 -5 V Circuit



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Figure 3-21 +5 V Regulator (7011073)



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Figure 3-22 +5 V Regulator Block Diagram

**3.4.4.2** +5 V Circuit Detailed Description – The circuitry shown in Figure 3-23 produces a regulated +5 V and has a current drive capability of 25 A. The 32 A version of the +5 V regulator contains circuitry similar to that shown in Figure 3-23.

The +5 V circuit consists of the following functional blocks:

- 1. Pass switch
- 2. Filter
- 3. Controller
- 4. Current limiting circuit
- 5. Overvoltage crowbar circuit.

The circuitry listed is discussed in succeeding paragraphs and applies to both the 25 A and 32 A versions of the +5 V regulator.

+5 V Pass Switch and Filter (Figure 3-23) – Due to the higher current output of the +5 V regulator, the pass switch consists of two power transistors (Q1 and Q2), which are turned on when current flows through D16 and D17. Transistor Q6 and T1 amplify the input current to a level that is sufficient to drive Q1 and Q2. Components Q3, R1, D4, and D3 form a fixed current source that regulates the base drive to Q1 and Q2 at approximately 2 A. Once D16 and D17 no longer conduct, Q6 and Q3 turn off. Transformer T1 reverses polarity, producing a current in D26, D2, and R3 which quickly dissipates the stored charge in Q1 and Q2. Therefore, transistors Q1 and Q2 are turned off rapidly. Resistors R5 and R6 are replaced by a BALUN transformer in the 32 A regulator.

In operation, the pass switch (Q1 and Q2) is repeatedly turned on and off generating a pulse train across D6 at the LC filter input (L1 and C5). When the pass switch is turned on, the raw dc voltage appears across D6. When the pass switch is off, D6 is forward biased clamping the filter input to approximately -1 V. The output voltage of the filter is equal to the time averaged (dc) value of the voltage across D6.

The magnitude of the raw dc voltage and the conduction time of the pass switch determine the filter output. For example, assume that raw dc equals 35 V and that the conduction time of the pass switch is 8  $\mu$ s during a 50  $\mu$ s period. The filter output voltage is approximated as follows.

Filter output voltage =  $[(35)(8/50)] + \{(-1)[(50 - 8)/50]\} = 4.76$  Vdc

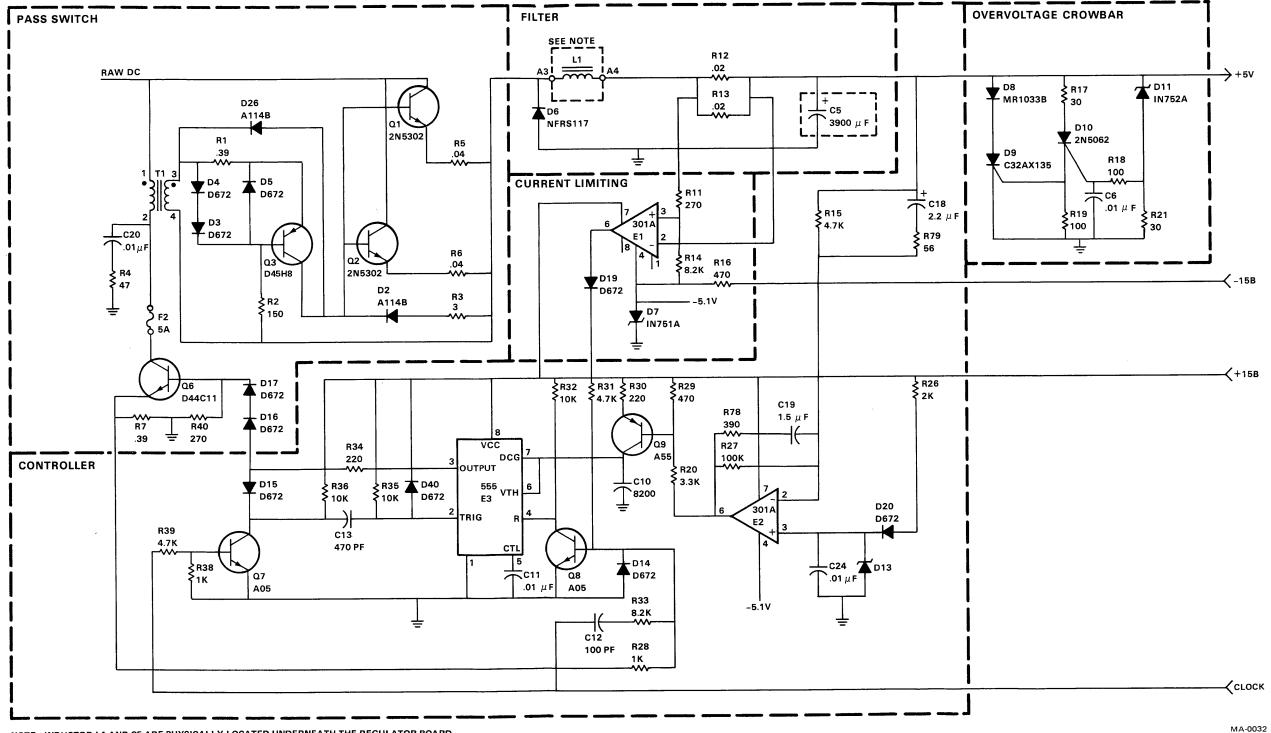
+5 V Controller (Figure 3-23) – The filter output voltage is fed back to the controller which regulates the filter output at +5 V by varying the conduction time of the pass switch. The major components of the controller are the operational amplifier, E2, and the 555 timer, E3.

Amplifier E2 compares the filter output to a 5.1 V zener reference and amplifies the difference. The amplifier output is an error voltage which increases (decreases) as the filter output decreases (increases).

The output of the controller is generated by E3 and is synchronized to the clock which is a 0 to +12 V squarewave with a period of 50  $\mu$ s. E3 (the 555 timer) was discussed earlier in the chapter.

When the clock signal goes high, Q7 is turned on, and a negative pulse appears at E3, pin 2, triggering the timer. The timer output at E3, pin 3, is latched to +12 V, producing a current in R34, which is bypassed to ground via D15 and Q7 during the time that the clock signal is high.

Triggering E3 also turns off the internal discharge transistor at E3, pin 7, allowing C10 to be charged by the constant current provided by Q9. When the voltage at E3, pin 6, equals 10 V, the timer is reset. (E3 pin 3 goes low and C10 is clamped to approximately 0.6 V because the discharge transistor is on.)



NOTE: INDUCTOR L1 AND C5 ARE PHYSICALLY LOCATED UNDERNEATH THE REGULATOR BOARD.

Figure 3-23 +5 V Circuit

Diodes D16 and D17 conduct current, and the pass switch is turned on from the time the clock signal goes low until E3 is reset. Note that the error voltage at E2, pin 6, affects the emitter current of Q9 and thus the rate at which voltage increases across C10. An increase (decrease) in error voltage results in an increase (decrease) in the conduction time of the pass switch.

Note that the timer is also reset when Q8 is turned on at the leading (rising) edge of the clock signal. The timer does not react to a trigger pulse at E3, pin 2, until the trailing (rising) edge of the reset pulse at E3, pin 4. Therefore, when the clock signal goes high, the timer is first reset (ensuring an end to the previous timer cycle) and then triggered (starting a new timer cycle).

During each 50  $\mu$ s clock period, the conduction time of the pass switch is between 0 and 25  $\mu$ s; the exact time is dependent on the error voltage. Refer to Figures 3-24 and 3-13.

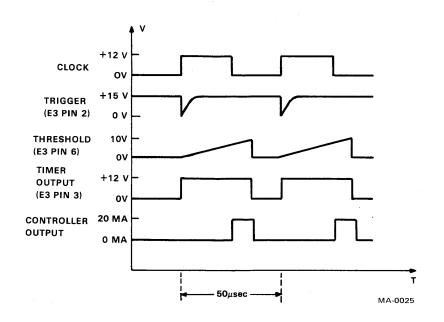


Figure 3-24 +5 V Controller Waveforms

+5 V Current Limiting Circuit (Figure 3-23) – Operational amplifier E1 is the major component of the current limiting circuit which protects the +5 V regulator from a current overload. The following discussion applies to both the 25 A and 32 A versions of the +5 V regulator although current values given apply to the 25 A version unless stated otherwise.

Operational amplifier E1 is used as a voltage comparator. The non-inverting (+) input voltage is determined by D7, R14, R11, and the voltage at point A4. The inverting (-) input voltage is determined by the voltage drop across R12 and R13 which are in series with L1. The inductor current increases when the pass switch is on, decreases when the pass switch is off, and varies around the current level supplied to the load.

If the inductor current reaches approximately 32 A during pass switch on time, the inverting (-) input voltage of E1 becomes less positive than the non-inverting (+) input voltage.

The E1 output goes positive (approximately +13 V), D19 is forward biased and Q8 turns on, resetting the timer (E3). The pass switch turns off and thus the *peak inductor* current is limited to approximately 32 A. The conduction time of the pass switch is decreased as the overload increases toward 32 A. The current supplied to the load is limited to approximately 25 A and the regulator output voltage decreases. Waveforms that apply to the +5 V current limiting circuit are shown in Figure 3-14.

A decrease in regulator output voltage causes a decrease in the non-inverting (+) input voltage at E1 so the inductor current required to trip E1 is also decreased. Therefore, the peak inductor current and the current supplied to the +5 V load decreases as the regulator output voltage decreases. Refer to Figure 3-16.

+5 V Overvoltage Crowbar Circuit (Figure 3-23) – Zener diode D11 and silicon controlled rectifiers D9 and D10 are the major components of the overvoltage crowbar circuit which protects the +5 V load from an excessively high voltage at the filter output (i.e., raw dc appears at the filter output due to a pass switch failure).

If the filter output voltage becomes higher than approximately 5.6 V, D11 conducts and the voltage difference between the output voltage and the zener voltage (5.1 V) appears across R21. Current flows to the gate of D10, so that D10 and, subsequently, D9 are fired. Once D9 is fired, the load current is bypassed to ground and the regulator output voltage is clamped to approximately 1.6 V.

The SCR (D9) conducts until its anode current falls below approximately 75 mA for approximately 50  $\mu$ s.

**3.4.4.3** Power Sequence Control Circuit Detailed Discussion (Figure 3-25) – The +5 V regulator contains a power sequence control circuit that provides control signals to power-down (or power-up) the voltage regulators in the H777. Unibus signals AC LO and DC LO are also controlled by the power sequence control circuit.

Line drivers Q14, Q13, Q12 and Q15 are N channel JFETs; Q14 and Q13 control the AC LO and DC LO lines respectively, and Q12 and Q15 control the +5 V regulator. The core regulator is controlled via the +20 OFF output. The MOS regulator is turned off when the master clock output is no longer a squarewave (Q8 turned on).

An N channel JFET of this type conducts current between drain and source at a gate-to-source voltage of approximately 0 V. A negative gate-to-source bias (-13 V) turns off the JFET, resulting in an essentially infinite impedance between drain and source. The line drivers are controlled by operational amplifiers E4, E5, and E6 which are used as voltage comparators. Zener diode D45 generates a 5.1 V reference voltage at the non-inverting (+) input of each amplifier. The inverting (-) inputs of E4, E5, and E6 are taken from the resistor network formed by R42, R43, R44, and R45 which divides down the voltage across C14. Transistor Q11 charges C14 to the raw dc voltage level. The operation of the power sequence control circuit is based on the voltage level across C14.

If the ac power goes down, the raw dc voltage decreases exponentially due to the capacitors across the output of the raw dc circuit. Diode D30 is forward biased and C14 discharges resulting in a power down sequence. Each amplifier output (i.e., E6) goes positive when its inverting (-) input falls below the reference voltage.

The line drivers are turned on in sequence, grounding the control lines. Signal AC LO is grounded first, approximately 5 ms later DC LO is grounded, and then the +5 V and core regulators are turned off (Figure 3-26).

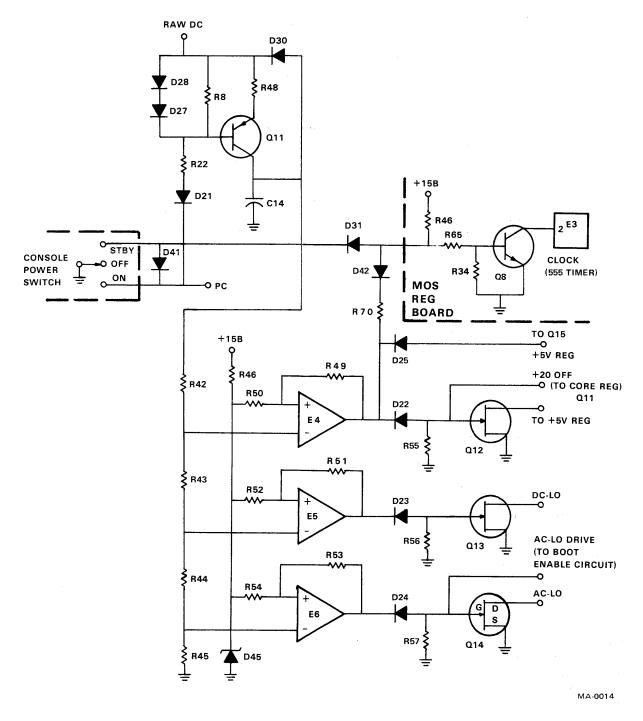


Figure 3-25 Power Sequence Control Circuit

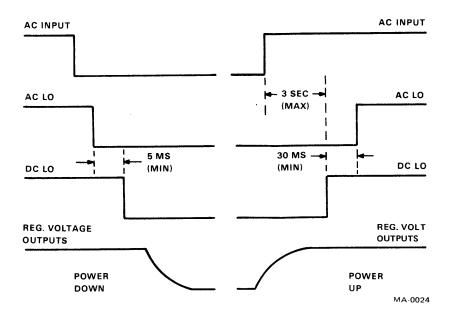
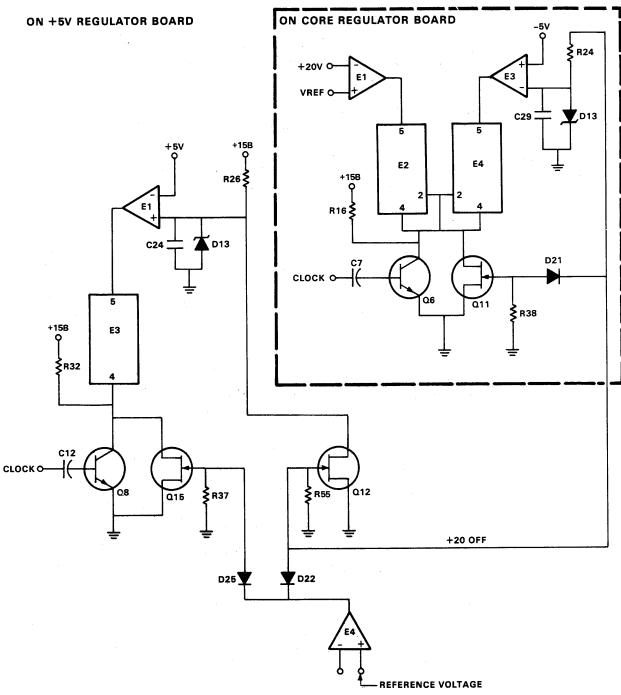


Figure 3-26 Power Up/Down Sequence

A power-down sequence is also initiated when the cathode of D21 is no longer grounded. Transistor Q11 turns off and the voltage across C14 decreases exponentially. Note that once the output of E4 goes positive, D42 is reverse biased. If the power supply is in the STANDBY mode, D31 is forward biased, Q8 stays off, and the master clock stays on. Therefore the MOS regulator remains on while the +5 V and core regulators are off. The MOS regulator is turned off at the same time that the +5 V and core regulators are turned off if the H777 is in the OFF mode.

Note that if the console power switch is not present, a power sequence can be initiated by the remote power controller via the PC input. Operation of the remote power controller is described in Paragraph 1.5. Placing a jumper plug between ground and the STBY input on the front console specifies the STANDBY mode when the H777 is powered down by the remote power control.

The power sequence control circuit turns off the +5 V and core regulators in the following manner (refer to Figure 3-27). When the output of E4 goes positive, Q15, Q12, and Q11 are turned on. The 555 timers, E3 in the +5 V regulator, and E2 and E4 in the core regulator, are reset by grounding pin 4. The pass switches in the +5 V and core regulators are turned off, and the output voltages (+5 V, +20 V and -5 V) decay to 0 V. Note that the reference voltages generated by D13 also fall to approximately 0 V.



MA-0037

Figure 3-27 Power Up/Down Control of Core and +5 V Regulators

3.4.4. Battery Monitor Circuit – The H777 power supply can operate with an optional battery backup unit (H775A) which provides a battery voltage input to the MOS regulator only during an ac power failure. Therefore, while the +5 V and core regulators are disabled, the MOS regulator can provide refresh power to MOS memory for a limited time. The battery in the H775A is charged by the raw dc voltage when ac power is present.

The status of the battery in the H775A is interpreted by the battery monitor circuit in the +5 V regulator. An LED on the front console of the BA11-L indicates the battery status by flashing at different rates.

The 25 A and 32 A versions of the +5 V regulator use different circuitry to accomplish the battery monitor function. The two circuits are discussed separately in the following paragraphs.

**Battery Monitor Circuit (25 A Version 7011073)** – The +5 V, 25 A regulator contains the battery monitor circuit shown in Figure 3-28. Transistors Q16 and Q17 are turned on, and the LED is lit if any output of E9 is low and if the monitor enable (MON EN) signal is low. As long as the H775A is turned on and its internal battery is not dead, the MON EN signal is held low.

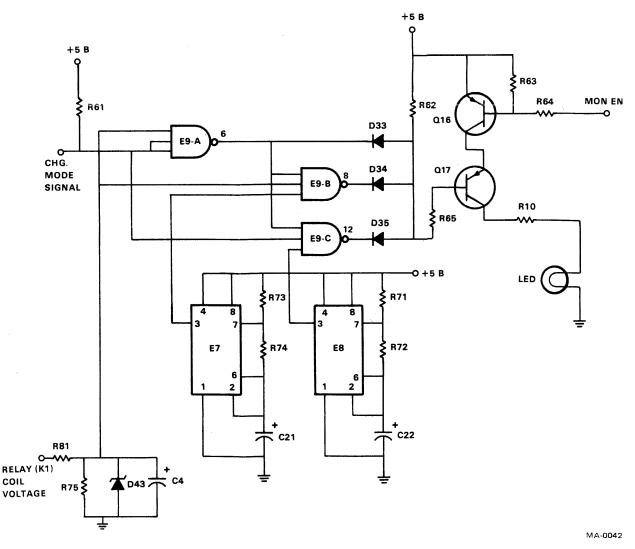


Figure 3-28 Battery Monitor Circuit in 25 A Regulator

The 555 timers, E7 and E8, are used as oscillators. Their outputs are squarewaves with frequencies of 0.5 Hz and 5 Hz respectively and are gated through E9-B and E9-C. The NAND gates in E9 are enabled by the charge mode signal from the H775A and the voltage across the coil of relay K1 in the raw dc circuit. The two enabling signals have the following meaning:

CHG MODE IS LOW	Battery is charging and is at less than 90 percent of charge ca- pacity at present.
CHG MODE IS HIGH	<ol> <li>Battery is charging and is at over 90 percent of charge capacity at present.</li> <li>Battery is discharging</li> </ol>
VOLTAGE ACROSS COIL OF K1 IS HIGH	The H777 is turned on or in standby.

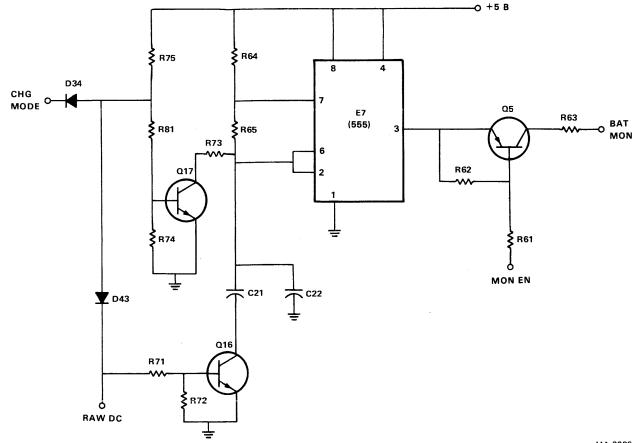
The operation of the battery monitor circuit is summarized in Table 3-2.

CHG Mode	Voltage Across Coil of Relay K1	State of LED	Battery Status Indicated
Low	Low	Off	Battery is dead or H775A is off
Low	High	Flashing Slow (1/2 Hz)	Battery charge less than 90% of capacity and increasing.
High	Low	Flashing Fast (5 Hz)	Battery is discharging
High	High	On	Battery charge is over 90% of capacity and increasing.

 Table 3-2
 Battery Monitor Operation in 25 A Regulator

**Battery Monitor Circuit (32 A Version 7012909)** – The 555 timer, E7, is the major component of the battery monitor circuit shown in Figure 3-29. The timer is used as an oscillator with a squarewave output at E7, pin 3, when Q17 is off. As long as the H775A is turned on and its internal battery is not dead, signal monitor enable (MON EN) is held low and the LED is lit when E7, pin 3, is high.

Transistors Q16 and Q17 are controlled by the raw dc voltage and the charge mode signal from the H775A. Transistor Q16 is used to change the frequency of the timer output which is 5 Hz when Q16 is off, and 0.5 Hz with Q16 on. (C21 and C22 are held in parallel when Q16 is on.) Note that when Q17 is turned on, the trigger input at E7 pin 2 is clamped low and therefore the timer output is held high.



MA-0026

Figure 3-29 Battery Monitor Circuit in 32 A Regulator

The charge mode signal and raw dc indicate the following.

CHG MODE IS LOW	Battery is charging and is at less than 90 percent of charge capacity at present.
CHG MODE IS HIGH	<ol> <li>Battery is charging and is at over 90 percent of charge capac- ity at present</li> <li>Battery is discharging</li> </ol>
Raw DC IS LOW	AC power has failed.

The operation of the battery monitor circuit is summarized in Table 3-3.

MON EN	CHG Mode	Raw DC	State of LED	Interpretation of Battery Status
High	X	X	Off	Battery is dead or H775A is off
Low	Low	High	Flashing Slow (1/2 Hz)	Battery charge less than 90% of capacity and increasing
Low	High	Low	Flashing Fast (5 Hz)	Battery is discharging
Low	High	High	On	Battery charge is over 90% of capacity and increasing.

Table 3-3	Batterv N	Ionitor (	<b>Operation</b> i	in 3	32 A	Regulator
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X = Don't care state

**3.4.4.5** Boot Enable Circuit (Figure 3-30) – The boot enable circuit asserts BOOT ENB L signal if the  $\pm 15B$  output of the MOS regulator falls below approximately 13 V (i.e., during a power failure or if the H777 is in the OFF mode). A reboot operation is performed during a power-up sequence if BOOT ENB L is asserted. Due to the  $\pm 15B$  power drop, the MOS memory may have lost its contents and therefore it is necessary to reboot the system.

The major components of the boot enable circuit are JFET Q4 and programmable unijunction transistor (PUT) Q19. As long as Q19 conducts, the gate-to-source voltage of Q4 is negative, and thus Q4 is turned off. Zener diode D38 (Vz = 13 V) is used as a level shifter.

If the +15B regulator output falls below approximately 13 V, Q18 becomes forward biased and the cathode of Q19 is clamped to approximately 0.6 V. The PUT (Q19) turns off and Q4 is turned on, clamping BOOT ENB L to ground.

Signal AC LO DRIVE is derived from the gate of the AC LO line driver shown in Figure 3-25. During a power-up sequence, when AC LO is negated, AC LO DRIVE is negative and D35 is forward biased. Current flows out of the gate of Q19 turning it on and Q4 is turned off. Thus, BOOT ENB L is negated when AC LO is negated.

**3.4.6** Line Time Clock (LTC) Circuit (Print Set Drawing 35411597-0-1) – This circuit is contained in the +5 V regulator. The LTC output is generated by Q10, from an ac input taken from one leg of the full wave rectifier D1. The LTC output is a 0 to 5 V squarewave which has the same frequency as the ac line voltage (47 to 63 Hz). The squarewave is available at the power distribution board and can be used to power a real-time clock.

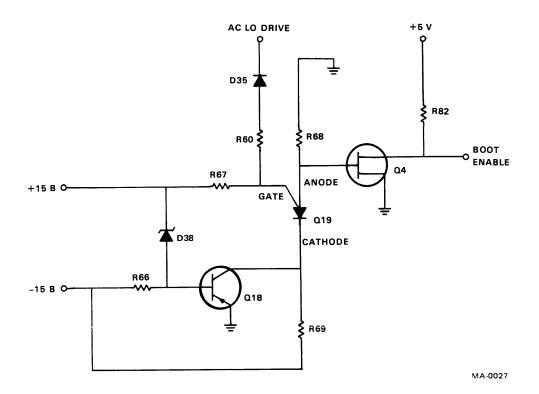


Figure 3-30 Boot Enable Circuit

# CHAPTER 4 H775A BATTERY BACKUP UNIT

#### 4.1 GENERAL

A self-contained battery backup unit, the H775A, is offered as an option for use with the H777 power supply. During an ac power failure, the H775A provides a battery input voltage to the MOS regulator only allowing the  $\pm 15B$  and  $\pm 5B$  outputs to stay operational. Therefore, the MOS regulator provides refresh power to MOS memory for a limited time after an ac power failure has occurred.

The battery backup is provided by two 12 V, 5 Ah batteries connected in series. In this chapter, for purposes of discussion, the two batteries are referred to as one 24 V battery rated at 120 Wh. Due to protective circuitry in the H775A, the battery is not allowed to discharge completely. The battery can supply up to 54 W instantaneously, and will support 32K of MOS MS11-JP memory (28 W) for a minimum of 2 hours.

When ac line voltage is present, the battery is charged by the raw dc voltage via the charging circuitry in the H775A. Battery recharge time is 14–16 hours.

Externally accessible terminals are provided for the addition of an external battery pack if longer holdup time is necessary (over two hours). Refer to Paragraph 4.3.

#### 4.2 PHYSICAL DESCRIPTION

The H775A shown in Figure 4-1 is housed in a rectangular box which measures 13.5 cm high by 10.8 cm long by 48 cm wide (5-1/4 in high by 4-1/4 in long by 19 in wide) and can be rack mounted.

A PC board containing the charging circuitry rests on a panel which is above the batteries. The batteries are electrically connected to the PC board at J3 and J4.

The ON-OFF switch is located on the front of the box and is a 2-pole magnetic circuit breaker with relay contacts which provides input and output overcurrent protection (10 A). The circuit breaker is electrically connected to the PC board at J2. Refer to Figure 4-2.

All input/output connections between the H777 and the H775A are made through one cable. The cable is terminated at the top connector on the H777 power distribution board and an 8 pin connector on the battery backup designated as J1. Refer to Figure 4-3.

An external battery can be electrically connected to the H775A by two binding posts designated as J5 and J7.

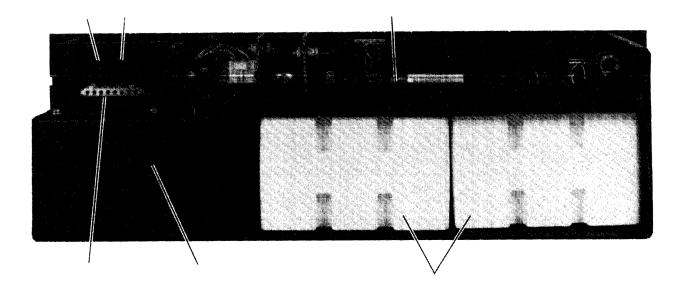


Figure 4-1 H775A Battery Backup Unit (Rear View)

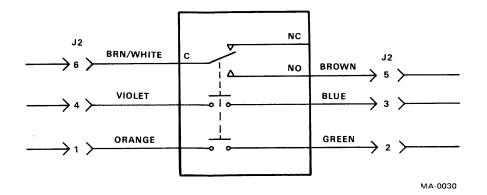
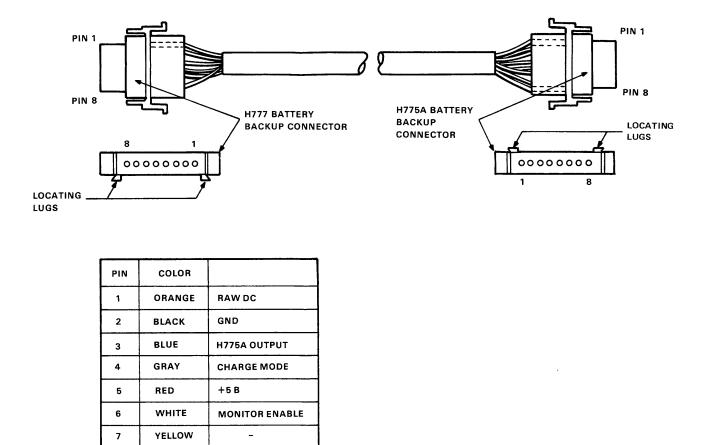


Figure 4-2 Input/Output Circuit Breaker



MA-0029

Figure 4-3 H775A Input/Output Cable

#### 4.3 FUNCTIONAL DESCRIPTION

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Figure 4-4 is a block diagram of the H775A battery backup unit. The H775A contains battery charging circuitry which consists of the voltage boost circuit, the regulator circuit, a charge rate switch and the charge rate switch control.

The raw dc voltage from the H777 (25-48 V) is stepped up to 45-48 V by the voltage boost circuit controlled by the regulator circuit.

The charge rate switch control determines the rate at which the battery charges by turning the charge rate switch (Q7) on or off. When the battery is being charged, Q7 is initially turned on yielding a high battery charge current and therefore the battery is charged at a fast rate.

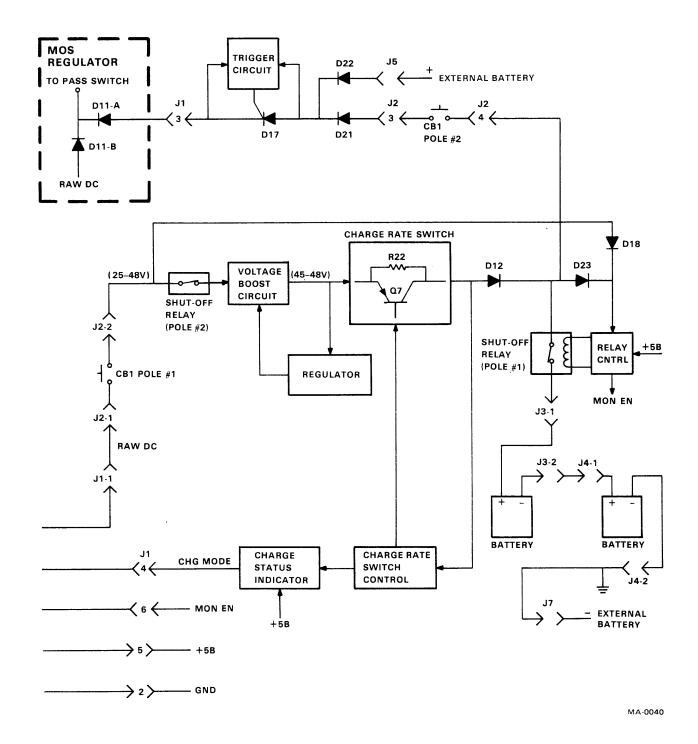


Figure 4-4 H775A Block Diagram

As the battery is charged its voltage increases. Transistor Q7 is turned off when the battery voltage reaches approximately 30.1 V which is equivalent to 90 percent of the battery charge capacity. Charging current is then supplied to the battery via a bypass resistor and the battery charges at a slow rate referred to as a trickle charge. The charge rate switch remains in the trickle mode (Q7 off) when the battery is fully charged.

When the ac line voltage fails, the raw dc voltage drops and the battery discharges. When the raw dc voltage drops below approximately 18 V, the charge rate switch control resets Q7; however, Q7 is not forward biased until the raw dc comes up again. Therefore, at the beginning of a battery charge the charge rate switch is in the fast mode.

The charge status indicator generates the charge mode (CHG MODE) signal which is fed to the battery monitor circuit in the +5 V regulator. The battery monitor circuit uses CHG MODE to determine the status of the battery. Signal CHG MODE is low when the battery is in the fast charge mode and high when the battery is trickle charged or discharging.

The battery backup voltage is provided to the MOS regulator via a silicon controlled rectifier (SCR). When the raw dc voltage drops below approximately 18 V, the trigger circuit fires the SCR and the battery voltage replaces the raw dc as the power source to the MOS regulator only. The SCR is turned off when the raw dc voltage comes up above the battery voltage.

The batteries in the H775A are prevented from discharging completely by the shut-off relay and its control circuit. If the raw dc or the battery voltage is above 18 V, the relay is kept closed by the relay control circuit. However, if the battery is discharging and its voltage decreases to 18 V, the relay opens and therefore the battery current is cut off from its load (the MOS regulator) and the input to the charging circuit is open. The shut-off relay is also opened if either the H777 or the H775A is turned off.

An external battery pack can be connected to the H775A if additional battery support is required (over two hours). However, the external battery is not protected from an overcurrent condition or a deep discharge condition.

#### 4.4 DETAILED CIRCUIT DESCRIPTION

#### 4.4.1 Voltage Boost Circuit

The voltage boost circuit shown in Figure 4-5 is an inductive flyback circuit. Transistors Q1, Q2 and Q3 form a current amplifier. When the regulator output goes high, Q1, Q2 and Q3 turn on, and the raw dc voltage drops across L1. Diode D2 is reverse biased, the inductor current increases, and current to the charge rate switch is provided by C10. When Q1, Q2 and Q3 are turned off, D2 is forward biased and the inductor current flows to the charge rate switch.

Components R2, R3 and Q4 set up a peak current limit. Once the limit has been reached, the voltage across R2 is sufficient to turn on Q4 which resets the regulator, terminating the conduction time of Q1, Q2 and Q3.

#### 4.4.2 Regulator Circuit (Figure 4-6)

The boosted voltage across C10 is fed back to the regulator that keeps the boosted voltage at approximately 48 V by setting the on and off time of transistors Q1, Q2 and Q3. The major components of the regulator are the operational amplifier, E3, and the 555 timers, E1 and E2.

The boosted voltage is divided down by R24 and R18 and compared to a 5.1 V reference voltage by E3 which also amplifies the difference. The output of E3 is an error voltage which increases (decreases) if the boosted voltage decreases (increases). The 5.1 V reference, generated by D4, is also used to bias Q5 and provide power to E1 and E2.

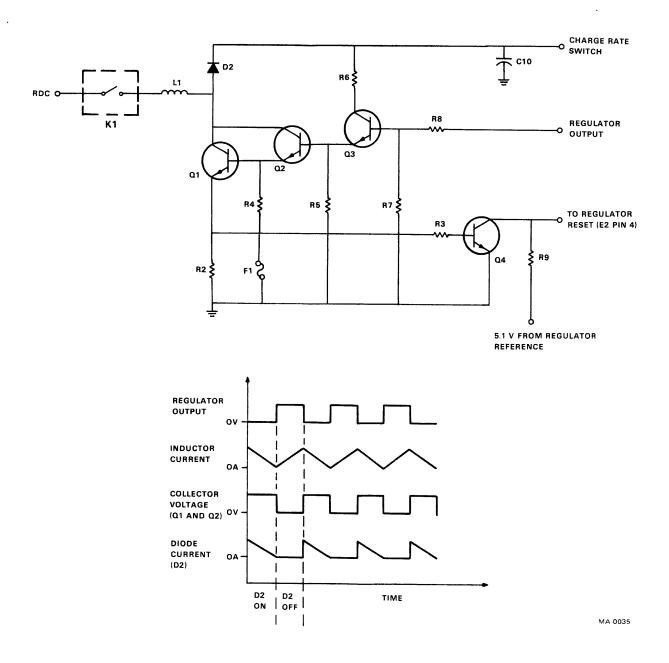
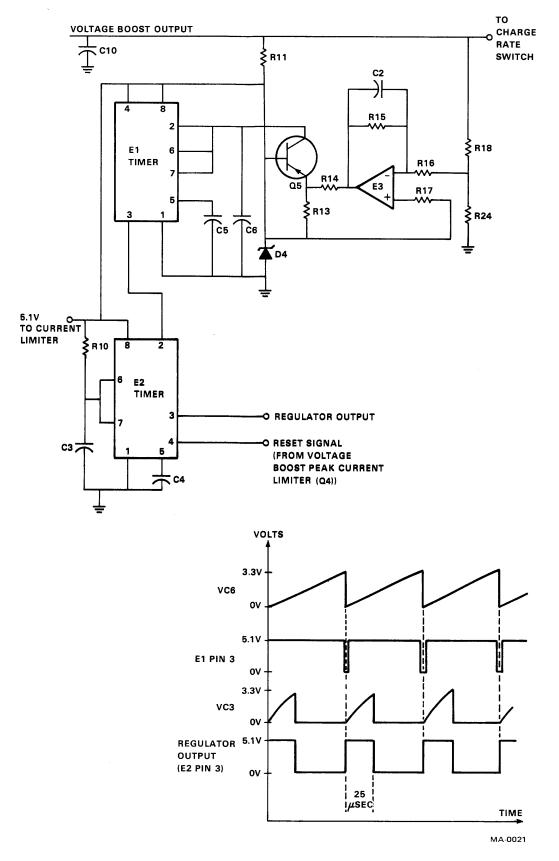
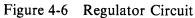


Figure 4-5 Voltage Boost Circuit





Transistor Q5 converts the error voltage to a current level allowed to charge C6 when the timer output at E1 pin 3 is high (the discharge transistor at E1 pin 7 is off). The capacitor voltage increases linearly from approximately 0.6 V until it reaches 3.3 V at which time E1 is reset. The discharge transistor turns on, which retriggers the timer by clamping the voltage at E1 pin 2 and C6 to approximately 0.6 V. Therefore, the timer is triggered almost immediately after it is reset resulting in a negative pulse at the timer output. The time interval between pulses is determined by the rate at which C6 is charged, which in turn depends on the magnitude of the error voltage.

The negative pulse at E1 pin 3 triggers E2, which is set up as a one-shot. When triggered, E2 pin 3 stays high for 25  $\mu$ s, as determined by R10 and C3. Therefore, the regulator output has a fixed high time of 25  $\mu$ s and a variable low time determined by E1 and the error voltage.

#### 4.4.3 Battery Charge Rate Status and Control (Figure 4-7)

Transistor Q7 is the charge rate switch. The major components of the charge rate switch control are transistors Q8 and Q11; Q11 is a Programmable Unijunction Transistor (PUT).

When the battery is charging from an initially low voltage, Q11 is off, and Q8 and Q7 are turned on. A high charging current, nominally 500 mA, flows to the battery via R20, R19, Q7 and D12 and therefore, the battery charges at a fast rate.

The gate voltage of Q11 is fixed at 5.1 V by D9 and the anode voltage of Q11 is determined by the battery voltage which is first divided down by R31 and R32. As the battery charges, its voltage increases. When the battery voltage reaches approximately 30.1 V, the anode-cathode voltage of Q11 becomes higher than the gate-cathode voltage, so Q11 turns on. The base drive to Q8 is bypassed to ground via D8 and Q11 and therefore, Q8 and subsequently, Q7 turn off. Note that when the battery has reached 30.1 V, it is charged to approximately 90 percent of its capacity.

When Q7 is turned off the battery voltage immediately decreases to 27 V. The battery is then charged to its full capacity at a slower rate by the trickle charge current. The trickle current, which is nominally 50 mA, flows to the battery via R20, R19, R22 and D12. When the battery is fully charged, the charge rate switch remains in the trickle state (Q7 is off) and the battery voltage is approximately 31 V, even though the battery is nominally rated at only 24 V.

Assume that the raw dc voltage drops below approximately 18 V causing the battery to discharge. Diode D12 is reverse biased, but voltage is present at the collector of Q7 until the boosted raw dc voltage decays across C10. Zener diode D10 acts as a level shifter. When the raw dc drops below approximately 18 V, Q10 turns off and subsequently, Q9 turns on and bypasses the anode current of Q11 to ground. The PUT (Q11) turns off, but the base drive to Q8 is bypassed to ground via D8 and Q9, so Q8 and Q7 remain off. Since Q11 is off, the charge rate switch will be in the fast mode (Q7 on) when the raw dc comes up again (Q9 off).

Transistors Q16 and Q6 are the major components of the charge status indicator circuit which generates the charge mode (CHG MODE) signal. Transistor Q8 controls Q16 and Q6 as well as the charge rate switch (Q7). When Q8 is turned on, CHG MODE is low, indicating that the battery is in the fast charge mode (Q7 on). When Q8 is turned off, CHG MODE is high, indicating that the battery is either in the trickle charge mode or discharging. Note that Q16 and Q6 are powered by the +5B output of the MOS regulator that is operational when the battery is discharging during an ac power failure.

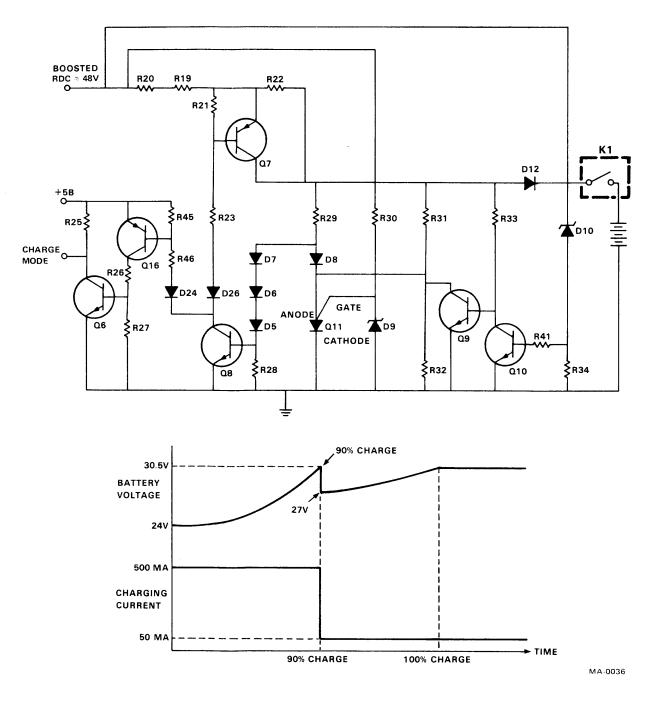


Figure 4-7 Battery Charge Rate Status and Control

#### 4.4.4 Battery Discharge Switch and Control (Figure 4-8)

The battery backup voltage is provided to the MOS regulator via D17 which is an SCR. Assume that D17 is initially off.

The battery supplies current to D15, which produces an 18 V threshold at the base of Q14. If the raw dc voltage drops below approximately 18 V, D11-A in the MOS regulator and Q14 are forward biased, creating a current path through R40. Transistor Q14 turns on Q13 which fires D17 and the battery discharges through D17 and D11-A. The voltage at the cathode of D17 reverse biases Q14 and subsequently, Q13 turns off. However, once the SCR is on, the gate current provided by Q13 is no longer necessary to keep it on.

The SCR (D17) turns off when the raw dc voltage (the SCR cathode voltage) is higher than the battery voltage (the SCR anode voltage) or when the battery current no longer flows to the SCR anode. Note that if the H775A is turned off or the MOS regulator draws over 10 A, the circuit breaker (CB1) opens and the battery power is cut off.

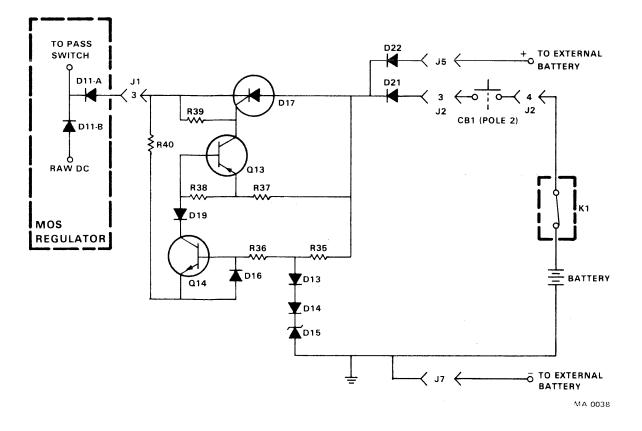


Figure 4-8 Battery Discharge and Control Circuit

#### 4.4.5 Battery Discharge Limit Circuit

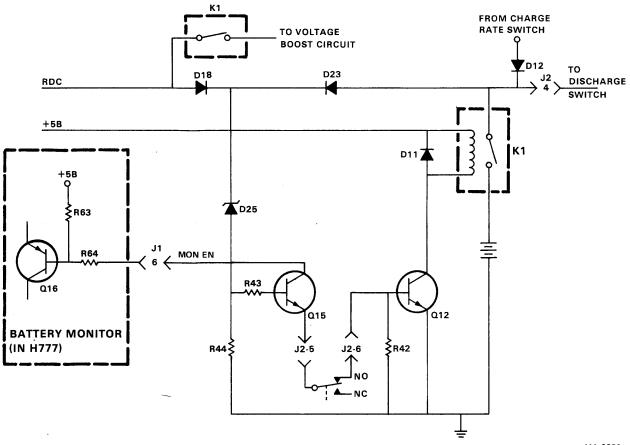
The major components of the circuit (Figure 4-9) are K1, Q12, Q15 and D25. The shut-off relay K1 is a normally open, double-pole, single-throw relay which is energized by Q12 under normal operating conditions. Therefore, K1 is closed and the battery can charge or discharge through it.

Zener diode D25 (Vz = 18 V) acts as a level shifter that monitors either the raw dc via D18 or the battery voltage via D23; whichever voltage is higher. If the raw dc is no longer present and the battery voltage decreases to 18 V, the base drive to Q15 is cut off. Transistor Q15 and, subsequently, Q12 turn off and K1 opens. The battery current is cut off from the load and the input to the charging circuit is open.

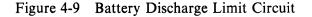
The magnetic circuit breaker (CB1) contains a double-throw relay. When the H775A is turned off or an overcurrent condition exists, CB1 is tripped so the relay in CB1 is deenergized and Q15 is disconnected from Q12. Transistors Q15 and Q12 turn off and K1 opens.

The monitor enable (MON EN) line connects the collector of Q15 to a pull-up resistor in the battery monitor circuit in the H777. When Q15 is off, the MON EN signal is high, which disables the battery monitor circuit. Therefore, the LED on the front console of the BA11-L is off.

Note that when the H777 is turned off, the +5B power from the MOS regulator is no longer present and therefore, K1 is open so the battery cannot be charged or discharged.



MA-0039



# CHAPTER 5 MAINTENANCE

#### 5.1 GENERAL

Maintenance procedures are divided into two categories: preventive maintenance and corrective maintenance. Preventive maintenance should be performed periodically to detect conditions that could lead to performance deterioration or malfunction. Corrective maintenance should be performed to isolate a fault or malfunction and to make necessary replacements.

This chapter contains the equipment and procedures needed to perform preventive and corrective maintenance on the BA11-L mounting box and the H775A battery backup unit. Corrective maintenance of the H777 power supply is emphasized.

A malfunction in the H777 should be isolated to a specific regulator or component in the ac control assembly. A faulty regulator should be replaced as a unit but the ac control assembly is component replaceable.

Instructions for the removal of the H777 from the BA11-L and the removal of the separate regulators are also included in this chapter.

#### 5.2 PREVENTIVE MAINTENANCE PHYSICAL INSPECTION

The following is a list of the steps required for mechanical checks and physical care of the BA11-L.

- 1. Check all fans to ensure that they are not obstructed in any way. The fan filter directly behind the front console should be periodically washed with water or another inorganic solvent.
- 2. Inspect all wiring and cables for cuts, breaks, frays, deterioration, kinks, strain and mechanical security. Repair or replace any defective wiring or cable covering.
- 3. Inspect the following for mechanical security: jacks, connectors, switches, screws, nuts, clamps, etc. Tighten or replace as required.

#### 5.3 CORRECTIVE MAINTENANCE

#### 5.3.1 Introduction

Maintenance of the H777 power supply and the H775A battery backup unit require the following equipment:

- 1. Tektronix 453 dual trace oscilloscope (or equivalent)
- 2. Weston Schlumberger model 4443 digital voltmeter (or equivalent) which can resolve 50 mV at 5 Vdc and has a range of a 0-50 Vdc.
- 3. A volt/ohmmeter (VOM)
- 4 The standard DEC tool kit.

The H777 contains an ac control assembly, +5 V regulator, MOS regulator and possibly a core regulator. A malfunction should be isolated to a specific regulator or a component in the ac control assembly by using the procedures outlined in Paragraphs 5.3.2–5.3.5. Figure 5-1 is a troubleshooting flowchart for the H777 power supply.

A faulty regulator should be replaced as a unit but the ac control assembly is component replaceable. Paragraph 5.3.6 contains instructions for the removal of the H777 from the BA11-L and removal of the separate regulators.

The H775A contains a circuit breaker, two batteries and a PC board containing the charging circuitry, discharge switch and the shut-off relay. A malfunction should be isolated using the procedures recommended in Paragraph 5.3.7. A fault in the PC board should be corrected by replacing the PC board.

#### 5.3.2 Power Supply (H777) Output Voltage Check

Output voltages should be checked at the power distribution board under normal load conditions with a DVM and an oscilloscope. Tables 2-1 and 2-2 list the signal assignments for the DD11-DK and DD11-CK backplane power harnesses which plug into the power distribution board. The power harness for the DD11-PK has the same pin assignments as the DD11-DK. Figure 2-11 shows the power distribution board. Probes can be inserted into the connectors next to the wires of the backplane harness. The output characteristics measured should be within the specifications listed in Table 5-1.

If all the voltage outputs are correct but a failing voltage is still suspected, repeat the measurements on the appropriate backplane connections. Refer to Figures 2-5 and 2-6 for the appropriate connections.

If some of the voltage outputs are incorrect, the appropriate regulator should be replaced.

If all the voltage outputs are incorrect follow the procedures outlined in Paragraph 5.3.3.

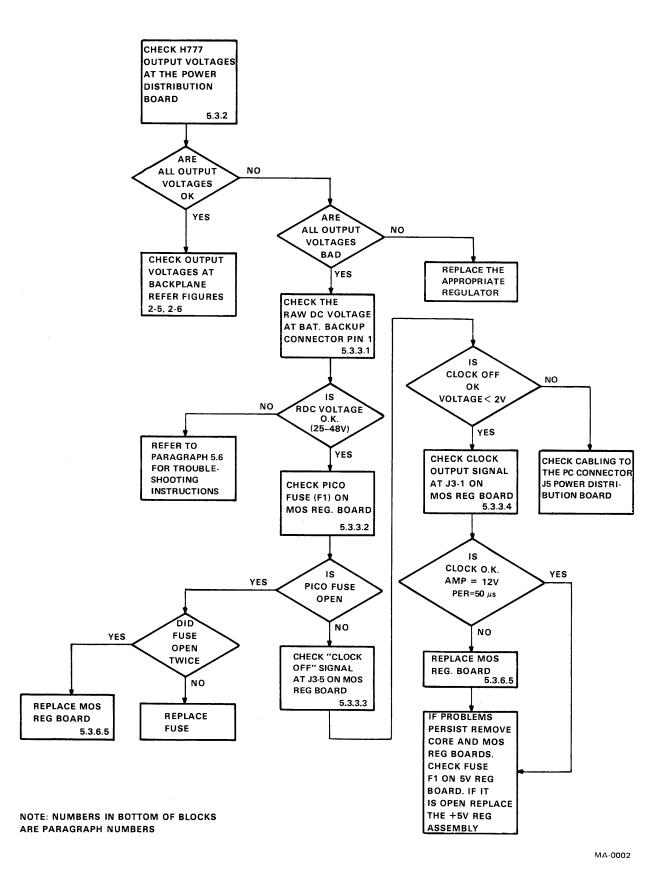


Figure 5-1 H777 Troubleshooting Flowchart

Regulator Assembly	Output Designation	Output Voltage and Tolerance	Current Output	Max Peak-Peak Ripple (%)
MOS Regulator (5411601)	+15B	$+15.3 V \pm 450 mV$	0–2 A*	2
	+15 V	+15.3 V -200 mV @+15B	0–1 A	2
	-15B	-15.3 V ±450 mV	0–2 A	2
	-15 V	+15.3 V -200 mV @-15B	0–1 A	2
	+5B	+5.1 V +100 mV -150 mV	0–4 A	2
Core Regulator (5411599)	+20 V	$+20.0 V \pm 500 mV$	0-6 A	2
	-5 V	-5.1 V +100 mV -150 mV	0–4 A	2
+5 V Regulator (7011073)	+5 V	+5.1 V +100 mV -150 mV	0–25 A	2
or +5 V Regulator (7012909)	+5 V	+5.1 V +100 mV -150 mV	0-32 A	2

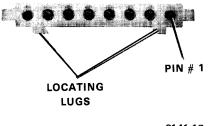
 Table 5-1
 Regulator Specifications

\*The total current output of +15B, +15V, -15B and -15V cannot exceed 4 A. Of this total, the +15V and -15V outputs can deliver a maximum of 1 A each. Refer to Paragraph 3.4.2.3.

#### 5.3.3 Major Power Supply Failure

If all the H777 power outputs are bad (not within the tolerance specifications), several possible causes should be investigated. The troubleshooting procedure in the succeeding paragraphs is suggested (Figure 5-1).

**5.3.3.1** Raw DC Voltage Check – The raw dc voltage is an unregulated dc which is the source voltage for all the regulated voltage outputs of the H777. A convenient place to check the raw dc voltage is at the battery backup connector on the power distribution board. The raw dc is present at pin 1 (Figure 5-2) and pin 2 is circuit ground.



8141-17

Figure 5-2 Raw DC Voltage Checkpoint

The voltage measured should be between 25 and 48 V. If the raw dc voltage is not within this specification, either the ac control assembly or the +5 V regulator is at fault. Refer to Paragraph 5.3.4 for troubleshooting measures to correct the raw dc loss.

**5.3.3.2** MOS Regulator Pico Fuse Check – Turn off the H777 and the H775A via their circuit breakers and wait 10 seconds for the surge relay in the H777 to drop out. Disconnect the power control (PC) connector J5 at the power distribution board. The pico fuse (F1) should be checked with an ohmmeter. Placement for the probes on the etched side of the MOS regulator board is shown in Figure 5-3. The raw dc normally passes to the regulator components via the 5 A pico fuse (F1). If F1 is open, it should be replaced. If problems persist and F1 is found to be open a second time, a faulty MOS regulator is indicated.

**5.3.3.3** CLOCK OFF Signal Test – The CLOCK OFF signal at J3-5 on the MOS regulator board can be accessed on the etched side of the board as shown in Figure 5-3. A convenient ground is also pointed out. If the CLOCK OFF voltage is greater than +2 Vdc, the master clock will not run. The power supply is probably not receiving the signal to turn on from a power switch on the front console or a remote power control. Check the console control cable and the cabling to the PC connector J5.

**5.3.3.4** Clock Output Check – An oscilloscope should be used to check the clock output which, in turn, is used to synchronize all the switching regulators in the H777. The clock output at J3-1 on the MOS regulator board can be accessed on the etched side of the board as shown in Figure 5-3. A convenient ground is also pointed out. The clock output should be a 0 to +12 V squarewave with a period of approximately 50  $\mu$ s. The voltage levels stated for the squarewave (0 and +12 V) are approximate values. If the clock signal seen on the oscilloscope is substantially different, the MOS regulator should be replaced.

**5.3.3.5** +5 V Regulator Fuse Check – Turn off the H777 and the H775A via their circuit breakers and wait 10 seconds for the surge relay in the H777 to drop out. Disconnect the power control (PC) connector J5 at the power distribution board. Remove the core and MOS regulator boards. Fuse F1 on the +5 V regulator should be tested with an ohmmeter. If F1 is open, a problem in the +5 V regulator is indicated and it should be replaced.

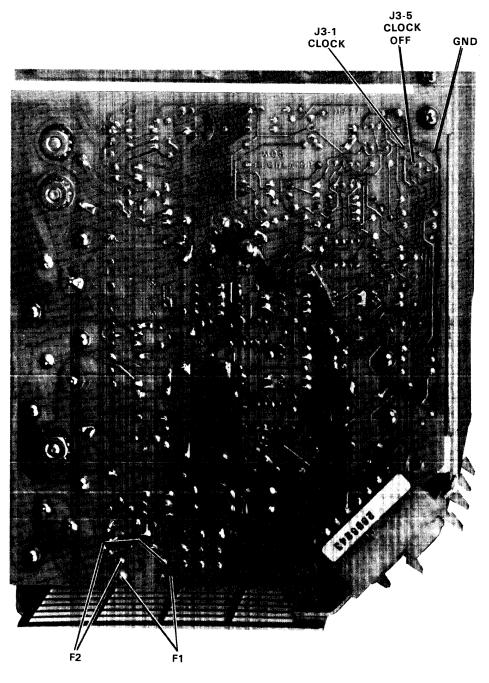
#### 5.3.4 Raw DC Voltage Failure

A raw dc voltage which is not within specifications indicates a problem in the ac control assembly or the +5 V regulator. The ac control assembly can be repaired by replacing its individual components and the +5 V regulator should be replaced as a unit.

The succeeding paragraphs explain procedures for finding a malfunction in the ac control assembly. Figure 5-4 is a troubleshooting flowchart. All voltages are measured at terminal board TB2 in the ac control assembly. The physical location of TB2 is shown in Figure 5-5 and the entire raw dc circuit (115 V version) is shown in Figure 5-6.

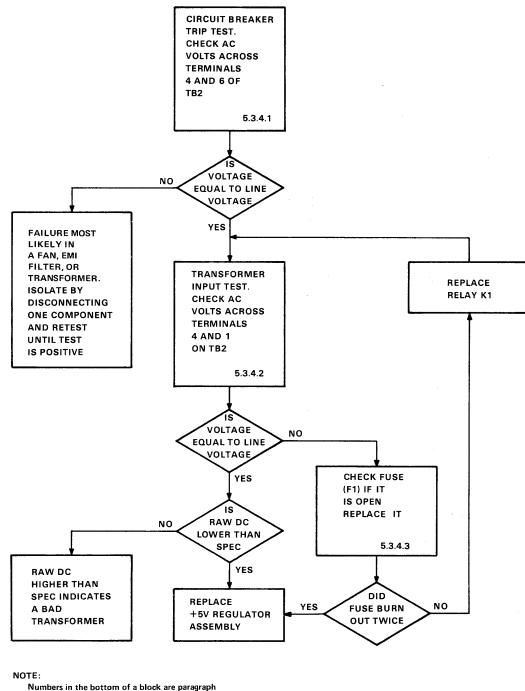
**5.3.4.1** EMI Line Filter Test – Measure the ac voltage across terminals 4 and 6 on TB2. The ac line voltage is fed to these terminals via the circuit breaker (CB1) and the EMI line filter and therefore the full ac line voltage should be measured between TB2-4 and TB2-6. The ac input specifications for the H777 are listed in Table 1-4.

The presence of ac line voltage across TB2-4 and TB2-6 indicates that the EMI line filter is not shorted and that the circuit breaker (CB1) is not tripped due to an overload. A current overload could be caused by a short in one of the fans, by a bad rectifier in the +5 V regulator, or possibly by a bad transformer. In the H777-AA, -AB, -BA or -BB, a short in the EMI line filter can trip the circuit breaker.



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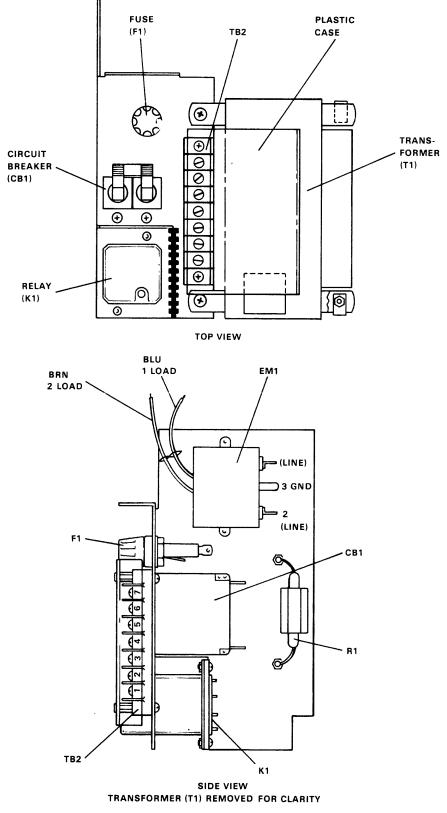
Figure 5-3 Etched Side of MOS Regulator Board



numbers with further explanation.

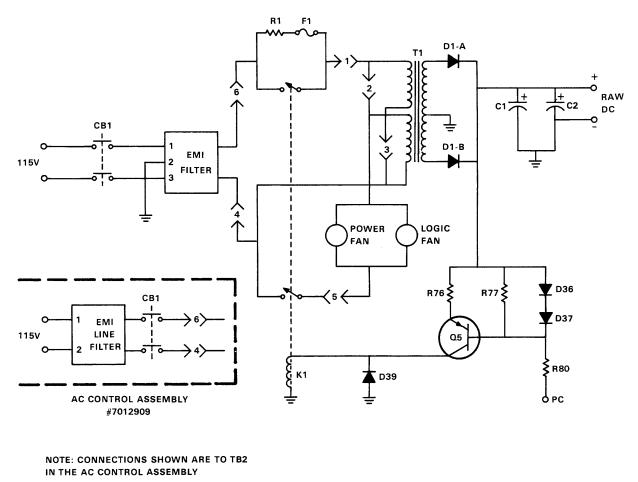
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Figure 5-4 Raw DC Troubleshooting Flowchart



MA-0047

Figure 5-5 AC Control Assembly Mechanical Configuration (7011075)



MA-0011



**5.3.4.2** Transformer Input Check – Measure the ac voltage across terminals 1 and 4 on TB2 which is the voltage across the transformer primary. The full ac line voltage should be measured here.

The transformer output (the secondary) is rectified and filtered in the +5 V regulator. If the voltage across TB2-1 and TB2-4 is within specifications and the raw dc voltage is too low (less than 25 V), the +5 V regulator is probably at fault. If the raw dc is too high (greater than 48 V), the transformer is probably bad. A high value of raw dc is unlikely because a bad transformer would probably trip the circuit breaker shutting down the H777.

**5.3.4.3** Fuse Check – Check the fuse (F1) in the ac control assembly. Fuse F1 is a 1 A slow blow fuse which should pass current only during ac power start-up. The purpose of F1 is to protect the surge resistor (R1) if relay K1 does not close during normal operation of the H777. Therefore, if F1 is open both F1 and K1 should be replaced. Power-up the H777 and recheck the raw dc voltage. If problems persist and the fuse is found to be open a second time, the problem is probably Q5 which is not providing current to the relay coil. Transistor Q5 is located in the +5 V regulator.

#### WARNING

# Do not activate the H777 if the relay (K1) is not in place. To do so will cause the fuse (F1) to open.

#### 5.3.5 AC LO and DC LO Corrective Maintenance

If all the power voltages of the H777 are operating within specifications and either AC LO or DC LO is asserted (grounded), disconnect J1 and J3 from the power distribution board. At the male side of the plug, check AC LO and DC LO. (Refer to Figure 2-11 and Tables 2-1 and 2-2.) If a signal high is measured, a problem in the +5 V regulator is indicated.

#### 5.3.6 Removal of Power Supply and Assemblies

#### 5.3.6.1 Power Supply Cover Removal –

1. With the processor box power switch in the ON position, turn off the circuit breaker.

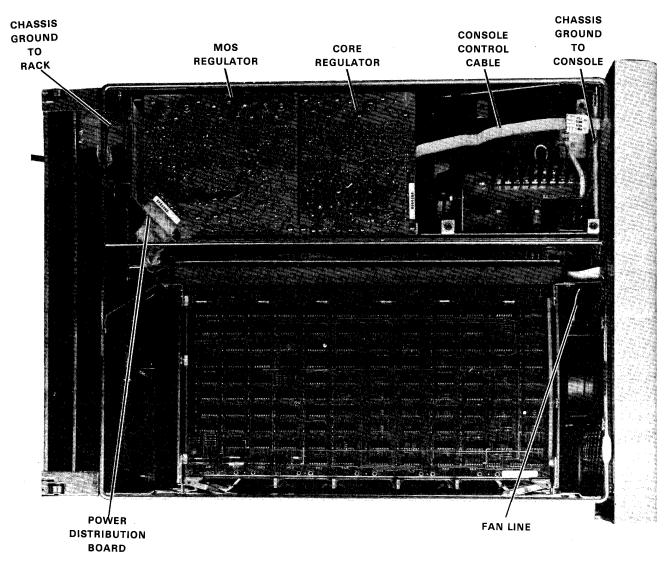
#### WARNING Step 1 must be done before step 2. Otherwise, the raw dc capacitors in the +5 V regulator will remain charged to approximately 40 V.

- 2. Disconnect the remote power control connector (J5) from the power distribution board.
- 3. The entire PDP-11 system should be turned off via the processor box power switch.
- 4. The power supply cover is mounted by eight screws; three on the top and five on the side. Once all the mounting screws are removed, lift the cover straight up.
- 5.3.6.2 Power Supply Removal (Figure 5-7) -

#### WARNING

Turn off the circuit breaker and wait for the surge relay (K1) to drop out (10 seconds maximum). Disconnect the remote power control connector (J5) from the power distribution board and remove the ac line cord from its socket. Turn off the H775A battery backup unit if one is present.

- 1. The BA11-L should be removed from any rack it is mounted in. Disconnect the green wire (chassis ground) at the back of the power supply from the rack. Two stops must be pushed in to slide the mounting frame completely out of its cover. The stops are accessible through holes in the cover toward the back on each side.
- 2. Disconnect all the connectors from the power distribution board (backplane harness, remote power control (J5) and the battery backup cable).



8141-4

Figure 5-7 BA11-L Mounting Box

- 3. Remove the four front console mounting screws and tilt the console forward. Disconnect the ribbon cable and the green wire (chassis ground).
- 4. Disconnect the connector from the logic module fan.
- 5. Remove one bottom, four side and two rear mounted screws.
- 6. Lift the H777 straight up to remove it from the BA11-L.

#### 5.3.6.3 AC Control Assembly Removal (Figure 5-8) -

- 1. Remove the power supply and the power supply cover using the procedures in Paragraph 5.3.6.2 and 5.3.6.1, respectively.
- 2. Remove the screw from the bracket on top of the power supply fan.
- 3. Remove the transformer (T1) outputs and the relay (K1) coil connections from the terminal board TB1 (also referred to as J1) in the +5 V regulator.

Transformer outputs	TB1-6, TB1-7 and TB1-8
Relay coil connections	TB1-4 and TB1-5

#### NOTE

If the core regulator is present, its four mounting screws must be removed. Then, the core regulator should be tilted so that TB1 can be accessed.

- 4. Disconnect the logic and power supply fan connectors
- 5. Remove the four transformer mounting screws from the bottom of the power supply box.
- 6. Tilt the assembly to expose the bottom of the circuit breaker and remove the line cord faston tabs.
- 7. Clear the ribbon cable and the green wire (chassis ground) from the ac control assembly. These wires were connected to the front console before the power supply was removed.
- 8. Lift out the ac control assembly.

#### 5.3.6.4 Core Regulator Removal -

#### WARNING

Turn off the circuit breaker and wait for the surge relay (K1) to drop out (10 seconds maximum). Disconnect the remote power control connector (J5) from the power distribution board and remove the ac line cord from its socket. Turn off the H775A battery backup unit if one is present.

1. Remove the power supply cover using the procedures in Paragraph 5.3.6.1.

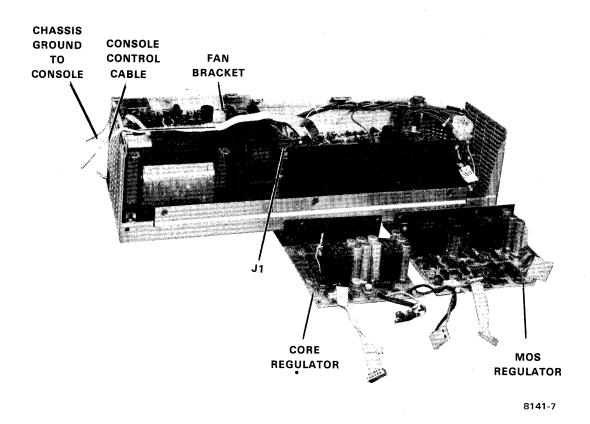


Figure 5-8 H777 Power Supply

- 2. Four screws that mount the core regulator should be removed. Two screws are on the top of the board at its edge and two screws are on the side holding the board to the heat sink.
- 3. Lift the core regulator board and disconnect J3 and J5 from the +5 V regulator board. Connector J3 is a 10-pin ribbon cable connector and J5 is a 2-pin connector.
- 4. Disconnect the three wires which are attached to terminal board J1 on the +5 V regulator.\*

J1-1	orange wire
J1-2	brown wire
J1-3	black wire

<sup>\*</sup>In the H777-CA, -CB, -DA and -DB, the three wires are connected to J1 by a fanning strip.

#### 5.3.6.5 MOS Regulator Removal –

#### WARNING

Turn off the circuit breaker and wait for the surge relay (K1) to drop out (10 seconds maximum). Disconnect the remote power control connector (J5) from the power distribution board and remove the ac line cord from its socket. Turn off the H775A battery backup unit if one is present.

- 1. Remove the battery backup cable at the top of the power distribution board if an H775A is present.
- 2. Remove the power supply cover using the procedure in Paragraph 5.3.6.1.
- 3. Four screws that mount the MOS regulator should be removed. Two screws are on the top of the board at its edge and two screws are on the side holding the board to the heat sink.
- 4. Lift the MOS regulator board and disconnect the 10-pin ribbon cable connector (J4) from the +5 V regulator board.
- 5. Disconnect the 9-pin Mate-N-Lok connector (J2) from the MOS regulator board.

5.3.6.6 Removal of the +5 V Regulator (7011073 or 7012909) -

#### WARNING

Turn off the circuit breaker and wait for the surge relay (K1) to drop out (10 seconds maximum). Disconnect the remote power control connector (J5) from the power distribution board and remove the ac line cord from its socket. Turn off the H775A battery backup unit if one is present.

- 1. Remove the power supply and the power supply cover using the procedures in Paragraphs 5.3.6.2 and 5.3.6.1, respectively.
- 2. Remove the core regulator and the MOS regulator using the procedures in Paragraphs 5.3.6.4 and 5.3.6.5, respectively.
- 3. Remove the remaining wires from the terminal strip designated TB1 (or J1) on the +5 V regulator board.
- 4. Clear the ribbon cable and the green wire (chassis ground) away from the ac control assembly. These wires were previously attached to the console.

NOTE Step 5 is not necessary when removing regulator 7012909.

- 5. Remove two mounting screws from the power distribution board.
- 6. Remove two screws from the bottom of the power supply box.
- 7. Remove the +5 V regulator.

#### 5.3.7 H775A Battery Backup Maintenance

The H775A battery backup unit is designed to provide battery power to the MOS regulator for a limited time after a power failure has occurred. There are five areas of malfunction which could inhibit the H775A from accomplishing its function.

- 1. The input/output cable at J1
- 2. The batteries
- 3. The shut-off relay circuit (on the PC board)
- 4. The discharge switch circuit (on the PC board)
- 5. The charging circuitry (on the PC board).

General procedures for isolating a malfunction in the H775A are discussed in the succeeding paragraphs. Figure 5-9 is a troubleshooting flowchart for the H775A.

If a malfunction has been found on the PC board, the entire board should be replaced.

**5.3.7.1 Input/Output Check** – One input/output cable is the only link between the battery backup unit (H775A) and the power supply (H777). The cable plugs into the top connector at the H777 power distribution board and connector J1 at the battery backup unit. The battery backup voltages should be checked at both ends of the cable to ensure proper continuity. Measurement probes can be placed into the male side of the connectors next to the wires. The battery backup connectors are shown in Figure 5-10 and the proper voltages are listed in Table 5-2.

**5.3.7.2** Battery Check – Figure 5-11 shows the component layout of the PC board in the H775A and Figure 5-12 is a block diagram of the H775A.

The battery voltage should be checked with a voltmeter across J3-1 and J4-2 on the PC board. Pin J4-2 is a circuit ground.

The battery voltage is produced by two batteries connected in series at J3 and J4 on the PC board. The two batteries are considered one in this manual.

The battery is nominally rated at 24 V but the battery, when fully charged, may measure as high as 31 V. In normal operation, the battery is prevented from discharging below 18 V by the shut-off relay circuit.

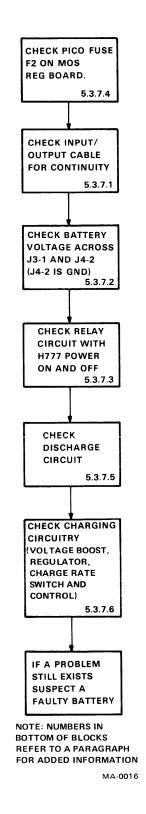
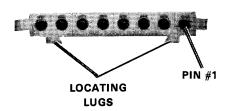
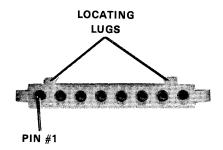
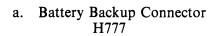


Figure 5-9 H775A Troubleshooting Flowchart

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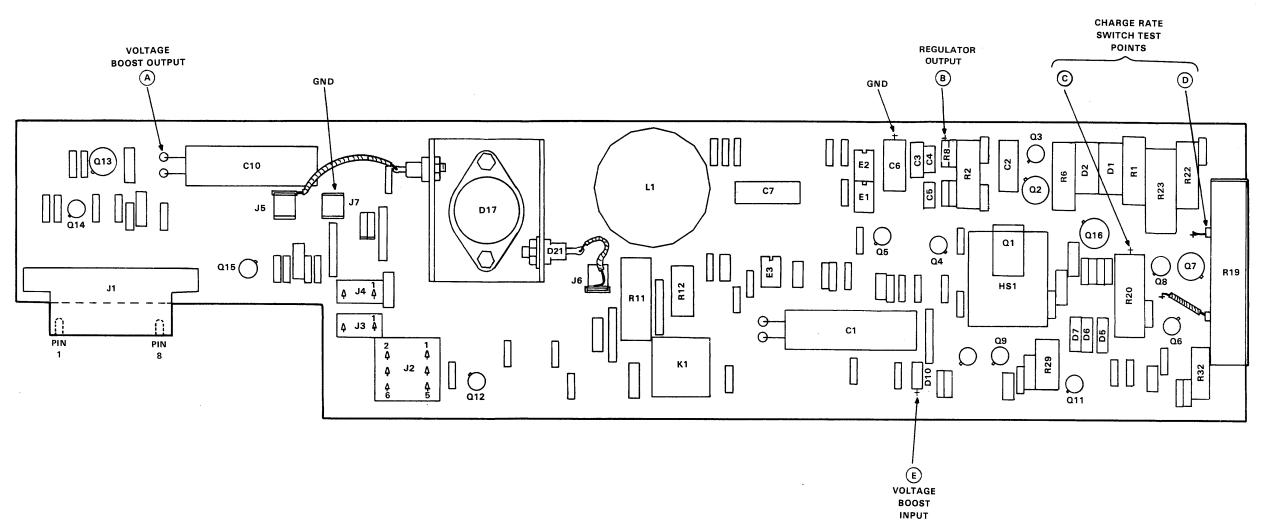
b. Battery Backup (J1) H775A

	Figure 5-10	H775A	Input/Output	Connectors
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H777 Battery Backup Connector Pin No.	H775A Battery Backup Connector	Wire Color Code	Function	Voltage Under Normal Operating Conditions
1	J1-1	Orange	Raw DC	25–48 V
2	J1-2	Black	GND	0 V
3	J1-3	Blue	H775	18–24 V
4	J1-4	Gray	Output Charge Mode	+5 or 0.4 V
5	J1-5	Red	+5B	+5 V
6	J1-6	White	MON EN	$+5 \text{ V or} \leq 1.2 \text{ V}$
7	J1-7	Yellow	Not Used	
8	J1-8	Brown	by H775A Not Used by H755A	

#### WARNING

The H777 battery backup connector is mechanically mounted to the MOS regulator board of the H777. The connector is designated J1 and refers to the MOS regulator board and is not the J1 shown on the power distribution board.



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## Figure 5-11 H775A Battery Backup Board

**5.3.7.3** Shut-Off Relay Circuit Check (Figures 5-11 and 5-12) – The battery is connected to the charging and discharging circuitry by the shut-off relay (K1). The proper operation of the shut-off relay and its control circuit can be verified by measuring two voltages.

Measure the voltage at pins J2-4 and J1-6 with a voltmeter. Both voltage measurements should be referenced to ground at J4-2 or J1-2.

Pin J2-4 is on the circuit side of the shut-off relay and therefore, if the voltage at J2-4 is equal to the battery voltage, the shut-off relay is closed. The relay should be closed if the battery voltage is greater than 18 V or the raw dc voltage is within specifications. However, if either the H777 or H755A is turned off, the relay should be open irrespective of the battery voltage or raw dc.

Pin J1-6 is the Monitor Enable (MON EN) line which connects the collector of a relay control transistor to a pull-up resistor in the battery monitor circuit of the H777. A low voltage (less than 1.2 V) indicates that the relay control transistors are turned on and therefore, the shut-off relay should be closed. A high voltage (+5 V) indicates that the relay should be open.

**5.3.7.4** Fuse Check – The battery output current of the H775A passes through fuse F2 on the MOS regulator board. Fuse F2 should be checked using the procedure in Paragraph 5.3.3.2. If fuse F2 is open, it should be replaced. If problems persist and F2 is found to be open a second time, a faulty MOS regulator is indicated.

**5.3.7.5** Discharge Circuit Check (Figures 5-11 and 5-12) – The discharge switch is an SCR. During an ac power failure, the SCR conducts and battery current flows to the MOS regulator at the H775A output. The following method is recommended to verify the proper operation of the discharge circuit.

Induce a power failure in the H777 by turning its circuit breaker off. Measure the voltages at pins J1-3 (the H777A output) and J2-3 (the battery voltage). Both measurements should be referenced to ground at pin J4-2 or J1-2. The voltage at J1-3 should be approximately 1.5 V lower than the voltage at J2-3. The voltage is caused by the offsets of the SCR and diode D21, both of which should be conducting. Note that the discharge circuit can only work properly if the battery voltage is 18 V or higher.

**5.3.7.6** Charging Circuit Check (Figures 5-11 and 5-12) – The charging circuitry consists of the voltage boost circuit, a regulator circuit and the charge rate switch and control circuit. Paragraph 5.3.7.3 contains troubleshooting procedures for the shut-off relay which connects the battery to the charging circuitry. The proper operation of the charging circuitry can be verified by measuring a few key voltages at points shown in Figure 5-11. Unless stated otherwise, all voltage measurements should be referenced to ground on the circuit board.

Measure the voltage at point A on the circuit board. The measured voltage is the voltage across C10 which is the voltage boost output and should be between 45 and 48 V. In normal operation, the raw dc is stepped up to 45–48 V by the voltage boost circuit which is controlled by the regulator circuit.

If the voltage measured at point A is not within specifications, the raw dc voltage (25-48 V) should be measured at point E on the circuit board. If the raw dc voltage is within specifications, the voltage boost or regulator circuit is probably faulty. If the raw dc voltage is not present, the circuit breaker has probably been tripped.

The regulator output can be checked at point B on the circuit board with an oscilloscope. The regulator output should be a pulse train with a 5 V amplitude and a fixed high time of 25  $\mu$ s. The regulation of the voltage boost output is accomplished by varying the frequency of the pulse train. If the high time is less than 25  $\mu$ s, there is a possibility that the regulator was reset prematurely, due to an overcurrent condition in the voltage boost circuit. Otherwise, there is probably a malfunction in the regulator circuit.

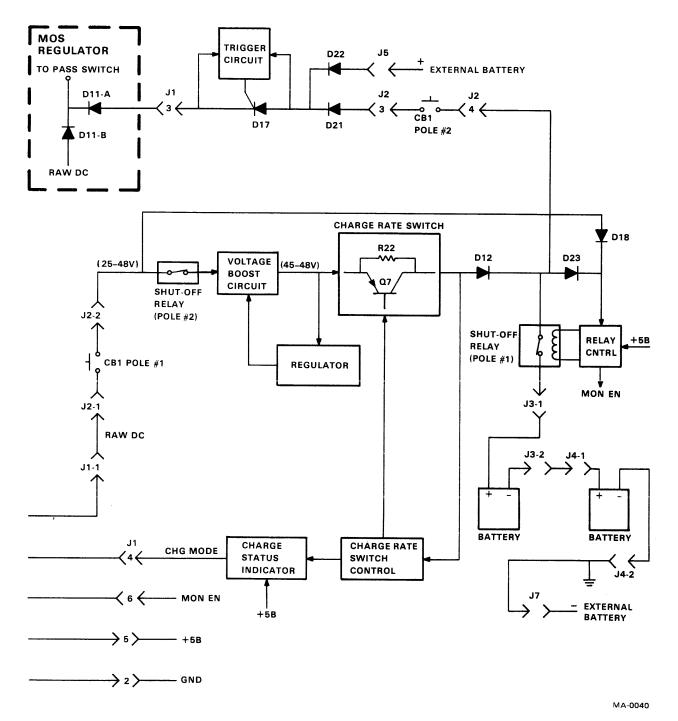


Figure 5-12 H775A Block Diagram

The state of the charge rate switch (Q7) determines the rate at which the battery is charged – fast mode (Q7 on) or trickle mode (Q7 off). The circuitry which controls Q7 also generates the charge mode (CHG MODE) signal which indicates to the H777 the state of the charge rate switch.

The state of the charge rate switch can be determined by monitoring the voltage across R19 and R20 with an oscilloscope at points C and D on the circuit board (Channel 1 C, Channel 1 Ground D). Resistors R19 and R20 are in series with the charge rate switch (Q7).

#### WARNING The oscilloscope should be floated as shown in Figure 5-13. While the scope is floated, avoid contact with the case of the scope and the internal ground lead of the scope probe.

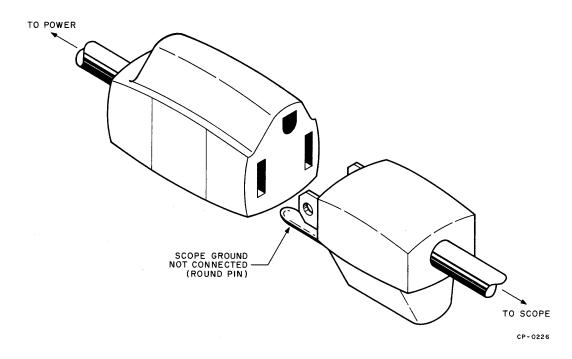


Figure 5-13 Floating Oscilloscope Connection

The CHG MODE signal can be monitored with an oscilloscope at J1-4 (the H775A input/output connector). Pin J1-2 is a circuit ground.

Signal CHG MODE and the charge rate switch should be monitored during the following procedure. Refer to Table 5-3.

WARNING While floating the scope, both channels cannot be used simultaneously. Therefore, the procedure in the following paragraph should be repeated.

H777 and H775A Battery Condition	Charge Mode	Approximate Voltage Across C and D	Charge Mode Signal
H777 power-up battery charging	Fast	+15 V	≤0.4 V
H777 power-up battery close to full charge (battery 30.1 V)	Trickle	+1.5 V	+5 V
H777 power-down (battery discharging)	Trickle	+1.5 V*	+5 V

 Table 5-3
 Troubleshooting Voltages for Charge Rate Switch and Control

\*Voltage decays to 0 V as raw dc decays to 0 V.

Power down the H777 by turning off its circuit breaker and wait for the surge relay to drop out (10 seconds maximum). Then turn the H777 on again. When the raw dc voltage comes up, the switch should be in the fast mode. If the battery voltage is over approximately 30.1 V (indicating a 90 percent charge), the switch should revert to the trickle state.

The CHG MODE signal and the voltage across C and D should indicate the same charge mode. If the CHG MODE signal indicates the correct charge mode and the voltage across C and D does not, the charge rate switch (Q7) is probably at fault. Otherwise, a malfunction probably exists in the control circuitry.

### 5.3.8 Battery Backup Component Replacement

The top panel of the box can be lifted once three screws on the back of the H775A are removed.

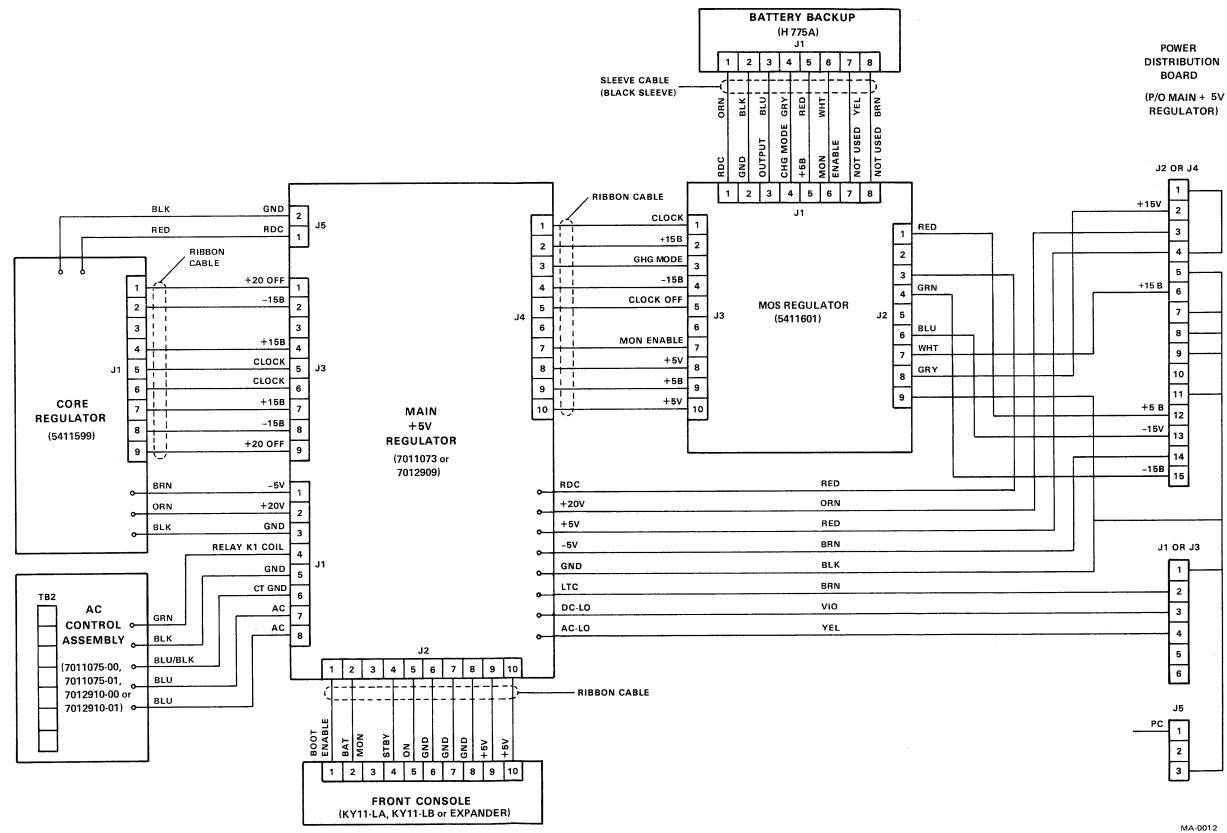
The batteries slide out from the back of the H775A once they are disconnected from the circuit board at J3 and J4.

To replace the circuit board, perform the following. Disconnect the input/output cable (at J1) and the other three connectors (J2, J3, and J4) from the circuit board. Remove the seven mounting screws from the board. Two of these screws also hold R19 (the ohmmeter resistor) to the board. Lift the circuit board off the tray.

The circuit breaker can be accessed after removing a back panel which is below the binding posts. The circuit breaker is mounted by four screws on the front of the H775A. The circuit breaker electrically connects to J2 on the circuit board.

#### WARNING The input/output cable must be disconnected before the circuit breaker is handled.

# APPENDIX A H777 INTERCONNECTION DIAGRAM



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BA11-L MOUNTING BOX TECHNICAL MANUAL EK-BA11L-TM-001

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