EK-BA11L-MM-PRE

P R E L I M I N A R Y

BA11-L Mounting Box

Maintenance Manual

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Written by PDP-11 Engineering

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THE BA11-L MOUNTING BOX MAINTENANCE MANUAL

CHAPTER 1

BA11-L PHYSICAL CHARACTERISTICS AND SPECIFICATIONS

1.1 GENERAL

This manual describes the BA11-L rack-mounted expander box manufactured by Digital Equipment Corporation. The BA11-L box is 19 inches wide, 5 1/4 inches high, and 25 inches deep. It provides power to the various components mounted in the box (see Figure 1-1).

1.1.1 Scope

This manual is designed to provide Digital Field service and customer maintenance personnel with sufficient installation, operation, and servicing information to install and maintain the box.

1.2 PHYSICAL CHARACTERISTICS

The BA11-L mounting box is designed to provide a strong mounting frame with maximum accessibility and serviceability. The mounting frame is divided into two sections; one section contains all the logic modules, the other section contains the H777 power supply.

The mounting frame slides into a rack mounting wrap around envelope that completely encloses all four sides of the frame. The front and back of the envelope are open for front to back air flow. The wraparound envelope mounts directly into a cabinet, without rack slides, and functions as the slide mechanism for withdrawing the frame and its contents.

An operator's console assembly (KY11LA) mounts on the front of the BA11-L frame. The console assembly contains the power control and limited function switches required for system operations.

Table 1-1 is a list of BA11-L physical and environmental specifications.

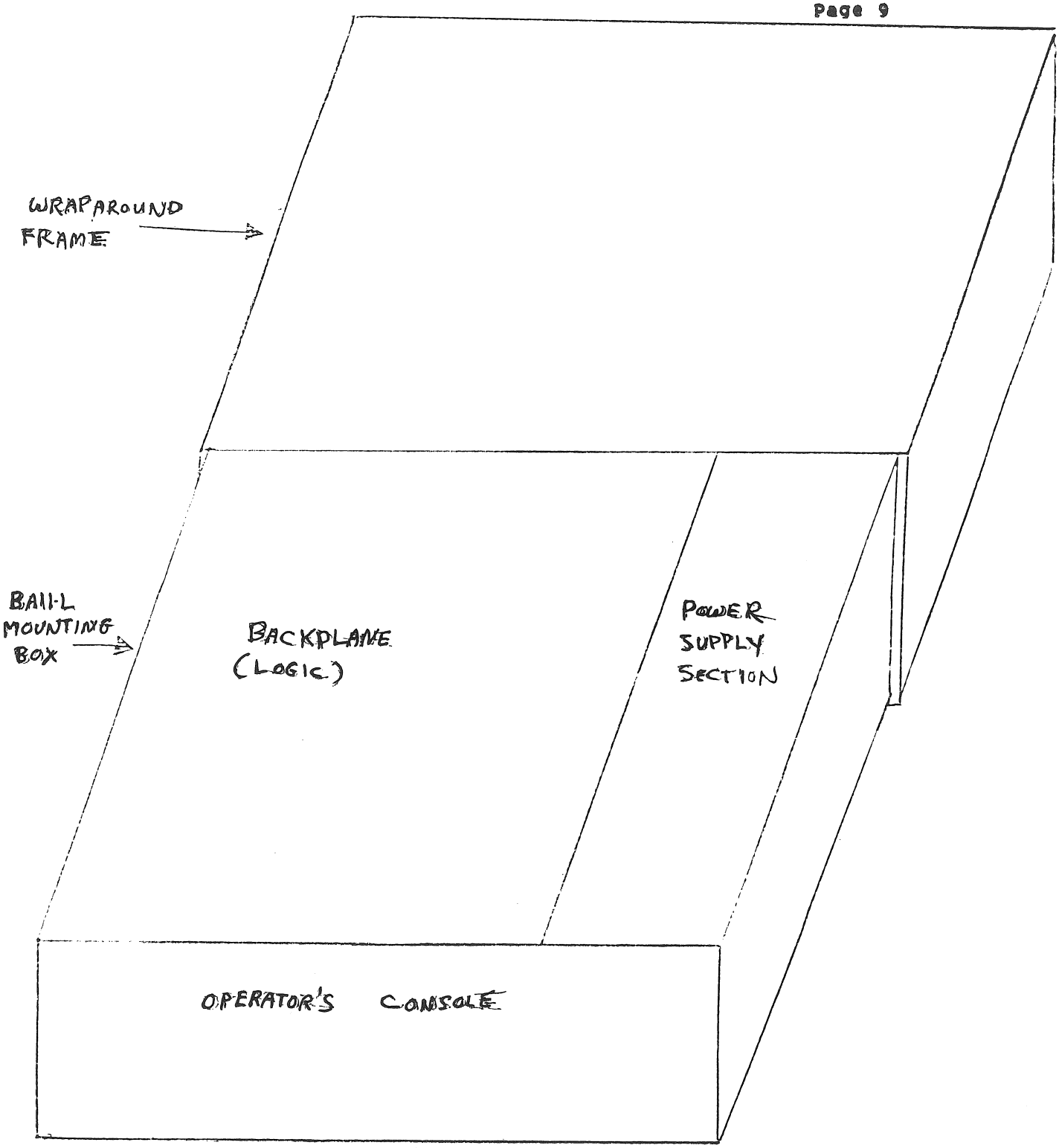

FIGURE 1-1
BA11-L Mounting Box (Extended From Wire Frame)

TABLE 1-1

BA11-L Specifications

BA11L Mounting Box	
Chassis size with operators console	5 1/4"H x 19"w x 25"D
Unconfigured weight with H777	
Module slots	9 maximum using DEC standard backplanes
Cooling efficiency for both fans at 90vac + or - %, 50hz	
Shock and vibration characteristics (operating)	1/2 sine shock pulse of 10 GPK and 10 + or -3ms, duration
(non-operating)	1/2 sine shock pulse of 40 GPK and 30 + or -10 ms, duration
Fan air movement direction	Front to rear, 2 channels
Cooling efficiency for both fans at 90vac + or -	See Bob Allen
H777 Power Supply	
Size	5"H x 6 1/2"W x 20"D less power cord
Weight (MOS version)	
Weight (Core Version)	
Input MOS (H777-C, H777-D)	90-132, 180-264 Vac RMS 47-63 Hz, Dual primary
Core (H777-A, H777-D)	104-127, 208-254 vac RMS 47-63 Hz Dual primary

Output*	Battery Support	+5V, + or -5%, 0-25 Amp +15V, + or -5%, 0-1 Amp -15V, + or -5%, 0-1 Amp +5V, + or -5%, 0-2 Amp -5V, + or -5%, 0-2 Amp +20V, + or -3%, 0-6 Amp	Average (DC meter readings)
Noise			
Ripple		3% p-p or less, of nominal voltage	

AC Lo and DC Lo must be > or =5 msec.

Protection:	Overload/short circuit protection recovers upon removal of overload. SSC = 50% x Irated Overvoltage crobar protection on +5 and +20 volts. Indirect overvoltage protection on MOS backup voltages.
Battery Interface:	Battery voltage 18-48V for MOS backup. Battery voltage 24-48V for system or core backup (recabling required). Current drain < or =2.5 Amp from 24V battery (64K MOS, MM11-S). Charging - 2 Amp max. available current @ 23-48 VDC. Signals - Charger mode, Key/Enable.
Adjustments:	+ or -15V adjusted to + or -12V by jumper. No other adjustments available.

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* Total DC power NTE 240 watts

Environmental:	Ambient; temperature Ø degrees C-6Ø degrees C humidity - per DEC STD, 1Ø2, Shock & Vibration; per DEC STD 1Ø2 for Class C equipment,
Cooling:	3ØØ LFPM min, airflow required (Fan mounted on BA11-L),
Efficiency:	6Ø% minimum - overall,

BATTERY BOX

Size:	5 1/4" x 19" Rack Mount x 4",
Input/Output:	+23-48 DC/+24 DC,
Capacity:	12Ø Watt hour @ 5Ø degrees C, @2,5 Amp rate,
Cell Type:	Sealed lead-acid, Nickel cadmium or GEL-cell may be used with appropriate charge in capacity spec,
Charger:	Constant current, dual rate
Weight:	15 lb,

1.3 OPTIONAL I/O CABLE RETRACTOR ASSEMBLY

An optional spring-loaded cable retractor assembly (part no.)that mounts to the rear of a standard 19" rack is available. Its function is to provide a service loop for Unibus and I/O cabling to protect them against fraying when the wire frame is extended.

The retractor assembly will accommodate all the round and flat cabling styles presently available.

1.4 H777 POWER SUPPLY PHYSICAL CHARACTERISTICS

The H777 power supply is a compact modular assembly designed to fit into the BA11-L box. It is rectangular in shape and open at both ends for front-to-rear air flow.

There are five modular subassemblies in the H777 (See figure 1-2):

- AC control assembly
- +5V main regulator
- MOS regulator
- Core regulator
- Fan

With the exception of the AC control assembly, all the subassemblies can be removed and installed while the H777 assembly is mounted in the BA11-L box.

NOTE

The H777 Power Supply is available in the following designations:

H777A - 115v supply - core and MOS (metal oxide semi-conductor) memory
H777B - 230v supply - core and MOS memory
H777C - 115v supply - MOS memory only
H777D - 230v supply - MOS memory only

Instructions on the top of the power supply specify the correct designation.

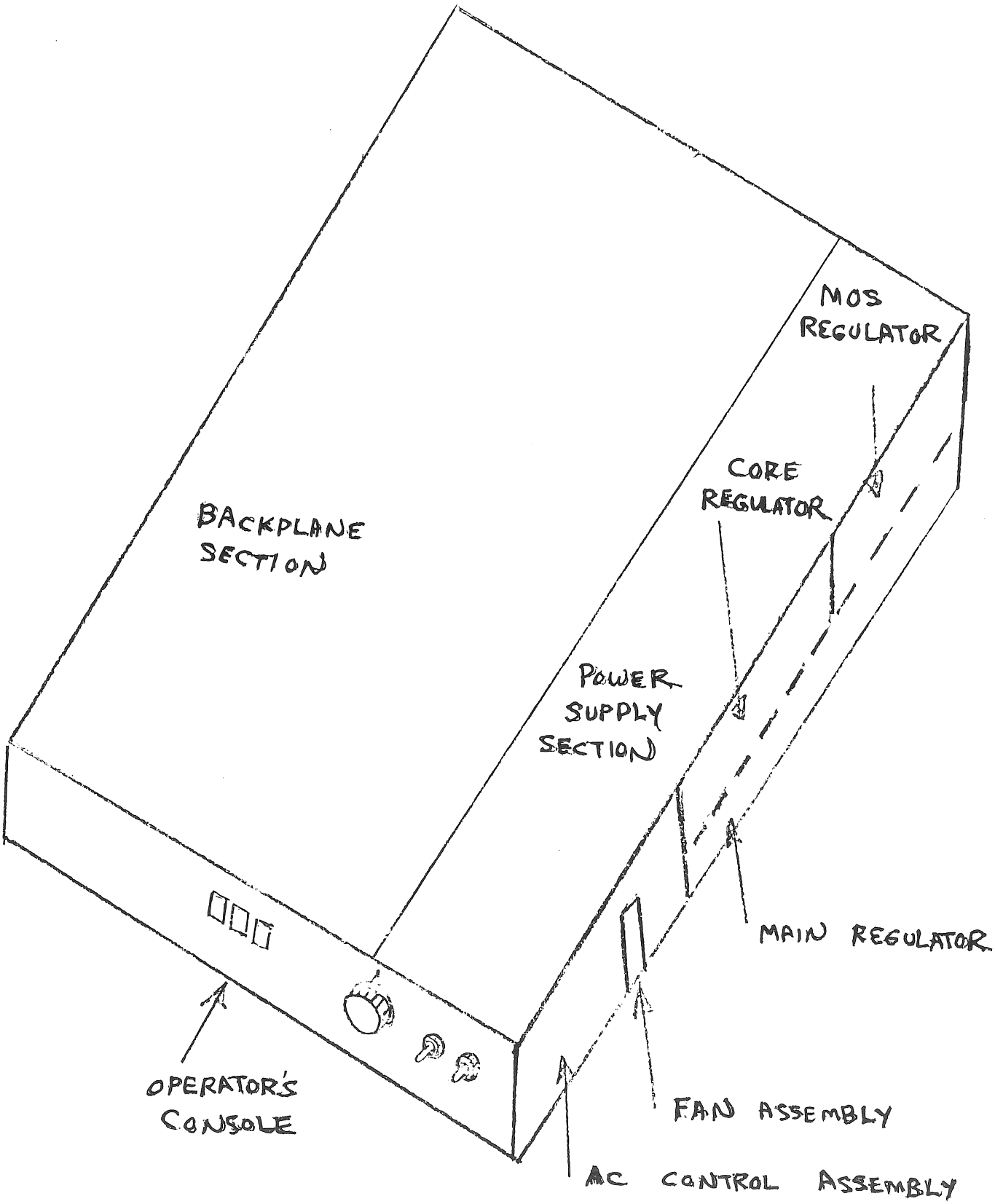


FIGURE 1-2

BA11L Mounting Box (Removed from Wraparound Envelope)

1.4.1 AC Control Assembly Physical Description (see Figure 1-3)

The AC control assembly contains the following components:

- Linear transformer (T1) - provides stepped-down voltage and isolation of the power supply from the AC line; operates at 47 to 63 hz.
- Circuit breaker - turns off AC power in the event of a power surge or when maintenance personnel desire to work on the power supply.

CAUTION

Never remove the power supply cover without turning circuit breaker off, as AC is still present.

- AC conversion terminal block - provides conversion from 115 vac to 230 vac (see directions on terminal block cover).
- Surge resistor - provides inrush current limiting when supply is connected to a-c source.
- Surge relay - bypasses surge resistor after the raw DC is established (normal operation).
- F1 surge protector - protects surge resistor if relay fails.
- EM1 line filter - keeps power supply noise isolated from AC source.

1.4.2 Main (+5v) Regulator Assembly Physical Characteristics

The main regulator assembly consists of a large and small printed circuit board assembly interconnected by a soldered power harness.

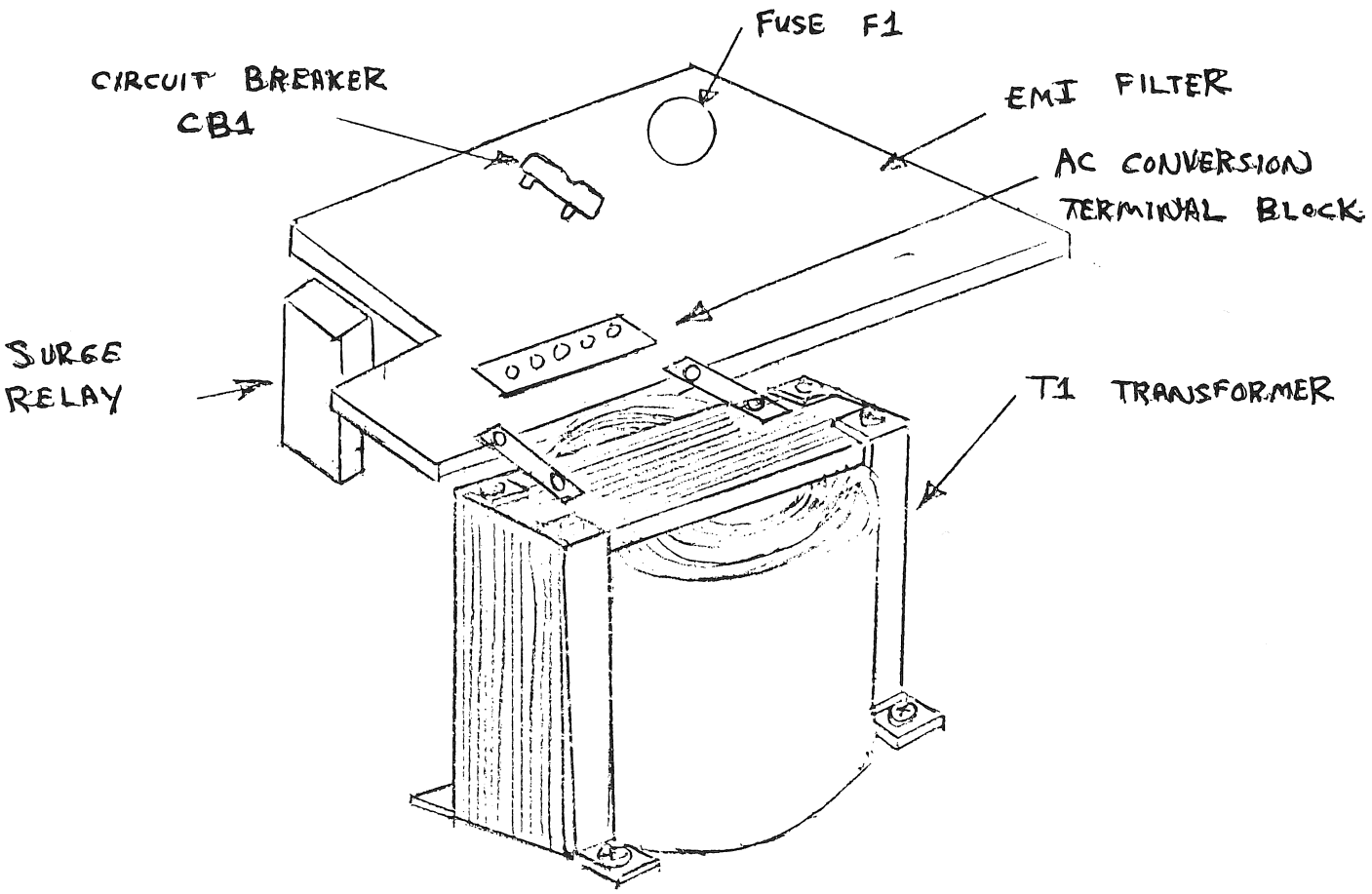


FIGURE 1-3

AC Control Assembly

The larger board (+5V regulator) contains a +5V low-voltage switching regulator, power sequence logic (AC LO, DC LO, LTC) and battery monitor logic. The small board (power distribution board) contains power connectors which provide outputs to two system unit power cables, and a power control connector.

There are no adjustments on the main regulator assembly.

A number of module interconnect and control connectors are mounted on the larger +5V board. These connectors are identified in Figure 1-4.

1.4.3 MOS Regulator Assembly (see Figure 1-5)

The MOS regulator is in reality three regulators: +15V, -15V and +5V. The +15V and -15V regulators have dual switched and unswitched outputs. The unswitched set runs on battery backup to run MOS (metal oxide semi-conductor) memory modules, the switched outputs run option modules requiring + or -15V and are powered off in standby and battery backup modes.

The regulator assembly mounts inverted on top of the +5 main regulator assembly. A small ribbon cable (MP3) and a large nine-pin power cable (MJ_2) provide interface connections to the rest of the supply. A straight, eight-pin connector (MJ1) mounted over the power Distribution Assembly provides a Battery Backup Option interface.

1.4.4 Core Regulator Assembly (see Figure 1-6)

The core regulator is an optional assembly in the H777. It is required when core memory modules are used as part of a system.

The core regulator, like the MOS regulator, is a multiregulator. The core modules require +20V and -5V.

The core regulator assembly mounts inverted beside the MOS regulator and on top of the MAIN +5V regulator.

The power and control signals from the core regulator interconnect via the main regulator assembly.

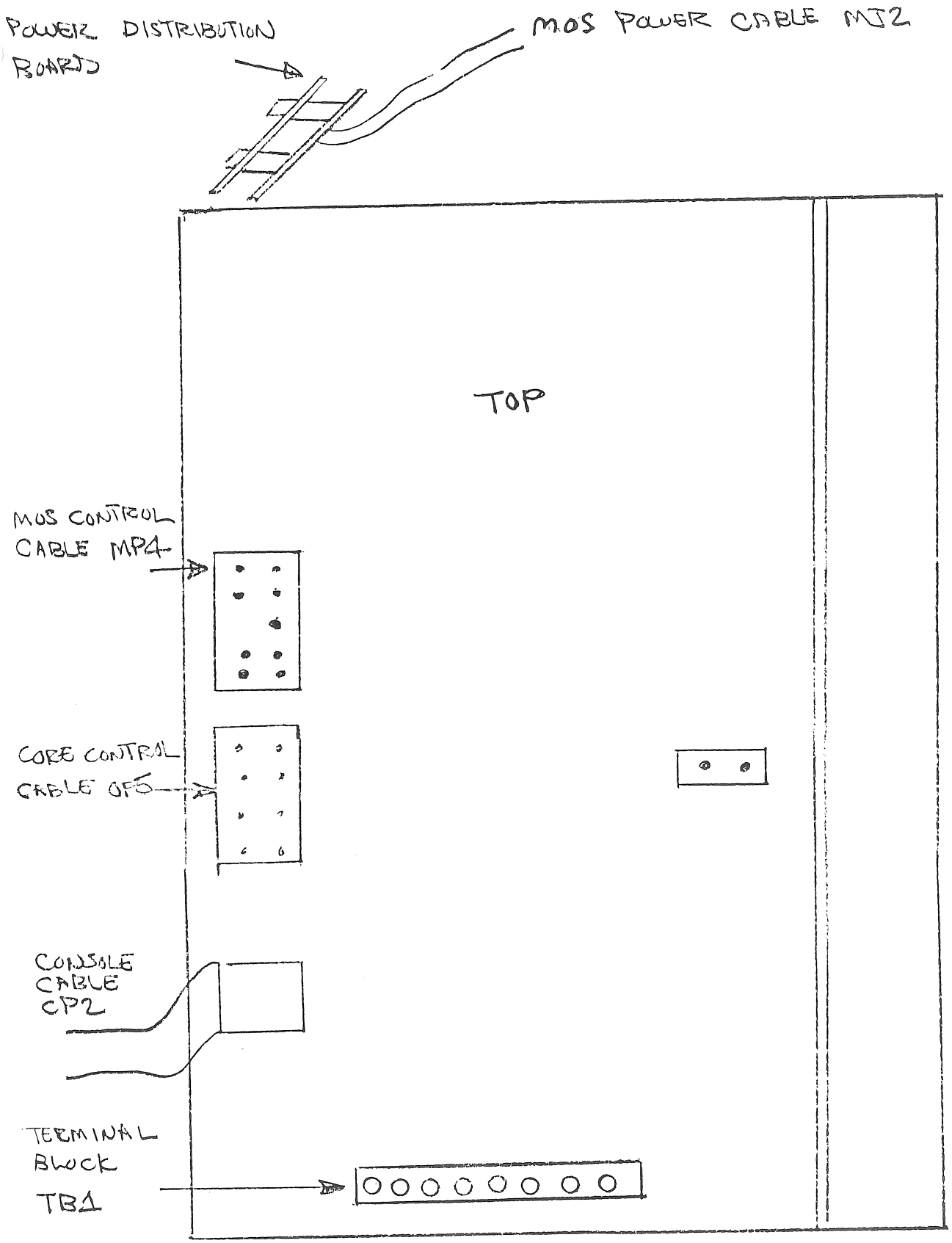


Figure 1-4

+5V Main Regulator Assembly

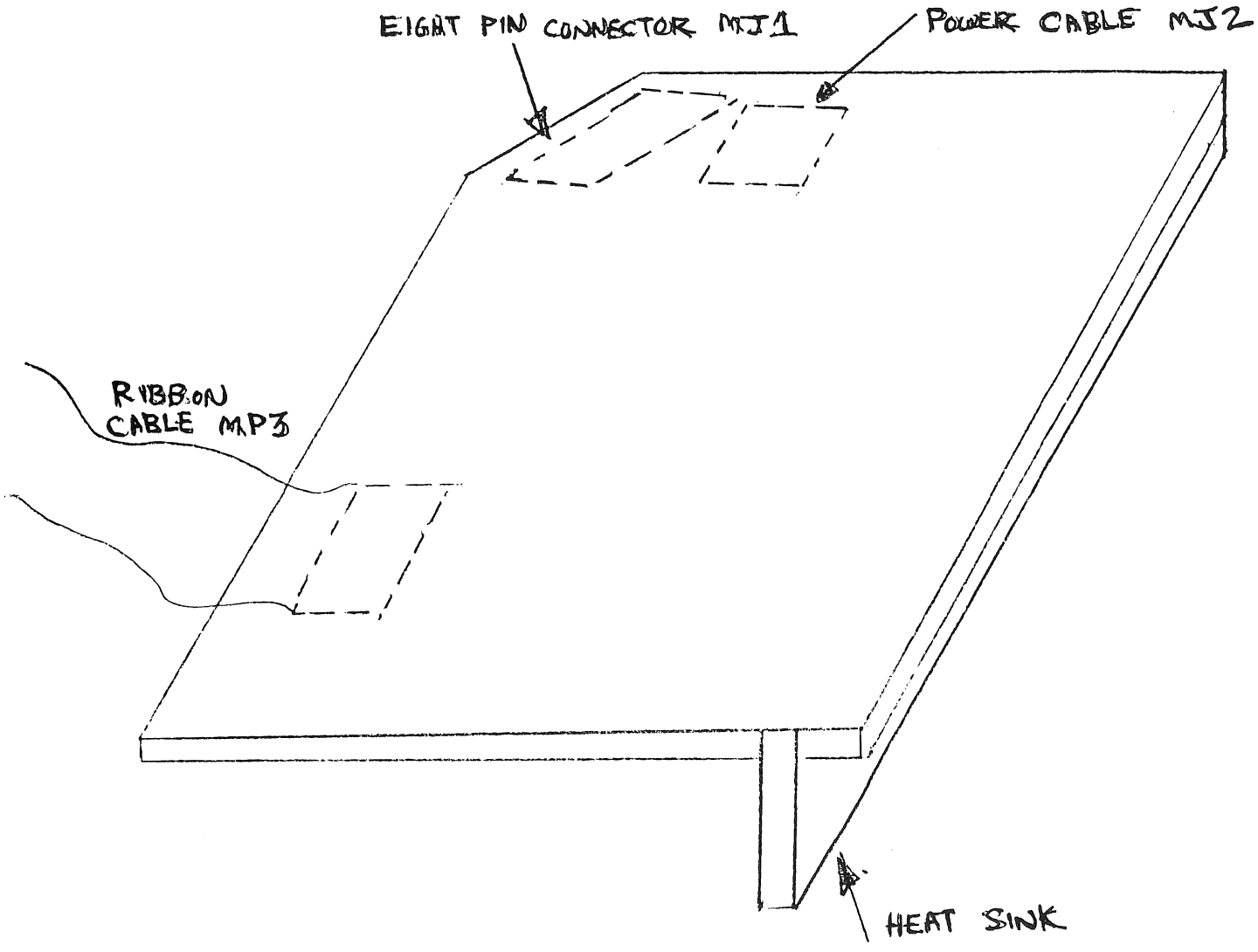


FIGURE 1-5

MOS Regulator Assembly

To Be Supplied

FIGURE 1-6

Core Regulator Assembly

CHAPTER 2

SYSTEM UNITS, OPTIONS AND HARNESS

2.1 SYSTEM UNITS CONCEPT

This chapter describes the concept of the DEC System Units in general and the DD11-P nine-slot backplane in particular. These units have been developed to implement the new Modified Unibus system while maintaining a Standard Unibus input/output interface. This development allows system interfaces to remain the same and increases the flexibility of internal interconnection.

2.1.1 System Units

The term system units has come into usage to identify the building block concept of all DEC systems. A System Unit consists of a matrix wired together to provide power and signal interconnections to accommodate a group of logic modules.

2.1.1.1 Single System Unit (see Figure 2-1) - The smallest System Unit is the Single System Unit. It consists of a four (1-4) by six (A-F) connector array, which is four hex slots used for module mounting, (see pDp-11/04 user's Guide - Configuration section). Many special system units are dedicated to a special set of modules, such as a disk interface. Slot 1 connectors A and B, and slot 4 connectors A and B are always used for Unibus Input and Unibus output connections, respectively.

2.1.1.2 Double System Units (see Figure 2-2) - This System Unit consists of a nine by six connector matrix. This unit has nine hex slots for module mounting.

Slot 1 connector A and B and slot 9 connector A and B are dedicated to Unibus input or beginning and Unibus output or termination, respectively.

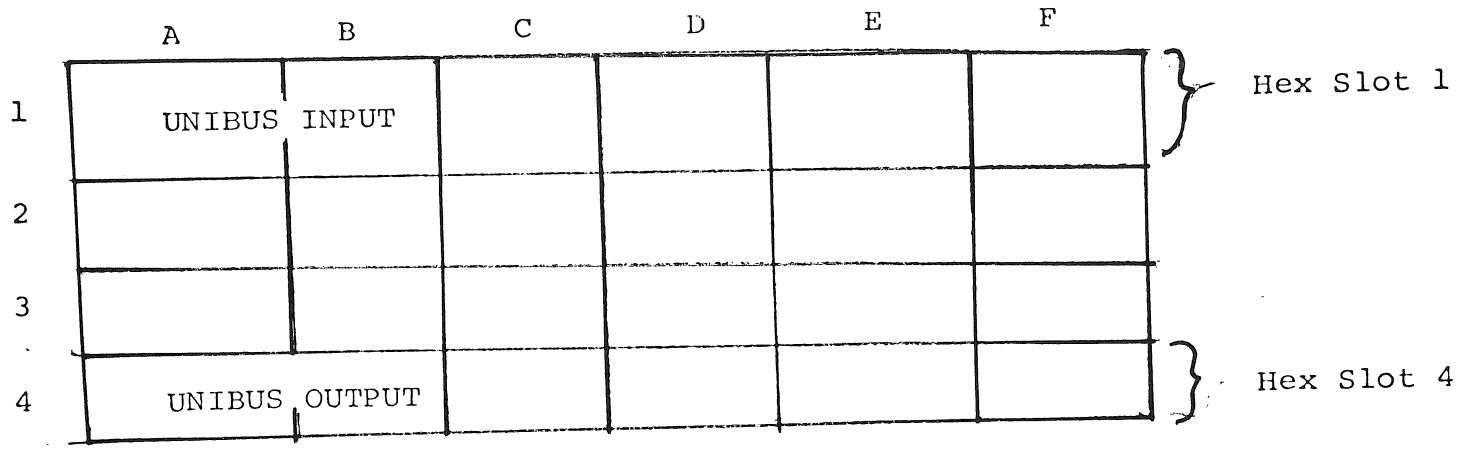


FIGURE 2-1

Single System Unit Array

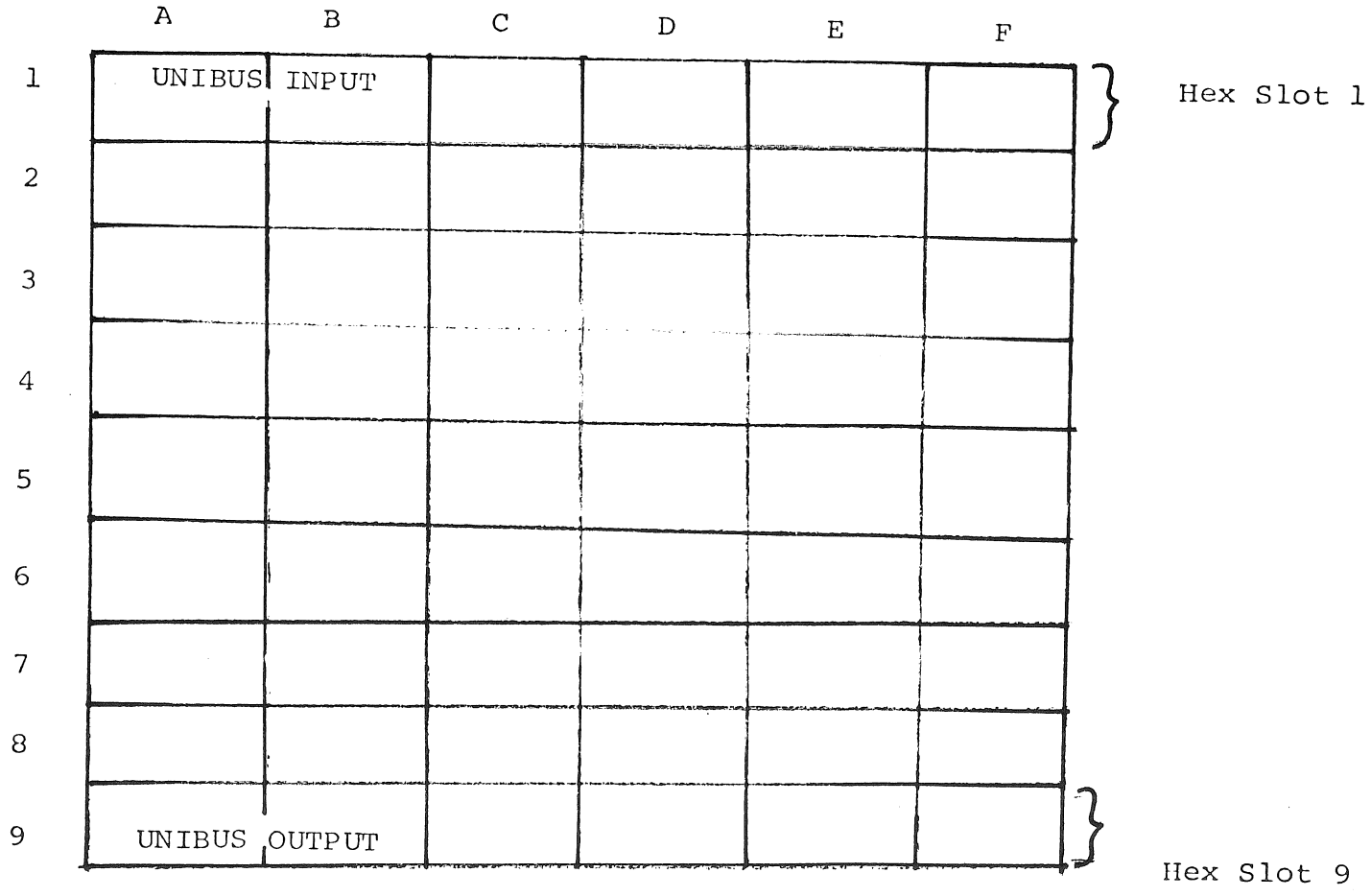


FIGURE 2-2
Double System Unit Array

2.1.1.3 Power Distribution - While Unibus control signals enter and leave a system unit via the Unibus cable, DC power for modules enters the System Unit via the DC Power Distribution Harness attached to the "A" connector end of the system unit printed circuit board backplane.

The power distribution harness, depending on type, consists of several high-current Mate-N-Lok connectors that are wired by a short harness to the System Unit (see Figure 2-3). The harness for the DD11-C backplane consists of a 15-pin Mate-N-Lok connector containing DC voltages and a 6-pin connector containing AC Lo, DC Lo and LTC signals. The harness for the DD11-P backplane consists of two 15-pin Mate-N-Lok connectors carrying DC voltages and a 6-pin connector containing AC Lo, DC Lo, and LTC signals. The power harness must be configured to match the power supply configuration employed by a given system. The H777 and H765 power supply systems used in the BA11-L (5 1/4") and BA11-K (10 1/2") expansion boxes have identical power distribution systems which means that the same power harnesses can be used in either box. See Table 2-1.

2.1.2. DD11-P Backplane

The DD11-P backplane is a double system unit designed for the PDP-11/34 and PDP-11/39 dual-hex CPU modules. Slot one is reserved for the CPU Control Module (M7266) and slot two is reserved for the CPU Data Path Module (M7265). The remaining seven slots are available for system configurations involving a wide variety of standard DEC memories and interfaces. Figure 2-4 defines slot usage.

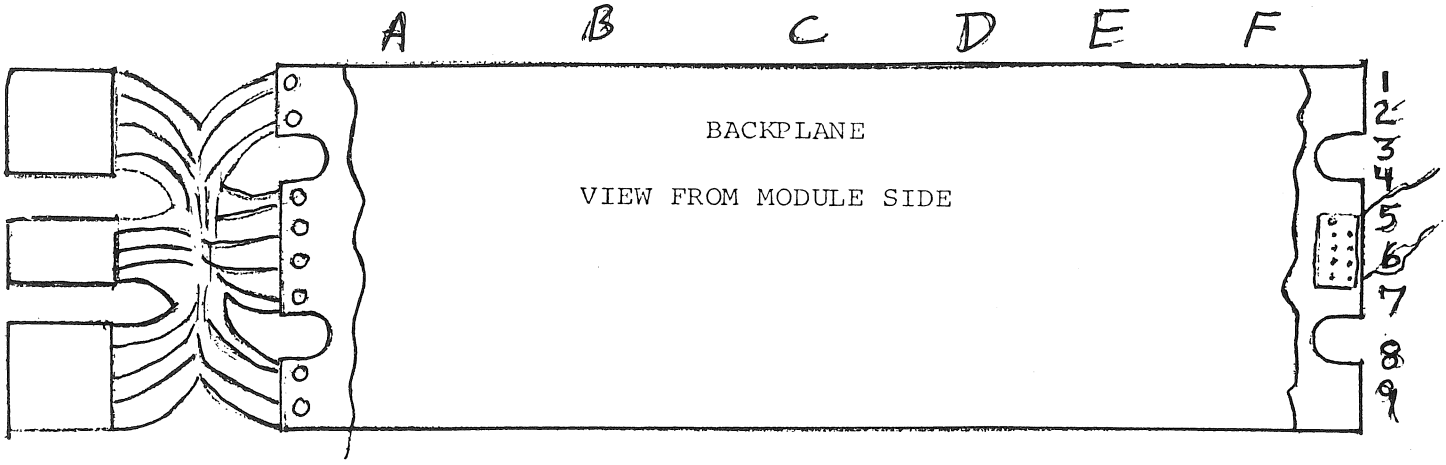


FIGURE 2-3

DD11-P Power Distribution Harness

BACKPLANE POWER HARNESS TO POWER DISTRIBUTION BOARD INTERFACE

TABLE 2-1

BA11-L/BA11-K Power Dist, BD Pin Assignment	Wire Color	DD11-C Harness Pin Usage D-IA-7011109	DD11-P Harness Pin Usage D-IA-7011108
#1 15-Pin Mate-N-Lok			
1 +5V	Red	X	X
2 +15V	Gray	X	X
3 +20	Orange	X	X
4 +5V	Red	X	X
5 GND	Black		
6 +15B	White	X	X
7 GND	Black		
8 GND	Black	X	X
9 GND	Black	X	X
10 (SPARE)	-----		
11 GND	Black		
12 +5V	Red	X	
13 -15V	Blue	X	X
14 -5V	Brown	X	
15 -15B	Green	X	X
#2 6-Pin Mate-N-Lok			
1 Lo GND	Black	X	X
2 LTC	Brown	X	X
3 DC Lo	Violet	X	X
4 AC Lo	Yellow	X	X
5 (SPARE)	-----		
6 (SPARE)	-----		
#3 15-pin Mate-N-Lok			
1 +5V	Red		X
2 +15V	Gray		X
3 +20V	Orange		X
4 +5V	Red		X
5 GND	Black		
6 +15B	White		
7 GND	Black		
8 GND	Black		X
9 GND	Black		X
10 (SPARE)	-----		
11 GND	Black		
12 +5B	Red		X
13 -15V	Blue		
14 -5V	Brown		X
15 -15B	Green		

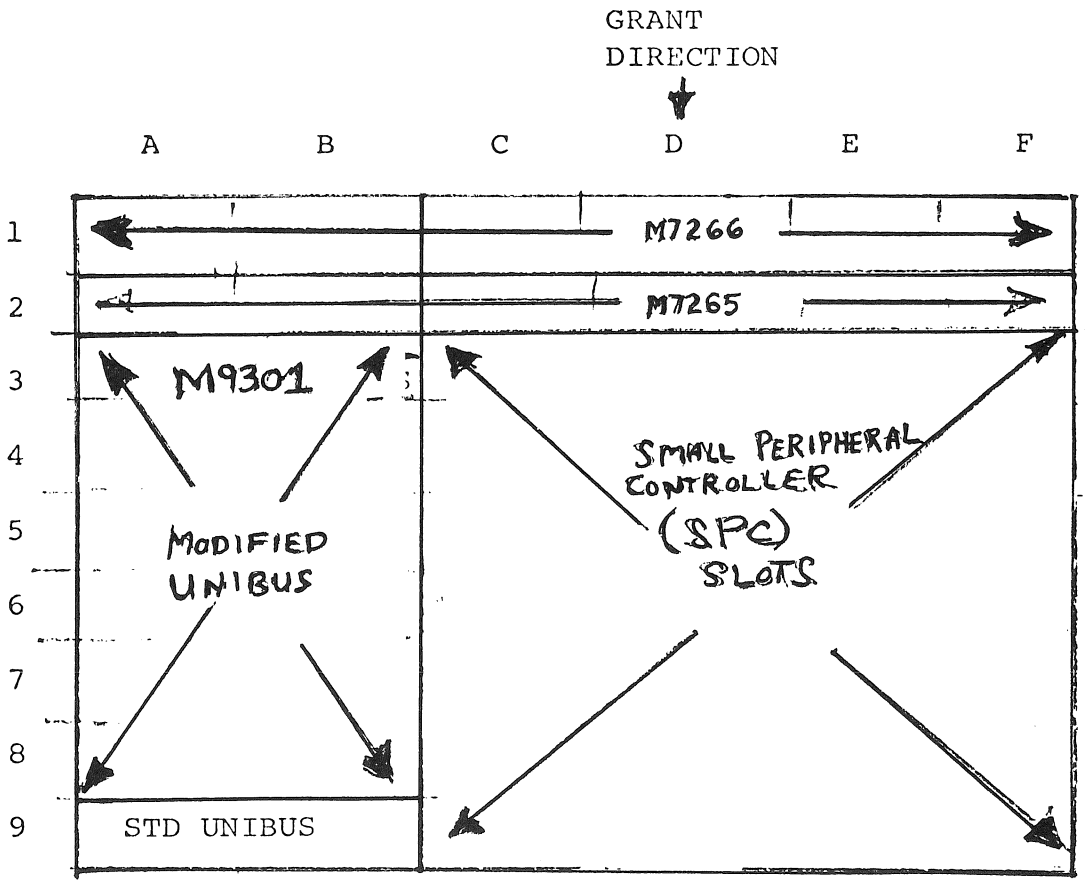


FIGURE 2-4

DD11-P Slot Usage

This backplane is very flexible, as there are no dedicated memory slots. The seven hex slots (slots 3 through 9) are broken up into two parallel bus structures: the SPC bus (paragraph 2.2.1.1) and the MUD bus (paragraph 2.2.1.2). Note that slot 9 connectors A and B are the standard unibus output slots.

2.1.2.1 Small Peripheral Controller (SPC) Bus - Small Peripheral Controllers can be quad (four-connector) or hex (six-connector) modules. The C, D, E, and F connectors are configured with all the unibus signals and some internal interconnect signals. Table 2-2 is a pin configuration chart of an SPC slot.

New layouts for SPC modules should consult to the New Module Layout Guide.

Any module specified as an SPC module can be mounted in any of the seven DD11-P expander slots (slots 3 through 8).

2.1.2.2 Modified Unibus Device (MUD) Bus - New battery-supported power rails were developed for MOS memory (MS11) and new core voltage rails were developed for the new core (MM11) memory. These features are included on the modified Unibus, which is incorporated in the DD11-P and DD11-C backplanes. In addition, the modified Unibus contains memory parity control signals. Devices such as MOS memory and the new core memory are connected to the modified Unibus and are designated Modified Unibus Devices (MUD).

This new bus is strictly internal to the DD11-C and DD11-P backplanes. To other system units the DD11-P and DD11-C look like standard Unibus system units.

The number of MUD modules used in the PDP11/34 and PDP11/39 systems vary; the module types are listed in Table 2-3.

The MUD bus is located on the A and B connector blocks on slots 2 to 8.

The pin configuration of the MUD bus is listed in Table 2-2.

A MUD module at present is either a double or a hex module. (Note that a double width MUD and quad width SPC can mount side by side to fill a hex slot.) The end of the Unibus must be terminated with an M9302 SACK turnaround terminator; no other terminator will work. The M9302 will be plugged into the last standard Unibus slot of the last backplane in the system. For example, in an 11/34 system with a nine-slot DD11-P backplane and a four-slot DD11-C backplane, the M9302 is plugged into slot 4A, 4B of the last backplane (four-slot backplane, in this case). As in another example, in an 11/04 system with two nine-slot DD11-P backplanes, the M9302 is plugged into slot 9A, 9B of the second DD11-P backplane.

Table 2-2 Modified Unibus and SPC Pins Slot 2-8

CONNECTOR SLOT

PIN#	A 1	A 2	B 1	B 2	C 1	C 2	D 1	D 2	E 1	E 2	F 1	F 2
A	INIT L	+5V	RESV BUS	+5V	NPG (IN)	+5V	TP	+5V	GND A	+5V	ABG OUT	+5V
B	INTR L	TP	RESV PIN	TP	NPG (OUT)	-15V	TP	-15V	ASSYN IN H	-15V	ABG IN	-15V
C	DØØ L	GND	BR5 L	GND	PA L	GND	A SEL 6	GND	A12 L	GND	SSYN L	GND
D	DØ2 L	DØ1 L	+5 BAT	BR4 L	LTC	D15 L	A OUT LOW	BR7 L	A17 L	A15 L	BBSY L	FOI N1
E	DØ4 L	DØ3 L	INT SSYN	PAR DET	TP	D14 L	A SEL 4	BR6 L	MSYN L	A16 L	FOI V2	DØ2 L
F	DØ6 L	DØ5 L	AC LO	DC LO	TP	D13 L	A SEL Ø	BR5 L	AØ2 L	C1 L	DØ5 L	DØ6 L
H	DØ8 L	DØ7 L	AØ1 L	AØØ L	D11 L	D12 L	AIN	BR4 L	AØ1 L	AØØ L	DØ7 L	A INT ENB
J	D1Ø L	DØ9 L	AØ3 L	AØ2 L	A INT B	D1Ø L	A SEL 2	A BR OUT	SSYN L	CØ L	NPR L	GND A
K	D12	D11 L	AØ5 L	AØ4 L	TP	DØ9 L	A OUT	BG7 SO	A14 L	A13 L	DØ3 L	A INT B
L	D14	D13 L	AØ7 L	AØ6 L	A INT ENB	DØ8 L	INIT L	BG7 OUT	A11 L	TP	DØ3 L	FOI LR
M	PA L	D15 L	AØ9 L	AØ8 L	TP	DØ7 L	A INT ENB A	BG6 SO	AIN	A OUT HIGH	INTR L	FOI MR
N	PAR P1	PB L	A11 L	A1Ø L	DC LO	DØ4 L	A INT A	BG6 OUT	A OUT LOW	AØ8 L	FOI N1	DØ4 L
P	PAR PØ	BBSY L	A13 L	A12 L	HALT REQ	DØ5 L	TP	BG5 SO	A1Ø L	AØ7 L	A BR OUT	FOI P2
R	+15 BAT	SACK	A15 L	A14 L	HALT GRT	DØ1 L	TP	BG5 OUT	AØ9 L	A SEL 4	FOI L2	FOI N1
S	-15 BAT	NPR L	A17 L	A16 L	PB L	DØØ L	TP	BG4 SO	A SEL 6	A SEL Ø	FOI N2	FOI P2
T	GND	BR7	GND	C1 L	GND	DØ3 L	GND	BG4 OUT	GND	A SEL 2	GND	SACK L
U	+20 (CORE)	BR6	SSYN L	CØ L	+15/+18	DØ2 L	TP	ABG IN	AØ6 L	AØ4 L	A INT A	A BR OUT
V	+20 (CORE)	+20 (CORE)	MSYN L	-5 (CORE)	AC LO	DØ6 L	ASSYN IN H	ABG OUT	AØ5 L	AØ3 L	A INT ENB A	FOI V2

CONNECTOR SIDE

TABLE 2-3

Modified Unibus Devices

M9301	Bootstrap/Terminator	Dual Module
M9306	MUD Terminator	Dual Module
M9850	Memory Parity Control	Dual Module
M7847	MOS Memory (MS-11)	Hex Module
G221	Core Memory (MM11-B, -C)	Hex Module with Quad Daughter
G222	Core Memory (MM11-D)	Hex Module with Hex Daughter

CAUTION

Never install an M9302 SACK Turnaround Terminator or an M930 Unibus in a MUD slot. Doing so will apply MUD power rails to bus grant and ground lines on the M9302.

2.1.2.3 Non-Processor Grant (NPG) Line - The NPG signal is used by only those interfaces designed to do Non processor Requests. A Non-Processor Request is a transfer of data from one device in a system to another device in the system without CPU intervention.

There are very few NPR devices that are also SPC devices. Therefore, the NPG line grant continuity is provided by wire-wrap jumpers on the backplane. When an NPR module is assigned to a slot, the corresponding wire-wrapped jumper on CA1 to CB1 of that slot must be removed. This jumper permits the Grant signal to be routed to the next module. The NPG signal routing through the backplane is shown in Figure 2-5.

2.1.2.4 Bus Grant (BG) Line - Bus Grant continuity cards are required in all slots that do not contain modules. These cards permit the Grant signal to be passed from module to module (see Figure 2-6).

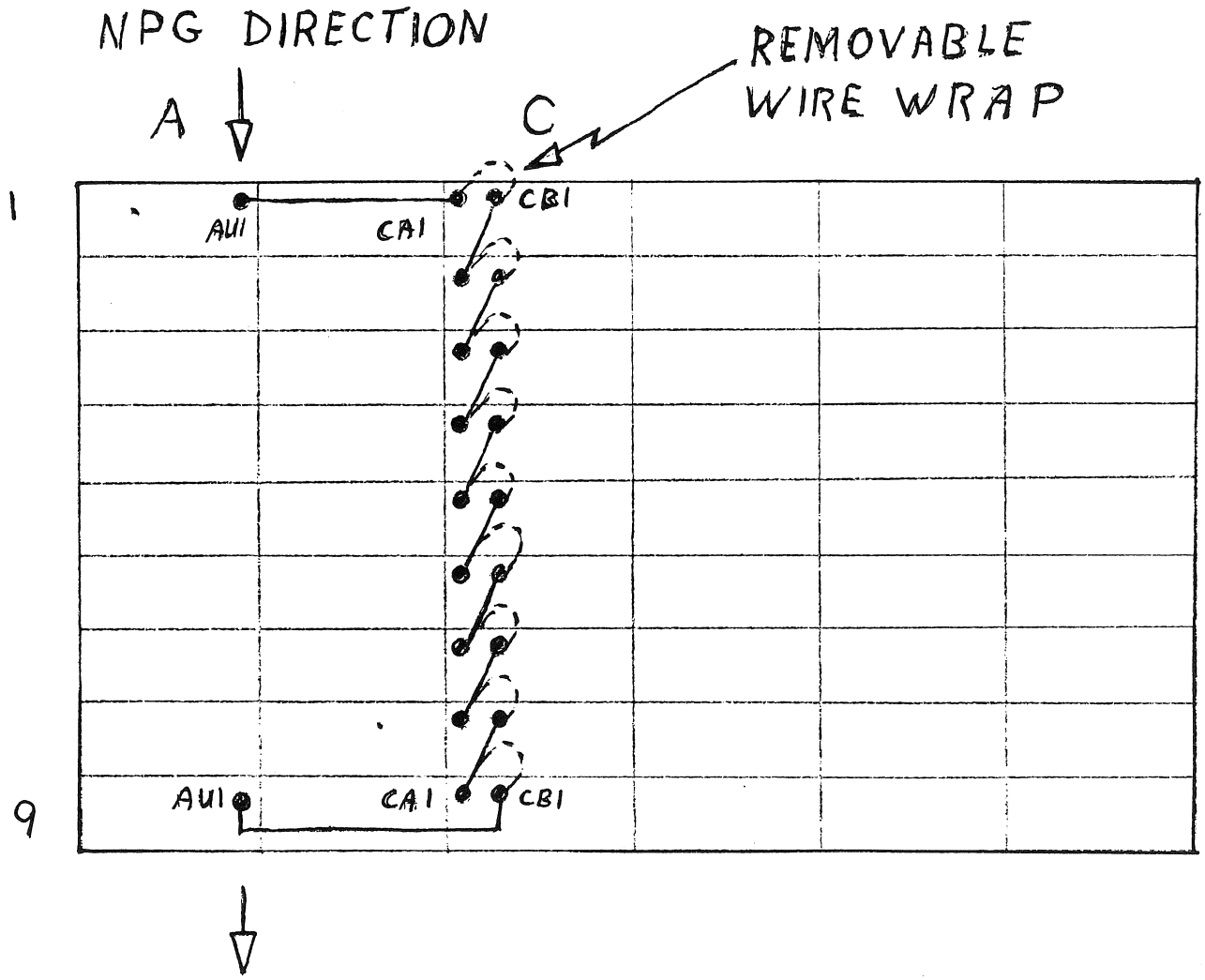


FIGURE 2-5

NPG Signal Routing

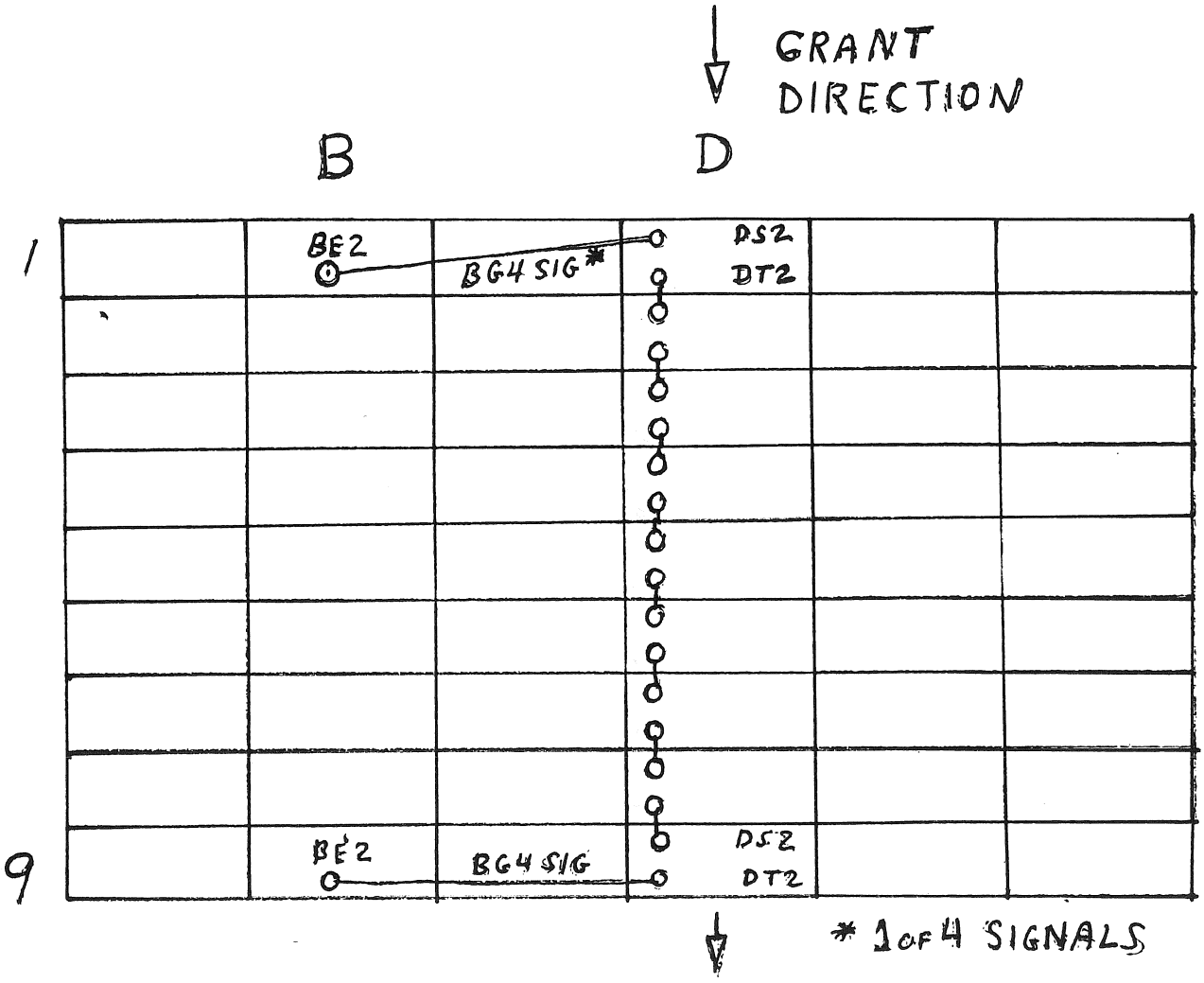


FIGURE 2-6

Bus Grant Routing

CHAPTER 3

H777 POWER SUPPLY

3.1 GENERAL

This chapter describes the H777 power supply, which is housed in the BA11-L Mounting Box. This supply provides the operating voltages for the PDP-11/34 and PDP-11/39 Processing Systems. A battery backup supply is available for systems employing MOS memory. The backup is designated H775 and provides backup power in the event of a power supply failure.

3.2 PHYSICAL DESCRIPTION

The H777 Power Supply mounts on the righthand side of the BA11-L mounting box (see Figure 3-1), and the DD11-P backplane is mounted on the left hand side of the box. power to the backplane is provided by a connector at the rear of the power supply; power to the operator's console is provided by a connector at the front of the power supply (see Figure 3-1).

The power supply contains the following five assemblies (see Figure 3-2):

- AC control assembly
- +5V main regulator
- MOS regulator + or -15V, +5V
- Core regulator +20V, -5V
- Fan

3.2.1 AC Control Assembly

The AC Control Assembly contains all of the hardware (i.e., line cord, relay, filter, circuit breaker, and main transformer) associated with the line voltage control. The H777 system is limited by its main transformer to 240 watts of regulated DC output. This limit should not be exceeded in steady state operation. (See Table 3-1 for complete characterization of the limits of operation). Internal thermal protection will shut-down the individual regulator assemblies before dangerous conditions are reached. This shutdown is a power-fail sequence and is provided by a thermal switch on the main

regulator in order to preserve MOS memory data.

The H777 provides a controlled turn-on by limiting the inrush current. With no controlled turn-on, high-surge currents could trip circuit breakers causing the shut-down of rack power. This feature is important in systems containing multiple mounting boxes.

To Be Supplied

FIGURE 3-1

BA11-L Mounting Box Showing Connectors and Cables

3.2.2 +5V Main Regulator

The +5 Main Regulator provides 25 Amps of regulated DC power and acts as a source of raw DC for other regulators. It also contains power up/down sequencing circuitry, control input (ON/OFF/STAND BY), and Unibus AC Lo, DC Lo signals.

3.2.3 MOS Converter

The MOS Converter provides + or -15 volts for use within the H777 and as an output to the DD11-P for MOS memory and various module options. Both switched and unswitched (battery backup) sources are provided. This assembly also supplies +5 volts (+5B) to the MOS Memories for battery-supported refresh operation. The H777 system clock is contained on the MOS converter assembly.

3.2.4 Core Memory Regulator (Optional)

The last assembly (optional regulator) is a removable unit capable of driving core memories at +20 and -5 volts from the raw DC source contained on the main regulator.

3.3 BLOCK DIAGRAM DESCRIPTION

Figure 3-3 is a block diagram of the H777 power supply. The figure shows the four major assemblies of the supply plus the optional H775 battery back-up unit. Each assembly is divided into functional blocks for the following description.

3.3.1 AC Control Assembly

The transformer, AC Control interface, and main rectifier/filter are shown in the upper left corner of Figure 3-3, and are labelled RAW DC (RDC). RDC flows to all of the regulator blocks which are contained in:

- the Main Regulator Assembly (upper right)
- the MOS Regulator (center right)
- the +20V Core Regulator (lower right)

Figure 3-3 also shows the type of output obtained from each power or signal producing block, along with its general destination.

3.3.2 Clock

The clock is a square-wave oscillator used to synchronize all of the switching regulators within the H777 and to provide the carrier upon which each pulse width Modulator (PWM) operates. The modulated carrier is fed to each power switch element at a duty cycle that is appropriate to maintain constant and proper voltage. The modulation of the carrier within each regulator is described in subsequent paragraphs.

To Be Supplied

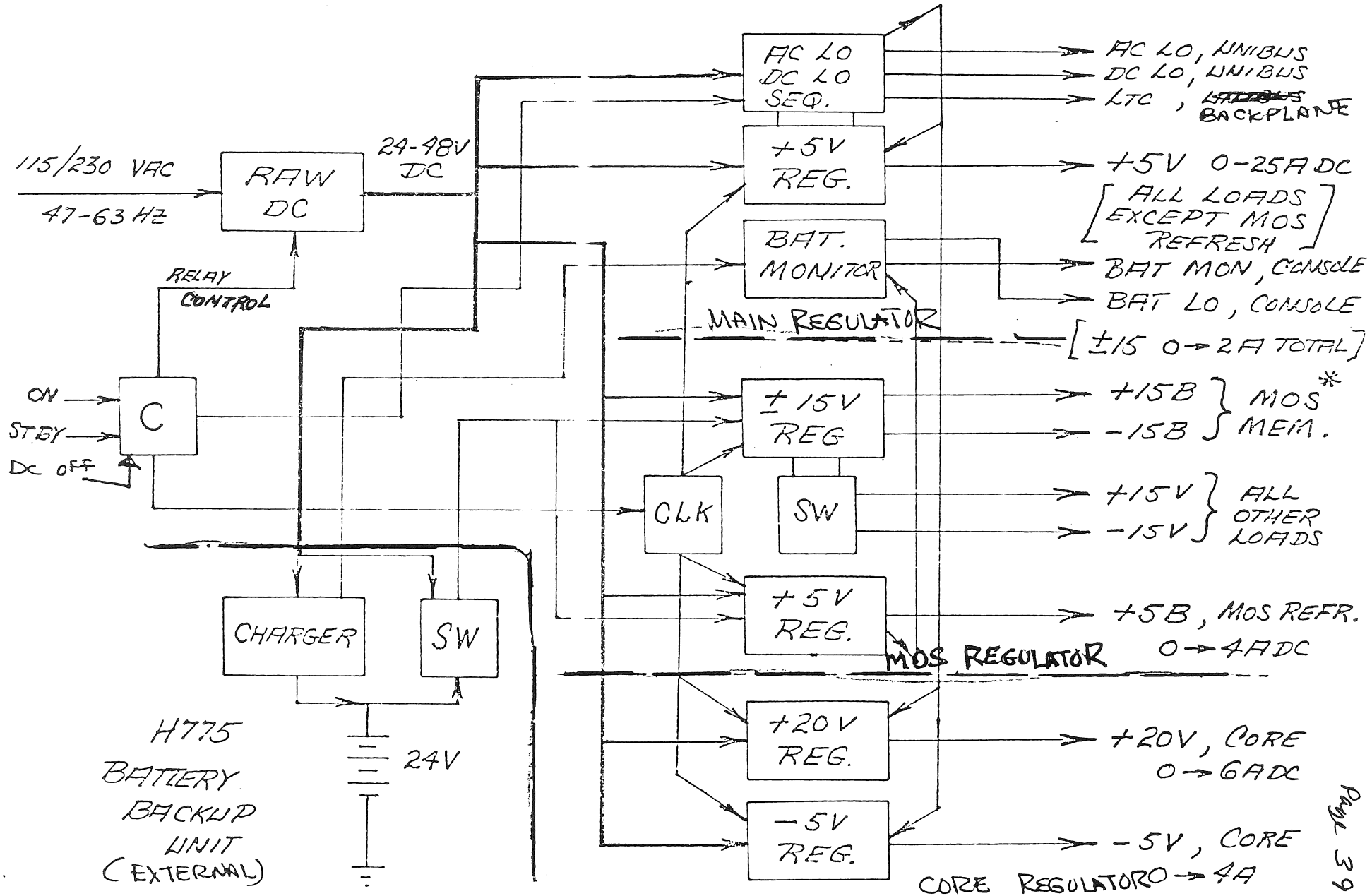
FIGURE 3-2

Major H777 Power Supply Components

See Page 39A

FIGURE 3-3

Block Diagram of H777 Power Supply


115/230 VAC
47-63 HZ
RAW DC
24-48V DC
RELAY CONTROL
ON
STBY
DC OFF
C
CHARGER
SW
24V
H775 BATTERY BACKUP UNIT (EXTERNAL)
AC LO
DC LO
SEQ.
+5V REG.
BAT. MONITOR
MAIN REGULATOR
±15V REG
CLK
SW
+5V REG.
MOS REGULATOR
+20V REG.
-5V REG.
AC LO, UNIBUS
DC LO, UNIBUS
LTC, BACKPLANE
+5V 0-25A DC
[ALL LOADS EXCEPT MOS REFRESH]
BAT MON, CONSOLE
BAT LO, CONSOLE
[±15 0→2A TOTAL]
+15B
-15B
MOS MEM.
*
+15V
-15V
ALL OTHER LOADS
+5B, MOS REFR.
0→4A DC
+20V, CORE
0→6A DC
-5V, CORE
CORE REGULATOR 0→4A

3.3.3 Switch for +15V Isolation

Note the SW (switch) box associated with the + or -15v regulator. This switch isolates the + or -15v (used for peripherals) from the + or -15B (used for MOS memory). If the system should go on battery back-up, isolation of the + or -15v from the + or -15B will maximize the battery back-up time for MOS memory which represents the critical volatile storage load. The peripherals (non-critical load) will, consequently, not have battery back-up in this case.

Another feature of the switched + or -15 output is that module swapping of non-memory modules may be accomplished in STBY mode without losing the contents of memory.

3.3.4 Control for Console Interface

The control box (designated C) represents the console interface where the power switch ON and STBY (Stand by) functions are applied to the H777. In the "STBY" state, the + or -15 and the +5B regulators are strobed to provide regulated voltages for MOS memory. The main +5 and optional +20v and -5V regulators are not strobed. In the "DC OFF" state, the clock is inhibited so that no carrier is applied to any of the regulators. In the "DC OFF" state, AC power is still applied.

3.4 DETAILED CIRCUIT DESCRIPTION

The following paragraphs provide a detailed description of the circuits comprising the H777 power supply.

3.4.1 Raw DC Circuitry (Refer to Figure 3-4)

The Raw DC section produces a low DC operating voltage (normally 33 + or -9 volts for each of the regulators. This single positive source supplies power to all of the regulators (so that battery support could be applied from one single battery). The RDC section also provides ride-through (power protection against the loss transients) for the power supply by virtue of the energy stored in capacitor "C".

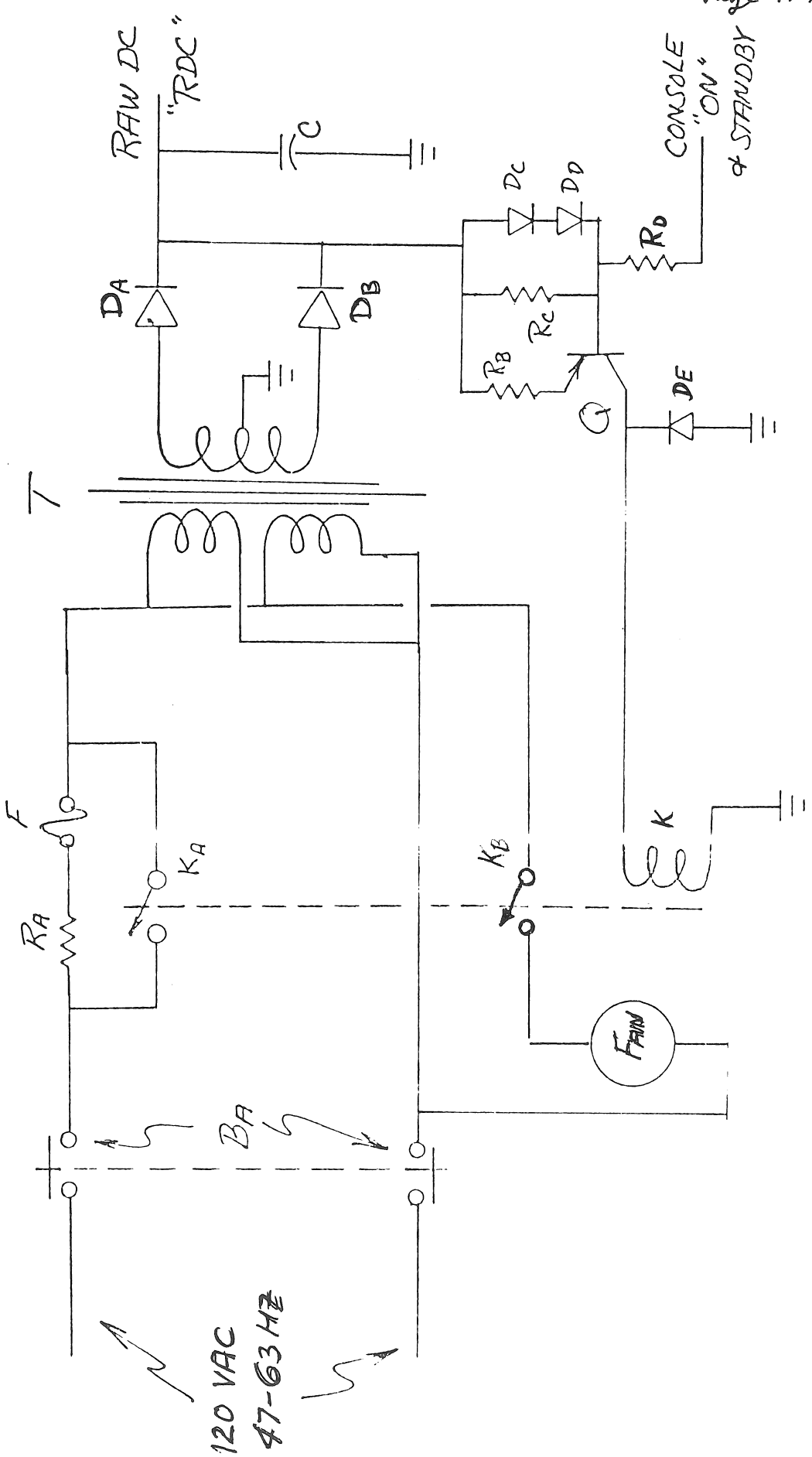
NOTE

All components to the right of "T" are located on the Main Regulator Assembly. The remaining components (except for fan) are located on the AC control assembly.

See Page 41A

FIGURE 3-4

Raw DC and Relay Driver Circuits H777


RAW DC
"RDC"
C
DA
DB
DC
DD
RD
CONSOLE
"ON"
or STANDBY
RC
RB
DE
G
T
F
KA
RA
KB
K
FAN
BA
120 VAC
47-63 HZ

3.4.1.1 Circuit Breaker BA - The Circuit Breaker (BA) provides overcurrent protection in the event of a failure within the H777 and creates a convenient line-disconnect for servicing.

3.4.1.2 Inrush Current Limiting - Resistor Ra limits inrush current on power line closure and is bypassed during operation by Relay Ka. The fuse (F) protects Ra in the event of Ka failing to close.

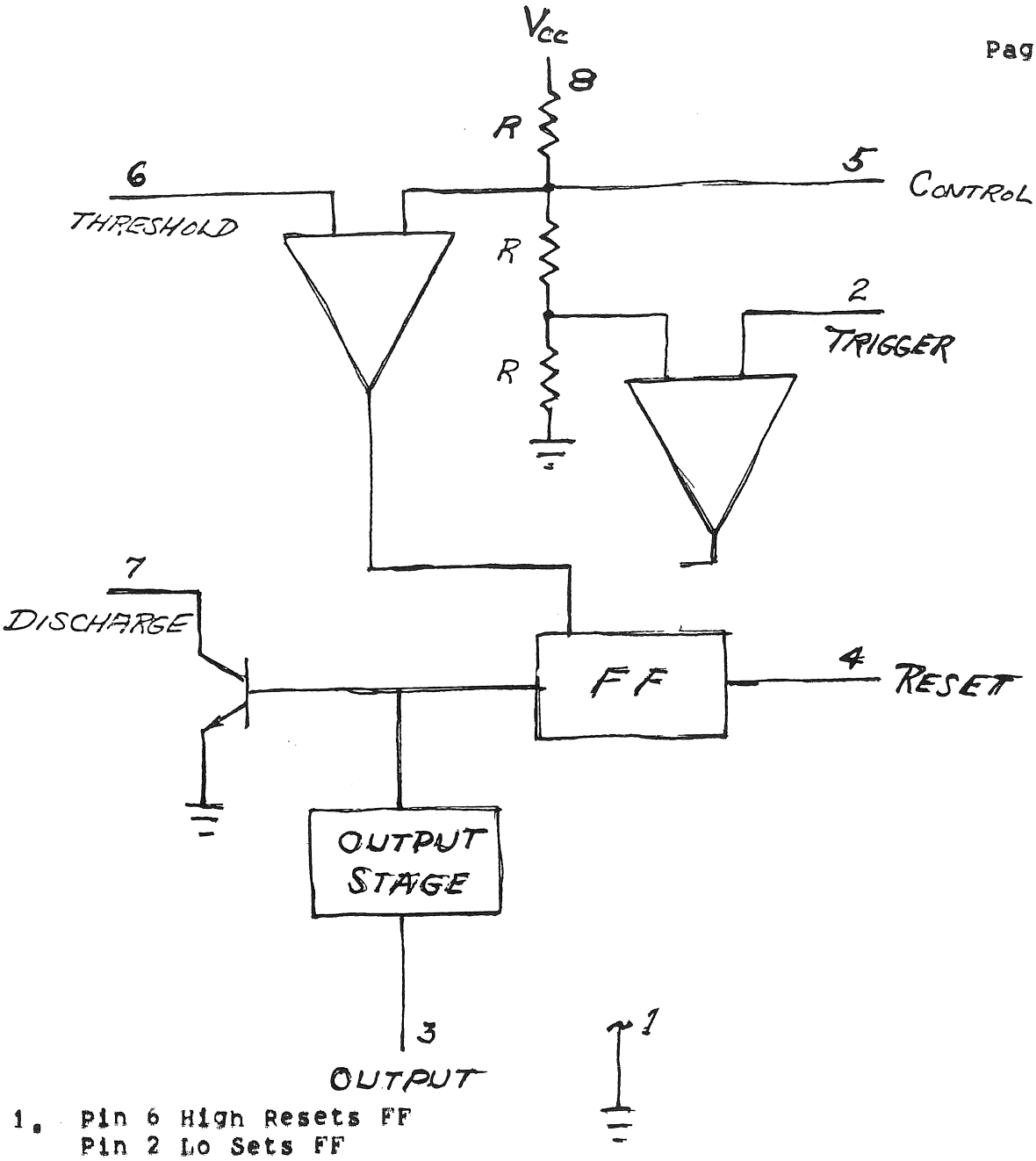
3.4.2 The 555 Timer (Refer to Figure 3-5)

The 555 Timer is located within the Clock logic. Because the 555 IC Timer performs various functions within the H777, a brief description of its operation is presented. The device, as used here, is an 8-pin DIP (dual inline package). Several of its characteristics are listed along with an internal block diagram in Figure 3-5.

The device contains a resistive divider chain to set an input to each of two comparators at 1/3 Vcc and 2/3 Vcc. The comparator outputs can set and reset a flip-flop, whose output controls a bilateral output driver, which is a device that can source or sink current.

The flip-flop can be manually reset by reducing the reset pin level at pin 4 to 0.4V. The output of the 555 inverts the state of the FF, as follows:

- FF Set = Output High (source current)
- FF Reset = Output Low (sink current)



1. Pin 6 High Resets FF
   Pin 2 Lo Sets FF
   Pin 3 High with FF set,
   Transistor "ON" with FF reset

2. Output can source or sink current (100 ma maximum)

3. Reset pin overrides trigger; holds output Low for reset low,

4. All "R" are equal value.

5. Output will remain High as long as Trigger is Lo (Pin 4 High).

6. V(cc) = 18V maximum

FIGURE 3-5

555 Timer

The so-called discharge transistor is "ON" when the output is low (FF Reset). The trigger comparator sets the FF when V(pin 2) < 1/3 Vcc(or < 1/2 V(pin 5).

The Threshold Comparator resets the FF when V (pin6) > 2/3 Vcc (or > V (pin5). Within the H777, the device is used as a relaxation (free-running) oscillator, as a one-shot, and as a pulse-width modulator (PWM).

The first application of this device is in generation of the H777 carrier or clock signal.

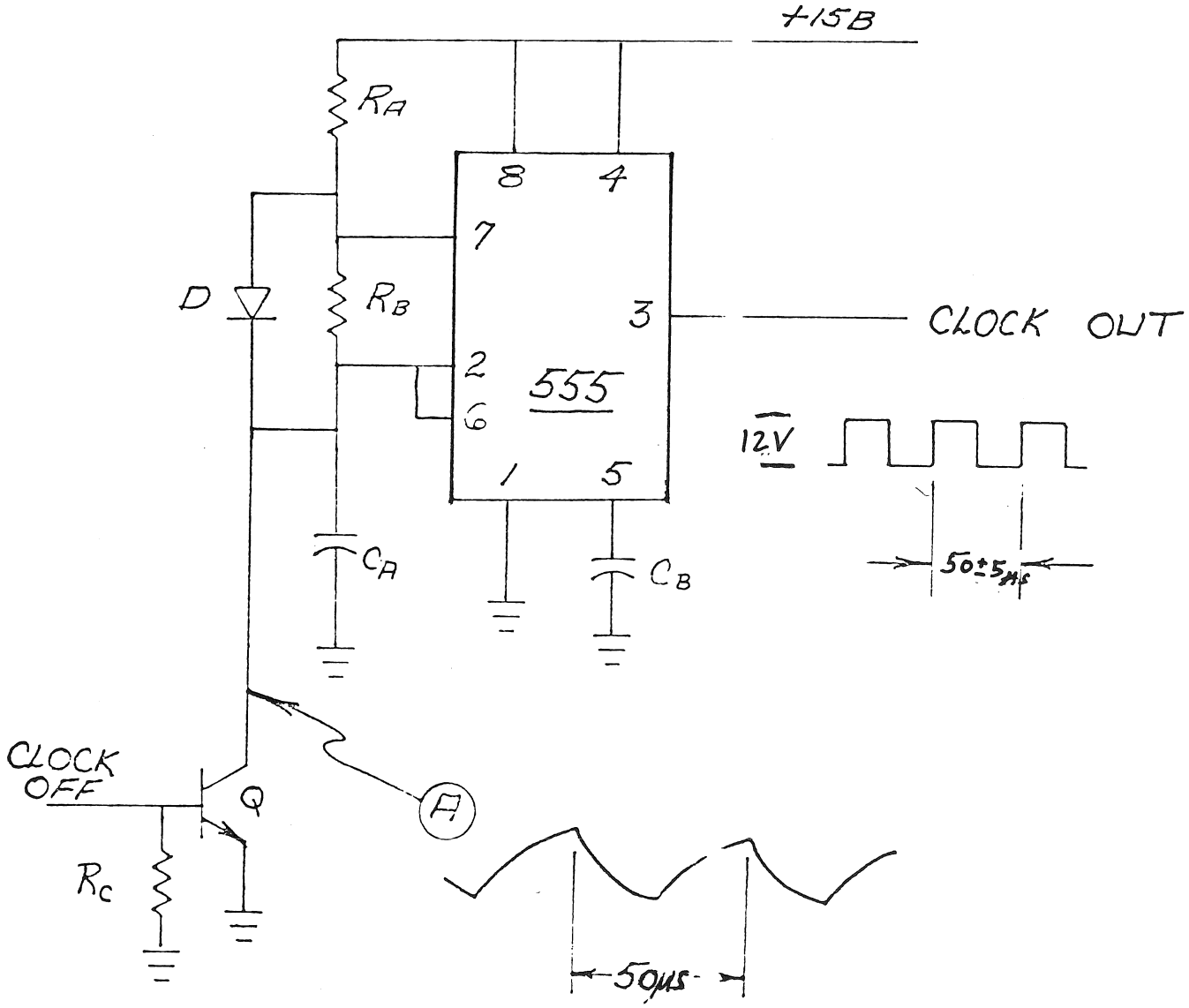
3.4.3 Clock Circuit (Refer to Figure 3-6)

The H777 Master Clock generates a 20 KHZ (+ or -2 KHZ) square wave carrier with an amplitude of 12 volts.

The circuit that generates this carrier centers around a 555 Timer as a Free Running Relaxation Oscillator.

In operation, the Timing Capacitor (Ca) is charged through Ra and D toward 15 volts. Upon reaching 10 volts (2/3 Vcc) the 555 "turns-over" and discharges Ca via Rb and its internal "discharge" transistor. That transition coincides with a negative-going transition at the output of Pin 3. When the voltage on Ca (Pin 2 & 6) falls to 5 volts (1/3 Vcc), the 555 "turns-over" again, opening the discharge transistor and allowing Ca to charge up again. That turn-over coincides with an output transition from Low to High. The cycle continues with Ca oscillating between 1/3 Vcc and 2/3 Vcc. Because the "turn-over" points are proportional to Vcc in fixed ratio, the oscillator frequency (or period) will be independent of Vcc.

The output of this clock can source and sink up to about 100 ma and still maintain an acceptable waveform.



Capacitive relaxation oscillator used to generate a 20 KHZ master clock-in the H777 MOS converter.

This clock synchronizes all of the switching regulators of the H777.

FIGURE 3-6

H777 Clock Circuit

3.4.4 Series-Connected Power Switching Stage (typical +5B, +20) (Refer to Figure 3-7)

This power handling stage is identical to those used in the +5B and +20 regulators and, with a different filter section, is similar to the + or -15 and -5V regulators of the H777. The main +5V switch is described in paragraph 3.4.8.

The power switch is Q(A). This is called the "Pass element". It gets base drive from Q(B) which in turn, is controlled from other circuitry via R(E). Current flow through R(E) switches the stage ON. Removal of the current allows the stage to resume blocking, or switch OFF. The combination of R(B), R(C), D(A), D(B), and Q(B) forms a Fixed Current driver for the pass Element. This driver limits the maximum base current that can flow in the pass element, thereby preventing overstress on the pass transistor base-emitter junction and protecting the driver from excess collector current in the event of pass element failure.

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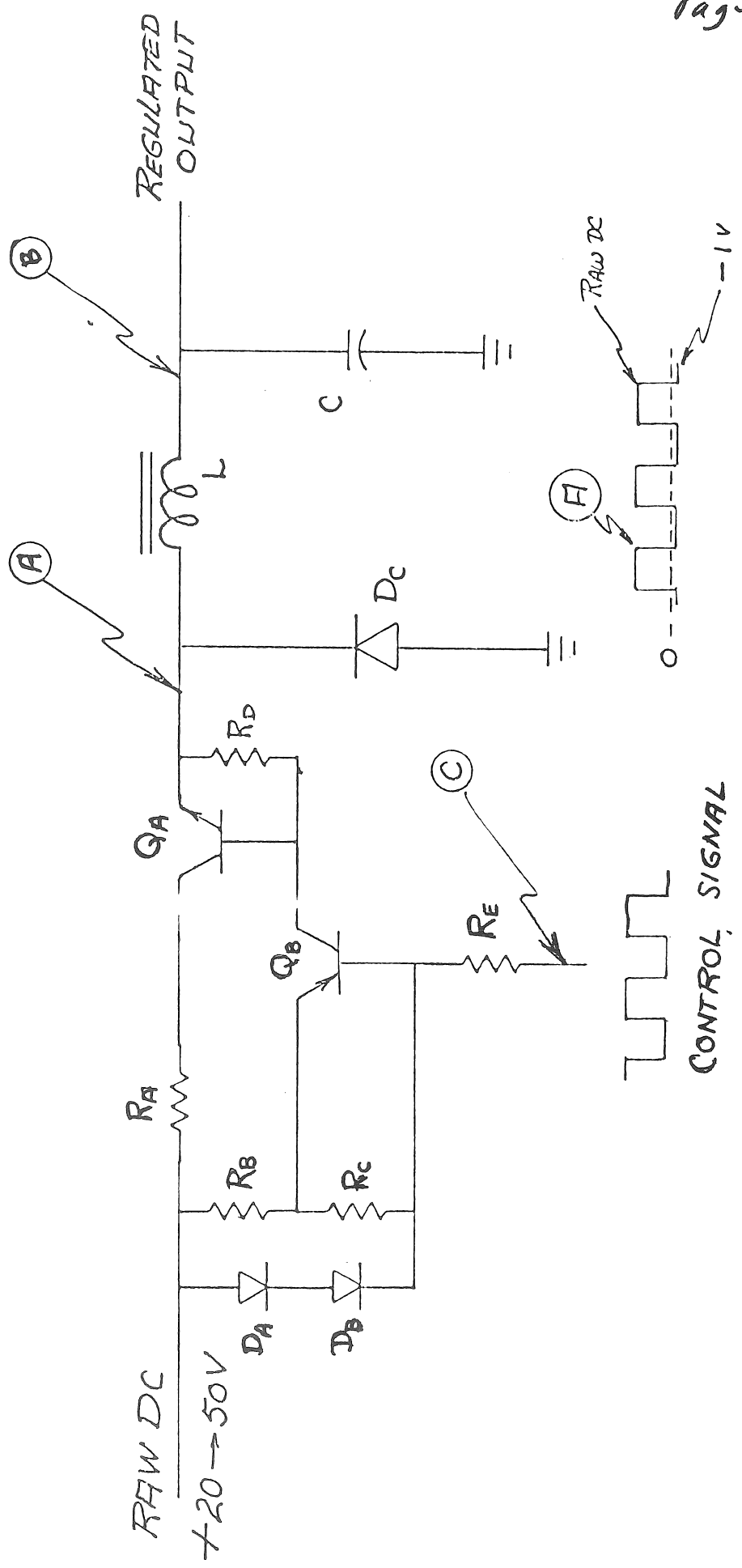
- L and C form an averaging filter.
- The voltage waveform at point A follows the current waveform at point C, and the filter averages that voltage to yield smooth DC at point B.
- D(C) is called a "free-wheeling" diode.

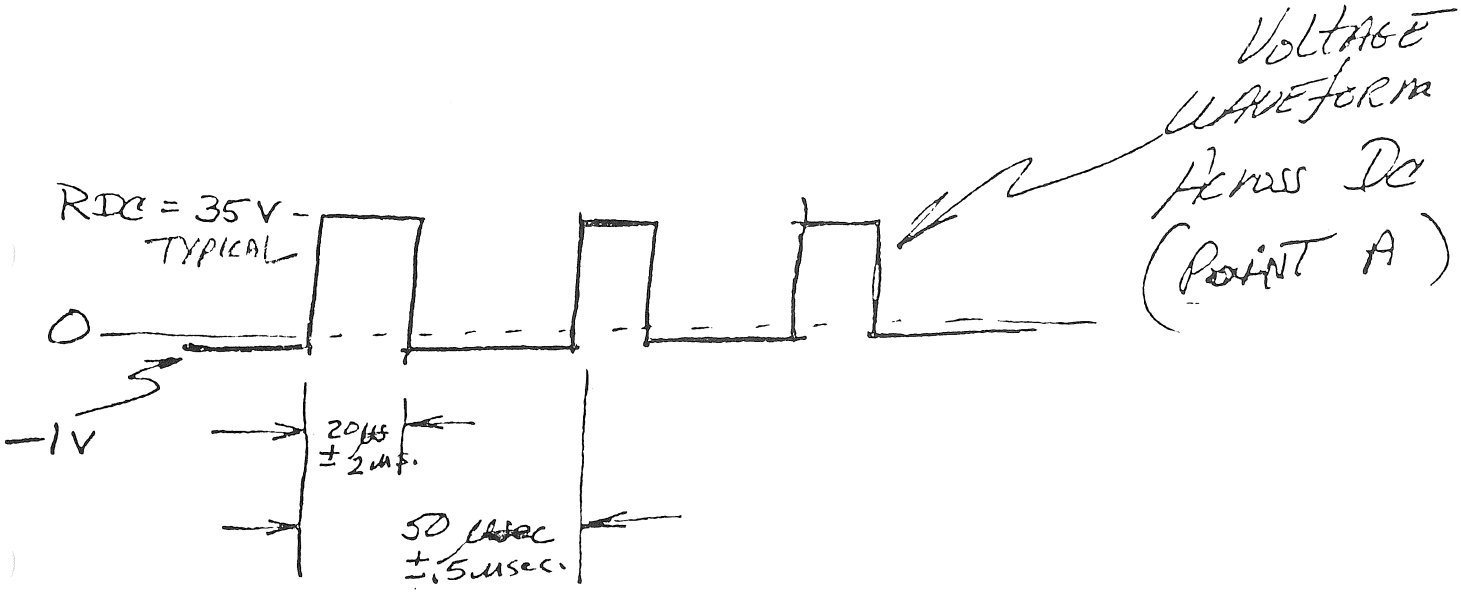
FIGURE 3-7

Typical Regulator Series Switching Stage


REGULATED OUTPUT
B
A
C
L
D_C
R_D
Q_A
Q_B
R_E
R_A
R_B
R_C
D_A
D_B
RAW DC
+20 → 50V
RAW DC
-1V
0
A
CONTROL SIGNAL

The raw DC source (20 to 50V) is switched across D(C) by the above action of the pass element and driver. The averaging filter (L and C) create a relatively smooth DC (from this chopped input) of a magnitude equal to the time average value of the chopped raw DC.

Example:



By changing the width of the "ON" pulse that is fed to the LC filter, the value of the output DC can be changed. The process called pulse width modulation (PWM) is accomplished by a feedback path as described in paragraph 3.4.

If RDC = 35V and the pass element is "ON" for 20 usec out of a 50-usec period: (Diode D(C) conducts for 30 usec 1v drop)

E(AVG) =

$$= 35v \times \frac{20}{50} - (1V) \times \frac{30}{50} = 13.4 \text{ Vdc output @ Point B}$$

If the pass element were "ON" for 8.0 usec

$$E(AVG) = 35 \times \frac{8.0}{50} - 1 \times \frac{42}{50} = 4.76 \text{ Volts output}$$

If RDC increases, the pulse width must decrease to maintain a constant output value. The reverse is also true. Note that changes in load current (the output current from the regulator) do not enter into the determination of output voltage. The 13.4 Vdc and 4.76 Vdc previously calculated are independent of load current. Therefore, modulation of the drive pulse width is only necessary to overcome changes in line

voltage (RDC Level) and to compensate for variable losses in components due to load current changes.

3.4.5 The Flyback Stage (+ or -15V Filter Scheme) (Refer to Figure 3-8)

Figure 3-8 shows a different method of connecting the previously described filter section; diode, choke, and capacitor. This scheme is used in the + or -15V regulator. Here the choke (L(A) connects across the filter input terminals, swapping places with the freewheeling diode (D(A)). A capacitor (C(A)) is still found across the filter "output" terminals. Note that the "power switch" is the same as previously described.

The same kind of PWM signal is applied by the power switch stage, this time across L(A), during the "ON" portion of the cycle. During the "OFF" portion of the cycle, the same series connection of L(A), D(A), AND C(A) exists. "Flyback" is the term applied to this period when energy previously stored in L(A) is released to maintain current flow around the series loop. When the power switch turns "OFF", the polarity of the voltage across L(A) reverses and its magnitude builds up until it reaches a level high enough to maintain current flowing in the same direction through L(A). The level that must be reached is equal to the voltage on C(A) plus one diode drop (D(A)). Current in the loop (L(A), D(A), C(A)) will decrease slowly until the switch turns on again, causing the current to rise in L(A). Note that the positive terminal (Anode) of C(A) is grounded. The output voltage from this Flyback circuit is, therefore, negative (-15V).

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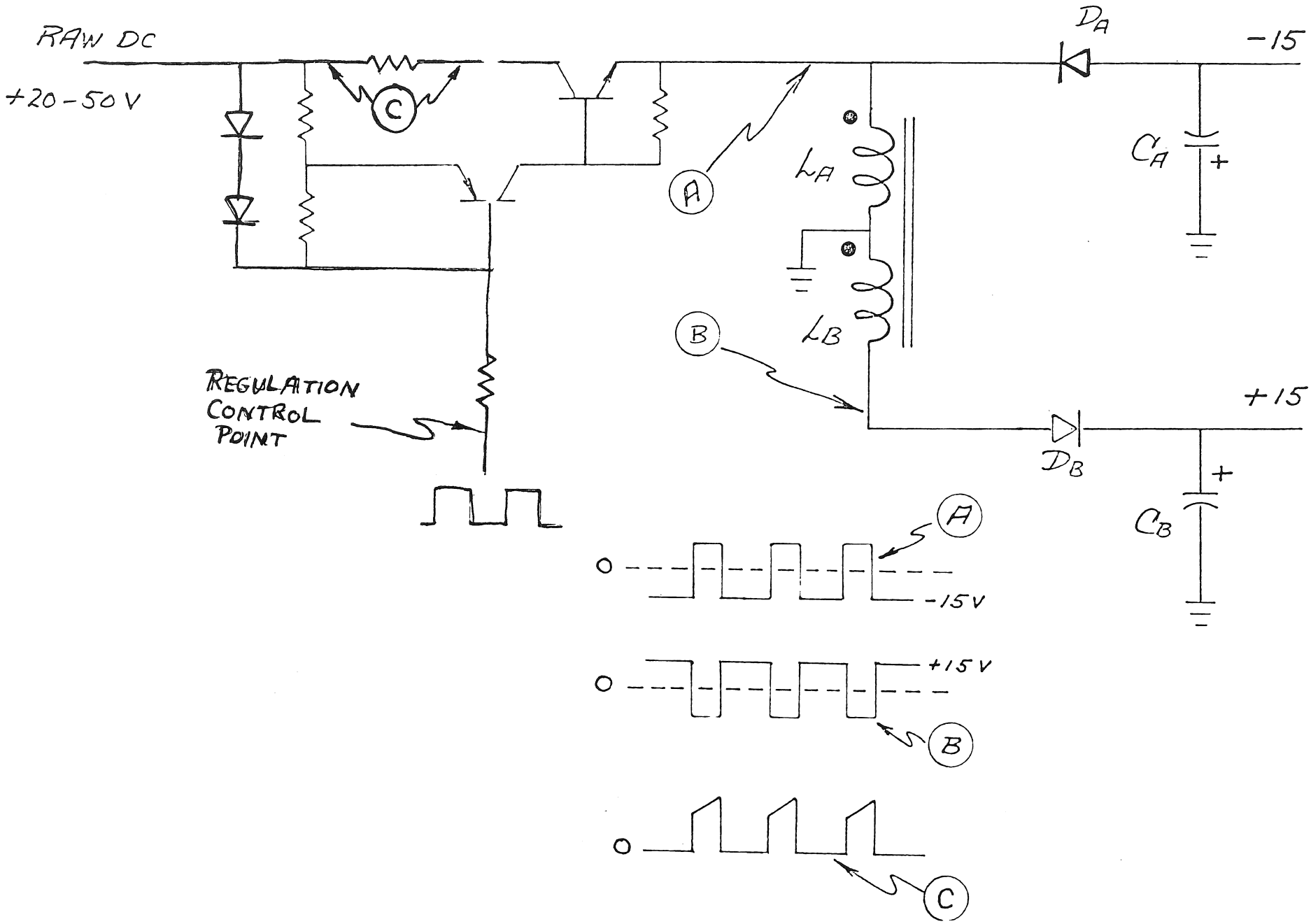
Either (+ or -) output can be used as the "sense point" or input to a feedback system that will provide a regulation capability.

FIGURE 3-8

Flyback Circuit Used in + or -15v Regulator (produces Symmetrical Output Voltages)


RAW DC
+20-50 V
C
A
L_A
L_B
B
D_A
-15
C_A
+
REGULATION
CONTROL
POINT
+15
D_B
+
C_B
A
-15V
+15V
B
C

The remaining components L(B) (which is wound on the same core as L(A)), D(B), and C(B) produce a positive output voltage of equal magnitude to the negative voltage on C(A). Either half of the filter network can operate in the Flyback mode described above. Energy stored in the core by current flowing through L(A) during "ON" time can be released to either C(A) or C(B) during "OFF" time. If, for example, C(A) (-15V) has a lower voltage across it when "Flyback" time starts, it will clamp both windings (L(A) and L(B)) at that voltage level (e.g., -14.5V). Because C(B) is at 15V, D(B) is reverse-biased and doesn't conduct. C(B), however, will discharge through the load, down to 14.5 volts so that D(B) can again conduct on later cycles. The situation is the same when (+15V) C(B) is low. Either output can be used to supply power (+15 or -15) and the other output will assume the same voltage magnitude. Therefore, either could be used as the reference for regulation purposes. In the H777 MOS converter, +15V (C(B)) is used as the sensed output for regulation.

3.4.6 Control Circuit for Regulating (Main +5) (Refer to Figure 3-9)

To achieve a "regulated" output voltage (one that remains relatively constant as line voltage and/or load current change) from the power supply, it is necessary to introduce a feedback system that monitors the output level and makes adjustments within the supply circuitry to compensate for changes in that level. The adjustment that is made is in the width of the drive pulse that feeds the power switch stage associated with the output line being regulated. As mentioned previously, the process is called Pulse Width Modulation (PWM) and in the 5411597, +5 module, it is accomplished via the circuitry of Figure 3-9. In this diagram, the input, or sense, voltage of the regulator) is located on the right hand side, the modulated pulse train output appears on the left. The circuit can be separated into four sections;

- Voltage Reference
- Error Amplifier
- Current Source
- Pulse Width Modulator

3.4.6.1 Voltage Reference - The voltage reference element is D(B), a + or -2% tolerance zener diode. R(A) feeds a known current level through D(B) to maintain the zener voltage at 5.1V + or -2%. Capacitor C(C) is used to slow down the rate of rise of the reference voltage (and, hence the output voltage) during turn-on of the power supply. D(A) and R(D) are used to drive the reference to zero when control point X is grounded through an active device (like a transistor). The 5.1V + or -2% reference voltage is fed to the non-inverting input of error amplifier E(1).

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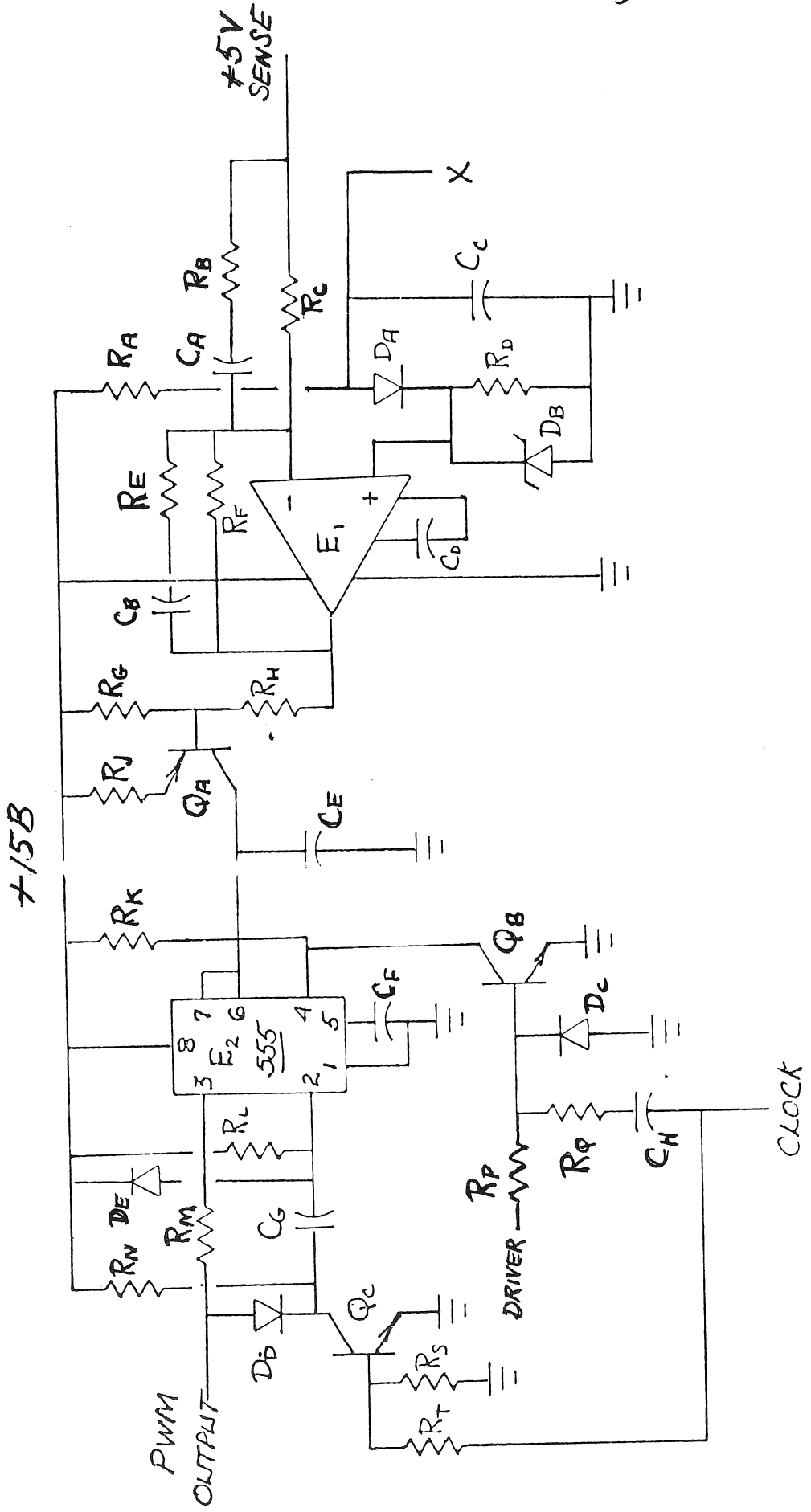
A (regulation) feedback path used in main +5 section of H777.

FIGURE 3-9

Feedback Path - Used in Main +5V Section of H777


+5V SENSE
X
+15B
R_A
C_A
R_B
R_C
C_C
D_A
R_D
D_B
R_E
R_F
E_1
C_D
C_B
R_G
R_H
R_J
Q_A
C_E
R_K
Q_B
C_F
E_2 555
D_C
R_L
R_P
R_Q
C_H
CLOCK
DRIVER
D_E
R_M
R_N
C_G
Q_C
D_D
R_S
R_T
PWM OUTPUT

3.4.6.2 Error Amplifier - The operational amplifier compares the sense voltage (+5) with the reference (5.1V + or -2%) voltage and amplifies the difference.

A portion of the amplifier output is fed back to the inverting input via R(F). The voltage divider action of R(F) and R(C) fixes the DC voltage gain of this amplifier circuit so that a given error voltage (Voutput - Vref) produces a known output level from the amplifier.

The voltage level (amplified error) at the op-amp output is converted to a Current level by Q(A), R(J), R(G), R(H) which operate as a variable current source.

Up to this point with the first three sections of the circuit operating, we can convert the difference between the supply output voltage and 5.1V to a known current level.

Vout - 5.1 = X ma. (Q(A) collector current)

NOTE

The function of C(B), R(E), C(A), R(B) (in the error amplifier circuit) is to modify the AC gain of the stage in a way that will assure stability of the system over a bandwidth that is wide enough to give the regulator adequate dynamic response.

3.4.6.3 Current Source - Capacitor C(E) is the main timing element of this regulator. The constant collector current from Q(A) causes C(E) to have a linear rate of rise of voltage (see Figure 3-10).

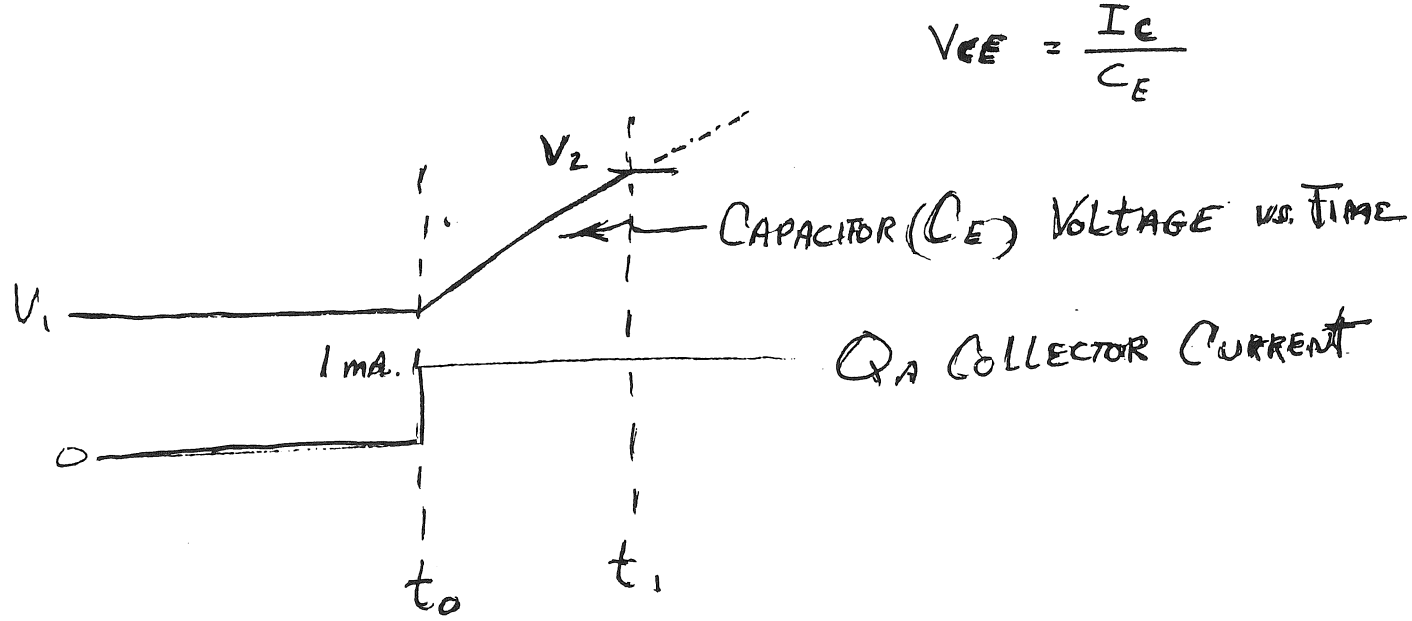


FIGURE 3-10

Capacitor (CE) Waveform

The Rate of Change of Capacitor Voltage is determined by the output current of the variable current source Q(A) (etc.).

3.4.6.4 Pulse Width Modulation - To understand the operation of the PWM Circuit (555), let us assume that at time zero (T(Ø)) the capacitor is at zero volts and the discharge transistor within E(2) (555) is ON. Pins 6 and 7 (threshold and discharge) are both tied to C(E) so the current from Q(A) is bypassed to ground and V(CE) stays at zero (see Figure 3-11).

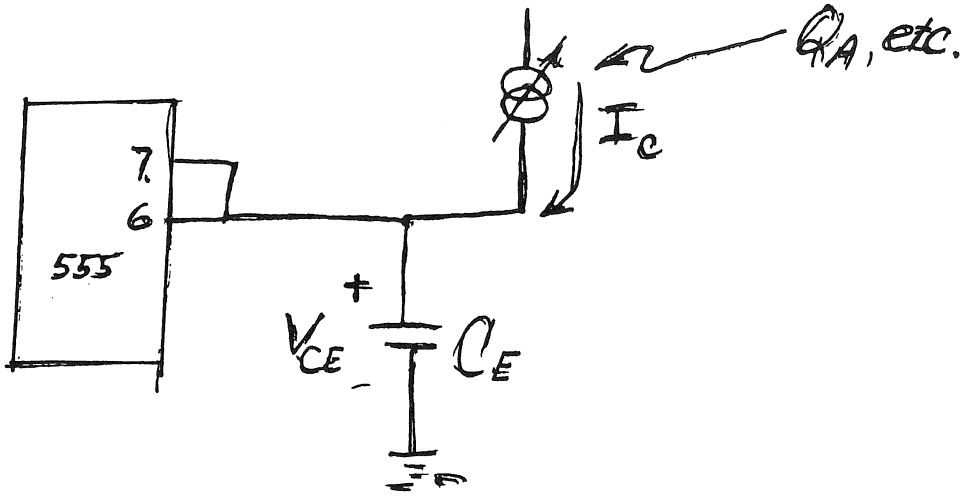


FIGURE 3-11

Q(A) Current Bypass

At this point (TØ) the clock signal goes high (+15V) and turns on Q(C). The collector voltage falls rapidly to about zero, causing Pin 2 of the 555 Timer to momentarily fall to zero, (Figure 3-12). This action triggers the timer and its output goes high. Pin 3 = +13.5V).

No output from the circuit is seen yet because Q(C) is turned ON and clamps the E2 output near zero volts through D(D). (This condition will exist for as long as the clock remains high.)

At the same time that pin 3 goes High, the internal discharge transistor turns "OFF", allowing the output current from Q(A) to begin charging C(E).

The voltage v(CE) rises at a fixed rate (for a constant output error signal) until it reaches the threshold point (approximately 1ØV) and resets the 555 Timer. This event occurs after the clock pulse has dropped back to zero turning off Q(C). Hence, an output pulse was produced by the circuit which started when the clock signal fell to zero and ended when V(CE) reached 1ØV.

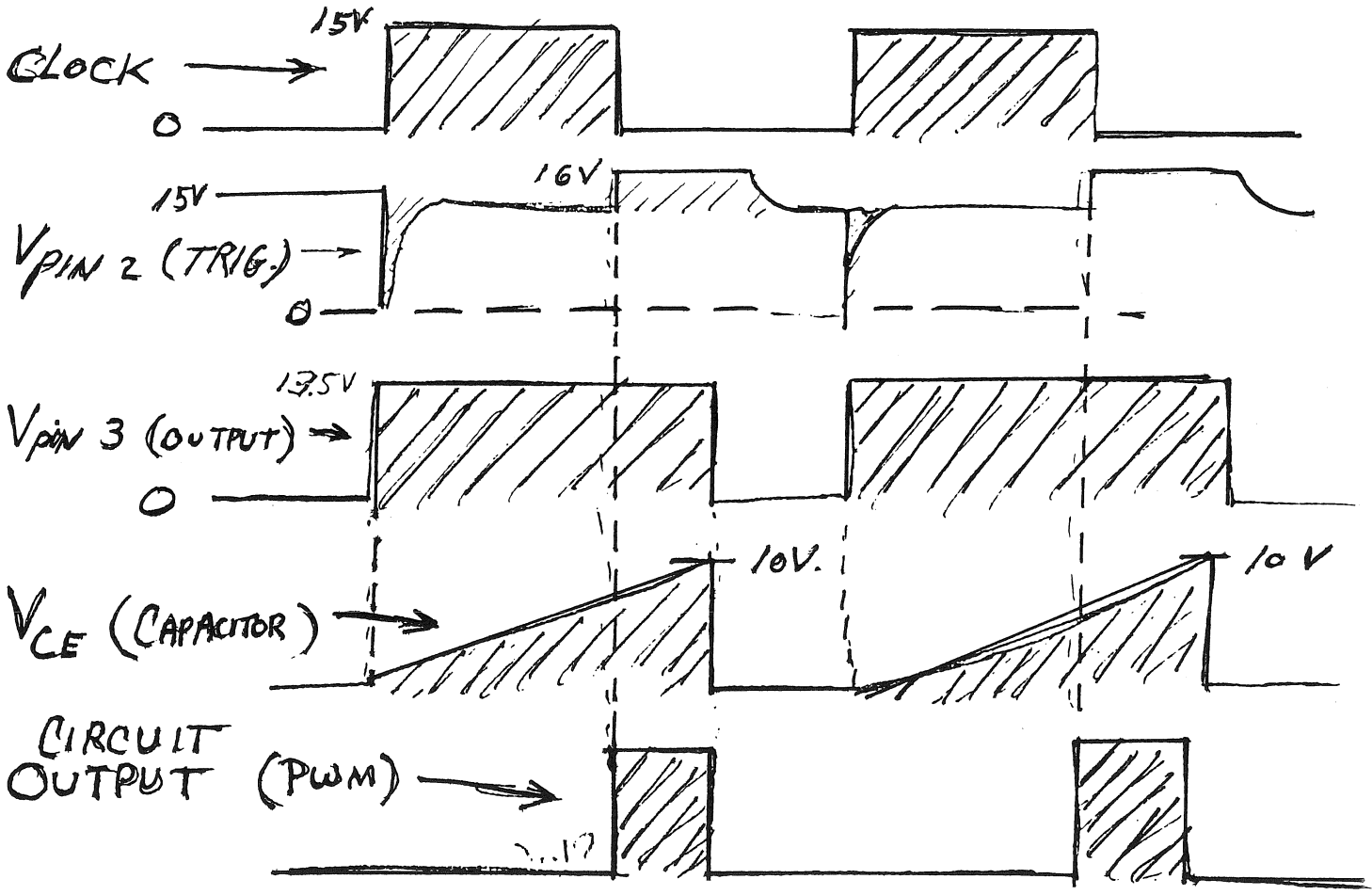


FIGURE 3-12

Summary of Timing Sequence

Observe that if the variable current source Q(A) outputs a higher current level (because the sense voltage became higher), V(CE) increases at a greater rate and therefore reaches Vthreshold (10V) sooner (see Figure 3-13). The clock pulse width is fixed (25 usec ON, 25 usec OFF) so the difference (equal to output pulse time) becomes less. The output pulse is narrower. This narrower pulse when applied to the power switch stage, will have a lower average value and will reduce the output voltage of the regulator (thus counteracting the original condition).

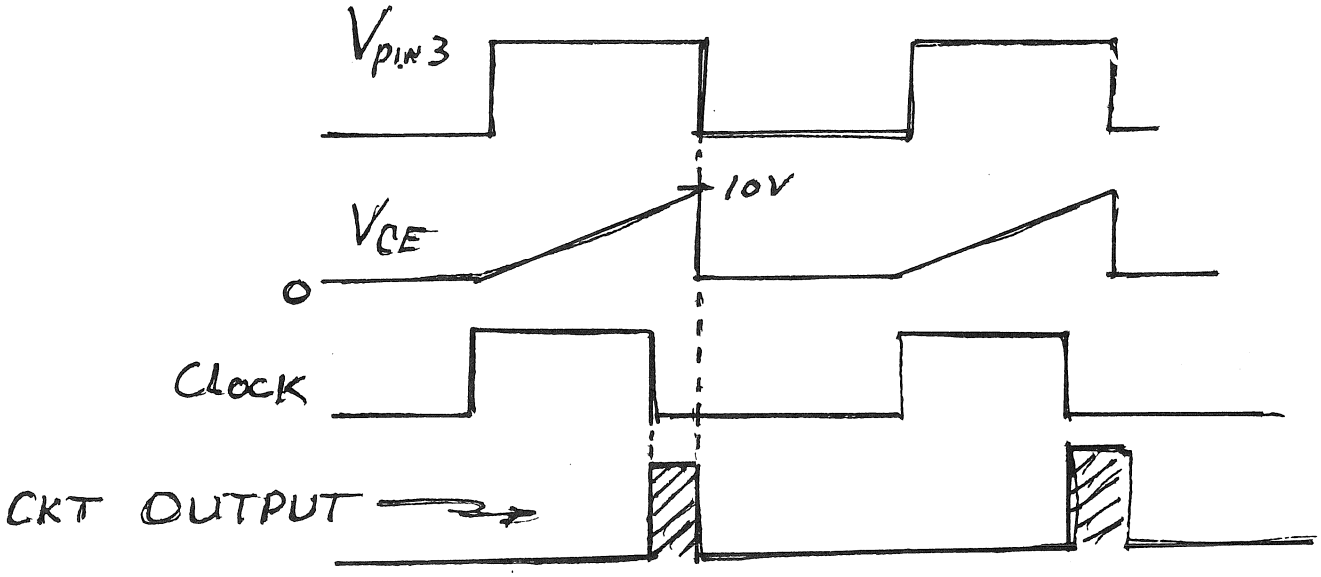


FIGURE 3-13

V(CE) Waveforms with Higher Current Level

If the output of Q(A) reaches a particular value such that the charge time of V(CE) is equal to or less than the high clock time (25 usec), no output pulse is produced. This establishes a minimum pulse width of zero (see Figure 3-14).

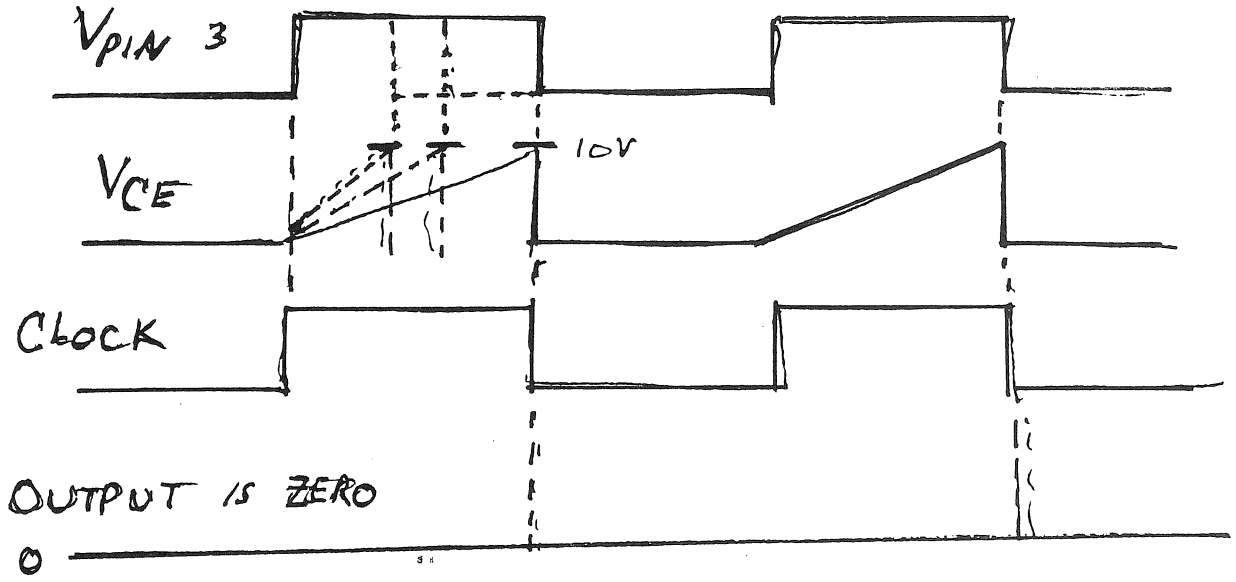


FIGURE 3-14

V(CE) Charge Time Vs. High Clock Time

An upper limit to the circuit output pulse width is established (at 25 usec) by reseting the timer (via Pin 4) at the beginning of each clock cycle. Thus, Q(B) momentarily turns ON at T(Ø) (clock goes high) to ensure that the output is Ø at the start of the timing interval.

Q(B) also performs the important function of allowing a signal from either the driver stage or the over-current detector give designation to truncate, or cut short, a pulse coming from the PWM stage (see paragraph 3.4.9.1). Application of a positive voltage to R(P) turns on Q(B) and immediately stops the pulse that is present at the output of 555 (and prevents further output as long as Q(B) is ON). Note that if an output pulse is truncated by a momentary application of reset voltage (to R(P)), the timer will wait until the next clock pulse to again produce an output. If each pulse is truncated as it is produced, an artificial (and variable) maximum has been set for the duty cycle of the regulator. This feature is the basis of the overload protection scheme, the H777.

3.4.7 Alternate Control Circuit for Regulating (Outputs other than +5, Main) (Refer to Figure 3-15)

The regulating loop circuit used in the MOS converter and +2Ø volt sections of the H777 is similar to the +5V regulator circuit except for the method of setting the charge time for the main timing

capacitor. In this scheme, the capacitor (C(B)) is fed from a constant voltage (instead of a constant current) source and charges along an exponential curve. (The main +5 capacitor charges linearly.) See Figure 3-16.

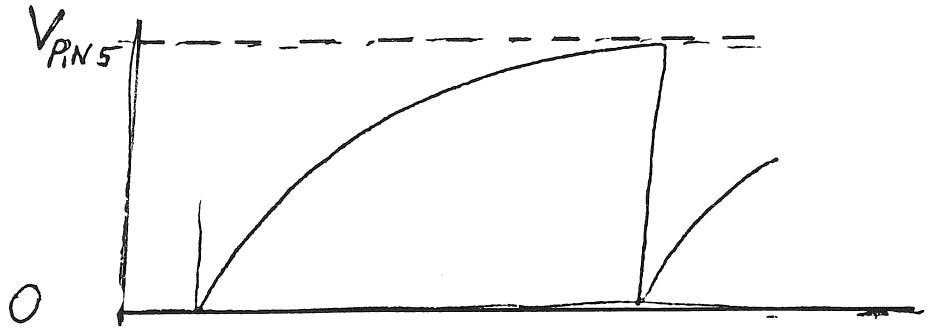


FIGURE 3-16

Main Timing Capacitor Charging Curve

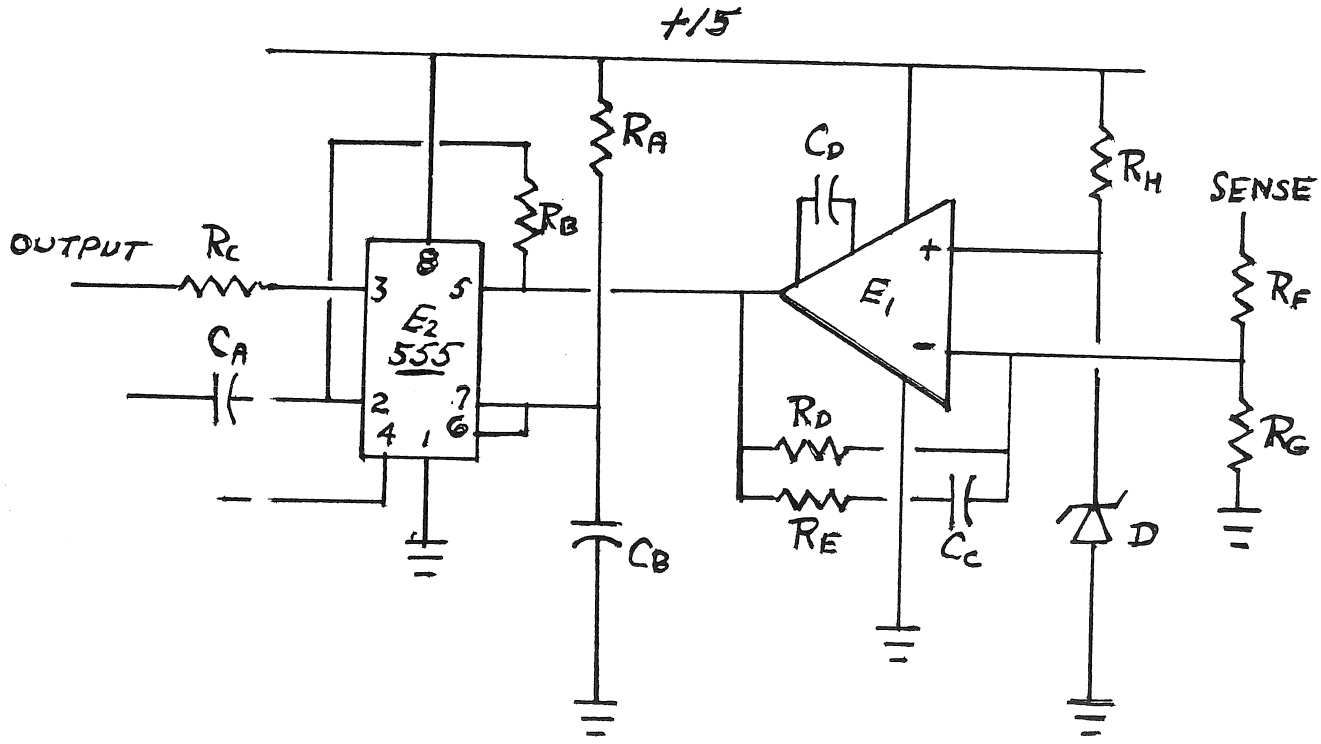


FIGURE 3-15

Alternate PWM Circuit (Used in Regulators Other Than Main +5V)

The trip point is now set directly by the output voltage of the error amplifier at pin 5 of the 555. By raising or lowering the threshold (Pin 5) the output pulse width can be widened or narrowed (see Figure 3-17). Note that trigger and reset control are the same as in Paragraph 3.4.6 on the main +5 regulator.

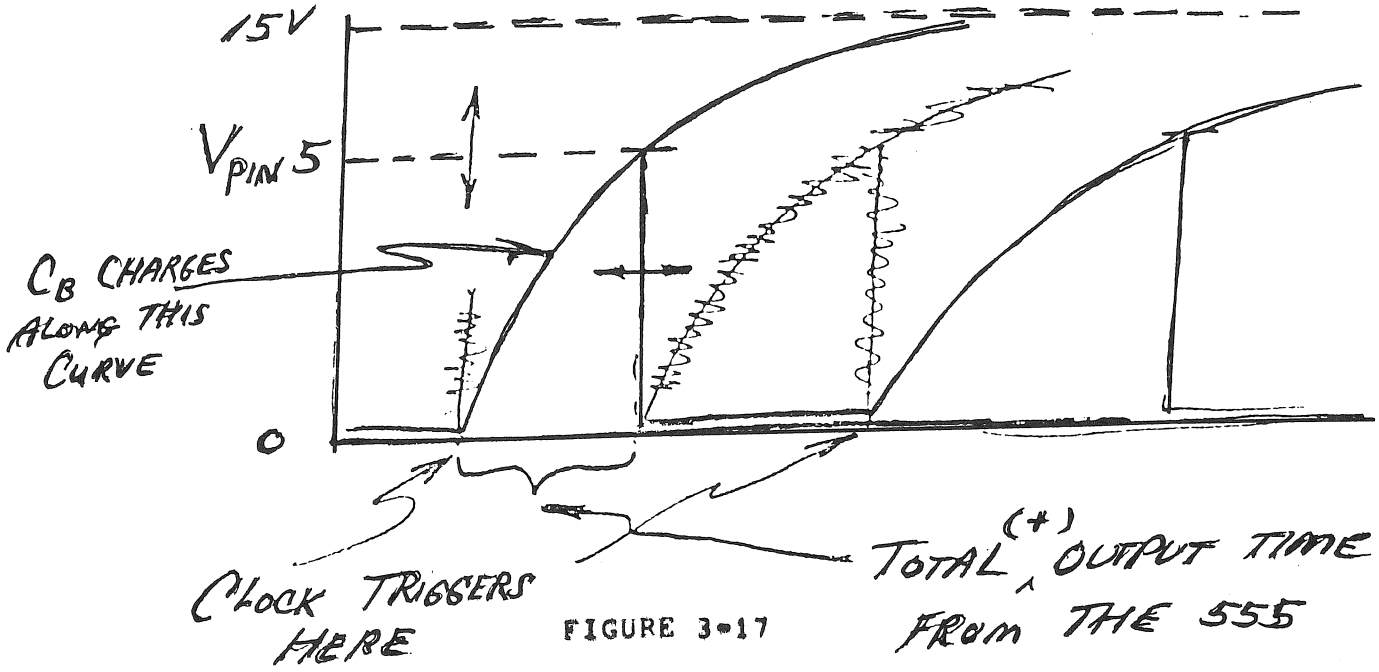


FIGURE 3-17

Effect of Varying Threshold

In the MOS Converter, the + or -15 volt loop uses the entire available pulse from the 555, so no clamp path is provided (diode to collector of trigger transistor Q(C)) on the circuit output (see Figure 3-9). The same applies to the +20 regulator PWM circuit.

The maximum pulse width is unlimited in the +20 regulator by omission of the R and C elements that couple the clock edge to the reset transistor. This is done to allow the regulator to reach a 100% duty cycle and thereby maintain its 20 volt output as the raw DC voltage approaches 20 volts.

Table 3-1 depicts the design limits for control PWM signals within each regulator of the H777.

TABLE 3-1
PWM Design Limits

Regulator	Pulse Width Min.	Pulse Width Max.	Trigger Clamp	Clocked Reset
Main +5	0	25 us	YES	YES
+ or -15 (MOS Conv)	3 us	50 us	NO	YES
+5 B(MOS Conv)	0	25 us	YES	YES
-5 (Option)	0	25 us	YES	YES
+20 (Option)	3 us	00	NO	NO

3.4.8 Base Drive Circuit (Main (+5) Regulator) (Refer to Figure 3-18)

The output current available from the 555 PWM circuits previously described (paragraph 3.4.7) is too small to directly drive the power switch stages of the various regulators in the H777. This section describes the circuitry used to match the PWM output generated by the main +5 loop to its power switch. (Paragraph 3.4.4 describes the function of this switch).

This regulator, because of its higher output current level, requires two "Pass elements", or power switches connected in parallel. Resistors R(A) and R(B) help force the two switches, Q(A) and Q(B), to share the load current. The two switches can be considered as one NPN device.

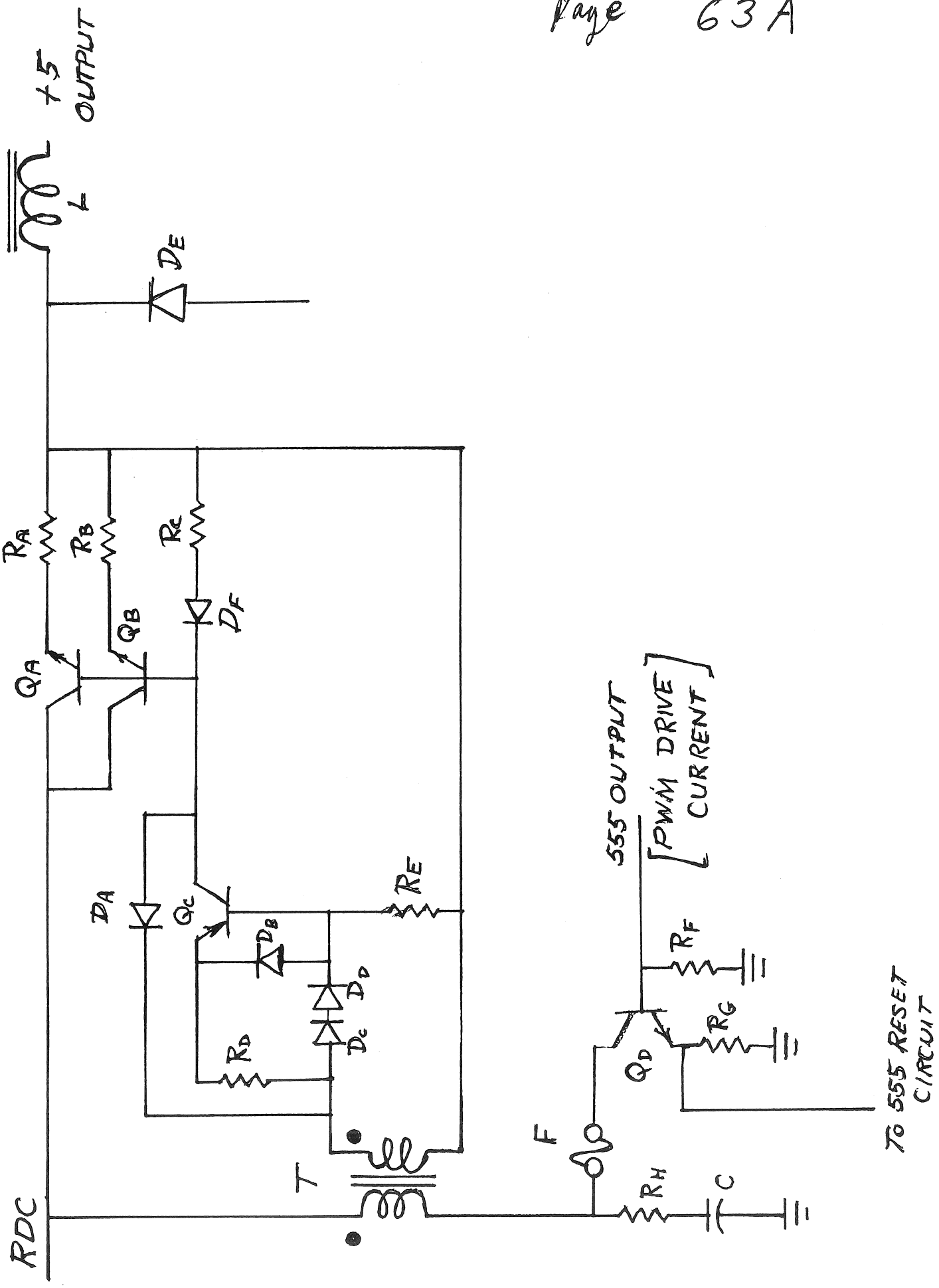
The PWM signal from the control "loop" circuit is received at the base of Q(D). This transistor, along with transformer T, amplifies the signal and couples it to the base of the power switch(s). A constant current circuit is inserted between the transformer secondary and the switch base. Q(C), R(D), D(C), and D(D) limit the base drive level to about 2.0 Amps. This level will remain fairly constant as the raw DC level varies.

See Page 63A

A high level base drive scheme for +5, 25A,DC series switching regulator

FIGURE 3-18

Base Drive Circuit for +5V Regulator


+5 OUTPUT
L
DE
RA
RB
RC
QB
DF
QA
DA
QC
RE
DB
DD
DC
RD
T
F
RH
C
RDC
555 OUTPUT
[PWM DRIVE CURRENT]
RF
RG
QD
TO 555 RESET CIRCUIT

An additional function provided by transformer T is to store energy during the drive pulse, to be used to reverse bias the switch transistor base-emitter junction when it is time to turn off. The energy stored in the core of T causes a current to flow counterclockwise (after Q(D) turns off) through R(C), D(F), D(A), and the transformer secondary. This draws current out of the switch transistor base and causes it to switch more rapidly.

The collector current vs. time in Q(D) will be a trapezoid (see Figure 3-19).

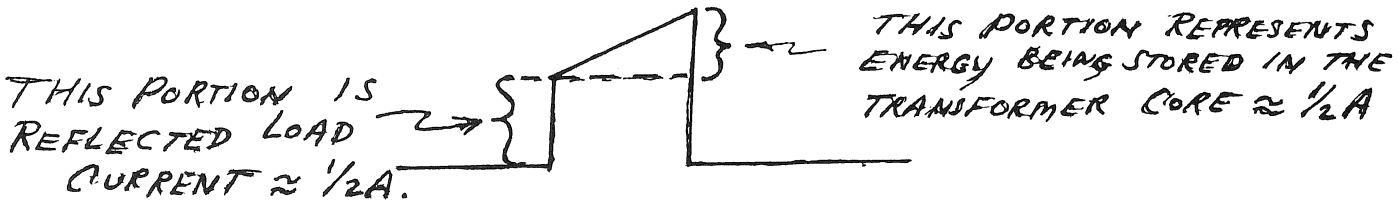


FIGURE 3-19

Q(D) Collector Current waveform

3.4.9 Protection Sequencing and Control Circuits

The following paragraphs describe the operation of protection, sequencing, and control circuits within the H717.

3.4.9.1 Current Limit Circuit - 54 - 11597 (Main +5 Regulator) (Refer to Figure 3-20). -- In Figure 3-20, elements L and C are the filter components in the 5V regulator output circuit (see paragraph 3.4.4). Current limiting in this regulator is achieved by inserting R(A) (.01) in series with L and monitoring the Peak Choke Current.

The current flowing through R(A) and the voltage across it have a triangular waveform (see Figure 3-21), rising while the pass stage is on and falling during conduction of the freewheeling diode. The triangle "rides" on the average DC output current level.

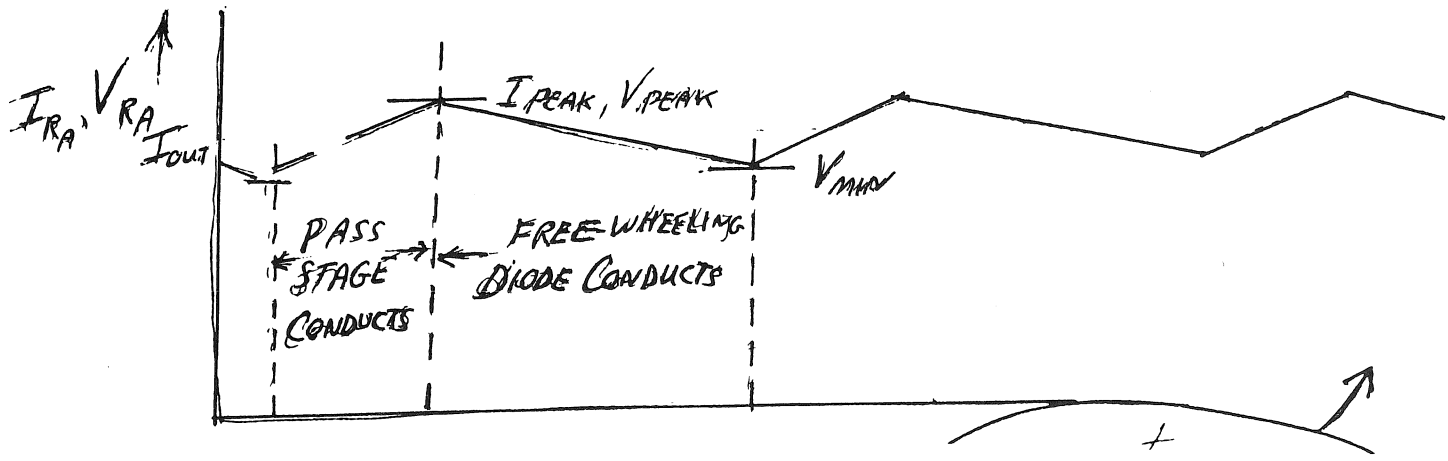


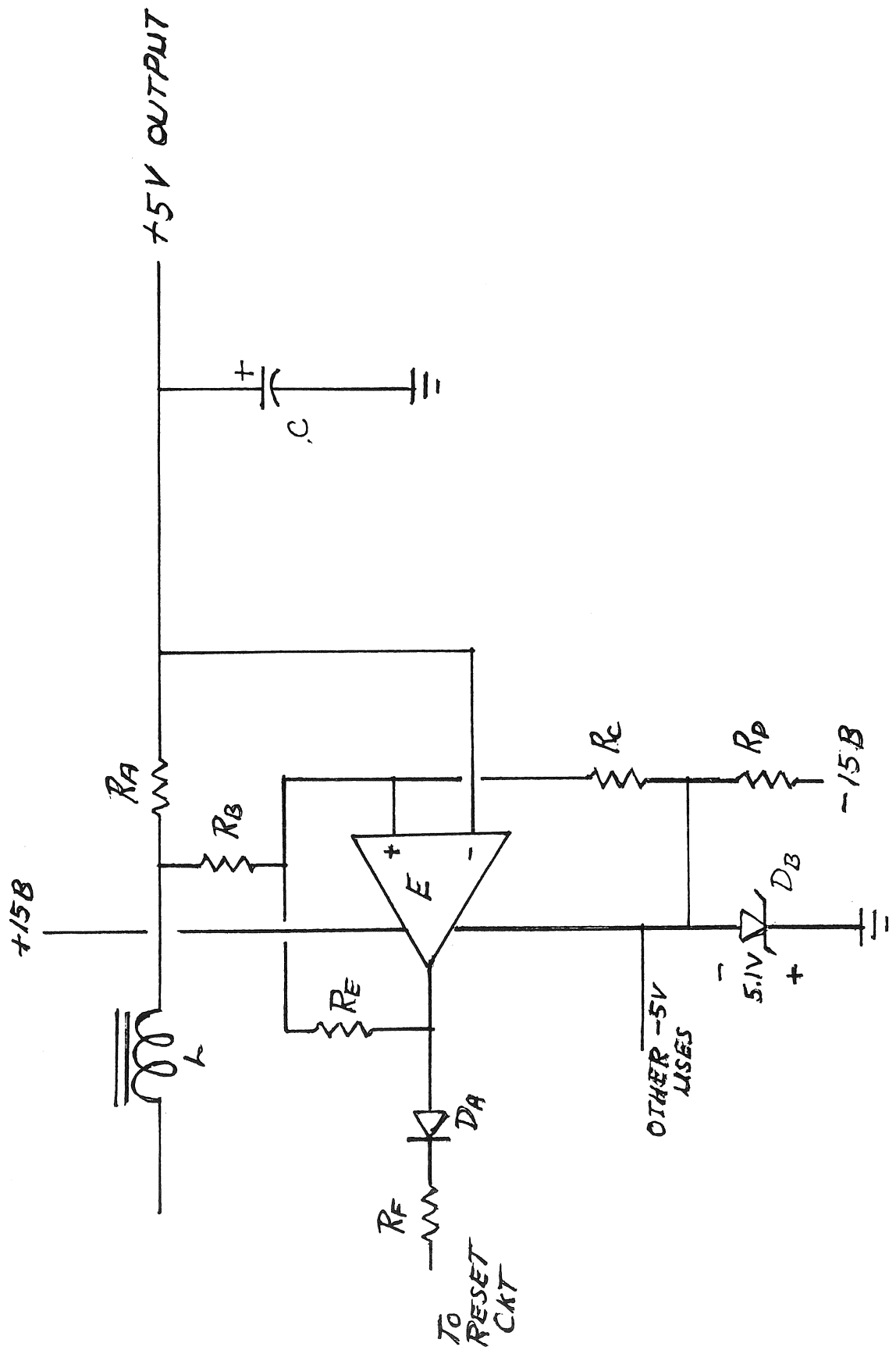
FIGURE 3-21

Current Through R(A)

See Page 66A

FIGURE 3-20

Foldback Current Limiting Circuit From Main 5V Regulator


+5V OUTPUT
C
+15B
RA
RB
RE
RF
DA
TO RESET CKT
L
E
RC
RD
-15B
DB
5.1V
OTHER -5V USES

(I)Out, the average regulator output current, can vary from near zero to about 25 Amps, but the triangular "choke component" of current remains the same. The peak and minimum current points are equidistant above and below the average value.

The operational amplifier in Figure 3-20 (E) serves as a threshold detector to reset the 555 Timer (in the regulator loop), when chock current exceeds a preset value. The trip point value is preset by drawing current through R(B) and R(C) (down to -5V) and thereby setting the non-inverting (+) input negative with respect to the inverting (-) input. In this condition the op-amp output will be fully negative (-4v). Output current flow, through R(A), balances out the preset negative bias on the op-amp and, when the voltage across R(A) begins to exceed the preset voltage across R(B), the operational amplifier will amplify the difference. Only a few millivolts positive differential is sufficient to saturate the op-amp output near +15 volts. The presence of positive voltage on the op-amp output resets the 555 and stops conduction of the pass stage until the next clock cycle begins.

Figure 3-22 is a series of waveform sketches that show the result of increasing load current beyond the trip level of the current limiting circuit.

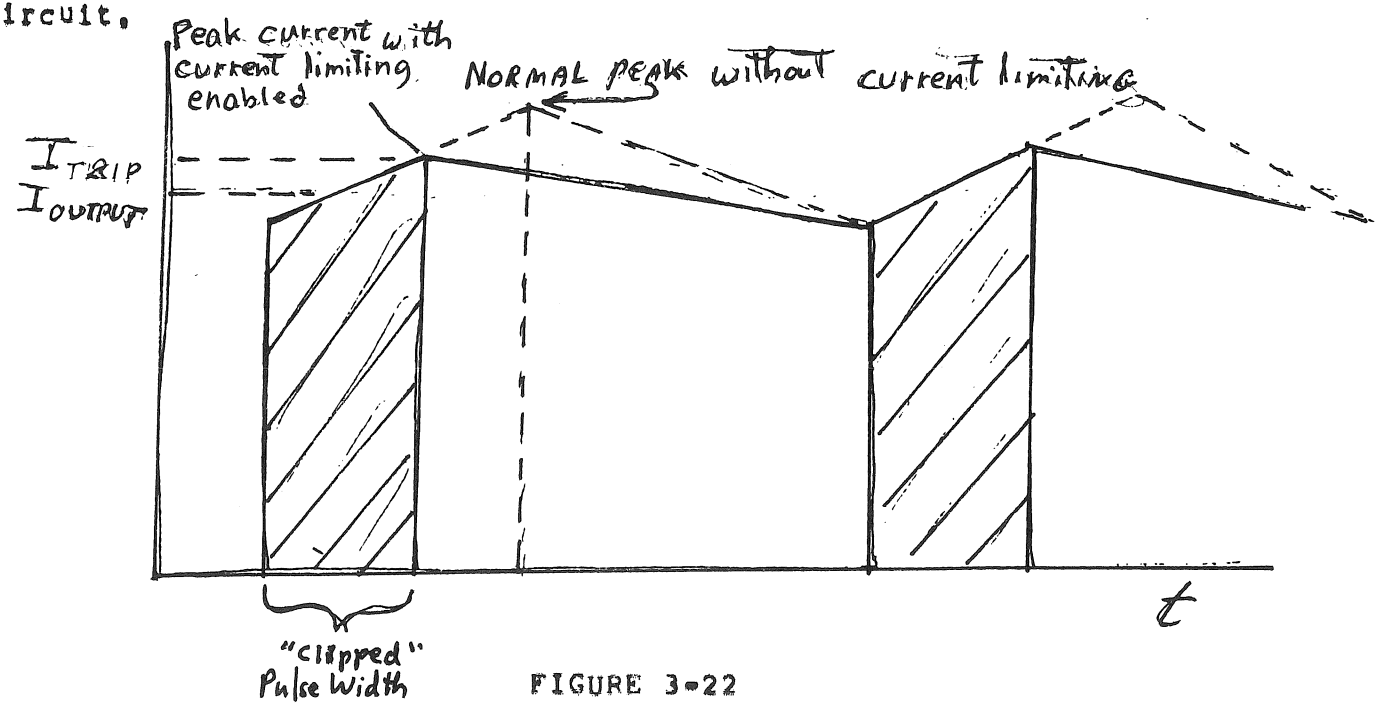


FIGURE 3-22

Increasing Load Current Beyond Trip Level

Note that as (I)Output continues to rise toward (I)Trip, the pulse width (pass stage ON time) will become narrower. (Because the choke current component is always triangular, its average value is 1/2 of its peak, so (I)Output is halfway between peak and valley).

The effect of narrowing the pass stage ON time is to reduce the duty cycle of the waveform applied to the LC filter, thereby lowering the output voltage of the power supply.

A foldback feature is built into this overload protection circuit. It operates because the preset bias, which sets the op amp trip point, is determined by the output voltage so that a curve of output voltage vs. current will foldback: (see Figure 3-23).

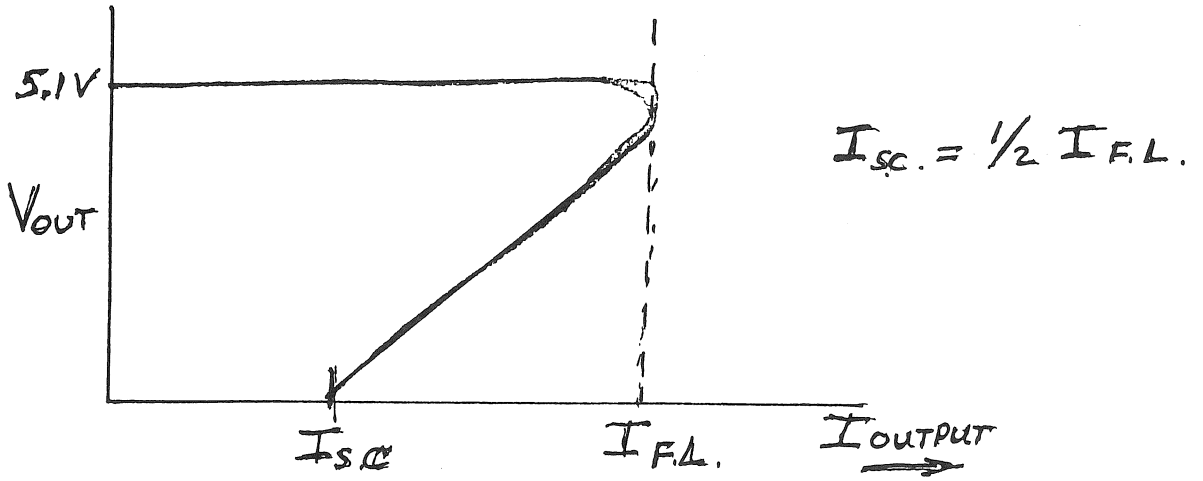


FIGURE 3-23

Output Voltage/Current Foldback

3.4.9.2 Current Limit Circuit - +5B Regulator

NOTE

Regulators other than main +5V are similar. (Refer to Figure 3-24)

In the +5B Regulator (MOS Converter) and in other H777 regulators, the composite load + choke current waveform is monitored by a series resistor in the collector circuit of the power switch stage. Here the detector element is the base-emitter junction of a PNP signal transistor, Q(A).

Collector current in Q(C) has the same form as that described in the previous section (see Figure 3-25).

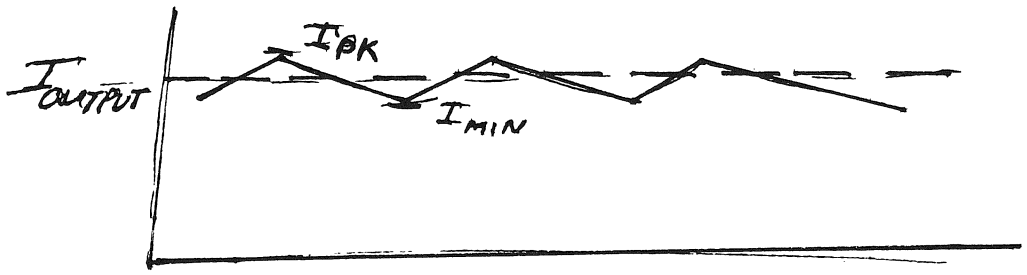


FIGURE 3-25

Q(C) Collector Current Waveform

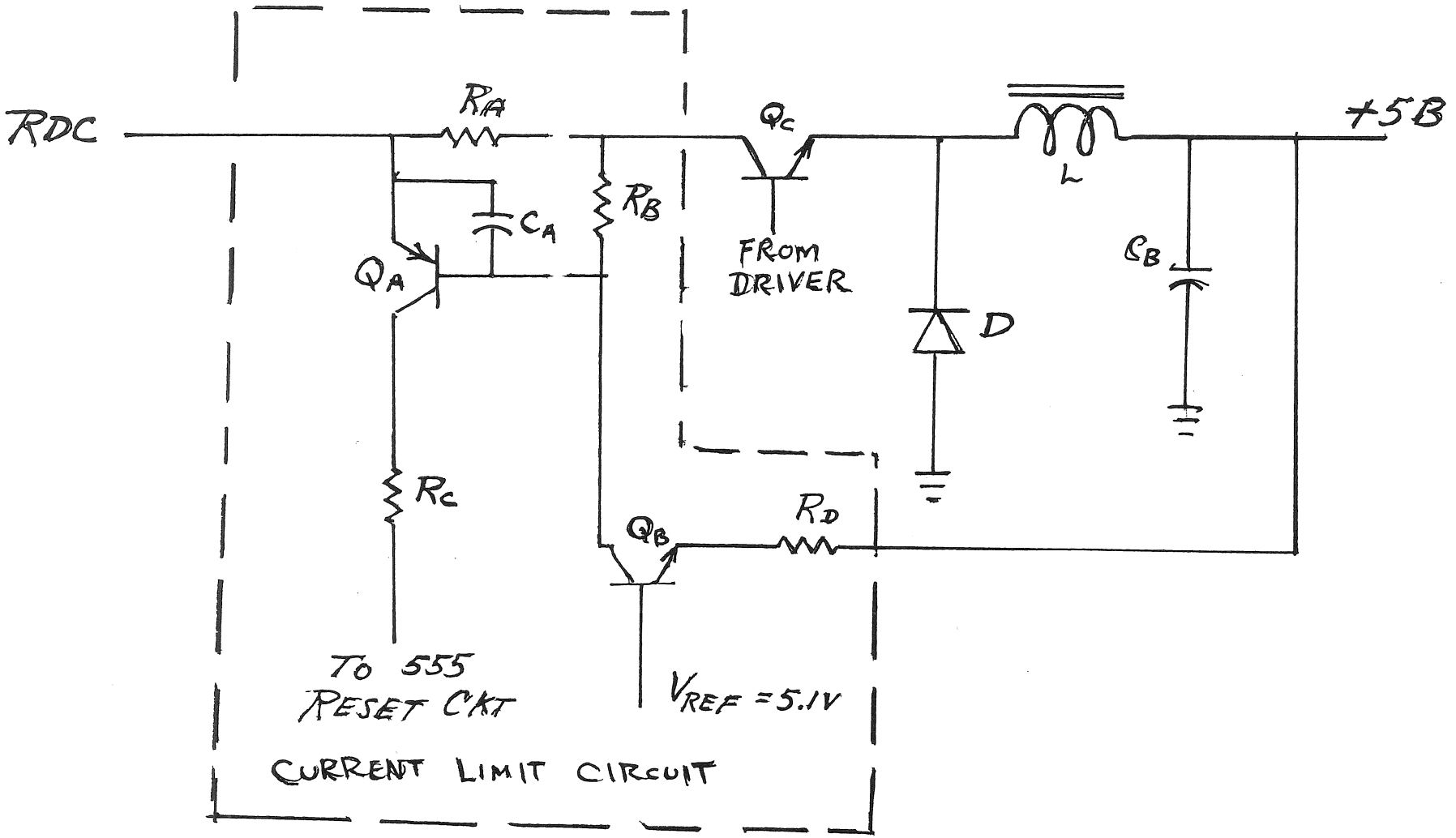
When the (I)PK value produces a voltage across R(A) that is sufficient to overcome the V(BE) of Q(A) (approximately Ø.6V), the base begins to draw current and collector current will flow through R(C) to reset the timer in the regulator loop. The net result is the same as that previously described.

See Page 70A

FIGURE 3-24

Current Limit Circuit for +5B Regulator

A FOLDBACK CURRENT LIMIT SCHEME USED ON +5B - MOS CONVERTER



C(A) provides noise suppression and eliminates premature reset due to the reverse recovery current flowing into the free wheeling diode (D).

Q(B) and R(D) are used to create a preset bias current through R(B) whose value increases as V(OUT) is pulled down below the reference (V(REF)) by an overload. This preset bias produces a foldback characteristic as described previously.

3.4.9.3 Crobar (Crowbar) Circuits Overvoltage Protection On +5, +5B and +20 Volt Regulators (Refer to Figure 3-26) - Because each of the above (+) output regulators will introduce a high voltage (Raw DC) at its load terminals in the event of a failure that prevents the pass element (power switch) from opening, crowbar circuits have been included to protect the load. The action of a crowbar circuit is to rapidly apply a very low impedence across the regulator output terminals in the event of an excessive voltage appearing there.

NOTE

A Crowbar Circuit is for overvoltage protection for the load. It has nothing to do with overload or short circuit protection for the regulator.

The actual crowbar element is a silicon-controlled rectifier (SCR D(A)) that conducts heavily from anode to cathode, once triggered by a momentary current from gate to cathode.

The trigger current is provided by another four-layer device (SCR D(B)). This smaller device improves the accuracy of the Crowbar circuit trigger voltage and assures an adequate drive pulse for rapid turn-on of D(A). R(C) and C are for improved noise immunity.

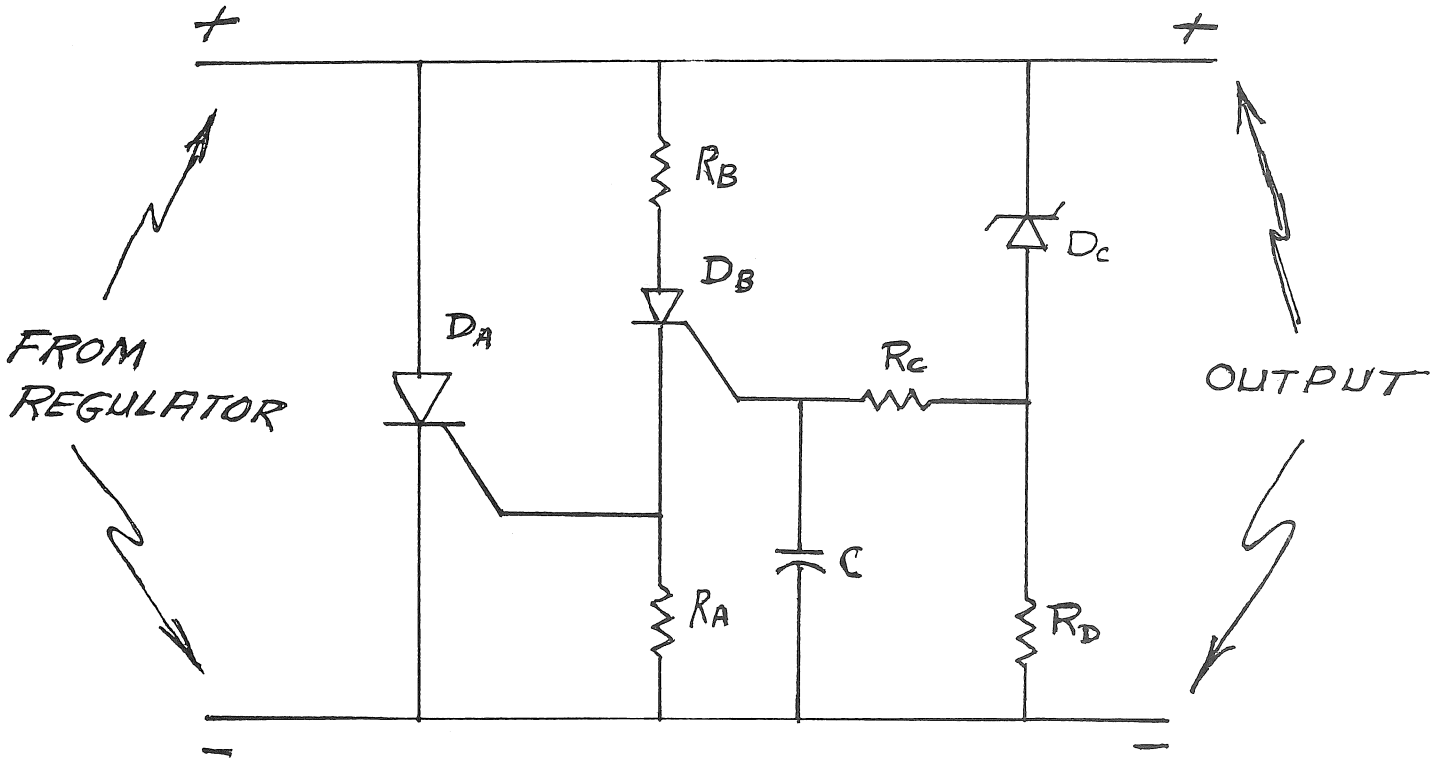
The actual trigger level for the circuit is set by D(C) which begins to conduct once its zener voltage level has been exceeded. Conduction of D(C) produces a voltage across R(D) equal to the output value less the zener value.

$$V(RD) = V(OUT) - V(Z)$$

When this voltage (V(RD)) reaches approximately 0.6V, current will begin to flow into the gate of D(B) via R(C). This current causes D(Z) to switch ON, creating gate current into D(A), which also switches ON -- effectively short-circuiting the regulator output terminals.

D(A) will remain in conduction until its anode current falls below a certain level (called "holding current", 100 ma) for a period of time (called "turn-off" time, 50 usec) after which it again appears as an open circuit.

Note that if a pass transistor has failed by shorting collector to emitter, the Crowbar will remain in conduction indefinitely, sinking large current from the raw DC source.



Similar crowbar circuits are used on:

- +5 main output
- +5B
- +20 core reg.

FIGURE 3-26

Typical Crowbar Circuit

To protect D(A) from this condition, each Crowbarred regulator has a fast blow fuse in series with the RDC source.

NOTE

No internal protection is provided for the Crowbar devices if an external source of power is connected across the output terminals of the H777.

3.4.9.4 Power Fail Detectors (Refer to Figure 3-27) - The H777 provides Unibus-compatible power failure signals (AC LO, DC LO), which are used to alert the processor and memory during power-up and power-down sequences.

The line drivers in H777 are of the open collector type and present a low impedance to ground when asserted. The signals are asserted when the AC Power input is below preset voltage levels:

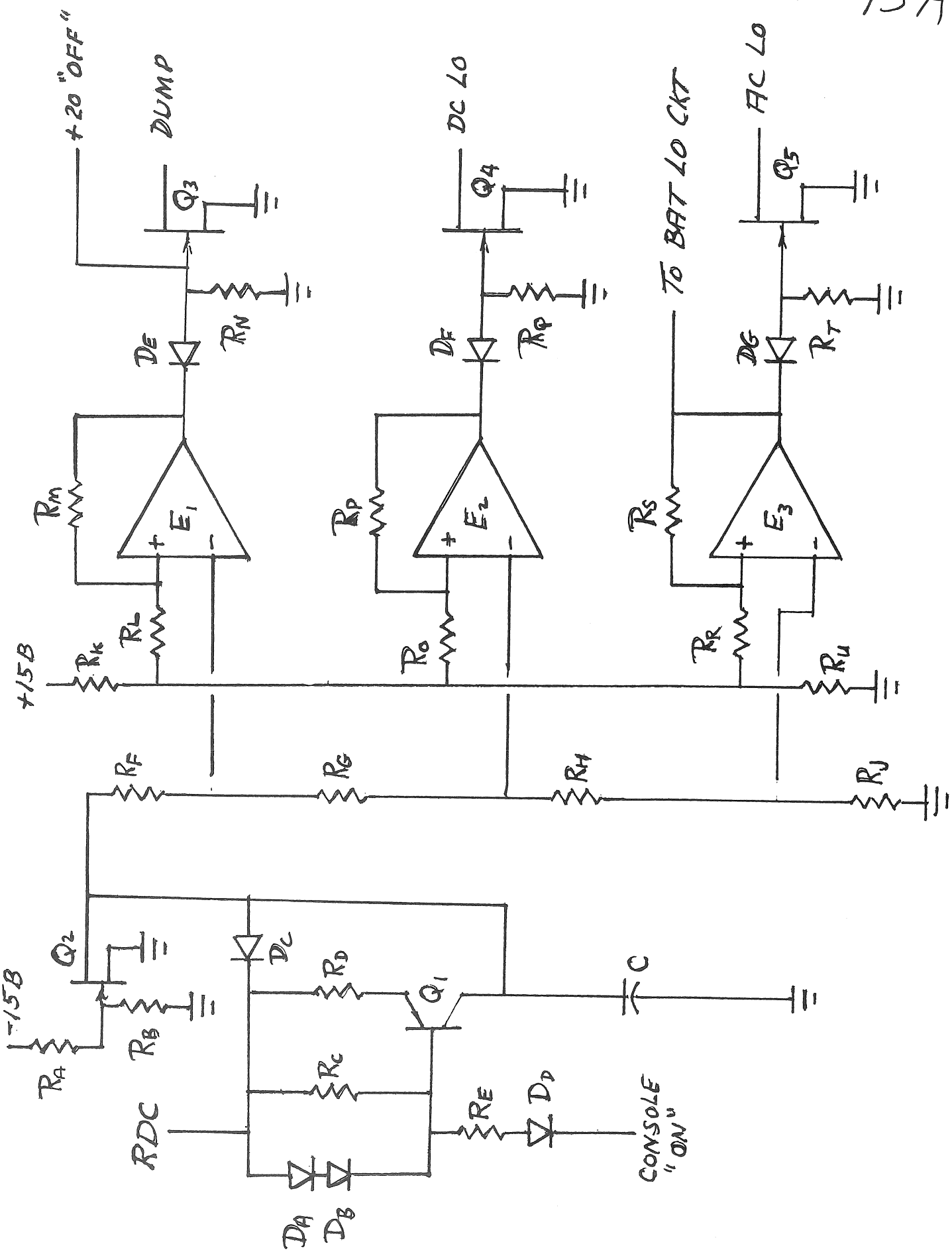
90 V(rms) for AC Lo
80 V(rms) for DC Lo

The line drivers Q(4) and Q(5) are N channel field effect transistors that display a very low ON resistance between drain and source (line to ground) as long as the gate to source bias voltage is near zero. When this bias is made negative, the devices will Open, presenting an essentially infinite impedance to ground on the AC LO and DC LO lines.

See Page 75A

FIGURE 3-27

Power Fail and Sequencer Circuitry


+20 "OFF"
DUMP
DC LO
TO BAT LO CKT
AC LO
Q3
Q4
Q5
DE
DF
DG
RN
RP
RT
E1
E2
E3
Rm
Rp
Rs
RL
Ro
RR
Rk
RU
+15B
RF
RG
RH
RJ
Q2
DC
RD
Q1
C
-15B
RA
RB
RC
RE
DD
RDC
DA
DB
CONSOLE "ON"

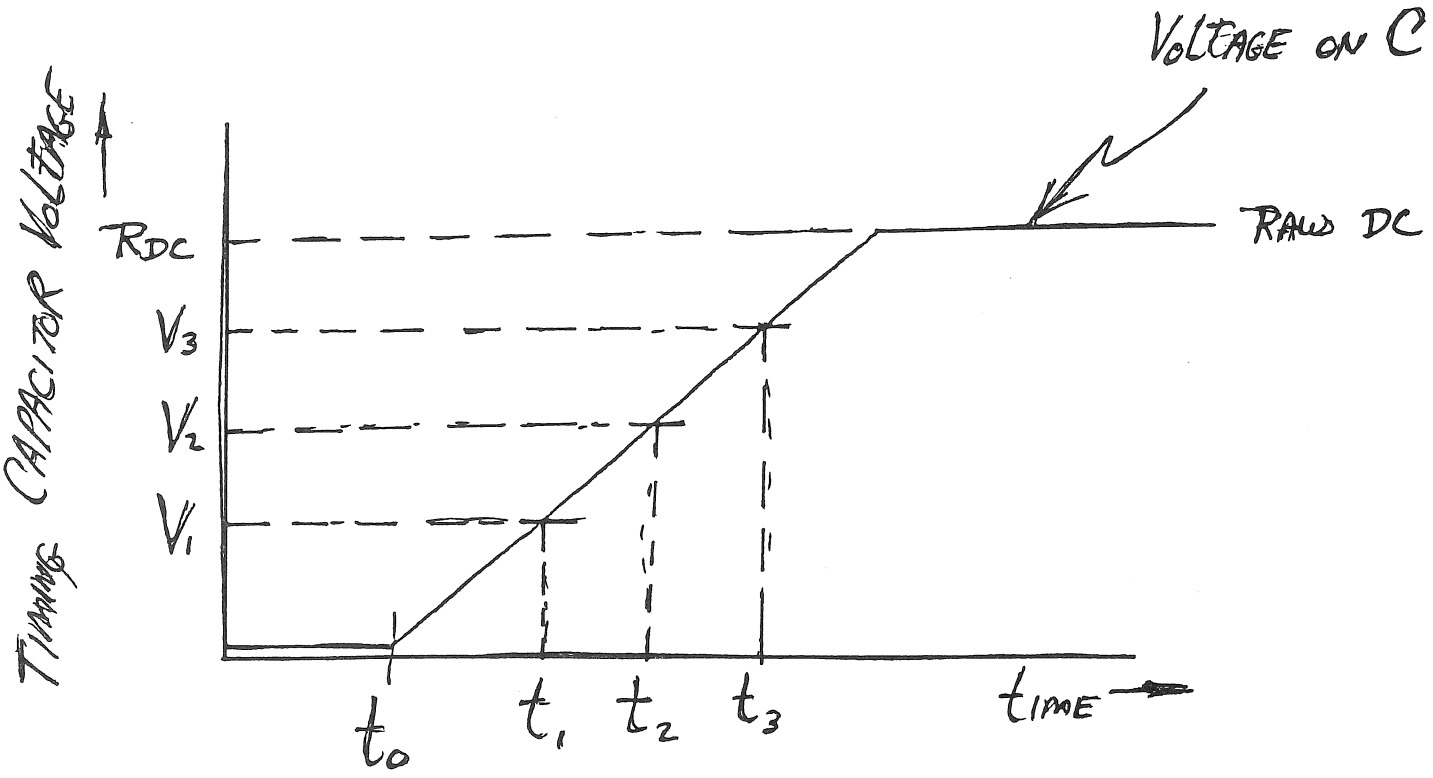
The Field effect transistor (FET) line drivers are controlled by threshold detectors E(2) and E(3) whose output swings from +15V to -15V depending on the relative polarity of the input. The detectors employ positive feedback (via R(P) and R(S)) to ensure that they are bistable, and not linear, in operation. Diodes D(F) and D(G) allow only the negative detector output to appear on the FET GATE (Bias voltage is zero or -15V.)

Note that a third stage is also present, E(1) and Q(3). This circuit turns the non-MOS regulators ON and OFF in sequence with the power fail signals, so that a normal power-down and/or power-up sequence can be performed when the power supply is switched to standby operation.

All three detectors have a common reference voltage (approximately 5V) determined by dividing +15V by 3 via R(K) and R(U). This reference is applied to the (+) or non-inverting inputs of the op-amp detectors.

The sensed voltages appear at the inverting inputs as fractions of the voltage across capacitor C. The various detectors switch from a high output (AC Lo, DC Lo unasserted) when the respective fractional voltage reaches 5 volts (vice versa, as capacitor voltage decreases).

The timing capacitor "C" is charged linearly by a switched current source (Q(1), R(D), R(C), etc.). Figure 3-28 is a diagram of the sequence.



Console switch turns "ON" current source @ t.

. @t(1) Cap Voltage = V(1); +5, +20, -5v regulators enabled
. @t(2) Cap Voltage = V(2); DC Lo unasserted
. @t(3) Cap Voltage = V(3); AC Lo unasserted

$$V(1) = \frac{5(RG+RH+RJ+RF)}{R} \qquad V(1)=\frac{5(R(G)+R(H)+R(J)+R(F)}{R(G)+R(H)+R(J)}$$

$$V(2) = \frac{5(R(G)+R(H)+R(J)+R(F))}{RH+RJ}$$

$$V(3) = \frac{5(R(G)+R(H)+R(J)+R(F))}{R(J)}$$

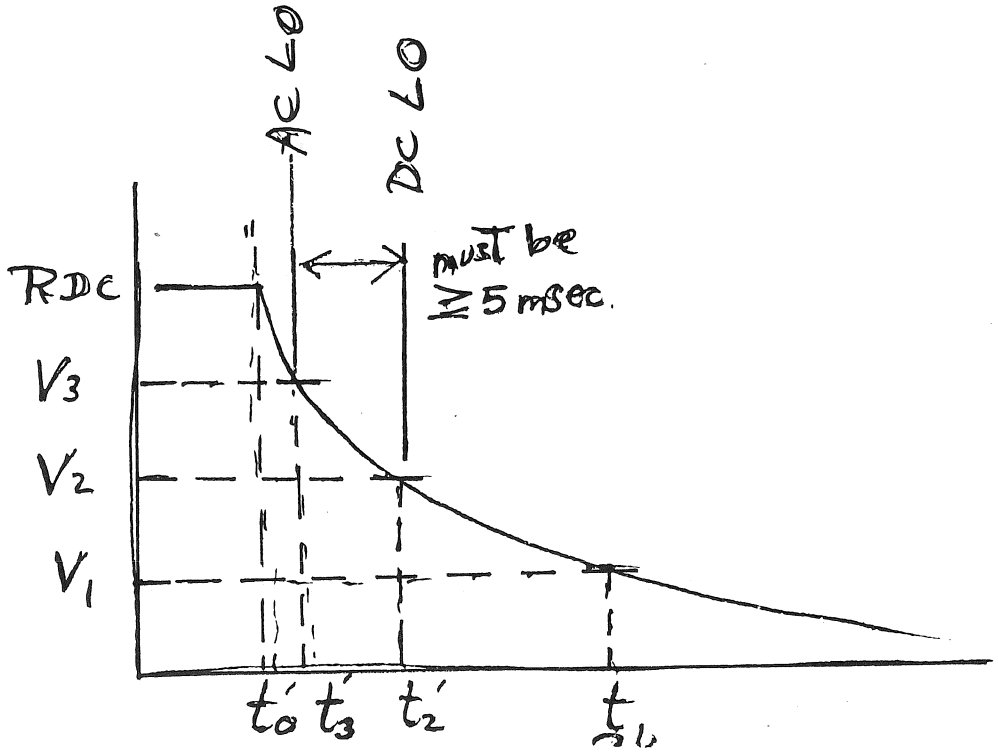
FIGURE 3-28

Power Fail Detector waveforms

During a power down sequence, the timing capacitor voltage decays along an exponential curve determined by either the RC product of C(R(F) + R(G) + R(H) + R(J)) or by the decreasing value of raw DC voltage drawing current from C through diode D(C), Either way, the sequence of events is reversed from the power-up order.

(AC Lo asserted; DC Lo asserted; +5, +20, -5 regulators disabled.)

During power down, the relative timing is of less importance as long as 5 ms between AC Lo and DC Lo is maintained. (See Figure 3-29).



V(3), V(2), and V(1) are the same as above.

FIGURE 3-29

Power Down Sequence

3.4.9.5 Battery Monitor Circuits (Refer to Figure 3-30) - The battery monitor circuit (located on the 5411597 regulator module) is employed to monitor the status of the H775 Battery Backup Unit when employed in a system. The H775 Battery Backup Unit is described in paragraph 3.5.

The battery monitor circuit contains a light-emitting diode (LED) which monitors the battery backup status as follows:

Condition	Status of Battery
Lamp Off	No H775 is present or battery is discharged (DEAD)
Lamp Flashing Slowly (1/2 HZ)	H775 is connected and battery is being charged - Capacity <90% of Max.
Lamp On	H775 is connected and battery is being trickle-charged - Capacity = or >90% of Max.
Lamp Flashing Rapidly (5 HZ)	H775 is connected and battery is being used (DISCHARGE)

The monitor circuitry is in three sections:

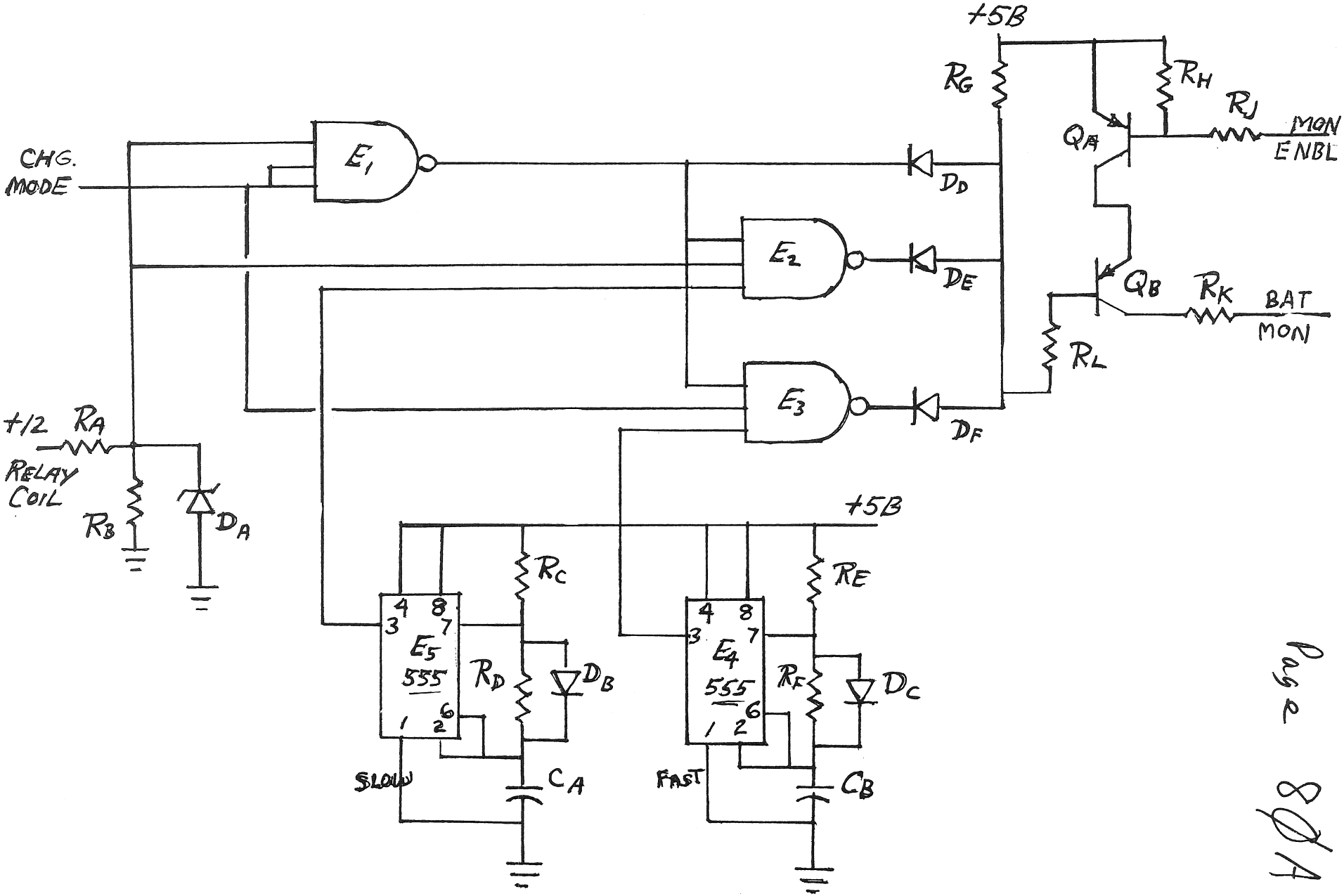
- Triple Nand Gate - Status decisions (E(1), E(2), E(3))
- Discrete LED Driver/Enable Circuit (Q(A), Q(B))
- Flashers - Relaxation oscillators (E(5), E(4))

The Nand gates operate on two system status lines (CHG) relay coil and turn on the LED Driver stage accordingly.

See Page 80A

FIGURE 3-30

Battery Monitor Circuits


+5B
RG
RH
RJ
MON ENBL
QA
CHG. MODE
E1
DD
E2
DE
QB
RK
BAT MON
RL
E3
DF
+12
RA
RELAY COIL
RB
DA
+5B
RC
RE
4
8
3
7
E5
555
1
2
6
RD
DB
SLOW
CA
E4
555
RF
DC
FAST
CB

If the output of E1, E2, or E3 is low, Q(B) is turned on, causing current to flow continuously through Q(A), Q(B), R(K) and the console LED (provided the "Mon Enable" line is grounded by plugging in the H775). Note that E(2) and E(3) can turn on the LED Driver also when all of their inputs are enabled. This condition exists only when the respective flashers (Oscillators E(4) or E(5) - see Section on Clock and 555 Timer for operation) have a high output.

The CHG MODE input line is controlled by the H775 according to the following table:

CHG MODE	H775 STATUS
Low	High charge rate
High	Trickle charge rate (AC Lo unasserted)
High	Discharging (AC Lo asserted)

The second status input is derived from the inrush relay coil voltage (clipped by D(A)), and merely indicates that the H777 is turned ON, or in standby operation.

Basic operation is best described by a status (or truth) table:

Charge Mode	Relay	State of LED
0	0(off)	OFF
0	1(on)	SLOW
1	0(off)	FAST
1	1(on)	ON

3.4.9.6 Electronic Switching of Non-MOS Loads (Refer to Figure 3-31) - The MOS Converter module, 54-11601, contains a pair of solid-state switches, Q(A) and Q(D), that connect + or -15V rails to all non-MOS Loads in the BA11-L. This is done to improve the useful battery back-up time by disconnecting non-critical + or -15 volt loads when the main +5 regulator is disabled (either by control switch or by loss of utility power). Another feature is that, in standby operation, MOS memory can be maintained while maintenance is performed on other sections of the machine.

The actual switch circuits are +15V and -15V. The +15V switch (Q(A), Q(B)) is simply a pair of complementary common-emitter amplifiers driven from main +5. Q(A) saturates, or is cut off, by the presence or absence of +5. The -15V switch is similar but uses a common base stage as a driver (Q(C).

3.4.9.7 Battery Lo Detector (Refer to Figure 3-32) - This circuit

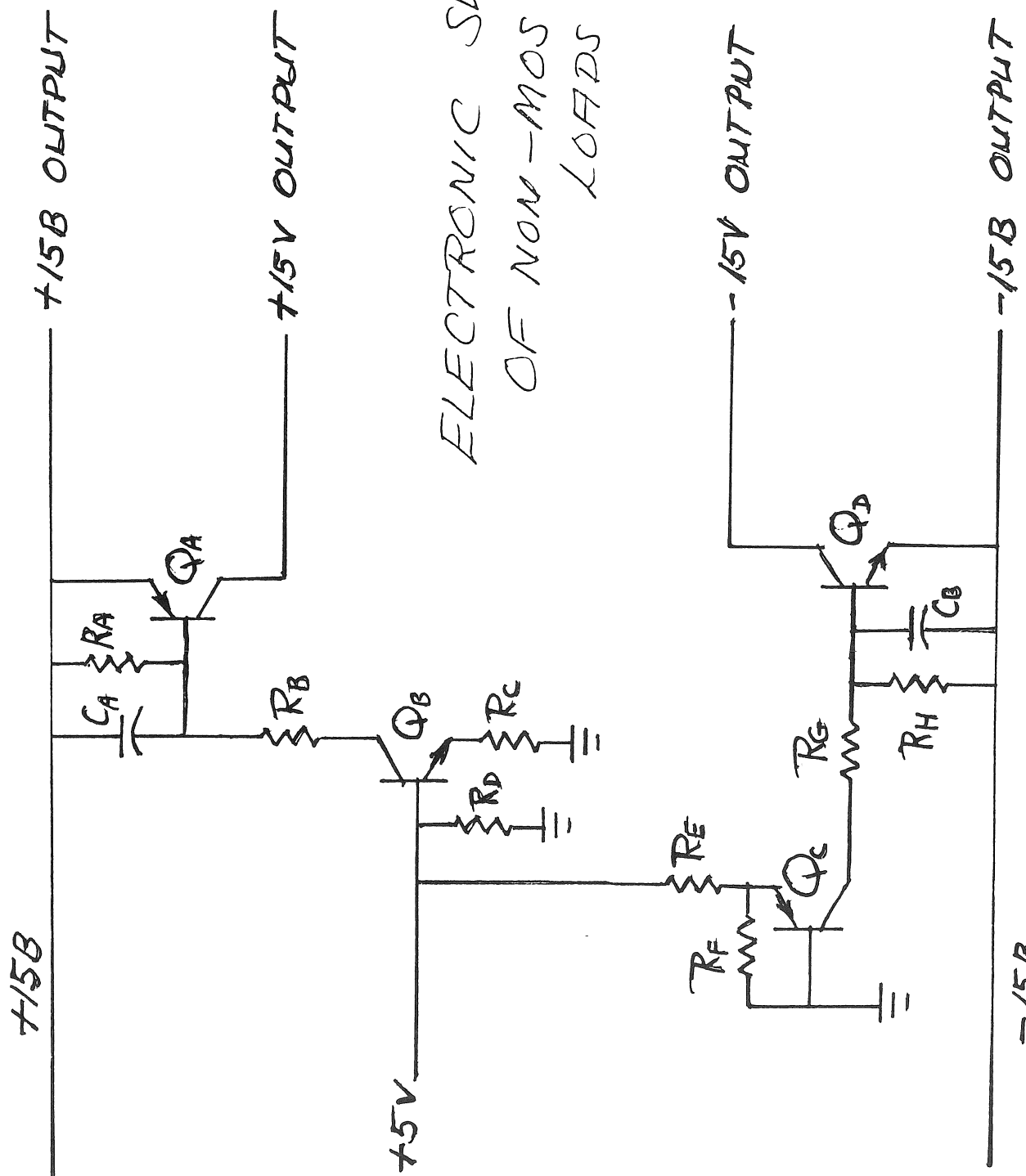
performs a memory function in that it latches "Bat Lo" asserted if + or -15V drops out during battery backup operation. Q(C) remains ON once asserted, until AC Lo is unasserted during a subsequent power-up sequence. The result is that the M9301 is signalled (via the combination of AC Lo and Bat Lo) that the MOS memory has or has not lost its contacts due to a voltage loss. The output that the M9301 creates, by interpreting AC Lo and Bat Lo, signals the processor to reboot on power-up or to resume operation, since memory is intact. This feature can be disabled by removal of the jumper cable between the console board and the M9301.

See Page 83A

FIGURE 3-31

Electronic Switching of Non MOS Loads

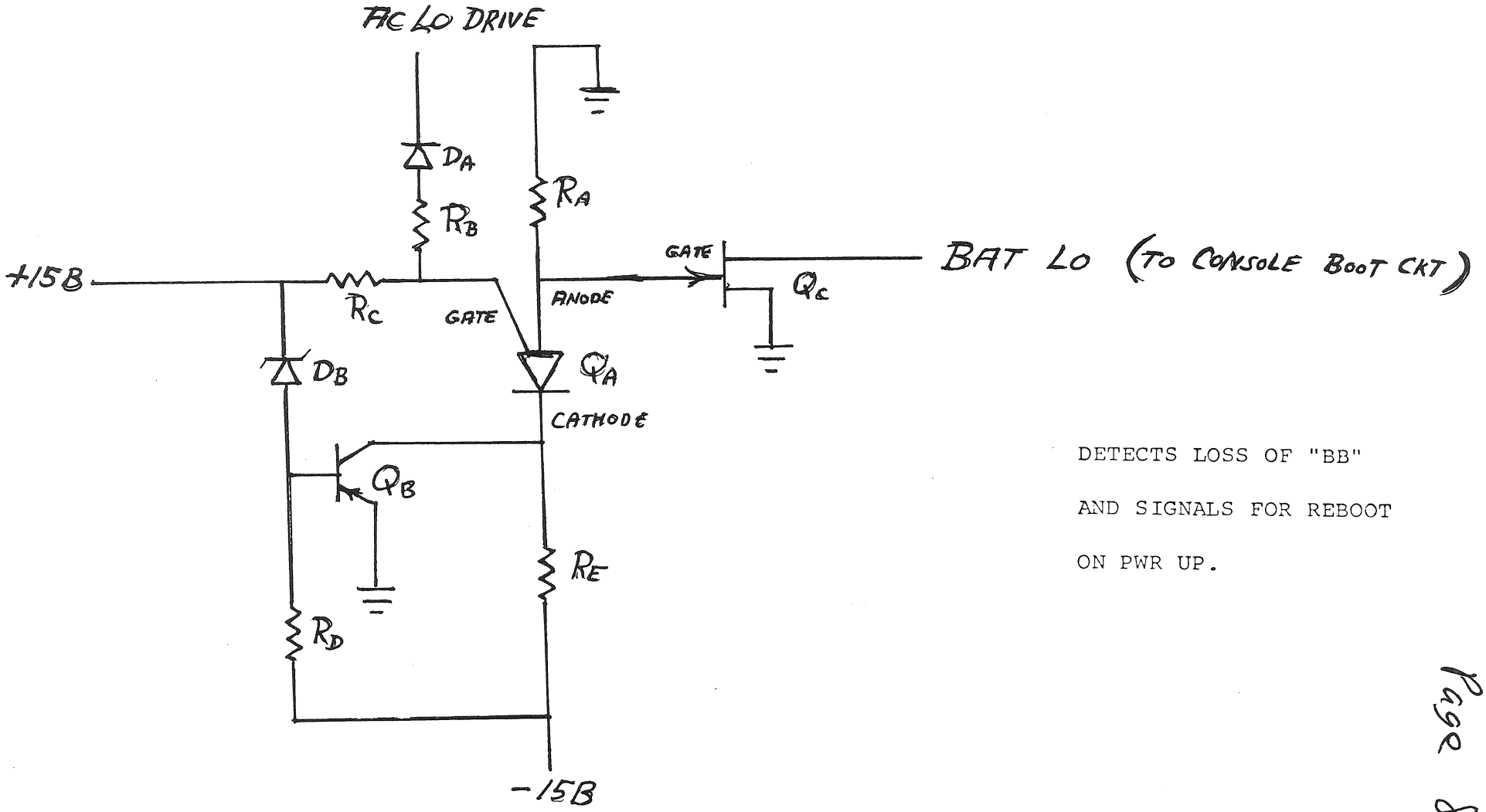
ELECTRONIC SWITCHING OF NON-MOS ±15V LOADS



See Page 84A

FIGURE 3-32

Battery Lo Detector



DETECTS LOSS OF "BB"

AND SIGNALS FOR REBOOT

ON PWR UP.

As with AC Lo and DC Lo, the driver is an N-channel (Junction Field Effect Transistor) (JFET), which is normally ON. Q(C) is opened, or turned OFF, by firing Q(A) to connect the JFET Gate to -15 volts. During operation of the H777 either on utility power or on batteries (MOS only), the Bat Lo line will be high (Q(A) is ON and Q(C) is OFF). When +15V begins to droop, due to the console switch being turned off or because the battery has been depleted, Q(B) will begin to conduct. (Threshold level is approximately 13V). Current is then shunted around the programmable unijunction transistor, Q(A), which recovers, or turns OFF. When Q(A) stops conducting, the gate of the FET, Q(C), returns to zero volts and the device resumes its low-resistance ON state. Bat Lo returns to GND level.

Q(A) will remain OFF, and Bat Lo will remain Low, until a subsequent power-up is performed and Q(A) is triggered ON by a negative level (-15V) appearing on its gate. The trigger voltage is derived from the Gate Signal on the AC Lo FET Line Driver. Hence, Bat-Lo remains low during power-up until AC Lo goes high.

3,4,9,8 Keep Alive Power (Refer to Figure 3-33) - A simple series (linear) regulator is used to keep the contact circuits in the + or - 15 volt portion of the MOS converter running at all times. As long as the H777 has utility power connected, there will be a raw DC Level present. This RDC voltage is reduced to a regulated +12 volts to enable the MOS Converter to startup when enabled by the console power switch, DC ON. Once operating, the + or -15V converter uses its own output (+15) to disable the keep alive regulator and for control power (for all internal circuitry). The keep alive function is necessary to permit restart, should a + or - 15V output be overloaded. Note that all other functions within the H777 depend on + or - 15 volts from the MOS Converter so they are disabled until it has come up.

The Keep-alive circuit is a simple series pass and zener diode regulator with protective current limiting provided by R(B), D(B), and D(C). Maximum available current is approximately:

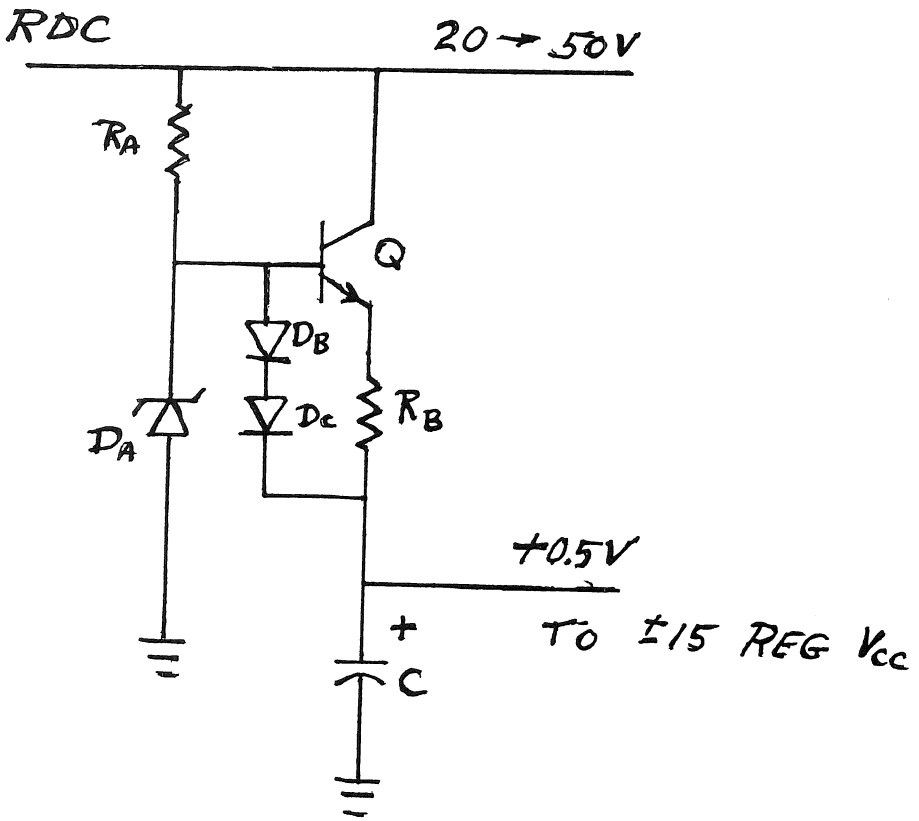
$$I_{max} = \frac{\emptyset,6V}{R(B)}$$

The line time clock signal (LTC) appears at the collector of a saturating amplifier circuit, which is driven by the secondary of the power transformer.

See Page 86A

FIGURE 3-33

Keep-Alive Power



A SIMPLE SERIES REGULATOR TO PROVIDE START-UP AND KEEP-ALIVE VOLTAGE IN THE ±15 PART OF MOS CONV.

THIS OUTPUT IS TAKEN OVER BY +15B WHEN RUNNING.

3.5 BATTERY BACK-UP

3.5.1 General Description

The H775 External Battery Back-Up Module is an uninterruptible power source designed primarily to provide DC refresh power to MOS memory in the event of a power line outage or dip. The module contains a 24 volt, 5 Amp/hour battery, and a charging circuit. It will supply up to 54 watts into a constant power load, and will support 32K of MOS memory (28 watts) for a minimum of 2 hours. Battery recharge time is 14-16 hours.

Externally accessible terminals are provided for the addition of an external battery pack, should longer hold-up time be necessary.

The standard features include an automatic shut-off circuit to prevent the battery from discharging too deeply, (complete discharge), and a charge status signal for monitoring the condition of the battery.

3.5.2 Mechanical Configuration

The H775 is housed in a 5 1/4 x 19 in. box suitable for rack mounting, with a depth of 4 1/4 in. All input and output connections are made through one 8-pin connector, as shown in Figure 3-34. Two binding posts are provided on the back for addition of the external battery. Fig. 3-35 is a diagram showing input and output connections. The ON-OFF switch is located on the front of the box. This is also a two-pole breaker for input and output overcurrent protection.

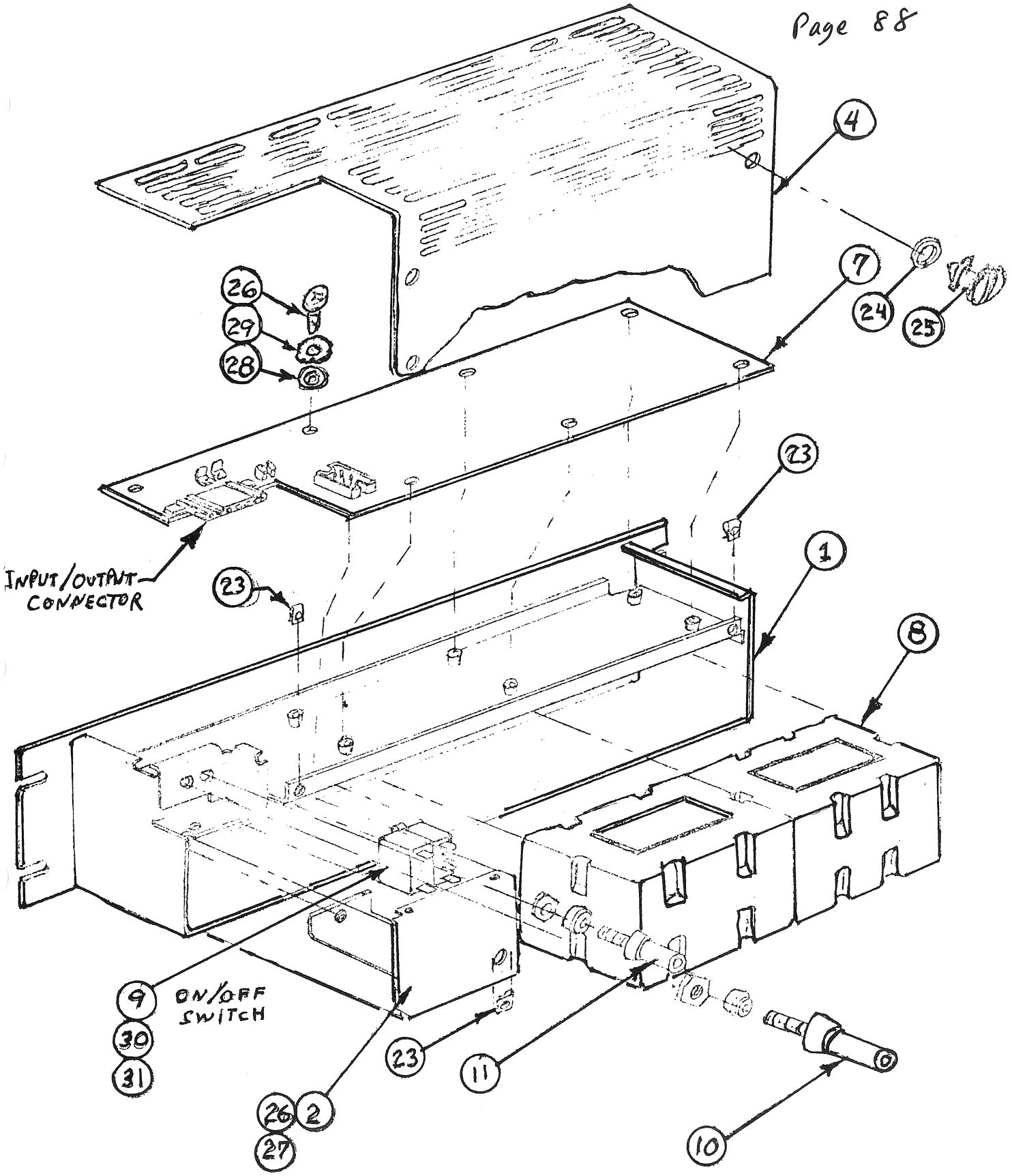


FIGURE 3-34
Battery Backup Unit (H775)

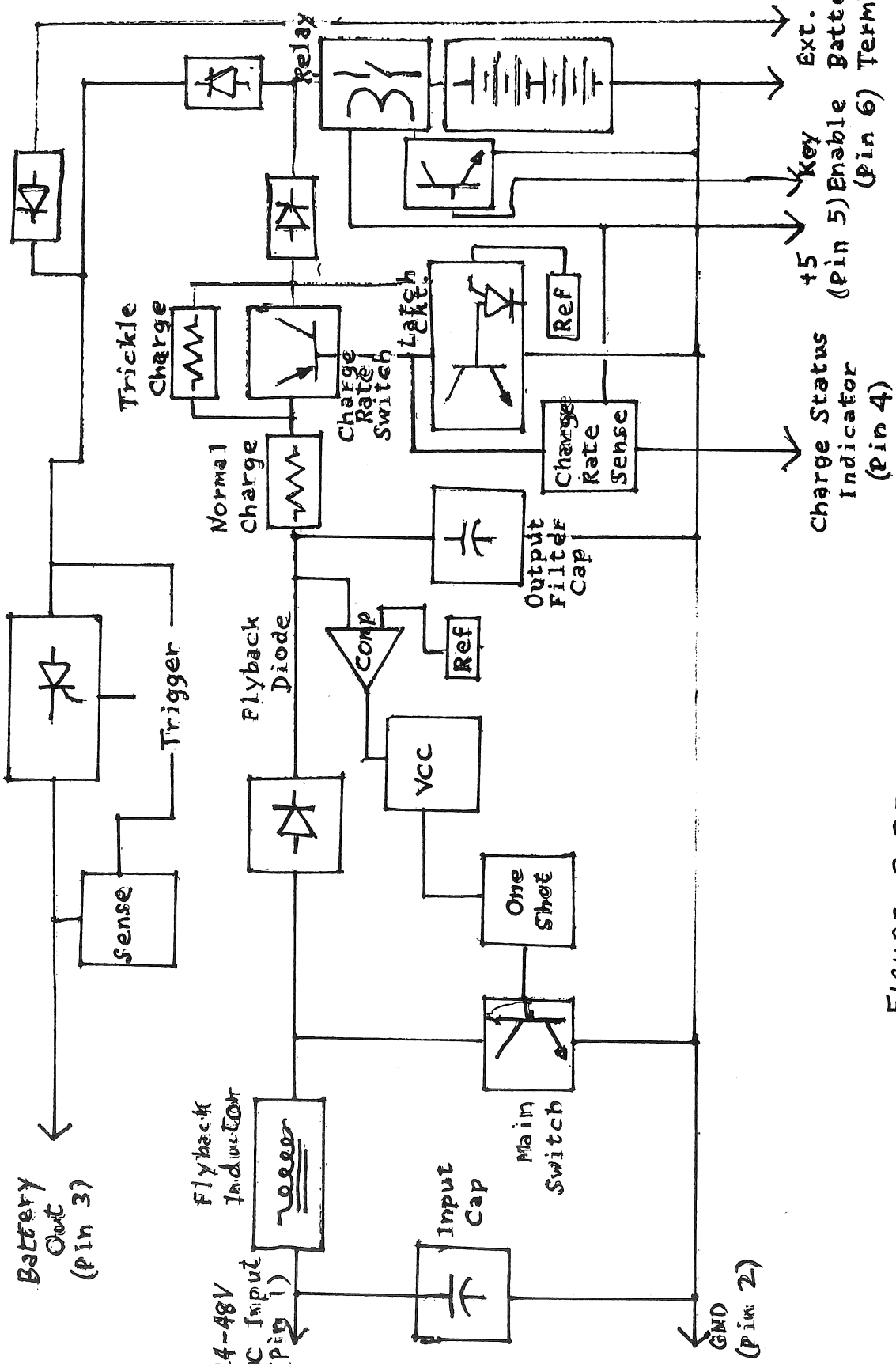


FIGURE 3-35

Functional Block Diagram of Battery Backup Unit

3.5.3 Detailed Circuit Description

3.5.3.1 Main Power Train

The front end of the charger circuit is a voltage boost circuit that employs inductive kick to step the raw 25 VDC of the H777 up to 45 volts, enough to charge the battery.

Fig. 3-36 shows the main body of the regulator. Q(A) is turned on, putting the raw DC across the inductor L, and the current I(L) starts to rise. After a preset length of time (25 usec), Q(A) turns off. At this time, the voltage at the collector will climb high enough to turn D(A), ON and the energy stored in "L" is dumped into the output cap C(A). R(A) is a current sense resistor. This limits the peak current in Q(A) by turning on Q(B), which, in turn, terminates the ON time of Q(A). Figure 3-37 is a graphic illustration of the operation of the main power train.

3.5.3.2 Control Circuit

The regulation scheme is shown in Figure 3-38. The output voltage is divided down by R(G) and R(H). This voltage is sensed by E1 and compared to the reference D(B). E2 is used as a variable frequency oscillator. The current source, consisting of Q(C), R(D) and the output of E1, charge up C(B) to the threshold of E2. At this time, the output of E2 will go low and trigger E3, which is used as a one shot. The output of E3 goes high for a fixed period of time, determined by R(C) and C(D), and turns on the main switch for this period. The peak current detector can terminate this pulse by pulling down pin 4, the reset pin, on E3. Should the output voltage on C(A) try to go too high, the output of E1 will go down and lower the frequency of E2. Figure 3-39 shows the timing relationships between various voltages.

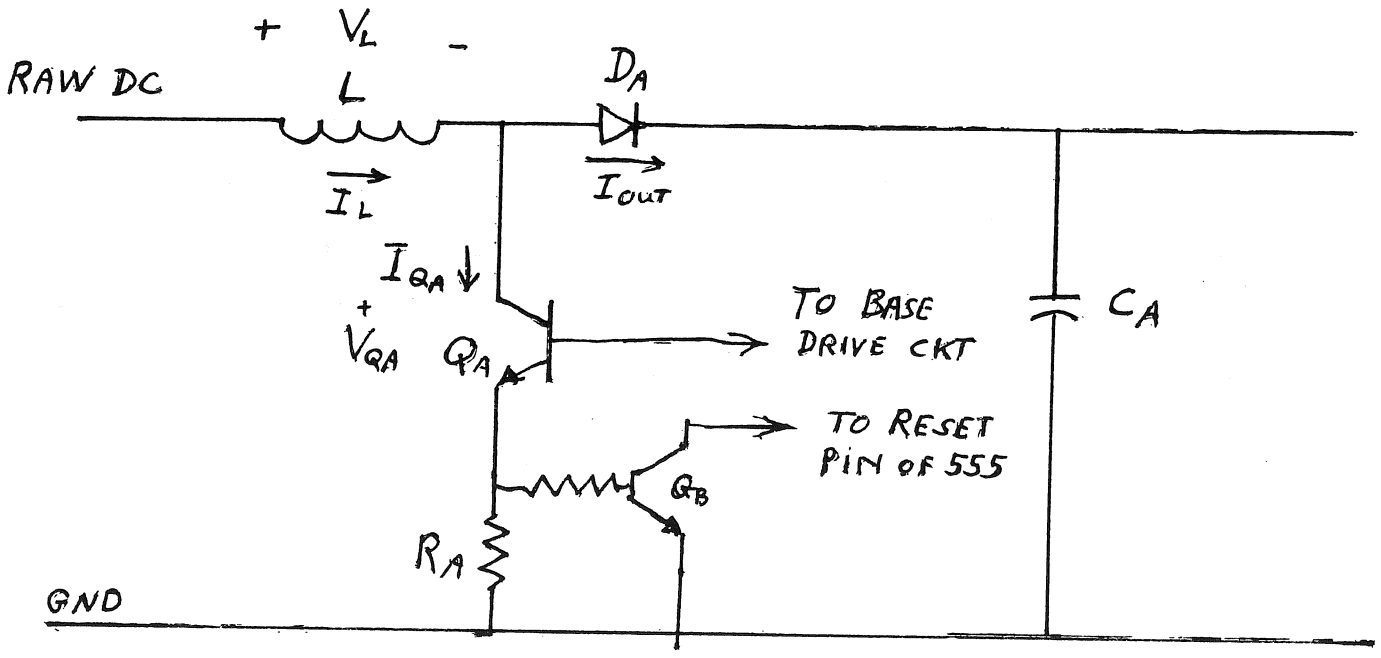
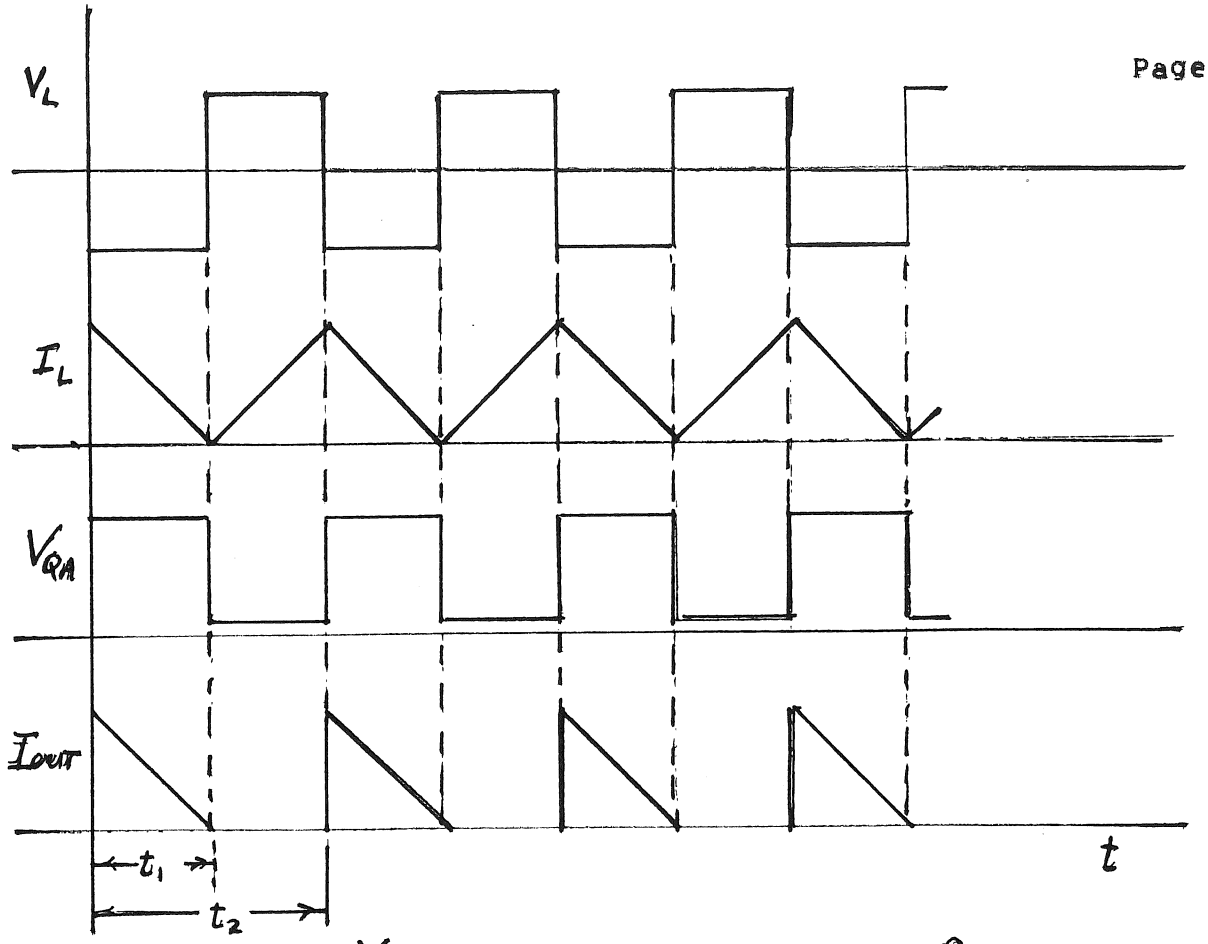


FIGURE 3-36

Main Power Train of Boost Regulator



VOLTAGE AND CURRENT TIMING RELATIONSHIPS

$t_1 \approx 25\,\mu sec.$

$t_2 \geq 50\,\mu sec.$

PEAK CURRENT DETECTOR

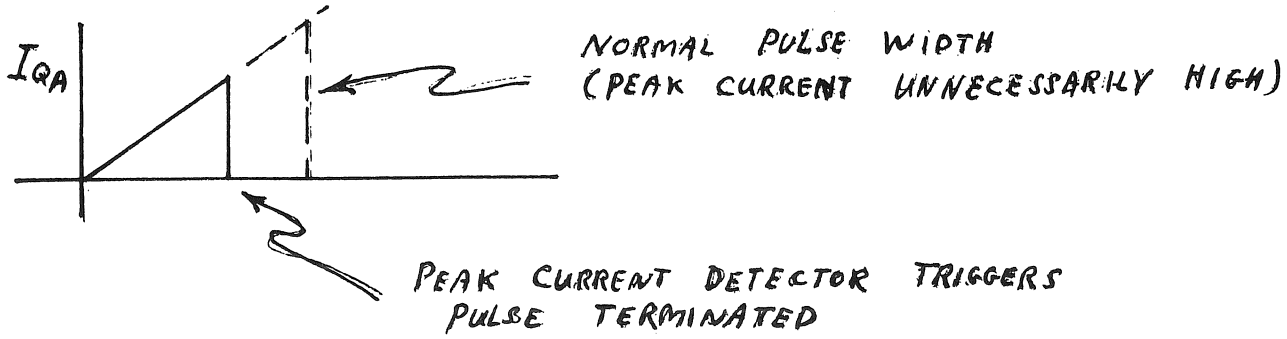


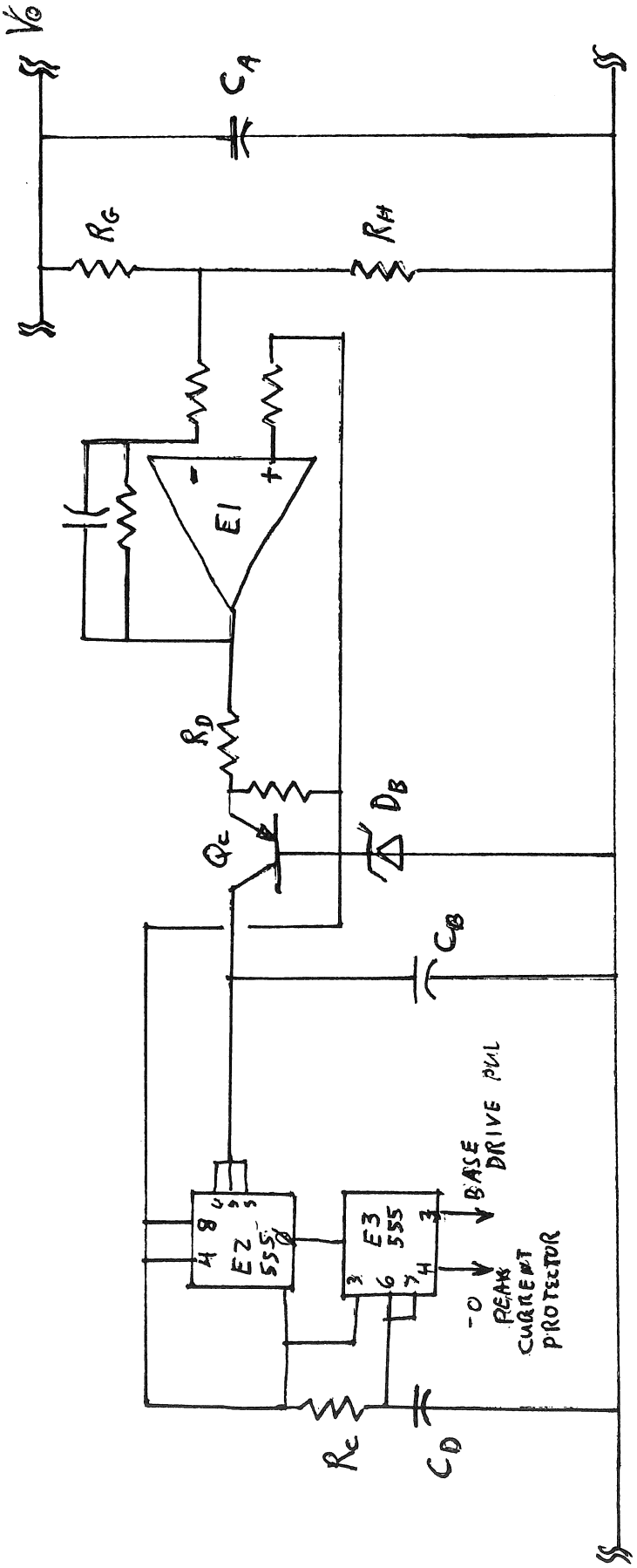
FIGURE 3-37

Operation of Main Power Train

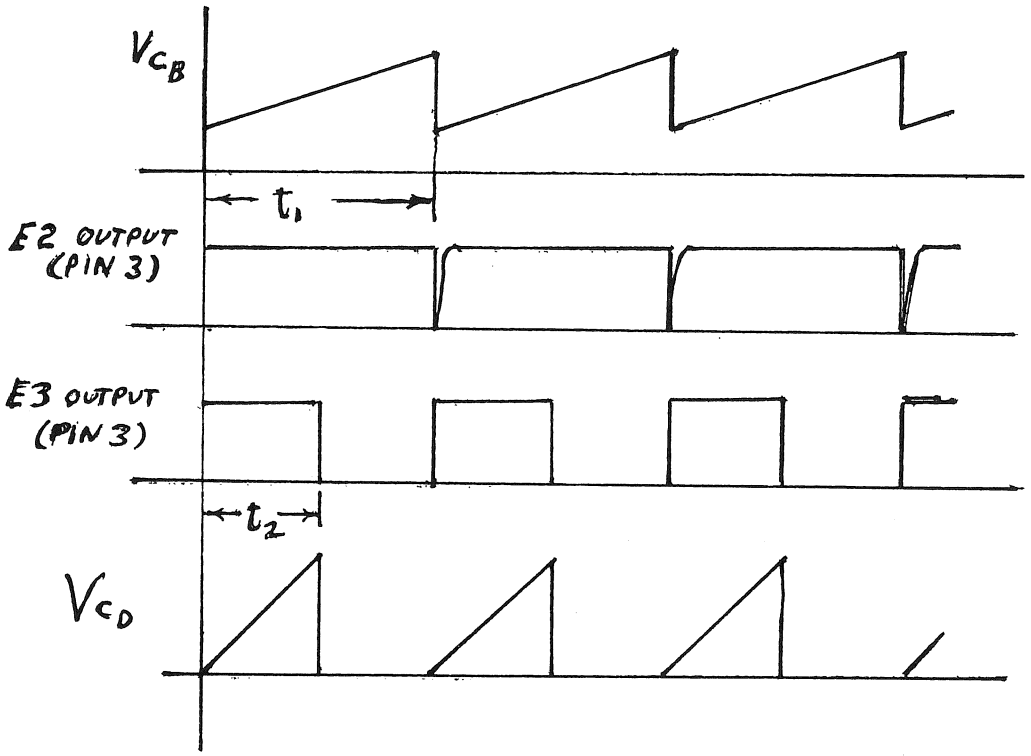
See Page 93A

FIGURE 3-38

Regulation Control Circuitry


Vo
CA
RG
RH
E1
RD
DB
QC
CB
E2
555
E3
555
BASE DRIVE PWL
REAR CURRENT PROTECTOR
RC
CD

3.5.3.3 Charge Rate Control - The charge control section is illustrated in Fig. 3-40. Initially, Q(D) and Q(G) are ON and the battery is charging at a rate determined by the output voltage on C(A) minus the battery voltage and the two resistors R(L) and R(M); nominally 0.5 Amps. The gate of Q(H), a programmable unijunction transistor, is set at 5.1V by D(D). The battery voltage, divided down by R(J) and R(K), will rise during charging. When the anode of Q(H) rises just slightly above the gate, Q(H) will turn ON. When this happens, Q(C) will no longer have any base drive, and will turn OFF. This, in turn will turn Q(D) OFF. This is defined as the trickle charge state, and the trickle current valve is determined by the difference between V(CA) and the battery voltage, and R(N), nominally 50 Ma. The circuit will remain in this state until either the battery is needed or system is turned off.



$t_1 \geq 50\ \mu sec$ (DETERMINED BY OUTPUT OF COMPARATOR)

$t_2 \leq 25\ \mu sec$ (SET BY OUTPUT OF ONE-SHOT E3) (MAY BE TERMINATED BY PEAK CURRENT DETECTOR)

FIGURE 3-39

Relative Timing of the Two 555 Timers

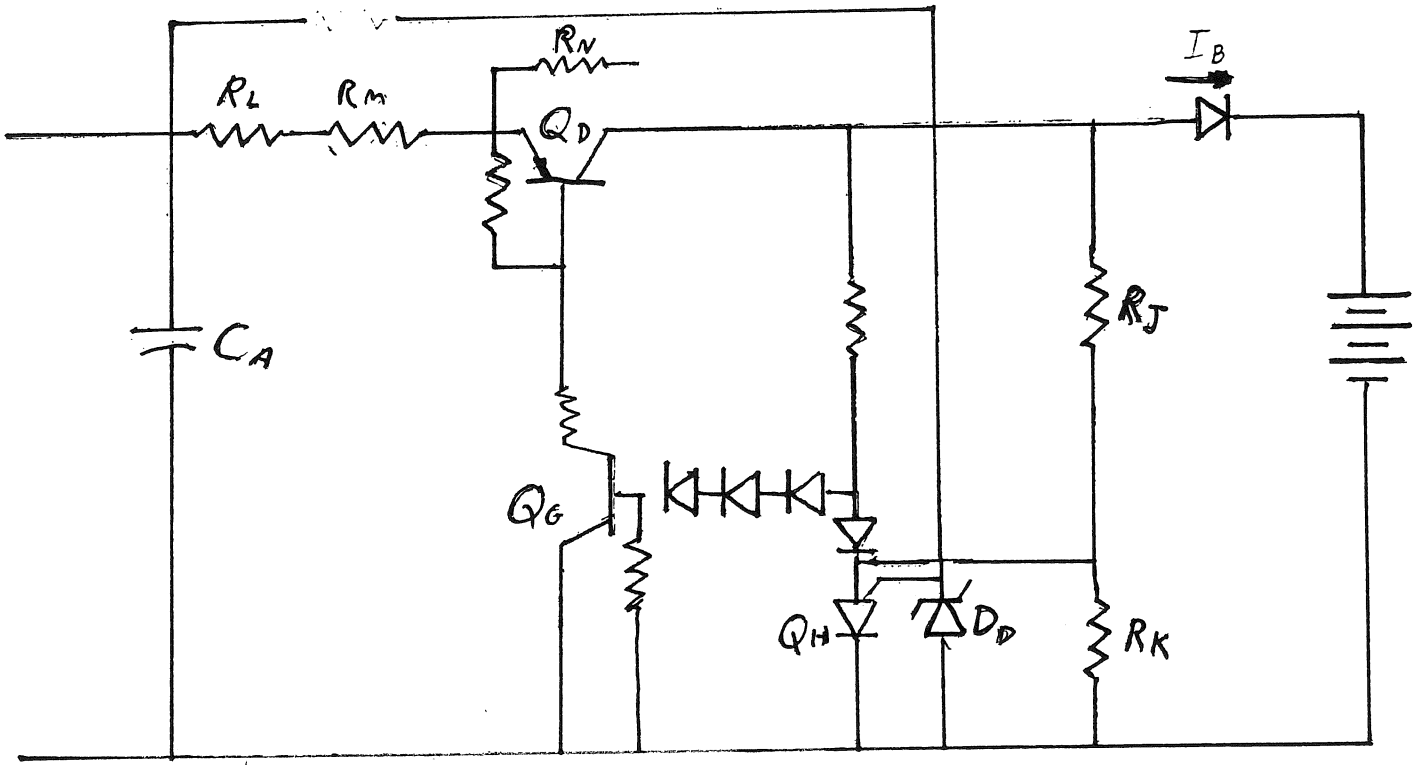
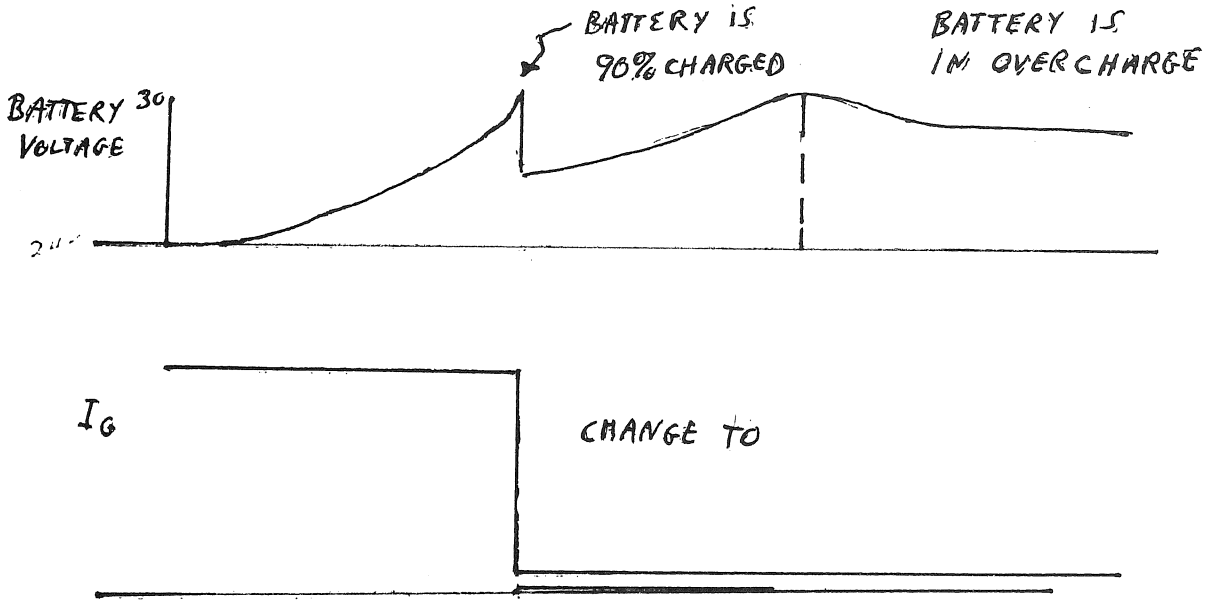


FIGURE 3-40

Charge Control Section



The above graph shows the relationship between the battery voltage and the charging current vs time at room temperature. The time scale is a function of temperature and battery aging. The times indicated will decrease by as much as 50% at the two temperature extremes (0 C and 65 C). As the battery ages, its charge acceptance decreases and the voltage rises earlier in the charging cycle.

3.5.3.4 Battery Output Section - The output section of the H775 is shown in Fig. 3-41. The BATTERY OUT line senses the raw DC of the H777. When this gets below the reference, set by D(H), D(J), and D(K), Q(R) will turn ON. This turns ON Q(P) and lets gate current flow into the SCR, D(F). With D(F) ON, the battery will supply the MOS regulators until one of two things occurs: 1) The raw DC returns, resetting the SCR, or 2) The battery depletes and shuts itself off. In the latter case, the system is completely disabled until the raw DC comes back up and the +5 volts from the MOS regulator returns.

Fig. 3-42 shows the self turn-off feature. When the raw DC is not present and the battery is discharging, Q(S) and Q(T) are ON and the relay is in the closed position. When the battery voltage drains down below the zener voltage (D(P)), Q(S) will turn OFF followed by Q(T) and the relay will open and prevent the battery from discharging too deeply and causing a serious degradation of the cycle life.

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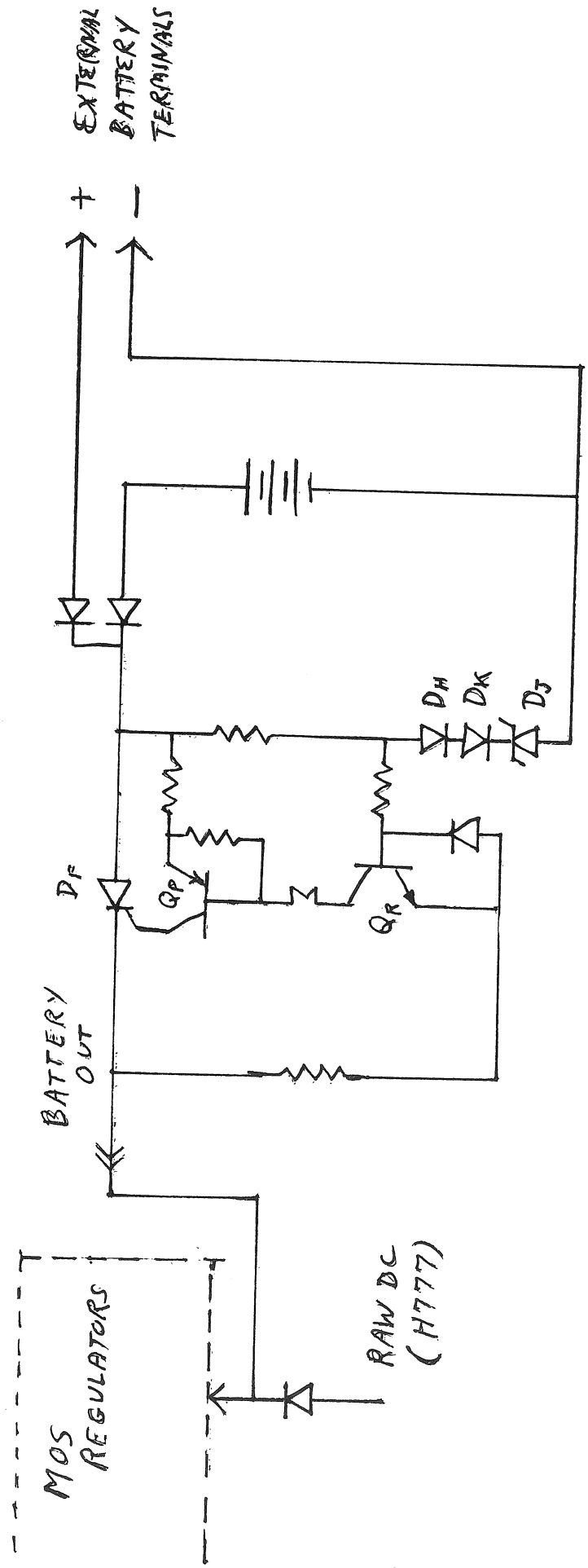
FIGURE 3-41

Output Circuit


EXTERNAL BATTERY TERMINALS
+
−
D_H
D_K
D_J
D_F
Q_P
Q_R
BATTERY OUT
MOS REGULATORS
RAW DC (H777)

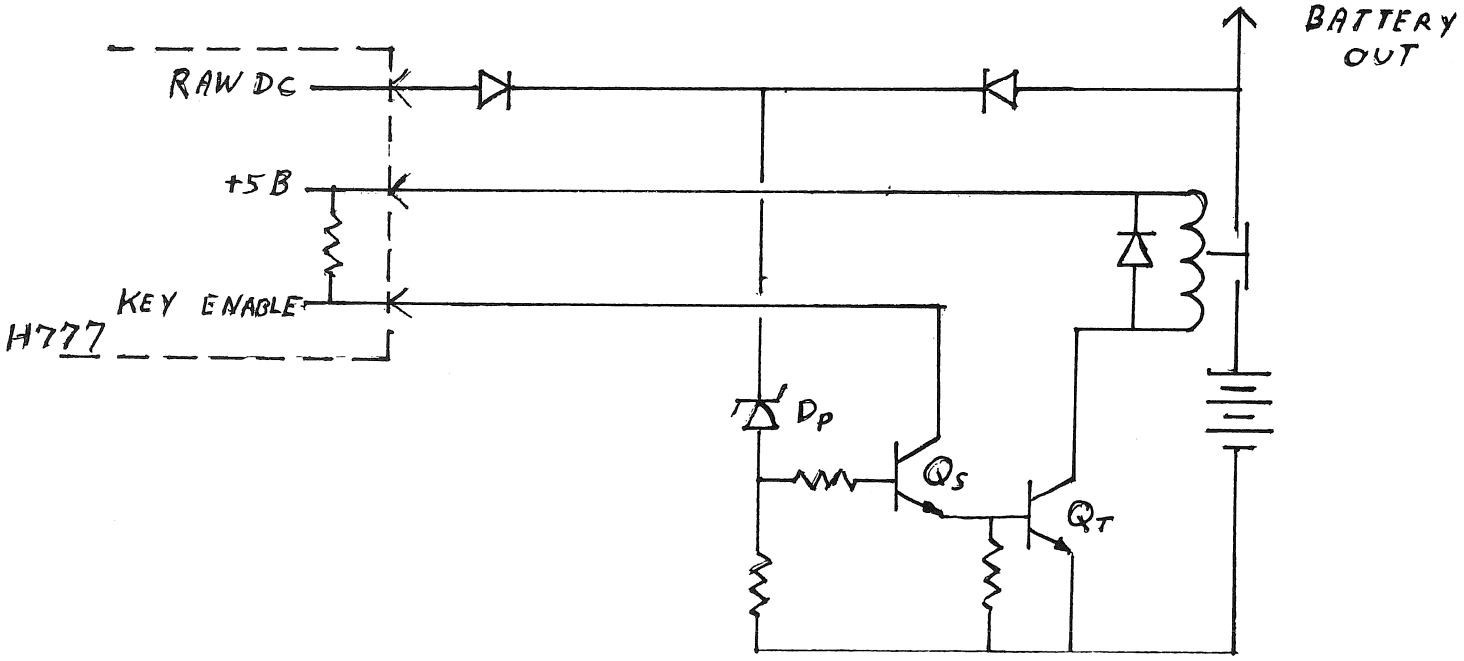
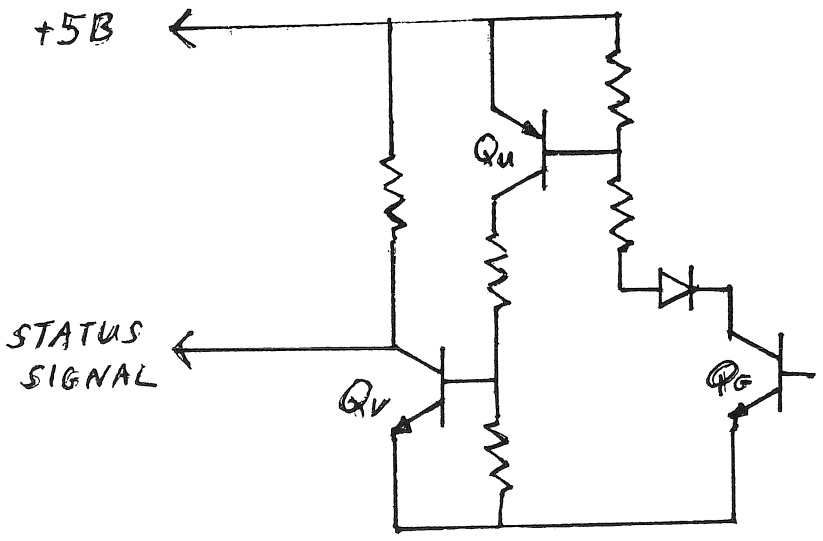


FIGURE 3-42

Self-Shutoff Circuit

3.5.3.5 Charge Rate Signal - The charge status signal is shown in Fig. 3-43. The purpose of this signal is to tell the H777 what charge mode the batery is in. When the battery is in the fast-charge mode, Q(G), Q(U) and Q(V) are all ON and the signal is low (= or <0.4V). When the battery is being trickle-charged, or when it is discharging, the signal is high (+5V). This was designed to be compatible with battery monitor circuitry in the H777.



CHARGE MODE	STATUS SIGNAL
FAST	≤ 0.4V.
TRICKLE	+5 V.
DISCHARGE	+5 V.

FIGURE 3-43

Charge status signal

CHAPTER 4

BA11-L MAINTENANCE

4.1 GENERAL

BA11-L maintenance procedures are divided into two categories: preventive maintenance and corrective maintenance. Preventive maintenance consists of specific tasks performed periodically to prevent failures caused by minor damage or progressive deterioration due to aging. Corrective maintenance is performed to isolate a fault or malfunction, or to replace a defective regulator.

4.2 PREVENTIVE MAINTENANCE

Preventive maintenance tasks consist of mechanical and electrical checks. All maintenance schedules should be established according to environmental conditions at the particular installation site. Mechanical checks should be performed as often as required to enable fans and air filters to function efficiently. All other preventive maintenance tasks should be performed on a regular schedule determined by reliability requirements. A recommended schedule is every 1000 operating hours or every three months, whichever occurs first.

A preventive maintenance log book should be established and necessary entries made according to a regular schedule. This data, compiled over an extended period of time, can be very useful in anticipating possible component failure.

4.2.1 Mechanical/Electrical

The following is a list of the steps required for mechanical checks and physical care of the BA11-L:

1. Check all fans to ensure that they are not obstructed in any way.

2. Remove console by removing four Phillips head screws. Remove air filter and clean, by immersing in water or by blowing dirt out with air gun. Dry filter, replace filter and console.

3. Inspect all wiring and cables for cuts, breaks, frays, deterioration, kinks, strain, and mechanical security. Repair or replace any defective wiring or cable covering.

4. Inspect the following for mechanical security: LED Holder assemblies, jacks, connectors, switches, power supply regulators, fans, capacitors, screws, nuts, clamps, etc. Tighten or replace as required.

5. Inspect power supply capacitors for leaks, bulges, or discoloration. Replace as required.

4.3 CORRECTIVE MAINTENANCE

The H777 power supply consists of field replaceable modules. Once a power system failure is discovered, the following steps, associated flow chart (figure 4-1), print set, and power supply description in chapter 3 can be utilized to isolate the malfunction to a faulty module.

4.3.1 Voltage Regulator Checks

There are no adjustments on the H777 power supply. The power supply voltages are supplied by the regulators listed in Table 4-1. Perform the following steps to ensure that the voltages are within tolerance.

1. Using a DVM, measure the output voltages under normal load conditions at the backplane. An out-of-tolerance regulator should be replaced. (Remember you need a 1% meter to measure tolerance correctly).

2. Using an oscilloscope, measure the peak-to-peak ripple content* on all DC outputs (Table 4-1).

4.4 H777 POWER SUPPLY

The five main subassemblies inside the supply can be broken down into two categories. First, those that can be removed from the assembly without removing the whole supply. The second are those that require the removal of the supply to affect their removal.

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* Ripple current must be measured using a scope probe with a tip ground probe. That is, a GND line no more than one inch long.

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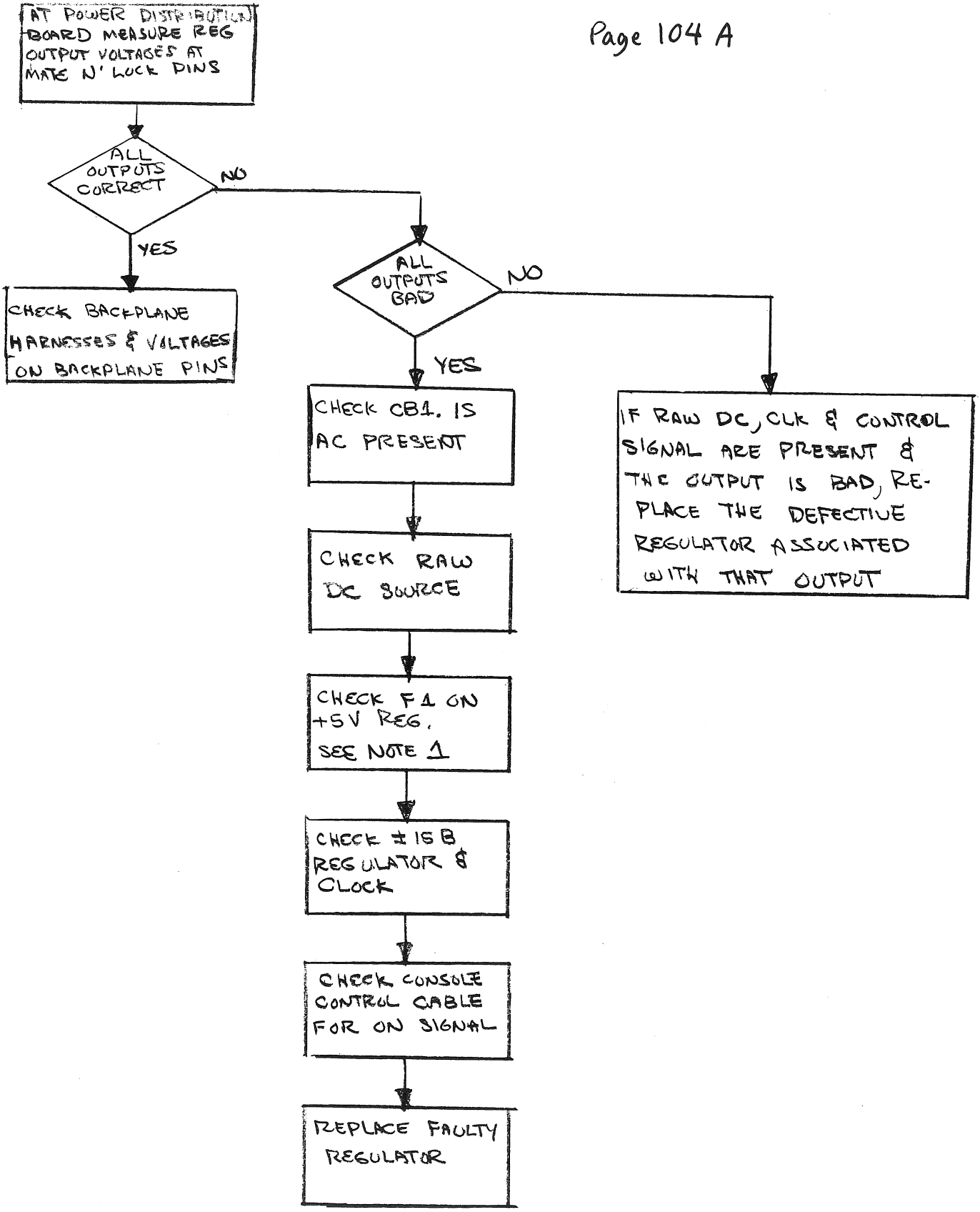
FIGURE 4-1

H777 Fault Isolation Flow Chart



NOTE 1

FUSE F1 WILL NOT BLOW UNLESS A REGULATOR HAS AN INTERNAL PROBLEM

FIGURE 4-1 H777 FAULT ISOLATION FLOW CHART

TABLE 4-1
REGULATOR OUTPUT SPECIFICATIONS

REGULATOR	OUTPUT	TOLERANCE	CURRENT	MAX P-P RIPPLE
+5V, MAIN	+5V	+ or - 5%	0-25amps	3%
MOS Regulator	+15,5B	+ or - 5%	0-2amps	3%
	+15V	+ or - 5%	shared with	3%
	-15,5B	+ or - 5%	all four	3%
	-15V	+ or - 5%	outputs	3%
	+5B	+ or - 5%	0-4amps	3%
Core Regulator	+20V	+ or - 3%	0-6amps	3%
	-5V	+ or - 5%	0-4amps	3%

4.4.1 H777 power Supply Removal

WARNING

Turn off DC power control switch on the console, turn off the circuit breaker CB1, and disconnect the AC line cord in this order to ensure that the Battery Backup Option will turn itself off.

1. Disconnect the console power control cable (CP2).
2. Remove four console mounting screws. Tilt console forward to remove CP2.
3. Disconnect the backplane harness, the power control harness, and battery backup harness from the Power Distribution Board.
4. Disconnect the logic fan AC plug.
5. Remove one botton, four side, and two rear mounting screws.
6. Lift the supply straight up to remove.

4.4.2 Removal of H777 Power Supply Subassemblies

The following procedure covers the removal of the main components of the supply. Any interaction is specified. The major components are:

1. Power supply cover
2. AC Control Assembly (remove the supply first)

3. Fan

4. MOS Regulator

5. Main +5V regulator (remove the supply first, then remove the MOS regulator from the supply).

4.4.3 Power Supply Cover Removal

1. Turn off circuit breaker CB1 before removing cover.

2. Turn console switch to OFF position.

WARNING

If console switch is shut off first, the internal raw DC capacitors will remain charged to approximately 40 volts.

3. The power supply cover is mounted by seven screws; three on top and four on the side (see figure 4-2). Lift cover straight up to remove.

To Be Supplied

FIGURE 4-2

4.4.4 Removal of AC Control Assembly

WARNING

Turn off circuit breaker CB1. Wait for surge relay to drop out (about 10 seconds maximum). Then turn off console switch and remove AC line plug from socket. Turn off H775 Battery Backup unit, if present.

1. Remove the supply first (See paragraph 4.4.1)
2. Remove the screw from the fan bracket on top of fan.
3. Remove the four bottom mounting screws from the transformer base (T1).
4. Remove the transformer (T1) outputs and the relay (K1) outputs from the +5 regulator (TB1).
5. Disconnect the logic and power supply fan connectors.
6. Tilt the assembly to expose the bottom of the circuit breaker. Remove the line cord fastoon tabs.
7. Disconnect console cable from +5V regulator.
8. Lift out the assembly.

4.4.5 Fan Removal (Power Supply)

WARNING

Turn off circuit breaker CB1. Wait for surge relay to drop out (about 10 seconds maximum). Then turn off console switch and remove AC line plug from socket. Turn off H775 battery back up unit, if present.

1. Remove AC plug from fan.
2. Remove screw from AC control bracket on top of fan.
3. Remove two screws from bottom of sheet metal.
4. Lift out fan.

To install a new fan, remove brackets from old fan. Install on replacement fan and reverse the removal procedure.

4.4.5.1 Fan Removal (Logic)

WARNING

Remove AC plug or turn off circuit breaker CB1 before removing fan.

1. Remove AC plug from fan.
2. Remove four console mounting screws and tilt the console (KY11-LA or KY11-LB) forward.
3. Remove air filter.
4. Remove four mounting screws from fan and lift out the fan.

4.4.6 MOS Regulator Removal

WARNING

Turn off circuit breaker CB1, wait for surge relay to drop out (about 10 seconds maximum). Then turn off console switch and remove AC line plug from socket. Turn off H775 battery backup unit, if present.

Turning off the MOS regulator will cause memory to lose all data.

1. Remove MJ1 battery backup option cable.
2. Remove two mounting screws on edge of board.
3. Remove two screws holding heat sink.
4. Lift regulator board and remove MJ2 9-pin Mate-N-Lok from Power Distribution Board.
5. Disconnect 3M cable from +5 regulator board.
6. Remove MOS regulator assembly.

4.4.7 Main +5V Regulator Removal

WARNING

Turn off circuit breaker CB1 before starting. Observe warning specified in Paragraph 4.3.4.

The MOS regulator must be removed prior to removing the main +5V regulator (See 4.3.4).

1. Remove MOS REGULATOR FIRST (Paragraph 4.3.4).
2. Remove TB1 connections.
3. Disconnect backplane harnesses from Power Distribution Board.
4. Disconnect power control connector from Power Distribution Board (if present).
5. Disconnect 3M cable from console. Remove Console first.
6. Remove screws from power distribution assembly.
7. Remove screws from bottom of the +5V regulator.
8. Remove the Regulator and Power Distribution Assembly.