EK-AXV11-UG-002

LSI-11 Analog System User's Guide

ADV11-C, AAV11-C, AXV11-C Modules with KWV11-C Real-Time Clock

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PREFACE

This manual is written for the user of DIGITAL's dual-height analog I/O printed circuit board options for the LSI-11 processor. The manual is divided into chapters that are specific to each analog board. Each chapter includes specifications, a functional description, programming information, and configuration data. The configuration data allows the user to change the operation of the boards to meet the user's application.

Chapter 1 is an introduction.

Chapter 2 describes the ADV11-C Analog Input Board.

Chapter 3 describes the AAV11-C Analog Output Board.

Chapter 4 describes the AXV11-C Analog Input/Output Board.

Chapter 5 describes the KWV11-C Programmable Real-Time Clock Board that is used in many applications to start analog-to-digital conversions.

Chapter 6 has calibration and testing procedures for the analog boards. Information on an optional analog test fixture is also included in this chapter.

A number of suggestions are made in the text pertaining to specific configurations and general good practice when connecting the boards to external equipment. No suggestion is made that exceeds the specifications for each board. The user has the responsibility for connecting these boards to each other and to external equipment.

CHAPTER 1
INTRODUCTION

1.1 GENERAL

This manual includes information on a series of analog boards that are I/O options for the LSI-11 family of processors. Each board may be used by itself on the LSI-11 bus, but typically each is used with one or more of the other boards to create an analog I/O system. The boards include the following.

ADV11-C Analog Input Board, A8000
AAV11-C Analog Output Board, A6006
AXV11-C Analog Input/Output Board, A0026
KWV11-C Programmable Real-Time Clock, M4002

The ADV11-C and the AXV11-C each accept up to 16 single-ended analog inputs or 8 differential analog inputs. Each has a programmable gain of 1, 2, 4, or 8 times the input signal. The user connects analog signals to the board through an I/O connector. After the analog-to-digital conversion is complete, the user gets the results by a programmed I/O transfer or by servicing an interrupt request.

In addition to the input channels, the AXV11-C has two digital-to-analog converters (DACs). Each DAC is loaded with digital data from the LSI-11 bus to be changed to an analog voltage. The user can change the format of the input data and output range and polarity.

The AAV11-C has four DACs. Each of the DACs has a separate register that can be written or read in byte or word format, allowing complete use of the LSI-11 instruction set. Each DAC is loaded from the LSI-11 bus to create an analog output voltage at its I/O connector. One of the registers can also be used as a 4-bit digital output for control signals, such as CRT intensity, blank, or erase.

The KWV11-C is included in this manual as this board has a crystal oscillator and two Schmitt triggers that are often used with the A/D input boards to start A/D conversions. An A/D conversion may be started at a crystal-controlled rate, at a line frequency rate (50/60 Hz), or from an external event input.

1.2 REFERENCES

The following manuals provide LSI-11 bus signal specifications and provide added information on other LSI-11 options.

Title	Part Number
Microcomputers and Memories	EB-18451-20
Microcomputer Interfaces Handbook	EB-20175-20
PDP-11 Bus Handbook	EB-17525-20

These manuals are available through your local DIGITAL sales office or contact:

Digital Equipment Corporation
Accessories and Supplies Group
P.O. Box CS2008
Nashua, New Hampshire 03061

CHAPTER 2
ADV11-C ANALOG INPUT BOARD

2.1 INTRODUCTION

The ADV11-C is an LSI-11 analog input printed circuit board, A8000. It accepts up to 16 single-ended inputs, or up to 8 differential inputs, either unipolar or bipolar. A unipolar input can range from 0 V to 10 V. A bipolar input can range from −10 V to +10 V. The ADV11-C also has a programmable gain on these inputs of 1, 2, 4 or 8 times the input voltage.

Analog-to-digital (A/D) conversions are started by a program command, an external trigger, or a real-time clock input. When the program command sets the A/D START bit in the control/status register, the ADV11-C starts the A/D conversion on the input channel selected.

The ADV11-C changes the analog input into digital data. The digital data goes to the A/D data buffer register and waits for a programmed data transfer to the LSI-11 processor or memory, or the ADV11-C puts an interrupt request on the LSI-11 bus and waits for the interrupt request to be acknowledged.

2.2 FEATURES

The ADV11-C has the following features.

- 16 single-ended analog input channels or 8 differential analog input channels; SE/DI jumper is field-selectable.
- Programmable gain of 1, 2, 4, or 8.
- 12-bit output data resolution.
- Output data notation in binary, offset binary, or 2's complement format.
- A/D conversions can be started by a program, a real-time clock, or an external trigger.
- A/D results can be received by a programmed I/O transfer or by servicing an interrupt request.
- Interrupts can be enabled and automatically set by A/D DONE and/or ERROR bits.
- Common mode rejection ratio of 80 db at maximum range.

2.3 ADV11-C SPECIFICATIONS

Identification	Dual-height module, A8000; part number 30-18693
Power Requirements	+5 V (±5%) @ 2.0 A
Bus Loads	
DC bus load	1
AC bus load	1.3

I/O Connector — 26 pins; 3M no. 3399-7026

Analog Input

No. of analog inputs — 8 channels using differential inputs, or 16 channels using single-ended inputs

Input range — 0 V to +10 V
−10 V to +10 V

Input gain (programmable)

Gain (± 0.05%)	**Range**
1	10 V
2	5 V
4	2.5 V
8	1.25 V

Maximum input signal — ±10.5 V (signal + common mode voltage)

Input impedance

Off channels	100 MΩ min in parallel with 10 pF max
On channels	100 MΩ min in parallel with 100 pF max
Power off	1 kΩ in series with a diode

Input bias current — 20 nA @ 25° C, max

Input protection — Inputs are current-limited and protected to ±30 V overvoltage without damage.

Common mode rejection ratio — 80 db @ 10 V range at 60 Hz

A/D Output

Data buffer register — 16-bit read-only output register

Resolution — 12-bit unipolar; 11-bit bipolar plus sign

Data notation — Binary, offset binary, or 2's complement

Coding

Notation Used	**Full-Scale Input Voltage**	**Output Code (Octal)**
Binary	+9.9976 V	007777
	0.0000 V	000000
Offset binary	+9.9951 V	007777
	0.0000 V	004000
	−10.0000 V	000000
2's complement	+9.9951 V	003777
	0.0000 V	000000
	−10.0000 V	174000

Sample and Hold Amplifier

Aperture uncertainty	Less than 10 ns
Aperture delay	Less than 0.5 μs from start of conversion to signal disconnect.
Front end settling	Less than 15 μs to $\pm$0.01% of full-scale value for a 20 V p–p input.
Input noise	Less than 0.2 mV rms

A/D Converter Performance

Linearity	$\pm$1/2 LSB
Stability (temperature coefficient)	$\pm$30 ppm/°C
Stability, long-term	$\pm$ 0.05% change per 6 months
System accuracy	Input voltage to digitized value $\pm$0.03%
Conversion time	25 μs from end of front end settling to setting the A/D DONE bit
System throughput	25K channel samples per second

Environment
(Per DEC Standard 102, Class C)

Temperature, operating*	5° C to 60° C (41° F to 140° F)
Temperature, not operating	−40° C to 66° C (−40° F to 150° F)
Relative humidity, operating	10% to 95% with max wet bulb of 32° C (90° F) and min dew point of 2° C (35° F) not condensing
Altitude, operating	2.4 km (8,000 ft) max
Altitude, not operating	9.2 km (30,000 ft)

2.4 ADV11-C FUNCTIONAL DESCRIPTION

Figure 2-1 shows a block diagram of the ADV11-C. It is addressed via the LSI-11 bus at its interface transceivers. The board has jumpers to select its device address. It has two addressable registers: the control/status register (CSR) and the data buffer register (DBR). The board also has jumpers to select the base interrupt vector. The ADV11-C has two interrupt vectors. One is enabled when A/D DONE is set in the CSR; the other may be enabled for an ERROR set in the CSR. The ERROR vector automatically receives the base interrupt vector address + 4. See Paragraph 2.6.1 to set up the address and vector jumpers.

*Lower the maximum operating temperature 1.8° C for each 1000 m above sea level (or 1° F for each 1000 ft above sea level).

Once addressed the transceivers send the bus data instruction to the CSR. The instruction selects 1 of 16 channels, determines the gain selected (GS0, GS1), and determines how the board will start an analog conversion. An analog conversion can be started by a real-time clock input, by an external event trigger, or under program control by setting the A/D START bit in the CSR.

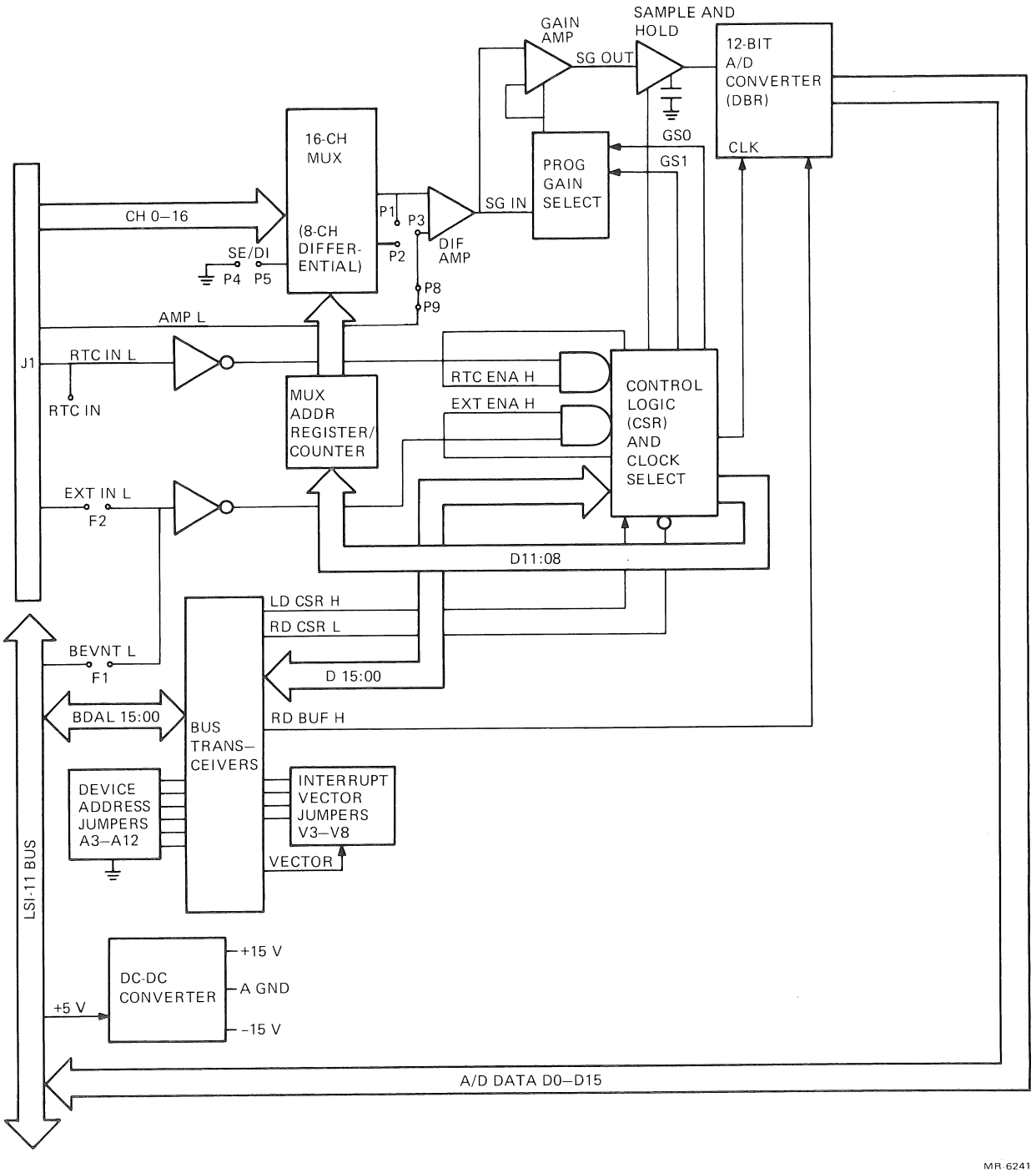


Figure 2-1 ADV11-C Block Diagram

The multiplexer uses single-ended or differential inputs. (See Paragraph 2.6.3.) Two jumpers (F2, F1) determine whether the external trigger comes from the I/O connector (J1) or from the LSI-11 bus 50/60 Hz line input (BEVNT L).

The output of the multiplexer goes to a differential amplifier then to a programmable gain amplifier. Its gain is set by writing bits 2 and 3 in the CSR. The gain selected (GS0 and GS1) may be 1, 2, 4, or 8 times the input voltage.

The output of the programmable gain amplifier goes to a sample and hold amplifier, where the analog signal is continuously sampled until one of the following inputs is received.

- A/D START bit set in the CSR
- Real-time clock input at I/O connector or at pin RTC IN
- External event trigger input at I/O connector or at LSI-11 bus BEVNT line.

When one of these inputs has been received, the sample and hold amplifier switches to "hold" and the 12-bit A/D converter digitizes the held analog voltage.

When the A/D conversion is complete, the A/D DONE bit is set in the CSR, and the sample and hold amplifier returns to sampling. If the DONE INT ENABLE bit is also set, an interrupt occurs to the LSI-11 bus. When the interrupt is acknowledged, the data is read by reading the data buffer register (DBR).

2.5 PROGRAMMING THE ADV11-C REGISTERS

The ADV11-C has the following two programmable registers.

Control/Status Register (CSR), read/write, byte-addressable register
Data Buffer Register (DBR), read-only, word-addressable register

This paragraph describes the mode of operation determined by setting bits in the CSR and defines the bits in both registers.

2.5.1 Selecting ADV11-C Mode of Operation

The user determines the mode of operation of the ADV11-C. The user selects how the A/D conversions are to start and how the digital data is transferred to the LSI-11 processor.

Starting an A/D Conversion – An A/D conversion can be started in one of three ways.

1. Real-time clock input: Set bit 5 in CSR
2. External trigger enable: Set bit 4 in CSR
3. A/D START bit: Set bit 0 in CSR

Transferring Data to LSI-11 – The digital data can be transferred to the LSI-11 processor or memory by a programmed I/O transfer or by servicing an interrupt request.

Using LSI-11 instructions, a programmed I/O transfer can write the CSR in the ADV11-C, read the CSR, and wait for an A/D DONE bit (bit 7), then read the DBR to get the A/D data.

If interrupts are used, set interrupt enable bit (bit 6) of the CSR. When the A/D conversion is complete, the A/D DONE bit (bit 7) sets, and an interrupt occurs to the LSI-11 processor. The processor services the interrupt request and gets the A/D data. After receiving the data, the software clears the A/D DONE bit in the ADV11-C's CSR.

An interrupt may also be programmed to occur on an error condition by setting bit 14 in the CSR.

2.5.2 ADV11-C Standard Device Address

The ADV11-C permits assigning a device address between 160000_8 and 177770_8. The standard device address is 170400_8. This is the starting address for the control/status register. The data buffer register automatically receives the starting address + 2, or 170402_8. Table 2-1 shows the standard address and interrupt vector address assignments. See Paragraph 2.6.1 to change the device address.

2.5.3 ADV11-C Standard Interrupt Vector Address

The interrupt vector can be assigned between 0 and 770_8 in increments of 10_8. The standard base interrupt vector for the ADV11-C is 400_8. This vector is assigned to the A/D DONE interrupt request. If the DONE INT ENABLE bit (bit 6) is set in the CSR, the A/D DONE bit (bit 7) enables the interrupt request to the LSI-11 bus. When the interrupt request is acknowledged by the LSI-11 processor, the interrupt service routine is started at the address contained in location 400_8.

The ADV11-C can also interrupt on an error. The error interrupt request is automatically assigned the base vector address + 4, or 404_8. If the ERROR INT ENABLE bit (bit 14) is set by the program, an interrupt request will occur at the occurrence of any error (bit 15 set).

The standard interrupt vector addresses are shown in Table 2-1. See Paragraph 2.6.2 to change the interrupt vector address.

Table 2-1 Standard Address Assignments

Description	Mnemonic	First Module Address	Second Module Address
Registers			
Control/Status	CSR	170400	170420
Data Buffer	DBR	170402	170422
Interrupt Vectors			
A/D DONE		400	410
ERROR		404	414

2.5.4 Control/Status Register (CSR)

The control/status register is a read/write register, shown in Figure 2-2. A control instruction is written into the CSR; the A/D status is read from the CSR. The bit definitions are described in Table 2-2.

2.5.5 Data Buffer Register (DBR)

The data buffer register is a read-only register that holds the digital data after the A/D conversion is complete. The DBR can be read after the A/D DONE flag is set in the CSR register. The format for the DBR is shown in Figure 2-3. The bit definitions are described in Table 2-3. The DBR is cleared after reading the register or on initializing the LSI-11 bus.

2.6 CONFIGURING THE ADV11-C

The ADV11-C, shown in Figure 2-4, has jumpers to set up the device address, the interrupt vector address, and the analog configuration. The user may select the A/D input range, polarity, and the output data notation.

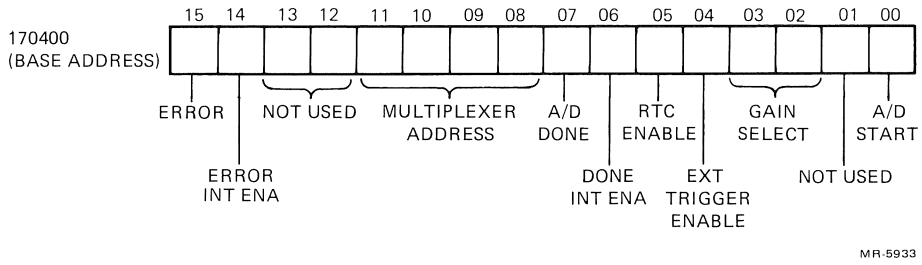


Figure 2-2 ADV11-C Control/Status Register (Read/Write)

Table 2-2 ADV11-C Control/Status Register Bit Assignments

Bit	Name	Description
0	A/D START	Write Only – When set this bit starts an A/D conversion. This bit is cleared by internal logic after starting conversion. It always reads back 0.
1	Not used	
2, 3	GAIN SELECT	Read/Write – Set these bits to select the gain for the analog input as follows. **Gain** **GS1 (bit 3)** **GS0 (bit 2)** 1 0 0 2 0 1 4 1 0 8 1 1
4	EXT TRIG ENABLE	Read/Write – When set this bit allows an external trigger to start an A/D conversion.
5	RTC ENABLE	Read/Write – When set this bit allows a real-time clock input to start an A/D conversion.
6	DONE INTERRUPT ENABLE	Read/Write – When set this bit enables an interrupt on A/D DONE (bit 7). Both bits are cleared by INIT.
7	A/D DONE	Read Only – This bit is set at the end of an A/D conversion and is reset by reading the A/D data buffer register.
8–11	MULTIPLEXER ADDRESS	Read/Write – These bits select 1 of 16 analog input channels.
12–13	Not used	
14	ERROR	Read/Write – When set this bit enables an interrupt on an ERROR (bit 15). Both bits are cleared by INIT.
15	ERROR INTERRUPT ENABLE	Read/Write – When set this bit indicates that an error has occurred due to one of the following. • Trying an external start or clock start during multiplexer settling time. • Trying a start while an A/D conversion is in process. • Trying any start while the A/D DONE bit is set. This bit can be cleared by writing the CSR or by an INIT.

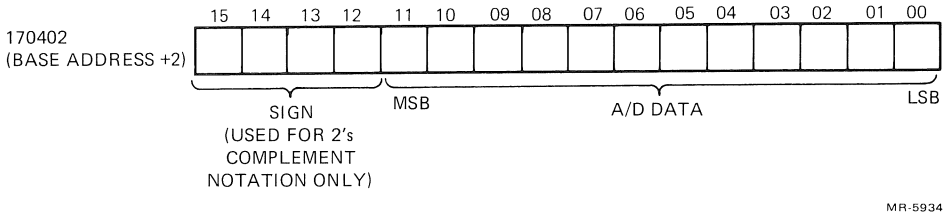


Figure 2-3 ADV11-C Data Buffer Register (Read Only)

Table 2-3 ADV11-C Data Buffer Register Bit Assignments

Bit	Name	Description
0–11	A/D DATA	These bits hold the parallel digital output after completion of the A/D conversion in one of the following data notations. • binary • offset binary • 2's complement The user selects the data notation; see Paragraph 2.6.4.
12–15	SIGN	These bits are the sign for the bipolar inputs when using 2's complement notation. These bits are not used for binary or offset binary notation.

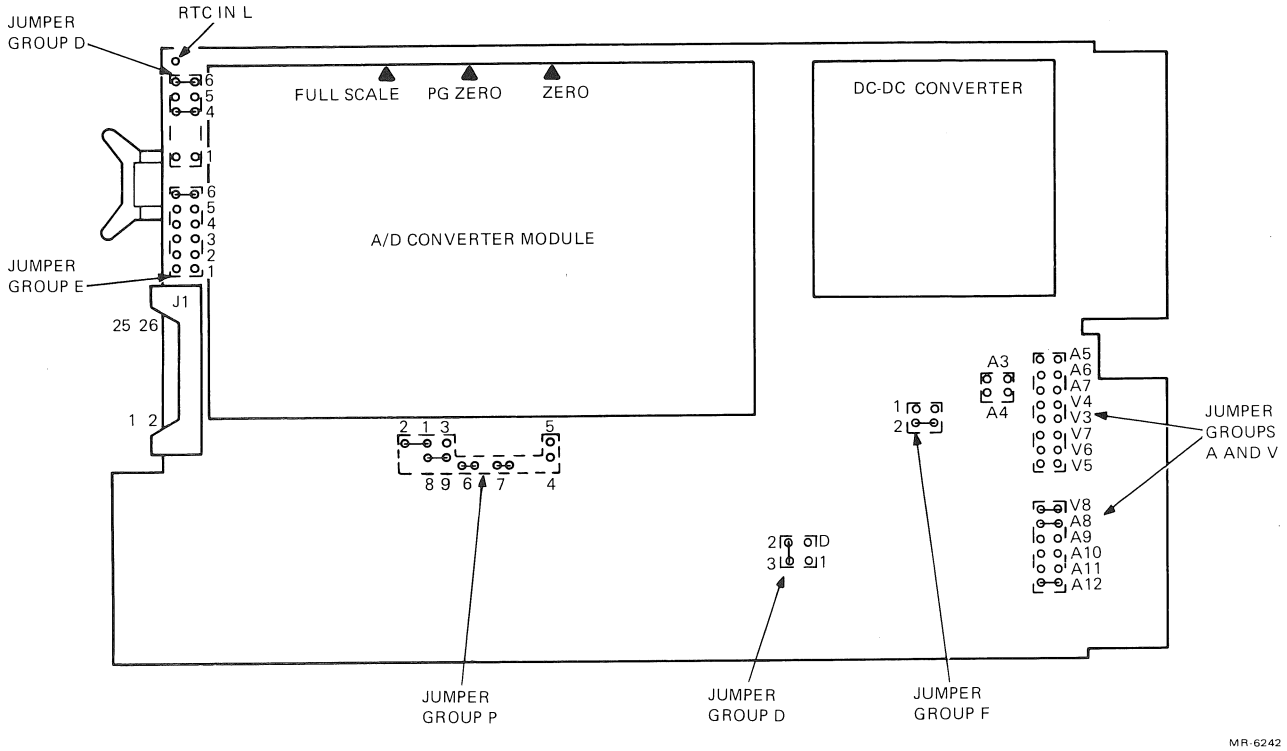


Figure 2-4 ADV11-C Physical Layout

There are two types of jumpers on the board. Some are point-to-point jumpers, in which each jumper pin has a unique number. A jumper is installed from one numbered pin to another. The other jumpers are pairs of pins. With each jumper type, a jumper wire is installed across a pair of pins.

This paragraph provides details on setting up the circuit board.

2.6.1 Selecting ADV11-C Device Address

The ADV11-C device address is the I/O address assigned to the A/D control/status register. The device address is selected by means of jumpers A3 through A12. (See jumper groups A and V in Figure 2-4). The jumpers allow the user to set the device address within the range of 160000_8 to 177770_8 in increments of 10_8. The device address is usually set at 170400_8, as shown in Figure 2-5. A jumper installed decodes a 1 in the corresponding bit position; a jumper out decodes a 0.

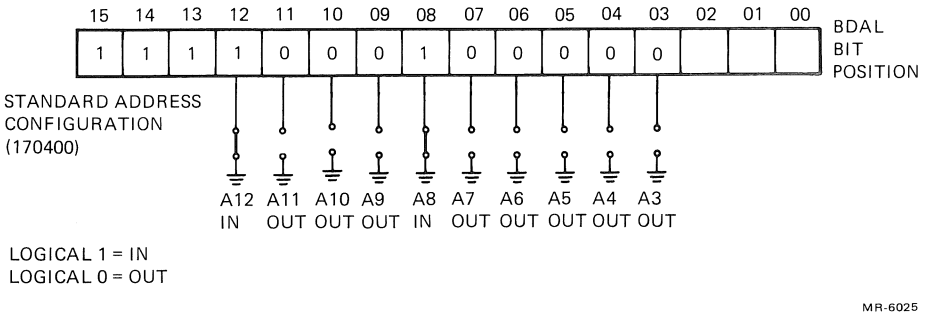


Figure 2-5 Selecting ADV11-C Device Address

2.6.2 Selecting ADV11-C Interrupt Vector Address

The ADV11-C is capable of generating two interrupt vectors to the LSI-11 processor. These interrupts, if enabled, occur when the A/D DONE bit or the ERROR bit is set in the CSR. The base interrupt vector address is assigned to A/D DONE. (The ERROR interrupt automatically is assigned the base interrupt vector address + 4.)

The base interrupt vector address can be set within the range of 0 to 770_8, in increments of 10_8. It is usually set to 400_8 by jumpers V3 through V8, as shown in Figure 2-6. (See jumper groups A and V in Figure 2-4).

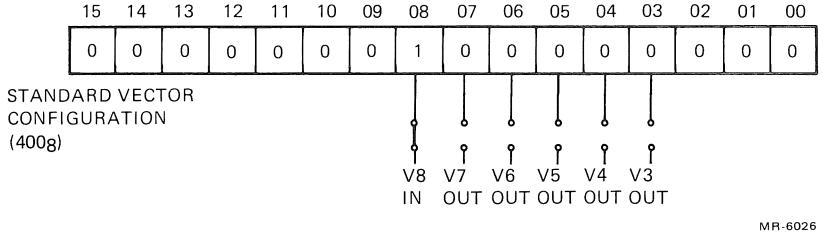


Figure 2-6 Selecting ADV11-C Interrupt Vector Address

2.6.3 Selecting ADV11-C Analog Input Range, Type, and Polarity

The ADV11-C allows software control over the full-scale range selection. The effective ranges provided by the programmable gain are as follows.

	Effective Input Range	
Gain	**Unipolar**	**Bipolar**
1	0 V to +10 V	±10 V
2	0 V to +5 V	±5 V
4	0 V to +2.5 V	±2.5 V
8	0 V to 1.25 V	±1.25 V

Table 2-4 shows the jumpers that must be installed to set up the analog input type. The board comes from the factory set for 16-channel single-ended, bipolar inputs. Refer to jumper group P in Figure 2-4.

Table 2-4 Selecting ADV11-C Analog Input Type

Input Type	Install Jumpers
Single-Ended Inputs*	P1 to P2; P8 to P9
Differential Inputs	P2 to P3; P4 to P5

*Factory configuration

NOTE
Jumpers P6 and P7 are factory installed for the programmable gain feature and should be left in.

2.6.4 Selecting ADV11-C A/D Output Data Notation

The ADV11-C allows the user to select the data notation to be used for the A/D output, as either binary, offset binary, or 2's complement notation. Table 2-5 shows the jumpers that must be installed to select the data notation. Refer to jumper groups D and E near the handle of the board, shown in Figure 2-4.

Table 2-5 Selecting A/D Output Data Notation

A/D Output Data Notation	Jumpers 1D	4D	5D	6D	5E	6E	Input Voltage	Output Code (Octal)
Binary	IN	OUT	OUT	IN	OUT	IN	+ full scale 0 V	007777 000000
Offset binary*	OUT	IN	OUT	IN	OUT	IN	+ full scale 0 V – full scale	007777 004000 000000
2's Complement	OUT	IN	IN	OUT	IN	OUT	+ full scale 0 V – full scale	003777 000000 174000

*Factory configuration

2.6.5 Selecting Source of External Trigger

The A/D conversions within the ADV11-C can be started in one of the following three ways.

1. Under program control, using the A/D START bit in the CSR.
2. By a real-time clock input at J1 pin 21 or at pin RTC IN.
3. By an external trigger, either at J1 pin 19 or at the BEVNT line on the LSI-11 bus.

The user can select the source of the external trigger using two jumpers on the board. (See jumper group F in Figure 2-4.) Table 2-6 shows the jumpers to install to select the source of the external trigger.

Table 2-6 Selecting ADV11-C External Trigger

External Trigger Source	Jumpers F1	Jumpers F2
BEVNT line (LSI-11 bus)	IN	OUT
EXT TRIG IN (J1 pin 19)*	OUT	IN

*Factory configuration

2.7 INTERFACING TO THE ADV11-C

Figure 2-4 shows the location of the I/O connector J1 on the ADV11-C. Analog input signals enter the board through this connector. Up to 16 single-ended analog inputs can be connected to J1 (CH 0–CH 15), or up to 8 differential analog inputs can be connected to J1 using CH 0–CH 7 and RETURN 0–7. A real-time clock input and an external trigger can also be connected to J1. Under program control, the clock or external trigger can be enabled to start an A/D conversion. The pin assignments for J1 are shown in Table 2-7.

The ADV11-C has two bus interface connectors that plug into the LSI-11 bus. These connectors have signals defined by LSI-11 bus specifications. Pin assignments and their functions are described in the *Microcomputer Interfaces Handbook*.

2.7.1 Single-Ended Inputs (16 Channels)

Single-ended analog inputs have one side of the user's analog source connected to the A/D converter amplifier and the other side connected to ground, as shown in Figure 2-7.

The benefit of single-ended inputs is that the user gets twice as many channels as in a differential input system. The disadvantage is the loss of the common mode rejection that is available with a differential system. Therefore, the recommended analog inputs are as follows.

- Input level: High, more than 1 V
- Input cable lengths: Short, less than 4.5 m (15 ft)

The user's source may be positioned some distance from the computer, and a voltage difference may occur between the user's source ground and the computer ground. This ground voltage difference (V_N) is included in the signal received by the A/D converter. To decrease this ground difference, plug the user's device into an ac receptacle as close as possible to the one providing power to the computer.

Table 2-7 ADV11-C Connector J1 Pin Assignments

Pin	Signal Name	Pin	Signal Name
1	CH 0	2	CH 8 or RETURN 0
3	CH 1	4	CH 9 or RETURN 1
5	CH 2	6	CH 10 or RETURN 2
7	CH 3	8	CH 11 or RETURN 3
9	CH 4	10	CH 12 or RETURN 4
11	CH 5	12	CH 13 or RETURN 5
13	CH 6	14	CH 14 or RETURN 6
15	CH 7	16	CH 15 or RETURN 7
17	A GND	18	AMP L
19	EXT TRIG IN L	20	D GND
21	RTC IN L	22	D GND
23	–	24	A/D REF
25	–	26	A/D REF

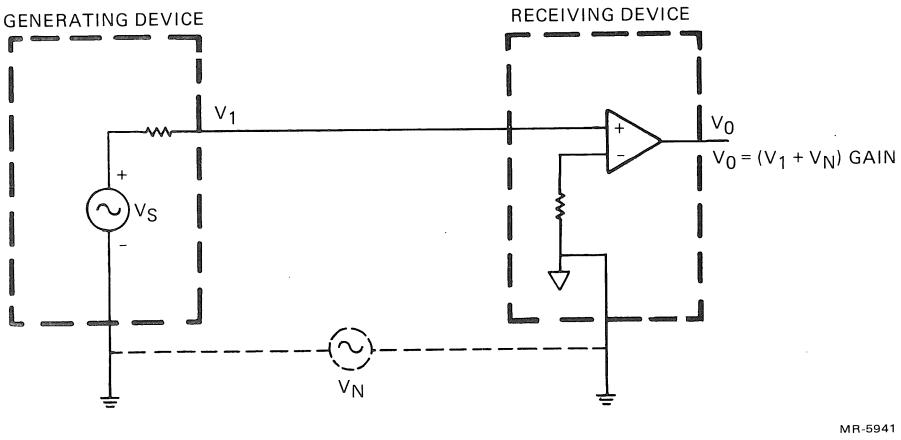


Figure 2-7 Single-Ended Analog Input

NOTE

Do not run a wire from the user's ground to the ADV11-C analog ground, as this wire forms a path for ground loop current that can affect the results on all input channels.

Floating input lines can be created by connecting the common side of the user's devices to the analog ground input on the ADV11-C (J1 pin 17). The ground point is shared among the channels. The signal return path from the A/D converter does not result in a current loop with the device ground.

2.7.2 Pseudo-Differential Inputs (16 Channels)

A pseudo-differential analog input system can be created by connecting all input sensors referenced to a common point, such as AMP L, as shown in Figure 2-8. This is possible because AMP L is an input at connector J1 (pin 18) for user connection. The input amplifier rejects the common mode noise. The recommended analog inputs are as follows.

- Input range: 100 mV to 10 V
- Input cable lengths: Less than 7.5 m (25 ft)

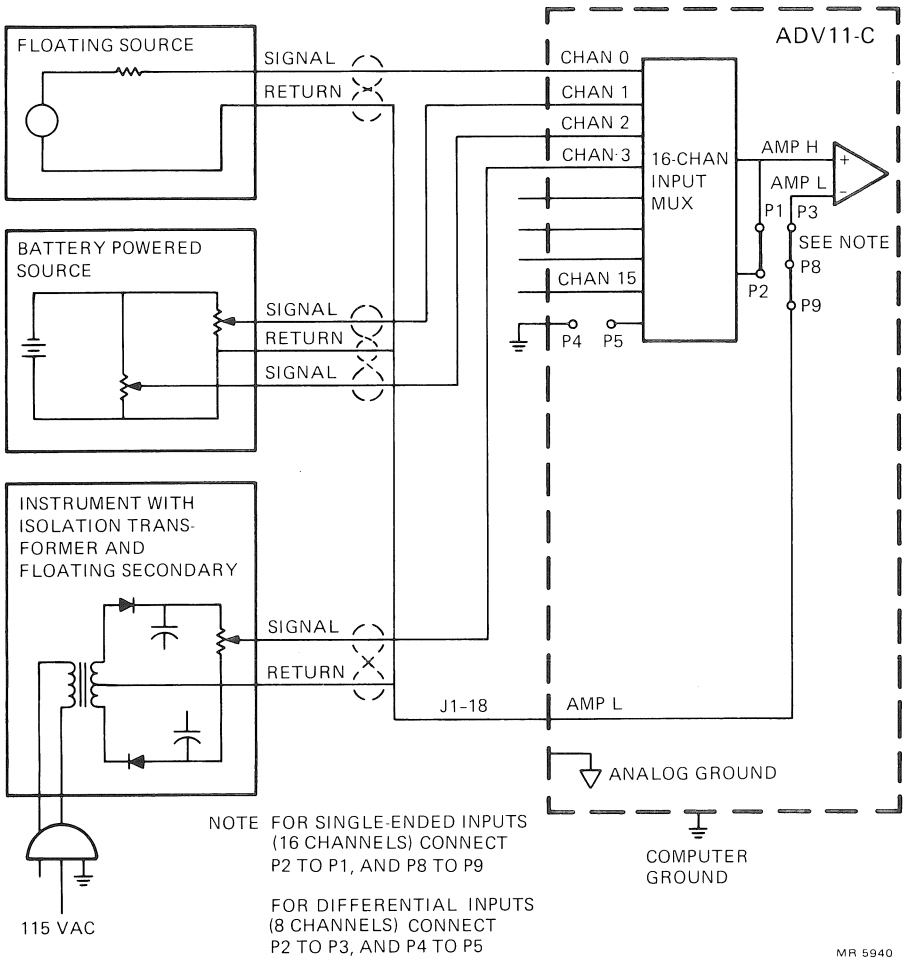


Figure 2-8 Pseudo-Differential Inputs

2.7.3 Differential Inputs (8 Channels)

Differential inputs have one side of the generating source connected to the positive (+) input of the A/D input amplifier and the other side of the source connected to the negative (−) input of the amplifier, as shown in Figure 2-9.

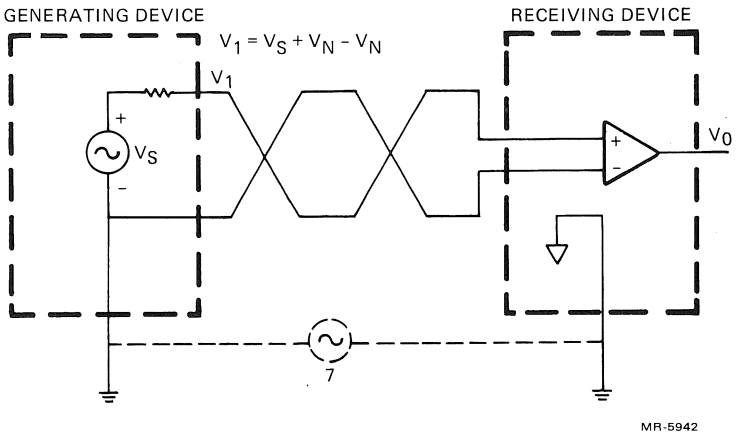


Figure 2-9 Differential Inputs

The benefit of differential inputs is that noise voltages appearing at the same time on both sides of the source are rejected by the A/D input amplifier. This is called common mode rejection, and provides a system with low noise. The amount of noise rejection is a ratio, the common mode rejection ratio (CMRR), given in decibels (dB). The CMRR for the ADV11-C is 80 dB at full-scale range. (See Paragraph 2.8.)

The disadvantage of differential inputs is that the number of available input channels is lowered by half.

The recommended analog inputs are as follows.

- Input range: 10 mV to 10 V
- Input cable length: As needed by user
- Cable type: Twisted-pair, shielded lines with low impedance

2.8 COMMON MODE REJECTION RATIO

The common mode rejection ratio is the ratio of the output voltage of the amplifier to the voltage that is common to both sides of its inputs. This ratio is given in units of decibels as follows.

$$\text{CMRR} = \text{dB} = 10 \text{ Log } \frac{V_{\text{in common mode}}}{V_{\text{out}} / \text{Gain}}$$

Example: An amplifier has a CMRR of 80 dB at a gain of 2. If the common mode voltage input is 5 V, the output voltage is computed as follows.

$$80 \text{ dB} = 10 \text{ Log } \frac{5 \text{ V}}{V_{\text{out}}/2}$$

$$\frac{80}{10} = \text{Log} \frac{10 \text{ V}}{V_{\text{out}}}$$

$$10^8 = \frac{10\ V}{V_{out}}$$

$$V_{out} = \frac{10\ V}{10^8} = .1 \times 10^{-6}\ V = .1\ \mu V$$

In the example, the noise common to both inputs to the amplifier is 5 V. The amplifier has a noise rejection CMRR of 80 dB. The noise level at its output is 0.1 μV.

2.9 PREVENTING FALSE SIGNALS

To get the best performance from an analog system, certain rules must be followed when connecting analog inputs to the system. This paragraph provides the rules and suggestions to get clean input signals and to lower the effects of electrical noise on the input amplifiers.

2.9.1 System Grounding

To provide a common reference potential, make sure that the computer's power supply ground is connected to the power line earth ground. DIGITAL supplies a standard grounding conductor with each memory and I/O cabinet.

Each DIGITAL computer system cabinet comes with ground terminals that should be connected to a low-impedance earth ground. The resistance from any metal surface or cabinet to the earth ground must not exceed 100 milliohms. To do this, use no. 4 AWG 5 mm (0.20 in) copper wire or stranded no. 4 AWG welding cable between the power supply ground and the power line earth ground.

Added information pertaining to selected grounding procedures is available in DEC Standard 002 or National Bureau of Underwriter bulletin NBFU No. 70.

2.9.2 Twisted-Pair Input Lines

The effects of magnetic coupling on the input signals can be decreased for floating single-ended or differential inputs by using twisted-pair input cables. The inductive noise on the two lines match, making the combined effect zero at the input to the ADV11-C.

With ground-referenced, single-ended inputs, the use of twisted-pair inputs has no effect.

2.9.3 Shielded Input Lines

The effects of electrostatic coupling on the input signals can be decreased by using shielded input cables. This is important if the device or source has high impedance. To prevent the shield from developing a ground loop and conducting current, connect it to ground at the source end only.

2.9.4 Allowing for Input Settling with High Source Impedance

Solid state multiplexers release a small charge to their input lines when changing channels. This can cause an error voltage when a new channel is selected. The ADV11-C allows for input settling to less than $\pm 1/2$ LSB, or approximately 9 μs. This time is usually enough for the charge to settle; however, more time may be needed when the multiplexer switches from an input channel with high source impedance, specifically when large capacitance occurs in the cables.

The product of the source impedance $\times$ cable shunt capacitance $= < 1\ \mu s$. Example: For a 1000 Ω source, the cable shunt capacitance should not exceed 1000 pF.

$(10^3\ \Omega \times 10^{-9}\ F = 10^{-6}\ s)$

If a twisted-pair cable has a shunt capacitance of 166 pF/m (50 pF/ft), then the maximum cable length from the 1000 Ω source should not exceed 6 m (20 ft). From a 100 Ω source, the cable length should not exceed 60 m (200 ft).

Settling time errors can be lowered greatly by increasing the time between conversions and adding a software delay between changing a channel and starting the A/D conversion.

2.9.5 Location in System

The ADV11-C board may be mounted in any available location in the system's backplane; however, the analog performance may be improved by installing the board away from the processor, memory boards, or noise-producing I/O boards. Note that no empty locations may occur in the backplane between the processor and any board that communicates with it.

CHAPTER 3
AAV11-C ANALOG OUTPUT BOARD

3.1 INTRODUCTION

The AAV11-C is an LSI-11 analog output printed circuit board, A6006, that has four digital-to-analog converters (DACs). The board also has bus interfacing circuits and control output circuits. A dc-dc converter converts from +5 V to ± 15 V to provide analog power.

Each DAC has a separate buffered register that provides 12-bit input data resolution. Each DAC register can be written or read in either word or byte format. Jumpers permit selection of the analog output voltage range for each register and its operating mode, either unipolar or bipolar. One of the registers, DAC D, also has four digital output bits for creating control signals to an analog device, such as a CRT.

3.2 FEATURES

The AAV11-C has the following features.

- Four D/A converter circuits.
- 12-bit digital input.
- Read/write, word or byte addressable registers.
- Unipolar or bipolar output.
- Binary input notation used for unipolar output; offset binary input notation used for bipolar output.
- Output voltage range selection of ±10 V or 0 V to +10 V.
- 4-bit digital output for control signals, such as CRT intensity, blank, unblank, erase.

3.3 AAV11-C SPECIFICATIONS

Identification	Dual-height module, A6006; part number 30-18691
Dimensions	13.16 cm × 21.6 cm (5.18 in × 8.5 in)
Power Requirements	+5 V ±5% @ 2.5 A
Bus Loads	
DC bus loads	1
AC bus loads	0.9
No. of D/A Converters	4
I/O Connector	20 pins; 3M no. 3421-7020

Digital Input	12 bits (binary encoded for unipolar output; offset binary for bipolar output)

Coding

Polarity	Input Code	Output Value
Unipolar	000000 =	+ Full scale
	007777 =	0 V
Bipolar	000000 =	+ Full scale
	004000 =	0 V
	007777 =	− Full scale

Digital Storage	4 separate read/write DAC registers for word or byte storage
Analog Output Voltage	±10 V @ 10 mA 0 V to 10 V @ 10 mA
Output Current	10 mA @ 10 V min
DC Output Impedance	0.5 Ω
Performance	
Linearity (0–10 V)	±1/2 LSB; ±1.2 mV at full-scale range
Differential linearity	±1/2 LSB
Offset error	Adjustable to zero
Offset drift	±15 ppm/°C max
Gain accuracy	Adjustable to (−) full-scale value
Gain drift	±30 ppm/°C max
Settling time	6 μs to 0.1% for a 20 V p–p output change
Environment	Ref: DEC Standard 102, Class C

3.4 AAV11-C FUNCTIONAL DESCRIPTION

Figure 3-1 shows a block diagram of the AAV11-C. It is addressable from the LSI-11 bus at its interface transceivers. An address switch pack determines the device address of the board. Setting the address switch pack is described in Paragraph 3.6.1.

When an address match occurs, DEV SEL H goes to the control logic and enables RDAL 00–02 to the control logic. These bits become SA 0–2 to select one of four DAC registers as follows.

Register Address	SA 0–2 02, 01, 00	Register Selected
170440	000	DAC A
170442	010	DAC B
170444	100	DAC C
170446	110	DAC D

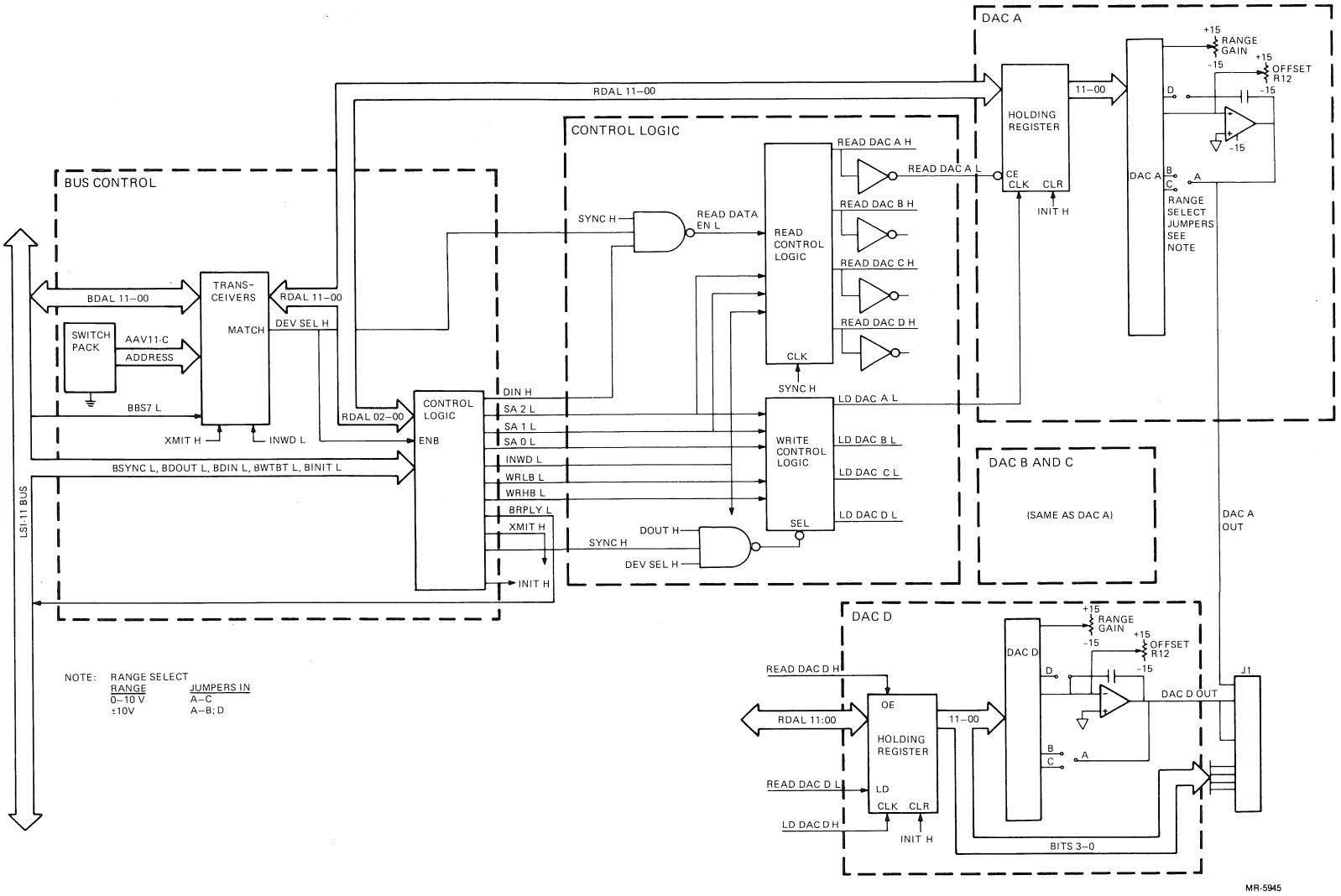


Figure 3-1 AAV11-C Functional Block Diagram

Binary data is written to these registers to be converted to an analog voltage. BDAL 00–11 becomes RDAL 00–11 within the AAV11-C. This is the input to the holding register of the DAC selected. LD DAC A, B, C, or D clocks the data into the DAC register.

DAC A, B, and C – Digital-to-analog conversions are performed in each of three DACs by identical circuits. (The fourth DAC is slightly different.) These three DACs have:

- A holding register to store the digital input.
- A DAC IC that generates a current to the input of an amplifier. The current is a function of the value in the holding register and the range select jumpers.
- An amplifier that changes its input current into a voltage proportional to its input.

Each DAC has an offset potentiometer to adjust the amplifier to negative full-scale range and a range gain potentiometer to adjust for positive full-scale range.

DAC D – DAC D is identical to DAC A, B, and C except that bits 0–3 from its holding register go to the I/O connector as well as to the DAC IC. These bits can be used for external equipment that needs control signals at programmable times. For example, these bits can be used for CRT intensity or erase signals.

Control signals in these bits will affect any D/A conversions that occur at the same time using DAC D.

3.5 PROGRAMMING THE AAV11-C

The AAV11-C has four addressable read/write registers. Each register is used by one of four digital-to-analog converters and can be addressed as one word or as two bytes, allowing complete use of the LSI-11 instruction set. The AAV11-C device address is the base address of the first register, usually 170440_8. The other registers are addressed in increments of 2_8 above the base address. Figure 3-2 shows the address decoding method of the AAV11-C.

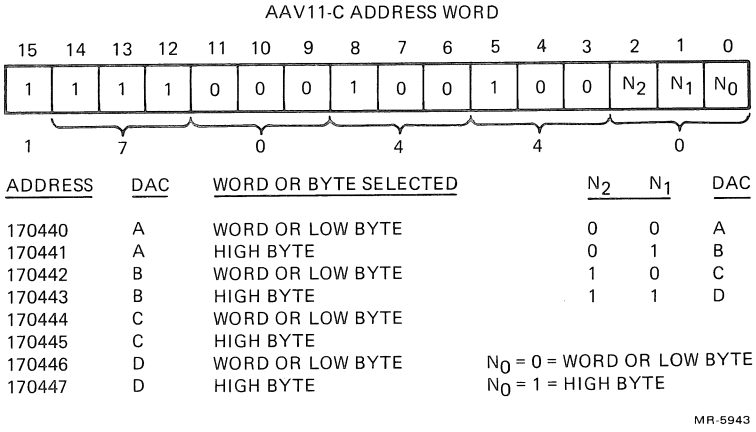


Figure 3-2 AAV11-C Address Decoding

The four registers of the AAV11-C are shown in Figure 3-3. Each register can be written or read as one word (bits 0–11) or as two bytes, bits 0–7 (low byte) and bits 8–11 (high byte). When the specific register is addressed, it forms the DAC DATA and controls the output of the board.

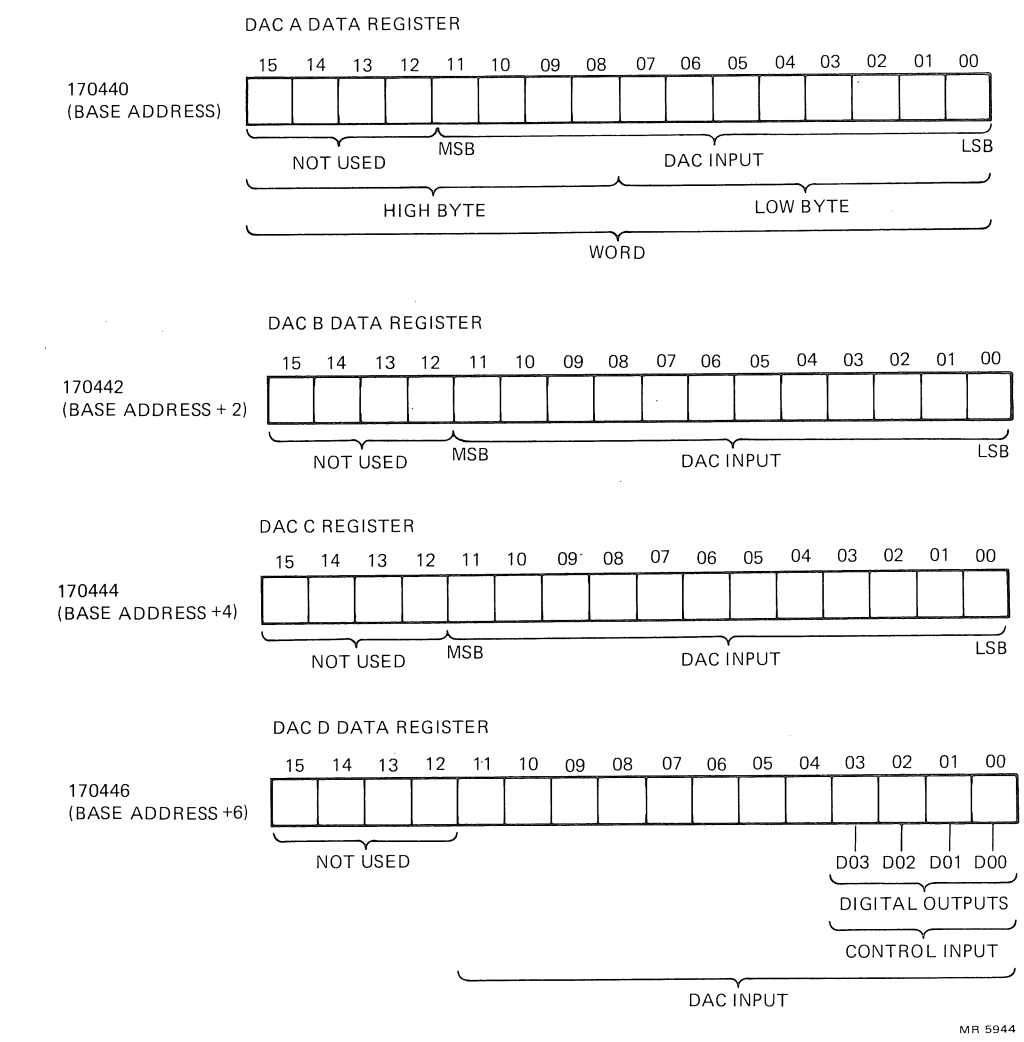


Figure 3-3 AAV11-C Four DAC Registers

The output of the board can be configured for either straight binary notation for unipolar operation or offset binary notation for bipolar operation. The expected output values are shown in Table 3-1.

The fourth DAC register has four bits that may be used for control signals. Bits 0–3 of this register are routed to the I/O connector on the board for use as CRT intensity, blank, erase, etc. Check the CRT installation manual to find out which bits are connected to the CRT inputs.

Control instructions in these four bit positions affect the output of any 12-bit D/A conversion that occurs on this register at the same time. However, because they use only the least significant bits of the word, the error is less than 0.5 percent of the full-scale value.

3.6 CONFIGURING THE AAV11-C

The AAV11-C, shown in Figure 3-4, has switches and two jumpers to set up the device address. The board also has jumpers to select the output voltage range for unipolar and bipolar operation. This paragraph provides details on setting up the circuit board.

Table 3-1 AAV11-C Data Notation and Output Values

Polarity	Notation	Input Code (Octal)	Output Value
Unipolar	Binary	000000	+ full scale (+9.9976 V)
		007777	0 V
Bipolar*	Offset binary	000000	+ full scale (9.9951 V)
		004000	0 V
		007777	− full scale (−10.000 V)

*Factory configuration

3.6.1 Selecting AAV11-C Device Address

The AAV11-C device address is the I/O address assigned to the first of the four DAC registers. The user selects the device address by means of a switch pack for address bits DAL 3–10 and two jumpers for bits DAL 11 and DAL 12. The device address can range from 160000_8 to 177770_8 in increments of 10_8. The device address is usually set at 170440_8, as shown in Figure 3-5. A switch in the ON position represents a 0; a switch in the OFF position represents a 1.

Jumper A11 is installed to place a 0 at address bit DAL 11. Jumper A12 is removed to place a 1 at address bit DAL 12.

3.6.2 Selecting AAV11-C Output Voltage Range

Each DAC on the AAV11-C has separate voltage range jumpers. These jumpers are found above their corresponding D/A converter IC on the printed circuit board. (See Figure 3-4.) When sent from the factory, the voltage range selected for all four DACs is bipolar ±10 V. Table 3-2 shows the jumpers to install to select the output voltage range.

3.6.3 DAC Calibration

Use the following procedure to calibrate the DAC registers. Refer to Table 3-1 for the designated values in the procedure.

1. Load the appropriate negative (−) full-scale code into the chosen DAC register.
2. Adjust the offset potentiometer for the correct − full-scale value.
3. Load the appropriate positive (+) full-scale code.
4. Adjust the range potentiometer for the correct + full-scale value.

Repeat the above procedure for other channels as required.

3.7 INTERFACING TO THE AAV11-C

Figure 3-4 shows the location of the connectors on the AAV11-C. DAC inputs and control signal inputs enter the board via the LSI-11 bus connectors. Pin assignments and their functions are described in the *Microcomputer Interfaces Handbook*.

Analog output voltages and digital control signals leave the board via the top edge connector J1. Table 3-3 shows the signal names on this connector. Each DAC has one output and a corresponding analog ground pin. The four least significant bits of DAC D (D00, D01, D02, and D03) are used for control signals to an analog device.

Figure 3-6 shows how the AAV11-C is connected to a device that uses differential analog inputs and one control input. Both the AAV11-C and the analog device must be set up for electrical compatibility. The device manual should define which pins to attach to the AAV11-C control bits. The software enables or disables the control bits.

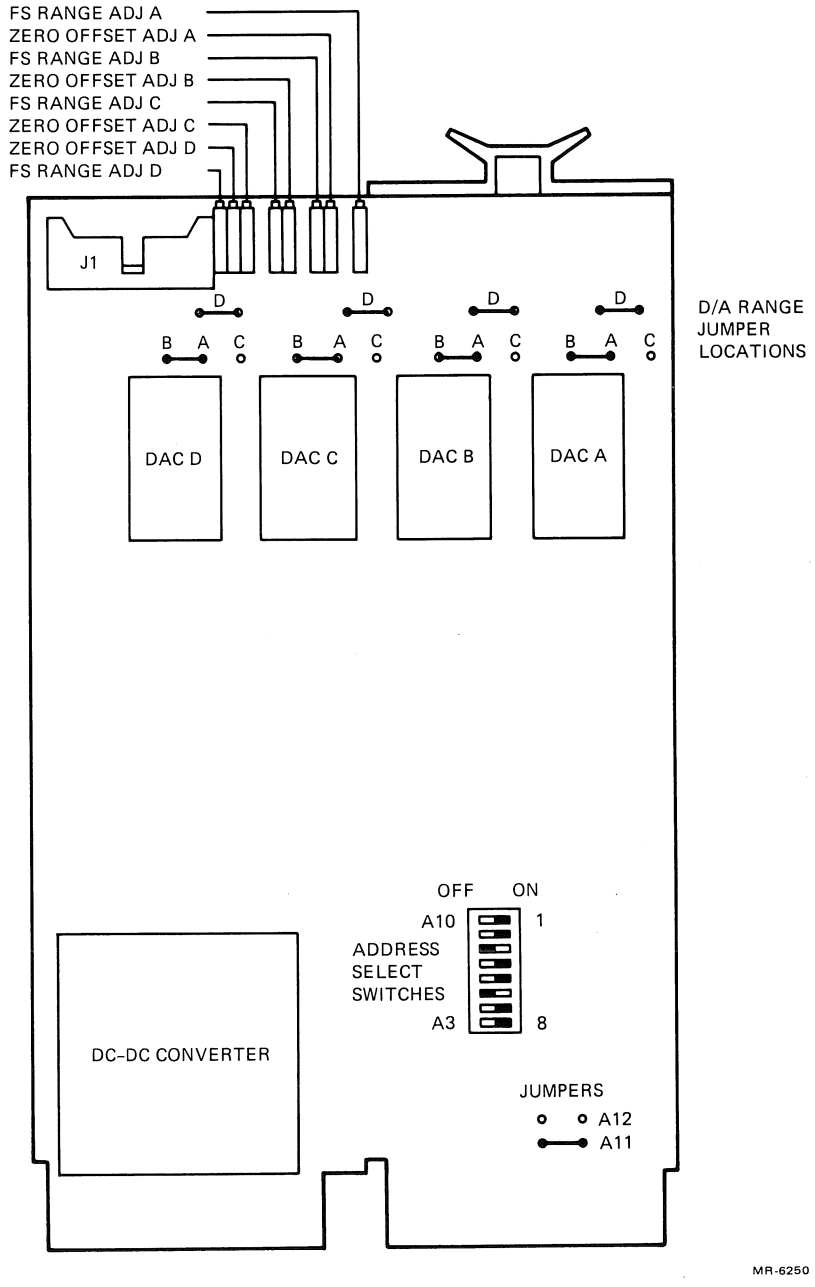


Figure 3-4 AAV11-C Physical Layout

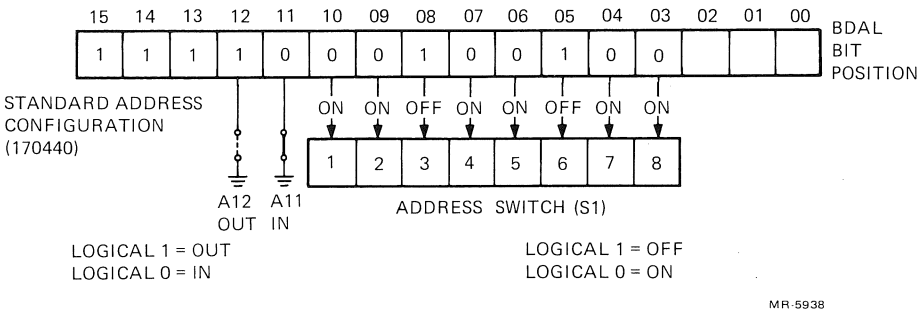


Figure 3-5 Selecting AAV11-C Device Address

Table 3-2 AAV11-C Output Voltage Range Jumpers

Polarity	Output Voltage Range	Install Jumpers
Unipolar	0 to +10 V	A to C
Bipolar*	±10 V	A to B; D

*Factory configuration

Table 3-3 AAV11-C Connector J1 Pin Assignments

Pin	Signal	Pin	Signal
1	D00 H	2	D GND
3	D01 H	4	D GND
5	D02 H	6	D GND
7	D03 H	8	D GND
9	–	10	–
11	A GND	12	A GND
13	DAC D OUT	14	A GND
15	DAC C OUT	16	A GND
17	DAC B OUT	18	A GND
19	DAC A OUT	20	A GND

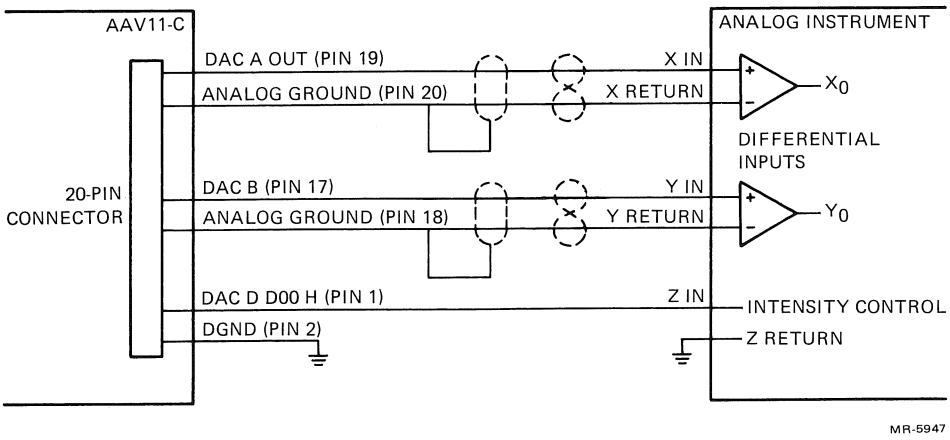


Figure 3-6 Connecting AAV11-C to a Differential Input Device

CHAPTER 4
AXV11-C ANALOG INPUT/OUTPUT BOARD

4.1 INTRODUCTION

The AXV11-C is an LSI-11 analog input/output printed circuit board, A0026. The board accepts up to 16 single-ended inputs, or up to 8 differential inputs, either unipolar or bipolar. A unipolar input can range from 0 V to +10 V. A bipolar input can range from −10 V to +10 V. The AXV11-C has a programmable gain on these inputs of 1, 2, 4, or 8 times the input voltage.

A/D conversions can be started by a program command, an external trigger, or a real-time clock input. The AXV11-C changes the analog input into digital data at its output. The digital data waits for a programmed data transfer to the LSI-11 processor or memory, or the AXV11-C puts an interrupt request on the LSI-11 bus and waits for the request to be acknowledged.

The AXV11-C also has two separate digital-to-analog converters (DACs). Each DAC has a write-only register that provides 12-bit input data resolution. On receiving the data, the AXV11-C changes the data to an analog output voltage.

4.2 FEATURES

The AXV11-C has the following features.

- 16 single-ended analog input channels or 8 differential analog input channels; SE/DI jumper is field-selectable.
- Programmable gain of 1, 2, 4, or 8.
- 12-bit output data resolution.
- Output data notation in binary, offset binary, or 2's complement format.
- A/D conversions can be started by a program, an external trigger, or a real-time clock.
- A/D results can be received by a programmed I/O transfer or by servicing an interrupt request.
- Common mode rejection ratio of 80 dB at maximum range.
- Two D/A converters (DACs).
- 12-bit digital input to each DAC.
- Each DAC has a unipolar or a bipolar output.
- Output voltage range selection of ±10 V or 0 V to 10 V.

4.3 AXV11-C SPECIFICATIONS

Identification	Dual-height module, A0026; part number 30-18689
Power Requirements	+5 V (±5%) @ 2.0 A
Bus Loads	
DC bus loads	1
AC bus loads	1.3
I/O Connector	26 pins; 3M no. 3399-7026
Analog Input	
No. of analog inputs	8 channels using differential inputs, or 16 channels using single-ended inputs
Input range	0 V to +10 V; −10 V to +10 V
Input gain (programmable)	**Gain (± 0.05%)** **Range**
	1 10 V 2 5 V 4 2.5 V 8 1.25 V
Maximum input signal	10.5 V (signal + common mode voltage)
Input impedance	
Off channels	100 MΩ in parallel with 10 pF max
On channels	100 MΩ in parallel with 100 pF max
Power off	1 kΩ in series with a diode
Input bias current	20 nA @ 25° C, max
Common mode rejection ratio	80 dB at 10 V full-scale range at 60 Hz
A/D Output	
Data buffer register	16-bit read-only output register
Resolution	12-bit unipolar; 11-bit bipolar plus sign
Data notation	Binary, offset binary, or 2's complement

A/D Output (Cont)

Coding

Notation Used	Full-Scale Input Voltage	Output Code (Octal)
Binary	+9.9976 V	007777
	0.0000 V	000000
Offset binary	+9.9951 V	007777
	0.0000 V	004000
	−10.0000 V	000000
2's complement	+9.9951 V	003777
	0.0000 V	000000
	−10.0000 V	174000

Sample and Hold Amplifier

Aperture uncertainty	Less than 10 ns
Aperture delay	Less than 0.5 μs from start of conversion to signal disconnect.
Front end settling	Less than 15 μs to ±0.01% of full-scale value for a 20 V p–p input
Input noise	Less than 0.2 mV rms

A/D Converter Performance

Linearity	±1/2 LSB
Stability (temperature coefficient)	±30 ppm/°C
Stabliity, long-term	±0.05% change per 6 months
Conversion time	25 μs from end of front end settling to setting the A/D DONE bit
System throughput	25K channel samples per second

D/A Converter Specifications

No. of D/A converters	2
Digital input	12 bits (Binary code is used for unipolar output; offset binary or 2's complement code is used for bipolar output.)
Analog output	±10 V or 0 V to +10 V
Output current	±5 mA max
Output impedance	0.1 Ω

D/A Converter Specifications (Cont)

Differential linearity	±1/2 LSB
Non-linearity	0.02% of full-scale value
Offset error	Adjustable to zero
Offset drift	±30 ppm/°C max
Gain accuracy	Adjustable to full-scale value
Gain drift	±30 ppm/°C max
Settling time	65 μs to 0.1% for a 20 V p–p output change
Noise	0.1% full-scale value
Capacitive load capability	0.5 μf

Environment
(Per DEC Standard 102, Class C)

Temperature, operating*	5° C to 60° C (41° F to 140° F)
Temperature, not operating	−40° C to 66° C (−40° F to 150° F)
Relative humidity, operating	10% to 95% with max wet bulb of 32° C (90° F) and min dew point of 2° C (35° F) not condensing
Altitude, operating	2.4 km (8,000 ft) max
Altitude, not operating	9.1 km (30,000 ft)

4.4 AXV11-C FUNCTIONAL DESCRIPTION

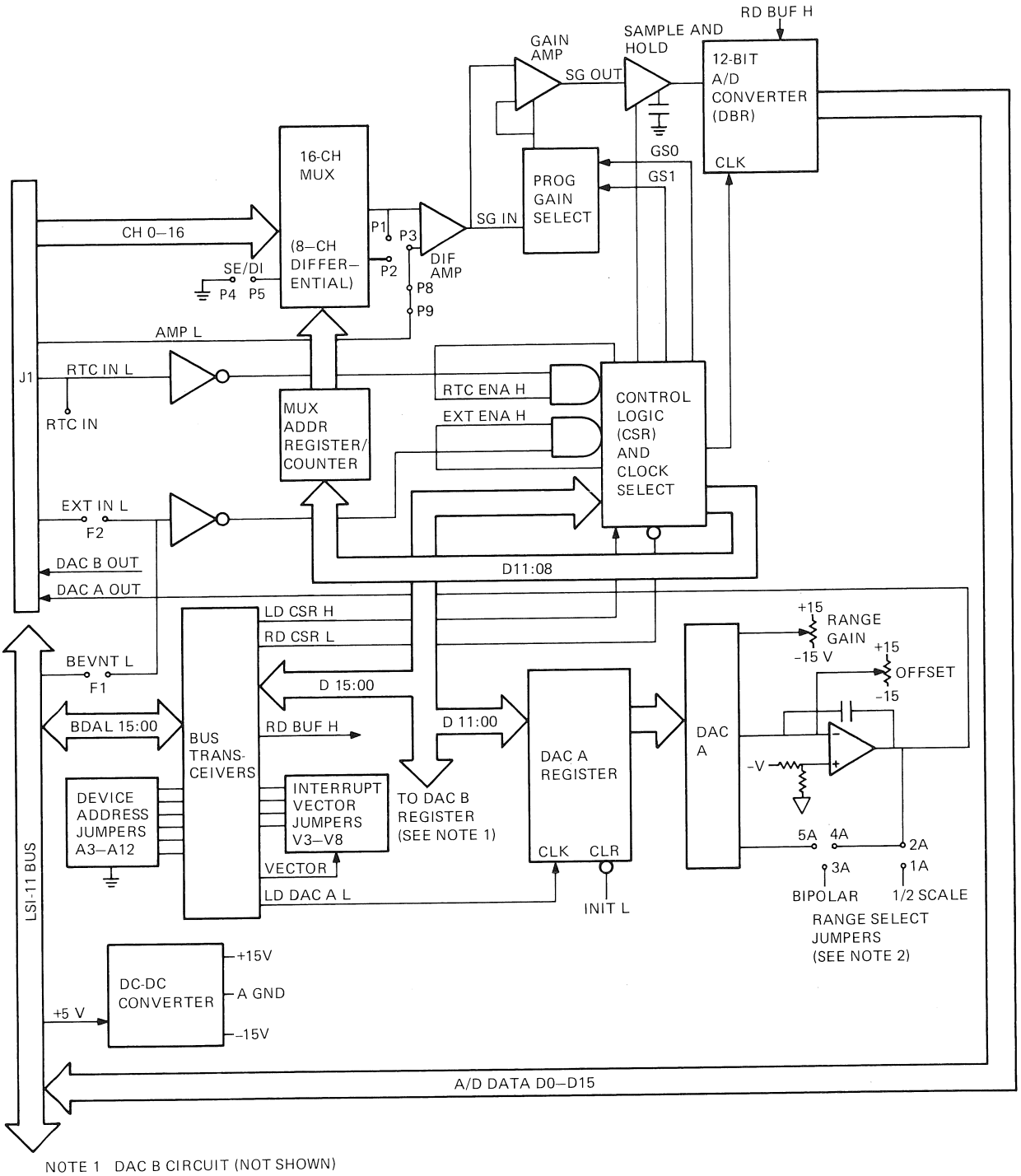
Figure 4-1 shows a block diagram of the AXV11-C. The board has jumpers to select its device address. It has four addressable registers: the control/status register (CSR), the data buffer register (DBR), DAC A register, and DAC B register. The board also has jumpers to select the base interrupt vector address. The AXV11-C has two interrupt vectors. One is enabled when A/D DONE is set in the CSR; the other may be enabled for an ERROR set in the CSR.

4.4.1 A/D Conversion

When the AXV11-C is addressed, the transceivers send the instruction from the LSI-11 processor to the CSR. The instruction selects 1 of 16 channels, determines the gain selected, and determines how the board will start the analog conversion. Jumpers determine if singled-ended or differential inputs are to be used. (See Paragraph 4.6.3.)

An analog conversion can be started by a real-time clock, by an external trigger, or under program control by setting the A/D START bit in the CSR. CSR bit 5 enables the real-time clock input; CSR bit 4 enables the external trigger input. Two jumpers (F2, F1) on the board determine whether the external trigger comes from the I/O connector (J1) or from the LSI-11 bus event line (BEVNT L).

*Lower the maximum operating temperature 1.8° C for each 1000 m above sea level (or 1° F for each 1000 ft above sea level).



NOTE 1 DAC B CIRCUIT (NOT SHOWN) IS THE SAME AS DAC A CIRCUIT

NOTE 2 RANGE SELECT JUMPERS

RANGE	DAC A JUMPERS	DAC B JUMPERS
± 10 V	3A–5A	1B–5B
0–10 V	1A–2A	2B–3B

Figure 4-1 AXV11-C Functional Block Diagram

The output of the multiplexer goes to a differential amplifier then to a programmable gain amplifier. The gain is set in the CSR with bits 2 and 3 (GS0 and GS1). The gain may be selected as 1, 2, 4, or 8 times the input voltage.

The output of the programmable gain amplifier goes to a sample and hold amplifier. The amplifier continuously samples the analog signal while waiting for the A/D START bit in the CSR, for a real-time clock input, or for an external trigger input. When one of these inputs has been received, the sample and hold amplifier changes to "hold" and the 12-bit A/D converter digitizes the held analog voltage.

When the A/D conversion is complete, the A/D DONE bit is set in the CSR and the sample and hold amplifier returns to sampling. If the DONE INT ENABLE bit is also set, an interrupt occurs to the LSI-11 bus. The contents of the 12-bit A/D converter is read by reading the A/D data buffer register (DBR).

4.4.2 D/A Conversion

The DAC register input data is addressed on the LSI-11 bus as follows.

Register	Address	Signal Generated
DAC A	base address + 4	SEL 4 L
DAC B	base address + 6	SEL 6 L

The signals SEL 4 L and SEL 6 L create LD DAC A and LD DAC B, respectively, to load either DAC A or DAC B. The digital data from the LSI-11 bus goes to the bus transceivers, then into the selected DAC register. Once the register is loaded, the digital-to-analog conversion takes place. The DAC IC generates a current to the input of an amplifier. The current is a function of the value in the register. (A zero offset adjustment is made at the input to this amplifier.)

The amplifier converts the current to a voltage proportional to its input, with its maximum range selected by jumpers. (A trim pot provides adjustment to full-scale range.) The voltage is then amplified to become DAC A OUT or DAC B OUT at the I/O connector J1.

4.5 PROGRAMMING THE AXV11-C

The AXV11-C has four programmable registers.

Register	Read or Write	Standard Address
Control/status register	Read/write	170400
Data buffer register	Read only	170402
DAC A register	Write only	170404
DAC B register	Write only	170406

This paragraph describes setting the mode of operation, defines the standard device address and vector address, and defines the bits in each register.

4.5.1 Selecting AXV11-C Mode of Operation

The user determines the AXV11-C mode of operation. The user selects how the A/D conversions are to start and how the digital data is transferred to the LSI-11 processor.

Starting an A/D Conversion – An A/D conversion can be started in one of the following three ways.

1. Real-time clock input: set bit 5 in CSR.
2. External trigger enable: set bit 4 in CSR.
3. A/D START bit: set bit 0 in CSR.

Transferring A/D Data to LSI-11 Processor – The digital data can be transferred to the LSI-11 processor or memory by a programmed I/O transfer or by servicing an interrupt request. Using LSI-11 instructions, a programmed I/O transfer can write the CSR in the AXV11-C, read the CSR and wait for an A/D DONE bit (bit 7), then read the DBR to get the A/D data.

If interrupts are used, set the DONE INT ENABLE bit (bit 6) of the CSR. When the A/D conversion is complete, the A/D DONE bit (bit 7) sets, and an interrupt occurs to the LSI-11 processor. The processor services the interrupt request and gets the A/D data. After receiving the data, the software clears the A/D DONE bit in the AXV11-C's CSR.

An interrupt may also be programmed to occur on an error condition by setting bit 14 in the CSR.

4.5.2 AXV11-C Standard Device Address

The AXV11-C permits assigning a device address between 160000_8 and 177770_8. The standard device address is 170400_8. This is the starting address for the AXV11-C registers. The control/status register (CSR) receives this first address; the A/D data buffer register automatically receives the starting address + 2, or 170402_8. The DAC A register receives the starting address + 4, and the DAC B register receives the starting address + 6. Table 4-1 shows the AXV11-C standard address and vector address assignments. See Paragraph 4.6.1 to change the device address.

Table 4-1 AXV11-C Standard Address Assignments

Description	Mnemonic	First Module Address	Second Module Address
Registers			
Control/Status	CSR	170400	170420
Data Buffer	DBR	170402	170422
DAC A	DAA	170404	170424
DAC B	DAB	170406	170426
Interrupt Vectors			
A/D DONE		400	410
ERROR		404	414

4.5.3 AXV11-C Standard Interrupt Vector Address

The interrupt vector can be assigned between 0 and 770_8 in increments of 10_8. The standard base interrupt vector for the AXV11-C is 400_8. This vector is assigned to the A/D DONE interrupt request. If the DONE INT ENABLE bit (bit 6) is set in the CSR, the A/D DONE bit (bit 7) generates an interrupt request to the LSI-11 processor. When the request is acknowledged by the LSI-11 processor, it starts the interrupt service routine at address 400 in its I/O page.

The AXV11-C can also interrupt on an error. The error interrupt request is automatically assigned the base vector address + 4, or 404_8. If the ERROR INT ENABLE bit (bit 14) is set in the CSR by the program, an interrupt request will occur at the occurrence of any error (bit 15 set).

The standard interrupt vector addresses are shown in Table 4-1. See Paragraph 4.6.2 to change the base interrupt vector address.

4.5.4 Control/Status Register (CSR)

The control/status register is a read/write register, shown in Figure 4-2. A control instruction is written into the CSR; the A/D status is read from the CSR. Table 4-2 defines the bits of the CSR.

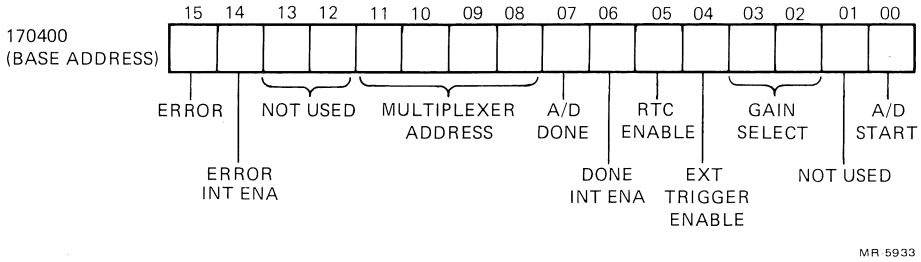


Figure 4-2 AXV11-C Control/Status Register (Read/Write)

Table 4-2 AXV11-C Control/Status Register Bit Assignments

Bit	Name	Description
0	A/D START	Write Only – When set this bit starts an A/D conversion. This bit is cleared by internal logic after starting conversion. It always reads back 0.
1	Not used	
2, 3	GAIN SELECT	Read/Write – Set these bits to select the gain for the analog input as follows. **Gain** / **GS1 (bit 3)** / **GS0 (bit 2)** 1 / 0 / 0 2 / 0 / 1 4 / 1 / 0 8 / 1 / 1
4	EXT TRIG ENABLE	Read/Write – When set this bit allows an external trigger to start an A/D conversion.
5	RTC ENABLE	Read/Write – When set this bit allows a real-time clock input to start an A/D conversion.
6	DONE INTERRUPT ENABLE	Read/Write – When set this bit enables an interrupt on A/D DONE (bit 7). Both bits are cleared by INIT.
7	A/D DONE	Read Only – This bit is set at the end of an A/D conversion and is reset by reading the A/D data buffer register.
8–11	MULTIPLEXER ADDRESS	Read/Write – These bits select 1 of 16 analog input channels.
12–13	Not used	
14	ERROR INTERRUPT ENABLE	Read/Write – When set this bit enables an interrupt on an ERROR (bit 15). Both bits are cleared by INIT.

Table 4-2 AXV11-C Control/Status Register Bit Assignments (Cont)

Bit	Name	Description
15	ERROR	Read/Write – When set this bit indicates that an error has occurred due to one of the following. • Trying an external start or clock start during multiplexer settling time. • Trying a start while an A/D conversion is in process. • Trying any start while the A/D DONE bit is set. This bit can be cleared by writing the CSR or by an INIT.

4.5.5 Data Buffer Register (DBR)

The data buffer register is a read-only register that holds the digital data after the A/D conversion is complete. The DBR can be read after the A/D DONE bit is set in the CSR. Figure 4-3 shows the format for the DBR; Table 4-3 defines its bits.

The DBR is cleared after reading the register or on initializing the LSI-11 bus.

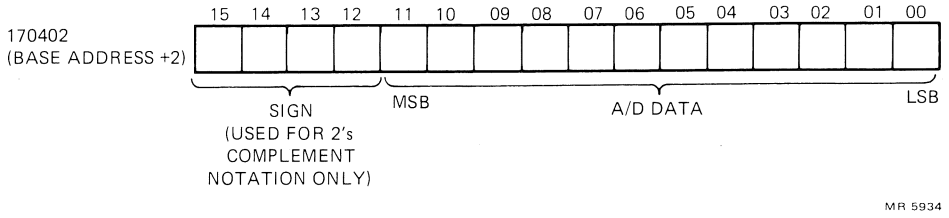


Figure 4-3 AXV11-C Data Buffer Register (Read Only)

Table 4-3 AXV11-C Data Buffer Register Bit Assignments

Bit	Name	Description
0–11	A/D DATA	These bits hold the parallel digital outputs after completion of the A/D conversion in one of the following data notations. • binary • offset binary • 2's complement The user selects the data notation; see Paragraph 4.6.4.
12–15	SIGN	These bits are the sign for the bipolar inputs when using 2's complement notation. These bits are not used for binary or offset binary notation.

4.5.6 DAC A and DAC B Registers

DAC A register and DAC B register are 12-bit write-only registers. They are loaded from the LSI-11 bus with digital data to be changed to an analog voltage. Figure 4-4 shows the format for each register. Each DAC responds immediately to the data word placed in its register. Each register holds its last value until it is written again or power is turned off.

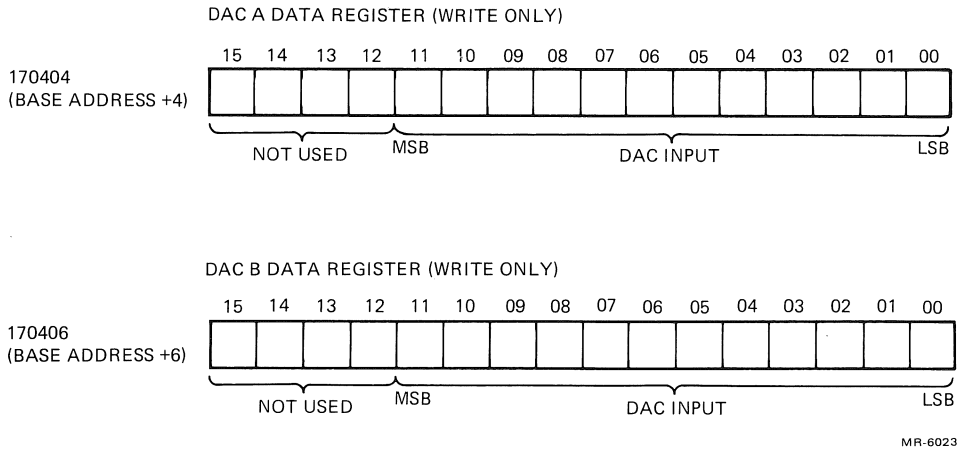


Figure 4-4 AXV11-C DAC A and DAC B Registers

The user may select the format of the input data and output range and polarity. However, both registers must use the same input data notation – binary, offset binary, or 2's complement format. The output ranges can be ±10 V or 0 V to +10 V. The two registers must use the same polarity. Table 4-4 shows the expected output of the DAC for the selected input. See Paragraph 4.6.3 to set up each of these registers.

Table 4-4 AXV11-C DAC Input and Output Values

Polarity	Input Data Notation	Input Code (Octal)	Output Voltage
Unipolar	Binary	007777 000000	+ full scale 0 V
Bipolar	Offset binary*	007777 004000 000000	+ full scale 0 V – full scale
Bipolar	2's complement	003777 000000 174000	+ full scale 0 V – full scale

*Factory configuration

4.6 CONFIGURING THE AXV11-C

The AXV11-C, shown in Figure 4-5, has jumpers to set up the device address, the interrupt vector address, the analog configuration, and the DAC configuration. The user may select the A/D input range, polarity, and the output data notation. The user may select the D/A input data notation, output range, and polarity of each DAC.

There are two types of jumpers on the board. Some are point-to-point jumpers, in which each jumper pin has a unique number. A jumper is installed from one numbered pin to another. The other jumpers are pairs of jumper pins. With each jumper type, a jumper wire is installed across a pair of pins.

This paragraph provides details on setting up the circuit board.

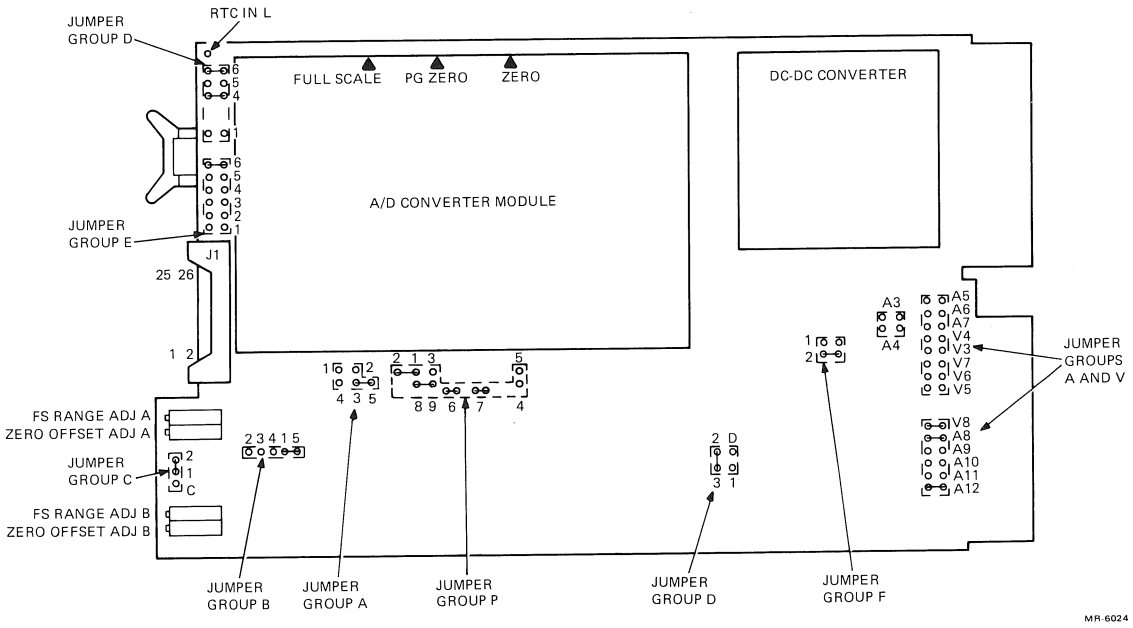


Figure 4-5 AXV11-C Physical Layout

4.6.1 Selecting AXV11-C Device Address

The AXV11-C device address is the I/O address assigned to the control/status register. The device address is selected by means of jumpers A3 through A12. (See jumper groups A and V in Figure 4-5.) The jumpers allow the user to set the device address within the range of 160000_8 to 177770_8. The device address is usually set at 170400_8, as shown in Figure 4-6. A jumper installed decodes a 1 in the corresponding bit position; a jumper out decodes a 0.

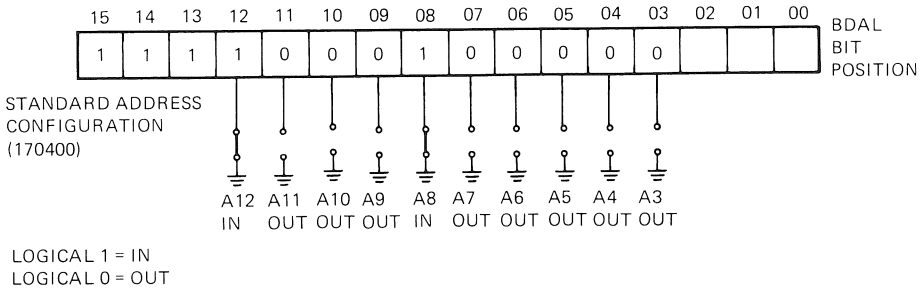


Figure 4-6 Selecting AXV11-C Device Address

4.6.2 Selecting AXV11-C Interrupt Vector Address

The AXV11-C is capable of generating two interrupt vectors to the LSI-11 processor. These interrupts, if enabled, occur when the A/D DONE bit or the ERROR bit is set in the CSR. The base interrupt vector address is assigned to A/D DONE. (The ERROR interrupt automatically is assigned the base interrupt vector address + 4.)

The base interrupt vector address can be set within the range of 0 to 770_8, in increments of 10_8. It is usually set to 400_8 by jumpers V3 through V8, as shown in Figure 4-7. (See jumper groups A and V in Figure 4-5.)

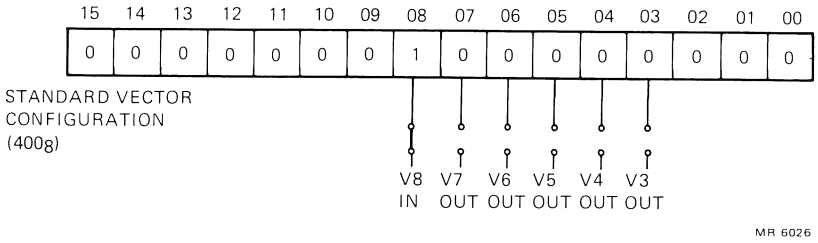


Figure 4-7 Selecting AXV11-C Interrupt Vector Address

4.6.3 Selecting AXV11-C Analog Input Range, Type, and Polarity

The AXV11-C allows software control over the full-scale range selection. The effective ranges provided by the programmable gain are as follows.

Effective Input Range

Gain	Unipolar	Bipolar
1	0 V to +10 V	±10 V
2	0 V to +5 V	±5 V
4	0 V to +2.5 V	±2.5 V
8	0 V to ±1.25 V	±1.25 V

Table 4-5 shows the jumpers that must be installed to set up the analog input type. The board comes from the factory set for 16-channel single-ended, bipolar inputs. Refer to jumper group P in Figure 4-5.

Table 4-5 Selecting AXV11-C Analog Input Type

Input Type	Install Jumpers
Single-Ended Inputs*	P1 to P2; P8 to P9
Differential Inputs	P2 to P3; P4 to P5

*Factory configuration

NOTE

Jumpers P6 and P7 are factory installed for the programmable gain feature and should be left in.

4.6.4 Selecting AXV11-C A/D Output Data Notation

The AXV11-C allows the user to select the data notation to be used for the A/D output, as either binary, offset binary, or 2's complement notation. Table 4-6 shows the jumpers that must be installed to select the data notation. Refer to jumper groups D and E near the handle of the board, shown in Figure 4-5.

4.6.5 Selecting Source of External Trigger

The A/D conversions within the AXV11-C can be started in one of the following three ways.

1. Under program control using the A/D START bit in the CSR.
2. By a real-time clock input at J1 pin 21 or at pin RTC IN.
3. By an external trigger, either at J1 pin 19 or at the BEVNT line on the LSI-11 bus.

The user can select the source of the external trigger using two jumpers on the board. (See jumper group F in Figure 4-5.) Table 4-7 shows the jumpers to install to select the source of the external trigger. (Jumper C1 to C2 should always be installed.)

Table 4-6 Selecting A/D Output Data Notation

A/D Output Data Notation	Jumpers 1D	4D	5D	6D	5E	6E	Input Voltage	Output Code (Octal)
Binary	IN	OUT	OUT	IN	OUT	IN	+ full scale 0 V	007777 000000
Offset binary*	OUT	IN	OUT	IN	OUT	IN	+ full scale 0 V – full scale	007777 004000 000000
2's Complement	OUT	IN	IN	OUT	IN	OUT	+ full scale 0 V – full scale	003777 000000 174000

*Factory configuration

Table 4-7 Selecting AXV11-C External Trigger

External Trigger Source	Jumpers F1	F2
BEVNT line (LSI-11 bus)	IN	OUT
EXT TRIG IN (J1 pin 19)*	OUT	IN

*Factory configuration

4.6.6 Selecting AXV11-C D/A Configuration

The user can select the input data notation and the output voltage range for the two D/A converters on the AXV11-C. DAC A and DAC B can be configured for different polarities; however, the input data notation selected and the output polarity selected must be the same for each DAC. Refer to Table 4-8 to set up DAC A; refer to Table 4-9 to set up DAC B. Jumper groups A, B, and D for the DACs are found below the A/D converter module, shown in Figure 4-5.

Table 4-8 Selecting DAC A Jumper Configuration

Range and Polarity	D/A Input Data Notation		
	Binary	Offset Binary	2's Complement
±10 V	N/A (not applicable)	3A to 5A* ~~D2 to D3~~ D1 to D3	3A to 5A ~~D1 to D3~~ D1 to D2
0 to +10 V	1A to 2A ~~D2 to D3~~ D1 to D3	N/A	N/A

*Factory configuration

Table 4-9 Selecting DAC B Jumper Configuration

Range and Polarity	D/A Input Data Notation		
	Binary	Offset Binary	2's Complement
±10 V	N/A (not applicable)	1B to 5B* ~~D2 to D3~~ D1 to D3	1B to 5B ~~D1 to D3~~ D1 to D2
0 to +10 V	2B to 3B ~~D2 to D3~~ D1 to D3	N/A	N/A

*Factory configuration

4.7 INTERFACING TO THE AXV11-C

Figure 4-5 shows the location of the I/O connector J1 on the AXV11-C. Analog input signals enter the board through this connector, and DAC output signals leave through this connector. Up to 16 single-ended analog inputs can be connected to J1 (CH 0–CH 15), or up to 8 differential analog inputs can be connected to J1 using CH 0–CH 7 and RETURN 0–7. A real-time clock input and an external trigger can also be connected to J1. Under program control, these two inputs can be enabled to start an A/D conversion. The pin assignments for J1 are shown in Table 4-10.

RTC IN has a separate pin, found near the printed circuit board handle, for easy installation of a wire jumper from a clock board, such as the KWV11-C CLK OVFL tab.

The AXV11-C has two bus interface connectors that plug into the LSI-11 bus. These connectors have signals defined by LSI-11 bus specifications. Pin assignments and their functions are described in the *Microcomputer Interfaces Handbook*.

Table 4-10 AXV11-C Connector J1 Pin Assignments

Pin	Signal Name	Pin	Signal Name
1	CH 0	2	CH 8 or RETURN 0
3	CH 1	4	CH 9 or RETURN 1
5	CH 2	6	CH 10 or RETURN 2
7	CH 3	8	CH 11 or RETURN 3
9	CH 4	10	CH 12 or RETURN 4
11	CH 5	12	CH 13 or RETURN 5
13	CH 6	14	CH 14 or RETURN 6
15	CH 7	16	CH 15 or RETURN 7
17	A GND	18	AMP L
19	EXT TRIG IN L	20	D GND
21	RTC IN L	22	D GND
23	DAC A RETURN	24	DAC A OUT
25	DAC B RETURN	26	DAC B OUT

4.7.1 Single-Ended Inputs (16 Channels)

Single-ended analog inputs have one side of the user's analog source connected to the A/D converter amplifier and the other side connected to ground, as shown in Figure 4-8.

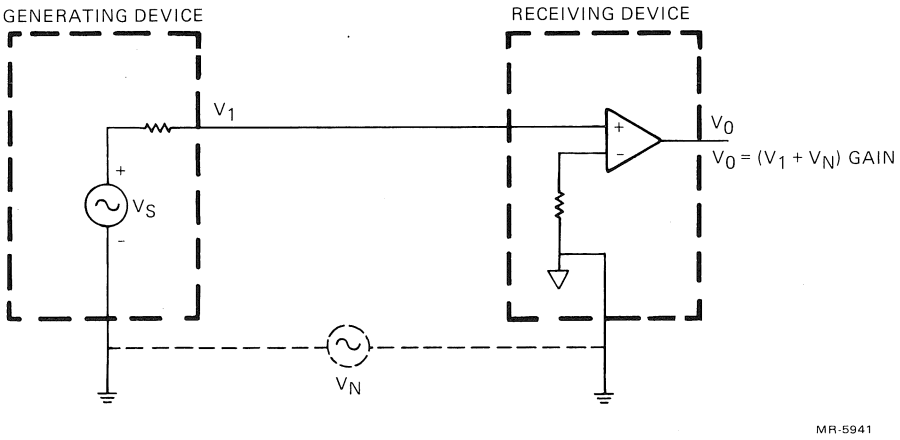


Figure 4-8 Single-Ended Analog Input

The benefit of single-ended inputs is that the user gets twice as many channels as with a differential input system. The disadvantage is the loss of the common mode rejection that is available with a differential system. Therefore, the recommended analog inputs are as follows.

- Input level: High, more than 1 V
- Input cable lengths: Short, less than 4.5 m (15 ft)

The user's source may be positioned some distance from the computer, and a voltage difference may occur between the user's source ground and the computer ground. This ground voltage difference (V_N) is included in the signal received by the A/D converter. To decrease this ground difference, plug the user's device into an ac receptacle as close as possible to the one providing power to the computer.

NOTE

Do not run a wire from the user's ground to the AXV11-C analog ground, as this wire forms a path for ground loop current that can affect the results on all input channels.

Floating input lines can be created by connecting the common side of the user's devices to the analog ground input on the AXV11-C (J1 pin 17). The ground point is shared among the channels. The signal return path from the A/D converter does not result in a current loop with the device ground.

4.7.2 Pseudo-Differential Inputs (16 Channels)

A pseudo-differential analog input system can be created by connecting all input sensors referenced to a common point, such as AMP L, as shown in Figure 4-9. This is possible because AMP L is an input at connector J1 (pin 18) for user connection. The input amplifier rejects the common mode noise. The recommended analog inputs are as follows.

- Input range: 100 mV to 10 V
- Input cable lengths: Less than 7.5 m (25 ft)

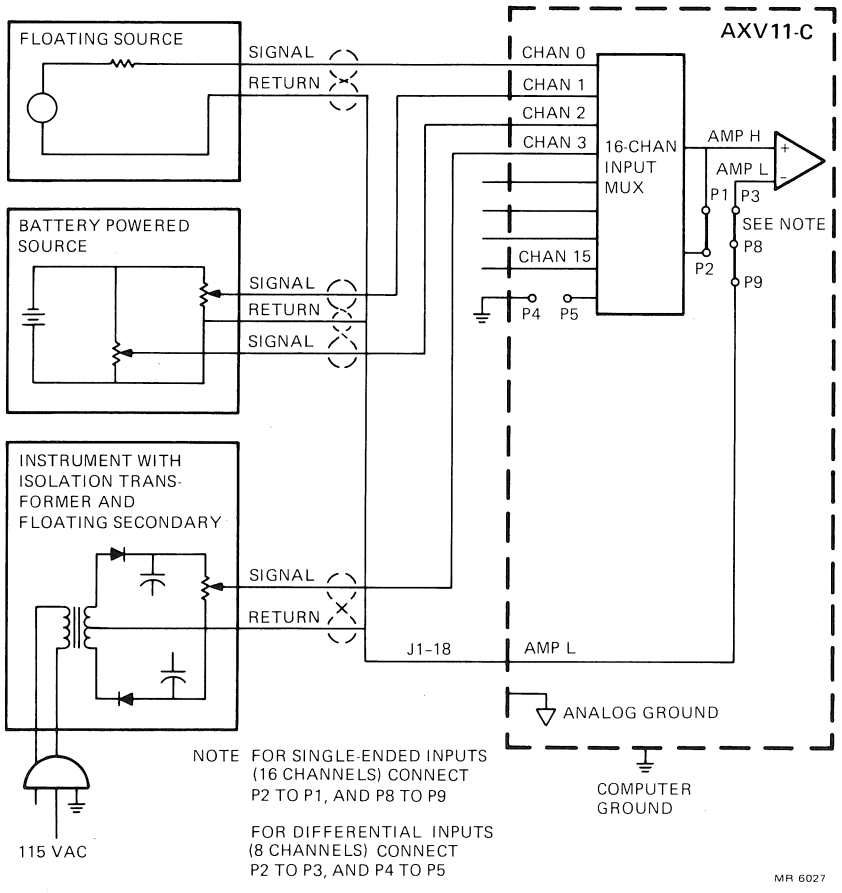


Figure 4-9 Pseudo-Differential Inputs

4.7.3 Differential Inputs (8 Channels)

Differential inputs have one side of the generating source connected to the positive (+) input of the A/D input amplifier and the other side of the source connected to the negative (−) input of the amplifier, as shown in Figure 4-10.

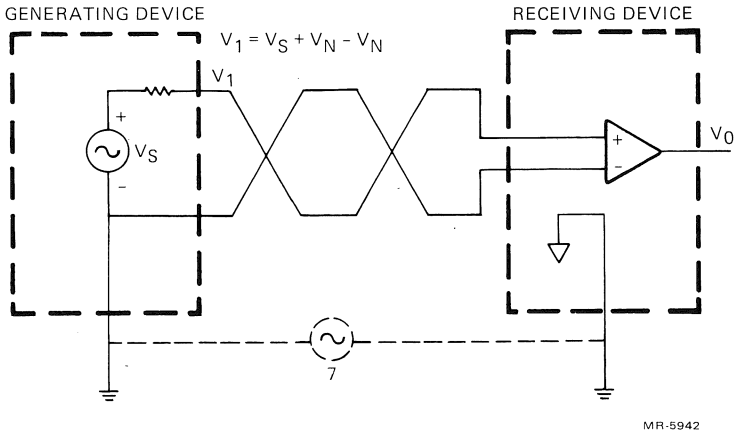


Figure 4-10 Differential Inputs

The benefit of differential inputs is that noise voltages appearing at the same time on both sides of the source are rejected by the A/D input amplifier. This is called common mode rejection, and provides a system with low noise. The amount of noise rejection is a ratio, the common mode rejection ratio (CMRR), given in decibels (dB). The CMRR for the AXV11-C is 80 dB at full-scale range. (See Paragraph 2.8.)

The disadvantage of differential inputs is that the number of available input channels is lowered by half.

The recommended analog inputs are as follows.

- Input range: 10 mV to 10 V
- Input cable length: As needed by user
- Cable type: Twisted-pair, shielded lines with low impedance

4.7.4 Preventing False Signals

To get the best performance from an analog system, certain rules must be followed when connecting analog inputs to the system. The rules help to provide clean input signals and to lower the effects of electrical noise on the input amplifiers. The rules and suggestions are the same as those given for the ADV11-C in Paragraph 2.9.

CHAPTER 5
KWV11-C PROGRAMMABLE REAL-TIME CLOCK

5.1 INTRODUCTION

The KWV11-C is a programmable real-time clock printed circuit board, M4002. It can be programmed to count from one of five crystal-controlled frequencies, from an external input frequency or event, or from the 50/60 Hz line frequency on the LSI-11 bus. The board can generate interrupts or can synchronize the processor to external events. The KWV11-C has a counter that can be programmed to operate in any one of the following modes.

Mode	Counter Operation
0	Single interval
1	Repeated interval
2	External event timing
3	External event timing from zero base

The KWV11-C has two Schmitt triggers that can be set to operate at any level between ±12 V on either the positive or negative slope of the external input signal. In response to external events, the Schmitt triggers can start the clock, start A/D conversions in an A/D input board, or generate program interrupts to the processor.

5.2 FEATURES

The KWV11-C has the following features.

- Resolution of 16 bits
- Five internal crystal frequencies – 1 MHz, 100 kHz, 10 kHz, 1 kHz, and 100 Hz.
- Two Schmitt triggers, each with slope and level controls that can be used to start the clock or generate program interrupts.
- Line frequency input from BEVNT bus signal (50/60 Hz).
- Four programmable modes.

5.3 KWV11-C SPECIFICATIONS

Identification	Dual-height module, M4002 (part number: 30-18690-00)
Power Requirement	+5 V ±5% @ 2.2 A +12 V ±3% @ 13 mA
Bus Loads	
DC bus load	1
AC bus load	1.0

Clock	
Crystal oscillator	10 MHz base frequency
Output ranges	1 MHz, 100 kHz, 10 kHz, 1 kHz, and 100 Hz
Oscillator accuracy	0.01%
Other sources	Line frequency or input at Schmitt trigger 1
I/O Connector	40 pins; 3M no. 3417-7040
Schmitt Trigger Input Signals	
No. of inputs	2
Input range	±30 V (max limits)
Triggering range	−12 V to +12 V adjustable
Triggering slope	Positive or negative, switch selectable
Source	User device
Response time	Depends on input waveform and amplitude; for TTL logic levels, typically 600 ns.
Hysteresis	Approximately 0.5 V, positive and negative
Characteristics	Single-ended input with 100 kΩ impedance to ground
Clock Output	
Signal	CLK OV L (clock overflow, asserted low)
Output pins	J1 pin RR and CLK OVFL tab
Function	Time base selection from an internal crystal-controlled frequency, an input at ST1, or a line frequency at BEVNT bus line.
Duration	Approximately 500 ns
Line driver	TTL compatible, open collector circuit with 470 Ω pull-up resistor to +5 V.
Max source current	5 mA when output is high ($\geqslant$ 2.4 V) measuring from source through load to ground.
Max sink current	8 mA when output is low ($\leqslant$ 0.8 V) measuring from external source voltage through load to output.

Schmitt Trigger 1 Output	
Signal	ST1 OUT L (asserted low)
Output pins	J1 pin UU and ST1 OUT tab
Function	External time base input or counter of external events. Input frequency is a function of the input signal.
Other characteristics	Same as clock output.
Schmitt Trigger 2 Output	
Signal	ST2 OUT L (asserted low)
Output pins	J1 pin SS
Function	Starts counter, sets ST2 flag, and generates an interrupt (if enabled); causes buffer preset register (BPR) to be loaded from counter.
Other characteristics	Same as clock output.
Environment	Ref: DEC Standard 102, Class C

5.4 KWV11-C FUNCTIONAL DESCRIPTION

Figure 5-1 shows a block diagram of the KWV11-C. It has two read/write registers that can be addressed by the processor – the control/status register (CSR) and the buffer/preset register (BPR). Two switch packs on the board allow the user to select the starting device address for these registers and the starting interrupt vector address.

The DMA bus transceivers monitor and generate bus signals for interrupts, data transfers, and addressing and timing controls. The bus transceivers receive address and data information from the LSI-11 bus. When an address match occurs, the bus transceivers transfer data to or from the control/status register or the buffer/preset register.

5.4.1 Control/Status Register

The control/status register (CSR) allows the processor to control the operation of the KWV11-C and to get status information on its current operating condition. The CSR has bits to enable interrupts, mode selection, clock rate selection, and starting the counter (GO bit). The CSR monitors the counter overflow flag, flag overrun, and the Schmitt trigger flag (ST2). In addition, the CSR enables some maintenance operations.

5.4.2 Buffer/Preset Register and Counter

The buffer/preset register (BPR) is a 16-bit, word-addressable, read/write register. This register has two functions depending on the mode of operation selected. In mode 0 or 1, the BPR is loaded from the program with the clock count. The clock count is the 2's complement of the number of clock inputs the counter is to receive before it overflows. The clock overflow (CLK OV L) sets a flag in the CSR and generates an interrupt request (if enabled). CLK OV L can also be connected directly to an A/D input board to start an A/D conversion.

In mode 2 or 3, the BPR provides indirect reading of the clock counter. An input to Schmitt trigger 2 (ST2) causes the BPR to be loaded with the contents of the counter. The counter is an internal register that is accessible only by reading the BPR in these modes. The counter keeps track of the number of clock pulses from the clock selector or the number of input pulses at Schmitt trigger 1 (ST1).

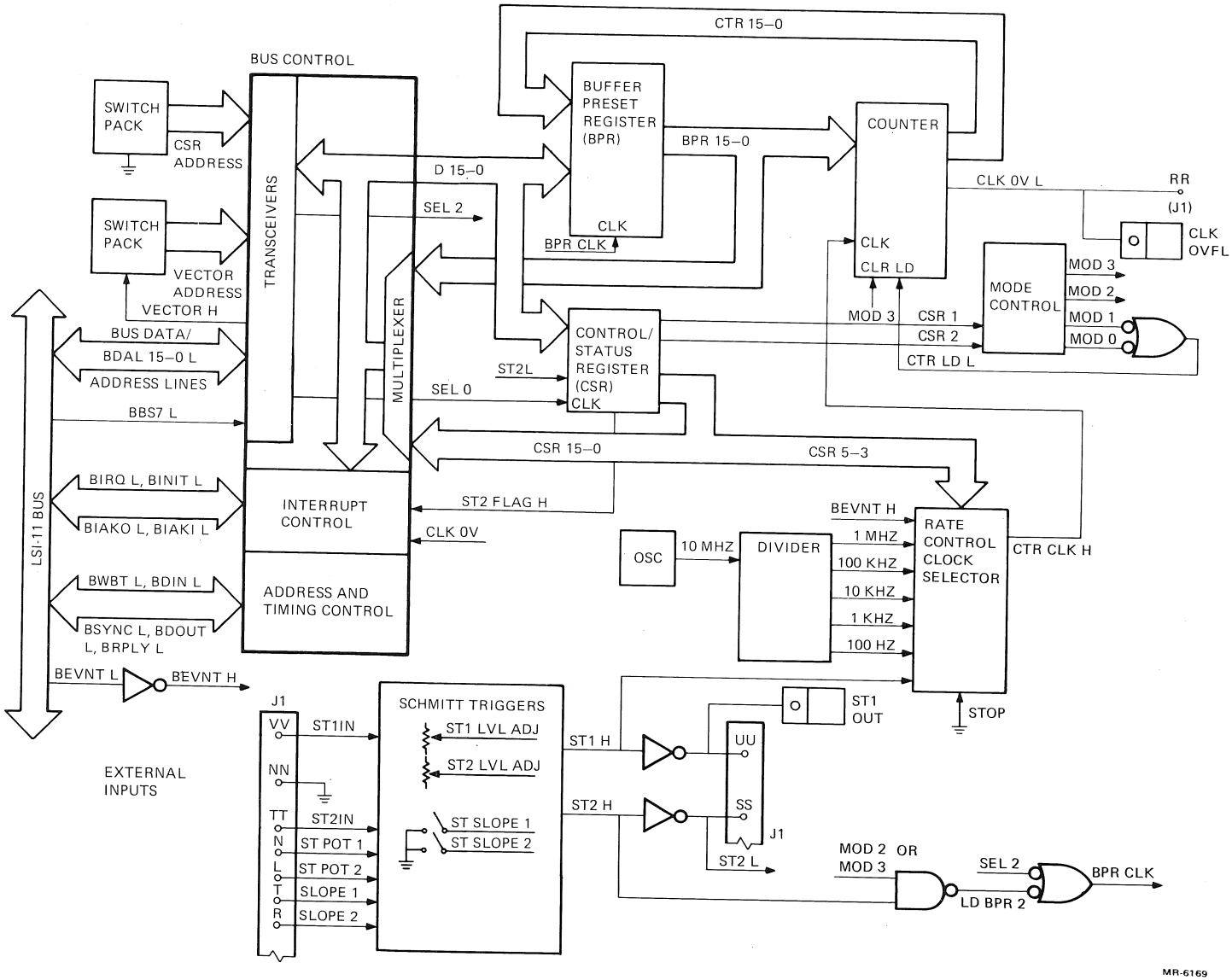


Figure 5-1 KWV11-C Functional Block Diagram

5.4.3 Oscillator, Divider, and Clock Selector

The clock selector provides the clock input to the counter. The clock selector has eight inputs, five of which are derived from a 10 MHz crystal oscillator and frequency divider network. The other inputs are: STOP, BEVNT, and ST1. STOP halts the counter; BEVNT is a 50 or 60 Hz line clock input from the LSI-11 bus; ST1 (Schmitt trigger 1) can be used as an input for an external clock or as an input to count external events.

5.4.4 Mode Control

CSR bits 1 and 2 determine the mode of operation of the KWV11-C. These bits are decoded in the mode control logic as follows.

CSR Bit 2	CSR Bit 1	Mode Selected
0	0	Mode 0 – Single interval
0	1	Mode 1 – Repeated interval
1	0	Mode 2 – External event timing
1	1	Mode 3 – External event timing from zero base

In either mode 0 or 1, the counter is loaded from the buffer/preset register. In mode 0, the counter increments at the clock selected rate until it overflows, then it waits for another GO command. In mode 1, the counter continues to count even after an overflow and can cause an interrupt at repeated intervals.

In mode 2, the counter increments at the clock selected rate (or at rate of external input). An input at ST2 causes the contents of the counter to be loaded into the BPR, where it can be read by the processor. In mode 3, the counter is reset to zero after loading its contents into the BPR. For more information on mode control, see Paragraph 5.5.3.

In all modes, if a second overflow occurs before the processor services the first overflow, or if a second ST2 input tries to set a previously set ST2 FLAG, a flag overrun bit is set in the CSR.

5.4.5 Schmitt Triggers

The KWV11-C has two Schmitt triggers – ST1 and ST2. Both have switches to select the threshold level and the slope selection (positive or negative). Selecting a positive slope allows the Schmitt trigger to fire on a low-to-high transition of the input signal; selecting a negative slope allows the Schmitt trigger to fire on a high-to-low transition.

The Schmitt triggers are used in different ways.

ST1 – Schmitt trigger 1 can be an external time base input or an external input for signals to be counted. ST1 is one of the inputs to the clock selector and can be selected as the clock for the counter. ST1 also goes to connector J1 and to tab ST1 OUT. A jumper wire can be connected from this tab to the RTC IN jumper pin on the A/D input printed circuit board.

ST2 – Schmitt trigger 2 can be used to start the counter, to set a flag in the CSR, or to generate an interrupt to the processor. When the ST2 GO ENABLE bit is set in the CSR, the ST2 input sets the GO bit, which starts the counter, sets the ST2 flag in the CSR, and generates an interrupt (if enabled).

5.5 PROGRAMMING THE KWV11-C

The KWV11-C has the following two programmable read/write registers.

Control/Status Register (CSR)
Buffer/Preset Register (BPR)

The standard address and interrupt vectors for the KWV11-C are shown in Table 5-1. This paragraph describes these registers and defines their bits.

Table 5-1 KWV11-C Standard Address Assignments

Description	Mnemonic	Address
Registers		
Control/Status	CSR	170420
Buffer/Preset	BPR	170422
Interrupt Vectors		
Clock Overflow	CLK OV	440
Schmitt Trigger 2	ST2	444

5.5.1 KWV11-C Control/Status Register

Figure 5-2 shows the bit assignments in the control/status register. Each bit can be written or read under program control; however, the maintenance bits, the flags, and the go bits have special programming considerations.

- The maintenance bits (8, 9 and 10) always read 0.
- The flags (7, 12, and 15) can not be set by the program.
- The go bits (0, 13) can be cleared by more than one method.

Table 5-2 defines each bit in the CSR.

5.5.2 KWV11-C Buffer/Preset Register

The address of the buffer/preset register is the standard device address + 2, or 170422_8. This register has two purposes. During mode 0 or 1 operation, this register is used to load the number of clock counts before the counter overflows. During mode 2 or 3 operation, this register is used to read the current count from the counter. Reading the BPR, indirectly reads the counter.

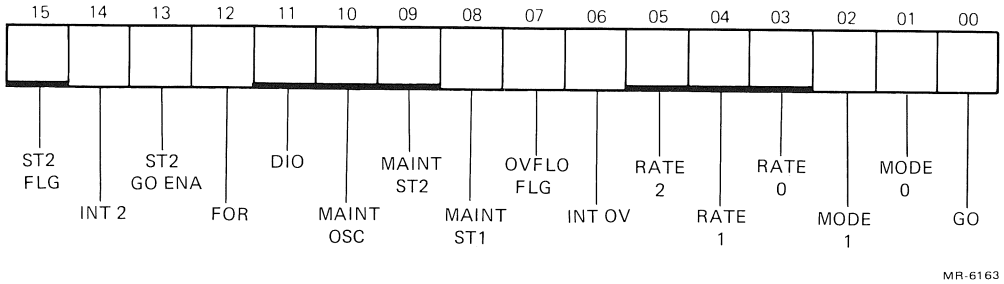


Figure 5-2 KWV11-C Control/Status Register

Table 5-2 KWV11-C Control/Status Register Bit Definitions

Bit	Name	Function	Set By/Cleared By
0	GO	Read/Write – Setting this bit starts the counter at a rate determined by the rate bits 3–5.	The GO bit is set and cleared under program control. In modes 1, 2, and 3, this bit remains set until cleared by the program. In mode 0 this bit is cleared automatically when the counter overflows. Clearing bit 0 or a BUS INIT resets the counter and stops the counting.
1, 2	MODE	Read/Write **2 1 Mode** 0 0 Mode 0 0 1 Mode 1 1 0 Mode 2 1 1 Mode 3	The mode is set and cleared under program control and by BUS INIT.
3–5	RATE	Read/Write – These bits select the clock rate or counting source for the counter. **5 4 3 Rate** 0 0 0 Stop 0 0 1 1 MHz 0 1 0 100 kHz 0 1 1 10 kHz 1 0 0 1 kHz 1 0 1 100 Hz 1 1 0 ST1 external input 1 1 1 Line (50/60 Hz)	The rate is set and cleared under program control and by BUS INIT.
6	INTOV (Interrupt on Overflow)	Read/Write – When this bit is set, the assertion of OVFLO FLAG generates an interrupt. Interrupt is also generated if bit 6 is set while OVFLO FLAG is set.	This bit is set and cleared under program control. If either bit 6 or 7 is cleared while an overflow interrupt request to the processor is pending, the request is cancelled.
7	OVFLO FLAG	Read/Write to 0 – If bit 6 is set, setting bit 7 generates an interrupt. Bit 7 must be cleared after the interrupt has been serviced to enable further overflow interrupts. If two enabled interrupts are requested at the same time by bits 7 and 15, bit 7 has the higher priority.	This flag is set each time the counter overflows. It is cleared under program control, or at the low-to-high transition of the GO bit, or by BUS INIT.
8	MAINT ST1	Write Only – Setting this bit simulates the firing of ST1. All functions started by ST1 can be exercised under program control by using this bit.	This bit is set under program control. Clearing is not needed. It is always read as a 0.
9	MAINT ST2	Write Only – Setting this bit simulates the firing of Schmitt Trigger 2. All functions started by ST2 can be exercised under program control by using this bit.	This bit is set under program control. Clearing is not needed. It is always read as a 0.
10	MAINT OSC	Write Only – For maintenance purposes, setting this bit simulates one cycle of the internal crystal oscillator used to increment the clock counter. (Bit 11 must be set.)	This bit is set under program control. Clearing is not needed. It is always read as a 0.

Table 5-2 KWV11-C Control/Status Register Bit Definitions (Cont)

Bit	Name	Function	Set By/Cleared By
11	DIO (Disable Internal Oscillator)	Read/Write – For maintenance purposes, this bit prevents the internal crystal oscillator from incrementing the clock counter. This bit is used with bit 10.	This bit is set and cleared under program control.
12	FOR (Flag Overrun)	Read/Write – Flag Overrun provides the programmer with an indication that the hardware is being asked to operate at a speed higher than is compatible with the software.	This flag is set when an overflow occurs and the OVFLO FLAG (bit 7) is still set from a previous occurrence, or when ST2 fires and the ST2 FLAG (bit 15) has been previously set. Bit 12 is cleared under program control, or at the low-to-high transition of the GO bit, or by BUS INIT.
13	ST2 GO ENABLE	Read/Write – When set, the assertion of ST2 FLAG sets the GO bit and clears the ST2 GO ENABLE bit.	The ST2 GO ENABLE bit is cleared under program control, or at the low-to-high transition of the GO bit, or by BUS INIT.
14	INT 2 (Interrupt on ST2)	Read/Write – When set, the assertion of ST2 FLAG (bit 15) causes an interrupt. If set while ST2 FLAG is set, an interrupt request is generated.	This bit is set and cleared under program control and by BUS INIT. When either bit 14 or 15 is cleared, any pending ST2 interrupt request is cancelled.
15	ST2 FLAG	Read/Write to 0 – Setting this flag starts an interrupt request if bit 14 is set. Bit 15 must be cleared after servicing an ST2 interrupt to enable further interrupts. If two enabled interrupts are requested at the same time by bits 7 and 15, bit 7 has the higher priority.	The ST2 FLAG is set by the firing of Schmitt Trigger 2 or the setting of the MAINT ST2 bit (in any mode) while the GO bit or the ST2 GO ENABLE bit is set. The ST2 FLAG is cleared under program control or at the low-to-high transition of the GO bit unless the ST2 GO ENABLE bit has previously been set. This bit is also cleared by BUS INIT.

5.5.3 Typical Program Sequences

This paragraph describes typical program sequences for operating the KWV11-C in each of the four modes of operation.

Single Interval (Mode 0)

This mode of operation is used to generate a fixed interval for such applications as known delays.

1. The program loads the BPR with the 2's complement of the number of clock pulses needed to generate the time delay at the user-selected clock rate. For example:

   Loading the BPR with −100, at a clock frequency of 1 kHz, generates 100 ms time delay.

2. The program loads the CSR with mode 0, the clock rate, and interrupt enable (INTOV) if needed.

3. The program sets the GO bit, or it sets the ST2 GO ENA bit and waits for an external event to set the GO bit.

4. When the GO bit is set, the counter is loaded with the contents of the BPR and starts counting. The counter increments until it overflows, at which time it clears the GO bit and stops counting.

5. The overflow causes the overflow flag (OVFLO) to be set in the CSR. If INTOV has been previously set, the OVFLO causes an interrupt to occur. If not, the KWV11-C waits for another program command.

6. The program either responds to the interrupt, or it responds as a result of checking the flags in the KWV11-C or in the A/D CSR. For example:

   The program can test the OVFLO flag in the CSR of the KWV11-C.

   If CLK OVL is used to start an A/D conversion, the program can check the A/D DONE flag in the A/D input board or allow the A/D DONE flag to generate an interrupt request.

7. The program reads the CSR, clears the OVFLO flag, and if no counting or mode changes are needed, sets the GO bit (or ST2 GO ENA bit) to start again at step 4 above.

Repeated Interval (Mode 1)
In this mode of operation, the user can generate a fixed frequency pulse train with any period within the range of the clock counter and the five crystal frequencies.

1. The program loads the BPR with the 2's complement of the number of clock pulses needed to generate the time delay at the user-selected clock rate. For example:

   Loading the BPR with -1 and selecting a 1 MHz clock rate generates a 1 MHz pulse train.

   In general, the overflow rate (pulse train) is equal to the clock rate divided by the absolute value that is loaded into the BPR.

2. The program loads the CSR with mode 1, the clock rate, and interrupt enable (INTOV) if needed.

3. The program sets the GO bit, or it sets the ST2 GO ENA bit and waits for an external event to set the GO bit.

4. When the GO bit is set, the counter is loaded with the contents of the BPR and starts counting. The counter increments until it overflows.

5. The overflow causes the counter to be loaded again with the count from the BPR and to start counting again. The overflow also sets the OVFLO flag in the CSR, which generates an interrupt if enabled.

6. If a second overflow occurs before the processor services the first overflow flag, then the flag overrun (FOR) bit is set in the CSR to inform the processor of a loss of data.

7. The program either responds to the interrupt, or it responds as a result of checking the flags in the KWV11-C CSR or in the A/D CSR. For example:

   The overflow (CLK OVL) can be used to start an A/D conversion in an A/D input board. When the A/D conversion is complete, A/D DONE in the A/D CSR can generate an interrupt request.

8. The program writes the KWV11-C CSR to clear the OVFLO flag, make necessary changes, and set the GO bit (or ST2 GO ENA bit). Then the program starts again at step 4 above.

External Event Timing (Mode 2)
In this mode of operation, the user can generate a pulse train while monitoring external events, can record the time of external events, or can count external events. Two external events can be monitored with respect to each other.

1. The program may load the BPR with the 2's complement of one of the following:
   - The number of line inputs (BEVNT) that will generate a real-time reference to record the time of an external event at ST2.
   - The number of clock pulses needed to generate the time delay at the user-selected clock frequency.
   - The number of external events to be counted at ST1 before an overflow occurs.
2. The program loads the CSR with mode 2, the clock input (ST1, BEVNT, or one of five frequencies), and interrupt enable (INTOV or INT2) if needed.
3. The program sets the GO bit, or it sets the ST2 GO ENA bit and waits for an external event to set the GO bit.
4. When the GO bit is set, the counter is cleared and it starts counting at the selected clock rate or number of inputs at ST1.
5. An input at ST2 places the current contents of the counter in the BPR and sets the ST2 flag in the CSR. If INT2 has previously been set, an interrupt is generated to the processor. The program can then read the BPR and record the time of the event.
6. If ST2 does not occur, the counter continues to increment even after an overflow. The overflow sets the OVFLO flag and generates an interrupt if INTOV is enabled.
7. The counter continues until the program clears the GO bit.

External Event Timing from Zero Base (Mode 3)
The program for this operation is the same as for mode 2, except the counter is automatically cleared after every ST2 pulse.

5.6 CONFIGURING THE KWV11-C

The KWV11-C, shown in Figure 5-3, has two switch packs, SW1 and SW2, to set up its device address and interrupt vector address. It also has a switch pack, SW3, to select Schmitt trigger slope and level controls. For each of the two Schmitt triggers on the board, the user may select a fixed reference level for TTL logic or a variable reference level that permits setting the Schmitt trigger threshold to any point between -12 V and $+12$ V. The user may also select whether the Schmitt trigger fires on the positive or negative slope of the input waveform.

Two tabs on the board provide outputs from the clock counter (CLK OVL) and Schmitt trigger 1 (ST1 OUT). Either of these output tabs can be used to connect a short jumper wire to the A/D input board (pin RTC IN) to start an A/D conversion.

This paragraph provides details on setting up the KWV11-C.

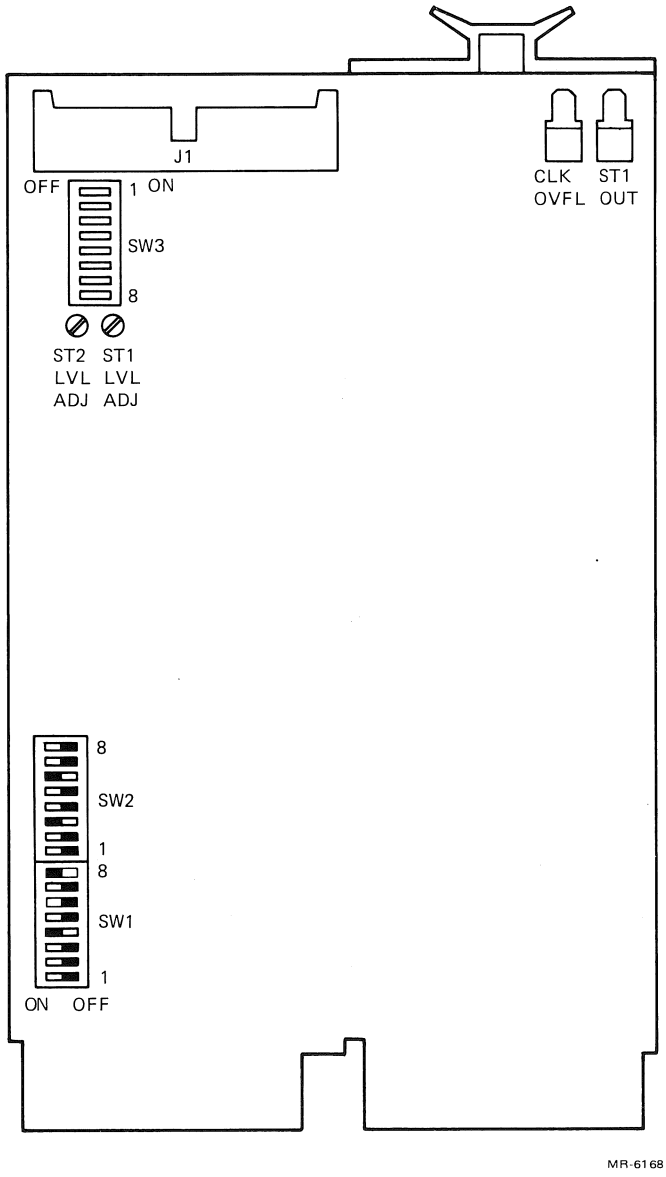


Figure 5-3 KWV11-C Physical Layout

5.6.1 Selecting the KWV11-C Device Address

The KWV11-C device address is the base I/O address assigned to the control/status register of the board. The device address is selected by means of two switch packs, SW1 and SW2. The switches allow the user to set the device address within the range of 170000_8 to 177774_8 in increments of 4_8. The device address is usually set at 170420_8, as shown in Figure 5-4. A switch in the ON position decodes a 1 in the corresponding bit position; a switch in the OFF position decodes a 0.

5.6.2 Selecting the KWV11-C Interrupt Vector Address

The KWV11-C is capable of generating two interrupt vectors to the LSI-11 processor. These interrupts can occur when one of the following occurs.

- Clock counter overflows
- Schmitt trigger 2 fires.

The base interrupt vector is assigned to the clock overflow interrupt and can be assigned any address between 0 and 770_8 in increments of 10_8. It is usually set to 440_8 by SW2, as shown in Figure 5-5. A switch in the OFF position decodes a 0; a switch in the ON position decodes a 1.

The interrupt vector for ST2 is automatically 4 address locations higher than the selected base interrupt vector.

5.6.3 Selecting Schmitt Trigger Reference Levels and Slopes

The KWV11-C has two Schmitt triggers that condition the input waveforms to a form needed by the user. Both can be adjusted to trigger at any level in the ± 12 V range (or at TTL fixed levels) and on either the positive or negative slope of the input signal. Each Schmitt trigger has three switches and a potentiometer, shown in Figure 5-6. The use of these switches and potentiometers are given in Table 5-3.

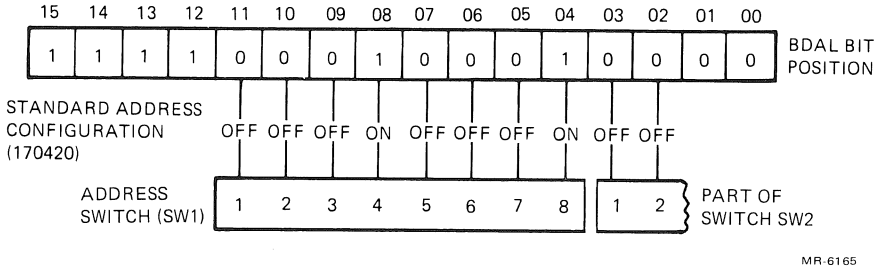


Figure 5-4 Selecting KWV11-C Device Address

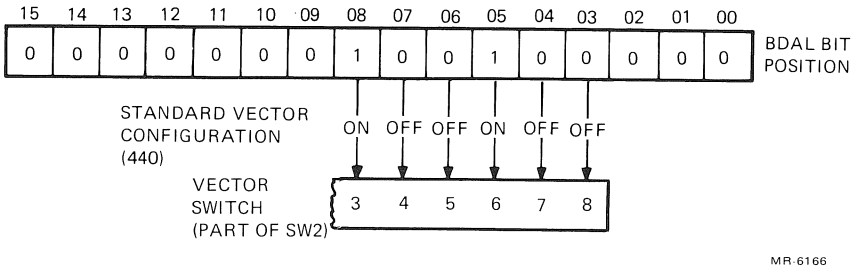


Figure 5-5 Selecting KWV11-C Interrupt Vector Address

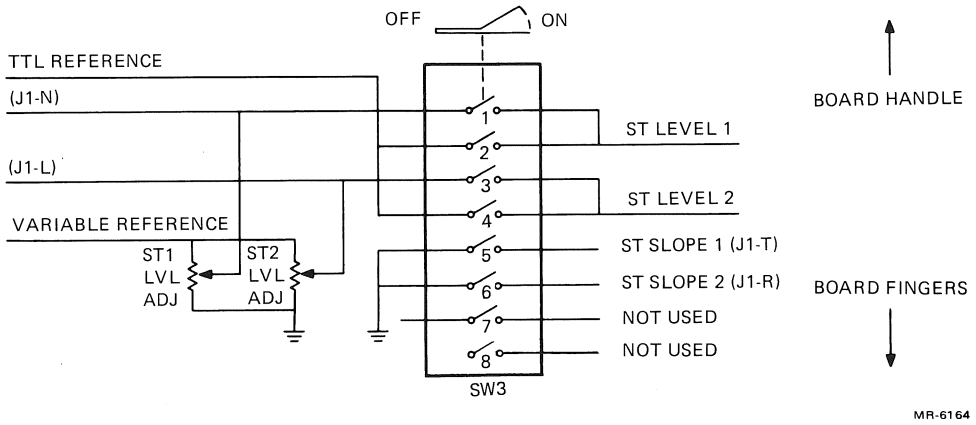
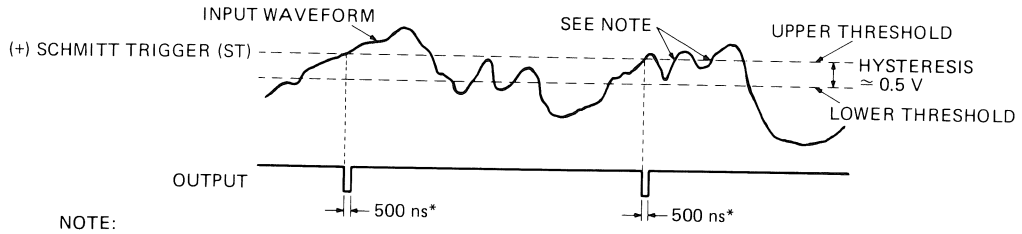


Figure 5-6 KWV11-C Slope and Reference-Level Switches

Table 5-3 Setting Schmitt Triggers on KWV11-C

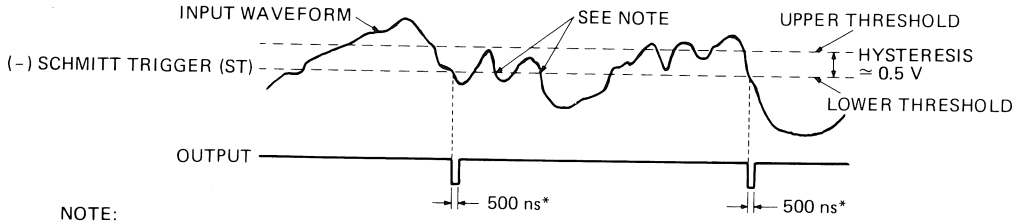
SW3 Switch No.	Function
1	With this switch ON and switch 2 OFF, ST1 fires at a level determined by the ST1 LVL ADJ potentiometer within a range of ±12 V. **NOTE** **Switches 1 and 2 can not be on together.**
2	With this switch ON and switch 1 OFF, ST1 fires at a fixed reference level for TTL logic. The potentiometer has no effect.
3	With this switch ON and switch 4 OFF, ST2 fires at a level determined by the ST2 LVL ADJ potentiometer within a range of ±12 V. **NOTE** **Switches 3 and 4 can not be on together.**
4	With this switch ON and switch 3 OFF, ST2 fires at a fixed reference level for TTL logic. The potentiometer has no effect.
5	When this switch is OFF, ST1 fires on the negative slope (high to low transition) of the input signal. When ON, ST1 fires on the positive slope (low to high transition).
6	When this switch is OFF, ST2 fires on the negative slope of the input signal. When ON, ST2 fires on the positive slope.
7, 8	Not used.

Figure 5-7 shows the relationship of an analog input signal to the Schmitt trigger output. Note that once the Schmitt trigger fires, it fires again only after the input signal moves past the opposite threshold and then again passes the user-selected threshold.



NOTE:
ST IS TRIGGERED AGAIN ONLY AFTER THE INPUT WAVEFORM DROPS BELOW THE LOWER THRESHOLD AND EXCEEDS THE UPPER THRESHOLD.

(a) POSITIVE SLOPE SELECTION (SLOPE SWITCHED ON)



NOTE:
ST IS TRIGGERED AGAIN ONLY AFTER THE INPUT WAVEFORM EXCEEDS THE UPPER THRESHOLD AND DROPS BELOW THE LOWER THRESHOLD.

(b) NEGATIVE SLOPE SELECTION (SLOPE SWITCHED OFF)

*400 ns MINIMUM

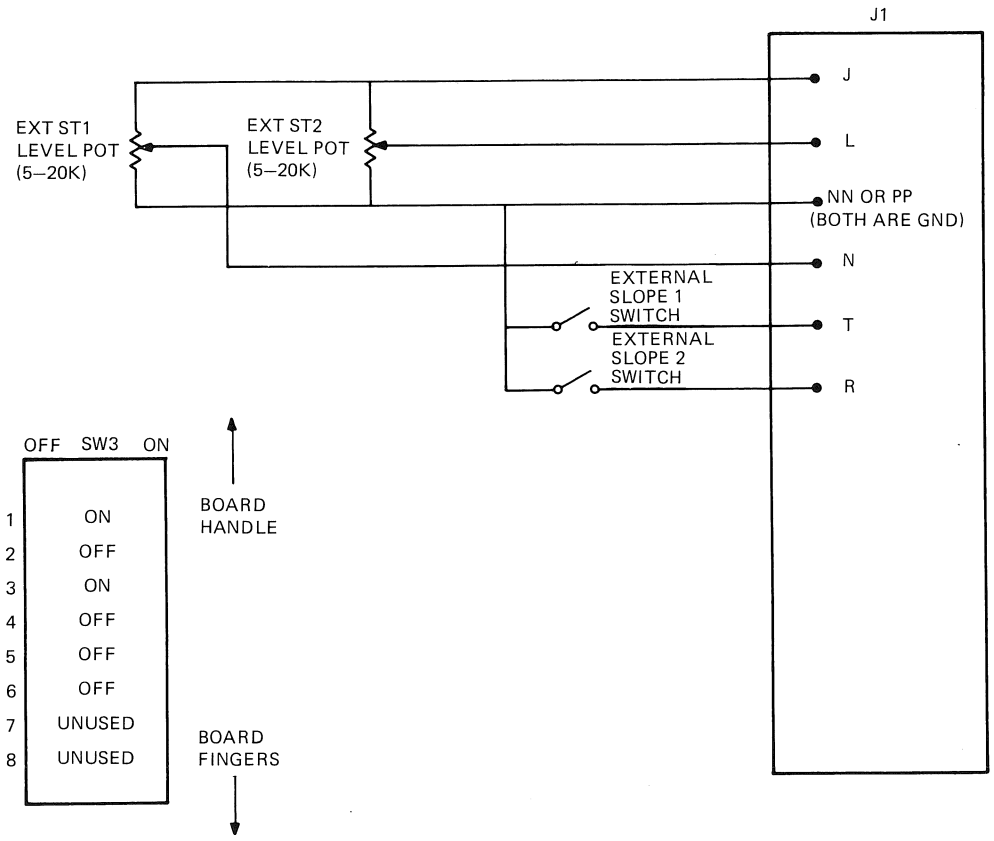
MR-5340
11-4549

Figure 5-7 Input-to-Output Waveforms for Positive and Negative Slopes

5.6.4 External Control of Schmitt Triggers

The connector J1 on the board allows the user to connect external slope and level controls for each Schmitt trigger. Connect external potentiometers and switches as shown in Figure 5-8. The value of the potentiometers should be between 5 kΩ and 20 kΩ. Selecting a potentiometer with more turns provides for a finer adjustment over the ±12 V range.

SW3 on the KWV11-C must be set as shown in Figure 5-8, and the potentiometers on the KWV11-C should be set to their center of rotation. At the center, the screwdriver slot should be aligned with the notch at its edge.



NOTES:

1. FOR PROPER OPERATION OF EXTERNAL LEVEL CONTROLS, BOTH POTENTIOMETERS ON THE KWV11-C BOARD MUST BE SET TO APPROXIMATE CENTER OF ROTATION.
2. SW3 SWITCHES 1–4 MUST BE SET AS SHOWN; SWITCHES 5 AND 6 CAN BE EITHER OFF FOR NEGATIVE SLOPE TRIGGERING OR ON FOR POSITIVE SLOPE TRIGGERING.

MR-6167

Figure 5-8 Example Circuit for External Control of Schmitt Triggers

5.7 INTERFACING TO THE KWV11-C

Figure 5-9 shows the pin assignments of the 40-pin I/O connector J1 on the KWV11-C. This connector is provided for user inputs and outputs.

In addition, two tabs (shown in Figure 5-3) provide output signals CLK OVFL and ST1 OUT. These tabs are electrically in parallel with pins RR and UU of J1. These tabs make it easier for the user to connect an external start signal from the KWV11-C to the A/D input board (pin RTC IN) using a jumper wire. The external start signal for an A/D conversion can be from Schmitt trigger 1 or from the clock counter overflow. See Paragraph 5.5.3 for typical program sequences.

The KWV11-C has two bus interface connectors that plug into the LSI-11 bus. These connectors have signals defined by LSI-11 bus specifications. Pin assignments and their functions are described in the *Microcomputer Interfaces Handbook*.

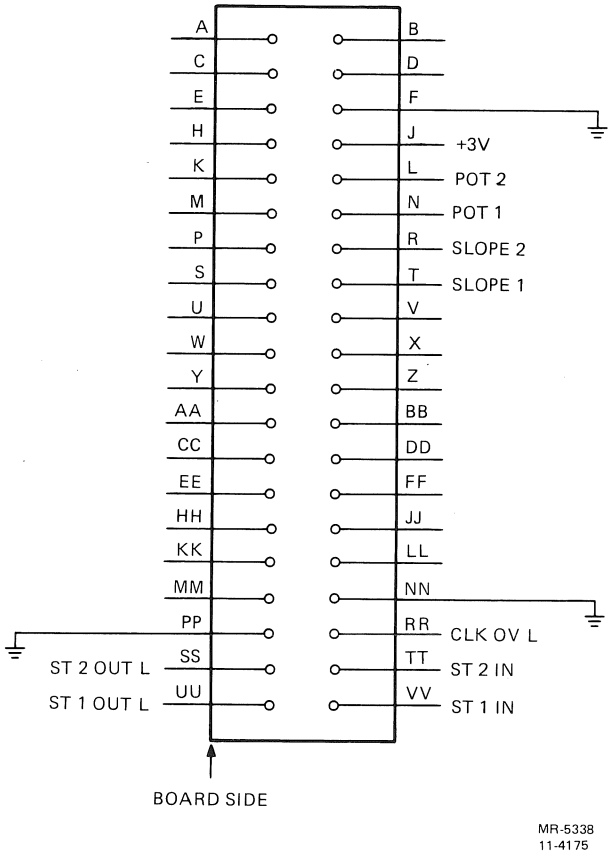


Figure 5-9 KWV11-C I/O Connector J1 Pin Assignments

CHAPTER 6
CALIBRATION AND TESTING

6.1 INTRODUCTION

The analog printed circuit boards are calibrated and tested using the AXV11-C/ADV11-C diagnostic (CVAXA) and an optional analog test fixture (part number 30-18692) (See Figures 6-1 and 6-2.) The diagnostic tests the AXV11-C or the ADV11-C, with or without the test fixture attached to the board. The diagnostic also allows connection to the AAV11-C or to the KWV11-C, so they may supply signals to test the AXV11-C or the ADV11-C. The diagnostic tests some of the functions of the AAV11-C and KWV11-C.

The AAV11-C can be completely tested using MAINDEC-11-DVAAA (CVAAA). The KWV11-C can be completely tested using MAINDEC-11-DVKWA (CVKWA).

The procedure for using the analog test fixture is described in Paragraph 6.4

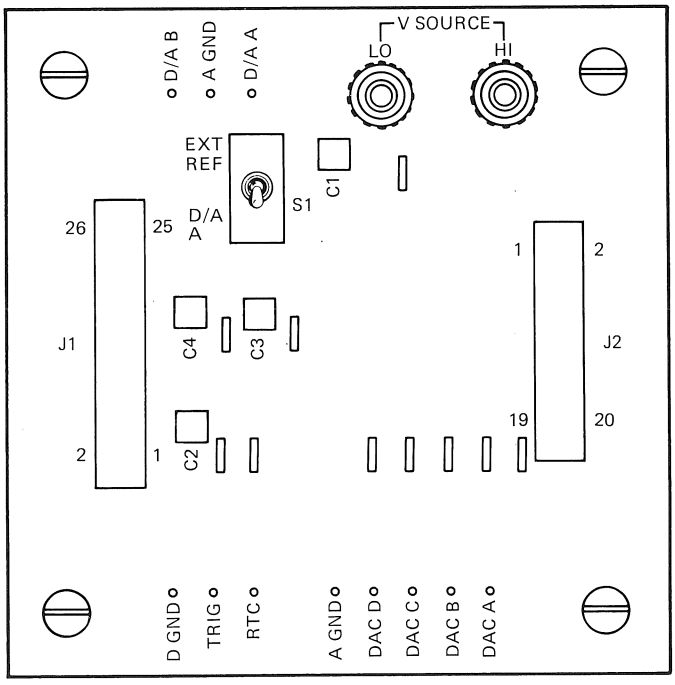


Figure 6-1 Analog Test Fixture

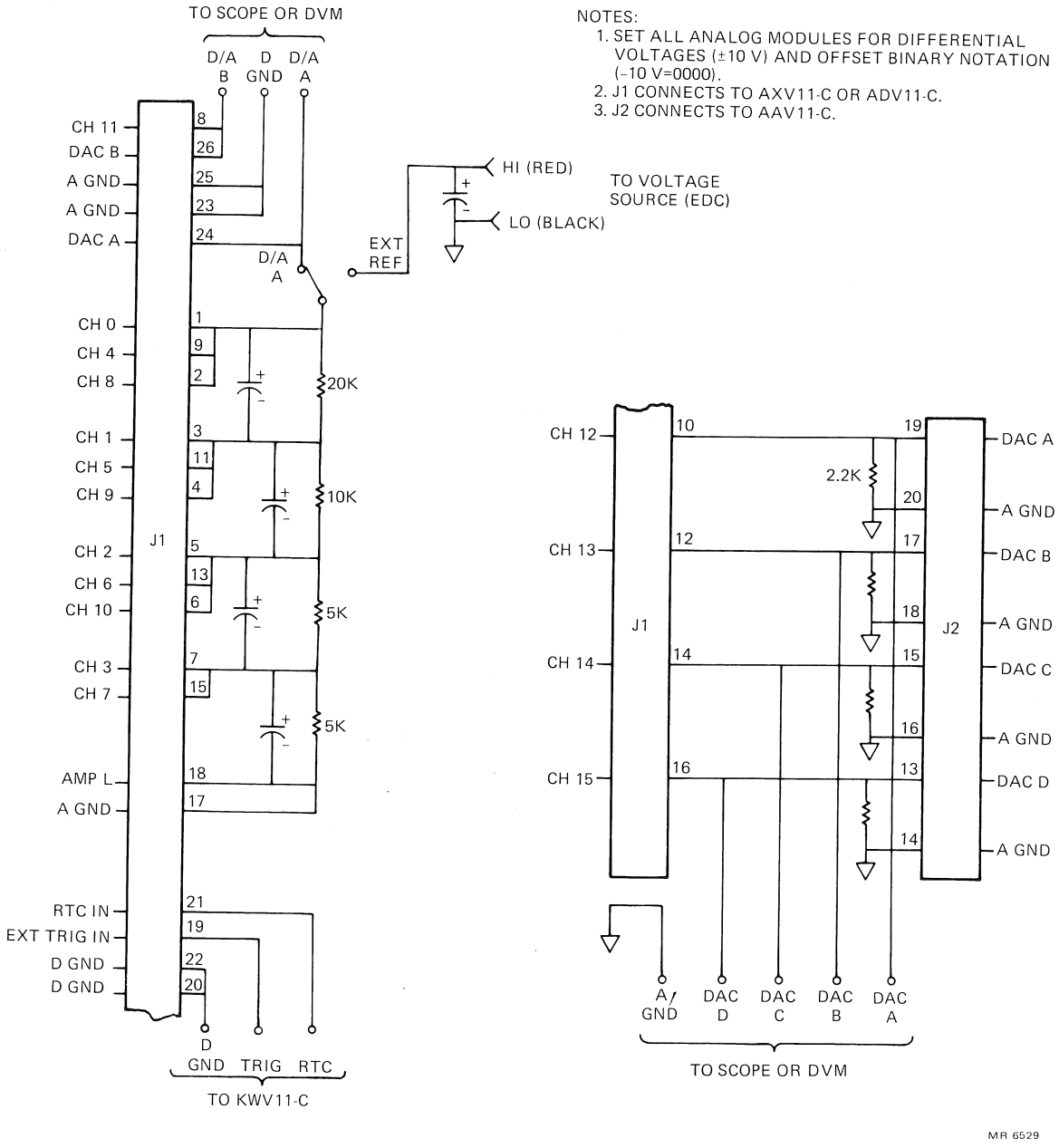


Figure 6-2 Analog Test Fixture Schematic

6.2 EQUIPMENT NEEDED

The following equipment is needed to run the AXV11-C/ADV11-C diagnostic.

LSI-11 computer with 8K words of memory
RX02 disk drive
I/O terminal
AXV11-C or ADV11-C
AAV11-C (optional)
KWV11-C (optional)

The diagnostic uses 8K words of memory and can be chained using XXDP+. When chained, only the logic tests are executed.

The following added equipment is needed to calibrate the analog boards using the analog test fixture.

Analog test fixture with 26-pin ribbon cable
Dual-height extender board
Digital volt meter with ±0.0001 volt accuracy
Precision voltage calibrator or standard
Oscilloscope
Diskette with XXDP+ and CVAXA diagnostic

6.3 CIRCUIT BOARD CONFIGURATION TO RUN DIAGNOSTIC AUTOMATICALLY

The diagnostic can test many configurations of the analog boards; however, to run the diagnostic automatically without changing any parameters, use the factory configuration of the boards, configured as follows.

- Standard device address
- Standard interrupt vector address
- Single-ended inputs
- Bipolar operation ±10 V
- Offset binary notation

Figure 6-3 shows the jumpers that are installed on the factory-configured AXV11-C. The ADV11-C is similar except that jumpers and circuits for DAC A and DAC B are missing. Table 6-1 shows the jumpers that are installed on these analog input boards.

On the AAV11-C the jumpers are installed as shown in Figure 3-4.

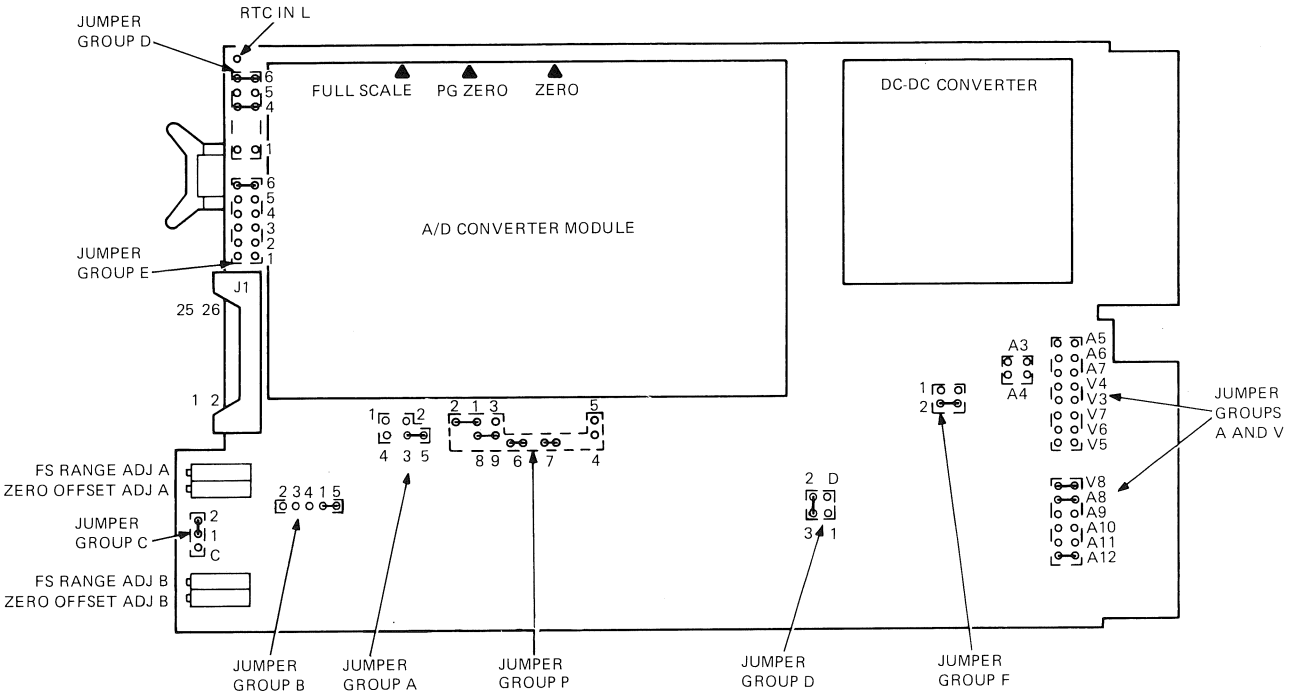


Figure 6-3 AXV11-C Configuration to Run Diagnostic Automatically

Table 6-1 Analog Input Board Jumpers to Run Diagnostic Automatically

AXV11-C Jumpers	ADV11-C Jumpers	Jumper Function
A8, A12	A8, A12	Standard address, 170400
V8	V8	Standard interrupt vector 400
4D, 6D, 6E	4D, 6D, 6E	Offset binary notation
D2 to D3	D2 to D3	±10 V
P1 to P2, P8 to P9	P1 to P2, P8 to P9	Enable single-ended inputs
P6, P7	P6, P7	Enable programmable gain feature
3A to 5A		Bipolar DAC A operation
1B to 5B		Bipolar DAC B operation
2F 1C to 2C	2F	External trigger enable

6.4 SET-UP PROCEDURE FOR USING ANALOG TEST FIXTURE

Use the following procedure to set up the analog board for calibration using the analog test fixture. The test fixture provides a voltage to each of the A/D input channels, as shown in Table 6-2. The test fixture also has connections for RTC IN and EXT TRIG.

1. Install the extender board in the backplane in the slot following the LSI-11 bus configured boards.

2. Insert the AXV11-C (or ADV11-C) analog board into the extender board.

3. Connect the 26-pin ribbon cable between J1 of the analog board and J1 of the analog test fixture.

4. Turn on the LSI-11 system and boot the disk drive with the CVAXA diagnostic diskette installed.

6.5 STARTING THE TEST

Load the CVAXA diagnostic. When started the diagnostic asks some questions that the operator must answer about the configuration of the analog system and if a test fixture is installed. For example:

Single-ended? **Y**
2's complement? **N**

Table 6-2 A/D Input Voltages From Test Fixture

Analog System	Channel Number	Input Voltage
ADV11-C only	0, 4, 8	+ full scale
	1, 5, 9	+ 1/2 full scale
	2, 6, 10	+ 1/4 full scale
	3, 7	+ 1/8 full scale
	11, 12 13, 14, 15,	0 V
ADV11-C with AAV11-C	0, 4, 10	+ full scale
	1, 5, 11	+ 1/2 full scale
	2, 6, 12	+ 1/4 full scale
	3, 7	+ 1/8 full scale
	13	+ full scale
	14 (AAV11-C DAC A)	Variable
	15 (DAC B)	with AAV11-C
	16 (DAC C)	output.
	17 (DAC D)	
AXV11-C only	0, 4, 8 (DAC A input)	+ full scale
	1, 5, 9	+ 1/2 full scale
	2, 6, 10	+ 1/4 full scale
	3, 7	+ 1/8 full scale
	11 (DAC B input)	+ full scale
	12, 13 14, 15,	0 V
AXV11-C with AAV11-C	0, 4, 10 (AXV11-C DAC A)	+ full scale
	1, 5, 11	+ 1/2 full scale
	2, 6, 12	+ 1/4 full scale
	3, 7	+ 1/8 full scale
	13 (AXV11-C DAC B)	+ full scale
	14 (AAV11-C DAC A)	Variable
	15 (AAV11-C DAC B)	with AAV11-C
	16 (AAV11-C DAC C)	output.
	17 (AAV11-C DAC D)	

The answers control running certain tests, and the answers must be correct or errors will be reported. A list of tests, shown in Table 6-3, prints on the terminal, followed by a message to type the letter or number of the test to be run, then press **RETURN**.

If **W** is typed, the diagnostic runs through the analog test and wrap-around test. The analog test verifies the correct operation of the A/D input multiplexer. The test fixture, if installed, supplies a voltage to each of the input channels. The actual converted value is compared to the expected value. If the actual exceeds the tolerance allowed, an error is reported.

If an AXV11-C is being tested, the diagnostic also verifies the operation of the two DACs on the board. The DACs are connected to A/D channels 0 and 13. The diagnostic loads each DAC and verifies the D/A output values.

If the AAV11-C is being tested, the diagnostic verifies the operation of its four DACs. They are connected to A/D channels 14–17. The diagnostic loads each DAC and verifies the D/A output values.

If an **L** is typed, the diagnostic executes the logic test. The logic test has 21 subprograms to test the functions of the A/D analog input board. The subprograms run sequentially without any other action. This test can be run as a quick check to test the integrity of the board.

If an **A** is typed, the diagnostic executes the logic test and wrap-around test.

If **1–7** is typed, the diagnostic executes one of seven I/O subtests and does not stop until terminated by the operator, by typing **CTRL C**. The I/O subtests run continuously to allow the operator to verify the output of an A/D board, print a converted value, or monitor an output signal. A/D calibration and board configuration can be checked. (See Paragraph 6.6).

At the end of a pass, the following printout occurs.

END PASS 1

Table 6-3 AXV11-C/ADV11-C Diagnostic Tests

Type	Test	Function
W	Wrap-around test	Performs analog subprograms to test A/D input multiplexer. Compares actual values to the voltages expected from text fixture. Verifies operation of DACs. Requires test fixture.
L	Logic test	Checks logic functions of A/D module.
A	Auto test	Performs logic test and wrap-around test. (Requires test fixture)
1	Print values of selected input channel and gain.	This test allows the operator to calibrate the A/D converter or to verify the input voltage.
2	Print values of scanned analog input channels and gain.	The operator can see the converted value across all channels and gains.
3	AXV11-C A/D input echoed to AXV11-C D/A output.	This test converts the analog voltage on a selected channel into digital data and loads the results into the AXV11-C D/A outputs.
4	AXV11-C D/A ramp	This test loads a ramp pattern into the D/A output registers and allows the operator to see the output levels of the AXV11-C DACs.
5	AXV11-C D/A calibration	This test loads the maximum negative full-scale code to the DACs. With a digital volt meter, the operator checks the output voltage. Pressing RETURN causes the test to load the midscale value. Pressing RETURN again causes the test to load the maximum full-scale code in the DACs.
6	AXV11-C D/A square wave	This test loads a square wave pattern in the DAC registers. The operator can monitor the output levels for distortion.
7	AXV11-C D/A output echoed to A/D input	This test loads a count pattern into the D/A registers. The D/A output is connected to the A/D input. The resulting printout shows the tracking of output to input codes.

6.6 CALIBRATING THE A/D CONVERTERS

Use the following procedure to calibrate the A/D converters on the AXV11-C or ADV11-C boards.

1. Connect the floating outputs of the voltage standard to the V SOURCE jacks on the analog test fixture as follows.

Voltage Standard	Analog Test Fixture
−Output	HI (red jack)
+Output	LO (black jack)

2. Set switch S1 on the test fixture to EXT REF.

3. Set the voltage standard to +9.9976 V.

4. Start Test 1 of the CVAXA diagnostic on Channel 0 mode 0.

CAUTION

When calibrating the A/D converter module on the analog board, do not adjust the potentiometer marked PG ZERO. This potentiometer is set at the factory for the programmable gain feature and should not be adjusted in the field.

5. On the side of the A/D converter module, Figure 6-2, adjust the ZERO potentiometer so the diagnostic printout is between 00000 and 00001.

6. Reverse the outputs from the voltage standard to the analog test fixture as follows.

Voltage Standard	Analog Test Fixture
−Output	LO (black jack)
+Output	HI (red jack)

7. Set the voltage standard to +9.9878 V.

8. Adjust the FULL SCALE potentiometer on the A/D module so the diagnostic printout is between 7776 and 7777.

9. Halt Test 1 by typing **CTRL C**.

6.7 CALIBRATING THE D/A CONVERTERS

Use the following procedure to calibrate the D/A converters on the AXV11-C.

1. Connect the digital volt meter (DVM) to the D/A A output pin on the test fixture (near the V SOURCE jacks).

2. Start Test 5 of the CVAXA diagnostic and select the channel number for the DAC on the board being calibrated. See Table 6-2.

3. Press **RETURN** on the terminal until approximately −10 V is read on the DVM.

4. Adjust the ZERO OFFSET ADJ A potentiometer on the analog board until exactly −10.0000 V is read.

5. Press **RETURN** on the terminal until approximately +10 V is read.

6. Adjust the FS RANGE ADJ A potentiometer until +9.9951 V is read.

7. Repeat procedure for DAC B, connecting DVM to D/A B output pin on the test fixture.

8. To halt Test 5, type **CTRL C**.

9. Start Test 4 of the CVAXA diagnostic and monitor the output of D/A A and D/A B with an oscilloscope. Their output should be a smooth waveform, as shown in Figure 6-4. Type **CTRL C** to stop Test 4.

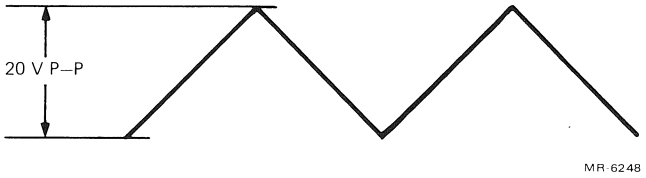


Figure 6-4 DAC Ramp Test Pattern

10. Start Test 6 of the diagnostic and monitor the outputs of D/A A and D/A B. Their outputs should be a square wave, as shown in Figure 6-5, indicating that no bits are missing. Type **CTRL C** to stop Test 6 completing the calibration procedure.

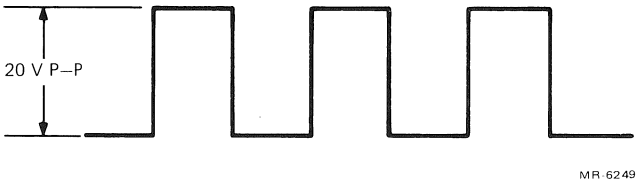


Figure 6-5 DAC Square Wave Test Pattern

6.8 ERROR REPORTING

When an error occurs, the diagnostic prints the following information.

ERRPC:	Location at which an error is detected
STREG:	Address of the control/status register
ADBUFF:	Address of the data buffer register
CHANL:	Channel number
NOMINAL:	Expected correct value
TOLERANCE:	Acceptable deviation from the nominal value
ACTUAL:	Actual data received
EXPECTED:	Expected correct data
SPREAD:	Actual deviation from the nominal value

GLOSSARY OF A/D WORDS

Absolute Accuracy – The analog error, given as a percent of the full-scale voltage, referenced to the National Bureau of Standards volt.

Acquisition Time – The time duration between the giving of the sample command and the point when the output remains within a specified error band around the input value.

Aperture Delay Time – The time elapsed between the hold command and the point at which the sampling switch is completely open.

Aperture Uncertainty – The change in aperture delay times between specific sample and hold commands.

Common Mode Rejection (CMR) – The ability of a differential amplifier to reject noise common to both inputs. Common mode rejection is given as a ratio, the Common Mode Rejection Ratio (CMRR). A differential amplifier with a gain of 10 and a CMRR of 80 dB (10,000:1) would have an output noise voltage of 0.5 μV if both inputs were 5 V.

$$dB = 10 \times \text{Log} \frac{V_{in} \text{ common mode}}{V_{out}/\text{Gain}}$$

Crosstalk – The amount of signal coupled to the output given as a percent of the input signal applied to all off channels.

Differential Inputs (True) – Two external signals applied to the input circuitry of an A/D system whereby the first is subtracted from the second. The difference is applied to the A/D system. This is used with twisted-pair wiring to lower noise pickup.

Example (see Figure G-1):

$$V_0 = (V+) - (V-)$$

$$= [V_1 + V(_1) \text{ noise}] - [V_2 + V(_2) \text{ noise}]$$

$$= [V_1 - V_2] + [V(_1) \text{ noise} - V(_2) \text{ noise}]$$

For twisted-pair wiring:

$$V(_1) \text{ noise} = V(_2) \text{ noise}$$

$$V_0 = V_1 - V_2$$

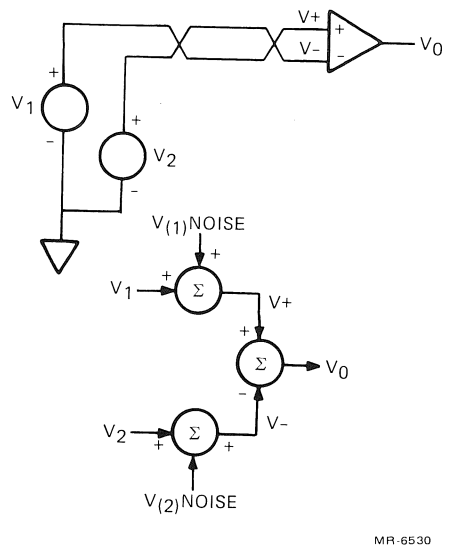


Figure G-1 Noise Cancellation with Differential Inputs

Differential Inputs (Pseudo) – This method of inputting is similar to true differential inputting except that the negative input to the A/D system is common to the other inputs.

Differential Linearity – The maximum deviation of an actual stated width from its theoretical value for any code over the full range of the converter. A differential linearity of $\pm 1/2$ LSB means that the width of each code over the range of the converter is 1 LSB $\pm 1/2$ LSB. Missing codes in an A/D converter occur when the output code skips a digit. This occurs when the differential linearity is worse than ± 1 LSB.

Drift – Drift is a function of the temperature coefficients of the components. It is the main cause of gain and offset errors.

Gain Error – The gain error is the percent by which the actual full-scale range differs from the theoretical full-scale range. This error is adjustable to zero.

Gain Temperature Coefficient – This is the amount of gain that changes with a change in temperature. This may be given in ppm/°C or °C/LSB at full scale. If an A/D has a gain temperature coefficient of 20° C/LSB at F.S., the A/D converted value will be off by 1 LSB at full scale if the temperature raises 20° above 25° C.

Input Bias Current – The amount of current that flows into the selected A/D channel from the source.

Input Impedance – The resistance seen at the input to an A/D system.

Linearity – Linearity is defined as the maximum deviation from a straight line drawn between the end points of the converter transfer function. Linearity may be given as a percent of full scale or as a fraction of an LSB.

Multiplexer – The multiplexer is a set of electronic switches that allow analog data from different channels to be given at different times to the sample and hold circuit or A/D converter.

Multiplexer Settling Time – When switching channels, the settling time is the maximum time needed to reach a specified error band around the input value.

Offset Error – The error by which the transfer function fails to pass through zero. This is usually adjustable to zero.

Quantization Error – Quantization error is the error allowed when digitizing an analog signal, due to the finite resolution of an A/D converter. An ideal converter has a maximum quantization error of $\pm$ 1/2 LSB.

Relative Accuracy – This is defined as the input-to-output error as a fraction of full scale with gain and offset errors adjusted to zero. Relative accuracy depends on linearity.

Resolution – The resolution of an A/D converter is defined as the smallest analog change that can be identified. Resolution is the analog value of the least significant bit (LSB).

$$\text{Resolution} = \text{LSB} = \frac{\text{Full-scale range}}{\text{Total code combinations}}$$

For example, if a system needs a weight measurement range of 10,000 lb, measured to the nearest 3 lb.

$$\text{Total Code Combinations} = \frac{10{,}000}{3\text{ lb}} = 3333 \text{ code combinations (minimum required)}$$

The A/D converter used has a resolution of 12 bits binary. The weight resolution for this example is computed using 12 bits as follows.

$$\text{Resolution} = 1\text{ LSB} = \frac{\text{Full-scale range}}{2^{12}\text{ code combinations}} = \frac{10{,}000}{4{,}096} = 2.4\text{ lb}$$

Sample and Hold Circuit – In order to make sure that the input voltage does not change during a conversion, a sample and hold circuit is needed. If the change during a conversion cycle is less than 1/2 LSB, then a sample and hold circuit is not needed.

Example:

Conversion Speed = 20 μs
Full-Scale Input Range (FSR), where $\omega_{max} = 2\pi(BW)$
Converter Resolution = 10 bits
LSB Value = .01 V/bit
1/2 LSB = 0.005 V

Maximum slew = 0.005 V/20 μs = 250 μV/μs = 250 V/s
(Rate needed for no sample and hold)

for $e_{in} = 1/2$ (FSR) $\sin \omega t$

then $de/dt = (1/2)\,\omega$ (FSR) $\cos \omega t$

$\therefore |de/dt|_{max} = (1/2)\,\omega_{max}(FSR) = (BW)(FSR)$,
where $\omega_{max} = 2\pi(BW)$

or 250 V/s = π (BW)(FSR)

BW = 250 V/s/π(10.24 V) = 7.77 Hz

Slew Rate – The capability of the output of an analog circuit to change its voltage in a given period of time. If the slew rate is 7 V/μs, the analog circuit output will change seven volts in one μs.

Successive Approximation – A method that is used to change the analog signal to a digital number. With this method, an analog signal is compared to a logic-generated signal. (See Figure G-2.) The logic always supplies a half-range signal at first as shown in Figure G-3 and Table G-1. For example, the input for the desired system is 7 V, and the full-scale input to the A/D converter is 10 V.

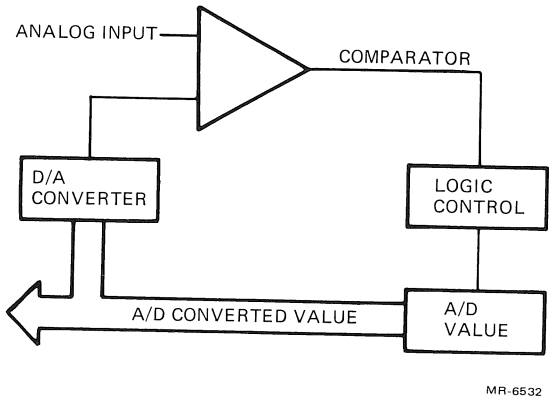


Figure G-2 Analog Circuit for Successive Approximation

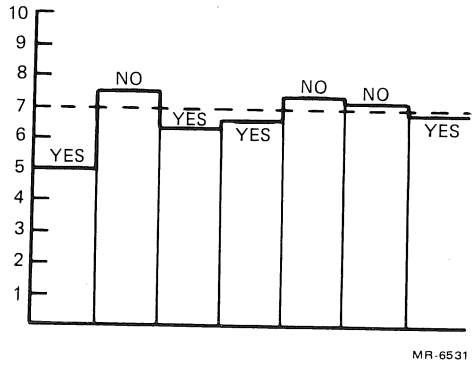


Figure G-3 Successive Approximation Decision Diagram

Table G-1 Example of Using Successive Approximation

Add	New Logic Voltage	Is the Input Greater Than New Voltage	A/D Buffer Bits	Decision	A/D Register Value*
5 V	5 V	Yes	6	Add +5 = +5	1000000
2.5 V	5 + 2.5 V	No	5	Do nothing	1000000
1.25 V	5 + 1.25 V	Yes	4	Add 1.25 = 6.25	1010000
0.625 V	6.25 + 6.25 V	Yes	3	Add 0.625 = 6.875	1011000
0.3125 V	6.875 + 0.3125 V	No	2	Do nothing	1011000
0.15625 V	6.875 + 0.1562 V	No	1	Do nothing	1011000
0.017125 V	6.875 + 0.078125 V	Yes	0	Add 0.078175	1011001

*This example uses a 7-bit A/D converter, where 011001 = approximately 7 V in 10 V full-scale range.

System Throughput – The system throughput is the rate of processing A/D data. It is dependent on the sampling speed needed to recover the data and the highest frequency component of the data.

In theory, the system throughput is based on the Nyquist sampling theorem, which states that a minimum of two samples per cycle are needed to completely recover continuous signals in an environment without noise. In typical devices, noise occurs, and 5 to 10 samples per cycle are needed.

For applications with dc and very low frequency signals, the sample rate is usually a multiple of the powerline frequency to provide almost infinite rejection of these frequencies.

The minimum sampling speed is the number of samples per cycle multiplied by the highest frequency component of the data. For time-multiplexed systems, the sampling speed needed is dependent on the system throughput, which is determined from data bandwidth, the number of channels, and the sampling factor using the following formula.

System throughput = N × n × (BW) samples/second

N = number of samples/cycle (sampling factor)
n = number of channels
BW = largest bandwidth of any channel

Example:

A system has three channels with the following bandwidths.

Channel 1 bandwidth: 100 Hz
Channel 2 bandwidth: 200 Hz
Channel 3 bandwidth: 250 Hz

N = 10
n = 3
BW = 250 Hz

The system throughput is computed as follows.

System throughput = 10 × 3 (250) = 7500 samples/second

In practice, the A/D system throughput is based on the following times.

Multiplexer settling time
Sample and hold settling time
A/D conversion time
A/D recovery time
Computer acquisition time (Software)

The system throughput = 1 ÷ total time, given in samples per second.

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