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AA11-K
4-channel D/A and display control user's manual

digital

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4-channel D/A and display control user's manual

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CONTENTS

CONTENTS (Cont)

ILLUSTRATIONS

TABLES

CHAPTER 1
INTRODUCTION

1.1 DESCRIPTION

The AA11-K includes four digital-to-analog converters (DACs) and an associated display control.

The display control permits the user to display data in the form of a 4096 × 4096 dot array. Under program control, a dot may be produced at any point in this array, and a series of these dots may be programmed sequentially to produce graphical output.

The display control may output to chart or X/Y recorder or CRT display unit. Normal configuration calls for its use with a VR17 CRT Display Monitor. However, it is capable of operating with other equipment, such as the Tektronix 602, 604 display oscilloscopes and 611, 613 storage oscilloscopes.

The AA11-K has four 12-bit DACs, each driven from a 12-bit buffer register, and circuitry that provides all controls necessary to output the analog signals to an external oscilloscope. Digital-to-analog (D/A) output is nominally ±5 V; however, this can be set to ±0.5 V or ±10 V.

Outputs are capable of driving up to 5000 pF of load.

Output operations are accomplished by loading the Display Status register and the D/A Buffer registers. Through use of Display Status register bits, the user can intensify the contents of the D/A Buffer registers, provide delays necessary for some oscilloscope applications; provide erase, write-through,

AA11-K FEATURES

- A 4-channel independently buffered 12-bit digital-to-analog converter
- Oscilloscope control logic for the four digital-to-analog channels
- 4096 × 4096 dot matrix capabilities
- Oscilloscope control signals available for controlling a variety of oscilloscopes, charts, and X/Y recorders
- Bipolar output ranges of ±5 V, ±10 V, ±0.5 V
- A quad-sized module that interfaces directly to the PDP-11 Unibus
- Status register control of intensify, write-through, non-store, and erase functions to provide flexibility for oscilloscope or other device control

and non-store control functions for storage oscilloscope applications, and enable interrupt on completion of oscilloscope intensification, erase, and external delay. The display control offers four program-controlled modes in which the oscilloscope can intensify a point. Jumpers provide additional display control flexibility by allowing the user to select the desired delay, intensification pulse polarity, magnitude, and duration.

1.2 BLOCK DIAGRAM

Figure 1-1 is a block diagram of the AA11-K. All the circuitry is located on the A638 4-Channel DAC module.

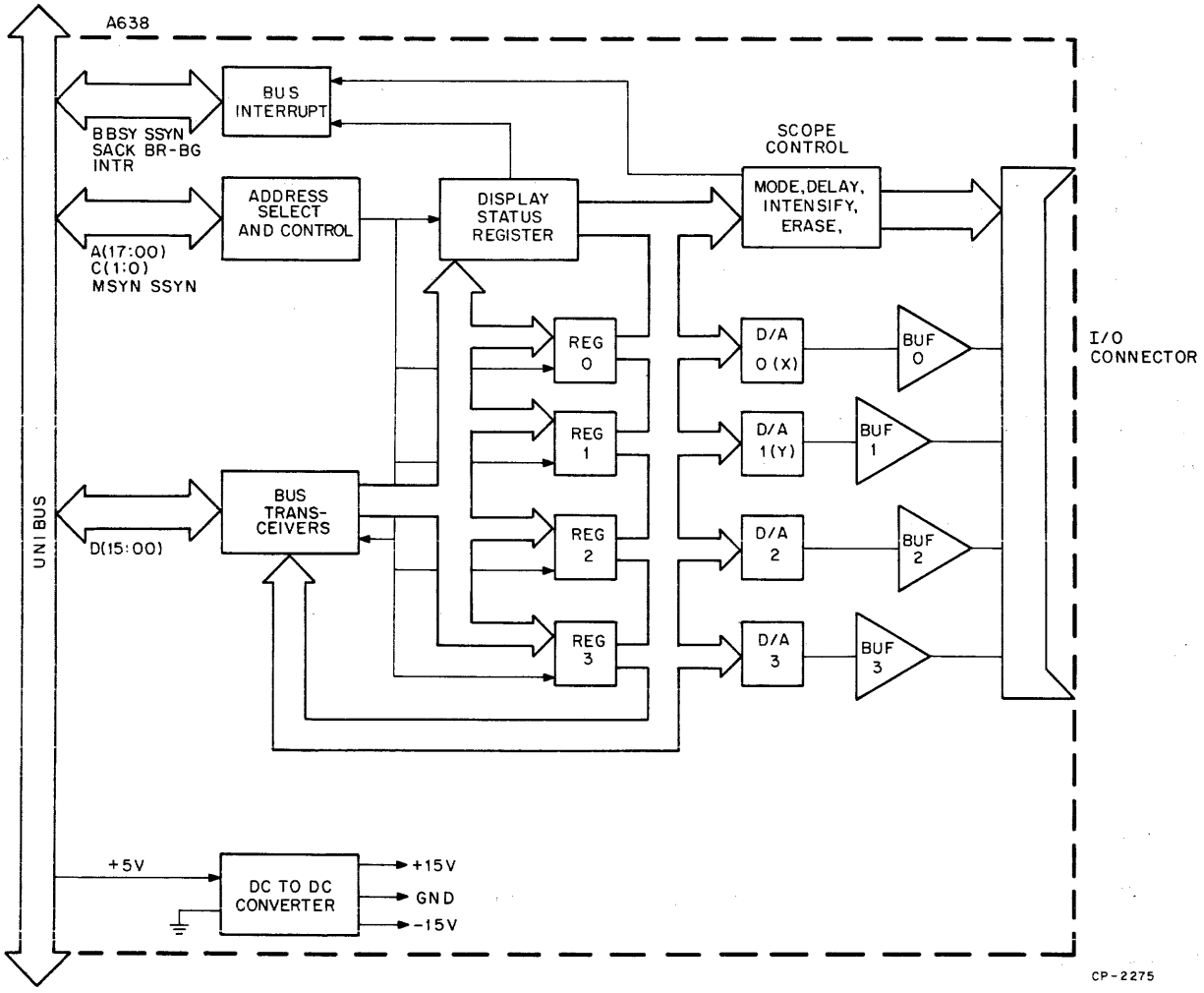

Figure 1-1 AA11-K Block Diagram

1.3 AA11-K SPECIFICATIONS (@±5 V RANGE)

Number of DACs	4
Digital Input	12 bits bipolar, straight binary; jumperable to 2's complement
Digital Storage	Read-write, word operable, single buffered
Output Voltage	±5 V; ±10 V, ±0.5 V jumperable
Resolution	1 part in 4096 of full range
Warmup Time	5 minutes minimum
Gain Accuracy	Adjustable
Gain Drift	10 ppm/° C maximum
Offset Accuracy	Adjustable
Offset Drift	20 ppm of F.S./° C maximum
Linearity	±1/2 LSB maximum
Differential Linearity	±1/2 LSB maximum, monotonic
Output Impedance	1 Ω maximum at D/A output
BC08R-08 Cable Impedance	4 Ω maximum
Drive Capability	±5 mA maximum per DAC
Slewing Speed	5 V/μs
Rise and Settling Time to 0.1% of final value	4 μs, 8 μs with 5000 pF load in parallel with 1 kΩ
Intensify	
INTENSIFY Pulse Width	2 μs; 6 μs in store mode
INTENSIFY Pulse Magnitude	3.3 V; 1.4 V jumperable
INTENSIFY Pulse Polarity	Jumperable (negative normally)
Intensification Delay	1. 3 μs in fast intensify mode 2. 20 μs; 80 μs jumperable 3. Externally determined by DELAY RETURN L

Logic Outputs	
NON-STORE L, WRITE THRU L, ERASE L, READY L	TTL open collector
BIT 9 L	TTL open collector, 1K pullup to +5 V
Logic Inputs	
ERASE RETURN L	Compatible with Tektronix 611, 613
DELAY RET L	TTL Input
Power Consumption (from processor power supply)	5 V ±5% @ 2.5 A
Environmental Specifications	Meet DEC STD 102, Class B*
Packaging	One Quad (11 in. × 8.5 in.) module
Unibus Interface	
Interrupt Vector Address	360
Priority Level	4
Bus Loading	1 bus load
Mounting	In any SPC slot

1.4 PROGRAMMING

Programming the AA11-K is accomplished through the Display Status register and the D/A Data registers. One hardware interrupt vector is associated with the display control.

1.4.1 Display Status Register

The Display Status register is a read/write register and is byte operable. The bit map is shown in Figure 1-2 and described in Table 1-1.

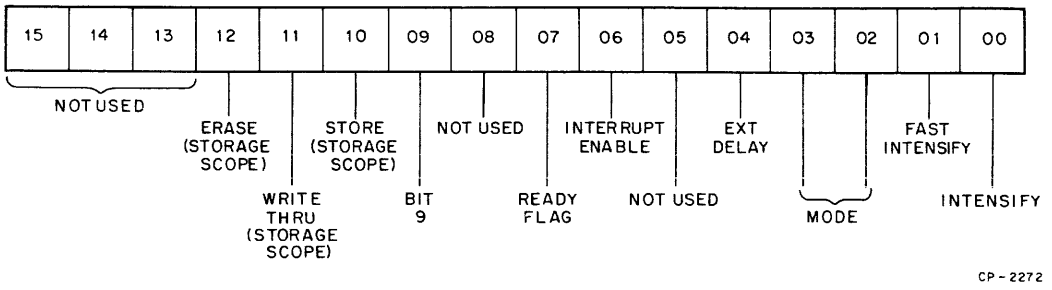

Figure 1-2 Display Status Register Format

*Class B Environment - Temperature 10° C (50° F) to 110° C (104° F); relative humidity 10% to 90%.

Table 1-1 Display Status Register

Bit	Name	Meaning and Operation
15–13	Unused	
12	Erase (write only)	Bit 12 = 1, erase data in the storage oscilloscope (write only).
11	Write Thru (read/write)	Bit 11 = 1, an intensified point will not be stored even though the user is in the store operation. (Works with WRITE THRU input of the oscilloscope.)
10	Store (read/write)	Bit 10 = 1, all intensified points will be stored. INTENSIFY pulse width increased from 2 to 6 μs.
09	Bit 09 (read/write)	A digital signal available to the I/O connector.
08	Unused	
07	Ready Flag (read only)	Bit 07 = 0, the oscilloscope is not ready, do not load or intensify points. Bit 07 = 1, the oscilloscope is ready.
06	Interrupt Enable (read/write)	Bit 06 = 1 and bit 07 in transition from a 0 to a 1 will cause an interrupt.
05	Unused	
04	EXT DELAY (read/write)	When bit 04 = 1, all internal timing stops and READY signal at the I/O connector goes low. When the external device (oscilloscope or XY recorder) returns a DELAY RET signal, an intensify pulse will be generated and the Ready flag will be set.
03, 02	Mode (read/write)	
	00 Normal	Intensification with bit 00 in SR
	01 X Mode	Intensification on loading X D/A (D/A 0)
	10 Y Mode	Intensification on loading Y D/A (D/A 1)
	11 XY Mode	Intensification on loading X or Y D/A.
01	Fast Intensify Enable (read/write)	Bit 01 = 0, all oscilloscope settling delays are as defined for each oscilloscope. Bit 01 = 1, settling delay is 3 μs.
00	Intensify (write only)	Bit 00 = 1, generates an intensify pulse in mode 00.

Interrupts occur when bit 06, Interrupt Enable, is set and bit 07, Ready Flag, sets. Bit 07 sets when an INTENSIFY pulse occurs or when an erase operation is complete. The Ready flag notifies the user that all delays (including EXTERNAL DELAYS) and operations are complete.

A point may be intensified in any of four control modes, selected by bits 02 and 03. In mode 0, a point is intensified by setting bit 00. Mode 1 intensifies a point upon loading the X D/A register; mode 2 intensifies a point upon loading the Y D/A register; mode 3 intensifies upon loading either the X or Y D/A register.

1.4.2 D/A Data Registers

The D/A Data registers are read/write registers; they are word operable. The data format of these registers is shown in Figure 1-3. See Paragraph 3.3.4 for digital input code.

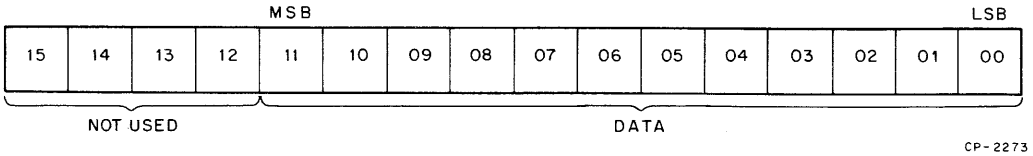

Figure 1-3 D/A Data Registers Format

When the display control is used with an oscilloscope grid, the coordinate scheme shown in Figure 1-4 is used. The display takes the form of a 4096 × 4096 dot array. Under program control, a bright spot is momentarily produced at any point in this array.

STANDARD* REGISTER ADDRESSES

Register	Address
Status	770416
X-D/A 0	770420
Y-D/A 1	770422
D/A 2	770424
D/A 3	770426

*The register address is switch-selected in increments of 40 locations. However, the relative location of the various registers will remain the same.

VECTOR ADDRESSES AND PRIORITY LEVELS**

Address	BR Level
360	4

**The vector address field is switch selectable from 010 to 770 in increments of 10.

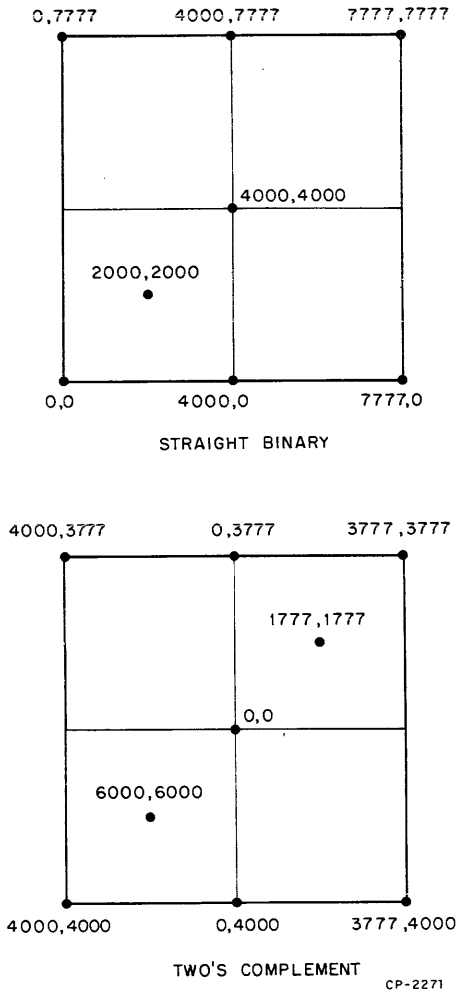

Figure 1-4 Oscilloscope Grid Coordinates

CHAPTER 2
OPERATION

2.1 OSCILLOSCOPE CONTROL DESCRIPTION

Point plotting on an oscilloscope or X-Y recorder is done by providing the desired voltage to the X and Y inputs, setting the beam or the pen in the desired spot.

After allowing time for the X-Y amplifiers to settle, an INTENSIFY (Z) pulse intensifies the positioned beam or a digital signal lowers the pen to plot a point.

By repeating the process of position/intensify, alphanumeric and graphic information can be plotted.

The AA11-K controls the oscilloscope with the ERASE, WRITE THRU, STORE, READY and BIT 9 open-collector TTL signals provided at the I/O connector.

2.2 D/A CONVERTERS

The four DACs have 12 bits straight binary or 2's complement input and a bipolar output normally set to ±5 V. The outputs can be jumpered to provide ±10 V or ±0.5 V if needed. If voltages other than those provided are required, use the attenuator in the oscilloscope (or plotter).

2.3 MODES

The INTENSIFY (Z) pulse can be initiated in four ways, as determined by bits 02 and 03 in the Display Status register (refer to Figure 2-1).

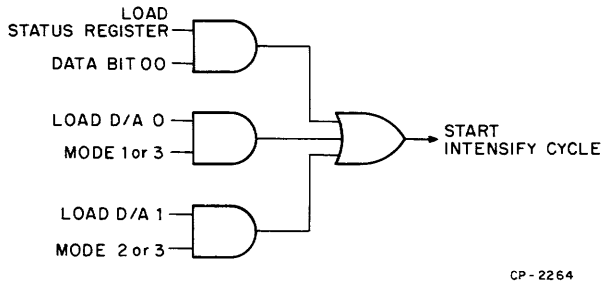

Figure 2-1 Intensify Logic Simplified

a. Mode 0 - Loading bit 00 into the Display Status register will generate a Z pulse after the provided delay.

b. Mode 1 - Loading D/A 0 Data register causes an Intensify cycle to start.

c. Mode 2 – Loading D/A 1 Data register causes an Intensify cycle.

d. Mode 3 – Loading either D/A 0 or D/A 1 will start the Intensify cycle.

The plot needed determines the mode best suited. For a stationary blinking cursor, use mode 0; for horizontal lines, use mode 1, etc.

2.4 DELAYS

Various oscilloscopes (or plotters) need different settling delays for their X-Y amplifiers.

A 20-μs delay is normally provided by the oscilloscope control delay circuit, shown in Figure 2-2. This delay can be jumpered to 80 μs if needed.

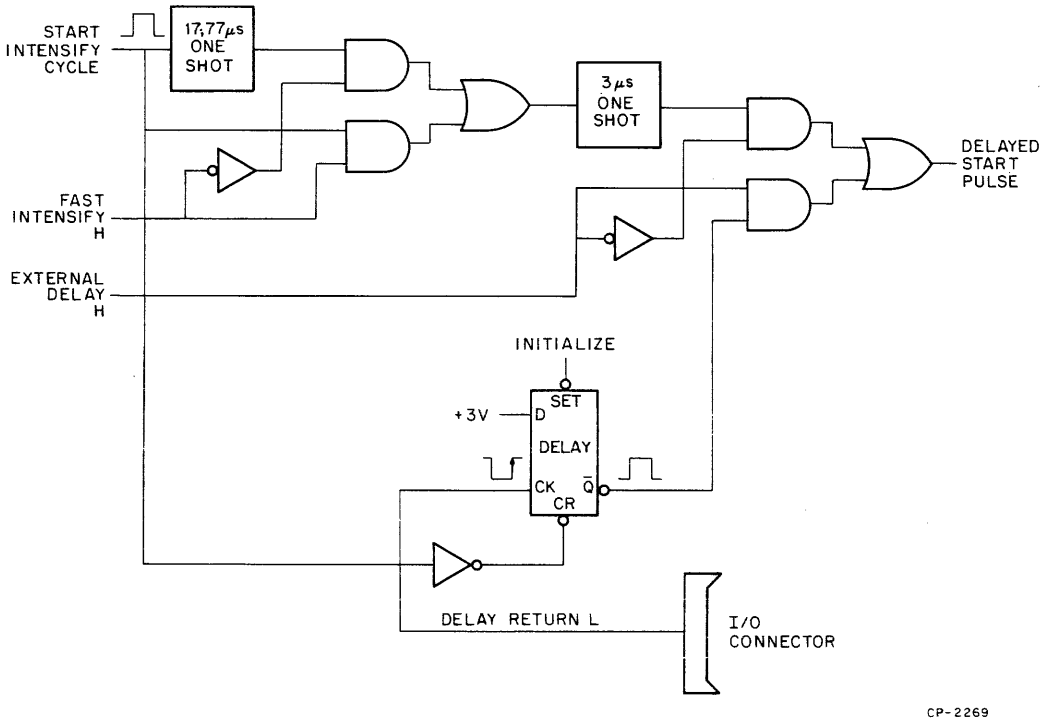

Figure 2-2 Delay Circuit Simplified

The AA11-K provides a 3-μs delay in Fast Intensify mode (bit 01 in the Display Status register is set) for very fast displays or small increments on a slow oscilloscope.

Delays longer than 80 μs can be accommodated by the External Delay mode (bit 04 in the Display Status register is set).

In this mode, an Intensify cycle is started in the AA11-K and halted pending a low-to-high transition supplied by the oscilloscope to the DELAY RETURN input.

2.5 INTENSIFY (Z) PULSE

The width of the pulse is normally 2 μs. In Store mode (bit 10 in the Display Status register set), the pulse width is increased to 6 μs.

The pulse can have positive or negative polarity (jumper selectable) and jumper selectable amplitude. The INTENSIFY (Z) pulse circuit is shown in Figure 2-3.

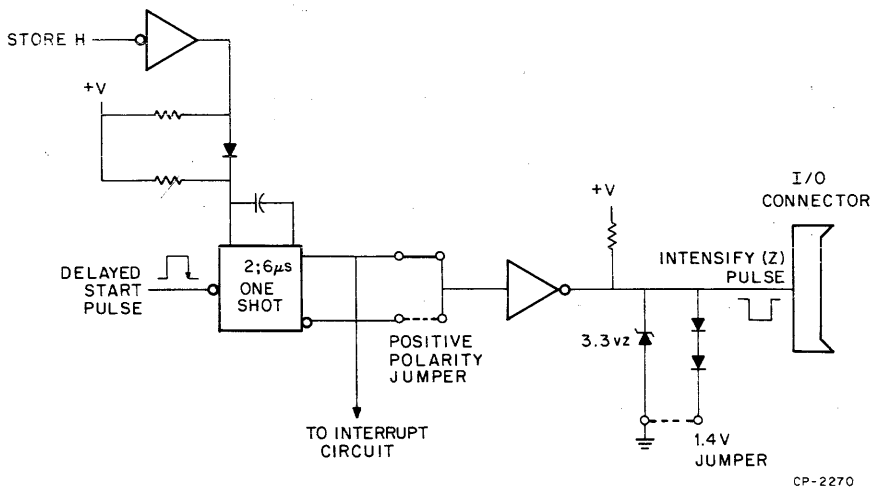

Figure 2-3 INTENSIFY (Z) Pulse

2.6 ERASE CYCLE

The erase cycle of a storage oscilloscope might take half a second.

The AA11-K will start an Erase cycle when bit 12 in the Display Status register is raised, and sense its completion as a low-to-high transition provided by the oscilloscope to the ERASE RETURN input of the AA11-K. After sensing the end of the Erase cycle, the processor can resume plotting.

2.7 INTERRUPT

The interrupt circuitry in the AA11-K is enabled by bit 06 in the Display Status register (refer to Figure 2-4).

The oscilloscope control interrupts the processor:

a. Whenever an Intensify pulse is generated, to notify the processor that the Intensify cycle with its delays (including EXTERNAL DELAY) are over, and the next point plot can be started.

b. At the end of an Erase cycle, to notify the processor that a new plot can be started.

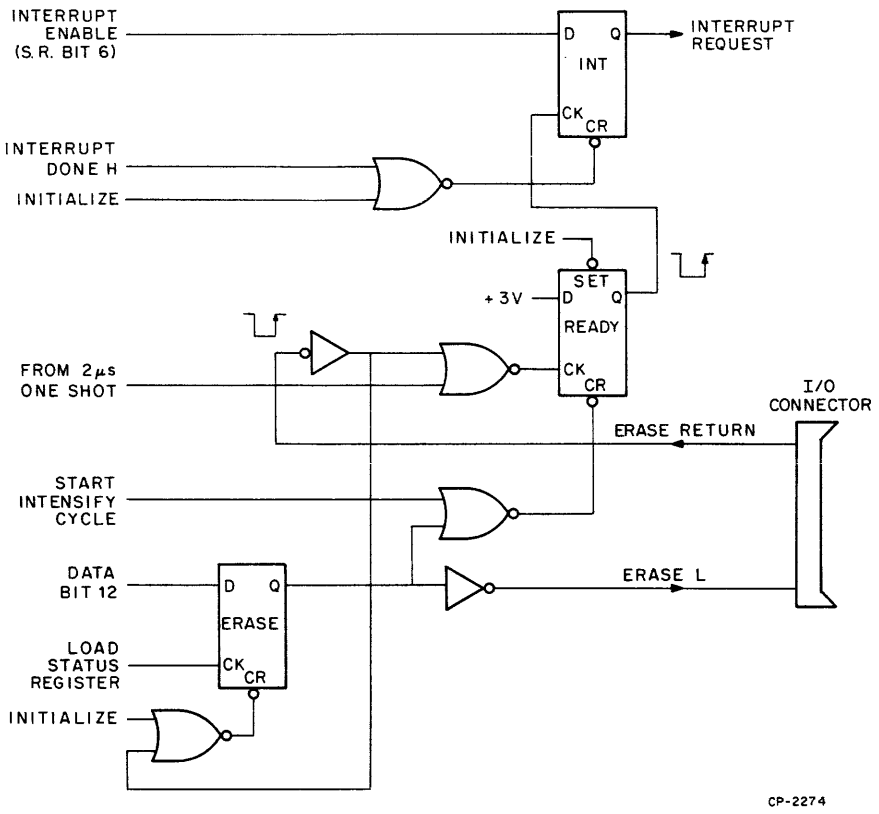

Figure 2-4 Erase Cycle Control

CHAPTER 3
INTERFACING

3.1 INTERFACE LOGIC SIGNALS

The AA11-K display control provides five programmable output logic levels: BIT 9 L, READY L, WRITE THRU L, NON-STORE L, and ERASE L. The AA11-K provides one output pulse, INTENSIFY, and accepts two logic inputs, ERASE RET L and DELAY RET L.

3.1.1 Electrical Characteristics

WRITE THRU L, NON STORE L, ERASE L, and READY L are open-collector contact closures to ground. These lines maintain a maximum output of 0.4 V while sinking 16 mA, and 0.7 V while sinking 40 mA. Maximum allowable output voltage (external pullup voltage) is 15 V. These output lines are compatible with the corresponding inputs of Tektronix 611 and 613 storage oscilloscopes.

BIT 9 L is a TTL-compatible output with 1K pullup resistor to +5 V. This line maintains an output of 0.4 V while sinking 11 mA, and 0.7 V while sinking 35 mA. It can drive seven TTL unit loads.

The INTENSIFY output pulse is TTL-compatible with jumper W27 disconnected (3.3 V, as shipped). This line can sink up to 20 mA and source up to 20 mA.

The ERASE RETURN L input line is specifically designed to interface with the Erase Interval signal of the Tektronix 611 storage oscilloscope or the Busy signal of the Tektronix 613 oscilloscope. This input can be driven from a standard TTL output.

The DELAY RET L is specifically designed for slow devices where the 20, 80 μs INTENSIFY delay is insufficient. It is TTL compatible.

3.1.2 Use of Logic Signals with Oscilloscopes

The output signal BIT 9 L is specifically intended to select channel 2 on the VR14 oscilloscope. This signal is driven by bit 09 of the Display Status register. When bit 09 is set (logical one), BIT 9 L is low, and channel 2 of the VR14 is selected. Since all Display Status register bits are initialized to 0, the VR14 is initially displaying channel 1, and channel 2 must be specifically programmed.

The WRITE THRU L output signal is intended for use with: the Write Thru input of the Tektronix 611 storage oscilloscope; Cursor input of the Tektronix 613 storage oscilloscope; or similar input of other storage oscilloscopes. When bit 11 of the Display Status register is set, WRITE THRU L is low, enabling the write through function of the storage oscilloscope. During write through, intensifying a point does not result in the point being stored. The point must be refreshed to be visible on the screen. This function is useful for finding the present beam position or for positioning movable cursors superimposed on a stored display.

The NON-STORE L output signal is intended to control whether or not intensified points are stored. It interfaces with the non-store input of Tektronix 611 and 613 storage oscilloscopes. When bit 10 (Store) of the Display Status register is set, NON-STORE L is high and intensified points are stored. Since Display Status register bits are initialized to 0, the system is initially in non-store mode.

The ERASE L output signal is intended to interface with the Erase inputs of Tektronix 611 and 613 storage oscilloscopes. When bit 12 of the Display Status register is set, ERASE L goes low, signaling the oscilloscope to begin an erase operation. The oscilloscope acknowledges the ERASE signal by means of an ERASE RET L signal (Erase Interval on Tektronix 611 storage oscilloscope or Busy on Tektronix 613 storage oscilloscope, connected to ERASE RET L on the AA11-K). The ERASE RET L signal clears bit 12 of the Display Status register, and ERASE L goes high. The ERASE RET signal stays low throughout the erase interval (0.5 second on the 611 and 0.9 second on the 613 oscilloscopes). At the completion of the erase operation, the low-to-high transition of ERASE RET L sets the Ready flag, bit 07 of the Display Status register. While ERASE RET L is low (during the erase operation), bit 12 of the Display Status register is held in the zero state, inhibiting further ERASE signals.

The DELAY RET L input is an indication from a slow oscilloscope that its amplifiers have settled.

The low-to-high transition of the DELAY RET L signal generates an INTENSIFY pulse which, in turn, sets the Ready flag and generates an Interrrupt if enabled.

NOTE
Information on interfacing with specific oscilloscopes is provided in Paragraphs 3.4.1 through 3.4.5.

READY L is brought to the I/O connector and is used to indicate the beginning of an External Delay cycle.

3.1.2.1 Other Uses of Logic Signals – The AA11's display control logic outputs can be thought of as general purpose outputs, for uses other than controlling oscilloscopes. In this context, the signals can be defined as in Table 3-1, in which the right-hand column refers to bits in the Display Status register.

Table 3-1 Output Signals

AA11-K Output Signal	Display Status Register Equivalent Signal Name
ERASE L	BIT 12L
WRITE THRU L	BIT 11L
NON-STORE L	BIT 10L
BIT 9 L	BIT 9L
READY L	BIT 7L

Of these signals, BIT 9 L is the most useful for TTL applications, since it has a pullup resistor to +5 V. The other four signals can be made directly TTL-compatible by means of an external pullup resistor to +5 V. If the open-collector outputs are used to drive relays or other inductive loads, provide suitable clamping diodes as shown in Figure 3-1 to ensure that the output voltage does not exceed 15 V on turn-off of the relays.

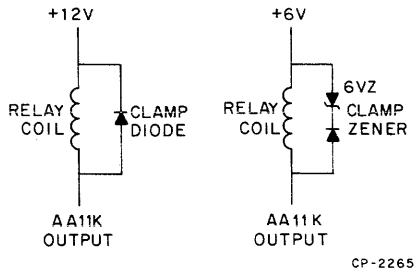

Figure 3-1 Clamping Circuits for Inductive Loads

3.1.3 Use with X/Y Recorders

With an X/Y recorder, one of the logic outputs is used to control a pen up/pen down signal. The X and Y D/A converters provide input to the X and Y channels of the recorder. Typically, recorders have a long delay between updating of analog inputs and readiness to display the new point (pen down). In general, this can be handled by a software delay (n passes through a loop) or by a real-time clock single-interval delay. Certain X/Y recorders provide an output signal that indicates the pen has settled. If this signal has a low-to-high transition when the pen has settled, it can be connected to the AA11-K DELAY RET L input.

When the pen has settled, the low-to-high transition of DELAY RET L generates an INTENSIFY pulse and resets the Ready flag causing an interrupt. The interrupt service routine lowers the pen to plot the point.

3.1.4 Use with Strip Chart Recorder

With a strip chart recorder, the four DACs provide analog input to four recorder channels. In some strip chart recorders, the motion of the paper (time axis) is controlled by a logic level that turns on a motor. In other recorders, the motion is controlled by logic pulses to a stepper motor, so that speed is a programmable function of pulse frequency. In either case, a single AA11-K logic output can be used to control the paper motion.

3.2 USER INTERFACING

3.2.1 Connections

The display control interfaces through Berg I/O connector J1 located on the A638 module shown in Figure 3-5. I/O connector pin assignments are listed in Table 3-2.

Table 3-2 I/O Connector Pin Assignments

Signal Name	Pin	Signal Name	Pin
LOGIC GND	A	LOGIC GND	B
HQ GND	C	INTENSIFY L	D
ERASE L	E	HQ GND	F
HQ GND	H	D/A 0 HQ GND	J
D/A 0 OUT	K	D/A 3 OUT	L
HQ GND	M	D/A 3 HQ GND	N
HQ GND	P	D/A 2 HQ GND	R
HQ GND	S	D/A 1 OUT	T
HQ GND	U	HQ GND	V
D/A 2 OUT	W	HQ GND	X
D/A 1 HQ GND	Y	HQ GND	Z
HQ GND	AA	HQ GND	BB
HQ GND	CC	LOGIC GND	DD
LOGIC GND	EE	WRITE THRU L	FF
ERASE RET L	HH	NON-STORE L	JJ
LOGIC GND	KK	LOGIC GND	LL
READY L	MM	-15V TEST	NN
BIT 9 L	PP	+15V TEST	RR
LOGIC GND	SS	DEL RET L	TT
+5V TEST	UU	LOGIC GND	VV

The AA11-K can be interfaced to the H322 Screw Terminal panel using the BC08R cable.

The H322 Screw Terminal assignments are listed in Table 3-3.

Table 3-3 H322 Screw Terminal Assignments

J4		J3		J2		J1	
1	BIT 9 L	1	HQ GND	1	INTENSIFY	1	HQ GND
2	LOGIC GND	2	HQ GND	2	LOGIC GND	2	HQ GND
3	+5V TEST	3	ERASE L	3	HQ GND	3	0 HQ GND
4	HQ GND	4	LOGIC GND	4	HQ GND	4	D/A 0 OUT
5	READY L	5	ERASE RET L	5	HQ GND	5	1 HQ GND
6	LOGIC GND	6	LOGIC GND	6	HQ GND	6	D/A 1 OUT
7	DELAY RET L	7	NON-STORE L	7	HQ GND	7	2 HQ GND
8	LOGIC GND	8	LOGIC GND	8	HQ GND	8	D/A 2 OUT
9	+15V TEST	9	WRITE THRU L	9	HQ GND	9	3 HQ GND
10	-15V TEST	10	LOGIC GND	10	HQ GND	10	D/A 3 OUT

3.2.2 Cables

The oscilloscope (analog output device) can be either grounded or floating. If the oscilloscope is grounded, either through its power plug or through contact between its chassis and a grounded cabinet, do not connect the oscilloscope ground to any of the AA11-K ground pins. Such a connection will result in a ground loop that may adversely affect display control results. If the oscilloscope is floating, connect its ground to the AA11-K logic ground, pin A of the I/O connector J1.

Oscilloscope X and Y inputs may be either differential or single ended. Differential inputs should be driven as in Figure 3-2.

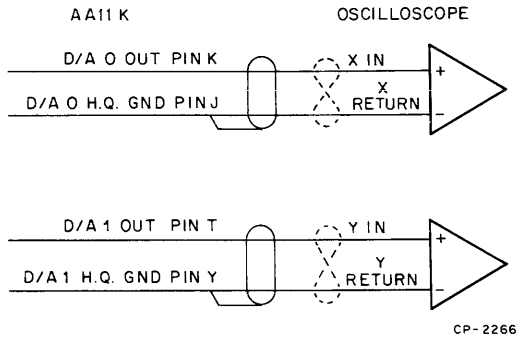

Figure 3-2 Connection to Oscilloscope with Differential Input

In driving oscilloscopes with single-ended inputs, the AA11-K analog grounds (pins J and Y) are not used. The return path for X and Y signal currents is through ground for a grounded oscilloscope or through logic ground (pin A) for a floating oscilloscope. Because the grounded, single-ended oscilloscope sees an input voltage that is the sum of the AA11-K output and the ground difference voltage between the oscilloscope and the AA11-K, noise and line frequency errors can be minimized by plugging the oscilloscope into an ac socket as close to the computer as possible. Running single-ended oscilloscopes in a floating configuration will eliminate noise and line frequency errors that are caused by ground voltage differences.

3.2.2.1 Twisted Pair Lines – The effect of magnetic coupling into the oscilloscope input lines can be minimized for a differential input oscilloscope by running the AA11-K output and its return line in a twisted pair. No benefit is derived from a twisted pair with a single-ended oscilloscope input.

3.2.2.2 Shielding – The effect of electrostatic coupling into the oscilloscope input lines can be minimized by shielding the input lines from the AA11-K to the oscilloscope. Connect the shield to ground only at one end. Grounding the shield at both ends will result in a ground loop that can adversely affect the DAC display.

3.2.2.3 Drive Capability – Careful selection of cabling is essential. The DAC outputs are capable of driving a maximum of 5000 pF. DAC output impedance is 1 Ω. BC08R-08 impedance (from AA11-K to H322) is 4 Ω. Output current limit is 5 mA.

3.3 OPERATIONAL SETUP

NOTE

Switch, jumper, and test point locations are shown in Figure 3-5.

3.3.1 Address Selection

The AA11-K address may be set between 760000 and 777740 (octal) in increments of 40 by means of switch S1. The preferred address is 770400. Set up the S1 switches as shown in Figure 3-3.

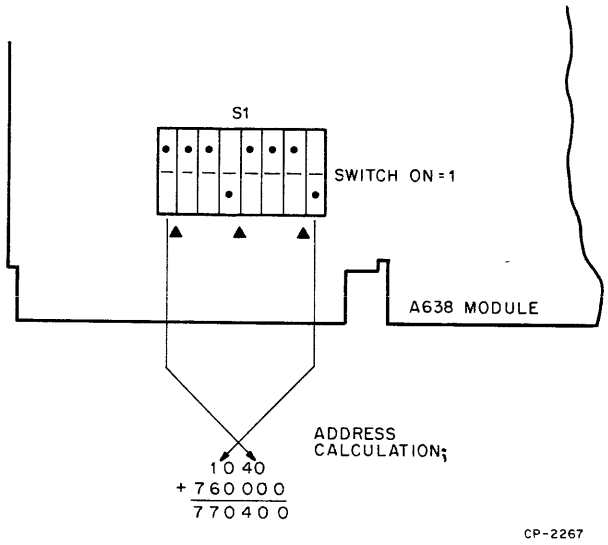

Figure 3-3 AA11-K Address Selection, Switch S1

3.3.2 Vector

The AA11-K vector space lies between 010 and 770, incremented in steps of 10 by means of switch S2. The preferred vector is 360. Set up the S2 switches as shown in Figure 3-4.

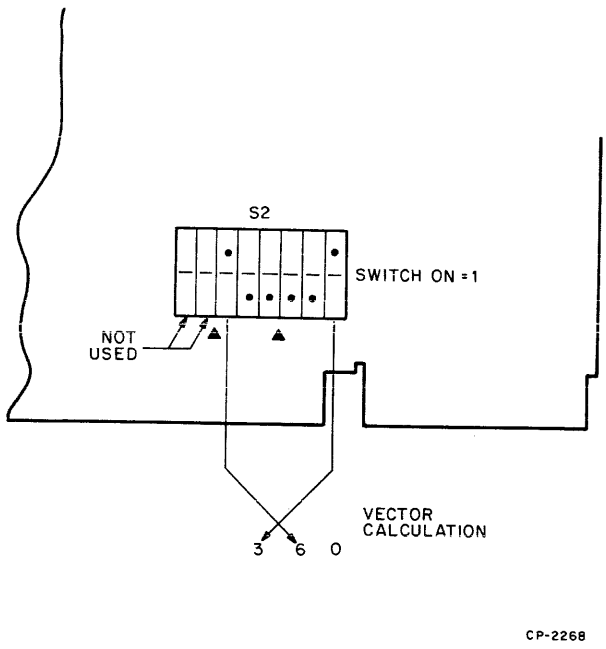

Figure 3-4 Vector Setup, Switch S2

3.3.3 Priority Jumper
The AA11-K is shipped with a level 4 priority jumper plug installed.

3.3.4 Digital Input Code
The digital input to the DAC can be either straight binary or 2's complement.

Output Voltage	Straight Binary	2's Complement
+F.S.	7777	3777
0 V	4000	0000
-F.S.	0000	4000

To configure all the DACs for 2's complement mode, remove jumper W1 and insert jumpers W30 and W32.

NOTE
When initialized, a 2's complement D/A register reads 4000.

3.3.5 Analog Output Range
The normal DAC output range is ±5 V. This may be changed to ±10 V or ±0.5 V by connecting the jumpers as shown in Table 3-4.

Table 3-4 Analog Output Range Selection

D/A Converters	Jumpers	Range ±5 V	±10 V	±0.5 V
0	W5 or W23	I	I	O
	W6 or W22	I	O	I
	W24	O	O	I
1	W7 or W20	I	I	O
	W8 or W19	I	O	I
	W21	O	O	I
2	W9 or W17	I	I	O
	W10 or W16	I	O	I
	W18	O	O	I
3	W11 or W14	I	I	O
	W12 or W13	I	O	I
	W15	O	O	I

I = IN
O = OUT

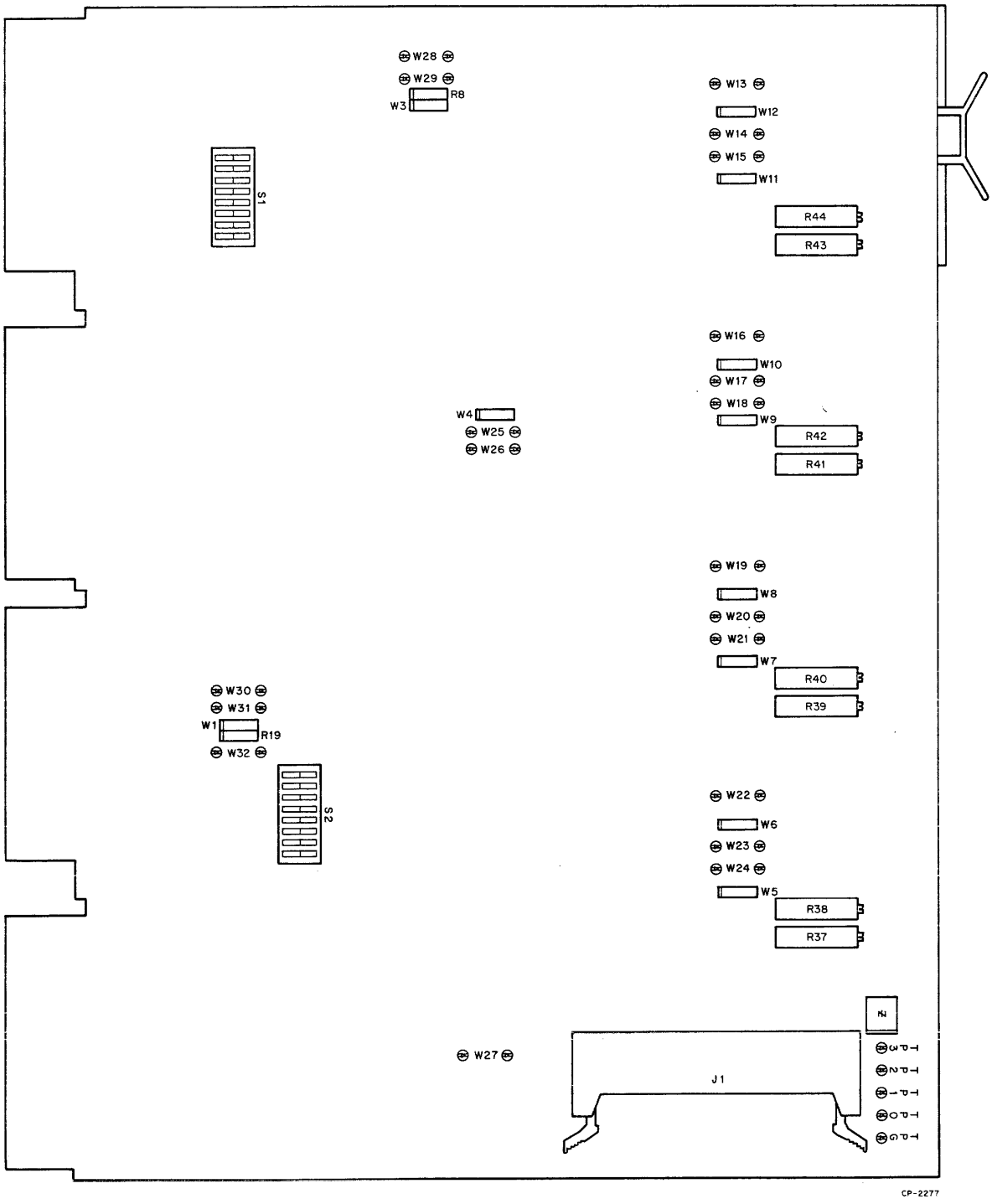

Figure 3-5 A638 Module, Locations of Switches, Jumpers, Potentiometers, and Test Points

For Offset and Gain adjustment, refer to Paragraph 3.5.1.

3.3.6 Intensification Delay

Normal intensification delay is 20 μs. This can be changed to 80 μs by removing jumper W3 and inserting W28.

3.3.7 INTENSIFY (Z) Pulse Polarity

Normally the INTENSIFY (Z) pulse is negative going. Cutting jumper W4 and inserting W26 yields a positive pulse.

Improper polarity results in erroneous signal blanking and visible retraces.

3.3.8 INTENSIFY Pulse Magnitude

Normal INTENSIFY pulse height is 3.3 V. Inserting jumper W27 yields a 1.4 V pulse.

3.4 INTERFACING SPECIFIC OSCILLOSCOPES

This section contains information on using the AA11-K to drive the VR17 and Tektronix 602, 604, and 613 oscilloscopes. The manufacturer's manual for the oscilloscope being used should be checked to obtain more information. Paragraph 3.1.2 provides general guidelines to be followed to interface with oscilloscopes other than those covered in the following paragraphs.

Some oscilloscopes may call for positive-only input voltage swings, with no means of adjustment for bipolar swings. In this case, it is necessary to use only eleven of the AA11-K D/A bits for positive excursions only. This provides 11-bit resolution, which is ample for most display applications. The AA11-K has a settling delay of 20 μs or 80 μs jumper selectable. For oscilloscopes other than VR17, 602, 604, 611, and 613, the user must determine whether either of these delays is adequate. If a settling time greater than 80 μs is required, the EXTERNAL DELAY or a software delay will be necessary.

3.4.1 VR17

The VR17 oscilloscope has differential analog inputs with ranges that can be internally adjusted for ± 5 V. Proper intensification delay is 20 μs. The intensification pulse is 3 V negative going, with 2-μs duration. The AA11-K is compatible with the VR17 as shipped, with no jumper changes required.

3.4.2 Tektronix 602

The Tektronix 602 has single-ended inputs with a nominal range of 0 to 1 V. This should be changed to ± 0.5 V by means of the position controls located on the front panel of the 602. The screen on the 602 is 8 cm (vertical) by 10 cm (horizontal). The user may choose to adjust the 602's vertical gain for ± 0.4 V full scale or ± 0.5 V full scale. At ± 0.4 V full scale, the AA11-K presentation is capable of overflowing the screen at top and bottom. At ± 0.5 V full scale, the AA11-K full-scale range does not overflow the screen, but a programmed square (n by n points) appears rectangular. If the 602 is left with ± 0.5 V inputs, the ± 0.5 V range should be set up on the AA11-K. As an alternative (which is preferable in noisy environments or if the oscilloscope is located away from the computer), the 602 inputs should be set for 10:1 attentuation per the instructions in the Tektronix 602 manual. With the 10:1 attenuators installed in the 602, full ± 5 V signals are used. The 20-μs intensification delay and 2-μs intensification duration are sufficient for the 602, so that W28 is not connected on the AA11-K. Because the 602 requires a positive-going 1 V intensification pulse, W4 should be cut and W26 and W27 should be connected.

3.4.3 Tektronix 604

The Tektronix 604 X and Y amplifiers can be used as differential inputs, when connected through rear panel BNC connectors, or as single-ended inputs when connected through the rear panel remote program connector. The differential input configuration provides superior performance in a noisy environment or at a distance from the computer. However, cabling into the BNCs may be somewhat difficult. Set the internal and vertical gain for either 8 V or 10 V full scale, depending on whether a square, overflowing or rectangular, non-overflowing display is desired. Set the position controls for zero corresponding to midscreen, so that ±5 V (or ±4 V vertical) results in full-scale deflection. The AA11-K is left at ±5 V output. An intensification delay of 20 μs is adequate with the 604. Because the 604 requires a positive-going intensification pulse, cut W4 and connect W26. The 604's intensification sensitivity is adjustable between 1 and 5 V. It must be set below 3 V, and W27 should remain disconnected, so that the AA11-K intensify output is 3 V.

3.4.4 Tektronix 611 Storage Oscillocope

The Tektronix 611 storage oscilloscope has single-ended inputs with 1 V range. This should be changed to a 10 V range by means of internal X10 attenuators, per instructions in the 611 manual. The X and Y positioning switches should be in the center position. This sets up the inputs for ±5 V, directly compatible with the AA11-K analog outputs. Intensification delay should be set for 80 μs. The 611 requires a positive-going intensification pulse (W4 disconnected, W26 connected). Because the 611's intensification threshold is nominally 1 V, the AA11-K INTENSIFY pulse should be left at 3 V. The 611's ERASE, NON-STORE, and WRITE THRU lines should be connected directly to the corresponding AA11-K outputs. The 611's Erase Interval signal should be connected to the AA11-K's ERASE RET L. The 611 contains a 500-ms timing circuit that controls its erase interval duration. This circuit requires another 500 ms of recovery time after the conclusion of the erase interval. If the user attempts to program another erase operation within 300 ms of the end of the previous erase operation, the timing circuit does not recognize the erase command. Under these conditions, ERASE RET L does not go low (the 611 fails to acknowledge the erase command). Therefore, the display control Ready flag does not get set, and it is possible for the program to hang up in a wait loop. If the user attempts to program another erase operation more than 300 ms but less than 500 ms after the previous erase operation, the erase command is recognized, but the erase interval duration is less than 500 ms, so that there may be incomplete erasure.

3.4.5 Tektronix 613 Storage Oscilloscope

The Tektronix 613 storage oscilloscope has differential inputs with 1 V range (and no easily settable X10 attenuator). Consequently, the AA11 must be run with a ±0.5 V output. The 613's horizontal and vertical "origin location" jumpers should each be in location 2 to set up the inputs for ±0.5 V. Intensification delay should be set for 80 μs. The 613 requires a positive-going intensification pulse (W4 disconnected, W26 connected). Because the 613's intensification threshold is nominally 1 V, the AA11-K intensification pulse should be left at 3 V. The 613's ERASE, NON-STORE, and WRITE THRU lines should be connected directly to the corresponding AA11-K outputs. The 613's BUSY signal should be connected to the AA11-K's ERASE RET L. The 613's Hard Copy Busy and Deflection Busy jumpers should be in their normal (inactive) position when used with the AA1-K to avoid setting the AA11-K's display control Ready flag at times other than the end of an intensification pulse or the end of an erase operation. The 613's erase interval timer does not have a recovery delay, so that no restriction is necessary on the interval between back-to-back erase operations.

3.5 TESTING AND CALIBRATION

The logic section of the AA11-K can be checked easily by loading and reading the four D/A Data registers and the Display Status register.

To check the analog section, test points are provided at the output of each DAC.

By using an accurate voltmeter or oscilloscope and loading the desired code into the D/A register, you can verify the functionality and calibrate the analog section of the AA11-K.

3.5.1 Offset and Gain Adjustment

Connect an accurate voltmeter to the output of the DAC.

Load the word indicated in Table 3-5 into the D/A register and adjust the indicated potentiometer to the desired voltage.

Table 3-5 Offset and Gain Adjustment

In	Load		Adjust				For		
	Straight Binary	2's Complement	D/A 0	D/A 1	D/A 2	D/A 3	±5 V Range	±10 V Range	±0.5 V Range
Offset Adjust	0000	4000	R 38	R 40	R 42	R 44	-5 V	-10 V	-0.5 V
Gain Adjust	7777	3777	R 37	R 39	R 41	R 43	+4.9976 V	+9.9951 V	+.49976 V

NOTE

In the ±0.5 range, the Offset and Gain potentiometer might have insufficient range for accurate adjustment, and typically the DAC will be within ±5% of desired Offset and Gain setting.

The Gain and Offset adjustments in the oscilloscope can compensate for these errors.

Reader's Comments

AA11-K 4-CHANNEL D/A AND DISPLAY CONTROL
USER'S MANUAL
EK-AA11K-TM-001

Your comments and suggestions will help us in our continuous effort to improve the quality and usefulness of our publications.

What is your general reaction to this manual? In your judgment is it complete, accurate, well organized, well written, etc.? Is it easy to use? _____

_____

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What features are most useful? _____

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_____

Does this manual satisfy the need you think it was intended to satisfy? _____

Does it satisfy *your* needs? _____ Why? _____

_____

_____

_____

Would you please indicate any factual errors you have found. _____

_____

_____

_____

Please describe your position. _____

Name _____ Organization _____

Street _____ Department _____

City _____ State _____ Zip or Country _____

CUT OUT ON DOTTED LINE

— — — — — — — — — — — — Fold Here — — — — — — — — — — — —

— — — — — — — — — — Do Not Tear - Fold Here and Staple — — — — — — — — —

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