DTR01/DR01
Channel Interface Subsystem
Technical Manual

digital equipment corporation • marlboro, massachusetts

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CHAPTER 1
INTRODUCTION

1.1 PURPOSE AND USE

The DTR01 is a channel port system which provides a general-purpose access to the KL10-B, C, D or E main memory unit via a user high-speed port interface.

The DTR01 subsystem enables a user interface/device to perform high-speed block transfers to or from the system's main memory unit via the mass storage bus and appropriate RH20 controller. Although the maximum subsystem rate within a block is one megabyte, the transfer rate is primarily determined by the user interface. Therefore, an adjustment for limiting the maximum transfer rate of the DR01 has been provided so that it will not exceed the bandwidth of the system.

The DR01-C and DTR01 subsystems can also be used to establish a high-speed interprocessor link between a KL10-B, C, D or E and another KL10-B, C, D or E, a PDP-11, or a PDP-11/70. (See Figure 1-1.)

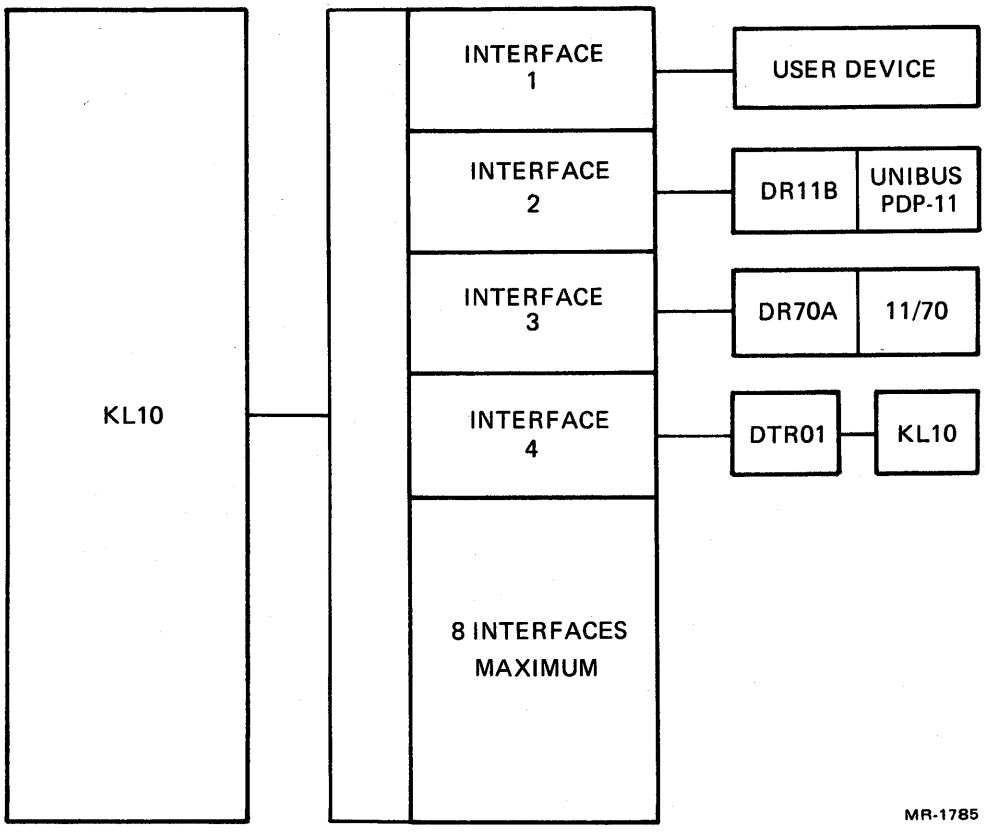


Figure 1-1 Possible DTR01 Subsystem Configurations

1.2 GENERAL DESCRIPTION

Communication and control between the DTR01 subsystem and the host processor is implemented with seven programmable registers located in each DR01-CL. Communication and control of the user interface/device is implemented via 8 status bits, 8 user function bits, 4 attention bits, and 1 user error bit along with 18 separate data in and out lines plus optional parity.

1.3 FEATURES AND CAPABILITIES

The DTR01 provides the following features.

- Performs high-speed block transfers (block can be any size to the maximum amount of core in the system) between main memory and user devices.
- Provides a high-speed channel interface with access to KL10-B, C, D or E main memory unit.
- Establishes high-speed interprocessor links between separate computer systems as follows.

  KL10-B, C, D or E to KL10-B, C, D or E

  KL10-B, C, D or E to Unibus PDP-11 system

  KL10-B, C, D or E to PDP-11/70 system
- Currently provides an interface from any user device interfaced through a direct memory access device interface (DR11-B) to a PDP-11 Unibus.
- Provides an interface expanded beyond a PDP-11 Unibus direct memory access interface (DR11-B) with the following additional features.

  Enables data input and output as either word or byte (switch selectable). Byte data is in the low order bits on 8 lines.

  Provides optional parity checking for data transferred with the user device.

  Provides for additional user-defined status and function bits.
- A maximum of 8 channel interfaces are available to user devices or computers.*

The user interface connects to dedicated slots in the DR01-CL interface unit. The user device currently interfaced through the DR11-B to the Unibus can be connected to the DTR01 subsystem with a minimum of changes, since the physical signal pins out of these connector slots are almost identical.

In addition to the standard interface connector, a second expanded interface connector slot is provided in the DR01-CL unit to increase the flexibility of the user interface.

*For link configurations, DR11-Bs or DR70As are not supplied. They are mounted externally in a PDP-11 cabinet or mounting box, not a part of the DTR01 system.

1.4 SPECIFICATIONS

1.4.1 Mechanical Specifications

There are three configurations of DTR01 Channel Interface Subsystems and two configurations of DR01 Channel Interfaces available. They are as follows.

DTR01-AA/AB

Description	H9502 cabinet containing power control, DR01 mounting box and DR01-CL logic plus RH20 option set. Contains space for two additional DR01-CL options and cabinet space for two additional DR01 mounting boxes (either DTR01-CC/CD or DR01-CA/CB).*
Prerequisite†	KL10-B, C, D or E
Dimensions	152 cm × 76 cm × 66 cm (60 in × 30 in × 26 in)
Weight	204 kg (450 lb)

DTR01-CA/CB

Description	H950 cabinet containing power control, DR01 mounting box, and DR01-CL logic plus RH20 option set. Contains space for two additional DR01-CL options and cabinet space for two additional mounting boxes (either DTR01-CC/CD or DR01-CA/CB).*
Prerequisite†	KL10-B, C, D or E
Dimensions	175 cm × 48 cm × 68 cm (69 in × 19 in × 27 in)
Weight	159 kg (350 lb)

DTR01-CC/CD (Second System Box)

Description	Mounting box containing DR01-CL logic plus RH20 option set. Only one DTR01-CC/CD may be added to a DTR01 CA/CB, AA/AB. Contains space for two additional DR01 CL options.
Prerequisites†	KL10-B, C, D or E and DTR01-CA/CB or AA/AB (space permitting)
Dimensions	27 cm × 48 cm × 69 cm (11 in × 19 in × 27 in)
Weight	50 kg (110 lb)

*Only one DTR01-CC/CD mounting box may be added to a DTR01-CA/CB, AA/AB cabinet.
†System prerequisite requires the KL10-B, C, D or E CPU to be at revision level 10 or greater.

DR01-CA/CB

Description	DR01 mounting box containing DR01-CL logic with space for two additional DR01-CL options.
Prerequisite	DTR01-CA/CB or AA/AB
Dimensions	27 cm × 48 cm × 69 cm (11 in × 19 in × 27 in)
Weight	50 kg (110 lb)

DR01-CL

Description	Channel interface logic unit
Prerequisites	DR01-CA/CB, or DTR01-CC/CD, or DTR01-CA/CB or DTR01-AA/AB (space permitting)
Dimensions	42 cm × 22 cm × 6 cm (17 in × 9 in × 3 in)
Weight	8 kg (18 lb)

1.4.2 Electrical Specifications

Electrical characteristics are provided in Table 1-1.

1.4.3 Operational Specifications

The following are the operational characteristics of the DTR01.

Transfer Rate	1 megabyte/second (max.) word mode 500 kilobytes/second (max.) byte mode (mode is switch-selectable)
Output Levels	TTL, 30 unit loads max., high = logic 1
Input Levels	TTL, 8 unit loads max., high = logic 1
User Cable or Link Cable*	9 m (30 ft) max. from user device to DTR01 channel interface
Host Cable*	BC06S, 30 m (100 ft) max. from RH controller to DTR subsystem
Commands	Read, Write, and Interface Clear (octal codes 71, 61, and 11 respectively only); all other codes are not valid.

*Only standard host 12 m (40 ft) and link 8 m (25 ft) cables will be supplied with the system. If special length cables are required, they must be specified at the time the system is ordered.

Table 1-1 Electrical Specifications

Configuration	Voltage	Current*	Frequency	Power	BTU
DTR01-AA	115 Vac ±10%	5 A	50/60 ±3 Hz	400 W	1320
DTR01-AB	240 Vac ±10%	2.5 A	50/60 ±3 Hz	400 W	1320
DTR01-CA	115 Vac ±10%	5 A	50/60 ±3 Hz	400 W	1320
DTR01-CB	240 Vac ±10%	2.5 A	50/60 ±3 Hz	400 W	1320
DTR01-CC	115 Vac ±10%	4 A	50/60 ±3 Hz	300 W	990
DTR01-CD	230 Vac ±10%	2 A	50/60 ±3 Hz	300 W	990
DR01-CA	115 Vac ±10%	4 A	50/60 ±3 Hz	300 W	990
DR01-CB	230 Vac ±10%	2 A	50/60 ±3 Hz	300 W	990
DR01-CL	+5 Vdc -15 Vdc	10 A 1 A		65 W	215

Power Connector: DTR01-CA uses NEMA L5-30P
DTR01-CB uses NEMA L6-20P
DTR01-AA uses NEMA L5-30P
DTR01-AB uses NEMA L6-20P

*These current values are estimated for the basic option configurations.

1.4.4 Environmental Operating Specifications

The following are the environmental operating specifications of the DTR01.

Temperature	10 - 40° C (50 - 104° F) max. Temperature change rate is 10° C (18° F) max. per hour.
Humidity	10% to 90% (no condensation)
Altitude	2 km (8000 ft)
Atmosphere	Noncorrosive
Shock	10 G for 10 ms

CHAPTER 2
SITE PREPARATION AND PLANNING

2.1 SITE CONSIDERATIONS

The basic system entry level unit is the DTR01, consisting of a DTR01 cabinet, DR01-CL interface and mounting box and RH20 controller. The DTR01 cabinet can be located within 30 m (100 ft) of the RH20 connected via BC06S cables. If space permits placing a second system box (DTR01-CC/CD) in the DTR01 cabinet, the DTR01 cabinet must be located within 30 m (100 ft) of each RH20 it is connected to via BC06S cables.

The DR01-CA/CB expander interface box is provided for additional system expansion and is mounted in the DTR01 cabinet.

The DR01-CL is the basic channel interface composed of a logic system unit. It provides a user interface access into the system. The DR01-CL can be mounted in either the DTR01 or DR01-CA/CB boxes. (See Paragraph 2.3 for further guidelines.) The DR01-CL is normally located as close as possible to the user interface (9 m or 30 ft maximum cable separation).

2.2 USER INTERFACE CABLING

The user interface is generally located external to the DTR01 cabinet and is cabled to the DR01 with two M9760-YA modules or other suitable terminators. A cable from the user interface is normally attached to the two M9760-YA modules which mount in the two double-height connector slots. As an alternative, if the user interface is small enough, it can be located in the same cabinet with the DR01 and the two units may be connected directly with two BC11A cables. However, this configuration is not generally recommended and the user interface must be powered separately. Figure 2-1 shows the location of the two user interface connector slots in the DR01 system unit.

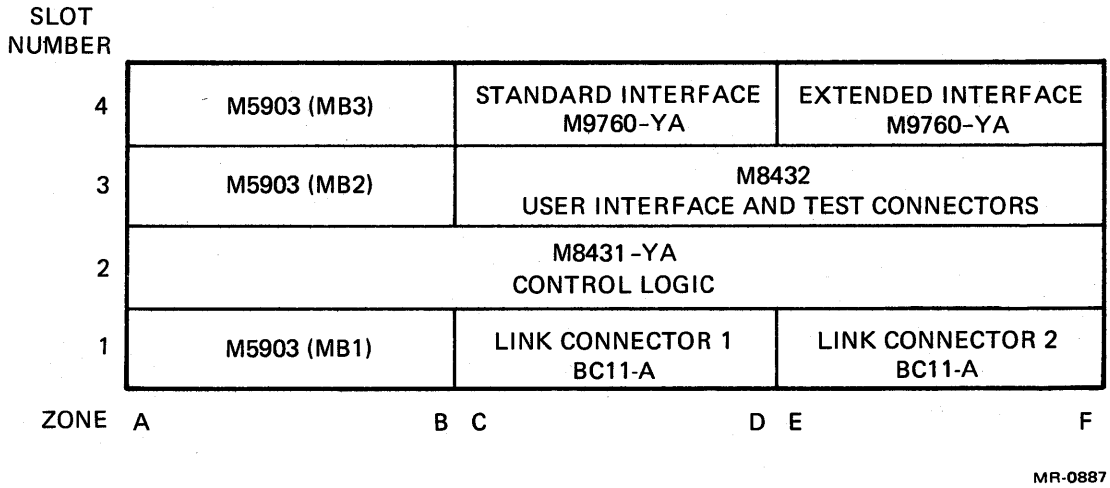


Figure 2-1 DR01 User Interface Connector Slot
View Shown From Backplane

Table 2-1 is a list of user interface signal pin assignments for each of the DR01 connector slots.

Table 2-1 Interface Signal Pin Assignments

Signal Source (See Note)	Signal	Slot	Pin	Zone	Lug Pin
TCC	DATA 00 OUT H	D04	S1	B	S1
TCC	DATA 01 OUT H	D04	R1	B	R1
TCC	DATA 02 OUT H	D04	U2	B	U2
TCC	DATA 03 OUT H	D04	P1	B	P1
TCC	DATA 04 OUT H	D04	T2	B	T2
TCC	DATA 05 OUT H	D04	N1	B	N1
TCC	DATA 06 OUT H	D04	S2	B	S2
TCC	DATA 07 OUT H	D04	M1	B	M1
TCC	DATA 08 OUT H	D04	R2	B	R2
TCC	DATA 09 OUT H	D04	L1	B	L1
TCC	DATA 10 OUT H	D04	P2	B	P2
TCC	DATA 11 OUT H	D04	K1	B	K1
TCC	DATA 12 OUT H	D04	N2	B	N2
TCC	DATA 13 OUT H	D04	M2	B	M2
TCC	DATA 14 OUT H	D04	L2	B	L2
TCC	DATA 15 OUT H	D04	K2	B	K2
USA	DATA 00 IN H	C04	C1	A	C1
USA	DATA 01 IN H	C04	D1	A	D1
USA	DATA 02 IN H	C04	D2	A	D2
USA	DATA 03 IN H	C04	E1	A	E1
USA	DATA 04 IN H	C04	E2	A	E2
USA	DATA 05 IN H	C04	F1	A	F1
USA	DATA 06 IN H	C04	F2	A	F2
USA	DATA 07 IN H	C04	H1	A	H1
USA	DATA 08 IN H	C04	H2	A	H2
USA	DATA 09 IN H	C04	J1	A	J1
USA	DATA 10 IN H	C04	J2	A	J2
USA	DATA 11 IN H	C04	K1	A	K1
USA	DATA 12 IN H	C04	K2	A	K2
USA	DATA 13 IN H	C04	L2	A	L2
USA	DATA 14 IN H	C04	M2	A	M2
USA	DATA 15 IN H	C04	N2	A	N2
USA	CYCLE REQUEST A	C04	A1	A	A1
USA	CYCLE REQUEST B	D04	U1	B	U1
USA	DEVICE STATUS 00	C04	P2	A	P2
USA	DEVICE STATUS 01	C04	L1	A	L1
USA	DEVICE STATUS 02	C04	R2	A	R2
USB	DEVICE STATUS 03	E04	N2	A	N2
USB	DEVICE STATUS 04	E04	P2	A	P2
USB	DEVICE STATUS 05	E04	R2	A	R2
USB	DEVICE STATUS 06	E04	D2	A	D2
USB	DEVICE STATUS 07	E04	T2	A	T2
TCB	FUNCTION BIT 00	D04	E2	B	E2
TCB	FUNCTION BIT 01	D04	J2	B	J2
TCB	FUNCTION BIT 02	D04	H1	B	H1
TCB	FUNCTION BIT 03	F04	H2	B	H2
TCB	FUNCTION BIT 04	F04	N2	B	N2
TCB	FUNCTION BIT 05	F04	K2	B	K2
TCB	FUNCTION BIT 06	F04	L2	B	L2
TCB	FUNCTION BIT 07	F04	P2	B	P2
DTC	READY H	D04	J1	B	J1

Table 2-1 Interface Signal Pin Assignments (Cont)

Signal Source	Signal	Slot	Pin	Zone	Lug Pin
FDC	GO H	D04	V1	B	V1
TCC	READ H	D04	D2	B	D2
TCC	END CYCLE H	C04	B1	A	B1
USA	ERROR H	C04	M1	A	M1
DTC	BUSY H	C04	S2	A	S2
TCC	INIT H	C04	U2	A	U2
USB	ATTN BIT 00 H	E04	E2	A	E2
USB	ATTN BIT 01 H	E04	H1	A	H1
USB	ATTN BIT 02 H	E04	J1	A	J1
USB	ATTN BIT 03 H	E04	K1	A	K1
USB	DATA 16 IN H	E04	A1	A	A1
USB	DATA 17 IN H	E04	F1	A	F1
USB	DPA LO IN H	E04	C1	A	C1
USB	DPA HI IN H	E04	D1	A	D1
TCB	DATA 16 OUT H	E04	B1	A	B1
TCB	DATA 17 OUT H	F04	H1	B	H1
TCB	OUT PARITY HI	F04	J1	B	J1
TCB	OUT PARITY LO	F04	K1	B	K1
USB	WORD MODE H	E04	L1	A	L1
USB	INHIBIT INPUT PARITY H	E04	E1	A	E1
ISR	AC LO H	F04	S2	B	S2
CPF	+3 volts	E04	U1	A	U1
Reserved for Link					
Do not use:					
C04R1					
C04V1					
C04T2					
D04F1					
D04F2					
D04H2					
E04F2					
E04L2					
E04L2					
E04S2					
E04U2					

NOTE

Since the DR01 interface does not contain any type of word counter, it must rely on the internal channel word count of the KL10-B, C, D or E to indicate transfer end. This causes some delay to exist between the last word transferred and the WCOV in the internal channel signalling transfer end and results in one or more additional END CYCLE pulses to the user's interface.

The user's interface should be designed to prevent a malfunction from occurring due to these additional pulses.

Note:

Signal Source	Drawing Referenced
TCC	M8432-0-1 sheet 5 of 5
USA	DR01-0-03 sheet 1 of 2
USB	DR01-0-04 sheet 1 of 1
TCB	M8432-0-1 sheet 4 of 5
DTC	DR01-0-03 sheet 1 of 2 and DTR01-0-2
FDC	DR01-0-03 sheet 1 of 2 and DTR01-0-2
ISR	M8431-YA-1 sheet 8 of 11
CPF	M8431-YA-1 sheet 4 of 11

All output signals are driven with 7437 drivers. These drivers can sink 60 mA in the output low state and can source 1.5 mA in the output high state. This is equivalent to a fan-out of approximately 30 unit loads.

All input signals are received by 7414 Schmitt trigger receivers for noise immunity. The signal inputs are terminated at the receiver input with a 180 ohm resistor to +5 V and a 390 ohm resistor to ground on the M9760-YA module. (See Figure 2-2.) This termination requires a driver in the user interface capable of sinking at least 25 mA. A driver such as the 7437 or 74H40 will satisfy this requirement. If the use of lower powered drivers is desired, the terminators may be removed from the M9760-YA module. However, it is not recommended to use lower power drivers for cable lengths greater than 1.5 m (5 ft).

2.3 SYSTEM CONFIGURATION GUIDELINES

Figure 2-3 provides a graphic description of the system's expansion capability by providing the system minimum and maximum configurations. The maximum configuration rules are listed below.

1. Eight DR01-CLs per Massbus (RH20)
2. Any RH20 option set used by DR01-CLs cannot be shared with other devices.
3. One Massbus per DR01 mounting box
4. Two Massbuses per DTR01 cabinet
5. Three DR01-CLs per DR01 mounting box
6. Three DR01 mounting boxes per cabinet
7. One additional (second) DR01 system box per DTR01 cabinet (DTR01-CC/CD). If a second DR01 system box is placed in the DTR01 cabinet, the maximum configuration per cabinet is:

   Massbus no. 1 = 3 DR01-CLs
   Massbus no. 2 = 6 DR01-CLs.

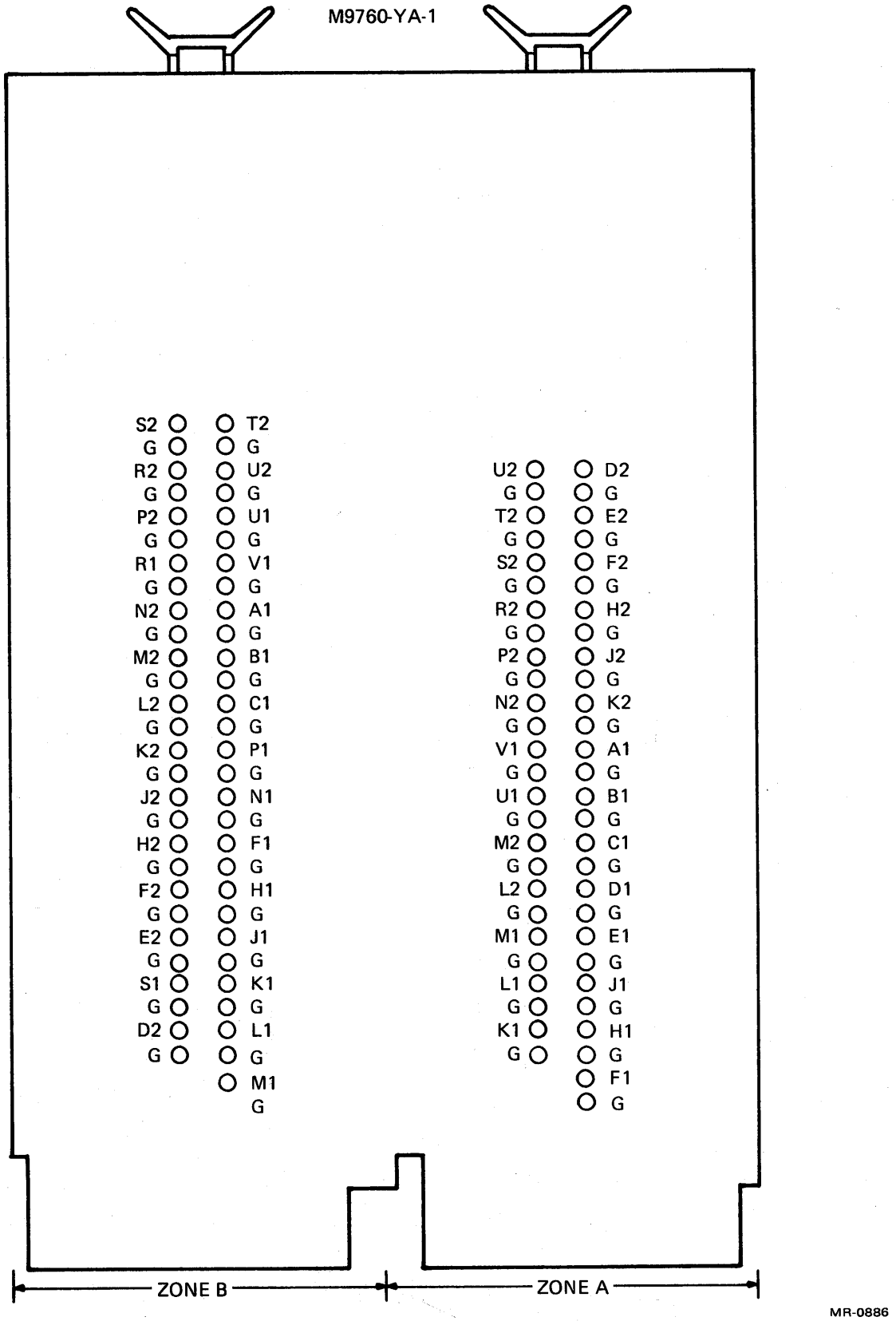


Figure 2-2 Module M9760-YA

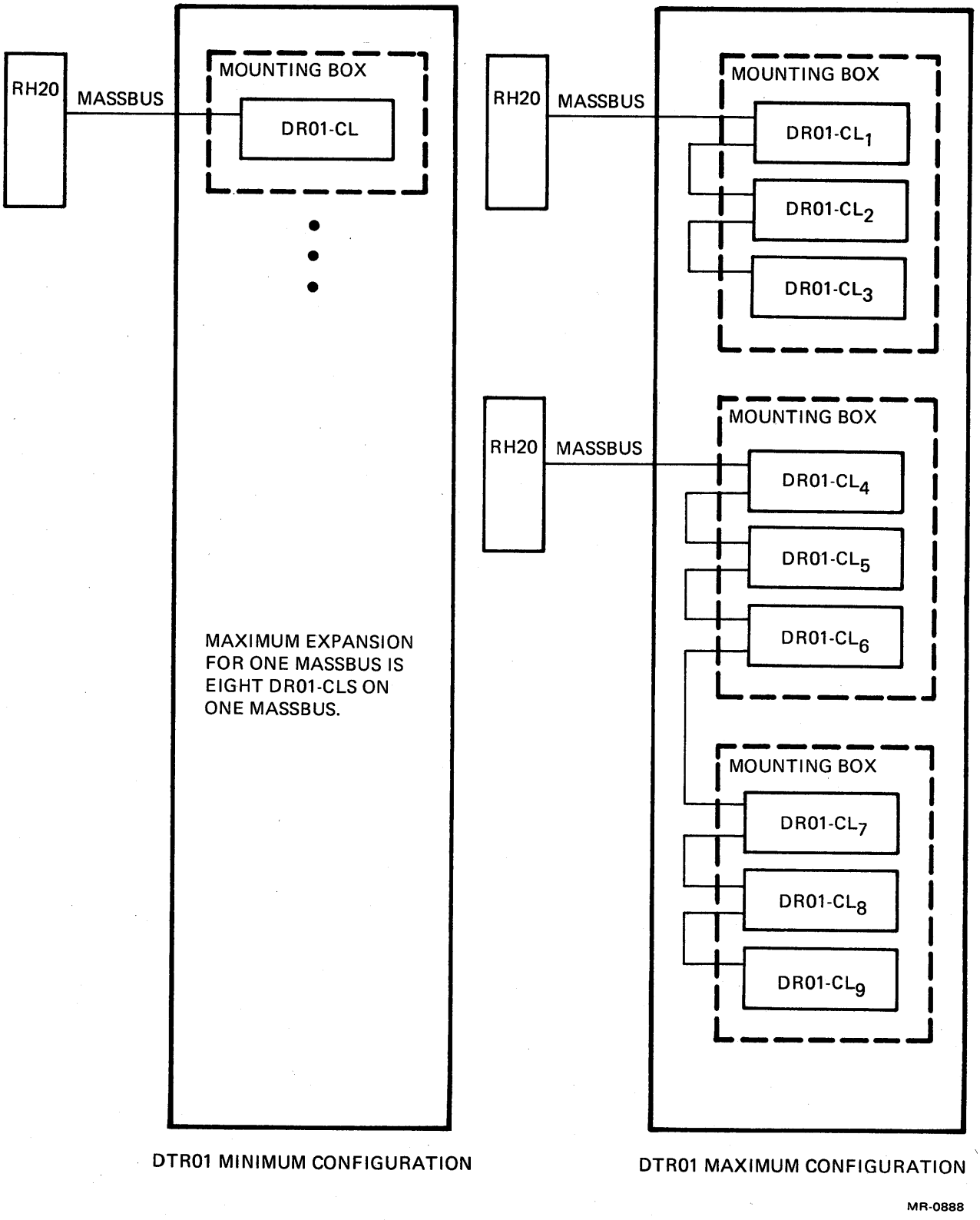


Figure 2-3 DTR01 Maximum and Minimum Configuration

CHAPTER 3
INSTALLATION

3.1 DTR01 INSTALLATION PROCEDURES

Verify that the KL10-B, C, D or E CPU in the system is at revision level 10 before proceeding with the installation. Observe the CPU revision sticker on the module enclosure door on the CPU logic.

NOTE
DO NOT proceed with the DTR01 installation if the KL10-B, C, D or E CPU is not at machine level 10.

Install the RH20 option module set into the next available channel backplane slot or another slot if preferred. Refer to the *RH20 Massbus Controller Unit Description* (EK-RH20-UD) and/or *KL10 System Installation Manual.*

3.2 RH20 CLOCK DESKEW PROCEDURE

Perform the RH20 clock deskew procedure for the RH20 being installed. (Refer to the *KL10 Maintenance Handbook* EK-KL10-HB.)

3.3 RH20/CHANNEL CONTROL LOGIC DIAGNOSTICS

Run the following RH20/Channel Control Logic Diagnostics. Refer to diagnostic listing fiche for program and error information.

DGKBD.A11	Version 0.10 (or later)
DGKBE.A11	Version 0.10 (or later)
DGRHB.A10	Version 0.11 (or later)

Upon successfully running the diagnostics above, connect the DTR01 cabinet/DR01-C logic to the RH20 with the supplied BC06S-XX cable. (See Figure 3-1.) Jumper W1 on each H870 (Massbus terminal pack) must be cut for the proper operation of the DR01. The total length of the Massbus cable should not exceed 30 m (100 ft) with BC06S round cable from the CPU.

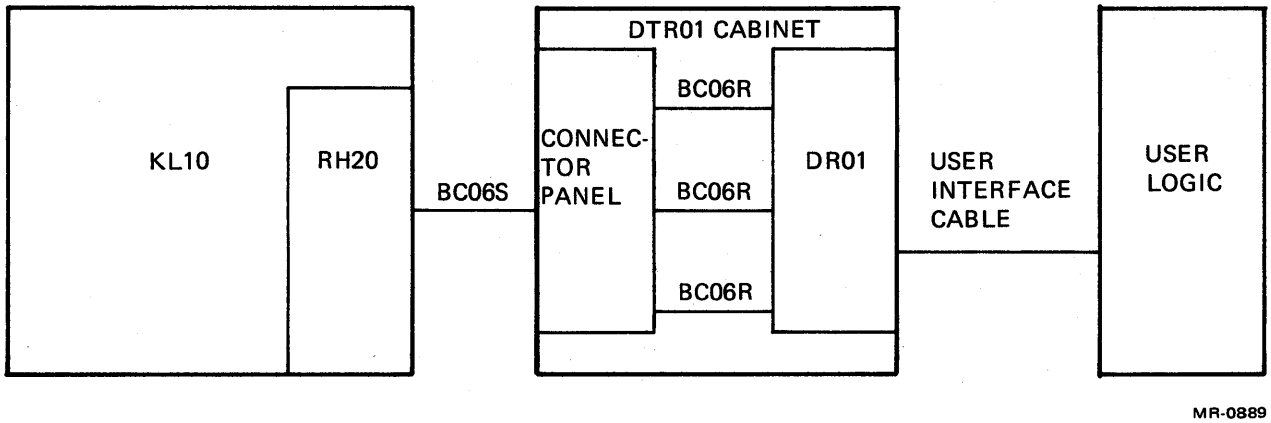


Figure 3-1 Massbus Cabling

3.4 USER INTERFACE CABLING

The user interface is cabled to the DR01 with the two M9760-YA modules. A cable from the user interface is normally attached to the two M9760-YA modules which mount in the two double-height connector slots.

3.5 GROUNDING

In addition to the ground wires in the user interface cable, the DR01 should be grounded to the user interface through a separate cable. This ground strap provides a low resistance path to ground. Also, the DR01 and the Massbus controller should share a common ground. Using the supplied ground cable, connect the DTR01 cabinet to the host system ground.

3.6 POWER UP UNIT

Plug the unit into the appropriate ac outlet and power up the DTR01 cabinet. Check all logic voltages.

+5 V ± 0.25 V
−15 V ± 0.5 V

3.7 DEVICE NUMBER SELECTION

Dual in-line package (DIP) switches, SW1-1, SW1-2, SW1-3 on the DR01 control board (M8431-YA) select the device number of the DR01 on the Massbus. (See Table 2-1.) (Switch in the ON position = 0; SW1-1 is LSB; SW1-3 is MSB.) The rocker switches represent an octal number from 0 to 7. The DR01 is shipped with the switches set for unit 7. Switch SW1-7 indicates byte mode when ON and word mode when OFF. Switch SW1-8 indicates inhibit input parity when ON and enable input parity when OFF.

3.8 MAXIMUM TRANSFER RATE ADJUSTMENT

The DR01 is shipped from the factory with its maximum rate set to 3.4 μs per 36-bit word. This is equivalent to a high-speed disk such as the RS04. The maximum transfer rate may be increased or decreased as required.

Verify that the sync clock (SCLK) timing is set up properly for the KL10-B, C, D or E version to which it is connected. Using Test 6 of the DFDRA diagnostic and a 1-word transfer, monitor pin D02M2 with an oscilloscope on the DR01-CL backplane. For a 25 MHz* KL10-B, C, D or E CPU the maximum settings are as follows.

SCLK width = 800 ns
SCLK period = 1.7 μs

The SCLK width adjustment potentiometer on the M8431-YA module is R3 located front/bottom. The SCLK period potentiometer is R6 located rear/top. Slot A of the module is at the top; Slot F is at the bottom. It may be necessary to limit the maximum transfer rate of the DR01 so that it does not exceed the bandwidth of the system. On heavily loaded systems, problems such as data late errors on other system devices or in the DR01 may occur during peak periods of system operation if the speed is not limited.

If the speed must be limited, first determine the maximum transfer rate allowable.

NOTE

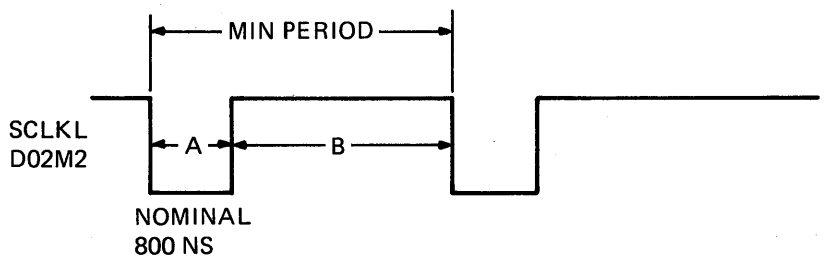
Determining the available bandwidth to the DR01 can be a very complex system problem requiring a comprehensive knowledge of the system architecture. If the system bandwidth is not extremely critical, an estimate of the available bandwidth may suffice; however, in critically loaded systems, customers should have the system bandwidth analyzed by DIGITAL personnel.

*For a 30 MHz KL10-B, C, D or E system the same settings are used but the period may be shortened with approval of the factory.

When the available bandwidth has been determined, adjust the DR01 as follows.

1. Calculate the reciprocal of the bandwidth to determine the minimum period of the transfer (for example, if the bandwidth is 500 kHz, the minimum period is 2 μs).

2. Monitor the SCLK L signal located on the DR01 backplane D02M2. Run the bandwidth portion of the DR01 diagnostic DFDRA using Test 6 and a 1-word transfer. The signal in Figure 3-2 should be observed at D02M2.



FOR 25 MHZ KL10 SYSTEM, THE MAXIMUM SETTING IS AS FOLLOWS:

A = 800 NS
B = 900 NS
PERIOD = 1.7 μS

MR-0890

Figure 3-2 25 MHz KL10-B, C, D or E System SCLK Setting

3. The low portion (A) of the SCLK L signal is normally set at 800 ns. This corresponds to the minimum setting of potentiometer R3 which is located at the bottom when DR01 is mounted vertically. Do not adjust R3 unless it is necessary to make the DR01 run slower than the adjustment allowed by potentiometer R6 described in the next step.

4. Potentiometer R6 controls the width of the high portion (B) of the SCLK L signal. Potentiometer R6 is at the top when DR01 is mounted vertically. Adjust R6 so that the total width of the low and high portions equals the desired minimum period calculated in step 1. If the range of the R6 adjustment does not allow slowing the DR01 enough, leave R6 at its maximum setting and increase R3 until the desired value is obtained.

3.9 M5903 ENABLE SWITCHES

Each M5903 Massbus transceiver has an enable switch that enables the receivers. The function of these switches is not implemented on the DR01 and the switches should always be set to the ON (up) position.

3.10 CHECKOUT AND ACCEPTANCE

Make sure the BC08R loopback cable is installed between J1 and J2 on the M8432 board and that the user connector modules (M9760-YA boards) have been removed from the DR01-CL logic. Also remove any link cables (i.e., nothing in CDEF01, CDEF04). Load the DTR01 diagnostic, DFDRA.A10 and continue with the DTR01 subsystem checkout. Refer to the DTR01 Checkout/Acceptance Procedure.

CHAPTER 4
OPERATION/PROGRAMMING

4.1 DTR01 OPERATION

The user must define an operation protocol to be used in communications between the host system and the user's device. The user function, status, and attention bits and also possibly a fixed message size and/or data block size to be transferred should be considered. Once a protocol is defined, the programming of the DTR01 subsystem can be accomplished.

A data transfer can be functionally performed as follows.

1. Determine if the DR01 interface is ready.
2. Load the user function/status as defined in the protocol.
3. Initialize and generate the desired channel transfer command list.
4. Initialize and generate the desired data buffer area.
5. With the user's program, load the read or write command indirectly via RH20 STCR, REG 40 into the RH20 secondary transfer command register (RHCS1, REG0 bits 00–05).
6. Wait for DONE (indicates transfer completed).
7. Check status and proceed.

4.1.1 Single-Word Transfer – Write

To transfer a single word of data from the host to the user interface device under program control, load the output buffer, RHOB (REG 7) with the desired data.

NOTE

This procedure assumes a single-word transfer protocol is defined so that the user interface is assured of taking stable data (i.e., some strobe signal may be provided via a dedicated user function bit).

4.1.2 Single-Word Transfer – Read

To transfer a single word from the user device interface to the host under program control, read the input buffer register, RHIB (REG 2).

NOTE

This procedure assumes that the user device will supply the data word stable for the interface to read. Caution must be taken to ensure stable data that is not changing when the program reads it by implementing a handshake protocol possibly with dedicated user function/status bits.

4.2 PROGRAMMING

4.2.1 Communication Between the DTR01 and the KL10-B, C, D or E Processor (See Figure 4-1)

Communication and control between the DTR01 subsystem (RH20 and DTR01) and the KL10-B, C, D or E processor is implemented with DATAO and DATAI instructions from the CPU. These instructions cause bits within the DR01 external registers to be loaded or cleared. The KL10-B, C, D or E CPU communicates with the RH20 Massbus controller via the EBus and the RH20 Massbus controller communicates with the DR01 via the Massbus.

Data is transferred through the DR01 registers to or from the RH20 Massbus controller via the MBus data lines. Data is transferred between the RH20 and the CPU via the CBus and between the CPU and main memory via the SBus.

A secondary method available to transfer data to and from the RH20 Massbus controller is via DR01 external registers 2_8 and 7_8, respectively, using DATAI and DATAO instructions. (See Paragraphs 4.1.1 and 4.1.2.)

4.2.1.1 Loading DR01/DTR01 External Registers – The CPU issues a DATAO or DATAI instruction to read or write the designated DR01/DTR01 registers. When using DATAO, setting bit 06, LR = 1 writes into the DR01 register (RS00-37_8) and setting bit 06, LR = 0 loads a register address (plus control data and a drive address if RS = 00–37_8) so that a register may be read by a subsequent DATAI. Repeated DATAI commands will read the same register; that is, DATAI will always read the register specified by the last DATAO (LR = 0 or 1).

When the RH20 detects an error caused by a nonexistent drive or control bus parity during the writing or reading of an external register, an interrupt occurs and the program is inhibited from writing any more registers with a DATAO unless DRAES, DATAI bit 09, was set by the DATAO that preceded or caused the error. (A DATAI is not inhibited and it can be used to read back the failing register and drive address.)

For a more detailed description of DATAO/DATAI instructions, refer to the *RH20 Massbus Controller Unit Description,* EK-RH20-UD.

4.2.1.2 DATAO – The DATAO command is used to write both internal and external registers. The bit format for the DTR01 DATAO (external registers) is shown in Figure 4-2.

The preparation register is not addressed directly. It is loaded with address and control information (bits 00–06, 09 and 14–18) by all DATAO commands, provided there has been no previous register access error detected (RAE, CONI bit 24 = 0) or there has been an error and it has been disabled (DRAES, DATAI bit 09 = 1). When RAE = 1 and DRAES = 0, the preparation register is not loaded and the DATAO command is not executed by the RH20. The following list explains the functions of the bits in the DATAO external register.

Bits	Description
00–05	REGISTER SELECT (RS) – Six-bit register select code. RS = 40–77$_8$ when addressing an internal register of RH20. RS = 00–37$_8$ when addressing an external register of DR01.
06	LOAD REGISTER (LR) – When equal to 1, causes the addressed register to be written. When equal to 0, only the preparation is loaded, thus providing a means to store address and control information for a subsequent register read operation (DATAI).
09	DRAES – Prevents RAE (CONI bit 24) from generating an RH20 interrupt request and from inhibiting subsequent register write operations.
15–17	DRIVE SELECT (DS) – Specifies the drive number (0–7$_8$) when addressing an external register (RS = 00–37$_8$).
18	CBEP – When writing an external register (RS = 00–37$_8$, LR = 1) causes even parity to be transmitted on the Massbus (control bus) data lines. Used by the diagnostics to cause parity errors in a drive.
20–35	EXTERNAL REGISTER DATA – Specifies the register contents when an external register is written.

4.2.1.3 DATAI – The DATAI command is used to read both internal and external registers. The register that is read is determined by the address and control data stored in the preparation register by a previous DATAO. Bit format for the DATAI command is shown in Figure 4-3. The following list explains the functions of the bits in the DATAI external register.

Bits	Description
00–05	REGISTER SELECT (RS) – The register select code which is stored in the preparation register.
06	LOAD REGISTER (LR) – Indicates the state of the LR bit stored in the preparation register. Equals 0 when the previous DATAO loaded only the preparation register. Equals 1 when the DATAO wrote the specified register.
08	CONTROL BUS PAR ERR (CBPE) – Indicates that bad parity was detected on the Massbus (control bus) data lines during the DATAI. Sets RAE (CONI bit 24).
09	DRAES – Indicates that register access errors have been disabled. Set by DATAO bit 09 = 1.
10	TRANSFER RECEIVED (TRA) – Indicates that a drive responded (asserted transfer on the Massbus) during the DATAI.
15–17	DRIVE SELECT (DS) – The drive select code stored in the preparation register by a DATAO.
19	CONTROL BUS PARITY BIT (CPA) – Indicates the state of the parity bit received on the Massbus (control bus).
20–35	EXTERNAL REGISTER DATA (ERD) – The contents of the register addressed by the DATAI.

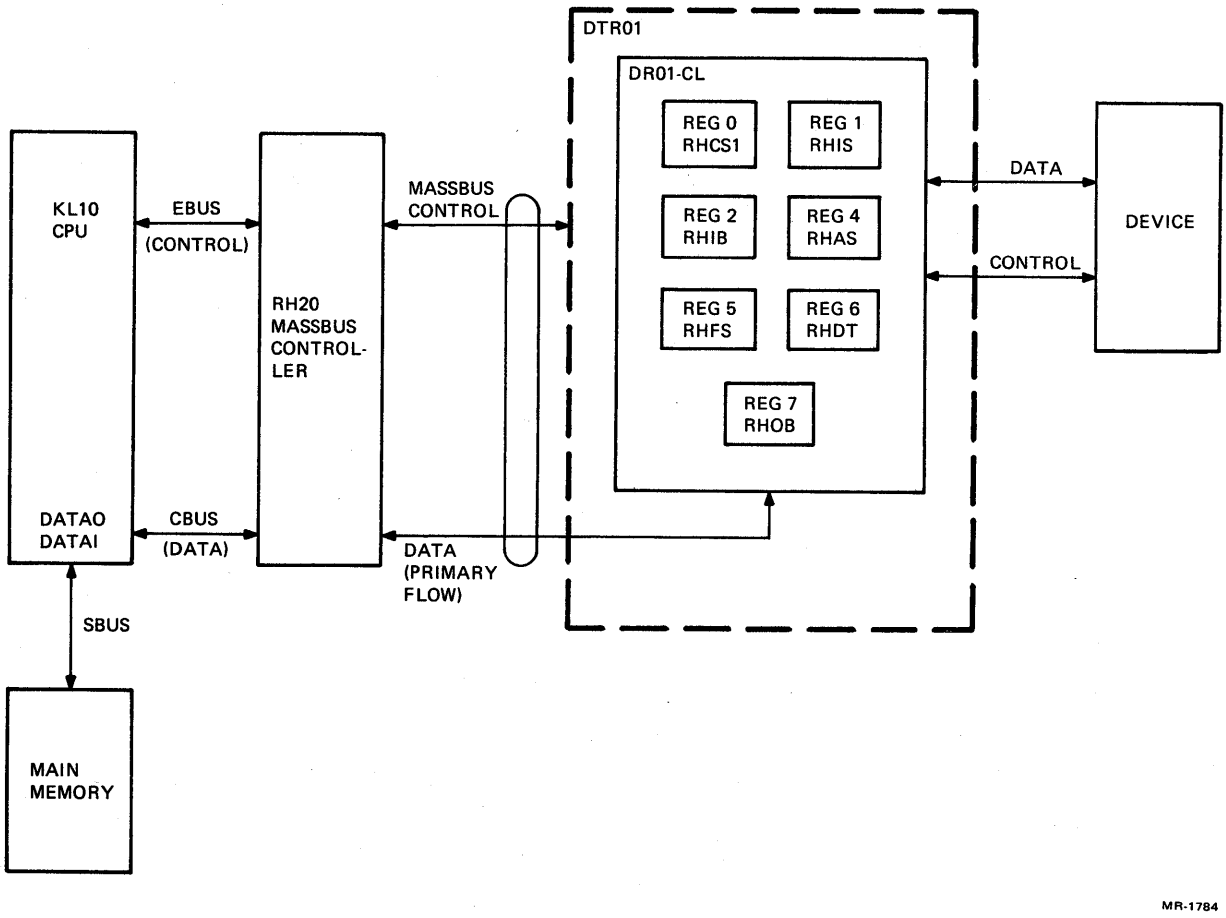


Figure 4-1 Communications Between DTR01 and KL10-B, C, D or E Processor

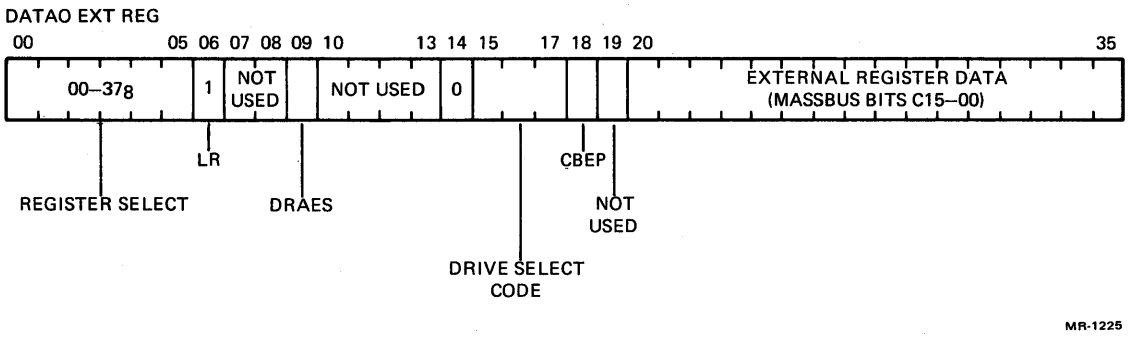


Figure 4-2 DATAO External Register

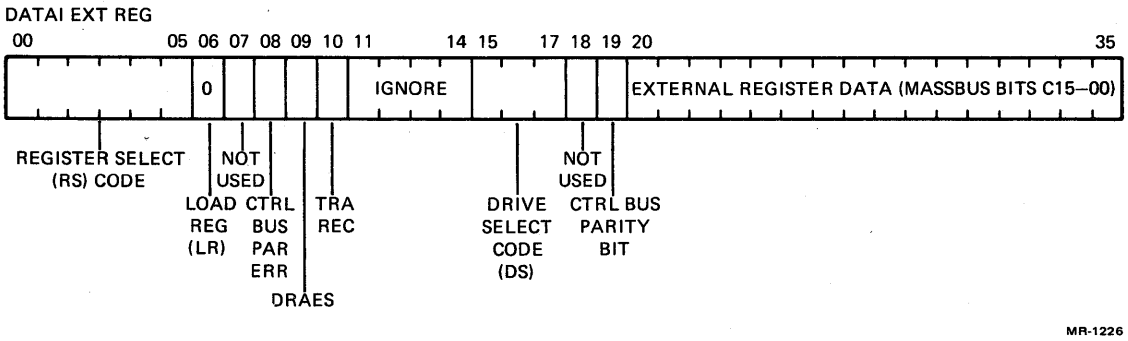


Figure 4-3 DATAI Bit Format

4.2.2 Programmable Registers in DR01-CL Channel Interface Unit

Communication and control between the DTR01 subsystem and the host processor is implemented with seven programmable registers located in each DR01-CL channel interface unit. Paragraphs 4.2.2.1 through 4.2.2.7 describe the seven programmable registers and formats.

4.2.2.1 Control and Status 1 Register (RHCS1) - REG 0 - Register 0 is the control status 1 (RHCS1) register. It is used by both the controller and the DR01 to store the device commands and hold operational status. Register bits 00 through 05 and bit 11 are dedicated for use by the interface as shown in Figure 4-4.

Register bits 00–05 indicate the command to be performed and are stored in the selected device (LSB = bit 0).

Bits	Description
15–12	Not used
11	Device Ready - Always read as a 1 (DRY)
10–06	Not used
05–01	F4–F1 - Command function code; can be written at any time

Function	F4–F1 (bits 05–01) Equal
Read	70_8
Write	60_8
Interface Clear	10_8

00 GO - The GO bit is a read/write bit that indicates interface busy. A lockout feature is not provided if the GO bit is set. Therefore, do not write this register during a data transfer.

Function is GO	Bits 05–00 Equal:
Read	71_8
Write	61_8
Interface Clear	11_8

4.2.2.2 Interface Status Register (RHIS) - REG 1 - This register provides general status information for the DR01-CL, the user-defined error bit, and attention signals. The register format is shown in Figure 4-5.

15 ATA - An attention condition sets the ATA bit and the ATA summary line. An ATA condition is caused by the error bit (ERR) setting or the setting of any user-defined attention or error bits. ATA is cleared by INIT, RH CONTROLLER CLEAR, loading a data transfer command with GO set, or writing the appropriate bit in the RHAS register, REG 4. The last two methods do not clear the error condition in the device. This is a read-only bit. ATA is set on power-up.

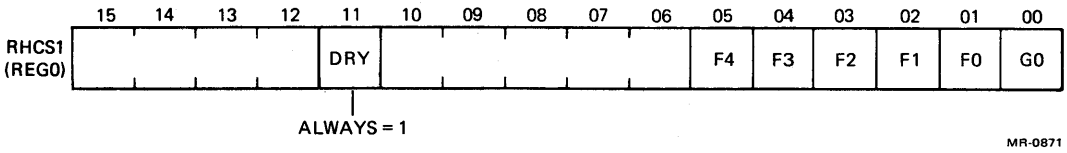


Figure 4-4 RHCS1 (REG 0) Bit Map

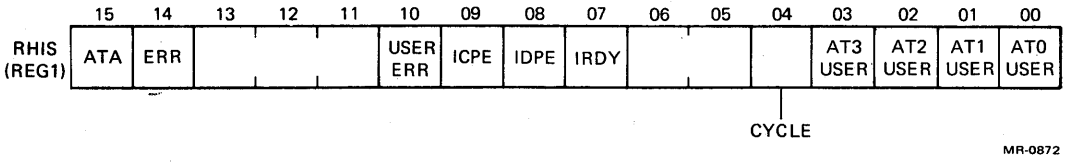


Figure 4-5 RHIS (REG 1) Bit Map

14 ERR – ERR is set when one or more error conditions (USER ERR, ICPE, and IDPE) have been set. ERR is a composite error bit (logical OR) of all error conditions in the RHIS register. The ERR bit is cleared only by INIT, RH CONTROLLER CLEAR or an INTERFACE CLEAR command while ERR is set. On power-up, ERR is set. This is a read-only bit.

13–11 Not used.

10 USER ERR – User-defined error condition from user interface sets USER ERR. USER ERR is cleared by writing an INTERFACE CLEAR command into RHCS1, assuming the interface clears with INIT set. This bit may be used to terminate a data transfer if the word count has not overflowed. Therefore, USER ERR may not indicate an actual error condition. The user status bits may be used to provide more detail concerning why the USER ERR is set. This bit is read-only.

09 ICPE – Sets ERR and indicates a parity error has occurred in transferring control data over the control bus. This bit is read-only.

08 IDPE – Indicates a parity error in transferring data over the data bus during a write device or a data parity error in data received from the user interface during a read device, if enabled. This bit is read-only.

07 IRDY – Indicates that the DR01-CL is ready to accept a new data transfer command. IRDY is set by completion of a block data transfer or an error condition. It is cleared by issuing a Data Transfer command with GO set. This is a read-only bit.

06–05 Not used.

04 CYCLE – This write-only bit is used to prime bus cycles if the user interface is not self-starting. Writing a 1 into this bit causes CYCLE in the interface to set, initiating transfers.

03–00 AT3–AT0 – Read-only, user-defined attention bit. Sets ATA and causes an interrupt if enabled. Cleared by removing the attention condition in the user interface.

4.2.2.3 Input Buffer Register (RHIB) – REG 2 – This register reflects the state of the DATA IN (0:15) lines from the user interface. DATA IN 16 and 17 are not readable via RHIB. This read-only register is shown in Figure 4-6.

15–0 DI15–DI0 – User input data lines

4.2.2.4 Attention Summary Register (RHAS) – REG 4 – This register consists of eight status bits, each corresponding to the ATA status bit of one drive. Bit 00 is the ATA bit of drive 0, bit 01 is the ATA bit of drive 1, etc. to bit 07. Bits 08–15 are not used. This read/write register is shown in Figure 4-7.

The timing of transfers on the control bus to and from this register is special. When this register (REG 4) is read by the controller, each drive gates its ATA bit out onto one of the C lines (drive 00 onto C00, etc.). Because all drives are responding at once, the normal handshake sequence is not valid. Instead, the controller waits the maximum delay time and then unconditionally strobes the C lines. The controller negates DEMAND after it has strobed the C lines. No drive may disable its C line output until it has negated transfer (typically after receiving the negation of DEMAND). When the transfer line becomes negated at the controller (after each drive has negated TRANSFER), the controller knows that the cycle is complete.

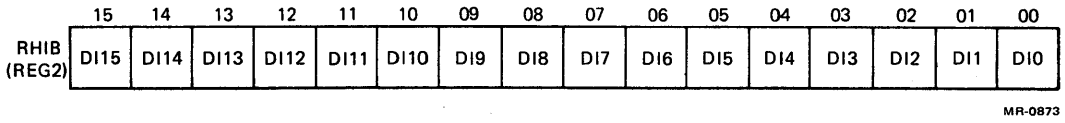


Figure 4-6 RHIB (REG 2) Bit Map

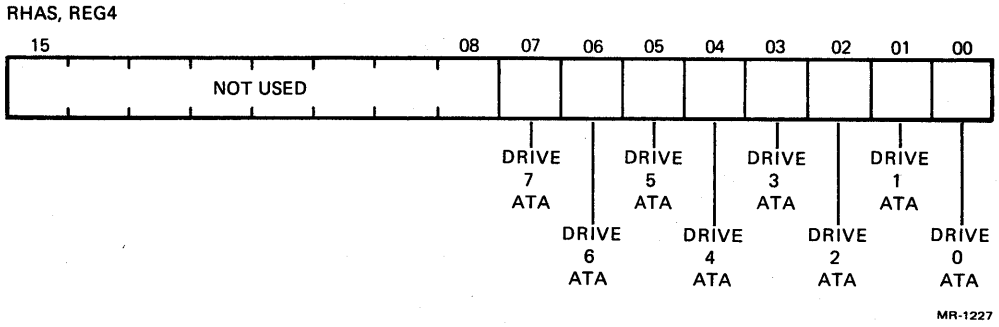


Figure 4-7 RHAS (REG 4) Bit Map

Since no single drive is generating all of the C bits, it is impossible for any drive to generate a valid parity bit. Therefore, the controller ignores the CPA line and does not check parity when reading the attention summary register.

When this register is selected, all drives respond. When reading this register, each drive presents its ATA bit in the appropriate bit position. When writing, each drive receives a bit from the control bus, and if the bit is set, the drive resets its ATA bit. For each bit position and drive, Table 4-1 applies when writing into this register.

Table 4-1 ATA Bit Status

Bit Written	ATA Before	ATA After
0	0	0
0	1	1
1	0	0
1	1	0

This scheme allows the program to reset the ATA bits which were already seen and acted upon, without accidentally resetting other ATA bits which may have become set in the meantime.

4.2.2.5 User Function and Status Register (RHFS) – REG 5 – This register provides eight general-purpose status bits and eight general-purpose user function bits. Each status bit reflects the state of a user-defined signal connected to the interface inputs (+3 V = 1, 0 V = 0). The output of the user function bits are made available to the user interface for any user-defined function. The register format is shown in Figure 4-8.

15–08 UF07–UF00 – User-defined function, read/write

07–00 ST07–ST00 – Status bit, read-only

4.2.2.6 Drive Type Register (RHDT) – REG 6 – This register is used to identify the interface types which exist on the Massbus. For the DR01-CL interface, this register always equals a 4 (000004 octal).

4.2.2.7 Output Buffer Register (RHB) – REG 7 – This write-only register provides a means of transferring a word of data to the user interface under program control. The outputs of this register appear on the DATA OUT lines (0:15). This register may not be used while a block data transfer command is in progress. The register format is shown in Figure 4-9. DATA OUT 16 and 17 cannot be written via this register (RHOB).

15–00 DO15–DO0 – Output data to user interface

4.2.3 Link Operation

In a link configuration the functional operation of the RHIS (REG 1) and RHFS (REG 5) bits differ from the standard operation. Paragraphs 4.2.3.1 and 4.2.3.2 define the RHIS (REG 1) and RHFS (REG 5) bits for a DTR01 interprocessor link operation.

NOTE

Link Relationship – Side A is the nearest interface; Side B is the farthest or other interface.

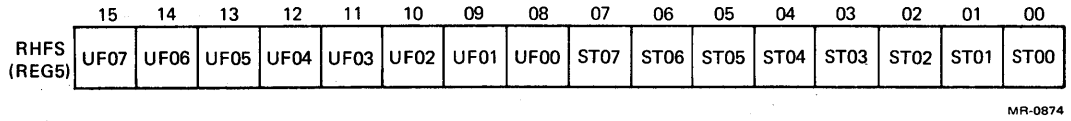


Figure 4-8 RHFS (REG 5) Bit Map

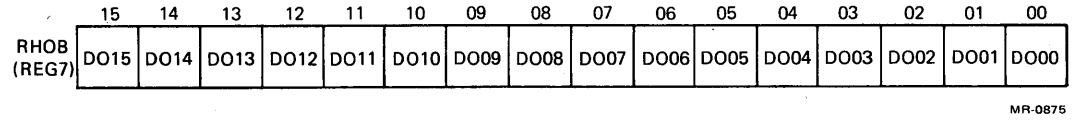


Figure 4-9 RHOB (REG 7) Bit Map

4.2.3.1 DR01-C/RH20 Registers Link Configuration* – RHCS1 (REG 0) is the same as the standard configuration. Refer to Figure 4-10 for bit map. RHIS (REG 1) is redefined as follows.

Bits	Description
15	ATA – Same as for standard definition
14	ERR – Composite error bit – includes LINK ERROR set by the other side. This is a read-only bit.
13–11	Not used
10	LINK ERR – Indicates that an error condition has been signaled from the other processor. This bit is set by the other processor writing its LKALERR bit in register 5. LINK ERR causes an ATTENTION INTERRUPT if INTERRUPT ENABLE is set. LINK ERR is normally used to terminate a data transfer if the word counts are not equal.
09	ICPE – Same as for standard definition
08	IDPE – Same as for standard definition
07	IRDY – Same as for standard definition
06–05	Not used
04	CYCLE – Maintenance-only bit
03	LATA03 – General-purpose link attention bit. This bit is set by the other processor setting its LINK FUNCTION 02 bit. Available for system software protocol definition.
02	LATA02 – General-purpose link attention bit. This bit is set by the other processor setting its LINK FUNCTION 01 bit. Available for system software protocol definition.
01	LKMASTER – Indicates to the processor that it has received control of the link. It is set after the other processor has released link mastership and a processor has set the LINK REQUEST bit in register 5. LKMASTER sets ATTENTION INTERRUPT and causes an interrupt if enabled.
00	LKBREQ – Indicates the state of the other processor's link request bit. LKBREQ is set when the other processor is requesting link mastership. LKBREQ sets ATTENTION INTERRUPT and causes an interrupt if enabled.

RHIB – (REG 2) This is the same as the standard configuration.

RHAS – (REG 4) This is the same as the standard configuration.

RHFS – (REG 5) The format of REG 5 is shown in Figure 4-11. RHFS (REG 5) is defined as follows.

* Also applicable for DR70A

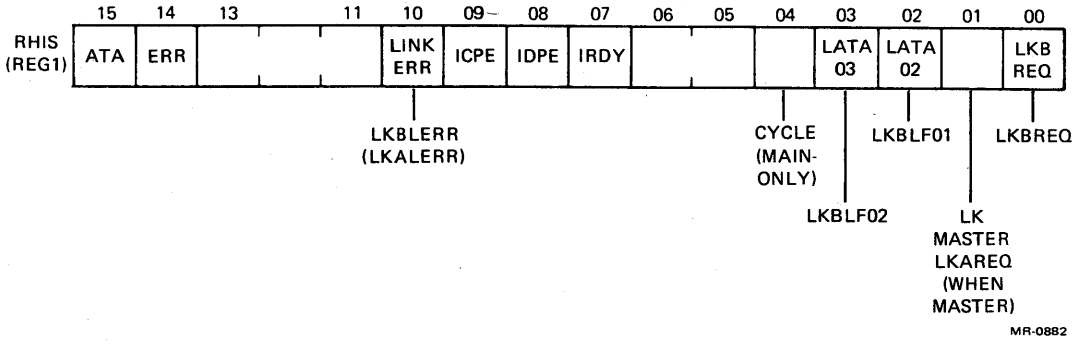


Figure 4-10 RHIS (REG 1) Link A

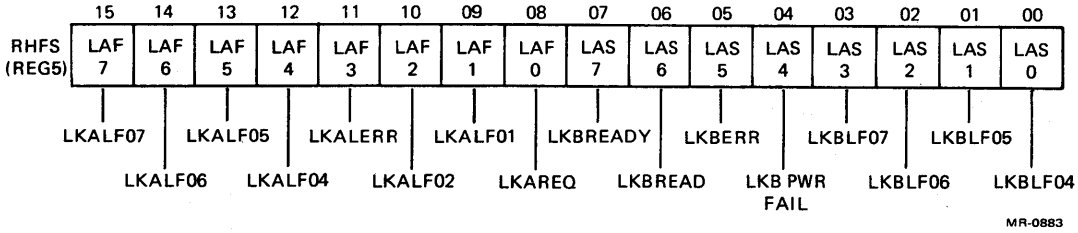


Figure 4-11 RHFS (REG 5) Link A

Bits	Description
15	LAF7-LKALF07 – General-purpose link function bit. Available to the system software protocol definition. Setting this bit sets LINK STATUS 03 on the B side.
14	LAF6-LKALF06 – General-purpose link function bit. Available to the system software protocol definition. Setting this bit sets LINK STATUS 02 on the B side.
13	LAF5-LKALF05 – General-purpose link function bit. Available to the system software protocol definition. Setting this bit sets LINK STATUS 01 on the B side.
12	LAF4-LKALF04 – General-purpose link function bit. Available to the system software protocol definition. Setting this bit raises LINK STATUS 00 on the B side.
11	LAF3-LKALERR – Link A link error bit. This bit is provided to the software to signal an error condition to the B side. This will cause the other side's ERR and ATA bits to set causing an interrupt. This bit normally terminates a data transfer if the word counts are not equal.
10	LAF2-LKALF02 – General-purpose link function bit. Available to the system software protocol definition. Setting this bit sets LINK ATTENTION 03 on the B side.
09	LAF1-LKALF01 – General-purpose link function bit. Available to the system software protocol definition. Setting this bit sets LINK ATTENTION 02 on the B side.
08	LAF0-LKAREQ – Link A side request bit. LINK REQUEST is asserted by processor A to become link master. If the other processor is not in control of the link, the requesting processor immediately becomes link master. Setting LINK REQUEST interrupts the other processor and sets LINK REQUEST ATTENTION on the B side. LKAREQ also sets LKMASTER ATTENTION on the A side when A becomes link master.
07	LAS7-LKBREADY – Link B side ready bit. Status bit provided to the A side indicating that the Link B side is ready for a transfer operation. This is a read-only bit.
06	LAS6-LKBREAD – Link B side read function line. Status bit provided to the A side indicating that the B side link is set up for a read data transfer to the B side. This is a read-only bit. Valid only when read bit is 0. When cleared, this bit indicates write.
05	LAS5-LKBERR – Link B side error bit. Status bit provided to the A side indicating that the B side has an active ERROR condition set. This is a read-only bit.
04	LAS4-LKB PWR FAIL – B power fail indicates a power failure condition in the other interface. This is a read-only bit.
03	LAS3-LKBLF07 – General-purpose link status bit. Available for system software protocol definition. Set by Link B side LINK FUNCTION bit 07. This is a read-only bit.
02	LAS2-LKBLF06 – General-purpose link status bit. Available for system software protocol definition. Set by Link B side LINK FUNCTION bit 06. This is a read-only bit.
01	LAS1-LKBLF05 – General-purpose link status bit. Available for system software protocol definition. Set by Link B side LINK FUNCTION bit 05. This is a read-only bit.

00 LAS0-LKBLF04 – General-purpose link status bit. Available for system software protocol definition. Set by Link B side LINK FUNCTION bit 04. This is a read-only bit.

RHDT – (REG 6) This is the same as the standard configuration.

RHOB – (REG 7) This is the same as the standard configuration.

4.2.3.2 DR01-C/DR11-B Register Link Configuration – Only the following bits are redefined as indicated on the following bit maps of RHIS (REG 1) and RHFS (REG 5). These redefined bits are described in Paragraph 4.2.3.1. Refer to Figure 4-12 for bit map.

Bits	**Description**
03	LATA 3 – General-purpose link attention bit. This bit is set by the other processor setting its Function 3 bit in the DR11-B interface. Available for system software protocol definition. Causes an ATA interrupt if enabled.
02	LATA 2 – General-purpose link attention bit. This bit is set by the other processor setting its Function 2 bit in the DR11-B interface. Available for system software protocol definition. Causes an ATA interrupt if enabled.
00	LKB REQ – Indicates that the other processor is requesting a transfer by setting its Function 1 bit in the DR11-B interface. Causes an ATA interrupt if enabled.
14	LAF6 – (LKALF06) General-purpose link function bit, available to system software for protocol definition. This bit set asserts the DSTAT C input line of the DR11-B.
13	LAF5 – (LKALF05) General-purpose link function bit, available to system software for protocol definition. This bit set asserts the DSTAT B input line of the DR11-B.
12	LAF4 – (LKALF04) General-purpose link function bit, available to system software for protocol definition. This bit set asserts the DSTAT A input line of the DR11-B.
11	LAF3 – (LKAREQ) Raises the ATTN line on the DR11-B interface. Available to system software for general-purpose definition to indicate an error condition or a transfer request.
07	LAS 7 (LKDBRDY) DR11-B side READY bit. Status bit provided to the A side to indicate that DR11-B is able to accept a new transfer command. Refer to Figure 4-13 for bit map.

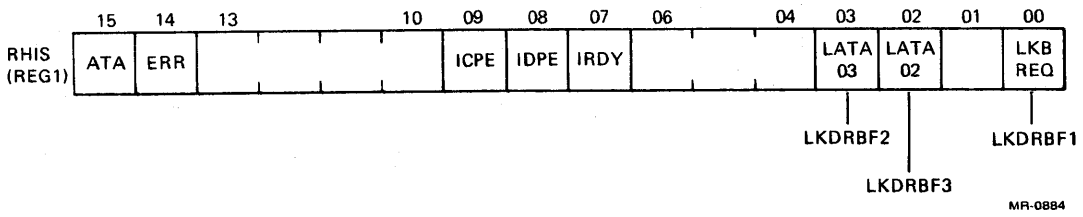


Figure 4-12 RHIS (REG 1) Link B

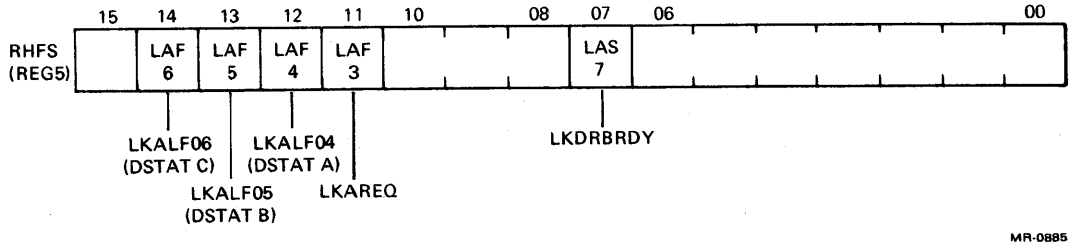


Figure 4-13 RHFS (REG 5) Link B

CHAPTER 5
TECHNICAL DESCRIPTION

5.1 SYSTEM DESCRIPTION

Figure 5-1 is a typical DTR01 subsystem. The basic unit in the DTR01 subsystem is the DR01-CL channel interface unit. The DR01 allows a user device to perform high-speed block data transfers to or from memory via the Massbus and an appropriate Massbus controller. The transfer rate is determined by the user device. Provisions have been made in the DR01 to limit the transfer rate of the user device so that it will not exceed the bandwidth of the system.

Normally the DR01 is used in conjunction with an RH20 Massbus controller as shown in Figure 5-1. A maximum of eight DR01s can be daisy-chained together with the first DR01 connected to the RH20 via the Massbus and the last DR01's Massbus connected to a Massbus terminator pack.

5.2 DATA TRANSFERS

Communication and control between the DTR01 subsystem and the host processor is implemented with seven programmable registers located in each DR01-CL channel interface unit (see Figure 5-2). The registers are loaded and cleared by DATAO and read by DATAI instructions from the CPU (see Paragraph 4.2). The actual data transfer between the user device and the CBus is enabled using a read or a write from the register control (see Figure 5-3). During a write operation, data is placed onto the CBus and travels via the RH20 write register from the Massbus to the DR01 interface and then over the device data lines to the device. During a read operation, data travels over the device data lines through the DR01 interface to the Massbus data lines and then onto the CBus via the RH20 data buffer read register. The following is a description of how these data transfers are accomplished.

The seven function registers are used to perform data transfers by performing the following steps.

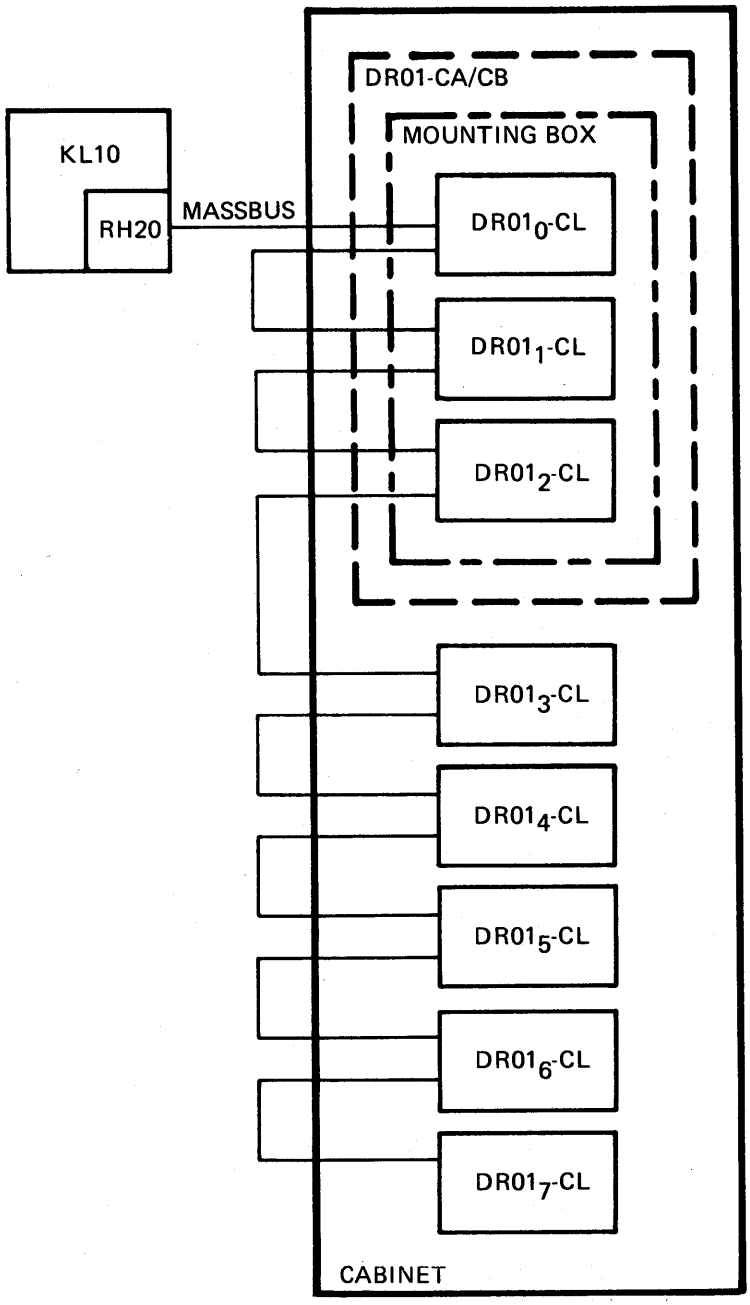
1. Determine if the DR01 interface is ready.
2. Load the user function/status as defined in the protocol.

Paragraph 4.2.1 provides the information for programming these steps using DATAO and DATAI instructions to read or write the seven external registers located within each DR01. Paragraph 4.2.2 provides a detailed description of the contents of each of the seven registers. Figures 5-4, 5-5, and 5-7 through 5-12 are flow diagrams which provide the data flow within the DR01 control (8431), the DR01 test card (8432) and the three Massbus transceivers (MB1, MB2, and MB3) for the DR01 registers.

5.2.1 REG 0 (RHCS1) Control and Status Register Signal Flow

As shown in Figure 5-4, the control and status register generates the function code and GO pulse to enable a READ, WRITE or INTERFACE CLEAR. It also contains the drive ready status (DRY). DRY is an unconditional status bit returned. This register is selected to be loaded or read onto the Massbus by DATAO or DATAI instructions from the KL10-B, C, D or E CPU.

All Massbus lines of the DR01 logic are reset by INIT which becomes true (+3 V) whenever the Massbus is initialized. The DR01 is initialized also when an INTERFACE CLEAR command (RHCS1, REG 0 bits 05–00 = 11_8; see Paragraph 4.2.2.1) is received by the interface. This means bit 00 or the GO bit = 1.



CONFIGURATION RULES:

1. MAX 8 DR01-CL per Massbus (RH20).
2. Dedicated RH20 for DR01 subsystem; no sharing.
3. MAX 1 Massbus per DR01 box
4. MAX 2 Massbus per cabinet.
5. MAX 3 DR01-CL per DR01 box
6. MAX 3 DR01 box per cabinet
7. Only 1 second system box per cabinet (DTR01-CC/CD).
8. If second system box in cabinet, max configuration is:
   MB NO 1 = 3 DR01-CL
   MB NO 2 = 6 DR01-CL

MR-0869

Figure 5-1 A Typical DTR01 System

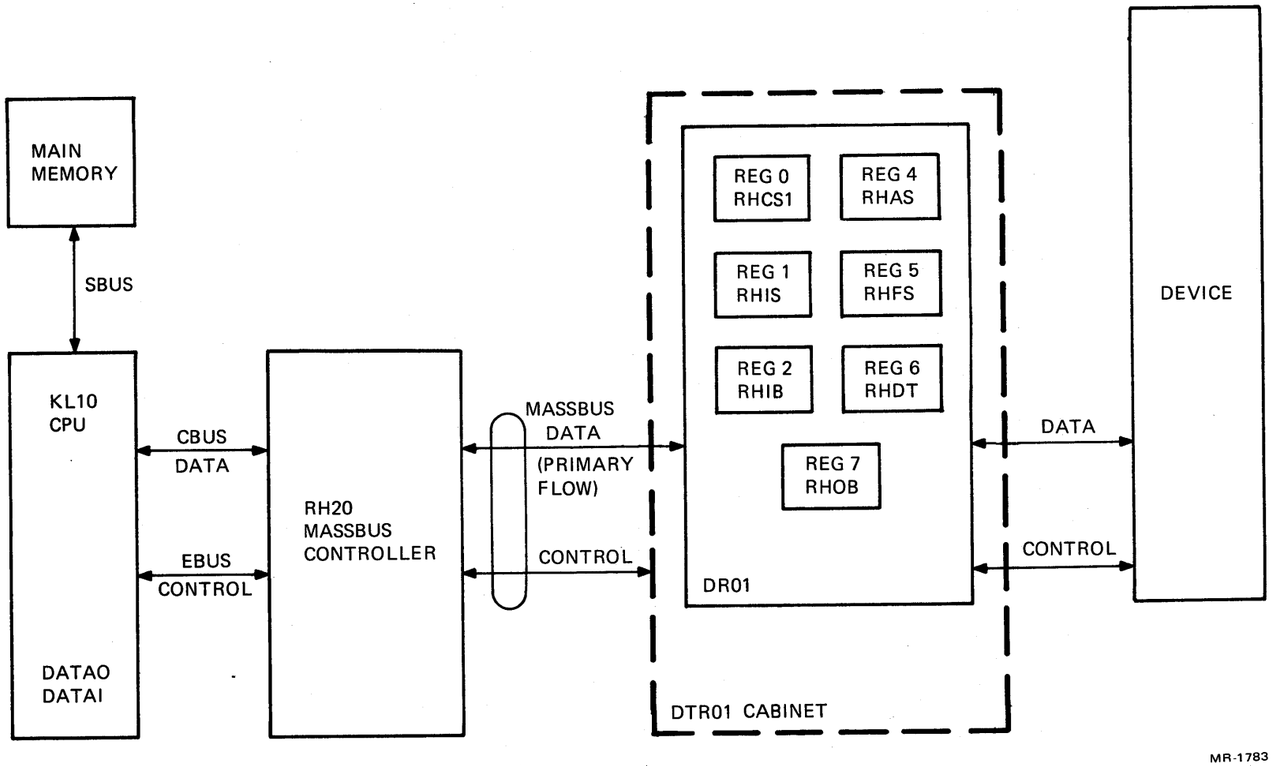


Figure 5-2 Communication Between DTR01 and KL10-B, C, D or E Processor

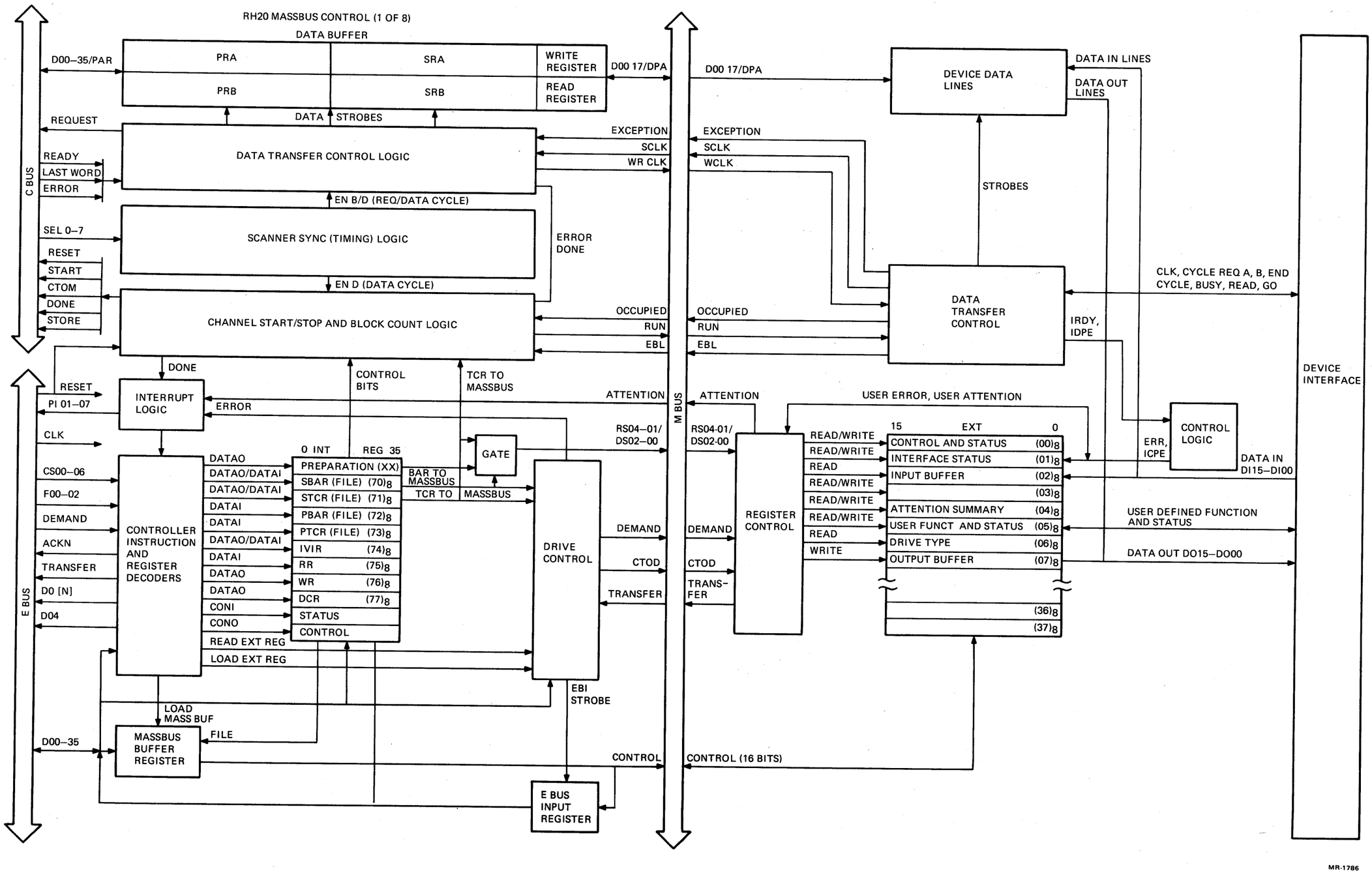


Figure 5-3 DTR01 Subsystem Data Flow Block Diagram

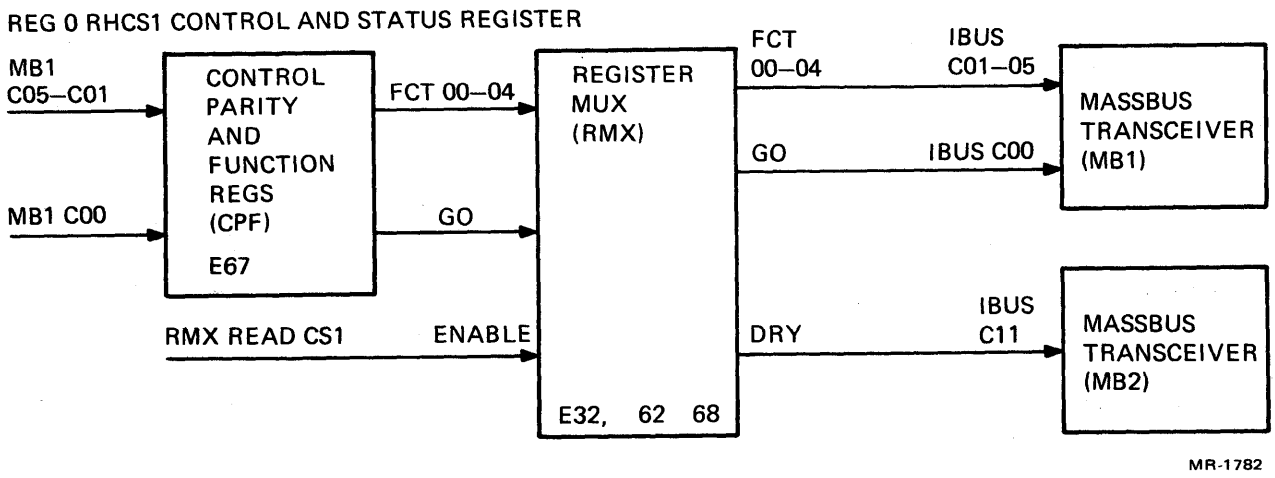


Figure 5-4 REG 0 (RHCS1) Control and Status Register
Circuit Block Diagram

The contents of RHCS1, REG 0 bits 01–05 are decoded to determine the type of command to be executed by the logic. Any invalid command code (other than READ, WRITE or INTERFACE CLEAR) will hang the DR01-CL interface in the busy state (GO = 1).

The GO bit is cleared at the completion of the data transfer command (negation of RUN from the Massbus). If the INTERFACE CLEAR command is issued, the GO bit remains set and INTERFACE CLEAR is asserted until the next command is received. Each time a new valid transfer command (READ or WRITE) is written into the command register, a GO pulse is generated to the user interface. The GO bit, if set, is readable also back to the CPU.

5.2.2 REG 1 (RHIS) Interface Status Register Signal Flow (See Figure 5-5.)
READY indicates that the interface is ready to do data transfers. READY occurs when BTC ENBL is low.

AS0–7 for attention summary register use is produced by the BCD decoder, E80 on the interface status register (ISR) when TCB AT00–AT03 are present. MB ATTN is produced at E63 flip-flop using TCB AT00–AT03. ERR and USER ERR are status bits which use the USA user error. The IDPE and ICPE are produced via the parity generation and checking circuitry. Control signal inputs to this circuit are RMX I BUS C00–C07 and RMXB I BUS C08–C15 and the data inputs to this circuit are MB1 D00–D05, MB2 D06–D11, and MB3 D12–D17. Parity is generated in the control parity and function registers (CPF) and output buffer registers (OBR and OBRB). Any parity errors are sent via interface status register (ISR) to the same circuit that produced ERR and USER ERR.

As shown in Figure 5-5, the interface status register generates the CYCLE bit. A data transfer is usually initiated when the cycle flip-flop is set either by the logical OR of the CYCLE REQUEST A or B user input lines or via the program writing a CYCLE bit, bit 04 of RHIS REG 1 (see Paragraph 4.2.2.2). As shown in the timing diagram (Figure 5-6), a data transfer cycle (either READ or WRITE) then begins provided that the previous cycle has been completed (indicated by the negation of BUSY and READY and while the interface is still receiving RUN from the Massbus). BUSY is asserted for each word or byte transferred. BUSY is also used to indicate the beginning of a new data transfer cycle.

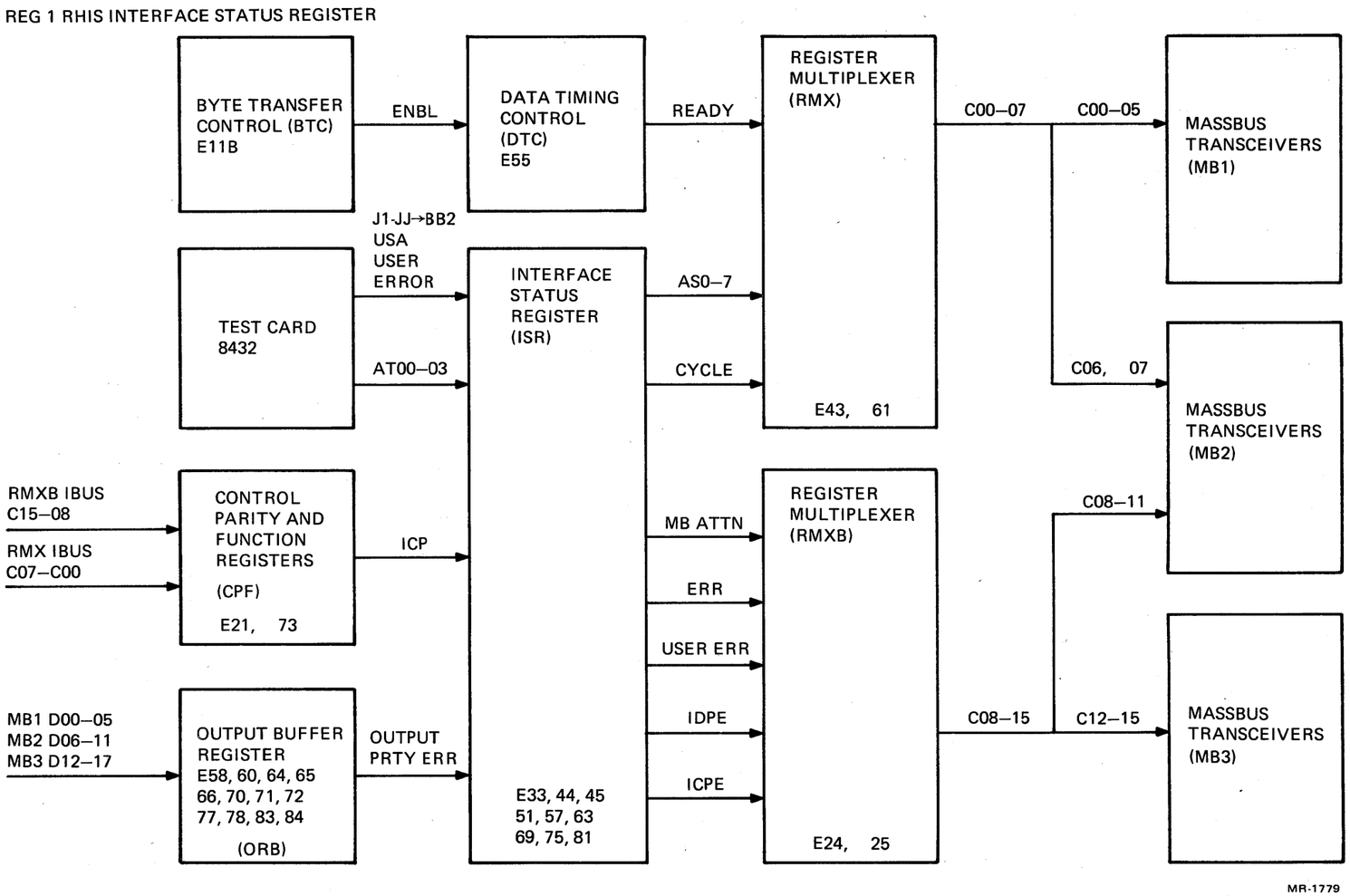


Figure 5-5 REG 1 (RHIS) Interface Status Register Circuit Block Diagram

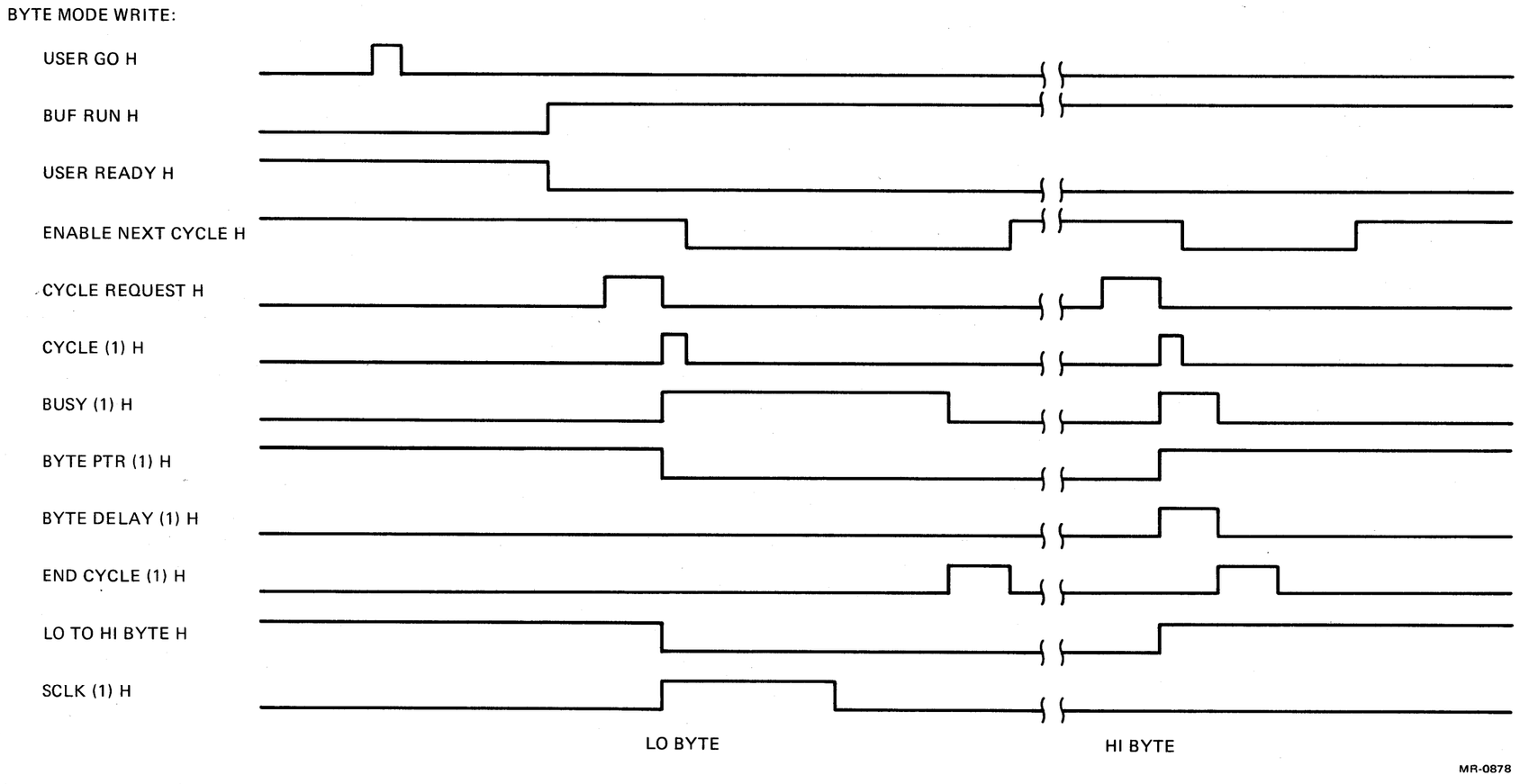


Figure 5-6 DTR01 Timing (Sheet 1 of 2)

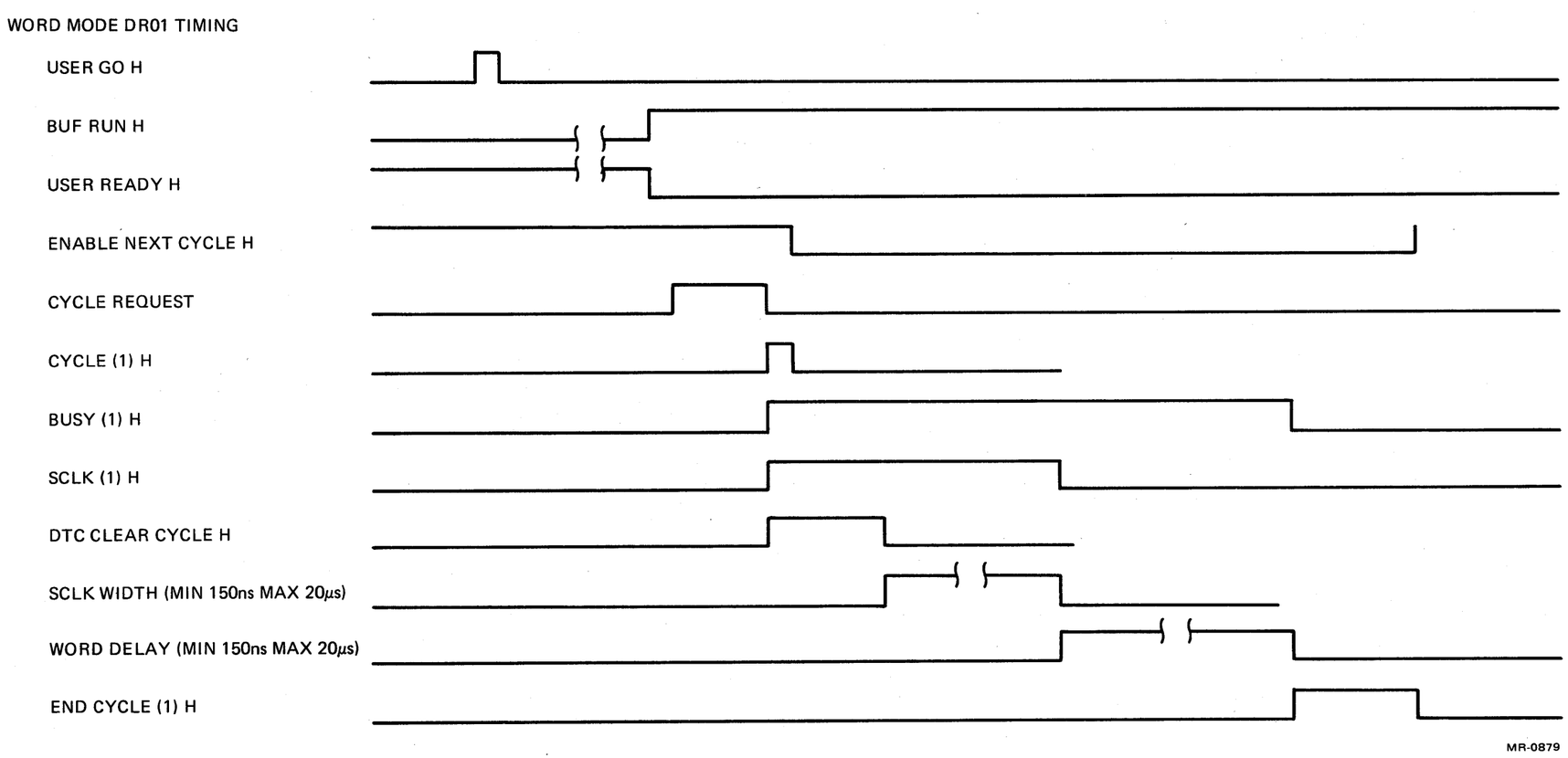


Figure 5-6 DTR01 Timing (Sheet 2 of 2)

If CYCLE REQUEST is received before the completion of the previous cycle, the request is stored and the new data transfer cycle begins as soon as the previous cycle is completed. Thus, the user device can overlay cycles so that the interface is primed to begin another cycle immediately upon completion of the first. If a CYCLE REQUEST is received before a valid data transfer command, it is ignored.

When a write command is received (RHCS1, REG 0 bits 05–00 = 61_8) from the host, negation of either CYCLE REQUEST A or B occurs. The DR01 data transfer control strobes out the data and the host may change the data lines if desired.

Completion of the data transfer is indicated by the negative transition of the BUSY signal and the assertion of the END CYCLE signal.

The BUSY signal is cleared as soon as the END CYCLE signal is asserted. The data from the previous cycle remains valid on the data lines until the new data is received from the Massbus controller. New data will be presented on the data lines along with the optional parity bit as soon as the data transfer cycle is complete (END CYCLE asserted and BUSY cleared). The data lines become stable when BUSY clears. The user device may then delay initiating another cycle until it has processed the data or it may immediately initiate another cycle if the data is strobed within the next 250 ns. BUSY will set immediately following the negative transition of CYCLE REQUEST only if the interface has completed the previous data transfer operation and READY is reset.

During a read operation, a READ command is received (RHCS1, REG 0 bits 05–00 = 71_8) from the host. The user device must provide the DATA IN (0–15) signals plus the optional parity bit (DPA IN LO and DPA IN HI). If parity is not used, the Input Parity Inhibit (IPI) signal must be asserted by the user interface to prevent an undesired parity error indication. Use of additional data bits (bits 16 and 17) is intended for interfacing to larger machines. They are not used with the PDP-11 systems. (See Figure 5-7.)

This interface performs no data packing or formatting of the data passed between the host and the user interface. For a read, device data lines from the user must be stable 50 ns prior to the high-to-low transition of either CYCLE REQUEST A or B. The user device must maintain the data lines stable until the cycle begins with the positive transition of the BUSY signal. At this point, the interface has strobed in the data and the user device may change the data lines if desired. Completion of the data transfer will be indicated by the negative transition of the BUSY signal and the assertion of the END CYCLE signal. The BUSY signal will be cleared as soon as the END CYCLE signal is asserted.

5.2.3 REG 2 (RHIB) Input Buffer Register Signal Flow

An alternate method of performing a read is by using the input buffer register (RHIB) REG 2 as shown in Figure 5-8 using a DATAI instruction from the KL10-B, C, D or E CPU. This transfer is performed over the Massbus C lines instead of over the CBus data lines as in the primary method described previously.

5.2.4 REG 4 (RHAS) Attention Summary Register Signal Flow

As shown in Figure 5-9, the attention summary register (RHAS) REG 4 uses the AT00–AT03 at the user device interface via the test card and the device select code US00–02 to develop the AS00–AS07 signals. The interface only asserts one bit if it reads attention service corresponding to its device select code.

5.2.5 REG 5 (RHFS) User Function and Status Register Signal Flow

As shown in Figure 5-10 Massbus control signals C08–C14 are used for the FR00–07 general-purpose user function bits which are user-defined. The DS00–07 general-purpose status bits reflect the state of user-defined signals connected to interface inputs via the test card. Both groups of eight signals are sent via the Massbus transceivers to the Massbus when the user function and status (RHFS) register is read.

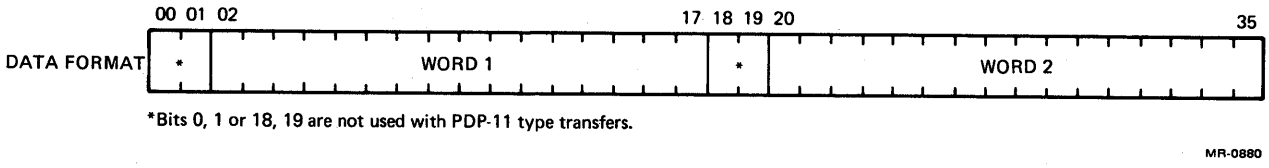


Figure 5-7 Data Format

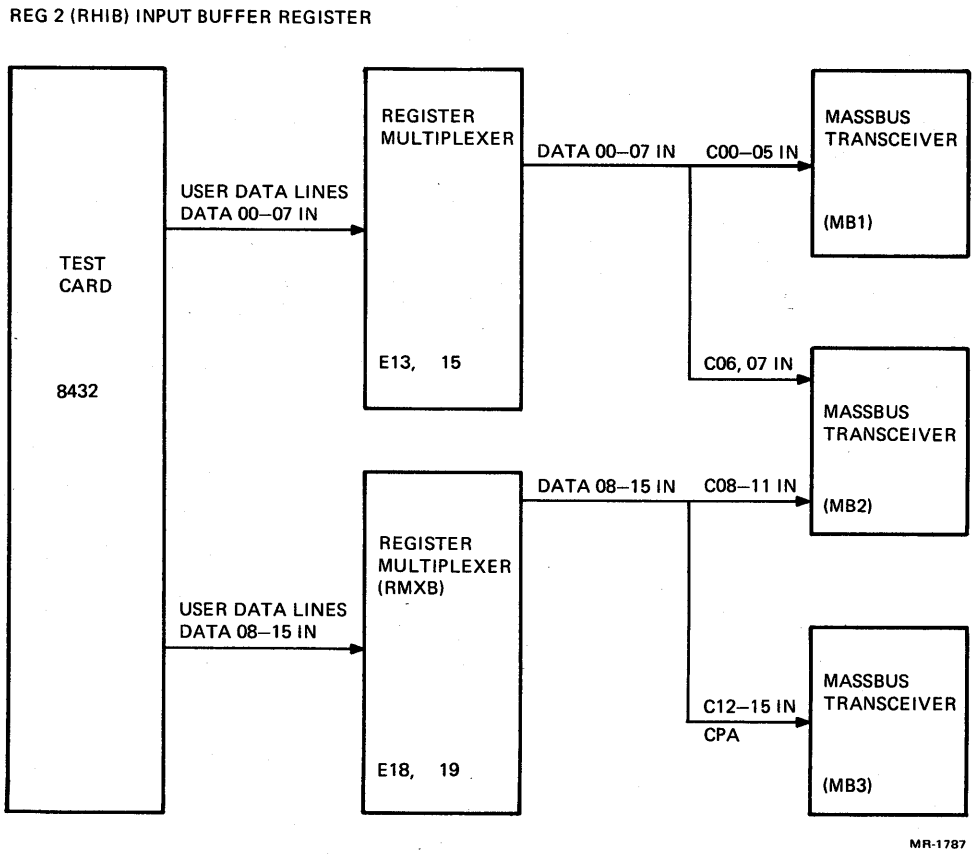


Figure 5-8 REG 2 (RHIB) Input Buffer Register Circuit Block Diagram

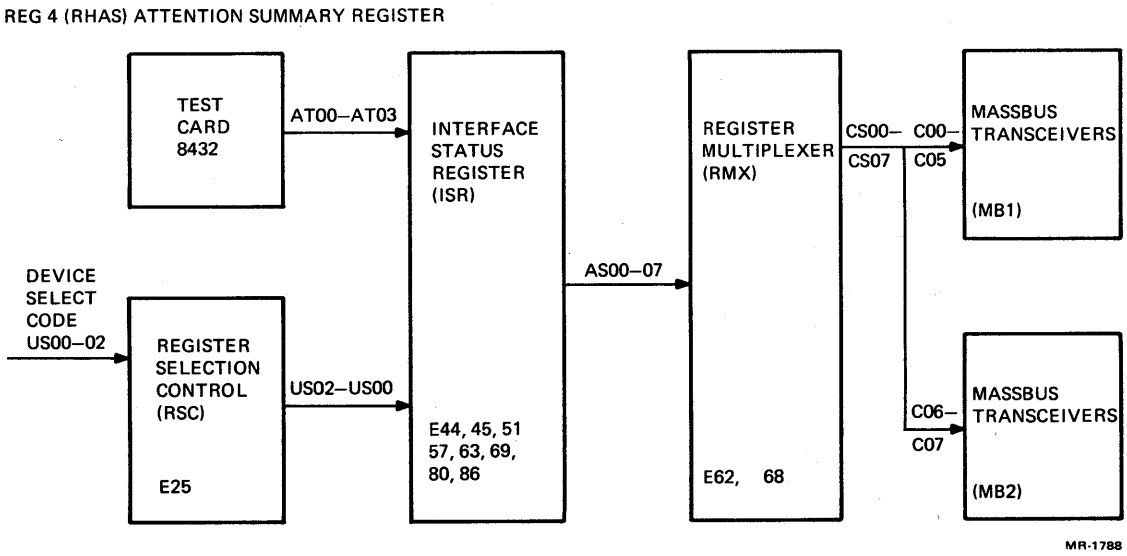


Figure 5-9 REG 4 (RHAS) Attention Summary Register Circuit Block Diagram

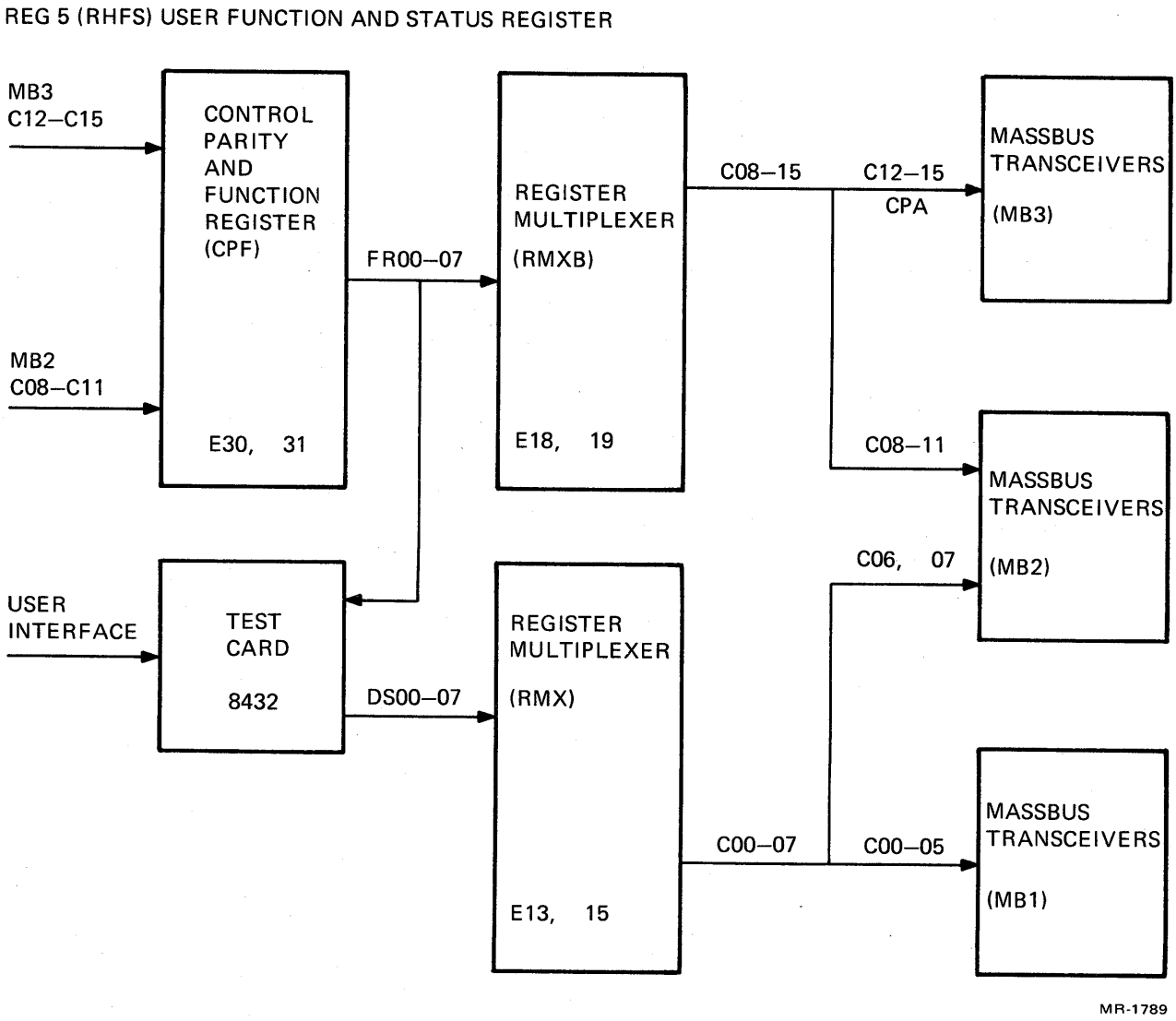


Figure 5-10 REG 5 (RHFS) User Function and Status Register Circuit Block Diagram

5.2.6 REG 6 (RHDT) Drive Type Register Signal Flow

Figure 5-11 illustrates the drive type circuit which uses the SEL RHDT signal to produce a 4_8 drive type code on control line 02 to the Massbus via Massbus transceiver MB1.

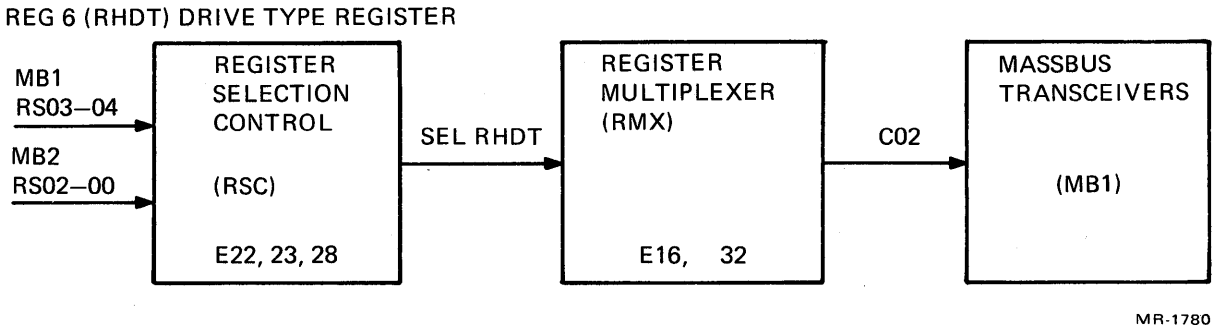


Figure 5-11 REG 6 (RHDT) Drive Type Register Circuit Block Diagram

5.2.7 REG 7 (RHOB) Output Buffer Register Signal Flow

An alternate method of performing a write is by using the output buffer register (RHOB) REG 7 as shown in Figure 5-12 using a DATAO instruction from the KL10-B, C, D or E CPU. This transfer is performed over the Massbus C lines instead of over the CBus data lines as in the primary method described previously.

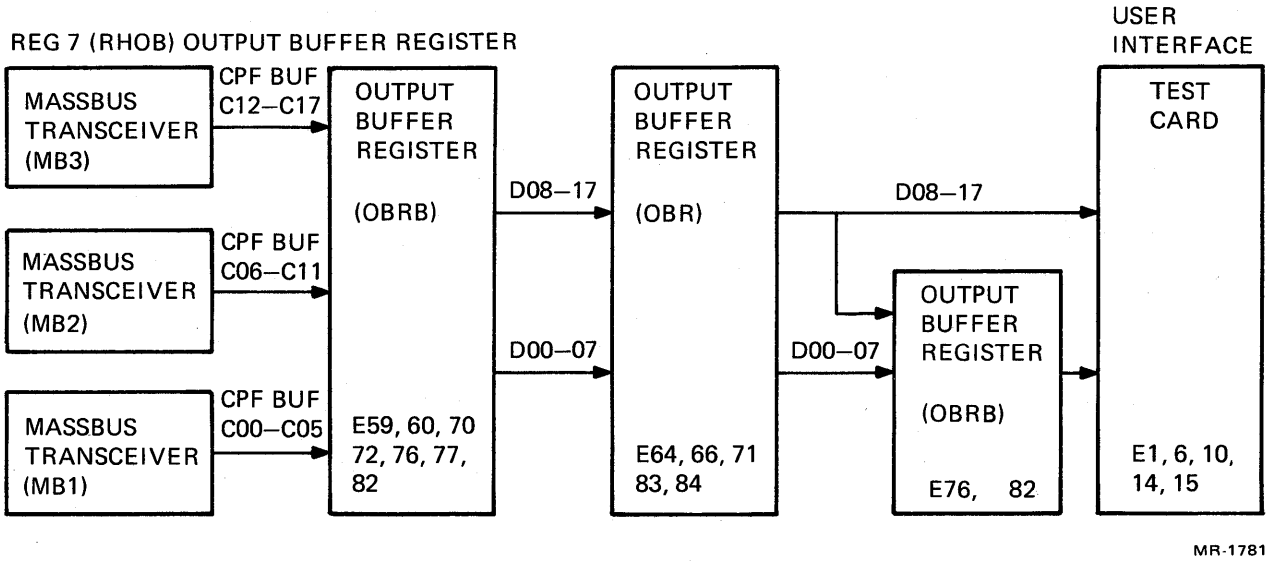


Figure 5-12 REG 7 (RHOB) Output Buffer Register Circuit Block Diagram

5.3 LINK OPERATION

The DTR01-C can be used to establish a high-speed interprocessor link between separate computer systems. This is accomplished by interconnecting two DR01-CL units, one on each system; or with a DR11-B interface via a BC11A type cable. The functional operation of the RHIS (REG 1) and RHFS (REG 5) bits differ from the standard operation. (See Paragraph 4.2.2.) Figure 5-13 shows how DTR01 link connectors are implemented. See Tables 5-1 and 5-2.

NOTE

Link relationship – Side A is the nearest interface, Side B is the farthest or other interface.

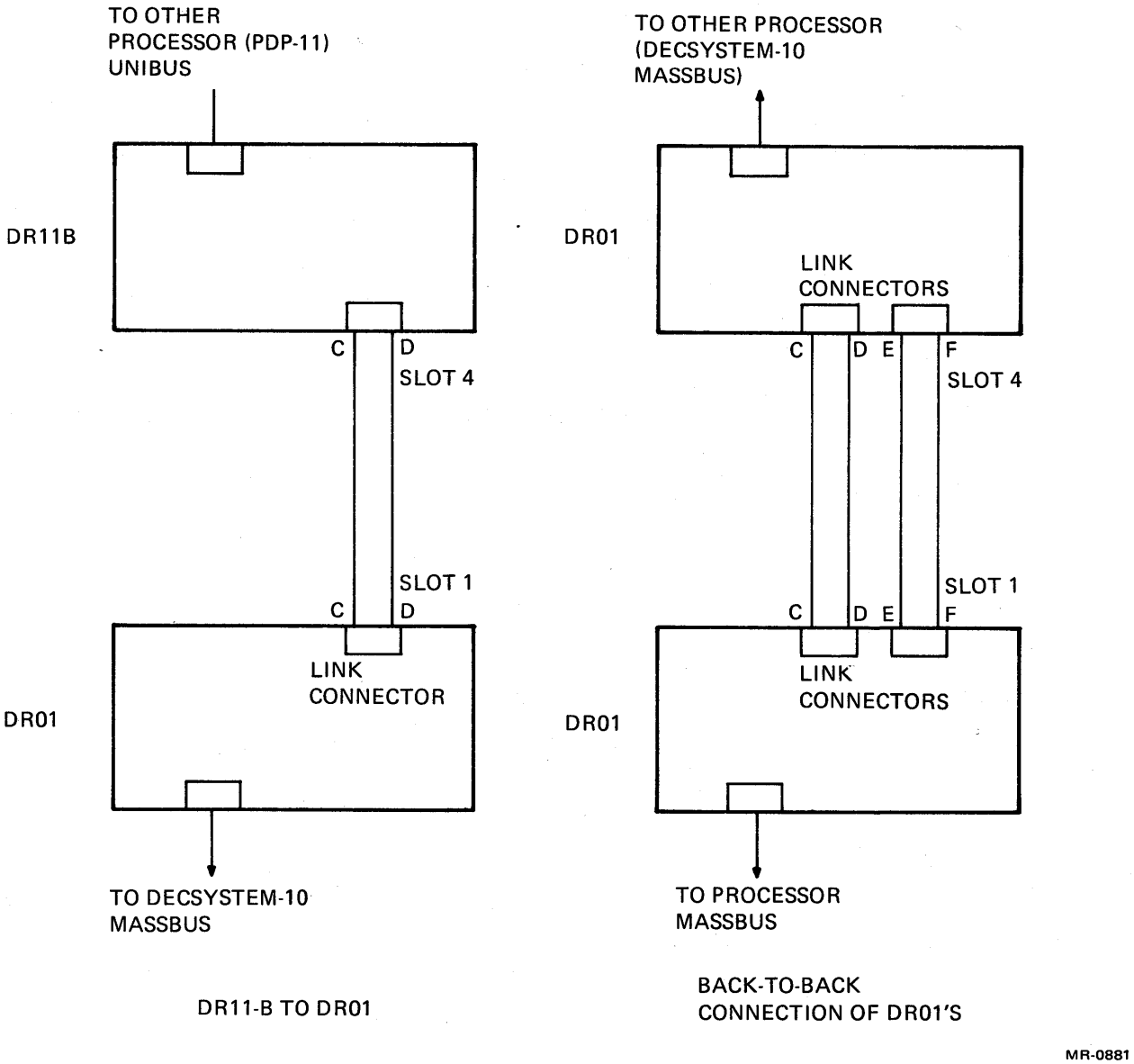


Figure 5-13 DTR01 Link Connectors

The back-to-back interconnection of two DR01s is shown in Figure 5-14.

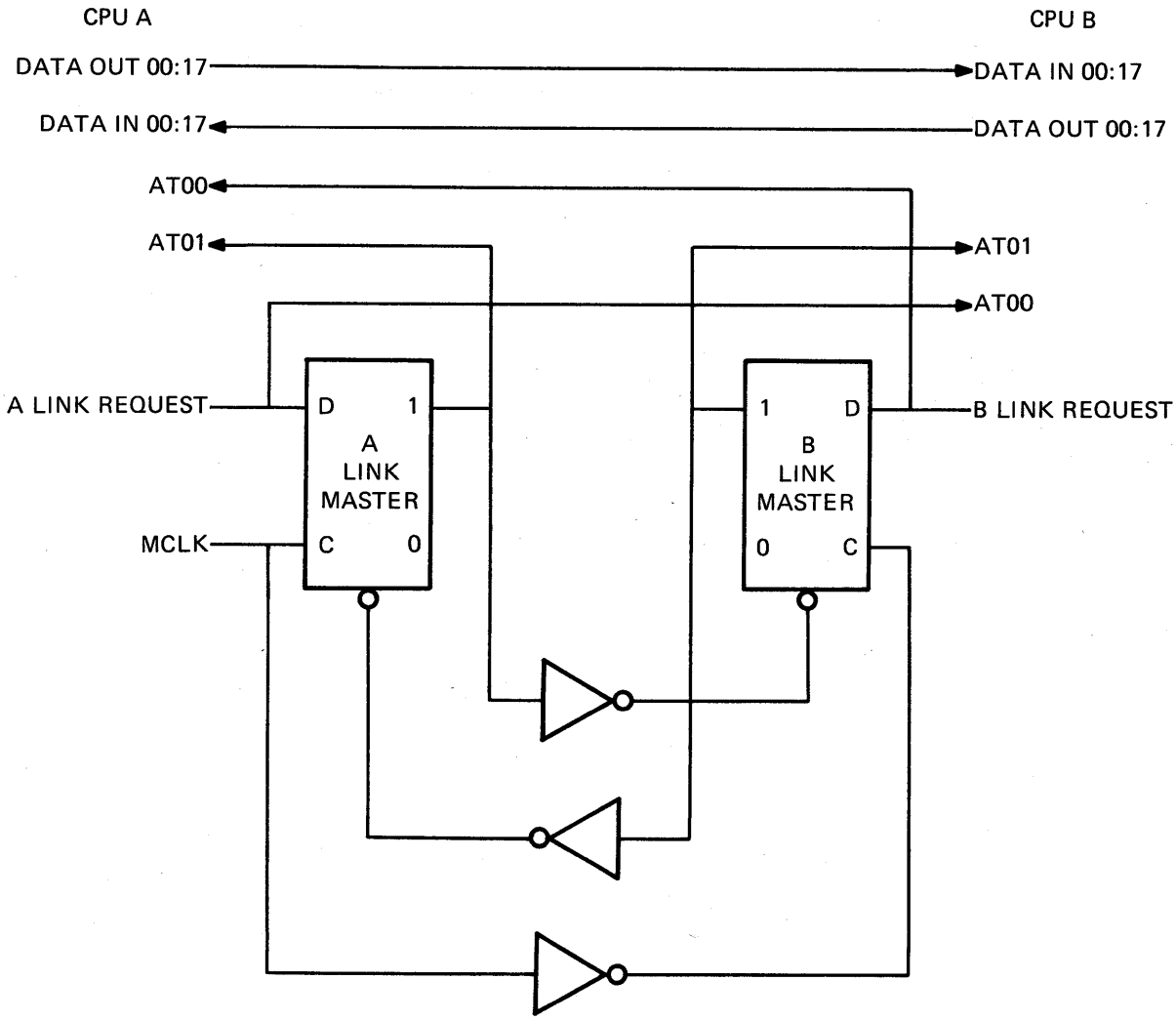


Figure 5-14 DTR01 Back-to-Back Signal Connections

Table 5-1 DR01 to DR01 Signal Connections

CPU A (DR01)	CPU B (DR01)
USA CYCLE REQUEST A	TCC END CYCLE
TCB FR00–FR02	USB AT00, AT02, AT03
DTC READY	USB DS07
TCC DATA 01–15 OUT	USA DATA 00, 02–15 IN
TCC READ	USB DS06
TCC END CYCLE	USA REQUEST CYCLE A
USA DATA 00–15 IN	TCC DATA 00–15 OUT
USA DS01	TCB FR05
USA ERROR	TCB FR03
+3 V SOURCE	DRB ENB
USA DS00, 02	TCB FR04, FR06
USB DATA 16 IN	TCB DATA 16 OUT
TCB DATA 16 OUT	USB DATA 16 IN
USB DPA LO IN	TCB LO PAR OUT
USB DPA HI IN	TCB HI PAR OUT
USB INHIBIT INPUT PARITY	
USB DATA 17 IN	TCB DATA 17 OUT
USB AT01	LOCKOUT
USB AT00, 02, 03	TCB FR00–FR02
USB WORD MODE	+3 A
+3 VC	USB USER WORD MODE
USB DS06	TCC READ
MCLK	E01F2
FDC ARB CLK	
FDC LINK MASTER (1) B	LOCKOUT
USB DS03	TCB FR07
USB DS04	AC LO
USB DS05	ISR ERR (1) B
USB DS07	DTC READY
FDC ARB CLK	MCLK
TCB DATA 17 OUT	USB DATA 17 IN
TCB HI PAR OUT	USB DPA HI IN
TCB LO PAR OUT	USB DPA LO IN
TCB FR03	ERROR
LOCKOUT	USB AT01
	FDC LINK MASTER (1) BH
TCB FR04–FR06	USA DS00–DS02
TCB FR07	USB DS03
ISR ERR (1) B	USB DS05
AC LO	USB DS04

Table 5-2 DR11-B to DR01 Signal Connections

CPU A (DR11-B)	CPU B (DR01)
D6 CYCLE REQUEST A	TCC END CYCLE
D6 END CYCLE OUT	USA REQUEST CYCLE A
D6 DAT 00–15 IN	TCC DATA 00–15 OUT
D6 DSTAT B	TCB FR05
D6 ATTN	TCB FR03
+3V F03 U1	DRB ENB
D6 WC INC ENB	
D6 DSTAT A, C	TCB FR04, TCB FR06
BA INC ENB	DRB INB
D6 FNCT 1, 2, 3	USB AT00, AT03, AT02
D6 READY	USB DS07
D6 DAT00–15 OUT	USA DATA 00–15 IN
D6 C1 CONTROL	FDC READ B
SINGLE CYCLE	DRB ENB

CHAPTER 6
PREVENTIVE MAINTENANCE

6.1 GENERAL

In addition to the normal preventive maintenance checks recommended for DEC devices, the corrective maintenance procedure (Paragraph 7.2) should be run periodically to check the DR01 operation.

Since there are no console switches on the KL10-B, C, D or E, the 16 switches on the PDP-11 are used together with 20 software switches to make up the 36 KL10-B, C, D or E switches. In stand-alone mode, the rightmost 16 address switches on the PDP-11 are mapped to the leftmost 16 switches for the KL10-B, C, D or E, the rightmost 20 KL10-B, C, D or E switches are software-defined, using the console command SW.

The 20 software switches may be examined at any time (even during typeout) by typing the following.

<CONTROL X>SW<CARRIAGE RET>

The software switches may be set at any time by typing:

<CONTROL X>SW<lefthalf> <righthalf>

where: <lefthalf> is the desired octal value of the left half of the switches (See Table 6-1)

<righthalf> is the desired octal value of the right half of the switches (See Table 6-2).

Table 6-1 Left Half Switches - Standard Definition

-10 SW	-11 SW	Octal	Use When 1	Meaning
0	15	400000	ABORT	Abort diagnostic at the end of the current pass
1	14	200000	RSTART	Restart diagnostic
2	13	100000	TOTALS	Print statistics
3	12	040000	NOPNT	Inhibits all but forced printouts
4	11	020000	PNTLPT	Output to LPT (or logical device in user mode)
5	10	010000	DING	Ring the bell on error (this is forced)
6	9	004000	LOOPER	Loop on error
7	8	002000	ERSTOP	Halt on error (switch ignored if in user mode)
8	7	001000	PALERS	Print all errors
9	6	000400	RELIAB	RELIAB - do each test more than once
10	5	000200	TXTINH	Shorten error printout
11	4	000100	INHPAG	Inhibit paging
12	3	000040	MODDVC	Not used
13	2	000020	INHCSH	Inhibit operation of the cache
14	1	000010	OPRSEL	Operator select
15	0	000004	CHAIN	Not used
16		000002	KAHZ50	Not used
17		000001	RESERVED	Not used

Table 6-2 Right Half Switches - Standard Definition

-10 SW	Octal	Use When 1	Meaning
18	400000	TRASW	Trace current test number
19	200000		Not used
20	100000		Not used
21	040000		Not used
22	020000		Not used
23	010000		Not used
24	004000	RCFGSW	Allow reconfiguration at the end of main diagnostic logic
25	002000	INHRSW	Skip portion of pass count printout
26	001000	LOOPTS	Loop on current test
27	000400	SPCTST	Loop on specific test
28–35	000377	TSTMSK	Mask for specific test number

The leftmost 16 KL10-B, C, D or E switches are unaffected by the SW command. The switches can be changed while the program is running by typing the following.

<CONTROL G>

In user mode, the switch definitions remain the same as in EXEC mode. However, all 36 switches are software-defined. When the diagnostic is started or restarted, the user will be asked about the switches and may then respond with the following options.

Response	Meaning
O	Leave switches 0.
S	Same as the last time switches were specified.
Y	Allows user to specify the switces in octal.
N	KL10: leave switches 0. KL10, KI10: use physical console switches.

6.2 HIGH PERFORMANCE CHECKOUT

The DR01 is a high-performance device and system problems caused by the simultaneous operation of a number of high performance options can be just as detrimental as a logic problem in the DR01. It is therefore recommended that the performance of systems containing a DR01 be thoroughly evaluated at the time of installation and after any major change in the system configuration. To evaluate the performance of the system, run the DTR01 diagnostic, DFDRA.A10 as instructed in the diagnostic listing under the monitor in user mode with other system modules simultaneously. If problems develop such as data late errors on any device in the system, attempt to correct the problem by limiting the transfer rate of the DR01.

A console mode is provided in the diagnostic to assist in accessing internal and external registers. Table 6-3 lists the commands used for the diagnostic console command mode.

Table 6-3 Command Data Commands

Command	Meaning
CFG	Change configuration
CMO	Change printout mode
CNI	Do CONI to read control status in RH20
CNO	Do CONO to load control data in RH20
CSW	Reset switch
DDT	Go to DDT
EXT	Back to program dispatcher
HLP	Print HELP message
IDT	Identify configuration
LAS	Load attention summary register
LCS	Load control and status 1 register
LDC	Load diagnostic control register
LDR*	Load register with data
LFS	Load function and status register
LIB	Load input buffer register
LIS	Load interface status register
LIV	Load interrupt vector register
LOB	Load output buffer register
LSB	Load secondary block address register
LST	Load secondary transfer control register
LWT	Load the write register
RAS	Read attention summary register
RCS	Read control and status 1 register
RDA*	Read registers from 0 up to 7
RDR*	Read register
RDT	Read drive type register
RFS	Read function and status register
RIB	Read input buffer register
RIS	Read interface status register
RIV	Read interrupt vector register
ROB	Read output buffer register
RPB	Read primary block address register
RPT	Read primary transfer control register
RRD	Read the read register
RSB	Read secondary block address register
RST	Read secondary transfer control register
SDT	Test data transfer with word count (33–100)
SWI	Print current state of switch

*Address must also be provided.

CHAPTER 7
SERVICE

7.1 GENERAL

The DR01 interface contains the testing circuitry required for maintenance purposes. Buffer/test module M8432 includes the test circuitry and most of the drivers and receivers that connect to the user interface. Figure 7-1 is a block diagram of the M8432 module.

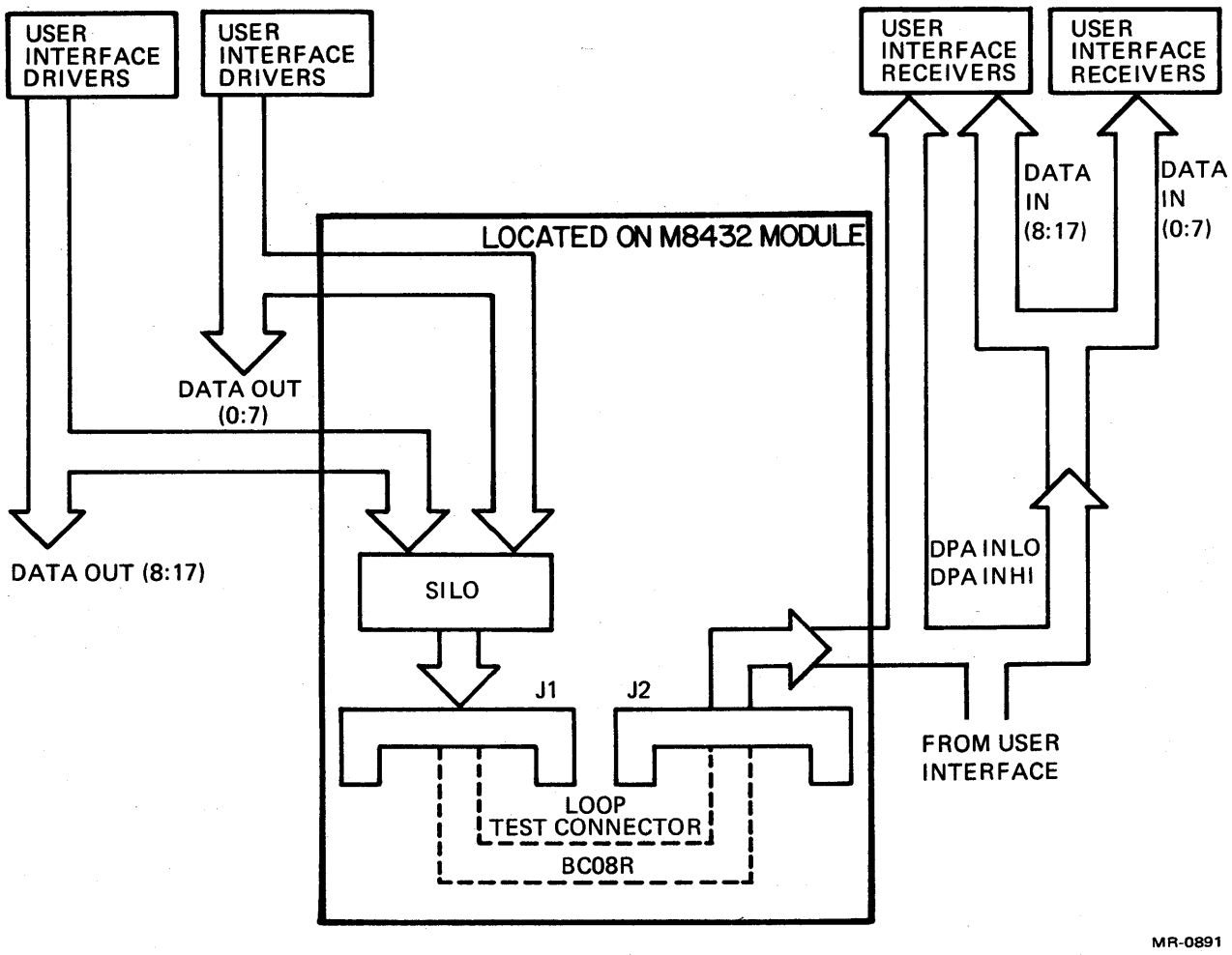


Figure 7-1 M8432 Buffer/Test Module Block Diagram

To use the DR01 in maintenance mode, the user interface cabling (M9760-YAs) must be removed. The BC08R test cable must then be installed between the two test connectors (J1 and J2) on the M8432. Refer to the maintenance cable signal drawing DTR01-0-3 which shows the signal interconnections in the maintenance mode.

7.2 CORRECTIVE MAINTENANCE

If a problem develops relating to the DR01, connect the BC08R cable as described above and run the DTR01 diagnostic, DFDRA.A10, as instructed in the diagnostic listing.

APPENDIX A
DTR01 INSTALLATION CONSIDERATION

A.1 POST INSTALLATION CONSIDERATIONS

If the interface connection of the customer/user does not include the extended user interface connector of the DTR01/DR01, the user might desire to disable certain floating input signals in slots E/F04 (extended user interface connector DR01-CL logic).

This can be accomplished by grounding the following pins on the M9760-YA cable connector module normally inserted in slots E/F04 of the DR01-CL logic.

Pin	Signal Disabled
EA1	USB DATA 16 IN
EF1	USB DATA 17 IN
EH1	USB AT01
EJ1	USB AT02
EK1	USB AT03
ED2	USB DS06
EE2	USB AT00
EN2	USB AT00
EN2	USB DS03
EP2	USB DS04
ER2	USB DS05
ET2	USB DS07

APPENDIX B
LINKING PROCEDURE

B.1 DR01/DR11-B LINKING PROCEDURE

The following procedure should be consulted to configure a link interconnection between a DR01-CL and a DR11-B interface.

1. Refer to the DR01/DR11-B link logic connection drawing, C-IC-DTR01-0-6.

2. Install a BC11A or equivalent type cable between slots C/D04 of the DR11-B interface and slots C/D01 of the DR01-CL logic to be linked. The cable length must not exceed 9 m (30 ft) in length.

3. Use a pair of the following connector boards: M908, M959, M930, M970, M974. Insert the pair into slots E/F01 of the DR01-CL logic of the supplied M9760-YA cable connector board and ground the following pins on the board to disable floating input signals in slot E/F01 (extended link connector slot).

Pin	Signal Disabled
EB1	USB DATA 16 IN
FH1	USB DATA 17 IN
FH2	ERROR H
FJ2	USB AT01
FK2	USA DS01
FL2	USA DS02
FN2	USA DS00
FP2	USB DS03
FR2	USB DS05
FS2	USB DS04

4. Set DR01-CL DI SWITCH SW1 as desired.

   a. Set SW1-1, SW1-2, and SW1-3 to the desired drive address.
   b. Select word mode (SW1-7 = OFF).
   c. Set no input parity check (SW1-8 = OFF).

5. Refer to the following drawings for further information on the DR01/DR11-B linkage.

   D-BD-DTR01-0-8
   DR01-C/DR11-B Register Link Configuration

   D-IC-DTR01-0-10
   DR01/DR11-B Link Signal Translation

   A-SP-DTR01-0-12
   DR01/DR11-B Linking Procedures

B.2 DR01/DR01 LINKING PROCEDURE

The following procedure should be consulted to configure a link interconnection between a DR01-CL and another DR01-CL interface.

1. Refer to the DR01 link connection drawing, C-IC-DTR01-0-7, for cable installation.

2. Install two BC11A or equivalent type cables between slots C/D04 and E/F04 of one DR01-CL interface and slots C/D01 and E/F01 of the other DR01-CL logic to be linked. The cable length must not exceed 9 m (30 ft) in length.

3. Set DR01-CL DIP SWITCH SW1 as desired

   a. Set SW1-1, SW1-2, and 1-3 to desired drive address
   b. Word mode should be selected (SW1-7 = OFF)
   c. Set no input parity check (SW1-8 = OFF).

4. Refer to the following drawings for further information on the DR01/DR01 linkage.

   D-BD-DTR01-0-9
   DR01-C/RH20 Register Link Configuration

   D-IC-DTR01-0-2
   DR01 Link Signal Translation

   A-SP-DTR01-0-13
   DR01/DR01 Linking Procedure

APPENDIX C
USER INTERFACE SPECIFICATION

C.1 USER INPUT/OUTPUT SIGNALS

This section describes the signals made available to the user device to control the operation of the interface. Paragraph C.1.1 describes the user input/output signals. Paragraph C.1.2 details the timing considerations and restrictions on the use of the signals.

C.1.1 Signals List

Tables C-1 and C-2 list the signals available to the user device. Input loading refers to the number of TTL unit loads the input signal must drive. A unit load is defined as:

2.4 V < Input high voltage < 5.0 V @ 40 μA plus terminator load

0.0 V < Input low voltage < 0.4 V @ 1.6 mA plus terminator load

where current flow is defined positive into the driven gate.

All output signals are driven with 7437 drivers. These drivers can sink 60 mA in the output low state and can source 1.5 mA in the output high state. This is equivalent to a fan-out of approximately 30 unit loads.

All input signals are received by 7414 Schmitt trigger receivers for noise immunity. The signal inputs are terminated at the receiver input with a 180 ohm resistor to +5 V and a 390 ohm resistor to ground. All signal inputs represent one unit load.

C.1.2 Timing Considerations

The negation of READY, as well as a nominal 1 μs pulse on the GO signal, indicates to the user device that a valid data transfer command has been received by the interface. The READ and WRITE signals will indicate which direction of transfer has been requested by the processor.

C.1.2.1 Read Operation – If the operation is to be a read, the user device must provide the DATA IN (0:15) signals plus optional parity bit (DPA IN LO and DPA IN HI).

NOTE

If parity is not used, the Input Parity Inhibit (IPI) signal must be asserted by the user device to prevent an undesired parity error indication. The use of the two additional data bits DATA IN 16 and 17 is not required on the PDP-11 and is intended for interfacing to larger machines such as the DECsystem 10.

In Figure C-1, the data lines must be stable 100 ns prior to the high-to-low transition of either CYCLE REQUEST A or B. The negation of either of these two signals will set the CYCLE flip-flop and will cause the interface to begin a data transfer cycle provided the following conditions are met.

1. The interface has completed the previous cycle (indicated by negation of the BUSY signal).
2. The interface is in the RUN mode (indicated by negation of READY).

Table C-1 User Input Signals

Name	No. of Signals	Description*
DAT17 IN– DAT00 IN	18	Data input from user device. **NOTE** **Bits 17 and 16 may be tied to ground if only 16-bit data transfers are desired.**
CYCLE REQUEST A,B	2	The logical OR of these two signals is used to set the CYCLE flip-flop in the interface. CYCLE initiates the sequence of performing a data transfer operation provided that the interface has been given a data transfer command. Either of these two inputs should be pulsed positve for 100 ns minimum duration to initiate a bus transfer sequence. CYCLE sets on the +3 V to ground transition of the input.
ST00–ST07	8	Device Status Bits 0:7. The signal levels applied to these lines appear as bits 00:07 of RHFS. Levels are: +3 V = logical 1; ground = logical 0.
ERROR	1	User-defined error bit. The level applied to this line appears as bit 10 in the interface status register (RHIS). Setting this bit will cause ATA and ERR to set and will cause an interrupt in the processor if the interrupt enable is set.
AT0–AT3	3	User-defined signals that can be used to cause an interrupt in the processor without indicating an error condition.
DPA IN LO DPA IN HI	1	Data Parity In – Implemented by the user to provide parity with incoming data to the interface. Parity checking on the input data is performed in the interface if IPI (Input Parity Inhibit) is not set (odd parity).
IPINH	1	Input Parity Inhibit – Asserted by the user to inhibit parity checking on data which it transfers into the interface.

*Maximum loading for each user input signal = 1 each

Table C-2 User Output Signals

Name	No. of Signals	Description
DAT17 OUT–DAT00 OUT	18	Data output to user device. These signals represent the contents of the interface output buffer which is loaded when the interface performs a write cycle. Levels are: +3 V = logical 1; ground = logical 0. All lines cleared to 0 by INIT.
INIT	1	This line is true (+3 V) whenever the Massbus is initialized which occurs on power up, power down, console start, REST instruction, or when an interface clear command is received by the interface.
F00–F07	8	These 8 lines are derived from the function bits in RHFS (bits 8–15) and are user-defined to specify device operation. Levels are: +3 V = logical 1; ground = logical 0. Clear by INIT.
READY	1	This signal is derived from the Interface Ready (IRY) bit in RHIS (bit 7). This signal is true (+3 V) after INIT; it becomes false (ground) when the GO bit is loaded with a data transfer command and it becomes true again when word count overflows or an error condition develops.
BUSY	1	BUSY indicates that data transfer sequence is in progress. BUSY is true (+3 V) when CYCLE is set and becomes false (ground) when the data transfer cycle is complete.
END CYCLE	1	This pulse is a 100 ns positive pulse that indicates the bus cycle is complete.
USER GO	1	This signal is a 1 μs positive pulse that results from setting the GO bit in RHCS1 with a data transfer command. Indicates that a new operation is to be performed.
READ	1	Indicates that a read command has been given to the interface by the controller; that is, the processor is requesting data to be input to the interface.
WRITE	1	Indicates that a write command has been given to the interface by the controller; that is, the processor is requesting to output data to the interface. Normally, the negation of the READ signal may also be used to indicate a write command.
DPA OUT LO DPA OUT HI	1	DATA PARITY OUT indicates the parity of the data in the output data buffer (odd parity). DPA OUT LO is for the low byte and DPA OUT HI is for the high byte.

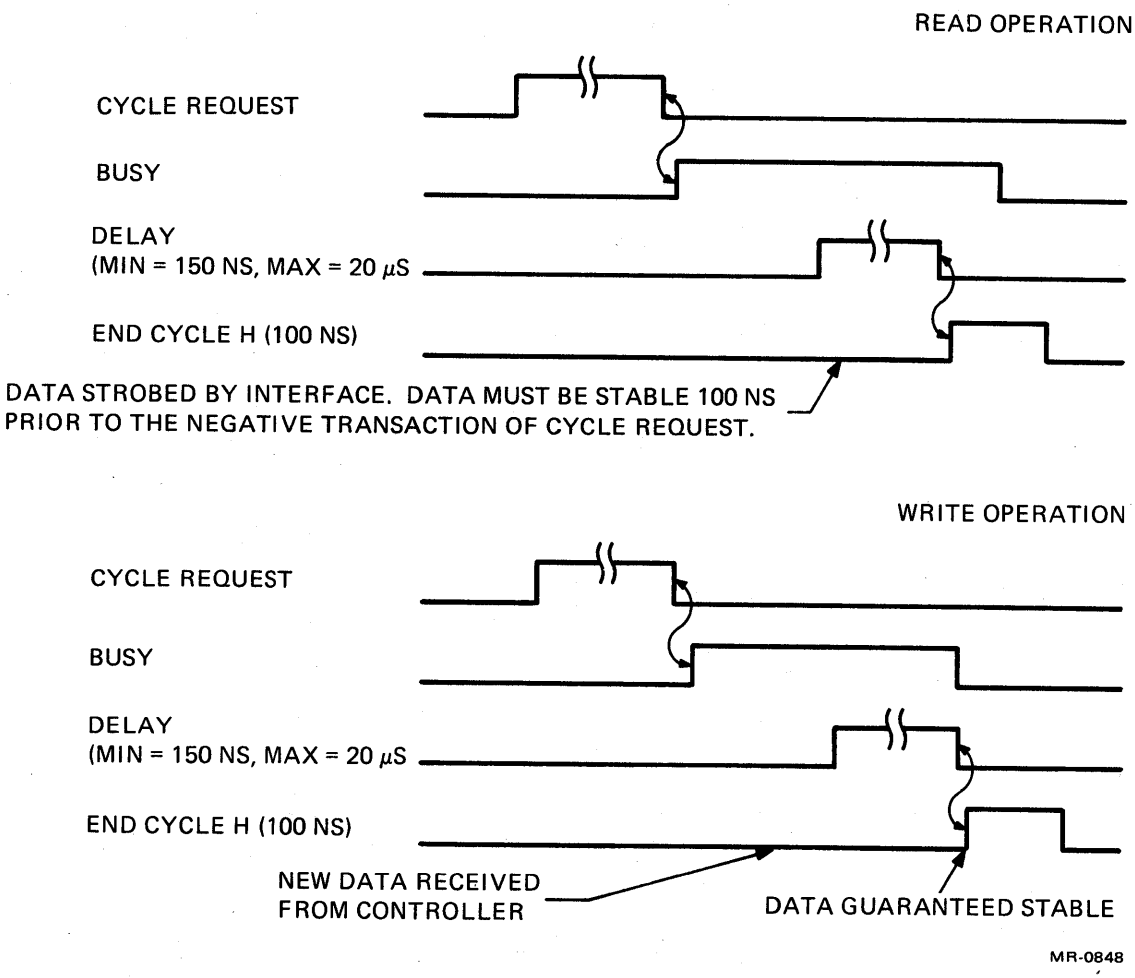


Figure C-1 Read and Write Timing Diagrams

If the CYCLE request is received before the completion of the previous cycle, the request will be stored and the new data transfer cycle will begin as soon as the previous cycle is finished. This allows the user device to overlap cycles so that the interface will be primed to begin a second cycle immediately upon completion of the first cycle. If a CYCLE REQUEST is received before a valid data transfer command, it will also be stored and acted on as soon as the command has been received from the processor.

The beginning of a new data cycle is indicated by the low-to-high transition of the BUSY signal. If both conditions 1 and 2 above are true, the cycle will begin immediately following the negative transition of CYCLE REQUEST. The user device must hold the data lines stable until the cycle begins (positive transition of BUSY signal). At this point, the interface has strobed in the data lines and there is no further need for the user device to hold the lines stable while the interface completes the transfer.

The completion of the data transfer will be indicated by the negative transition of the BUSY signal and the assertion of the END CYCLE signal. The BUSY signal will be cleared as soon as the END CYCLE signal is asserted.

C.1.2.2 Write Operation – When a write command has been received from the processor, the negation of either of the CYCLE request signals will have basically the same effect as in a read but the direction of the transfer will be opposite. (See Figure C-1.)

As in a read operation, if the CYCLE REQUEST is received before it can be processed by the interface, it will be stored as soon as a new data transfer cycle can be started.

The beginning of the data transfer cycle is indicated by the low-to-high transition of the BUSY signal. The data from the previous transfer cycle will remain valid on the DATA OUT (0:15) lines until the new data is received from the Massbus controller (approximately in the middle of the data cycle). The new data will be presented to the user device on the DATA OUT lines along with an optional parity bit as soon as the data transfer cycle is complete (assertion of END CYCLE and clearing BUSY). The data lines will be stable as soon as BUSY clears. The user device may then delay initiating another cycle until it has processed the data or it may immediately initiate another cycle if the data is strobed well within the next 250 ns. Figure C-1 shows the timing diagram of the read and write operations.

NOTE

BUSY will set immediately following the negative transition of CYCLE REQUEST only if the interface has completed the previous data transfer operation and the READY signal is reset.

DTR01/DR01 CHANNEL INTERFACE
SUBSYSTEM TECHNICAL MANUAL
EK-DTR01-TM-001

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