DEC-8L-D0BA-D

KP8/L

POWER FAILURE OPTION FUNCTIONAL DESCRIPTION

DIGITAL EQUIPMENT CORPORATION □ MAYNARD, MASSACHUSETTS

1st Printing April 1969

KP8/L
POWER FAILURE

FUNCTIONAL DESCRIPTION

INTRODUCTION

The KP8/L Power Failure Option causes an interrupt signal to the PDP-8/L computer, allowing computer operation for a fixed-time after a primary power interruption. With proper programming, an interrupt from the KP8/L insures data storage of the several machine registers of interest (accumulator, link, program counter, etc.) in core memory. When the option is enabled, restoration of power restarts the computer at memory location 0000_8, after a suitable delay, to allow for voltage stabilization. A program subroutine, entered when power returns, places the previously stored data back in their proper registers. The option can be disabled to prevent restart.

The KP8/L Option consists of an M703 Integrated-Circuit module partially controlled by the PDP-8/L G826 Regulator and Power Detector module. Both modules are contained within the processor logic frame.

LOGIC DESCRIPTION

The following paragraphs describe the sequence of events that occurs when power is interrupted. The basic power-fail programming technique is also described.

When primary power is removed, detection circuits in the G785 module and G826 module (Regulator and Power Detector, Drawing D-BS-PDP8-L-13) react to a decrease in the +5V dc voltage, and generate a low logic level, $\overline{\text{SHUTDOWN}}$. This signal sets the KP8/L PWR LOW flag flip-flop (Drawing D-BS-KP8L-0-1). PWR Low (0) generates INT RQST (Drawing D-BS-PDP8-L-10). A program interrupt occurs if the processor interrupt facility is enabled. The interrupt is effected in the usual manner with a search subroutine using the octal instruction 6102 (SPL, Skip on Power Low) to enable the $\overline{\text{PWR SKIP}}$ gate signal to locate the interrupting source. The PWR SKIP gate is enabled by PWR LOW (1), the power-fail device selection code (10_8, from MB03 through MB08), and the interrogation timing signal IOP2(1). $\overline{\text{PWR SKIP}}$ generates I/O SKIP (Drawing D-BS-PDP8-L-10) which allows entry into the power fail service subroutine (Figure 1). The service subroutine stores the contents of the AC, Link, and PC in core memory. Also, any critical information that might be lost in a power failure is transferred first to the AC, and then into core memory during this subroutine. When a program interrupt occurs, and the interrupt facility is enabled, the contents of the PC are automatically stored in location 0000_8. Because location 0000_8 is used later with the restart program, this content (PC word) is then relocated in memory. Finally, a JMP instruction to address X is stored in location 0000_8, and the HLT instruction is executed. Address X is the starting location of the restart program. The HLT instruction must be included in the power fail service routine following the instructions that store the contents of the registers after all register storage has occurred.

Adequate time for search and execution of the above subroutine is provided by the 1-ms single-shot delay activated by the $\overline{\text{SHUT DOWN}}$ signal. The activated low output, STOP OK, inhibits the Regulator Control of the G826 module from initiating the normal machine down cycle. After the 1-ms delay, the STOP OK signal goes high; the

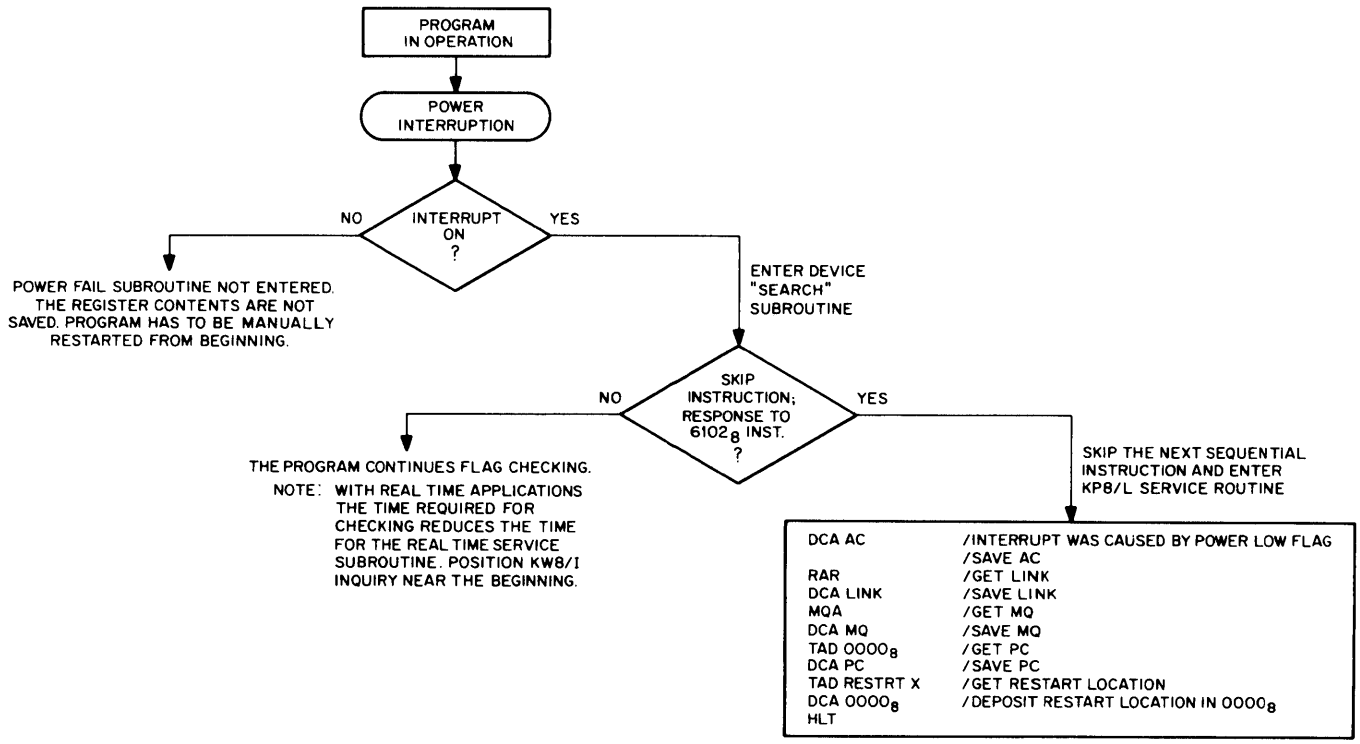


Figure 1 Power Fail Service Subroutine

Regulator Control disables the memory voltage; and STOP OK and POWER OK combine to insure that the RUN flip-flop is cleared (reset) at the next processor time pulse TP3 (Drawing D-BS-PDP8-L-2).

Restoration of primary power initializing signals throughout the PDP-8/L to clear the major timing and machine-state flip-flops, including PWR LOW. Before the computer can start, a restart signal must be generated. The integrating 300 ms single shot delay (drawing D-BS-KP8L-0-1) is enabled when normal voltages are restored (both SHUT DOWN, and STOP OK are high logic levels). If no additional power interruptions occur, the single-shot will time out and try to generate the restart signal after the 300-ms delay. The microswitch on the M703 module handle can be set to DISABLE to inhibit this pulse, or to ENABLE to allow it. When a 1-ms RESTART pulse is generated, it acts as a KEY ST signal in activating the manual function timing generator, by producing the same signals: KEY ST and KEY ST + EX + DP (Drawing D-BS-PDP8-L-2). A 0000_8 starting address is forced by $\overline{\text{RESTART}}$, inhibiting the transfer from the PC register to the MA register during MFTS1(1) (Drawing D-BS-PDP8-L-4). Program events are shown in Figure 2.

NOTE

A JMP or JMS instruction must be in location 0000_8 because it cannot be predicted what the PC register will contain when a power failure occurs since the PC register contents are not known.

ENGINEERING DRAWINGS

The following drawings D-BS-KP8L-0-1 and D-CS-M703-0-1 pertaining to the KP8/L Option are contained in this section.

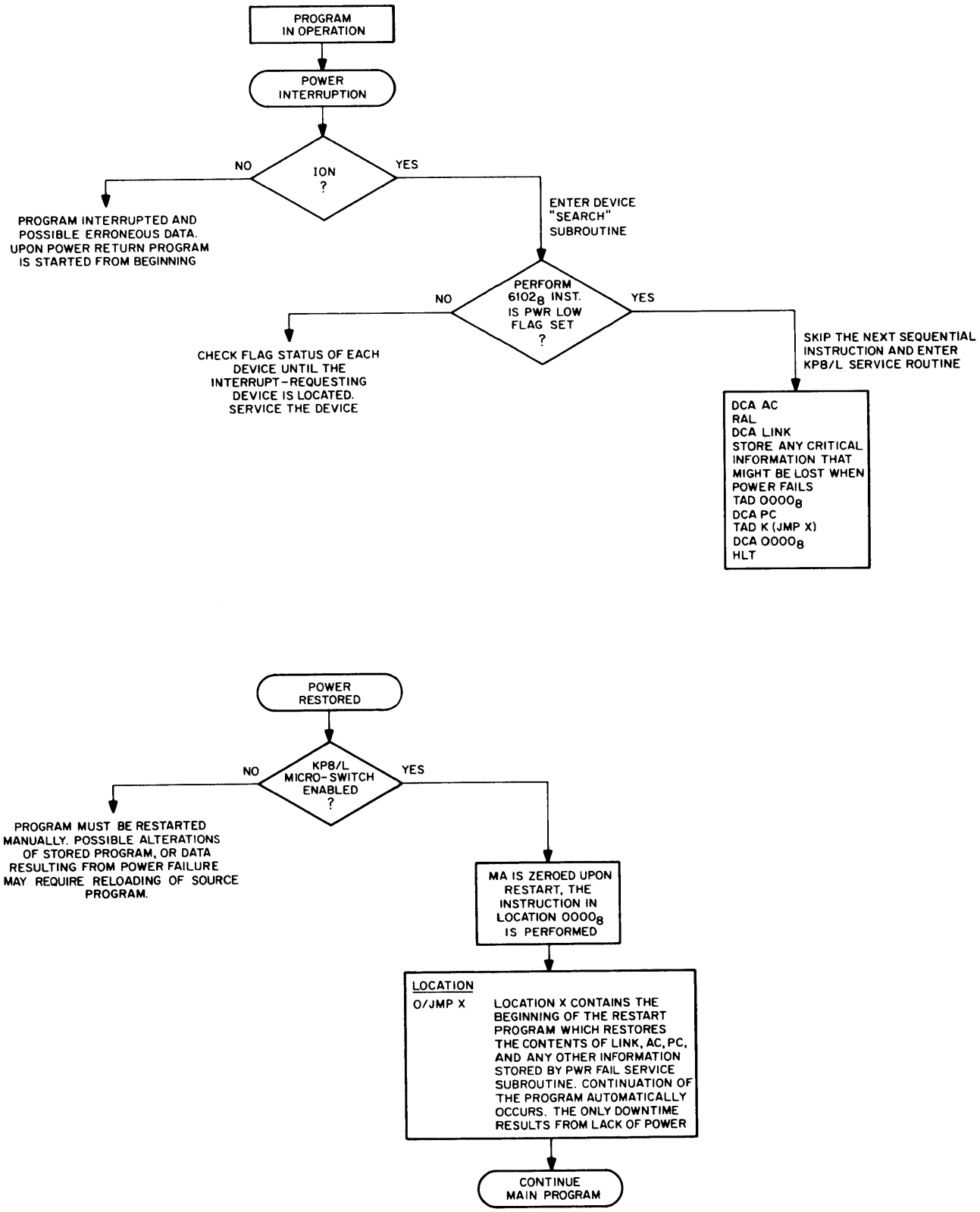
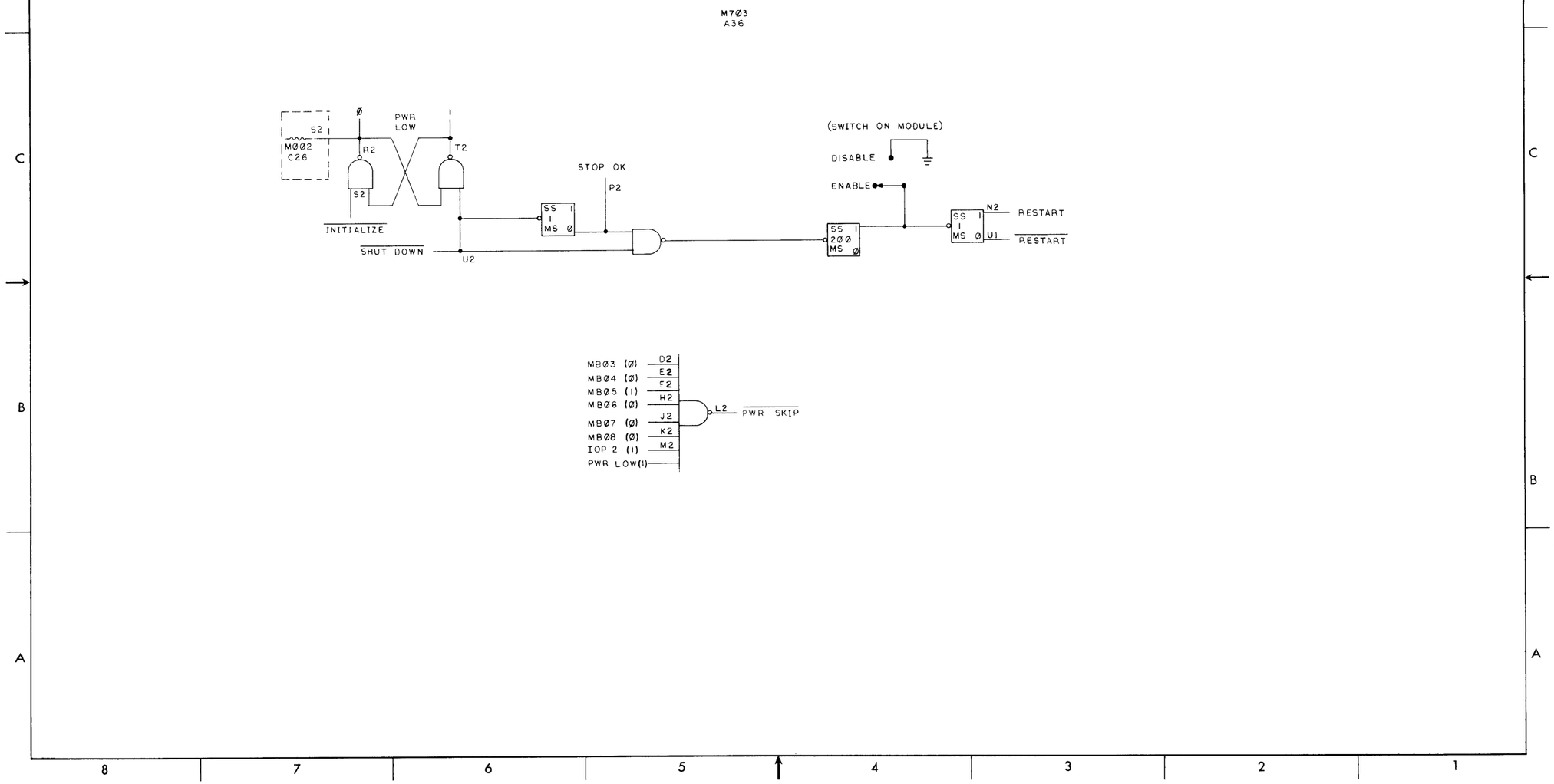


Figure 2 Power Restoration Program Events


M703
A36
S2
M002
C26
Ø
PWR
LOW
1
R2
T2
S2
INITIALIZE
SHUT DOWN
U2
SS I
I
MS Ø
STOP OK
P2
(SWITCH ON MODULE)
DISABLE
ENABLE
SS I
200
MS Ø
SS I
I
MS Ø
N2
U1
RESTART
RESTART
MBØ3 (Ø)
MBØ4 (Ø)
MBØ5 (1)
MBØ6 (Ø)
MBØ7 (Ø)
MBØ8 (Ø)
IOP 2 (1)
PWR LOW(1)
D2
E2
F2
H2
J2
K2
M2
L2
PWR SKIP