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PDP-8/A MINIPROCESSOR USERS MANUAL

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CHAPTER 1
INTRODUCTION AND DESCRIPTION

This manual provides the user with the necessary information to operate, interface to, maintain, and troubleshoot the PDP-8/A Miniprocessor manufactured by Digital Equipment Corporation, Maynard, Massachusetts.

The PDP-8/A is the newest model of the PDP-8 family consisting of the PDP-8/E, PDP-8/F, PDP-8/M and PDP-8/A. The following illustrates how the PDP-8/A relates to its family members.

KIT-8/A	PDP-8/A	PDP-8/M	PDP-8/E
Modules	Small to Medium Configurations	Medium to Large Configurations	Large Configurations

KIT-8/A is a module set version of the PDP-8/A configured to solve application problems that do not require a complete computer package with power, front panel, chassis, and cooling. Kits consist of processor, memory, option boards, and mounting hardware including:

Central Processor Unit, Hex Module (M8315)

Read/Write Random Access Memory (RAM), Quad Module (M8311)

Read Only Memory (ROM), Quad Module (M8312)

Reprogrammable Read Only Memory (PROM), Quad Module (M8349)

DKC8-AA I/O Option Board with Serial I/O, Parallel I/O, Real-Time Crystal Clock, and Programmer's Panel Control, Hex Module (M8316)

KM8-AA Extended Option Board with Memory Extension, Timeshare Control, Power Fail/Auto-Restart, and Bootstrap Loader, Hex Module (M8317)

MM8-AA(8K) and MM8-AB(16K) Core Memory Modules

PDP-8/A – There are two basic types of computers in the PDP-8/A family. The first type is the PDP-8/A, which uses semiconductor memories (MS8 and MR8). The second type is represented by a series of computers, each of which uses 8K or 16K core memory (MM8); this series consists of the 8A400, 8A420, 8A600, 8A620, 8A800, and 8A820 computers. When a reference applies to both types of computers, the designation "PDP-8/A" is used. "PDP-8/A Semiconductor" refers to the semiconductor-memory computer, while "8A400," for example, refers to a specific core-memory machine and "8A" refers to the core-memory machines in general.

PDP-8/A Semiconductor (Semiconductor Memory); designed to provide the security and data integrity of hard wired, solid state logic and relay controllers, and in addition, provide the flexibility, power, and low cost of a computer. Space is available to install 10 modules.

Semiconductor memory:

RAM 1K, 2K, 4K (M8311)
ROM 1K, 2K, 4K (M8312) On Quad Modules
PROM 1K with 256 word RAM (M8349)

Battery backup:

System 1 to 7 minutes with provision for additional external batteries

8A (Core Memory); provides the lowest cost computers in the 8K to 32K memory range for small computer systems and mainframes. The PDP-8/A Central Processor Unit and two new core memories are used. Space is available for 12 or 20 modules.

Core memory:

8K (MM8-AA) and 16K (MM8-AB) Hex Modules (two slot spaces are required for each module).

Most of the options available for other members of the PDP-8 family are compatible with the PDP-8/A (see Paragraph 2.4 for a list of those that are not compatible). However, the DKC8-AA I/O Option module, the KM8-AA Extended Option module, and several memory modules have been designed exclusively for the PDP-8/A.

Companion Documents include:

1. *Introduction to Programming* – 1973
2. *OS/8 Handbook*
3. *PDP-8/A Miniprocessor Handbook* – 1975-1976
4. *PDP-8/A Operators Handbook*(DEC-8A-HOPHB-A-D)
5. *PDP-8/A Engineering Drawings*
6. *PDP-8/E Maintenance Manual* Volume II (DEC-8E-HMM2A-D-D) and III (DEC-8E-HMM3A-C-D).

All of these documents are available from Communications Services, Digital Equipment Corporation, Maynard, Massachusetts, 01754.

Table 1-1 lists the functional characteristics of the PDP-8/A.

Table 1-1
PDP-8/A Functional Characteristics

Type	Single address, fixed word length, parallel transfer programmed data processor.
Word Length	12 bits.
Cycle Time	1.5 μs minimum (See memory speeds).

Memory Type	Cycle Time (μs)	
	Fetch Major State	All Other States
ROM Only	1.5	1.5
ROM/RAM (ROM Cycle)	1.6	1.6
ROM/RAM (RAM Cycle)	2.7	3.1
RAM Only	2.4	2.8
Core Memory	1.5	1.5

Memory Types	RAM	1K, 2K, 4K
	ROM	1K, 2K, 4K
	PROM	1K
	Core	8K, 16K
Memory Expansion	Up to 32K.	
Hardware Registers	5(AC, MQ, MB, PC, CPMA).	
Auto Index	8 Auto Index registers per 4K memory field.	
Addressing Capability	One instruction may address 256 locations directly or 4096 locations indirectly.	
Instruction Set	6 memory reference instructions, 20 microprogrammable operate microinstructions, and 8 input/output transfer instructions for the CPU and each of up to 60 I/O devices.	
Instruction Execution Time	Operate microinstruction	1.5 μs*
	Directly addressed MRI	3.0 μs*
	Indirectly addressed MRI	4.5 μs*
Input/Output Capability	Programmed data transfer, program interrupt system transfer, and 12 channels of internal and/or external direct memory access (data break).	
Auto Start Feature	The CPU contains an auto-start which can start the CPU at one of six switch selectable addresses upon application of power.	

*Cycle times reflect 1.5 μs memory.

Table 1-1 (Cont)
PDP-8/A Functional Characteristics

Options	Two new option boards which may be used separately or together. 1. Front Panel Control Serial Line Unit Parallel I/O Real Time Clock 2. Power Fail/Auto Restart Memory Extension Timeshare Control Bootstrap Loader
Size (W X H X D)	19 X 10.5 X 10.5 in. (48 X 27 X 27 cm) – PDP-8/A Semiconductor, 8A400, 8A600, 8A800. 19 X 10.44 X 23 in. (48 X 26.52 X 58.42 cm) – 8A420, 8A620, 8A820.
Weight	55 lb (25 kg) – PDP-8/A Semiconductor, 8A400, 8A600, 8A800. 117 lb (53 kg) – 8A420, 8A620, 8A820.
Operating Environment	Ambient temperature 41° to 122° F (5° to 50° C) Relative humidity 10% to 95% maximum, Wet bulb 90° F (32° C)
Power Requirement	Approximately 150 W at 115 Vac, 50 or 60 Hz or 230 Vac, 50 or 60 Hz (voltage and frequency specified at time of order).

1.1 SYSTEM DESCRIPTION

The PDP-8/A is a general purpose miniprocessor. Its processor structure is single-address, fixed word length, parallel transfer, using 12-bit, two's complement arithrnetic. The cycle time of the processor is 1.5 μs. Standard features include one level of indirect addressing and facilities for instruction skipping, program interrupts as a function of input/output device conditions, and auto-restart features.

Five 12-bit registers are used to control computer operations, address memory, perform arithmetic or logical operations, and store data. An optional Programmer's Console provides switches and indicators that permit convenient monitoring and modification of machine operation.

The flexible, high capacity input/output capabilities of the PDP-8/A allow it to operate a great variety of peripheral devices. More than 60 input/output device options including high-speed paper-tape equipment, card readers, line printers, disk and magnetic tape bulk storage devices, and a wide range of data acquisition, transmission, and display peripherals are available from DIGITAL for the PDP-8/A.

Each PDP-8/A system is completely self-contained. A single source of 115 or 230 Vac power is required; internal power supplies produce all the necessary operating voltages for the system. The basic PDP-8/A computer consists of a rack-mountable chassis with a power supply and an Omnibus (backplane) into which are inserted the central processor, the memory system, and the optional Programmer's Console and console terminal control. In the PDP-8/A, a bus is defined as a group of signal lines carrying related information, such as the 12 bits of an instruction or data word. The Omnibus may be considered a wide bus containing several buses along with many other signal lines. Each PDP-8/A Omnibus has a slot for the central processor unit, two slots reserved for the two option boards, plus several identical nondedicated module slots. Each slot will accept a 144-pin quad or hex-sized module. (Some slots will accept a 180-pin hex module.) The Omnibus provides two-way signal paths between corresponding pins of the modules that are plugged into it.

A PDP-8/A computer pictured in Figure 1-1 shows both the Limited Function Panel (the panel on the bottom with three switches and three indicators) and the Programmer's Console. The Programmer's Console can be located remotely from the chassis; in such a case, or when the system does not include a console, a blank panel is attached.

PDP-8/A computers have three different mechanical assemblies that can be characterized by the number of available Omnibus slots; that is, the PDP-8/A semiconductor computer assembly has a 10-slot Omnibus, while the 8A computer assemblies have either a 12-slot or a 20-slot Omnibus. Table 1-2 relates the various PDP-8/A computers to some of the basic system components. Note that the 8A400 can be considered the basic 8A computer, having a core memory, an 8A CPU, and a 12-slot Omnibus. Thus, the 8A420 differs only in that it has a 20-slot Omnibus; the 8A600 differs in that it has a PDP-8/E CPU; the 8A620 differs in that it has a PDP-8/E CPU and a 20-slot Omnibus; the 8A800 differs in that it has an FPP-8/A (not indicated in Table 1-2); and, the 8A820 differs in that it has an FPP-8/A and a 20-slot Omnibus. Also, note that only 8A computers that use a PDP-8/E CPU can be expanded.

Table 1-2
PDP-8/A Computer Assemblies

Computer	CPU	Memory*	Basic Power Assembly	Omnibus	Expandable
PDP-8/A	KK8-A	Semiconductor	H763	H9192 (10-Slot)	No
8A400	KK8-A	Core	H9300	H9194 (12-Slot)	No
8A420	KK8-A	Core	BA8-C	H9195 (20-Slot)	No
8A600	KK8-E	Core	H9300	H9194 (12-Slot)	Yes. As many as 20 slots can be added.
8A620	KK8-E	Core	BA8-C	H9195 (20-Slot)	Yes. As many as 20 slots can be added.
8A800	KK8-A	Core	H9300	H9194 (12-Slot)	No
8A820	KK8-A	Core	BA8-C	H9195 (20-Slot)	No

*A KM8-A (or KM8-E) Extended Memory Option module must be included in all the 8A computers, since their basic memory capacity is 8K or 16K; the KM8 is optional with the PDP-8/A Semiconductor computer, since the basic memory can be less than, greater than, or equal to 4K.

Figure 1-2 represents, pictorially, the PDP-8/A Omnibus and the relationship of the fundamental system components (i.e., CPU, memory, power supply, option, and peripheral interfaces). These components are described briefly in the following paragraphs.

Figure 1-1 PDP-8/A Miniprocessor

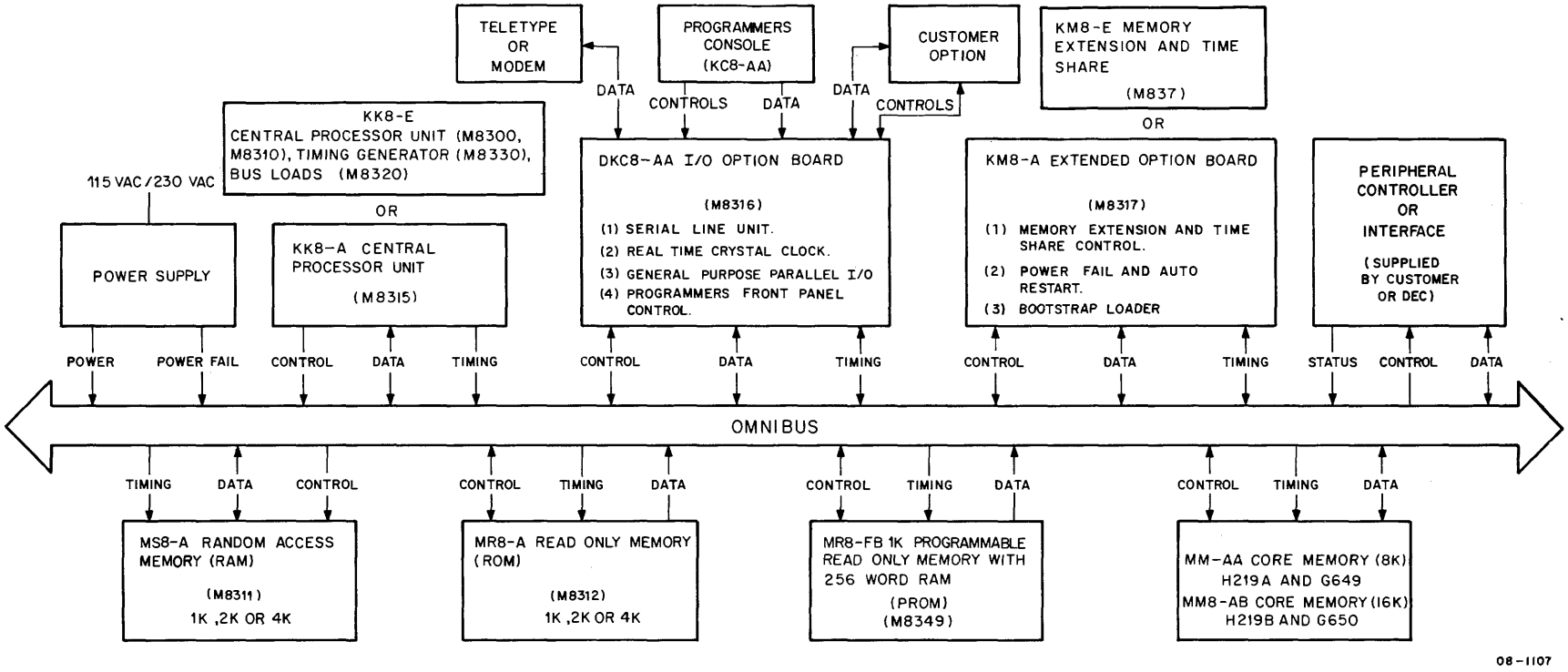

Figure 1-2 PDP-8/A System Block Diagram

1.1.1 Central Processor Unit (CPU)

The KK8-A is contained on one hex module and has all the circuitry needed to manipulate data and generate control signals; this circuitry includes the major registers and gating, the instruction decoder, the timing generator, and the auto-start logic. The KK8-E is comprised of 4 hex modules. Two of these, M8300 and M8310, constitute the CPU; another is the Timing Generator (M8330), and the last is the Bus Loads (M8320).

1.1.2 KC8-AA Programmer's Console

The DKC8-AA I/O Option board contains the circuitry required to connect the PDP-8/A Programmer's Console to the Omnibus. This console consists of an array of controls and indicators that facilitate computer operation and maintenance. Key pad switches provide convenient control of the system by allowing the operator to start and stop program execution, examine and modify the contents of memory, select various modes of operation, and load and execute short machine language programs.

1.1.3 Limited Function Panel

The Limited Function Panel (Figure 1-3), which is often used without the Programmer's Console in dedicated applications, provides the necessary controls to apply power to the computer and start a program. A PANEL LOCK switch, which is significant only when a Programmer's Console is present, allows the operator to disable most of the console switches. This feature protects an operating program from being disturbed by accidental closure of a switch.

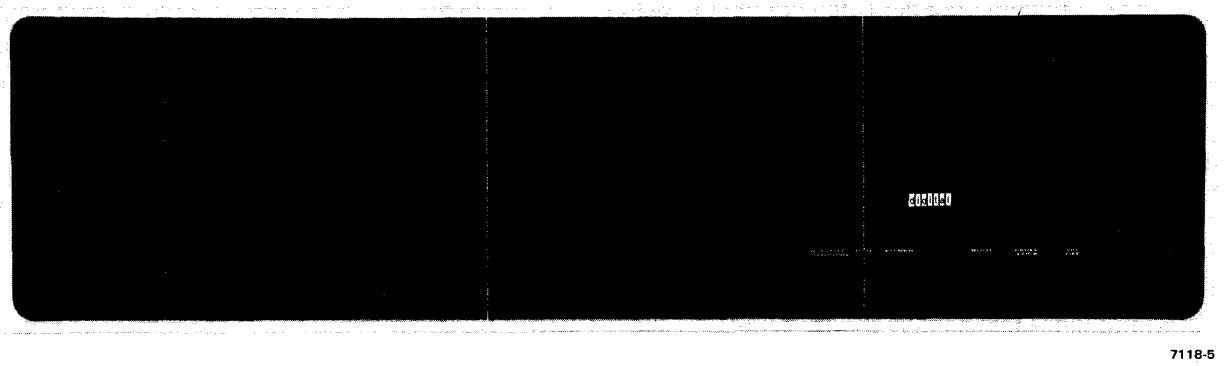

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Figure 1-3 PDP-8/A Limited Function Panel

1.1.4 Memory

The PDP-8/A memory can be configured from ROM, RAM, PROM, or core memory to meet the user's particular requirements. Memory sizes below 4K, (such as 1K RAM, 1K ROM, and 1K PROM) are allowed, and the memory system can be expanded to 32K provided there is adequate current available from the power supply. Each of the various memory options available is discussed in the following paragraphs.

1.1.5 MM8-A Core Memory

The MM8-A is a 12-bit word, random access core memory system for the 8A computer. There are two versions available, the MM8-AA (8192 12-bit words) and MM8-AB (16,384 12-bit words). Memory cycle time is 1.5 μs. A one inch thick hex module board contains the core stack, drive circuits, sense circuits, address decoders, etc. These circuits perform all the operations required to transfer data into or out of core memory. The system plugs into one Omnibus slot but occupies two spaces on the Omnibus because of the thickness of the module.

1.1.6 MS8-A Read/Write Semiconductor Memory (RAM)

The read/write semiconductor memory is a random access memory (RAM) mounted on a single quad board with a capacity of 1K, 2K, or 4K 12-bit words. Memory cycle time is 2.4 μs for instruction fetches and 2.8 μs for all other states.

1.1.7 MR8-A Read Memory (ROM)

The MR8-A is a semiconductor read only memory mounted on a single quad board with a capacity of 1K, 2K, or 4K 12-bit words. Memory cycle time with ROM memory only is 1.5 μs.

For those systems containing both ROM and RAM, a 13th bit in each memory location containing ROM and RAM may be set to a logical 1 when the ROM is programmed to allow the program to address a word in read/write memory. When the 13th bit is on, the content of that memory location is interpreted as a memory address instead of an operand and used to address the desired RAM memory location. This allows the programmer to use instructions that require read/write operations (i.e., JMS, DCA, ISZ Instructions) when writing the ROM program.

1.1.8 MR8-FB Reprogrammable Read Only Memory (PROM)

The MR8-FB is an ultraviolet-erasable semiconductor memory mounted on a single quad board with a capacity of 1024 12-bit words of PROM and 256 words of read/write memory. PROM memory also has a 13th bit which can be set to one, to address one of the 256 RAM locations. When the 13th bit is one, the eight least significant bits read from a PROM location are used as an address to select one of the RAM locations. This allows the programmer to use instructions that require read/write operations.

1.1.9 G8016 Power Supply Regulator Module

The G8016 Power Supply module provides +5 Vdc and −15 Vdc and +15 Vdc for the semiconductor versions of the PDP-8/A Miniprocessor. The supply consists of a quad size board containing all the power generation and regulation circuitry necessary to provide these voltages. The power available is:

+5 Vdc	20 A	
+15 Vdc	0.75 A max	} sum < 1 A
−15 Vdc	0.75 A max	}

1.1.10 G8018 Power Supply Regulator Module

The G8018 module supplies power for core memory systems for the 8A. It differs from the semiconductor power supply module in that more power is available:

−5 V	2 A
+5 V	25 A
+15 V	2 A
−15 V	2 A
+20 V	4 A

NOTE

The G8016 and G8018 Power Supply modules are not interchangeable. The semiconductor supply (G8016) will operate only with the PDP-8/A Semiconductor computer; the core memory supply (G8018) will operate only with the 8A computers.

1.1.11 Interfacing

The PDP-8/A Omnibus is an internal input/output bus designed to eliminate random wiring and provide convenient access to data and control signals. Interfacing is accomplished by inserting modules into non-dedicated slots.

The KA8-E positive I/O bus interface provides an extension to the bus system that facilitates interfacing PDP-8 family positive bus equipment with the PDP-8/A. The positive I/O bus was designed for use with PDP-8/I and PDP-8/L compatible peripherals, but it may be employed with almost any positive bus equipment.

PDP-8/A systems provide three types of data transfer: programmed data transfers, program interrupt transfers, and direct memory access transfers. Programmed data transfer is the easiest to implement and is the most direct method of handling data I/O. Program interrupt transfers provide an extension of programmed I/O capabilities by allowing I/O operations involving two or more devices to be performed concurrently. The data break system uses direct memory access for applications involving extremely fast data transfer rates. All three I/O techniques are described in Chapter 9 of the *Miniprocessor Handbook*. A detailed description of the Omnibus and its signals is contained in Chapter 3 of this manual.

1.1.12 Option Modules

The PDP-8/A has two multi-option hex modules available. The M8316 module, which contains four separate PDP-8/A options, and the M8317 module, which contains three options. Each of these modules and the options provided by them are discussed in the following paragraphs and more fully described in Chapter 6.

1.1.13 DKC8-AA I/O Option Board (M8316)

The M8316 module contains a Serial Line Unit (SLU), a Real Time Crystal Clock, a General Purpose 12-Bit Parallel I/O, and the Programmer's Console control.

1.1.14 KM8-A Extended Option Board (M8317)

The M8317 module contains the Memory Extension and Timeshare Control, Power Fail and Auto Restart, and the Bootstrap Loader options.

1.1.15 Peripheral Options

Digital Equipment Corporation designs and manufactures many of the peripheral devices offered with the PDP-8/A. All peripheral options purchased from Digital include the necessary cables, controllers, interfaces, etc. required for system operation. Most options can be added to the system simply by inserting the modules into the Omnibus and making cable connections between the modules and the peripherals.

1.2 CONSOLE OPERATION

There are two types of panels for the PDP-8/A – the Limited Function Panel and the Programmer's Console. The Limited Function Panel is supplied with each PDP-8/A. The Programmer's Console is optional.

1.2.1 Limited Function Panel

The Limited Function Panel (Figure 1-3) has the necessary switches to apply power and to bootstrap the computer, and indicators – POWER ON, RUN, and BATTERY CHARGING – to determine whether the computer is operating. Table 1-3 describes the function of the various switches and indicators on the Limited Function Panel.

1.2.2 Programmer's Console

The key pad switches and indicators on the PDP-8/A Programmer's Console (Figure 1-4 and Table 1-4) augment the Limited Function Panel by allowing manual control of computer operation, and by presenting a convenient indication of program conditions within the computer. PDP-8/A program execution can be started, stopped, monitored, or switched among various modes of operation. The key pad switches also provide a means of selecting a memory location or major register for examination and allow selective modification of read/write memory.

1.2.3 Entering Data From the Programmer's Console

Data is entered into registers from the programmer's console by first pressing the numbered key pad switches corresponding to the octal number to be entered, then the key pad switch corresponding to the register into which the data is to be entered. For example, to load an octal number 7000 into the switch register, press 7, then press 0 three times, and then press LSR. The data entered will be transferred to the switch register. To read the data that was entered in the switch register, press SR and then DISP; the data is displayed in the 4 character octal readout.

Table 1-3
PDP-8/A Limited Function Panel
Controls and Indicators

Control or Indicator	Function
ON/OFF	In the up position, this switch applies power to the computer and all controls and indicators. Power is removed by moving the switch down.
PANEL LOCK	In the up position, this switch disables all key pad switches except Switch Register (SR) and the read functions. The RUN and BATTERY CHARGING indicators are not affected.
BOOT	When this switch is down, the Omnibus SW line is disabled (voltage level high). When it is up, the SW line is asserted (low). This switch is used to start programmable read only memory (PROM) and bootstrap loader programs. The key pad BOOT switch on the Programmer's Console has the same function.
BATTERY CHARGING	This indicator is a LED. It lights when the battery backup supply is charging in the PDP-8/A semiconductor computers; in the 8A420, 8A620, and 8A820 computers, it lights when both G8018 regulators are operating properly. The indicator is present on the 8A400, 8A600, and 8A800 computers, but is not used.
POWER	This indicator is a LED, lit when ac power is applied to the computer.
RUN	This indicator is a LED, lit when the RUN flip-flop is set.

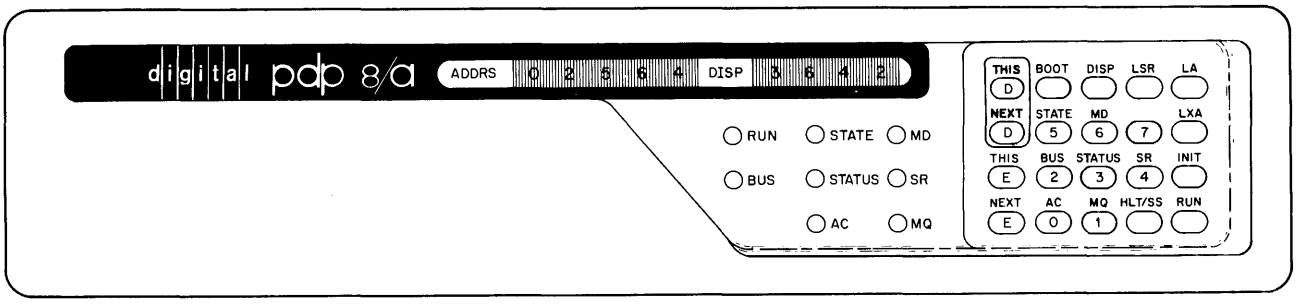

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Figure 1-4 PDP-8/A Programmer's Console

1.2.4 Examining Memory Locations

To determine the content of a location in memory, enter the memory field and press LXA, then enter the memory address and press LA. Press MD and then DISP. Now press E THIS and the contents of this memory location will be displayed in the 4-character octal readout. If you wish to examine two or more consecutive memory locations, content of the next memory location will be displayed each time E NEXT is pressed.

1.2.5 Entering Data in Memory

To enter (deposit) data in a memory location, first enter the field into which data is to be deposited and press LXA, then enter the address and press LA. Now enter the data and press D THIS. If you wish to enter data into two or more consecutive memory locations, press D NEXT after each entry is made.

Table 1-4
PDP-8/A Programmer's Console Controls and Indicators

Control or Indicator	Function
ADDRS	ADDRS is a 5 character octal readout that displays the content of the 3-bit Extended Memory Address (EMA) register and the 12-bit Memory Address (MA) register. The five characters (digits) show the address of the memory location to be accessed next.
DISP	DISP is a 4 character octal readout that displays the content of the register that has been selected for display. The Accumulator (AC), Multiplier Quotient (MQ), Status Register, Switch Register (SR), State, Memory Data (MD), or Data Bus (BUS) content may be read. To select one of these for display, first press the appropriate key pad switch (e.g., AC) and then press DISP. One of the LED indicators to the left of the key pad will be lit, indicating which data is displayed in the readout. DISP also indicates the number button that is pressed; i.e., if 3 (STATUS) is pushed, 3 appears in the right-most DISP position (if DISP is pushed after 3, the STATUS indicator lights and the DISP readout indicates the Status register contents). Thus, the operator can view the addresses being entered and the data being deposited.
RUN	This indicator is a LED, lit when the RUN flip-flop is set.
Key Pad Switches	
AC (0)	When key pad AC and then DISP are pressed, the content of the AC at Time State 1 is displayed in the 4 character octal readout. The AC indicator to the left of the key pad will also light.
MQ (1)	When key pad MQ and then DISP are pressed, the content of the MQ register is displayed in the 4 character octal readout. The MQ indicator to the left of the key pad will also light.
BUS (2)	When key pad BUS and then DISP are pressed, the content of the DATA BUS (DATA 0–11) at Time State 1 is displayed in the 4 character octal readout. The BUS indicator to the left of the key pad will also light.
STATUS (3)	When key pad STATUS and then DISP are pressed, the content of the Status Register is displayed in the 4-bit octal readout (Figure 1-5). The STATUS indicator to the left of the key pad will also light. The six most significant bits of the Status Register (bits 0–5) indicate either a set or cleared condition (logical one or logical zero). Thus, the octal readout for these digits must be decoded to determine whether the bit is set or cleared.
First Digit Position: Illegal Characters 2, 3, 6, and 7	An octal 4 or 5 indicates that the link is set. An octal 1 or 5 indicates that the Omnibus interrupt request line is asserted.

Table 1-4 (Cont)
PDP-8/A Programmer's Console Controls and Indicators

Control or Indicator		Function
Key Pad Switches (Cont)		
Second Digit		An octal 4, 5, 6, or 7 indicates that the INTERRUPT INHIBIT flip-flop is set. The INTERRUPT INHIBIT flip-flop is located in the memory extension and timeshare option. An octal 2, 3, 6, or 7 indicates that the interrupt system is enabled. An octal 1, 3, 5, or 7 indicates that the USER MODE line is asserted. Signal USER MODE originates in the memory extension and timeshare option on the Extended option board to disable execution of all OSR, LAS, HLT and IOT instructions when the computer is operating in Timeshare mode.
Third Digit		Displays the content of the 3-bit instruction field register (IF0–2) contained in the memory extension and timeshare option on the extended option board.
Fourth Digit		Displays the content of the 3-bit data field register (DF0–2) contained in the memory extension and timeshare option on the extended option board.
SR (4)		When key pad switch SR and then DISP are pressed, the content of the SR (switch register) will be displayed in the 4 character octal readout. The SR indicator to the left of the key pad will also light.
STATE (5)		When key pad switch STATE and then DISP are pressed, the condition of the major states, 3 bits of the instruction register (IR0–2), and 6 major Omnibus signals are displayed in the 4 character octal readout (Figure 1-6). The STATE indicator to the left of the key pad will also light. The octal readout must be decoded to determine if the individual bits are in a set or cleared condition (a logical one or a logical zero).
First Digit Position	Illegal Characters 3, 5, 6, and 7	A zero indicates that the processor is in the DMA state. An octal 1 indicates that the processor is in the Execute major state. An octal 2 indicates that the processor is in the Defer major state. An octal 4 indicates that the processor is in the Fetch major state.
Second Digit		Displays the content of the 3-bit Instruction Register (IR0–2).

Table 1-4 (Cont)
PDP-8/A Programmer's Console Controls and Indicators

Control or Indicator	Function
Key Pad Switches (Cont) Third Digit	An octal 4, 5, 6, or 7 indicates that the MD DIR line on the Omnibus is asserted. Signal MD DIR is low and bit 6 is a logical one during operations that read data from memory. MD DIR is high and bit 6 is a logical 0 during operations that write data into memory. An octal 2, 3, 6, or 7 indicates that BREAK DATA CONT line on the Omnibus is asserted. BREAK DATA CONT is low and bit 7 is a logical one during some direct memory access (DMA) operation. An octal 1, 3, 5, or 7 indicates that the SW line on the Omnibus is asserted. This occurs only when BOOT on the Programmer's Console or the Limited Function Panel is pressed.
Fourth Digit	An octal 4, 5, 6, or 7 indicates that the I/O PAUSE line on the Omnibus is asserted. Signal I/O PAUSE L is generated during the execution of an IOT instruction. An octal 2, 3, 6, or 7 indicates that the BREAK IN PROG line on the Omnibus is asserted (one or more devices are requesting a data break). The highest priority device will begin a DMA operation at the beginning of the next cycle. An octal 1, 3, 5, or 7 indicates that the BREAK CYCLE line on the Omnibus is asserted (a DMA operation is taking place).
MD (6)	When MD and then DISP are pressed, the data on the 12-bit MEMORY DATA bus (MD0–11) on the Omnibus are displayed in the four character octal readout. The bus normally carries the content of the last memory location addressed by the 15-bit memory address register.
LA	Pressing LA (load address) loads the contents of the entry into the Central Processor Memory Address (CPMA) register and enables the FETCH major state for the next processor cycle.
LXA	Pressing LXA (Load Extended Address) loads the right-most digit of the entry into the Data Field (DF) register and the next digit of the entry into the instruction Field (IF) register.
INIT	Pressing INIT (Initialize) generates an INIT pulse that clears the AC, the LINK, all I/O device flags and registers, and all interrupt system flip-flops. This is equivalent to a programmed CAF instruction.
RUN	Pressing RUN generates a MEM START L signal, and sets the RUN flip-flop. The program starts executing at the address that is in the CPMA register.

Table 1-4 (Cont)
PDP-8/A Programmer's Console Controls and Indicators

Control or Indicator	Function
Key Pad Switches (Cont)	
LSR	Pressing the LSR switch loads the entry into the Switch Register. The Switch Register serves as a 12-bit temporary storage register for data entries. The contents of the Switch Register can be read under program control by the OSR and LAS instruction.
BOOT	Pressing BOOT twice causes the SW flip-flop to assert and then negate the SW line on the Omnibus. The transition from assertion to negation of the SW line causes a bootstrap operation to be performed. The signal from this BOOT switch is ORed with the signal generated by BOOT on the Limited Function Panel so that either switch can assert the SW signal on the Omnibus.
E THIS	Pressing E THIS (Examine This) loads the contents of the memory location addressed by the CPMA register into the Memory Buffer (MB) register. The CPMA and PC are not incremented after this operation. To observe the content of the MB, press MD, then DISP.
E NEXT	Pressing E NEXT (Examine Next) loads the content of the memory location addressed by the CPMA into the Memory Buffer (MB) register and increments the CPMA and PC registers. This feature allows the operator to step through a program and observe the operation of one of the major registers, buses, etc., in the octal readout.
D THIS	Pressing D THIS (Deposit This) loads the content of the entry into the MB register and into memory at the address specified by the CPMA register. The CPMA and PC are not incremented by this operation.
D NEXT	Pressing D NEXT (Deposit Next) loads the content of the entry into the MB register and into memory at the address specified by the CPMA register. At the end of the operation, the PC and CPMA registers are incremented.
HLT/SS	Pressing HLT/SS (Halt/Single Step) while the machine is running will cause it to stop. If the machine is stopped, pressing HLT/SS causes the machine to execute one machine cycle.

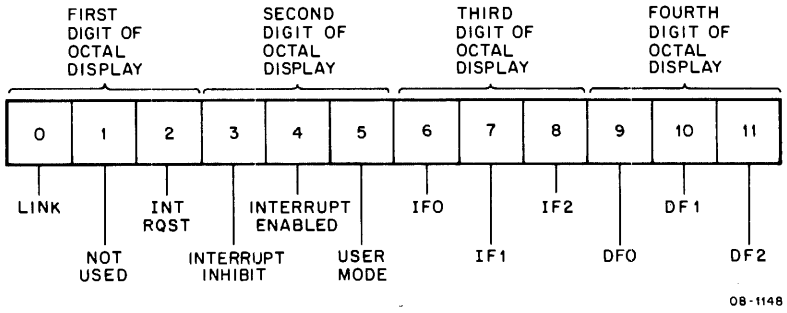

Figure 1-5 Status Information

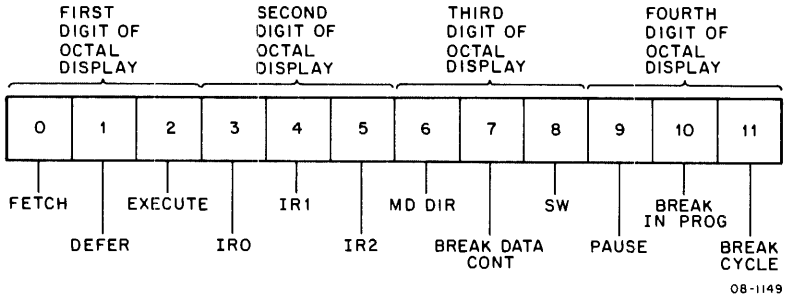

Figure 1-6 State Information

CHAPTER 2
INSTALLATION AND ACCEPTANCE TEST

This chapter contains supplementary information and procedures for installing the PDP-8/A Computer System. Basic installation and planning information, such as space requirements, environmental requirements, installation requirements, and system configuration data, are provided in Chapter 13 of the *PDP-8/A Miniprocessor Handbook*. Installation functions are summarized in Table 2-1.

All PDP-8/A computers and modules are tested thoroughly at DIGITAL's manufacturing facilities before they are shipped. However, many switches and jumper wires can be arranged by the customer for specific purposes; furthermore, there is a need both to verify the accuracy of system interconnections and site preparations, and to detect possible hidden damage incurred during shipping. Consequently, a number of initial operating tests are also included in this chapter.

Table 2-1
Summary of Installation Functions

Identify space and power required for system configuration.
Survey proposed site
Prepare site in accordance with environmental space and power requirements.
Unpack equipment and check inventory checklist.
Install equipment.
Run acceptance test.
Enter results of acceptance test in log book.

2.1 SITE CONSIDERATIONS

Adequate site planning and preparation can simplify the installation process and result in an efficient, more reliable PDP-8/A system installation. DEC Sales Engineers or Field Service Engineers are available for counseling and consultation with user personnel regarding the installation.

Site planning should include a list of the actual components to be used in the installation; this list should also include such items as storage cabinets, supplies, work tables, etc.

Primary planning considerations are:

1. The availability and locations of adequate power
2. Protection against direct heat sources
3. Electrical noise radiation

4. Shock

5. The existence of fire protection devices.

If existing environmental conditions dictate, air conditioning and/or dehumidifying equipment (though not required for the PDP-8/A) can become part of the site planning program.

2.1.1 Power Source

The power source should be free from conductive interference. In addition, all computer system supplies should be connected to the same power source to avoid loading and source differentials that may affect computer operation.

2.1.2 I/O Cabling Requirements

The cabling for rack-mounted equipment can be routed into the chassis through an opening located in the rear of the chassis. Subflooring is not necessary because casters elevate the cabinet high enough to provide sufficient cable clearance. The cabling should be located where it cannot be damaged. This is especially important if the processor and peripherals are not in close proximity.

2.1.3 Fire and Safety Precautions

The PDP-8/A Power Supply contains a thermal cut-out switch, circuit breaker, and fuses for protection against overheating and overloading. Both the cabinet and the power receptacle must be adequately grounded to ensure safe operation. A water pipe or steel beam provides an adequate ground. Refer to Chapter 13 of the *PDP-8/A Miniprocessor Handbook* for grounding and power installation procedures.

WARNING

The frame of the computer must be grounded to protect personnel from dangerous electrical shock.

Grounding is achieved automatically when a 3-wire plug is used. However, a voltage reading from frame to ground should be performed initially.

Electrical fires, although extremely unlikely, should always be extinguished by a Class 3 (CO_2) fire extinguisher.

2.2 UNPACKING INSTRUCTIONS

All PDP-8/A computers are packaged in two containers, the inner container holding the computer, and a type of protective material. The steps in this section are sufficiently general to apply to any PDP-8/A. To unpack the PDP-8/A computer, proceed as follows:

1. Open the outer carton and remove the inner carton.

2. Open the inner carton.

3. Carefully remove the cardboard from the top and sides of the computer.

4. Carefully remove the computer from the box.

5. Inspect the computer for damage. If the computer is damaged, notify the carrier immediately.

6. Unpack any other boxes included in the shipment.

7. Check that all equipment, software, manuals, etc., are present as specified on the shipping list inside the carton.

8. Save the cartons and packing material to use if the PDP-8/A is later repacked.

2.3 PACKING INSTRUCTIONS

Two kinds of packages are used for PDP-8/A computers. The kind used and the applicable packing instructions depend on the type of PDP-8/A chassis assembly.

2.3.1 BA8-C Chassis Assembly

The 8A420, 8A620, and 8A820 computers use a BA8-C chassis assembly (20-slot Omnibus). Figure 2-1 illustrates the packing procedure. First, the computer is placed in the inner container (9905417), the empty space is filled with plastic protective material (AIR CAP, SD-120), and the container is sealed. The sealed inner container is surrounded with protective foam material which is enclosed by the two telescope caps. Finally, the package is secured by two plastic straps.

2.3.2 Other PDP-8/A Chassis Assemblies

CAUTION

The G8016 Regulator board assembly used on PDP-8/A semiconductor computers contains a battery. This battery, while not of sufficient voltage to cause electrical shock, represents a possible hazard if shorted. If repacking this type of computer, ensure that there is no loose metal, such as solder, wire, or sheet metal parts inside the cabinet.

The PDP-8/A semiconductor computer and the 8A400, 8A600, and 8A800 computers use a chassis assembly that has a 10-slot or 12-slot Omnibus. To pack these computers proceed as follows:

1. Place the computer in the smaller of the two shipping cartons with the back (side with power cord) of the computer against the side of the carton.

2. Place the beveled die-cut sheet with foam protector (part number 9905675) in front of the computer (Figure 2-2). If the Limited Function Panel and a pop panel are on the computer, the beveled edge should be down inside the carton. If the computer has a Programmer's Console, the beveled edge should be up so that the cut-out in the cardboard fits the Programmer's Console.

3. Place the die-cut sheet with foam (part number 9905667) downward over the computer. The end with two pieces of foam should be fitted around the fans and the other end should be positioned so that the cardboard fits behind the cabinet mounting flange and the foam is against the side of the carton.

4. Close the flaps and seal the carton with tape.

5. Surround the sealed carton with protective foam material and enclose with telescope caps (Figure 2-3).

6. Strap in both directions using steel or plastic strapping.

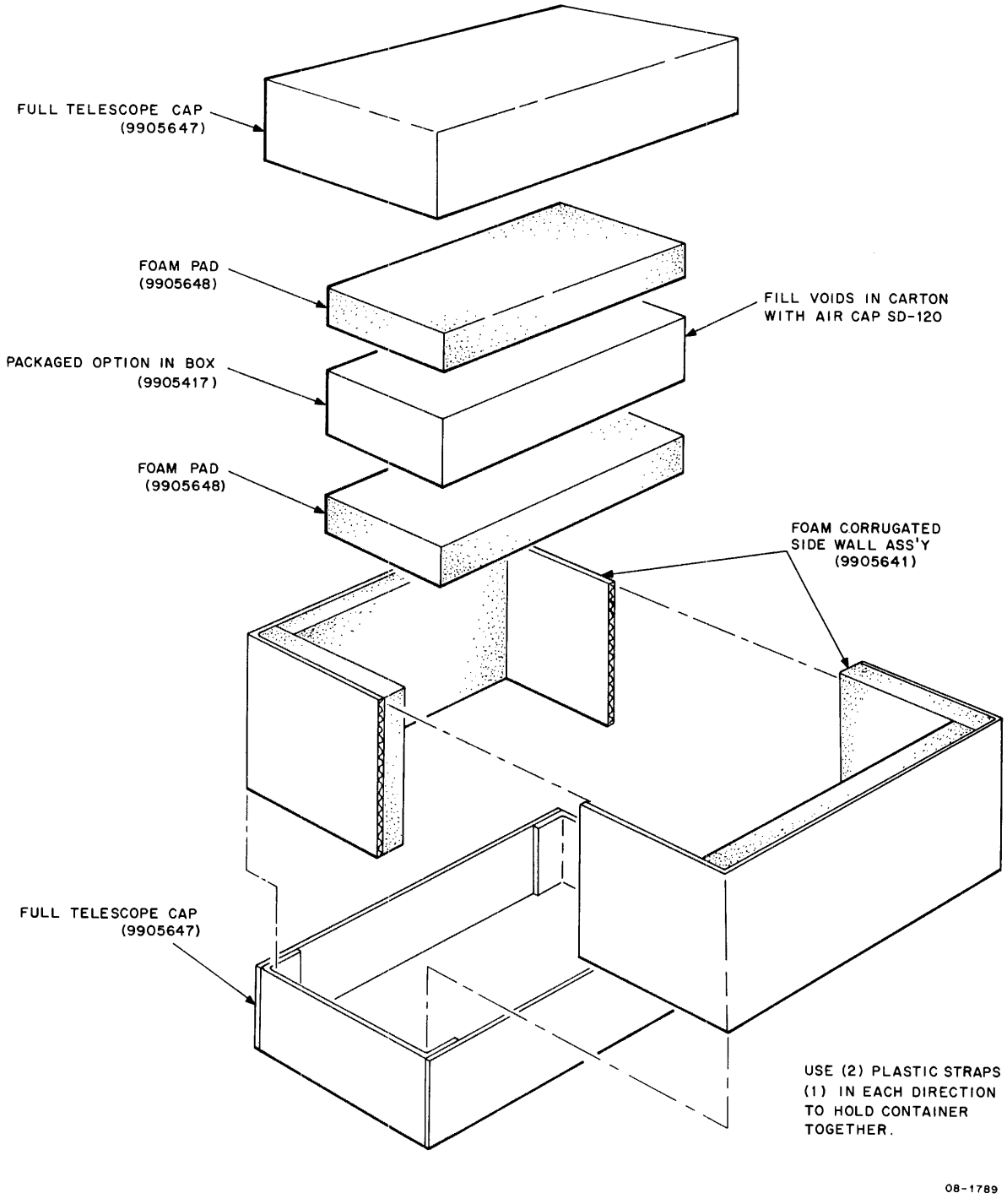

Figure 2-1 8A420, 8A620, 8A820 Packaging

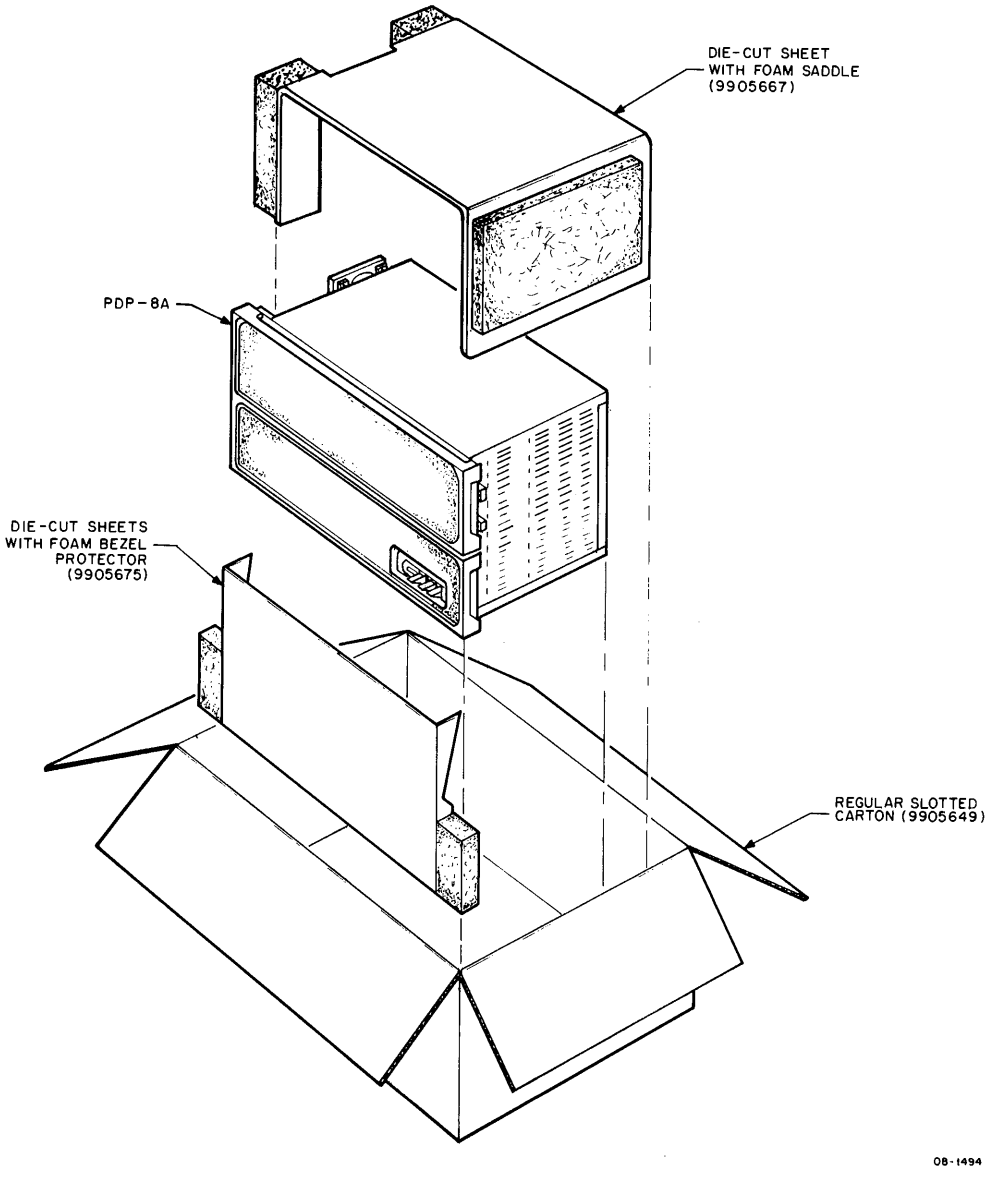

Figure 2-2 PDP-8/A Computer Packaging (Inner)

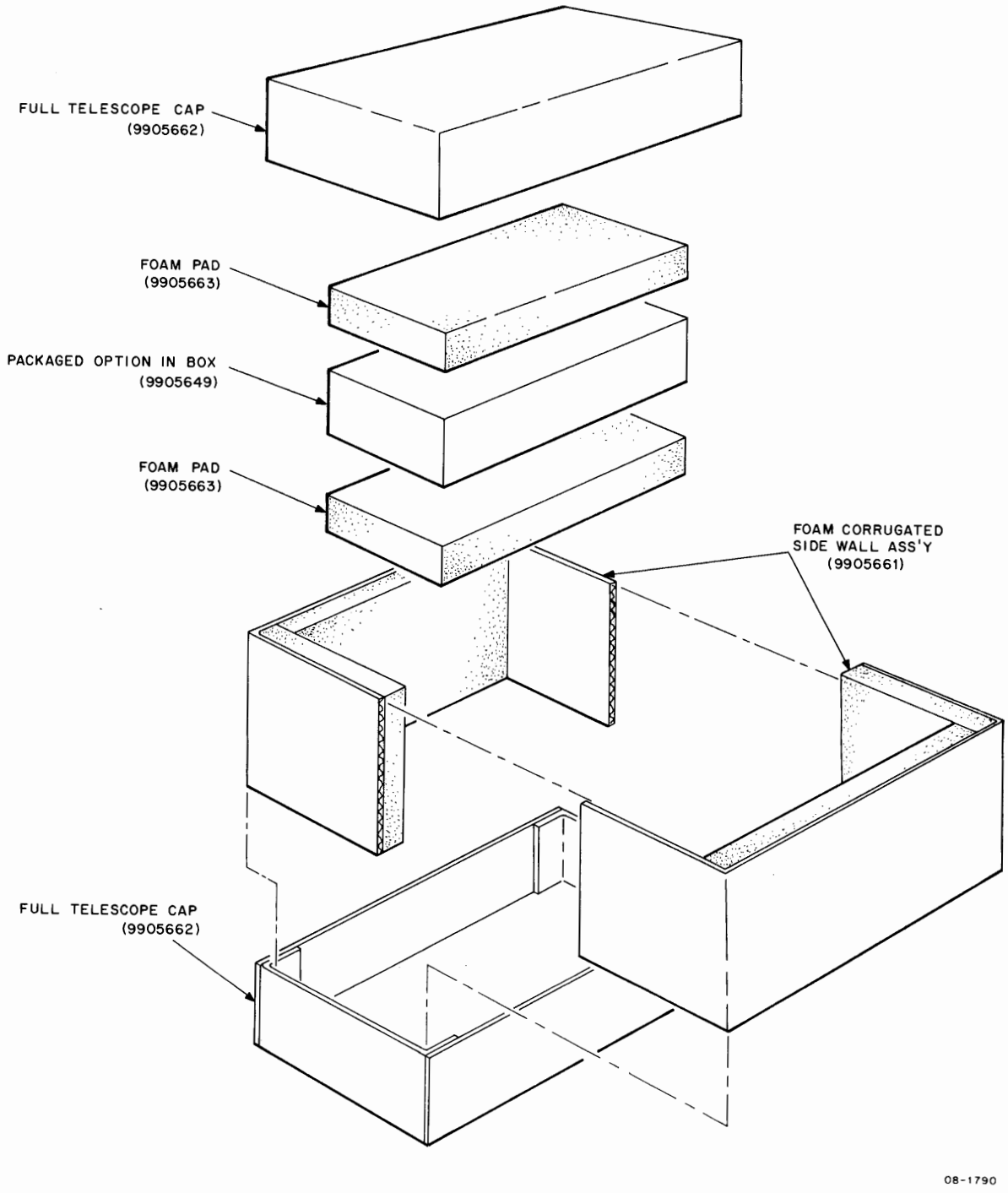

Figure 2-3 PDP-8/A Computer Packaging (Outer)

2.4 PDP-8/A BASIC SYSTEM COMPONENTS

A PDP-8/A basic system comprises many components. The following three systems are the most common:

1. A basic* PDP-8/A, a memory, and a Limited Function Panel.

2. A basic PDP-8/A, a memory, a Limited Function Panel, a KM8-A Extended Option board, a DKC8-AA I/O Option board, and a Programmer's Console (Paragraph 2.6 describes operating tests for this system).

3. A system as described in type 2 above, but accompanied by a Teletype® and diagnostic** programs (Paragraph 2.8 describes operating tests for this system).

As Table 1-2 indicated, a PDP-8/E CPU (KK8-E) can be used with the PDP-8/A system (8A600 and 8A620). In addition to the CPU, most DIGITAL PDP-8/E options will operate with the PDP-8/A computers. The following will not:

1. KP8-E Power Fail/Auto-Restart option
2. DK8-EA Line Frequency Real-Time Clock option
3. MM8-E 4K Core Memory
4. MM8-EJ 8K Core Memory

The KE8-E option (Extended Arithmetic Element) and the TD8-E DECtape Control will operate only with the 8A600 and 8A620 computers.

Modules can be inserted in almost any PDP-8/A Omnibus slot. There are, however, some restrictions and these are summarized in Table 2-2. Notice that an M8320 module (Bus Loads) is inserted in slot 1 of the 8A600 and 8A620 computers. This module must be modified before it can be used in the 8A600 and 8A620 computers. If the modification has been accomplished, R55 (Figure 2-4) will have been removed; if R55 is present, carry out the procedure outlined in DEC ECO M8320-00007.

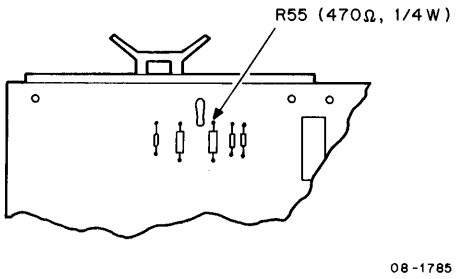

Figure 2-4 Part of M8320 Module Showing R55, Which is Removed for 8A Operation

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*A basic PDP-8/A is defined as a Central Processor Unit (CPU) and a chassis assembly (chassis, Omnibus, and power supply).

**Diagnostics are test programs written to find faults in the logic. The PDP-8/A programs are supplied on paper tape. Diagnostic programs are optional and may be ordered from the Software Distribution Center, 146 Main Street, Maynard, Massachusetts 01754.

Table 2-2
PDP-8/A Computers, Dedicated Omnibus Slots

Omnibus Slot	8A600	8A600 & KE8-E	8A620	8A620 & KE8-E	PDP-8/A Semiconductor, 8A400, 8A420, 8A800, 8A820
1	M8320	M8320	M8320	M8320	M8315
2	M8316	M8316	M8316	M8316	M8316
3	M8317	M8317	M8317	M8317	M8317
4					
5					
6					
7					
8		M8300			
9		M8310			
10	M8300	M8341			
11	M8310	M8340			
12	M8330	M8330			
13					
14					
15					
16				M8300	
17				M8310	
18			M8300	M8341	
19			M8310	M8340	
20			M8330	M8330	

Note 1: M8316 and M8317 are interchangeable in slots 2 and 3.
Note 2: Module numbers are related to options as follows:

M8315 – CPU (KK8-A)
M8316 – I/O Option Board (DKC8-AA)
M8317 – Extended Option Board (KM8-AA)
M8320 – Bus Loads
M8300 – CPU
M8310 –
M8330 – Timing Generator
} KK8-E

2.4.1 Chassis Descriptions

Three chassis types are available. The PDP-8/A Semiconductor computer chassis is illustrated in Figure 2-5 (the front panels have been removed). Modules are inserted in the Omnibus from the front of the unit. Both quad- and hex-size modules can be inserted; the fingers on connectors E and F of the hex size modules do not carry Omnibus signals (some hex modules do not have connectors E and F). Figure 2-6 illustrates the dimensions of the same computer, as well as indicating the ac line and fuse locations.

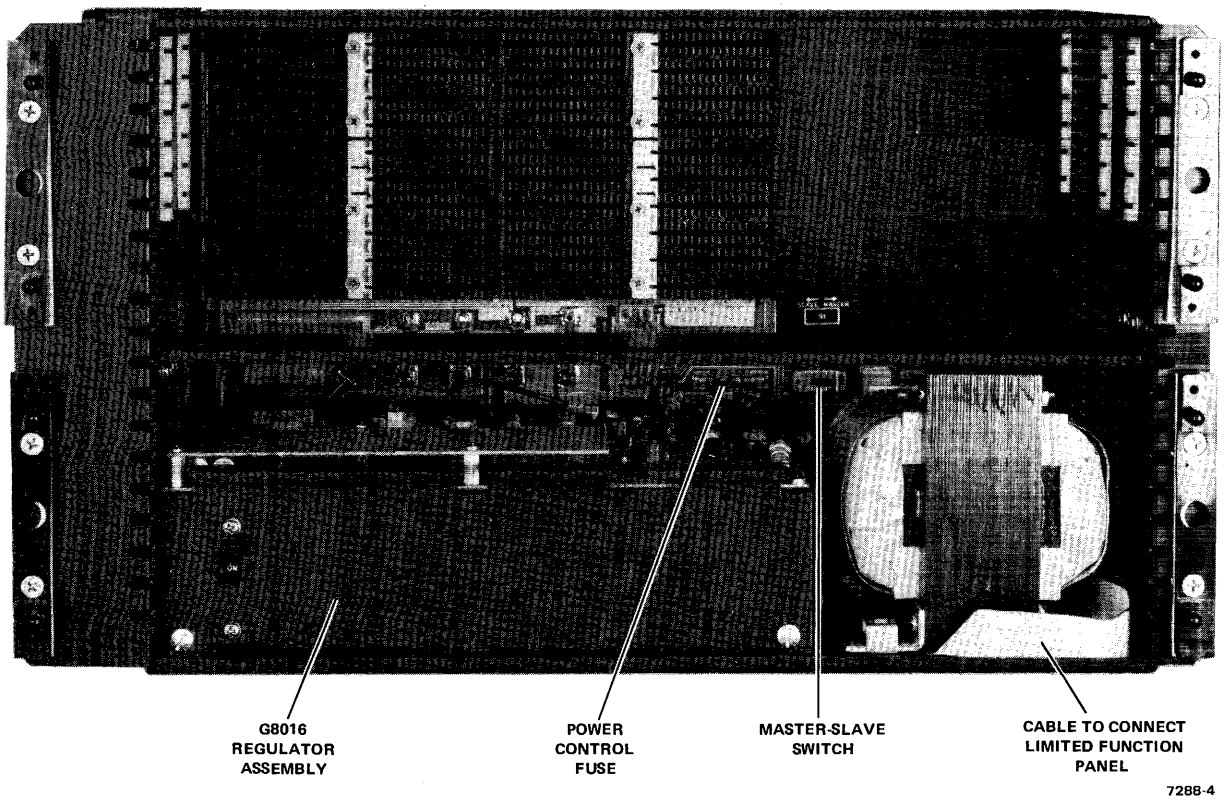
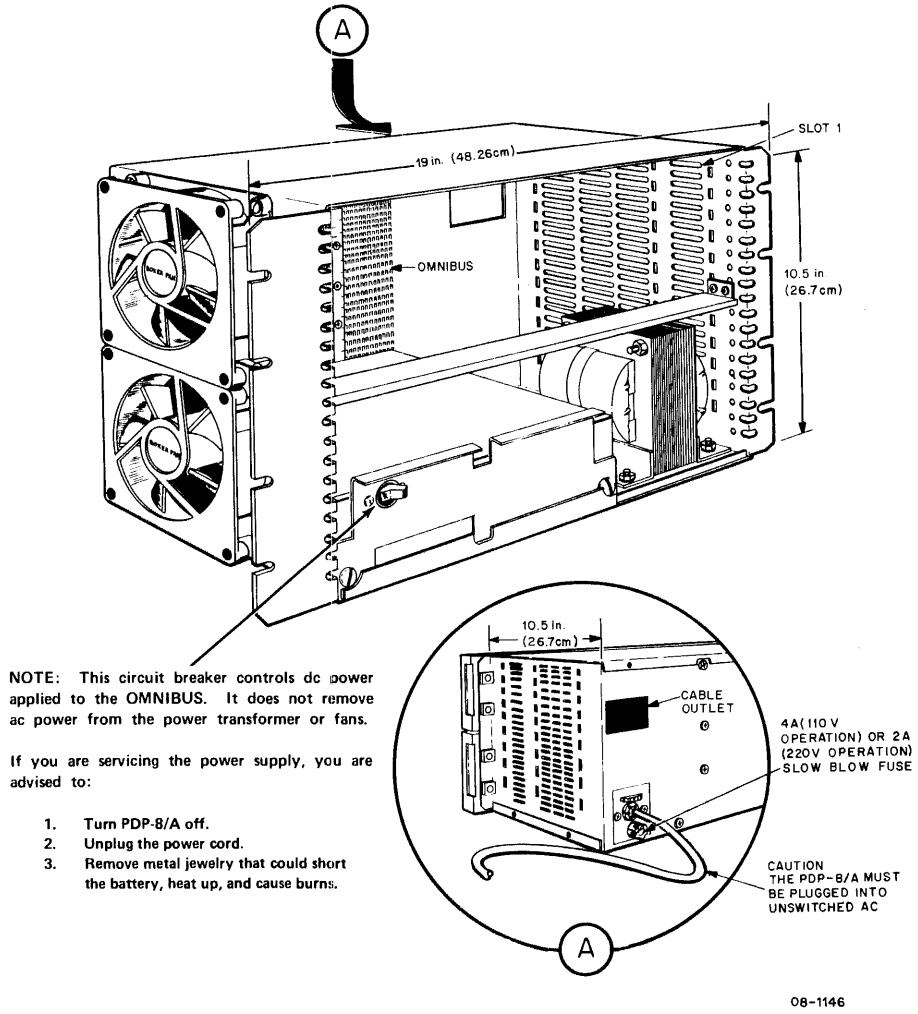


Figure 2-5 PDP-8/A Semiconductor Chassis



NOTE: This circuit breaker controls dc power applied to the OMNIBUS. It does not remove ac power from the power transformer or fans.

If you are servicing the power supply, you are advised to:

1. Turn PDP-8/A off.
2. Unplug the power cord.
3. Remove metal jewelry that could short the battery, heat up, and cause burns.

Figure 2-6 PDP-8/A Semiconductor Computer Chassis Dimensions

Figure 2-7 shows the chassis that is used with 8A400, 8A600, and 8A800 computers. The dimensions are the same as the PDP-8/A Semiconductor chassis; interior components are different. The G8018 regulator assembly has been removed to show the connector in which the assembly is inserted. The Omnibus connector blocks in the connector E position are needed to accommodate the E connector of the core memory modules.

Figure 2-8 shows the chassis used with the 8A420, 8A620, and 8A820 computers. The example shown is an 8A620, containing the KK8-E CPU and Timing Generator, as well as the Bus Loads module. The H9195 Omnibus is mounted on the Center Wall assembly (DEC Part Number 70-12561); modules are inserted from the front of the unit. Two G8018 regulator assemblies are contained in the rear of the chassis; the regulator boards are inserted in PC board slots that are mounted on the rear of the Center Wall assembly. Figure 2-9 is an outline drawing that gives the chassis dimensions and illustrates the placement of the G8018 assembly.

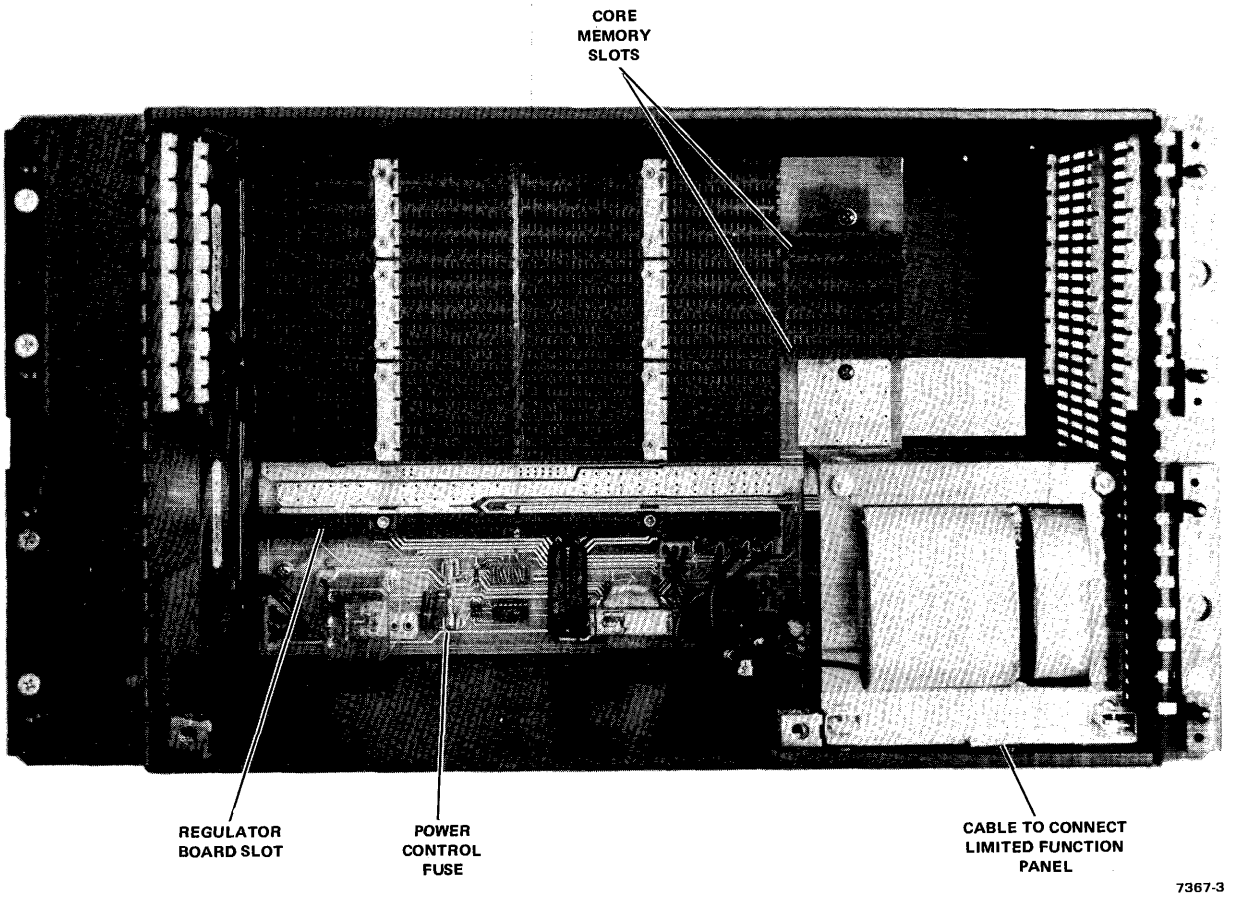
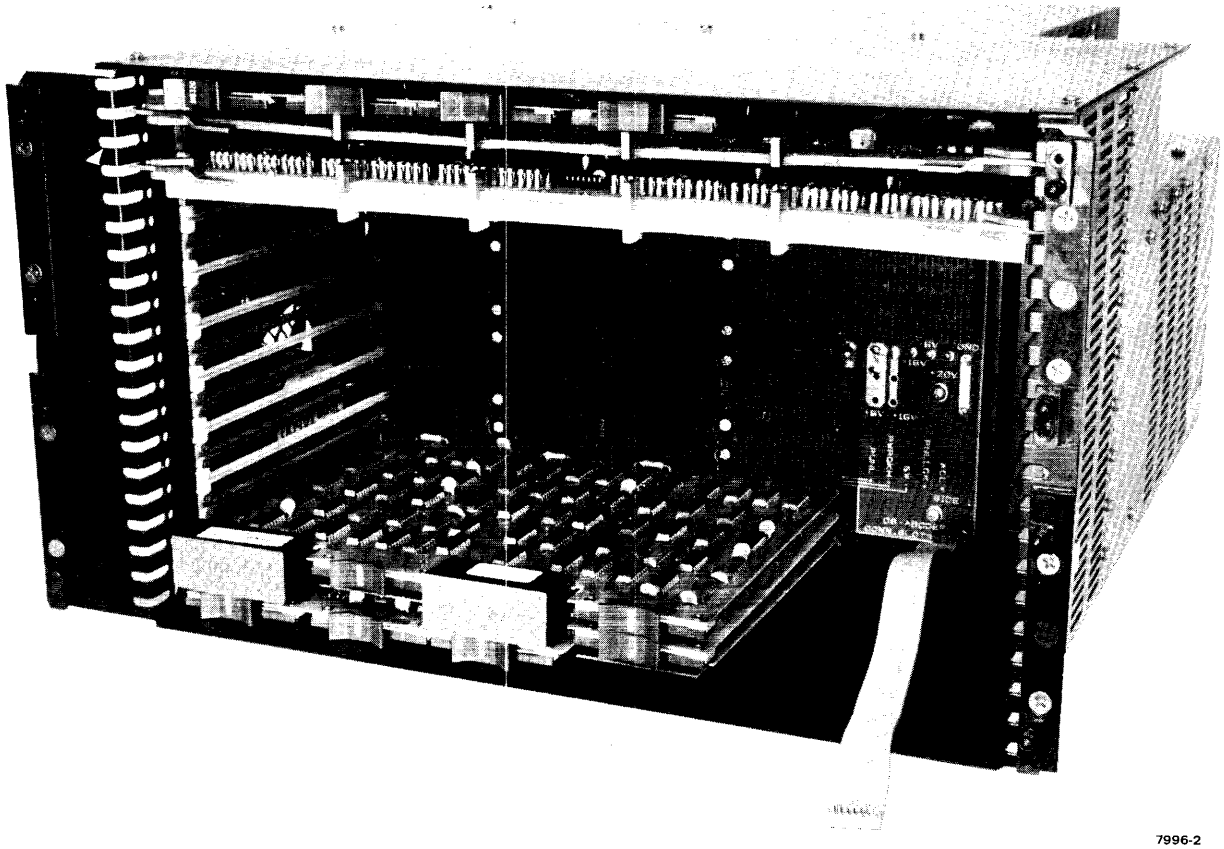


Figure 2-7 PDP-8/A Chassis (H9300)
(Transformer Cover Removed)



7996-2

Figure 2-8 PDP8/A Chassis
(8A240, 8A620, 8A820)

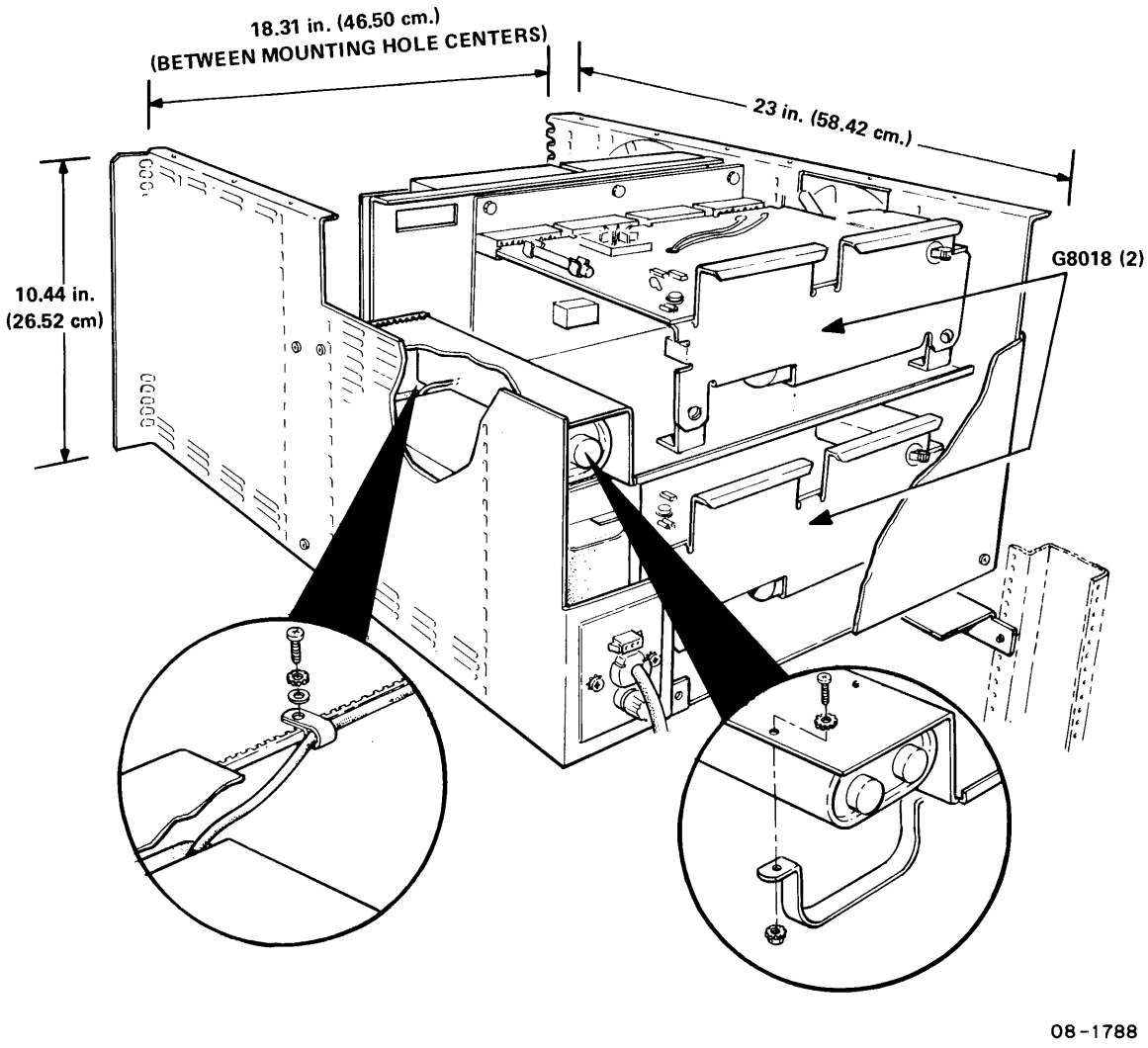


Figure 2-9 8A420/620/820 Chassis Dimensions

2.4.2 Expansion Techniques

Table 1-2 noted that the 8A600 and 8A620 computers could be expanded. Either a BA8-C or an H9300 can be added to the basic chassis increasing the system capacity accordingly. Figure 2-10 illustrates the basic chassis and the expansion possibilities available for each type.

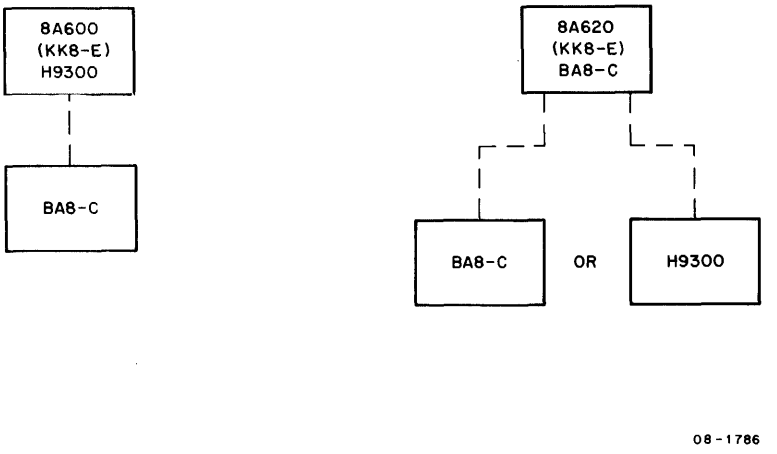


Figure 2-10 8A600/8A620 Expansion

The basic chassis is connected to the expander chassis by BC08H cable assemblies. One cable connector is inserted into either the top slot or the bottom slot of the basic chassis, depending on whether the expander chassis is located above or below. The other connector is inserted into slot 1 or slot 20 of the expander chassis. If the 8A620 is being expanded with an H9300 chassis assembly, the M8300, M8310, and M8330 modules must be removed from the basic chassis and placed in slots 10, 11, and 12, respectively, of the expander chassis. If the computer includes a KE8-E option, this too must be removed from the basic chassis and inserted in the appropriate Omnibus slots of the expander. Refer to the *PDP8 Configuration Guide* for definitive guidelines concerning expansion.

2.4.3 PDP-8/A Module Descriptions

The major units that constitute a PDP-8/A are described in the following paragraphs, along with the module switch settings.

CAUTION

Switch settings may be accidentally changed unless modules are removed and inserted carefully.

2.4.3.1 KK8-A Central Processor Unit (CPU) – The KK8-A, shown in Figure 2-11 is a multilayer hex module (M8315) which resides in the top slot of the Omnibus. The KK8-A has an auto-start feature used to start the computer automatically when power is turned on.

NOTE

If you are not using the CPU Auto-Start feature, turn switch S1-7 ON and switches S1-1 through S1-6 and S1-8 OFF.

If you are using the CPU Auto-Start feature, set switches as shown in Table 2-3.

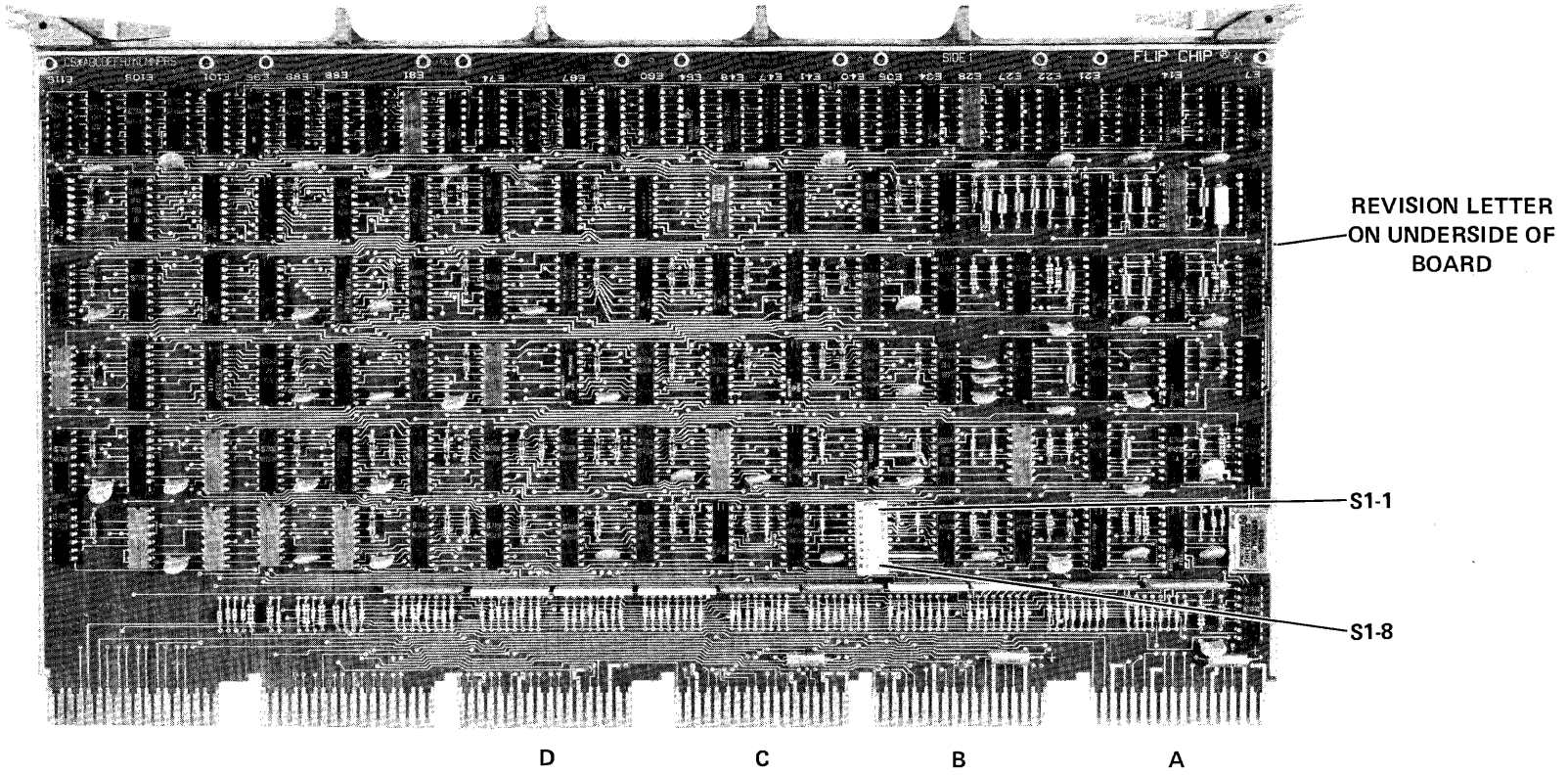


Figure 2-11 KK8-A (M8315) CPU Module

Table 2-3
KK8-A (M8315) Central Processor Unit Switch Settings

Switch	Function (When in the ON Position)
S1-1	Start in field 7 (OFF position specifies Field 0)
S1-2	Start at address 4000
S1-3	Start at address 2000
S1-4	Start at address 1000
S1-5	Start at address 0400
S1-6	Start at address 0200
S1-7	CPU Auto Start Disabled
S1-8	OFF

Starting address 0000 may be selected by leaving switches S1-2 through S1-6 all OFF. Only one switch in the group S1-2 through S1-6 may be ON at any time. Failure to observe this precaution will result in a malfunction, even if the auto-start feature is not used.

2.4.3.2 MS8-A Read/Write Random Access Memory (RAM) – The MS8-A, shown in Figure 2-12, is a quad module (M8311), semiconductor, read/write Random Access Memory available in the following configurations:

Option	Memory Size	Module Number
MS8-AA	1K	M8311-YA
MS8-AB	2K	M8311-YB
MS8-AD	4K	M8311-YD

NOTE
If you are using a 4K RAM in Field 0, set switches S1-1, 2, 3, 4, 5, 6 and 10 ON and turn S1-7, 8, and 9 OFF.

Set switches as shown in Table 2-4 if other memory configurations are used.

2.4.3.3 MR8-A Read Only Random Access Memory (ROM) – The MR8-A, shown in Figure 2-13, is a quad module (M8312), Read Only Random Access Memory, available in the following configurations:

Option	Memory Size	Module Number
MR8-AA	1K	M8312-YA
MR8-AB	2K	M8312-YB
MR8-AD	4K	M8312-YD

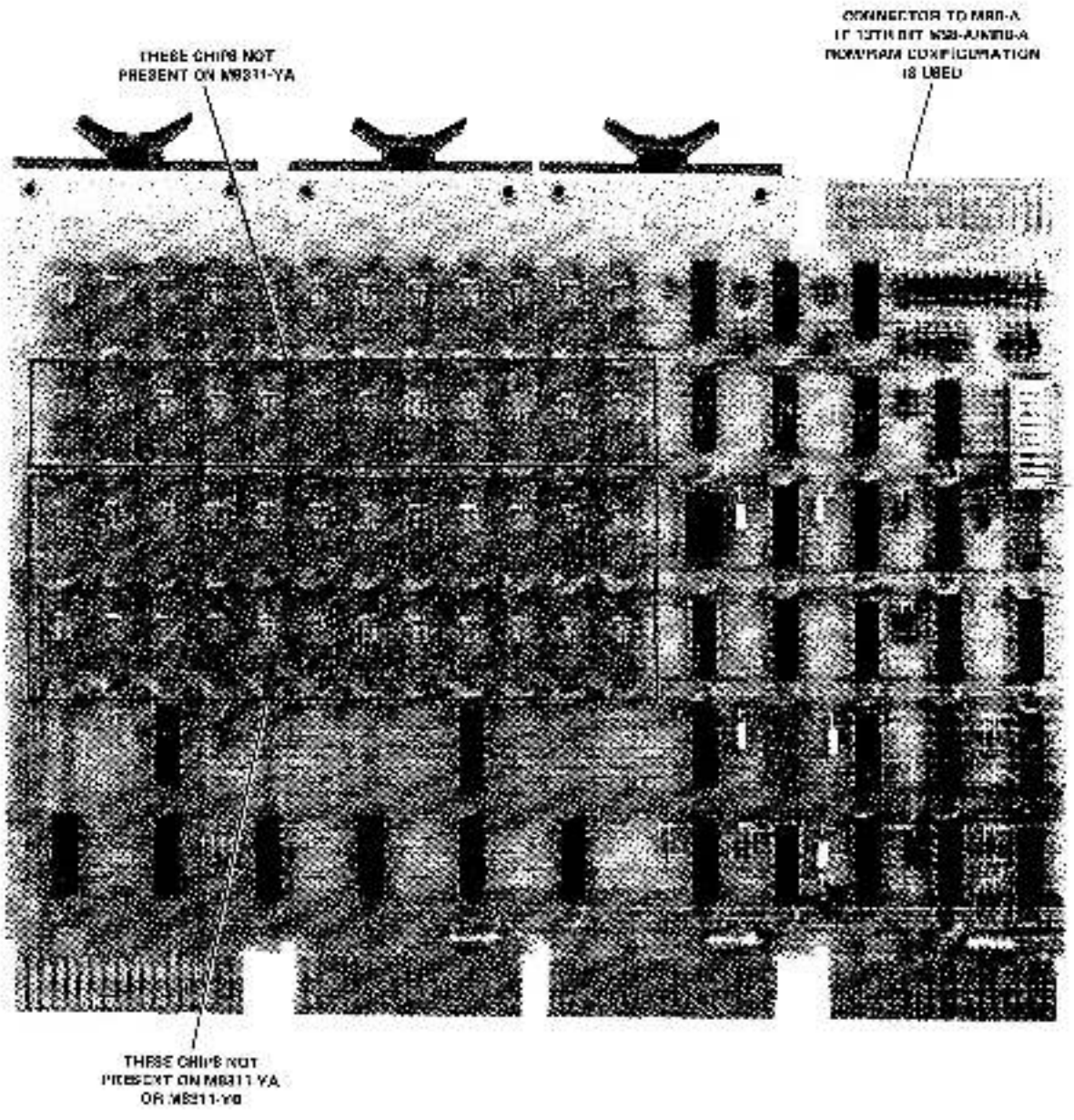


Figure 2-12 M8I-A (M9311) Read/Write Random Access Memory

Table 2-4
MS8-A Read/Write Memory Switch Settings

Switch	Function/Position
S1-1, 2, and 3	Field Selection

S1-1	S1-2	S1-3	Field Selected
ON	ON	ON	0
OFF	ON	ON	1
ON	OFF	ON	2
OFF	OFF	ON	3
ON	ON	OFF	4
OFF	ON	OFF	5
ON	OFF	OFF	6
OFF	OFF	OFF	7

S1-4 and 5 — First Address

S1-4	S1-5	First Address in this RAM is
ON	ON	0000
ON	OFF	2000
OFF	ON	4000
OFF	OFF	6000

S1-6	ON for 4K Memory M8311-YD
S1-7	OFF
S1-8	ON for 2K Memory M8311-YB
S1-9	ON for 1K Memory M8311-YA
S1-10	Test switch, normally ON

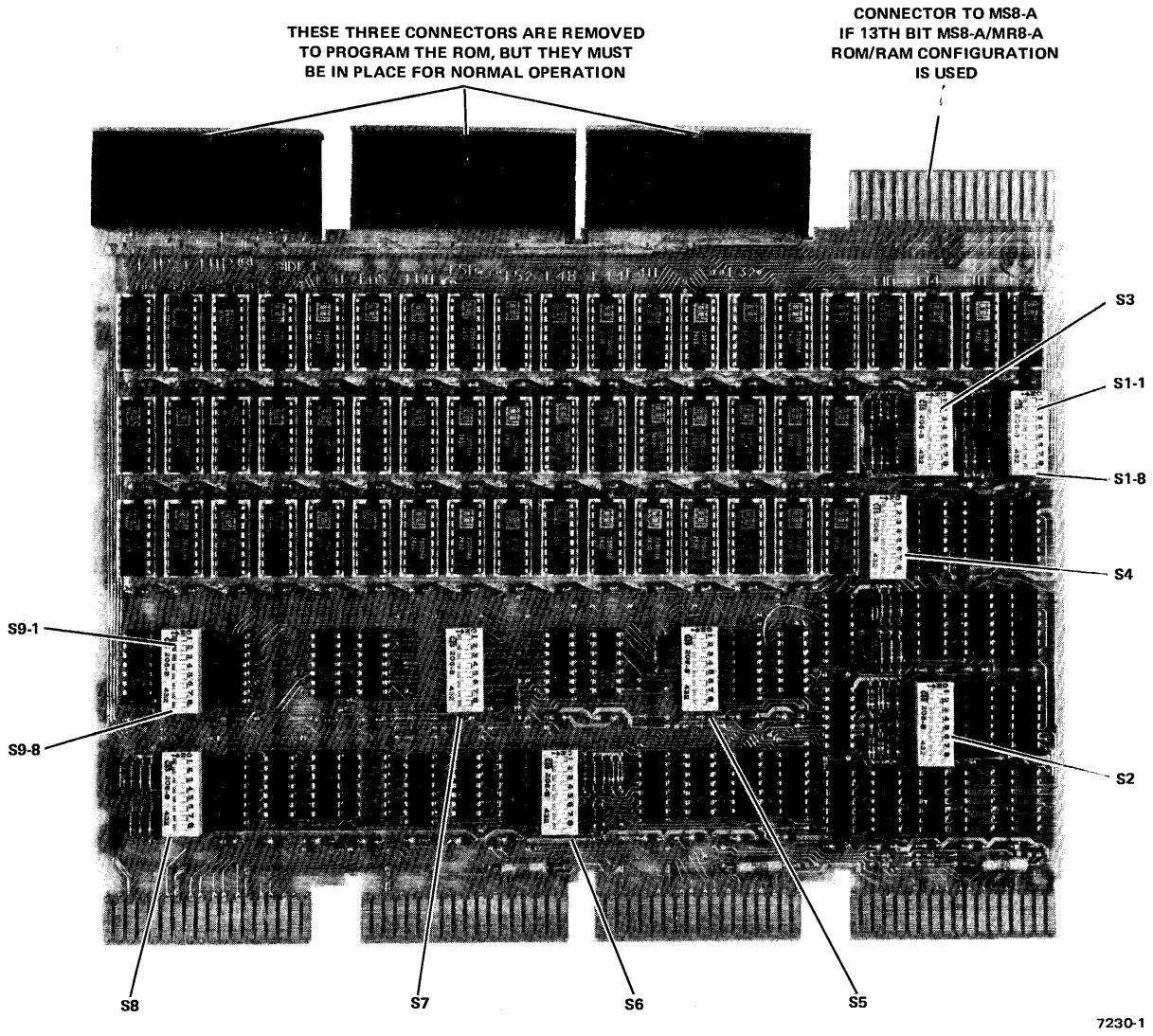


Figure 2-13 MR8-A (M8312) Read Only Memory (ROM)

The first address is always location 0000 of the selected memory field.

NOTE

If you are using a 4K ROM in Field 0 with no connections to RAM, set switches as follows: S1-1 through S1-8; S5-1 through S5-8; S7-1 through S7-8; S8-1 through S8-8; S9-1 through S9-8; S4-1, 2, 3, 6, 7, 8; and S6-3, 8; all ON. S2-1 through S2-8; S4-4, 5; S6-1, 2; all OFF. If a RAM is used with top connectors, change S4-7 to OFF.

Table 2-5 lists the switch settings for other memory configurations.

CAUTION

All switches must be OFF when the M8312 is being programmed (i.e., while data is being loaded into ROM).

Table 2-5
MR8-A Read Only Memory Switch Settings

Switch	Function/Position
S1-1 to S1-8	ON
S2-1, 8, and 5	Size Select Switch Settings S2-1 / S2-8 / S2-5 / Memory Size ON / ON / OFF / 1K ON / ON / OFF / 2K OFF / OFF / OFF / 4K
S2-2 and 4	OFF
S2-3, 6, and 7	Field Select Switch Settings Field / S2-6 / S2-3 / S2-7 0 / OFF / OFF / OFF 1 / ON / OFF / OFF 2 / OFF / ON / OFF 3 / ON / ON / OFF 4 / OFF / OFF / ON 5 / ON / OFF / ON 6 / OFF / ON / ON 7 / ON / ON / ON
S3-1 to S3-8	ON
S4-1, 2, 3, 4, 6, and 8	ON
S4-5	OFF
S4-7	OFF for ROM/RAM Combination; otherwise ON
S5-1 to S5-8	ON
S6-1 and S6-2	OFF
S6-3, 4, 5, 6, 7, and 8	ON
S7-1 to S7-8	ON
S8-1 to S8-8	ON
S9-1 to S9-8	ON

2.4.3.4 MM8-AA 8K Core Memory – The MM8-AA, shown in Figure 2-14, is a hex module (G649) with H219A stack assembly that contains 8K of core memory.

NOTE
If you are using core memory in fields 0 and 1, install W1-3 and W1-2 and remove W2-4 and W3-4.

Install or remove jumpers as shown in Table 2-6 if other memory fields are in use.

Table 2-6
MM8-AA 8K Core Memory Jumper Installation

Fields Used	W1-3	W1-2	W2-4	W3-4
0 and 1	IN	IN	OUT	OUT
2 and 3	OUT	IN	IN	OUT
4 and 5	IN	OUT	OUT	IN
6 and 7	OUT	OUT	IN	IN

2.4.3.5 MM8-AB 16K Core Memory – The MM8-AB, shown in Figure 2-15, is a hex module (G650) with H219E stack assembly that contains 16K of core memory.

NOTE
If the MM8-AB is installed in fields 0 through 3, jumpers W1-3 and W1-2 should be installed and W2-4 and W3-4 should be removed.

Install or remove jumpers as shown in Table 2-7 if other memory fields are used.

Table 2-7
MM8-AB 16K Core Memory Jumper Installation

Fields Used	W1-3	W1-2	W2-4	W3-4
0 to 3	IN	IN	OUT	OUT
4 to 7	OUT	IN	IN	OUT

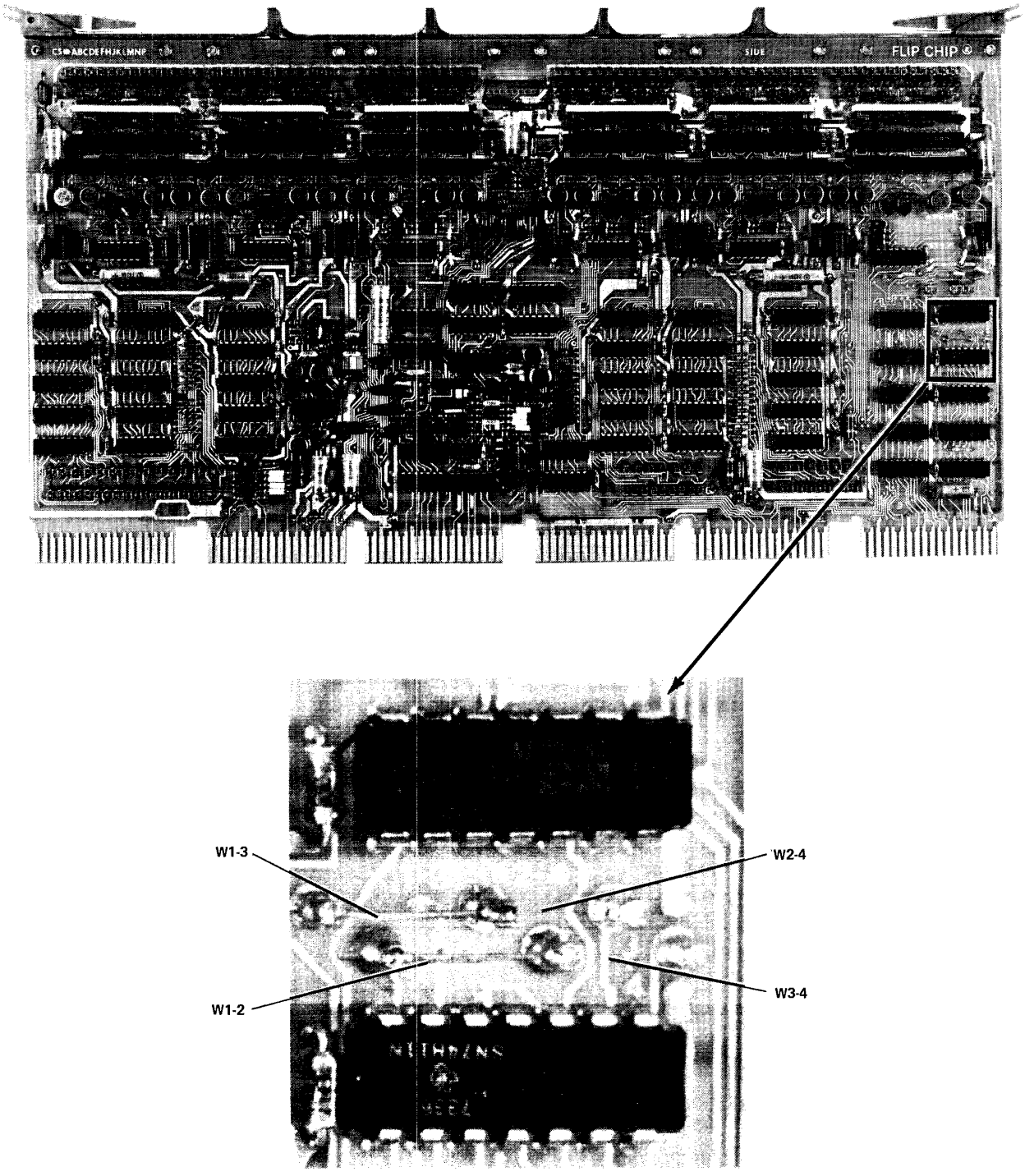


Figure 2-14 MM8-AA Core Memory

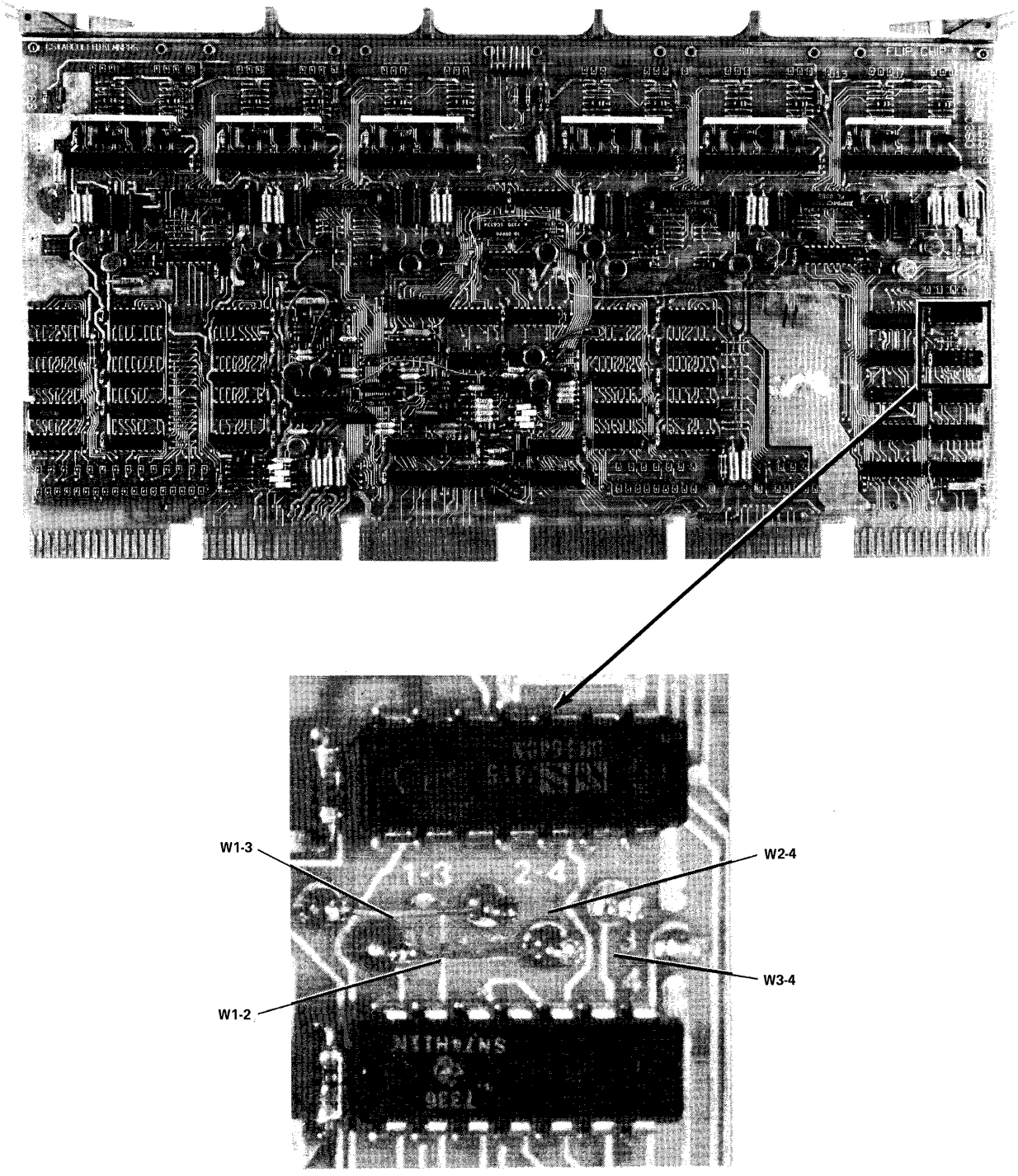


Figure 2-15 MM8-AB Core Memory

2.4.3.6 DKC8-AA I/O Option Board – There are two DKC8-AA hex modules (M8316) in existence; one is defined as etch revision C (shown in Figure 2-16), the other as etch revision D (shown in Figure 2-17). The etch revision is identified on side 2 of the PC board (side 1 is the component side). Lettering similar to the following appears near the lower right corner (when viewing side 2).

Option Board 1
Side 2
M8316
5010900D

The letter D indicates the D etch revision. The information in this section is not totally applicable to each revision level; differences that exist are indicated in the description.

The DKC8-AA combines four options:

1. Serial Line Unit (SLU), 110 to 9600 (50 to 9600 for revision D) baud rate interface for Teletype, VT50, or other compatible serial line unit.

2. Real-time Clock – Crystal controlled at 100 Hz.

3. General Purpose Parallel I/O – 12-bit I/O for user's device or another PDP-8/A.

NOTE

The General Purpose Parallel I/O on the D etch revision of the M8316 module can be used as an interface for the LA180. Data to the LA180 must be supplied in complemented form. The IOTs are different from the LA8 interface designed for the LA180. A BC80-A cable, available from DIGITAL, must be used to connect the General Purpose Parallel I/O (J5) to the LA180.

4. Console Logic – Logic to connect the KC8-AA Programmer's Console to the Omnibus.

NOTE

Revision C: For Teletype (ASR-33) operation without real-time clock software, set switches S1-4, 6, and 8 to the ON position; set switches S1-1, 2, 3, 5, and 7 to the OFF position.

Revision D: For Teletype (ASR-33) operation without real-time clock software, set switches S1-1, 3, 4, 6, 8, and 9 to the ON position; set switches S1-2, 5, and 7 to the OFF position (S1-10 is a spare).

For other operation, set switches as shown in Tables 2-8 and 2-9.

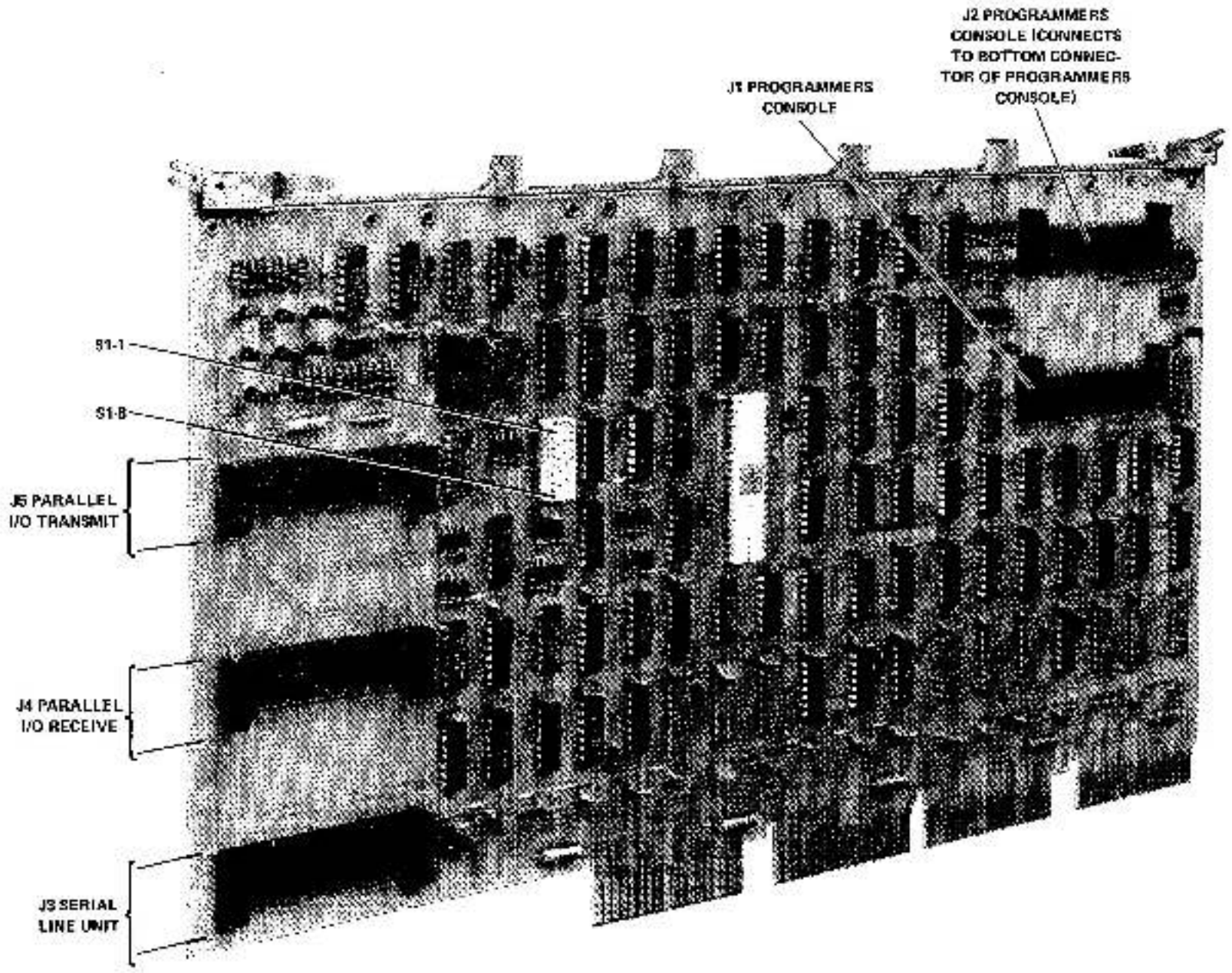


Figure 2-18 DKCB-AA (M8316) I/O Option Board

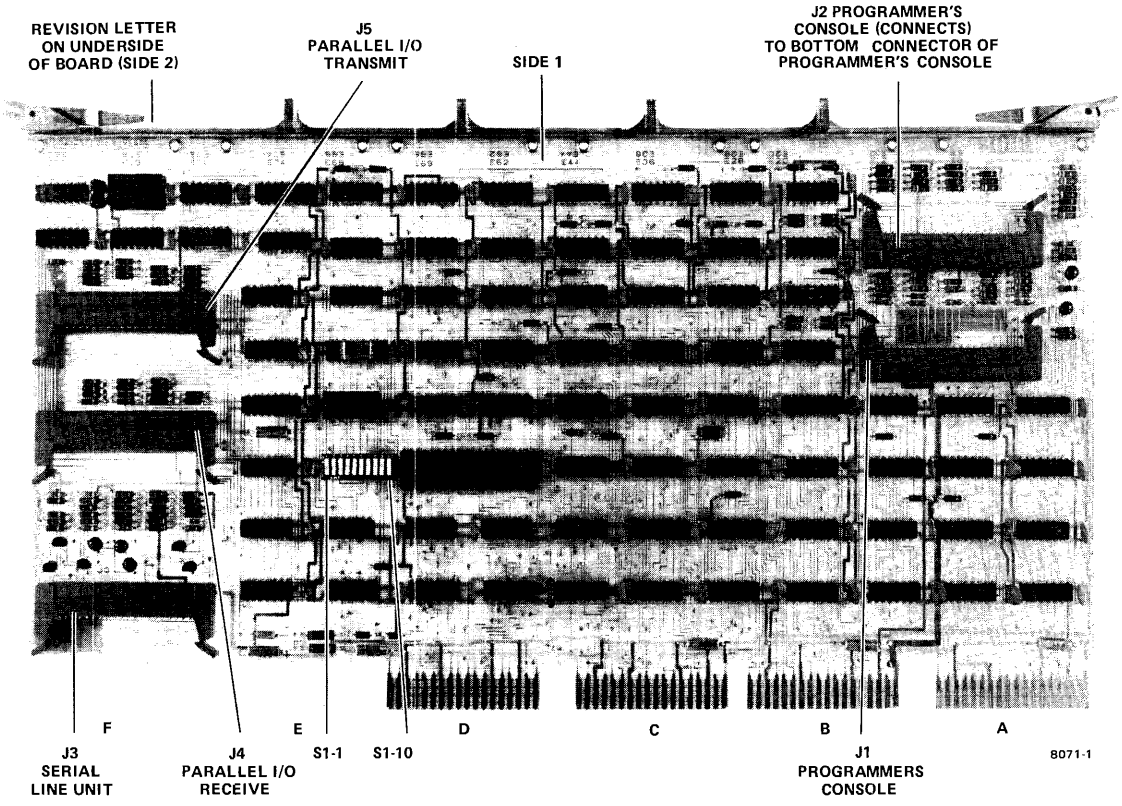


Figure 2-17 D Etch Revision of DKC8-AA (M8316) I/O Option Board

Table 2-8
DKC8-AA I/O Option Board Switch Settings for C Etch Module

Switch	Function
S1-2, 2 and 3	Baud rate as shown below:

S1-1	S1-2	S1-3	Baud Rate
OFF	OFF	OFF	110
OFF	OFF	ON	150
OFF	ON	OFF	300
OFF	ON	ON	600
ON	OFF	OFF	1200
ON	OFF	ON	2400
ON	ON	OFF	4800
ON	ON	ON	9600

S1-4	Clear Data Available at Time State 1 (normally ON)
S1-5	ON enables Real Time Clock
S1-6	Test (normally ON, OFF for special testing)
S1-7	ON for 1 stop bit, OFF for two stop bits
S1-8	ON enables TTY filter in 20 mA CKT (used only for 100 baud)

Table 2-9
DKC8-AA Option Board Switch Settings for D Etch Module

Switch	Function
S1-1, 2, 3, and 4	Baud rate as shown below:

S1-4	S1-3	S1-2	S1-1	Baud Rate
ON	ON	ON	ON	50
ON	ON	ON	OFF	75
ON	ON	OFF	ON	110
ON	ON	OFF	OFF	134.5
ON	OFF	ON	ON	150
ON	OFF	ON	OFF	300
ON	OFF	OFF	ON	600
ON	OFF	OFF	OFF	1200
OFF	ON	ON	ON	1800
OFF	ON	ON	OFF	2000
OFF	ON	OFF	ON	2400
OFF	ON	OFF	OFF	3600
OFF	OFF	ON	ON	4800
OFF	OFF	ON	OFF	7200
OFF	OFF	OFF	ON	9600
*OFF	OFF	OFF	OFF	19.2K

S1-5	ON = Real Time Clock enabled OFF = Real Time Clock disabled
S1-6	ON = Test Switch (always ON)
S1-7	ON = 1 Stop Bit in SLU character OFF = 2 Stop Bits in SLU character
S1-8	ON = ASR/KSR 33 DR35 filter in (across SLU 20 mA REC'V Leads ON if Baud rate is 110 or below) OFF = filter out
S1-9	ON = TS1 clears DATA AVAIL flip-flop in Parallel I/O Section OFF = DATA AVAIL not cleared by TS1

*Serial Line will *not* run at this Baud rate. This setting is *not* to be used.

2.4.3.7 KM8-A Extended Option Board – The KM8-A, shown in Figure 2-18, is a hex module (M8317) combining the following options:

1. Power Fail/Auto-Restart
2. Bootstrap Loaders – Provide commonly used I/O loaders.
3. Memory Extension and Timeshare Control

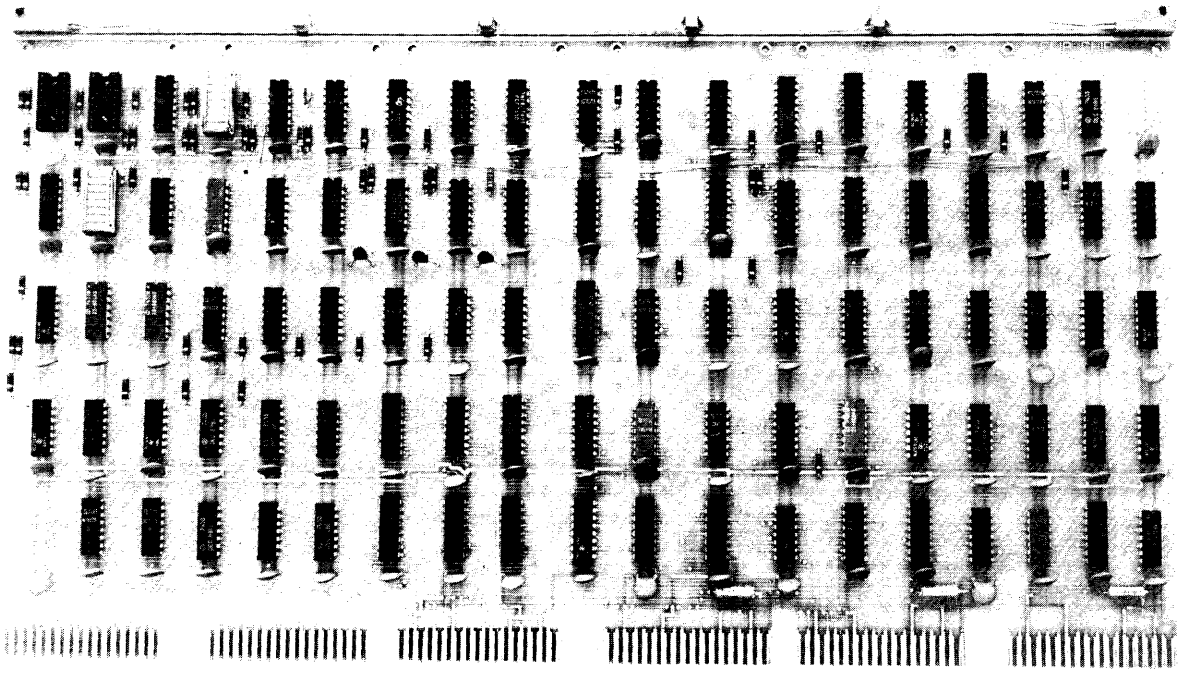
NOTE

If you are using paper tape under control of the bootstrap switches, no Auto-Restart, and timeshare enabled, set the following switches ON: S1-1 through S1-4, S1-8, S2-1, S2-5 through S2-7; set the following switches OFF: S1-5 through S1-7, S2-2 through S2-4, and S2-8.

Other switch settings for the KM8-A are listed in Tables 2-10 through 2-13.

NOTE

There are two types of bootstrap ROM's used on the KM8-A. E82 and E87 have different labels on them for the two different bootstrap ROM's. Modules that have E82 and E87 (Figure 2-18) labeled 87A2 and 88A2 should use Table 2-11 for switch settings. If E82 and E87 are labeled 158A2 and 159A2, use Table 2-12 for switch settings.



7299-1

Figure 2-18 KM8-A (M8317) Extended Option Board

Table 2-10
Auto-Restart Select Switch Settings

Restart Address	S2-2	S2-3	S2-4
0	OFF	OFF	OFF
200	OFF	ON	OFF
2000	ON	OFF	OFF
4200	ON	ON	OFF

Table 2-11
Bootstrap Select Switch Settings
(for ROMs Labeled 87A2 and 88A2)

Program	S2-5	S2-6	S2-7	S2-8	S1-1	S1-2	S1-3	Memory Address
*HI-LO RIM	ON	ON	ON	OFF	ON	ON	ON	7737
*RK8-E	ON	OFF	ON	OFF	ON	OFF	ON	0024
*TC08	ON	OFF	OFF	ON	OFF	ON	ON	7613
*RF08/DF32D	OFF	ON	ON	ON	ON	OFF	OFF	7750
*TA8-E	OFF	ON	ON	OFF	ON	OFF	OFF	4000

*May only be used with 4K of Read/Write Memory in field 0.

Table 2-12
Bootstrap Select Switch Settings
(for ROMs Labeled 158A2 and 159A2)

Program	S2-5	S2-6	S2-7	S2-8	S1-1	S1-2	S1-3	Memory Address
HI LO RIM	ON	ON	ON	OFF	ON	ON	ON	7737
RK8-E	ON	OFF	ON	OFF	ON	OFF	ON	0024
RX8-E	ON	OFF	OFF	ON	OFF	ON	ON	0033
RF08/DF32D	OFF	ON	OFF	ON	OFF	ON	OFF	7750
TA8-E	OFF	ON	OFF	OFF	OFF	ON	OFF	4000

Table 2-13
Bootstrap/Auto-Restart Switch Settings

Feature	Start Switch or Activating Signal	S1-6	Switches S1-7	S1-8
Bootstrap Enabled and Auto-Restart Disabled	BOOT Key	OFF	OFF	ON
Bootstrap Enabled and Auto-Restart Enabled	BOOT Key or AC OK*	ON	ON	ON
Bootstrap Disabled and Auto-Restart Enabled	AC OK*	ON	ON	OFF
Bootstrap Enabled and Auto-Restart Disabled	AC OK*	ON	OFF	OFF
Bootstrap Enabled and Auto-Restart Disabled	AC OK* or BOOT Key	ON	OFF	ON
Bootstrap and Auto-Restart Disabled		OFF	OFF	OFF
		S2-1		
Timeshare Enabled		OFF		
Timeshare Disabled		ON		
		S1-4		
Bootstrap Activated in Run or Stopped State		OFF		
Bootstrap Activated in Stopped State Only		ON		
Not Used		S1-5		

*Starts if power voltage becomes adequate.

2.4.3.8 Semiconductor Memory Power Supply – The Semiconductor Memory Power Supply can supply 20 A at +5 V. It will support only semiconductor memory (RAM and ROM). The G8016 regulator (Figure 2-18) plugs into a dedicated backplane slot near the bottom of the chassis. The power supply has battery backup for power failures. The machine will be totally supported for approximately 30–40 seconds after an ac line failure.

NOTE

All PDP-8/A Power Supply dc voltages are provided to drive logic inside the basic chassis. DIGITAL is not responsible for the performance of the PDP-8/A if any dc power is used outside the PDP-8/A chassis.

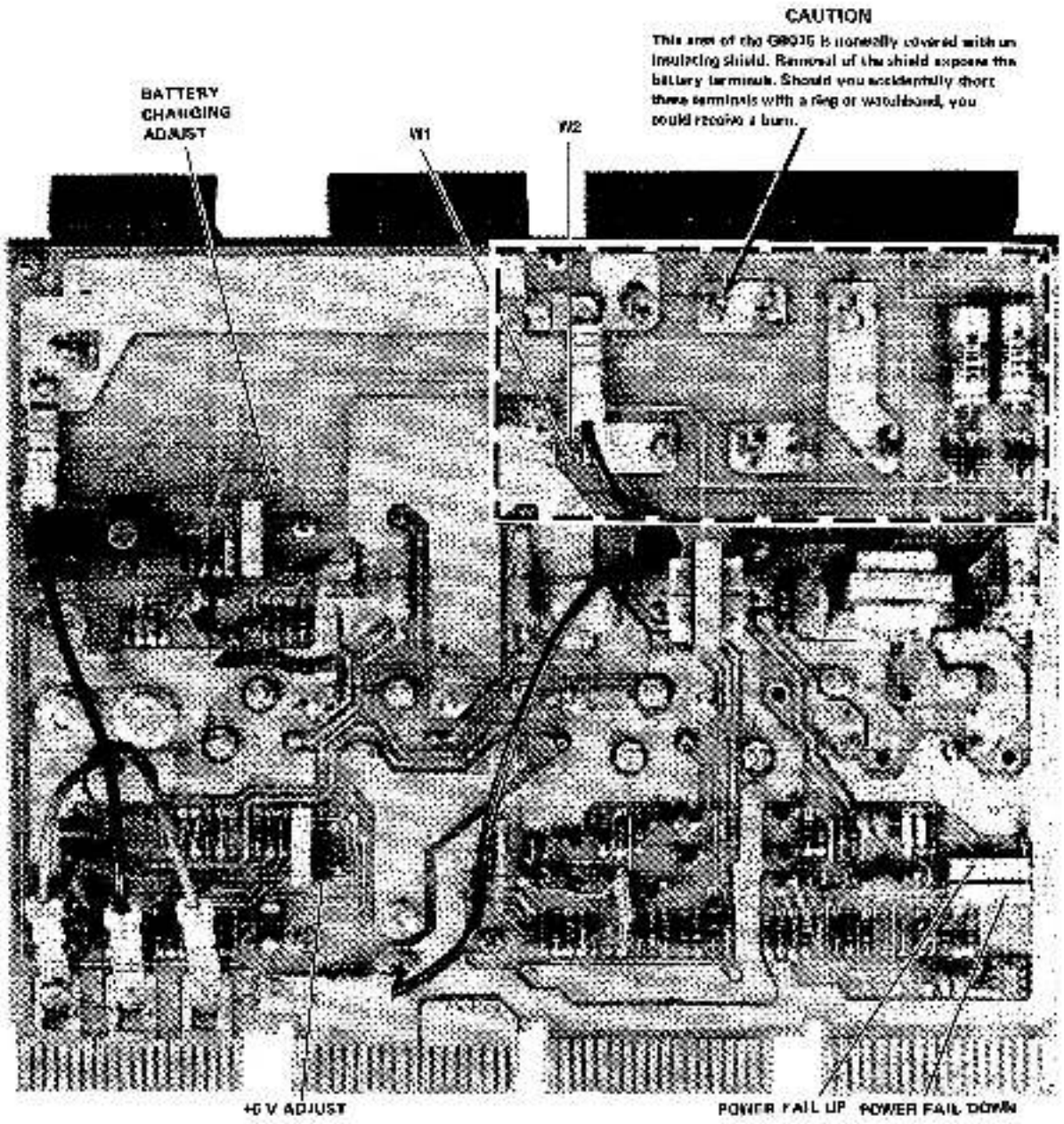


Figure 2-19 Semiconductor Memory Regulator Board (G8016)

NOTE

To enable control of the PDP-8/A power from the ON-OFF Switch, set the MASTER/SLAVE switch to the MASTER (to the right) position. (The switch is identified in Figure 2-5.)

In the 8A computers the MASTER/SLAVE switch is mounted on the printed circuit board that includes the ON/OFF, PANEL LOCK, and BOOT switches. This board is attached to the rear of the Limited Function Panel; remove the panel to gain access to the MASTER/SLAVE switch. The switch is illustrated in Figure 2-20; if is shown in the MASTER position (to the right when viewing the front of the switch).

2.4.3.9 Core Memory Power Supply Regulator – The core memory power supply supplies the following voltages at the currents specified:

+5 V @ 25 A
–5 V @ 2 A
+15 V @ 2 A
–15 V @ 2 A
+20 V @ 4 A

It will support core memory. The G8018 regulator (Figure 2-21) plugs into a dedicated backplane slot near the bottom of the chassis. (The board slot is pictured in Figure 2-7).

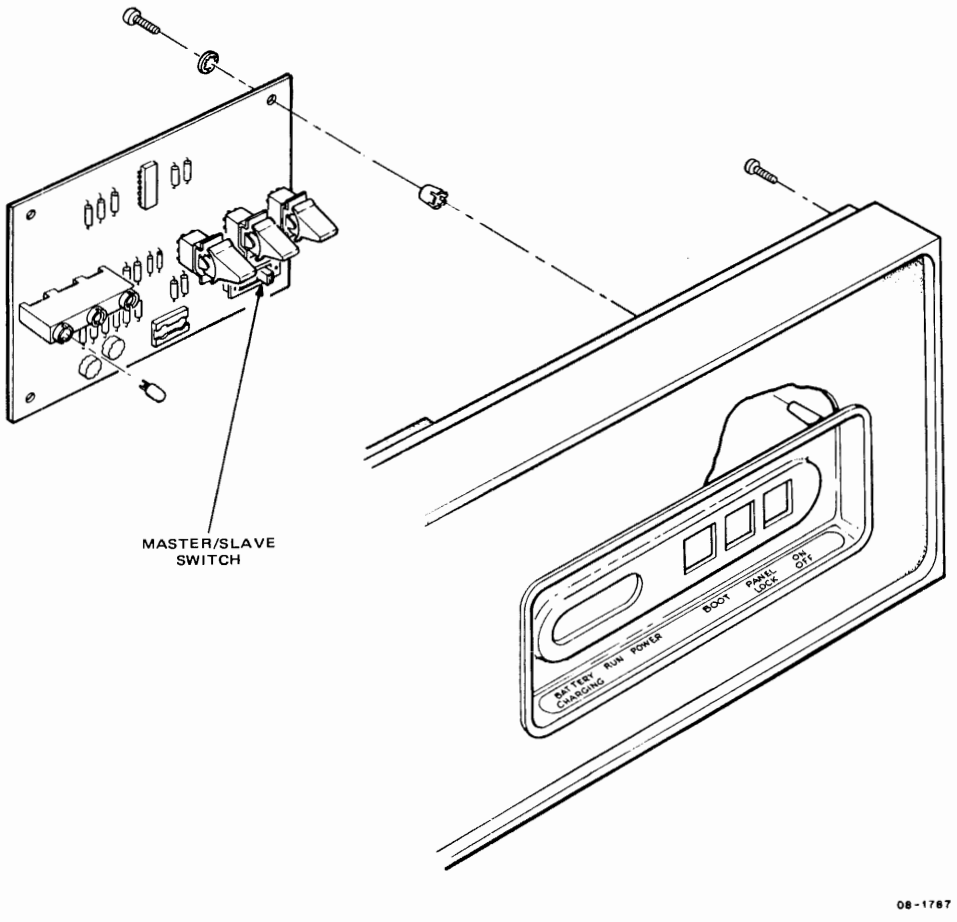


Figure 2-20 8A MASTER/SLAVE Switch

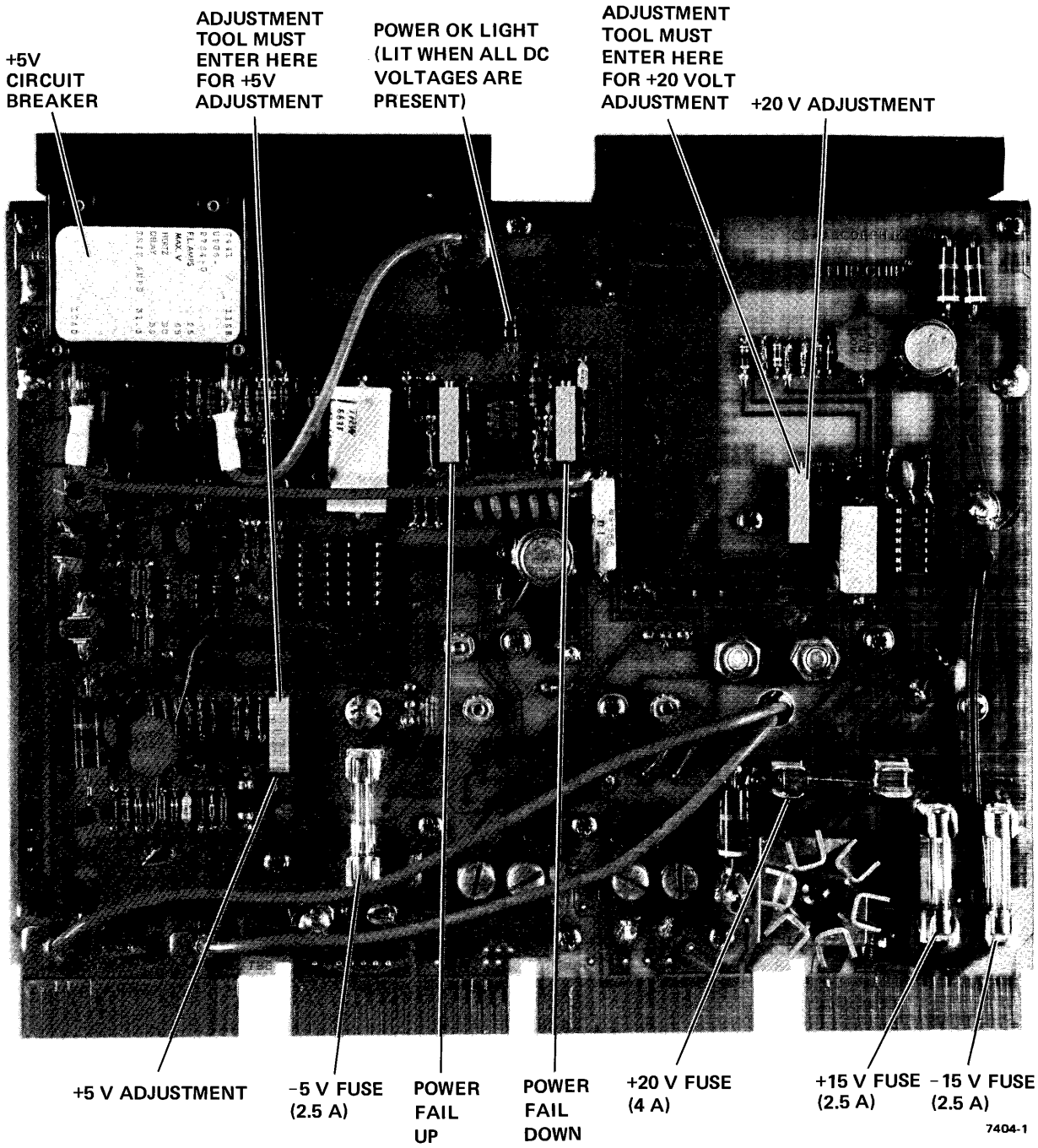


Figure 2-21 G8018 Core Memory Regulator Board

2.4.3.10 Limited Function Panel (Figure 2-22) – The Limited Function Panel has three external switches and three indicator lights (the MASTER/SLAVE switch is mounted in the rear of the panel for 8A computers).

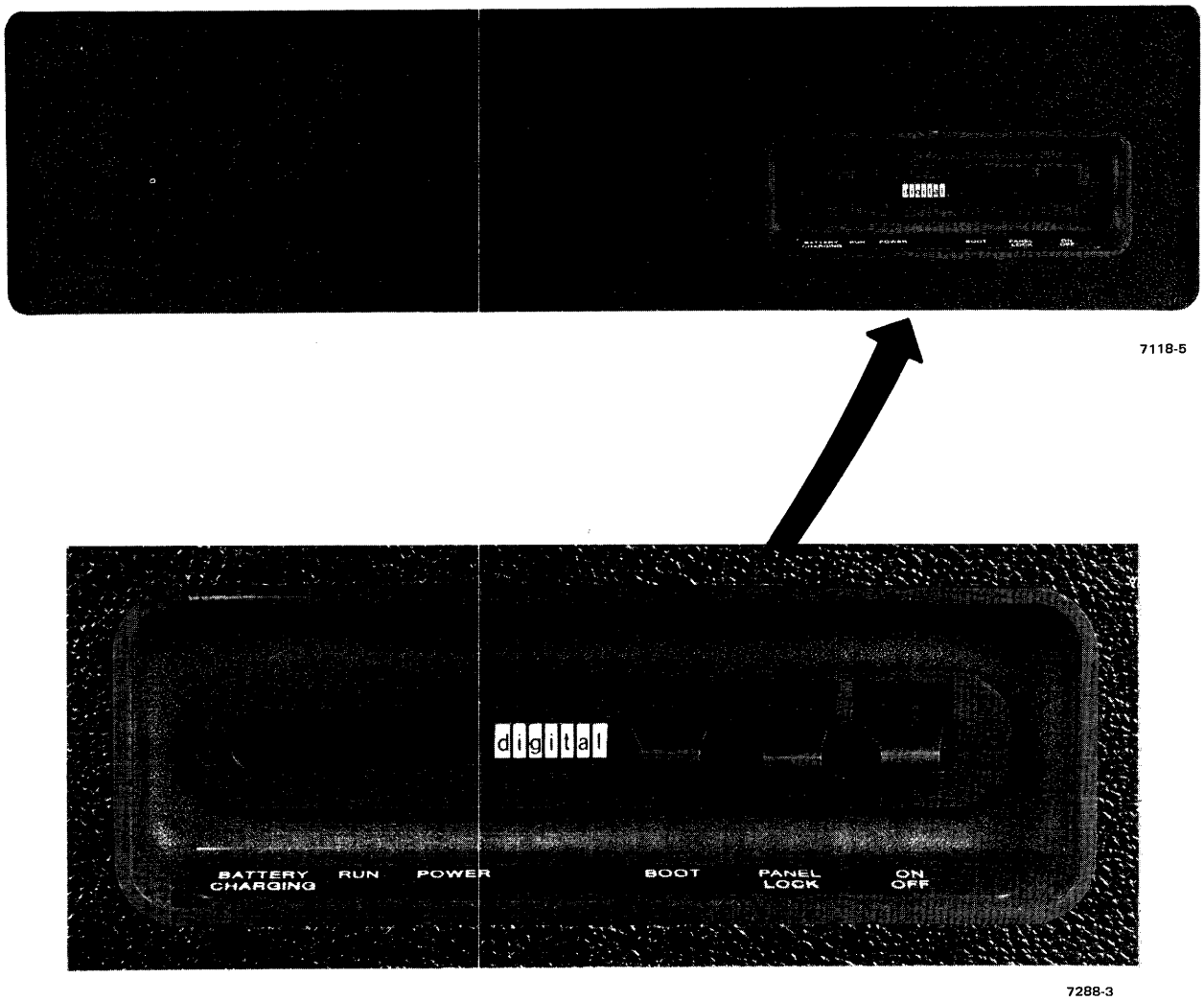


Figure 2-22 Limited Function Panel

Lights

1. POWER light indicates the PDP-8/A is operating on ac power.

2. RUN light indicates the PDP-8/A RUN flip-flop is set.

3. The BATTERY CHARGING light indicates either that the power supply battery is being charged (PDP-8/A semiconductor computer) or that both G8018 regulators are operating properly (8A420, 8A620, and 8A820 computers). The light is present on the 8A400, 8A600, and 8A800 computers, but is not used.

Switches

1. ON-OFF switch turns ac power on in the up position (this switch will not turn battery power on unless ac is present). Turn power off before removing the power cord from the wall receptacle. Otherwise the PDP-8/A will run on battery power for as long as the battery lasts.

2. On those systems having a Programmer's Console, the PANEL LOCK switch disables the following switches: HLT/SS, E NEXT, E THIS, D THIS, D NEXT, LA, LXA, INIT, BOOT, and RUN. The down position activates the Programmer's Console; the up position panel-locks the console.

3. The BOOT switch initiates the bootstrap function (if it is enabled) on the KM8-A Extended Option Board (M8317). It is normally left in the down position. This BOOT switch is not affected by PANEL LOCK.

2.4.3.11 KC8-AA Programmer's Console (Figure 2-23) – The Programmer's Console has seven-segment LED displays of the Extended Memory Address (EMA). Memory Address (MA), and the Status Register. The console can be located up to 15 feet from the PDP-8/A. Two BCO8R cables connect the console to the M8316 module (J1 and J2).

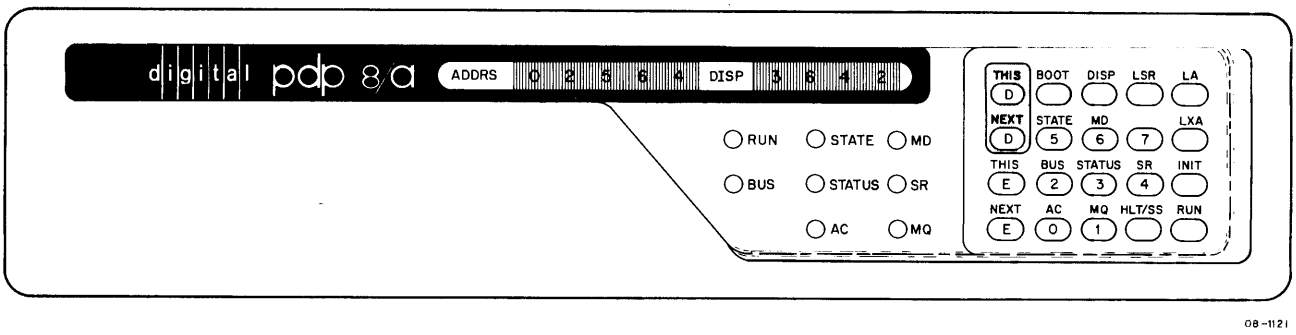


Figure 2-23 KC8-AA Programmer's Console

2.5 INSTALLING THE PDP-8/A AND TURNING POWER ON FOR THE FIRST TIME

2.5.1 Environmental and Power Requirements

Recommended operating conditions for the PDP-8/A are an ambient temperature of 5° to 50° C (41– 122° F) and a noncondensing relative humidity of 10–95%. Voltage requirements are 90–132 Vac single phase (using approximately 3.2 A), or 180–264 Vac single phase (using approximately 1.6 A). Line frequency may be 49–51 Hz or 59–61 Hz, depending on the power transformer used in the power supply. Check the label at the rear of the computer to determine the correct voltage and frequency.

WARNING

Be sure that the ac outlet provides a non-current-carrying ground.

2.5.2 Turning on the Computer for the First Time

After unpacking the computer, allow at least 30 minutes for the machine to stabilize to ambient temperature before applying power. This time should be increased to one hour or longer when the difference between storage or shipping temperature and the operating ambient temperature exceeds 30° F (17° C).

Install the equipment using the following procedure:

1. Check switch settings on all modules. (See instructions in Paragraph 2.4.3).

2. Ensure that the regulator circuit breaker is ON. (The breaker is pictured in Figure 2-6.)

3. Turn OFF the ON/OFF switch on the Limited Function Panel (Figure 2-22).

4. Ensure that all ac power is received from the same branch circuit if the system has more than one power cord.

5. Plug in the power cord. If a power control is used, plug the power cord into the receptacle marked UN-SWITCHED AC.

WARNING
Do not touch the computer after plugging it in until proper grounding has been checked.

6. Before touching the computer, check frame to ground voltage to ensure that less than 10 Vac is present.

7. Without touching any metal part of the PDP-8/A, turn the power ON/OFF switch ON.

8. Repeat step 6. In case of difficulty, have an electrician check the socket into which the computer has been connected (electrical connections are illustrated in Figure 2-24). If no difficulty is encountered, the computer frame is properly grounded and there is no danger in touching it.

9. Power is now applied to the PDP-8/A. The fans should be running and the BATTERY CHARGING light should light momentarily or stay on. (The light is not used in the H9300 chassis assembly.) If none of these occur, check the MASTER/SLAVE switch (Paragraph 2.4.3.8). Turn the power OFF before checking the MASTER/SLAVE switch. This switch should be in the MASTER (to the right) position. Then turn the power ON. If the condition still exists, refer to the basic maintenance section in Paragraph 2.10.

10. Turn the PDP-8/A power switch OFF and the Teletype LINE/OFF/ LOCAL switch to the OFF position.

11. Connect the Teletype signal cable to the short cable (DEC Part No. BC05M-1F, plugged into J3 of the M8316) in the PDP-8/A. The cable connectors are keyed for proper mating.

12. Plug the Teletype into the same ac outlet as the PDP-8/A.

13. Turn power ON/OFF switch on the PDP-8/A to ON.

14. Turn the Teletype LINE/OFF/LOCAL switch to LINE. Only the hum of the running motor of the Teletype and the PDP-8/A fans should be heard.

2.6 TESTING PDP-8/A WITHOUT PAPER TAPE DIAGNOSTICS

The procedures in this section are used to test the PDP-8/A computer from the Programmer's Console. No paper tape diagnostic programs are required for these tests.

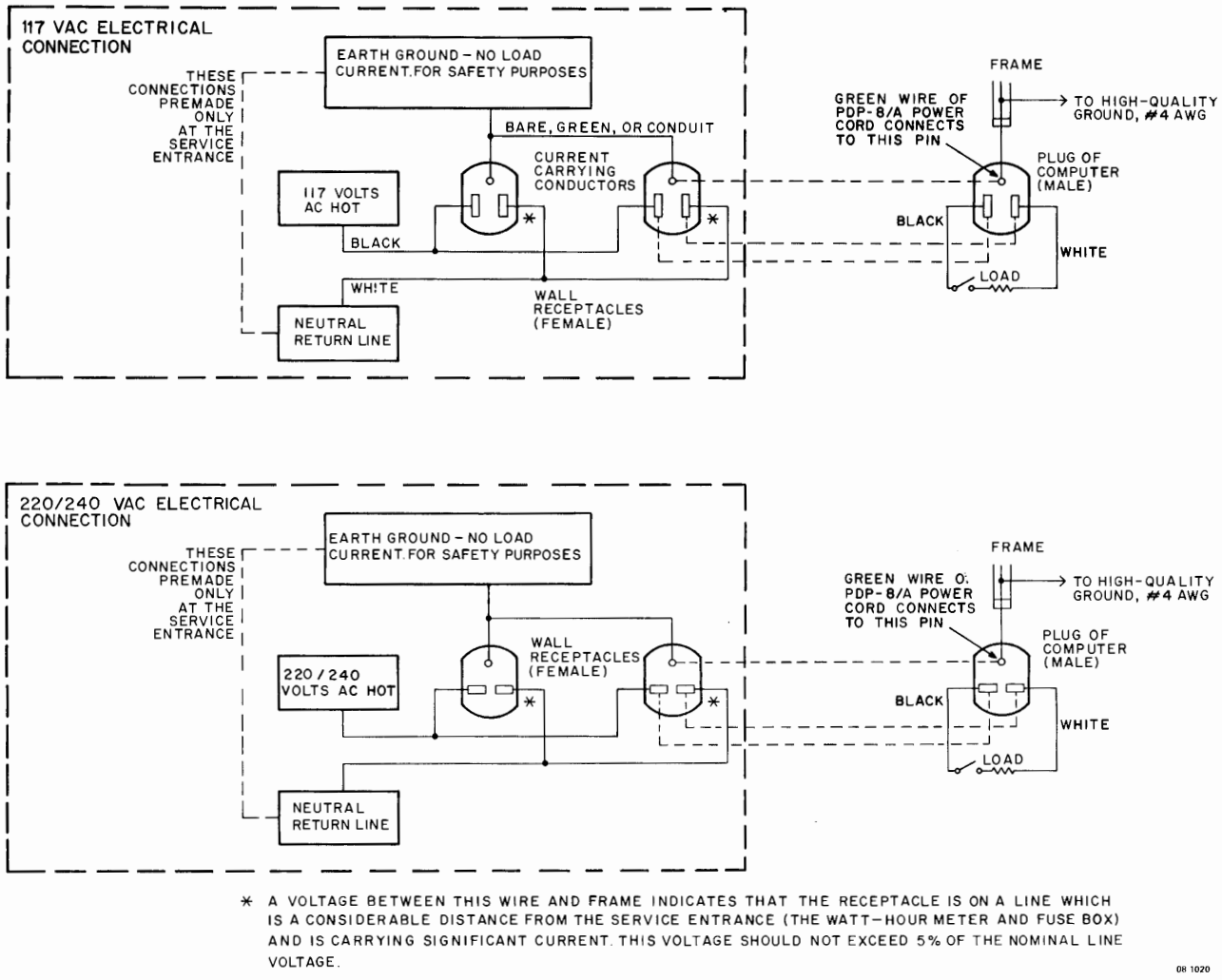


Figure 2-24 PDP-8/A Electrical Connections

2.6.1 Programmer's Console

The Programmer's Console is shown in Figure 2-23 and is fully described in the *PDP-8/A Miniprocessor Handbook* and in Paragraph 1.2. Its use in testing the PDP-8/A is described in detail in the paragraphs that follow.

2.6.2 Central Processor Test Routines

When no MAINDECs are available, small routines may be keyed into memory and run to check PDP-8/A operation. These tests will not completely check out a PDP-8/A, but will find the most common failures. All routines start at address 0200. If any failures occur, carefully examine each instruction of the routine. If the instructions are correct, switch power off and check all of the module switch settings (all memory contents are lost when power is switched off and the routines must be reloaded). If the routine is not entered properly, re-enter the routine and try to run it again.

These routines are also useful when MAINDEC programs cannot be loaded because of a hardware problem.

2.6.3 Entering Test Routines from the Programmer's Console

The following procedure should be used to run Routine 1, the first PDP-8/A test:

1. Press, in order, MD, DISP – this will let you see what you deposit.
2. Press, in order, 0 0 0 0 LXA – select memory field 0
3. Press, in order, 0 2 0 0 LA – start loading instructions at address 200.
4. Press, in order, 7 0 0 1 D NEXT – deposit an instruction.
5. Press, in order, 2 3 0 0 D NEXT – deposit an instruction.
6. Press, in order, 5 2 0 1 D NEXT – deposit an instruction.
7. Press, in order, 5 2 0 0 D NEXT – deposit an instruction.
8. Press, in order, 0 2 0 0 LA – now get ready to start at location 200.
9. Press, in order, AC, DISP – Do this to see the accumulator (AC).
10. Press, in order, INIT and RUN – start the program.

All other routines should be entered into memory using this procedure.

NOTE

If you make a mistake while you are entering a number, and you have not pressed D NEXT, LA etc., you can correct the entry by re-entering the entire number. The number appearing in the DISP indicator is the entry that the PDP-8/A will use.

2.6.4 Central Processor Test Routines

The following routines should be used to check the CPU:

Routine 1

This program will increment the AC slowly so that the user can see that it is working. The internal numbering system of the PDP-8/A does not use 8 and 9.

```
0200    7001    /Increment the AC by 1 – start here.
0201    2300    /Increment a location and skip if it is zero.
0202    5201    /Jump back 1.
0203    5200    /Start program over again.
```

Routine 2

This routine should print a pattern of all printable characters. Omit this routine if your PDP-8/A is not equipped with a Teletype, or similar terminal.

NOTE

Ensure that the Teletype is set to LINE for routines 2 and 3.

The following line will print out while this routine is running. Characters may or may not be printed after the letter Z, depending on the column width of the terminal. These extra characters should be disregarded. Disregard the first line printed.

! #$%&'()*+,-./0123456789:;<=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ (Random Characters)

```
0200    7001    /Increment the AC by 1 – start here.
0201    6046    /Transmit.
0202    6041    /Am I done transmitting?
0203    5202    /No I am not done transmitting.
0204    5200    /Yes I am done. Jump back and start over.
```

Routine 3

This routine will print what is typed on the terminal (echo characters). Type several lines of sentences, making sure the terminal prints out what you type. Omit this step if your PDP-8/A is not equipped with a terminal.

```
0200    6031    /Has a key been pressed?
0201    5200    /No, go back and wait.
0202    6036    /A Key was hit, Read it.
0203    6046    /Transmit the character to the printer.
0204    6041    /Am I done printing?
0205    5204    /No. Go back one.
0206    5200    /Yes I am done. Let's go back to wait for another key.
```

Routine 4

The following program checks some of the operate instructions. The program should halt at location 00216 (ADDRS should read 00217) with the AC cleared. (AC=0000)

```
0200    7240    /Clear the AC, then complement the AC.
0201    7001    /Increment the AC by 0202.
        7640    /Skip if AC=0, then clear the AC.
0203    7402    /Error halt. Computer should not halt here.
0204    7120    /Set the link to 1.
0205    7010    /Rotate the AC right one. The AC should then equal 4000.
0206    7510    /Skip if the AC bit 0=0.
0207    7410    /Skip unconditionally.
0210    7402    /Halt. Computer should not halt here.
0211    7001    /Increment the AC by one.
0212    7002    /Byte swap, AC should equal 0140.
0213    1202    /Add 7640 to 0140.
0214    7420    /Skip if link equals 1.
0215    7402    /Halt on error.
0216    7402    /Good halt if AC = 0000.
```

Routine 5

The following routine tests the ISZ instruction. The program should halt at location 00207 (ADDRS should read 00210) with AC cleared (AC=0000). To read the AC, press AC and then the DISP button.

```
0200    7500    /Clear the AC and link.
0201    3300    /Store 0 in location 300.
0202    7001    /Index the AC.
0203    2300    /Index location 300.
0204    5202    /Jump back and do again.
0205    7440    /Done check if AC = 0000.
0206    7402    /Error (AC and location 300 should be zero).
0207    7402    /Good halt.
```

Routine 6

This routine tests the JMS instruction. This routine should halt with ADDRS = to 00215 with the AC cleared (AC=0000). To read the AC, press AC and then the DISP button.

```
0200    7300    /Clear the AC and link.
0201    3300    /Zero Pass counter.
0202    3204    /Zero entry.
0203    4204    /JMS to subroutine.
0204    0000    /Return address written here.
0205    1204    /Get return address.
0206    7041    /Complement and index the AC.
0207    1215    /Add to known good return address.
0210    7440    /Skip on 0 AC.
0211    7402    /Error halt.
0212    2300    /Increment Pass counter.
0213    5202    /Do again.
0214    7402    /Good halt.
0215    0204    /Constant.
```

Routine 7

This routine tests the Jump instructions. The program should halt at location 00214 (ADDRS should read 00215). Run this test twice.

```
0200    5210    /Jump 210.
0201    7402    /Error halt.
0201    5206    /Jump 206.
0203    7402    /Error halt.
0204    5212    /Jump 212.
0205    7402    /Error halt.
0206    5204    /Jump 204.
0207    7402    /Error halt.
0210    5202    /Jump 202.
0211    7402    /Error halt.
0212    2300    /Loop to do this program 4096 times.
0213    5200    /Start program over again.
0214    7402    /Good halt after 4096 passes.
```

2.7 LOADING THE RIM AND BINARY LOADERS

Programs in binary format may be used in machines with 4K or more of Read/Write Memory. The RIM loader must be used to load the Binary Loader. The Binary loader is then used to load a program in binary format.

The RIM and Binary Loaders reside in the highest 1K of a 4K memory. Machines with less than 4K of memory require the RIM loader to be loaded at addresses in the lowest 1K of memory. Use of the Binary Loader on machines with less than 4K of Read/Write memory is not recommended because of the length of the Binary Loader routine. Each test procedure will tell you where to load the RIM loader.

2.7.1 Loading the RIM Loader

The RIM Loader is a 17-instruction program needed to load the Binary Loader and other RIM formatted tapes. There are two methods of loading the RIM loader: Manually loading each instruction through the Programmer's Console keys (described in the next few paragraphs), and using the bootstrap option, if there is 4K or more of Read/Write memory and the KM8-A Extended Option Board (M8317) is in the computer. If you use the second method, turn to Paragraph 2.7.3.

Enter RIM Loader through the Programmer's Console keys as follows:

Press keys from left to right as ordered in the following steps (1 through 22).

1.	MD	DISP	/Enables memory data to the readout display
2.	0000	LXA	/Sets instruction and Data field to 0
3.	XXXX	LA	/ADDRS should read the 0XXXX value, see the bottom of this table for the value of XXXX.
4.	6032	D NEXT	/DISP should read 6032
5.	6031	D NEXT	/DISP should read 6031
6.	5357	D NEXT	/DISP should read 5357
7.	6036	D NEXT	/DISP should read 6036
8.	7106	D NEXT	/DISP should read 7106
9.	7006	D NEXT	/DISP should read 7006
10.	7510	D NEXT	/DISP should read 7510
11.	5357	D NEXT	/DISP should read 5357
12.	7006	D NEXT	/DISP should read 7006
13.	6031	D NEXT	/DISP should read 6031
14.	5367	D NEXT	/DISP should read 5367
15.	6034	D NEXT	/DISP should read 6034
16.	7420	D NEXT	/DISP should read 7420
17.	3776	D NEXT	/DISP should read 3776
18.	3376	D NEXT	/DISP should read 3376
19.	5356	D NEXT	/DISP should read 5356
20.	0000	D NEXT	/DISP should read 0000
21.	0000	D NEXT	/DISP should read 0000
22.	XXXX	LA	/ADDRS should be 0XXXX*

*XXXX If you have a 4K RAM, enter 7756. If you have less than 4K of RAM, enter 0156 for loading all tests except version A of the MS8-A test (Enter 1756 for this case only).

2.7.2 Checking the RIM Loader

After completing the RIM loader procedure, the program may be checked by repeating the first three steps and pressing E NEXT. Each time E NEXT is pressed, the next four digits of the program should appear in the DISP lights. When you are sure RIM loader is in memory correctly, proceed to the Binary Loader procedure, or load and run RIM format MAINDECs (Paragraph 2.8) if you have less than 4K of read/write memory in your system.

2.7.3 Loading the Binary Loader

NOTE

Do not use the Binary Loader procedure if the memory size is less than 4K.

1. Place the tape labeled Binary Loader (DEC-08-LBAA-PM) in the Teletype reader, with the START/STOP/FREE lever set to FREE. Position the tape so that the printed arrow on the tape points toward you, and the single row of data holes at the beginning of the tape is over the read head (Figure 2-25).

2. Ensure that the LINE/OFF/LOCAL switch of the Teletype is set to LINE, and the papertape reader's START/STOP/FREE lever is set to the START position (Figure 2-26).

3. If the KM8-AA Extended Option Board (M8317) is not available, the RIM loader must be loaded at this time using the RIM loading procedure (Paragraph 2.7.1).

4. If the RIM loader was keyed in manually, press (in order) 7756, LA, INIT, and RUN. The RUN light should be on. The Teletype reader should be reading tape.

5. If the KM8-AA Extended Option Board (M8317) was set up for Hi-Lo RIM, ensure that the BOOT switch on the Limited Function Console is down; then press the BOOT key on the Programmer's Console twice. The RUN light should go on and the Teletype reader should read tape.

6. If the tape fails to read in or stops before the end of tape, reload the RIM loader using the RIM Loader procedure (Paragraph 2.7.1).

7. After the tape is read to the trailing single row of data holes, press the HLT/SS key. The reader should stop reading tape. The Binary Loader should now be in memory.

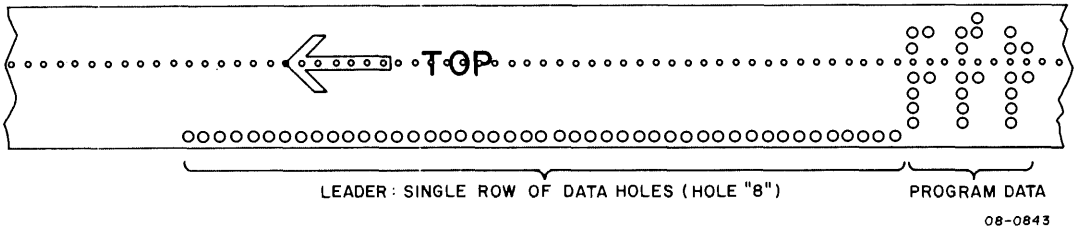


Figure 2-25 Paper Tape Leader

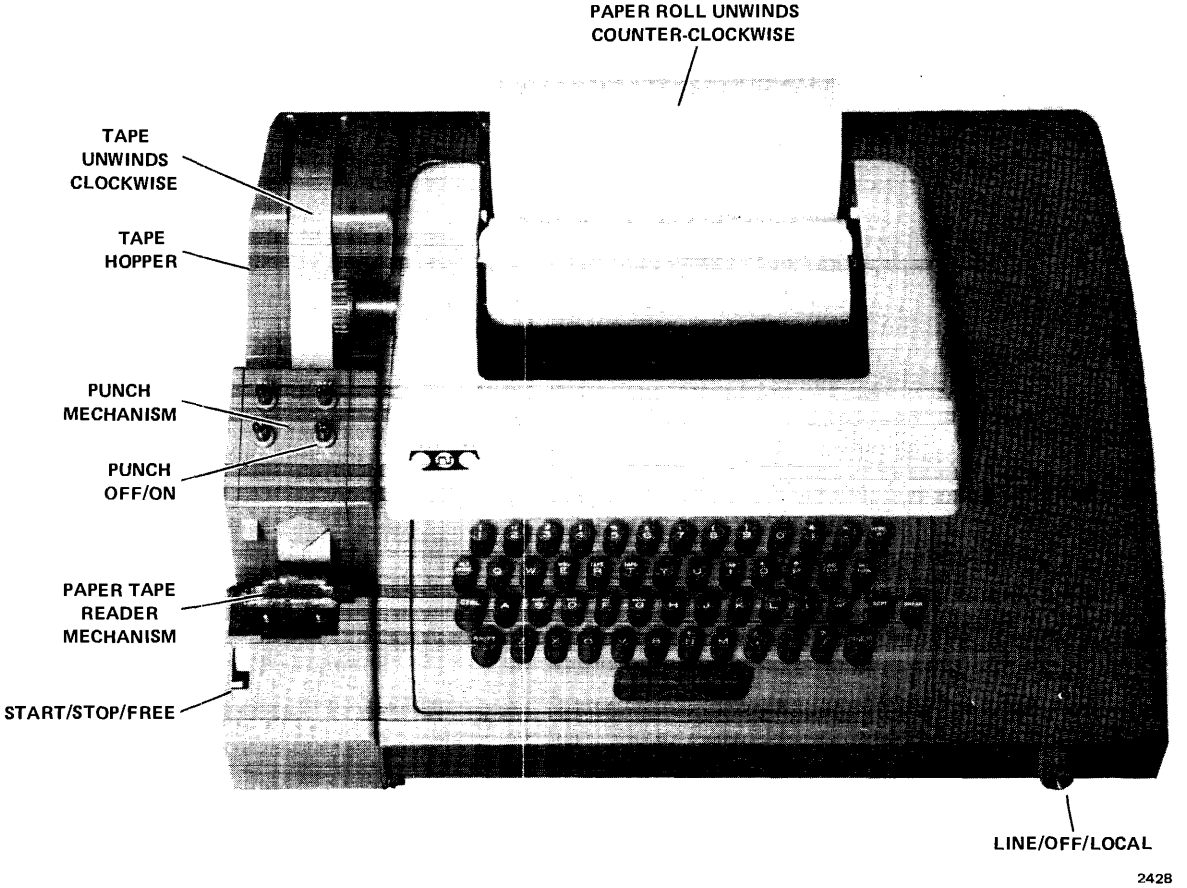


Figure 2-26 LT33 Teletype Controls

2.7.4 Loading Binary Formatted Paper Tapes

1. Press (in order) 7777, LA, MD, DISP and E THIS. The DISP register should read 5301. If it does not, check the RIM Loader and reload the Binary Loader.

2. If the content of address 07777 was 5301, press 7777, LA, and LSR.

3. Place the binary formatted paper tape in the reader, with the single row of data holes over the read head.

4. Place the Teletype LINE/OFF/LOCAL switch to LINE.

5. Place the reader switch in the START position.

6. Press (in order) INIT, then RUN. The reader should start reading tape.

7. The Programmer's Console RUN light should go out when the first bit of trailer (row of single data holes at the end of tape) is over the read head. The reader should automatically stop. Move the reader lever to STOP or FREE.

8. Press (in order) AC, then DISP. The DISP register should read 0000. If the DISP register does not equal 0000, the tape must be reloaded.

9. Now the program is ready to run.

2.8 TESTING THE PDP-8/A USING MAINDEC DIAGNOSTIC PROGRAMS

MAINDECs are test programs designed to test the KK8-A or KK8-E CPU, the DKC8-AA I/O Option Board, the KM8-A Extended Option Board, and read/write memory. The minimum PDP-8/A system that can be tested with MAINDEC programs consists of a box, an Omnibus, a power supply and the following options:

Option	Description
KK8-E or KK8-A	CPU
DKC8-AA	I/O Option Board
KC8-AA	Programmer's Console
LT33-D	ASR-33 Teletype

with at least 1K of Read/Write memory starting in location 0000 of field 0.

The PDP-8/A read/write memory can be any of the following:

Memory	Size, Type
MS8-AA	1K Semiconductor
MS8-AB	2K Semiconductor
MS8-AD	4K Semiconductor
MM8-AA	8K Core
MM8-AB	16K Core

If your machine has a MR8 Read-Only Memory, you should consult your local Field Service representative before attempting to run MAINDECs.

2.8.1 Central Processor Unit (CPU) Test

The Central Processor Test is a good overall test of the PDP-8/A. It is recommended that this test be the only one run unless specific problems are encountered.

The CPU Test checks the CPU for proper operation. The program first checks the HALT instruction (that's why the program stops at step 7); then tests the remaining instructions.

Two variations of the CPU test exist. One of these variations applies if the PDP-8/A has 4K or more of Read/Write memory; the other, if it has less than 4K. In the steps below, the steps which are memory-size-dependent are enclosed in boxes. You should enter the information or perform the operation indicated for your memory configuration (refer to sticker on the back of the PDP-8/A).

1. Load RIM Loader (see Paragraph 2.7.1), starting with one of the following addresses:

   >or=4K: 7756
   <4K: 0156

2. >or=4K: Load Bin Loader (See Paragraph 2.7.3)
   < 4K: Skip this step

3. Place "PDP-8/A CPU Test" in paper-tape reader. Ensure that the header/trailer code (hole "8") is over the read head. Tape number is:

   >or=4K: MAINDEC-08-DJKKA-PB
   < 4K: MAINDEC-08-DJKKA-PM1.

4. Run the appropriate loader.

   >or=4K: Press 0000 and LXA.
   Press 7777 and LSR.
   Press 7777 and LA.

   < 4K: Press 0156 and LA.

   Press INIT.
   Press RUN.
   Tape will read into memory.

   >or=K: Tape will stop automatically. Press AC, DISP. DISP indicators should equal 0000.

   < 4K: Tape must be stopped when trailer is reached. Press HLT/SS.

5. Set up location 0021 in the program as follows:

   Press 0021 then LA.
   Press 4000 then D THIS.

6. Start Program as follows:

   Press 0000 then LSR.
   Press 0200 then LA.
   Press INIT.
   Press RUN.

7. Program will stop (RUN lght will go off) with ADDRS = 00222. Press STATUS and then DISP.

   DISP indicators should equal 4000.
   Press AC, then DISP.
   DISP indicators should equal 7777.

8. Press RUN. Allow program to run for 10 minutes. If no errors are detected the program will not halt.

9. While program is still running, press any key on the Teletype.

   Program should halt.

2.9 ADDITIONAL DIAGNOSTIC TESTS

These programs should be run to isolate specific problems. It is not recommended that they be run as a periodic confidence check.

2.9.1 Memory Test

The MS8-A MOS Memory Test checks all locations in memory field 0 for proper operation. It relocates itself in memory and tests all of memory not occupied by the program. This test assumes that the CPU is functioning correctly.

1. Load RIM Loader (see Paragraph 2.7.1), starting with address:

   >or=4K: 7756
   <4K: 0156*

*Use 1756 if the tape is the A revision (MAINDEC-08-DJMSA-A-PM). The revision letter is the single letter just before the final PM.

2. Place tape labeled "1-4K MS8-A MOS Memory Test" (MAINDEC-08-DMSA-A-PM) in the paper-tape reader.

3. Run RIM Loader using one of the following;

   >or=4K: Press 0000, and LXA.
   Press 7756, and LA.

   <4K: Press 0156*, and LA.

   *Use 1756 if tape is the A revision (MAINDEC-08-DJMSA-A-PM).

   Press INIT, then RUN.
   Tape will read into memory.
   Tape must be stopped when trailer is reached (press HLT/SS).

4. Set up location 0021:

   Press 0021 and LA.
   Press 4000 and D THIS.

5. Set up location 0023:

   Press 0023 and LA.
   Do one of the following:

   If 4K: Press 7777, and D THIS
   If 2K: Press 3777, and D THIS
   If 1K: Press 1777, and D THIS.

6. Start program as follows:

   Press 0000, then LSR.
   Press 0200, then LA.
   Press INIT, then RUN.

7. Allow program to run for 5 minutes. There should be no halts. At the end of 5 minutes, while program is still running:

   Press 0400, then LSR.

   Program will halt.

2.9.2 DKC8-AA Test

The DKC8-AA I/O Option Test program tests for proper operation of the Serial I/O, Parallel I/O, and Real Time clock contained on the M8316 module. In addition to the paper tape(s), the following equipment is needed:

W987 Quad Module Extender

Three Termi-point Jumpers (Available in a package of 100, type 915. Any length may be used, although 8 in. is probably most useful).

BC08R cable (any stock length)

These items are supplied as a portion of the PDP-8/A maintenance kit, and may also be ordered separately using the numbers just mentioned. This test requires placing the DKC8-AA on a module extender; hence a table to support the Programmer's Console or cables to extend the panel cables should be available.

1. Turn PDP-8/A power OFF. Without altering the M8316 switch settings, remove the M8316 from the PDP-8/A. Be sure to provide enough slack in the Teletype cable and the parallel I/O cables to allow easy removal of the module. Plug the W987 Quad Extender into the slot previously occupied by the M8316, and plug the M8316 into the extender. Remove the parallel I/O cables (if used) from J4 and J5, marking the cables so they can be properly reinstalled at the end of this test. Plug one end of the BC08R cable into J4. Plug the other end of the BC08R cable into J5. There should be one fold and no twists in the cable. Do not remove the Teletype cable or the cables to the Programmer's Console. Turn PDP-8/A power ON.

2. Using the same procedure as for steps 1, 2, 3, and 4 of the CPU test, (Paragraph 2.8.1) load the tape into memory.

CAUTION
Do not use the loading procedure for memory test.

The tape to be loaded is:

>or=4K: MAINDEC-08-DJDKA-PB1
<4K: MAINDEC-DJDKA-PM1

3. Without turning power off, remove the Teletype cable from J3 and install three Termi-Point jumpers as follows:

J3-E to J3-H
J3-K to J3-KK
J3-S to J3-AA

Change S1-5 on the M8316 from OFF to ON. Make no other switch changes at this time.

4. Set up location 0021 as follows:

Press 0021 then LA.
Deposit one of the following numbers by entering it via the numeric keys, then press D THIS:

Memory Size	Enter
1K	6000
2K	6001
4K	6003
8K	6007
16K	6017

5. Start program as follows:

Press 0000, LSR then LXA.
Press 0200, INIT then RUN.

6. Allow program to run for 5 minutes. There should be no halts while program is still running:

Press 0400 then LSR.

Program will halt.

Then:

>or= 4K: Skip to Step 9
< 4K: Continue on to Step 7.

7. (Omit if >or= 4K) Return S1-5 to off. Remove the Termi-point jumpers from J3 and re-install the Teletype cable. (Be sure it is installed so the printed A on the cable connector is at the same end as the printed A on J3.) Load:

   MAINDEC-08-DJDKA-PM2

   and then repeat steps 3, 4, and 5 of this test. Allow program to run for 5 minutes (no halts). Then:

   Press 0400 then LSR.

   Program will halt.

8. (Omit if >or= 4K). Return S1-5 to off. Remove the Termi-point jumpers from J3 and re-install the Teletype cable as described in step 7.
   Load:

   MAINDEC-08-DJDKA-PM3

   and then repeat steps 3, 4, and 5. Allow program to run for 5 minutes (no halts). Then:

   Press 0400 then LSR.

   Program will halt.

9. Do this step regardless of memory size.

   For a C etch revision: Set S1-3 and S1-7 ON; leave S1-5 ON.
   For a D etch revision: Set S1-1, 2, 4, 5, and 7 ON; set S1-3 OFF.
   Continue for either revision.
   Remove the Termi-point jumpers from J3.
   Now connect:

   J3-F to J3-J
   J3-E to J3-M

   Start program, as described in step 5, and allow program to run for 5 minutes (no halts). Then:

   Press 0400 then LSR.

   Program will halt.

   Then do one of the following:

   >or= 4K; Skip to step 11
   < 4K: Do step 10

10. Skip this step if > or = 4K.)
For a C etch revision: Set S1-3, 5, and 7 OFF.
For a D etch revision: Set S1-1, 3, and 4 ON; set S1-2 and 7 OFF.
Continue for either revision.
Remove Termi-point jumpers from J3. Replace Teletype cable as described under step 7. Load

MAINDEC-08-DJDKA-PM4

and repeat steps 3, 4, and 5. Allow program to run for 5 minutes. Then:

Press 0400 then LSR.

Program will halt.

11. Do this step regardless of memory size.
For a C etch revision: Set S1-3 and S1-7 ON; set S1-8 OFF.
For a D etch revision: Set S1-1, 2, 4, and 7 ON; set S1-3 and S1-8 OFF.
Continue for either revision.

Press 0000 then LSR.

Then do one of the following:

>or = 4K: Press 4000 then LA.
<4K: Press 1200 then LA.

Press INIT and then RUN.

The program should run for 30 seconds ± 0.5 seconds from the time the RUN button is pressed; then halt.

Now:

>or = 4K: Press 4023 or LA.
<4K: Press 1223 then LA.

Press INIT and then RUN.

Program will halt.

Turn on S1-3 and S1-7.
Turn off S1-8.

Press 0001 and LSR.
Press RUN.

WARNING
Do not press INIT.

The program should run for 30 seconds ± 0.5 seconds, and then halt.

12. Do this step regardless of memory size.

    Turn PDP-8/A power OFF.
    For a C etch revision: Set S1-3, 5, and 7 OFF; set S1-8 ON.
    For a D etch revision: Set S1-1, 3, 4, 8, and 9 ON; set S1-2, 5, and 7 OFF.

    Continue for either revision. Remove all Termi-point jumpers. Replace Teletype cable on J3, being sure the pin letters on the cable and board connector match. Remove the BC08R cable from J4 and J5. Re-install parallel I/O cables (if used). Remove the W987 Quad Extender from the PDP-8/A, and re-install the M316. Be careful not to alter switch settings accidently while inserting the M8316.

2.9.3 KM8-A Extended Option Board Test

NOTE

Make sure you have the correct diagnostic program. MAINDEC-08-DJKMA-A- is for M8317 modules having ROMs E82 and E87 labeled 87A2 and 88A2; MAINDEC-08-DJKMA-B- is for ROMs labeled 158A2 and 159A2.

The KM8-A Extended Option Board Test program tests the circuitry contained on the M8317 module. As in the previous test, the module under test is placed on a W987 Quad Module Extender to allow the operator to alter switch settings without turning off power to the PDP-8/A. Again, it is advisable to have a table to support the Programmer's Console.

The following series of tests are designed for operation on a PDP-8/A with 4K or more of memory, since two of the three options on this module require at least 4K of memory. Also available for this option are test programs which will run in 1K of memory. Consult your local DIGITAL sales office if more information on the 1K programs is needed.

1. Turn OFF power to the PDP-8/A, and place the M8317 on the W987 Quad Extender. The M8317 must be plugged into slot 2 or 3 of the Omnibus.

2. Write on paper the position of all switches on the M8317, and then place all these switches in the OFF position. Unplug the controllers for any bootstrappable options (such as the PC8-E, TA8-E, RK8-E controllers and the KA8-E Positive I/O adapter), but leave the Teletype connected.

3. Turn on power, and load RIM at address 7756 using the keys. Do not attempt to use the bootstrap – it was disabled at step 2. Load the Binary Loader (see Paragraphs 2.7.1 and 2.7.3).

4. Read in the tape (MAINDEC-08-DJKMA-PB) using the Binary Loader. (See Paragraph 2.7.4).

5. Set up location 0021 as follows:

   Press 0021 then LA.

Deposit one of the following numbers (depending on memory size) by entering it via the numeric keys and then pressing D THIS.

Memory Size	Enter
4K	7003
8K	7007
12K	7013
16K	7017
32K	7037

Start program:

Press 0000, LXA, then LSR.
Press 0200, INIT, then RUN

6. Allow program to run for 10 minutes. Then:

   Press 0400 and LSR.

   Program will halt.

7. Turn S2-1 on. Then:

   Press 4255 then LA.
   Press 0000, LSR, INIT, and then RUN.

   Program will halt.

8. Set up for bootstrap test:

   Press 4465, LA, INIT, then RUN.

   Program will halt.

9. Test the paper tape bootstrap as follows:

   Turn ON S2-5, S2-6, S2-7, S1-1, S1-2, S1-3, S1-6, S1-7, and S1-8. Make sure Teletype reader lever is in either the STOP or FREE position.

   Press:

   BOOT
   BOOT
   HLT/SS
   0000, then LSR
   4401, LA, INIT, and then RUN

   Program will halt with ADDRS = 04462 if paper tape bootstrap is correct.

NOTE

There is no point in checking a bootstrap unless your PDP-8/A is equipped with the option, (e.g., unless your PDP-8/A is equipped with an RK8-E, do not bother to test the RK8-E bootstrap).

10. Check any other bootstraps as follows:

    Repeat step 8.

    Set switches according to Table 2-14 or 2-15, depending on the bootstrap you are testing. Leave S1-6, S1-7, and S1-8 ON.

    Press:

    BOOT
    BOOT
    HLT/SS

    NOTE

    There are two different types of ROMs for the M8317 module. Those modules that have ROMs labeled 87A2 and 88A2 should use Table 2-14 for bootstrap select switch settings (see Figure 2-18 for switch and ROM locations). Those modules that have ROMs labeled 158A2 and 159A2 should use Table 2-15 for switch settings.

    Enter the value of SR from Tables 2-14 and 2-15, then press in order;

    LSR, 4400, LA, INIT, then RUN

    Program will halt with ADDRS = 04462 if Bootstrap is correct.

Table 2-14
Bootstrap Switch Settings for ROMs (E82 and E87) Labeled 87A2 and 88A2

Bootstrap	S2-5	S2-6	S2-7	S2-8	S1-1	S1-2	S1-3	SR
HI LO RIM	ON	ON	ON	OFF	ON	ON	ON	0000
RK8-E	ON	OFF	ON	OFF	ON	OFF	ON	0004
TC08	ON	OFF	OFF	ON	OFF	ON	ON	0001
RF08/DF32D	OFF	ON	ON	ON	ON	OFF	OFF	0002
TA8-E	OFF	ON	ON	OFF	ON	OFF	OFF	0003

Table 2-15
Bootstrap Switch Settings for ROMs (E82 and E87)
Labeled 158A2 and 159A2

Bootstrap	S2-5	S2-6	S2-7	S2-8	S1-1	S1-2	S1-3	SR
HI LO RIM	ON	ON	ON	OFF	ON	ON	ON	0000
RK8-E	ON	OFF	ON	OFF	ON	OFF	ON	0004
RX8-E	ON	OFF	OFF	ON	OFF	ON	ON	0003
RF08/DF32D	OFF	ON	OFF	ON	OFF	ON	OFF	0001
TA8-E	OFF	ON	OFF	OFF	OFF	ON	OFF	0002

11. Make sure the BATTERY CHARGING light on the Limited Function panel is off. If this light is on, leave PDP-8/A power on but do not attempt the following test until the BATTERY CHARGING light is off.

NOTE
Unless you have experienced a recent power failure while the PDP-8/A was running or have unplugged the PDP-8/A power cord without first turning the ON/OFF switch to OFF, it is very unlikely that the BATTERY CHARGING light will be on by the time you get to this test.

12. Turn ON S1-1, 3, 6, 7, and 8; S2-3, 5, and 7. Turn OFF S1-2, 4, and 5; S2-1, 2, 4, 6 and 8.

13. Enter the following:

    Press 4600 then LA.
    Press 0000, LSR, INIT, then RUN.

    PDP-8/A will halt.

14. Press 0002, LSR, INIT, and then RUN.

15. Without operating the panel ON/OFF switch, unplug the power cord of the PDP-8/A from the wall receptacle. ADDRS should display 04764, and the RUN lights on the Limited Function Panel and the Programmer's Console should be off.

    Re-insert the power cord. The program should begin running again. Do not leave power cord unplugged any longer than necessary, since the batteries will discharge.

16. Repeat step 15 four times.

17. Turn OFF power. Return the M8317 switches to the original positions, wrtten down at step 2. Remove the W987 Quad Extender, and replace the M8317 in the PDP-8/A box. Be careful not to disturb the switch settings on this module or any adjacent modules while so doing. Replace the Programmer's Console.

2.9.4 Testing Extended Memories

A good test of extended memories, the CPU and the memory extension control may be made by running the 1K to 32K Random Memory Reference Instruction Exerciser Test. This test may also be used in systems with as little as 1K of memory.

1. Load RIM loader, as described in Paragraph 2.7.1 starting with one of the following addresses:

   >or = 4K: 7756
   <4K: 0156

2. Place MAINDEC-08-DJEXA-PM in paper-tape reader, enter same address as given for step 1, and press:

   LA.
   1000, then LXA.
   INIT, then RUN.

   Press HLT/SS when trailer is over read station.

3. Set up location 0021 by pressing:

   0021 and LA

Memory Size	Enter
1K	4000
2K	4001
4K	4003
8K	4007
12K	4013
16K	4017
32K	4037

   Enter number corresponding to memory size from chart, then press D THIS.

4. Enter the following:

   Press 0000 then LSR.
   Press 0200, INIT, and then RUN.

5. Run two minutes for each 1K of memory (4K: 8 minutes, 8K: 16 minutes, etc.).

2.10 BASIC PDP-8/A MAINTENANCE

Table 2-16 lists some basic PDP-8/A problem symptoms and their possible causes.

Table 2-16
Basic PDP-8/A Troubleshooting

Symptom	Possible Cause/Solution
No lights, fans not running	Fuse Blown. Power Switch is OFF. AC power not connected. MASTER/ SLAVE switch in wrong position.
Fans running, but no lights	Circuit breaker on the regulator assembly is OFF.
RUN light does not come on after BOOT switch is activated	Check switches on KM8-A Extended Option Board (M8317). Switch settings are in Tables 2-10 through 2-13.
BATTERY CHARGING light stays on	The battery requires a minimum of 15 hours of charging after a complete discharge. The light normally flashes on momentarily after power on if battery has been fully charged.
RUN light comes on when power switch is turned on	This function is switch selectable on KK8-A CPU Module (M8315) and KM8-AA Extended Option Module (M8317).
RUN light stays on after AC power is unplugged	Do not unplug AC power unless PDP-8/A power is shut off. The PDP-8/A behaves as if there has been a power failure, and the battery supply takes over.
Peripheral will not BOOT with BOOT switch	BOOT switch on Limited Function Panel in wrong position, it should be down. PANEL LOCK should be down. Check switches on the Extended Option Board (M8317). Check baud rate switches on DKC8-AA I/O Option Board (M8316). Switch settings are in Paragraph 2.4.3.6.
Machine remains powered even with ON/OFF switch set to OFF	Fuse in power control relay circuit is blown. Set ON/OFF switch to OFF, then unplug the power cord before attempting to change this fuse.
Light on the G8018 Regulator board is out (8A computers).	Turn off power, remove regulator board, check +5 V circuit breaker and -15 V, ±15 V, and +20 V fuses.

CHAPTER 3
INTERFACING TO THE OMNIBUS

This chapter provides the necessary interfacing information for users to understand operation of the Omnibus or to build a special interface for the PDP-8/A. It deals primarily with hardware design considerations required to build an interface for the Omnibus. Programming information is contained in two other PDP-8 documents, *Introduction to Programming* and *Programming Languages*. A user who plans to write a program for his/her interface should be familiar with these documents. However, DIGITAL has many device handlers and software packages the user may be able to use as written, or modified, to operate devices with the PDP-8/A.

Signals are transferred from module to module on a device called the Omnibus. All PDP-8 modules and options that are compatible with the PDP-8/A plug into the Omnibus. The Omnibus is an etched board with rows of connectors soldered to it. The pin assignment is the same on all connectors. The Omnibus is comprised of 96 signals and provides the means to transfer these signals from module to module.

There are many advantages to the Omnibus approach. Because all connectors on the Omnibus carry the same signals, a module can be placed anywhere on the bus with the following exceptions:

1. The CPU must be plugged into either the top slot (slot 1) or the bottom 3 slots (refer to Table 2-2).

2. The PDP-8/A option boards must be plugged into slots 2 and 3 (either module in either slot). MOS memory cannot be plugged into slots 2 or 3.

3. All hex modules should be plugged into the top slots followed by quad modules in the lower slots.

3.1 OMNIBUS PHYSICAL DESCRIPTION

The Omnibus (Figure 3-1) consists of standard DEC H863 connector blocks mounted on an etched circuit board and wave soldered. The connectors are arranged to accept hex and quad type modules (Figure 3-2). The Omnibus has 10 slots if it is a semiconductor machine and 12 or 20 slots if it is a core memory machine. Core memory machines use an extra connector (E) to supply +20 V and −5 V to the MM8-AA and MM8-AB core memory modules.

All pins on the Omnibus are parallel-wired (e.g., pin CM2 of slot 1 is wired to pin CM2 of slot 2) to form a parallel bus comprised of 96 Omnibus signals. The parallel bus is used to connect the central processor, memory, peripherals, and options. All modules must plug into the Omnibus.

The Omnibus is mounted on the PDP-8/A chassis (Figure 3-3 shows an 8A chassis). Modules are inserted and removed from the front of the chassis. For connections to the outside world, connectors on the sides of the modules connect to a shielded coaxial cable or flat ribbon cable. An opening in the chassis allows cables to be routed to the user's device.

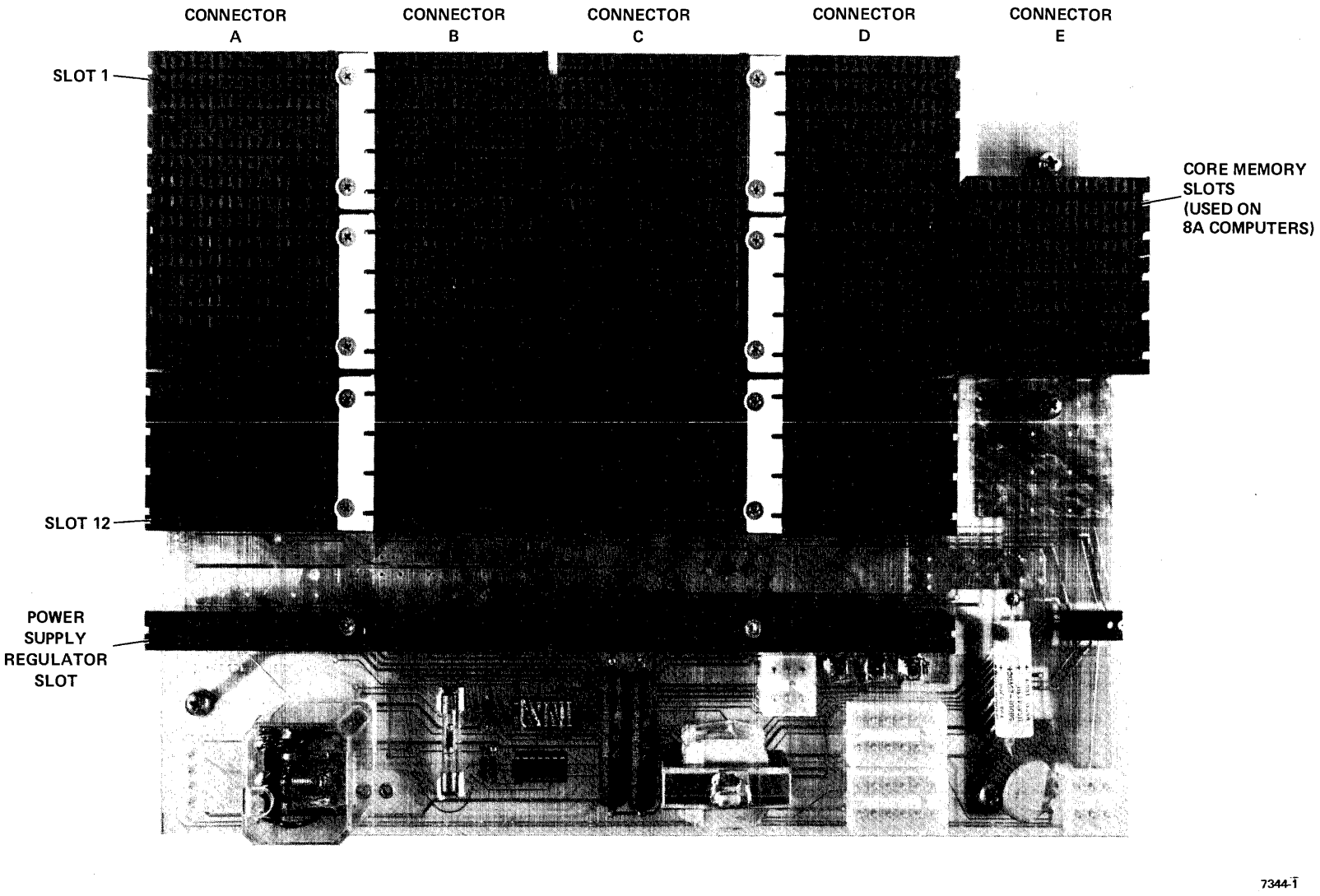


Figure 3-1 PDP-8/A Omnibus (H9194)

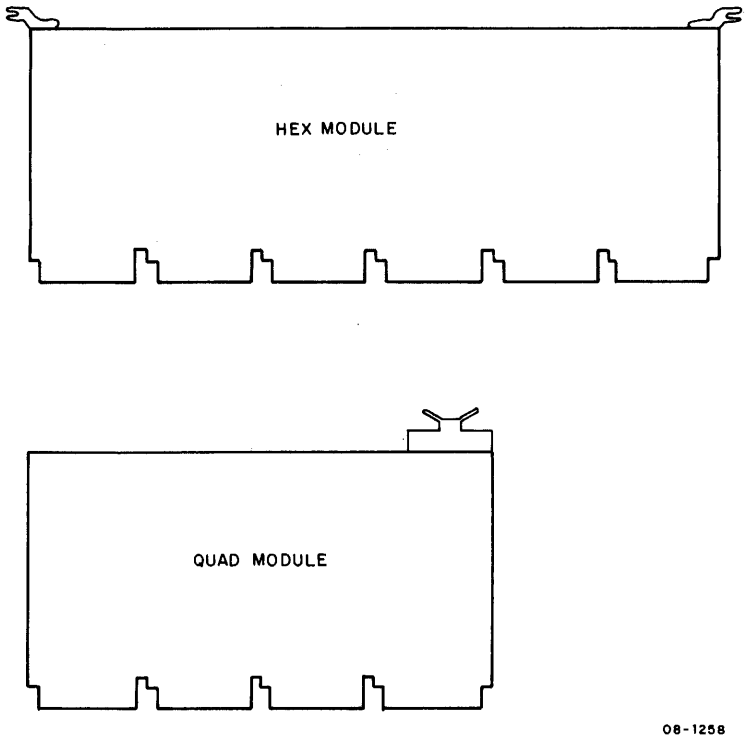


Figure 3-2 PDP-8/A Hex and Quad Modules

3.2 BUS SPECIFICATIONS

	Logic Levels
Logical 1	Maximum Voltage: +0.4 V
	Minimum Voltage: -0.5 V
Logical 0	Maximum Voltage: +5.0 V
	Minimum Voltage: +3.0 V

3.3 METHODS OF DATA TRANSFER

There are three methods of accomplishing input/output data transfers: Programmed I/O Transfers, Interrupt Transfers, and Data Break Transfers.

3.3.1 Programmed I/O Transfer

The simplest method of accomplishing an input/output transfer is to employ the Programmed I/O Transfer. This method relies upon the processor to check the Status Flag and service the flag with a subroutine.

3.3.2 Interrupt Facility

A more efficient method of input/output transfers is to employ the Interrupt System. This method uses the Programmed I/O Transfer, but the device signals the processor when a transfer is requied by grounding an INTERRUPT REQUEST line. The processor responds at the end of the current instruction by entering a service routine.

3.3.3 Data Break Transfer

A still more efficient method of transfer is to employ the Data Break System. Whenever the data break device decides that it is time to transfer, it generates MS, IR DIS to force the processor into a Direct Memory Access state and CPMA DIS to disable the CPMA register. This leaves the data break device free to supply its own address and to manipulate the Major Registers Control logic so that it can input and output data. The processor responds to a

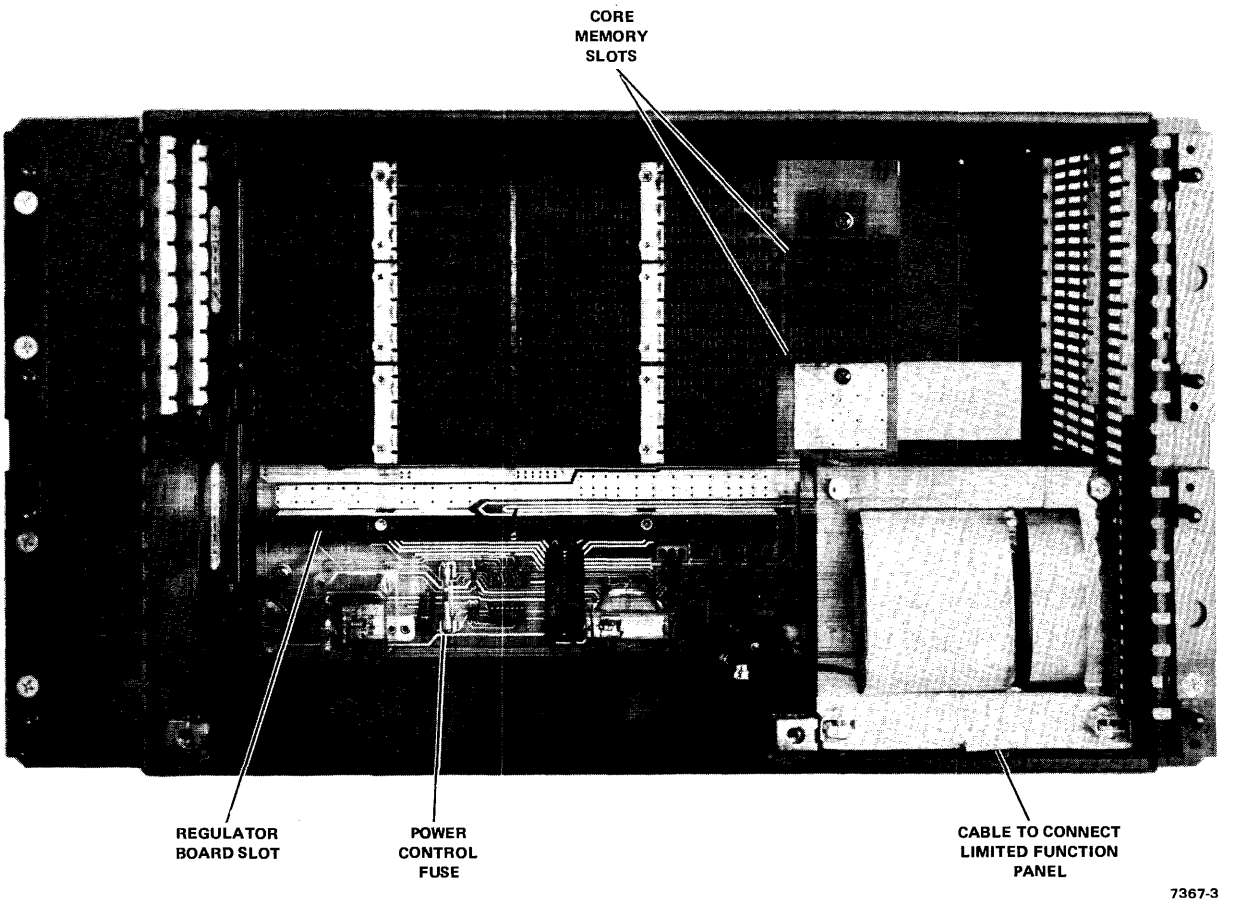


Figure 3-3 8A Chassis (H9300)

break at the end of the current cycle. In general, data break requires more hardware than Programmed I/O. Additional logic is necessary to handle addressing, etc., and some Programmed I/O is necessary to initialize and check the status of the device.

3.3.4 The External Bus

The External Bus, which is mechanically and electrically organized the same as the I/O Bus on the PDP-8/L or the PDP-8/I computers, plugs into the Omnibus by way of the Positive I/O Bus Interface and the Data Break Interface. Each of these modules receives the same signal on the same pins as any other module plugged into the Omnibus. The interfacing details of the External Bus are given in Paragraph 3.1.9 and Volume II of the *PDP-8/E Maintenance Manual* (DEC-8E-HMM2A-D-D).

The *PDP-8/A Miniprocessor Handbook* contains the information required to select the type of interface required for the user's device and describes each of the transfer methods in detail.

3.4 MODULE CONFIGURATION ON THE OMNIBUS

The basic PDP-8/A system is comprised of one Central Processor Unit and at least one memory module. Other modules may be plugged into the Omnibus to add additional memory, options, or device interfaces to the system. Table 3-1 lists the PDP-8/A-compatible modules along with their Omnibus slot assignments.

Hex and quad modules cannot be inter-mixed on the Omnibus. All hex modules should be put together in the top slots and all quad modules in the bottom slots.

For options that require additional modules to hold all the logic, two or more modules may be connected with H851 top connectors (Figure 3-4).

Table 3-1
Slot Assignments for Modules on the Omnibus

Option	Option Designation	Type of Module	Number of Modules	Omnibus Slot Assignment
Optical Mark Card Reader Control	CM8-F	Quad	1	4–last*
Card Reader Control	CR8-F	Quad	1	4–last
Interprocessor Buffer	DB8-EA	Quad	1	2–last
I/O Option Module	DKC8-AA	Hex	1	2–3
Synchronous Modem Interface	DP8-EA, EB	Quad	2	2–last
Buffered Digital I/O	DR8-EA	Quad	1	2–last
Positive I/O Interface	KA8-E	Quad	1	4–last
Programmer's Console	KC8-AA, AB	PNL.MT.	0	N.A.
Data Break Interface	KD8-E	Quad	1	4–last
Redundancy Check Option	KG8-EA	Quad	1	4–last
Central Processor Unit	KK8-A	Hex	1	1
Central Processor Unit	KK8-E	Quad	2	Refer
Timing Generator	KK8-E	Quad	1	to
Bus Loads	KK8-E	Quad	1	Table 2-2
Asynchronous Data Interface	KL8-JA	Quad	1	2–last
	KL8-M	Quad	1	2–last
Extended Option Module	KM8-A	Hex	1	2–3
Line Printer Control	LE8-XX	Quad	1	2–last
Line Printer Control	LS8-F	Quad	1	2–last
Core Memory (8K)	MM8-AA	Hex	2	4–8
Core Memory (16K)	MM8-AB	Hex	2	4–8
Read Only Memory (1K)	MR8-AA	Quad	1	2–last
Read Only Memory (2K)	MR8-AB	Quad	1	2–last
Read Only Memory (4K)	MR8-AD	Quad	1	2–last
Reprogrammable Read Only Memory	MR8-FB	Quad	1	2–last
Read/Write Memory (1K)	MS8-AA	Quad	1	4–last
Read/Write Memory (2K)	MS8-AB	Quad	1	4–last
Read/Write Memory	MS8-AD	Quad	1	4–last
Reader Punch Control	PC8-E, PR8-E	Quad	1	4–last
RK05 Disk Control	RK8-EA	Quad	3	4–last
TU60 Cassette Interface	TA8-AA	Quad	1	2–last
TU10 DEC Magtape Control	TM8-EA, -FA	Quad	4	4–last
Point Plot Display Control	VC8-E	Quad	2	2–last
Video Display and Terminal Control	VT8-E	Quad	3	4–last
DK8-EP Real Time Clock	DK8-EP	Quad	2	2–last
AD8-A A/D Converter	AD8-A	Quad	1	2–last

*'Last' applies except when considering both a non-expanded 8A600 or 8A620, and the added chassis of an expanded 8A600 or 8A620 (refer to Table 2-2).

3.5 OMNIBUS PIN ASSIGNMENT

Figure 3-5 relates the PDP-8/A modules (both quad and hex) and the Omnibus signals. The connectors are illustrated in the lower part of the figure. The component side of the module is side 1. Individual pins are specified in this manner: BH1 means connector B, pin H, side 1; DM2 means connector D, pin M, side 2, and so on. Each connector pin has a corresponding pin on the Omnibus that carries a specific PDP-8/A signal. The upper part of Figure 3-5 relates the signal names to the Omnibus/module connector pins. The L (low) or H (high) after the signal name identifies the assertion level for that signal. For example, MDO L is asserted (a logical one) when it is low (+0.4 to –0.5 V). Most signals on the Omnibus are tied through a load resistor to +5 Vdc. High level signals should be a minimum of +2.6 Vdc and low level signals should be +0.4 Vdc, as defined by TTL logic.

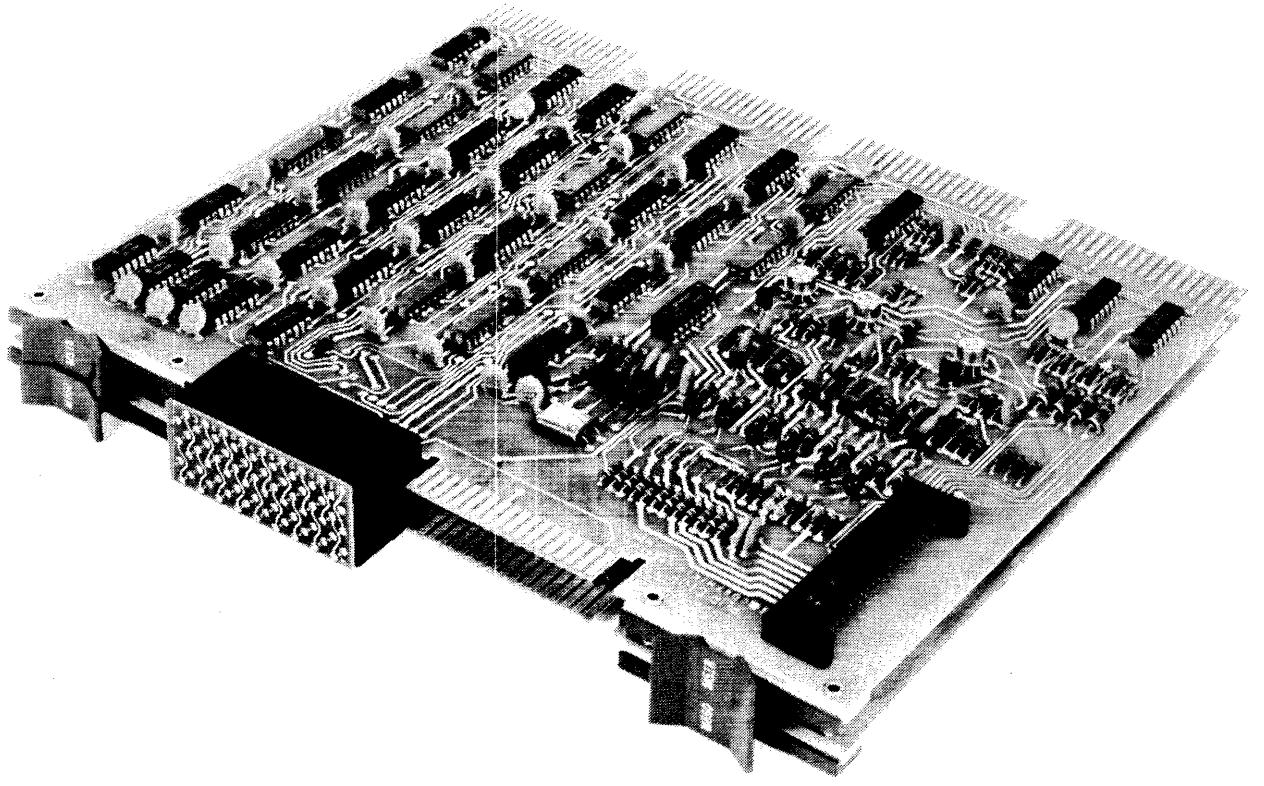


Figure 3-4 Modules Connected With H851 Type Connector

The Omnibus is wired so that the signal appearing on a specific pin is the same for most slots on the Omnibus. For example, pin CK1 of every Omnibus slot carries signal BUS STROBE L. There are some exceptions and these are noted in Figure 3-5. In slot 1, which has the KK8-A CPU plugged into it, pins AA1 and CA1 are tied to +5 Vdc instead of being test points as indicated in Figure 3-5. These pins supply the extra +5 Vdc current required for the M8315 module. Slots 2 and 3 also have pins with signals but they are different from the signals in the other slots.

1. BA1 of slots 2 and 3 carries BATTERY EMPTY L
2. BB1 of slots 2 and 3 carries AC LOW L
3. DA1 of slots 2 and 3 carries PANEL LOCK L

PIN	CONNECTOR, SIDE									
	E1	E2	D1	D2	C1	C2	B1	B2	A1	A2
A	TP	+20V	TP NOTE 5	+15V	TP NOTE 2	+5V	TP NOTE 3	+5V	TP NOTE 2	+5V
B	TP	NOT USED	TP	−15V	TP	−15	TP NOTE 4	−15V	TP	−15V
C	GND	GND	GND	GND	GND	GND	GND	GND	SP GND NOTE 1	GND
D	TP	NOT USED	MA8L	IRØ L	I/O PAUSE L	TP1 H	MA4 L	INT STROBE H	MAØ L	EMAØ L
E	TP	+20V	MA9 L	IR1L	CØL	TP2 H	MA5 L	BRK IN PROG L	MA1 L	EMA 1L
F	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
H	TP	MEM REFRESH (+5V)	MA1ØL	IR2 L	C1L	TP3 H	MA6 L	MA,MS LOAD CONT L	MA2 L	EMA2 L
J	TP	MEM REFRESH (+5V)	MA11L	FL	C2 L	TP4H	MA7 L	OVERFLOW L	MA3 L	MEM START L
K	TP	+20V	MD8 L	DL	BUS STROBE L	TS1 L	MD4 L	BREAK DATA CONT L	MDØ L	MD DIR L
L	TP	NOT USED	MD9 L	EL	INTERNAL I/O L	TS2 L	MD5 L	BREAK CYCLE L	MD1 L	SOURCE H
M	TP	−5V	MD1Ø L	USER MODE L	NOT LAST XFER L	TS3 L	MD6 L	LA ENABLE L	MD2 L	STROBE H
N	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
P	TP	+20V	MD11 L	F SET L	INT ROST L	TS4 L	MD7 L	INT IN PROG H	MD3 L	INHIBIT H
R	TP	NOT USED	DATA 8 L	PULSE LA H	INITIALIZE H	LINK DATA L	DATA 4 L	NTS STALL L	DATA Ø L	RETURN H
S	NOT USED	NOT USED	DATA 9 L	STOP L	SKIP L	LINK LOAD L	DATA 5 L	RES H	DATA 1 L	WRITE H
T	JUMPER	GND	GND	GND	GND	GND	GND	GND	GND	GND
U	JUMPER	NOT USED	DATA 1Ø L	KEY CONTROL L	CPMA DISABLE L	IND 1 L	DATA 6 L	RUN L	DATA 2 L	ROM ADDRESS L
V	TP	NOT USED	DATA 11 L	SW	MS,IR DISABLE L	IND2 L	DATA 7L	POWER OK H	DATA 3 L	LINK L

Notes

1. This pin is connected to ground on the bus but serves as a logic signal within modules for testing.
2. Pins AA1 and CA1 in slot 1 supply +5 V to the CPU module.
3. Pin BA1 of slots 2 and 3 supplies BATTERY EMPTY to the option modules.
4. Pin BB1 of slots 2 and 3 supplies AC LOW to the option modules.
5. DA1 of slots 2 and 3 supplies PANEL LOCK to the option modules.

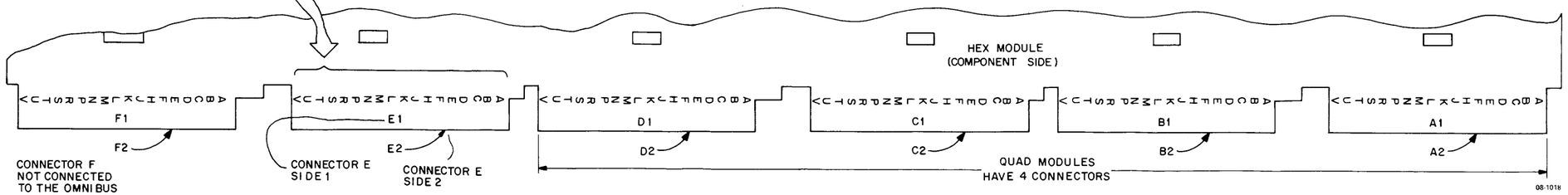


Figure 3-5 Omnibus Signal Locator

3.6 MAJOR GROUPS OF SIGNALS

The 96 signals of the Omnibus can be divided into nine major classes.

3.6.1 Memory Address – 15 Lines

The 15 signals EMA<0:2>L and MA<0:11>L form a bus which defines the currently active memory address. The source of MA<0:11>L is the CPU during instruction processing, and the currently active data break device during Direct Memory Access (DMA) operations. The source of EMA<0:2>L is the memory extension control during instruction processing, and the currrently active data break device during DMA operations. Load resistors within the CPU define EMA<0:2>L as zeros (highs) if there is no memory extension control in the system.

3.6.2 Memory Data and Memory Direction Control – 13 Lines

3.6.2.1 MD<0:11>L – The 12 signals MD<0:11>L form a bidirectional data path between memory and CPU. In addition, these lines are monitored by Programmed I/O devices to determine device code and sub-device operation, and by data break devices to obtain output (memory-to-DMA device) words.

3.6.2.2 MD DIR L – The source of information on MD<0:11>L is controlled by MD DIR L. If MD DIR L is low, the data of the currently active memory is gated onto MD<0:11>L. If MD DIR L is high, the contents of the CPU's memory buffer register are gated onto MD<0:11>L.

3.6.3 Data Bus – 12 Lines

The 12 signals DATA<0:11>L form a multi-purpose 12-bit bus used for data exchange between peripheral and CPU, for data input from DMA devices, for front-panel monitoring of selected registers, and for the determination of data break priority.

3.6.4 I/O Control Signals – 10 Lines

This group of signals controls the I/O dialogue between CPU and programmed peripherals. This group includes INITIALIZE H, which is used for clearing peripheral flags.

3.6.5 DMA Control Signals – 8 Lines

This group of signals controls the operation of data break (DMA). Several of these signals are also activated for certain front panel operations. Included in this group is RUN L, which is used for clearing data break requests when the computer is halted.

3.6.6 Timing Signals – 9 Lines

Five time pulses serve as system clocks. Similarly, four time state levels serve as system enabling levels. All of these signals originate within the main timing generator of the CPU.

3.6.7 CPU States – 6 Lines

The major state of the CPU appears on FL, DL, or EL (FETCH, DEFER, or EXECUTE); the operation code of the instruction currently being processed appears on IR<0:2>L.

3.6.8 Memory Timing Signals – 5 Lines

Five signals originate in the main timing generator of the CPU and are bused to all memories. These signals (SOURCE H, RETURN H, WRITE H, INHIBIT H, and STROBE H) control all memory operations.

3.6.9 Miscellaneous Signals – 18 Lines

These signals do not fit into any of the above categories. A large percentage of them are used by the Programmer's Console. Two signals (ROM ADDRESS L and NTS STALL L) are driven by some types of memories under special conditions, and are monitored by the CPU and other memories. The rest of these signals are truly miscellaneous. Included in this group is a signal (POWER OK H) that reports the validity of the power supply voltages.

3.6.10 Special Signals

Slots 2 and 3 of the Omnibus carry some special signals which are used on the PDP-8/A option modules. They are: AC LOW L, BATTERY EMPTY L (associated with the battery back-up power supply), and PANEL LOCK (disables operations from the Programmer's Console when the PANEL LOCK switch is placed in the down position).

3.6.11 Interconnections

The interconnection of various system parts via the Omnibus is shown below:

	CPU	MEM EXT	MEM	I/O	DMA *	PANEL
	b o o i u t n t h	b o o i u t n t h	b o o i u t n t h	b o o i u t n t h	b o o i u t n t h	b o o i u t n t h
MEM ADD	X	X	X		X	X
MEM DAT	X	X	X	X	X	X
DATA BUS	X	X		X	X	X
I/O CTRL	X	X		X		X
DMA CTRL	X	X			X	X
TIMING	X	X		X	X	X
CPU ST	X	X				X
MEM TIM	X		X			
MISC	X	X	X			X

*This is just the DMA portion of what is usually a complex peripheral. Such a peripheral usually uses the programmed I/O signals as well.

3.7 DETAILED DESCRIPTION OF THE 96 OMNIBUS SIGNALS

This paragraph describes the logical operation of each of the Omnibus signal lines. The paragraphs are arranged similar to Paragraph 3.6 for easier correlation.

3.7.1 Memory Address – 15 Lines

These signals are changed starting at the leading edge of PULSE LOAD ADDRESS H or TP4 H and remain static through the entire memory cycle.

3.7.1.1 EMA <0:2>L. – Must be settled 50 ns prior to leading edge of SOURCE H and RETURN H.

Signal	Pin	
EMA0 L	AD2	Most Significant Bit
EMA1 L	AE2	
EMA2 L	AH2	Least Significant Bit

3.7.1.2 MA <0:11>L. – Must be settled 50 ns prior to leading edge of SOURCE H and RETURN H.

Signal	Pin	
MA0 L	AD1	Most Significant Bit
MA1 L	AE1	
MA2 L	AH1	
MA3 L	AJ1	
MA4 L	BD1	
MA5 L	BE1	
MA6 L	BH1	
MA7 L	BJ1	
MA8 L	DD1	
MA9 L	DE1	
MA10 L	DH1	
MA11 L	DJ1	Least Significant Bit

3.7.2 Memory Data and Direction Control – 13 Lines

3.7.2.1 MD<0:11>L. – These lines form the data path to and from memory. If MD DIR L remains low for the entire memory cycle, information from memory may be placed on the MD lines as late as 150 ns prior to TP2; otherwise, the information must be present 250 ns before TP2. If MD DIR L is allowed to go high, the new MD information from the CPU's Memory Buffer register must be on the Omnibus 150 ns prior to the leading edge of INHIBIT H, and must remain static for the duration of INHIBIT H for proper memory operation. It is desirable that the MD lines remain static into Time State 1 (TS1) of the next machine cycle to facilitate displaying the contents of memory when single-stepping programs.

Signal	Pin	
MD0 L	AK1	Most Significant Bit
MD1 L	AL1	
MD2 L	AM1	
MD3 L	AP1	
MD4 L	BK1	
MD5 L	BL1	
MD6 L	BM1	
MD7 L	BP1	
MD8 L	DK1	
MD9 L	DL1	
MD10 L	DM1	
MD11 L	DP1	Least Significant Bit

3.7.2.2 MD DIR L – L=memory driving MD lines; H=CPU's MB register driving MD lines. MD DIR L is always low from 100 ns after the leading edge of TP1 H to the leading edge of TP2 H, when it may be allowed to go high. The gating from MD DIR L to the drivers of the MD bus is static; hence care should be taken to guarantee that this line does not "glitch". If MD DIR L remains low for the entire memory cycle, the information on the MD lines is valid from the time it is placed on the Omnibus through the end of the memory cycle. No extra time need be allotted for computing and storing information in the CPU's MB register, and no time need be allotted for MB driver turn-on and bus propagation after TP2.

Signal	Pin
MD DIR L	AK2

3.7.3 Data Bus – 12 Lines

DATA <0:11>L. The data is a multi-purpose, 12-bit bus whose use is a function of the machine state. During TS1 of every memory cycle, the data bus carries indicator information as defined by the IND lines, (Paragraph 3.7.9.1).

During TS2 of FETCH cycles, the data bus carries the contents of the AC. During TS2 of DMA cycles, the data bus carries information to be placed in memory, or information to be added to the contents of memory. During TS3 of IOT instructions, the information on the data bus is a function of the I/O control lines (Paragraph 3.7.4.5). During TS3 of OP2 instructions, the contents of the CPU's AC are placed on the data bus if the CLA bit (bit 4 of the instruction word) is zero, and the contents of the control panel's switch register are placed on the data bus if bit 9 of the instruction word is a one. This implements the OSR and LAS instructions. During TS4 of all machine cycles, the data bus is reserved for determining data break (DMA) priority. See Paragraph 3.7.5 for more details.

A good general rule is for all logic to stay off the data bus unless there is a valid reason for placing data on that bus. The data bus must be left free for use by the CPU.

Signal	Pin	
DATA0 L	AR1	Most Significant Bit
DATA1 L	AS1	
DATA2 L	AU1	
DATA3 L	AV1	
DATA4 L	BR1	
DATA5 L	BS1	
DATA6 L	BU1	
DATA7 L	BV1	
DATA8 L	DR1	
DATA9 L	DS1	
DATA10 L	DU1	
DATA11 L	DV1	Least Significant Bit

3.7.4 I/O Control Signals – 10 Lines

Basic I/O devices may perform data exchange between the AC of the CPU and the device's registers. The state of the device is tested using skip instructions. These devices need not make connection to C2 L, BUS STROBE L, and NOT LAST XFER L.

More complicated I/O devices may use BUS STROBE L and NOT LAST XFER L to stall the CPU, perform multiple transfers in a single IOT, and/or modify the PC (and/or the Link).

3.7.4.1 I/O PAUSE L – Pin CD1 – I/O PAUSE L is low if F L, MD0 L and MD1 L are low and USER MODE L and MD2 L are high. Also included is a gating term from the timing chain. It is the command to all Programmed I/O peripherals to compare their device codes with the contents of MD<3:8>L. If a peripheral finds equality with MD<3:8>L, it decodes MD<9:11>L to determine the sub-device operation to be performed. The peripheral has 100 ns in which to decode its subdevice operation and assert information onto the C lines and data bus. Similarly, it must remove all information 100 ns after I/O PAUSE L is negated.

I/O PAUSE L remains asserted during extended I/O cycles until the CPU has been restarted. (Paragraph 3.7.4.7)

Although not mandatory, it is strongly urged that the peripheral logic design incorporate load-relief logic to minimize loading on the DATA and MD buses when I/O PAUSE L is negated. Loading rules require load relief if there is more than one Programmed I/O peripheral.

3.7.4.2 INTERNAL I/O L – Pin CL1 – INTERNAL I/O L alerts the KA8-E Positive I/O Bus Adapter that an I/O device on the Omnibus has recognized the IOT being processed. If the KA8-E finds this line not asserted, it processes the IOT by stopping the CPU and entering an expanded I/O cycle.

All internal (Omnibus) I/O devices ground this line if they find equality between MD<3:8>L and their device code when I/O PAUSE L is low.

3.7.4.3 SKIP L – Pin CS1 – SKIP L is sampled by the CPU at TP3 to determine if an I/O skip should occur. The skip occurs if SKIP L is low. This line is sampled every TP3 (not just during IOT instructions) if the processor is not in the DMA state.

3.7.4.4 INT RQST L – Pin CP1 – INT RQST L is sampled by the CPU at the leading edge of INT STROBE H if all other interrupt conditions are met to determine if an interrupt request is pending. This line is asserted by a peripheral device when a condition that causes an interrupt is encountered. Since the CPU contains a synchronizing flip-flop, this line may be asserted at any time. In addition, if this line is grounded 100 ns or more before TP3, the SRQ instruction will skip.

3.7.4.5 C<0:2>L – Pins CE1 (C0 L); CH1 (C1 L); CJ1 (C2 L) – C<0:2>L control the type of transfer during an IOT as shown below:

C<0:2>L			Transfer
0	1	2	
H	x	H	AC → DATA<0:11>L → AC (Peripheral may "or" information onto DATA<0:11>L)
L	H	H	AC → DATA<0:11>L; 0 → AC
L	L	H	DATA<0:11>L → AC
x	H	L	DATA<0:11>L+PC → PC
x	L	L	DATA<0:11>L → PC

x = doesn't matter. In general, peripherals use only SKIP L to modify the PC, and so do not make connection to C2 L. See Paragraph 3.8.4 for the impact on timing.

3.7.4.6 BUS STROBE L – Pin CK1 – BUS STROBE L is a negative-going pulse which causes the AC or PC to be loaded during an IOT. BUS STROBE L is also used in conjunction with NOT LAST XFER L during long I/O cycles (Paragraph 3.7.4.7).

During an IOT, gating within the CPU generates a single BUS STROBE L pulse at TP3 time if NOT LAST XFER L is high (i.e., if the IOT is not an extended IOT). If an extended I/O cycle is in process (i.e., if NOT LAST XFER L is low at TP3 H), the peripheral must generate all BUS STROBE L pulses. The AC or PC (depending on C2 L) is loaded at the leading (falling) edge of BUS STROBE L.

3.7.4.7 NOT LAST XFER L – Pin CL1 – Most peripheral controllers require only one transfer per IOT; hence the single transfer at TP3 time is adequate. Such peripherals do not ground NOT LAST XFER L and do not drive BUS STROBE L. Other, more complex peripherals (the KA8-E Positive I/O Interface, for example) require extended timing and use NOT LAST XFER L to "stall" the CPU in an I/O cycle.

To stop the CPU in TS3 of an I/O cycle, ground NOT LAST XFER L prior to TP3 H of the IOT.

The CPU will remain in TS3, and will not generate INT STROBE H or BUS STROBE L. Timing is now controlled by the peripheral.

The peripheral may make any number of transfers by controlling C<0:2>L, generating BUS STROBE L and keeping NOT LAST XFER L at ground.

The CPU is restarted by allowing NOT LAST XFER L to go high before the leading (falling) edge of BUS STROBE L. In addition to making a final data transfer, the CPU restarts by generating INT STROBE H, entering TS4 and by negating I/O PAUSE L.

3.7.4.8 INITIALIZE H – Pin CR1 – INITIALIZE H is asserted (high) by:

1. Pressing the Programmer's Console INIT key.

2. Executing the CAF instruction (octal 6007).

3. Negating the POWER OK H.

INITIALIZE H statically clears the AC, Link, interrupt system, and peripheral flags. It also sets the interrupt enable flip-flops of peripherals that must remain program-compatible with older versions that did not have an interrupt enable flip-flop. (Two important devices in this category are the TTY and paper-tape reader/punch interrupt enables.)

3.7.5 DMA Control Signals – 8 Lines

Data breaks (DMA) allow a peripheral to communicate directly with memory, bypassing the CPU. The only CPU register available to the DMA device is the MB; all other CPU registers must be preserved. Data breaks may occur between any CPU cycles, but a data break cannot be performed while the CPU is in the midst of an extended I/O cycle because the currently active memory is then supplying information to the bus.

Data breaks take place in the following sequence:

1. At INT STROBE H leading edge, the decision to request a data break is made at the peripheral by setting its break request flip-flop.

2. A device starting a data break unconditionally asserts CPMA DISABLE L and BREAK IN PROG L until its break request flip-flop is cleared.

3. Data break priority is determined on DATA<0:11>L when TS4 L is asserted. Each data break device is assigned a unique line on DATA<0:11>L, with DATA0 L being the highest-priority line. Each requesting device asserts its line on DATA<0:11>L, and examines the state of all higher-priority lines to determine if they are all high. For example, a device asserting DATA5 L examines DATA<0:4>L to make sure these lines are all high. The device finding all higher-order lines high proceeds to step 4 below; all other devices remain in step 3.

4. The device winning the priority test sets its MA Control flip-flops at the leading edge of TP4 H. (The path from TP4 H to the Memory Address lines must have as little delay as possible; hence two flip-flops are recommended to provide adequate drive without introducing the delay of a buffer (Paragraph 3.7.5.7). The MA Control flip-flops gate the break address onto the 15 Memory Address lines, and assert MS, IR DISABLE L and (if this cycle is a data exchange cycle) BK CYCLE L.

5. At TP1 H, the active device asserts MA, MS LOAD CONT L.

6. For input to memory, the active device merely places its data on DATA<0:11>L during TS2. For output from memory, the device asserts BREAK DATA CONT L during TS2 L, and loads its register with the contents of MD<0:11>L at the leading edge of TP2 H, TP3 H, or TP4 H. For Add To Memory, the device places the data to be added on DATA<0:11>L during TS2, and asserts BREAK DATA CONT L during TS2. The modified information is loaded into the CPU's MB and overflow flip-flop at TP2 H, and may be read by the device at TP3 H or TP4 H. (TP3 H is generally used, since OVERFLOW L is valid only at this time.) The data prior to modification may be read at the leading edge of TP2 H.

7. At the completion of a data break, all lines are in the same order and at the same times in which they were asserted.

   Three-cycle data breaks are merely three one-cycle data breaks with a special control to handle Word Count and Current Address cycles. BREAK CYCLE L is not asserted during these two cycles; it is asserted only for the final, data exchange cycle.

   DMA latency is the longest machine cycle, plus the time of TS4.

3.7.5.1 BRK IN PROG L – Pin BE2 – This signal provides indicator information to the console. It is grounded at INT STROBE H leading edge if a break is to take place, and asserts the console BRK IN PROG bit of the Major State Register.

3.7.5.2 CPMA DISABLE L – Pin CU1 – CPMA DISABLE L is asserted (low) by break devices if data breaks are to occur. It is sampled by the CPU and memory extension control at the leading edge of TP4 H. If CPMA DISABLE L is low at that time, the memory extension control's field bits and the CPU's Memory Address bits are removed from EMA<0:2>L and MA<0:11>L. If CPMA DISABLE L is negated (high) at the leading edge of TP4 H, the memory extension field bits and the CPU's Memory Address register are gated to EMA<0:2>L and MA<0:11>L respectively.

3.7.5.3 MS, IR DISABLE L – Pin CV1 – When MS, IR DISABLE L is high, the Major State and IR flip-flops drive the Major State and IR lines on the Omnibus (Paragraph 3.8.1). When MS, IR DISABLE L is asserted (low), the Major State and IR lines are not driven by the CPU. Unless some external device asserts a Major State, the CPU is then in the DMA state.

3.7.5.4 MA, MS LOAD CONT L – Pin BH2 – When MA, MS LOAD CONT L is negated (high), the CPU and memory extension control function normally. Asserting this line inhibits the loading of new information into the CPU's Major State and Memory Address registers, and into certain control flip-flops of the memory extension control. This signal must not change while TP4 H is high. It is normally changed at TP1 time.

3.7.5.5 BREAK DATA CONT L – Pin BK2 – This signal is ignored unless F L, D L, and E L are all high. BREAK DATA CONT L should be stable as early in TS2 as possible, and defines the information loaded into the MB at TP2 H. If BREAK DATA CONT L is high during TS2 of a DMA, DATA<0:11>L is loaded into MB<0:11>. If BREAK DATA CONT L is low during TS2 of a DMA, MD<0:11>I plus DATA0:11>L is loaded into MB<0:11>. Making BREAK DATA CONT L low and placing no information (zeros) on DATA<0:11>L causes a DMA that does not modify memory.

3.7.5.6 OVERFLOW L – Pin BJ2 – This line is asserted (low) during TS3 if a carry occurs at TP2. Hence this line is asserted if any of the following occur:

1. Auto Index or JMS wrap-around
2. ISZ overflow
3. Data break overflow or carry

3.7.5.7 BK CYCLE L – Pin BL2 – Panel information from the data break device. Low indicates that a break data transfer cycle is in process.

3.7.5.8 RUN L – Pin BU2 – This signal is really a CPU state since it indicates that the CPU's timing generator is running (when low). It is included in this group of signals because its most important function is as a gating term used to clear all break requests when negated (high).

3.7.6 Timing Signals – 9 Lines

Five pulses and four levels originate in the timing generator of the CPU and are used as system clocks and enabling levels respectively. Time pulses are nominally 100 ns wide (INT STROBE H is more loosely defined. Refer to Paragraph 3.8.1). Time states change nominally 50 ns after the leading edge of the time pulse. When the CPU is stopped, the machine is at the beginning of TS1. Applying a single MEM START L causes the timing chain to start and continue to run until:

1. The STOP L line on the Omnibus is asserted at TP3, or
2. The CPU encounters a HLT instruction at TP3, or
3. POWER OK H is negated at TP3 and the current memory cycle is complete.

A time state precedes the time pulse of the same number; INT STROBE H is coincident with TP3 H except when in an extended IOT operation; TS1 L is automatically entered at the end of TS4.

Signal	Pin
TS1 L	CK2
TS2 L	CL2
TS3 L	CM2
TS4 L	CP2
TP1 H	CD2
TP2 H	CE2
TP3 H	CH2
TP4 H	CJ2
INT STROBE H	BD2

3.7.7 CPU STATE – 6 Lines

3.7.7.1 Major State Lines

The CPU Major State appears on these lines unless MS, IR DISABLE L is asserted (Paragraph 3.7.5.3). The Major State as seen by the CPU's instruction decoder is taken from these lines, thus it is possible to build special options which force instructions to the CPU. Normally, the Major State lines change at TP4.

Major State	Pin
F L	DJ2
D L	DK2
E L	DL2

3.7.7.2 IR<0:2>L – These reflect the state of the CPU's instruction register provided MS, IR DISABLE L is high. A low on IR<0:2>L represents a one in the corresponding bit of the Instruction Register. As in the case of the Major State lines, the IR lines are disconnected from the Instruction Register if MS, IR DISABLE L is low. The instruction seen by the CPU during D and E Major States is obtained from these lines. During instruction FETCH, the Direct JUMP, IOT, and operate instructions are decoded directly from the MD lines. As with the Major State lines, it is possible to force instructions during defer or execute cycles. The IR is loaded at TP2 of an instruction FETCH (F L is low), or at TP4 if an interrupt is being honored (INT IN PROG H is high).

Signal	Pin
IR0 L	DD2
IR1 L	DE2
IR2 L	DH2

3.7.8 Memory Timing Signals – 5 Lines

These signals are defined in terms of the 1.5 μs memory cycle. (See Paragaraph 3.8.2 for waveforms.)

3.7.8.1 SOURCE H – Pin AL2, and RETURN H – Pin AR2 – These signals become asserted (high) at the same time and direct the memory to turn on its read/write currents. RETURN H becomes negated 50 ns later than SOURCE H, thereby defining the voltage to which the memory stack is charged.

3.7.8.2 WRITE H – Pin AS2 – WRITE H controls the direction of current flow in the memory stack. It is high during write and low during read. If WRITE H is low, the positive-going transition of SOURCE H is usually used to clear all Memory Buffer registers.

3.7.8.3 INHIBIT H – Pin AP2 – INHIBIT H is a gating level to the inhibit drivers of core memory. When high, it causes the selected memory's inhibit drivers to turn on.

3.7.8.4 STROBE H – Pin AM2 – The leading edge of STROBE H provides a time reference from which the strobe in each individual memory is derived. Each memory delays this edge by an optimum amount for that memory, and then strobes its sense amplifiers. The selected memory must have its data on MD<0:11>L at or before strobe leading edge plus 150 ns (this time does not include bus charging time).

3.7.9 Miscellaneous Signals – 18 Lines

IND1 L	IND2 L	Information on DATA<0:11>L
H	H	Status Word*
H	L	MQ<0:11>
L	H	All zeros (highs)
L	L	AC<0:11>

*STATUS WORD (Figure 1-5)

Bit	Information
0	LINK
1	Not used
2	INT RQST L (low on DATA2 L if INT RQST L [Pin CP1] is low)
3	INT INH Flip-Flop**
4	INTERRUPT DELAY Flip-Flop (denotes interrupt on)
5	User Mode L**
6–8	IF<0:2>**
9–11	DF<0:2>**

**From memory extension control if present, otherwise these remain high (zeros).

3.7.9.1 IND1 L – Pin CU2, and IND2 L – Pin CV2 – These signals control the information gated to DATA<0:11>L during TS1. Since DATA<0:11>L is defined as low for a 1, ones in register bits place lows on DATA<0:11>L.

Gating circuitry in any logic driving IND1 L and IND2 L should ground IND1 L and allow IND2 L to go high if LA ENABLE L is asserted (low) (Paragraph 3.7.9.9).

3.7.9.2 MEM START L – Pin AJ2 – Grounding MEM START L causes the timing chain of the CPU to start. MEM START L may be a 100 ns negative-going pulse, or it may be a level that is low if TS1 L is asserted and the logical decision to start the machine has been made. MEM START L must not be asserted (low) beyond TP2 H, since it may then interfere with possible HLT instructions.

A single MEM START L pulse causes the CPU to start and continue to run until halted by the program or by the STOP L line (Paragraph 3.7.9.3).

3.7.9.3 STOP L – Pin DS2 – STOP L is sampled by the CPU at the leading edge of TP3 H of every machine cycle. If STOP L is asserted (low), the CPU completes its current memory cycle and stops in TS1 (just after TP4 H goes to ground). At that point in its cycle, the CPU can display:

New Memory Address (on EMA<0:2>L and MA<0:11L)

New Major State (on F L, D L, and E L)

Memory Data of last-referenced location (on MD<0:11>L)

Status or AC or MQ (on DATA<0:11>L, depending on IND1 L and IND2 L)

Any other lines on the Omnibus for which display provision has been made

STOP L is asserted by HLT/SS on the Programmer s Console, and is also asserted when:

Single deposit (D THIS) operation is in process

Examine operation is in processor

A HLT instruction (octal 7402) is executed.

POWER OK H is low KEY CONTROL L is low during examine or deposit condition (Paragraph 3.7.9.9).

3.7.9.4 LINK L – Pin AV2 – LINK L is low if the LINK bit of the CPU is a one, and high if the LINK is a zero.

3.7.9.5 LINK LOAD L – Pin CS2, and LINK DATA L – Pin CR2 – These two signals allow loading of the LINK from the Omnibus. Loading occurs on the leading (falling) edge of LINK LOAD L, and the data loaded into the LINK is a one if LINK DATA L is low. These two signals should be used only in extended I/O cycles while NOT LAST XFER L is low.

3.7.9.6 F SET L – Pin DP2 – This line is asserted (low) if the Major State gating of the CPU indicates the next Major State will be a FETCH. The conditions causing this line to be asserted are:

1. A Major State of EXECUTE, no interrupt being honored (Paragraph 3.7.9.8).
2. A Major State of DEFER and an IR of 5 (JMP instruction).
3. A Major State of FETCH, a JMP instruction and MD3 L high (direct jump).
4. A Major State of FETCH and an IOT instruction.
5. A Major State of FETCH and an operate instruction.
6. DMA (F L, D L and E L all high).

3.7.9.7 USER MODE L – Pin DM2 – This line is normally driven by the timeshare portion of the memory extension control and is tied high by a load resistor in the CPU if no memory extension control is in the system. USER MODE L is changed only at TP4 time.

If USER MODE L is high, the CPU and control panel function normally. If USER MODE L is asserted (low), the following operations are inhibited:

1. The HALT instruction (inhibited in the CPU)

2. The OSR and LAS instructions (inhibited in the panel logic)

3. I/O PAUSE L remains high even though an IOT instruction is fetched from memory (inhibited in the CPU).

Interruption of the program, upon detection of any of these conditions, is handled by the memory extension control.

3.7.9.8 INT IN PROG H – Pin BP2 – INT IN PROG H is allowed to go high if:

1. The interrupt system has been turned on by an ION or RTF instruction and at least one subsequent instruction fetch has occurred.

2. An interrupt request has been recognized by the INT SYNC flip-flop of the CPU (which sets at the leading edge of INT STROBE H if INT RQST L and FSET L are both low).

3. There is no interrupt inhibiting condition. This condition is preserved in the INT INHIBIT flip-flop in the memory extension control, and is generated if a CIF, CUF, SUF, RMF or RTF instruction has been processed and a JMP or JMS has not yet occurred to complete the field change.

INT IN PROG H is used by the CPU to load 0 into the CPU's MA, force the Major State to EXECUTE and IR to JMS, and to turn off the interrupt system. INT IN PROG H is also used by the memory extension control to load the save field, and to clear the IB, IF and DF. INT IN PROG H goes high at INT STROBE H time, and is not negated again until the interrupt system is turned off (INT IN PROG H, INT STROBE H and not DMA).

3.7.9.9 LA ENABLE L – Pin BM2, and KEY CONTROL L – Pin DU2 – These lines must not be asserted unless the CPU is in the DMA state (MS, IR DISABLE L low and F L, D L, and E L all high). If LA ENABLE L is low, any logic driving IND1 L and IND2 L must assert IND1 L and turn off any drivers driving IND2 L.

The function of LA ENABLE L, KEY CONTROL L, and BREAK DATA CONT L are defined as follows:

Load Address Enable	Key Control	Break Data Control	Function
L	L	L	XLA 7
L	L	H	XLA 0
L	H	L	Non-stop deposit
L	H	H	Load address
H	L	L	Panel examine
H	L	H	Panel deposit
H	H	L	Add to memory*
H	H	H	Break deposit*

*See Paragraph 3.7.5.5.

E THIS or E NEXT on the Programmer's Console asserts STOP L, performs one memory cycle at the address in the CPU's MA register, does a break add to memory, and increments the MA.

D THIS or D NEXT on the Programmer's Console asserts STOP L, performs one memory cycle at the address in the CPU's MA register, does a break deposit with the Entry Register of the console providing input data, and increments the MA.

Load Address – There are two possible functions. If PULSE LA H is asserted, the MA is loaded from DATA<0:11>L. If MEM START L is asserted, the CPU starts, performing an examine at whatever location is in the CPU's MA. At TP3 H, the contents of DATA<0:11>L are loaded into the PC and transferred to the CPU's MA at TP4 H. The CPU is not stopped. (STOP L is not asserted.)

Non-stop Deposit – Same as panel deposit except STOP L is not asserted, so the CPU continues to run. Useful for loading bootstrap programs into memory.

XLA0 – There are two modes of operation. If PULSE LA H is asserted, the memory extension control is loaded with whatever is on DATA<6:11>L. If MEM START L is asserted, the CPU starts and does an examine at whatever location is in the CPU's MA. The memory extension control is loaded at TP3 H, but 0 is on DATA<6:11>L so the memory extension control's IF, IB, and DF registers are cleared. STOP L is not asserted, so the CPU continues to run.

XLA7 – Like XLA0 with MEM START L, except that the CPU places 7777 on DATA<0:11>L, loading 7 into the IB, IF, and DF. The AC must be 0 for this function to work properly.

3.7.9.10 PULSE LA H – Pin DR2 – PULSE LA H causes the CPU's MA register to be loaded if KEY CONTROL L is high; or the memory extension control's IB, IF, and DF registers to be loaded if KEY CONTROL L is low. PULSE LA H is a nominal 100 ns positive-going pulse.

3.7.9.11 ROM ADDRESS L – Pin AU2 – ROM ADDRESS L is examined by core and other read/write memories. If ROM ADDRESS L is high, the read/write memory functions normally. If ROM ADDRESS L is low, the read/write memory is disabled. ROM ADDRESS L is asserted by small ROMs which overlay read/write memories, thus providing a small number of read-only locations in a large read/write memory. The gating for this signal must be fast.

There are only 25 ns from the time the address lines have been established to the time this signal must be asserted.

ROM ADDRESS L also modifies the JMS instruction by inhibiting the incrementing of the new PC contents. This action causes the JMS instruction to act like a JMP instruction (except for timing) if a JMS to ROM is attempted.

3.7.9.12 NTS STALL L – Pin BR2 – NTS STALL L (Next Time State Stall L) provides a means of stalling machine operation to accomodate memories slower than the one for which the timing chain was designed.

When NTS STALL L is high, the timing chain of the CPU functions normally. If NTS STALL L is asserted (low), the timing chain functions normally to the middle of the next time pulse. The time state changes and the time pulse completes in the normal 100 ns, but the timing chain stalls at the beginning of the new time state. The stalling of the time state continues until NTS STALL L goes high, restarting the timing chain. NTS STALL L has no effect on the duration of the five memory timing signals. It merely stretches the time before read, the time between read and write, and the time after write before new address. NTS STALL L must be low, 100 ns, before the leading edge of a time pulse to guarantee stalling in the next time state. The timing generator will not stall in the next time state if NTS STALL L is high for the 100 ns prior to the leading edge of the time pulse.

NTS STALL Low at	Time State Becomes Longer at	And There is
TP1 H	TS2	Longer time from end of read to TP2, allowing the CPU to accommodate memories with long read access time.
TP2 H	TS3	Longer time from when MB is loaded to the start of write.
TP3 H	TS4	Longer time from start of write to time address is changed, accommodating memories with long write times.
TP4 H	TS1	Longer time from address change to start of read.

Watch break latency when using NTS STALL.

3.7.9.13 SW – Pin DV2 – This line reflects the state of the bootstrap flip-flop controlled by the switch on the Programmer's Console ORed with the state of the bootstrap switch on the Limited Function Panel. The signal is low if the switch is up on the Limited Function Panel.

On machines equipped with bootstrap options, the low-to-high transition of this line initiates bootstrap operation if the CPU is halted. If there is no bootstrap option in the machine, this line is available for any use the user may devise.

3.7.9.14 POWER OK H – Pin BV2 – POWER OK H originates in the power supply and reports the state of the dc voltages to the CPU, memory extension control and core memories. The dc supplies are in regulation if this signal is high (Paragraph 3.9).

As the dc supplies fall toward ground, POWER OK H will be negated but may go somewhat positive again as the +5 V supply nears ground. POWER OK H must remain at less than 0.4 V until all supply voltages are less than 30% of their nominal value, otherwise, modification of core memory contents may occur.

POWER OK H being low asserts STOP L. POWER OK H going low is also applied to an integrator in the CPU, the output of which generates INITIALIZE H and is used as a master clear for the timing chain. Similar integrators in each of the core memories enable and disable the memory current supplies.

Negating POWER OK H does the following:

1. STOP L is asserted immediately.

2. At the next TP3 H, RUN L is negated by the CPU.

3. At the following TS1, all break devices clear their break requests and the memory extension control initializes its EMA Enable flip-flop. The gating to accomplish this is usually the AND of POWER OK H being low, TS1 L being low, and RUN L being high.

4. After a delay (15–500 μs) long enough to allow the longest possible memory cycle to complete, the timing chain is preset to the beginning of TS1 with TP4 low. All memory timing signals are made low. The CPU's control flip-flop, which gates the CPU's MA onto the Memory Address lines, is placed in the "enabled" state. INITIALIZE H is generated, clearing the AC, LINK and interrupt system.

5. After a similar delay, each core memory disables its current sources so that memory cannot be altered if memory timing signals should become asserted as the dc voltages go away.

Upon application of power:

1. The CPU, extension control and peripherals are all initialized.

2. Memory current sources are enabled 1 to 70 ms after POWER OK H is asserted. This enabling is accomplished by an integrating capacitor, so that "spikes" on POWER OK H are filtered out.

3. The internal clear signal and the Omnibus INITIALIZE H signal are negated 200 to 1000 ms after POWER OK H is asserted.

4. All portions of the computer should be ready to run 0.1 sec after POWER OK H is asserted. MEM START L will not be recognized until after INITIALIZE H is negated.

3.7.9.15 RES – Pin BS2 – RES is an unused line. Digital Equipment Corporation reserves the right to define this line at a later date, and disclaims any responsibility to make this definition agree with any prior illicit use.

3.7.9.16 Special Signals – Special signals AC LOW L, BATTERY EMPTY L, and PANEL LOCK are carried only on pins in slots 2 and 3 of the Omnibus.

3.7.9.16.1 AC LOW L – Pin BB1 (Slots 2 and 3 Only) – AC LOW L is asserted when the ac voltage falls below 95 Vac ±3% and is negated when ac voltage goes above 105 Vac ±3% (with corresponding values to 220/240 Vac operation). AC LOW L is controlled by a detector in the power supply which senses changes in the ac voltage levels. On semiconductor machines, the system can continue to operate in the absence of ac power for up to 45 seconds fully loaded. In these machines AC LOW is the signal to switch to battery backup power. With core memory machines, AC LOW causes an interrupt that allows the program time to transfer the contents of the active registers to nonvolatile core memory.

3.7.9.16.2 BATTERY EMPTY L – Pin BA1 (Slots 2 and 3 Only) – BATTERY EMPTY L is asserted when a circuit in the power supply senses that the battery voltage has fallen below a certain value. This indicates that the battery has only 1.0 ms of run time remaining before the computer is halted by negation of POWER OK H (Paragraph 3.7.9.14).

3.7.9.16.3 PANEL LOCK L – Pin DA1 (Slots 2 and 3) – PANEL LOCK L is asserted when the PANEL LOCK switch is in the up position to disable all key pad switches except Switch Register (SR) and the read functions.

3.8 TIMING

Many signals on the Omnibus are wire-ORed. For these signals, the high level is determined by a load resistor and the low level is determined by one or more open-collector gates which ground the signal. Bus capacitance is moderately high; hence fall times in such situations are fast and rise times are slow (about 100 ns). This 100 ns is considered in the following timing diagrams by adding the 100 ns to the set-up times where necessary. This requires C<0:2>L to be defined from 450 ns before the leading edge of BUS STROBE L; 100 ns of this time is allotted to charging C<0:2>L.

3.8.1 Time Pulses and Time States

The time pulses (TP1 H, TP2 H, TP3 H, INT STROBE H, and TP4 H) plus their associated time states (TS1 L, TS2 L, TS3 L, and TS4 L) serve as the timing reference from which all other timing is derived (Figure 3-6). Timing pulses and time states are derived from a master crystal clock (20 MHz) in the timing generator of the CPU. This clock has a stability of 0.1%; hence the time between positive edges of time pulses is accurate to 0.1%. Time pulse widths are 90–110 ns; the uncertainty is caused by gate skew and threshold variation. Time states change nominally at 50 ns after the leading edge of the time pulses, but logic delays and loading introduce an uncertainty in this time.

Figure 3-7 details time pulse and time state change (this applies to TP1 H, TP2 H and TP4 H.)

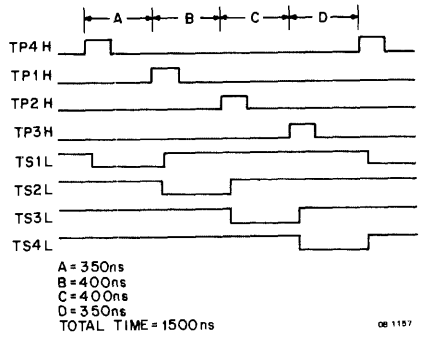


Figure 3-6 Timing For One Memory Cycle

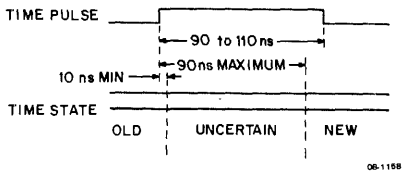


Figure 3-7 Time State and Time Pulse Change Timing

Figure 3-8 details TP3 H timing if NOT LAST XFER L is high and if I/O PAUSE L is high. (See Paragraph 3.8.5 for other conditions.)

3.8.2 Memory Timing

Normal memory timing is based on 1.5 μs core memory, and is shown in Figure 3-9.

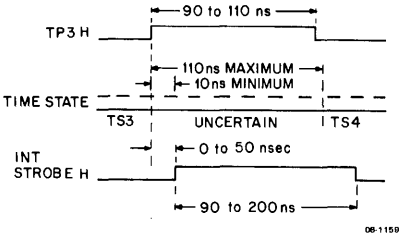


Figure 3-8 TP3 Timing During IOT Transfer

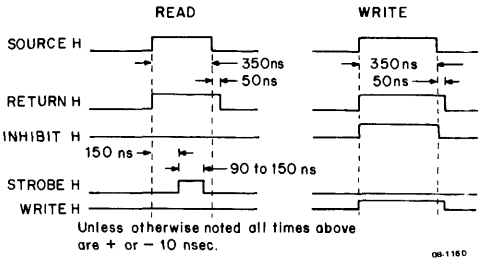


Figure 3-9 Memory Timing

3.8.3 Relationship Between CPU and Memory Timing

The timing relationship between the (read) CPU and memory is shown in Figures 3-10 (Read) and 3-11 (Write).

MD<0:11>L changes at TP2 H only if MD DIR L is allowed to go high. If MD DIR L remains low, MD<0:11>L is settled on bus at STROBE H leading edge +250 ns.

The times given take into consideration the type of load on MD<0:11>L, EMA<0:2>L and MA<0:11>L and its position, plus maximum bus capacitance.

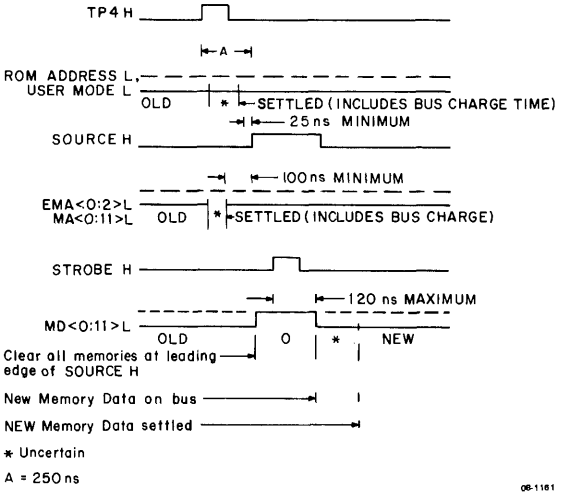


Figure 3-10 Memory Timing

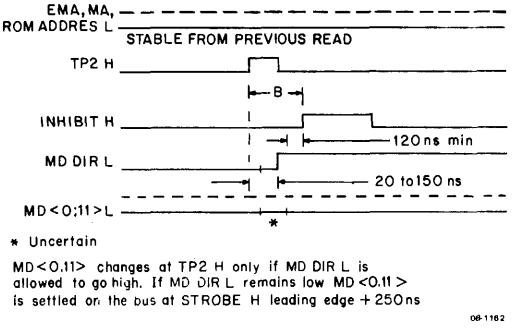


Figure 3-11 Write Timing

3.8.4 Basic I/O Timing

The Basic I/O timing in Figure 3-12 assumes the following:

1. Single transfer during IOT
2. No modification of PC (no connection to C2)L
3. C<0:1>L do not go to ground and then positive between the falling edge of I/O PAUSE L and the rising edge of TP3 H.

The peripheral must place its data on DATA<0:11>L and assert any C lines at least 250 ns prior to TP3 H. SKIP L must be asserted at least 100 ns before TP3 H if a skip is to occur. Peripheral registers are loaded at the leading edge of TP3 H. Peripheral registers must be edge-triggered, since DATA<0:11>L may start to change before TP3 H goes low again.

The timing for the CAF instruction is shown in Figure 3-13.

3.8.5 Expanded I/O Timing

The restrictions of Paragraph 3.8.4 regarding single transfer and limited use of C<0:2>L do not apply.

The timing required to stop the CPU (this operation is not confined to IOTs) using NOT LAST XFER L is shown in Figure 3-14.

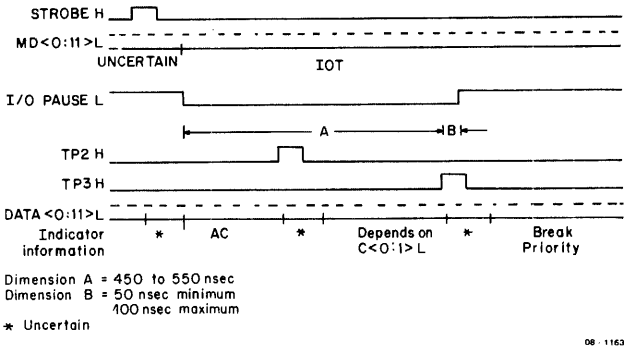


Figure 3-12 Basic I/O Timing

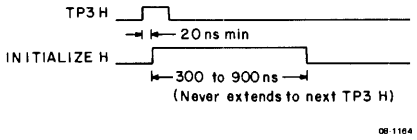


Figure 3-13 C A F Instruction Timing

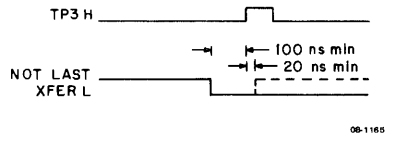


Figure 3-14 Timing to Stop CPU Using Not Last XFER L

Figure 3-15 shows the timing required to make transfers to or from the AC, or to the PC.

Peripheral data registers should be edge-triggered and loaded at the leading edge of BUS STROBE L (since the contents of the Data Bus may change as a result of sending BUS STROBE L to the CPU).

External loading of LINK must take place only in an expanded I/O cycle, and not at restart time. Figure 3-16 shows the timing for this operation.

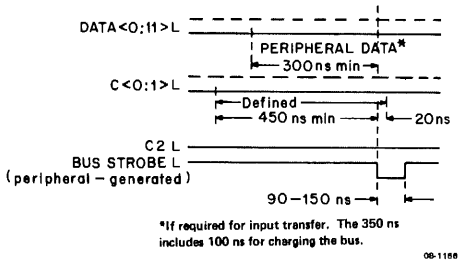


Figure 3-15 Transfer Timing

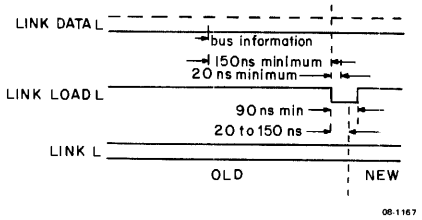


Figure 3-16 External Loading of Link Timing

Figure 3-17 shows the timing to restart the CPU after the peripheral has completed its data transfers. Loading LINK is not allowed during this operation because of timing restrictions as the CPU leaves TS3.

3.8.6 Data Break Timing

The timing required to initiate a data break is shown in Figure 3-18. These signals are controlled by the device making the break request.

3.8.6.1 Data Exchange – The data exchange timing is shown in Figure 3-19. Data to be placed in memory or used to modify memory must be in a register which has been loaded prior to TP1 H.

3.8.6.2 Final Operations – The timing required to end a data break transfer is shown in Figure 3-20.

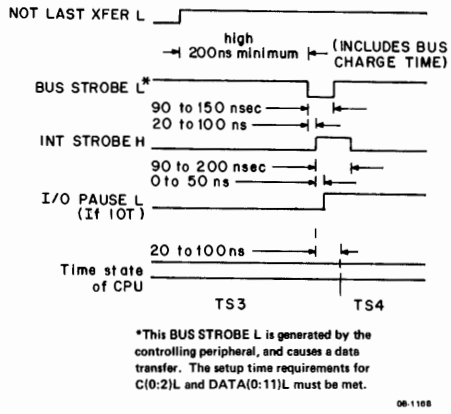


Figure 3-17 CPU Restart Timing

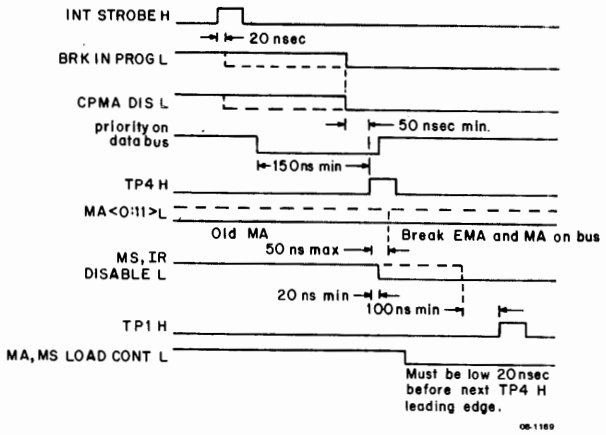


Figure 3-18 Data Break Timing

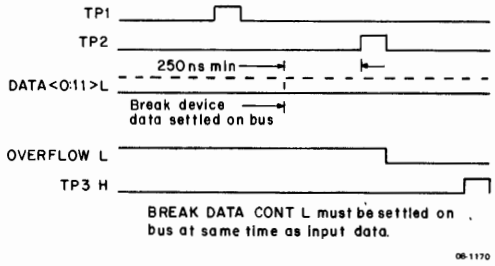


Figure 3-19 Data Exchange Timing

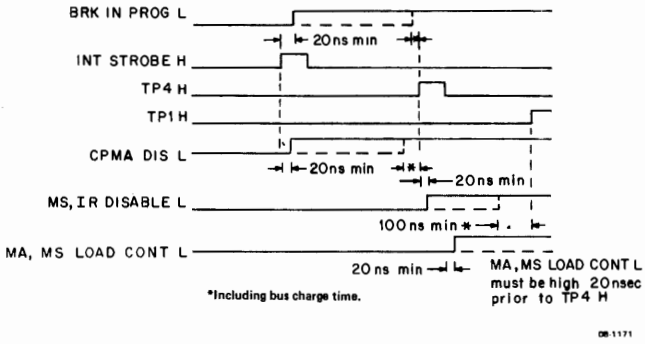


Figure 3-20 End of Data Break Timing

3.8.7 CPU Major States

The timing for the Major State of the CPU is shown in Figure 3-21.

3.8.7.1 IR (FETCH Cycle) – The timing for a FETCH cycle is shown in Figure 3-22.

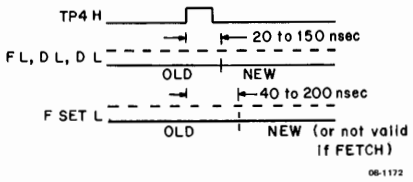


Figure 3-21 CPU Major States Timing

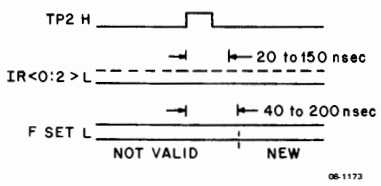


Figure 3-22 FETCH Cycle Timing

3.8.7.2 Interrupt Recognition – The timing associated with interrupt recognition is shown in Figure 3-23.

3.8.8 Timing Start and Stop

The timing for starting and stopping the CPU is shown in Figures 3-24 and 3-25.

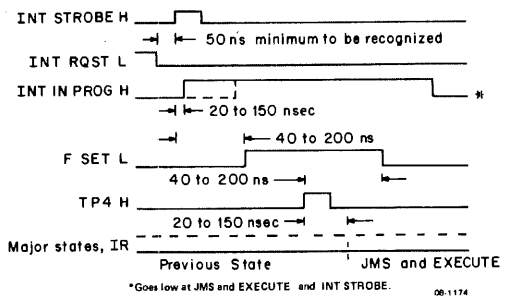


Figure 3-23 Interrupt Timing

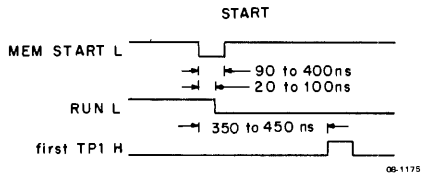


Figure 3-24 Start Timing

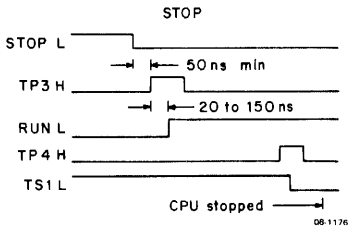


Figure 3-25 Stop Timing

3.9 ASYNCHRONOUS SIGNALS

The following signals are allowed to change asynchronously with respect to the CPU's timing chain:

POWER OK H (when negated also causes INITIALIZE H to change)
SW
IND1 L
IND2 L
INT RQST L
STOP L

3.10 SPECIAL SIGNALS

The following signals should be asserted only when the CPU is not running:

MEM START L (Paragraph 3.7.9.2)
PULSE LA H (90 ns min width positive pulse)

3.11 ELECTRICAL CHARACTERISTICS AND INTERFACING

3.11.1 Logic Levels

Low = -0.5 V to +0.4 V
High = +3.0 V to +5.0 V.

3.11.2 Bus Loads

All bus load resistors are on the CPU module (instead of at the end of the bus) and the resistors are returned to +5 Vdc. The Omnibus is restricted to 12 slots and may not be extended. Maximum bus capacitance is limited to 150 pF of which 30 pF is caused by the 12 slot bus and connectors.

3.11.3 Driving the Omnibus

Table 3-2 is a list of Omnibus signals, their load type, if they must sink, drivers, and number of inputs. The load type (1 through 6), and type of driver (OC, TRI, and UTI) are defined at the end of Table 3-2.

Table 3-2
Load Resistor and Drivers Summary

Signal	Load Type	Driver Must Sink (mA)	Drivers	Number of Inputs (TTL)
BREAK CYCLE L	1	16	----	----
BREAK DATA CONT L	1	16	1-OC	1/2
BRK IN PROG L	1		----	----
BUS STROBE L	6	60	1-OC	2
C0 L	1	16	----	1/2
C1 L	1	16	----	1/2
C2 L	1	16	----	1/2
CPMA DISABLE L	1	16	----	2
D L	1*	30	TRI	2
DATA 0 L	2	16	3-OC	2
DATA 1 L	2	16	2-OC	2
DATA 2 L	2	16	3-OC	2
DATA 3 L	2	16	2-OC	2
DATA 4 L	2	16	3-OC	2
DATA 5 L	2	16	2-OC	2
DATA 6 L	2	16	2-OC	2
DATA 7 L	2	16	2-OC	2
DATA 8 L	2	16	2-OC	2
DATA 9 L	2	16	2-OC	2
DATA 10 L	2	16	2-OC	2
DATA 11 L	2	16	2-OC	2
E L	1*	30	TRI	4
EMA0 L	2	30	----	----
EMA1 L	2	30	----	----
EMA2 L	2	30	----	----
F L	1*	30	TRI	7
FSET L	1	Do not drive TTL output	1-OC	----
IND1 L	1	16	----	1
IND2 L	1	16	----	1
INHIBIT H	5	Do not drive TTL output	1-TTL	----
INITIALIZE H	3	See Note 1	E.F.	1-UTI
INT IN PROG H	2	16	2-OC	4 1/2
INT RQST L	1	16	----	1-UTI
INT STROBE H	4	Do not drive TTL output	TTL	----
INTERNAL I/O L	1	16	1-OC	----
I/O PAUSE L	5	Do not drive TTL output	TTL	1
IR0 L	1*	16	TRI	1/2
IR1 L	1*	16	TRI	1/2
IR2 L	1*	16	TRI	1/2
KEY CONTROL L	1	16	1-OC	1 1/2
LA ENABLE L	1	16	1-OC	2 1/2
LINK DATA L	1	16	1-OC	1
LINK L	1	Do not drive	1-OC	----
LINK LOAD L	6	60	1-OC	1
MA 0 L	2*	30	TRI	1
MA 1 L	2*	30	TRI	1
MA 2 L	2*	30	TRI	1

Table 3-2 (Cont)
Load Resistor and Drivers Summary

Signal	Load Type	Driver Must Sink (mA)	Drivers	Number of Inputs (TTL)
MA 3 L	2*	30	TRI	1
MA 4 L	2*	30	TRI	1
MA 5 L	2*	30	TRI	1
MA 6 L	2*	30	TRI	1
MA 7 L	2*	30	TRI	1
MA 8 L	2*	30	TRI	1
MA 9 L	2*	30	TRI	1
MA 10 L	2*	30	TRI	1
MA 11 L	2*	30	TRI	1
MA, MS LOAD CONT L	1	16	———	1
MD 0 L	1*	16	TRI	4
MD 1 L	1*	16	TRI	4
MD 2 L	1*	16	TRI	4
MD 3 L	1*	16	TRI	4
MD 4 L	1*	16	TRI	2 1/2
MD 5 L	1*	16	TRI	4
MD 6 L	1*	16	TRI	3 1/2
MD 7 L	1*	16	TRI	3 1/2
MD 8 L	1*	16	TRI	3 1/2
MD 9 L	1*	16	TRI	2 1/2
MD 10 L	1*	16	TRI	3 1/2
MD 11 L	1*	16	TRI	3
MD DIR L	2	16	1-OC	1
MEM START L	2	16	1-OC	2
MS IR DISABLE L	1	16	1-OC	1
NOT LAST XFER L	1	16	———	3
NTS STALL L	2	16	———	1
OVERFLOW L	1	Do not drive	1-OC	———
POWER OK H	——	See Note 2	———	1-UTI
PULSE LA H	3	See Note 2	———	1
RES	1	16	———	———
RETURN H	5	Do not drive TTL output	TTL	———
ROM ADDRESS L	2	30	———	1
RUN L	——	Do not drive TTL output	TTL	———
SKIP L	1	16	———	1
SOURCE H	5	Do not drive TTL output	TTL	———
STOP L	1	16	3-OC	2
STROBE H	5	Do not drive TTL output	TTL	———
SW	2		———	———
TP1 H	4	Do not drive TTL output	TTL	———
TP2 H	4	Do not drive TTL output	TTL	3
TP3 H	4	Do not drive TTL output	TTL	7
TP4 H	4	Do not drive TTL output	TTL	———
TS1 L	5	Do not drive TTL output	TTL	1

*Active pull-up when CPU tristate drivers are enabled.

Table 3-2 (Cont)
Load Resistor and Drivers Summary

Signal	Load Type	Driver Must Sink (mA)	Drivers	Number of Inputs (TTL)
TS2 L	5	Do not drive TTL output	TTL	----
TS3 L	5	Do not drive TTL output	TTL	3
TS4 L	5	Do not drive TTL output	TTL	2 1/2
USER MODE L	1	16	----	2
WRITE H	5	Do not drive TTL output	TTL	1

NOTES

1. INITIALIZE H and PULSE LA H. Driver must supply 30 mA at +3 V, and source less than 1 mA at ground. An emitter follower is recommended. Typical circuit is shown in Figure 3-26.

2. POWER OK H. This line is driven high by circuitry within the power supply, but can be grounded by options (such as the bootstrap loaders) which need to initialize the CPU and memory extension MA Control flip-flops. The power supply driver must supply a minimum of 30 mA at +3 V, and must not supply more than 100 mA when the output is shorted to ground. Peripheral drivers must sink 200 mA at 0.4 V, and sink less than 1 mA leakage at +5 V.

3. The DEC 8881 (P/N 19-09705) will meet the 16 and 30 mA requirement. Two 8881's in parallel will meet the 60 mA requirement.

LOAD 1: 470 Ω to +5 V, Clamp to +3 V.
LOAD 2: 390 Ω to +5 V, Clamp to +3 V.
LOAD 3: 2--470 Ω in series to -15 V, Clamp diode with anode ground.
LOAD 4: 390 Ω to +5 V, ferrite bead in series with pin to limit rise time.
LOAD 5: 390 Ω to +5 V, series ferrite bead, Clamp to +3 V on "finger" side of ferrite bead.
LOAD 6: 150 Ω to +5 V, Clamp to +3 V.
TRI = Tristate driver
UTI = Utilogic input (SIGNETICS 314, 380, 384 or equivalent)
OC = Open collector

3.12 DRIVE AVAILABLE FOR PERIPHERALS

Table 3-3 lists the currents that are available for driving options, memories, etc, from the CPU and memory extension. Signals marked * are generally not used as output from CPU or memory extension.

3.13 RECEIVERS AND LOAD RELIEF TECHNIQUES

The use of Utilogic gates (Signetics SP314, SP380, etc) or other high impedance circuits as bus receivers is strongly recommended. These gates have high threshold and low input drive, and thus present maximum noise immunity while introducing minimum bus reflections. Since 10 mA is available only on CPU timing and memory timing signals, buffering and load relief techniques must be used to decrease loading on the Omnibus.

A typical I/O decoder is shown in Figure 3-26. Note the use of buffered I/O PAUSE L. This signal keeps the MD receivers from loading the MD lines, since buffered I/O PAUSE L supplies all needed base current to the three gates on the MD lines unless I/O PAUSE L is low. Similar techniques should be employed for signals from DATA<0:11>L to peripherals.

Table 3-3
Omnibus Signal Drive Currents

Signal	Source mA @ +3	Sink mA @ GND
BREAK CYCLE L	3	5
BREAK DATA CONT L	3	5
BRK IN PROG L	3	5
BUS STROBE L	*	*
C<0:2>L	*	*
CPMA DISABLE L	*	*
D L	3	3
DATA<0:11>L	2	2
E L	3	3
EMA<0:2>L	3	3
F L	3	3
FSET L	5	5
IND1 L	*	*
IND2 L	*	*
INHIBIT H	10	10
INITIALIZE H	10	3
INT IN PROG H	2	2
INT RQST L	*	*
INT STROBE H	10	10
INTERNAL I/O	5	5
I/O PAUSE L	10	10
IR<0:2>L	3	3
KEY CONTROL L	3	3
LA ENABLE L	3	3
LINK DATA L	*	*
LINK L	5	5
LINK LOAD L	*	*
MA<0:11>L	5	5
MA, MS LOAD CONT L	*	*
MD<0:11>L	2	2
MD DIR L	3	3
MEM START L	*	*
MS, IR DISABLE L	*	*
NOT LAST XFER L	*	*
NTS STALL L	*	*
OVERFLOW L	5	5
RES	5	Depends on driver
RETURN H	10	10
ROM ADDRESS L	3	3
RUN L	5	5
SKIP L	*	*
SOURCE H	10	10
STOP L	*	*
STROBE H	10	10
TP<1:4>H	10	10 Each
TS<1:4>L	10	10 Each
USER MODE L	3	3
WRITE H	10	10

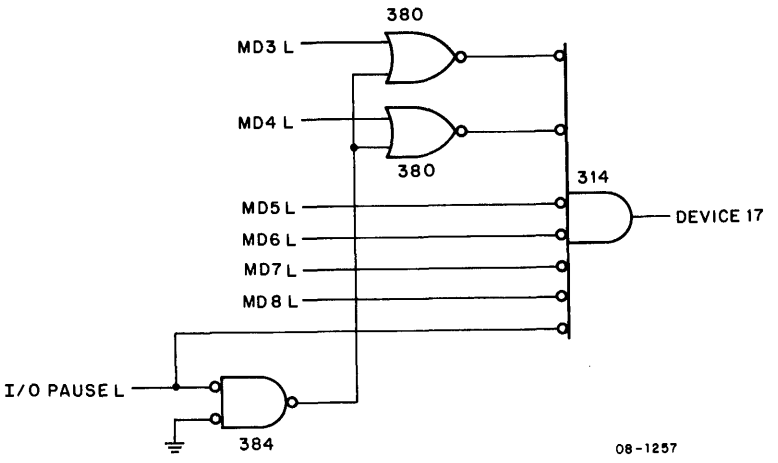


Figure 3-26 Typical I/O Decoder

3.14 INTERFACE EXAMPLES

This section provides the user with interface examples and timing for Programmed I/O, Interrupt, and Data Break transfers. For a more complete description of these examples refer to Chapter 9 of the *Miniprocessor Handbook.*

The interface examples contain some special integrated circuits. These IC's, which are listed below, were chosen to minimize loading on the Omnibus. Do not replace them with other devices having the same function unless you have compared input loading and threshold figures (for input devices) or output driver and leakage (for the output device).

Input Devices Device No.	**Manufacturer Type**	**DEC Part No.**
314	SIGNETICS SP314A	19-09704
380	SIGNETICS SP380A	19-09485
384	SIGNETICS SP384A	19-09486
Output Devices Device No.	**Manufacturer Type**	**DEC Part No.**
8881	Several 7438	19-09705

3.14.1 Programmed I/O Interface Example

The Programmed I/O Interface (Figure 3-27) that illustrates the most commonly used transfer consists of:

1. A device selection circuit
2. A device operations decoder
3. I/O control logic and
4. Input/output buffers.

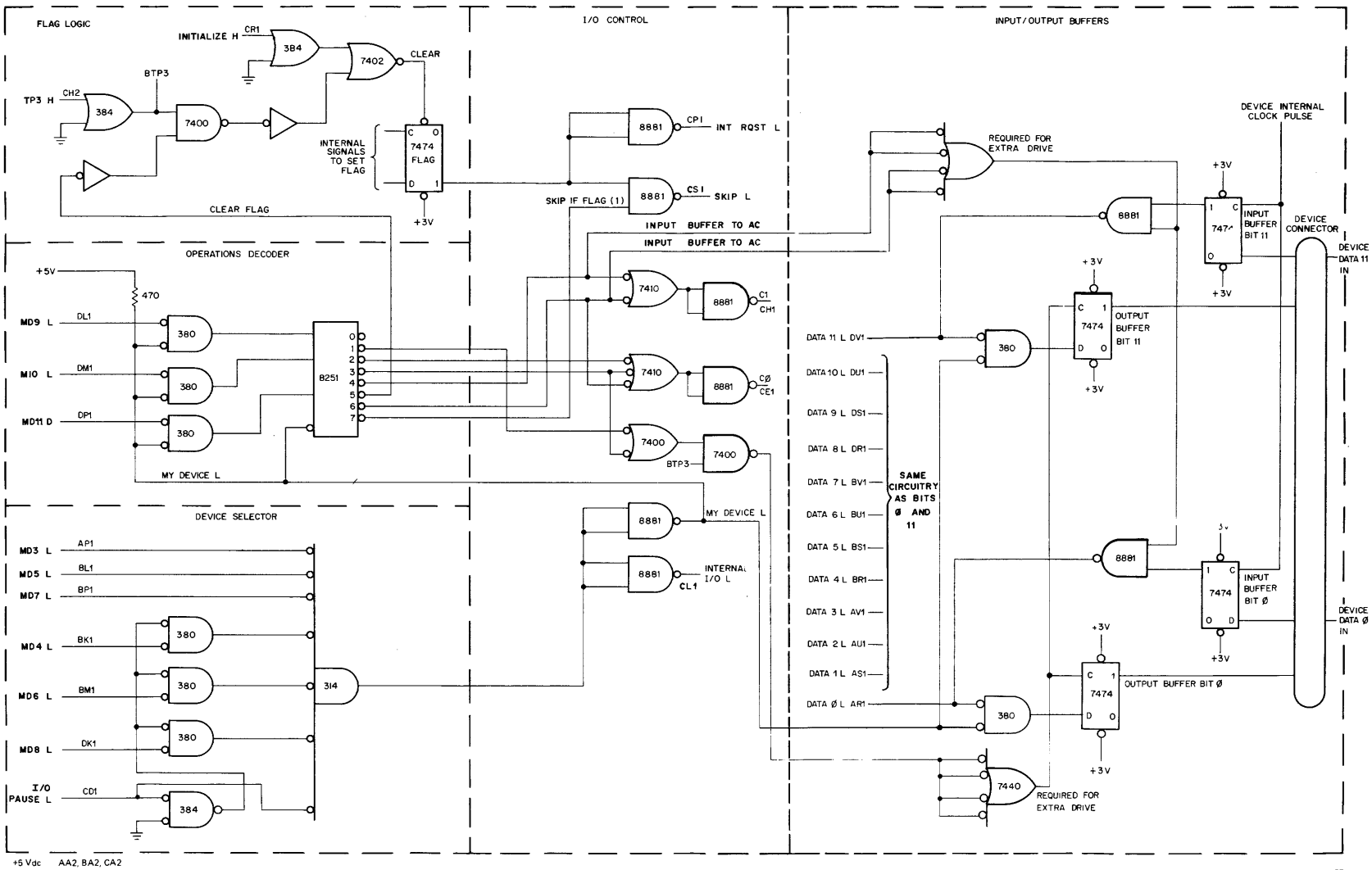


Figure 3-27 Sample Programmed I/O Interface

Device Selection Circuit – MD3-8 bits are used to carry the device select information. The example in Figure 3-27 shows the DEC380 and DEC314 being used as a simple device select and operations decoder. When octal 52 is received and signal I/O PAUSE L is asserted by the processor, gate 314 is qualified. The output is used to assert signals INTERNAL I/O L and MY DEVICE L. No operation can occur unless signal MY DEVICE L is asserted by the device selection decoder.

Operations Decoder – MD9-11 bits determine the type of operation to be performed. Three DEC380's are shown (Figure 3-27) receiving these bits. The outputs of these gates are in turn presented to a binary-to-octal decoder type 8251 and the decoded results control the interface. The IOTs in Table 3-4 illustrate the various types of transfers available.

Table 3-4
IOTs For Sample Interface

IOT	Function
6520	Not used.
6521	Transfer content of the AC to the output buffer.
6522	Clear the AC.
6523	Transfer the content of the AC to the output buffer and clear the AC.
6524	Transfer the content of the input buffer to the AC (OR transfer).
6525	Clear the flag.
6526	Transfer the content of the input buffer to the AC (jam transfer).
6527	Skip if flag is set (1).

3.14.2 Flag Logic

The flag is represented as a 7474 D-type flip-flop. The C and D inputs are used by the peripheral device to set the flag. If the flag is an input flag, it is set when data is loaded into the input holding register. If the flag is an output flag, it is set when the data in the output holding register has been processed by the peripheral, (i.e., when new data may be loaded into the output register without disturbing the output devices operation). Two flags are required for both input and output transfers.

3.14.3 Interrupt Request

The basic I/O interface may also be used to perform interrupt transfers by adding a gate to assert the interrupt request line when a flag is set by an external signal (Figure 3-25). The processor responds to the INT RQST line by completing the current instruction and then executing a JMS to location 0. Simultaneously, the interrupt system is turned off. The execution of the JMS instruction saves the current program count in location 0. It is up to the program to identify the interrupting device by polling (testing) device flags sequentially. After the device has been serviced, the interrupt service routine returns to the main program with a JMP indirect instruction. It is a good idea to have an interrupt gate in the logic even if the interrupt system is not going to be used. There is no penality for adding this gate because the CPU will not respond to the state of INT RQST unless the interrupt system is enabled or an SRQ instruction is fetched. Including this gate allows the user to recode the program for interrupt without changing the hardware.

3.14.4 Output Buffer

The output buffer receives processor data during IOT instructions and outputs data to a device under control of device timing. This buffer must be a D-type (edge-triggered) register. The command signal that loads the output buffer also initiates action within the peripheral. The output flag should be cleared at or before the time this buffer is loaded and should not be set again until the device has completely processed the data word.

3.14.5 Input Buffer

The input buffer receives device data at the device timing and applies the data to the data bus during an IOT instruction. The same signal that loads the input buffer is often used to set the input flag.

3.14.6 I/O Control

The I/O control includes INT RQST, which immediately responds when the flag is set; SKIP, which is asserted when IOT 6527 is decoded and the flag is set; C0 and C1, which may be asserted by the operations decoder during various conditions of data transfer; and input/output enabling logic, which responds to the operations decoder and controls the I/O buffers (Table 3-5).

3.14.7 Input/Output Timing for Programmed I/O Interfaces

A timing diagram corresponding to the programmed I/O interface example is illustrated in Figure 3-28. An explanation of the time periods from A to J is:

Period	Time	Function
A--D & E--J	350 ns	Time required to perform the transfer (PAUSE).
A--B & E--F	70 ns	Time required to decode the device selection and assert INTERNAL I/O.
A--C & E--H	100 ns	Time required to decode the IOT and assert the necessary "C" lines or SKIP and supply data if needed.
D & J		The time when the transfer takes place. Note that the data bus will change at this time. This is the reason that edge triggering must be used.

Note: The C lines control the direction of data transfer.

3.15 PROGRAM INTERRUPT TRANSFERS

The main difference between Programmed Interrupt transfers and Programmed I/O transfers is the software required. Chapter 6, Introduction to Programming, contains a thorough discussion of software for the interrupt system.

The hardware required for Interrupt transfers is the same as already described under Programmed I/O tranfers, except the gate driving INT RQST L is required.

3.15.1 Interrupt Timing

Within each IOT, timing is the same as that already described for Programmed I/O transfers. Since several devices may be simultaneously active using the interrupt system, the speed of response of the interrupt system is of interest.

The state of the interrupt system is sampled 350 ns before the end of every machine cycle. If a device requests an interrupt, the CPU will start executing the JMS to location 0, a maximum of 3 machine cycles plus 450 ns after receipt of the request. The JMS to location 0 takes one machine cycle, and the interrupt system is disabled in that same machine cycle. From this point on, the response time of the interrupt system depends on the instruction sequence of the interrupt handler. A typical interrupt handler program requires about 40 machine cycles to completely handle an interrupt. In critical cases, the user should count up the maximum number of machine cycles that can occur with the interrupt system disabled.

3.15.2 Data Break Interface Example

The basic break interface required to transfer data consists of a Break Memory Address register (BKMA) to address memory independently of the processor; a Break Priority Network to assure the activation of the device with the highest priority; Input/Output Buffers, and Break Control Logic. A sample data break interface is illustrated in Figure 3-29. The data break sequence of events is described in terms of the primary data break control signals and the processor timing given in Paragraph 3.7.5.

Table 3-5
Transfer Control Signals

Type of Transfer	Transfer Control Lines		Information Gated Onto the Data Bus	Bus Set-up Time with Respect to BUS STROBE	Action Required by Peripheral at Interface	Action by Processor	Contents of Data Bus During Transfer
	*C0	*C1					
Output AC Data Bus. AC unchanged.	H	H	AC Register	280 ns	Load data bus into buffer.	Transfers AC to Data Bus. AC remains unchanged.	AC register only. User modification of this type of transfer may bring undesirable results.
Output AC DATA Bus	L	H	AC Register	280 ns	Ground CO.	Transfers AC to Data Bus and clears AC.	AC Register.
AC Cleared					Load data bus into buffer.		
Input AC Peripheral Data	H	L	Peripheral Data and content of AC Register.	280 ns	Gate peripheral data to data bus. Ground C1.	Transfers content of AC to the Data Bus. The ORed result loaded into the AC.	AC ORed with Peripheral Data.
Input Jam. Data Bus AC.	L	L	Peripheral Data	280 ns	Gate peripheral data to data bus. Ground C0 and C1.	Transfer data bus to AC Register.	Peripheral Data.

*C0 is connected to pin CE1. C1 is connected to pin CH1 on the Omnibus.

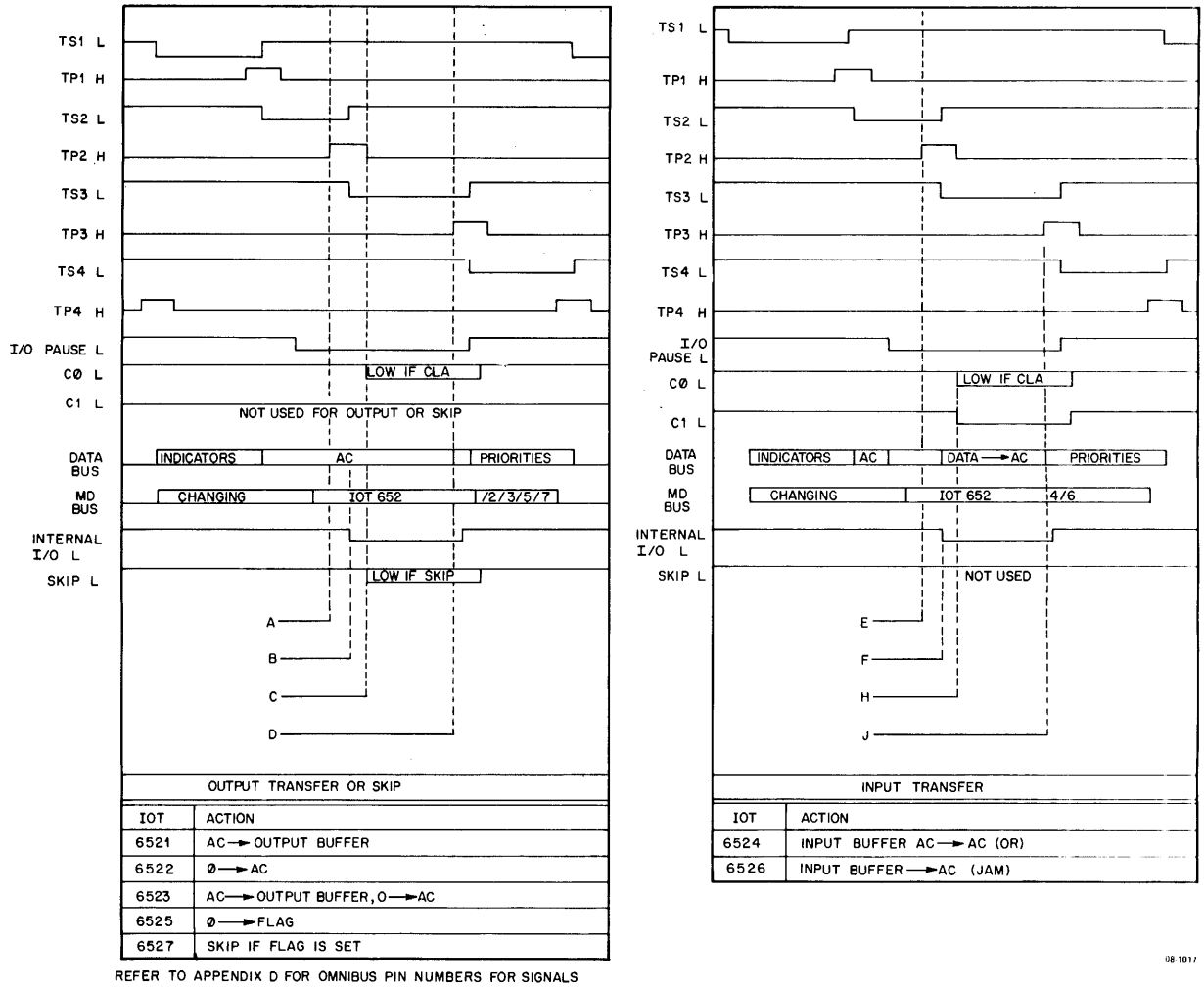


Figure 3-28 Timing for Sample Programmed I/O

3.15.3 Data Break Timing

The important timing consideration in data break (Figure 3-30), as in program interrupt, is whether sufficient time is available from the time the flag (in this case, the break request) is set to the time the data is moved in or out of memory. The PDP-8/A honors break requests between major states of an instruction. The break system is synchronized 350 ns before the end of every memory cycle. At the same time the processor tests for the possibility of interrupt, it tests for the possibility of break. The break system takes precedence over interrupts. Assuming no extendedI/O the processor requires no more than 1 memory cycle +400 ns to recognize a break request.

As a rule, the user should assign highest priority to the device that has data available for the shortest amount of time. The user should assume that all devices request data breaks simultaneously and calculate the response time of the break system as seen by each device to ensure that response time is less than the maximum allowable for that device.

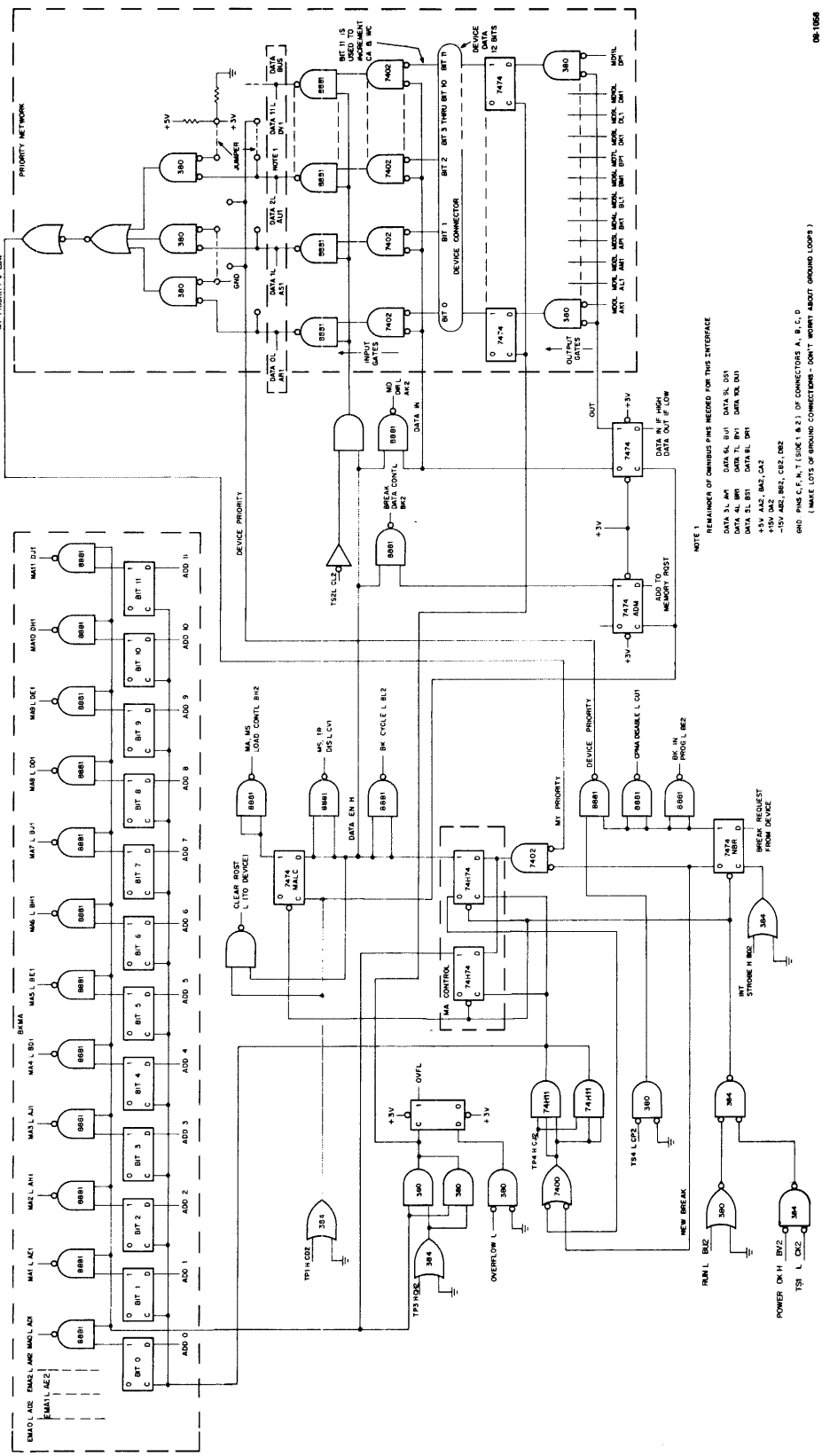


Figure 3-29 Sample One Cycle Data Break Interface

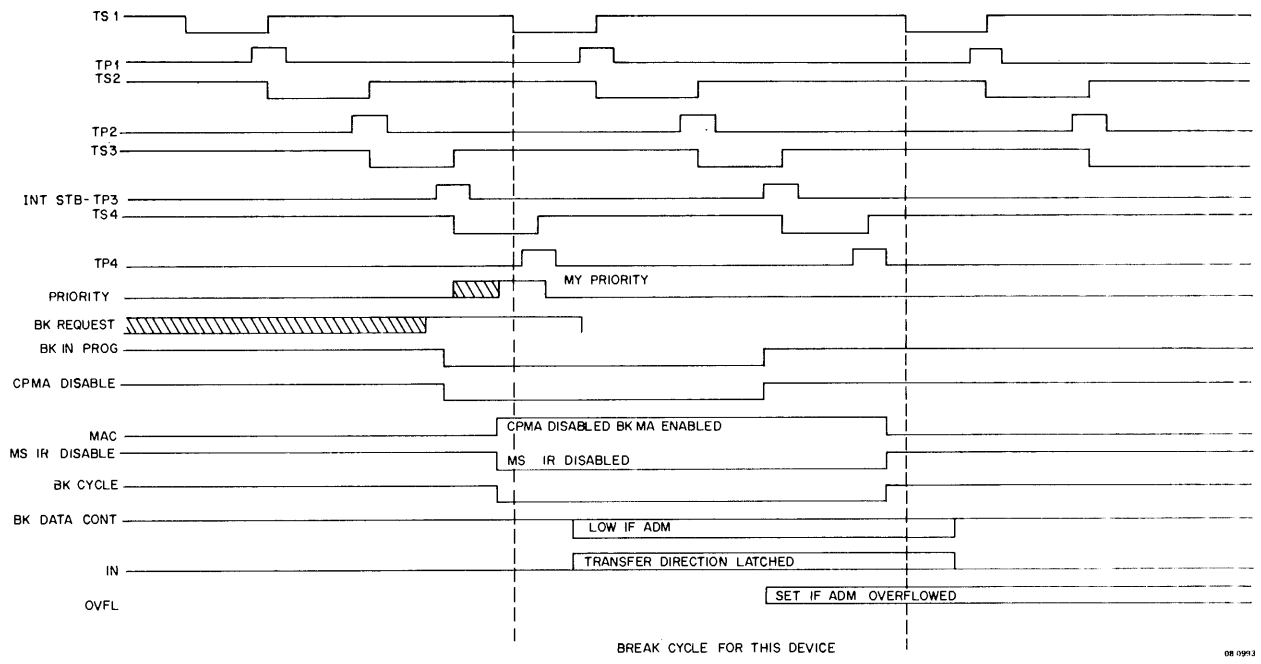


Figure 3-30 Data Break Control Timing Diagram

3.16 THREE-CYCLE DATA BREAK

It is possible to use memory locations as Word Count (WC) and Current Address (CA) registers by using a more complex DMA control. Figure 3-31 is a simplified diagram illustrating the interaction between the processor and a three-cycle data break device. The initial set-up and exit phases include operations similar to those required for a single-cycle data break; however, the data transfer phase of a three-cycle break is divided into a WC cycle, a CA cycle, and a data transfer cycle.

During initial set-up, the running program uses instructions to load the memory locations designated as the device WC and CA registers, then executes IOT instructions that initialize the device and specify any necessary transfer parameters. Once the device control circuitry has been enabled, the processor is free to perform other tasks while the peripheral accesses storage locations and executes the data break transfers.

Each three-cycle data break begins with a WC cycle during which the device gates the address of its WC register onto the Omnibus. The address is fixed (hardwired), and is usually an even number (bit 11 0) address. During the word count cycle, the contents of the word count location is returned from memory and applied to one leg of the processor's adder register. The device gates a 1 into the other adder inputs via the data bus, thereby incrementing the word count. The resulting addition is tested for overflow while the incremented word count is restored to memory. If overflow occurs, the peripheral clears its enabling circuits and sets its device flag as soon as the current transfer has been completed. In any event, the device concludes each WC cycle by testing the data bus to determine whether any higher priority device has entered a break request.

If there is no higher priority request on the data bus, the device immediately begins its CA cycle. The CA memory address is usually one greater than the WC address. The CA memory location is incremented in the manner just described, and the incremented value is restored to memory and also transferred to the device break address register. Break priority is tested again at the end of the CA cycle.

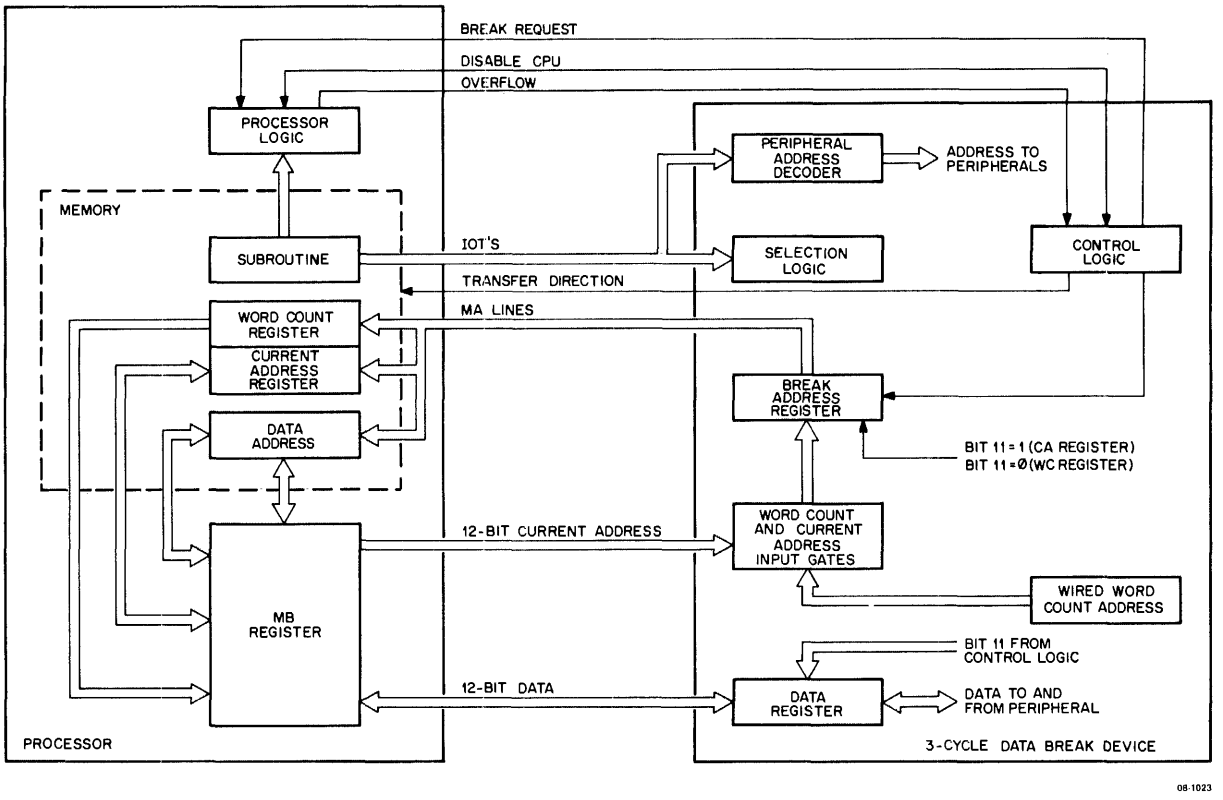


Figure 3-31 Three Cycle Data Break Simplified Block Diagram

During the data transfer cycle, the peripheral generates a signal to specify the direction of the transfer, gates the contents of its break address register onto the Omnibus, and either accepts or transmits one word of data. If WC overflow did not occur during the WC cycle, the device relinquishes control of the processor and begins to prepare for the next data transfer. When WC overflow does occur, the device flag is set and the running program executes IOT instructions to perform any operations that may be required to terminate the block I/O process.

Chapter 5 of *Introduction To Programming* contains the necessary information to program a three cycle data break device.

3.17 GENERAL CAUTIONS REGARDING INTERFACE DESIGN

1. Minimize capacitance on the Omnibus lines. The Omnibus will work properly only if the 100 ns allowed for bus charge time is met. Limit wire lengths on interface modules to 6 inches per signal. In general, this requirement means you should place bus receivers and drivers near the pins (which you will do anyway to minimize the crossovers if making a printed circuit board).

2. Good ground grids on interface boards are mandatory.

3. Observe normal TTL rules for +5 volt bypassing. (Normal DIGITAL bypassing is 0.01 mfd per IC, plus a 6.8 mfd tantalum capacitor where power supply voltage enters board.)

4. Except when gating EMA<0:2>L and MD<0:11>L to bus (50 ns max), a peripheral has 100 ns to react.

3.18 TRANSMISSION LINE EFFECTS

Rise-times on the Omnibus are generally long compared to propagation velocities. Hence most Omnibus signals should be treated as capacitively-loaded lines.

Some signals driven by TTL drivers are a different matter entirely. These signals must be kept short (less than 1 foot) and critical rise times controlled.

The signals which must be so treated are the nine CPU timing signals, the five memory timing signals, and I/O PAUSE L.

The characteristic impedance of the Omnibus itself (about 120 ohms) is a very small part of the overall picture. Of far more importance is the value and position of the capacitive load presented by boards connected to the Omnibus.

3.19 EXTERNAL BUS

There are two additional basic techniques of receiving and sending data to the Omnibus:

1. Using the KA8-E Positive I/O Bus Interface option.

2. Using the KA8-E Positive I/O Bus Interface and the KD8-E Data Break Interface.

3.19.1 Positive I/O Bus Interfacing

Previous discussions have brought out the fact that peripherals can be interfaced with either the Omnibus or the external bus. This means that a PDP-8/A user can utilize not only devices designed exclusively for the PDP-8/A, but also devices originally designed for use with the PDP-8/I and PDP-8/L computers – and even devices of his own manufacture.

This paragraph deals with the external bus, its applications, and the technique of interfacing peripherals to the bus. Equipment that was designed for the PDP-8/I and PDP-8/L may be used by interfacing to the external bus; it can also be used with the PDP-8/A. The user may want to transfer data between the PDP-8/A and a remote location. The external bus, which is designed to drive long interconnecting lines, is ideally suited for this application.

This paragraph is intended to answer general question about the external bus and its relationship to the Omnibus. For a detailed description and timing information about the KA8-E and KD8-E; refer to Volume II of the *PDP-8/E Maintenance Manual.* You may obtain a copy of this manual from Digital Equipment Corporation, Communications Services, 146 Main Street, Maynard Massachusetts, 01754.

3.19.2 The Nature of the External Bus

The external bus is a number of signal lines (88, excluding grounds) that enable data transfers between the PDP-8/A and peripherals. These lines carry data and control signals between the peripheral and two interface boards – the Positive I/O Bus Interface (KA8-E) and the Data Break Interface (KD8-E) that plug into the PDP-8/A Omnibus. These two boards convert the Omnibus signals into PDP-8/I and PDP-8/L-type bus signals. For instance, PDP-8/I peripherals need IOP pulses to perform instructions. The PDP-8/A does not generate internal IOP pulses, but it does provide signals (MD bits 09, 10, and 11) that can be converted into IOP pulses by the Positive I/O Bus interface. Other signals normally required by these peripherals are, in essence, available on the Omnibus. For example, BAC (buffered accumulator) bits must be supplied for the PDP-8/I peripherals. The PDP-8/A data lines carry the necessary accumulator information. The Positive I/O Bus Interface merely buffers the DATA bits and, thus, provides the external bus BAC signals.

Although the external bus consists of signal lines from both the Positive I/O Bus Interface and the Data Break Interface, it is not always necessary to use both boards. When only Programmed I/O transfer peripherals are used, the Positive I/O Bus Interface provides all the necessary signals. If data break peripherals are to be connected, both interfaces must be used. Because each data break peripheral requires its own data break interface board, the number of signal lines comprising the bus may vary. There may be as many as 12 of these data break peripherals connected in the system, each contributing 36 signal lines to the external bus. Figure 3-32 illustrates the bus and its use when applied to a series of peripherals.

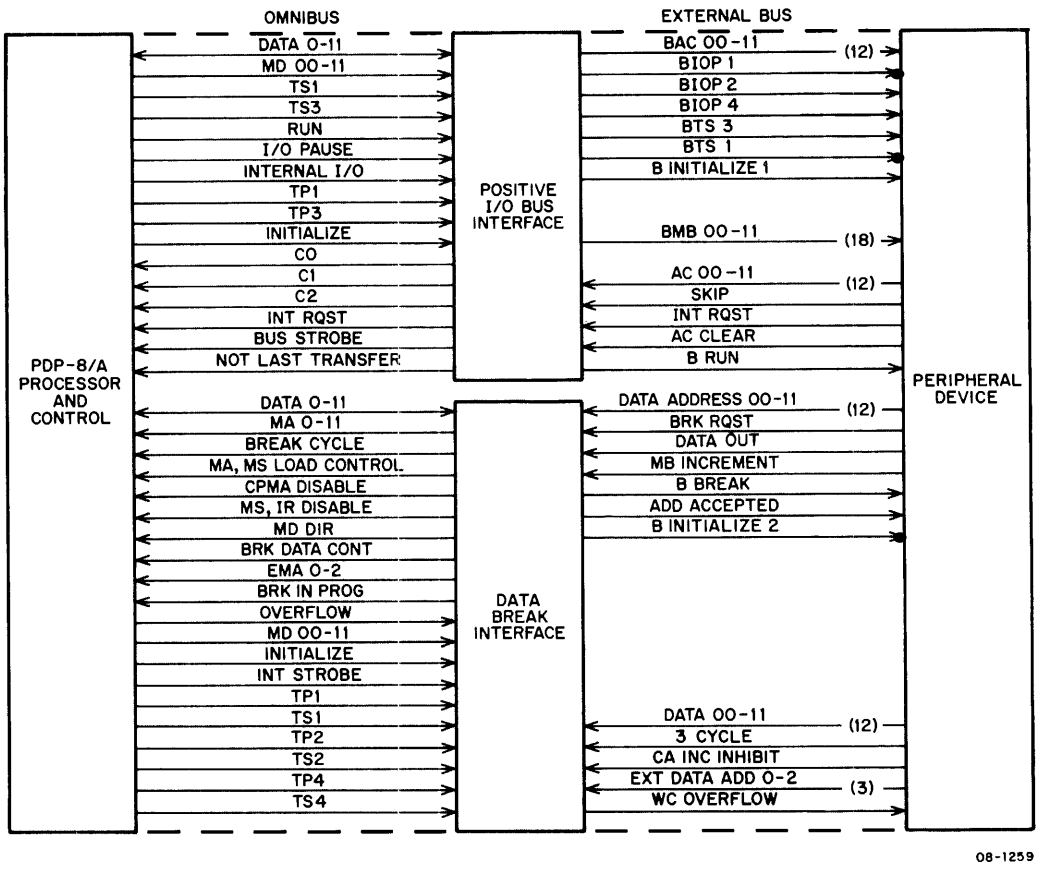


Figure 3-32 Parallel Connection of Peripherals

3.19.3 External Bus Signals

Figure 3-33 shows not only the external bus signals, but also those Omnibus signals that are used by the two interfaces. Signal directions are shown for both buses. Some of the Omnibus signals – DATA 0-11, for instance – are common to both interfaces, but for clarity this commonality has been disregarded. The external bus signals are grouped according to the interface connector where they originate. Paragraph 3.19.4 lists the bus signals and the connector and pin where each may be found). When similar signal lines are represented by one line of the drawing, as BAC 00-11, the actual number of lines is indicated in parentheses. The external bus signals are discussed in detail in the following paragraph with emphasis on the relationship between these signals and the Omnibus signals.

3.19.4 External Bus Signals

3.19.4.1 BAC 00-11 – These signals represent the content of the PDP-8/A Accumulator register (AC). Information in the AC is transferred on the Omnibus data lines to the Positive I/O Bus Interface. The interface buffers the signal and provides the BAC output. The BAC bits are strobed into registers in the peripheral when an IOT instruction is generated. 1 = +3 V.

3.19.4.2 AC 00-11 – The signals on these lines represent the contents of a register in the peripheral. This information is transferred to the Positive I/O Bus Interface where it is put on the data lines for transfer to the PDP-8/A AC. 1 = GND.

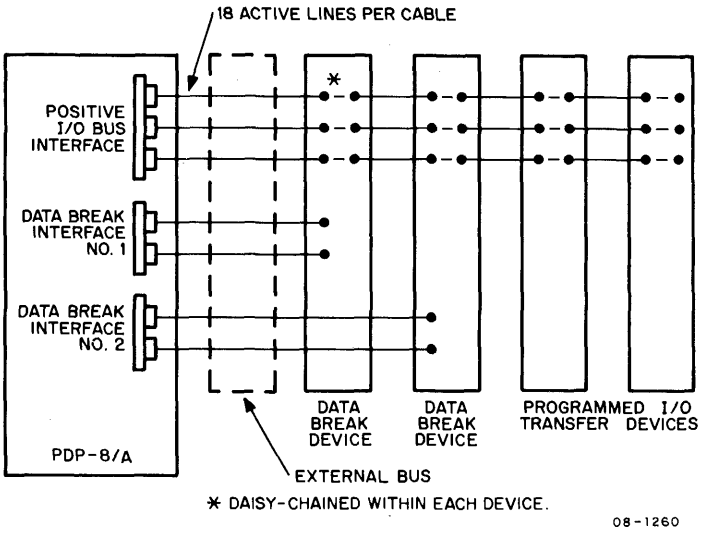


Figure 3-33 External Bus Signals and Related Omnibus Signals

3.19.4.3 BMB 00-11 – The signals on these lines represent the contents of the Memory Sense registers. This information is transferred from memory on the Memory Data (MD) lines. The MD lines are monitored by the positive I/O bus interface and the signals are converted to the BMB bits. These bits are used during IOT instructions; BMB03-08 carry the device selection code, while BMB09-11 are converted to BIOP pulses. 1 = +3 V.

3.19.4.4 BIOP 1, 2, and 4 – These pulses are generated in response to the voltage levels on MD09-11 (BIOP4-1, respectively). These pulses generate IOT pulses within the peripheral, causing it to perform a certain operation. The width of the BIOP pulses and the interval between pulses are variable and can be adjusted on the Positive I/O Bus Interface. Pulse = +3 V.

3.19.4.5 BTS1, BTS3 – These signals represent the TS1 and TS3 signals of the Omnibus. They synchronize operations in the peripheral with those in the computer and perform functions peculiar to the peripheral. They are primarily used in data break timing. Pulse = +3 V.

3.19.4.6 B RUN – If this signal is GND, the computer is executing instructions.

3.19.4.7 AC CLEAR – When this signal is asserted (brought to GND) along with the AC bits, the result is a jam transfer of data to the AC. The signal may also be asserted by a separate IOP, clearing the AC.

3.19.4.8 SKIP – SKIP is asserted (grounded) by an IOT instruction. It causes the next sequential instruction to be skipped. If the SKIP bus is asserted during more than one IOT of an I/O instruction, the program skips a corresponding number of instructions. No more than three skips can be made by a single instruction.

3.19.4.9 B INITIALIZE 1 – This 600 ns duration positive pulse is used to clear AC and link and to clear all flags in peripherals. It is generated at power turn on, and by the Clear All Flags (CAF) IOT, 6007.

3.19.4.10 DATA 00-11* – These lines transfer data from a data break peripheral to the data break interface. The peripheral transfers the information when it receives the B BREAK signal from the interface, indicating the start of the true break cycle. At TS2 of this break cycle, the data break interface transfers the data to the Omnibus DATA 0-11 lines, which carry the data to the PDP-8/A memory buffer. 1 = GND.

*Pertains to DATA Break interface only.

3.19.4.11 B BREAK* – This signal is generated in the data break interface and transferred to the peripheral, where it enables a parallel loading of data, either into or out of the peripheral. The data break interface, in addition to generating B BREAK, asserts the Omnibus BREAK CYCLE line, notifying the computer that the break cycle has begun. 1 = GND.

3.19.4.12 DATA OUT* – This signal is produced by the peripheral and sampled by the data break interface. When DATA OUT is asserted (grounded) during the break cycle, data is transferred from the computer's memory to the peripheral.

3.19.4.13 DATA ADD 00-11* – These lines transfer address information from the peripheral to the OMNIBUS MA lines. If the peripheral is a 3-cycle break device, the address represents the memory location of the word count. Since this location is always the same for a 3-cycle device, the DATA ADDRESS lines are hard-wired in the peripheral. This address must be even (ending in 0, 2, 4, or 6) for word count. The data stored in this location represents the 2's complement of the number of data words to be transferred. The next sequential location is read from memory as the Current Address register.

The data stored in this location represents the memory address of the data to be transferred. If the peripheral is a 1-cycle break device, the address on the DATA ADDRESS lines is provided by a register in the peripheral and represents the memory address of the data to be transferred. The address on the DATA ADDRESS lines is sampled by the TP4 pulse. The OMNIBUS CPMA DISABLE line is asserted by the data break interface at TP4 to enable the DATA ADDRESS information to be placed on the MA lines. 1 = GND.

3.19.4.14 BRK RQST* – This signal is asserted (brought to ground) by the peripheral when it is ready for a word transfer. When BRK RQST is present at INT STROBE time, the data break operation is entered. The OMNIBUS INT IN PROG line is asserted, and a load enable signal is provided for the data break interface break memory address (BKMA) register.

3.19.4.15 ADD ACCEPTED* – This signal is generated by the data break interface when a BRK RQST signal has initiated the data break operation. ADD ACCEPTED is used in the peripheral to clear the BRK RQST flip-flop. Pulse = GND.

3.19.4.16 MB INCREMENT* – When this signal is at ground level during the true break cycle, the contents of the memory location are acted upon as outlined in the following table.

MB Increment	Data Out	Operation Performed	Descriptive Term Used for Operation
Low	Low	Contents of the memory location are incremented.	MB INC
Low	High	Data on the DATA 00–11 lines is added to the contents of the memory location.	Add to Memory (ADM)

3.19.4.17 CA INCREMENT INH* – When this signal is asserted (grounded) during the CA cycle of a 3-cycle data break, the CA is not incremented.

3.19.4.18 3 CYCLE* – This signal is transferred from the peripheral to the data break interface to notify the interface logic to set either the WC flip-flop (3-cycle transfer) (ground input) or the B flip-flop (1-cycle transfer).

3.19.4.19 WC OVERFLOW* – The interface transfers this signal to the peripheral to notify it that the word count location in memory has become zero and that the data transfer should end. The signal is also present when overflow occurs during MB increment or ADM. Pulse = GND.

*Pertains to DATA Break interface only.

3.19.4.20 EXT DATA ADD 0-2* – These three lines are used when a KM8-AA Memory Extension and Timeshare interface is included in the basic PDP-8/A. The peripheral uses the lines to indicate the particular memory field involved in the transfer.4

During a 3-cycle data break, WC and CA cycles always occur in field 0, while only the B cycle occurs in the field specified by the extended data address. 1 = GND.

3.19.4.21 B INITIALIZE 2* – This positive signal clears all flags in the peripheral and is essentially the INITIALIZE signal of the Omnibus. It is used by the break device in lieu of B INITIALIZE 1 to reduce loading on the latter.

*Pertains to Data Break interface only.

CHAPTER 4
CENTRAL PROCESSOR UNIT

4.1 CENTRAL PROCESSOR UNIT, GENERAL DESCRIPTION

The detailed description of the central processor unit (CPU) relies on logic drawings extracted from the complete set of drawings and schematics that appear in Appendix H. The extracted drawings are functional and often comprise logic from more than one sheet of the complete set. Generally, the extracts do not include integrated circuit pin numbers; these can be found in the print set. Appendix H also contains flow diagrams that relate to the significant CPU operations. Become familiar with these flow diagrams; they not only describe the overall CPU operation concisely, but also help you understand difficult areas in the detailed logic descriptions.

The CPU manipulates data in response to a predetemined sequence of instructions. In the PDP-8/A both the data and the instructions are stored in memory. An instruction is brought from memory to the processor where it is decoded to determine, first, what to do to the data, and second, what data is affected. When the data has been manipulated, the result is stored within the processor, transferred to a memory location, or transferred to some peripheral equipment.

The CPU logic is contained on a hex-size printed circuit board that plugs into the Omnibus and is assigned the module designation M8315. Because the Omnibus accepts only four printed circuit board connectors, two of the connectors (E and F) extend off the Omnibus. The fingers on these connectors are test points that provide access to certain significant signals in the Instruction Decoder and in the Timing Generator. These test points are shown in the logic drawings (CS M8315-0-1) in Appendix H of this manual.

Figure 4-1 is a block diagram of the CPU. The Programmer's Console, although not physically part of the CPU, is functionally inseparable. The operator can communicate with the major registers and cause data transfers to occur by operating various console buttons. Data is transferred between the console and the processor on the DATA lines in response to control signals generated within the console logic. The console is provided at the customer's option; a Limited Function Panel (not illustrated in the block diagram) is provided with each PDP-8/A. This panel enables an operator to turn power on, to lock out most of the Programmer's Console functions (if the console is part of the system), and to initiate memory and processor timing, provided certain options are plugged into the Omnibus.

The basic timing cycle of the PDP-8/A is 1.5 μs and is divided into four time states. The Timing Generator (TG), besides determining the basic timing cycle, provides the synchronizing signals that enable specific CPU operations to occur during assigned time states. These synchronizing signals are applied to all CPU functional sections as well as to memory and to options and peripherals.

To perform all the operations involved in retrieving, storing, and modifying information, the CPU utilizes the major registers. Data is transferred between registers, between registers and memory (via the Omnibus MD lines), between registers and peripherals (via the Omnibus DATA lines), and between registers and internal options. Transfers are accomplished by a major register gating network that selects the particular register to take part in the transfer and performs some operation on the data being transferred. The selection and operation performed are determined by control signals developed within the Instruction Decoder (ID); the ID also provides the control signals that determine the destination of the transferred data.

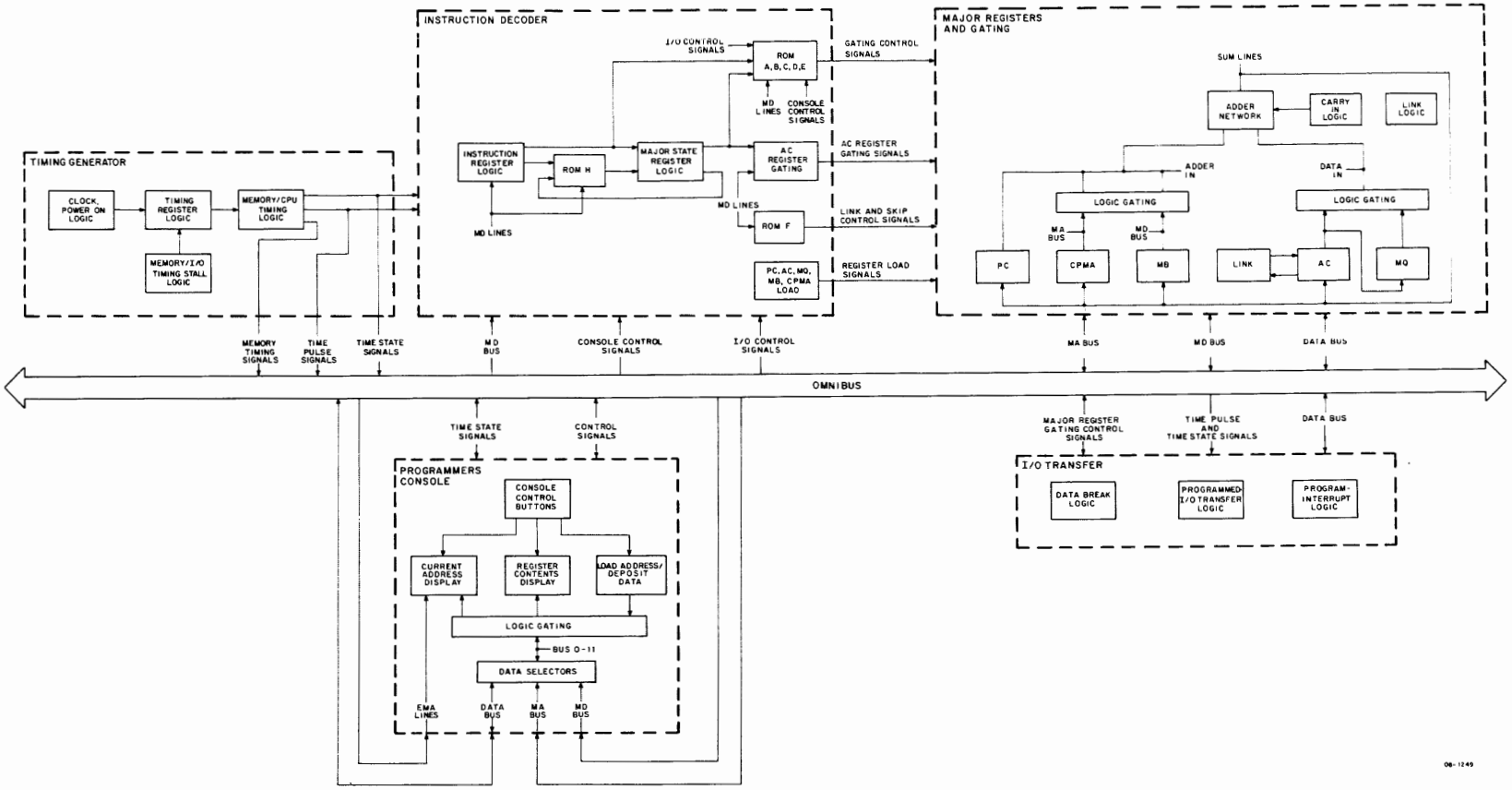


Figure 4-1 CPU Block Diagram

The signals that control the major registers and their gating are developed within the ID largely in response to three variables:

1. Basic instructions (as decoded by the Instruction Register logic)

2. Processor major states (as determined by the Major State Register logic)

3. Time states and time pulses.

These variables are combined in a number of Read-Only Memories (ROMs) to produce control signals that make the major register gating network function.

4.2 TIMING GENERATOR

The various PDP-8/A operations take place in designated time periods of the operating cycle. These time periods are delimited by signals produced in the Timing Generator, located on the CPU printed circuit card. Signals TS1 through TS4 divide the timing cycle into four nearly-equal states, while signals TP1 through TP4 identify the end of each time state; these two groups of signals form the foundation for all control signals used in the CPU and in memory.

Figure 4-2 is a block diagram of the Timing Generator. Central to the generator is the Timing Register logic that provides gating signals for both the CPU Timing logic and the Memory Timing logic. Basic inputs to the Timing Register logic are supplied by a crystal-controlled clock and by initializing logic that operates when power is applied to the CPU and when the user initiates timing. Normal operation of the Timing Register logic can be modified by either the Memory Stall logic or the I/O Transfer Stall logic. The former suspends timing to accommodate memory that has a slower-than-normal cycle time; the latter suspends timing to facilitate multiple I/O transfers between the CPU and a peripheral.

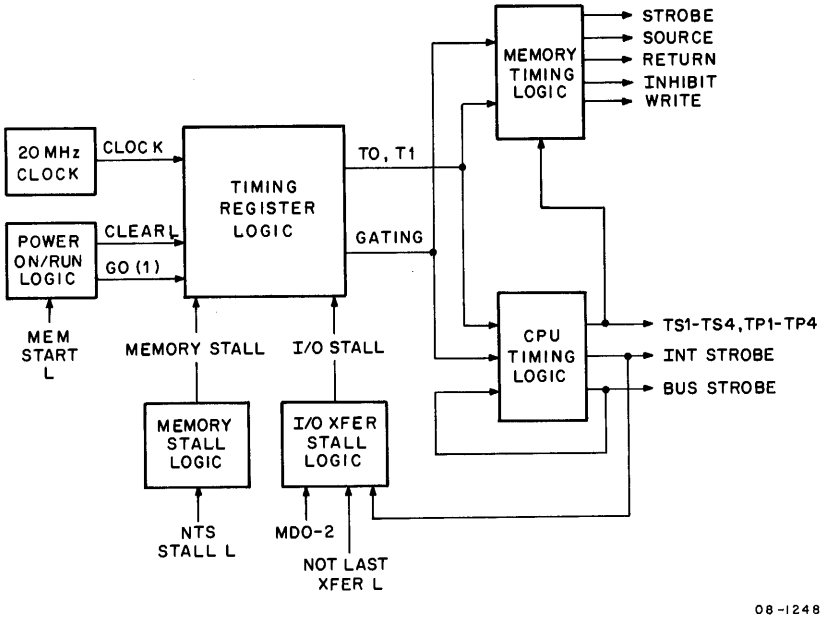


Figure 4-2 Timing Generator Block Diagram

4.2.1 Power On/Run Logic

The Power On/Run logic is shown in Figure 4-3. The CLEAR L signal and the GO(1) signal are generated in this logic and are used to begin the timing register operation. The RUN L signal is also produced and is used by the front panel to indicate that timing cycles are being generated. Included in this logic is the auto-start circuit that enables a user to have a program begin automatically at a pre-selected address.

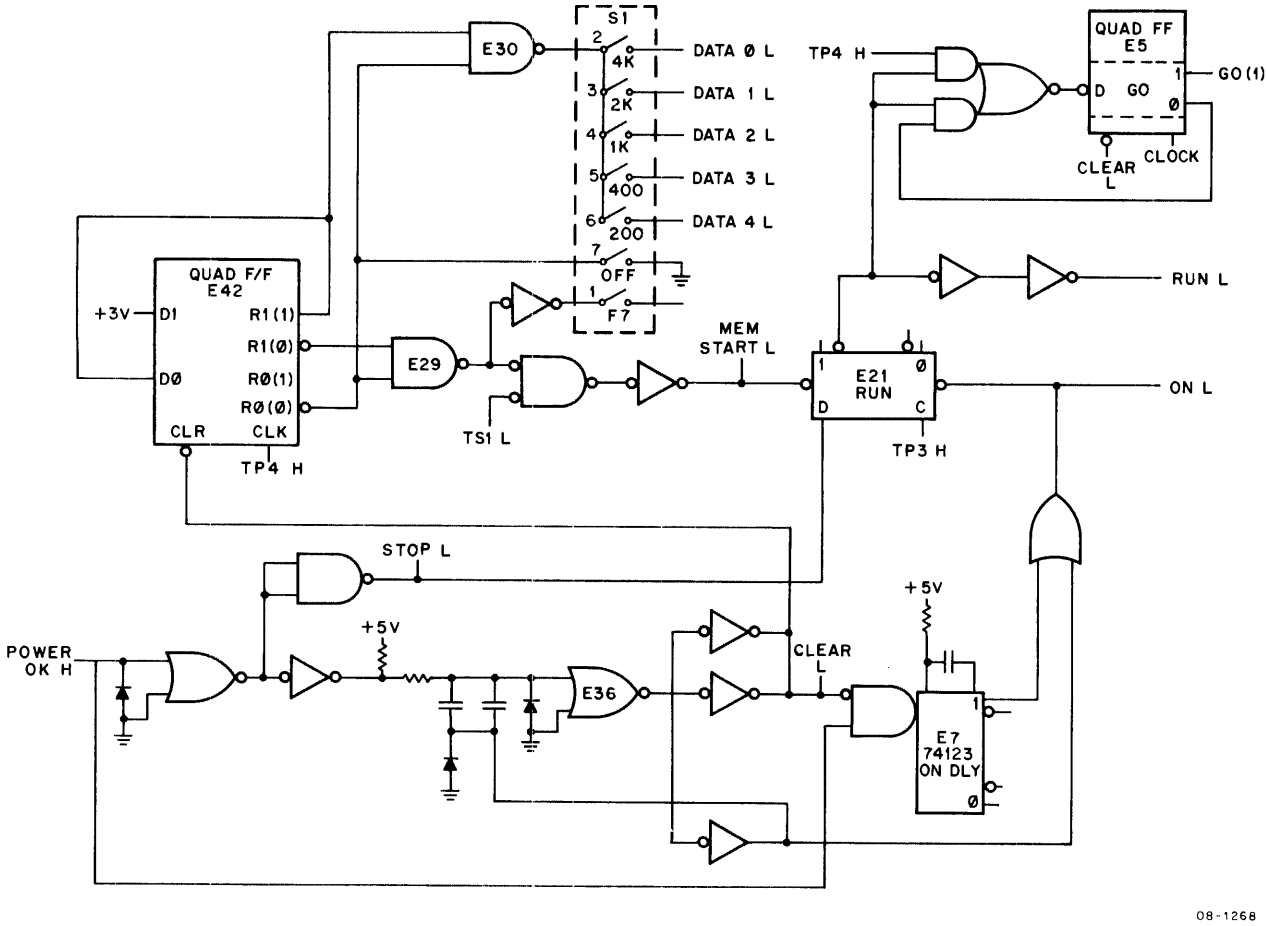


Figure 4-3 Power ON/RUN Logic

When the power is turned on, POWER OK H (a logic signal generated in the dc power supplies) remains low until the dc voltages have attained a predetermined value. Throughout the time that POWER OK H is low, the CLEAR L signal is asserted. Also, during this time, the dc voltages, while not yet at the predetermined value, are of sufficient magnitude to allow the logic to operate. Consequently, the ON L signal is generated, holding the RUN flip-flop in the clear state. When POWER OK H is asserted, the ON DLY one-shot multivibrator is triggered (CLEAR L is negated approximately 30 μs later because of the delay circuit that includes NOR gate E36; this delay has greater significance when POWER OK H is negated for some reason, as will be shown later in this section). The ON L signal remains low 100 ms, long enough for all memory circuits to stabilize before operations are attempted.

When the ON L signal is negated, the RUN flip-flop can be set if MEM START L is asserted. MEM START L can be asserted automatically or manually, depending on the user's wish. For the moment, assume that the auto-start feature is disabled and the user causes the MEM START L signal to go low by pushing the RUN button on the Programmer's Console. The RUN flip-flop is set, asserting the RUN L signal and enabling the next clock pulse to set the GO flip-flop. The resulting high GO(1) signal permits the Timing Register to begin its shifting operation.

The MEM START L signal can be asserted automatically soon after ON L is generated. The CLEAR L signal holds both E42 flip-flops in the clear state when power is applied. If the OFF contact of switch S1 is open, as shown in Figure 4-3, the MEM START L line is grounded (the Timing Generator is always in time state one – TSL L is asserted – when not running). Thus, as soon as ON L is negated, the RUN flip-flop is set by the MEM START L signal. The nature of the RUN flip-flop (DEC74S74) is such that when the clear and preset inputs are low at the same time, both the 1 and 0 outputs are high. When one of the inputs goes high, the other input then prevails. Thus, when ON L goes high, MEM START L sets the RUN flip-flop.

The auto-start feature is selected by the user with switch S1, a two-position switch with individually movable contacts. If the OFF contact is open, the auto-start feature is enabled; when this contact is closed (in the ON position), the resulting ground prevents automatic assertion of MEM START L. When auto-start is selected, the program begins automatically at the address specified by one of the top five contacts (Figure 4-3). Thus, if contact 4K is closed, the program will begin at address 4000(8); if contact 400 is closed, the program starts at address 0400(8) (although all five contacts may be left open, causing the program to start at address 0000(8), only one of the contacts may be closed at any time). If contact F7 is open, the address selected will be in instruction and data field 0; if F7 is closed, the address is in instruction and data field 7. When there is no memory extension control on the Omnibus, field 0 is selected regardless of the setting of contact F7. Refer to Paragraph 4.6.4, which describes the sequence of operation for the auto-start feature.

The Timing Generator can be halted by a program instruction, by various front panel operations, or by negation of the POWER OK H signal. All of these occurrences cause the STOP L signal to be asserted; the next TP3 H pulse clears the RUN flip-flop, and TP4 H then enables a clock pulse to clear the GO flip-flop. The timing halts at the beginning of TS1 L.

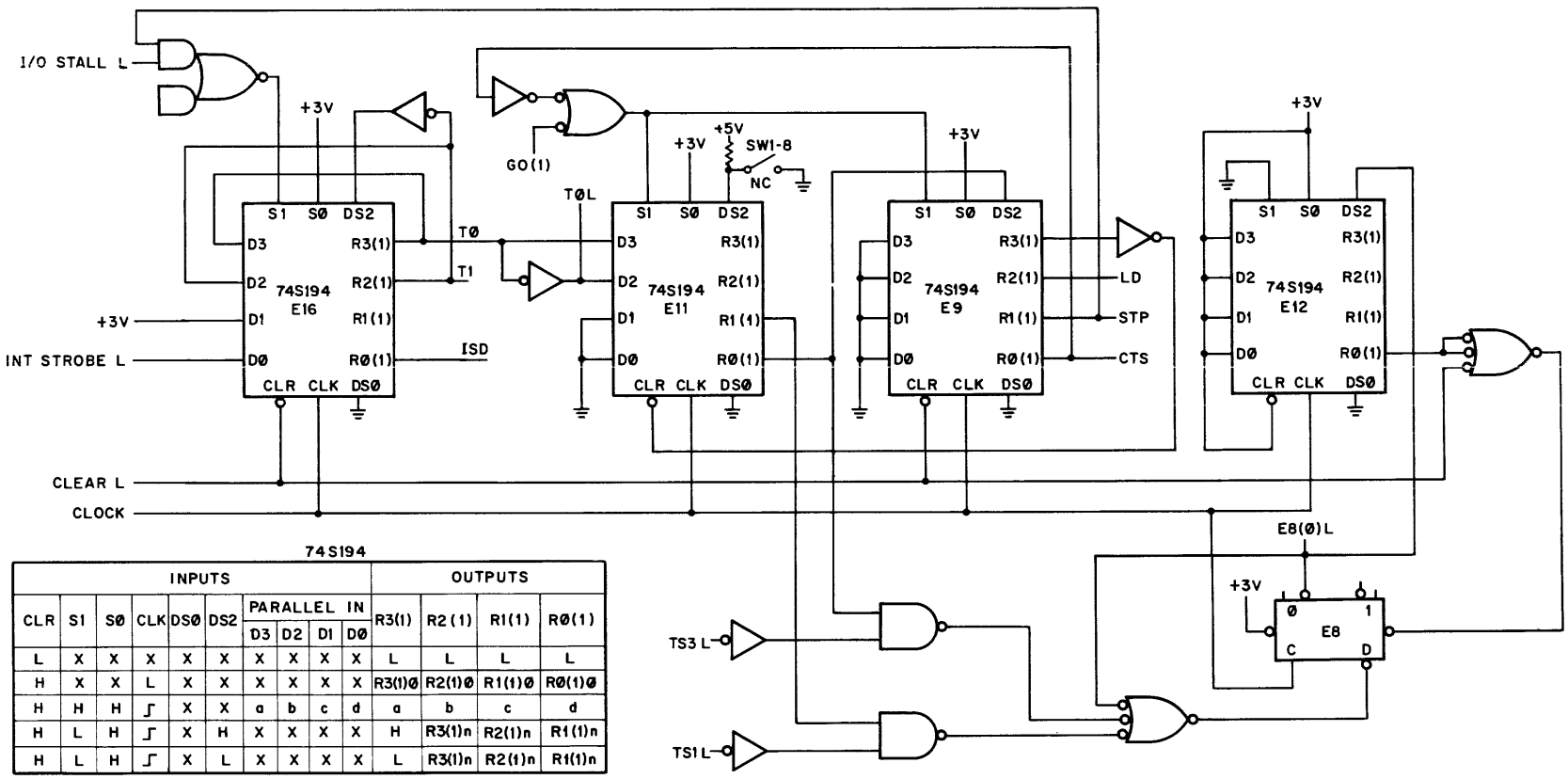
When POWER OK H goes low, because power is turned off or because a dc voltage drops below a desired level, a delay circuit prevents the CLEAR L signal from immediately clearing the GO(1) flip-flop, and, thereby halts timing prematurely (premature timing halt is undesirable because of the likelihood of altering the contents of core memory). Instead, the delay of approximately 30 μs ensures that the RUN and GO flip-flops are cleared at TP3 time and TP4 time, respectively; thus, timing proceeds to its normal conclusion.

4.2.2 Timing Register Logic

The Timing Register logic is shown in Figure 4-4. The register comprises four DEC74S194 integrated circuits – 4-bit, bi-directional, shift registers. The four registers are shown in the configuration that applies during normal operation, i.e., when neither of the stall networks is active.

The diagram in Figure 4-5 will help you visualize the process used to generate the timing signals. Conditions at time t_0 of this diagram can be characterized thusly: Power has been applied to the CPU; the 20 Mhz clock is producing clock pulses; the dc voltages have attained a level sufficient to assert the POWER OK H signal; timing has not yet been started by the user (MEM START L is high). Under these conditions the outputs of registers E9 and E16 are low, the outputs of E11, except R2(1), are low, and the outputs of E12 may be low or high, depending on the state of flip-flop E8 at power-on.

When the user causes MEM START L to be asserted, the GO flip-flop in the Power On/Run logic is set, asserting the GO(1) signal. Registers E9 and E11 are placed in the right shift mode. Each clock pulse shifts a low into R3(1) of E11, while shifting-down the high that began in R2(1). When the high is shifted into E9-R1(1), the STP (Set Time Pulse) signal places register E16 in the right shift mode. The next clock pulse causes E16-R3(1) (T0) to assume a state opposite to that exhibited by E16-R2(1) (T1) before the clock pulse. Simultaneously, the CTS signal places E9 and E11 in the parallel load mode. The new state of T0 is then loaded into E11, E11 and E9 revert to the right shift mode, and the shifting process is repeated. Each time the STP signal goes high, E16 is placed in the right shift mode and either T0 or T1 changes state. Because the change of state is coincidental with the transition of register stage E9-R0(1), the signal from this stage is called CTS (Change Time State), although the change is actually effected by the STP signal. The T0 and T1 signals, besides being essential in the Timing Generator, are used in the CPU to generate many major register gating signals.



74S194

INPUTS										OUTPUTS			
CLR	S1	SØ	CLK	DSØ	DS2	PARALLEL IN				R3(1)	R2(1)	R1(1)	RØ(1)
						D3	D2	D1	DØ				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	R3(1)Ø	R2(1)Ø	R1(1)Ø	RØ(1)Ø
H	H	H	⌐	X	X	a	b	c	d	a	b	c	d
H	L	H	⌐	X	H	X	X	X	X	H	R3(1)n	R2(1)n	R1(1)n
H	L	H	⌐	X	L	X	X	X	X	L	R3(1)n	R2(1)n	R1(1)n

X = Don't care
a, b, c, d = Level of steady-state inputs at D3, D2, D1, DØ.
RN(1)Ø = Level of RN(1) before the indicated steady-state conditions were established.
RN(1)n = Level of RN(1) before the most recent upward transition of the clock.

08-1250

Figure 4-4 Timing Register Logic

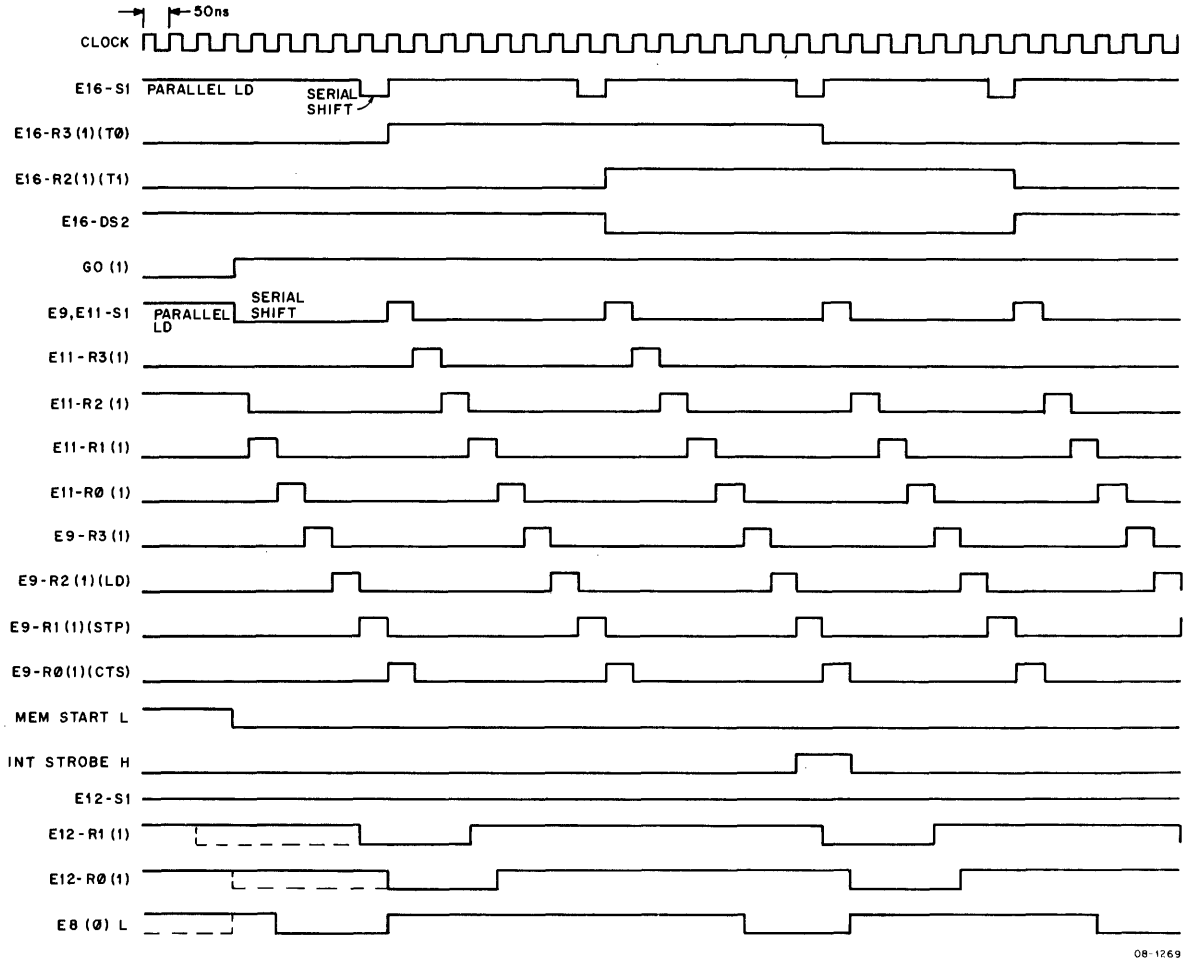


Figure 4-5 Timing Register Normal Timing

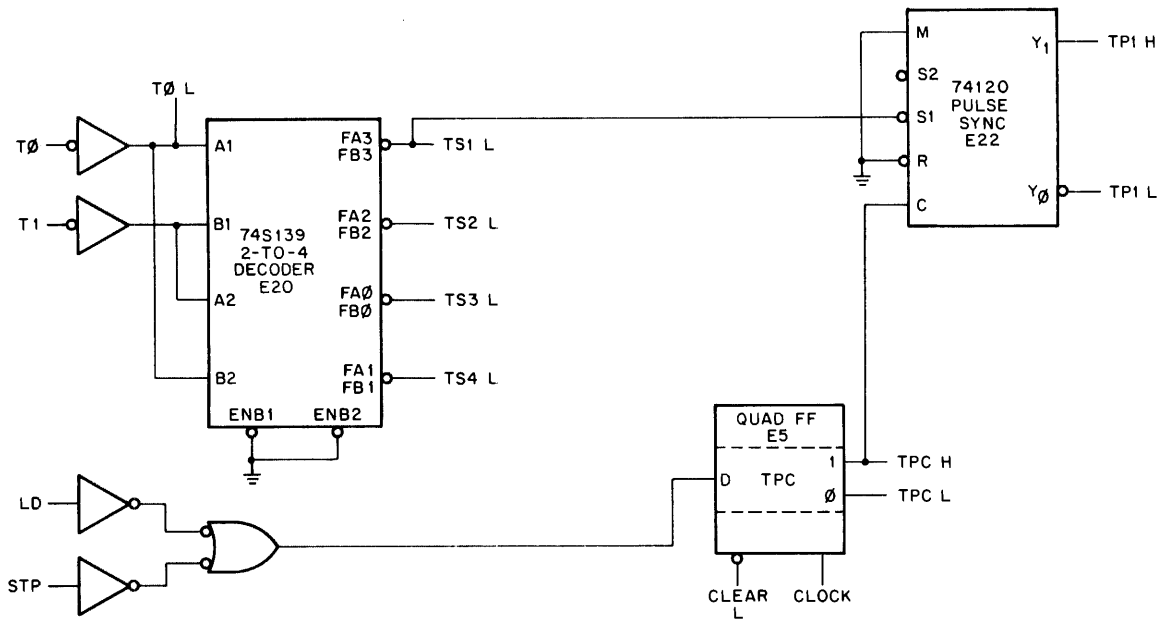
4.2.3 CPU Timing Logic

The CPU Timing logic is shown in Figure 4-6. The Timing Register signals T0 and T1 are applied to a decoder, DEC74S139, which generates the four time state signals (refer to the function table). Then each time state signal is applied to a pulse synchronizer, DEC74120, the associated time pulse signal is produced (the pulse synchronizers for TP2, TP3, and TP4 are not shown; they are similar to that of TP1).

The Timing Register signals LD and STP enable the clock to set and clear the TPC (Time Pulse Clock) flip-flop. The resulting TPC H signal acts as clock for the pulse synchronizer, generating a time pulse signal of 100 ns width. Figure 4-7 is a diagram of the CPU timing signals.

4.2.4 Memory Timing Logic

The Memory Timing logic is shown in Figure 4-8, while a timing diagram is given in Figure 4-9. STROBE H, SOURCE H, RETURN H, INHIBIT H, and WRITE H are used by memory to control the read and write portions of the timing cycle. RETURN H and SOURCE H, generated during both halves of the cycle, turn memory current on; the conjunction of these two signals determines the width of the current pulse. RETURN H remains high 50 ns longer than SOURCE H to ensure that the memory stack does not retain a capacitive charge. STROBE H, generated only during the read half of the cycle, provides a time reference from which the outputs of the sense amplifiers are sampled. WRITE H and INHIBIT H are asserted only during the write half of the cycle; WRITE H enables the proper read/write switches, while INHIBIT H turns on the inhibit drivers associated with memory control. Refer to Chapter 5 for details concerning memory operation.



74S139

INPUT		OUTPUT			
T0	T1	TS1 L	TS2 L	TS3 L	TS4 L
L	L	L	H	H	H
H	L	H	L	H	H
H	H	H	H	L	H
L	H	H	H	H	L

74120

INPUT		OUTPUT
R	S1	
L	H	INHIBITED
L	L	TP1 L, TP1 H

NOTE:
TP2, TP3, & TP4 generated in the same way as TP1.

08-1270

Figure 4-6 CPU Timing Logic

4.2.5 I/O Transfer Stall Logic

Because of gating delays, some PDP-8/A-compatible peripherals need more time for an I/O transfer than is available with normal processor timing; furthermore, some peripherals must make more than one I/O transfer during a single IOT instruction. To satisfy these requirements, the I/O Transfer Stall logic, shown in Figure 4-10, interrupts normal processor timing and stall the timing signals in TS3. The peripheral controller must assert the NOT LAST TRANSFER L signal to initiate the stalling operation. At the next occurrence of TP3 the processor timing is halted. The peripheral transfers the information, generating a BUS STROBE L signal with each word of data transmitted. This continues until the controller negates the NOT LAST XFER L signal, signifying that the next BUS STROBE L signal issued will be the last. This last BUS STROBE L signal restarts the processor timing, allowing TS3 to end and TS4 to begin.

The I/O Transfer Stall differs from the Memory Stall significantly: The former stalls timing only in TS3, the latter in any time state; an I/O Transfer Stall occurs near the end of the time state, while the Memory Stall occurs at the beginning; I/O Transfer Stall affects the memory timing signals in no way, while Memory Stall is primarily concerned with these signals. Despite these differences, the stalling process is effected, essentially, in the same way, i.e., the CTS signal, which places shift registers E9 (Figure 4-10) and E11 in parallel-load when high, is held active by the signal at the corresponding register input (input D0 of E9); therefore, the Timing Register cannot be shifted down and timing signals are stalled.

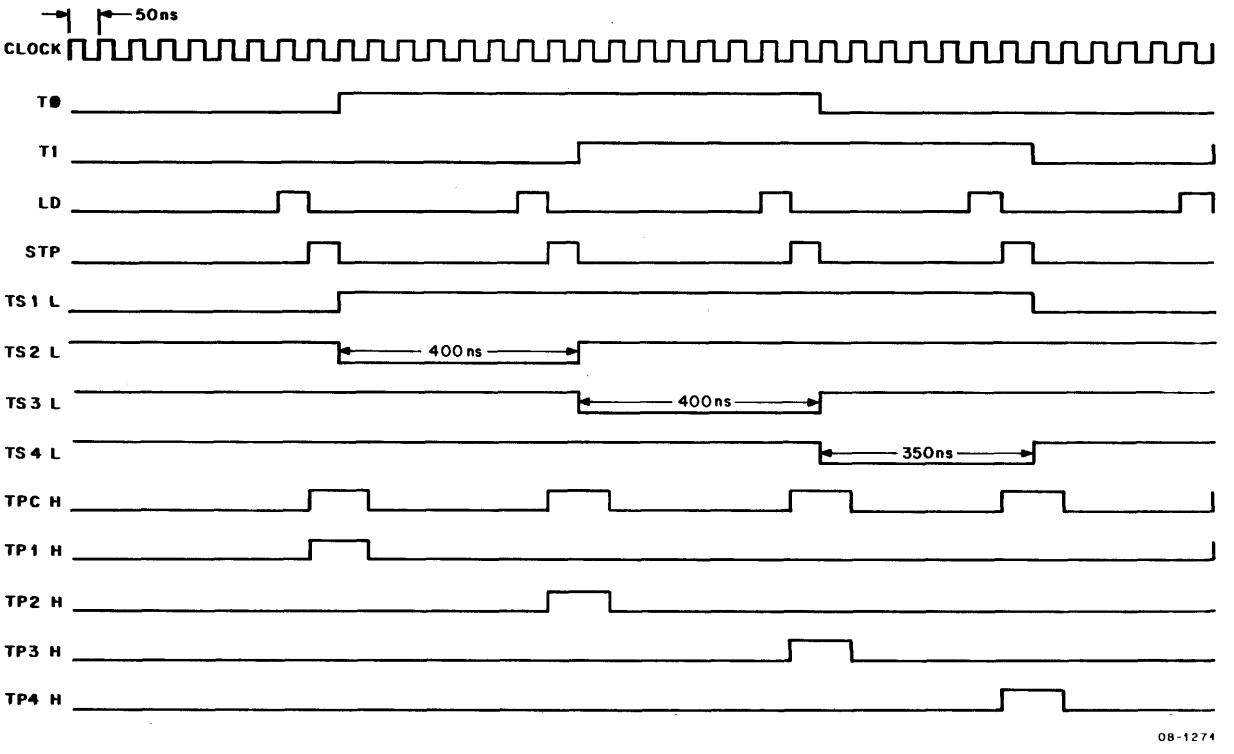


Figure 4-7 CPU Timing Signals

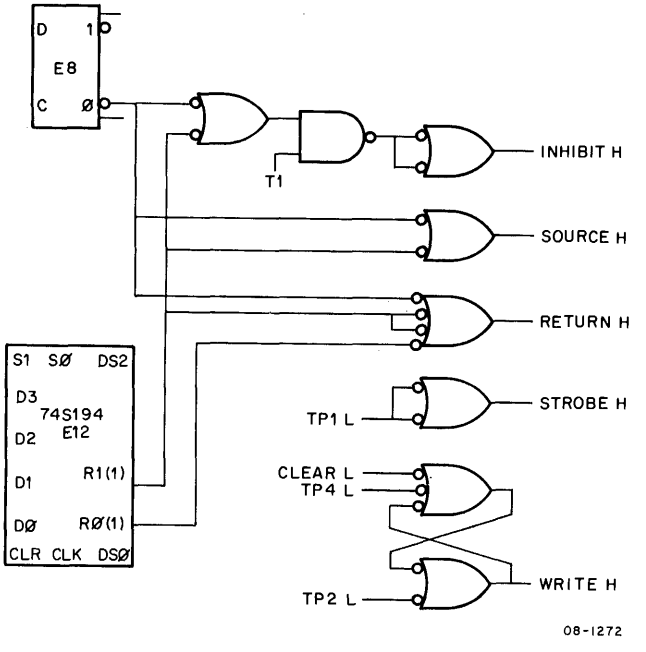


Figure 4-8 Memory Timing Logic

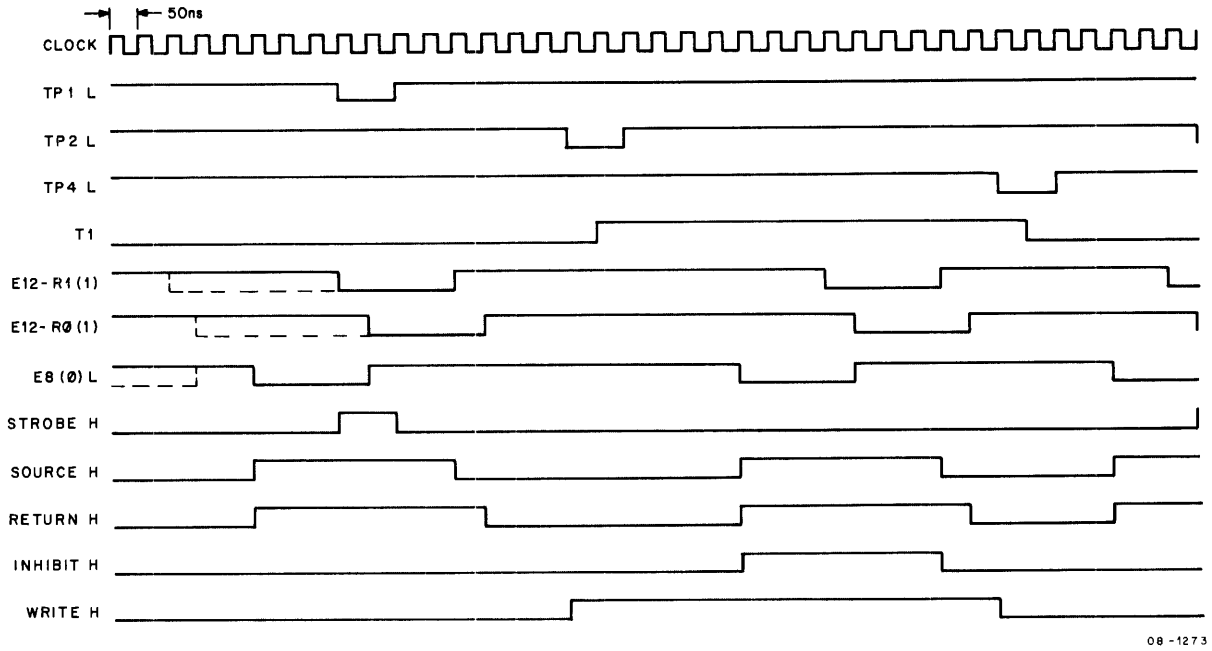


Figure 4-9 Memory Timing Signals

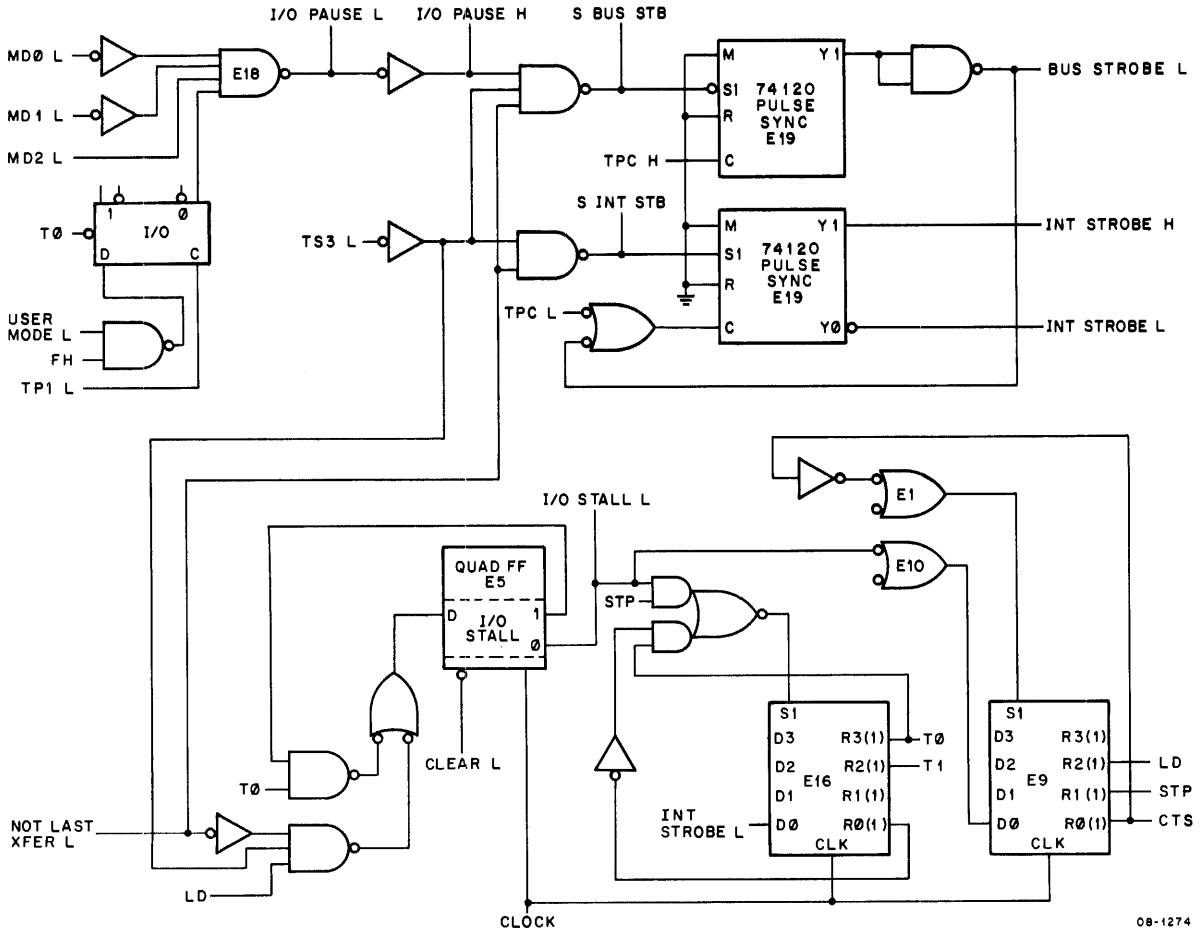


Figure 4-10 I/O Transfer Stall Logic

The logic in Figure 4-10 is effective not only when timing must be stalled, but also when an I/O transfer can be made without the necessity of interrupting the timing cycle. When the instruction in the addressed memory location is an IOT instruction, NAND gate E18 asserts the I/O PAUSE L signal when the TP1 L signal comes true during the Fetch cycle. If the IOT instruction does not require an extended timing cycle, the NOT LAST XFER L signal remains high; thus, during TS3 both the S BUS STB and S INT STB signals are asserted. The TPC signals generated at TP3 time trigger the pulse synchronizers producing the BUS STROBE L signal and the INT STROBE signals. The active BUS STROBE L signal causes the AC register or the PC register to be loaded, while the active INT STROBE L signal enables the timing cycle to proceed into TS4.

If the timing cycle must be extended, the peripheral controller grounds the NOT LAST XFER L line before TP3, preventing the pulse synchronizers from being triggered by the TPC pulses. The controller must provide a BUS STROBE L signal along with each data transfer. To stall the timing cycle, the NOT LAST XFER L signal must cause the CTS signal to be suspended in its high state (Figure 4-11). NOT LAST XFER L does this by enabling the clock to set the I/O STALL flip-flop, which is then latched in the set state; I/O STALL L generates the required high DO input at shift register E9, suspending CTS and, consequently, holding E9 in parallel load. Because E16 is halted in parallel load by the same signal, I/O STALL L, the Timing Register stalls just before the normal end of TS3 L, even though the TP3 pulse is completed.

The timing cycle remains stalled until NOT LAST XFER L is negated, at which time S INT STB is asserted (S BUS STB is also asserted but has no significance at this time). The last BUS STROBE L generated triggers the INT STROBE pulse synchronizer, producing both INT STROBE signals. The first clock pulse to occur after INT STROBE L is asserted brings the ISD signal low, thereby placing E16 in the right shift mode and causing the D-input of the I/O STALL flip-flop to go low. The next clock pulse clears the I/O STALL flip-flop and places E16 in parallel load once again. The third clock pulse brings the CTS signal low, and normal timing operation is resumed.

4.2.6 Memory Stall Logic

The Memory Stall logic is shown in Figure 4-12. This logic is designed to modify the normal operation of the Timing Generator so that memories that have a cycle time slower than 1.5 μs can be used with the PDP-8/A CPU. A slower memory grounds the Omnibus NTS STALL L line to halt the Timing Generator during one or more processor time states of a timing cycle. In order to stall the generator in a particular time state, the memory logic must assert the NTS STALL L signal at least 100 ns before the time pulse that precedes the time state in which the stall is to occur. For example, to suspend the timing in TS3, the memory must assert NTS STALL L at least 100 ns before TP2. The timing will halt at the beginning of TS3, except for the TP2 signal, which is completed during its normal time; the timing remains in the stalled condition until the NTS STALL L signal is negated.

Figure 4-13 is a timing diagram that illustrates the process just described, i.e., the Timing Generator is stalled at the beginning of TS3. This diagram shows NTS STALL L being asserted during TP1 and negated approximately 700 ns later. Fifty nanoseconds after NTS STALL L is negated, the normal timing resumes and TS3 L is asserted for the usual period of 400 ns. Note that the WRITE H signal is stalled along with the processor timing signals. This is the only memory timing signal whose duration is affected by the stalling process; all other memory signals are active for the usual length of time regardless of the time state chosen for stalling. For example, if NTS STALL L is asserted before TP1, the timing halts at the beginning of TS2; however, STROBE H, SOURCE H, RETURN H, and TP1 are completed in the normal period of time.

Table 4-1 indicates the result achieved by stalling the timing generator at the start of each of the time states.

4.3 FRONT PANEL OPERATIONS

There are two types of control panels for the PDP-8/A. The Limited Function Panel is supplied with each computer; it enables an operator to turn the computer on, and it provides several elementary indications of the PDP-8/A's operating condition. The Programmer's Console, KC8-AA, is an option that enables one to control computer operations and to make step-by-step checks on significant conditions within the computer.

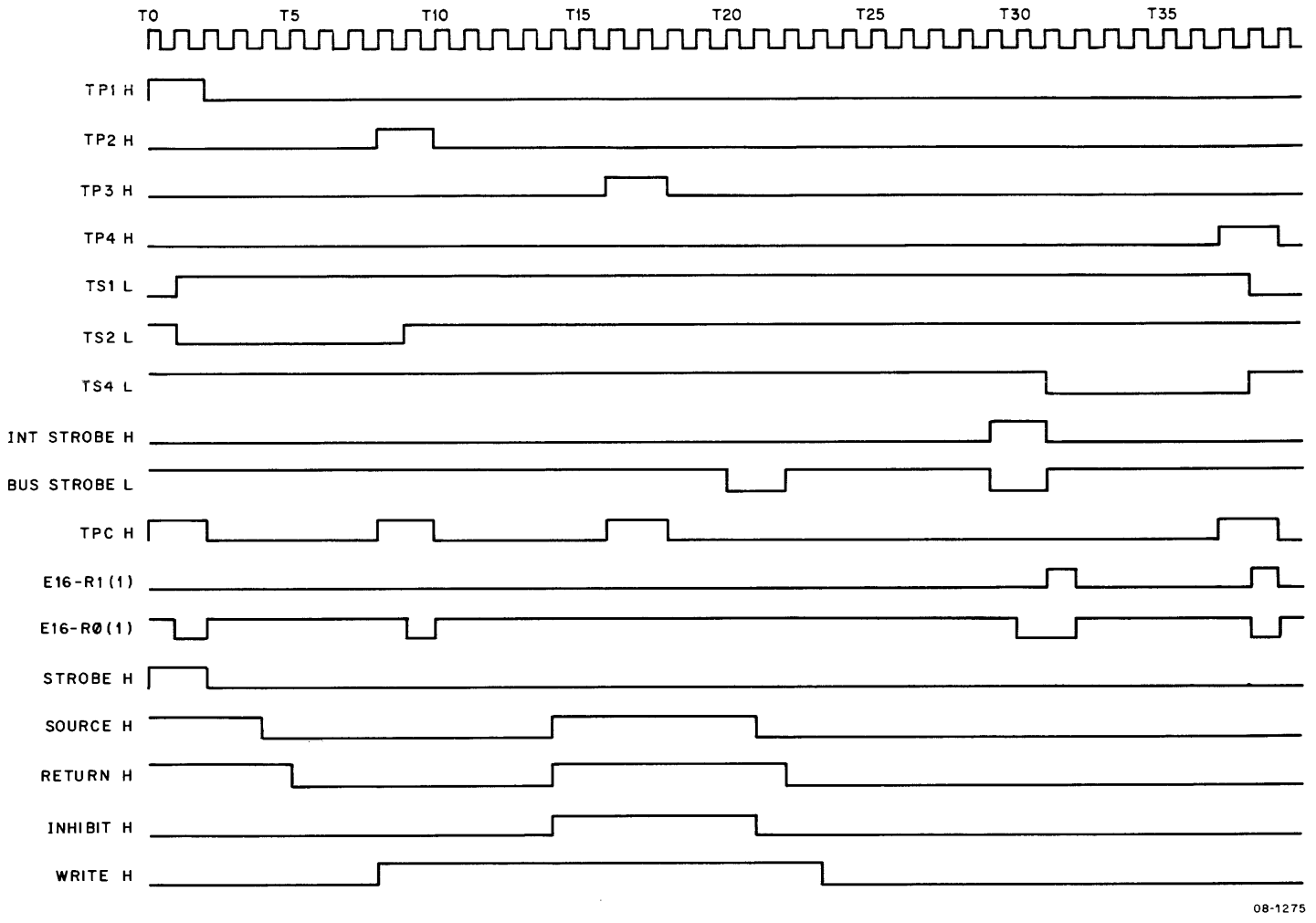


Figure 4-11 I/O Timing (NOT LAST XFER L Asserted) (Sheet 1 of 2)

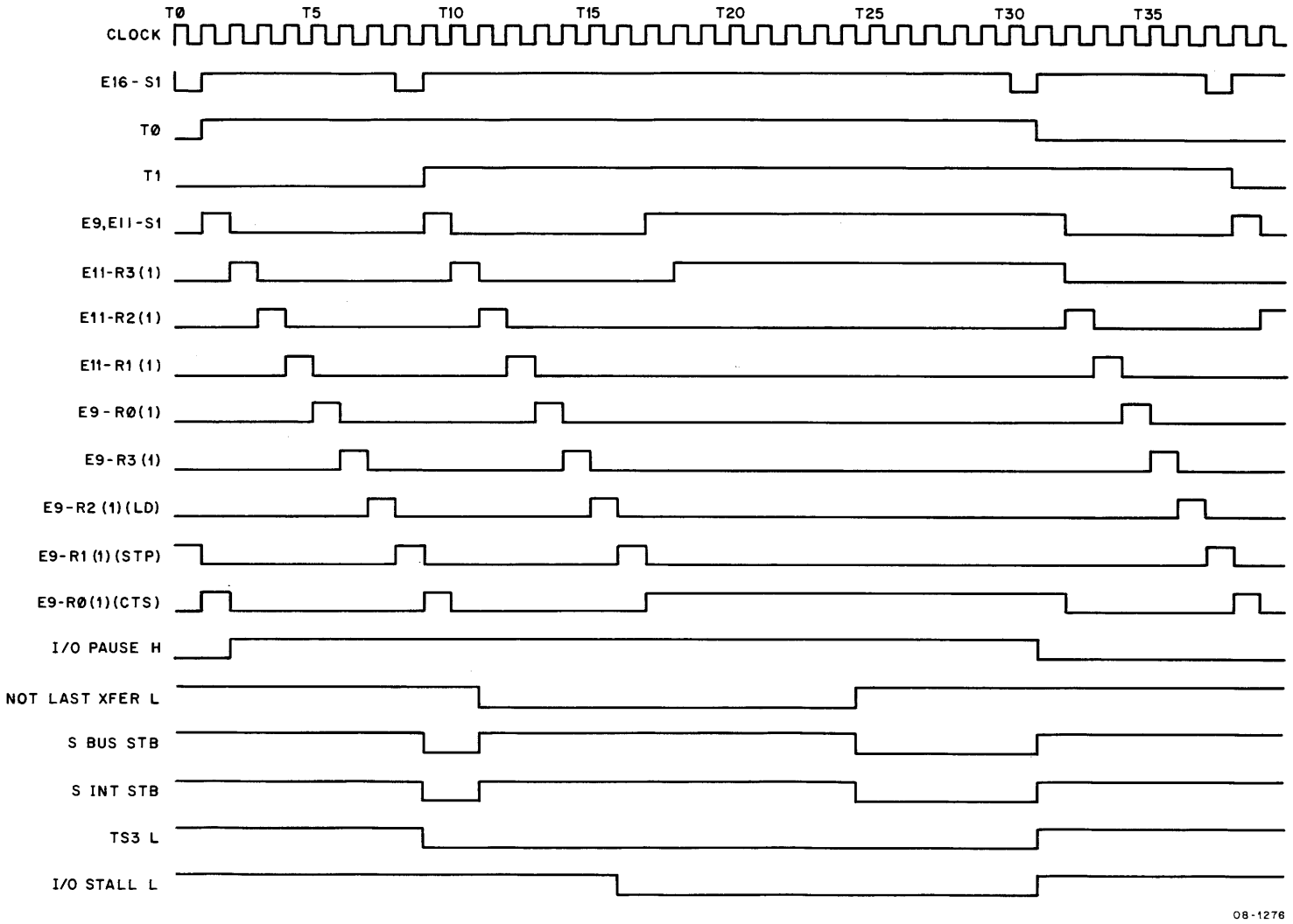


Figure 4-11 I/O Timing (NOT LAST XFER L Asserted) (Sheet 2 of 2)

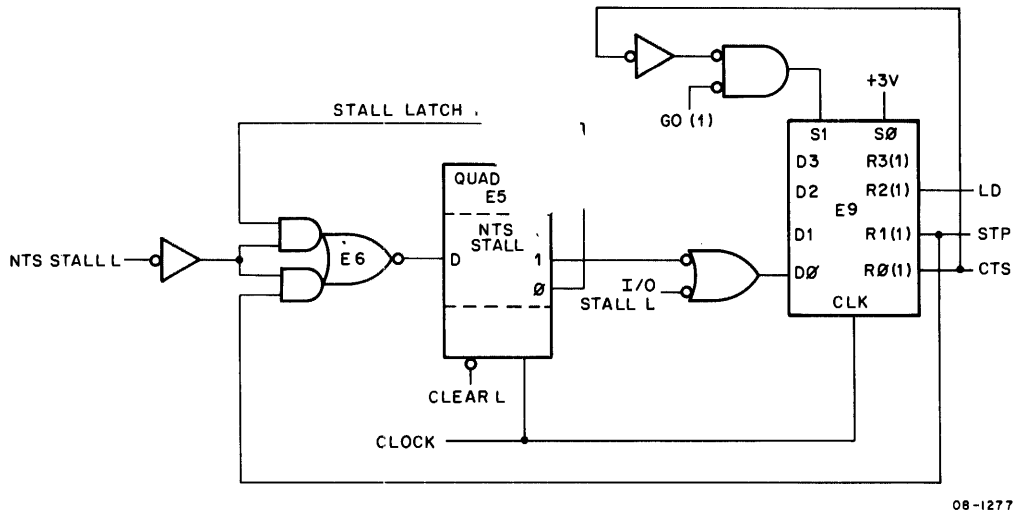


Figure 4-12 Memory Stall Logic

4.3.1 Limited Function Panel

Two Limited Function Panels are in use; one is used with the PDP-8/A Semiconductor computer, while the other is used with the 8A computers. The switches, indicators, and circuit components of each panel are mounted on a circuit board that is attached to the rear of the panel; the switches protrude through the panel and the indicators are visible through panel openings. The circuitry associated with each panel is the same, but the location of circuit components differs, as is shown by Figures 4-14 and 4-15. Connector J1 of the 8A-type circuit board connects to the H9194 Omnibus, while J1 of the PDP-8/A semiconductor-type circuit board connects to the H9192 Omnibus via the Power Board Assembly. The following description applies equally to each circuit board, except where noted otherwise.

The three LED indicators provide a basic indication of the computer's operating condition. In the PDP-8/A Semiconductor computer, the BATTERY CHARGING indicator lights when the battery charger circuit on the power supply regulator board is operating; when charging current ceases to flow, the LED is extinguished, indicating that the battery is fully charged. In the 8A420, 8A620, and 8A820 computers the BATTERY CHARGING indicator lights when both G8018 regulators are operating correctly. The indicator is not used in the 8A400, 8A600, and 8A800 computers. The POWER indicator monitors the secondary of the power transformer; when lighted, it indicates that ac power has been applied to the computer. The RUN indicator lights when the Timing Generator is turned on and the Omnibus RUN L signal is asserted. RUN L turns off transistor E1C allowing the LED to glow; when the Timing Generator is off, E1C conducts and the LED remains dark.

The three switches on the front of the panel permit limited control of the computer. The PANEL LOCK switch is shown in the active (up) position, the position that disables the console pushbuttons, except LSR and DISP. The BOOT switch, shown in the inactive (down) position, is used to initiate bootstrap loading of programs. When the switch is in the position shown, transistor E1A is off and the BOOT signal is high (BOOT becomes SW L on the Omnibus). To initiate a bootstrap operation, the operator must raise the BOOT switch and then return it to the down position. When the switch is raised, transistor E1D is turned off, causing E1A to turn on; this action brings the SW L signal low. When the switch is returned to the down position, E1A is turned off and the SW L signal goes high. The low-to-high transition is used by the Bootstrap Loader option (M8317) to begin the bootstrap operation.

The computer's primary power can be controlled from two locations – the Limited Function Panel, where the ON/OFF switch enables the operator to turn the power on or off, and a remote position, where the POWER REQUEST signal can be switched to turn the power on or off. The MASTER/ SLAVE switch determines the source of primary power control. With the switch in the MASTER position the panel ON/OFF switch assumes control; with the switch in the SLAVE position, the remote location assumes control (the power can be turned off by the panel ON/OFF switch even though the SLAVE position has been selected).

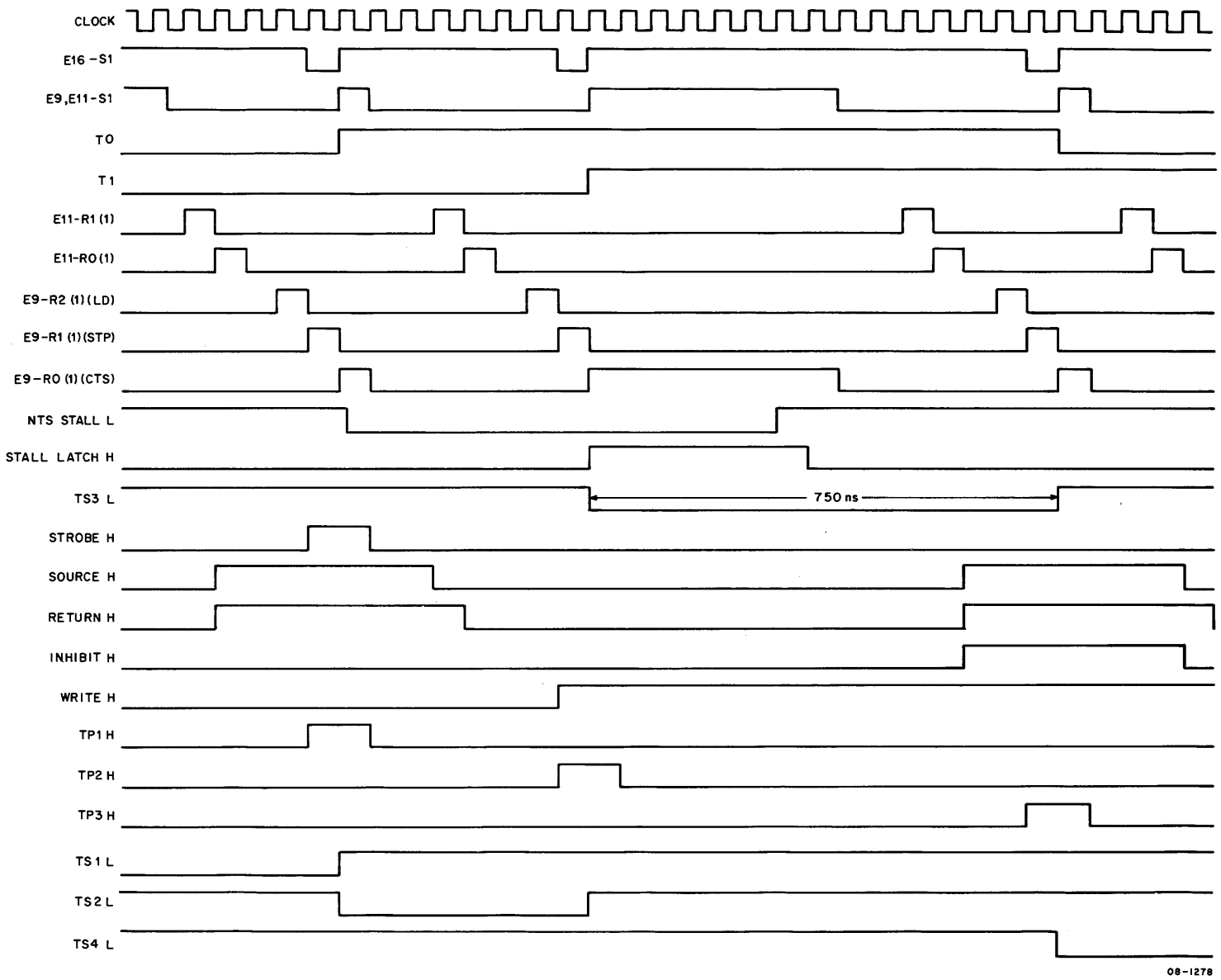


Figure 4-13 Timing, NTS STALL L Asserted

Table 4-1
Time State Stall Results

NTS STALL L Asserted Before	Time State Stalled	Result
TP1	TS2	The time from the end of read to TP2 is increased, accommodating memories with long read-access time.
TP2	TS3	The time from the loading of the MB register to the start of write is increased.
TP3	TS4	The time from the start of write to the change of address is increased, accommodating memories with a long write time.
TP4	TS1	The time from the change of address to the start of read is increased.

The two switches are illustrated in Figures 4-14 and 4-15, along with part of the associated circuitry. The circuitry and the signals are discussed in detail in Chapter 7, Power Supply; only the result of the switching operation is presented here. Table 4-2 shows what happens when the switches are in the indicated positions. The LINE LEVEL signal shown in the figures is a measure of the ac line voltage and is present as long as the ac line is connected to the computer.

4.3.2 Programmer's Console

Figure 4-16 is a block diagram of the PDP-8/A Programmer's Console logic. Included in the block diagram is the console control logic, part of the I/O option board (DKC8-AA) that plugs into the Omnibus. The console logic is contained on two printed circuit boards that are mounted on the rear of the console. The two boards connect electrically by short lengths of cable; the console connects to the I/O option board by a cable that can be as long as 15 feet, enabling the console to be located remotely from the PDP-8/A mainframe.

There are 20 pushbuttons, 8 LED (light-emitting diodes) indicators, and 9 7-segment LED displays visible on the front of the console. See Chapter 1 for a description of the indicators and controls for both the Programmer's Console and the Limited Function Panel.

The Programmer's Console pushbuttons can be grouped into number buttons and function buttons. Number buttons are used to specify addresses and data, and to select the data from a specific source (for example, the AC register or the DATA bus) for display in the DISP readout. When a number button is pushed, the number is displayed as the right-most digit in the DISP readout. If a second number button is pushed, it appears as the right-most digit, while the first is shifted left by one position. Any number of digits may be entered in the DISP readout, although only the four displayed have meaning; collectively, the digits are referred to as the "entry."

Function buttons are used to start and stop CPU timing, to initialize selected CPU hardware, to load addresses and data specified by the entry, and to display the data from the source selected by the entry.

When the operator pushes a function button, the logic generates the signals KFUN0 L, KFUN1 L, and KFUN2 L in a combination that is peculiar to that button. The button is identified as "number" or "function" by the NUM H signal or the FUN L signal, respectively (only one number or one function button can operate at the same time). Either of these two signals causes the clock timing logic to assert three basic timing signals, KEY STB H, MCLOCK L, and KEY F L.

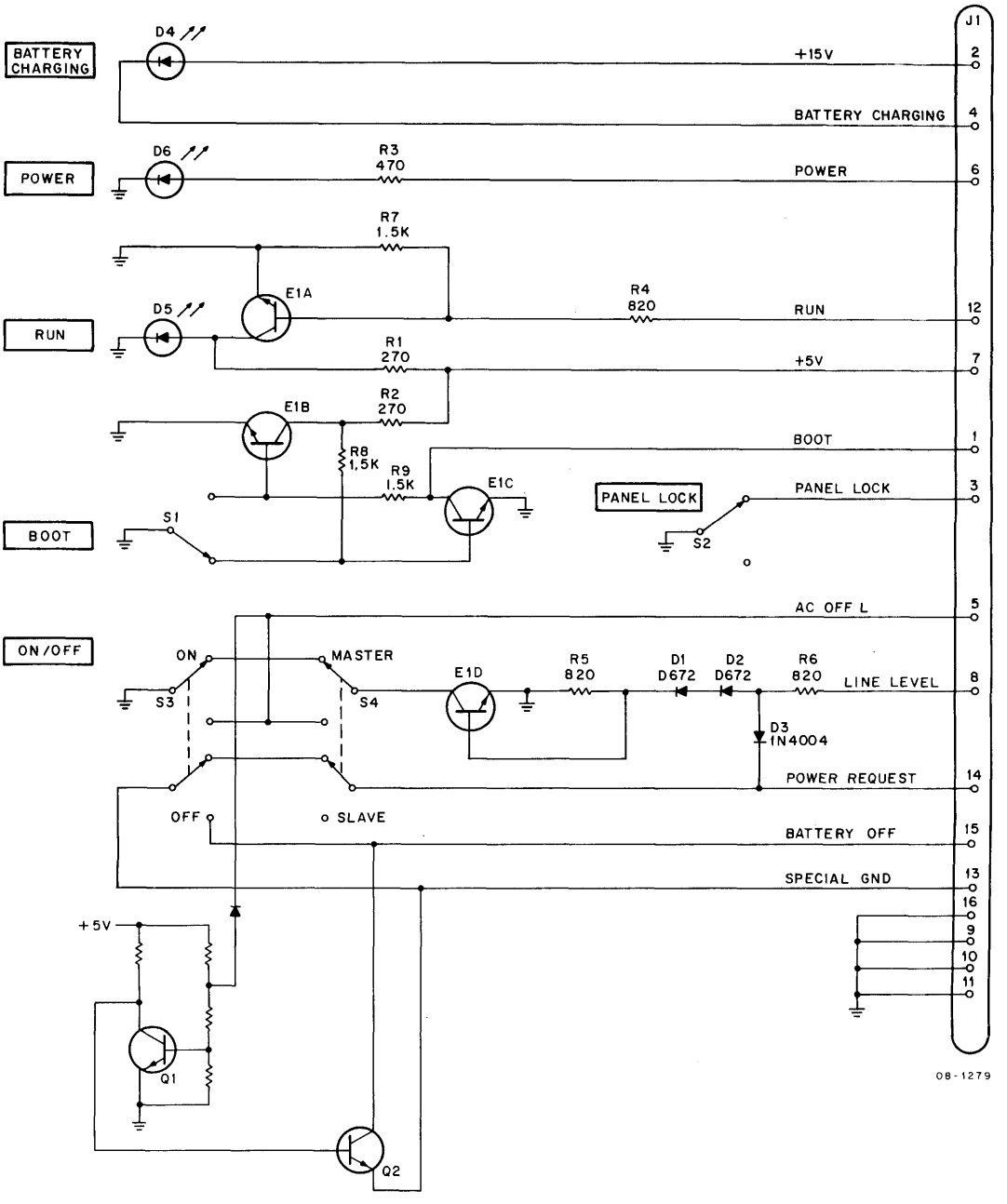


Figure 4-14 Limited Function Panel Circuit Board Schematic, 8A Computers

If a number button has been pushed, the signal combination representing that button is loaded into the number shift register, gated through a data selector by the GATE ENT L signal, and loaded into the DISP flip-flops. The readout control logic generates signals that multiplex the number data to the DISP readout circuits on the DISPLAY 0, 1, and 2 lines, while at the same time asserting signals that direct the number data to the correct digit of the DISP readout. When the operator pushes a second number button, the first number is shifted to bit position two of the number shift register, while the second number is loaded into bit position one. Both numbers are gated to the readout circuits as just described and displayed in the correct digit position. A third and fourth number can be entered in the same way. The DISP readout then shows the octal representation of whatever the entry is intended to specify, the most significant bit of the data being contained in the left-most digit. This entry is displayed until the operator pushes either another number button, changing the content of the number shift register, or a function button, disposing of the entry.

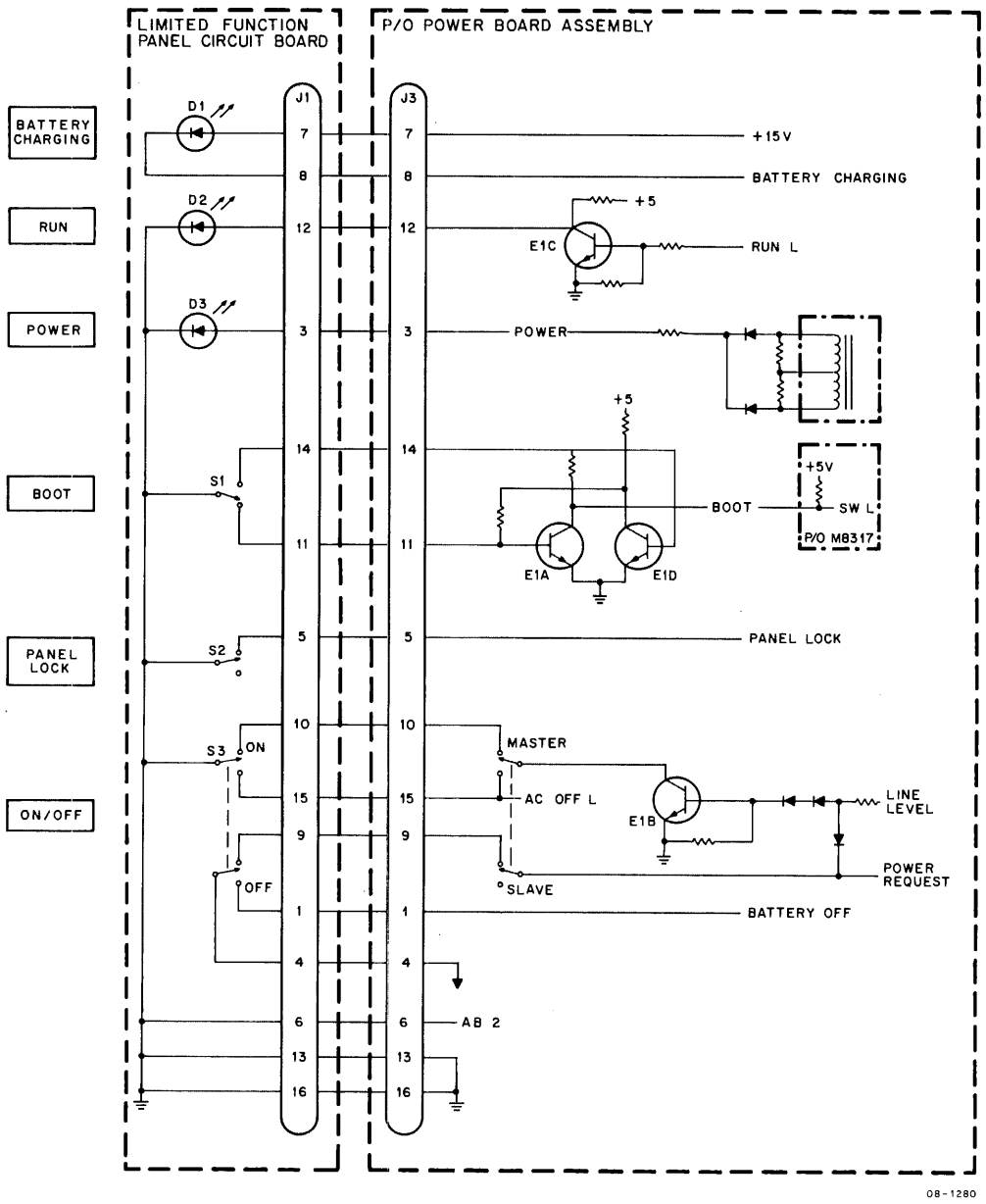


Figure 4-15 Limited Function Panel Circuit Board Schematic, PDP-8/A Semiconductor Computer

The disposition of the entry depends upon what the entry represents; i.e., is it an address or is it data? If it is an address, the operator can transfer it to the CPMA register by pushing the LA (load address) button. When this button is pushed, the signals representing the LA function are loaded into the latch circuits and applied to a decoder. The decoder output causes the gating logic to generate signals that gate the entry to the CPMA register via the Omnibus DATA lines. First, the GATE ENT L signal selects the output of the number shift register for transfer to the console control logic on the BUS 0–11 lines. Then, the KCCN1 SR ENABLE L signal is asserted by the interface gating logic, placing the entry on the Omnibus DATA 0–11 lines. Transfer control signals asserted by the interface gating logic direct the information on the DATA lines to the CPMA register and cause the register to be loaded.

Table 4-2
Primary Power Control

ON/OFF Switch		MASTER/SLAVE Switch
ON	**OFF**	
Condition of transistor E1B is irrelevant. POWER REQUEST signal is grounded (irrelevant in this situation). Line voltage is applied to the power transformer.	AC OFF L is grounded, causing the ac line voltage to be removed from the power transformer. BATTERY OFF is grounded to prevent the battery supply from operating.	MASTER
If POWER REQUEST is not grounded at the remote location, E1B is on; thus, AC OFF L is low and ac line voltage is not applied to the power transformer. BATTERY OFF is grounded in the power supply to prevent the battery supply from operating. If POWER REQUEST is grounded, E1B is off. AC OFF L and BATTERY OFF are high. Line voltage is applied to the power transformer.	AC OFF L is grounded, causing the ac line voltage to be removed from the power transformer. BATTERY OFF is grounded to prevent the battery supply from operating.	SLAVE

If the entry is data, rather than an address, it can be deposited in a memory location that is addressed as just described. The DTHIS or DNEXT button causes the gating logic to assert the GATE ENT L signal, placing the entry on the BUS 0–11 lines. Again, the KCCN1 SR ENABLE L signal passes the entry to the Omnibus DATA 0–11 lines where it is routed to the MB register and placed on the MD 0–11 lines.

Rather than depositing the data in memory, the operator can load it into the switch register for future use by pressing the LSR button. At any later time, he or she can display the contents and, if necessary, make changes manually; the operator can also program certain operations that use whatever data is stored in the register.

To display the contents of a register or of another available source, the operator pushes one of the buttons numbered from 0 to 6. The source of data represented by each of these numbers is indicated above the button. Thus, when the operator wishes to view the contents of the AC register, for example, he or she first pushes the button numbered "0". The signals representing number 0 are loaded into the number shift register and the number is displayed in the right-most digit of the DISP readout. Then, the operator pushes the DISP function button. The output from the BCD-to-decimal decoder clocks the ENT0 H, ENT1 H, and ENT2 H signals into flip-flops; the flip-flop outputs, DISP0 H, DISP1 H, and DISP2 H, cause the AC indicator to light. At the same time, the interface gating logic asserts Omnibus signals that gate the AC register contents onto the DATA 0-11 lines; the KCCN1 DATA ENA L signal gates the DATA line signals through the selector to the BUS 0–11 lines. From the BUS 0–11 lines the AC contents are routed through the DISP flip-flops and the multiplexer to the DISP readout; they are displayed there until another number or function button is pushed.

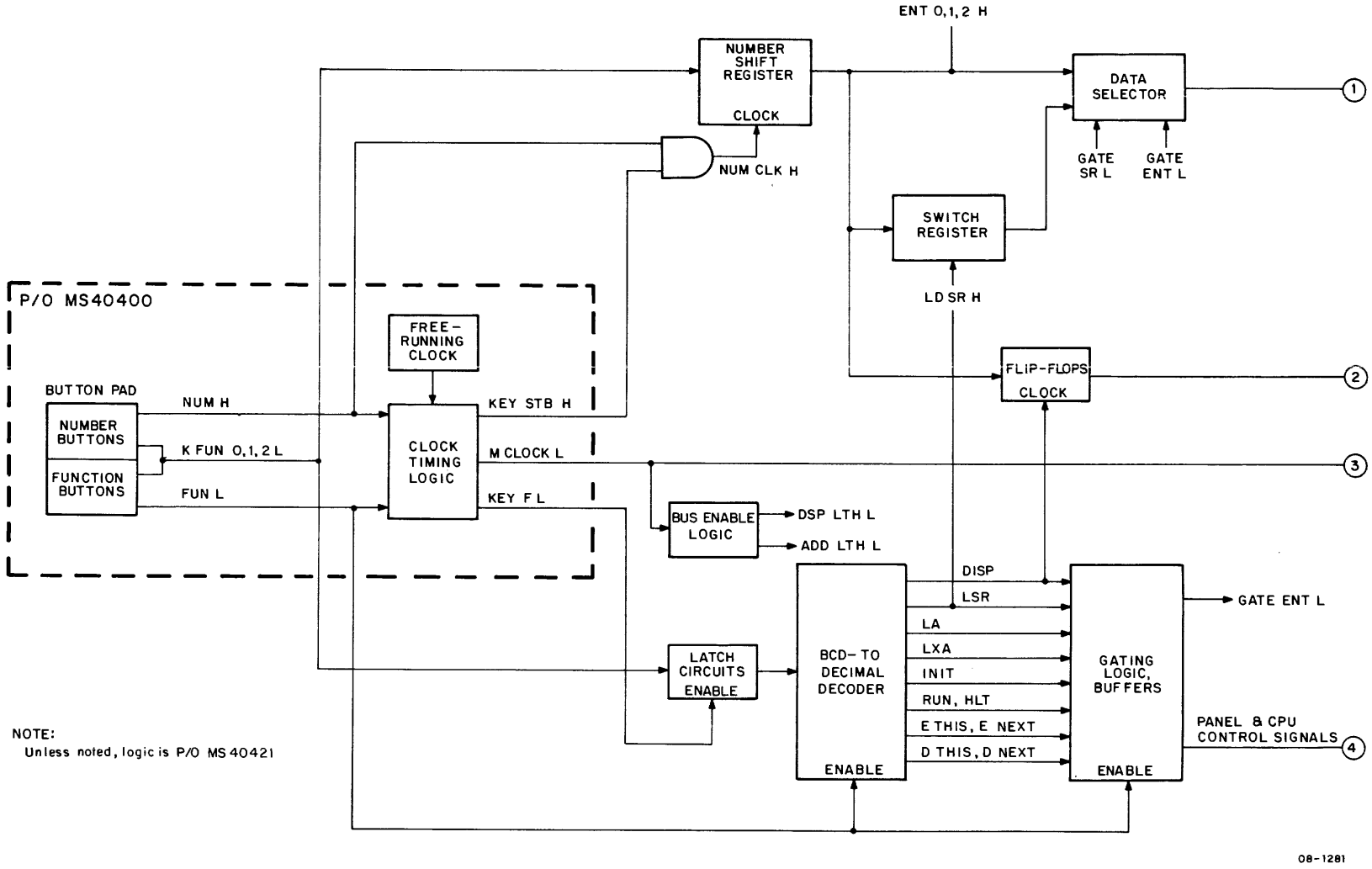


Figure 4-16 Programmer's Console Block Diagram (Sheet 1 of 2)

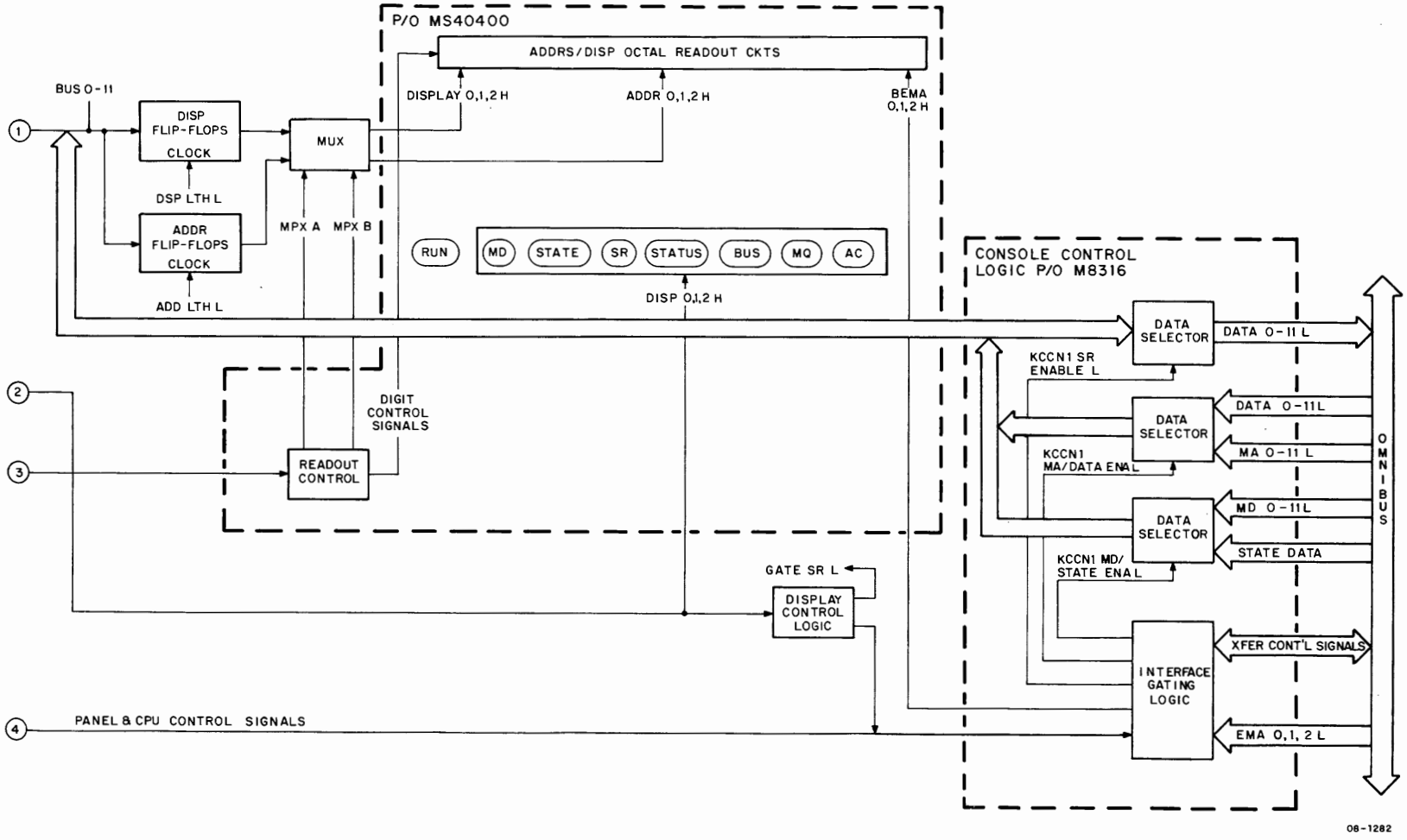


Figure 4-16 Programmer's Console Block Diagram (Sheet 2 of 2)

4.3.2.1 Clock Timing Logic – The clock logic is shown in Figure 4-17. The logic includes two priority encoders (E1 and E6), two one-shot multivibrators (E18), two flip-flops (E23), and a 4-bit shift register (E24). The one-shot multivibrators comprise a free-running clock-pulse generator that produces a 400 ns MCLOCK L pulse every 1 ms. This MCLOCK L signal is used throughout the console logic and is fundamental to the operation of the clock timing logic.

When the operator pushes a button on the front of the console, one of the priority encoders generates a binary representation at the A0, A1, and A2 outputs. These outputs become the KFUN0 L, KFUN1 L, and KFUN2 L signals that are important in the logic that follows (Table 4-3 lists the console pushbuttons and the corresponding binary representations.) The encoder also produces a signal at the GS output (FUN L or NUM L); this indicates the identity (function or number) of the selected pushbutton and causes a low voltage level to be applied to the serial-input line (DS0) of the 4-bit shift register (unless a button on the console is pushed, this shift register is constantly right-shifting a high voltage level that appears at the serial input; consequently, the register is always fully-loaded, except when front panel operations are in progress). The 4th MCLOCK L pulse to appear after the button has been pushed shifts a low into bit position 4 of the register (R3(1)), thereby causing flip-flop E23A and, in turn, E23B to be set. Thus, the KEY F L and KEY STB H signals are generated, KEY STB H being somewhat less than 400 ns wide due to the delay in E24 and E23. Figure 4-18 shows the timing of the clock timing logic.

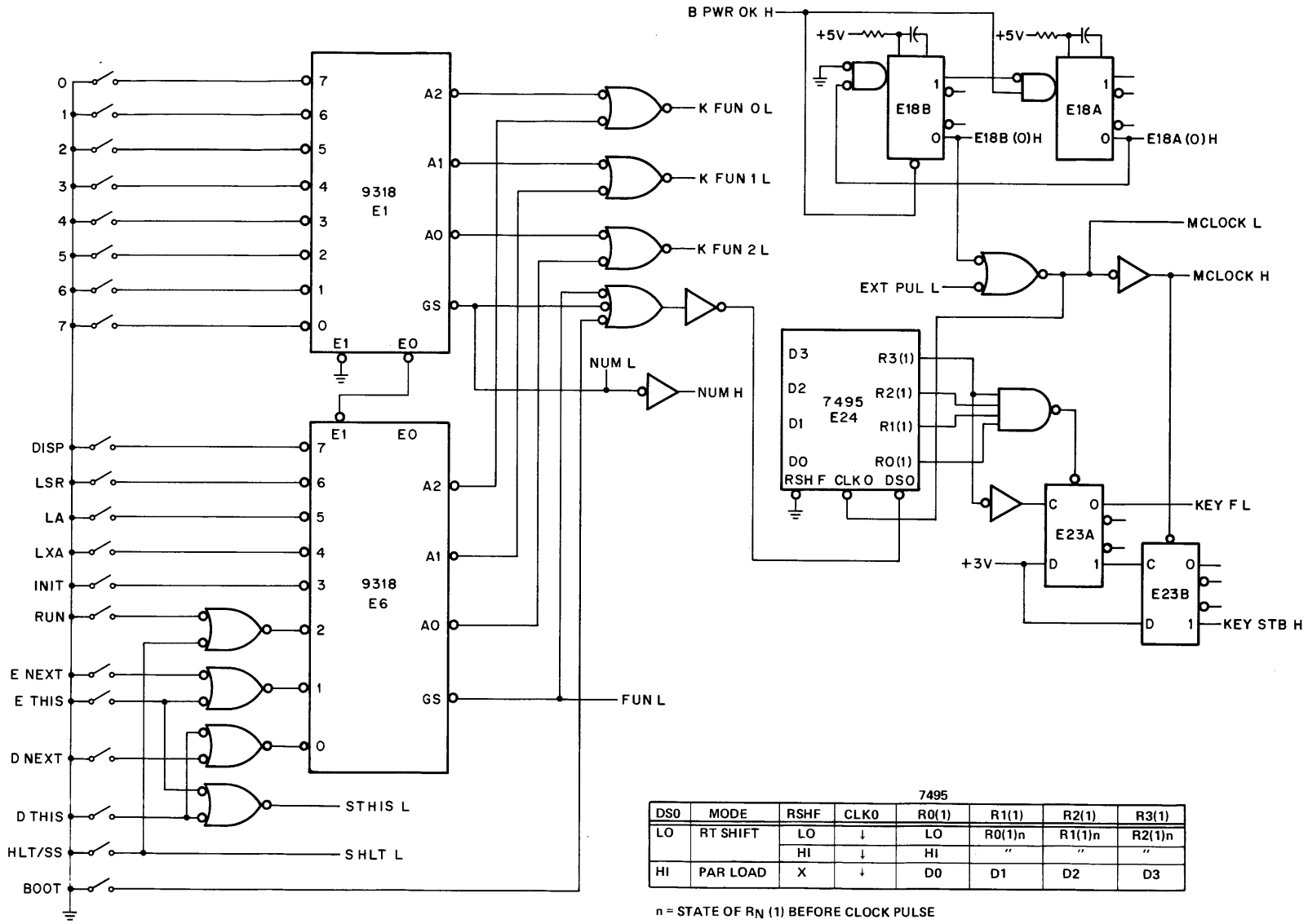
Note that 4 MCLOCK L pulses must be counted by the shift register after the pushbutton has been activated (i.e., when NUM L is asserted). This requirement ensures that switch contact-bounce will not affect circuit operation. For the same reason, four pulses must be counted after the button has been released (if a new button is pushed before this happens – a near physical impossibility – the KEY STB H signal will not be generated).

If two or more buttons are pushed simultaneously, the priority encoders ensure that only the button having highest priority is represented at the encoder outputs. Highest priority is assigned to the 0 number button and to the DISP function button; the remaining buttons are assigned priorities that correspond to their relative positions in Figure 4-17 (e.g., button 7 has the lowest priority in the number group; the HLT/SS button has lowest priority in the function group).

The number buttons have priority over the function buttons. When a number button is pushed, the encoder E0 output is high. This output is applied to the E1 input of the function encoder and disables it, keeping all outputs high.

4.3.2.2 Register Logic – The Register logic is shown in Figure 4-19. (Figure 4-23 relates signals in this paragraph and in paragraphs 4.3.2.3 and 4.3.2.4). The logic consists of 4-bit shift registers E1, E2, and E3, quad flip-flops E5, E6, and E7 (these flip-flops comprise the switch register), and data selectors E9, E10, and E11. When a console button is pushed, a binary-coded representation appears on the KFUN lines. If the button is one of the number group, the NUM CLK H signal is generated, loading the signals into R0(1) of each shift register (the E MODE L signal is high at this time (Figure 4-23); hence, the shift registers are in the parallel load mode, ensuring that the as-yet unused bit positions are loaded with ground-level signals). Because the button is from the number group, the GATE ENT L signal is generated periodically and gates the signals through the data selectors to the BUS lines.

If the operator pushes a second number button, the NUM CLK H signal right-shifts the registers; consequently, the signals representing the first number are shifted to R1(1), while the signals representing the second number are shifted into R0(1) (note that the E MODE L signal is low at this time). Data representing four numbers can be entered in the registers and gated to the BUS lines. For example, consider what happens when the operator wishes to deposit data word 6203(8) in memory. After selecting the memory address, he or she pushes the four octal numbers consecutively, beginning with 6. When the operator has entered all four numbers, the data is represented on the BUS lines as shown in Table 4-4. By pushing the DTHIS and DNEXT button, the data is routed through the logic and deposited in the selected memory location. This action then negates the GATE ENT L signal, removing the data from the BUS lines after it has been operated on. However, the data is retained in the shift register until the operator pushes another number button.



7495

DS0	MODE	RSHF	CLK0	R0(1)	R1(1)	R2(1)	R3(1)
LO	RT SHIFT	LO	↓	LO	R0(1)n	R1(1)n	R2(1)n
		HI	↓	HI	"	"	"
HI	PAR LOAD	X	↓	D0	D1	D2	D3

n = STATE OF R_N (1) BEFORE CLOCK PULSE

08-1283

Figure 4-17 Clock Timing Logic

Table 4-3
Clock Timing Control Signals

Pushbutton	DEC9318 Output	Control Signal Generated						
		KFUN0L	KFUN1L	KFUN2L	NUMH	FUNL	STHISL	SHLTL
0(AC)	A0, A1, A2, GS	X	X	X	X			
1(MQ)	A1, A2, GS	X	X		X			
2(BUS)	A0, A2, GS	X		X	X			
3(STATUS)	A2, GS	X			X			
4(SR)	A0, A1, GS		X	X	X			
5(STATE)	A1, GS		X		X			
6(MD)	A0, GS			X	X			
7	GS				X			
DISP	A0, A1, A2, GS	X	X	X		X		
LSR	A1, A2, GS	X	X			X		
LA	A0, A2, GS	X		X		X		
LXA	A2, GS	X				X		
INIT	A0, A1, GS		X	X		X		
RUN	A1, GS		X			X		
ENEXT	A0, GS			X		X		
ETHIS	A0, GS			X		X	X	
DNEXT	GS					X		
DTHIS	GS					X	X	
HLT/SS	A1, GS		X			X		X
BOOT								

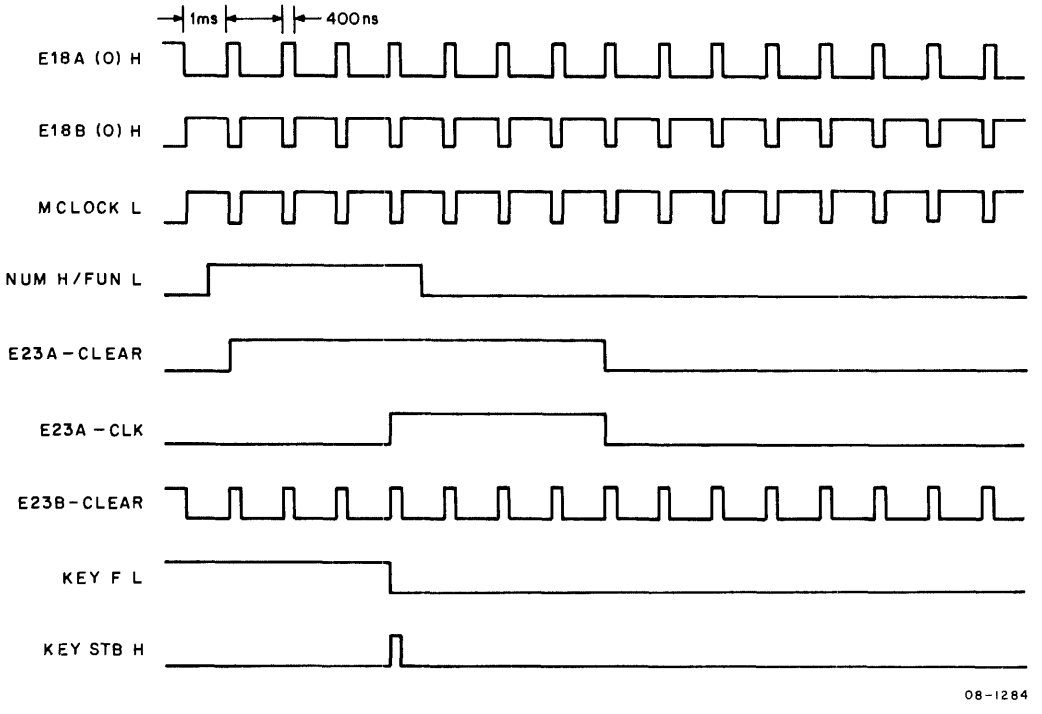


Figure 4-18 Timing, Clock Timing Logic

The operator can load the switch register from the shift register at any time by pushing the LSR button. The data is retained in the switch register unless a power down condition occurs, clearing the register, or until new data is loaded from the shift register. Data is gated from the switch register to the BUS lines by the GATE SR L signal. This signal is asserted whenever the operator has selected the switch register contents for display in the DISP readout, or when a program instruction has directed that the switch register contents be placed on the Omnibus DATA lines (SR DATA L is asserted).

The operator displays the contents of some source by, first, pushing the appropriate button and, second, pushing the DISP button. The binary-coded representation of the source is loaded into R0(1) of the shift registers and, thus, appears on the ENT0, ENT1, and ENT2 lines. These lines carry the binary-coded signals to the display control logic and to the display indicators.

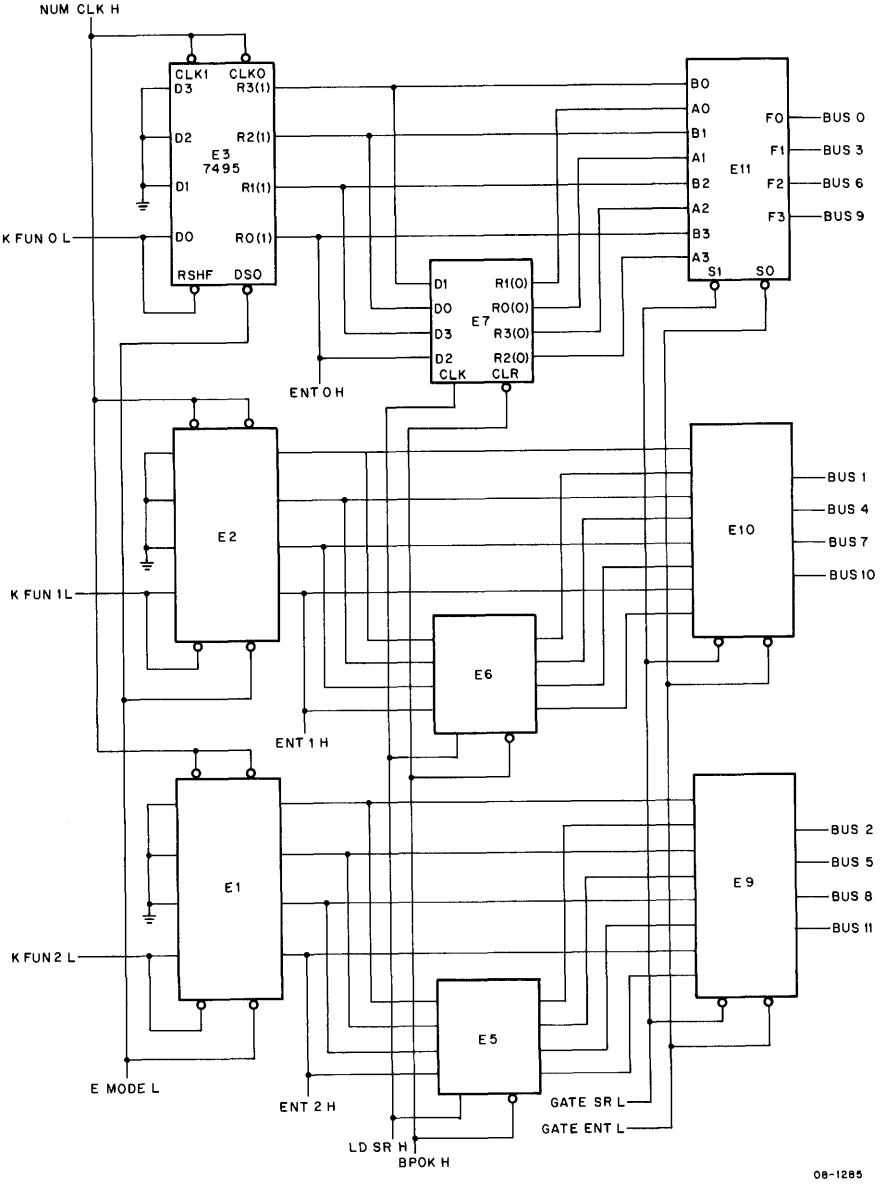


Figure 4-19 Register Logic

Table 4-4
Register Logic Bus Line Data

Octal Number	Bus Line	Voltage Level
6	0	HI
	1	LO
	2	LO
2	3	LO
	4	HI
	5	LO
0	6	LO
	7	LO
	8	LO
3	9	LO
	10	HI
	11	HI

4.3.2.3 Multiplexer Logic – The Multiplexer logic, shown in Figure 4-20, consists of hex flip-flops E12 through E15 and multiplexers E17 through E19. Data on the BUS lines is clocked into the flip-flops and gated by the multiplexers to the readout circuits via the DISPLAY lines or the ADDR lines. The data on the BUS lines is either the entry, which will be displayed in the DISP readout until disposed of, the contents of some source (the AC register, for example), which will be displayed in the DISP readout, or the address of the currently-addressed memory location, which will be displayed in the ADDRS readout.

Entry data is gated from the register logic onto the BUS lines by the GATE ENT L signal. When GATE ENT L is low, the DSP LTH L pulse clocks the BUS lines data into hex flip-flops E13 and E15. The flip-flop outputs are applied to multiplexer E19 and half of multiplexer E18. The multiplexers are controlled by signals MPX A and MPX B, which are generated by the readout control logic. The readout control logic also generates enabling signals that are applied to the DISP and ADDRS readout circuits. Each of these enabling signals is applied to a 7-segment LED display. The enabling signals and the MPX signals are related in such a way that the correct data is displayed in each LED display. The block diagram in Figure 4-21 illustrates the method of gating the BUS lines data to the proper LED display. Figure 4-23 shows the timing of the signals involved in the procedure.

The table in Figure 4-21 relates the enable signals, the MPX signals, and the BUS lines. For example, the readout control logic asserts enable signal 0 when both MPX A and MPX B are low. Signal 0 is applied to the anode connection of the right-most LED display (the one showing the LSD of the 4-bit octal DISP readout). The MPX signals gate the multiplexer A inputs to the DISPLAY lines; thus, the data on the BUS 9, BUS 10, and BUS 11 lines is applied to the cathode connection of the LED displays. Only the right-most display indictates a number at this time.

The contents of a register, or some other source, are gated to the DISP readouts in the same way as is entry data. The address of the currently-addressed memory, however, is clocked into hex flip-flops E12 and E14 (Figure 4-20) by the ADR LTH L signal. This address is gated onto the BUS lines from the Omnibus DATA lines by the MA ENA L signal, which is asserted periodically provided that neither the LA, the LXA, nor the DEP button has been activated. The MPX signals place the current address on the ADDR lines and the address is displayed in the ADDRS readouts.

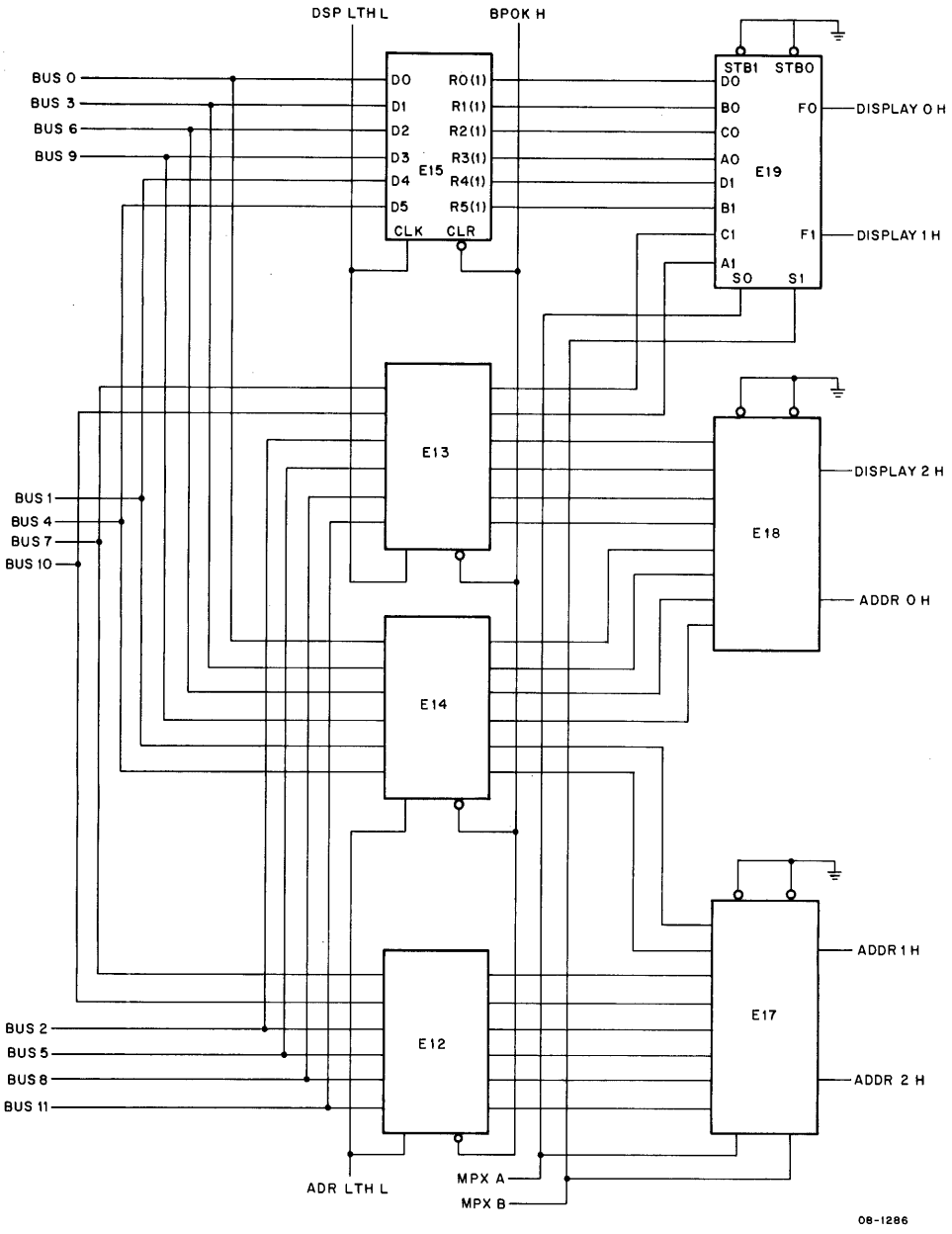


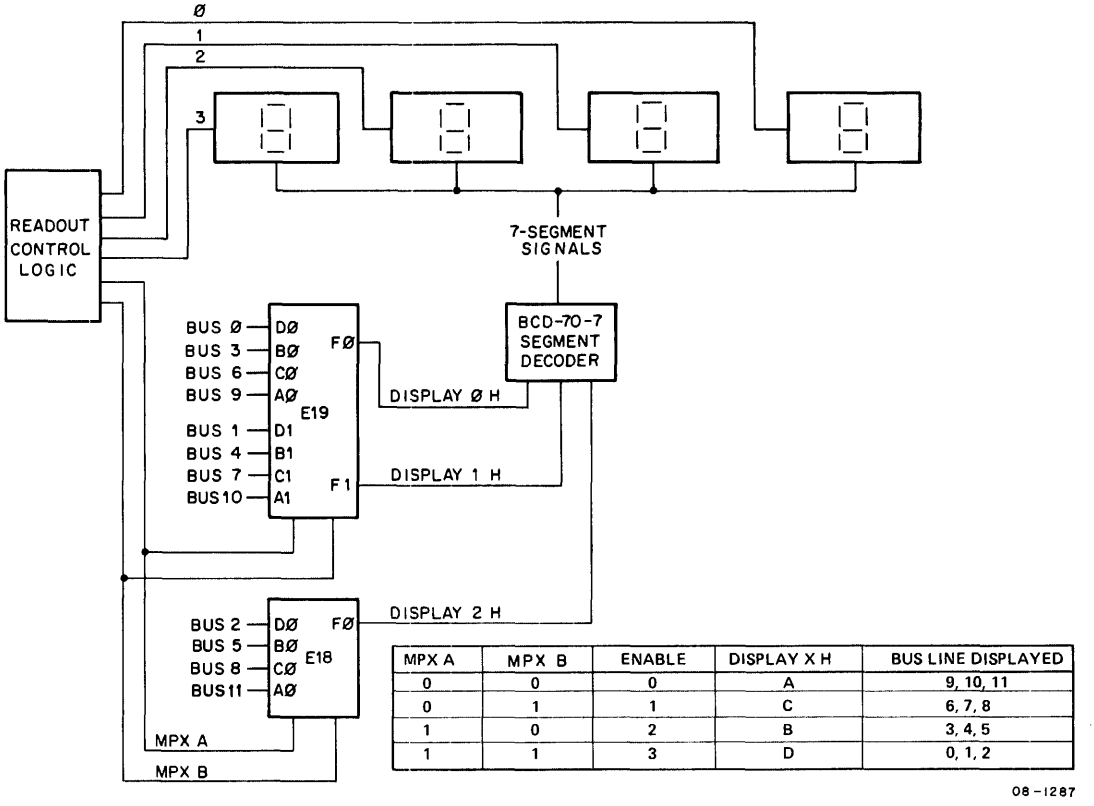
Figure 4-20 Multiplexer Logic

4.3.2.4 Register/Multiplexer Gating Logic Timing – The signals that control the Register logic and the Multiplexer logic are produced by the gating logic shown in Figure 4-22; the signals are related by the timing diagram in Figure 4-23. The lower portion of Figure 4-23 shows timing signals that are generated in the ADDRS/DISP Readout Circuit logic; these signals are included to illustrate their relationship to the MPX signals.

The timing diagram shows what happens when the operator pushes a number button, the AC button in this example, and then the DISP button. The KFUN signals (not shown) are parallel loaded into the shift register by NUM CLK H, after which the E MODE L signal goes low to place the register in the right shift mode. GATE ENT L gates the entry to BUS lines 9, 10, and 11, and the DSP LTH L signal clocks the entry into the flip-flops. MPX A and MPX B gate the entry to the DISPLAY lines and it is displayed in the right-most position of the DISP readout when the 0 signal is low.

The MA ENA L signal is asserted periodically. When this signal is low, the address on the Omnibus MA lines is placed on the console BUS lines. The ADR LTH L signal clocks the address into the flip-flops; the MPX signals gate the address to the ADDR lines, and it is displayed in the ADDRS readout. Note that MA ENA L is negated whenever the LA, the LXA, or the DEP button is pushed. Each of these buttons asserts the GATE ENT L signal for as long as the button is held down, and entry data is placed on the BUS lines for transfer to the Omnibus. Thus, address information must be kept off the BUS lines during this period.

When the DISP button is pushed at t(1) time, the E MODE L signal is negated by KEY STB H, and GATE ENT L remains high. The entry is gated to the DISP key logic on the ENT lines and loaded into flip-flops there. This action causes the AC indicator to light and asserts three signals – BUS EN L, IND1 L, and IND2 L – that transfer the contents of the AC register to the BUS lines. The DSP LTH L signal clocks the AC register data into the flip-flops, the MPX signals place the data on the DISPLAY lines, and the data is displayed in the DISP readout. As before, the address on the MA lines is displayed in the ADDRS readout (the address remains unchanged throughout the timing illustrated).



MPX A	MPX B	ENABLE	DISPLAY X H	BUS LINE DISPLAYED
0	0	0	A	9, 10, 11
0	1	1	C	6, 7, 8
1	0	2	B	3, 4, 5
1	1	3	D	0, 1, 2

Figure 4-21 MPX/Enable Signal Relationship

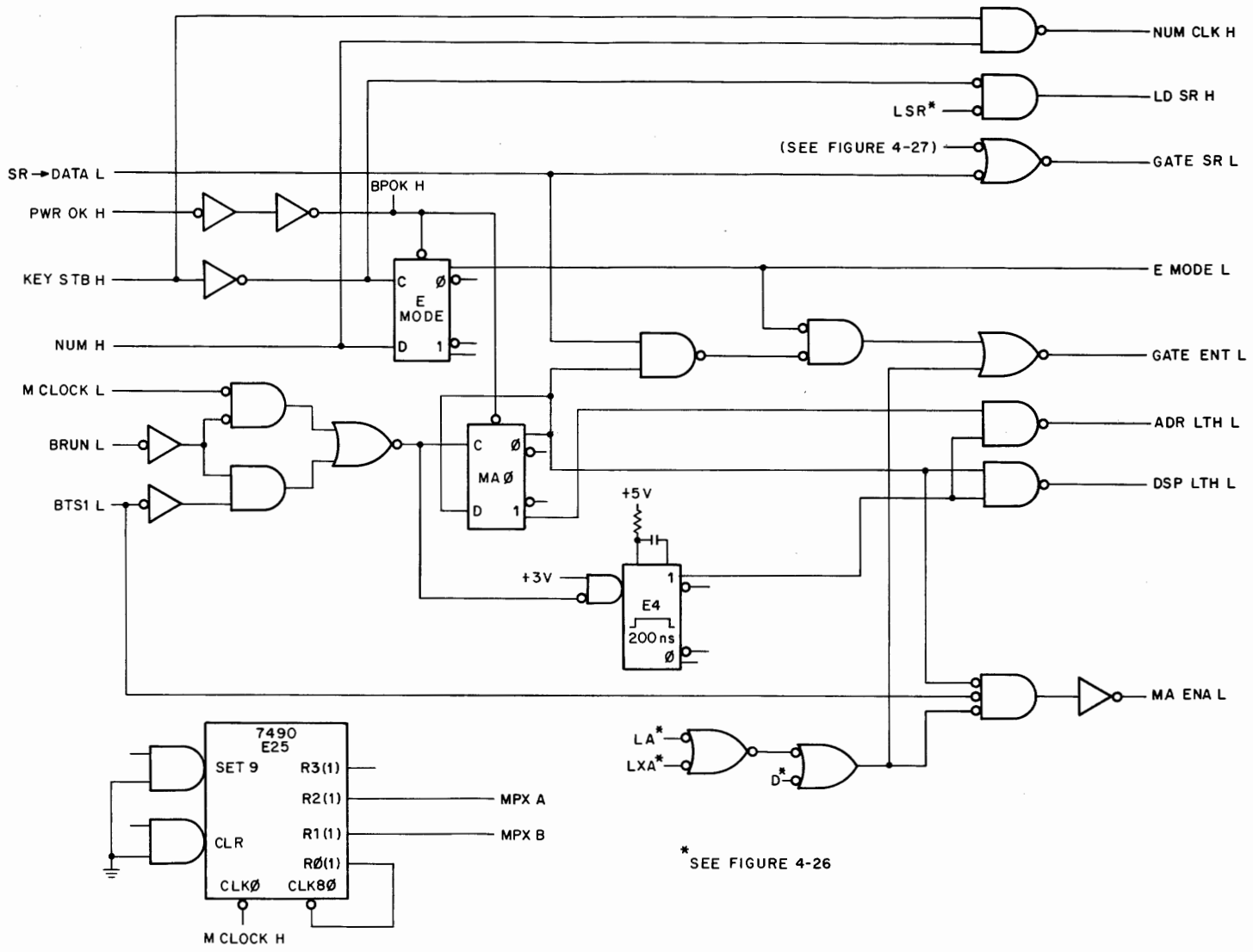


Figure 4-22 Register/Multiplexer Gating Logic

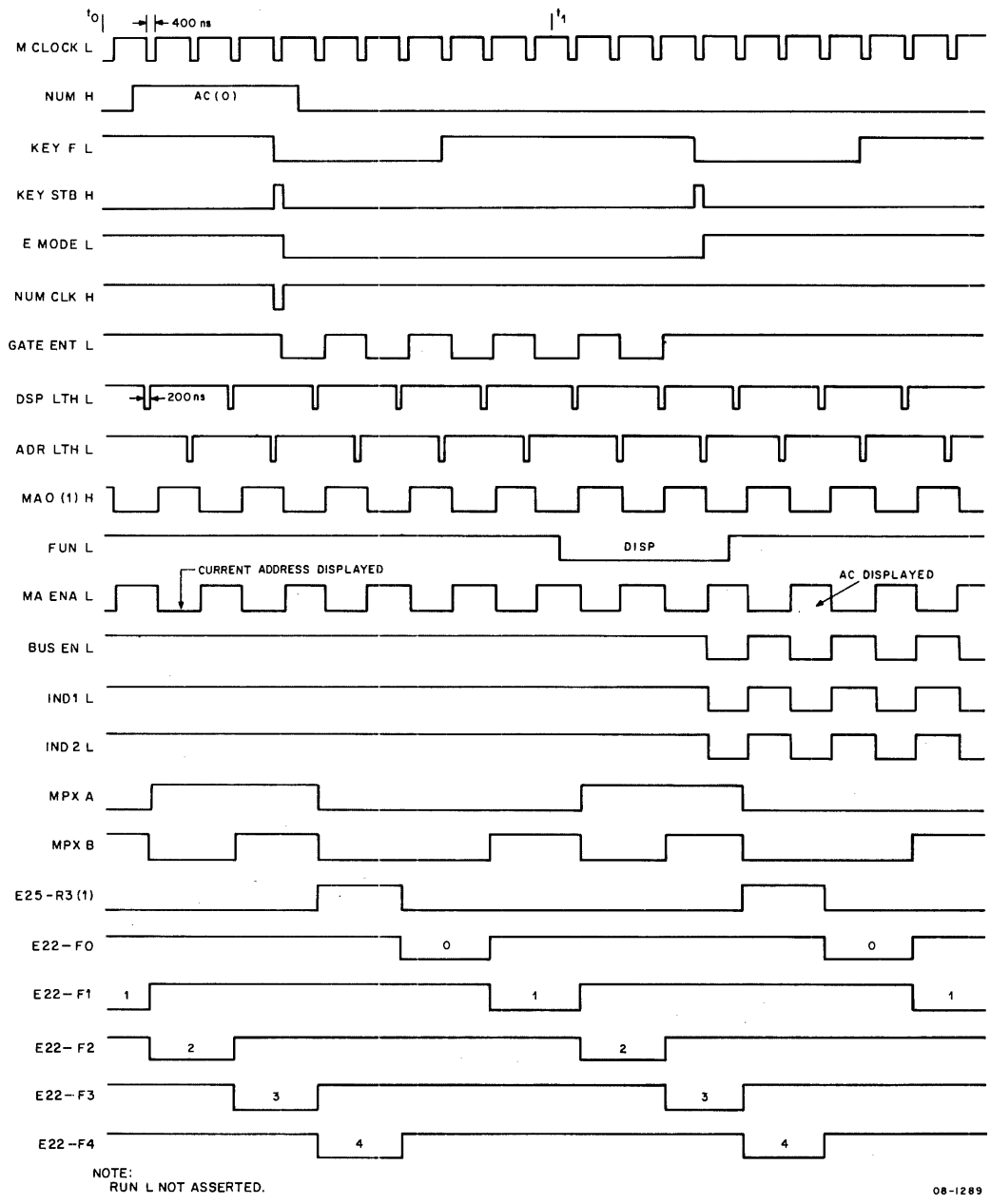


Figure 4-23 Register/Multiplexer Gating Signal Timing

4.3.2.5 ADDRS/DISP Readout Circuit Logic – The logic shown in Figure 4-24 consists largely of 7-segment LED displays. The DISP information is displayed on components E3, E4, E5, and E7; ADDRS information on components E9, E11, E12, E14; and extended memory information on component E15.

The relationship between the MPX signals and the display enable signals (0, 1, 2, 3, and 4) has been discussed and is not repeated here (refer to Paragraphs 4.3.2.2 and 4.3.2.3). When an enable signal is generated, the corresponding transistor is turned on, supplying anode current to one or more of the LED displays. For example, if 0 goes low, Q2 conducts, providing anode current for LED displays E3 and E9. Either E8 or E13, each a decoder/driver, provides high sink-current outputs that are applied to the LED cathodes. Thus, the octal information carried on the DISPLAY lines or the ADDR lines is displayed by the correct component.

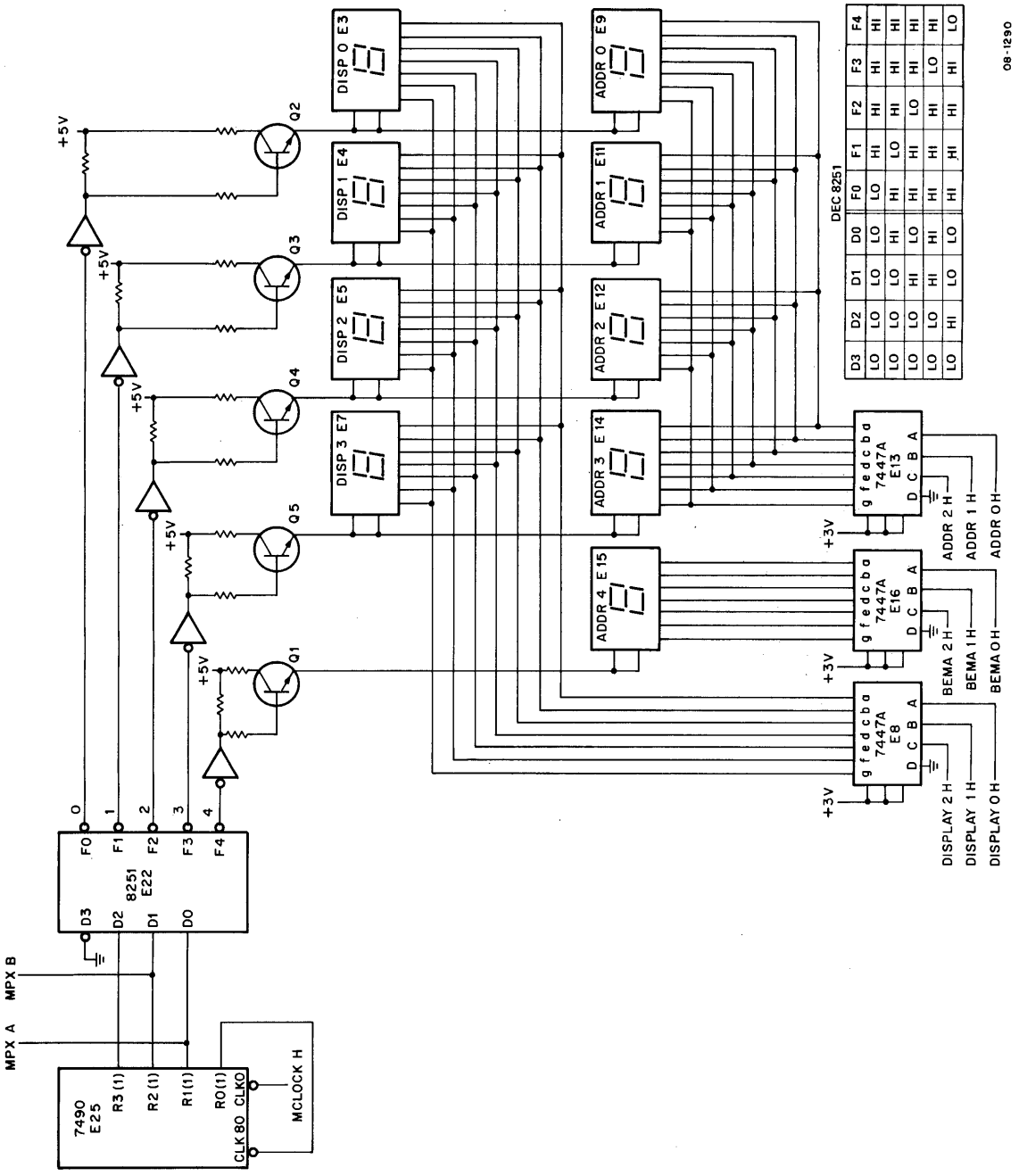


Figure 4-24 ADDRS/DISP Readout Circuits

Table 4-5 relates the displayable octal digits to the input/output signal levels of the DEC7447A decoder/drivers, while Figure 4-25 shows how the octal digits are derived in the 7-segment displays. When the digit 2 is to be displayed in one of the ADDRS LED displays, for example, output pins a, b, d, e, and g of E13 go low. The LED segments with the corresponding designations are activated and the digit appears in the readout.

Table 4-5
DEC7447A Input/Output Signals

Octal Number	Input Pins			Output Pins						
	C	B	A	a	b	c	d	e	f	g
0	LO	LO	LO	LO	LO	LO	LO	LO	LO	HI
1	LO	LO	HI	HI	LO	LO	HI	HI	HI	HI
2	LO	HI	LO	LO	LO	HI	LO	LO	HI	LO
3	LO	HI	HI	LO	LO	LO	LO	HI	HI	LO
4	HI	LO	LO	HI	LO	LO	HI	HI	LO	LO
5	HI	LO	HI	LO	HI	LO	LO	HI	LO	LO
6	HI	HI	LO	HI	HI	LO	LO	LO	LO	LO
7	HI	HI	HI	LO	LO	LO	HI	HI	HI	HI

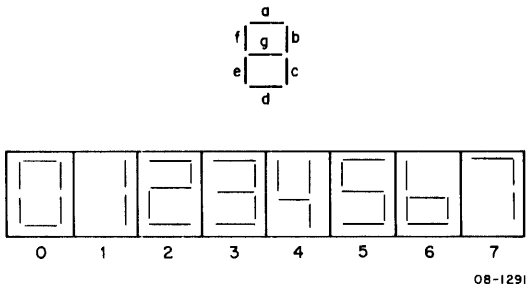
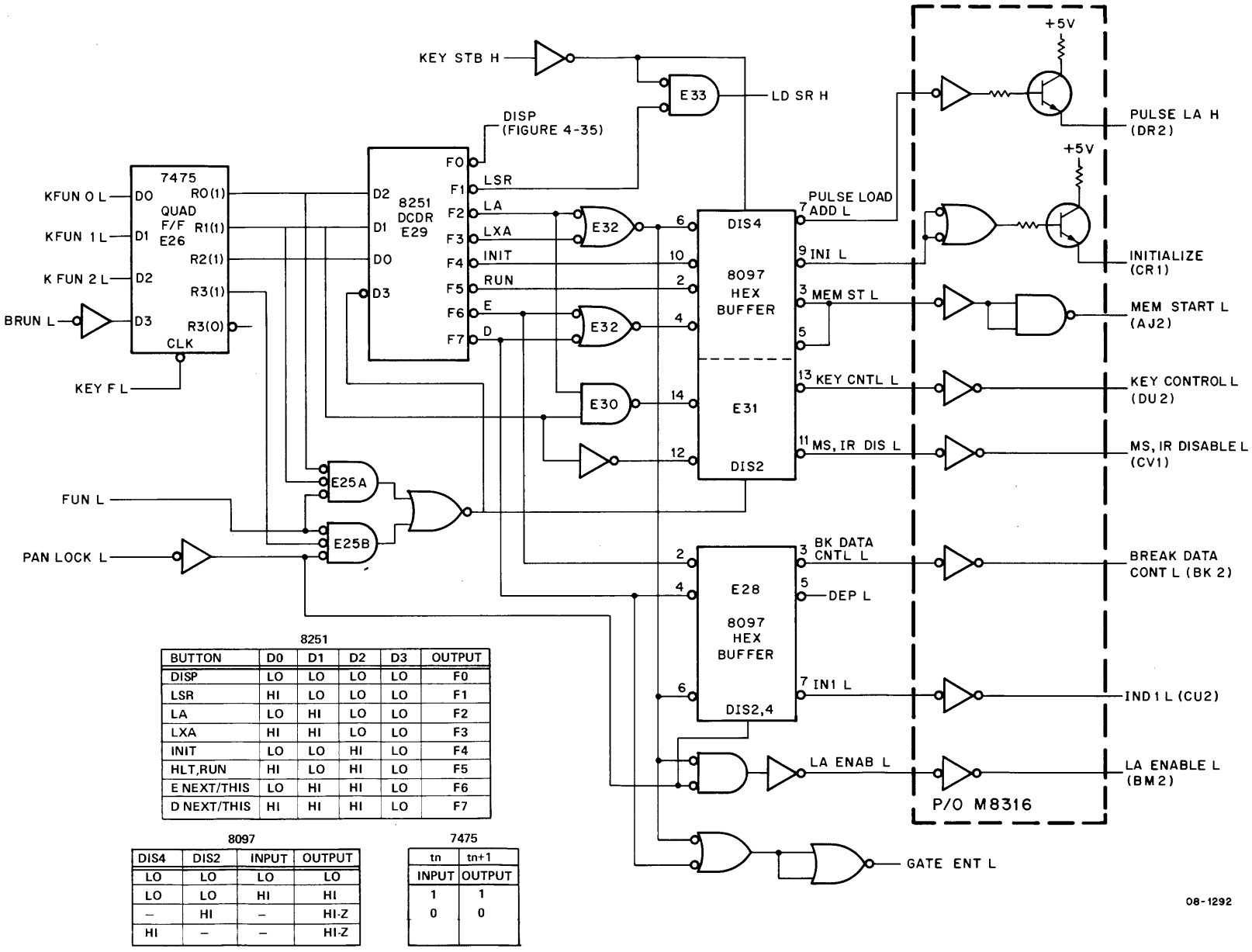


Figure 4-25 OCTAL Designations - Resultant Displays

4.3.2.6 Function Button Logic – Figure 4-26 shows the Function Button logic. The latch, E26, the BCD-to-decimal decoder, E29, and the gating logic, including hex buffers E28 and E31, are illustrated.

When a button is pushed, the binary code is clocked into the latch by the KEY F L signal. The latch output is decoded by E29 to produce an output signal that corresponds to the selected button (the 8251 function table in Figure 4-26 relates the decoder outputs to the function buttons). Note that the input at D3 of the decoder must be low. This requirement can be met in one of two ways: First, if the CPU is not running and the PANEL LOCK switch is in the off position, any function button will enable NAND gate E25B; second, if the CPU is running, the DISP button or the LSR button will enable NAND gate E25A. The second method ensures that the operator cannot inadvertently disrupt the CPU when it is in automatic operation (as will be seen, neither the DISP button nor the LSR button disrupts operation).

The decoder output signal is applied to gating logic that generates the necessary control signals (the gating logic for the DISP button is shown in a separate illustration, Figure 4-25). Table 4-6 lists the control signals generated by each function button and gives a summary of the result achieved. Refer to Paragraph 4.6.4 for a discussion of the CPU gating during console operations.



8251

BUTTON	D0	D1	D2	D3	OUTPUT
DISP	LO	LO	LO	LO	F0
LSR	HI	LO	LO	LO	F1
LA	LO	HI	LO	LO	F2
LXA	HI	HI	LO	LO	F3
INIT	LO	LO	HI	LO	F4
HLT,RUN	HI	LO	HI	LO	F5
E NEXT/THIS	LO	HI	HI	LO	F6
D NEXT/THIS	HI	HI	HI	LO	F7

8097

DIS4	DIS2	INPUT	OUTPUT
LO	LO	LO	LO
LO	LO	HI	HI
–	HI	–	HI-Z
HI	–	–	HI-Z

7475

tn	tn+1
INPUT	OUTPUT
1	1
0	0

Figure 4-26 Function Button Logic

Table 4-6
Function Button Control Signals

Function Button	Control Signal Generated	Signal Function
LSR	LD SR H	Load entry into Switch Register.
LA	MS, IR DIS L	Asserts the Omnibus MS, IR DISABLE L signal, placing the CPU in the DMA state and, thus, permits the console to communicate directly with memory (refer to Paragraph 4.6.4, Data Break Transfers).
	GATE ENT L	Gates the entry from the number shift register to the console BUS lines.
	LA ENAB L	Causes the Programmer's Console control to generate the KCCN1 SR ENABLE L signal, thereby gating the entry from the BUS lines to the Omnibus DATA lines.
	IN1 L	Generates the IND1 L signal ensuring that only the entry is placed on the DATA Bus. IND1 L and IND2 L determine the type of information placed on the DATA bus during TS1. The information can be any of the following: **IND1 L / IND2 L / DATA Bus Information** HI / HI / Status word (see Table 4-15 for the Status word description) HI / LO / MQ register contents LO / HI / Logic 0 (HI) LO / LO / AC register contents
	PULSE LOAD ADD L	After the entry has been gated from the DATA bus to the CPMA register, PULSE LA H causes the CPMA LOAD signal to be generated, loading the entry into the register. Note that buffer E31 generates PULSE LOAD ADD L when KEY STB H is asserted, which is quite some time after the entry has been placed on the DATA bus (the top four outputs of E31 are controlled by the enable input at DIS4, while the bottom 2 outputs are controlled via DIS2).
LXA	MS, IR DIS L GATE ENT L LA ENAB L IN1 L	See entry for LA.
	KEY CNTL L	Causes the Omnibus KEY CONTROL L signal to be asserted. This signal and LA ENABLE L combine to gate the entry from the DATA bus to the IF and DF registers of the extended memory option.

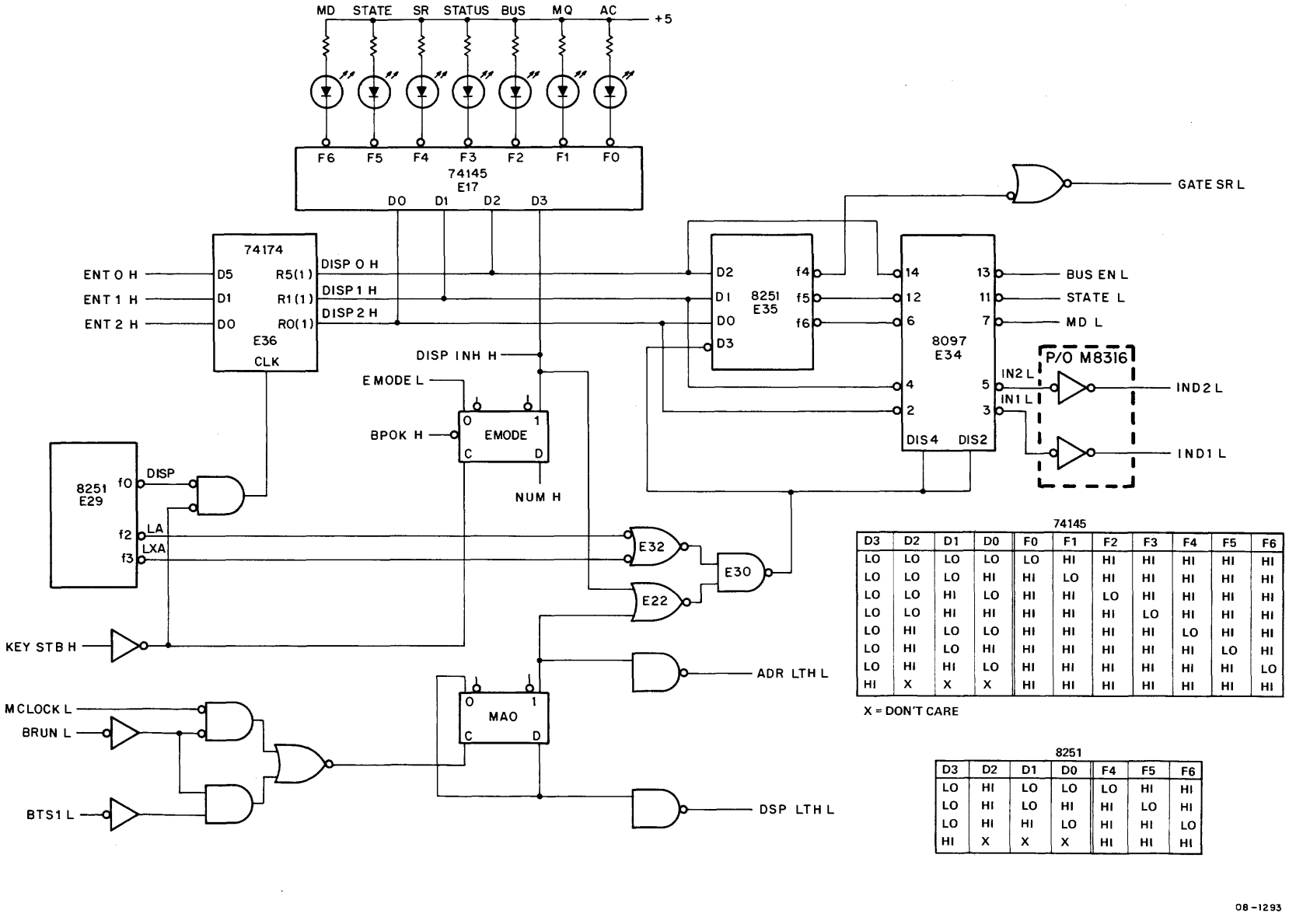
Table 4-6 (Cont)
Function Button Control Signals

Function Button	Control Signal Generated	Signal Function
	PULSE LOAD ADD L	Causes the extended memory control (M8317) to generate a clock pulse that loads the entry into the IF and DF register.
INIT	INI L	Asserts the Omnibus INITIALIZE L signal, causing the AC, the Link, the interrupt system, and peripheral flags to be cleared.
RUN	MEM ST L	Asserts the Omnibus MEM START L signal, causing the CPU timing generator (TG) to start generating timing signals.
ETHIS	MEM ST L	See 'RUN'.
	MS, IR DIS L	See 'LA'.
	KEY CNTL L BK DATA CNTL L	These two signals assert Omnibus signals KEY CONTROL L and BREAK DATA CONT L, respectively; these Omnibus signals, along with LA ENABLE L, control CPU major register gating operations in the DMA state. When BREAK DATA CONT L and KEY CONTROL L are low and LA ENABLE L is high, the following sequence of events occurs: During TS1 the contents of the CPMA register are incremented and loaded into the PC register; during TS2 the contents of the addressed memory location are placed on the MD lines and loaded into the MB register; during TS3 the Omnibus STOP L signal is generated causing the TG RUN flip-flop to be cleared at TP3 time (the TG halts in TS1, after TS4 operations have been completed — see 'THIS L' for a description of TS4 operations). The operator can cause the data contained in the MB register to be displayed in the DISPLAY readout by pushing the MD button and then the DISP button. Alternatively, the operator can push the console buttons in the following order to examine a memory location: LA; MD; DISP; ETHIS.
	THIS L (Generated by clock timing logic)	Asserts the Omnibus MA, MS LOAD CONT L signal, preventing TP4 from loading the CPMA register. Thus, the addressed memory location remains unchanged and the operator can modify the data by using the deposit function.

Table 4-6 (Cont)
Function Button Control Signals

Function Button	Control Signal Generated	Signal Function
ENEXT		This pushbutton generates the same signals as does ETHIS, except for THIS L. Hence, the CPMA register is loaded at TP4 time and a new address is placed on the MA lines during TS1 of the next timing cycle. The operator can use this button to examine consecutive memory locations. The following order is most advantageous: MA; MD; DISP; ENEXT; ENEXT . . .; ENEXT.
DTHIS	MEM ST L	See 'RUN'.
	MS, IR DIS L	See 'LA'.
	GATE ENT L	Gates the entry from the number shift register to the console BUS lines.
	DEP L	Asserts the console KCCN1 SR ENABLE L signal, which gates the entry from the BUS lines to the Omnibus DATA lines; the entry is placed on the CPU SUM lines and loaded into the MB register at TP2 time. During the write half of the timing cycle the entry is written into the addressed memory location.
	KEY CNTL L	When LA ENAB L and BK DATA CNTL L are high and KEY CNTL L is low, the following sequence of events occurs in the CPU major register gating: During TS1 the contents of the CPMA register are incremented and loaded into the PC register; during TS2 the DATA lines are gated to the CPU SUM lines; during TS3 the STOP L signal is generated, causing the RUN flip-flop to be cleared at TP3 time (the TG halts in TS1, after TS4 operations have been completed — see 'THIS L' for a description of TS4 operations).
	THIS L (Generated by clock timing logic)	Asserts MA, MS LOAD CONT L, preventing TP4 from loading the CPMA register. Thus, the addressed memory location remains unchanged.
DNEXT		This button generates the same signals as does DTHIS, except for THIS L. Thus, DNEXT can be used to deposit data in consecutive memory locations.

4.3.2.7 DISP Button Logic – Figure 4-27 shows the logic associated with the DISP button. This button is used when the operator wishes to display the contents of a register (AC, MQ, or SR), or the information carried by a bus (DATA, MD), or STATE information. The pushbutton has two functions: It causes the appropriate console indicator to light, signifying the source of the information being displayed; and it generates the control signals that gate the appropriate data to the display readout on the console.



74145

D3	D2	D1	D0	F0	F1	F2	F3	F4	F5	F6
LO	LO	LO	LO	LO	HI	HI	HI	HI	HI	HI
LO	LO	LO	HI	HI	LO	HI	HI	HI	HI	HI
LO	LO	HI	LO	HI	HI	LO	HI	HI	HI	HI
LO	LO	HI	HI	HI	HI	HI	LO	HI	HI	HI
LO	HI	LO	LO	HI	HI	HI	HI	LO	HI	HI
LO	HI	LO	HI	HI	HI	HI	HI	HI	LO	HI
LO	HI	HI	LO	HI	HI	HI	HI	HI	HI	LO
HI	X	X	X	HI	HI	HI	HI	HI	HI	HI

X = DON'T CARE

8251

D3	D2	D1	D0	F4	F5	F6
LO	HI	LO	LO	LO	HI	HI
LO	HI	LO	HI	HI	LO	HI
LO	HI	HI	LO	HI	HI	LO
HI	X	X	X	HI	HI	HI

08-1293

Figure 4-27 DISP Button Logic

Whenever a number button is pushed, the binary code for that button is entered in the number shift register; the code is carried on the ENT0 H, ENT1 H, and ENT2 H lines to the DEC74174 hex flip-flop (E36 in Figure 4-27). When the operator pushes the DISP button, decoder E29 generates the DISP signal that enables KEY STB H to load the binary code into E36. Hence, the code appears on the DISP0 H, DISP1 H, and DISP2 H lines.

A DEC74145 decoder, E17, monitors the DISP lines and causes an appropriate indicator to light. The function table in Figure 4-27 indicates the relationship between the DISP lines and the source indicators (note that the EMODE flip-flop must be in the clear state for an indicator to be lighted; this flip-flop ensures that a lighted indicator is turned off when the next number button is pushed).

A DEC8251 decoder, E35, and a hex buffer, E34, also monitor the DISP lines; these two components generate the signals that cause the information to be gated to the DISPLAY readout. Table 4-7 relates the number buttons, the DISP0 H, DISP1 H, DISP2 H signals, and the control signals generated by E34 and E35. The top four entries (buttons 0 through 3) indicate that BUS EN L is asserted, along with some combination of IND1 L and IND2 L. BUS EN L causes information on the Omnibus DATA lines to be gated to the console BUS lines (Paragraph 4.3.2.9), while the IND signals select the type of information that is placed on the DATA lines by the CPU major register gating (refer to the LA entry in Table 4-6, which relates IND signals and DATA bus information). The last three entries also indicate some combination of the IND signals being generated; however, the signals fall into the "don't care" category in these situations. The MD L and STATE L signals gate information from the MD bus and from selected Omnibus lines, respectively, onto the console BUS lines, while the GATE SR L signal gates the console switch register contents to the BUS lines. The information on the BUS lines is clocked into flip-flops in the multiplexer logic by the DSP LTH L signal (Figure 4-20) and displayed in the DISPLAY readout.

Table 4-7
Display Control Signals

Button	DISP0 H	DISP1 H	DISP2 H	Control Signal(s)
0(AC)	LO	LO	LO	BUS EN L, IND1L, IND2L
1(MQ)	LO	LO	HI	BUS EN L, IND2L
2(BUS)	LO	HI	LO	BUS EN L, IND1L
3(STATUS)	LO	HI	HI	BUS EN L
4(SR)	HI	LO	LO	GATE SR L, IND1L, IND2L
5(STATE)	HI	LO	HI	STATE L, IND2L
6(MD)	HI	HI	LO	MD L, IND1L

When a source has been selected for display, the source identity is loaded into the hex flip-flop E36. Hence, the DISP lines reflect this identity until another source is selected for display. In some circumstances, the control signals generated by E34 and E35 could impair operation, consequently, some means must be provided to prevent the signals from being generated in such circumstances. These means are provided by NAND gate E30, which, when inhibited, disables E34 and E35. The contents of a source are displayed during alternate periods of the MCLOCK L signal (when the CPU is not running) or during TS1 of alternate timing cycles. The display information timeshares the BUS lines with current address information that is displayed in the ADDR readout. This timesharing is accomplished by the MA0 flip-flop, which alternately enables and disables NOR gate E22; thus, E34 and E35 are disabled during the time that the address information is being routed to the ADDR readout.

NOR gate E22 also inhibits E30 when the EMODE flip-flop is set. As noted earlier, a lighted indicator is turned off by this flip-flop when a number button is pushed. More importantly, the control signals are negated so that the entry can be viewed in the DISPLAY readout as it is being entered via the number buttons.

Another situation that requires E34 and E35 to be disabled arises when either the LA or the LXA pushbutton is activated. In such a situation an address is placed on the BUS lines and gated to the Omnibus DATA lines; consequently, display information must be kept off the DATA lines during the time that these functions are active. This is accomplished by NOR gate E32, which inhibits NAND gate E30 when the LA or LXA signal is generated by decoder E29.

4.3.2.8 THIS, HLT, BOOT Logic – The logic shown in Figure 4-28 has several functions. Consider the HLT/SS pushbutton. If the CPU is running when the operator pushes this button, the Omnibus STOP L signal is asserted and the RUN flip-flop is cleared at TP3 time (Figure 4-3); the CPU stops in TS1. If the CPU is stopped when the button is pushed, not only is the STOP L signal asserted, but also the MEM ST L signal (Figure 4-28); hence, the CPU executes one timing cycle before stopping in TS1. Note that the PANEL LOCK L signal must be negated for the DEC8097 hex buffer to operate. Thus, the CPU cannot be halted when the PANEL LOCK switch on the Limited Function Panel is in the up position. Furthermore, as Figure 4-26 shows, if the PANEL LOCK switch is on when the CPU is stopped, the processor cannot be started.

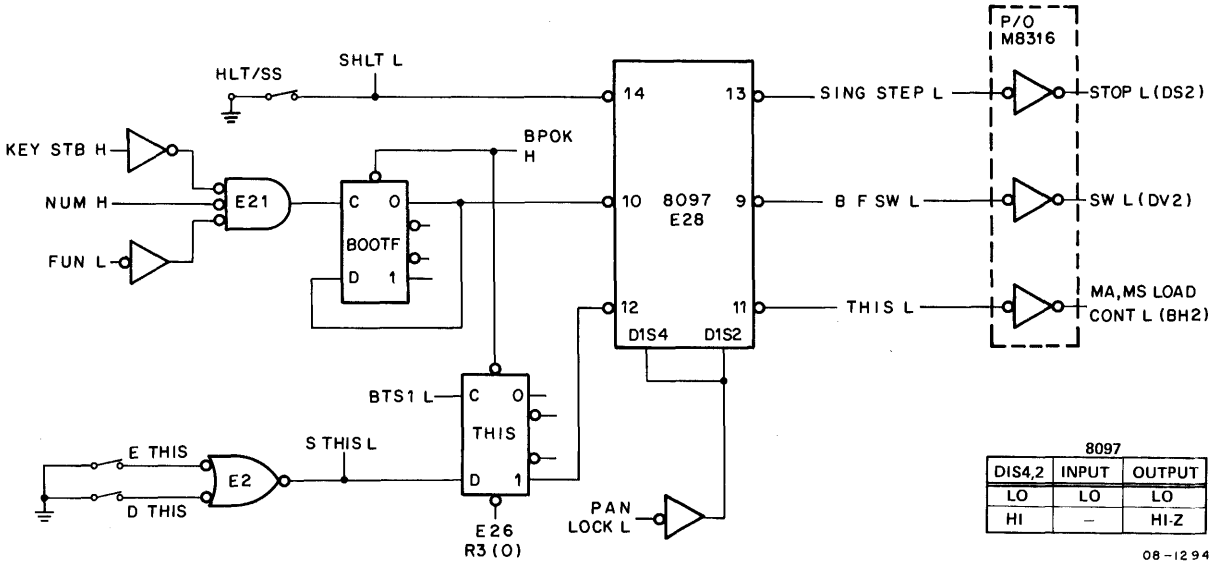


Figure 4-28 THIS, HLT, BOOT Logic

Both the ETHIS and the DTHIS pushbuttons start a timing cycle. The single cycle that is executed differs from that executed by the ENEXT/DNEXT functions in one way, i.e., the memory address is not updated when the THIS functions are used. The THIS flip-flop, which is clocked at the end of TS1, is cleared when either of the THIS buttons is pushed; thus, the MA,MS LOAD CONT L signal is asserted, preventing the CPMA LOAD signal from being generated at TP4 time of the timing cycle.

The dc set input of the THIS flip-flop is connected as shown to prevent improper operation should the ETHIS or DTHIS button be pushed by mistake while the CPU is running. The dc set line is held low when the RUN L signal is asserted, preventing the flip-flop from being cleared by the BTS1 L signal should STHIS L be inadvertently generated.

The BOOT pushbutton enables the operator to load bootstrap programs. A low-to-high transition of the Omnibus SW L signal causes the bootstrap option control (M8317) to initiate a bootstrap operation, provided the CPU is not running. To bring about this transition of the SW L signal, the operator must push the BOOT button twice. The first push causes NAND gate E21 to set the BOOTF flip-flop (the KEY STB H pulse is generated when BOOT is pushed, but neither NUM H nor FUN L is asserted); the second push causes the flip-flop to be cleared. Thus, the SW L signal first goes low and then goes high, initiating the bootstrap operation.

4.3.2.9 Console Control Logic – The Console Control logic is part of the I/O Option board (M8316) that plugs into the PDP-8/A Omnibus. Data is transferred between the Omnibus and the console logic via the Console Control logic. The complete logic drawings for the console control are included in Appendix H of this manual. Figures 4-29 and 4-30 show portions of that logic to illustrate how data is handled by the control.

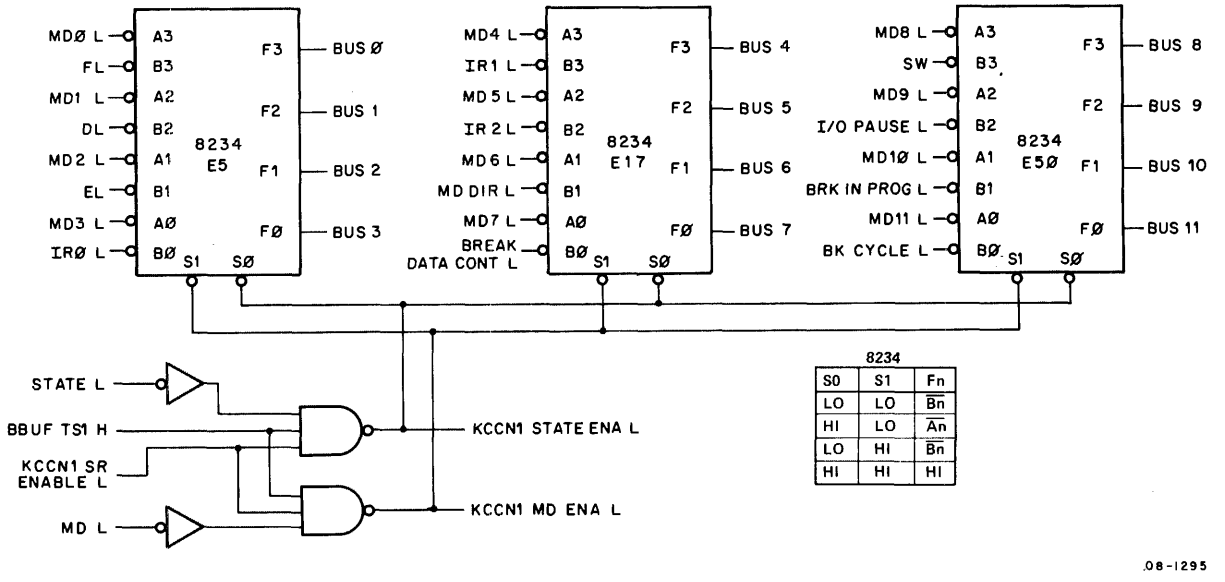


Figure 4-29 Console Control Logic — STATE, MD

Figure 4-29 shows how STATE data and data carried by the MD lines are placed on the console BUS lines. The DEC 8234 multiplexers are controlled by the two enable signals, KCCN1 MD ENA L and KCCN1 STATE ENA L. When the operator pushes the appropriate console button – MD or STATE – and then pushes the DISP button, either MD L or STATE L is asserted by the DISP button logic. If the CPU is in TS1 and KCCN1 SR ENABLE L is negated, the applicable data is gated onto the BUS lines.

Logic that performs a function similar to that of Figure 4-29 is shown at the top of Figure 4-30. Multiplexer E1 places either MA bus information or DATA bus information on the BUS lines. Only the multiplexer that accommodates bits 0 through 3 is shown; bits 4 through 11 are handled in like manner. Remember that MA bus data is displayed during alternate periods of the MCLOCK L signal when the CPU is halted, or during TS1 of alternate timing cycles when the CPU is running. The information on the DATA bus can be displayed during those alternate periods when MA bus data is not displayed. If the operator wants to view the contents of the MQ register, for example, he or she pushes number button 1 and then the DISP button. The BUS EN L signal is asserted, the MQ contents are placed on the BUS lines and displayed in the DISPLAY readouts.

The foregoing operation, as well as those carried out by the logic in Figure 4-29, depends on the KCCN1 SR ENABLE L signal being negated. The logic that generates KCCN1 SR ENABLE L is shown at the bottom of Figure 4-30. This signal gates Bus-lines information onto the DATA bus in three situations: When either the LA or the LXA pushbutton is activated, generating LA ENAB L and causing the entry to be loaded into the CPMA register; when either the DTHIS or the DNEXT pushbutton is activated, generating DEP L during TS2 and causing the entry to be loaded into the MB register; or, when either an LAS (7604) or an OSR (7404) operate instruction is programmed, generating SR DATA L during TS3 and causing the result of the specified operation to be loaded into the AC register.

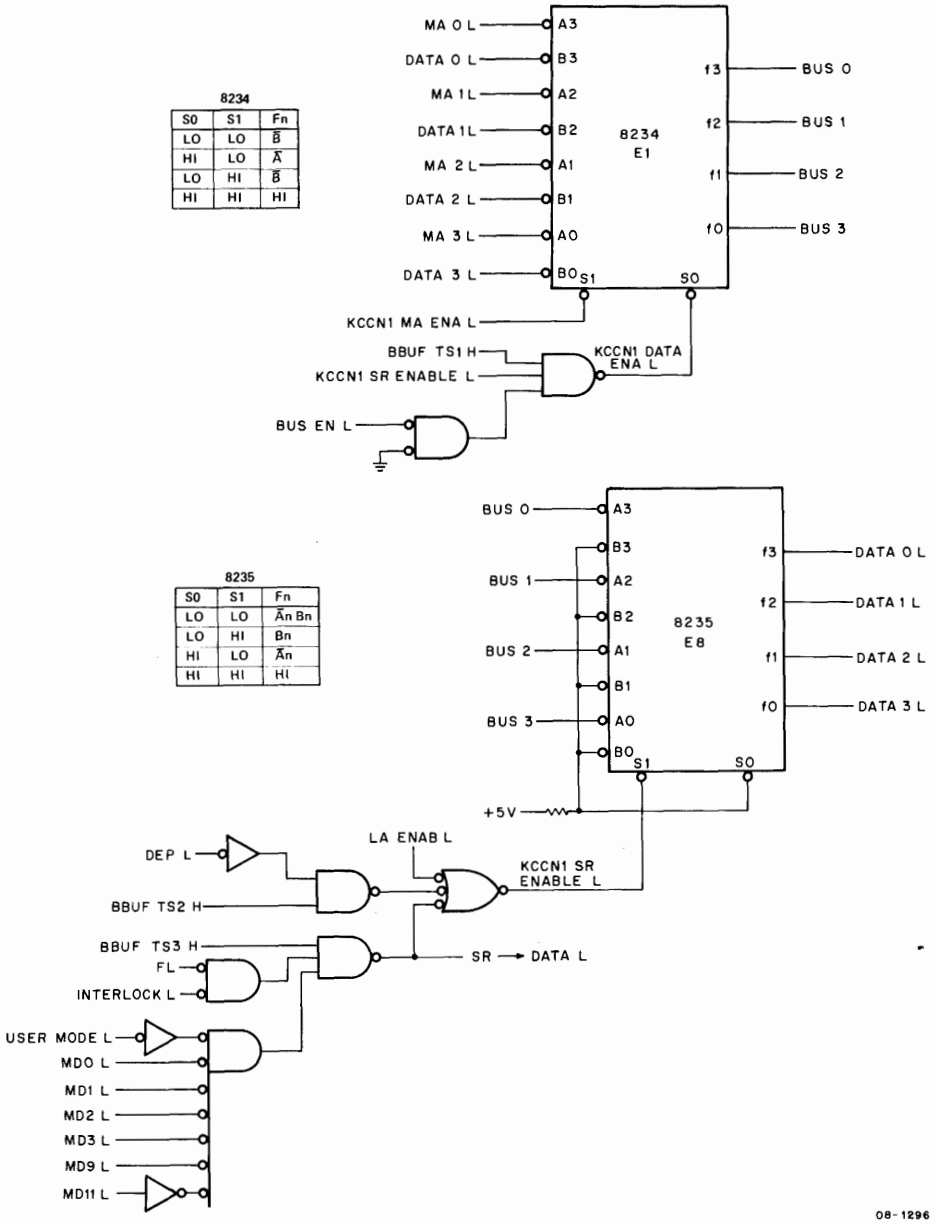


Figure 4-30 Console Control Logic-MA, DATA, SR ENABLE

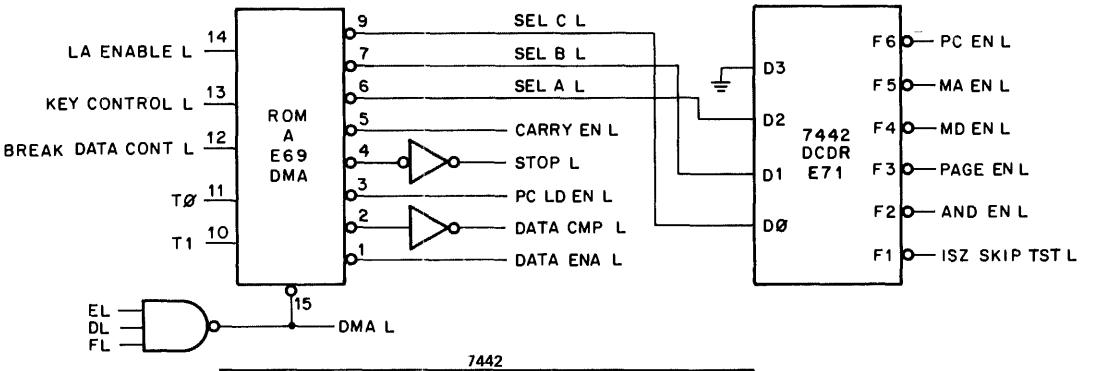
4.4 INSTRUCTION DECODER

Logic within the ID, monitors the MD lines, decoding the information thereon and generating major register gating control signals. The gating control signals are developed largely in response to basic instructions, CPU major states, and time states and time pulses. In addition, Programmer's Console operations and I/O transfers can control major register gating to some extent.

The ID logic (Figure 4-16) includes the Instruction Register, the Major State Register, the AC Register gating, and a number of Read-Only Memories (ROMs). The ROMs play a most important part in the CPU operation. Major register gating responds, basically, to program instructions or as a result of directions entered manually at the Programmer's Console. Program instructions include memory reference instructions, operate instructions, and IOT instructions; each

of these types of instructions can be subdivided further. Furthermore, each instruction behaves differently depending on the particular major state and time state. Consequently, major register gating control signals must be generated under a variety of circumstances. A most convenient method of accommodating such an abundance of variables is to devote a ROM to a significant set of circumstances. Thus, we have ROM D dedicated to operate microinstructions during TS3, ROM J responding to Processor-IOT instructions during TS4, ROM F decoding skip and link instructions during TS3, and so on.

The ROMs are illustrated in Figures 4-31 through 4-38 as they appear in the logic diagrams. All except ROM F (a 1024-bit ROM) are 256-bit ROM organized as 32 8-bit words selected by a 5-bit input code. Pins 10 through 14 are the input pins, pin 14 representing the most significant bit of the input code. Pins 1 through 7 and 9 are the output pins, while pin 15 is an enable input (a low voltage applied to this pin enables the ROM to function). For ROM F the input pins are 1 through 7 and 15 (15 is most significant), the output pins are 9 through 12 (10 and 12 are not used), and the enable pins are 13 and 14.

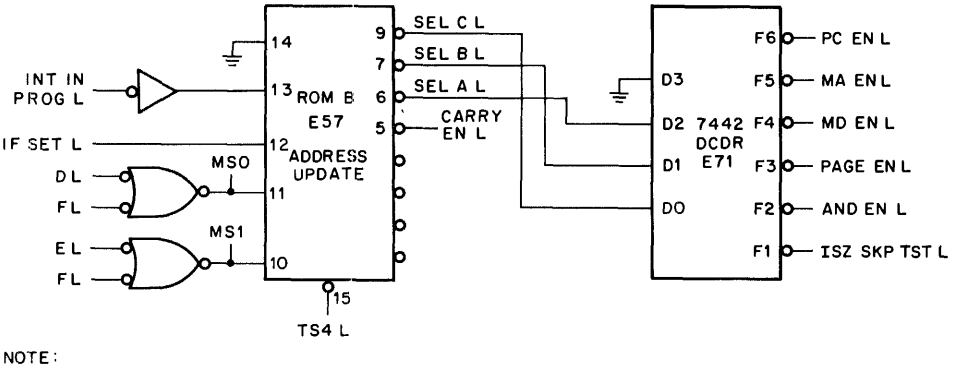


7442

D3	D2	D1	D0	F1	F2	F3	F4	F5	F6
LO	LO	LO	HI	LO	HI	HI	HI	HI	HI
LO	LO	HI	LO	HI	LO	HI	HI	HI	HI
LO	LO	HI	HI	HI	HI	LO	HI	HI	HI
LO	HI	LO	LO	HI	HI	HI	LO	HI	HI
LO	HI	LO	HI	HI	HI	HI	HI	LO	HI
LO	HI	HI	LO	HI	HI	HI	HI	HI	LO

08-1297

Figure 4-31 ROM A Logic



NOTE:
For 7442 function table see ROM A.

08-1298

Figure 4-32 ROM B Logic

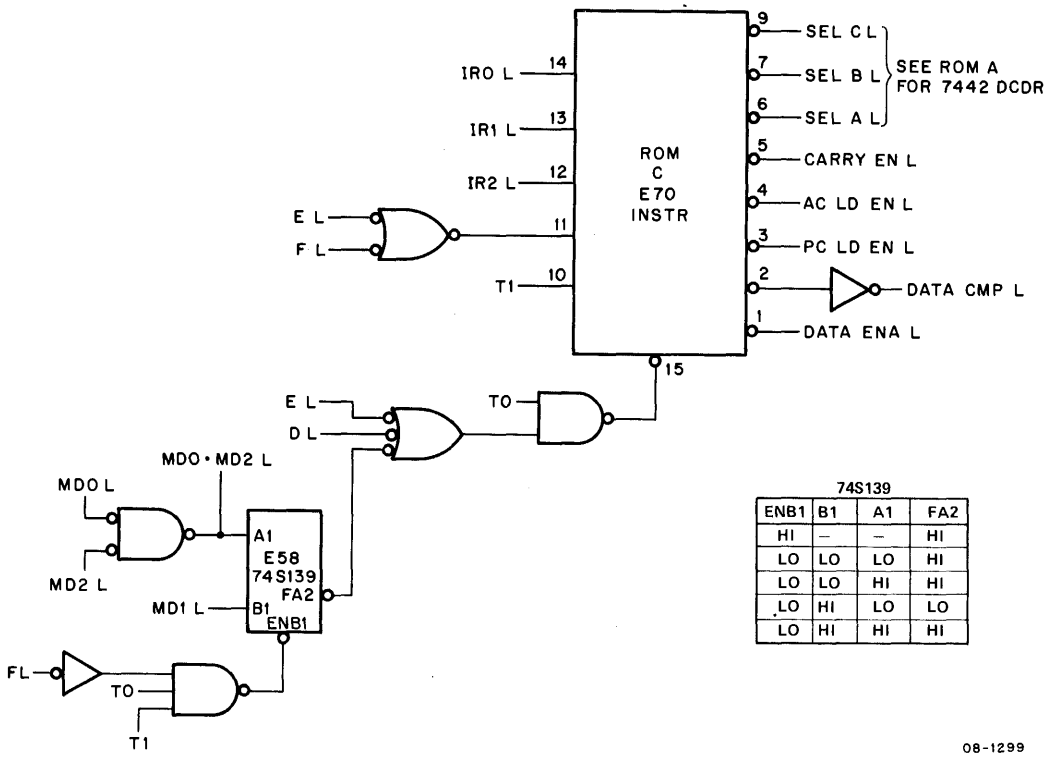


Figure 4-33 ROM C Logic

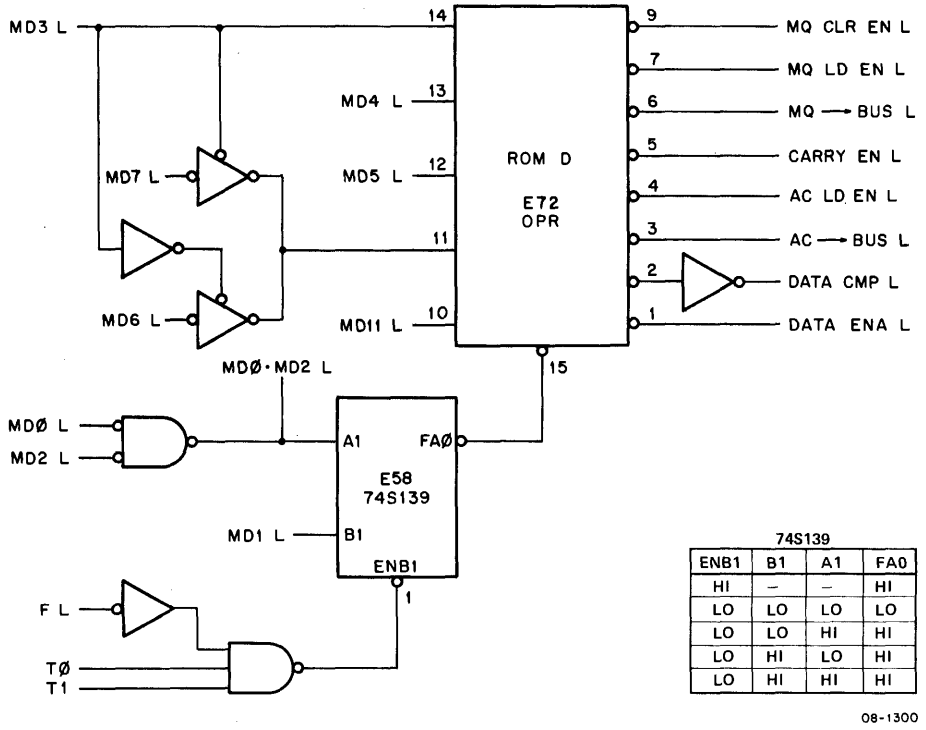


Figure 4-34 ROM D Logic

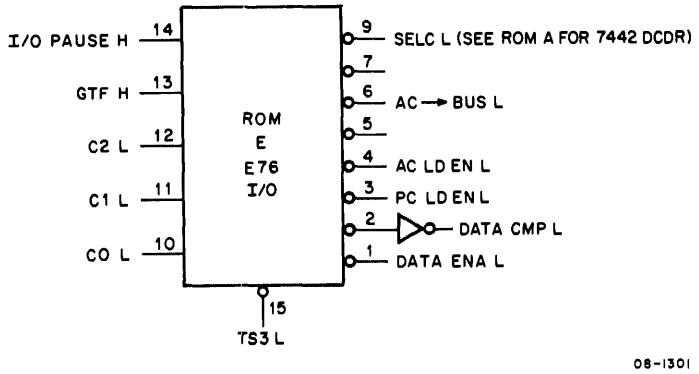


Figure 4-35 ROM E Logic

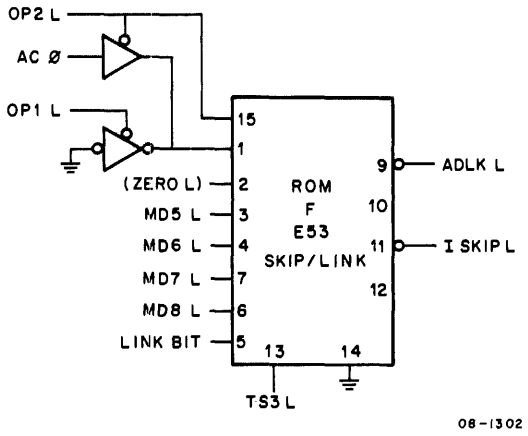


Figure 4-36 ROM F Logic

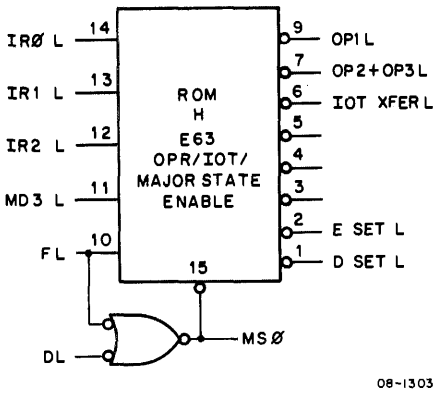


Figure 4-37 ROM H Logic

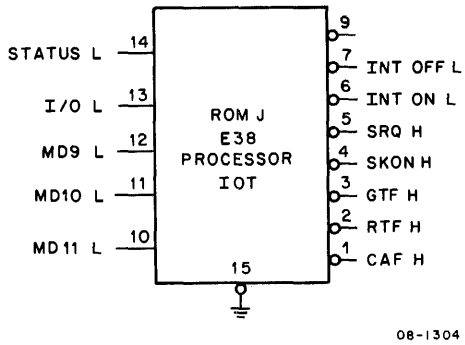


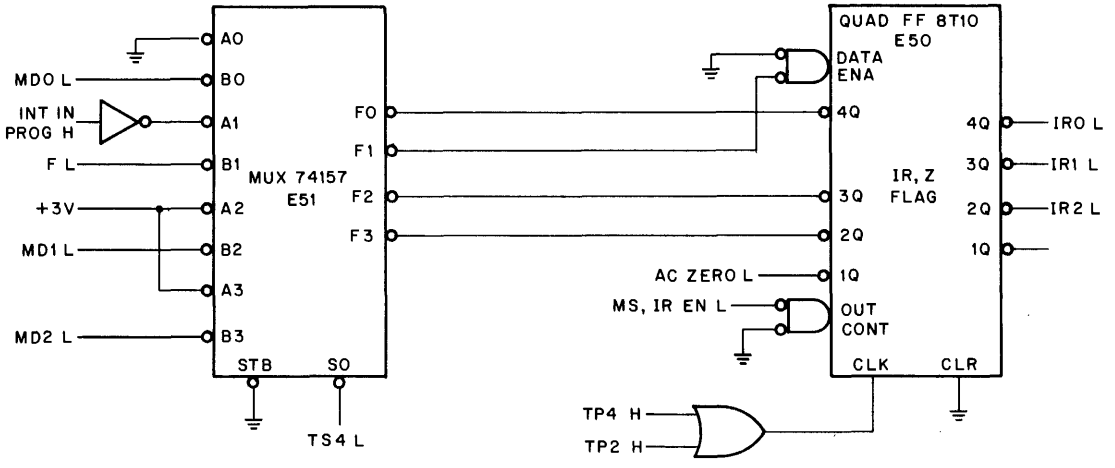
Figure 4-38 ROM J Logic

Note that most of the ROM input signals are taken from the MD lines, the Instruction Register (IR lines), and the Major State Register. For the moment it is enough to be aware of the logic shown in Figures 4-31 through 4-38. In Paragraph 4.5, tables are provided that enable one to determine easily the input/output relationship for each ROM and to relate the ROM outputs to the major registers and gating. ROMs H and J are used for other than major register gating purposes and are discussed in Paragraphs 4.4.2 and 4.6, respectively.

In addition to the logic already mentioned, the ID includes logic that supplements the ROMs for special purposes. This logic is discussed in paragraphs following the Instruction Register and Major State Register descriptions.

4.4.1 Instruction Register Logic

The Instruction Register logic is shown in Figure 4-39. Operations in each CPU Major State are determined by the type of instruction contained in the addressed memory location. This instruction is placed on the MD lines during TS2 of a Fetch cycle. MD bits 0, 1, and 2, which identify the basic instruction, are applied to the B inputs of the DEC74157 multiplexer. During TS2, these input signals are gated to the multiplexer outputs and applied to the data inputs of the quad flip-flop. Because the CPU is in the Fetch state, both enabling inputs of the quad flip-flop are low, and at TP2 time the individual flip-flops are clocked. The flip-flop outputs, which represent the basic instruction (see the IR Table), are distributed throughout the CPU logic on the IR lines.



74157

S0	An	Bn	Fn
LO	LO	X	LO
LO	HI	X	HI
HI	X	LO	LO
HI	X	HI	HI

8T10

NQ IN	DATA ENA	OUT CONT	NQ OUT
LO	LO	LO	LO
HI	LO	LO	HI
X	HI	LO	NO CHANGE
X	X	HI	HI-Z

IR TABLE

IR0	IR1	IR2	INST
HI	HI	HI	AND
HI	HI	LO	TAD
HI	LO	HI	ISZ
HI	LO	LO	DCA
LO	HI	HI	JMS
LO	HI	LO	JMP
LO	LO	HI	IOT
LO	LO	LO	OPR

08-1305

Figure 4-39 Instruction Registers Logic

During TS4, the signals on the A inputs of the multiplexer are gated to the flip-flop inputs. Providing an interrupt has not been honored, the flip-flop is placed in a "no change" state; thus, the flip-flop outputs remain unchanged at TP4 time. However, if the INT IN PROG H signal had been asserted at TP3 time, the flip-flop's contents are changed at TP4 time. The IR lines then represent the JMS instruction and, because the Major State register logic asserted the E L signal at the same TP4 time, the CPU enters the Execute state and performs the JMS operations. An interrupt can be honored during any major state timing cycle, as long as the cycle is the last one of the instruction; therefore, the IR lines can be changed at TP4 of any state, as the logic demonstrates.

The MS, IR EN L signal can be negated at TP4 time by a data break peripheral or by the Programmer's Console. The flip-flop outputs are removed from the IR lines and the CPU enters the DMA state.

When MS, IR EN L is asserted again, the IR lines assume the states that existed before the DMA interruption and the interrupted instruction operations are resumed. If the MS, IR EN L signal is negated at the same time that the IR flip-flops are clocked to the JMS state (as a result of INT IN PROG H being asserted), the CPU enters the DMA state. On completion of the DMA operations, the CPU enters the Executive state and performs the JMS operation.

4.4.2 Major State Register Logic

The CPU operations are grouped functionally into the four major states – Fetch, Defer, Execute, and DMA. The first three are entered actively when flip-flops in the Major State Register logic are set (only one major state flip-flop may be active at any given time). The fourth state, DMA, results when none of the first three has been entered.

The logic is shown in Figure 4-40 and includes ROM H. Table 4-8 relates the input and output signals of ROM H, the basic instruction involved, and the present and next CPU Major State. For example, input code 22(8) occurs during the Fetch cycle of a DCA instruction, resulting in the E SET L signal being asserted by the ROM. Note that the INPUT SIGNAL LOW column indicates the signals that must be low to achieve the desired input code (this convention is chosen because most of the Omnibus signals are active when low). Three stages of the 8T10 quad flip-flop are used to generate the F L, D L, and E L signals. The quad flip-flop is enabled by the MS, IR EN L signal; when this signal is negated (MS, IR DISABLE L has been asserted by a peripheral or by the Programmer's Console) the flip-flop outputs are removed from the output lines and the DMA L signal is asserted.

The flip-flops are clocked by the CPMA LOAD signal, which is generated during automatic operation at TP4 time and during manual operation when the LA button is pushed. Some type of manual operation always precedes automatic operation; for example, to initiate automatic operation of a stored program, the operator must load the CPMA register with the starting address of the program. He loads this address by pushing the console LA button, causing the Programmer's Console logic to assert first, the MS, IR DISABLE L signal and, second, the PULSE LA H signal. MS, IR DISABLE L causes the DMA L signal to be asserted. This action results in ROM H being disabled; consequently, both the D SET L signal and the E SET L signal are negated, and IF SET L in the Major State register logic is asserted. Because of gating differences in the Programmer's Console logic, MR, IR DISABLE L is asserted much earlier than PULSE LA H. Thus, IF SET L is low when CPMA LOAD goes high, and the Fetch stage of the quad flip-flop is set, asserting the F L signal. If the operator now pushes the RUN button, the CPU begins automatic operation in the Fetch state of the addressed instruction.

Since all instructions begin in the Fetch state, this state is entered from any state that completes an instruction. Thus, Fetch can be entered from the Execute state of a 2- or 3-cycle instruction; Fetch can be entered from the Defer state of a 2-cycle instruction; Fetch can be entered from the Fetch state of a one-cycle instruction; finally, Fetch can be entered from the DMA state. When the Fetch state of a multi-cycle instruction has been completed, either a Defer state or an Execute state follows, unless the operator pushes the HLT/SS button or a data break device causes suspension of program control. Either event can cause a halt or interruption when the Fetch state is completed; then the DMA state is entered. When operations in this state have been carried out, control is returned to the program, and the multi-cycle instruction can be completed.

ROM H provides the outputs that control the Major State Register flip-flops; Table 4-8 relates these outputs to the input select codes. The table shows those circumstances in which either the D SET L signal or the E SET L signal is asserted. When neither of these signals is low, IF SET L is asserted. For example, ROM H is disabled during the Execute state; consequently, IF SET L is asserted during all Execute cycles.

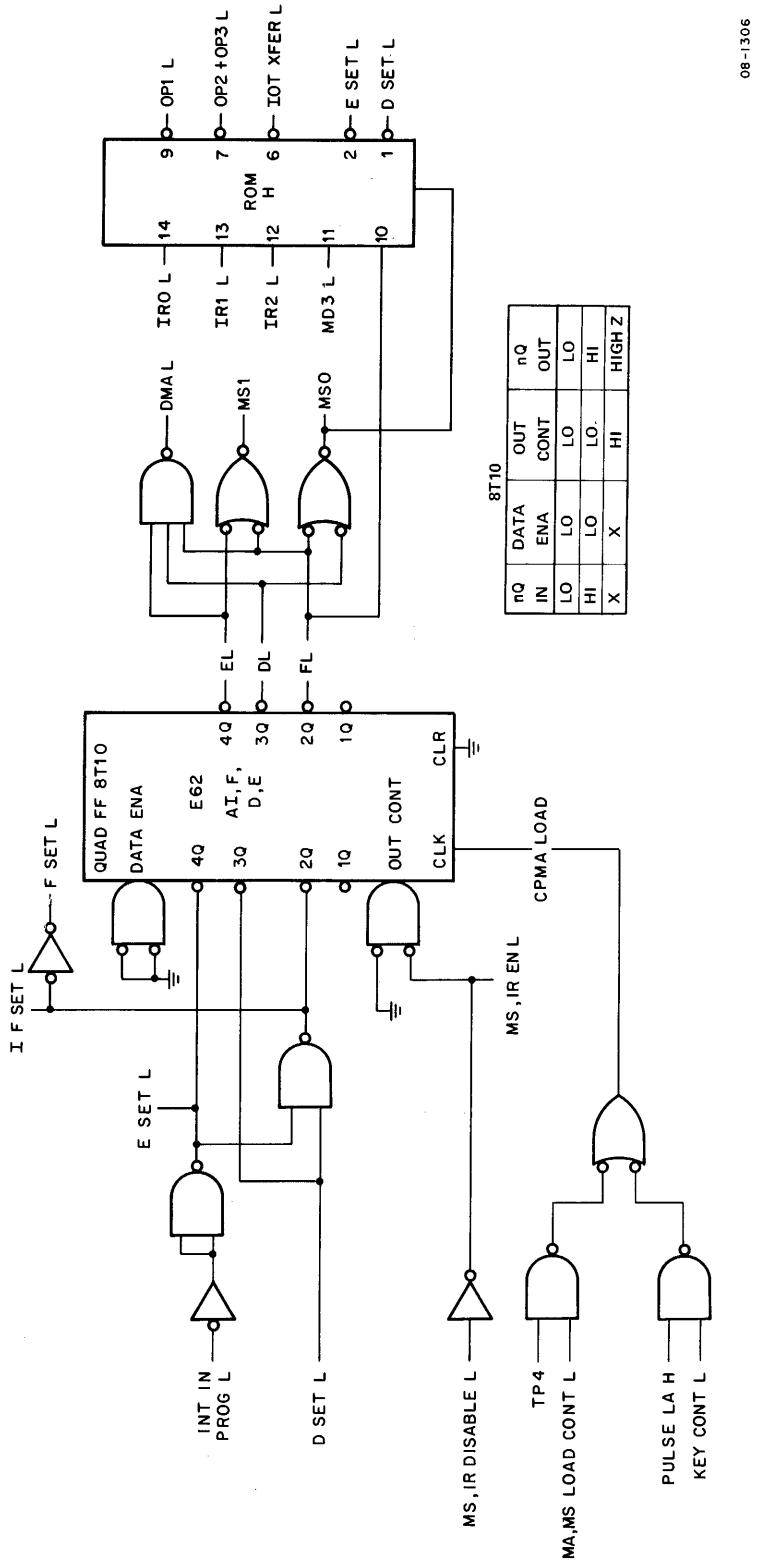


Figure 4-40 Major State Registers Logic

Table 4-8
ROM H Input/Output Signals

(ROM is enabled for Fetch or Defer Major State)

Input Code	Input Signal Low					ROM Output Signal	Basic Instruction Programmed	Present Major State/Next Major State
	IR0 L	IR1 L	IR2 L	MD3 L	F L			
0	X	X	X	X	X	OP2 + OP3 L	OPERATE	Fetch/Fetch (IF SET L is low)
2	X	X	X		X	OP1 L	OPERATE	Fetch/Fetch (IF SET L is low)
4	X	X		X	X	IOT XFER L	IOT	Fetch/Fetch (IF SET L is low)
6	X	X			X	IOT XFER L	IOT	Fetch/Fetch (IF SET L is low)
10	X		X	X	X	D SET L	JMP	Fetch/Defer
11	X		X	X			JMP	Defer/Fetch (IF SET L is low)
12	X		X		X		JMP	Fetch/Fetch (IF SET L is low)
13	X		X				JMP	Defer/Fetch (IF SET L is low)
14	X			X	X	D SET L	JMS	Fetch/Defer
15	X			X		E SET L	JMS	Defer/Execute
16	X				X	E SET L	JMS	Fetch/Execute
17	X					E SET L	JMS	Defer/Execute
20		X	X	X	X	D SET L	DCA	Fetch/Defer
21		X	X	X		E SET L	DCA	Defer/Execute
22		X	X		X	E SET L	DCA	Fetch/Execute
23		X	X			E SET L	DCA	Defer/Execute
24		X		X	X	D SET L	ISZ	Fetch/Defer
25		X		X		E SET L	ISZ	Defer/Execute
26		X			X	E SET L	ISZ	Fetch/Execute
27		X				E SET L	ISZ	Defer/Execute
30			X	X	X	D SET L	TAD	Fetch/Defer
31			X	X		E SET L	TAD	Defer/Execute
32			X		X	E SET L	TAD	Fetch/Execute
33			X			E SET L	TAD	Defer/Execute
34				X	X	D SET L	AND	Fetch/Execute
35				X		E SET L	AND	Defer/Execute
36					X	E SET L	AND	Fetch/Execute
37						E SET L	AND	Defer/Execute

Consider the table entry for input code 21(8), for example. This combination of input signals is obtained when the CPU is in the Defer state of an indirectly-addressed DCA instruction. DCA is normally a 2-cycle instruction, but indirect addressing means that the Defer state must be completed before the instruction is executed. Thus, the E SET L signal is asserted during the Defer cycle, and the E L signal is generated at TP4 time.

Note that the INT IN PROG H signal asserts E SET L. INT IN PROG H is asserted when an interrupt request is honored by the interrupt logic of the timing generator module. At TP4 time the Execute state is entered; E SET L can be asserted in this manner during either a Fetch, a Defer, or an Execute state, provided the particular state is the final state of an instruction.

As shown earlier, Fetch can be entered from the DMA state. If MS, IR DISABLE L is asserted because manual operations are being performed, Fetch always follows DMA. However, if MS, IR DISABLE L has been asserted by a data break peripheral, the Fetch state may or may not follow the DMA state. A data break operation can begin at the end of any Major State. Program control is halted for one timing cycle (control can be halted for three cycles, as well; for convenience, a halt of one cycle is considered). When the Data transfer has been completed, program control is reestablished and the previously interrupted operation continues. An example of the interrupting process is given in the following paragraph.

If operations are being carried out in the Fetch state of a 2-cycle DCA instruction, the E SET L signal is asserted. If a peripheral initiates a data break during this Fetch state, MS, IR DISABLE L is asserted at TP4 time. At the same time, CPMA LOAD is produced by TP4 and MA, MS LOAD CONT L, and Execute flip-flop is set; however, MS, IR DISABLE L removes the flip-flop outputs from the output lines and the DMA state is entered, instead of the Execute state. It could be assumed that the next TP4 pulse (of the DMA state) would set the Fetch flip-flop; however, at TP1 of the DMA state the peripheral asserts MA, MS LOAD CONT L, thereby preventing the TP4 pulse in question from setting the flip-flop. Instead, this TP4 negates MS, IR DISABLE L. The Execute flip-flop is still set and, thus, E L is asserted. Operations begin in the Execute state of the interrupted instruction. At TP1 of this state, MA, MS LOAD CONT L is negated, completing the return to uninterrupted operation.

4.4.3 DATA ENA/DATA CMP Logic

Figure 4-41 shows supplementary logic that generates the DATA ENA L and/or the DATA CMP L signals. These signals are used in major register gating to select the information on the DATA lines or the complement of that information for application to the adders; alternatively, a logic 0 may be gated to the adders. Table 4-9 relates the state of the two signals to the type of data gated to the adders.

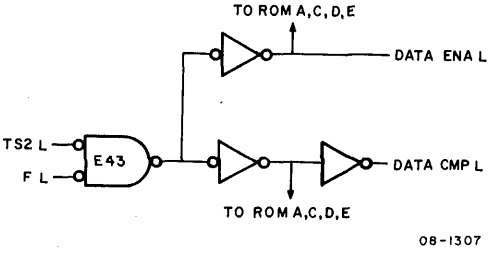


Figure 4-41 Data ENA/Data CMP Logic

As Figure 4-41 shows, ROMs A, C, D, and E can control the two signals, and do in all but one instance, i.e., during TS2 of a Fetch cycle. In this instance the two signals cause the AC contents to be gated to the adder and placed on the major register gating SUM lines (AC->BUS L is asserted by the logic shown in Figure 4-44). If an SZA instruction has been issued, the AC contents will be tested by the Skip logic (Paragraph 4.5.3).

Table 4-9
DATA ENA/DATA CMP Gating

Signal		Data Transferred to Adder
DATA ENA L	DATA CMP L	
HI	HI	HI (Logic 0)
HI	LO	HI (Logic 0)
LO	LO	Complement of information on DATA lines
LO	HI	Information on DATA lines

4.4.4 Address Update Logic

Figure 4-42 shows supplementary logic that generates PC LD EN L, CARRY EN L, and SEL B L. All three signals are used to implement the MA+1>PC operation that takes place during TS1 of each Fetch cyle and during TS1 of selected DMA cycles.

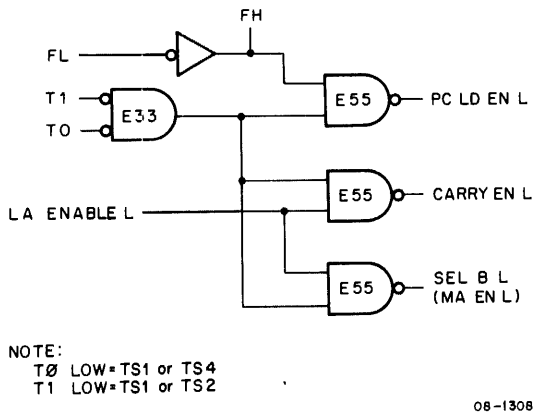


Figure 4-42 Address Update Logic

During TS1 the SEL B L and CARRY EN L signals are asserted, assuming LA ENABLE L is high. SEL B L causes decoder E71 (Figure 4-31) to assert the MA EN L signal, gating the CPMA address to one input of the adders (DATA CMP L and DATA ENA L provide a logic 0 at the other adder input). CARRY EN L enables the Carry In logic to add 1 to the address. If the CPU is in a Fetch cyle, PC LD EN L is asserted by NAND gate E55, enabling the PC, AC, MQ CLK signal to load the PC register at TP1 time. However, if the CPU is in the DMA cycle, PC LD EN L is asserted by ROM A (Figure 4-31); again, the PC register is loaded at TP1 time. This operation is carried out whenever the console E NEXT, D NEXT, E THIS, or D THIS button is pushed.

When the operator loads an address with either the LA pushbutton or the LXA pushbutton, the console logic asserts the LA ENABLE L signal to prevent spurious incrementing of the address. LA ENABLE L can also be asserted during the BOOT (or NON-STOP) DEPOSIT procedure. In this procedure PC LD EN L, CARRY EN L, and SEL B L are generated by ROM A, the PC register is incremented at TP1 time, data is written into memory, and the CPU continues to run (unlike the normal deposit function that halts after a single timing cycle).

4.4.5 Major Register Load Signal Logic

The logic that generates the major register load signals is shown in Figure 4-43. At the top is the logic that produces the clock signal for the PC, the AC, and the MQ registers. When a particular register's load enable signal (PC LD EN L, for example) is asserted, the PC, AC, MQ CLK signal causes data to be loaded into that register. Table 4-10 lists the timing pulses and shows the conditions under which a particular pulse causes PC, AC, MQ CLK to load a given register. Included is the reason each register is being loaded.

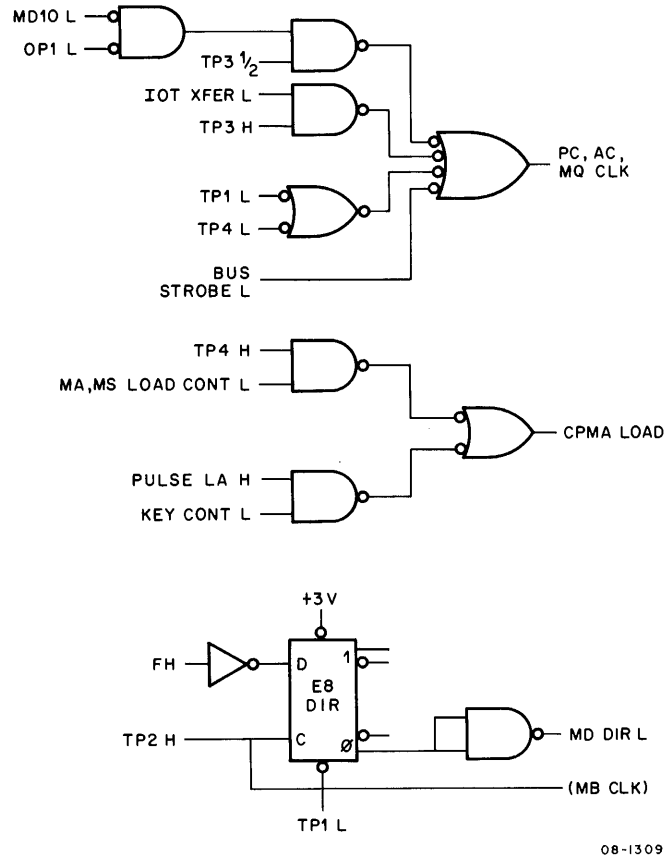


Figure 4-43 Major Register Load Signal Logic

Logic that procudes the CPMA LOAD signal appears in the middle of Figure 4-43. The CPMA register is loaded at each TP4 time, providing the MA, MS LOAD CONT L signal has not been asserted, and when the operator loads an address with the Programmer's Console LA pushbutton.

When the LA button on the console is pushed, the console logic causes the entry to be gated to the CPMA register. PULSE LA H is asserted and, since KEY CONT L is negated by the LA pushbutton, the CPMA LOAD signal loads the address into the register.

Each TP4 pulse generates a CPMA LOAD signal when MA, MS LOAD CONT L is high. MA,MS LOAD CONT L can be asserted by a data break peripheral to ensure that the CPU returns to the correct major state at the end of the data break (Paragraph 4.6.2). Or, MA,MS LOAD CONT L can be asserted by the console E THIS or D THIS pushbutton. When either of these pushbuttons is activated, the address selected for examining or depositing is incremented and loaded into the PC register at TP1 time; hence, MA,MS LOAD CONT L prevents the incremented address from being loaded into the CPMA register at TP4 time.

Table 4-10
PC, AC, MQ CLK Signal Loading

Timing Pulse	Necessary Condition	Register Loaded/Reason
TP1	Fetch cycle	PC/Updated address stored in PC
	DMA cycle	PC/Updated address stored in PC
TP3	DMA cycle	PC/An Auto-Start address provided by the Programmer's Console is loaded from the DATA lines; it is transferred into the CPMA at TP4 time
	Defer cycle	PC/During a JMP I instruction, the address to which program control is to be transferred is loaded into the PC
	Fetch cycle	PC/During a JMP instruction, the address to which program control is to be transferred is loaded into the PC
		AC or MQ/Operate instructions can cause either or both registers to be loaded
	Execute cycle	PC/During a JMS instruction, the address to which program control is to be transferred is loaded into the PC
		AC/During a DCA instruction, 0000 is loaded into the AC, clearing it.
		During a TAD instruction, the result of the addition of the AC contents and the contents of the addressed memory location is loaded into the AC
		During an AND instruction, the result of the logical-ANDing of the AC contents and the contents of the addressed memory location is loaded into the AC
BUS STROBE L	IOT transfer in progress	AC or PC/Information placed on the DATA lines by a peripheral is loaded into the AC or the PC
TP3 1/2	RTR or RTL microinstruction programmed	AC/The contents of the AC register are shifted left or right by one place
TP4	RAR, RAL, RTR, or RTL microinstruction programmed	AC/The contents of the AC register are shifted left or right by one place; if RTR or RTL, this is the second shift to occur during TS4

The logic that generates the MD DIR L signal is shown at the bottom of Figure 4-43. Each TP1 pulse clears the DIR flip-flop, asserting the MD DIR L signal during the read portion of the memory cycle; thus, data in the addressed memory location is placed on the MD lines. At TP2 time the DIR flip-flop is kept in the clear state if the instruction is in the Fetch state; hence, the data placed on the MD lines during the read half of the memory cycle is rewritten in the same location during the write half of the cycle. If the instruction is in other than the Fetch cycle, the DIR flip-flop is set at TP2 time and MD DIR L is negated. This action gates the contents of the MB register, which is loaded at each TP2 time, onto the MD lines; consequently, the MB register becomes the source of the data that is written into memory during the write operation.

4.4.6 AC Register Control Logic

The logic in Figure 4-44 controls the AC register during many of its possible manipulations. Shown at the top of Figure 4-44 is logic that generates the AC->BUS L signal. ROM D and ROM E are the primary producers of AC->BUS L. The logic shown is needed for isolated events. Note that the gating of the signals results in AC->BUS L being asserted during TS2 of a Fetch cycle, and during TS2 or TS3 of an Execute cycle.

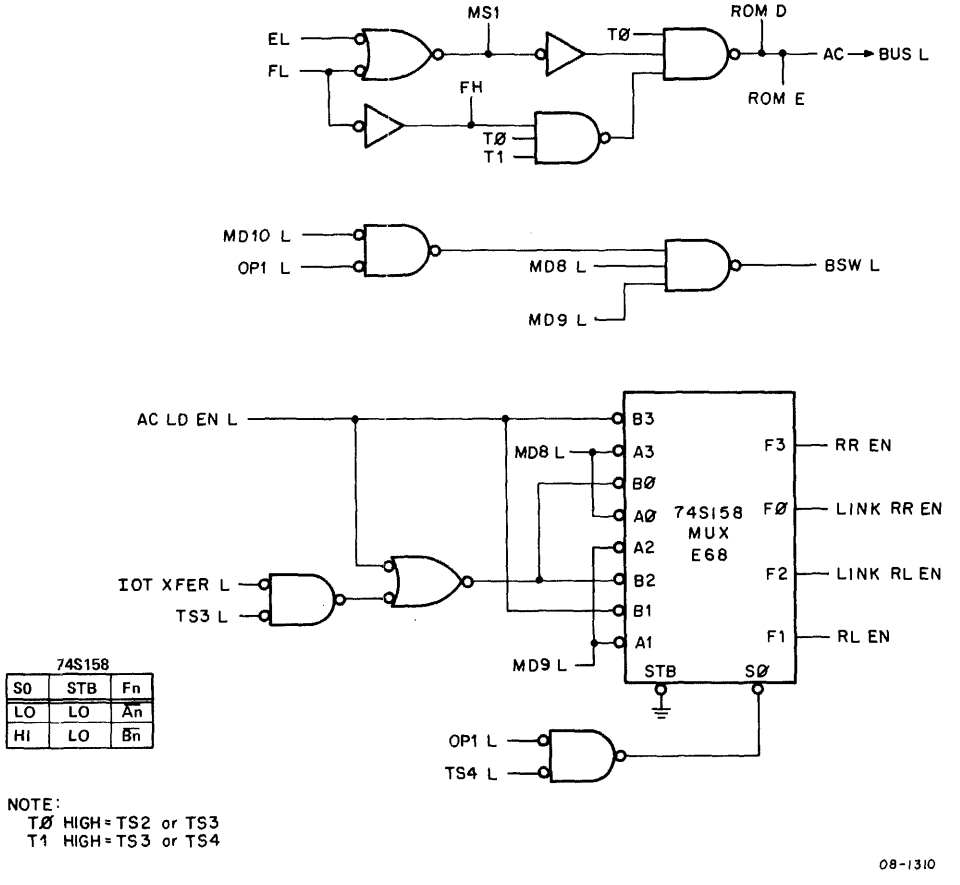


Figure 4-44 AC Register Control Logic

In the first instance, a Fetch cycle, the AC register contents are placed on the DATA lines during TS2, gated to the adders by the DATA CMP L and DATA ENA L signals (Figure 4-53), and placed on the SUM lines. The SUM lines are tested by the Skip logic (Paragraph 4.5.3) in carrying out the SZA microinstruction. If the AC contents were 0000, the ZERO L signal is loaded into the Z-flag flip-flop at TP2 time and the next program instruction is skipped.

In the second instance, an Execute cycle, two uses are made of the AC->BUS L signal. For one, the AC contents are placed on the DATA lines during TS2 of the DCA instruction, gated to and loaded into the MB register at TP2 time, and written in the addressed memory location. For another, the AC contents are placed on the DATA lines during TS3 of the TAD instruction, gated to the adders, where the add operation is accomplished, and loaded into the AC register at TP3 time.

Below the AC->BUS L logic is the byte-swap logic that generates the BSW L signal in response to the BSW microinstruction(7002). When the BSW instruction is issued, the AC contents are placed on the DATA lines during TS3, gated to the adders, and put on the SUM lines. The BSW L signal, which is asserted at TP2 time, causes the information on the SUM 0 line to be gated to the input of AC bit 6, and the information on the SUM 6 line to be gated to the input of AC bit 0. Likewise, AC bits 1 and 7, 2 and 8, 3 and 9, 4 and 10, and 5 and 11 are swapped. At TP3 time, the AC is loaded and the byte swap has been carried out.

At the bottom of Figure 4-44 is the logic that controls the loading and shifting of the AC register and the Link (the LNK RR EN and LNK RL EN signals are used to control the Link and are explained in Paragraph 4.5.4; they are shown here only for information). The AC register comprises DEC74S194 bidirectional shift registers that can be parallel loaded and shifted either left or right. The signals RR EN and RL EN, generated by multiplexer E68 in Figure 4-44, determine the mode of operation for the register, as outlined below.

RR EN	RL EN	AC Register Mode
HI	HI	Parallel-load
HI	LO	Right-shift
LO	HI	Left-shift
LO	LO	Do-nothing

The AC register can be loaded from the SUM lines at TP3 times, at BUS STROBE L time, at TP3 1/2 time (Paragraph 4.4.5), i.e., during TS3 and TS4. Most of the AC operations involve parallel loading in TS3. During, TS3 the state of the AC LD EN L signal determines the state of the RR EN and RL EN signals. If AC LD EN L has been asserted by ROM C, D, or E, RR EN and RL EN place the AC register in the parallel load mode and the register is loaded at TP3 time or at BUS STROBE L time.

During TS4 of a Group 1 operate microinstruction, the state of MD bits 8 and 9 determine the state of RR EN and RL EN, respectively. This device permits the rotate instructions (RAR, RAL, RTR, and RTL) to shift the AC register right or left. For example, the RAR (7010) instruction – rotate AC and Link right one – asserts the MD8 L signal, while negating the MD9 L signal. As a result, RR EN is high and RL EN is low, producing a right shift of the AC register at TP4 time (AC11 is shifted into the Link register). If RTR (7012) – rotate AC and Link right two – is programmed, the AC is clocked at TP3 1/2 time as well as at TP4 time (AC10 is shifted into the Link register).

4.5 MAJOR REGISTER GATING

The major registers of the PDP-8/A perform all the operations needed to implement program instructions. For example, the PC register keeps track of the program steps, the CPMA register selects the memory location provided by the PC, and the AC register uses the data in the selected memory location to carry out arithmetic operations. Information of one type or another (data, addresses, etc.) must be exchanged by the major registers or transferred between a register and some source or destination, such as a peripheral or core memory. The major register gating network, illustrated in block diagram form in Figure 4-45, enables this exchange and transfer of information. The block diagram shows the gating for bit 0 of the 12-bit data word; all other bits are gated similarly and differences that exist are noted in subsequent discussions.

74S194

CLR	S0	S1	MODE	DS3	DS0	CLK	$R_n(1)$
LO	–	–	–	–	–	–	LO
HI	HI	HI	PAR LD	–	–	↑	Dn
HI	HI	LO	RT SHIFT	HI	–	↑	HI
HI	HI	LO	RT SHIFT	LO	–	↑	LO
HI	LO	HI	LT SHIFT	–	HI	↑	AC1
HI	LO	HI	LT SHIFT	–	LO	↑	AC1
HI	LO	LO	–	–	–	–	NO
HI	–	–	–	–	--	LO	CHANGE

8T10

OUT CONT	DATA ENA	CLK	nQ OUT
LO	LO	↑	nQ IN
LO	HI	↑	NO CHANGE
HI	–	–	HI-Z

8097

DIS 2,4	OUTPUT
LO	INPUT
HI	HI-Z

74S158

S0	STB	Fn
LO	LO	$\overline{An}$
HI	LO	$\overline{Bn}$
–	HI	HI

8234

S0	S1	Fn
LO	LO	Bn
HI	LO	$\overline{An}$
LO	HI	$\overline{Bn}$
HI	HI	HI

8235

S0	S1	Fn
LO	LO	$\overline{An}\,\overline{Bn}$
HI	LO	$\overline{An}$
LO	HI	Bn
HI	HI	HI

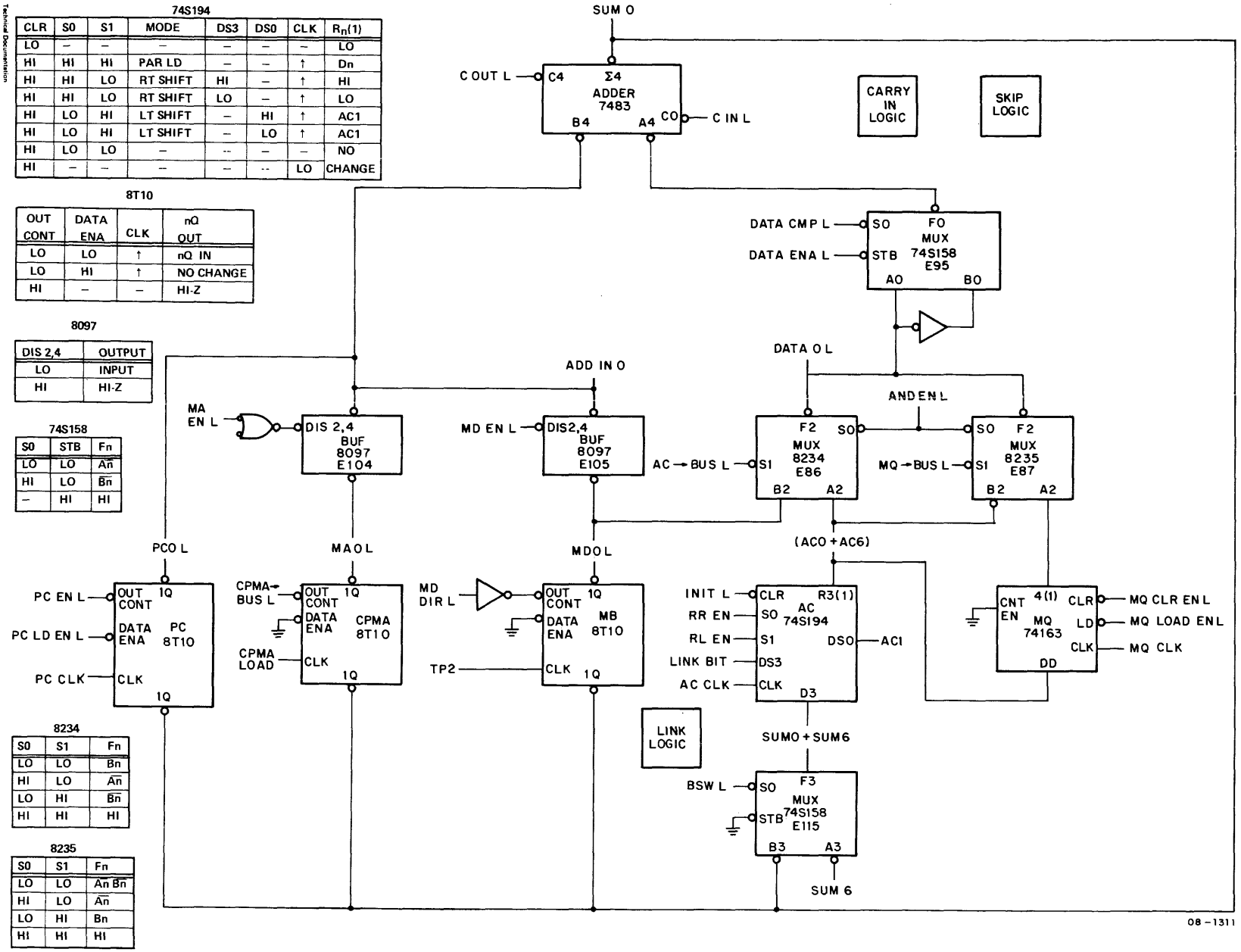


Figure 4-45 Block Diagram, Major Register and Gating (BIT0)

Central to the major register gating is the DEC7483 full adder. When information is transferred from or to a major register, it passes through the adder, where it may or may not be modified, and is placed on the SUM line. Each register, except the MQ, is loaded from the SUM line. The register that is to receive the data is determined by various control signals; these are generated in response to the instruction identity, the CPU major state, the timing generator time state, or to some combination of these factors.

For example, the program count in the PC register is transferred to the CPMA register at the end of one instruction to indicate the memory location of the next instruction of the program. Hence, during TS4, the PC EN L signal gates the PC0 bit to the adder via the ADD IN 0 line. During the same time state, the DATA CMP L and DATA ENA L signals disable the DEC74S158 data selector (E95), causing a logic 0 to be applied to the other input of the adder (pin A4). The result, PC0, is placed on the SUM 0 line and loaded into the CPMA register by the CMPA LOAD signal, which is generated by each TP4 pulse. Some circumstances require that a program instruction be skipped; this can be done if the program count in the PC register is incremented by the adder before being placed on the SUM line. The CPU Carry In logic generates the C IN L signal during TS4, causing the adder to increment the program count. The result, PC+1 (the logic 1 is added directly to bit 11 of the PC), is loaded into the CPMA register.

At times, information must be transferred between a major register and some source external to the CPU. A peripheral, for instance, can transfer data to the AC register during a programmed I/O dialogue. The peripheral places the data on the DATA bus. During TS3 it is gated through the data selector to the adder and placed on the SUM line. The byte-swap multiplexer (E115) gates the data to the AC register and the register is loaded by the PC, AC, MQ, CLK signal at TP3 time. The data transfer can be made in the opposite direction, as well. In this case, the AC->BUS L signal places the AC contents on the DATA bus during TS3. The peripheral is responsible for clocking the data from the DATA bus into a peripheral buffer register. The original data may be returned to the AC register and reloaded at TP3 time; alternatively, the data selector can be disabled so that logic zeroes are placed on the SUM lines and clocked into the AC.

The foregoing examples are presented merely to familiarize you with the block diagram in Figure 4-45. To become familiar with the operation of the major registers and gating, one should become adept at following the gating of PDP-8/A instructions through the logic represented in the block diagram.

Most of the major register enable signals and the various multiplexer control signals were introduced in the ID discussion, Paragraph 4.4. There, it was pointed out that a number of ROMs play an important part in decoding instructions and generating major register gating control signals. The logic for each ROM was illustrated and mention was made of tables relating the ROM input and output signals. Two of these tables (4-11 and 4-12) appear in this paragraph. Other tables appear in the Skip logic, in the Major State Register logic, and in Paragraph 4.6, I/O Transfer Logic. Each table relates the input and output signals of a particular ROM and gives a brief resume of the result achieved by each output condition. For example, Table 4-11 provides information about ROM D, which generates major register gating signals when operate microinstructions are programmed. The INPUT CODE column lists the codes represented by the input signals in octal form. The INPUT SIGNAL LOW column indicates the signals that must be low to achieve the desired input code (this convention is chosen because most of the PDP-8/A Omnibus signals are active when low). The ROM OUTPUT SIGNAL column shows the signals that are generated for each input code (consider the inverter at output pin 2 as part of the ROM), while the INSTRUCTION OCTAL CODE column indicates the group of operate instructions that relate to each input code. Finally, the RESULT column summarizes the events that take place in the major register gating logic in response to the signals generated by the ROM.

Each of the 256-bit ROMs has a similar explanatory table asociated with it. At the top of each table is a notation as to when the ROM is enabled. ROM D is enabled when pin 15, is low, i.e., during TS3 of an operate instruction. Some of the ROM tables include a column headed DCDR OUTPUT SIGNAL. These ROMs generate three signals – SEL A L, SEL B L, and SEL C L – that are applied to a BCD-to-decimal decoder, E71. The decoder then asserts the signal indicated in the DCDR OUTPUT SIGNAL column.

To use the ROM tables with the block diagram in Figure 4-45 first consider what variables are represented by examining the instruction. Then find the ROM that is enabled for the set of variables exhibited. For instance, operate instructions are executed, for the most part, during TS3. ROM D is enabled during TS3, so refer to Table 4-11. For a specific example, think about the CMA (7040) instruction – complement the AC. Table 4-11 shows four entires in the INPUT CODE column that apply to the octal code 70XX. Two of them, 34 and 36, generate the CARRY EN L signal, which is not needed to complement the AC; consequently, those entries can be ignored. Both of the remaining entires generate AC->BUS L and AC LD EN L. However, entry 35 generates DATA CMP L as well as DATA ENA L, a combination that results in the complement of the information on the DATA lines being gated to the SUM lines. Thus, the events take place as follows: AC->BUS L gates the content of AC0 to the DATA 0 line (Figure 4-45); multiplexer E95 gates the complement of the AC0 bit to the adder, which places the information on the SUM 0 line; multiplexer E115 passes the information on the SUM 0 line to the AC0-bit input, from where it is loaded at TP3 time.

As another example, consider the basic AND instruction that directs a logical ANDing of the AC contents and the contents of the addressed memory location. This is an interesting example, since the major register gating operates intricately while executing the AND instruction. First of all, locate the ROM table that applies to basic instructions – Table 4-12. The entry for input codes 34 and 35 apply in this example. Input code 34 produces the MD EN L signal that gates the operand of the AND instruction through buffer E105 and the adder to the MB register during TS2. At TP2 time, the MB register is loaded and becomes the source of data for the MD lines (this ensures that the operand is re-written during the write operation). During TS3, input code 35 produces the AND EN L signal. As can be seen from the function tables in Figure 4-45, AND EN L causes multiplexer E86 to gate the complement of the data on the MD0 line to the DATA0 line; at the same time, multiplexer E87 places the content of the AC0 bit on the DATA0 line. If both MD0 L and the AC0 bit are logic 1 (MD0 L is low and AC0 is high), DATA0 L is high, which is not logic 1 but which is quickly converted to logic 1 by multiplexer E95. Thus, the SUM 0 line goes low, multiplexer E115 places a high at the input of the AC0 bit, and a logic 1 is loaded into the AC at TP3 time. If either MD0 L or AC0 is logic 0, a logic 0 is loaded into AC0 at TP3 time.

Most of the gating control signals are generated by the various ROMS. Those few that are not are produced by either the supplementary logic discussed in Paragraphs 4.4.3 through 4.4.6, or by the Carry In logic, the Skip logic, and the Link logic. The last three groups of logic are discussed in detail in Paragraphs 4.5.2 through 4.5.4. Section 4.5.1 discusses Page logic, which modifies the block diagram of Figure 4-45 in certain circumstances.

4.5.1 Page Logic

The operand of a memory reference instruction (MRI) or the effective address of an indirectly-addressed JMP instruction can be stored in the current page or in page 0. The logic shown in Figure 4-46, which is only partially illustrated in the block diagram of major register gating, satisfies either eventuality.

At TP4 of the Fetch cycle, the address of the MRI operand, for example, must be loaded into the CPMA register. If the operand is on the same page as the MRI, only the relative address bits (5 through 11) of the CPMA register need be changed; hence, MA bits 0-4 are loaded into CPMA0-4, respectively, to specify the current page, while MD bits 5-11 are loaded into CPMA5-11, respectively, to specify the relative address. However, if the operand is located on page 0, both the relative address bits and the page bits must be changed; thus, zeroes are loaded into CPMA0-4, while MD bits 5-11 are, again, loaded into CPMA5-11.

The MD4-bit is used to indicate current page or page 0. When MD4 L is asserted, the MRI operand or the JMP I effective address is on the current page. The PAGE EN L signal is asserted by ROM B for an MRI (Table 4-13) or by ROM C for the JMP I instruction (Table 4-12). As Figure 4-46 shows, MA bits 0-4 are placed on ADD IN lines 5-11 (MD bit 5 is gated by an 8093 tri-state quad buffer). When the MD4-bit indicates page 0, zeroes are placed on the ADD IN 0-4 lines, while the MD lines are again gated to ADD IN lines 5-11.

Note (Table 4-12) that the PC, rather than the CPMA, is loaded for the JMP I instruction. Also, this operation takes place during TS3 rather than during TS4.

Table 4-11
ROM D Input/Output Signals

(ROM Enabled for OPR·TSE)

Input Code	Input Signal Low						ROM Output Signal	Instruction Octal Code	Result
	MD3 L	MD4 L	MD5 L	MD6 L	MD7 L	MD11 L			
0	X	X	X		X	X	DATA ENA L, AC LD EN L, MQ → BUS L, MQ CLR EN L	77XX	MQ → AC, Clear MQ
1	X	X	X		X		DATA ENA L, AC LD EN L		DATA → AC
2	X	X	X			X	DATA ENA L, AC LD EN L, MQ → BUS L		MQ → AC
3	X	X	X				DATA ENA L, AC LD EN L		DATA → AC
4	X	X			X	X	DATA CMP L, AC LD EN L, MQ CLR EN L	76XX	Clear AC, Clear MQ
5	X	X			X		DATA ENA L, AC LD EN L		DATA → AC
6	X	X				X	DATA CMP L, AC LD EN L		Clear AC
7	X	X					DATA ENA L, AC LD EN L		DATA → AC
10	X		X		X	X	DATA ENA L, AC LD EN L, MQ → BUS L, MQ LD EN L	75XX	Swap AC and MQ
11	X		X		X		DATA ENA L, AC → BUS L, AC LD EN L		AC → AC
12	X		X			X	DATA ENA L, AC → BUS L, AC LD EN L, MQ → BUS L		Inclusive OR, AC and MQ
13	X		X				DATA ENA L, AC → BUS L, AC LD EN L		AC → AC
14	X				X	X	DATA CMP L, AC LD EN L, MQ LD EN L	74XX	AC → MQ, 0 → AC
15	X				X		DATA ENA L, AC → BUS L, AC LD EN L		AC → AC
16	X					X	DATA ENA L, AC → BUS L, AC LD EN L		AC → AC
17	X						DATA ENA L, AC → BUS L, AC LD EN L		AC → AC
20		X	X	X		X	DATA ENA L, DATA CMP L, AC LD EN L, CARRY EN L	73XX	DATA+1 → AC
21		X	X	X			DATA ENA L, DATA CMP L, AC LD EN L		DATA → AC
22		X	X			X	DATA ENA L, AC LD EN L, CARRY EN L		DATA+1 → AC
23		X	X				DATA ENA L, AC LD EN L		DATA → AC
24		X		X		X	DATA ENA L, DATA CMP L, AC LD EN L, CARRY EN L	72XX	DATA+1 → AC
25		X		X			DATA ENA L, DATA CMP L, AC LD EN L		DATA → AC
26		X				X	DATA ENA L, AC LD EN L, CARRY EN L		DATA+1 → AC
27		X					DATA ENA L, AC LD EN L		DATA → AC
30			X	X		X	DATA ENA L, DATA CMP L, AC → BUS L, AC LD EN L, CARRY EN L	71XX	Complement and increment the AC
31			X	X			DATA ENA L, DATA CMP L, AC → BUS L, AC LD EN L		Complement the AC
32			X			X	DATA ENA L, AC → BUS L, AC LD EN L, CARRY EN L		Increment the AC
33			X				DATA ENA L, AC → BUS L, AC LD EN L		AC → AC
34				X		X	DATA ENA L, DATA CMP L, AC → BUS L, AC LD EN L, CARRY EN L	70XX	Complement and increment the AC
35				X			DATA ENA L, DATA CMP L, AC → BUS L, AC LD EN L		Complement the AC
36						X	DATA ENA L, AC → BUS L, AC LD EN L, CARRY EN L		Increment the AC
37							DATA ENA L, AC → BUS L, AC LD EN L		AC → AC

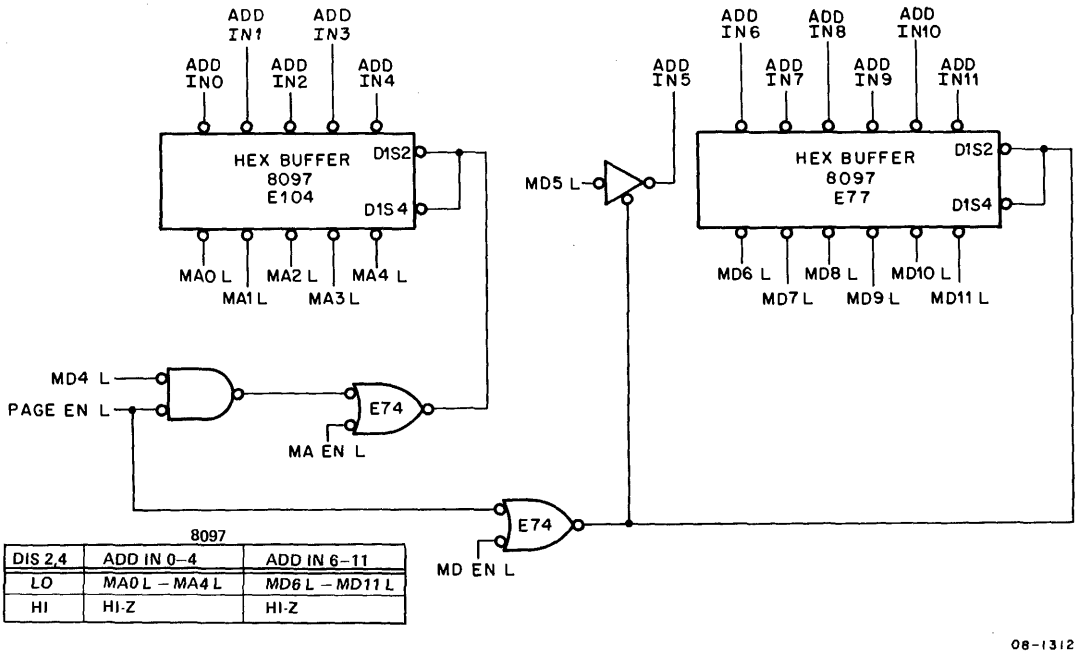


Figure 4-46 Page Logic

4.5.2 Carry In Logic

The Carry In logic is shown in Figure 4-47. The C IN L signal enables the processor to increment data. This signal is applied to the carry input of adder bit 11. There, it is added to two other inputs – the addend and the augend; any carry from the addition is applied to adder bit 10, and so on, until a carry from adder bit 0 (C OUT L) is applied to the Link logic.

Data must be incremented for a variety of operations. This variety involves all the CPU Time States as well as the CPU Major States. The digital multiplexer, DEC74151, has the versatility to cope with the many enabling signals that are encountered. The 74151 data select inputs at S0, S1, and S2 determine which of the 8 input lines is routed to the output. The table in Figure 4-47 shows the inputs and outputs and lists the involved time states as well.

Consider the major event that occurs during TS1 of a Fetch or DMA timing cycle, i.e., the address on the MA lines is incremented and loaded into the PC register at TP1 time. Because the address must be incremented, the Carry In logic must assert the C IN L signal during TS1. The 74151 table shows that during TS1, the input at either D0 or D4 is gated to the output and causes the C IN L signal to go low. Thus, the address can be incremented during the Fetch state as well as during a DMA cycle, when either the E NEXT or the D NEXT button on the Programmer's Console might be pushed.

The Defer and Execute states do not require an incrementing process during TS1; however, since the adders are not used at this time, it is unnecessary to prevent C IN L from being asserted. Note that CARRY EN L is asserted during TS1, provided the LA ENABLE L line has not been grounded by the Programmer's Console. When either the LA or LXA pushbutton is activated, the address to be loaded is placed on the DATA lines and gated through the adders to the CPMA register. Hence, the console also grounds the LA ENABLE L line so that C IN L does not increment the selected address.

Table 4-12
ROM C Input/Output Signals

(ROM Enabled during TS3 of Fetch if JMP, or during TS2 or TS3 of Defer or Execute)

Input Code	Input Signal Low					ROM Output Signal	Basic Instruction	DCDR Output	Result
	IR0 L	IR1 L	IR2 L	F L + E L	T1				
11	X		X	X		DATA CMP L, PC LD EN L, SEL A L	JMP	PAGE EN L	If MD4 L is logic 1 (operand is on current page), MA0–4 is loaded into PC0–4, MD5–11 is loaded into PC5–11. If MD4 L is logic 0 (operand is loaded into PC0–4, MD5–11 is loaded into PC5–11.
12	X		X		X	DATA CMP L, CARRY EN L, SEL C L, SEL B L		MD EN L	MD + 1 → MB; (contents of indirectly-addressed auto-index register are incremented and used as effective address)
13	X		X			DATA CMP L, PC LD EN L, SEL C L, SEL B L		MD EN L	MD → PC (PC is loaded with the address to which program control will be transferred)
14	X			X	X	DATA CMP L, CARRY EN L, SEL C L	JMS	PC EN L	PC → MB; PC + 1 → MB if Skip flip-flop is active (program count to which control will return after forced-JMS is completed, is stored in locatio
15	X			X		DATA CMP L, PC LD EN L, CARRY EN L, SEL B L		MA EN L	MA + 1 → PC (program control is transferred to the location of the first subroutine instruction)
16	X				X	DATA CMP L, CARRY EN L, SEL C L, SEL B L		MD EN L	MD + 1 → MB (contents of indirectly-addressed auto-index register are incremented and used as effective address)
17	X					DATA CMP L			No operation
20		X	X	X	X	DATA ENA L	DCA		AC → MB (AC register placed on data bus by AC register control logic, data bus gated to MB register)
21		X	X	X		DATA CMP L, AC LD EN L			0 → AC
22		X	X		X	DATA CMP L, CARRY EN L, SEL C L, SEL B L		MD EN L	MD + 1 → MB (contents of indirectly-addressed auto-index register are incremented and used as effective address)
23		X	X			DATA CMP L			No operation
24		X		X	X	DATA CMP L, CARRY EN L, SEL C L, SEL B L	ISZ	MD EN L	MD + 1 → MB (data in specified location is incremented to test for 7777_8 count)
25		X		X		DATA CMP L, SEL B L, SEL A L		ISZ SKP TST L	1 → skip (if incremented data was 7777_8, C OUT L is asserted, Overflow flip-flop is cleared at TP2, and Skip flip-flop goes active at TP3)
26		X			X	DATA CMP L, CARRY EN L, SEL C L, SEL B L		MD EN L	MD + 1 → MB (contents of indirectly-addressed auto-index register are incremented and used as effective address)
27		X				DATA CMP L			No operation
30			X	X	X	DATA CMP L, SEL C L, SEL B L	TAD	MD EN L	MD → MB
31			X	X		DATA ENA L, AC LD EN L, SEL C L, SEL B L		MD EN L	MD → ADDER, AC → ADDER (AC → BUS L generated by AC register control logic); binary addition result to AC
32			X		X	DATA CMP L, CARRY EN L, SEL C L, SEL B L		MD EN L	MD + 1 → MB (contents of indirectly-addressed auto-index register are incremented and used as effective address)
33			X			DATA CMP L			No operation
34				X	X	DATA CMP L, SEL C L, SEL B L	AND	MD EN L	MD → MB
35				X		DATA CMP L, DATA ENA L, AC LD EN L, SEL A L, SEL C L		AND EN L	MD → DATA BUS, AC → DATA BUS; Logical-AND result to AC
36					X	DATA CMP L, CARRY EN L, SEL C L, SEL B L		MD EN L	MD + 1 → MB (contents of indirectly-addressed auto-index register are incremented and used as effective address)
37						DATA CMP L			No operation

Note: T1 Low = TS1 + TS2
T1 High = TS3 + TS4

Table 4-13
ROM B Input/Output Signals

(ROM Enabled During TS4)

Input Code	Input Signal Low					ROM Output Signal	DCDR Output Signal	Result
	GND	INT	IF SET L	MS0	MS1			
0	X	X	X	X	X	CARRY EN L, SEL C L	PC EN L	PC → CPMA; PC + 1 → CPMA if Skip flip-flop is active
1	X	X	X	X		CARRY EN L, SEL C L	PC EN L	PC → CPMA (indirectly-addressed JMP inst).
2	X	X	X		X	CARRY EN L, SEL C L	PC EN L	PC → CPMA; PC + 1 → CPMA if Skip flip-flop is active
3	X	X	X					
4	X	X		X	X	SEL A L	PAGE EN L	*
5	X	X		X		SEL C L, SEL B L	MD EN L	MD → CPMA (address of the operand of an indirectly-addressed MRI instruction)
6	X	X			X			
7	X	X						
14	X			X	X			
15	X			X				
16	X				X			
17	X							

Note: MS0 Low = FL + DL
MS1 Low = FL + EL

*If MD4 L is logic 1 (operand is on current page), MA0–4 is loaded into CPMA0–4, MD5–11 is loaded into CPMA5–11.
If MD4L is logic 0 (operand is on page 0), logic 0 is loaded into CPMA0–4, MD5–11 is loaded into CPMA 5–11.

74151

S2	S1	S0	(TIME STATE)	STB	F0
L	L	L	(TS1)	L	$\overline{D0}$
L	L	H	(TS4)	L	$\overline{D1}$
L	H	L	(TS2)	L	$\overline{D2}$
L	H	H	(TS3)	L	$\overline{D3}$
H	L	L	(TS1)	L	$\overline{D4}$
H	L	H	(TS4)	L	$\overline{D5}$
H	H	L	(TS2)	L	$\overline{D6}$
H	H	H	(TS3)	L	$\overline{D7}$

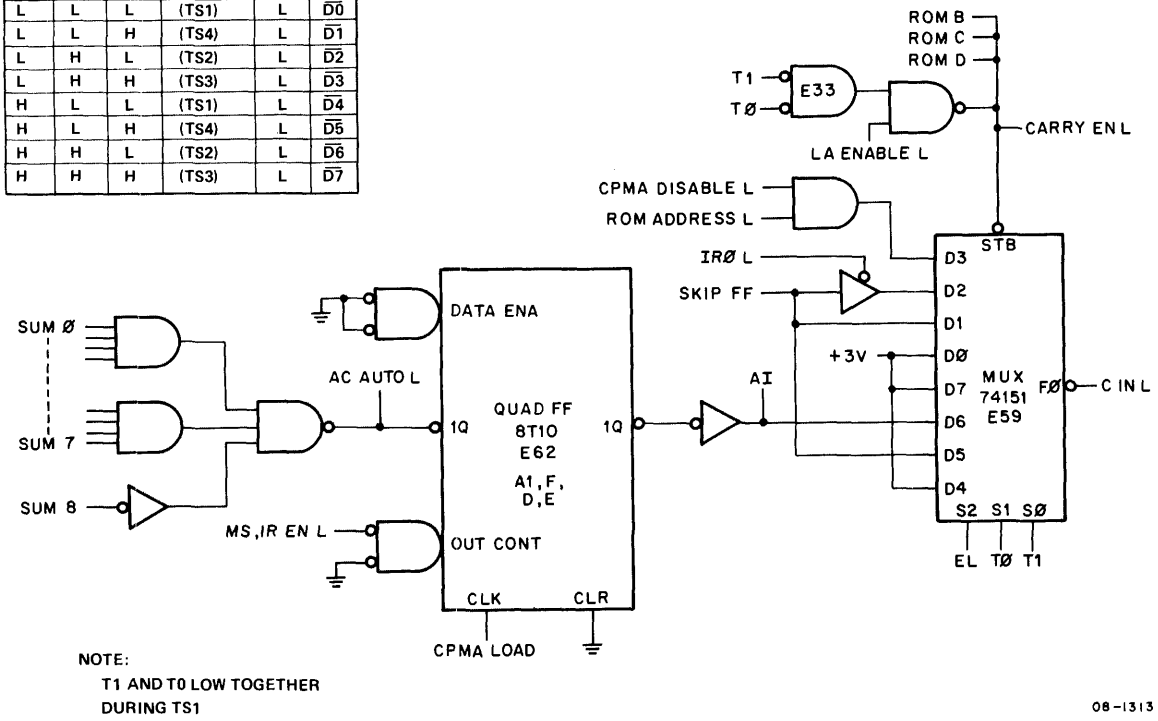


Figure 4-47 Carry In Logic

During TS2, no Fetch operations require data to be incremented. In the Defer state, however, an auto-index register (memory locations 0010 through 0017) might have been referenced by the instruction being performed (refer to *Introduction to Programming,* 1972, for a discussion of auto-indexing). In this case, the content of the register is incremented before being used as the instruction operand; thus, the information on the MD lines (the auto-index register contents) must be incremented during TS2 before being loaded into the MB register at TP2 time. The 74151 table shows that during TS2 of all but the Execute state, a high input at D6 causes the C IN L signal to go low. The signal at D6, AI, is high when the data on SUM lines 0 through 8 indicates that an auto-index register has been referenced. The CARRY EN L signal is asserted by ROM C during this operation; refer to Table 4-12 for verification.

In the Execute state, two situations require that the C IN L signal be asserted during TS2. First, an ISZ instruction can direct the CPU to increment the data in the specified location and then skip the next instruction if the result of the incrementation is 0000. Second, the CPU interrupt system might have honored an interrupt request during an instruction wherein the SKIP FF signal had been asserted; consequently, rather than storing the program count in memory location 0000, the CPU must store the incremented program count during TS2 of the forced JMS instruction.

In both these situations, a high input at D2 of the multiplexer causes the C IN L signal to be asserted (CARRY EN L is asserted by ROM C). For the ISZ instruction, the IR0 L signal is high and, therefore, D2 is high. For the forced JMS instruction IR0 L is low and, because the SKIP FF signal is high, pin 2 is high.

TS3 operations in the Fetch state that require the C IN L signal to be asserted, involve the IAC operate microinstruction. If IAC has been programmed, the contents of the AC register are placed on the DATA lines during TS3 and gated to the adder. A 0 is gated to the ADD IN line of the adder, while the input at pin 12 of the multiplexer causes the C IN L signal to go low (the CARRY EN L signal is asserted by ROM D). The result, AC+1, is placed on the SUM lines and loaded into the AC at TP3 time. Similar operations take place when the IAC command is microprogrammed with other Group 1 microinstructions.

A JMS instruction requires that the address on the MA lines be incremented during TS3 of the Execute state. When a JMS instruction is programmed, the operand of the instruction specifies the first memory location of the subroutine. In this location (Y, for example) must be stored the program count, to which the program will return upon completion of the subroutine. The first instruction of the subroutine is contained in location Y+1 and, in order to transfer control to location Y+1, the address on the MA lines (location Y) must be incremented during TS3. A high input at D3 of the multiplexer asserts the C IN L signal (ROM C asserts the CARRY EN L signal). D3 is high providing both CPMA DISABLE L and ROM ADDRESS L are negated.

During TS4 of both the Fetch and the Execute cycles, the program count in the PC register is transferred to the CPMA register. However, certain situations require a skip of one program instruction; hence, the program count in the PC register must be incremented before being transferred to the CPMA. One of these situations arises when a Group 2 operate microinstruction, such as SKP, is programmed; another results from an IOT instruction causing a peripheral to assert the Omnibus SKIP L signal; finally, an ISZ instruction might have been programmed. In each situation the SKIP flip-flop is set at TP3 time, asserting the SKIP FF signal. This signal at D1 or D5 causes the 74151 multiplexer to assert the C IN L signal during TS4 of both the Fetch and Execute cycles (the CARRY EN L signal is asserted by ROM B).

4.5.3 Skip Logic

The Skip logic, shown in Figure 4-48, samples the contents of the AC register and/or the Link, and the state of the Omnibus SKIP line. If the sampled data meets specified conditions, the program count is incremented before being transferred to the CPMA register at TP4 time; consequently, the next program instruction is skipped (Table 4-13).

The Skip operation is used primarily during the implementation of operate microinstructions. The majority of the Group 2 operate microinstructions, and nearly half of the combined microinstructions involve the Skip operation. ROM F decodes the Skip microinstructions and asserts the ISKIP L signal during TS3. The Skip flip-flop is cleared at TP3 time, and the SKIP FF signal causes the Carry In logic to increment the program count. Two examples are offered to demonstrate how the logic responds to skip instructions.

Consider the Group 2 operate microinstruction SMA (7500) – skip on a minus AC. Remember that minus numbers in the PDP-8/A are those between 4000(8) and 7777(8), i.e., bit 0 is logic 1. Thus, during TS3 of the SMA instruction, ROM F will assert the ISKIP L signal if AC0 is logic 1 (a high voltage level). When SMA is placed on the MD lines and the IR register decodes MD bits 0, 1, and 2, the inputs to ROM F are as follows.

ROM F Input Pin	**15**	**1**	**2**	**3**	**4**	**7**	**6**	**5**
Voltage Level	LO	AC0	HI	LO	HI	HI	HI	HI/LO
Input Octal Code		1 (If AC0 is logic 1)		5			6/7	

The ROM F pattern specification in Appendix J shows that the binary data contained in octal location 156(8) is 1000. Thus, the ROM outputs are as follows.

ROM F Output Pin	**9**	**10**	**11**	**12**
Voltage Level	HI	LO	LO	LO
Output Signal Asserted	ISKIP L			

Location 157(8) causes both the ADLK L and the ISKIP L signals to be asserted. If the AC is positive, i.e., AC0 is logic 0, the ISKIP L signal remains high for any of the four possible inputs – 056(8), 057(8), 016(8), and 017(8) (inputs 016(8) and 017(8) result if input pin 2 is low, in which case the AC is zero).

The SZA (7440) microinstruction – skip on a zero AC – tests the AC for a zero condition. During TS2 the AC->BUS L signal is asserted (Figure 4-44) and the contents of the AC register are placed on the SUM lines. If all AC bits are zero (low voltage levels), the ZERO L signal is asserted and clocked into the flip-flop at TP2 time. The ROM input code is 026(8) or 027(8), and ISKIP L is asserted by itself or together with ADLK L.

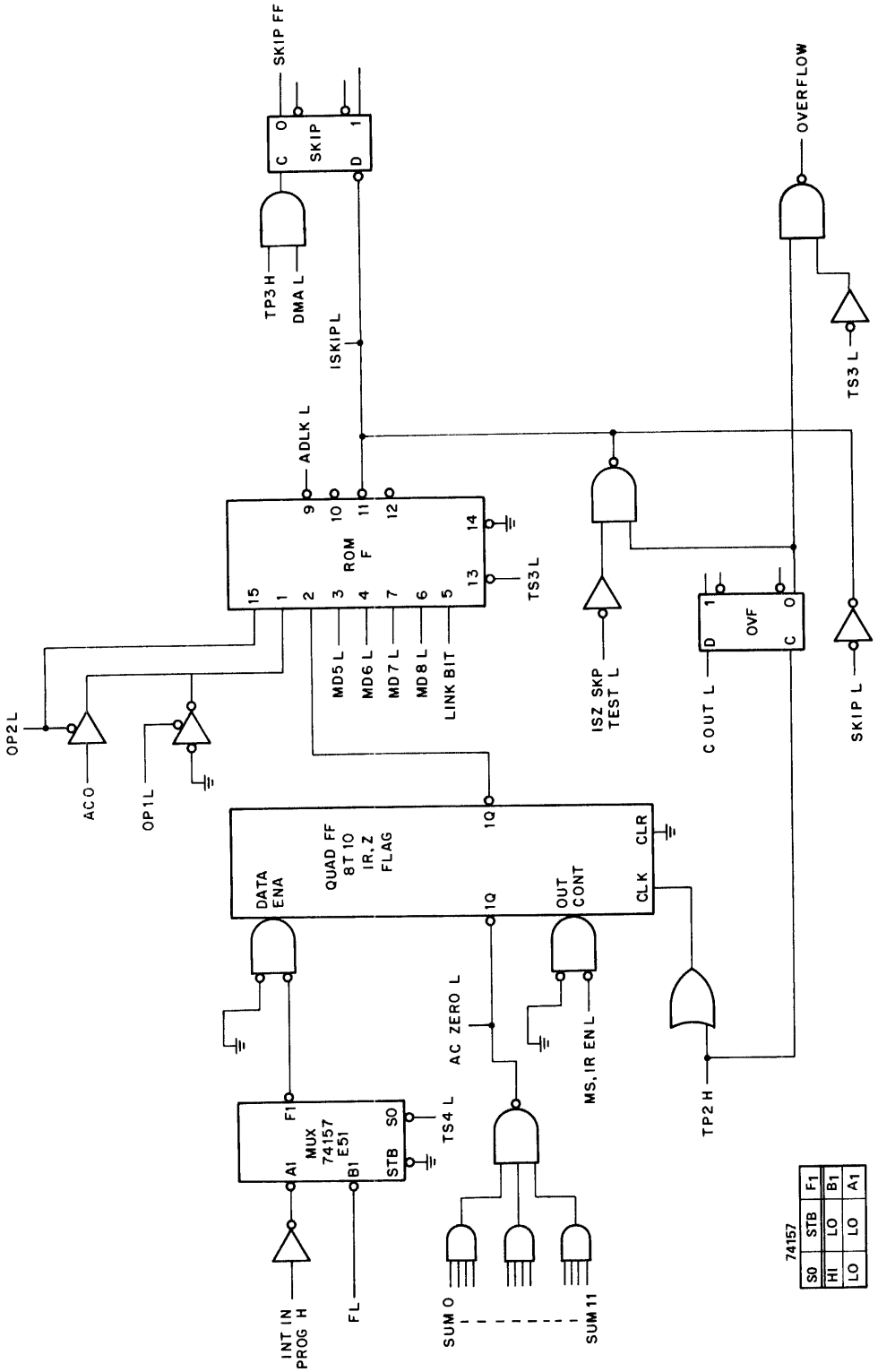


Figure 4-48 Skip Logic

The ISKIP L signal can be asserted two other ways: a peripheral can ground the Omnibus SKIP L line during an IOT instruction, causing ISKIP L to be asserted during TS3; or, an ISZ instruction can cause the OVF (OVERFLOW) flip-flop to be cleared, while also generating the ISZ SKP TEST L signal, thereby asserting ISKIP L.

An ISZ instruction directs the CPU to increment the data in the specified location and skip the next instruction if the result of the incrementalism is 0000(8) (the operand of the instruction must be 7777(8) for such a result to occur). The data is incremented during TS2 (Table 4-12; if the result is 0000(8), the C OUT L signal is asserted by adder 0 and the OVF flip-flop is cleared at TP2 time. During TS3, ISZ SKP TEST L is generated by ROM C and the ISKIP L signal is asserted. The Skip flip-flop is cleared at TP3 time and the following program instruction is skipped. Also during TS3, the OVERFLOW L signal is asserted. This signal is commonly used with a 3-cycle data break device; in such an application, OVERFLOW L is used by the device control to indicate the last transfer of the data break operation (Paragraph 4.6.4).

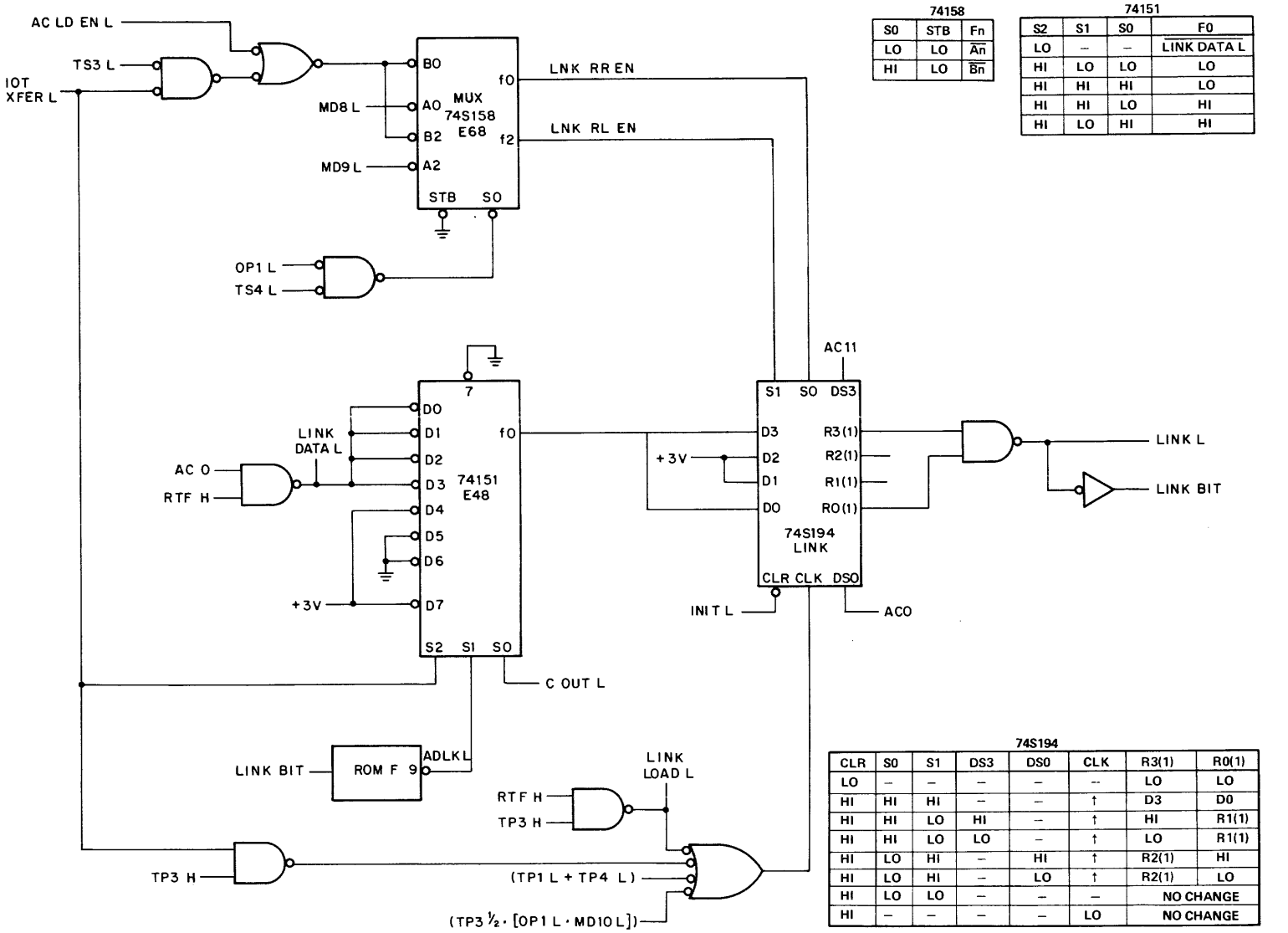
Note that the Skip flip-flop is clocked at TP3 time of all but a DMA cycle. This restriction is necessary because of the possibility of a data break device assuming control of the CPU immediately after a program interrupt request has been honored. Consider the following sequence of events: The Skip flip-flop is cleared at TP3 time of an SMA operate instruction, asserting the SKIP FF signal; an interrupt request is honored at the same time (the INT IN PROG H signal is asserted at INT STROBE L time); a data break device takes control of the CPU by asserting the CPMA DISABLE L signal at the same TP3 time and the MS, IR DISABLE L signal at the following TP4 time. The first event would normally cause the program count to be incremented and transferred to the CPMA register at TP4 of the SMA instruction. However, when the INT IN PROG H signal is asserted, ROM B (Table 4-13) is prevented from generating the necessary gating signals. If the third event did not occur, INT IN PROG H would force the CPU into the Execute cycle of the JMS instruction, during which cycle the incremented program count would be stored in location 0000(8) for retrieval at the conclusion of the program interrupt (Table 4-12). But, event three does occur and, thus, control of the CPU is assumed by the data break device before the instruction register is forced to the JMS instruction. When the data break device relinquishes control of the CPU, the Execute cycle of the JMS instruction will be entered and the PC+1 will be stored in location 0000(8), provided the Skip flip-flop is still clear and SKIP FF is high. This provision is accomplished by prohibiting any TP3 that occurs during the data break operation from setting the Skip flip-flop.

4.5.4 Link Logic

The Link is used with a TAD instruction and with Group 1 operate microinstructions that manipulate both the Link and the AC register. A TAD instruction causes the contents of a specified memory location to be added to the contents of the AC register. The result of the addition can include a carry from adder 0. Since such a carry is significant, it is registered in the Link shift register. The shift register can then be manipulated so that the information can be used in other AC operations. The Group 1 microinstructions can be used to clear and comple-ment the Link independently of the AC register, or to rotate the Link right or left along with the contents of the AC.

The Link logic is shown in Figure 4-49. The state of the link can be represented by the LINK BIT signal, which is monitored by ROM F (Figure 4-48 shows all the input signals that are monitored by the ROM). When the Link is to be complemented, because either a TAD instruction or a CML instruction is issued, ROM F controls the DEC74151 multiplexer with the ADLK L signal. The multiplexer provides Link inputs that are the complement of the Link's previous state. For example, assume that the Link contains a logic one. Thus, the LINK BIT signal is high. If the CML instruction is issued, ROM F decodes its input signals and negates the ADLK L signal. The f0 output of E48 goes low; this level is parallel loaded into the Link shift register at TP3 time, complementing the previous state of the Link (during TS3 of an operate instruction, ROM D in Table 4-11 asserts the AC LD EN L signal; the DEC 74S158 data selector causes LNK RR EN and LNK RL EN to go high, placing the Link shift register in the parallel load mode).

When a TAD instruction is issued, the C OUT L signal may or may not be asserted. If not, the f0 output of E48 assumes the same level as the previous state of the Link; i.e., if the Link was high before the TAD instruction, ADLK L goes low when ROM F decodes its input signals, and the f0 output goes high. Hence, the Link retains its previous state (during TS3 of the Execute cycle of a TAD instruction, ROM C asserts the AC LD EN L signal; thus, the Link shift register is kept in the parallel load mode). However, if the TAD instruction had resulted in a carry out, both ADLK L and C OUT L are asserted and the f0 output goes low, complementing the Link.



74158

S0	STB	Fn
LO	LO	$\overline{An}$
HI	LO	$\overline{Bn}$

74151

S2	S1	S0	F0
LO	–	–	LINK DATA L
HI	LO	LO	LO
HI	HI	HI	LO
HI	HI	LO	HI
HI	LO	HI	HI

74S194

CLR	S0	S1	DS3	DS0	CLK	R3(1)	R0(1)
LO	–	–	–	–	–	LO	LO
HI	HI	HI	–	–	↑	D3	D0
HI	HI	LO	HI	–	↑	HI	R1(1)
HI	HI	LO	LO	–	↑	LO	R1(1)
HI	LO	HI	–	HI	↑	R2(1)	HI
HI	LO	HI	–	LO	↑	R2(1)	LO
HI	LO	LO	–	–	–	NO CHANGE	
HI	–	–	–	–	LO	NO CHANGE	

08-1315

Figure 4-49 Link Logic

When the Link is to be cleared (CLL), ROM F negates the ADLK L signal no matter what the previous Link state. The f0 output of E48 is low, and the Link is cleared at TP3 time of the instruction.

Two of the processor IOT instructions are involved with the Link bit (Paragraph 4.6.2. The GTF instruction can be used to transfer the state of the Link to the 0 bit of the AC register. The RTF instruction enables the programmer to return a previous Link state from the AC register to the Link register. When the RTF instruction is issued the LINK DATA L signal causes the f0 output of E48 to assume the state of the AC0 bit. Then this state is loaded into the Link register at TP3 time by the LINK LOAD L signal (during TS3 of an IOT instruction, the LNK RR EN and LNK RL EN signals are high, keeping the Link shift register in the parallel load mode).

During TS3 of an operate instruction, ROM D asserts the AC LD EN L signal; the Link shift register is placed in the parallel load mode by LNK RR EN and LNK RL EN. If the instruction is a rotate instruction (RAR, RAL, RTR, RTL), the state of the Link during TS3 is loaded into the Link shift register at TP3 time; i.e., the Link is not changed when the shift register is clocked at TP3 time. During TS4, either LNK RR EN or LNK RL EN goes low, depending on the direction of shift (i.e., if the instruction directs a rotation to the right, LNK RL EN goes low, while LNK RR EN goes low for a rotation to the left); the Link shift register is placed in the right shift or left shift mode. If the instruction is RTR or RTL, the Link shift register is clocked at TP3 1/2 time, halfway through TS4. At this time, the content of AC bit 11 is loaded into R3(1) of the Link (assume the instruction is RTR); at the same time, AC bit 10 is shifted into AC11. At TP4 time, the Link is clocked again and the content of AC bit 11 (originally in AC bit 10) is loaded into R3(1) of the Link. Both R2(1) and R1(1) were loaded with logic 1 (positive voltage in the Link) at TP3 time; hence, both R0(1) and R3(1) are high after the two clocking operations and the LINK BIT signal exhibits the correct state. The original content of the Link shift register has been rotated two places to the right. The single-rotate instructions are effected similarly, but the Link shift register is clocked only at TP4 time, resulting in a shift of but one position.

4.6 I/O TRANSFER LOGIC

4.6.1 Programmed I/O Transfer Logic

Programmed I/O transfers use IOT instructions to initiate data exchanges between a user device and either the AC register or the PC register. Information is transferred to and from a device on the Omnibus DATA bus. Figure 4-50 illustrates the major register gating for a programmed I/O transfer, while Figure 4-51 shows both the logic that generates the gating control signals and a diagram that relates essential timing signals.

When an IOT instruction involving a data transfer is issued, the user device asserts the Omnibus C lines to generate the necessary major register gating control signals. For example, if an IOT instruction directs a particular device to transfer data to the PC register, the device asserts the C1 L signal and the C2 L signal and places the data on the DATA bus. ROM E produces DATA ENA L and PC LD EN L, thereby gating the data to the PC register during TS3. At TP3 time, essentially, the PC, AC, MQ CLK signal loads the data into the PC register.

Table 4-14 relates the input and output signals for ROM E and outlines the results achieved by the possible combinations of the C line signals. Note that six possible types of data transfers exist, which are represented by input codes 20(8) through 27(8). Input code 37 results when a GTF instruction is issued and the GTF H signal is asserted by the Processor IOT logic (Paragraph 4.6.2). The timing diagram in Figure 4-51 shows how the PC, AC, MQ CLK signal is generated during a normal I/O transfer cycle, i.e., when the IOT instruction does not require an extended timing cycle. (Paragraph 4.2.5 has a detailed discussion of I/O timing for both non-extended and extended timing cycles.)

4.6.2 Processor IOT Logic

A number of internal IOT instructions are designated processor IOT instructions. They are represented as 600X(8) and are concerned, in general, with program interrupts. The appropriate logic is shown in Figure 4-52.

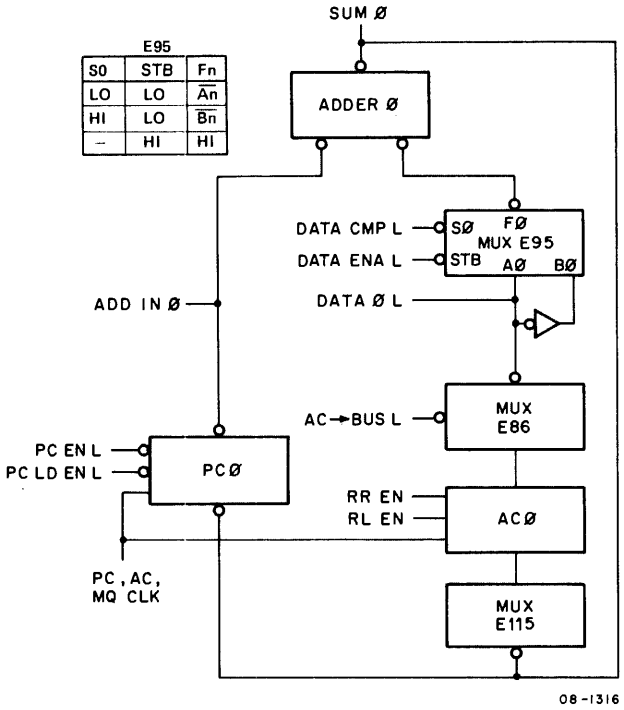


Figure 4-50 Major Register Gating (BIT00), Programmed I/O Transfer

When a processor IOT instruction is programmed, the INTERNAL I/O L signal is asserted so that peripherals interfaced to the Omnibus via the KA8-E option (Positive I/O Bus interface) will ignore the IOT instruction. The seven processor IOT signals are generated by ROM J. Table 4-15 lists the inputs and outputs for the ROM in detail. Note that only inputs 20(8) through 27(8) are used for the processor IOTs. Inputs 10(8) through 17(8) are used when STATUS information is to be placed on the DATA lines during TS1.

Either a peripheral or the Programmer's Console can cause STATUS information to be placed on the DATA lines by negating the IND1 L and IND2 L signals. When this is done the STATUS L signal is asserted by the DEC74S139 decoder during TS1, and ROM J generates the GTF H signal. The status of the INT ENA flip-flop is gated to the DATA 4 line, the status of the INT RQST line is gated to the DATA 2 line, and the status of the Link Bit is gated to the DATA 0 line. If the operator has used the Programmer's Console to negate the IND signals, the STATUS information is gated to the console and displayed during TS1 (the programmer will have halted the CPU before attempting to display the STATUS information).

The GTF H signal is also asserted when the GTF instruction is programmed. In this case, the I/O L signal is generated and the significant operation takes place during TS3 (when the STATUS L signal can be only high). Again, the DATA 4, DATA 2, and DATA 0 lines reflect the status of the INT ENA flip-flop, the INT RQST L signal, and the Link Bit, respectively. This information, and that carried on the remaining DATA lines, is gated to the AC register and loaded at TP3 time (Table 4-14, especially the entry for Input Code 37(8)).

The RTF instruction causes ROM J to assert RTF H and INT ON H. RTF H restores a previous state of the Link, while INT ON H turns on the interrupt system. Both the GTF and RTF instructions have minor significance within the processor itself; their full potential is realized only when a KM8-AA Memory Extension option is included in the system.

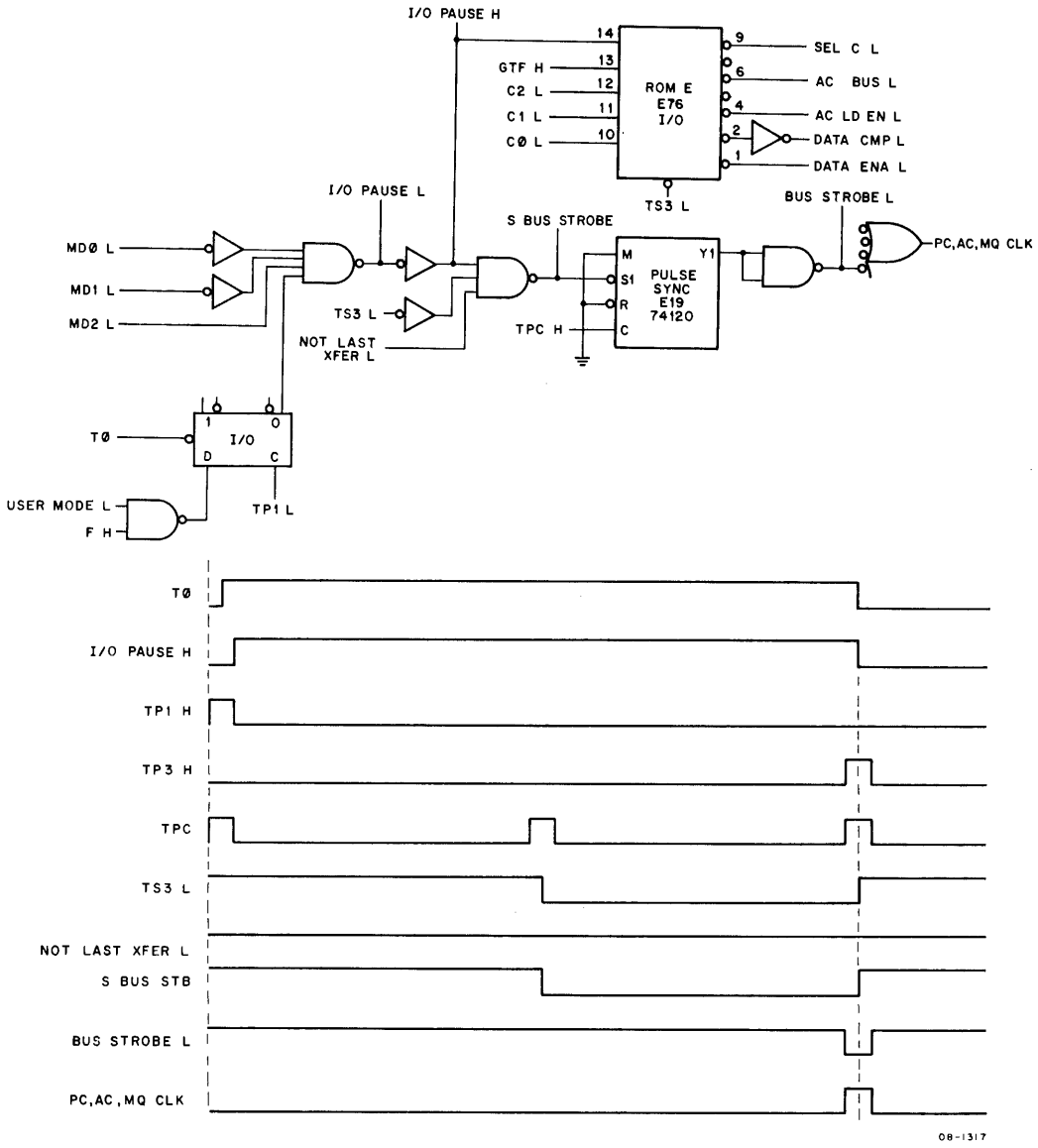


Figure 4-51 Programmed I/O Transfer Logic

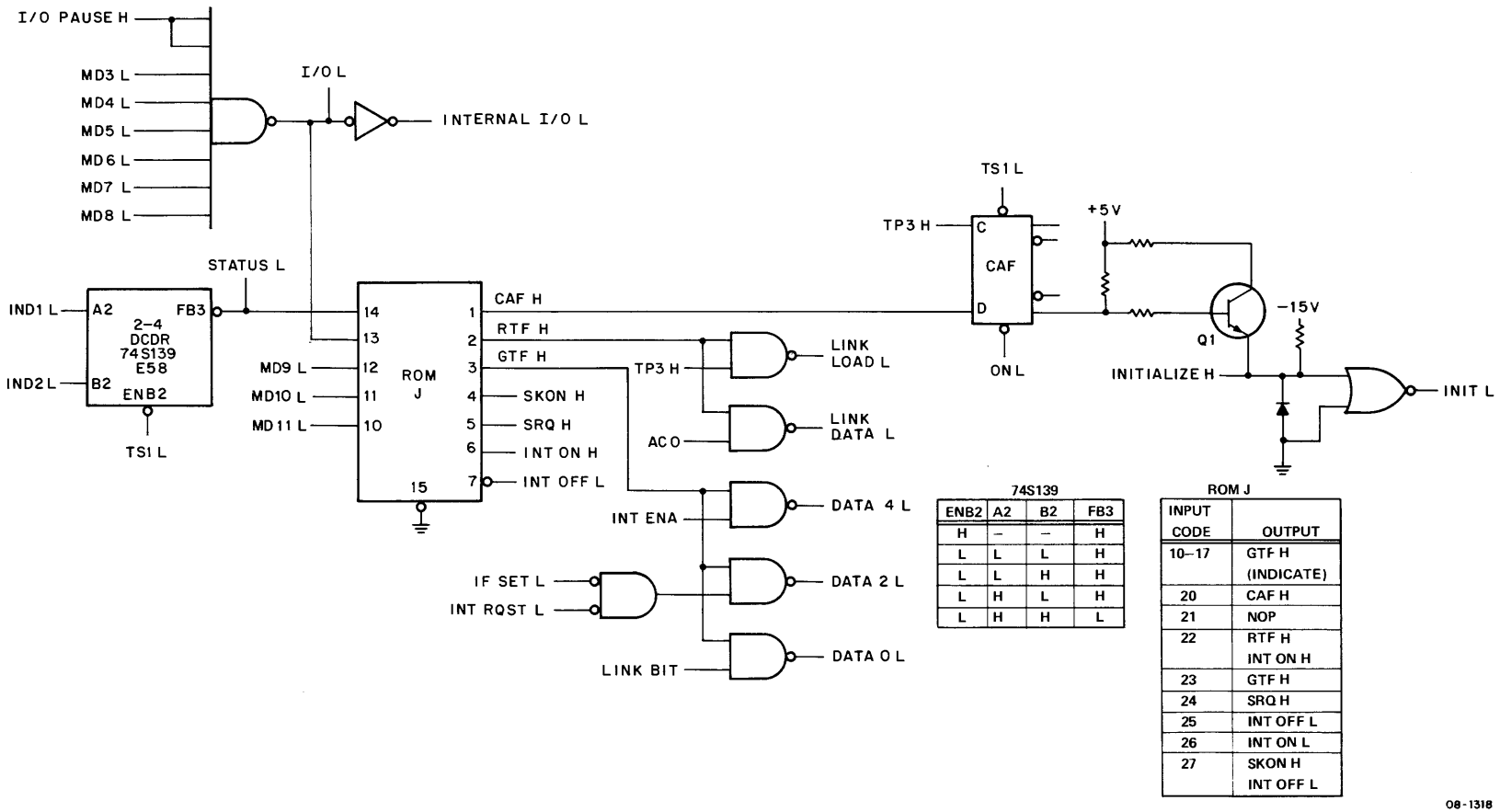
The CAF instruction causes the ROM to generate CAF H; thus, the CAF flip-flop is set at TP3 time. Transistor Q1 is turned on, asserting the Omnibus INITIALIZE H signal as well as the CPU INIT L signal. The CAF flip-flop is cleared when the TS1 L signal goes low, negating the initializing signals at the start of the next program instruction; the flip-flop is cleared even if the operator has been single-stepping the CPU and ends with the CAF instruction (the timing generator asserts the TS1 L signal before halting). When power is turned on, ON L is held low for 100 ms after POWER OK H goes high. The initializing signals are generated for this length of time to enable all system equipment to complete the necessary initializing operations. When ON L goes high, TS1 L clears the CAF flip-flop and the initializing signals are negated.

The SKON H, SRQ H, INT ON H, and INT OFF L signals are program interrupt-generated signals. They are discussed in detail in Paragraph 4.6.3.

Table 4-14
ROM E input/Output Signals

(ROM Enabled During TS3)

Input Code	Input Signal Low					ROM Output Signal	DCDR Output	Result
	I/O PAUSE H	GTF	C2 L	C1 L	C0 L			
0	X	X	X	X	X	DATA CMP L		
1	X	X	X	X		DATA CMP L		
2	X	X	X		X	DATA CMP L		
3	X	X	X			DATA CMP L		
4	X	X		X	X	DATA CMP L		
5	X	X		X		DATA CMP L		
6	X	X			X	DATA CMP L		
7	X	X				DATA CMP L		
20		X	X	X	X	DATA ENA L, PC LD EN L		Input data to PC register
21		X	X	X		DATA ENA L, PC LD EN L		Input data to PC register
22		X	X		X	DATA ENA L, PC LD EN L, SEL C L	PC EN L	Input data added to PC contents, result loaded into PC
23		X	X			DATA ENA L, PC LD EN L, SEL C L	PC EN L	Input data added to PC contents, result loaded into PC
24		X		X	X	DATA ENA L, AC LD EN L		Input data to AC register
25		X		X		DATA ENA L, AC LD EN L, AC→ BUS L		AC to the data lines (output transfer), AC contents returned to AC; input data can be OR'ed with AC
26		X			X	DATA CMP L, AC LD EN L, AC→ BUS L		AC to the data lines (output transfer), zero to the AC
27		X				DATA ENA L, AC LD EN L, AC→ BUS L		AC to the data lines (output transfer), AC contents returned to AC; input data can be OR'ed with AC
37						DATA ENA L, AC LD EN L		Link bit to AC0



74S139

ENB2	A2	B2	FB3
H	–	–	H
L	L	L	H
L	L	H	H
L	H	L	H
L	H	H	L

ROM J

INPUT CODE	OUTPUT
10–17	GTF H (INDICATE)
20	CAF H
21	NOP
22	RTF H INT ON H
23	GTF H
24	SRQ H
25	INT OFF L
26	INT ON L
27	SKON H INT OFF L

08-1318

Figure 4-52 Processor IOT Logic

Table 4-15
ROM J Input/Output Signals

(ROM Enabled Permanently)

Input Code	Input Signal Low					Processor-IOT Instruction	Result
	STATUS L	i/O L	MD9 L	MD10 L	MD11 L		
10	X		X	X	X	GTF H	Status word gated to data lines during TS1. Information on data lines shown below.
11	X		X	X		GTF H	
12	X		X		X	GTF H	
13	X		X			GTF H	
14	X			X	X	GTF H	
15	X			X		GTF H	
16	X				X	GTF H	
17	X					GTF H	
20		X	X	X	X	CAF H	
21		X	X	X		NOP	
22		X	X		X	RTF H, INT ON H	
23		X	X			GTF H	
24		X		X	X	SRQ H	
25		X		X		INT OFF L	
26		X			X	INT ON H	
27		X				SKON H, INT OFF L	

Data Bit	Information
0	Link Status
2	Status of INT RQST L signal
4	Status of Interrupt Enable flip-flop
5	USER MODE L signal status*
6–8	IF<0:2>*
9–11	DF<0:2>*

*From memory extension control, if present.

4.6.3 Program Interrupt Logic

Program interrupt data transfers are more efficient than programmed I/O transfers. In the program interrupt transfer mode, the program is interrupted only when an option demands attention by asserting the Omnibus INT RQST L signal. The interrupt system monitors this INT RQST L signal. If the system is turned on when this signal is asserted, the processor executes a hardware-generated JMS to location 0. Simultaneously, it turns off the interrupt system; thus, further interrupts can occur only when the present one has been serviced. A program subroutine is entered to determine the identity of the requesting option. When this identity has been established, a servicing subroutine allows the option to take part in a programmed I/O dialogue with the processor.

The Interrupt logic is shown in Figure 4-53. The system can be turned on when the ION instruction asserts the INT ON H signal. Each stage of the DEC8271 quad flip-flop must be in the clear condition; if so, the DEC74153 multiplexer gates a high to input D1 of the quad flip-flop and a low to input D2. The quad flip-flop is set at INT STROBE L time, asserting the INT ENA signal. During the next Fetch cycle, the high at multiplexer input B1 is gated to input D2 of the quad flip-flop; again, input D2 of the flip-flop is high. D3 of the flip-flop might be high, as well, provided, first, that the INT RQST L signal has been asserted by a peripheral and, second, that the Fetch cycle being performed is that of a 1-cycle instruction, i.e., IF SET L is low. However, if we assume that the Fetch cycle is part of a multi-cycle instruction, D3 is low; thus, at INT STROBE L time INT DLY and INT ENA, only, are asserted. During the concluding cycle of the instruction, and if the INT RQST L signal is low, all inputs to the quad flip-flop, except D0, are high. At INT STROBE L time INT ENA, INT DLY, and INT SYNC go high and the INT IN PROG H signal is asserted.

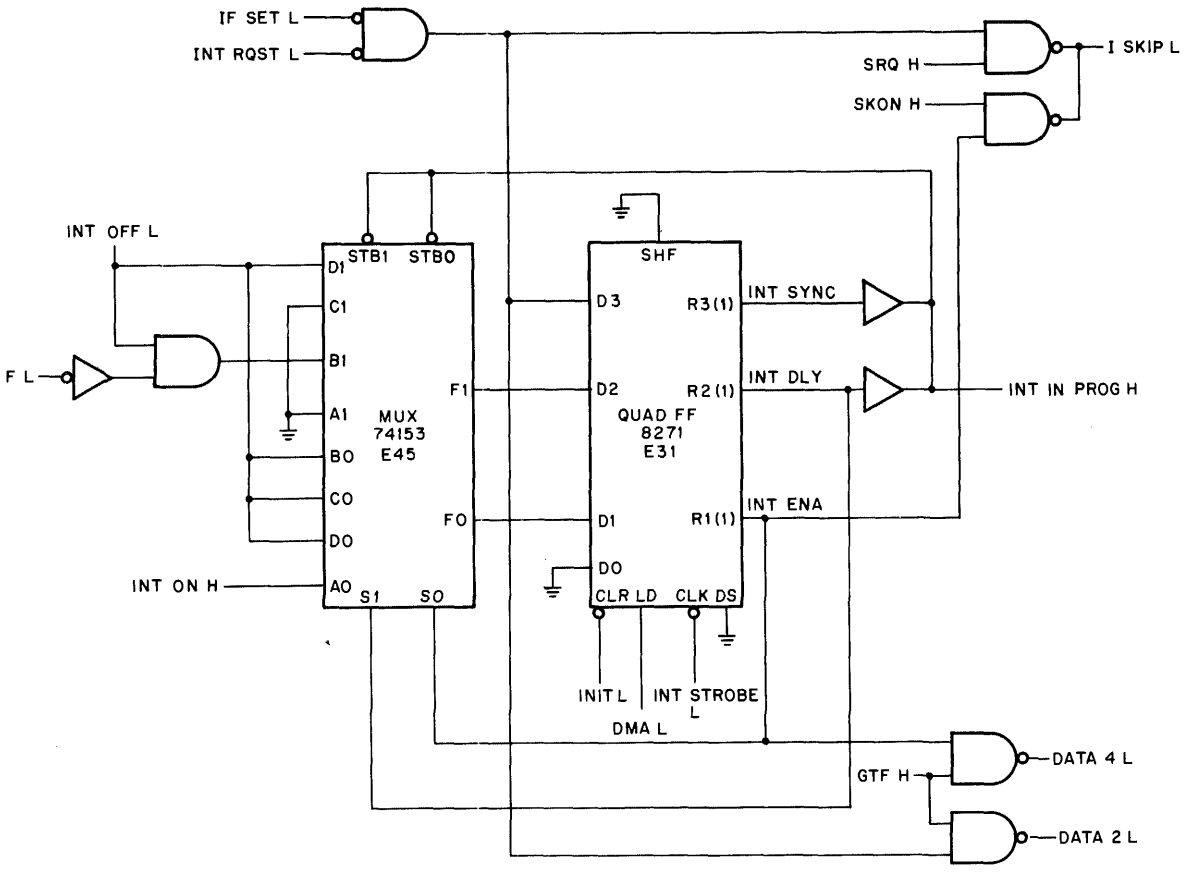
Because INT IN PROG H is high during TS4, the Instruction register is forced to JMS at TP4, while the Major State register is forced to the Execute state. During this Execute state cycle, the program count to which control will return after the program interrupt, is stored in memory location 0000. The INT STROBE L pulse that occurs during the forced-JMS Execute cycle clocks the quad flip-flop, negating the INT DLY and INT ENA signals and, as a result, the INT IN PROG H signal (note that it now makes no difference what happens to the INT SYNC signal). The CPU then proceeds to the interrupt servicing routine. At the end of the routine, an IOT instruction turns on the interrupt system again. Note that there is a delay of at least one complete timing cycle from the time that the INT ENA signal goes high until the INT IN PROG H signal can again be asserted (if data break devices suspend the normal timing, there can be a delay of many more than one cycle). This delay enables the CPU to obtain the return address from memory location 0000, restoring control to the program before allowing a new interrupt to occur.

The IOF instruction turns off the interrupt system by asserting the INT OFF L signal. Because both INT DLY and INT ENA are high and INT SYNC is low when the system is on (the system can be on without an interrupt request), the multi-plexer gates the lows at its D0 and D1 inputs to the quad flip-flop. The INT STROBE L signal then clocks the flip-flops, negating INT ENA and INT DLY.

Two CPU IOT instructions test the status of the interrupt system. The SKON instruction asserts the I SKIP L signal if the interrupt system is on, i.e., if the INT ENA signal is high. If I SKIP L is low, the SKIP flip-flop is set at TP3 time. Then, during TS4, the C IN L signal is asserted, the program count in the PC register is incremented, and the instruction following SKON is skipped. Because the INT OFF L signal is generated along with the SKON H signal (Figure 4-52), the interrupt system is turned off just after INT ENA is sampled. The SRQ instruction can also cause a program instruction skip, but only if an interrupt request has been generated by a peripheral.

4.6.4 Data Break Transfers

Data transfers between a data break device and memory or between the Programmer's Console and memory occur in the CPU DMA state. This state provides direct communication between the device and memory, allowing the device to assume control of major register gating by asserting a number of Omnibus signals when it is ready to make a data transfer. Figure 4-54 illustrates the part of major register gating that is most involved with data breaks, while Figure 4-55 shows the logic that generates the applicable gating signals.



74153

S1	S0	STB0,1	F0	F1
L	L	L	A0	A1
L	H	L	B0	B1
H	L	L	C0	C1
H	H	L	D0	D1
–	–	H	L	L

8271

SHF	LD	OUTPUT AFTER CLOCK (INT STROBE L)
L	L	SAME AS BEFORE CLOCK
L	H	SIGNAL AT CORRESPONDING INPUT

08-1319

Figure 4-53 Program Interrupt Logic

When the data break device is ready to begin a transfer, it asserts the MS,IR DISABLE L and CPMA DISABLE L signals; the former disables both the IR register and the Major State register (E62), forcing the CPU to the DMA state, while the latter negates CPMA->BUS L at TP4 time, removing the CPMA register from the MA lines. With the CPMA register disabled, the device can specify the memory location from or to which data will be transferred.

Three types of data break transfers are available to a peripheral, i.e., Input (Break Deposit), Output, and Add to Memory (ADM). Table 4-16 provides the input/output signal relationship for ROM A. The entries for input codes 30(8) through 37(8) apply to the Break Deposit and ADM operations; the Output transfer is just a variation of ADM. For example: If the device is to make an ADM transfer, it places the memory address on the MA lines after asserting CPMA DISABLE L and MS,IR DISABLE L; at TP1 of the DMA cycle, the device asserts MA, MS LOAD CONT L so that TP4 of the DMA cycle does not clock the CPMA register (Paragraph 4.4.2); at the beginning of TS2, the device asserts BREAK DATA CONT L, causing the MD EN L signal to be produced by the decoder associated with ROM A (Figure 4-31 shows the decoder) and, thus, gating the data in the addressed location to the adder; also, early in TS2

the device places the information to be added on the DATA bus, from where it is gated to the adder by multiplexer E95; the result is placed on the SUM lines and loaded into the MB at TP2; because MD DIR L goes high at TP2, the MB contents are placed on the MD bus and stored in the addressed memory location during the write operation. If an output transfer is to be performed, the device follows the same procedure as for the ADM, without placing information on the DATA lines; the data to be transferred to the device can be taken from the MD lines at TP2, TP3, or TP4 time.

The ADM operation might result in a carry-out from adder 0 (C OUT L is asserted). If so, the OVF flip-flop, Figure 4-55, is cleared at TP2 time, and the OVERFLOW L signal is generated during TS3. The device can use this signal as directed by the program; however, OVERFLOW L is commonly used with a 3-cycle data break device to indicate the last transfer of the data break operation.

The Non-stop Deposit function, entries 10(8) through 13(8) in Table 4-16, is intended to be used, primarily, during bootstrap operations. The function gives the same result as Panel Deposit, but because STOP L is not generated, the CPU continues to run. When the BOOT button on the Programmer's Console is pushed (or when the BOOT switch on the Limited Function Panel is pressed), the Bootstrap Loader option provides the starting address for the bootstrap operation and asserts MEM START L, LA ENABLE L, and BREAK DATA CONT L. The option places information on the DATA bus during each TS2 until the bootstrap program is loaded entirely, at which time normal CPU operations are resumed.

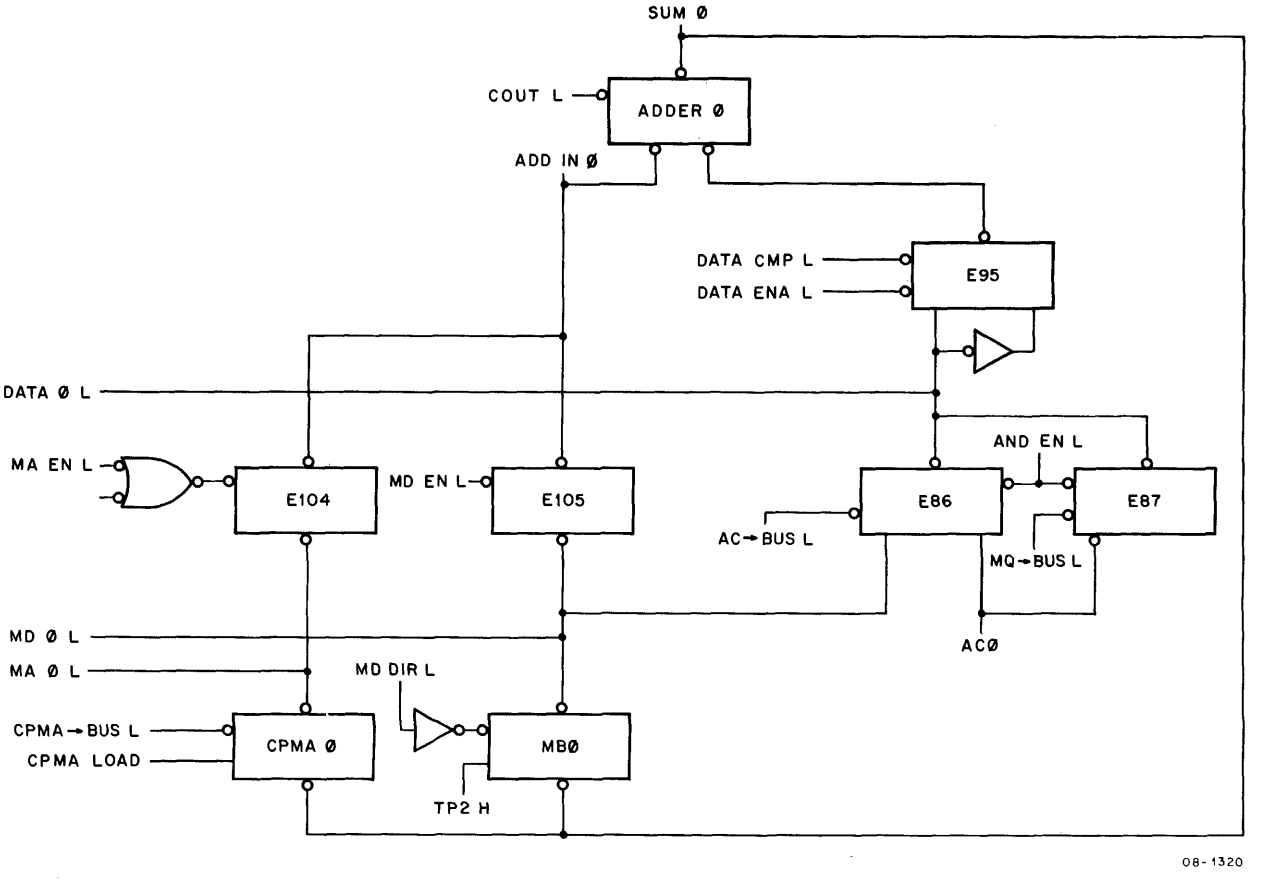


Figure 4-54 Major Register Gating (BITO), Data Break Transfer

Table 4-16
ROM A Input/Output Signals

(ROM Enabled for DMA State)

Input Code	Input Signal Low					CPU Time State	ROM Output Signal	DCDR Output Signal	Result	
	LA ENABLE L	KEY CONTROL L	BREAK DATA CONT L	T0	T1					
0	X	X	X	X	X	TS1	DATA CMP L		LOAD	When console 'LXA' button is pushed, address is placed on data bus (DATA 6–11), gated to IF and DF registers and loaded by PULSE LA H.
1	X	X	X	X		TS4	DATA CMP L, SEL A L, SEL C L	AND EN L	EXTENDED	
2	X	X	X		X	TS2	DATA CMP L, SEL C L, SEL B L	MD EN L	ADDRESS,	See text
3	X	X	X			TS3	DATA CMP L, SEL A L, SEL C L	AND EN L	FIELD 7	
4	X	X		X	X	TS1	DATA CMP L		LOAD	When console 'LXA' button is pushed, address is placed on data bus (DATA 6–11), gated to IF and DF registers and loaded by PULSE LA H.
5	X	X		X		TS4	DATA CMP L		EXTENDED	
6	X	X			X	TS2	DATA CMP L, SEL C L, SEL B L	MD EN L	ADDRESS,	See text
7	X	X				TS3	DATA CMP L		FIELD 0	
10	X		X	X	X	TS1	DATA CMP L, PC LD EN L, CARRY EN L, SEL B L	MA EN L		MA+1 → PC at TP1
11	X		X	X		TS4	DATA CMP L, SEL G L	PC EN L	NON-STOP	PC contents loaded into CPMA at TP4.
12	X		X		X	TS2	DATA ENA L		DEPOSIT	Information on data bus gated to MB, loaded at TP2, deposited in addressed memory location.
13	X		X			TS3	DATA CMP L			No major register operation.
14	X			X	X	TS1	DATA ENA L			When console 'LA' button is pushed, address is placed on data bus, gated to CPMA, and loaded by CPMA LOAD signal.
15	X			X		TS4	DATA CMP L, SEL C L	PC EN L	LOAD	
16	X				X	TS2	DATA CMP L, SEL C L, SEL B L	MD EN L	ADDRESS	See text
17	X					TS3	DATA ENA L, PC LD EN L			
20		X	X	X	X	TS1	DATA CMP L, PC LD EN L			MA+1 (See Figure 4-54) loaded into PC at TP1.
21		X	X	X		TS4	DATA CMP L, SEL C L	PC EN L	PANEL	PC contents loaded into CPMA at TP4, providing MA, MS LOAD CONT L is high (signal is low if 'E THIS' button is pushed).
22		X	X		X	TS2	DATA CMP L, SEL C L, SEL B L	MD EN L	EXAMINE	Data in addressed location loaded into MB at TP2; operator used 'MD' and 'DISP' buttons to display MB contents.
23		X	X			TS3	DATA CMP L, STOP L			Timing generator 'RUN' flip-flop cleared at TP3, halting timing cycle after TS4 is completed.
24		X		X	X	TS1	DATA CMP L, PC LD EN L			MA+1 (See Figure 4-54) loaded into PC at TP1.
25		X		X		TS4	DATA CMP L, SEL C L	PC EN L	PANEL	PC contents loaded into CPMA at TP4, providing MA, MS LOAD CONT L is high (signal is low if 'D THIS' button is pushed).
26		X			X	TS2	DATA ENA L		DEPOSIT	Console entry data placed on data bus, gated to MB, loaded at TP2, deposited in addressed memory location.
27		X				TS3	DATA CMP L, STOP L			Timing generator 'RUN' flip-flop cleared at TP3, halting timing cycle after TS4 is completed.
30			X	X	X	TS1	DATA CMP L			No major register operation.
31			X	X		TS4	DATA CMP L		ADD TO	No major register operation.
32			X		X	TS2	DATA ENA L, SEL C L, SEL B L	MD EN L	MEMORY BREAK	Data in addressed location gated to adder, added to information placed on data bus by peripheral; result loaded into MB at TP2, returned to memory.
33			X			TS3	DATA CMP L			No major register operation.
34				X	X	TS1	DATA CMP L			No major register operation.
35				X		TS4	DATA CMP L		BREAK	No major register operation.
36					X	TS2	DATA ENA L		DEPOSIT	Peripheral places information on data bus; information gated to MB register, loaded at TP2, written into addressed memory location.
37						TS3	DATA CMP L			No major register operation.

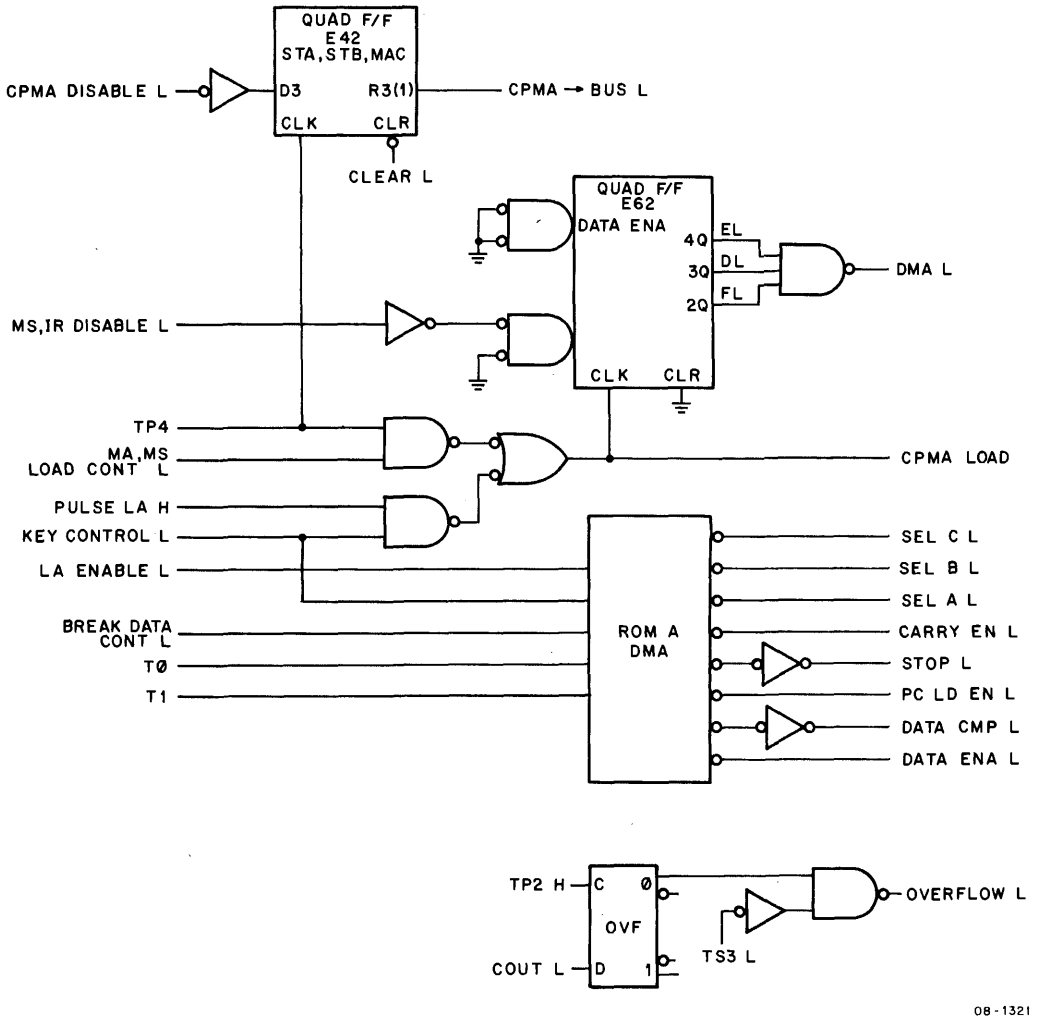


Figure 4-55 Data Break Transfer Control Signal Logic

Communication between memory and the Programmer's Console is also effected during the DMA state. The Panel Exam and Panel Deposit functions permit an operator to examine or deposit data in an addressed location (refer to Paragraph 4.6.4 for details); the Major Register gating during all timing cycles of both functions is outlined in Table 4-16.

The Load Address and Load Extended Address functions can be initiated by the Programmer's Console LA and LXA pushbuttons, respectively. The applicable TS1 operations are shown in the table. Each of these functions can be initiated by the auto-start feature that is available with the PDP-8/A CPU. This feature was introduced in Paragraph 4.2.1; the Major Register gating and the appropriate timing will be detailed in the following paragraphs.

Figure 4-56 shows the auto-start timing, while Figure 4-57 illustrates the associated logic. The discussion that follows assumes that contact 4K of switch S1 is closed and contact F7 is open, i.e., the starting address is in memory field 0.

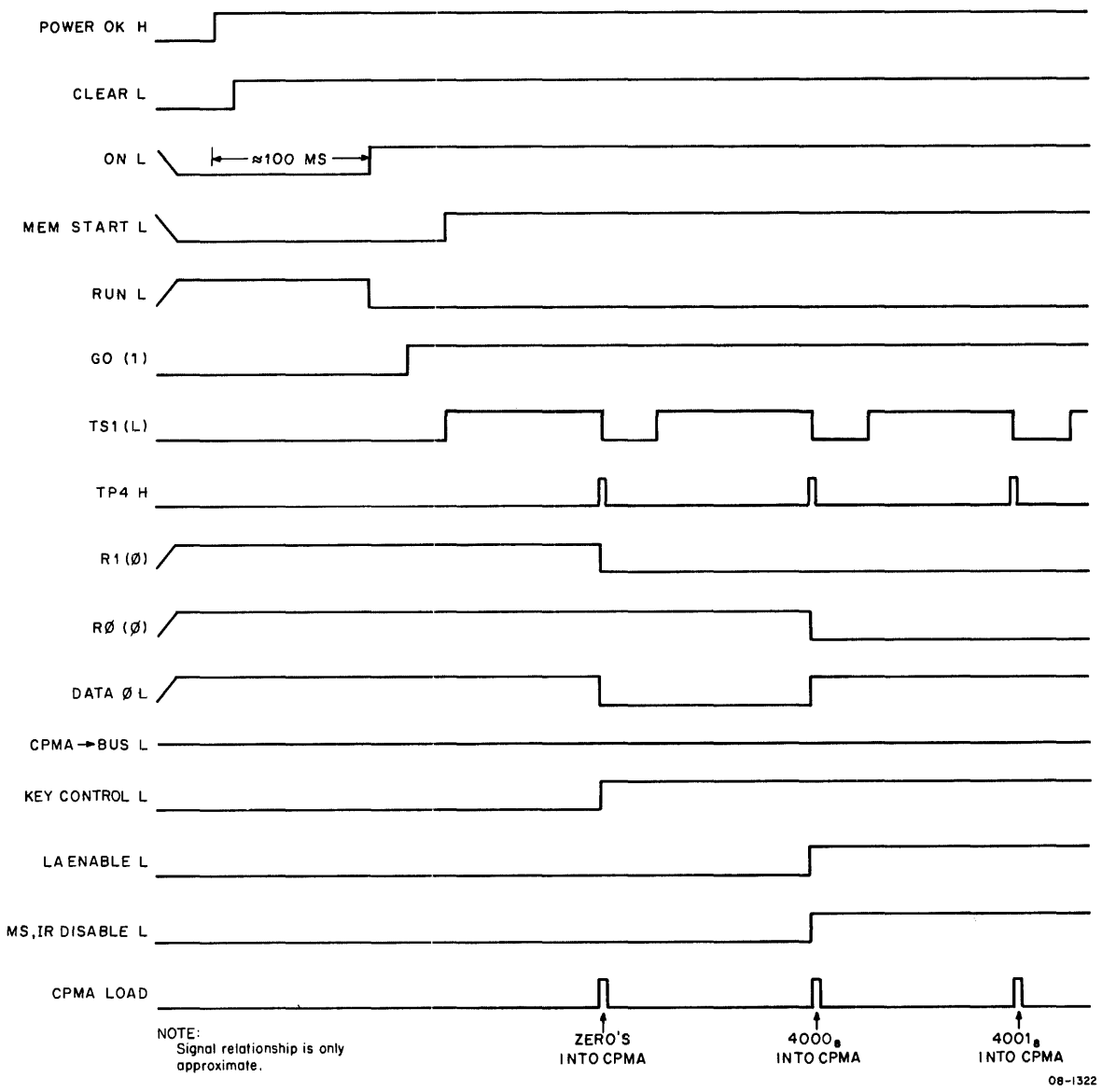


Figure 4-56 AUTO-START Timing

When the auto-start sequence begins, the memory field address is loaded into the IF and DF registers of the KM8-AA Extended Memory option. This event occurs during the first timing cycle of the sequence, when the KEY CONTROL L and LA ENABLE L signals are asserted. The entries in Table 4-16 for input codes 4(8) through 7(8) apply to this first timing cycle. During TS1 no major register operations take place (the RESULT entry for TS1 indicates what happens when an extended address is loaded from the Programmer's Console). During TS2, the data in the addressed memory location – a location that is both random (the state of the CPMA at power-on is uncontrollable) and immaterial – is gated through Major Register gating to the MB register, loaded at TP2, and returned to the memory location (MD DIR L goes high at TP2). This operation is of no significance to the auto-start feature, but is necessary so that the data in the memory location is retained. During both TS3 and TS4 the DATA lines are high (multiplexers E86 and E87 are disabled), and the IF and DF registers are loaded with logic 0. Since the SUM lines are also high during TS3 and TS4, the CPMA register is loaded with zeroes at TP4.

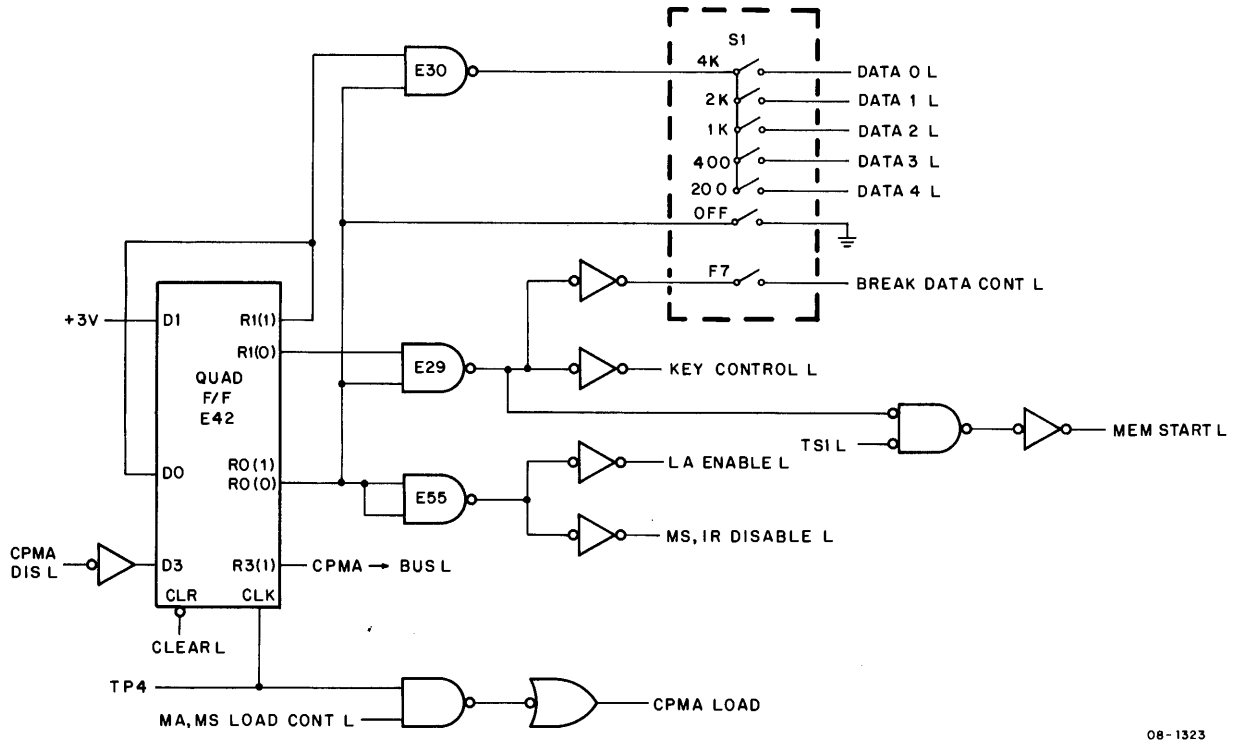


Figure 4-57 AUTO-START Timing, CPU Logic

During the second timing cycle of the sequence, KEY CONTROL L is negated, while DATA 0 L is asserted; input codes 14(8) through 17(8) of Table 4-16 are pertinent. In TS1, no operation takes place (the RESULT entry indicates what happens when an address is loaded from the Programmer's Console). During TS2, the data in location 0000(8) is gated to the MB, loaded, and returned to memory. In TS3 the information on the DATA lines, 4000(8), is gated to the PC register and loaded at TP3 time. During TS4, the PC contents are gated through Major Register gating to the CPMA register and loaded at TP4 time. At this same TP4 time MS,IR DISABLE L is negated and the CPU goes into the Fetch cycle, carrying out the instruction in location 4000(8).

If the auto-start address had been located in memory field 7, Major Register gating operations in TS3 and TS4 would have been as outlined in the entries for input codes 1(8) and 3(8) of Table 4-16. During both time states the AND EN L signal gates the contents of the AC register through multiplexer E87 to the DATA bus. If the AC contains zeroes, as it must for this function to work properly, 7777(8) is placed on the DATA bus and the IF and DF registers are loaded with 7(8). All other autostart operations are the same as for memory field 0.

CHAPTER 5
MEMORY OPTIONS

PDP-8/A Memory Options are as follows:

MR8-A Read Only Memory (ROM) in 1K, 2K, or 4K sizes.

MS8-A Random Access Read Write memory (RAM) available in 1K, 2K, or 4K sizes.

MR8-FB Reprogrammable Read Only Memory (PROM) available in 1K size with 256 words of read/write RAM memory.

MM8-AA 8K Core Memory

MM8-AB 16K Core Memory

The PDP-8/A memory system can be configured from ROM, RAM, or PROM or combinations of these memories. The memory system can be expanded up to 32K provided there is adequate current available from the power supply.

Each of the various memory options is discussed in the following sections.

SECTION 1
MR8-A READ ONLY MEMORY (ROM)

5.1 MR8-A READ ONLY MEMORY (ROM) DESCRIPTION

The MR8-A is a semiconductor memory option for the PDP-8/A. It consists of either 1K, 2K or 4K X 12 data storage locations which are addressed in the same way as core memory locations. However, unless operated together with a writable memory such as the MS8-A (RAM), it is a read only device.

A write capability is furnished by the MS8-A RAM memory. Special circuitry enables the MR8-A to utilize the write capabilities of the RAM. Each of the 4K locations in the ROM has an additional 13th bit, which when set to a logical 1, directs the access of a location in the RAM. Write type instructions have operands whose locations in the ROM have the 13th bit set to a 1, specifying that the remaining 12 bits are to be treated as an address of a RAM word.

Programming methods used with core memories can be adopted (without substantial alteration) to the ROM/RAM combination.

The capacity of the MR8-A depends on the number of memory chips on the board. The normal complement is a 16 X 3 array of Silicon Gate MOS chips, each organized in a 256 words X4 bit matrix. This constitutes a 4K X 12 memory. In addition, 4 chips are required for the 13th bit. This standard configuration can be changed by removing chips in 1K blocks.

Additional information on the memory chips is contained in subsequent paragraphs and in Appendix D.

The description that follows is divided into two parts: a general discussion with blocks of logic, such as address selection and timing and control, and a more detailed description of the logic in each block.

5.1.1 MR8-A Physical Description

The MR8-A is a quad module (Figure 5-1) with four bottom connectors (A, B, C, and D) which plug into the Omnibus. In addition, it has four top connectors, three (F, H, and J), which are used for programming and one (E) which provides interconnection with the RAM module (M8311).

Figure 5-2 shows the arrangement of the ROM and RAM boards and the Omnibus.

5.1.2 MR8-A Specifications

The MR8-A specifications are listed in Table 5-1.

5.2 FUNCTIONAL DESCRIPTION

The MR8-A ROM memory performs three basic functions:

1. ROM address decoding
2. ROM content accessing
3. When 13th bit is set, RAM addressing

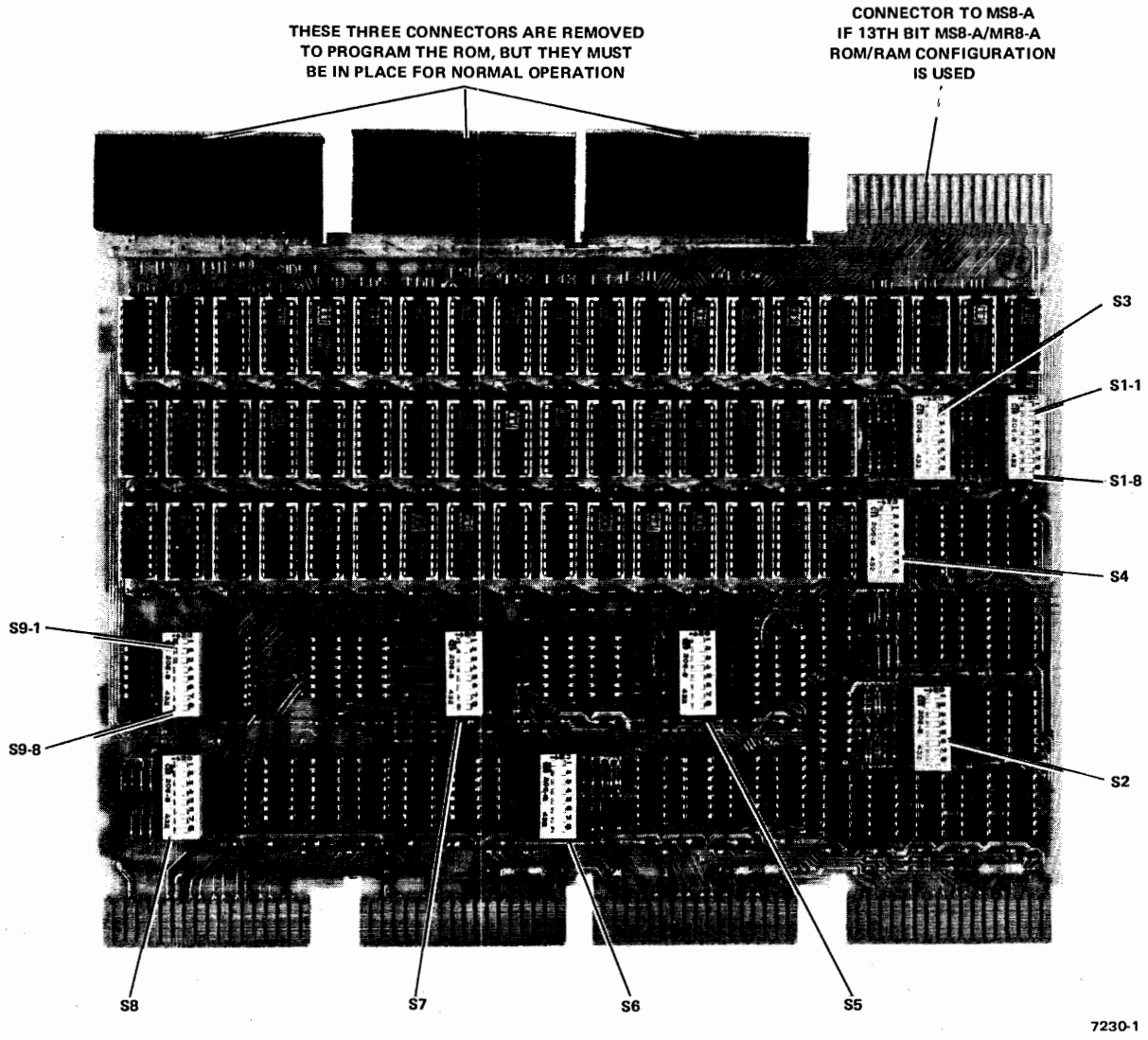


Figure 5-1 MR8-A ROM Memory Module (M8312)

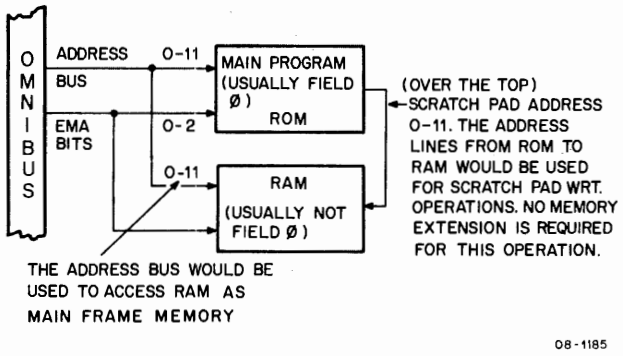


Figure 5-2 ROM/RAM Configuration

Table 5-1
MR8-A Specifications

Characteristic	Specification	
Power Requirements for the 1024 Bit Chip	**Typical**	**Worst Case**
1K size memory	+5 V ± 5% 2 A	+5 V ± 5% 2.7 A
4K size memory	+5 V ± 5% 5 A	+5 V ± 5% 7.4 A
Memory Cycle Time		
ROM (alone)	1.5 μs	
ROM-RAM (ROM cycle)	1.6 μs	
ROM-RAM (RAM cycle)	300 ns are added to the normal RAM cycle	
Programming Method	By external means (MR8-SA Programmer)	
Memory Capacity	1K, 2K or 4K	
Temperature	5 to 50° C	
Environment	Standard Computer Environment	
Testing	The tape used in programming the ROM is utilized to run the diagnostics.	

The major logic blocks and signal flow for accomplishing these functions are shown in Figure 5-3. The timing of the signals during one memory cycle is shown in Figure 5-4. A list and definition of the signals used in the timing diagram are defined in Table 5-2.

A general description of the operation of the MR8-A based on the functional blocks, the connecting signal lines, and the timing diagram follows.

Detailed descriptions of each of the logic blocks are presented in Paragraph 5.4.

5.2.1 Addressing

At TP4 the ROM memory register is cleared and a new address is placed on the Memory Address lines MA<0-11>.

The eight least significant address bits MA<4-11> are driven directly to the memory chip array of 16 columns by three rows and are applied in parallel to each chip where they are decoded by the chip circuitry; one word out of 256 on each chip is selected.

The four most significant address lines, MA<0:3>, are decoded to select one of 16 chip columns. The addresses can range from 0-400(8) (the first column) to 7377-7777(8) (the 16th column), i.e., from 0 to 4096(10).

The address select logic also determines whether the address is within the ROM's memory space in the larger 32K computer memory. This is done by decoding the three extended Memory Address lines, EMA<0:2>. A signal FIELD H is transmitted to the control logic when a valid address has been decoded.

5.2.2 Timing and Control

The basic timing is provided by the processor, which generates four time pulses (TP1-TP4), four time states (TS1-TS4), and two memory control signals (MD DIR L and RETURN H). However, additional control and timing signals are required by the MR8-A for the selection of one out of two modes of operation mentioned above, ROM or ROM-RAM combination.

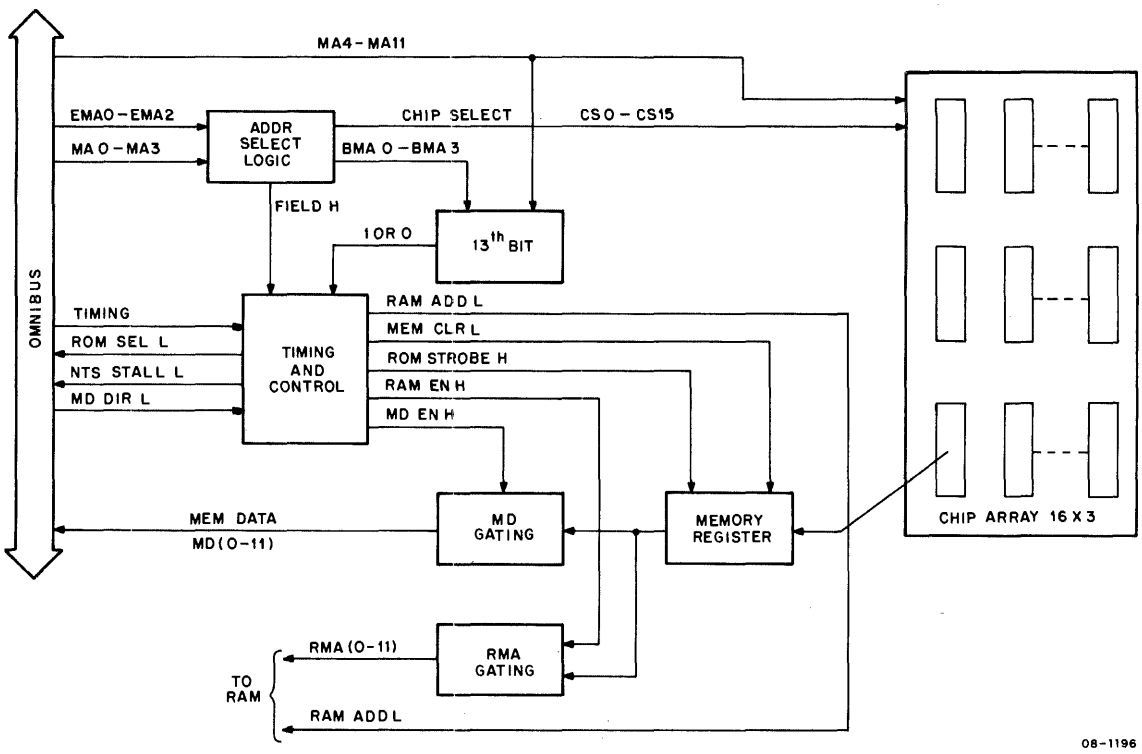
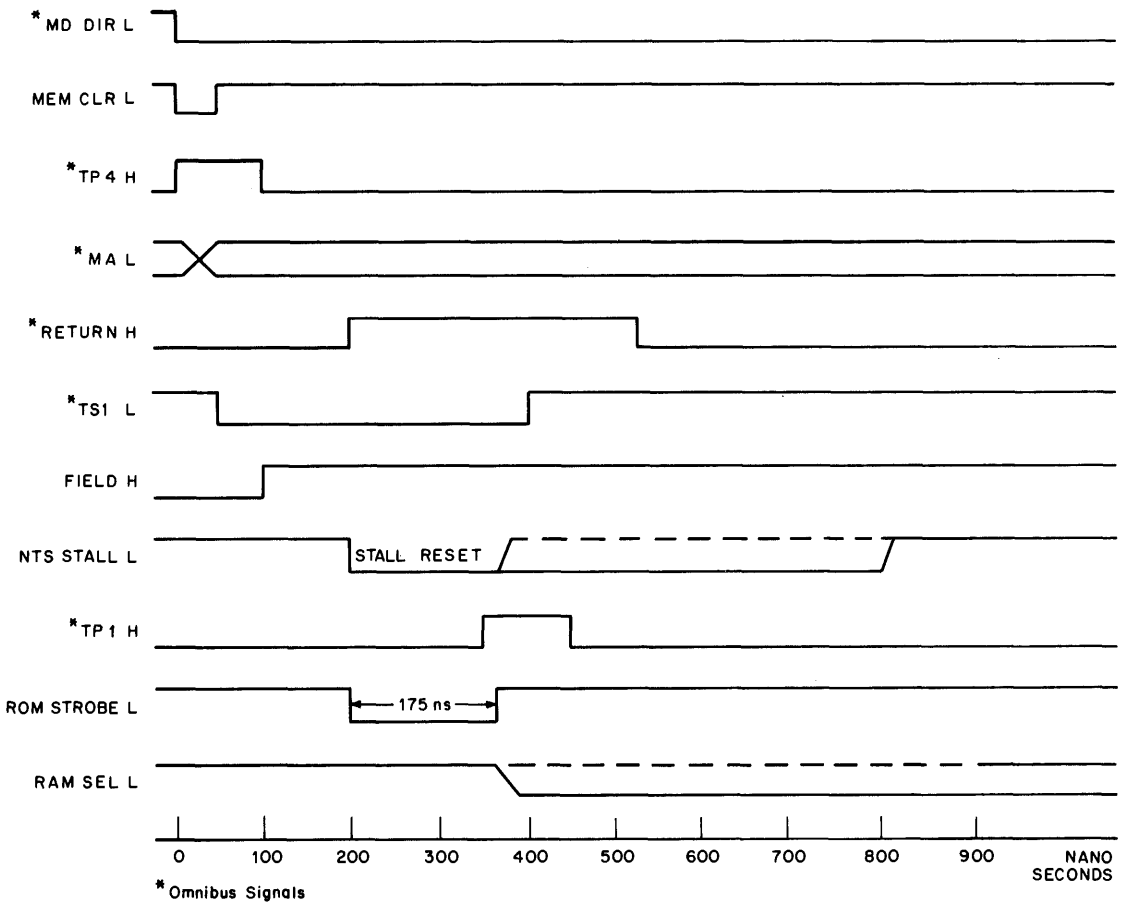


Figure 5-3 ROM Block Diagram

Table 5-2
MR8-A Signal Definitions

Signal Name	Description
RAM SEL L	An enabling signal for the RAM transmitted through the E Connector.
RMA0 L – RMA11 L	Twelve RAM address lines leading to the RAM through the E Connector, and equivalent to the MA0–MA11 lines of the Omnibus.
ROM STROBE H	Clocks ROM memory register contents onto the MD or RMA lines.
MEM CLR L	Clears ROM memory register.
FIELD H	Asserted when the memory field and memory size have been selected. Used to enable the timing and control logic.
CHIP SELECT	16 signal lines, one for each column of three chips in the 16 X 3 memory array, are selected by the address decode logic.
MD EN H	A gating signal generated in the control logic. Directs the register data to the MD lines (ROM cycle).
RMA EN H	A gating signal generated in the control logic. Directs the register data to the RMA lines (ROM/RAM cycle).
BMA (0–3)	Four signals derived from the corresponding MA <0–3>. Used to generate the 13th bit (Figures 5-3 and 5-7).



NOTE: If the 13th bit is set, RAM SEL L will be asserted and the STALL L line will not be released at the end of STROBE L. The NTS STALL line will be held by the MR8-A for 400–800 ns by which time the MS8-A will have asserted NTS STALL and taken control of the cycle.

08 -1183

Figure 5-4 ROM Timing Diagram

The ROM chips have a fast enough access time (80 ns) to be compatible with the READ time and the total memory cycle time provided by the processor. However, when operating with the RAM additional time is required, first because the RAM chips are slower, and second, because of the delays due to switching from one circuit to the other. A longer memory cycle time must be generated. This involves disabling the normal processor timing and activating another timing chain. The new timing chain is located on the RAM module, M8311. However, the circuitry for initially stopping the processor clock is part of the ROM module. This circuitry asserts NTS STALL and stalls the processor at the next time state. Besides the capability to initiate STALL, the circuitry can also override STALL and return to normal processor timing.

5.2.3 Input and Output Signal Definition

The MR8-A utilizes signals that originate in the central processor and in other modules of the PDP-8/A. In addition, the ROM generates signals for the operation of the RAM. The Omnibus signals are as follows:

1. MA 0-11 L
2. MD 0-11 L
3. EMA 0-2 L
4. TS1 L
5. MD DIR L
6. NTS STALL L
7. TP4 H
8. ROM ADDR L
9. POWER OK H
10. RETURN H

The Omnibus signals are completely defined in Chapter 3.

Signals generated by the MR8-A are defined in Table 5-2.

5.3 PROGRAMMING

The ROM chips are programmed electrically using the fusible link technique. Initially all bits of the ROM are in the 0 state. Information is introduced by selectively programming 1s in the proper bit locations. In addition, the chips that make up the 13th bit must be a 1 in each address location that is allocated for write operations in the ROM-RAM configuration. That is, all locations that will be modified during the execution of a program must be flagged. In this category are instructions requiring a write operation such as DCA, ISZ, and JMS, as well as locations used as autoindex registers, and those reserved for the programming of peripherals.

5.3.1 Programming Operation

In programming, the address selection is accomplished by means of the same decoding circuitry used in the read mode. A high voltage is applied to the four output pins, the Vcc, and Chip Set 1 Sel 1 terminals, to physically alter a fusible nichrome link. The voltage pulses are approximately 48 V. To isolate these from the board circuitry, the chip contacts that are used during programming are brought out to three top connectors (F, H, and J) using the fingers on one side of the board only.

The connections to the board logic are made to the corresponding fingers on the opposite side of the board. During normal operation, single width connectors join the contacts on both sides of the board. However, during programming, the connectors are removed and three cables from the programmer (blaster) are attached to the module. These cables have special connectors that make contact with the fingers on one side only – the chip terminal side. Additional protection to the circuitry is provided by a series of switches that are opened during programming (Paragraph 5.5.)

5.3.2 Programming Procedure

The programming of the ROM involves generating a paper tape containing the ROM pattern and then writing this pattern into the ROM using a computer controlled blaster. The MR8-SA blaster is a special facility available at Digital for programming simultaneously all the chips on the board. Detailed description of both hardware and software aspects of this facility are found in the *PDP-8/A Miniprocessor Handbook*. However, a brief summary of the procedures used is included here to complete the presentation.

5.3.2.1 Preparation of the Paper Tape – In the preparation of the paper tape, the locations requiring a write function are flagged. As an example, let one such instruction in the program (at location 200) be:

1. 200/DCA 250	Write accumulator contents into Location 250.
2. 250/(1) 1000	Location 250 in ROM is flagged. It contains RAM Address 1000.
2a. 250/DWRITE 1000	Assembler statement for tagging writable Location.

In a core program, line 1. would be all that is required. When using the ROM-RAM combination, both line 1. and 2. are needed.

A patch has been developed for the PAL 8 assembler to transform core type programs into a format required by the ROM-RAM combination.

The writable locations in ROM are tagged using the DWRITE statement. The RAM addresses are specified. The assembler then generates a paper tape in the format used by the MR8-SA ROM programmer, which will program the appropriate 13th bits. The format for the MR8-SA tape is shown in the *PDP-8/A Miniprocessor Handbook,* Chapter 11. The 12-bit data word, in this case the address in the Read/Write memory, is punched as a normal data word, but in the second line of the data word, hole 7 is punched to signify to the programmer that the 13th bit for this address should be set.

5.3.2.2 Blasting – The paper tape is loaded into a PDP-8/A computer that operates the blaster. An 8K memory is required. The entire board is blasted at one time instead of individual chips.

5.4 DETAILED LOGIC DESCRIPTION

The block diagram in Figure 5-3 should be used to understand the relationship between the blocks of logic and the signals that are generated by these blocks. Table 5-2 defines these signals. All Omnibus signals are defined in Chapter 3.

5.4.1 Addressing Block Diagram Description

The addressing section of the MR8-A accesses 4096 separate memory locations in the standard ROM by means of 12 memory address lines (MA<0:11>) and 3 Extended Memory Address lines (EMA <0:2>).

In addition, one 4K field must be selected from among 8 using 3 EMA lines of the extended memory control circuit. The 13th bit logic is closely linked with the address circuitry. The detailed block diagram of the address select logic, Figure 5-5 shows these functions.

The eight least significant lines MA<4:11> are decoded by a circuit which is an integral part of the chip. One of 256 locations is thus selected.

Address lines MA<0:3> are used to generate 16 chip enable signals that are routed to the 16 X array of chips. Each of the 16 lines activates three chips arranged vertically on the board. Since each chip has 4 bits per word, a 12-bit word is addressed. The total number of words accessed is 256 X 16 or 4096.

The MR8-A field select switch settings are compared with the EMA inputs to select the field. Field size is decoded by means of a similar circuit. The output of this field circuit is an enabling signal FIELD H which allows the selection of this field of memory.

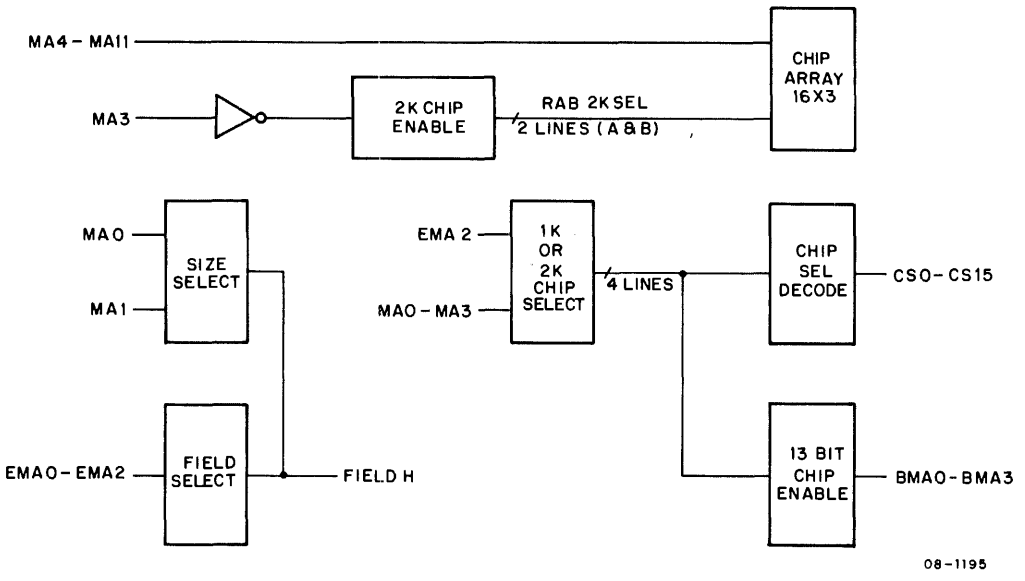


Figure 5-5 Detailed Block Diagram of Address Select Logic

5.4.2 Field and Size Selection

The MR8-A is a 1K, 2K, or 4K memory that can be located at any 4K boundary at a 32K memory array, i.e., it must start at address zero of one of eight 4K memory fields. The field selection logic is shown in Figure 5-6.

Three switches (S2-6, S2-3, and S2-7) and a comparator circuit consisting of three Exclusive-NOR gates with their outputs tied together decode the Memory Extension address on lines EMA<0:2>.

The output signal FIELD H is true only if each one of the inputs from the switch settings matches that of the corresponding EMA line, e.g., if EMA0 is low, switch S2-7 must be closed. The output of the corresponding Exclusive-NOR gate is a high and all other switch setting inputs must similarly correspond to their respective EMA line.

A table of memory fields vs switch settings is shown in Table 5-3.

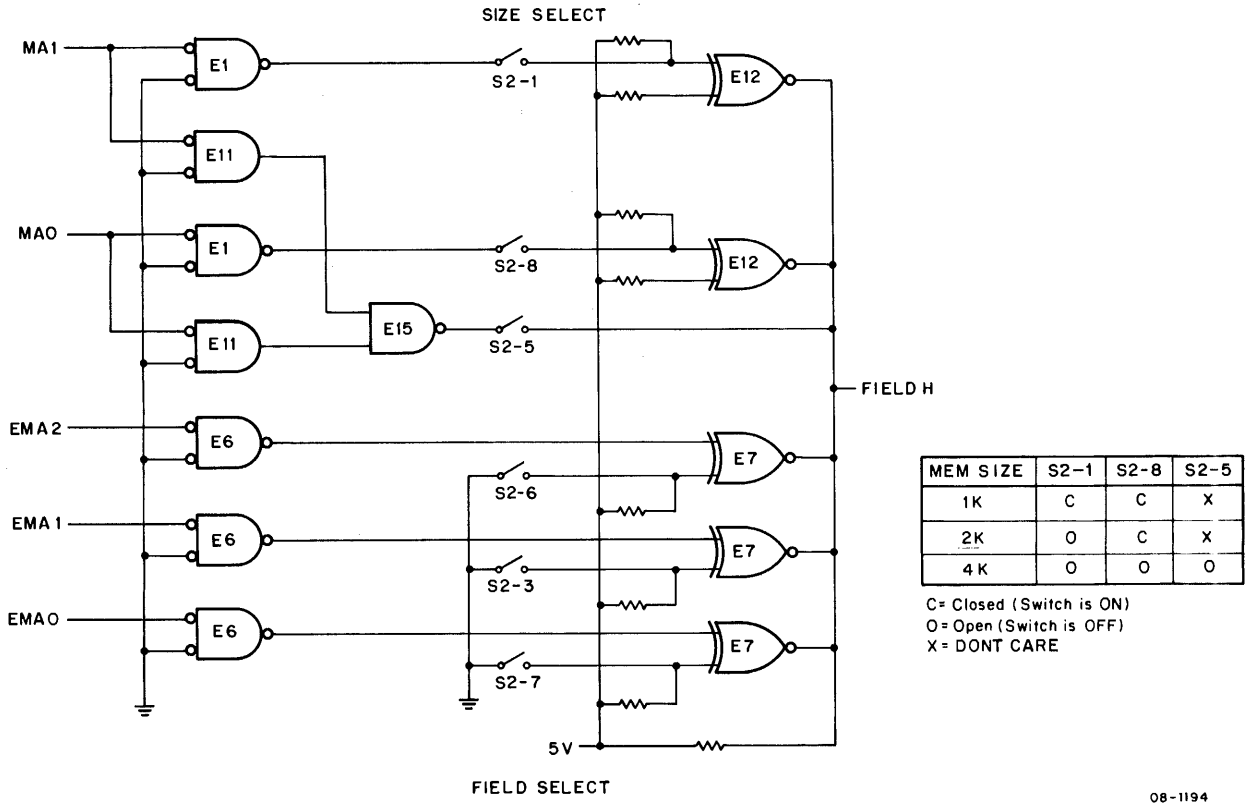
Each Field has an address range of 4K. Field 0, as an example, is composed of addresses 0-7777(8). A full complement of 1K chips on the MR8-A will start at address 0 and end at the 4K boundary of the field.

A similar arrangement of NOR gate comparators and switches selects the proper size. The two most significant address lines MA0 and MA1 are utilized for this purpose.

The states of these lines for the respective field sizes are shown in Table 5-4.

The switch settings that correspond to the states of MA0 and MA1 are shown in Table 5-5.

The memory size selection circuit and the field selection circuit constitute a combined five bit comparison network shown in Figure 5-6 that generates FIELD H, which, in turn is gated to produce the enabling signal ROM ADD L.



MEM SIZE	S2-1	S2-8	S2-5
1K	C	C	X
2K	O	C	X
4K	O	O	O

C = Closed (Switch is ON)
O = Open (Switch is OFF)
X = DONT CARE

Figure 5-6 Field and Size Selection

Table 5-3
Switch Setting to Select Memory Field

Field	Switch Settings		
	S2-6	S2-3	S2-7
0	O	O	O
1	C	O	O
2	O	C	O
3	C	C	O
4	O	O	C
5	C	O	C
6	O	C	C
7	C	C	C

O = Open (Switch is OFF)
C = Closed (Switch is ON)

Table 5-4
MA0 and MA1 States for Memory Field Sizes

ADDR Line	MEM Size		
	1K	2K	4K
MA0 L	0	0	X
MA1 L	0	X	X

Logic 0 is HI
X = Doesn't Matter

Table 5-5
Switch Settings for States MA0 and MA1

MEM Size	Switch		
	S2-1	S2-8	S2-5
1K	C	C	X
2K	O	C	X
4K	O	O	O

C = Closed (Switch is ON)
O = Open (Switch is OFF)
X = Doesn't Matter

5.4.3 Chip Select Decoder

The address decoding circuit provides for the utilization of a 1K (256 X 4) chip. In the 1K chip, the 8 least significant address bits (MA4 to MA11) are routed directly to the chip.

The four most significant bits, MA0 to MA3, are decoded to generate the 16 chip select signals CS0 to CS15 for the 16 X 3 chip array.

The decoding network is shown in Figure 5-7. Address lines MA0 to MA3 are routed via one side of the AND-OR gates to two 4 to 8 decoders (IC7442) to generate 16 chip select lines. Each chip select line represents 256 words.

The address decoding scheme is shown in Table 5-6.

5.4.4 The 13th Bit

The same type memory chip is used in the 13th bit as in the other 12 bits of the memory array. However, the chips are organized in a 256 X 4 matrix for a total of 1024 bits. To be useful as a 13th bit a transformation of the 256 X 4 into 1024 X 1 matrix is required. A 4 to 1 multiplexer, IC 74153, is used for this purpose as shown in Figure 5-8.

The MA2 and MA3 lines are used to strobe the Multiplexer. The four combinations of the two lines and their corresponding address ranges are shown in Table 5-7.

The output of the multiplexer has an address range of 1K.

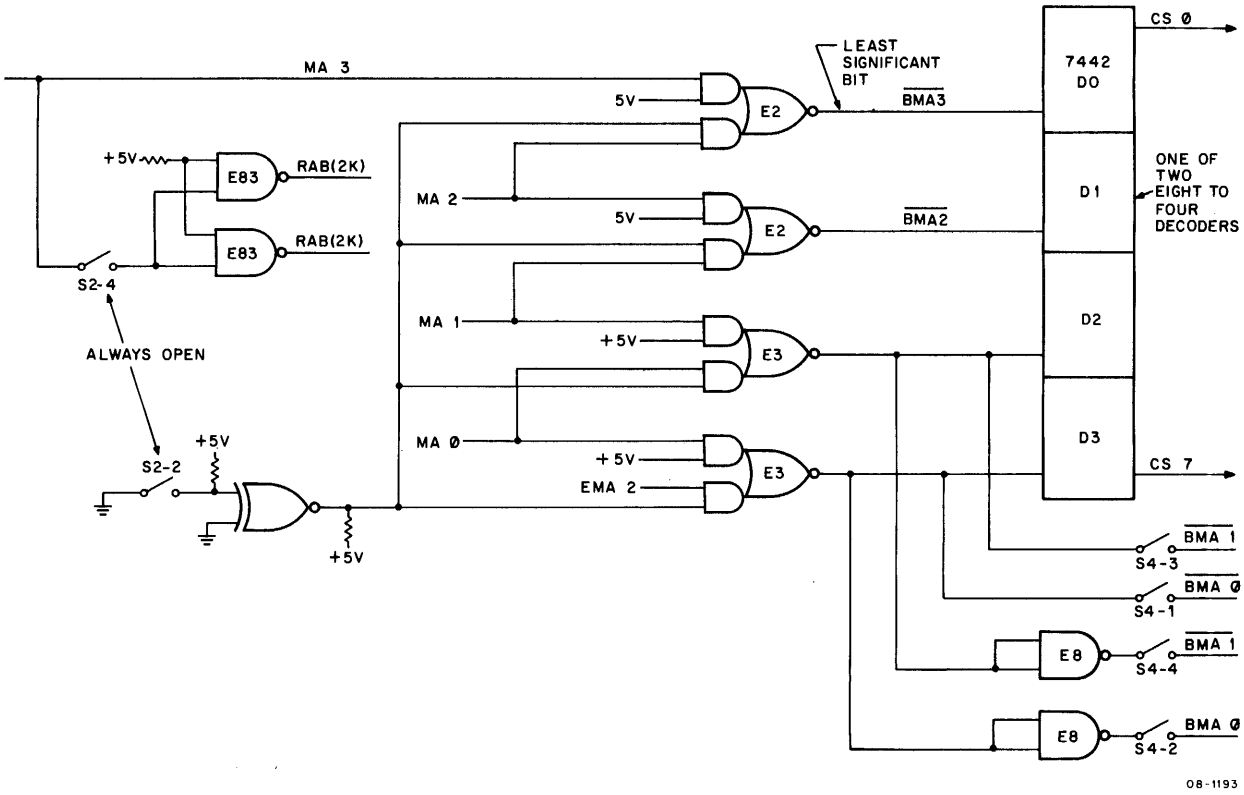


Figure 5-7 Chip Select Decoding

Table 5-6
Address Decoding

Address Lines	MSB 0	1	2	3	4	5	6	7	8	9	10	LSB 11
Bit Value	2048	1024	512	256	128	64	32	16	8	4	2	1
	Decoded on one of two ICs (7442)					Decoded on Chip						

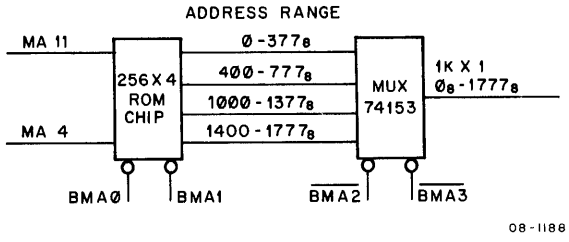


Figure 5-8 13th Bit Mapping into 1K X 1 Array

Table 5-7
States of MA3 and MA2 to Select an Address Range

MA3	MA2	Address Range
0	0	$0 - 255\ (0 - 377_8)$
1	0	$256 - 511\ (400 - 777_8)$
0	1	$512 - 767\ (1000 - 1377_8)$
1	1	$768 - 1023\ (1400 - 1777_8)$

To obtain a 4K address range (4K words one bit wide), four such Chip-MUX assemblies are used and the most significant bits MA0 and MA1 are used (Figure 5-9).

The output of this configuration is 1 bit, the 13th bit, with an address range of 4K, which in turn is used as key control element of the ROM.

5.4.5 Timing and Control

The Timing and Control Logic of the MR8-A is shown in Figure 5-10. It contains two timing one-shots and two control flip-flops.

One timing element asserts NTS STALL L and the other generates the ROM STROBE signal which clocks the control flip-flops and the memory register.

Switch S6-1 grounds the 13th bit. All inputs to the control flip-flops are 0 and therefore the output is a ROM output. This switch permits isolation of the ROM during trouble shooting.

S4-7 is closed and S4-8 is opened when there is no writable memory, and ROM operates in the read-only mode. The switch settings are reversed, S4-8 closed and S4-7 open when the mode of operation is ROM-RAM. A complete list of switch settings is found in Paragraph 5.5.

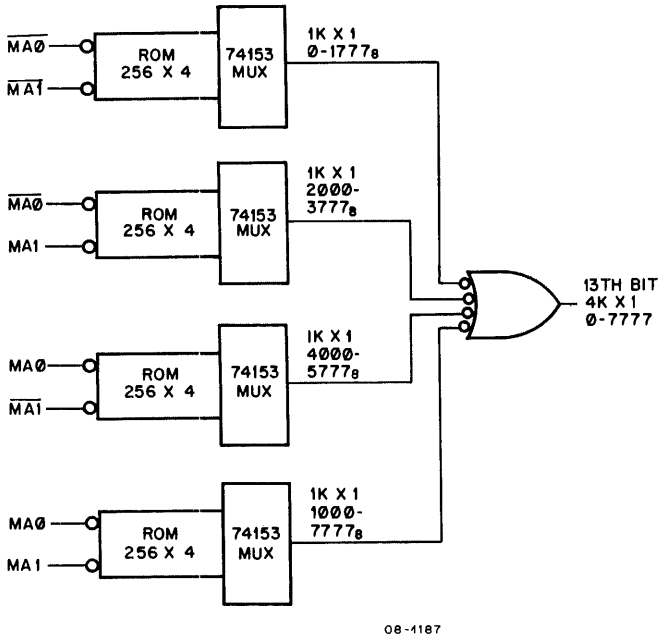


Figure 5-9 13th Bit Mapping into 4K x 1 Array

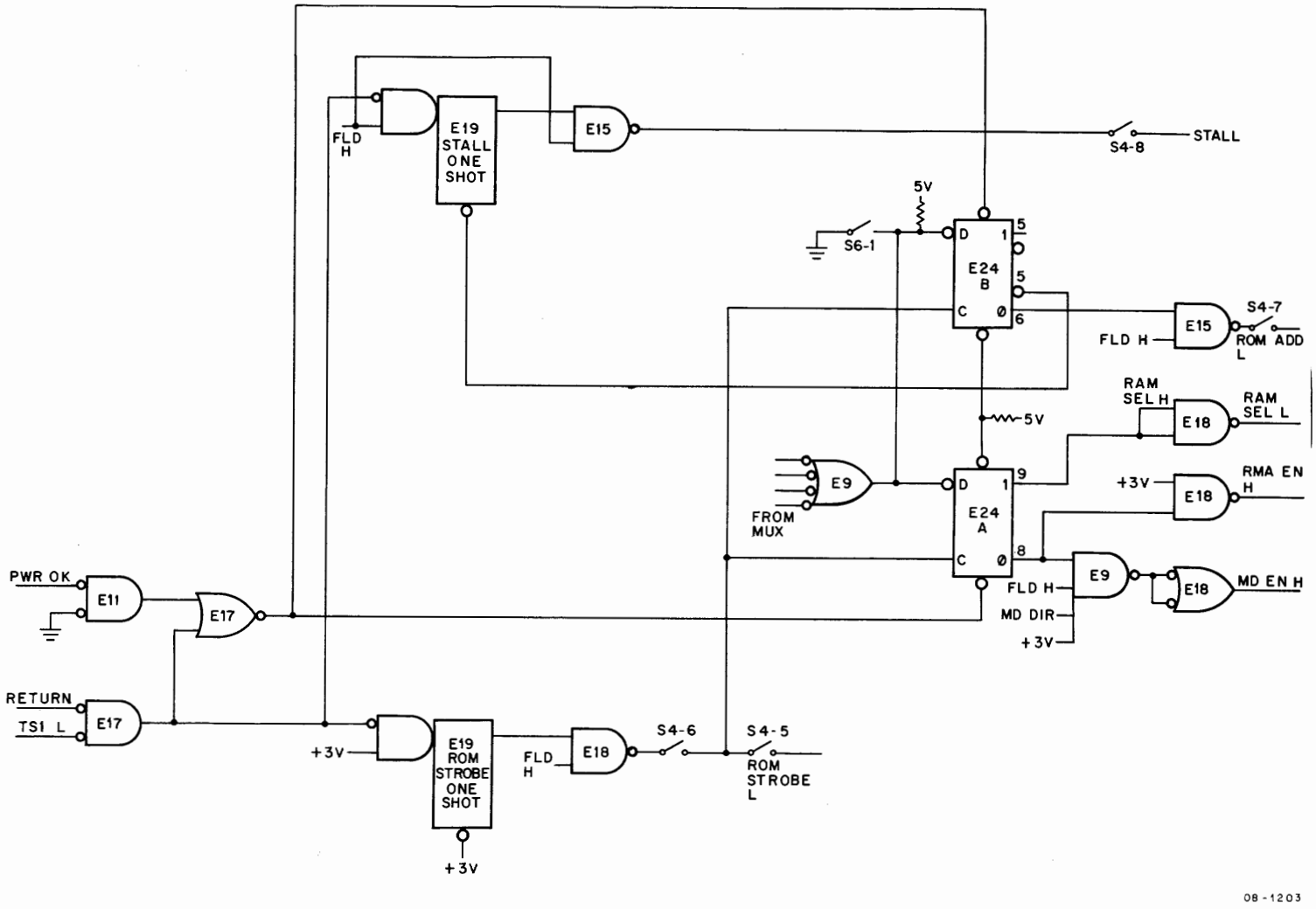


Figure 5-10 Timing and Control Logic

5.4.6 Timing Generation

The STALL one-shot has a delay of 600 ± 200 ns. It is triggered when the Omnibus signal RETURN H goes high and is gated with FIELD H which is asserted when a valid selection is made by the memory field and size select circuits. STALL is asserted immediately and is maintained for the duration of the pulse 600 ± 200 ns unless overridden by a Reset generated in the STALL control flip-flop. The conditions for aborting STALL will be explained in a subsequent paragraph that discusses the utilization of the timing pulses in the control scheme.

The STROBE one-shot is triggered at the same time as the STALL one-shot, i.e., when RETURN H goes high. The pulse duration is 175 ± 25 ns. The output is gated with FIELD H (for the same reason as is the STALL one-shot) and inverted by the NAND gate E-18. A positive pulse used to clock the two control flip-flops and the ROM memory register appears at the end of the timed delay.

5.4.6.1 Control Flip-Flops – The two control flip-flops shown in Figure 5-10 are used to generate the control signals. The D input to both is the 13th bit and they are both clocked by the STROBE one-shot. The output, after inversion, of the lower flip-flop when the data input is high (13th bit = 1), is RAM SEL L. RMA EN H is asserted gating the data to the RAM address lines. Both signals are used in the ROM-RAM cycle.

When the data input is a low (13th bit = 0) the output after inversion is RAM SEL H (not a RAM cycle) and MD EN H is asserted enabling the MD lines routing memory data to the processor. The output of the STALL Control flip-flop resets the STALL one-shot. When the data input is a low (13th bit = 0) and ROM ADD L is asserted the stall reset permits ROM to continue operation in a read only mode while ROM ADD L disables other Read-Write memories, RAM among others.

5.4.6.2 Sequence of Control Operations – The sequence of the control operations is shown in the two timing diagrams (Figure 5-4 and 5-11).

Refer to the timing diagram in Figure 5-11. NTS STALL L is asserted at RETURN time regardless of whether it is ROM or ROM-RAM cycle (point 1). At STROBE time (point 2), a decision is made whether to continue or abort STALL. This decision is made by the STALL control flip-flop in response to the 13th bit data input, if pin E24-5 is low resetting the STALL one-shot (point 3). Simultaneously, MD EN H (Pin E24-8) is asserted (point 4). When it is a ROM-RAM cycle, STALL is continued and RAM is selected.

5.4.6.3 Initial Conditions – It should be noted that initally the two control flip-flops are set in opposite states. The STALL flip-flop is set (pin 5 high) during a RAM cycle. The other flip-flop is in the reset condition (pin 8 high) during a ROM cycle. So both the ROM and RAM cycles are "armed." When the selection is made at ROM STROBE, one fires and the other is disarmed. This is shown graphically in the timing diagram (Figure 5-11). This decision does not take place instantaneously. Pulling and releasing NTS STALL requires a time delay of approximately 80 ns. The memory cycle then is 1.6 μs instead of the normal 1.5 μs.

5.4.6.4 Single Stepping – In the single step mode of operation, MEM CLR L is enabled. Initially this clears the memory register and all register flip-flop outputs to the gates go to zero, enabling the MD or the RMA lines.

If it is a ROM cycle RAM SEL H is high at the beginning of TP4 and E15 asserts MEM CLR L (Figure 5-12); therefore, the memory register will be cleared immediately.

The data on the MD lines comes from two sources, the ROM and RAM registers. The ROM register is cleared immediately to make sure that valid data is placed on the MD lines in case the current cycle is a ROM cycle. Should it turn out to be a RAM cycle, the initial output on the lines will be 0s until the RAM data appears. Because of the inherent delay in the RAM cycle no valid data will be lost.

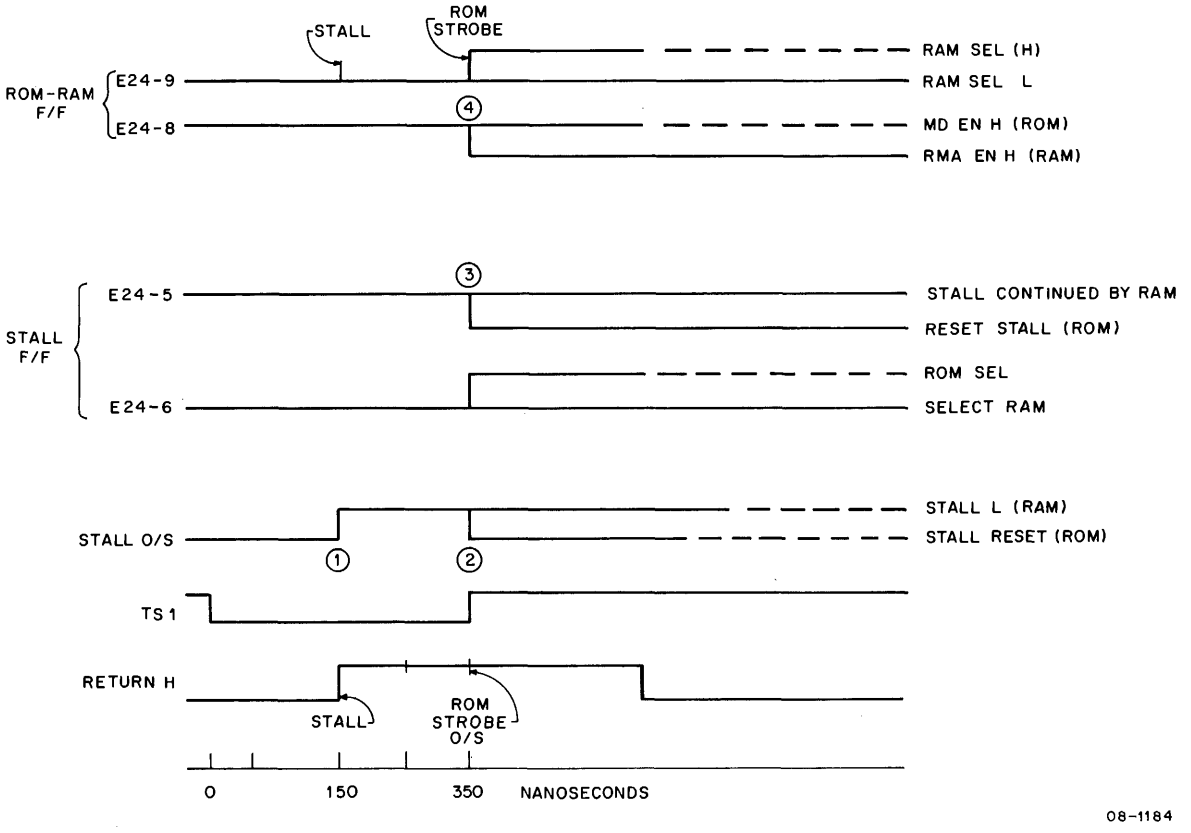


Figure 5-11 ROM-RAM Selection Timing

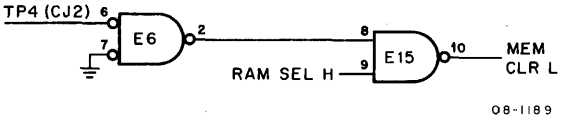


Figure 5-12 Single Step Operation

5.4.7 Memory Data and Memory Register

The first 1K block of the 4K ROM memory shown in Figure 5-13 is typical of all 4 1K blocks.

It consists of:

1. Twelve preprogrammed chips, arranged in a 4 X 3 array
2. Address and chip enable inputs,
3. A memory output register that accepts the data content of the memory chips, and
4. Transfer lines to the processor (MD lines) and RAM memory (RMA lines).

These are described in the following paragraphs. The physical layout of the chips on the board is shown in Figure 5-14.

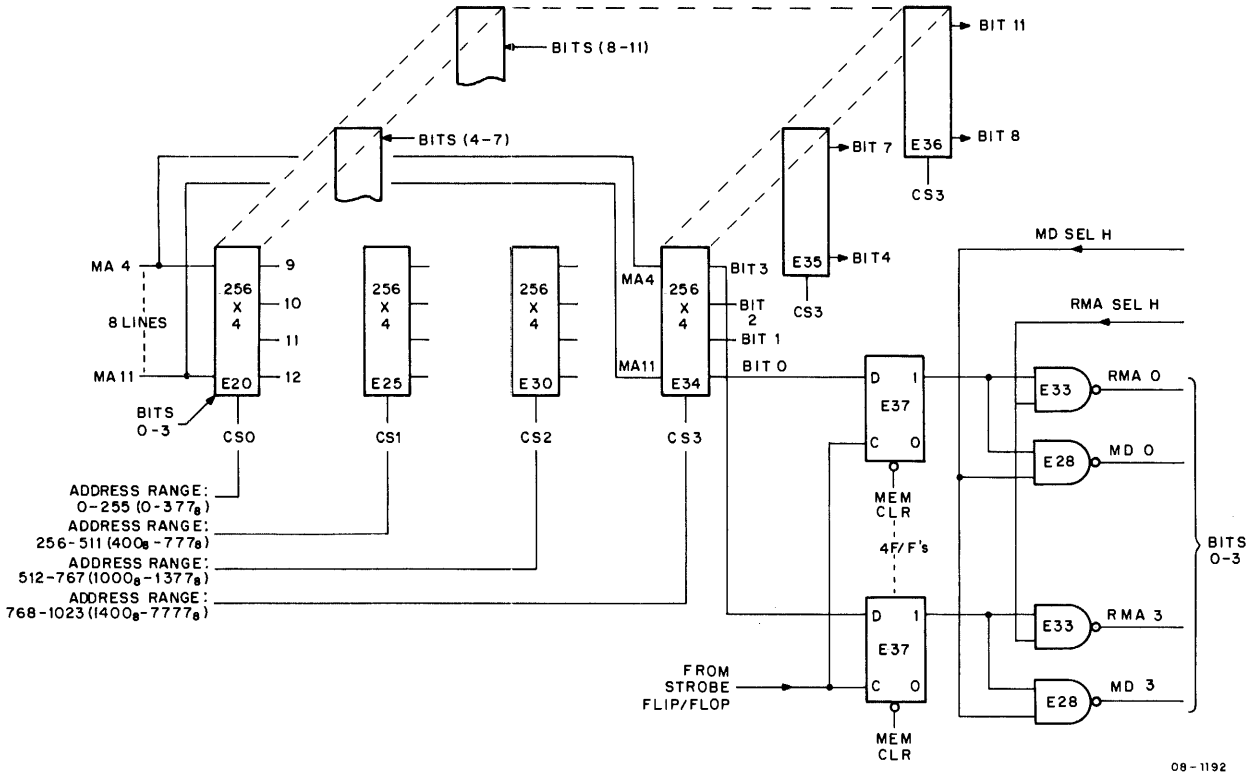


Figure 5-13 Arrangement of 1K Memory

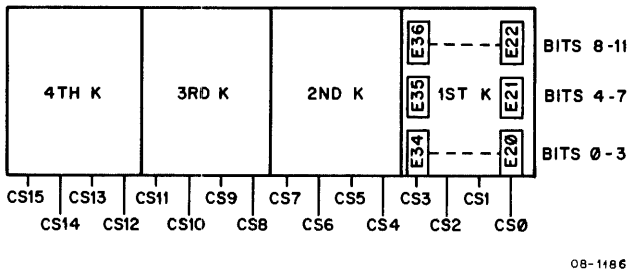


Figure 5-14 ROM 4K Memory – Physical Layout of Module

5.4.7.1 Memory Chips – The semiconductor chips are the storage elements of the ROM memory. Basically they can be programmed electrically after they are mounted on a module. Three of the four top connectors on the module F, H, and J, provide access to circuit elements on the chips that can either be shorted or opened by the application of a high voltage to selected connector pins. This introduces either a logical one or zero into the selected memory cells. Two techinques are available for programming the memory chips after they have been mounted on the module: – fusible link and avalanching. In general, a high voltage or current pulse alters the internal circuitry of the chip providing either a new current path or opening an existing one.

The individual chips are mounted on sockets for easy replacement and reprogramming in the event of failure or error.

5.4.7.2 Address and Chip Enable Inputs – Eight address lines (MA<4:11>) are decoded on the chip and select one of 256 locations. The chip select lines select one of four chips in a 1K block. Each chip is organized as 256 words by 4 bits. Three chips are required for a 12 bit word.

5.4.7.3 Memory Output Register – The memory output register consists of 12 flip-flops (74175's) one for each bit in the memory chip, i.e., four flip-flops per chip and 12 for each memory location. The output of the register is routed to the MD or RMA lines by the STROBE pulse described above.

5.4.7.4 Data Transfer Lines – Routing the memory register contents is controlled by the gating signals MD SEL H and RMA SEL H which originate in the Control and Timing section. In the event MD SEL H is asserted the memory contents are placed on the MD lines. When RMA SEL H is asserted the memory data is routed out on the RMA lines.

5.4.7.5 Physical Layout – The physical layout of the memory is shown in Figure 5-13. It consists of four 1K blocks described in the preceding paragraphs. Each 1K block consist of 12 chips arranged in an 4 X 3 array. The least significant address is on the right and the most significant on the left. The four least significant bits are on the bottom.

5.5 MR8-A SWITCH LIST

The following is a list of the settings for the various switches on the MR8-A: They are listed in numerical order for easy reference. Switches are open for normal operation unless noted.

S1	SW1 - SW8	OPEN FOR PROGRAMMING CLOSED FOR OPERATION
S2	SW1 - SW8	OPEN FOR PROGRAMMING
	SW1	MEM SIZE - CLOSED FOR 1K, OTHERWISE OPEN
	SW2	ALWAYS OPEN
	SW3	FIELD SEL - CLOSED FOR FIELD 2, 3, 6, 7
	SW4	ALWAYS OPEN
	SW5	MEM SIZE - OPEN
	SW6	FIELD SEL - CLOSED FOR FIELD 1, 3, 5, 7
	SW7	FIELD SEL - CLOSED FOR FIELD 4, 5, 6, 7
	SW8	MEM SIZE - OPEN FOR 4K, OTHERWISE CLOSED
S3	SW1 - SW8	OPEN FOR PROGRAMMING CLOSED FOR OPERATION
S4	SW1 - SW8	OPEN FOR PROGRAMMING
	SW1 - SW4	CLOSED FOR OPERATION
	SW5 - SW6	TEST ONLY - CLOSED FOR OPERATION
	SW7	ROM ADDR - CLOSED IF USED AS ROM WITHOUT READ/WRITE MEMORY
	SW8	STALL - CLOSED IF USED WITH READ/ WRITE MEMORY
S5	SW1 - SW8	OPEN FOR PROGRAMMING CLOSED FOR OPERATION
S6	SW1 - SW2	OPEN FOR PROGRAMMING CLOSED FOR COMPLETE ROM COMPARE
	SW3 - SW8	OPEN FOR PROGRAMMING CLOSED FOR OPERATION

S7	SW1 - SW8	OPEN FOR PROGRAMMING CLOSED FOR OPERATION
S8	SW1 - SW8	OPEN FOR PROGRAMMING CLOSED FOR OPERATION
S9	SW1 - SW8	OPEN FOR PROGRAMMING CLOSED FOR OPERATION

SECTION 2
RANDOM ACCESS MEMORY (RAM)

5.6 SEMICONDUCTOR RANDOM ACCESS MEMORY (RAM-MS8-A) DESCRIPTION

The Random Access Memory (RAM), MS8-A, is one of three types of semiconductor memories that are available for the PDP-8/A. The others, the ROM (Read Only Memory), MR8-A, and the PROM, MR8-FB, are described in Sections 1 and 3 respectively.

Physically the RAM memory is a quad module (M8311), 10 X 8-1/2 inches in size. The basic building block is a static MOS chip which contains 1K X 1 bit storage cells organized in a 32 X 32 (1024 bits) matrix. In addition, address decoding circuitry is an integral part of each chip. Twelve of these building blocks comprise a 1K X 12 bit memory.

The memory size can be increased in increments of 4K up to 32K. However, power requirements listed in Paragraph 5.2.3 must be considered. Standard size MS8-A options are 1K, 2K, and 4K.

The static MOS is inherently slower than the processor memory cycle of 1.5 μs. The RAM Read/Write cycle takes 2.8 μs and a Read only cycle takes 2.4 μs.

The RAM provides a Write capability for the otherwise Read only ROM. This is accomplished by indirect addressing, i.e., when certain ROM locations are addressed they point to (Go To) RAM. Details of the RAM-ROM combined operation are described in subsequent paragraphs.

Another feature is the ability of the relatively small RAM to operate in a large PDP-8/A memory field – as large as 32K. The addressing circuitry provides the capability of positioning the small RAM, 1K to 4K, at specific locations in this field. However, RAM cannot be in the same field as a core memory.

The RAM memory operates on 5 Vdc and draws approximately 3 A independent of its state of activity. Power must be ON to preserve the programmed contents. Protection against momentary power failure is incorporated in the power supply circuitry. A battery is used to supply power for the MS8-A when ac power is lost for short periods. Intervals of power loss up to 40 seconds can be tolerated, however, should longer power failures occur, the RAM program must be reloaded.

5.6.1 Physical Description

The MS8-A RAM memory is packaged on one standard quad module, the M8311. The four bottom connectors (A, B, C and D) plug into the Omnibus. In addition, one connector (E) at the top provides interconnection with the ROM module (M8312). The MS8-A module is shown in Figure 5-15.

The ROM-RAM configuration is shown in Figure 5-2.

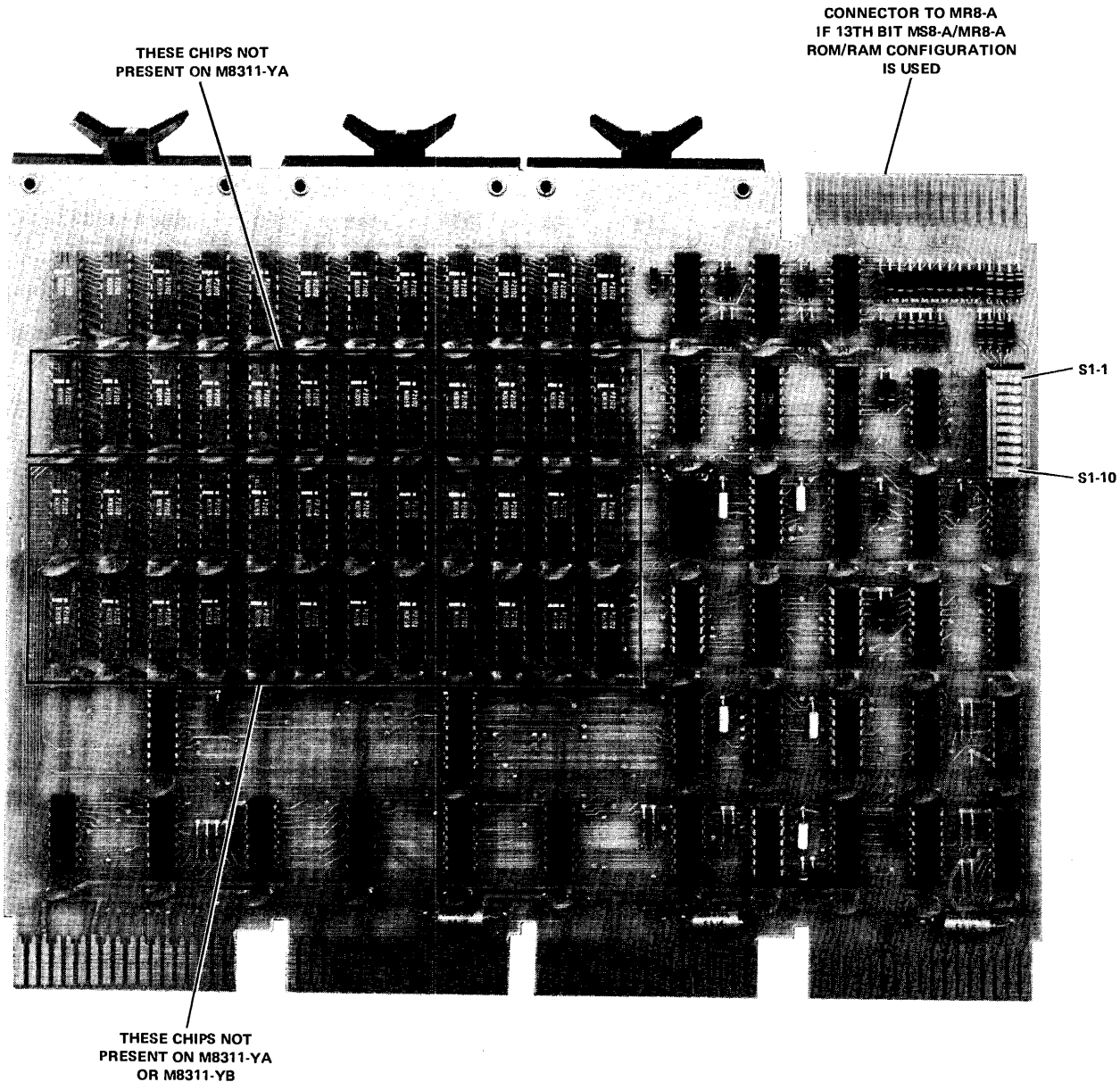


Figure 5-15 RAM MS8-A Module M8311

5.6.2 MS8-A Specifications

The MS8-A Specifications are listed in Table 5-8.

5.7 FUNCTIONAL DESCRIPTION

The MS8-A RAM can operate in either of two modes: – As a mainframe memory or as an auxiliary write memory for the ROM. The basic memory structure to implement the functions of address selection, timing and storage are discussed in the following paragraphs.

The overall functional block diagram is shown in Figure 5-16. The blocks to the right of the Omnibus are located on the M8311 module; those blocks to the left, such as ROM MR8-A, provide signal inputs to the RAM memory but are not physically part of the M8311. The circuit elements on the module can be conveniently grouped on the basis of their function into four major blocks:

1. Address Select Logic
2. Timing and Control
3. Chip Array
4. Memory Data.

By looking at the input and output signals of these blocks we can get an overview of their operations.

5.7.1 Address Select Logic

The Address Select logic performs many functions. First it establishes the mode of operation of the RAM; either mainframe memory or an auxiliary write memory for the ROM – a ROM-RAM combination. The start of this selection is the signal RAM SEL L coming from the ROM. Second, it decodes the extended memory control field address. A unique address of one out of eight 4K fields is contained in the 3 EMA lines (EMA<0:2>). The address logic compares the 3-digit code with the field assigned to the RAM which is contained in three switch settings. The RAM may be in a different field than ROM and still be a scratch pad memory. Third, it selects, by comparing the settings of 2 switches with the two most significant address lines, MA(0:1)/RMA(0:1), the starting address at any 1K boundary within the 4K field. As an example a 1K memory can be assigned address ranges 0-1777(8), 2000-3777(8) etc., depending on the switch settings.

The results of a successful selection are the activation of the timing and control circuitry through MEM SEL L, and enabling signals to the chip select circuitry, EN<0:3>.

Table 5-8
MS8-A Specifications

Characteristic	Specification	
Power Requirements	**Typical**	**Worst Case**
1K	5 V ± 5% 1.4 A	2.4 A
4K	5 V ± 5% 3.5 A	4.6 A
Memory Cycle Time	**Fetch State**	**All Other States**
Mainframe Memory (RAM)	2.4 μs	2.8 μs
Scratch Pad Memory (ROM/RAM)	2.7 μs	3.1 μs
Memory Capacity	1K, 2K, 4K (expandable to 32K)	
Temperature	5 to 50° C	
Environment	Standard Computer Environment	

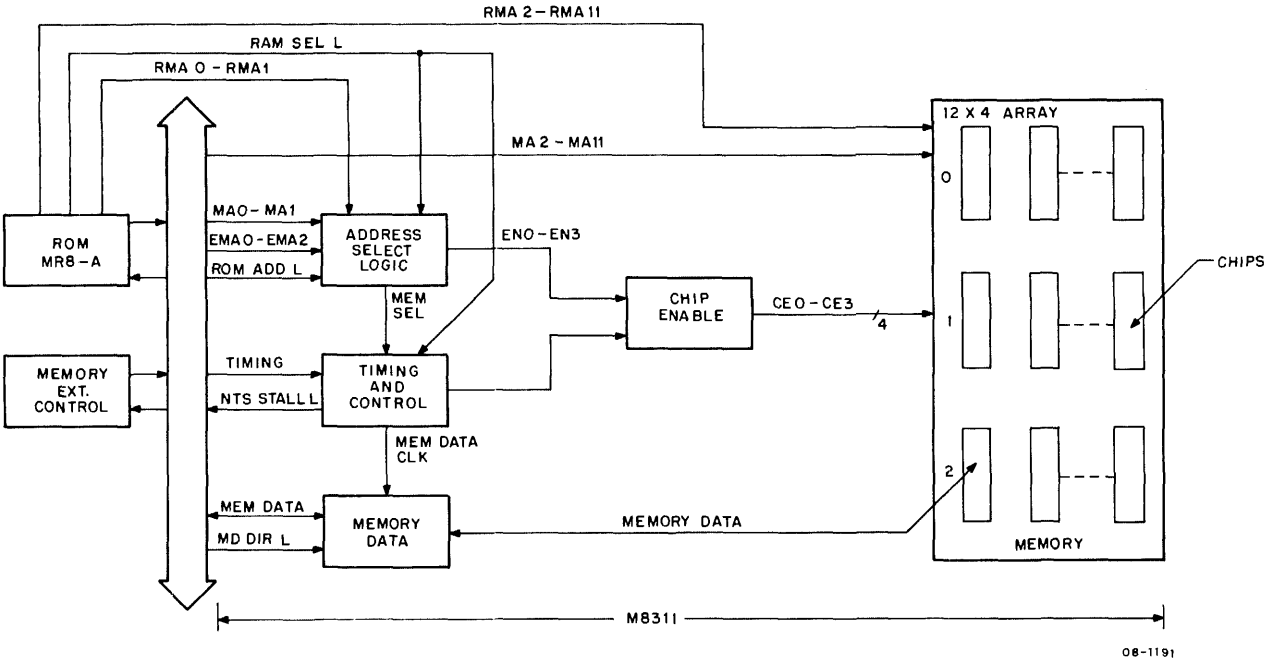


Figure 5-16 MS8-A Block Diagram

5.7.2 Timing and Control

The timing network is the second major logic block of the RAM module. The inputs are the basic processor clock signals listed in Table 5-9, the MEM SEL signal from the address select logic and RAM SEL L. It contains its own clock and control logic which generate the timing and control signals for the read and write operations of the memory.

The major problem is to fit in a longer memory cycle than the normal processor cycle. This involves stopping the processor clock during the read part of the cycle by assserting NTS STALL L and starting the memory clock. When the read operation is over, the RAM timing chain is deactivated and the processor clock is restarted. This is repeated during the second part of the cycle in all Major States except Fetch.

5.7.3 Memory Chip Array

The next major logic block is a 12 X 4 array of the 1K chips. These are N-channel static MOS devices organized in 1024 words X 1 bit.

Each chip has 1024 cells, each containing six transistors. Two are cross-coupled and act as the storage element; two function as loading elements similiar to resistors; the remaining two are gating devices for addressing each separate cell in the matrix. In addition to the memory array proper, the chip circuitry includes the following:

1. Address decoding
2. Sensing
3. Write
4. Chip enable logic.

Ten address terminals on the chip connect to the 10 least significant address lines, MA (2-11) or RMA (2-11), depending on the memory mode, mainframe or scratchpad for ROM. The lines are arranged in groups of five to select the cells for either reading or writing into.

Table 5-9
MS8-A Signal Descriptions

Signal	Description
FIELD H	Asserted when a valid field selection has been made. Used to enable the relative address selection logic.
MEM SEL L	Asserted when a valid address has been selected. Used to enable the MS8-A timing chain and the control flip-flops.
MEM DATA CLK	Clocks RAM memory register contents onto the MD lines.
CE L (3–0)	4 chip enable lines, one for each row of 12 chips that enable the chip logic.
EN (3–0)	4 outputs of relative address ROM (IC 8223) corresponding to the respective chip enable lines.

5.7.4 Memory Data

The memory data logic implements the transfer of data into and out of the memory cells. This involves the memory output register, timing signals from the timing and control logic, and an Omnibus signal, MEM DATA DIR L which controls the direction of the transfer into or out of the memory cell. When the MD DIR L signal is low, the transfer is out of the memory into the processor or a read operation. When the signal is high, the direction of data transfer is into the memory out of the processor or a write operation. The MD lines carry data, processor instructions, addresses, and operands as well as select and operation codes for I/O devices.

5.7.5 Operation

The sequence of events during the read part of a RAM cycle is shown in Figure 5-17.

The timing is shown on the left and proceeds from TP4 at the top starting the read cycle with a change in memory address and ending at TP2 at the bottom when the CPU takes the memory data.

The sequence of events for the write cycle is shown in Figure 5-18.

When operating as a scratchpad memory ROM-RAM cycle there is an additional delay of 300 ns in the decision by the ROM as to whether it is a ROM or ROM-RAM cycle (see Section 1 for details). The MS8-A timing chain is used to time out this initial delay. After 300 ns, the timing chain is reset and the rest of the timing proceeds as in the RAM cycle.

5.8 INPUT AND OUTPUT SIGNALS

The following signals are defined in Chapter 3.

MA 0-11 L	EMA 0-2 L
MD 0-11 L	FETCH L
MD DIR L	NTS STALL L
TS1 L	TS2 L
TP1 H	TP2 H
TP3 H	TP4 H
SOURCE H	ROM ADD L

The RMA 0-11 L and RAM SEL L signals are defined in Table 5-2.

The signals generated in the MS8-8A are defined in Table 5-9.

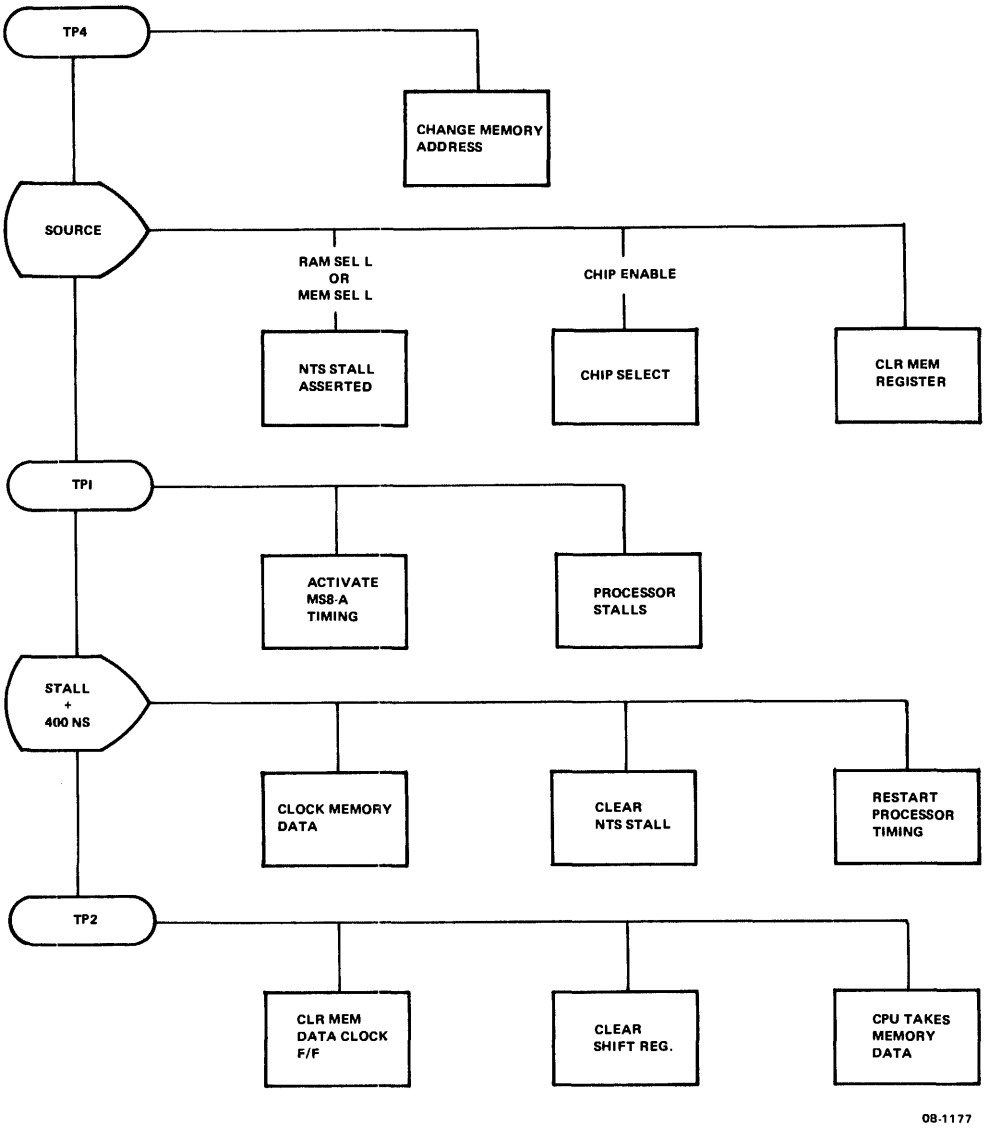


Figure 5-17 Read Cycle Flow Chart

5.9 PROGRAMMING

The programming of the RAM when operating alone, as a read/write memory, is the same as for a core memory. When operating in conjunction with the ROM, the programming involves a special procedure for programming the ROM. This is described in detail in Chapter 11 of the *Miniprocessor Handbook*.

5.10 DETAILED LOGIC DESCRIPTION

The block diagram (Figure 5-16) should be used to understand the relationship between the groups of logic. You should refer to flow diagrams in Figures 5-17 and 5-18 for the operation sequence during read and write operations. A detailed description of the logic is presented in the next paragraphs in the following order:

1. Address Selection Logic
2. Timing and Control Logic
3. Memory Data and Memory Register

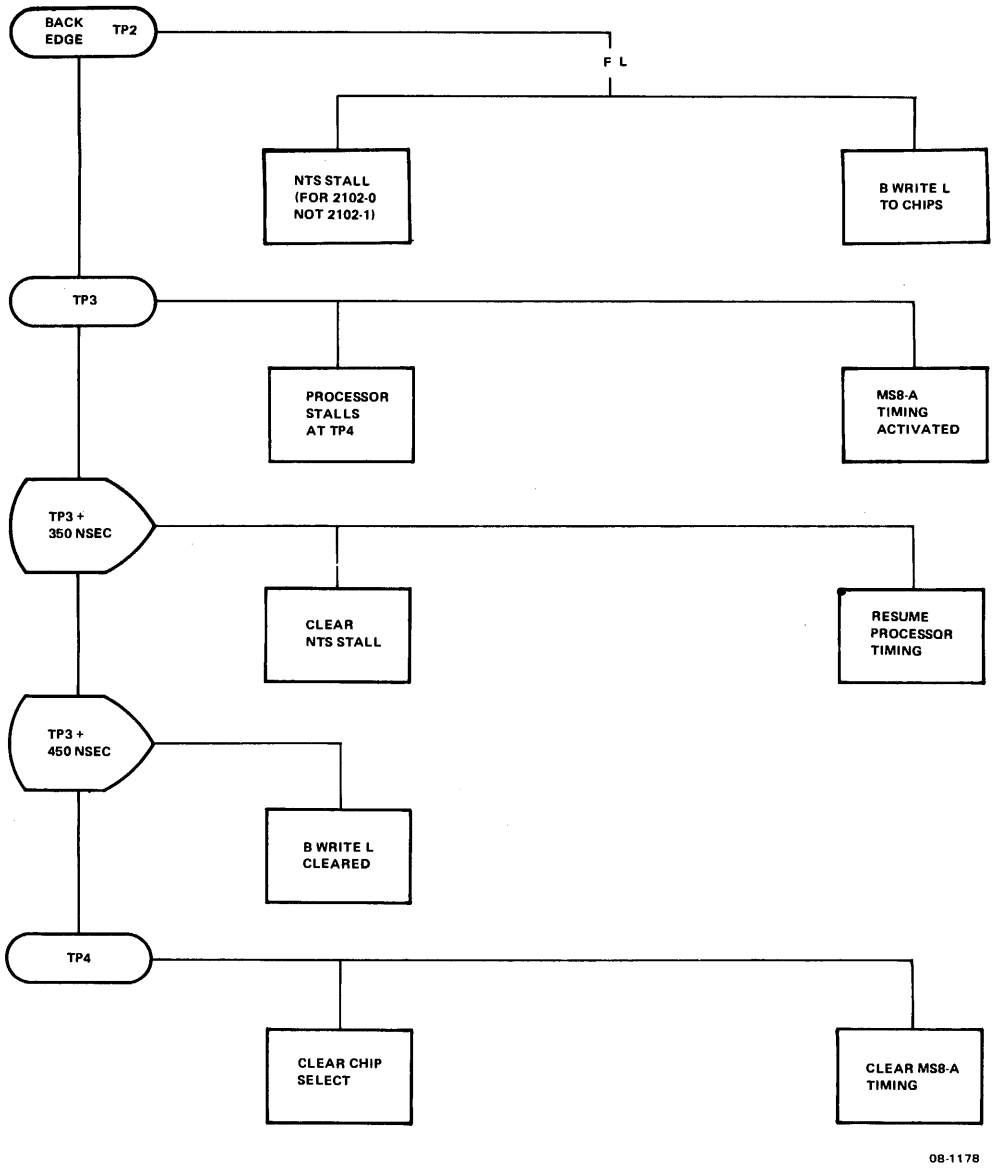


Figure 5-18 Write Cycle Flow Chart

5.10.1 Address Selection Logic

The address selection logic includes field selection, relative address and memory size selection.

5.10.2 Field Selection

Figure 5-19 shows the field selection logic. The first selection is made of a particular 4K memory field by means of the three EMA lines (EMA0 to EMA2) which originate in the extended memory option on the KM8-A module. If the KM8-A is not in the system, these lines are zeros, and field zero is selected. They select one of eight 4K memory fields.

The switches (S1-3 to S1-0) can be set to any digital code between 0 and 7. This number is compared with the number that appears on the EMA line by a 4-bit comparator circuit (IC 8242). Three bits decode the field number. The 4th bit tests the enabling signal ROM ADD L for a high. If there is a match, the RAM memory recognizes its own address and enables further processing by generating a signal FIELD H.

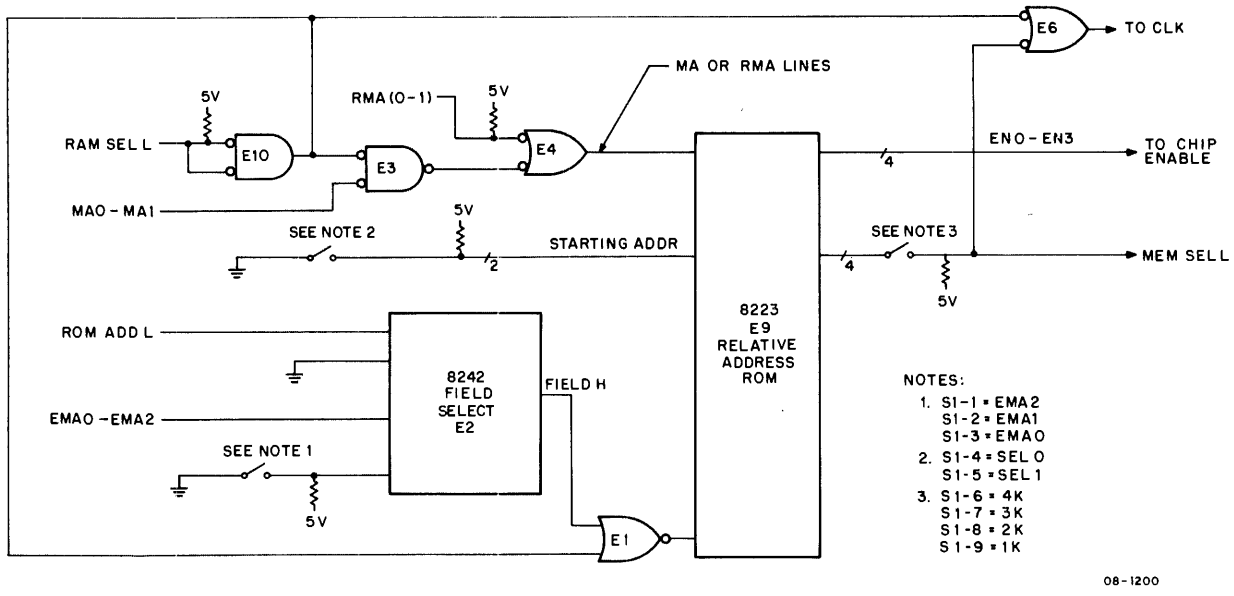


Figure 5-19 Address Selection Logic

5.10.3 Starting Address

The RAM memory is usually relatively small in comparison to total computer memory space. Furthermore, it is a specialized memory and it is important to conserve as much of its space as possible. One means of doing it is to use a reference. Address and program the RAM memory relative to this reference. As an example, memory address 5273(8) can be divided into two parts 4000(8) + 1273(8). The reference part of the address, 4000, can be a switch setting and only the relatively small number 1273(8) need have a RAM location. However, additional logic is required to subtract the reference from the total address. The small ROM (IC 8223) is programmed to perform this subtraction. The truth table is shown in Figure 5-20.

The inputs to the ROM (IC 8223) include, besides the ORed FIELD H and RAM SEL H signals, the two most significant bits of the address, MA <0:1> and two lines from the switch references, SEL 0 and SEL 1. The logic in the ROM automatically subtracts the switch reference address from the total address and generates the four signals, EN<0:3>, that are routed to the chip enable lines CE<3:0>. They, in turn, enable four rows of 12 chips each. The AND-OR gating of MA, RMA, and RAM SEL L on the input side of the ROM selects the operating mode, either main memory or scratchpad memory to the MR8-A ROM.

5.10.4 Memory Size Selection

On the output side of the ROM IC are four memory size selection switches. This size selection on the output side must be compatible with the reference selection on the input side. The truth table for the ROM shows the compatible memory size.

Referring to the above example and using the truth table (shaded portion), note the following:

Address 5273(8) falls in the range of addresses 4000-5777; MA0 is 1 and MA1 is 0. For a starting address of 4000(8) SEL 0 is 1 (S1-4 is open) and SEL 1 is 0 (S1-5 is closed). The output is ENO enabling the first row of chips, since only a 1K memory is required for the difference between 5273 and 4000(8) which is 1273(8).

Finally, a compatible memory size is either 1K or 2K, i.e., closing either switch S1-9 or S1-8 will assert MEM SEL L.

SWITCH OFF=1			INPUT						OUTPUT								
		STARTING	FIELD	REF SELECT		INPUT ADDRESS			CHIP ENABLE				SWITCH SELECT				
S1-4	S1-5	ADDRESS	SELECT	SEL0	SEL1	MA0	MA1	PIN NO.	EN3	EN2	EN1	EN0	4K	3K	2K	1K	
			14	13	12	11	10	ADDRESS	1	2	3	4	5	6	7	9	
								RANGE									SELECT
ON	ON	0	0	0	0	0	0	$0\text{-}1777_8$	0	0	0	1	0	0	0	0	ZEROS
			0	0	0	0	1	$2000\text{-}3777_8$	0	0	1	0	0	0	0	1	ONLY
			0	0	0	1	0	$4000\text{-}5777_8$	0	1	0	0	0	0	1	1	
			0	0	0	1	1	6000-7777	1	0	0	0	0	1	1	1	
ON	OFF	2000_8	0	0	1	0	1	$2000\text{-}3777_8$	0	0	0	1	1	0	0	0	
			0	0	1	1	0	$4000\text{-}5777_8$	0	0	1	0	1	0	0	1	
			0	0	1	1	1	$6000\text{-}7777_8$	0	1	0	0	1	0	1	1	
OFF	ON	4000_8	0	1	0	1	0	$4000\text{-}5777_8$	0	0	0	1	1	1	0	0	
			0	1	0	1	1	$6000\text{-}7777_8$	0	0	1	0	1	1	0	1	
OFF	OFF	6000_8	0	1	1	1	1	6000-7777,	0	0	0	1	1	1	1	0	

08-1204

Figure 5-20 ROM (IC8223) Truth Table

5.11 TIMING AND CONTROL LOGIC

The RAM operations are controlled by timed signals which originate in the central processor and in the MS8-A timing chain. The processor timing chain generates four time states, TS1 to TS4, and four time pulses, TP1 to TP4. In addition, the following signals are utilized:

1. SOURCE H,
2. B WRITE L
3. MEM DIR L.

For a complete list of all signals see Table 5-9.

In addition, the slower RAM memory contains an auxiliary timing chain which operates in conjunction with the processor main timing in the following manner. The processor clock is stopped during the read portion of the memory cycle. It is also stopped during the write portion of the memory cycle, provided the processor is not in the FETCH state. The MS8-A timing is started as the main clock is stopped. When the operation is completed (either read or write), the auxiliary timing chain is disabled and the processor timing is resumed.

The timing is further modified when the memory operates in combination with the ROM, the ROM-RAM mode. To compensate for the additional time required, for the settling of the address signals originating in the ROM there is a 300 ns delay. For details refer to Section 1.

5.11.1 MS8-A Timing Chain

The main components in the MS8-A timing chain shown in Figure 5-21, are the ten MHz crystal clock, a Serial In-Parallel Out shift register, and two synchronizing flip-flops. The shift register can be visualized as a tapped delay line except that the intervals are very accurately timed. The data entered at the input shifts at each clock pulse progress from R0 to R8 for a maximum time span of 800 ns, divided into 8 discrete 100 ns intervals. Each clock pulse advances the input one interval.

The shift register clock controlled by the logic is allowed to start and stop. It can be reset after the completion of the timing of one event and be started for the timing of another. It should be noted that the output of R0 is fed back to the reset of the synchronizing flip-flops. The result of this arrangement is that only one 1 bit is advanced along the register, the rest being 0s.

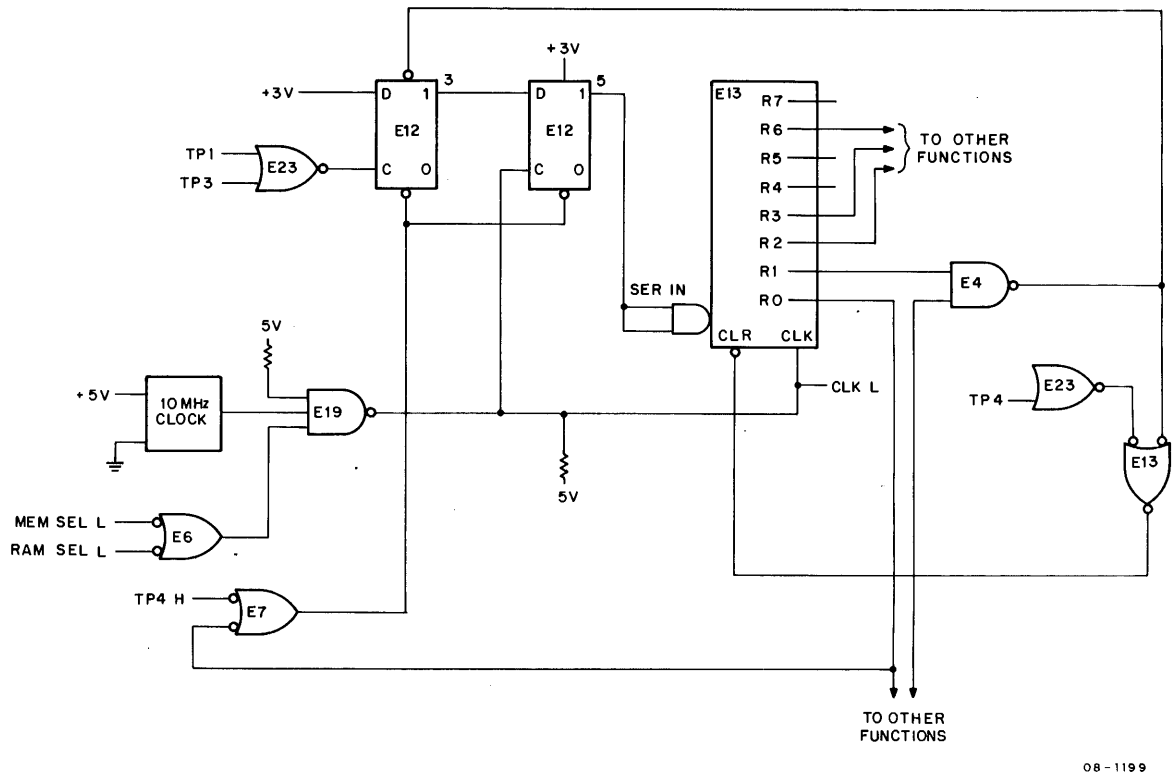


Figure 5-21 Memory Timing Chain

The shift register outputs are connected to control flip-flops that, in conjunction with other gating signals, enable the memory chips at the proper time and clock the contents of the memory into the memory output register. In addition, they disable the main clock and assert NTS STALL L. After a selected interval, the main clock is restarted, and NTS STALL L is negated.

5.11.2 Operation of a RAM Cycle

5.11.2.1 Read Cycle – Figure 5-17 is the timing diagram for the detailed logic shown in Figures 5-22 through 5-26. The read cycle is started at TP4 and the synchronizing flip-flops and the shift register are cleared, initializing the timing chain. In addition, the chip enable control flip-flop is cleared. At SOURCE time, (SOURCE H is generated approximately 200 ns from TP4 H), the memory register is cleared assuring a high to low transition on the MD lines. In addition, the STALL and CHIP ENABLE flip-flops are clocked. If there is a valid address, STALL L is asserted and the CHIP ENABLE signal is routed to the memory. The processor stalls at time TS2 and the timing chain of the MS8-A controls the remainder of the read cycle.

The control elements involved are the memory data clock and the STALL control flip-flops shown in Figure 5-26. At the expiration of a time interval, 800 ns, the signal MEM DATA CLOCK is generated and NTS STALL is cleared, restarting the processor timing. At TP2, the processor takes the memory data. The shift register and memory data clock flip-flops are cleared completing the read operation.

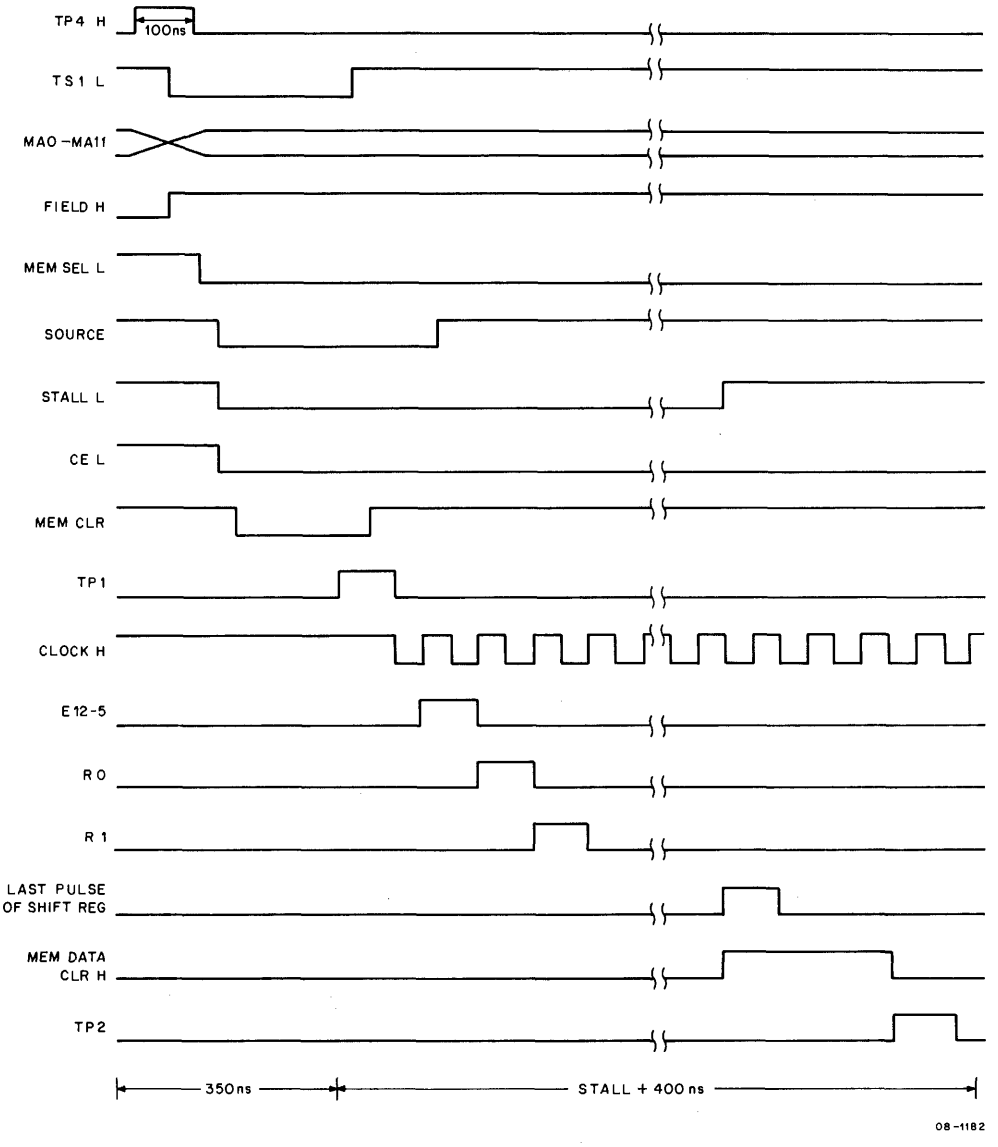


Figure 5-22 Read Cycle Timing Diagram

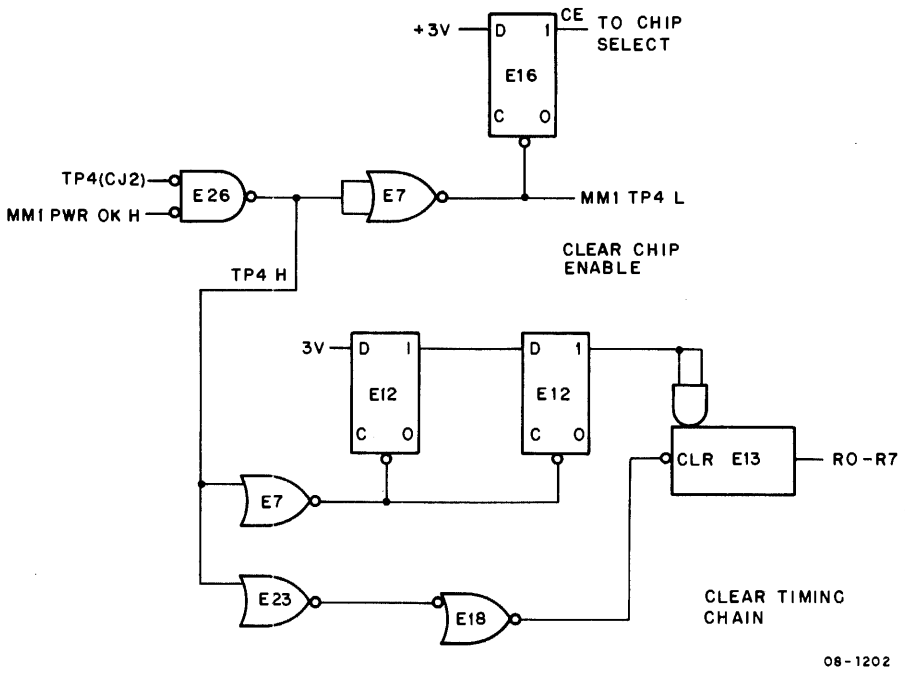


Figure 5-23 TP4 Logic

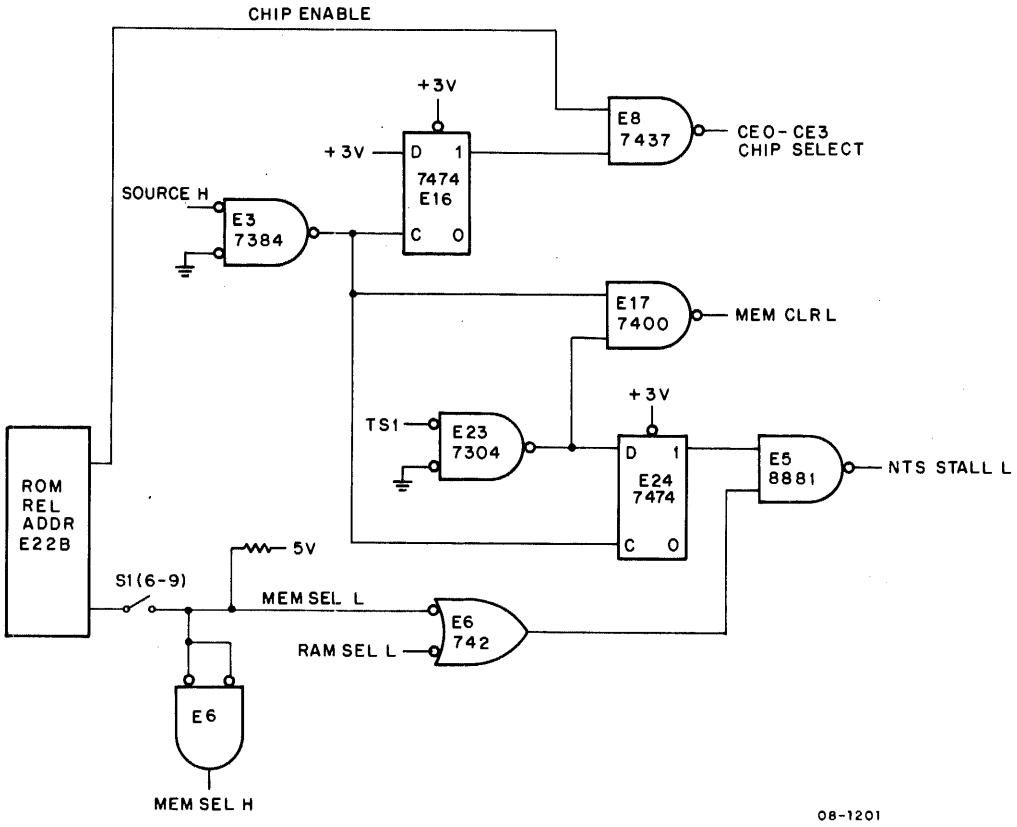


Figure 5-24 Source Time Logic

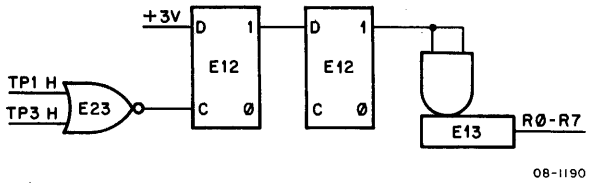


Figure 5-25 Operations at TP1

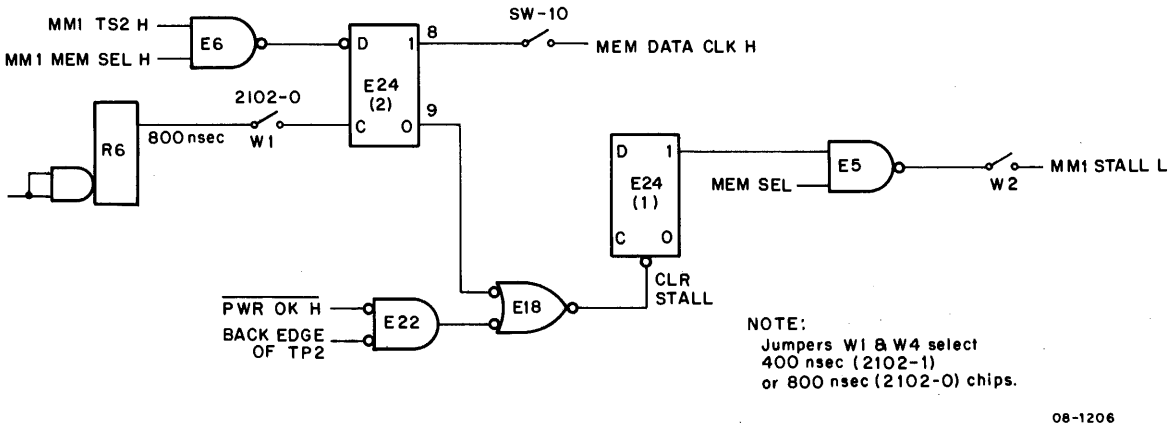


Figure 5-26 Stall + 400 ns Logic

5.11.2.2 Write Cycle – The flow chart and timing diagram are shown in Figures 5-18 and 5-27 and the logic diagram in Figure 5-28. The write cycle starts on The trailing edge of TP2 which clocks the STALL and B WRITE L flip-flops (Dual E11). The data inputs to both flip-flops are high. If the signal F L is high, indicating a write operation, the outputs of the flip-flop are high. The output of the inverter asserts NTS STALL L and B WRITE L respectively.

NTS STALL L is pulled during time state TS3 by the trailing edge of TP2. During time state TS4, the PDP-8/A stalls and the MS8-A timing chain takes control. 350 ns after TP3 and STALL, NTS STALL is cleared and the main processor timing is resumed. The write control flip-flop is cleared 100 ns later. At TP4, the MS8-A timing chain and chip select are cleared, completing the entire memory cycle.

5.11.3 Operation of a ROM-RAM Cycle

When the RAM operates in conjunction with the ROM, there is an additional delay due to the decision by the ROM whether it is ROM only or a ROM-RAM cycle. During this decision time of approximately 300 ns, the 13th bit is read and appropriate circuits are enabled. (See the ROM description in Section 1 for greater detail.)

There are two events which have to be timed – the RAM read cycle, which has been described above, and the selection of RAM by ROM, which precedes it.

The MS8-A timing chain times out this additional decision delay and at the end of 300 ns resets the shift register. The timing chain is restarted and times out the RAM read cycle. The timing chain is therefore activated twice during the read portion of the ROM-RAM memory cycle. The additional logic is shown in Figure 5-29 and the timing diagrams are shown in Figures 5-30 and 5-31. The operation is as follows (Refer to Figure 5-30 and 5-31).

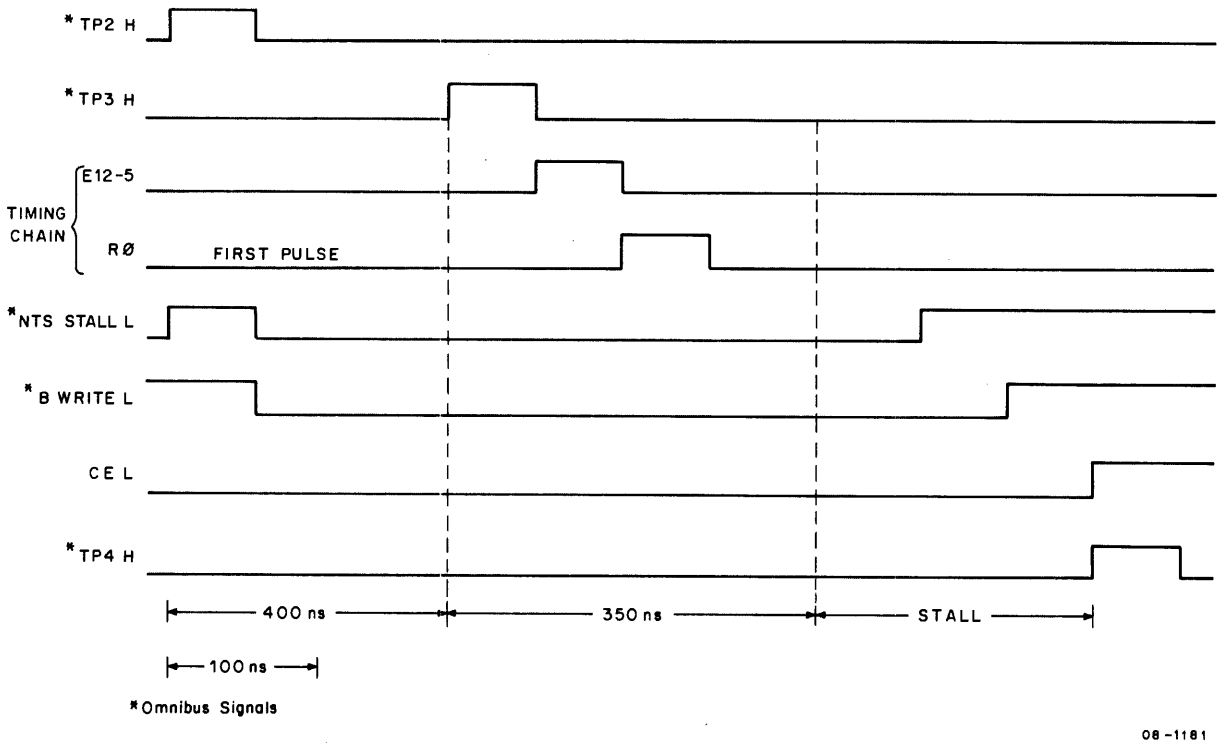


Figure 5-27 Write Cycle Timing Diagram

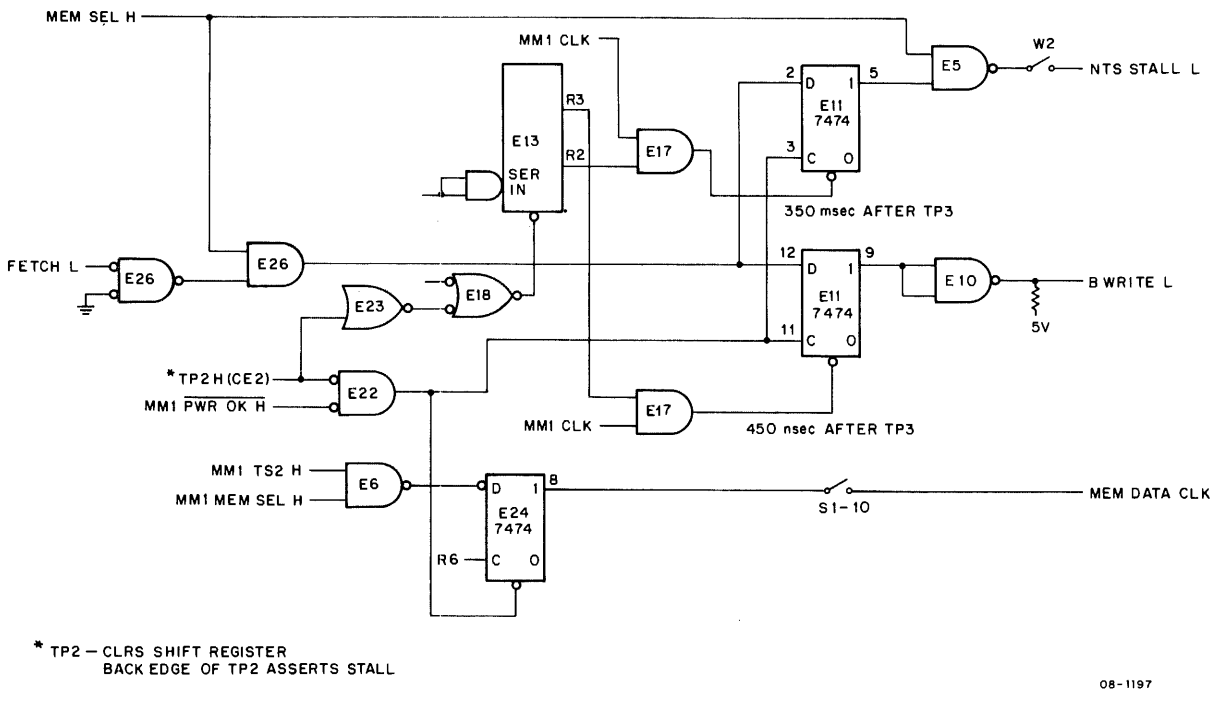


Figure 5-28 Write Cycle Logic

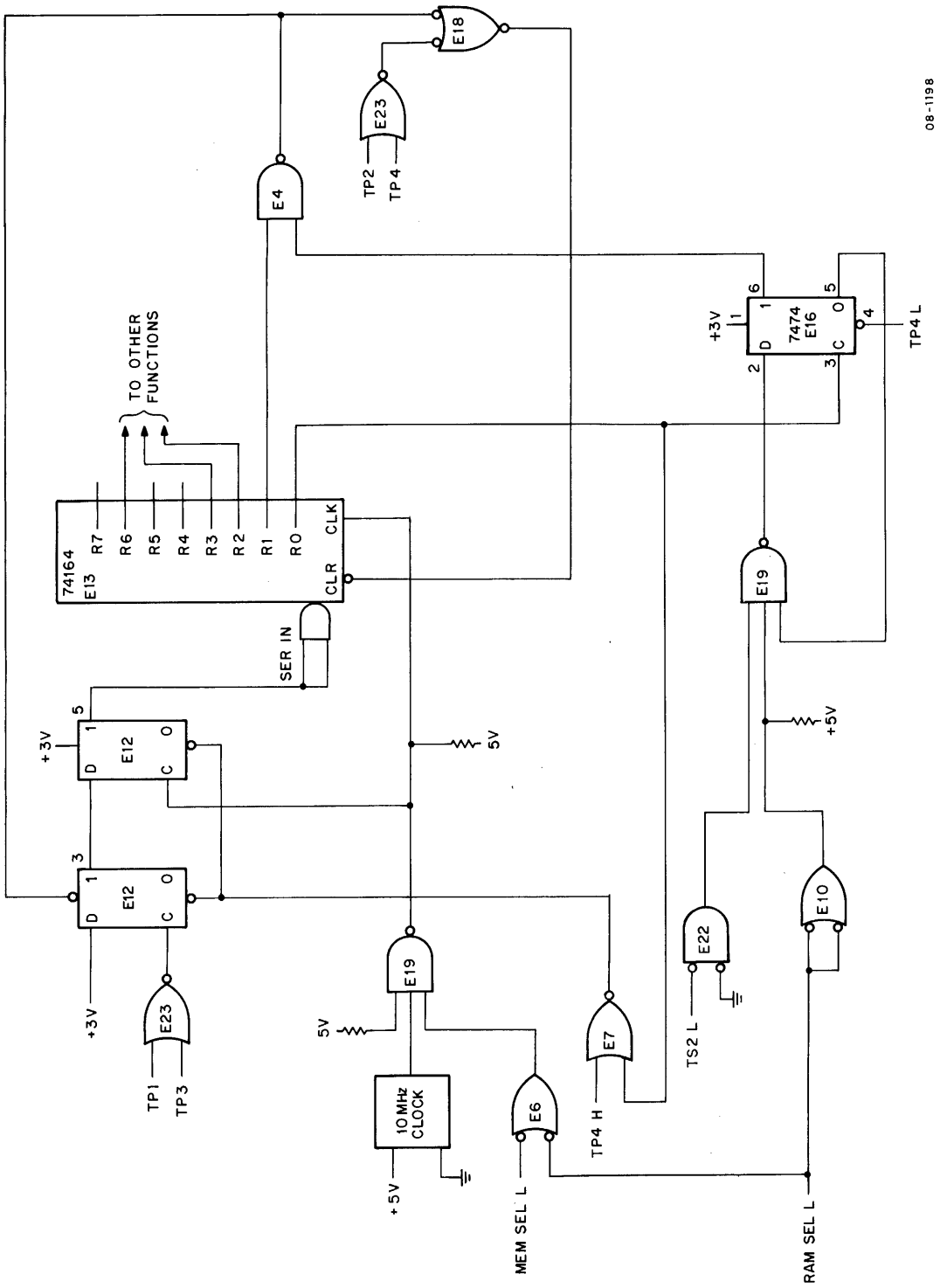
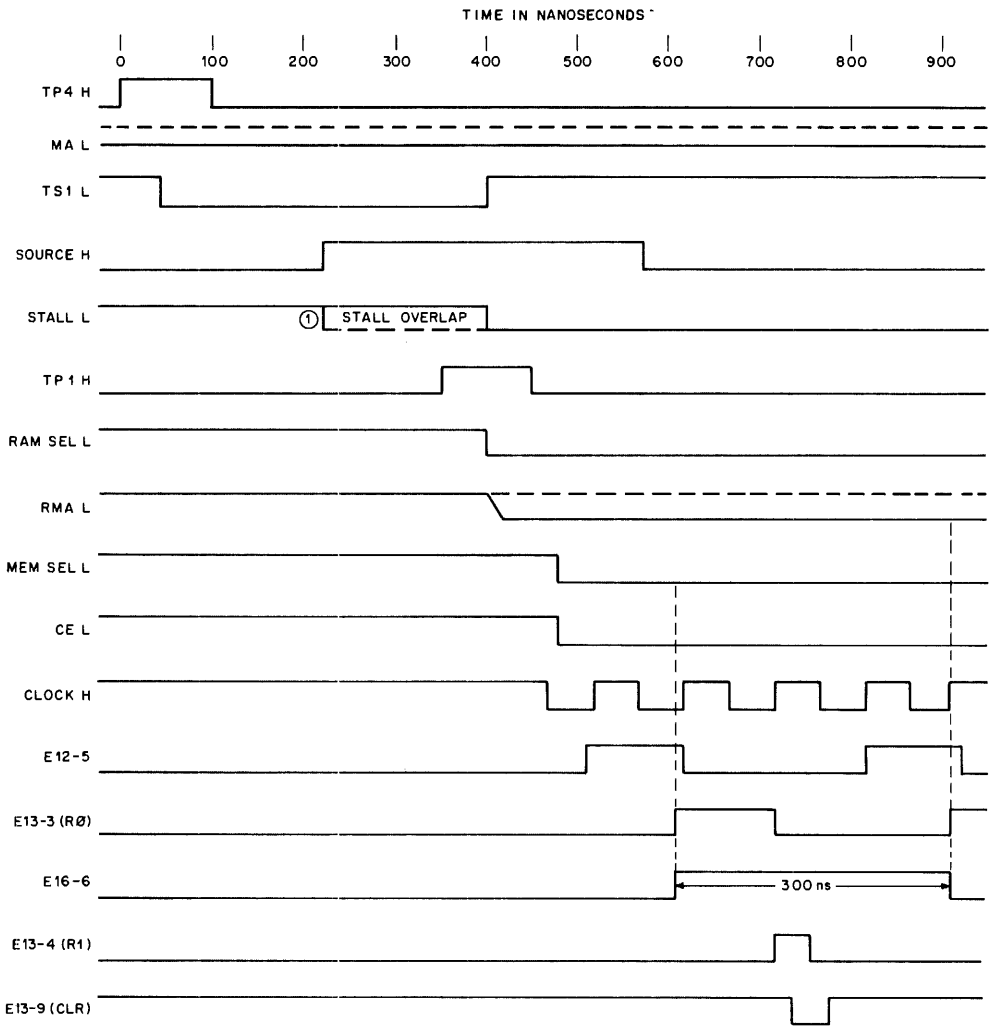


Figure 5-29 ROM-RAM Initial Delay Logic



NOTE 1. 'STALL L' is asserted first (at SOURCE time) by the ROM memory, and is asserted at 'RAM SEL L' by the MS8-A. From the second positive transition on E12-5, the memory cycle is the same as a normal Read/Write Cycle.

08-1180

Figure 5-30 ROM-RAM Initial Delay Timing Diagram

At TP1 the synchronizing flip-flops are clocked. TS2 L follows at about the midpoint of the TP1 pulse. The RAM SEL L signal appears at the input to E19. The data input to E16 pin 2 turns low. On the second clock pulse, a high appears at the input of the shift register. At the third clock pulse, R0 is high and E16 is clocked. At the fourth clock pulse, both inputs to the NAND gate E4 are high. The output of E4, after inversion, clears the shift register and sets the synchronizing flip-flop. This completes the first timing operation. The second timing operation now begins. This time the shift register is not reset at R1 since the data output of E16 is a low. The result is that the timing proceeds as in the previous cycle.

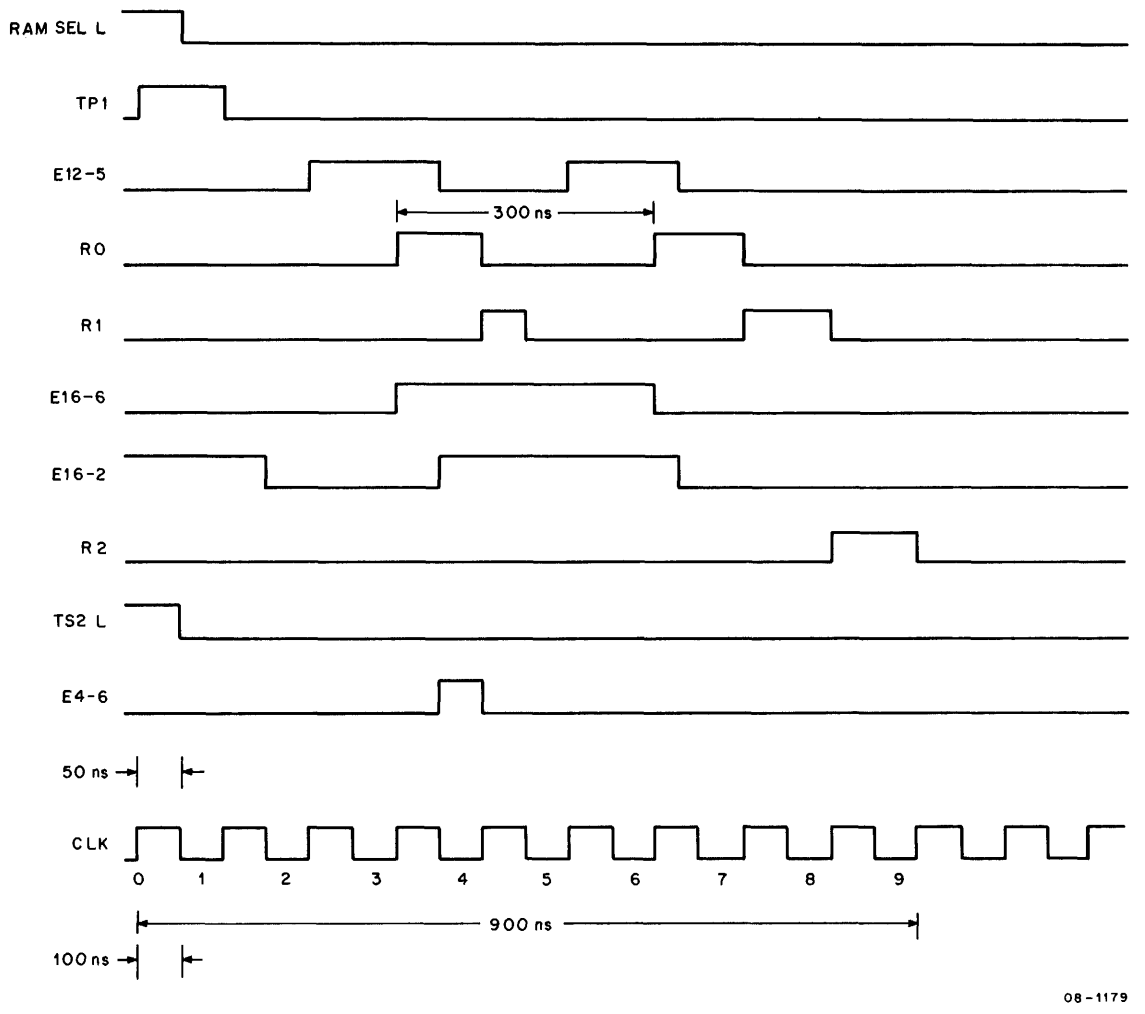


Figure 5-31 Detailed Timing of Initial Delay in ROM-RAM Cycle

5.11.4 Memory Data and Memory Output Register

A typical 1K memory that consists of 12 1024 X 1 chips is shown in Figure 5-32.

The ten address input terminals (A<0:9>) are connected to either the MA or RMA lines by the gating circuitry. The RMA lines (RMA2 - RMA11) are selected when RAM SEL H is true. Two control inputs are available on the chip: Chip Enable and B WRITE L, in addition to the data input and output terminals. (Terminals 11 and 12 respectively.)

The output data of the 12 chip array during a read operation is routed to a bank of 12 "D" type flip-flops. Their output in turn is gated with the Omnibus signal MEM DIR L, which directs the memory data onto the MD lines. This occurs when the flip-flops are clocked by the signal MEM CLR L. During the write portion of the memory cycle the chips accept data from the MD lines. When the control signal B WRITE L is true and MEM DIR L goes high.

5.12 SWITCH DEFINITIONS

The switch functions and settings are defined in Table 5-10.

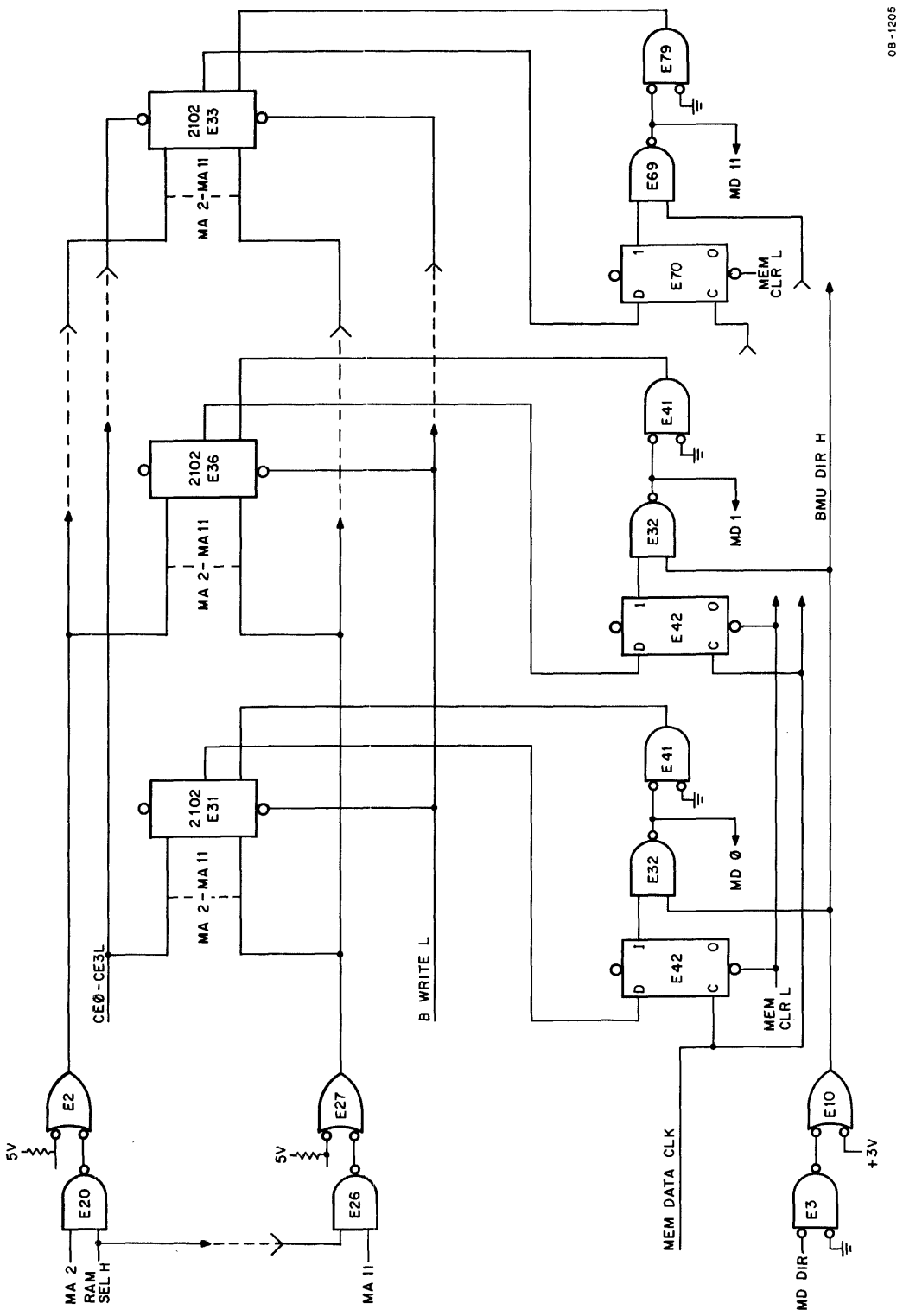


Figure 5-32 Memory Array and Output Register

Table 5-10
MS8-A Read/Write Memory Switch Settings

S1-1, 2, and 3	Field Selection			
	S1-1	**S1-2**	**S1-3**	**Field Selected**
	ON	ON	ON	0
	OFF	ON	ON	1
	ON	OFF	ON	2
	OFF	OFF	ON	3
	ON	ON	OFF	4
	OFF	ON	OFF	5
	ON	OFF	OFF	6
	OFF	OFF	OFF	7
S1-4 and 5	First Address			
	S1-4	**S1-5**	**First Address in this RAM**	
	ON	ON	0000	
	ON	OFF	2000	
	OFF	ON	4000	
	OFF	OFF	6000	
S1-6	ON for 4K Memory M8311-YD, OFF for 1K or 2K			
S1-7	OFF			
S1-8	ON for 2K Memory M8311-YB, OFF for 1K or 4K			
S1-9	ON for 1K Memory M8311-YA, OFF for 2K or 4K			
S1-10	Test switch, normally ON			

SECTION 3
MR8-FB REPROGRAMMABLE READ ONLY MEMORY (PROM)

5.13 MR8-FB 1K MEMORY

The MR8-FB (Figure 5-33) is a memory option for PDP-8/A computers. It is used in applications where 1. non volatility of a program's instructions is desired, and 2. less than 256 writable locations per 1024 locations are required for program execution.

The MR8-FB contains two semiconductor memory element types: reprogrammable read only memory and bipolar random access read/write memory. For the purpose of simplicity in this manual these memory elements will be referred to as PROM and RAM respectively.

When 13th bit=0, DATA Out = PROM DATA and RAM is not accessed
When 13th bit=1, DATA Out = RAM DATA and PROM DATA = RAM Address

The PROM section of the MR8-FB is organized as 1024 13-bit words. Once loaded, the content of the PROM is permanent unless the PROM chips are exposed to an intense source of ultraviolet light.

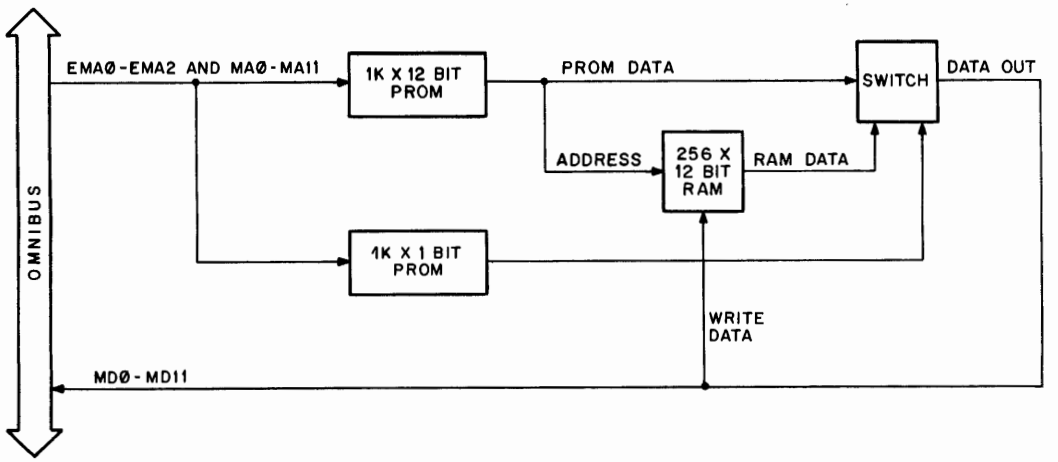


Figure 5-33 Simplified MR8-FB Block Diagram

The RAM section is organized as 256 12-bit words. The PROM is accessed at the address applied to the memory address bus. The data out of the PROM is gated onto the memory data bus or applied to the address inputs of the RAM. The path activated is determined by the state of the 13th bit of the PROM word. Although the PROM is accessed in all cases, any 256 locations of the PROM may be defined as read/write.

Other characteristics of the MR8-FB are as follows:

Physical – M8349 quad size module

System Memory Space – Each MR8-FB in a system occupies a 1024 (2000(8)) word block. The location of this block within the 32K of available memory space is defined by the user via diode placement.

Program Startup – The user has the option of program start at relative location 0 or 200 of the MR8-FB. When enabled by the installation of a jumper, the start-up logic is activated by the BOOT switch or key on the front panel.

Battery Backup for RAM – Connectors are provided to supply the RAM only with power if power is lost to the rest of the system (RAM loses data when power is removed.)

5.13.1 MR8-FB Specifications

Characteristic	Specification
Power Requirements	+5 V @ 3.8 A – 15 V @ 350 mA
Memory Cycle Time	3.7 μs
PROM Erasure Method	Ultraviolet Light
PROM Program Loading Method	By External Programmer (MR8-SL)
Memory Capacity	1K of PROM with 256 words of Read/Write Memory (RAM)
Operating Temperature	0 to 55° C
Testing	Two diagnostic programs, Internal Test (loaded into the MR8-FB) and PROM Diagnostic are supplied to check the MR8-FB. PROM diagnostic is supplied on paper tape and runs in additional read/write memory to verify the contents of the MR8-FB corresponds to the users papertape.

NOTE

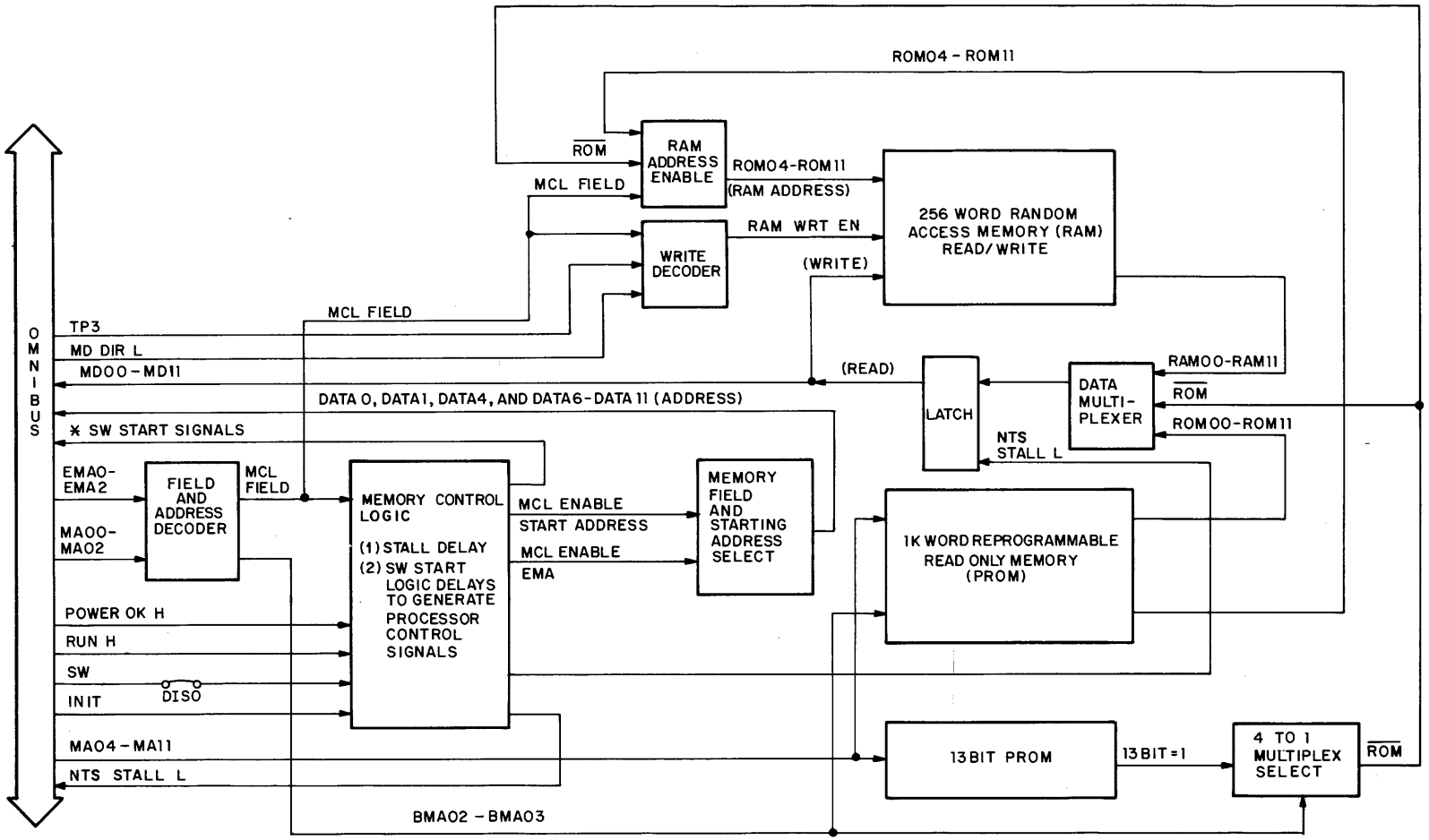
The data tape used to program the MR8-FB must be available to run the diagnostic.

5.13.2 MR8-FB Description

Figure 5-34 is a detailed block diagram of the MR8-FB. The functional groups of logic shown in Figure 5-34 are discussed in the following paragraphs.

5.13.3 Address Decoder

The Address Decoder contains address select diodes that can be arranged to assign a 2000(8) block of addresses to the MR8-FB. When EMA0-EMA2 and MA 00-MA 11 are applied to the select diodes in the correct states, MCL FIELD L is asserted to indicate that the MR8-FB is selected by the program. Also included is the Field Selection Decoder, which, by using three jumpers, selects the field where the PROM program will run.



* The SW start signals are PULSE LA, MEM START, MS, DIS, LA EN, KEY CONT. These signals are explained in TABLE 9-4 of the SMALL COMPUTER HANDBOOK - 1972

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Figure 5-34 MR8-FB Block Diagram

5.13.4 Starting Address Decoder

The Starting Address Decoder is used to start a program whose starting address is location 000(8) or 200(8) of any 1K memory in any memory field when BOOT on the Programmer's Console is pressed twice or BOOT on the Limited Function Panel is raised and then lowered.

5.13.5 Bootstrap Operation

When BOOT on the Programmer's Console is pressed twice or BOOT on the Limited Function Panel is raised and lowered, the PROM initializes the CPU, loads a starting address, selects a memory field, and starts the program at the address and field specified by the Starting Address Decoder. Figure 5-35 is a timing diagram for the Bootstrap operation. The MR8-FB signals used in this and other timing diagrams are explained in Table 5-11. When BOOT is activated the PROM must:

1. Initialize the CPU.

2. Load the starting address of the program, determined by jumpers (ST AD) on the board.

3. Load Extended Address (Memory Field), determined by by jumpers (EMA) on the board. The instruction and Data Fields are connected together so both are enabled with one jumper.

4. Start the Program.

The BOOT feature may be used only on one MR8-FB and only if another option that uses BOOT Start is not installed on the Omnibus. The BOOT function is selected by the installation of the DIS jumper in the memory control logic of the M8349 module.

5.13.6 Memory Control and Timing Logic

The memory control logic generates the necessary control signals to initialize the CPU and start a program at the specified starting address during BOOT operations. It also produces the timing signals required for memory operation.

5.13.7 Read or Read/Write

During a read operation the contents of the PROM memory location addressed by the program are applied to the MD lines to be read into the processor. The timing diagram in Figure 5-36 assumes that the 13th bit is 0 and the contents of the addressed PROM location are applied to the MD lines.

When the 13th bit is a 1, the 8 least significant bits (04-11 of the PROM output) are used as an address rather than an operand to point to a read/write location in the 256-word RAM. Figure 5-37 shows the timing required for this operation. The type of operation (read or write) is determined by the operand in the RAM location addressed by PROM or by an operand in PROM that writes in this location.

5.13.8 1K PROM

Figure 5-38 is a block diagram of the 1K PROM. Only 256 words are shown in the diagram. A 256-word, 12-bit PROM (12 X256 ROM matrix) is formed by one 256 word, 8-bit ROM and half of one 256 word, 8-bit ROM. Using six ROM chips in this way produces 1024 12-bit words of PROM. This is done by selecting one chip and either the upper or lower half of another chip for each read operation (Figure 5-39). As an example, if memory location 0000 is selected, E26 and the lower half of E50 are enabled.

5.13.9 13th Bit PROM

The 13th bit PROM chip provides the additional bit for each of the 2000(8) locations in PROM. If this bit is set to 1, the contents of the PROM location addressed by the program are used to select a location in read/write memory. The 13th bit is not seen by the processor or program.

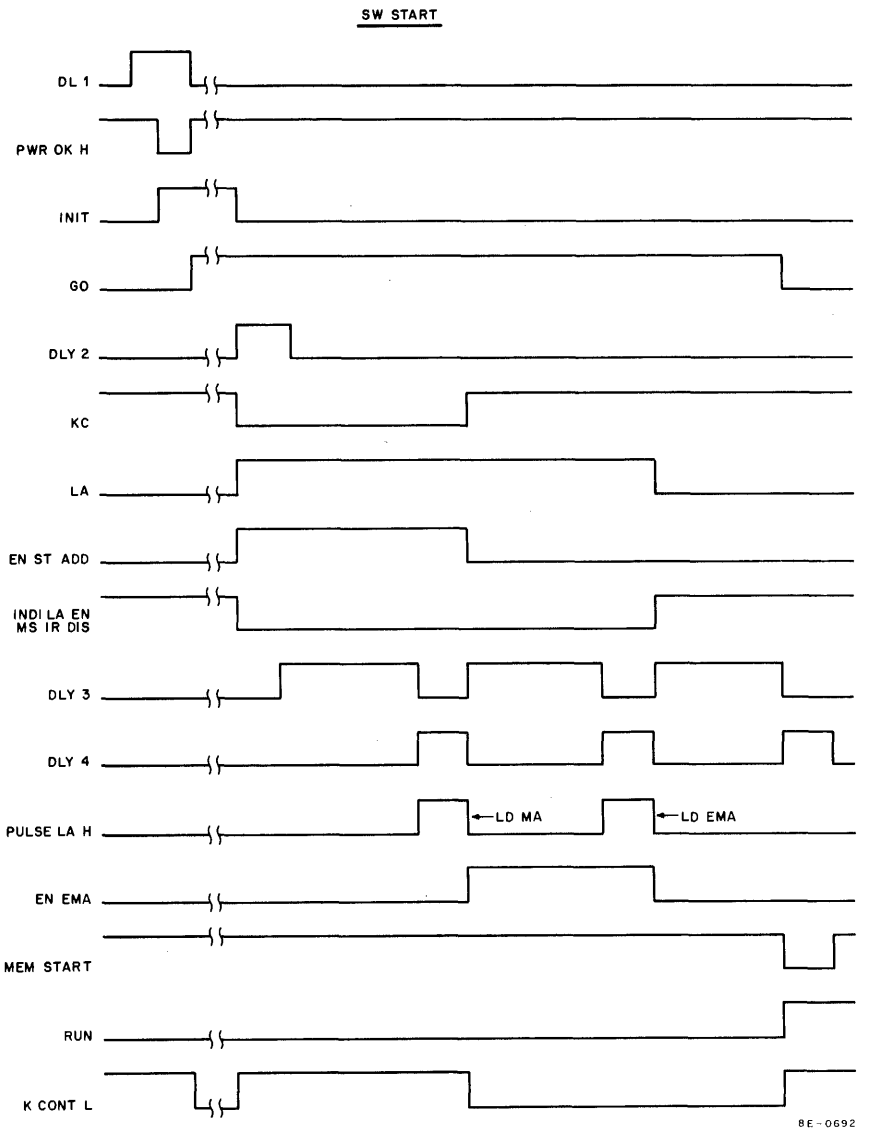


Figure 5-35 Bootstrap Operation Timing

5.13.10 ROM Address Flag

The ROM Address flag is always disabled on the MR8-FB. YA1 should never be installed. This is used on some configurations of PROM that are in the same field as core memory.

5.13.11 Read/Write Memory (RAM)

The RAM is composed of twelve 256 X 1-bit chips. When the 13th bit of a PROM location is set, the 8 least significant bits of PROM in that location are used to address the RAM. The contents of RAM are then applied to the MD lines instead of PROM. The output of RAM is selected when ROM L is made true by the 13th bit.

To write in a RAM location RAM MD DIR H must be asserted to generate a WRITE EN. If WRITE EN L is asserted, data on the MD lines is written into the RAM location addressed by PROM, at TP3 time.

Table 5-11
MR8-FB Signals

Signal	Description
DLY 1	DLY 1 (Delay 1) is a one-shot multivibrator that ouptuts a 3 ms pulse when BOOT on the Limited Function Panel is pressed and raised, or BOOT on the Programmer's Console is pressed twice. This pulse sets the MCL GO flip-flop and pulls PWR OK low to start the timing and generation of CPU signals required to load the starting address and memory field from the Starting Address Decoder.
DLY 2	DLY 2 (Delay 2) is a one-shot multivibrator that outputs a 100 ns pulse on the trailing edge of INIT H when MCL GO is set (1). This pulse sets MCL LA, clears MCL KC, and triggers DLY 3 on the trailing edge. This enables the following signals to be applied to the Omnibus: *MS IR DIS L *LA EN L *IND 1 L *KEY CONT L MCL EN ST ADDR H is then asserted to apply the starting address to the Omnibus.
DLY 3	DLY 3 (Delay 3) is a one-shot multivibrator that is triggered by the trailing edge of DLY 2 to generate a 250 ns pulse. The 0-side of DLY 3 is applied to DLY 4, which is triggered on the trailing edge of this pulse. This is used to separate the setting of levels from the pulse that loads these levels into the processor.
DLY 4	DLY 4 (Delay 4) is a one-shot multivibrator that is triggered on the trailing edge of DLY 3. This delay, along with DLY 3, is triggered three times in the timing cycle. Twice DLY 4 produces PULSE LA L and the last time it produces MEM START L.
EN EMA H	EN EMA H (Enable EMA) is asserted at DLY 3 time when MCL GO (1), MCL KC (1), and MCL LA (1) are asserted. This puts the field select bits on the Data Bus, so that at the next PULSE LA, it is strobed into the processor.
EN ST ADDR H	EN ST ADDR H (Enable Starting Address) is asserted at DLY 2 time when MCL GO (1), MCL KC (0), and MCL LA (1) are asserted. This puts the starting address on the Data Bus, so that at the next PULSE LA, it is strobed into the processor.
INIT*	INIT (Initialize) is asserted if PWR OK H is asserted to clear all flags, the AC, and the interrupt and break systems.
IND 1*	IND 1 is asserted low at the same time as LA EN L to ensure that only the data lines are on the Data Bus when the starting address is transferred during SW operations.
KEY CONT L*	KEY CONT L is asserted by the MR8-FB to generate STOP L, enable loading of the EMA, reset the RUN flip-flop, and disable the interrupt system.

*These signals are defined in detail in Chapter 3.

Table 5-11 (Cont)
MR8-FB Signals

Signal	Description
MCL GO H	The MCL GO flip-flop is set by a DLY 1 pulse when BOOT on the Limited Function Panel is pressed and raised or BOOT on the Programmer's Console is pressed twice. This signal enables the gates required to apply starting address, memory field, and CPU control signals to the Omnibus.
MEM START L*	MEM START L is grounded prior to TP2 time to initiate a memory cycle. Memory cycles are continued until STOP is set.
PULSE LA H*	PULSE LA H is asserted twice during a SW operation to transfer the contents of the Data Bus to the CPMA Register. The Data Bus contains the starting address one time and the EMA bits the other time.
PWR OK H	PWR OK H (Power OK) is normally negated (low) by the power supply output dropping below a predetermined level to initialize and stop the processor. In the MR8-FB, PWR OK H is negated during a SW operation to initialize the CPU.
RAM 00 – RAM 11	RAM 00 – RAM 11 is the 12-bit output of the read/write memory location which is addressed by a location in PROM and applied to the MD lines if the 13th bit at that PROM location is set.
ROM 00 – ROM 11	ROM 00 – ROM 11 is the 12-bit output of PROM when a memory location in PROM is addressed by the program. If the 13th bit is set to 1, ROM 04 – ROM 11 are used to address a location in RAM.
RAM MD DIR H	RAM MD DIR H is asserted by MD DIR L from the Omnibus to generate RAM WRT EN. RAM WRT EN is applied to the RAM chips to enable data on the MD lines to be written into RAM.
RAM WRT EN	RAM WRT EN L is asserted to enable the write input to all RAM chips during a write operation. This signal is controlled by RAM MD DIR L whose state is determined by MD DIR L from the Omnibus, and by TP3*.
RETURN H*	RETURN H is asserted during a read or write operation. It is used in the MR8-FB during the read part of a cycle to trigger the NTS STALL one-shot multivibrator.
ROM ADDR L	ROM ADDR L is not used on the MR8-FB.
ROM L	ROM L is the output of the 13th bit multiplexer. It is used to select the output (ROM 00 – ROM 11 or RAM 00 – RAM 11) to be put on the MD lines. It also enables RAM for a write operation.
NTS STALL L	NTS STALL L is asserted for 2.2 μs to allow time for access to PROM memory and for data to settle on the MD lines. The trailing edge of NTS STALL L is used to clock ROM 00 – ROM 11 or RAM 00 – RAM 11 out of the Data Multiplexer and onto the MD lines during a read operation.

*These signals are defined in detail in Chapter 3.

Table 5-11 (Cont)
MR8-FB Signals

Signal	Description
SW*	SW is asserted (low) when BOOT is activated to start the timing sequence which loads the starting address. Note the SW DIS jumper must be installed to use this feature with the MR8-FB. BOOT on the Limited Function Panel must be pressed, then raised, or BOOT on the Programmer's Console must be pressed twice to start the SW start timing cycle.

*These signals are defined in detail in Chapter 3.

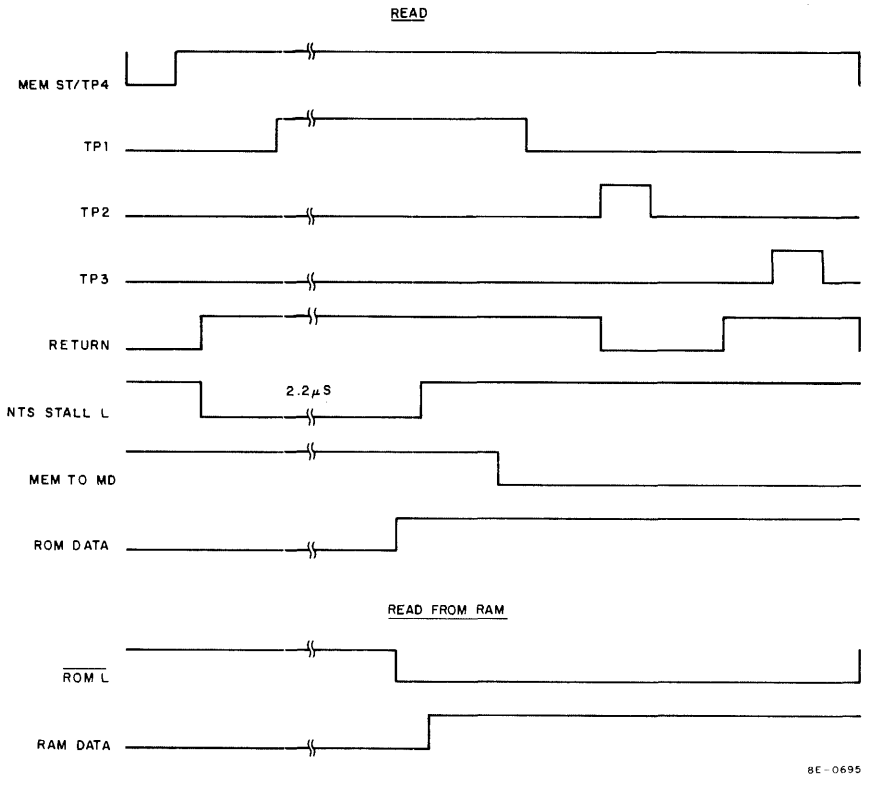


Figure 5-36 Read Timing

5.13.12 Data Multiplexer

The Data Multiplexer selects either ROM 00-ROM 11 or RAM 00-RAM 11 to be applied to the MD lines during a read operation. ROM L is asserted if the 13th bit is a 1 to select RAM 00-RAM 11. If the 13th bit is 0, ROM L is negated and ROM 00-ROM 11 is applied to the MD lines.

5.14 MR8-FB PROGRAMMING

The PROM chip is an ultraviolet (UV) erasable device. Seven PROMs provide the 1K X 12 plus 1K X 1 bit storage. The programming pulses needed are of high (35-48 V) amplitude. To isolate these from the TTL logic, all pins of the PROM chips are brought out to top fingers on the 1-side of the module. The TTL levels associated with the normal PROM functions are brought to the corresponding fingers on the 2-side. In normal operation, single-width top connectors join the 1-side to the 2-side of the module. To program the PROM, the top connectors are removed and four cables are connected to the fingers instead. These cables make contact with the 1-side only and are interlocked to prevent application of destructive voltages if the cables are plugged in incorrectly.

The PROM, when erased, contains all 0s. When programming the PROM, ones are inserted where needed. The 0 can be put in only by erasing the whole PROM. The PROM is reprogrammable a minimum of 100 times.

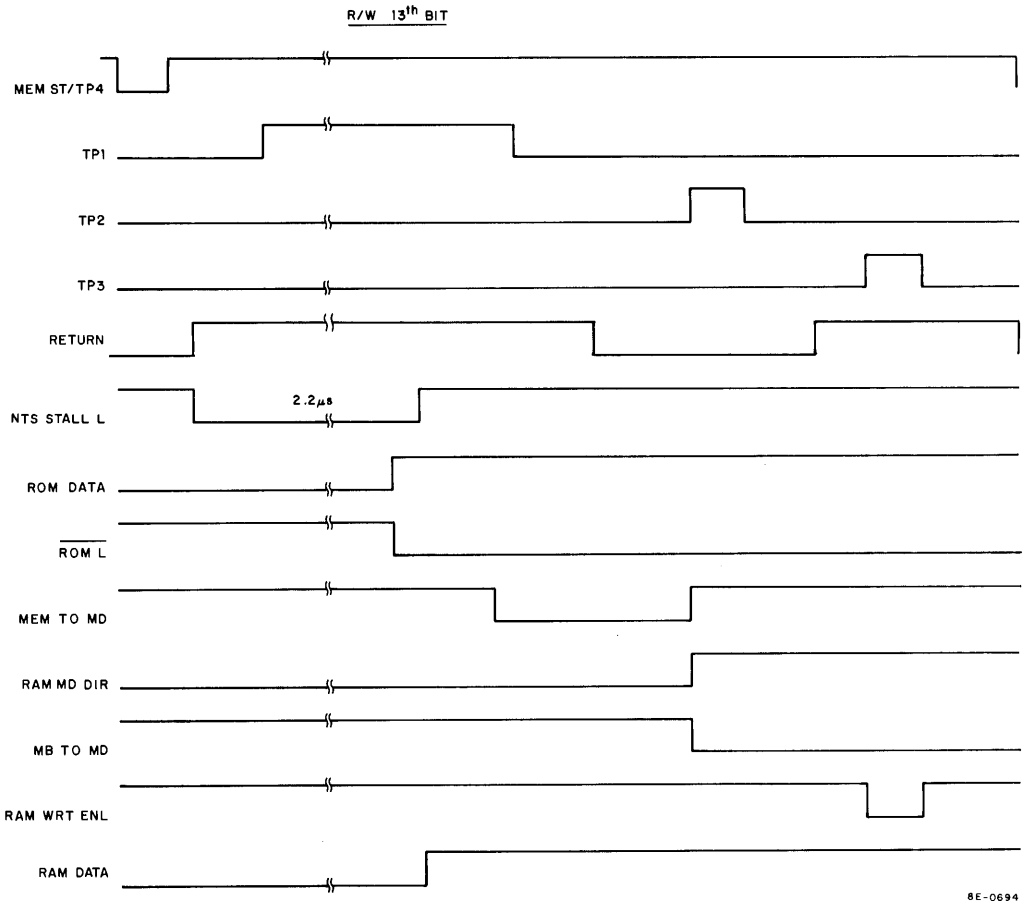


Figure 5-37 13th Bit Read/Write Timing

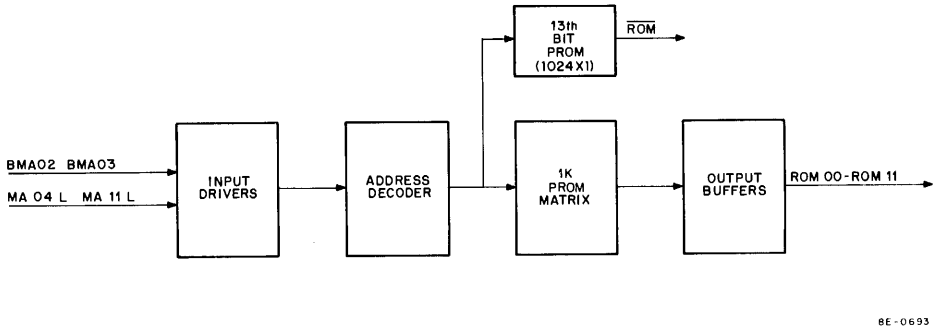


Figure 5-38 PROM Block Diagram

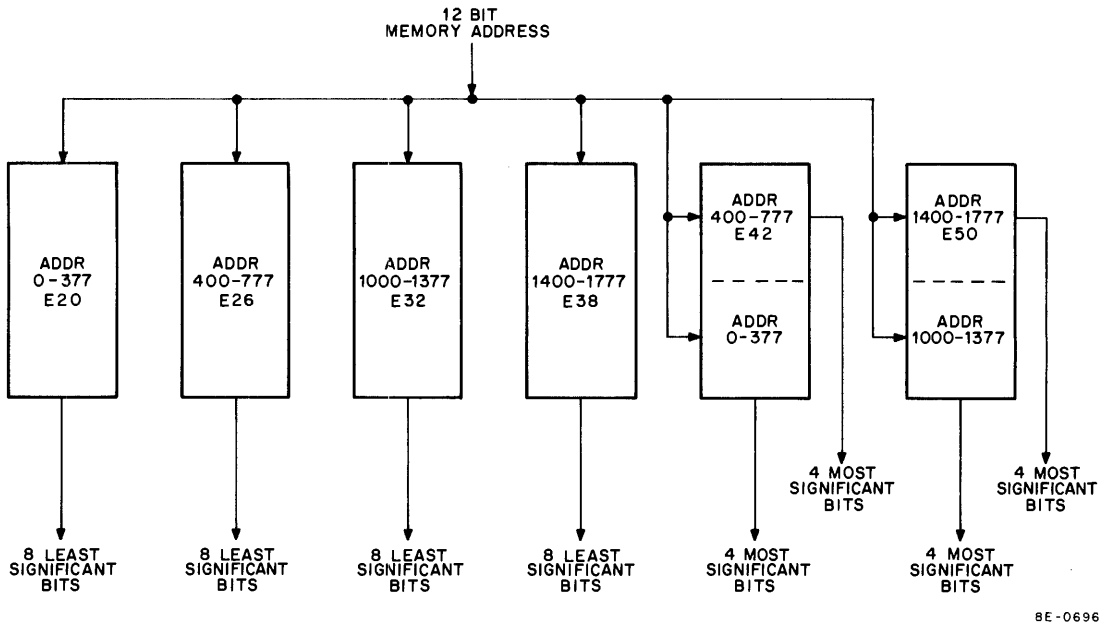


Figure 5-39 PROM Addressing Scheme

A normal problem with read-only memories is that codes must be specially written to avoid instructions that require a write operation (i.e., JMS, DCA, and ISZ) and the placing of variable locations in R/W memory. In this PROM, that restriction is removed if the total number of alterable locations in a piece of core is 256 or less. This is done by making the PROM a 13-bit memory. On a read access, if the 13th bit is a 1, the least significant 8 bits stored in the ROM are treated as an address, rather than an operand, and point to a read/write location. The 1K of PROM provides 256 of these locations.

By checking a program as it is written, it is possible to tag all operands that may be changed in the course of execution and then to modify the program controlling the PROM programmer to set the 13th bit for this address and place the next available RAM address in this location. Thus, whenever this location in PROM is accessed, the actual data will be read from or written into the corresponding RAM location.

Programming Example

```
210/        TAD CONST
211/        DCA TEM
212/        ISZ CNTR
213/        TAD TEM
214/        JMS SUBR
210/        01254
11/         03361
12/         02255
13/         01361
14/         04300

254/        0010        /CONSTANT 10
255/        10001       /POINTS TO RAM LOCATION 1
361/        10002       /POINTS TO RAM LOCATION 2

300/        10003       /POINTS TO RAM LOCATION 3 FOR RETURN ADDRESS STORAGE
```

After PROM is programmed, it must be checked using the MR8-FB diagnostic and the data tape used to program the PROM. PROM is read and compared to the program tape. The read/write locations specified by the 13th bit are exercised to determine if they read and write correctly.

Refer to *Introduction to Programming–1972* for other PDP-8/A programming information. The rules for programming and generating paper tapes to program the MR8-FB are given in the *MR8-F Program Format Description* (DEC-08-OMRAA-C-D).

5.14.1 PROM Erasing Procedure

The PROM data may be erased by exposure to high intensity, short-wave, or ultraviolet light at a wave length of 2537 A. The recommended integrated dose (i.e., UV intensity × exposure time) is 6 W sec/cm(2). The ultraviolet lamps should be used without short wave filters and the PROM should be placed about one inch away from the lamp tube. This operation has the effect of writing all 0s into the PROM.

WARNING

Short wave ultraviolet light can cause "sunburning" of the eyes and skin. Eyes should be protected from exposure.

5.15 DETAILED LOGIC DESCRIPTION

The MR8-FB logic has been divided into functional groups for discussion purposes. The block diagram, Figure 5-34, should be used to understand the interaction of the logic, the signal flow within the module, and the input or output signals.

5.15.1 Address Decoder

Figure 5-40 shows the Address Decoder logic. The address assigned to the MR8-FB is selected by cutting out one of the diodes on each address bit. As an example, if the address assigned to the MR8-FB requires EMA 2 L to be 1, diode D3 is taken out, so that when EMA 2 L is a 1, E24 and E17 do not ground the base of Q1. When the correct combination of 1s and 0s (the address of the MR8-FB) are applied to the Address Decoder logic, the base of Q1 is positive and E9 is enabled to assert MCL FIELD H and MCL FIELD L. This enables the memory address bits (MA 04-MA 11) to be applied to the 1K PROM chips and select a PROM memory location. This also enables the 13th bit decoder to determine if the 13th bit at that memory location is a 1.

5.15.2 Timing and Processor Control for SW Start of Memory

The logic used to initialize the processor, load the starting address and memory field, and start the program is shown in Figure 5-41. The timing required for this operation is shown in Figure 5-35.

A BOOT operation timing chain was implemented with four time-delay one-shot multivibrators designated DLY 1 through DLY 4. The 74123 IC (Figure 5-41) consists of two one-shot multivibrators that output a pulse each time the input is triggered. The duration of the output pulse is determined by an external resistor and capacitor.

If the SW DIS jumper is installed, the timing chain is started by SW H from the Limited Function Panel when BOOT is pressed and then returned to the up position or when BOOT is pressed twice on the Programmer's Console. A positive-going transition on the SW line sets DLY 1 for 3 ms. The RC network and feedback on the input line removes switch contact bounce.

PWR OK H is negated (pulled low) shortly after the DLY 1 pulse is generated if the RUN ON jumper is installed to supply a ground to E48, or if the RUN OFF jumper is installed and RUN L is negated (high). With the RUN OFF jumper installed as shown in Figure 5-41, SW operation takes place only when the processor is not running. If the jumper is installed in the RUN ON position, the SW operation takes place anytime BOOT is activated. When PWR OK H goes low, the processor generates a 560 ms INIT H pulse to clear the processor and options.

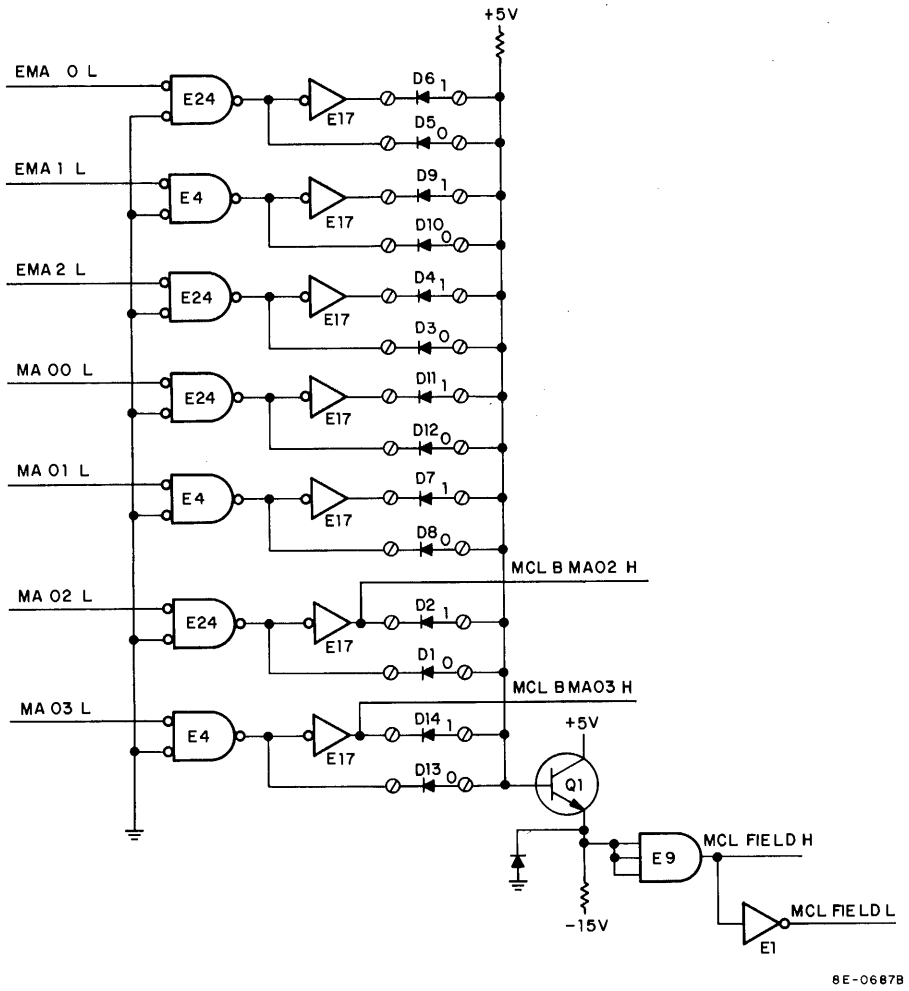


Figure 5-40 Address Decoder Logic

After the 3 µs delay DLY 1 times out and the 0 side goes high, it clocks the MCL GO flip-flop. MCL GO sets and MCL GO (1) H is true. This signal enables the signals to the starting address and field select logic, as well as most of the signals used by the processor during an SW start sequence. The timing out of DLY 1 also removes the NOT PWR OK signal, allowing PWR OK to go high (true).

When INIT times out and goes low, and with MCL GO set, DLY 2 is triggered to generate a 100 ns pulse. DLY 2 on the leading edge ensures that MCL KC is 0 and it sets MCL LA to 1. With MCL LA and MCL GO set, IND 1 L, LA EN L, and MS IR DIS L are applied to the Omnibus. With MCL KC cleared, MCL EN ST ADDR H becomes true and the starting address is applied to the data lines.

When DLY 2 times out (100 ns), its trailing edge triggers DLY 3, which produces a 250 ns pulse. This delay allows the signals generated by the previous delay to settle on the Omnibus.

On the trailing edge of DLY 3, DLY 4 is triggered, producing a 100 ns pulse. The DLY 4 pulse, along with MCL LA being set, enables NL gate, E59 and produces PULSE LA H which loads the starting address into the processor. This pulse is fed back to DLY 3, MCL LA, and MCL KC. On the trailing edge of DLY 4, DLY 3 is triggered and MCL KC is set. Because MCL KC was a 0, MCL LA remains set.

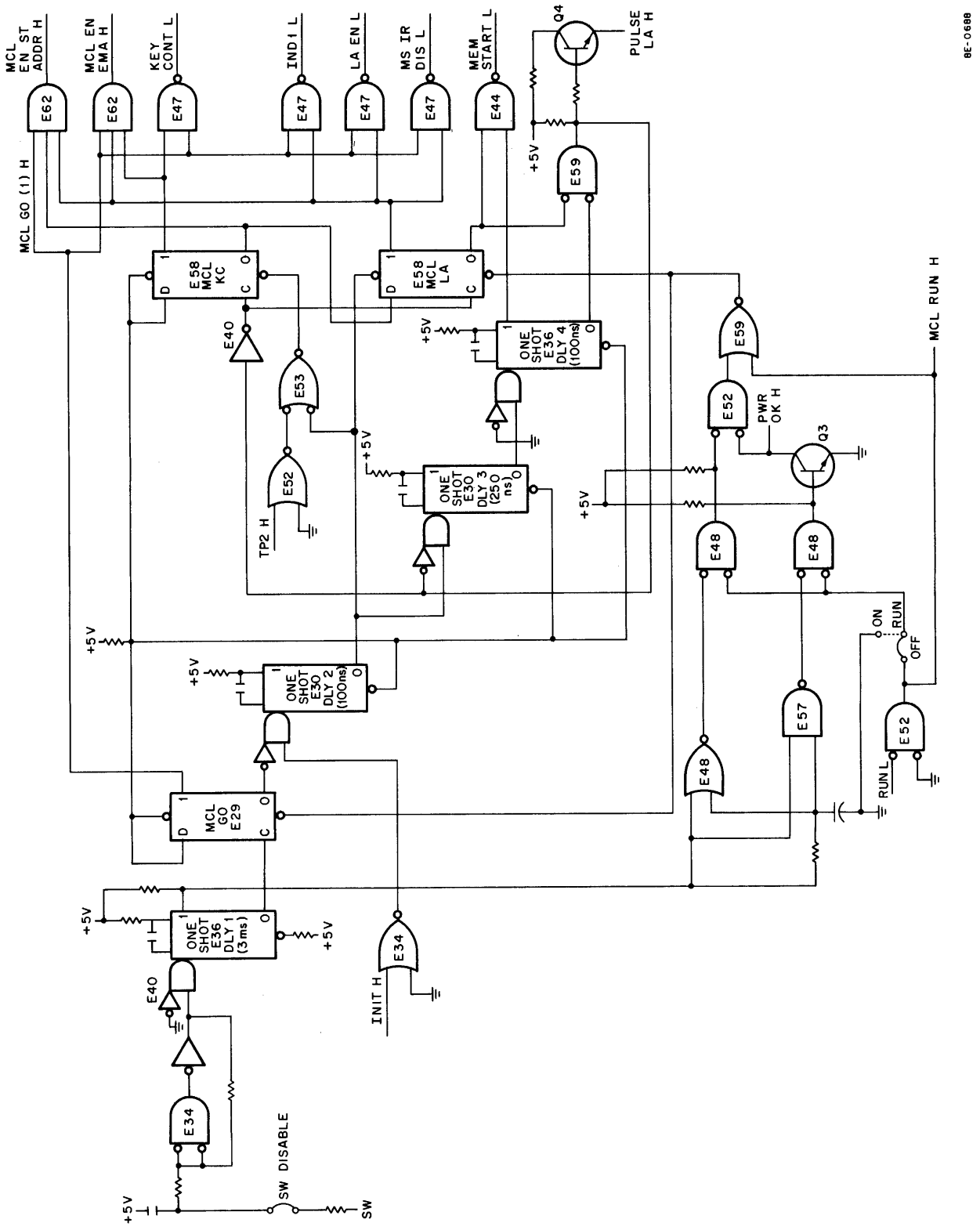


Figure 5-41 ML8-F Timing and SW Operation Control Logic

Now that MCL KC is set, MCL EN ST ADDR is removed, MCL EN EMA H is enabled, and the field address is applied to the Omnibus. KEY CONT L is also applied to the Omnibus.

Once again DLY 3 times out and triggers DLY 4. This again produces the 100 ns PULSE LA H signal, retriggers DLY 3, and clears MCL LA on its trailing edge. With MCL LA removed, all signals are disabled except MEM START.

When DLY 4 is triggered again by the trailing edge of DLY 3, the only signal generated is MEM START L. MEM START L is applied to the Omnibus to start the timing chain on the timing board of the processor and the RUN flip-flop sets. When RUN sets, MCL GO clears to disable the SW start logic. The next TP2 pulse clears MCL KC.

At this time, the program starts at the address specified by the starting address and field select logic (Figure 5-35).

5.15.3 Field and Starting Address Select Logic

The field and starting address select logic is shown in Figure 5-42. This logic determines the starting address and field in which the program that is started with BOOT key resides. The starting address and field are selected by jumpers. Removing a jumper causes a 1 to be placed onto the associated Data Bus line; otherwise, a 0 is placed on that line. These jumper bits are applied to the data bus when either MCL EN ST ADDR H or EN EMA H in the control logic is true (Figure 5-41). DATA 6-8 and DATA 9-11 on the Data Bus are transferred to the IF and DF of memory extension control when PULSE LA H is asserted (Figure 5-42). DATA 00 and DATA 01 determines the 1K block of memory in which the program resides, and DATA 4 determines the starting address (000(8) or 200(8)).

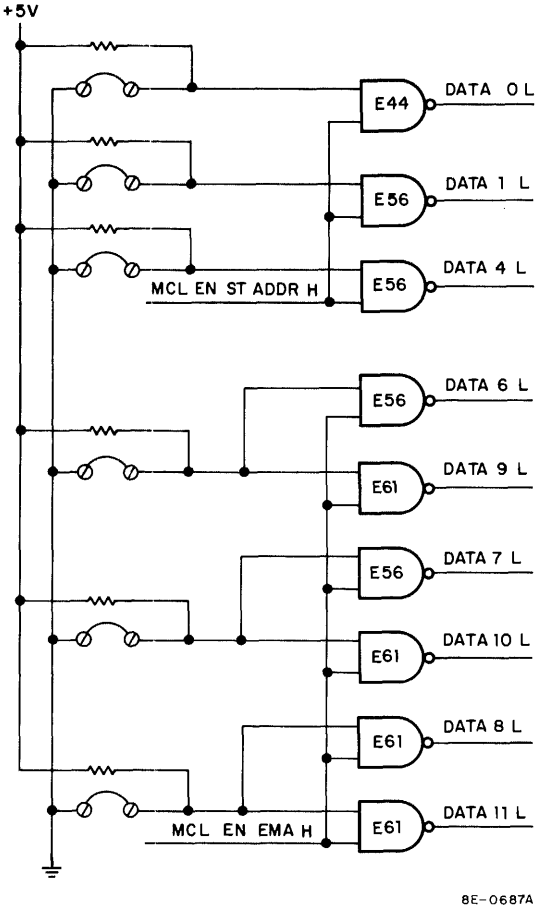


Figure 5-42 Field and Starting Address Select Logic

5.15.4 Memory Address Control Signal Generation

The logic shown in Figure 5-43 generates NTS STALL L, and ROM ADDR L to control PROM and ROM memory access.

5.15.5 NTS STALL

NTS STALL L (E21B) is triggered by WRITE H and RETURN H. It generates a 2.2 μs pulse which is applied to the memory timing module. NTS STALL L increases the memory cycle by 2.2 ns to allow for the longer access time of PROM and time for the data on the MD lines to settle before it is transferred to the processor.

5.15.6 ROM ADDR

The MR8-FB does not occupy memory locations assigned to a regular core memory, the jumper on the output of E44 is not installed, and ROM ADDR is never set. This feature is used on other versions of PROM not available for the PDP-8/A.

5.15.7 1K PROM Memory and Control Logic

Figure 5-44 shows 400(8) words of PROM, the control logic required to read PROM, and the chip for the 13th bit addressing. Reading of the other PROM chips is accomplished the same way as the 400(8) locations show (Engineering Drawing D-CS-M8349-0-0).

The Memory Address bits (MA 04-MA 11) are applied to the address inputs of the PROM 1702A chips when MCL FIELD L is asserted by the Address Decoder (Figure 5-40). MCL FIELD L is asserted when this PROM is addressed by the program. BMA 02 and BMA 03 are applied to NAND gates E12 where they are decoded to enable the two addressed chips to be read. As an example, if BMA 02 and BMA 03 are both 0s, E12D is enabled and E26 and the lower half of E50 are selected. This is done by supplying a low input to CS of these 2 chips. The CS input to the 13th bit chip is grounded so this chip is read every time. The output PROM is applied to the Data Multiplexer (Figure 5-45) except when bit 13 is a 1. When bit 13 of the memory location addressed by the program is a 1, ROM H and ROM L out of E16 are asserted. Bit 13 is a 1 when the program must address a location in read/write memory. When ROM L is asserted, the eight least significant bits of PROM (ROM 4-ROM 11) are applied to the RAM chips to select a location in RAM.

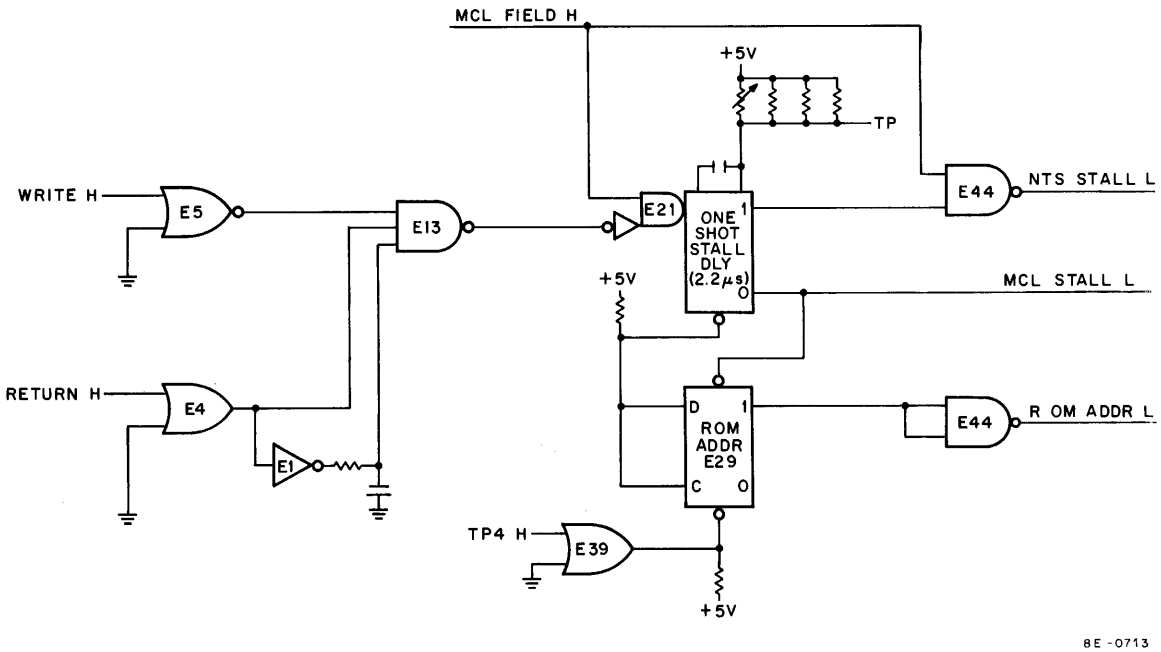


Figure 5-43 Memory Address Control Signal Generator

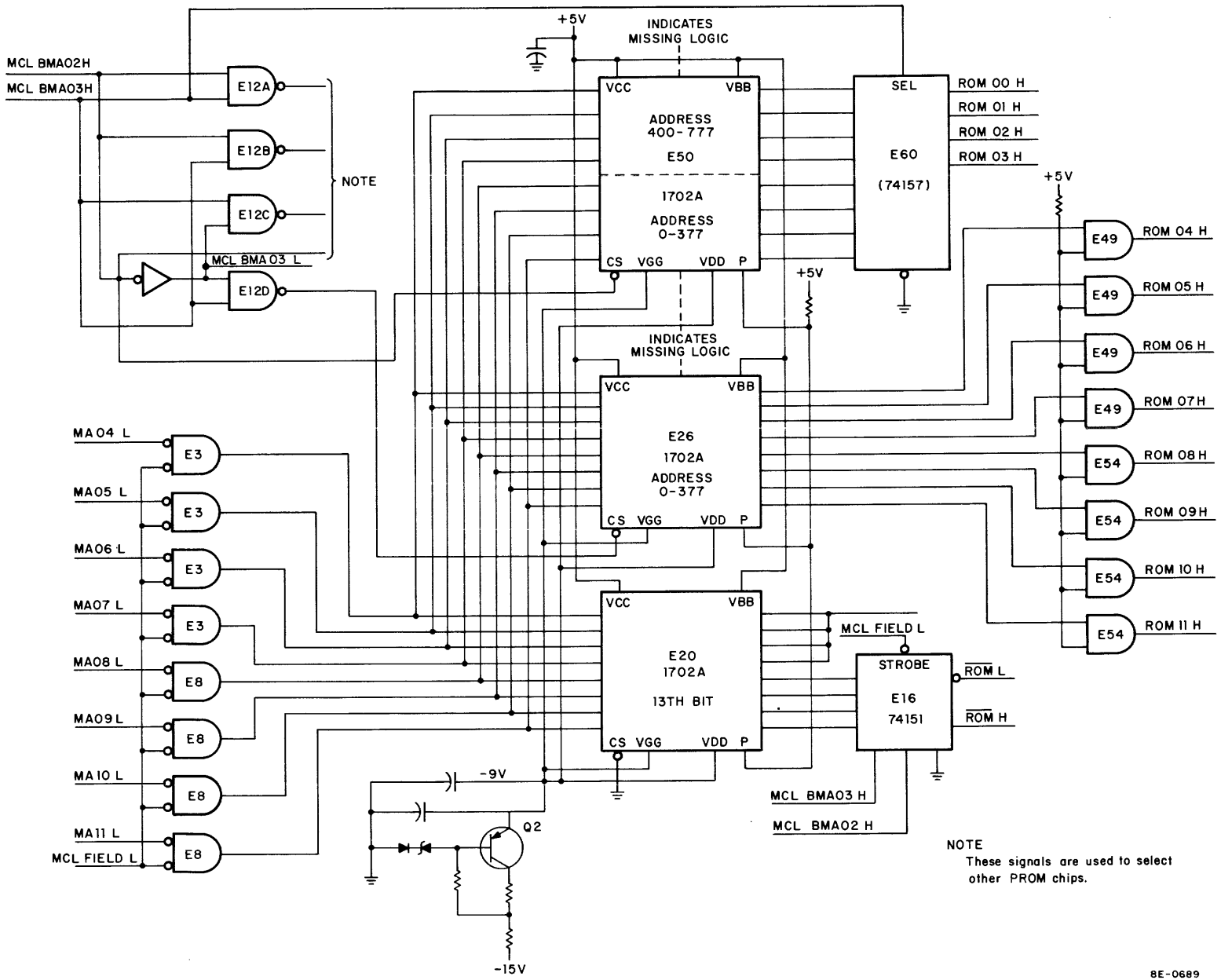


Figure 5-44 PROM and Control Logic

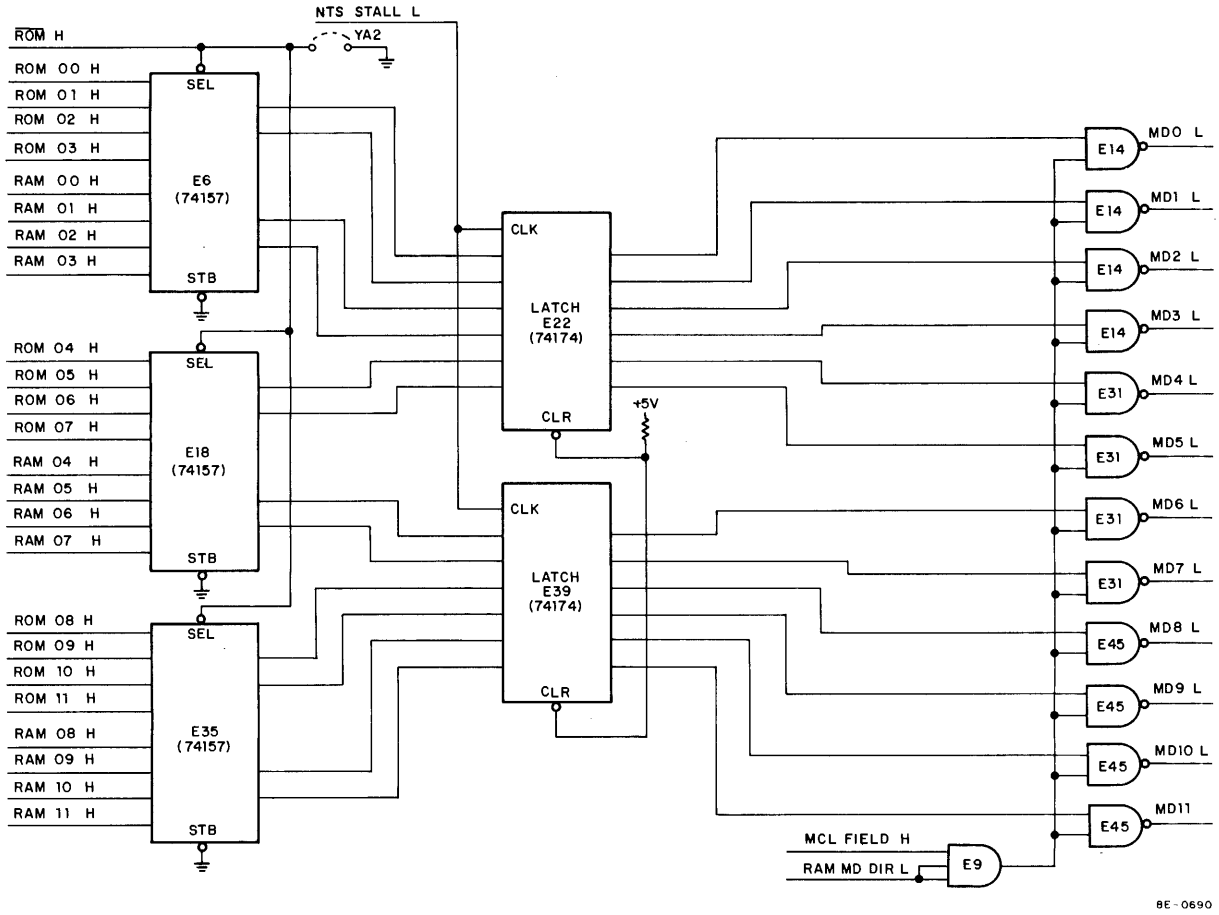


Figure 5-45 ROM and RAM Data Multiplexer and Latch

5.15.8 256 Read/Write Memory and Control Logic

ROM 00-ROM 11 are applied to the 74200 RAM chips when ROM L is asserted. ROM L is asserted if bit 13 is a 1. MCL FIELD L is always asserted when the PROM is addressed. ROM 04-ROM 11 selects an address in RAM and RAM 00-RAM 11 are applied to the Data Multiplexer (Figure 5-45). The timing for this operation is shown in Figure 5-37.

If the instruction specifies a write operation for RAM, MD DIR L from the Omnibus is negated (high) and RAM WRT EN L is asserted at TP3 time. RAM WRT EN L is applied to the WRT input of all twelve RAM chips and the data on the MD lines (MD 00-MD 11) is written into the RAM location selected by ROM 04-ROM 11.

The tabs shown in Figure 5-47 are used to supply +5 V from a battery so that RAM will not be changed if power fails. The jumper shown takes the +5 V from the Omnibus to supply the RAM chips. It can be changed to use the battery voltage if this is desired by the user.

5.15.9 ROM and RAM Data Multiplexer

The ROM and RAM Data Multiplexer is shown in Figure 5-46. The multiplexer consists of three 74157 ICs that select either ROM 00-ROM 11 or RAM 00-RAM 11 to be applied to the MD lines. If the 13th bit is a 1, ROM H is true (high) and RAM 00-RAM 11 are selected as an output; otherwise ROM 00-ROM 11 are selected.

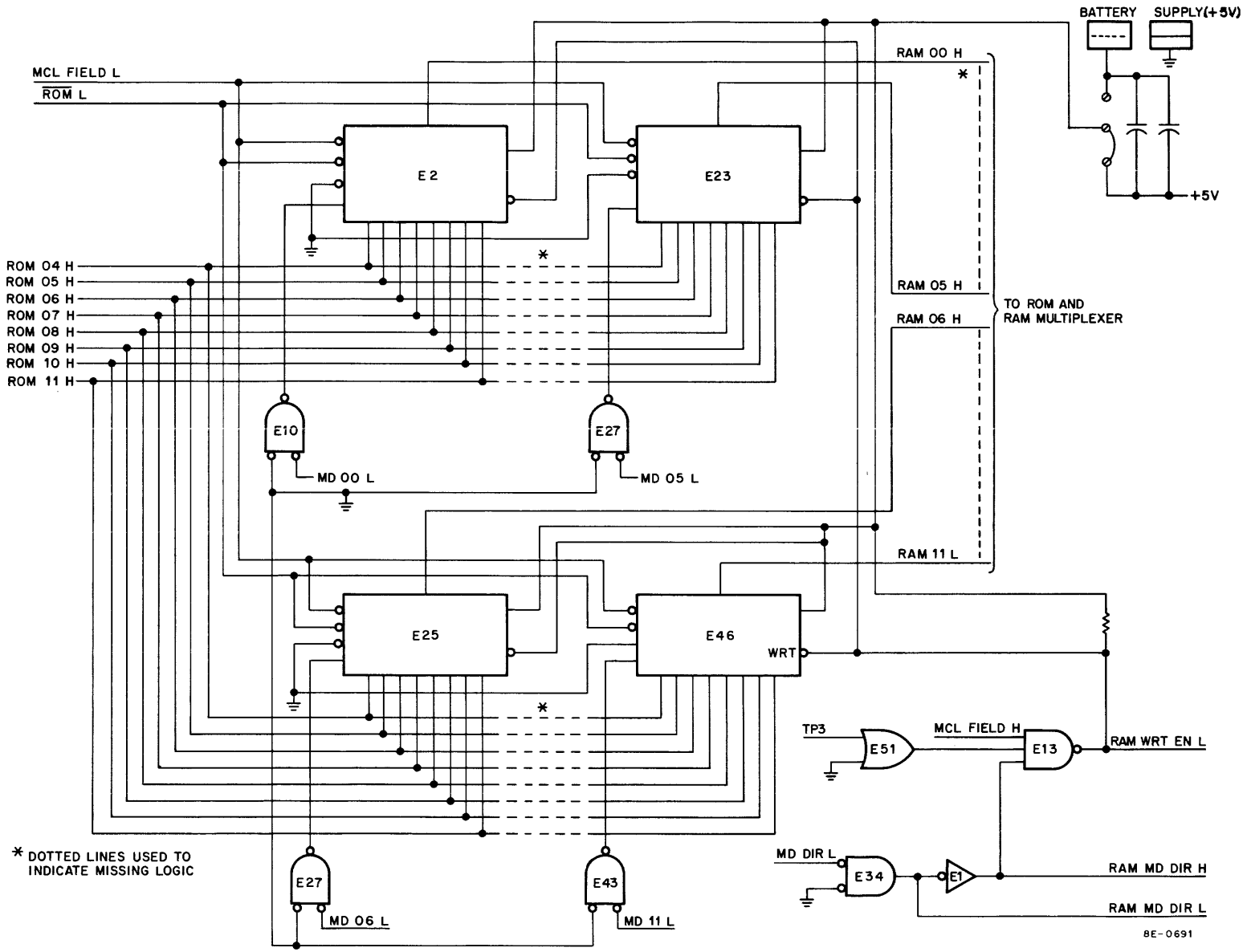


Figure 5-46 RAM Memory (256 Word)

The output of the Data Multiplexer is applied to a Latch Register (E22 and E39) where the selected output is clocked onto the Line Driver Buffer by NTS STALL L (Figure 5-44). The Line Drive Buffers are enabled by MCL FIELD H and RAM MD DIR L. MCL FIELD H is asserted any time this PROM is selected and RAM MD DIR L is high during read operations.

5.16 MAINTENANCE

The general procedures concerning preventive and corrective maintenance are given in Chapter 8. When a malfunction in the MR8-FB is suspected, the technician should use the diagnostic programs to determine the nature of the problem. Refer to option schematic drawing E-CS-M8349-0-0 for IC locations and pin numbers. Test points are provided on the module to facilitate trouble-shooting.

NOTE

If any 1702A PROM chips are changed during a trouble-shooting or maintenance operation, all of PROM must be erased and reprogrammed.

SECTION 4
CORE MEMORY SYSTEMS

5.17 MEMORY SYSTEM, GENERAL DESCRIPTION

The standard PDP-8/A core memory, designated MM8-AA(8K) or MM8-AB(16K), is a random access, coincident-current, magnetic, read/write memory with a cycle time of 1.5 microseconds. The memory includes ferrite cores wired in a 3-D, 3-wire, planar configuration. The basic unit can store up to 8192 (8K) of 16384 (16K) 12-bit words, and can be expanded to 32K words in 8K or 16K increments.

5.18 MEMORY SYSTEM, FUNCTIONAL DESCRIPTION

The memory system performs three basic functions for the PDP-8/A processor:

1. It decodes and selects the desired core location in which a 12-bit word is stored or will be stored.

2. It reads a 12-bit word from the selected location.

3. It writes a 12-bit word into the same selected location.

These functions are illustrated in Figures 5-47 and 5-48, for which one memory cycle is represented. The MA register in the CPU is loaded at the beginning of the memory cycle. The address bus (MA0-MA11) will have settled at the memory 50 ns before the SOURCE H (high) signal on AL2. Memory address decoders receive the MA bits and turn on the corresponding driver and sink current selection switches. XY current flows when the read or write current source is pulsed by the internal memory timing.

The outputs from the 12 selected cores are fed to their respective sense amplifiers. A strobe signal is used to gate the sense amplifier into the Sense Register. If MD DIR L is low (as it always is during the READ portion of the memory cycle), the output of the Memory Register is placed on the MD lines. During the write portion of the memory cycle, the memory selection system uses the same address inputs and control signals; however, control signal WRITE H will go high, causing the write current switches to be activated. To write the content of the Sense Register back into core, MD DIR L will be low (active). Otherwise, the content of the Sense Register will be inhibited from being placed on the MD lines, and a word from the processor will be written into core. The Sense Register is an integral part of the Sense Amplifier. The INHIBIT TIME 2A L signal from the timing circuit controls the gating circuits, and only when INHIBIT TIME 2A L is low will the Inhibit Drivers be activated. A logic zero received from the MD lines and INHIBIT TIME 2A L causes the corresponding Inhibit Driver to produce inhibit current.

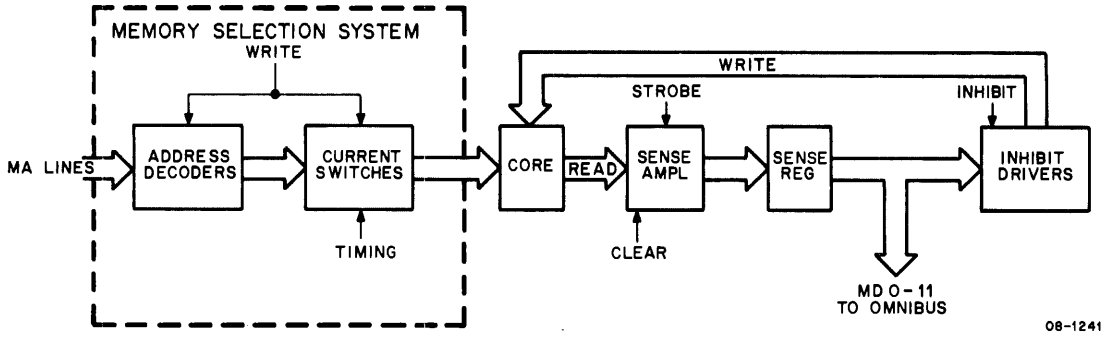


Figure 5-47 Core Memory System Functional Block Diagram

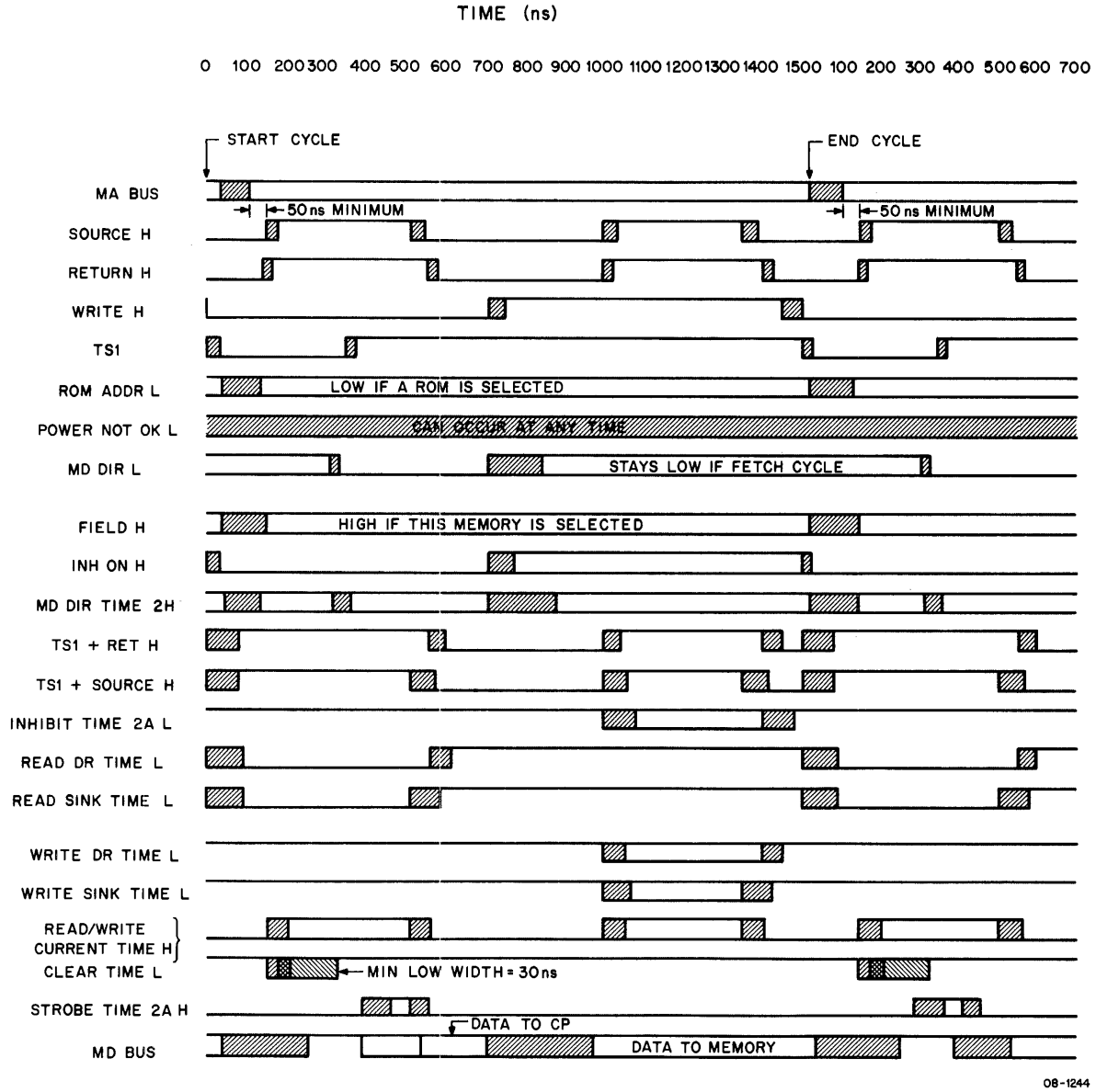


Figure 5-48 Core Memory Timing Diagram

5.19 MM8-AA 8K CORE MEMORY SYSTEM

The organization of the MM8-AA memory system is illustrated in Figure 5-49. One hex-size board with a piggy back H219A stack board is used to contain the memory system as follows:

1. G649 baseboard contains 12 Sense Amplifiers, Memory Registers, and Inhibit Drivers with the corresponding control logic, and current control, address decoding, selection switches, X-current source, Y-current source, and Power Fail circuit.

2. H219A Memory Stack contains 12 mats of 8192 cores per mat, X/Y diode selection matrix, and Stack charge circuit.

5.19.1 Memory Core

The basic storage element in the MM8-AA Memory System (and in the MM8-AB, as well) is a small (18 Mil OD), toroidal (ring-shaped) piece of ferrite material called a magnetic core. A single core, mounted on a ground plane, is illustrated in Figure 5-50. Three wires pass through each core to accommodate the X- and Y-selection and the sense/inhibit function.

5.19.2 Hysteresis Loop

The characteristics of the magnetic core can be shown by a graph, plotting the current (the magnetizing force) versus flux-density (the resulting magnetism) hysteresis loop as illustrated in Figure 5-51. This hysteresis loop illustrates the magnetizing current, I, produced by the current contained in the three wires plotted along the horizontal axis, and the resulting flux density, beta, through the core along the vertical axis. Two directions of current are shown.

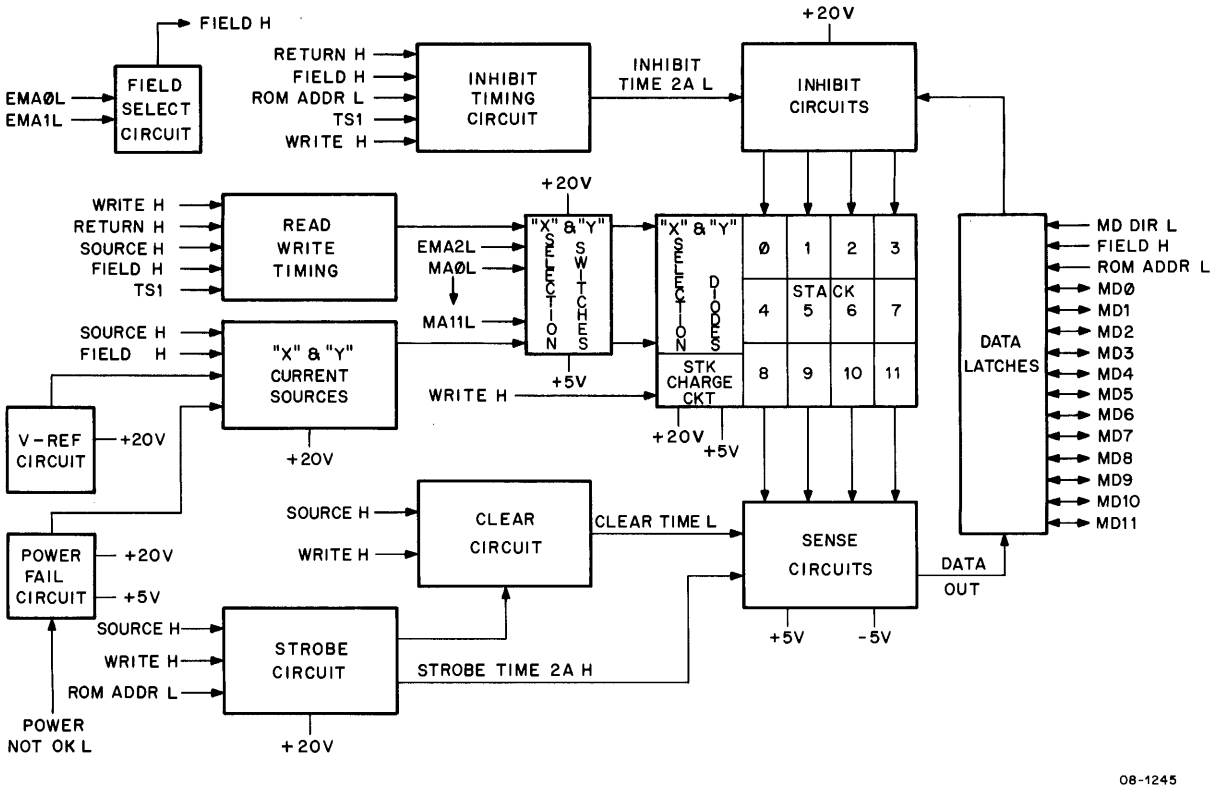


Figure 5-49 MM8-AA Core Memory Block Diagram

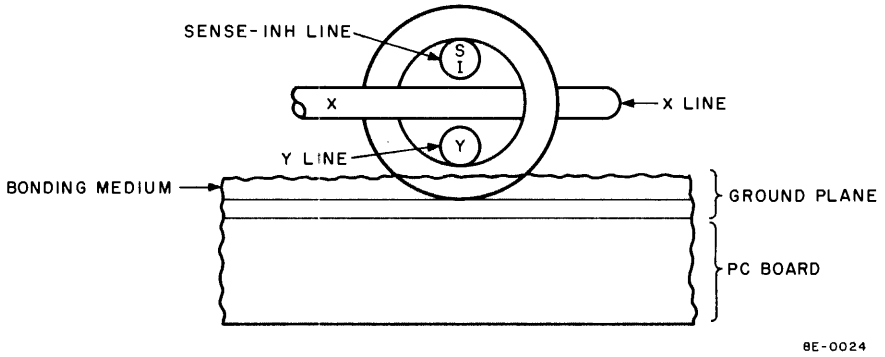


Figure 5-50 Magnetic Core

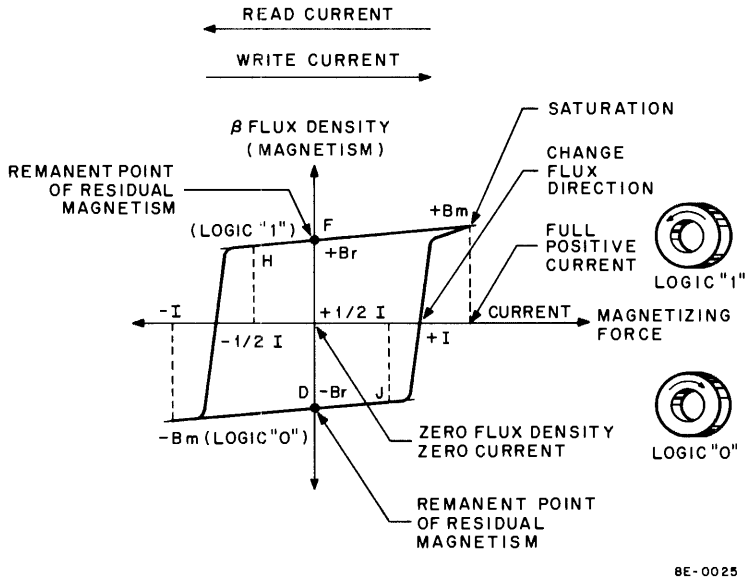


Figure 5-51 Magnetic Core Hysteresis Loop

Read current, with respect to the graph, is directed from right to left. If a logic 1 is stored in the core, B will move from the remanent point, +Br, down to saturation at -Bm when the read current is turned on. When the magnetizing current is removed, the flux density settles down to the remanent point at -Br. Write current is directed from left to right with respect to the graph. If a 1 is to be written into core, the flux density will move from the point -Br to point +Bm on the graph and then settle down to +Br when the magnetizing current is removed. Thus, points -Bm and +Bm are the extreme saturation points, and points -Br and +Br are the extreme points in the normal logic states.

5.19.3 X/Y Select Lines

X/Y drive selection is accomplished by the coincidence and addition of two half select currents at one core in each bit of the word length. All other cores on these activated X/Y lines will see only one half select current and will not switch. A half selected core in the one state will move from +Br to H and move back to +Br at the end of the read current. During write a half selected core will move from -Br to J and return to -Br.

5.19.4 Read Operation

Read occurs during the first half of the memory cycle. Its function is to sample either a logic 1 or logic 0 fully selected core. Thus, both the X- and Y-read half-select currents must be applied for the Sense/Winding to receive a signal resulting from the switching of flux in a core storing a 1. If the core is in logic 0 state, no change in flux state occurs and, therefore, no signal appears on the Sense/Line.

5.19.5 Write Operation

Write occurs during the second half of the memory cycle. Because write follows read, the cores at the selected address have been cleared to a logic 0 state. If the fully selected core (X- and Y-currents) is not inhibited, the magnetic flux moves from point –Br to +Bm then returns to +Br on the graph, and a logical 1 is stored in the core. However, to store a 0 in core, it is necessary to cause a less than fully selected condition. This can be achieved by generating an inhibit current and applying this current to the Sense/Inhibit line. If this inhibit current is in the opposite direction to the X- and Y-current, the net result of the change in flux will be from point –Br to point J on the graph. The resultant effect is the cancelling of half of the full current required to switch the state of the core. When all currents are removed, the flux state reverts back to –Br on the graph.

5.19.6 Magnetic Core In Two-Dimensional Array

A partial three-wire memory configuration is illustrated in Figure 5-52. Half-select currents are produced for one X-line and one Y-line. If, for example, the core at X3, Y2 is selected, the corresponding wires going through each row would contain half-select current. For the X3 row, Y1 core would contain only half-select current, and Y2 core would contain full-select current. All other cores in row Y2 would contain half-select current. The Sense/Inhibit line terminates at the Sense Amplifier and the Inhibit Driver in the manner shown in Figure 5-52. There are two termination points on the Sense Amplifier side, and one termination point at the Inhibit Drivers.

The third wire (the Sense/Inhibit line) receives the resulting signal from the core which sees coincident current. Y Read current direction is from the top of the illustration down. Y Write current direction is from the botton of the illustration to the top. The Inhibit current opposes the Y write current in those cores where zeros are to be written.

5.19.7 Assembly Of 12-Stacked Core Mats

The MM8-AA Memory is a 128 × 64 configuration (128 X-rows and 64 Y-rows). This configuration provides 8,192 cores per mat, for which one core can be selected during any one memory cycle and therefore, one bit of information per mat.

The memory stack component layout is illustrated in Figure 5-53. Figure 5-54 illustrates the X- and Y-windings within memory stacks.

The MM8-AA is a 12-bit word memory system; thus, 12 mats are used. Each mat stores one unique bit of information, which is detected and sensed by one unique line called the Sense/Inhibit line. Sense/Inhibit lines are used to detect and sense 12 unique bits of information. The arrangement of the X select lines is quite different from that of the Y axis. All 12 mats contain 128 X-lines and 64 Y-lines. The threading of each of the X- and Y-lines continues from one mat to the next through all 12 mats. For example, row X31 of mat 0 is common to row X31 of mat 1, which is common to all subsequent mats at row X31. The common factor to each mat is the selection line that is threaded through 12 × 64 cores or 768 cores. The intersection of X31 and Y29, therefore, occurs 12 times in the 12 mats. Because each mat contains a unique Sense/Inhibit line, 12 unique bits of information can be stored to form a 12-bit word.

5.19.8 Core Selection System

Core selection is accomplished by enabling the desired X-line and the desired Y-line and allowing current to pass through the selected lines. To accomplish the selection of the X- and Y-lines, a decoding network that receives the Memory Address bits and decodes for line selection is required. An X- and Y-current source is also required.

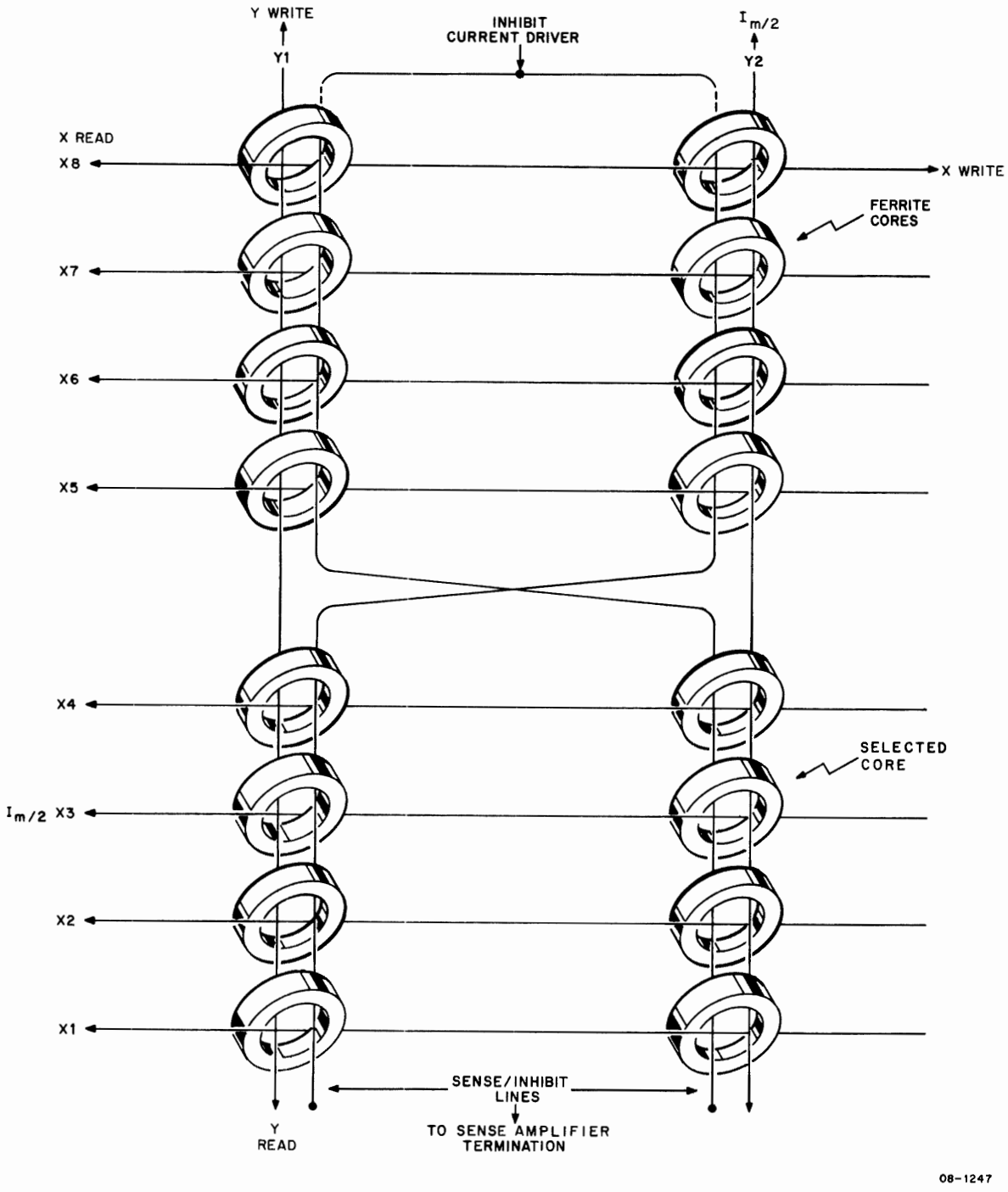
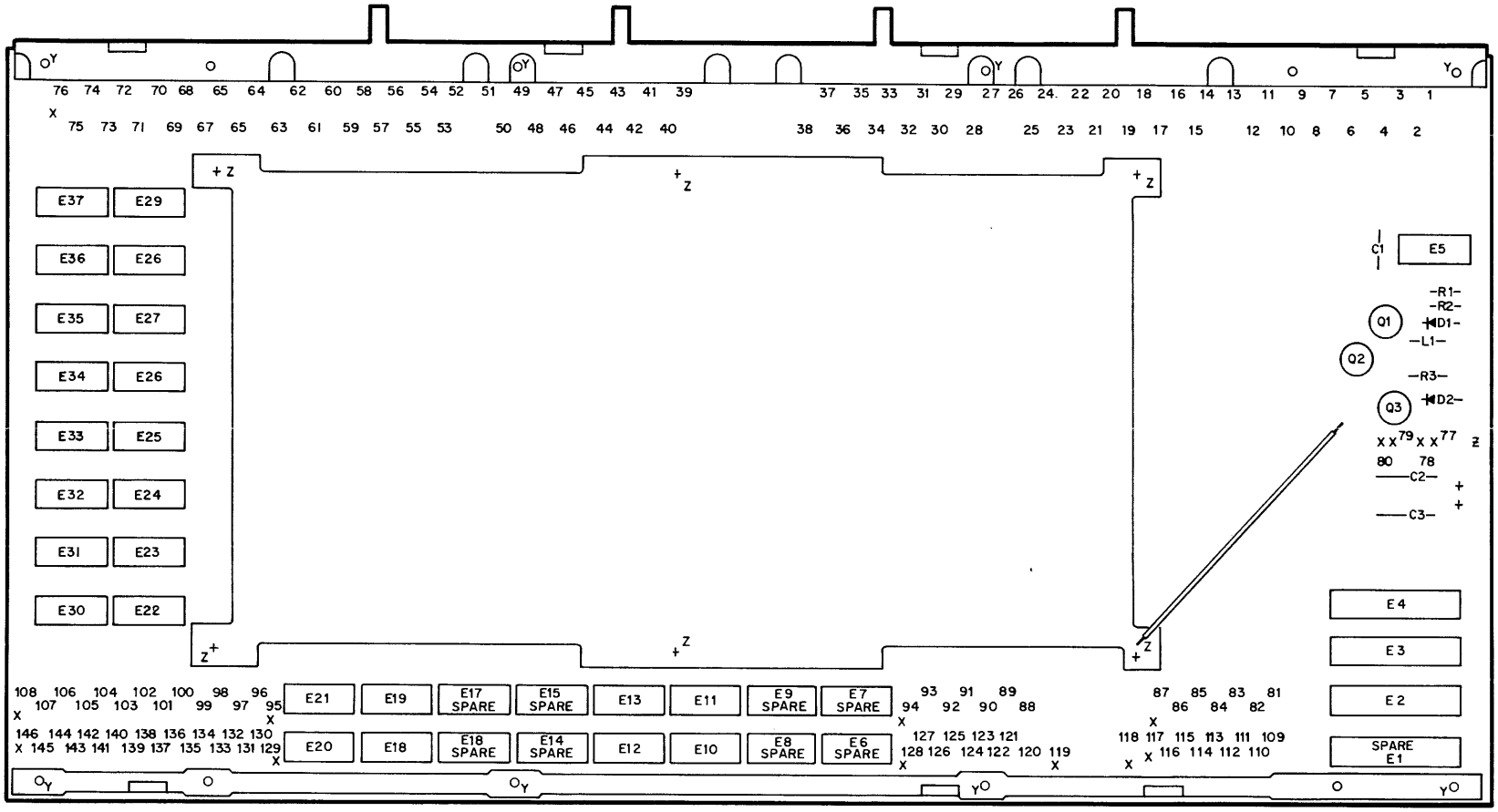


Figure 5-52 Three Wire Memory Configuration



NOTES:
1. E1, E6 thru E9, and E14 thru E17 are spares and these spaces are not used on the MM 8-AA. These spares are used on the MM 8-AB to expand from 8K to 16K.
2. Omit plus, 79, 118, 119.

08-1211

Figure 5-53 Core Stack Layout

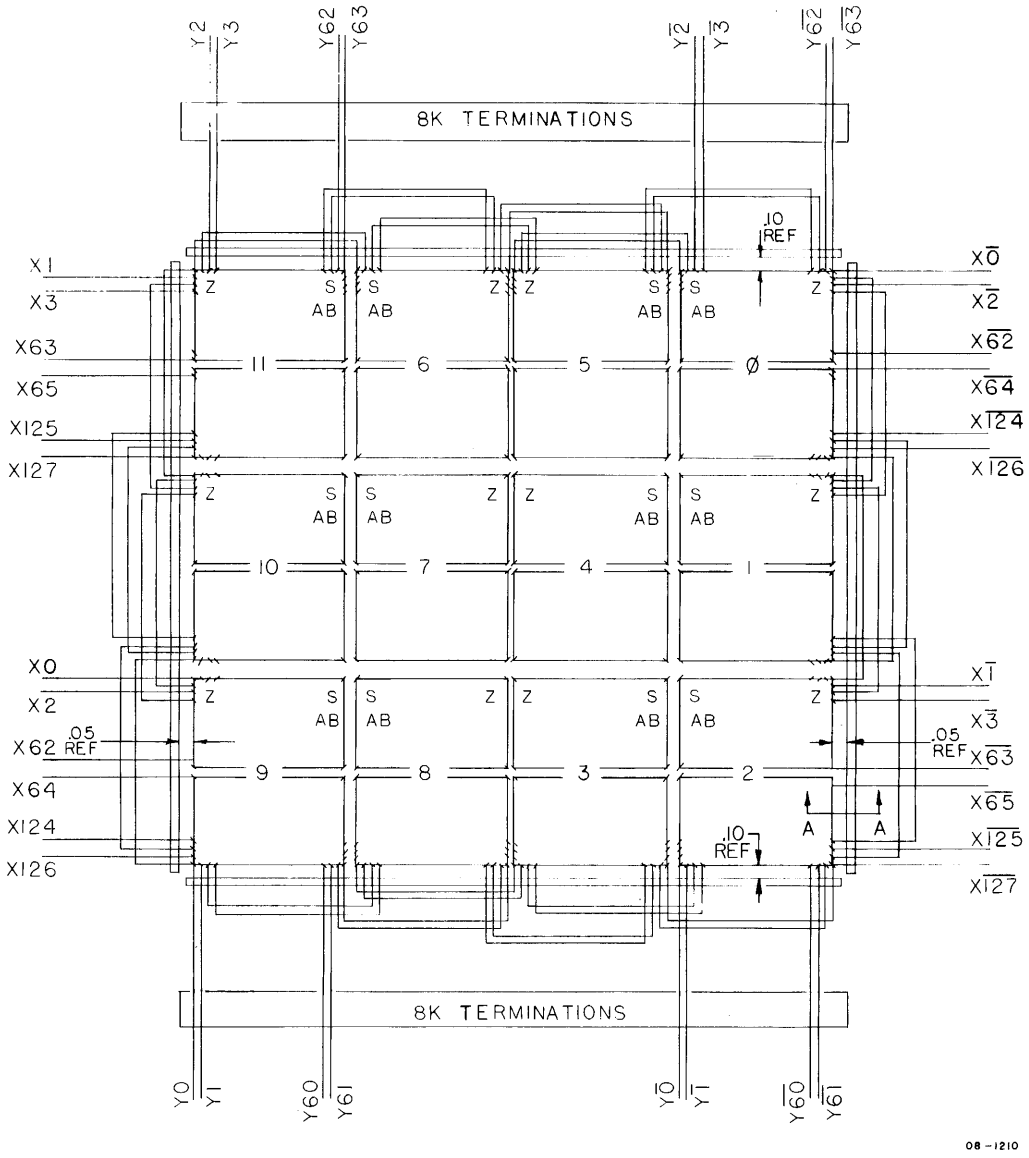


Figure 5-54 8K + 12 Bit Stack and Sense Lines

In the block diagram (Figure 5-49) the primary selection components involved are:

1. The Memory Address decoder, which receives Memory Address bits and control signals to select (enable) the corresponding switch and driver.

2. An X and Y current source to provide the necessary select X and Y currents.

3. A source or driver switch and a sink to apply current to the selected row and to forward-bias the selection diode.

4. One read or write diode in the selection diode block becomes forward-biased by the driver and switch, while all other diodes are back-biased by the stack charge circuit.

5. One selected X row containing 768 cores and a selected Y row containing 1536 cores.

A simplified view of one selected read/write path is shown in Figures 5-55 and 5-56.

5.19.9 Organization Of X/Y Drivers And Current Source

Figure 5-57 illustrates the organization and decoding of the X/Y drivers and current source, and the primary signals required to make line selection and current switching possible. Five decoders are used to select one of 128 X-lines and one of 64 Y-lines as determined by the content of bits MA0 through MA11. A pulsed X- and Y-current, provided by the X- and Y-current source, are applied to the drivers. The read timing signals are applied directly to the 75325 IC read drivers and sinks which switch current through the stack. The write operation uses similar decoding.

5.19.10 X And Y Current Sources – General Description

The current source will be described in more detail in Paragraph 5.19.31.

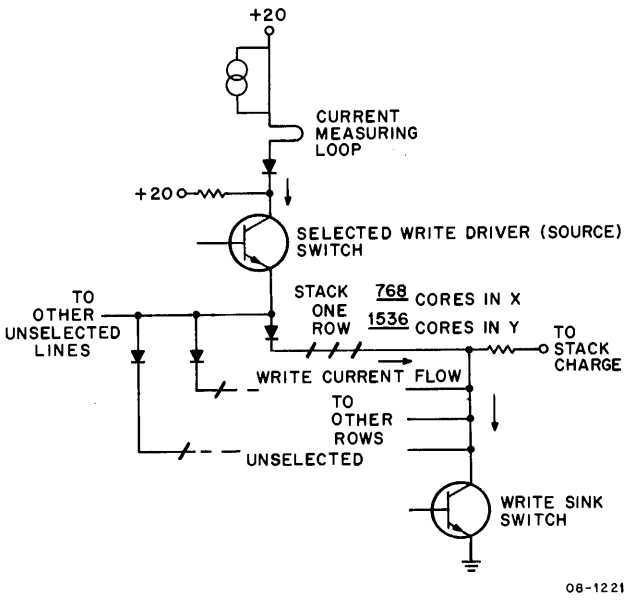


Figure 5-55 Current Path For Write Current

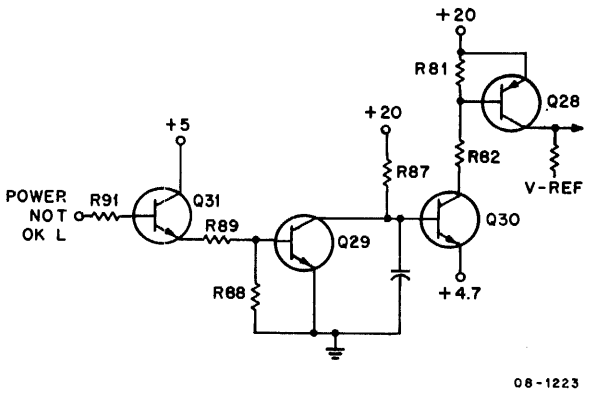


Figure 5-56 Current Path For Read Current

The two current sources supply temperature-dependent X/Y currents to the memory stack selection switches. The current sources are turned on after the stack selection switches and it is the timing input to the current source which determines the position and the width of the stack current. The amplitude of the current is proportional to a reference voltage which tracks the temperature of the baseboard.

5.19.11 Stack Charge Circuit

The Stack Charge circuit (Figure 5-58) switches the stack charge voltage from near ground for a read operation to near +20 V for a write operation. When control signal WRITE H is negated, level shifting circuits along with an output transistor Q2 switch the output to ground. When WRITE H is asserted, the output switches to +20 V. The stack charge driver provides the reverse bias condition on the non-selected diodes in the memory stack. Reverse biasing the non-selected diodes eliminates sneak currents. Refer to Paragraph 5.19.15 for the organization of the planar stack diode matrix.

5.19.12 Power Fail Circuit

The power fail circuit (Figure 5-59) responds to the POWER NOT OK L signal from the processor. Its primary function is to ensure that selected memory locations are not changed due to a power failure. The power supply senses a voltage change when the dc voltage drops and grounds the POWER NOT OK L line before the voltage becomes too low. Less than 20 μs later, the memory timing chain is shut off. Between 20 and 50 μs after the POWER NOT OK L signal is asserted, the memory power fail circuitry turns off the X- and Y-current sources. When the machine is turned on initially and the POWER NOT OK L signal is asserted, access to the memory is not allowed until 50 μs after power has been applied.

5.19.13 Core Selection Decoders

Five decoders (7442 ICs) (Figure 5-57) are used to decode Memory Address register bits MAR0 L through MAR11 L and EMA2 L. These bits are combined with WRITE H, FIELD H, TS1, SOURCE H, and RETURN H signals to enable the appropriate sink and source switches. Signal WRITE H INV is generated when WRITE H is not asserted, while WRITE H BUF is asserted along with WRITE H. The WRITE H signal is developed in the Timing Generator during the last half of the memory cycle. SOURCE H is necessary to turn on the selected read and write sinks, and RETURN H is necessary to turn on the selected source switches. Both RETURN H and SOURCE H are developed in the Timing Generator. RETURN H remains on for 50 ns longer than SOURCE H to minimize power dissipation in the 75325 IC switches.

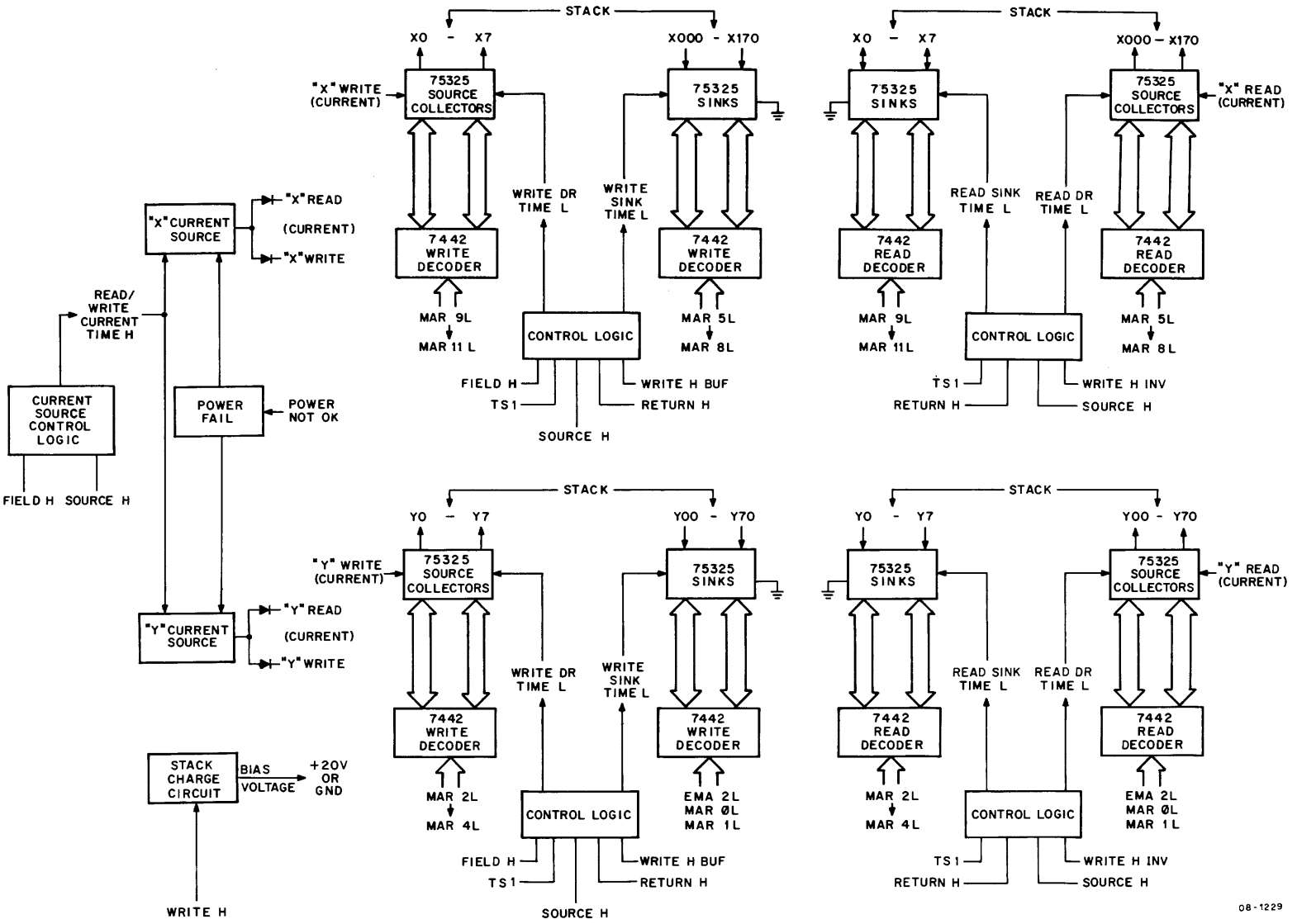


Figure 5-57 Decoding of X and Y Driver Current Sources Block Diagram

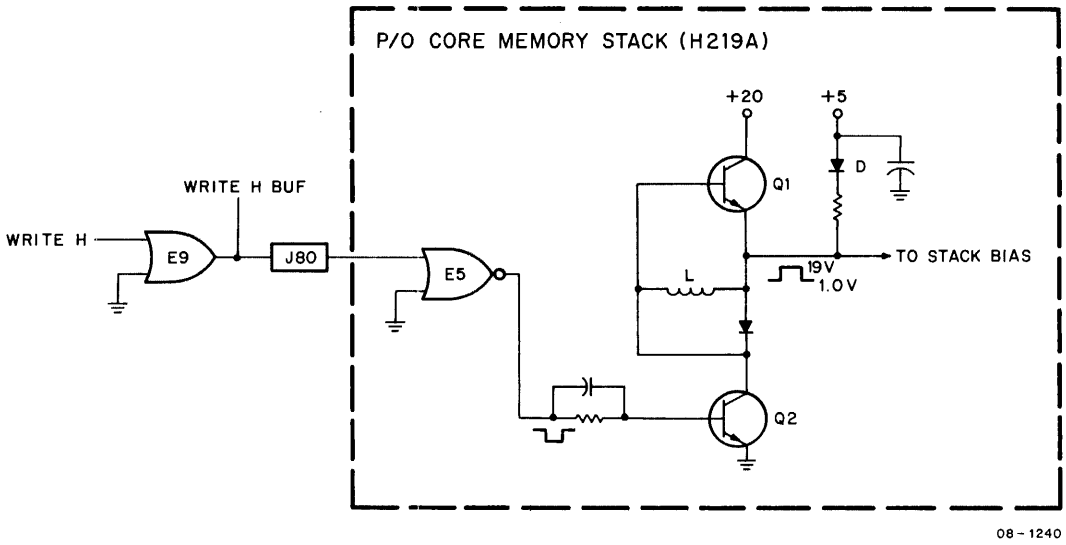


Figure 5-58 Stack Charge Circuit

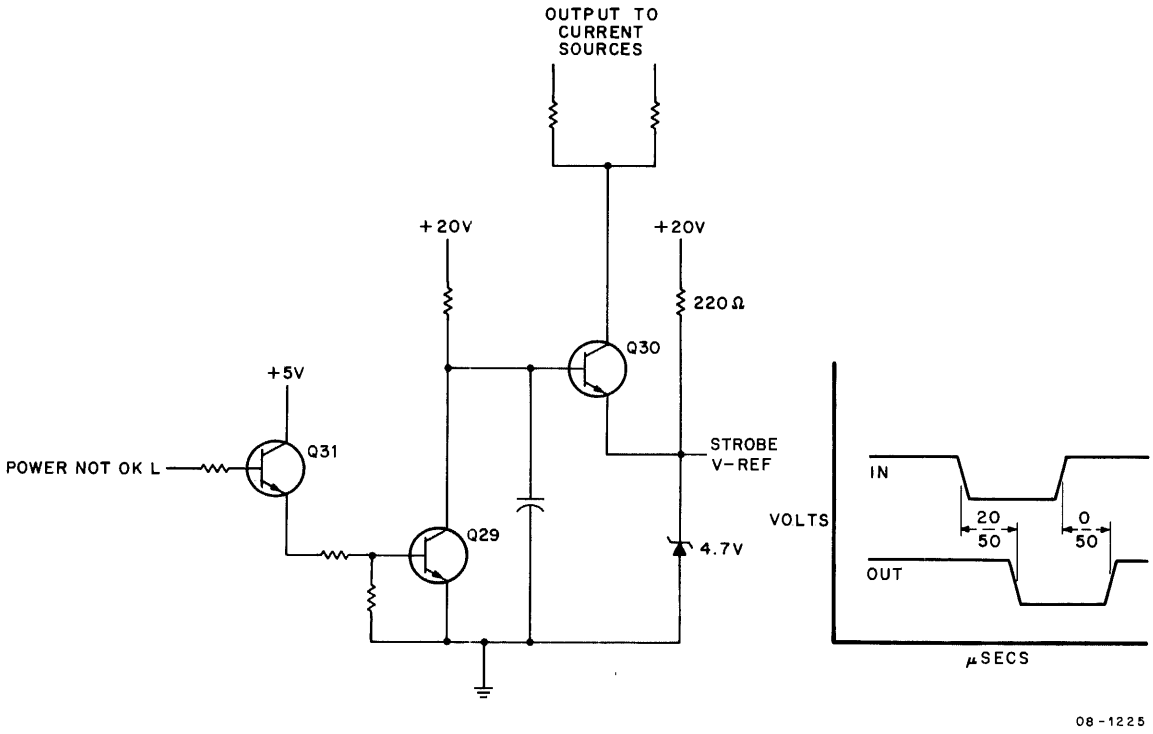


Figure 5-59 Power Fail Circuitry

5.19.14 Address Decoding Scheme

The block diagram in Figure 5-57 illustrates the method used to decode the MAR bits and EMA2 L. The process turns on either a write or read source collector and the corresponding sink, thereby completing a current path through the stack. The decoder is arranged as follows: The write selection decoders are on the left side of the illustration and the read selection decoders are on the right side. The X selection decoders decode bits MAR5 L through MAR11 L. The Y selection decoders decode bits EMA2 L and MAR0 L through MAR4 L. The X decoding scheme consists of a 16 X 8 matrix; the Y decoding scheme consists of an 8 X 8 matrix. The decoder outputs are applied to the selected switches. The outputs of the selected switches connect to the selection diodes (Paragraph 5.19.5) which, in turn, are connected to lines that are threaded through the memory cores. The arrangement of the illustration (Figure 5-57) permits correlation with the engineering drawing schematics (G649).

The decoding scheme of the MAR bits and the EMA bits is illustrated in Figure 5-60. The illustration shows the five parts of the the memory address, what is decoded, and where in the field of the drawing the decoders are located. Table 5-12 lists the necessary input control signals, the content of the memory address, the input pins, the output pins, and the selected X- or Y-line. With this information, the user can easily trace through all of the components on any signal/current path to find the selected components.

5.19.15 Diode Selection Matrix

Each of the X- and Y-select lines are connected to a corresponding string of diodes (Figure 5-61). Selection is such that any one of the eight upper select lines will pass current in a path determined by whether it is a read or write operation. In Figure 5-61, for X-selection, the example illustrates line X(12) being selected. The current passes through 768 cores and back through one of the diodes. The path the current takes from this point is determined by the diode that is forward-biased. The forward-biasing of a diode is accomplished by operating the switch and driver. If it is a write operation, WX2 is forward-biased and the current takes the path from WX2 to X10. If it is a read operation, RX2 is forward-biased and the current takes the path from X10 to RX2. All diodes except the selected diode are reverse-biased.

5.19.16 Operation Of Selection Switches

Figure 5-62 illustrates the switching operation of the currents through X0 select line. On the upper side, a pair of transistors is used to either drive or sink current, depending on whether the operation is read or write. A complementary pair of transistors on the lower side is used to either drive or sink the current. A line between the upper and lower side is threaded through 768 cores. The read operation begins with the decoders. When an X-line such as X0 is to be selected, the read driver and read sink must first be turned on. To turn on the read driver and read sink, the input to the 75325 must be positive with respect to the emitter. This occurs only when the output of the decoder is low (active).

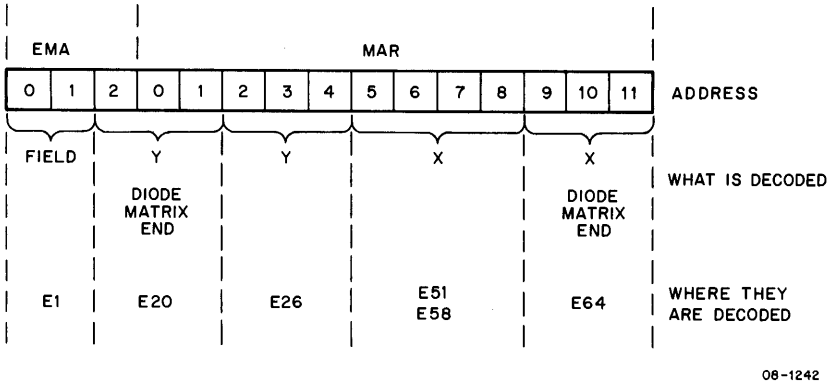


Figure 5-60 Decoding Relationships

Table 5-12
Core Selection Decoding Scheme
"X" READ

Function	Control Logic		MAR5 L ↓ MAR8 L	MAR9 L ↓ MAR11 L	Source Output Pins	Sink Input Pins	Selected Source (Octal)	Selected Sink (Octal)
			0000	—	J101	—	000	—
			0001	—	J136	—	010	—
			0010	—	J100	—	020	—
			0011	—	J135	—	030*	—
			0100	—	J99	—	040	—
Turn on Source Collectors	TS1 + RET H	= H	0101	—	J133	—	050	—
	TS1 + SOURCE H	= H	0110	—	J98	—	060	—
	WRITE H INV	= H	0111	—	J96	—	070	—
	READ DR TIME L	= L	1000	—	J130	—	100	—
			1001	—	J95	—	110	—
			1010	—	J137	—	120	—
			1011	—	J134	—	130	—
			1100	—	J132	—	140	—
			1101	—	J97	—	150	—
			1110	—	J131	—	160	—
			1111	—	J129	—	170	—
			—	000	—	J139	—	0
	TS1 + RET H	= H	—	001	—	J108	—	1
Turn on Sinks	TS1 + SOURCE H	= H	—	010	—	J105	—	2
	WRITE H INV	= H	—	011	—	J107	—	3
	READ SINK TIME L	= L	—	100	—	J142	—	4
			—	101	—	J140	—	5
			—	110	—	J141	—	6*
			—	111	—	J106	—	7

*EXAMPLE: Source Collector = 030
Sink = + 6
(Total) Line Selected = 036 Octal

Table 5-12 (Cont)
Core Selection Decoding Scheme
"X" WRITE

Function	Control Logic	MAR9 L ↓ MAR11 L	MAR5 L ↓ MAR8 L	Source Output Pins	Sink Input Pins	Selected Source (Octal)	Selected Sink (Octal)
		000	———	J103	———	0	——
		001	———	J146	———	1*	——
		010	———	J143	———	2	——
	FIELD H = H	011	———	J145	———	3	——
Turn on	TS1 + RET H = H	100	———	J138	———	4	——
Source Collectors	TS1 + SOURCE H = H	101	———	J104	———	5	——
	WRITE H BUF = H	110	———	J102	———	6	——
	WRITE DR TIME L = L	111	———	J144	———	7	——
		——	0000	———	J101	——	000
		——	0001	———	J136	——	010
		——	0010	———	J100	——	020
		——	0011	———	J135	——	030
	FIELD H = H	——	0100	———	J99	——	040
	TS1 + RET H = H	——	0101	———	J133	——	050
Turn on Sinks	TS1 + SOURCE H = H	——	0110	———	J98	——	060
	WRITE H BUF = H	——	0111	———	J96	——	070
	WRITE SINK TIME L = L	——	1000	———	J130	——	100
		——	1001	———	J95	——	110
		——	1010	———	J137	——	120*
		——	1011	———	J134	——	130
		——	1100	———	J132	——	140
		——	1101	———	J97	——	150
		——	1110	———	J131	——	160
		——	1111	———	J129	——	170

*EXAMPLE: Source Collector = 1
Sink = +120
(Total) Line Selected = 121 Octal

Table 5-12 (Cont)
Core Selection Decoding Scheme
"Y" WRITE

Function	Control Logic	MAR2 L ↓ MAR4 L	EMA 2 L MAR0 L MAR1 L	Source Output Pins	Sink Input Pins	Selected Source (Octal)	Selected Sink (Octal)
		000	—	J93	—	0	—
		001	—	J94	—	1	—
	FIELD H = H	010	—	J120	—	2	—
Turn on	TS1 + RET H = H	011	—	J89	—	3	—
Source Collectors	TS1 + SOURCE H = H	100	—	J124	—	4*	—
	WRITE H BUF = H	101	—	J123	—	5	—
	WRITE DR TIME L = L	110	—	J88	—	6	—
		111	—	J121	—	7	—
		—	000	—	J85	—	00
		—	001	—	J113	—	10
	FIELD H = H	—	010	—	J86	—	20
	TS1 + RET H = H	—	011	—	J114	—	30
Turn on Sinks	TS1 + SOURCE H = H	—	100	—	J87	—	40
	WRITE H BUF = H	—	101	—	J116	—	50
	WRITE SINK TIME L = L	—	110	—	J115	—	60
		—	111	—	J117	—	70*

*EXAMPLE: Source Collector = 4
Sink = +70
(Total) Selected Line = 74 Octal

Table 5-12 (Cont)
Core Selection Decoding Scheme
"Y" READ

Function	Control Logic		EMA 2 L EMA 0 L EMA 1 L	MAR2 L ↓ MAR4 L	Source Output Pins	Sink Input Pins	Selected Source (Octal)	Selected Sink (Octal)
			000	—	J85	—	00	—
			001	—	J113	—	10	—
	TS1 + RET H	= H	010	—	J86	—	20*	—
Turn on	TS1 + SOURCE H	= H	011	—	J114	—	30	—
Source Collectors	WRITE H INV	= H	100	—	J87	—	40	—
	READ DR TIME L	= L	101	—	J116	—	50	—
			110	—	J115	—	60	—
			111	—	J117	—	70	—
	TS1 + RET H	= H	—	000	—	J128	—	0
	TS1 + SOURCE H	= H	—	001	—	J126	—	1
Turn on Sinks	WRITE H INV	= H	—	010	—	J90	—	2
	READ SINK TIME L	= L	—	011	—	J91	—	3
			—	100	—	J127	—	4
			—	101	—	J125	—	5*
			—	110	—	J122	—	6
			—	111	—	J92	—	7

*EXAMPLE: Source Collector = 20
Sink = + 5
(Total) Selected Line = 25 Octal

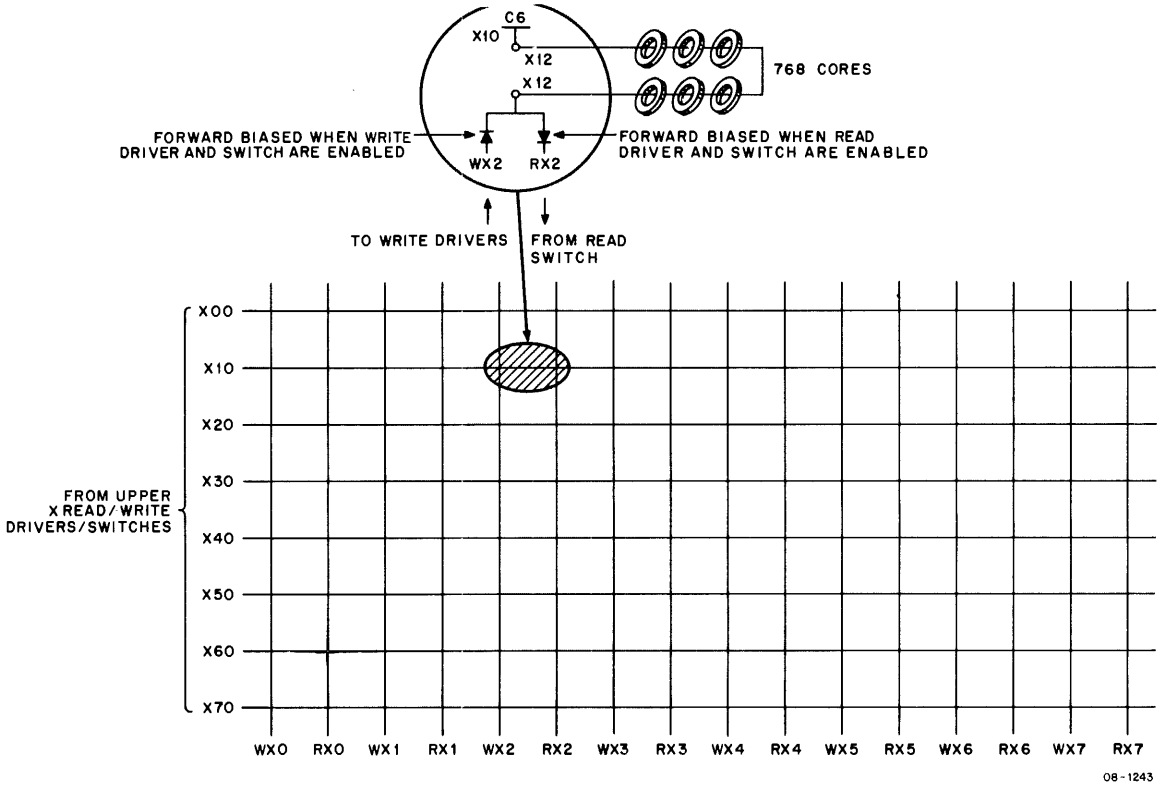


Figure 5-61 Organization of Planar Stack Diode Matrix For X Select Lines

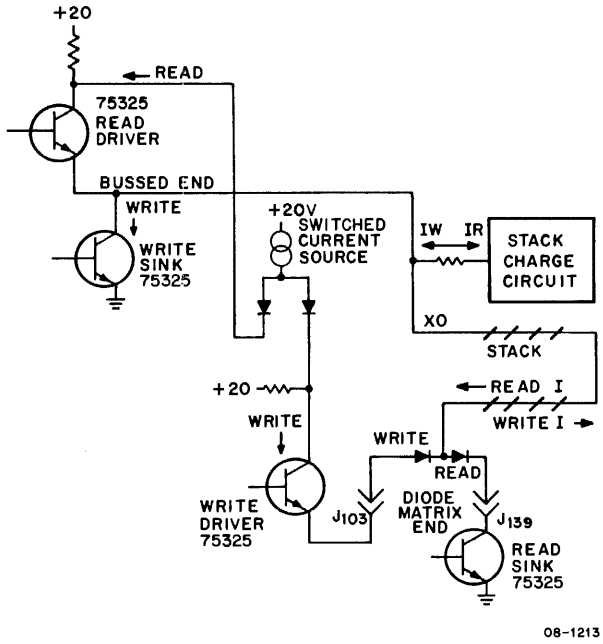


Figure 5-62 Operation Of Selection Switches To Select Line X0

5.19.17 Operation Of The Core Selection Switches

The cores that contain a selected X-line and selected Y-line define the location in which a 1 or 0 will be either written in or read out. Figure 5-63 illustrates a small portion of memory and the corresponding X selection devices. The Y decoding is similar and may be obtained from sheet 5 and 6 of the MM8-AA print set in Appendix H. Using Table 5-12, the selection of any given core can be traced from the Memory Address register through the decoders and switches to the selected line and core.

To select the Y read stack line No. 25 (octal), the procedure using Table 5-12 is as follows:

A source collector switch to select one end of the stack line and a sink switch to select the other end of the stack line must be turned on together. This completes the current path from the current source through the source collector switch, through the selected stack line, through the sink switch to ground.

Addresses EMA2L, EMA0L and EMA1L are decoded to select any 1 out of 8 source collectors – in our example we are selecting the address combination that gives us binary 010 (octal 2).

Addresses MAR2 L, MAR3 L, and MAR4 L are decoded to select any 1 out of 8 sink switches. In our example we are selecting the address combination that gives us binary 101 (octal 5). Table 5-13 shows selected stack lines for all combinations of selected source collectors and selected sinks.

When a read driver and sink pair are selected and the current source is pulsed, a read current will flow from current source through read driver, stack diode matrix, and read sink to ground. During the read time period the state of the stack charge circuit output will be low. The function of the stack charge circuit during read is to hold all lines except the selected line to ground to prevent forward biasing the nonselected read diodes.

One current source is shared by the read and write source switches. The description of the write operation is similiar to the above description of the read operation. The exception is the level of the stack charge circuit output which will be in a high state of approximately 20 V. The function of the stack charge during write is to back bias the unselected write diodes.

5.19.18 Sense/Inhibit Function

The previous paragraphs have described the memory core, the selection of memory core, and the selection of memory core in terms of the read/write operation. However, to perform a read or a write operation, sense amplifiers are necessary to sense the state of the selected cores, and inhibit drivers are necessary to write 0s into core. Control logic and data registers are also required to control the data flow to and from memory. These necessary circuits are illustrated in a simplified diagram (Figure 5-64). The circuits designated correspond to bit 0.

5.19.19 Sense/Inhibit Line

The line that is used to sense a 1 during read is also used to transmit inhibit current when a 0 is to be written during the write portion of the memory cycle. The Sense/Inhibit line passes through 8192 cores of one bit mat. Two ends of this line are terminated through diodes to ground at the input to the Sense Amplifier. The Inhibit Driver feeds a center tap on the Sense Inhibit line (see Figure 5-64).

5.19.20 Read/Write Operation

The read operation involves the Sense Amplifier and the necessary control logic in conjunction with the selection system. During the read portion of the memory cycle, the selected core develops a signal on the Sense/Inhibit line only if a 1 was previously stored in core. The sense registers in the sense amplifier are previously cleared and STROBE TIME 2A H gates either a 1 or 0 into the Sense Register. When a 1 is sensed, the Sense Amplifier applies a low signal to the MD line (Figure 5-64).

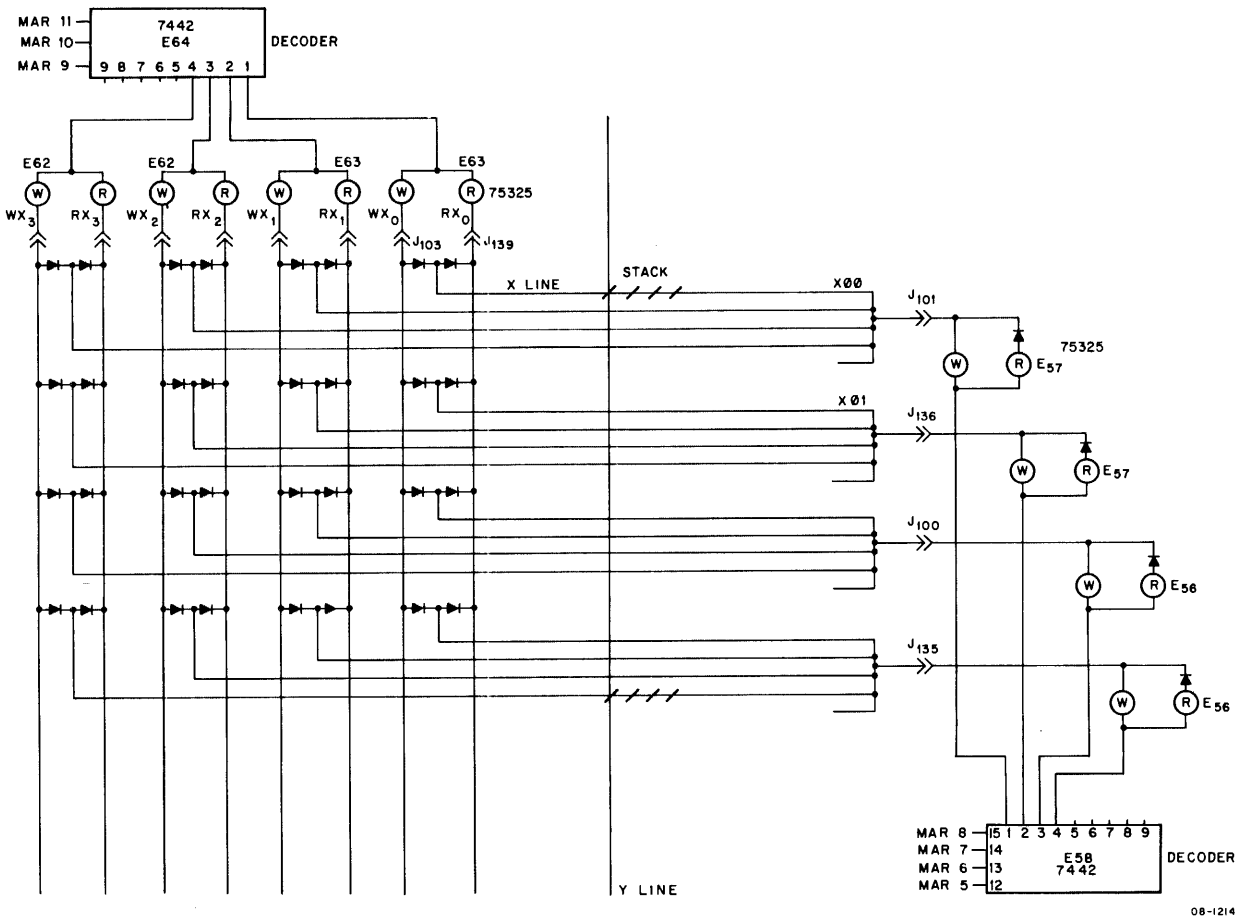


Figure 5-63 Detailed Operation Of Selection Switches

Table 5-13
Core Selection Y READ

Selected Source	Selected Sink							
	0	1	2	3	4	5	6	7
00	0	1	2	3	4	5	6	7
10	10	11	12	13	14	15	16	17
20	20	21	22	23	24	25	26	27
30	30	31	32	33	34	35	36	37
40	40	41	42	43	44	45	46	47
50	50	51	52	53	54	55	56	57
60	60	61	62	63	64	65	66	67
70	70	71	72	73	74	75	76	77

All numbers are in octal.

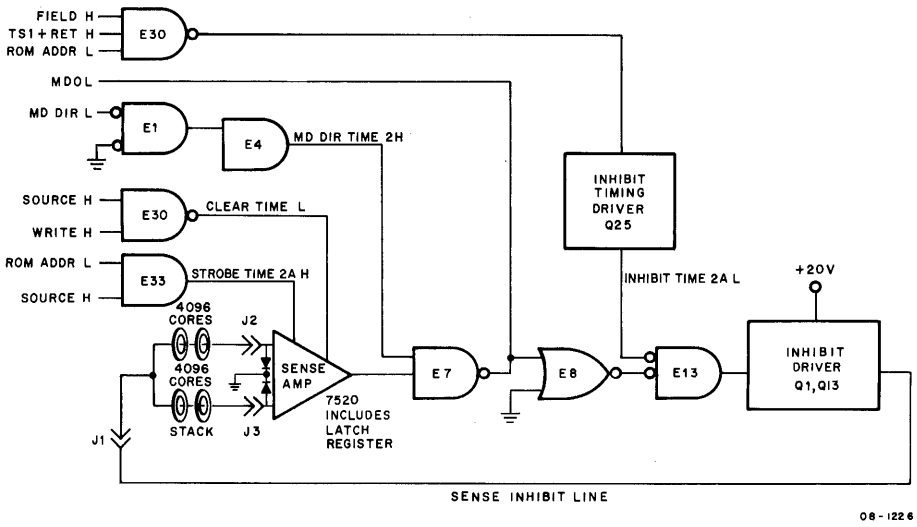


Figure 5-64 Inhibit Operation For Bit 0

The output of the core stack which is stored in the sense register will be rewritten into the same core location during the write half of the timing cycle. The MD DIR L pulse which gates the sense register data to the inhibit driver also puts the same data on the bus where it is available to the CPU or a peripheral device.

The write operation involves the inhibit drivers, load gates such as E7, E8, sense register, and the necessary control logic in conjunction with the selection system. The inhibit driver load gates receive ones and zeros via the MD lines from either the MB register in the processor or the sense register. Control gating signals for the inhibit driver load gate, E13, are:

1. TS1 + RET H
2. FIELD H, which indicates that the proper memory has been selected.
3. Not ROM Address

5.19.21 Inhibit Control Logic

The Inhibit Control logic (Figure 5-65) provides a gating control signal to the inhibit driver during the write portion of the memory cycle. The logic receives RETURN H from the Omnibus, FIELD H from the Field Select Control logic, and TS1 and ROM ADDR L from the Omnibus. The write control bus signal is added into the Field Select Control logic.

5.19.22 Field Select Control Logic

There can be as many as 4 MM8-AA memories in the system, each memory being assigned to one 8K-block of memory addresses. A particular memory responds only to addresses within its assigned block. The logic shown in Figure 5-66 allows the memory to determine if one of its assigned locations is being addressed. If so, the logic asserts the FIELD H signal and data is transferred to or from the addressed location.

The EMA0 L and EMA1 L signals are used to specify an 8K-block of addresses. Selective installation of jumpers in the logic (Figure 5-66) permits the logic to respond to any one of 4 combinations of the EMA signals. For example, the jumper configuration depicted allows the FIELD H signal to be generated when locations in field 0 (0–8K) are addressed, i.e., when both EMA0 L and EMA1 L are negated. Table 5-14 lists the EMA signals and relates them to both assigned memory address blocks and installed jumpers.

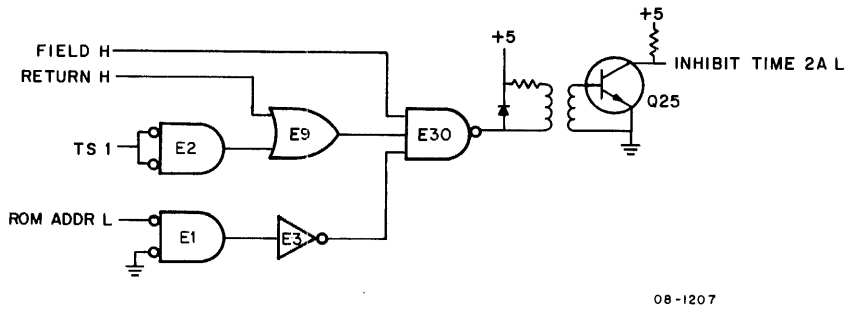


Figure 5-65 Inhibit Control Logic

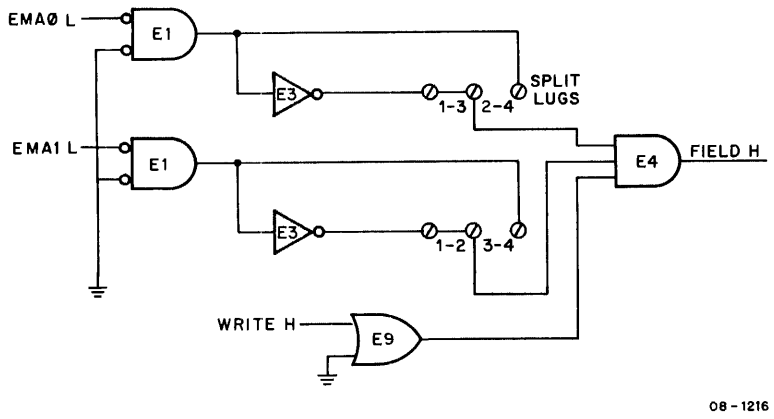


Figure 5-66 Field Select Control Logic

Table 5-14
Address Block Selection

EMA0 L	EMA1 L	Memory Address Block	Installed Jumpers
HI	HI	0–8K	1-3 and 1-2
HI	LO	8K–16K	2-4 and 1-2
LO	HI	16K–24K	3-4 and 1-3
LO	LO	24K–32K	3-4 and 2-4

5.19.23 Sense Register Enable Logic

The sense register enable logic is shown in Figure 5-67. When MD DIR TIME 2 H is asserted, the content of the sense register is gated onto the MD line and to the inhibit driver.

5.19.24 Sense Register Clear Timing

The logic associated with the generation of the CLEAR TIME L signal is illustrated in Figure 5-68. The timing signals are shown in Figure 5-69. The SOURCE H signal triggers flip-flop E39 and creates a low at the output of NAND gate E30. This is the leading edge of CLEAR TIME L, and the trailing edge is determined by the leading edge of the STROBE 0 signal.

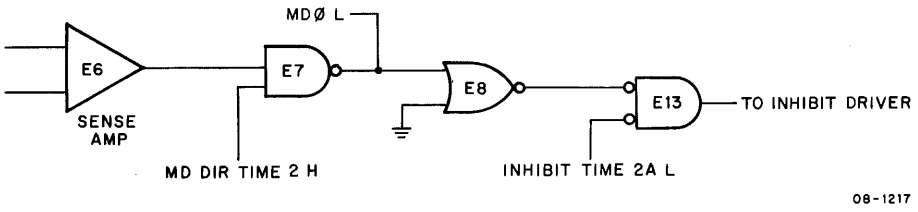


Figure 5-67 Memory Sense Register Enable Logic for Bit 0

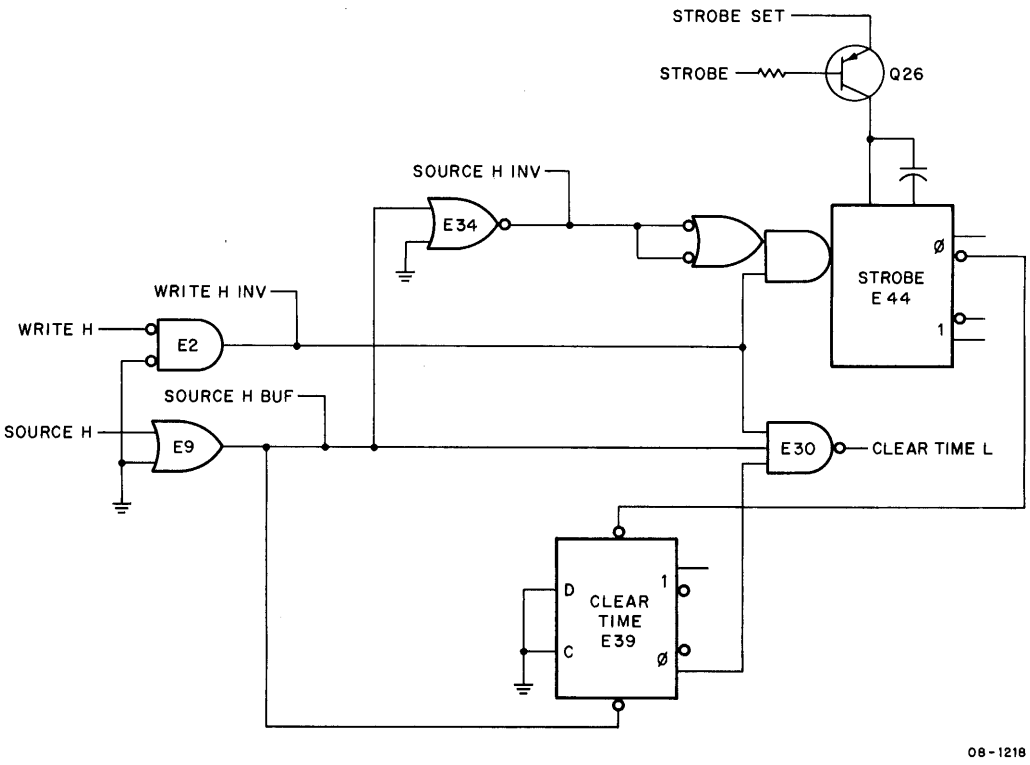


Figure 5-68 Clear Time Control Logic

5.19.25 Strobe Control Logic

The Strobe Control logic is shown in Figure 5-70. The timing signals that generate the strobe are shown in Figure 5-69. SOURCE H triggers the STROBE one-shot, E44, and the trailing edge of the one-shot signal clocks flip-flop E39. The output of E39 determines the leading edge of the STROBE TIME 2A H signal. The trailing edge of STROBE TIME 2A H is set by SOURCE H going low. The width of the STROBE one-shot output is proportional to the amplitude of a constant current supplied by transistor Q26 in the strobe adjustment circuit (Figure 5-71). The current in Q26 and, hence, the position of the strobe may be adjusted through the use of jumpers in the emitter circuit of Q26. These jumpers are shown in Figure 5-71, and Table 5-15 relates the jumper placement to the width of the one-shot output. Paragraph 5.19.26 discusses the jumper placement in detail.

5.19.26 Strobe Setting Jumpers

The jumper configuration is used to adjust the strobe position to account for the worst case tolerances in both the strobe one-shot circuitry and its associated timing-logic circuitry. The ability to choose any one of sixteen strobe settings provides the advantage of maximizing the memory margins over the entire operating temperature range.

Table 5-15
Strobe Select Jumpers

W9	W10	W11	W12	Octal Equivalent	Decimal Equivalent	
0	0	0	0	0	0	
0	0	0	1	1	1	
0	0	1	0	2	2	
0	0	1	1	3	3	
0	1	0	0	4	4	
0	1	0	1	5	5	
0	1	1	0	6	6	
0	1	1	1	7	7	Strobe Time Variation
1	0	0	0	10	8	≈ 3 ns per step
1	0	0	1	11	9	
1	0	1	0	12	10	
1	0	1	1	13	11	
1	1	0	0	14	12	
1	1	0	1	15	13	
1	1	1	0	16	14	
1	1	1	1	17	15	

0 indicates [jumper out]
1 indicates [jumper in]

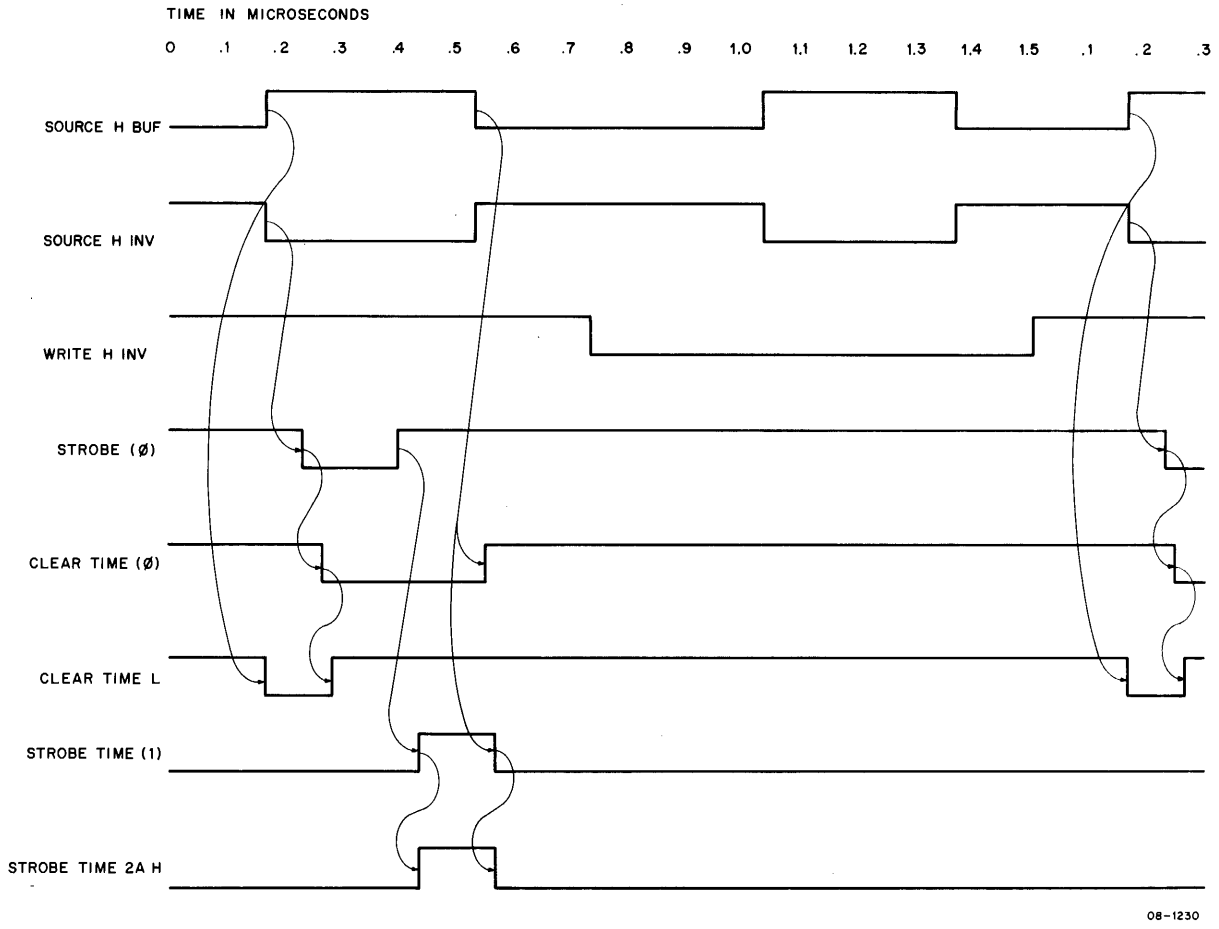


Figure 5-69 Strobe and Clear Timing

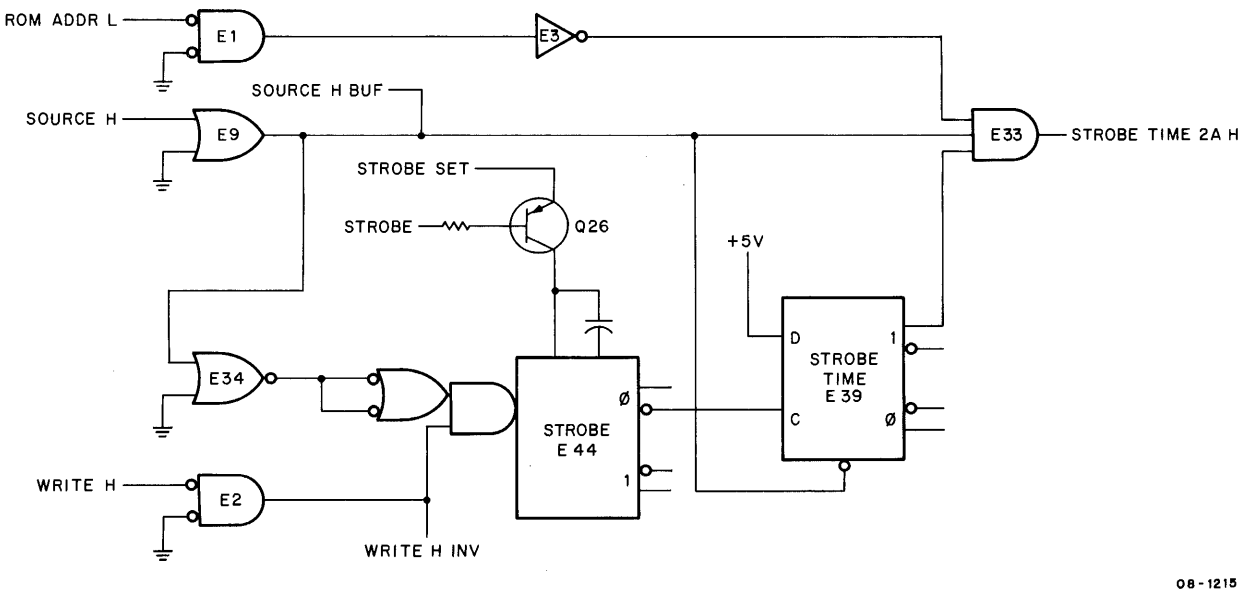


Figure 5-70 Strobe Control Logic

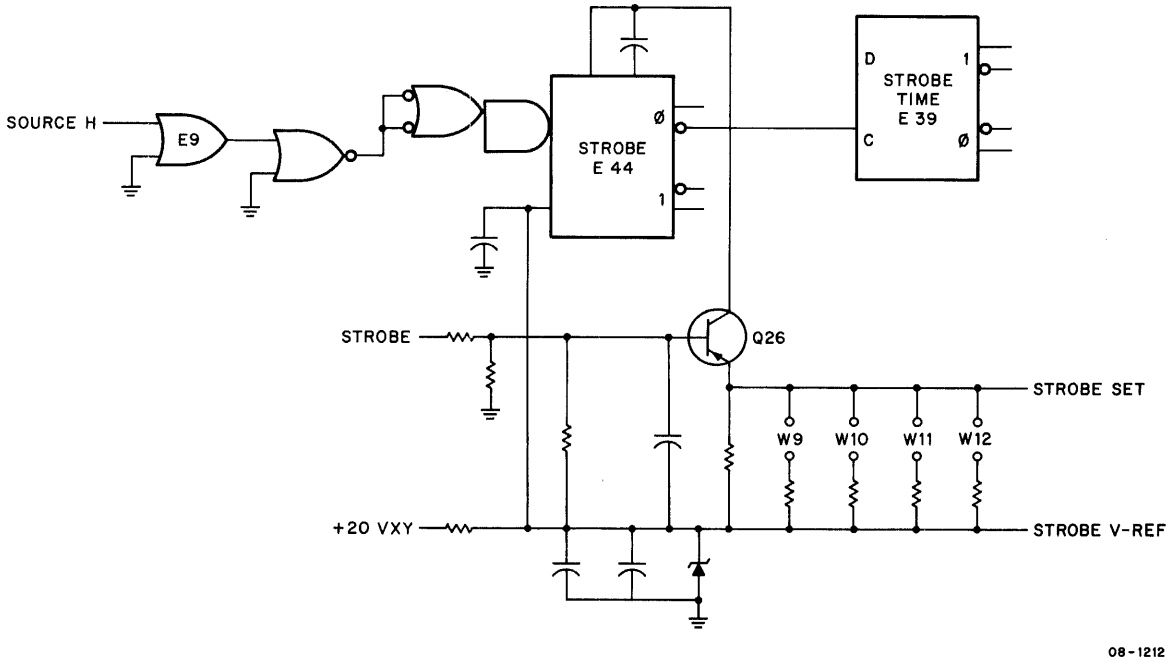


Figure 5-71 Strobe Adjustment

The average strobe setting* is 260 ns from the low-to-high transistion of SOURCE H (430 ns from time zero T_0). With all jumpers (W9–W12) installed the strobe occurs 235 ns from SOURCE H; with all jumpers removed the strobe occurs 280 ns from SOURCE H. Each step between the above two end settings varies the strobe linearly from 235 ns to 280 ns, or 3 ns/step. The exact strobe setting is determined during memory system test using a 2223DA, 60 cycle, 115 V tester with program AUTOCAT-08-DHMBA-X-PB.

5.19.27 Sense Amplifiers

Twelve sense amplifiers (7520 IC) are required to sense signals on the twelve sense lines (Figure 5-72 illustrates one of the sense amplifiers). If the selected core in a given mat contains a 1, a pulse is received on the Sense/Inhibit winding. This pulse is amplified by the sense amplifier and then used to set a logic 1 into the sense register. If the selected core contains a 0, the signal received by the sense amplifier is below threshold, no pulse appears at the output of the sense amplifier, and the sense register remains in the 0 state. The sense amplifier is strobed with a narrow pulse to ensure that the signal on the sense lines is sampled at a time of optimum signal-to-noise ratio. This strobing is necessary because the cores in the 0 state produce noise when sensed and because many of the cores in each mat receive half-selected pulses. The total sum of the noise can be considered delta noise, which apppears at the early portion of the core switching time. The noise generated by the half-selected cores ceases shortly after the half-selected pulses are started. Therefore, the sense amplifier is strobed during the latter part of read time, when the output resulting from a selected core-reversing state is highest in proportion to the noise from half-selected cores (maximum signal-to-noise ratio). Because the delta noise is confined to a smaller amplitude with respect to ground, the strobe control ensures that any sampling of the 1-state occurs after the amplitude of the noise is below threshold.

5.19.28 Sense Register

The only data register in the memory is a latch, which is made up of two gates in the sense amplifier package. The latch is set by a one signal from core and is reset by the clear signal generated in timing. The latch is not set by data from the bus.

* Exact strobe setting varies slightly from system to system.

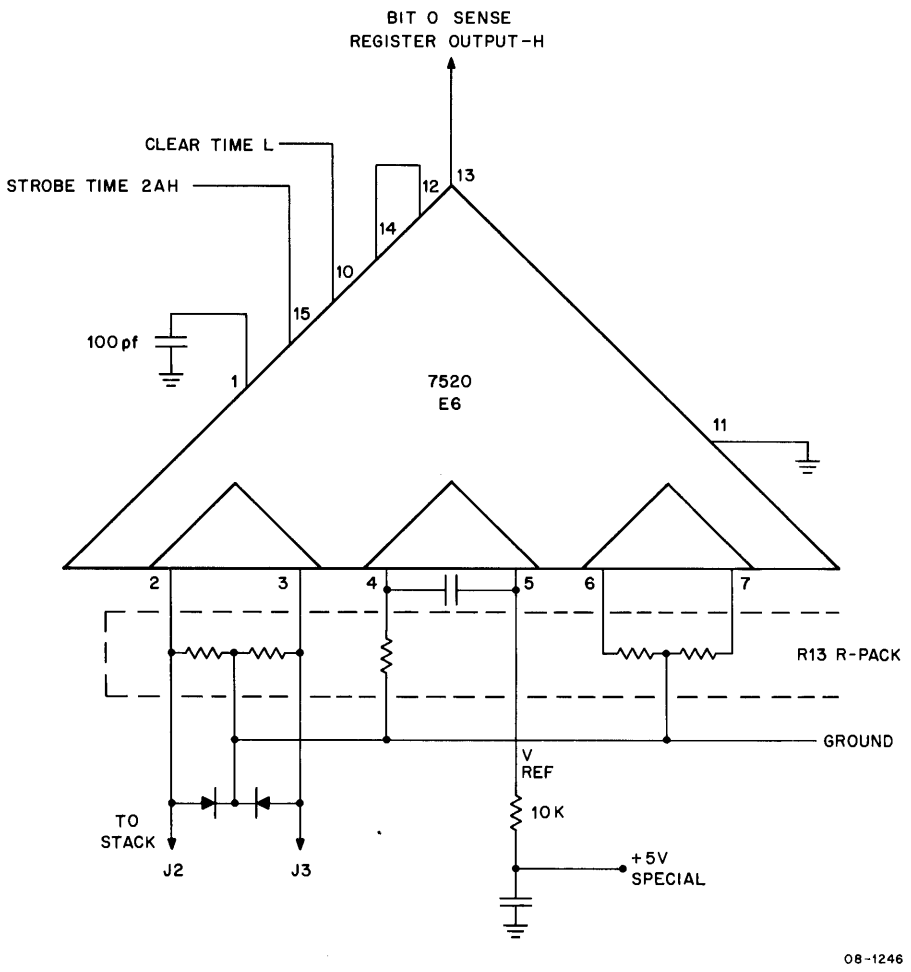


Figure 5-72 Sense Amplifiers

5.19.29 Inhibit Driver Load Gates

During read, the content of the selected core is stored in the sense amplifier latch and passes through gate E7 to the MD bus (Figure 5-73). MD DIR TIME 2H will be high during read time. The same data signal will be on the input to the last inhibit gate, E13; thus, the inhibit driver will turn on when the INHIBIT TIME 2A L pulse is applied to NAND gate E13 during the write portion of the cycle.

5.19.30 Inhibit Drivers

The inhibit driver for bit 0, shown in Figure 5-74, supplies inhibit current to the selected core when a 0 is to be written. A zero will be represented by a low state on pin 2 of E13. For the inhibit time period, pin 3 will be pulsed low and pin 1 will go high. Current will flow into the base of Q13, which will saturate. The collector of Q13 swings from +20 V down to +1.4 V. C83 acts as a low impedance source of current, which flows from C83 through D63, through the lower primary winding, and through Q13 to ground.

The initial primary current drawn from C83 may reach a peak of 600 to 800 mA. As a result of the high peak primary current, which lasts for 60 ns, the rise time of the transformer secondary is significantly improved. The proper value of capacitor in C83 will optimize the rise time of the secondary current without causing overshoot.

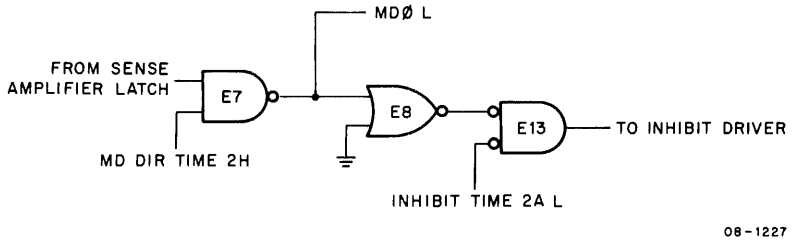


Figure 5-73 Inhibit Drivers Load Gates

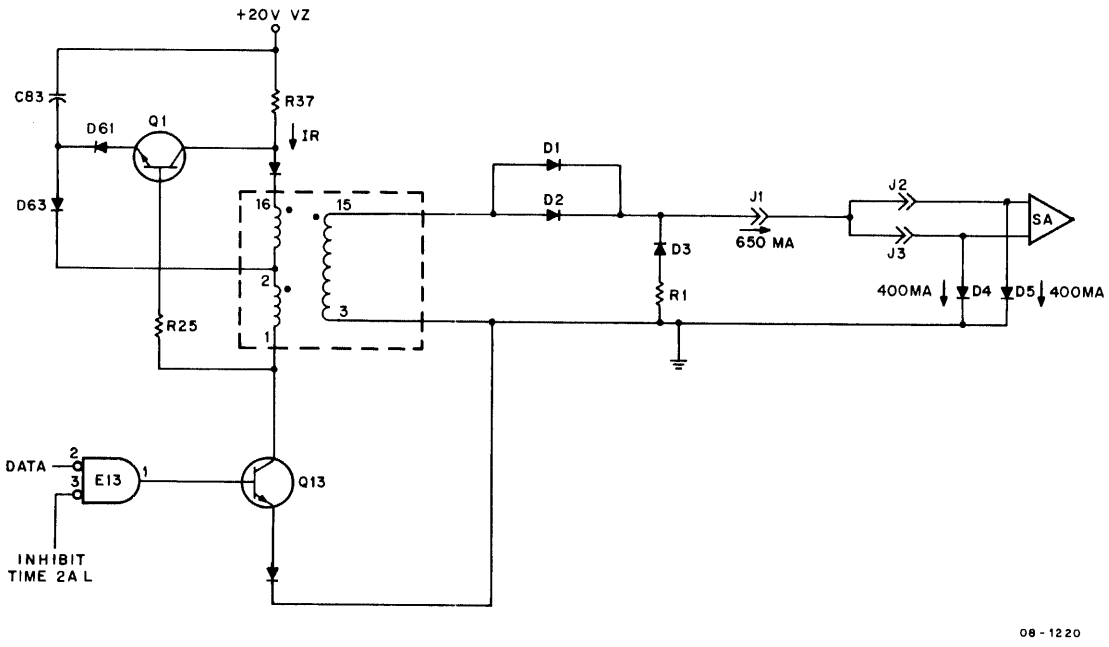


Figure 5-74 Inhibit Drivers Bit 0

Following the current rise time, the primary current amplitude is determined by the limit resistor R37. The current in the secondary will build up with a rise time of approximately 100 ns. Diodes D1 and D2 will be forward biased and a current of ≈650 mA will flow into the stack at pin J1. The sense inhibit winding is split, with 4K cores on each half. The current will divide equally in the stack and will return to the G649 base board and ground via pins J2 and J3.

At the end of the inhibit timing pulse the base of Q13 will go low and Q13 will turn off. During turnoff the collector of Q13 will swing positive causing Q1 to conduct and recharge C83.

5.19.31 Current Source

The X current source is illustrated in Figure 5-75. The current source is a pulsed source which produces a current width dependent on a timing input to E42. The current amplitude is adjusted by the use of jumpers W5-W8 (Table 5-16).

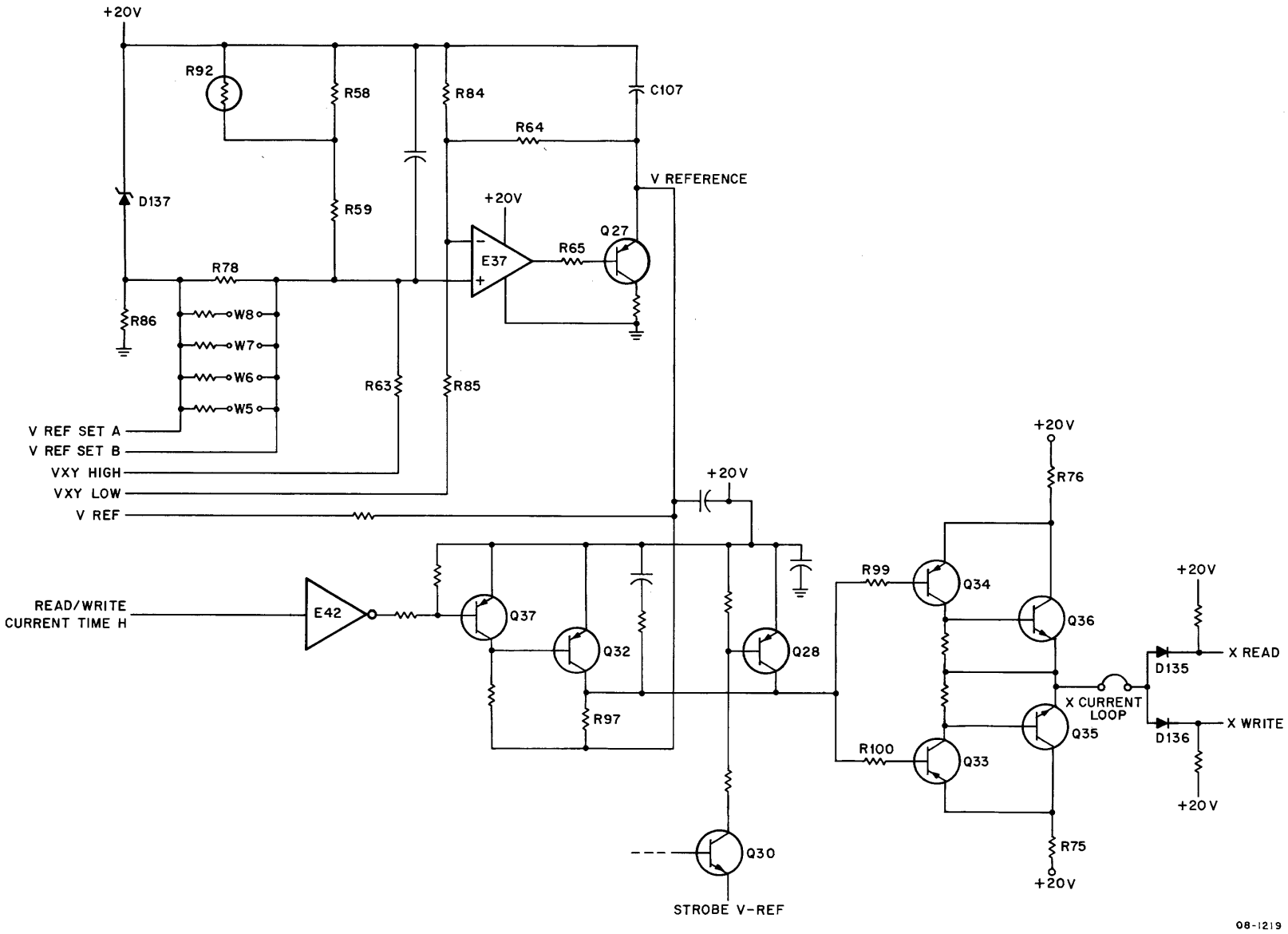


Figure 5-75 Current Source

The jumpers are set at the factory and under no circumstances should they be modified in the field. The setting is made by cutting combinations of jumpers. Sixteen discrete steps in reference voltage may be obtained by the jumper combinations shown in Table 5-16. Each step is equal to 0.08 V. Nominal reference voltage is approximately +13.9 V @ 25° C.

A voltage is created by Zener diode D137 and is further adjusted by the following networks. R78 and the thermistor network make up a divider to establish the value of the reference voltage at the non-inverting input of comparator E37. The reference voltage can be adjusted for a current which gives an optimum margin by clipping one or more of the jumpers W5–W8. The thermistor network, which consists of R92, R58, and R59, will cause the reference voltage to vary as a function of temperature.

This reference voltage is buffered and applied to output transistors Q33 and Q34. Q36, Q37, and Q32 act as on/off switches while the rest of the path of the reference voltage is linear.

When the READ/WRITE CURRENT TIME H signal goes high, Q37 turns on and Q32 turns off; thus, the reference voltage appears at the collector of Q32 and across the load resistors R76 and R75. The base of Q34 will swing from +20 V down to a V(REF) which is approximately 14.0 volts. Q34 will turn on, providing base current to Q36, which conducts and causes current to flow into the stack through diodes D135 and D136. Q33 and Q35 are in parallel with Q34 and Q36 and provide one half of the load current. The X current path has been described and the Y path is identical to the X.

5.19.32 POWER NOT OK

If a power supply is not within limits, POWER NOT OK L will be low at the input to Q31 (Figure 5-76). Q31 and Q29 will be off and Q30 and Q28 will be on, clamping the base of Q34 in Figure 5-75 to approximately +20 V.

Table 5-16
V REF Jumpers

W5	W6	W7	W8		
OUT	OUT	OUT	OUT	1	High Voltage
OUT	OUT	OUT	IN	2	
OUT	OUT	IN	OUT	3	
OUT	OUT	IN	IN	4	
OUT	IN	OUT	OUT	5	
OUT	IN	OUT	IN	6	
OUT	IN	IN	OUT	7	
OUT	IN	IN	IN	8	
IN	OUT	OUT	OUT	9	
IN	OUT	OUT	IN	10	
IN	OUT	IN	OUT	11	
IN	OUT	IN	IN	12	
IN	IN	OUT	OUT	13	
IN	IN	OUT	IN	14	
IN	IN	IN	OUT	15	
IN	IN	IN	IN	16	Low Voltage

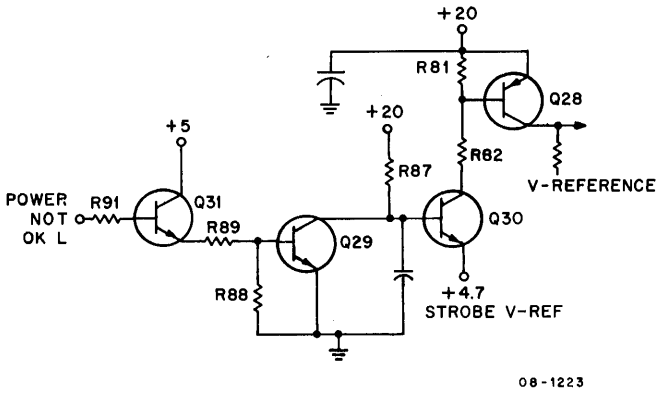


Figure 5-76 POWER NOT OK Circuit

Q34 and Q36 will not conduct until the POWER NOT OK L signal goes high. While POWER NOT OK L clamps the output transistors Q33 and Q34, no X current can flow to the stack. The Y current is also clamped by Q30. The memory will continue to operate for 20 μs after the POWER NOT OK L signal goes low. This allows time for the processor to complete any required storage. When the POWER NOT OK L signal goes high, the processor must wait 50 μs before the memory can be cycled. This allows time for all filter capacitors in the memory to charge.

5.19.33 Test Points

All test points (Table 5-17) for on-line testing are brought out to J147, a 7-pin connector on side (1) of the G649 near the handle. (Pins 1 and 7 are marked in etch on the module). This connector makes it possible to margin the STROBE and X and Y drive currents by attaching a field service margining fixture. The connection of the margining fixture and the pin signals are illustrated in Figure 5-77. Signals on certain test points are shown in Figure 5-78.

NOTE

Do not attempt to margin the G649, Etch C (MM8-AA); the margins achieved will be too wide to be acceptable.

Table 5-17
Voltage Test Points

Name	Pin	Voltage (In Volts)
VXY HIGH	EB1	16.7 ± 1
VXY LOW	EE1 will be lower than VXY HIGH	16.5 ± 1
VREF	ED1	13.8 ± 0.8
VREF SET B	EH1	16.7 ± 1
VREF SET A	EJ1	3.1 ± 0.4
STROBE	EM1	2.4 ± 0.5
TP	EV1 will be	20 ± 1
	when BV2 is	> 2.5
	EV1 will be	4.9 ± 0.3
	when BV2 is	< 0.5
Field Service Connector J147 Pin #		
+5 V	1	5 ± 0.3
	2	2.3 ± 0.3
GND	3, 6	
SPARE	4	
VXY LOW 1	5	16 ± 1
VXY HIGH 1	7	16 ± 1

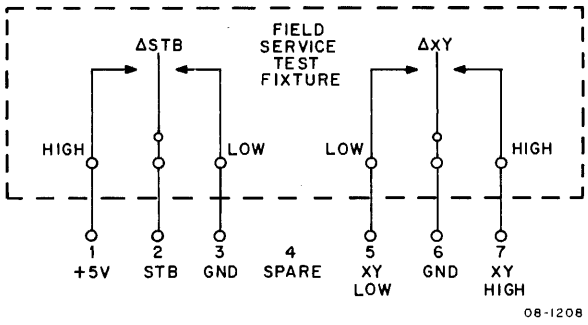


Figure 5-77 Margining Test Fixture Connections

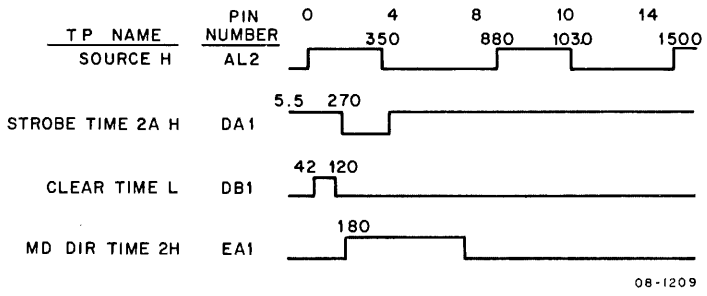


Figure 5-78 Test Point Signals

The memory may be margined in the following manner:

1. With the processor halted, connect the cable from the field service margining fixture to J147, ensuring that the pin numbers of male and female connectors agree.

2. Set the X/Y switch to the nominal (center off) position and the STB switch to the HIGH poisiton.

NOTE

The processor should always be halted before changing either switch; only one parameter should be margined at a time while the other switch is in the nominal (center off) position.

3. Run any appropriate diagnostic, e.g., EXTENDED MEMORY DATA AND CHECKERBOARD.

4. Repeat steps 2 and 3 with the STB switch in the LOW position, making certain that the processor is halted while changing switch positions.

5. Repeat the above steps with the STB switch in the nominal (center off) position while toggling the X/Y switch first to X/Y HIGH and then to X/Y LOW.

Any diagnostic failure that can be attributed solely to this procedure will denote a marginal and therefore defective memory system.

Use of the STB switch will result in a ±10 ns change in a strobe position. Use of the X/Y switch will result in a ±10 mA change in X and Y current amplitude during both read and write.

5.19.34 Circuit Variables

There are a number of variables in the memory system, such as X/Y field address, current amplitude, and strobe position.

The field address is factory set at address 0 and may be changed by field service to fit the customer's application. This is done by solder lugs and jumpers as described in Paragraph 5.19.22.

The X/Y current is factory set and should not be changed in the field.

The strobe position is factory set and should not be changed in the field.

5.19.35 Core Memory Troubleshooting

Some memory data errors and their possible causes are listed in Table 5-18.

Table 5-18
Memory Data Errors Possible Causes

Symptom	Cause	Check
One bit 1 or 0	Inhibit	Collector of 2N3725
One bit 1 or 0	Sense Amp	Pin 13 of Sense Amp
Random/All 0	XY Current Low	VREF @ ED1
Random/All 1	XY Current High	VREF @ ED1
Random/All 1	Inhibit Timing	Collector Q25
Random/All = 1	Inhibit Current/Volt Low	+20 V
Random = 0	Inhibit Current/Volt High	+20 V
Random = 1	5 V Spec S.A. Threshold	CK VOLT @ C122

5.20 MM8-AB 16K CORE MEMORY SYSTEM

The MM8-AB 16K core memory is similar to the MM8-AA 8K core memory described in Paragraph 5.19. The functional differences between the MM8-AA and MM8-AB are as follows:

1. Most component designations illustrated are different because of the difference in the quantity of components and board layout. Refer to the MM8-AB print set in Appendix H for component numbers and locations.

2. On the MM8-AA, field selection is accomplished by EMA0 L and EMA1 L. On the MM8-AB, field selection is accomplished by EMA0. EMA1 L is used in the inhibit timing, the strobe timing, and the Y axis decoding circuitry.

3. There are two inhibit timing circuits and two strobe circuits in the MM8-AB.

4. The Y axis in the the MM8-AB is twice that of the MM8-AA in order to double core storage capacity.

5. In the MM8-AB, the inhibit 2-to-1 transformer has been repackaged in a single in-line transformer; the number of transformers is twice that of the MM8-AA.

6. The number of cores on an X line is increased from 768 to 1536 in order to increase storage from 8K to 16K.

The organization of the MM8-AB memory system is illustrated in Figure 5-79. One hex size board with a piggy-back H219B stack board is used to contain the memory system as follows:

1. G650 baseboard contains 12 Sense Amplifiers, Memory Registers, and Inhibit Drivers with the corresponding control logic, current control, address decoding, selection switches, X-current source. Y-current source, and power fail circuit.

2. H219B Memory Stack contains 12 mats of 16,384 cores per mat. X and Y diode selection matrix, and stack charge circuit.

5.20.1 Assembly Of Twelve Core Mats

The MM8-AB Memory is a 128 X 128 configuration (128 X-rows and 128 Y-rows). This configuration provides 16,384 cores per mat, for which one core can be selected during any one memory cycle and therefore, one bit of information per mat.

The memory stack component layout is illustrated in Figures 5-80, 5-81, and 5-82. Figures 5-81 and 5-82 illustrate the X- and Y-windings within memory stacks.

The MM8-AB is a 12-bit word memory system; thus, 12 mats are used. Each mat stores one unique bit of information for each address, which is detected and sensed by one unique line called the Sense/Inhibit line. Sense/Inhibit lines are used to detect and sense 12 unique bits of information. The arrangement of the X/Y select lines is quite different from inhibit. All 12 mats contain 128 X-lines and 128 Y-lines.

5.20.2 Address Decoding Scheme

The block diagram in Figure 5-83 illustrates the method used to decode the MAR bits and the EMA bits. The process turns on either a write or read source collector and the corresponding sink, thereby completing a current path through the stack. The decoder is arranged as follows: The write selection decoders are on the left side of the illustration and the read selection decoders are on the right side. The X selection decoders decode bits MAR5 L through MAR11 L. The Y selection decoders decode bits EMA1 L, EMA2 L, and MAR0 L through MAR4 L. Both decoding schemes consist of a 16 X 8 matrix. The decoder outputs are applied to the selected switches. The outputs of the selected switches connect to the selection diodes which, in turn, are connected to lines that are threaded through the memory cores. The arrangement of the illustration (Figure 5-83) permits correlation with the engineering drawing schematics (G650).

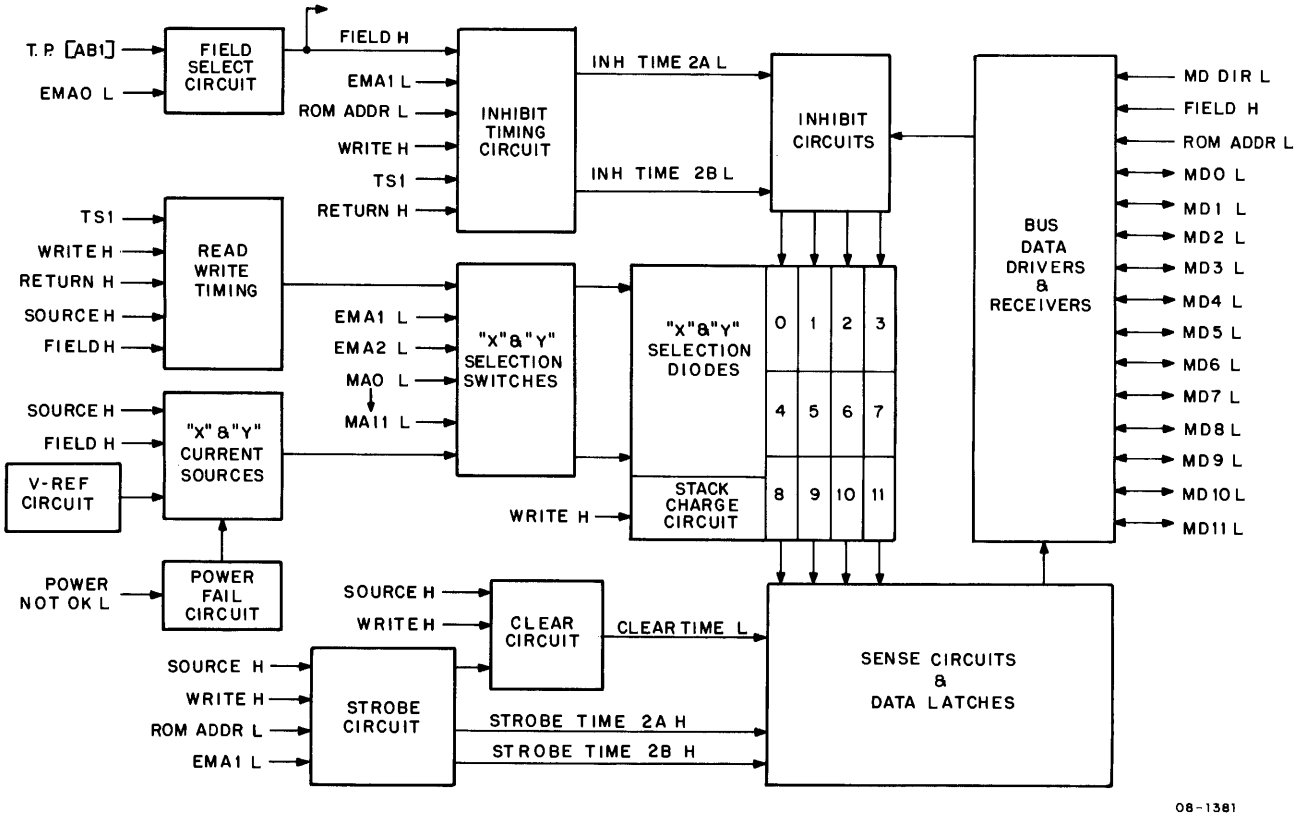


Figure 5-79 MM8-AB 16K Core Memory

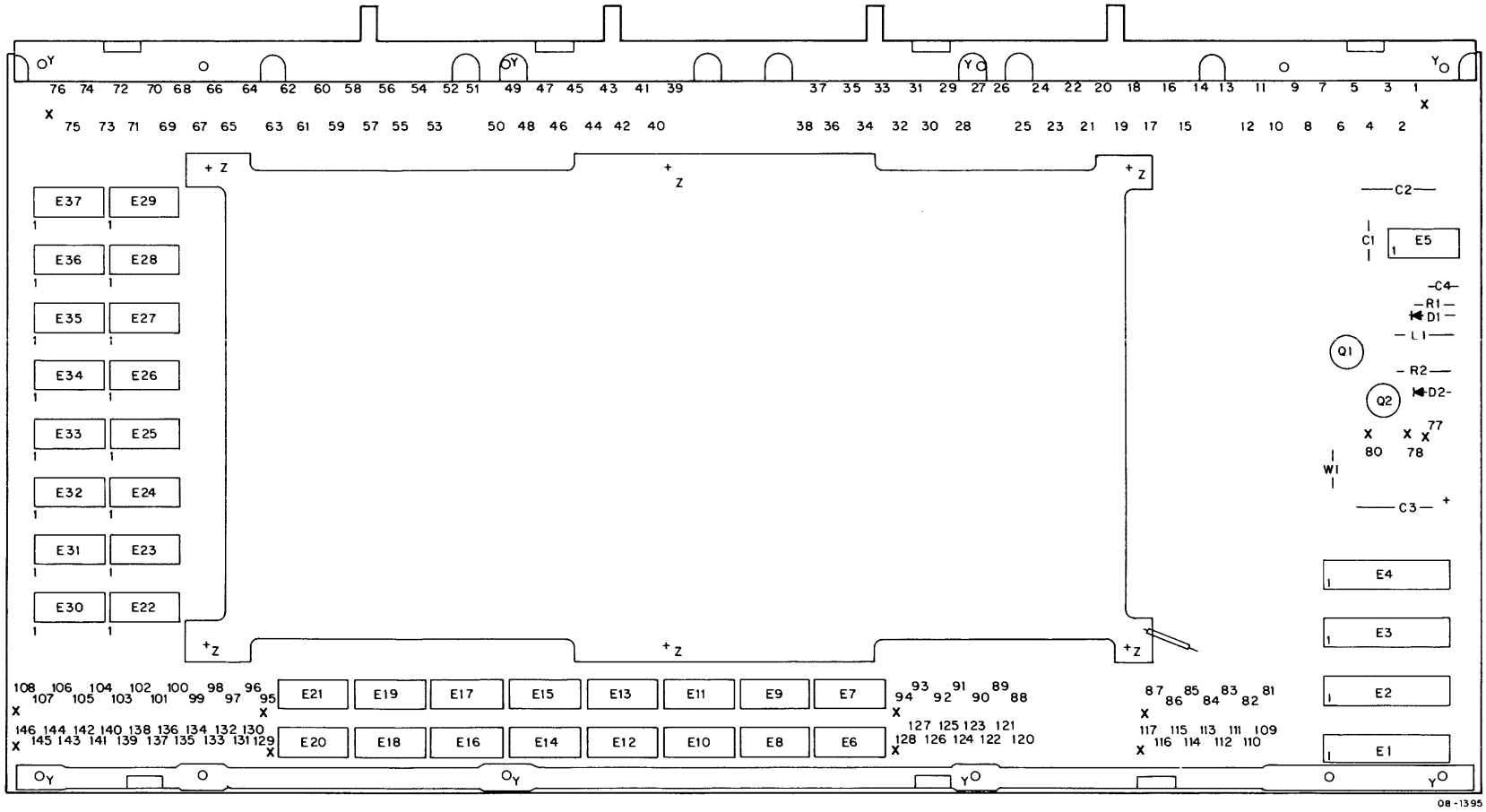


Figure 5-80 MM8-AB 16K Core Memory
Stack Layout

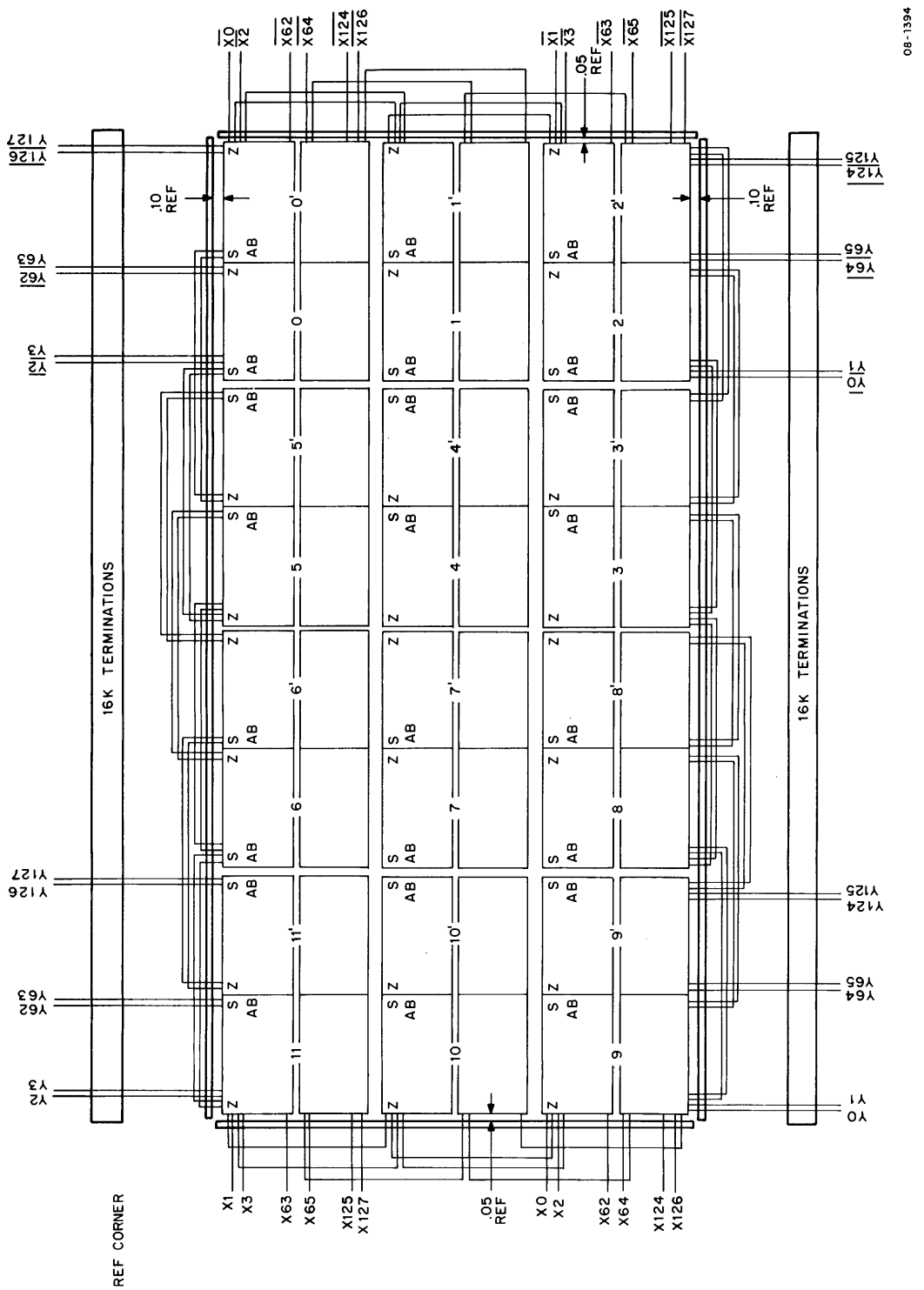


Figure 5-81 16K x 12 Stack and Sense Lines

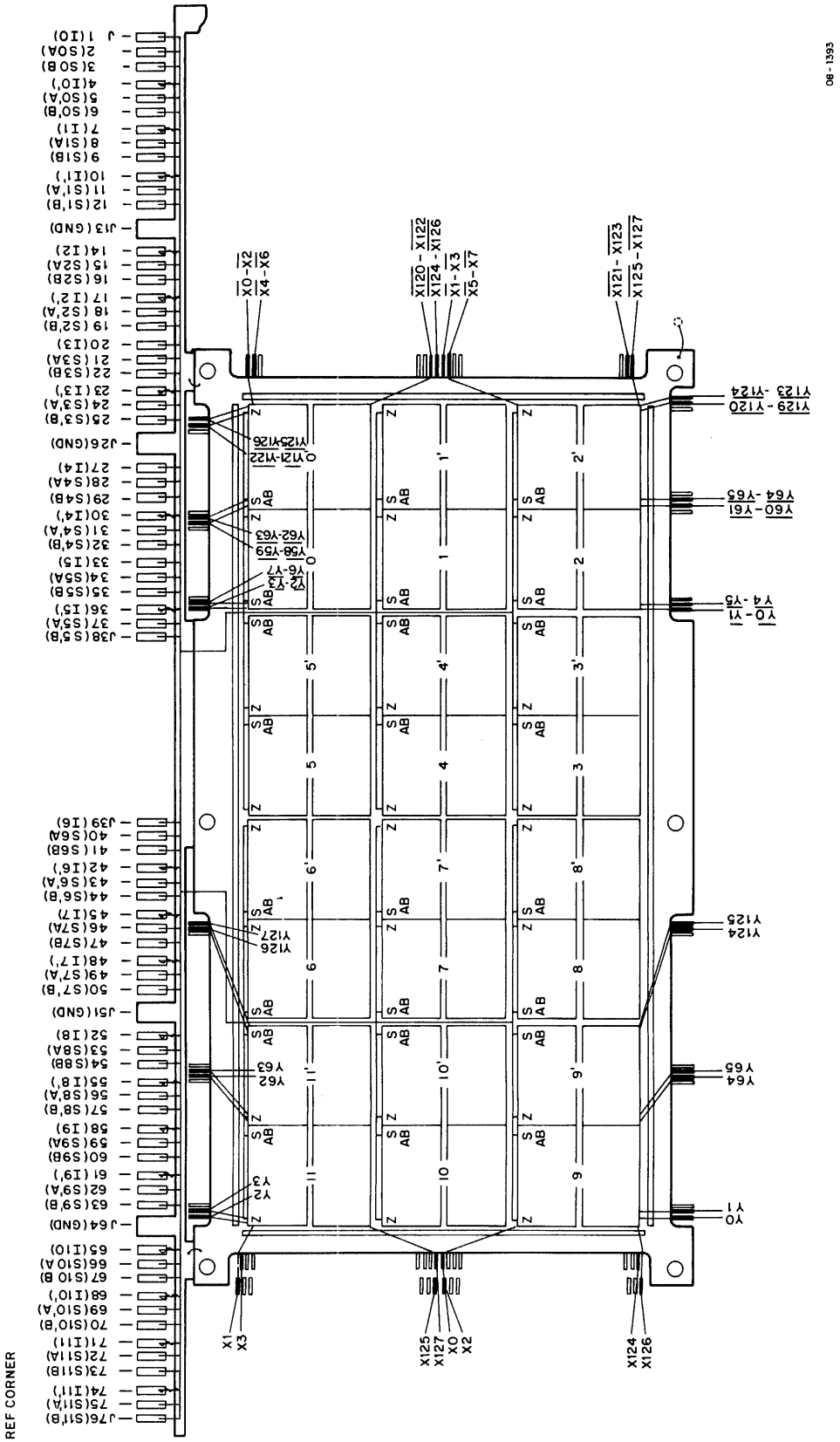


Figure 5-82 16K Core Memory Module Wiring Assembly

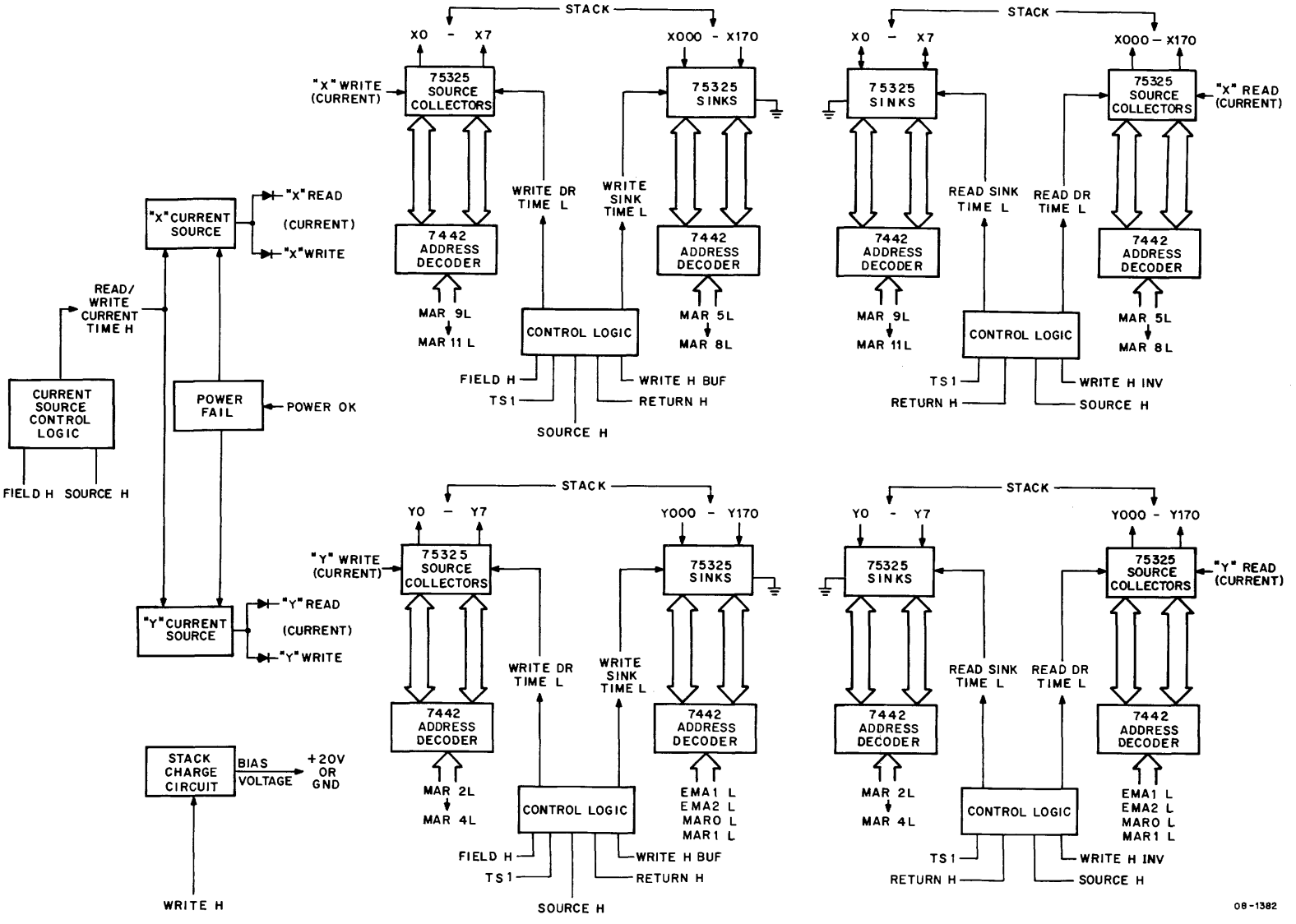


Figure 5-83 Decoding of X and Y Driver Current Sources Block Diagram

The decoding scheme of the MA bits is illustrated in Figure 5-84. The illustration shows the five parts of the memory address, plus what is decoded, and where in the field of the drawing the decoders are located. Table 5-19 lists the necessary input control signals, the content of the memory address, the input pins, the output pins, and the selected Y-line (the core selection decoding logic for the MM8-AB X-axis is identical to that of the MM8-AA core memory). With this information, the user can easily trace through all of the components on any signal/current path to find the selected components.

5.20.3 Operation Of The Core Selection Switches

The cores that contain a selected X-line and selected Y-line define the location in which a 1 or 0 will be either written in or read out. Figure 5-85 illustrates a small portion of the memory core selection logic, which is similar to the MM8-AA core selection logic. The difference is that on the MM8-AB, the X line is threaded through 1536 cores instead of 768. The Y decoding is similar and may be obtained from sheet 6 of the MM8-AB print set in Appendix H. Using Table 5-19, the selection of any given core can be traced from the Memory Address Register through the decoders and switches to the selected line and core.

To select the Y read stack line No. 25 (octal) the procedure using Table 5-19 is as follows: A source collector switch to select one end of the stack line and a sink switch to select the other end of the stack line must be turned on together. This completes the current path from the current source, through the source collector switch, through the selected stack line, through the sink switch to ground.

Addresses EMA1 L, EMA2 L, MAR0 L, and MAR1 L are decoded to select any 1 of 16 source collectors. In our example we are selecting the address combination that gives us binary 0010 (octal 02).

Addresses MAR2 L, MAR3 L, and MAR4 L are decoded to select any 1 of 8 sink switches. In our example we are selecting the address combination that gives us binary 101 (octal 5). Table 5-20 shows selected stack lines for all combinations of selected source collectors and selected sinks.

5.20.4 Read/Write Operation

The read operation involves the sense amplifier and the necessary control logic in conjunction with the selection system. During the read portion of the memory cycle, the selected core develops a signal on the Sense/Inhibit line only if a 1 was previously stored in core. The sense registers in the sense amplifier are previously cleared and STROBE TIME 2AH or 2BH gates either a 1 or 0 into the sense register. When a 1 is sensed, the sense amplifier applies a low signal to the MD0 line (Figure 5-85).

The output of the core stack, which is stored in the sense register, is rewritten into the same core location during the write half of the timing cycle. The MD DIR TIME 2 H pulse gates the sense register data to the inhibit drivers and places the data on the MD bus where it is available to the CPU or a peripheral device.

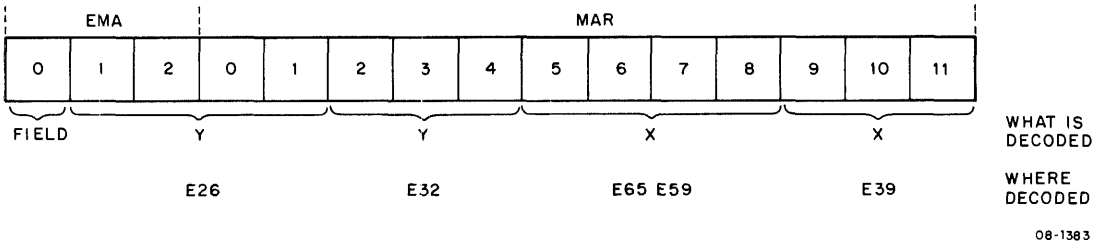


Figure 5-84 Decoding Relationships

Table 5-19
Core Selection Decoding Scheme
"Y" READ

Function	Control Logic	EMA 1 L EMA2 L MAR0 L MAR1 L	MAR2 L ↓ MAR4 L	Source Output Pins	Sink Input Pins	Selected Source (Octal)	Selected Sink (Octal)
Turn on Source Collectors	TS1 + RET H = H	0000	—	J85	—	000	—
		0001	—	J113	—	010	—
	WRITE H INV = H	0010	—	J86	—	020*	—
	READ DR TIME L = L	0011	—	J114	—	030	—
		0100	—	J87	—	040	—
		0101	—	J116	—	050	—
		0110	—	J115	—	060	—
		0111	—	J117	—	070	—
		1000	—	J81	—	100	—
		1001	—	J109	—	110	—
		1010	—	J82	—	120	—
		1011	—	J110	—	130	—
		1100	—	J83	—	140	—
		1101	—	J111	—	150	—
		1110	—	J84	—	160	—
		1111	—	J112	—	170	—
Turn on Sinks		—	000	—	J128	—	0
	TS1 + SOURCE H = H	—	001	—	J126	—	1
	WRITE H INV = H	—	010	—	J90	—	2
	READ SINK TIME L = L	—	011	—	J91	—	3
		—	100	—	J127	—	4
		—	101	—	J125	—	5*
		—	110	—	J122	—	6
		—	111	—	J92	—	7

*EXAMPLE: Source Collector = 020
Sink = + 5
(Total) Selected Line = 025 Octal

Table 5-19 (Cont)
Core Selection Decoding Scheme
"Y" WRITE

Function	Control Logic	MAR2 L ↓ MAR4 L	EMA 1 L EMA 2 L MAR0 L MAR1 L	Source Output Pins	Sink Input Pins	Selected Source (Octal)	Selected Sink (Octal)
Turn on Source Collectors	FIELD H = H	000	———	J93	———	0	——
	TS1 + RET H = H	001	———	J94	———	1	——
		010	———	J120	———	2	——
	WRITE H BUF = H	011	———	J89	———	3	——
	WRITE DR TIME L = L	100	———	J124	———	4*	——
		101	———	J123	———	5	——
		110	———	J88	———	6	——
		111	———	J121	———	7	——
Turn on Sinks	FIELD H = H	——	0000	———	J85	——	000
	TS1 + RET H = H	——	0001	———	J113	——	010
		——	0010	———	J86	——	020
	WRITE H BUF = H	——	0011	———	J114	——	030
	WRITE SINK TIME L = L	——	0100	———	J87	——	040
		——	0101	———	J116	——	050
		——	0110	———	J115	——	060
		——	0111	———	J117	——	070*
		——	1000	———	J81	——	100
		——	1001	———	J109	——	110
		——	1010	———	J82	——	120
		——	1011	———	J110	——	130
		——	1100	———	J83	——	140
		——	1101	———	J111	——	150
		——	1110	———	J84	——	160
		——	1111	———	J112	——	170

*EXAMPLE: Source Collector = 4
Sink = +070
(Total) Selected Line = 074 Octal

Table 5-20
Core Selection, Y Read

Selected Source Collector	Selected Sink							
	0	1	2	3	4	5	6	7
000	0	1	2	3	4	5	6	7
010	10	11	12	13	14	15	16	17
020	20	21	22	23	24	25	26	27
030	30	31	32	33	34	35	36	37
040	40	41	42	43	44	45	46	47
050	50	51	52	53	54	55	56	57
060	60	61	62	63	64	65	66	67
070	70	71	72	73	74	75	76	77
100	100	101	102	103	104	105	106	107
110	110	111	112	113	114	115	116	117
120	120	121	122	123	124	125	126	127
130	130	131	132	133	134	135	136	137
140	140	141	142	143	144	145	146	147
150	150	151	152	153	154	155	156	157
160	160	161	162	163	164	165	166	167
170	170	171	172	173	174	175	176	177

All numbers are in octal.

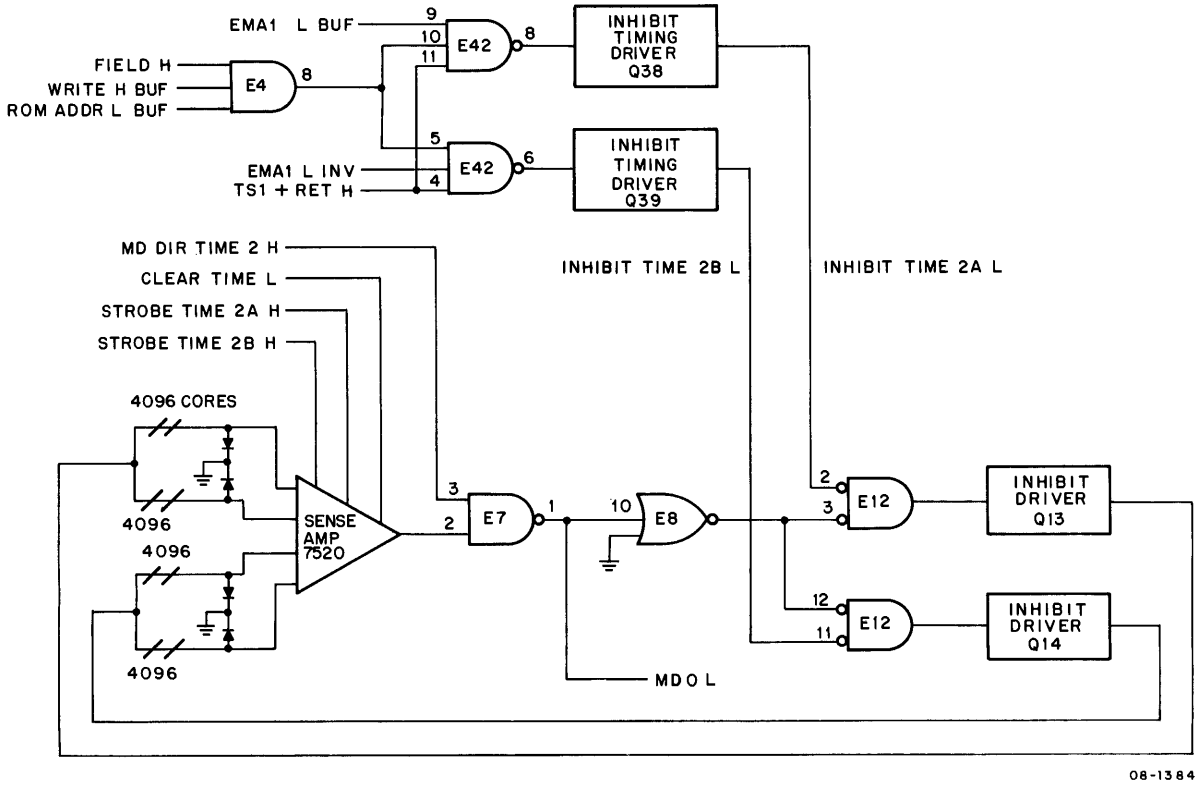


Figure 5-85 Inhibit Operation For Bit 0

The write operation involves the inhibit drivers, load gates such as E7 and E8, the sense register, and the necessary control logic in conjunction with the selection system. The inhibit driver load gates receive ones and zeros via the MD lines from either the MB register in the processor or the sense register. Control gating signals for the inhibit driver load gate are as follows:

1. TS1 + RET H
2. FIELD H
3. ROM ADDR L BUF
4. EMA1 L BUF
5. EMA1 L INV
6. WRITE H BUF

5.20.5 Field Select Control Logic

The function and operation of the MM8-AB field select control loic (Figure 5-86) is the same as the MM8-AA, except the inputs are different. The MM8-AB memory uses only one bit, EMA0 L, as an input.

The MM8-AB is configured in 16K boundaries and can be expanded to 32K. Table 5-21 relates EMA0 L to the assigned memory address blocks and to the installed jumpers.

Table 5-21
Address Block Selection

EMA0 L	Memory Address Block	Installed Jumpers
HI	0–16K	1-2 and 1-3
LO	16K–32K	1-2 and 2-4

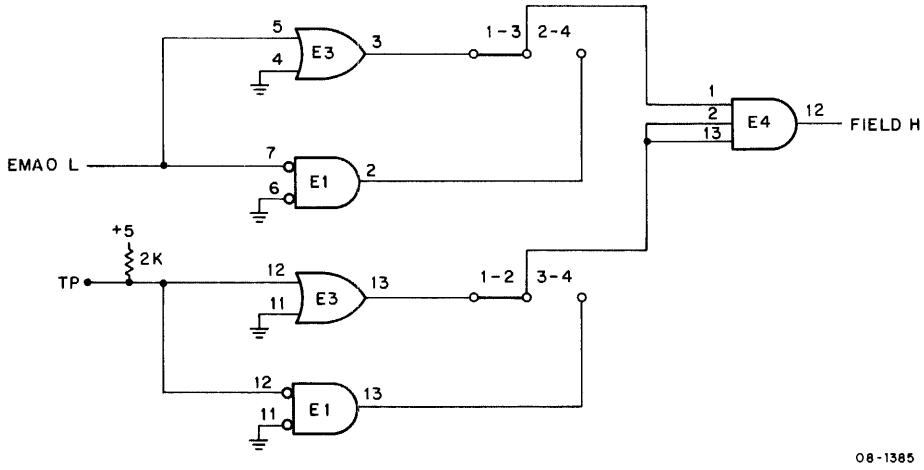


Figure 5-86 Field Selection Logic

5.20.6 Inhibit Control Logic

The top part of Figure 5-85 shows the inhibit control logic. The signals used to create the inhibit timing signals are listed in Paragraph 5.20.4. All signals contribute to gating the inhibit operation while TS1 + RET H determines the width of the inhibit current pulse.

5.20.7 Sense Register Enable Logic

The Sense Register Enable logic is shown in the bottom half of Figure 5-85. When MD DIR TIME 2 H is asserted, the content of the sense register is gated onto the MD line and to the inhibit driver.

5.20.8 Sense Register Clear Timing

The logic that generates the CLEAR TIME L signal is shown in Figure 5-87. SOURCE H generates the CLEAR TIME L signal at E42; the trailing edge of the signal is determined by the output of the STROBE one-shot multivibrator (E51). The timing relationship is illustrated in Figure 5-88.

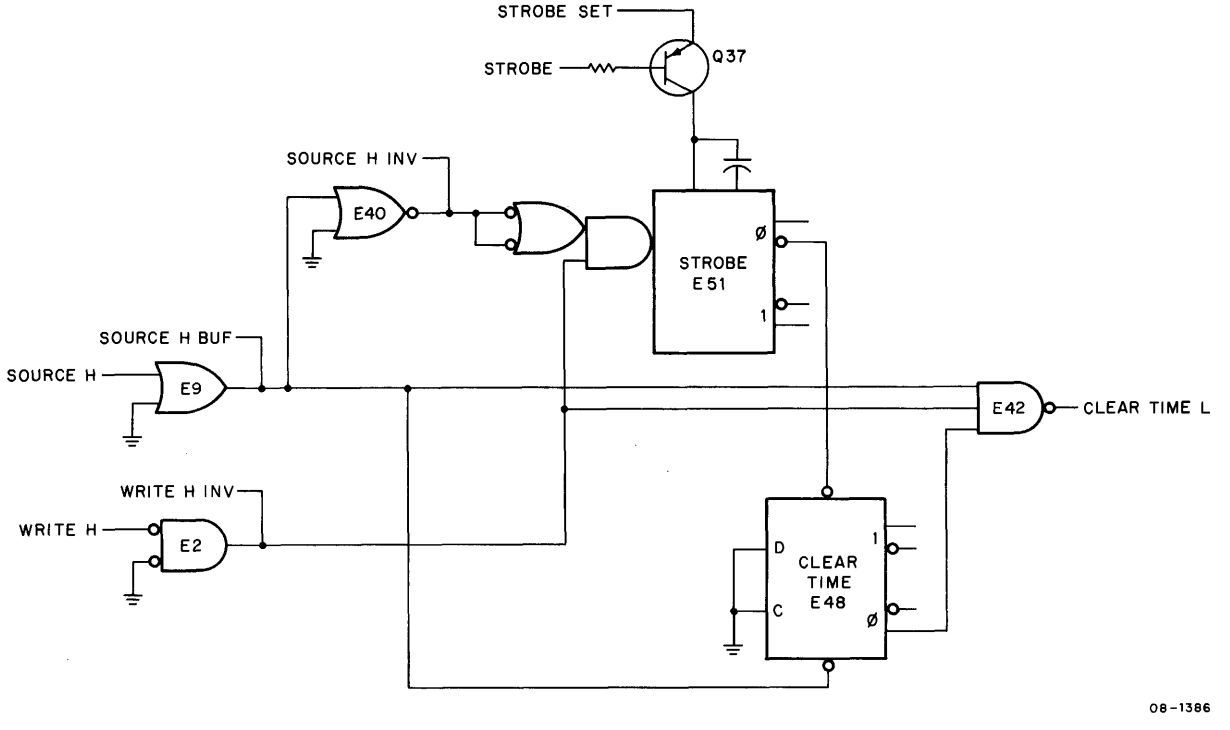


Figure 5-87 Clear Time Control Logic

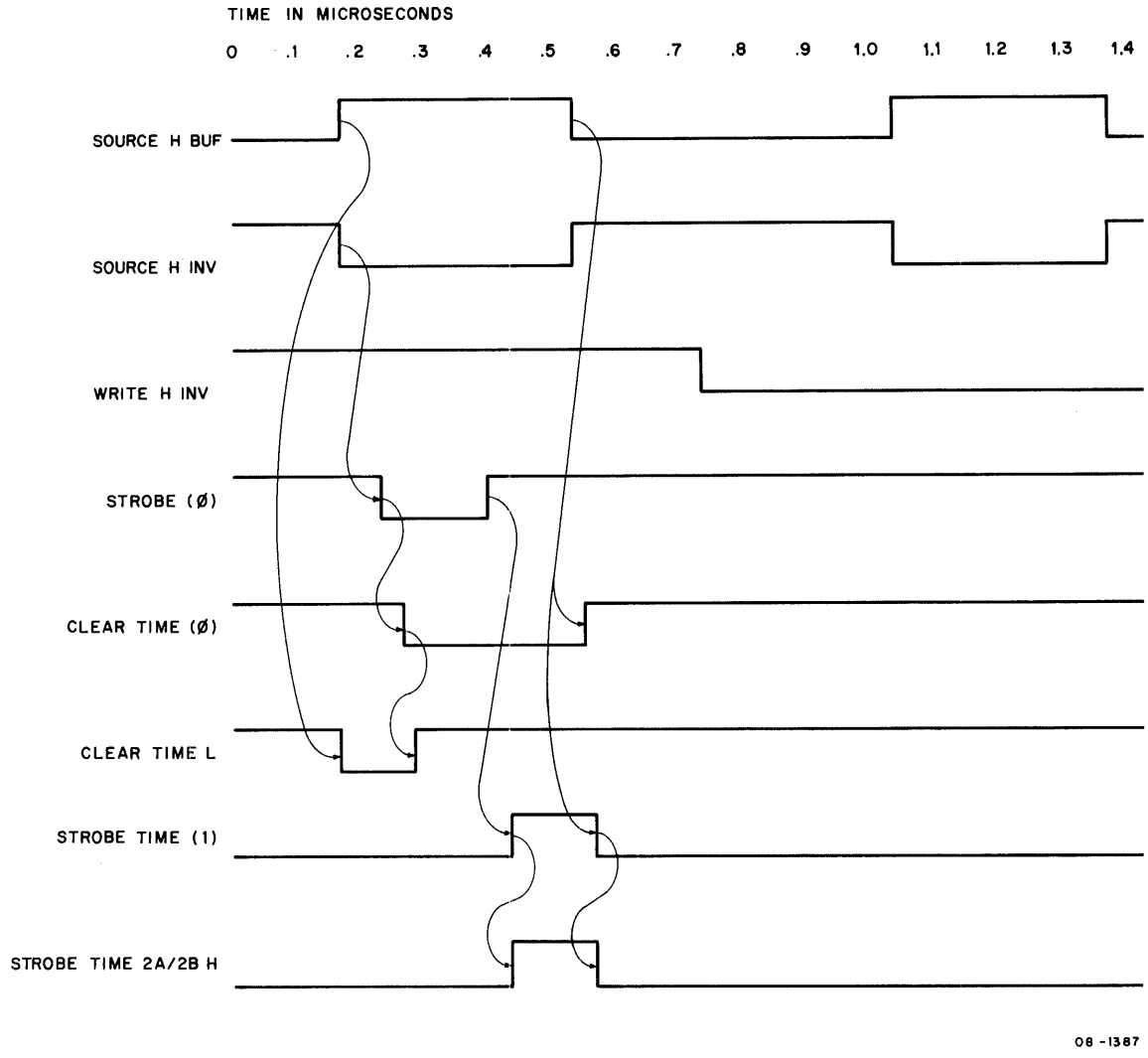


Figure 5-88 Strobe and Clear Timing

5.20.9 Strobe Control Logic

The Strobe Control logic is shown in Figure 5-89. The timing signals that generate the strobes are shown in Figure 5-88. SOURCE H INV triggers the STROBE one-shot, E51, and the trailing edge of the one-shot clocks the STROBE TIME flip-flop, E48. The output of E48 determines the leading edge of the STROBE TIME 2A/2B H signals; the trailing edge is set by SOURCE H going low. The width of the STROBE one-shot output is proportional to the amplitude of the constant current supplied by Q37. The current in Q37 and, hence, the position of the strobe signals can be adjusted by jumpers in the emitter circuit of Q37. The jumpers, W9 through W12 (shown in the G650 logic drawings in Appendix H), are counterparts of jumpers W9 through W12 in the MM8-AA memory (Figure 5-71); hence, Table 5-15, which relates jumper placement to the STROBE one-shot output, applies to both memories.

5.20.10 Strobe Setting Jumpers

The operation of the strobe circuit, adjustment, and jumper installation is the same as that for the MM8-AA which is described in Paragraph 5.19.26.

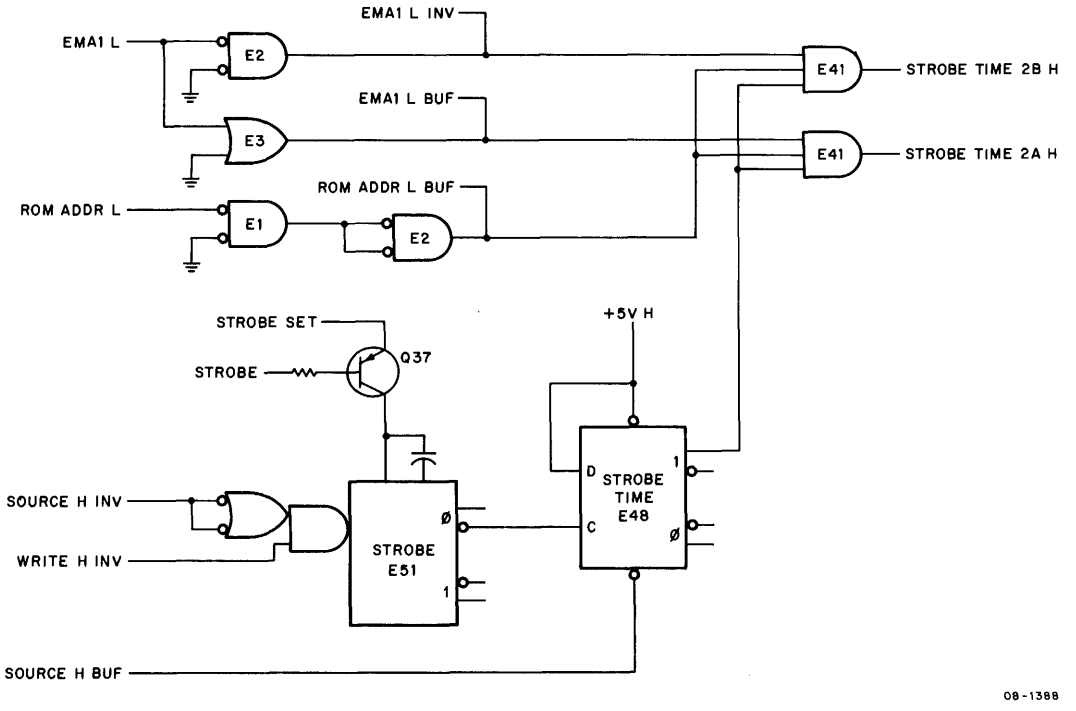


Figure 5-89 Strobe Control Logic

5.20.11 Inhibit Driver Load Gates

During a read operation, the content of the selected core is stored in the sense amplifier latch. The stored output is fed to pin 2 of E7 and is gated onto the Omnibus by MD DIR TIME 2 H (Figure 5-90).

The read data is also present at pins 3 and 12 of E12. The inhibit winding for the MM8-AB is divided into two 8K windings. One of the two inhibit windings is selected at E12 by timing signals INH TIME 2A L or INH TIME 2B L. These timing signals are generated from the memory address.

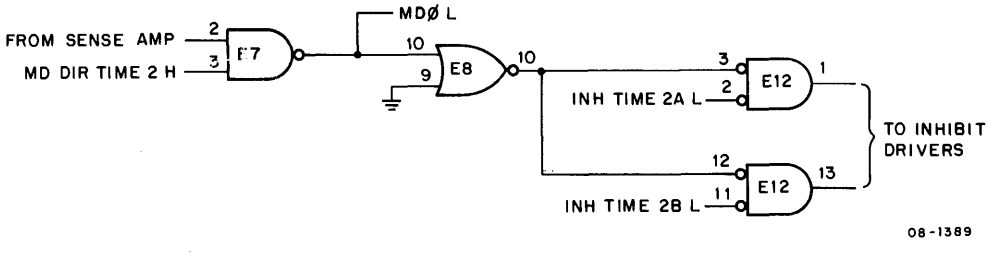


Figure 5-90 Inhibit Driver Load Gates

5.20.12 Sense Amplifier

The sense amplifier logic of the MM8-AB is identical to that of the MM8-AA, described in Paragraph 5.19.27, but the application is different in the MM8-AB. Input pins 6 and 7 (Figure 5-72) are connected to an 8K sense line and a second strobe line (STROBE TIME 2B H) on pin 11 is added to control the additional 8K sense winding.

One dual sense amplifier is fed by the 8K sense lines and the two strobe signals, STROBE TIME 2A/2B H, determine which of the two sense lines is selected. A resulting logical one signal is gated into the single latch circuit on the amplifier output.

5.20.13 Inhibit Drivers

The inhibit drivers shown in Figure 5-91 are an expansion of the MM8-AA drivers shown in Figure 5-74. Each bit requires two inhibit drivers to supply inhibit current to each of its two 8K windings. Since only one of the two drivers is on at a given time Q1, C1, D5, and R31 are shared. A zero is represented by a low on pins 3 and 12 of E12. For the inhibit time period, either INHIBIT TIME 2A L or INHIBIT TIME 2B L is low, turning on either Q13 or Q14. If Q13 is selected and saturated, its collector swings from +20 V down to 1.4 V. C1 acts as a low impedance source of current which flows through D2, the primary winding, and Q13 back to ground. The initial surge of current in the primary winding significantly improves the rise time of the stack current. The circuit recovery operation is similar to the MM8-AA recovery operation described in Paragraph 5.19.30. C1 is recovered through Q1 during the fall time of the primary current.

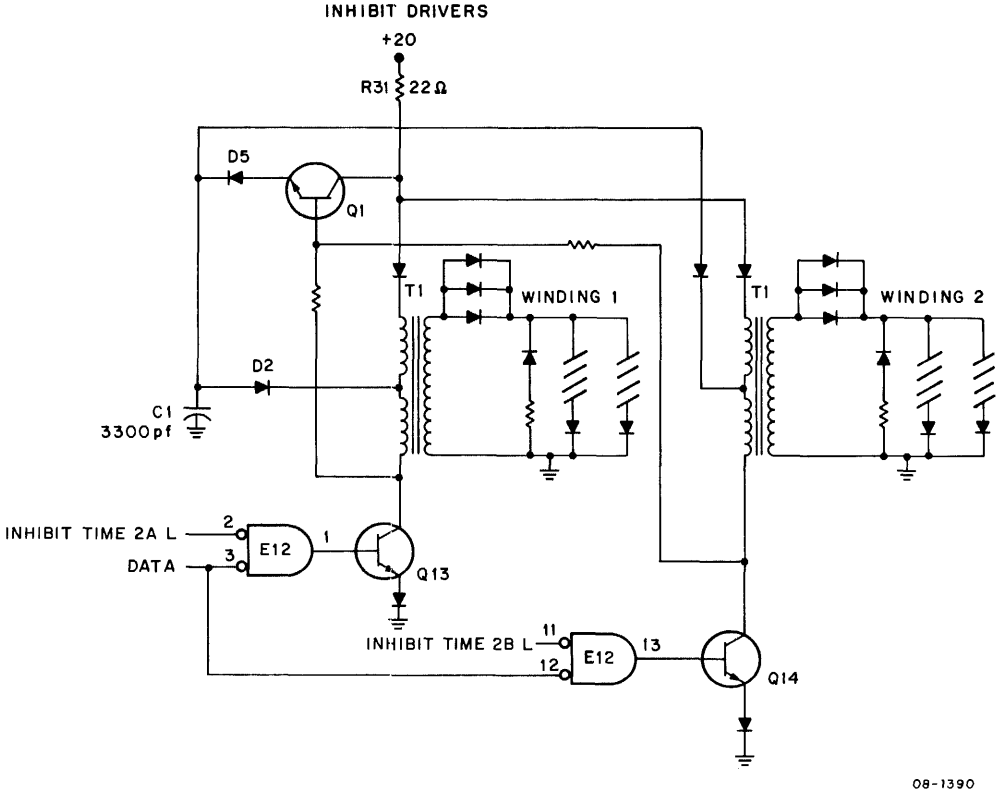


Figure 5-91 Inhibit Drivers for Bit 0

5.20.14 Current Source

With the exception of component designations, the MM8-AB current source is identical to the MM8-AA current source described in Paragraph 5.19.31. The same circuit with MM8-AB component designations is shown in Figure 5-92. Table 5-16 also applies to the MM8-AB system.

A voltage is created by Zener diode D100 and is further adjusted by the following networks. R125 and the thermistor network make up a divider to establish the value of the reference voltage at the non-inverting input of comparator E44. The reference voltage can be adjusted for a current that gives optimum margins by clipping one or more of the jumpers W5–W8. The thermistor network, which consists of R137, R119, and R120, causes the reference voltage to vary as a function of temperature.

This reference voltage is buffered and applied to output transistors Q52 and Q53. Q48, Q57, and Q56 act as on/off switches while the remainder of the path of the reference voltage is linear.

When the READ/WRITE CURRENT TIME H signal goes high, Q57 turns on and Q56 turns off; thus, the reference voltage appears at the collector of Q56 and across the load resistors R93 and R94. The base of Q52 will swing from +20 V down to a V(REF) which is approximately 14.0 volts. Q52 will turn on, providing base current to Q48, which conducts and causes current to flow into the stack through diodes D97 and D98. Q53 and Q49 are in parallel with Q52 and Q49 (Figure 5-92) and provide one half of the load current. The X current path has been described and the Y path is identical to the X.

5.20.15 POWER OK

The POWER OK circuit is shown in Figure 5-93. If a power supply is not within limits POWER OK will be low at the input to Q40. Q40 and Q41 will be off, and Q42 and Q44 will be on, clamping the base of Q52 (Figure 5-92) to approximately +20 V.

Q52 and Q48 will not conduct until the POWER OK signal goes to its high logic state. While POWER OK clamps the output transistors Q52 and Q53, no X current can flow to the stack. The Y current is also clamped by Q42. The memory will continue to operate for 20 μs after the POWER OK signal goes low. This allows time for the processor to complete any required storage. When the POWER OK signal goes high the processor must wait 50 μs before the memory can be cycled. This allows time for all filter caps in the memory to charge.

5.20.16 Test Points

The MM8-AB Test Points are the same as for the MM8-AA described in Paragraph 5.19.33.

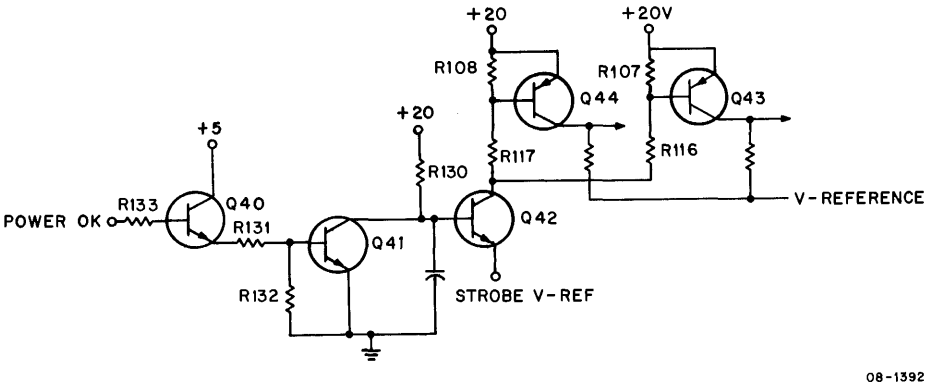


Figure 5-93 POWER NOT OK Circuit

CHAPTER 6
PDP-8/A OPTION MODULES

The DKC8-AA I/O Option module (M8316) and the KM8-A Extended Option module (M8317) are multi-option modules designed specifically for the PDP-8/A computer. The DKC8-AA I/O Option contains a general purpose 12-bit word Parallel I/O, a Serial Line Unit, Real Time Clock, and the Programmer's Console interface. The KM8-A Extended Option contains the Memory Extension control, Timeshare, Power Fail/Auto-Restart, and the Bootstrap Loader. Other PDP-8 family computers provide these options or similar options on separate quad modules, but the PDP-8/A is designed to accept hex sized modules allowing more than one option per module.

This chapter is divided into two sections, Section 1 describes the DKC8-AA I/O Option module and Section 2 the KM8-A Extended Option module. Each section contains a block diagram description of the entire option, followed by a block diagram description and detailed logic description of each component on the option. The installation and acceptance test procedures for these modules are contained in Chapter 2. The detailed logic description of the Programmer's Console interface on the DKC8-AA option is in Chapter 4.

SECTION 1
DKC8-AA I/O OPTION MODULE (M8316)

The DKC8-AA I/O Option Module (M8316) contains four PDP-8/A options on one hex size module (the module is illustrated in Figure 2-15).

1. A Serial Line Unit (SLU) for interfacing to 20 mA or EIA serial devices.
2. A General Purpose 12-bit parallel I/O.
3. A Real Time crystal clock.
4. Programmer's Console interface which provides the interface between the Programmer's Console and the Omnibus.

6.1 DKC8-AA I/O OPTION MODULE BLOCK DIAGRAM DESCRIPTION

Figure 6-1 is a block diagram of the DKC8-AA I/O Option Module. The options on this module are described in the following paragraphs.

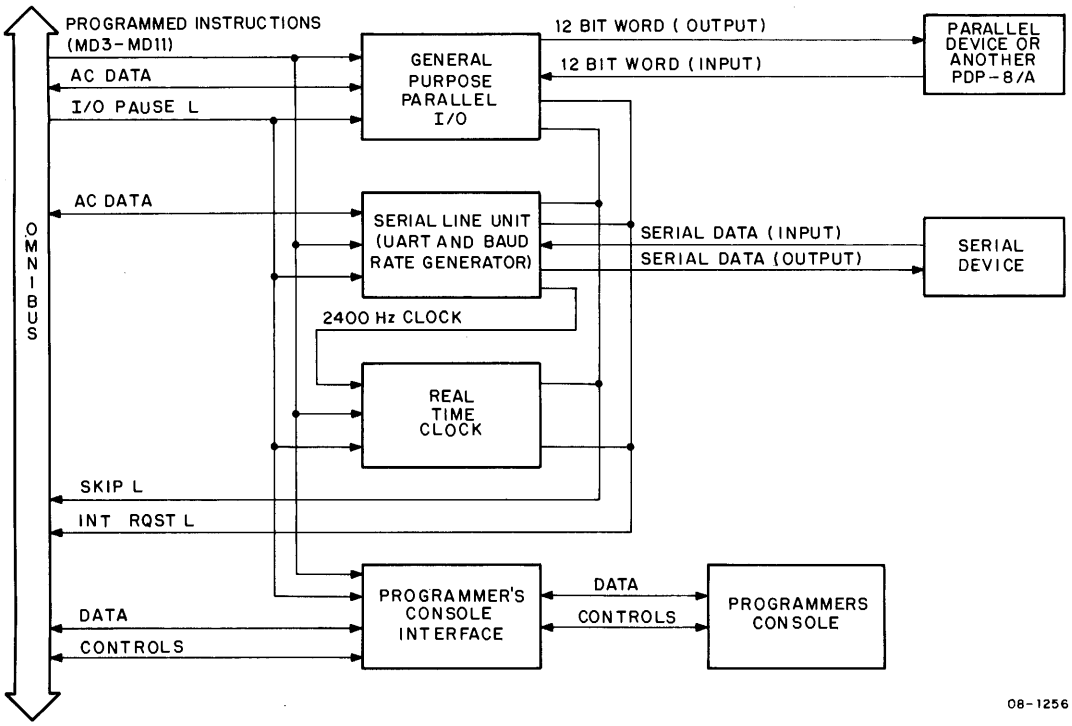


Figure 6-1 DKC8-AA I/O Option Module Block Diagram

6.1.1 Serial Line Unit (SLU)

The Serial Line Unit (SLU) consists of a universal asynchronous receiver transmitter (UART) driven by a packaged oscillator. The SLU provides an interface for use between the PDP-8/A Omnibus and any asychronous external device which has electrically compatible data leads and which operates with one of the serial data formats available with this interface.

Operation of the SLU is via programmed I/O. The skip and interrupt request lines of the computer are used. Data transfers are between the PDP-8/A Accumulator and registers in the UART.

6.1.2 General Purpose 12-Bit Parallel I/O

The General Purpose Parallel I/O on the DKC8-AA module allows the PDP-8/A to transmit or receive one 12 bit word at a time between user designed logic on single ended data lines, or two PDP-8/A processors to transfer data to each other, provided each processor has a DKC8-AA I/O option board and the proper cables.

All data transfers are between the AC and an external device via programmed I/O. Data transfer rate is software limited to 50K words/second.

6.1.3 Real Time Crystal Clock

The Real Time Crystal Clock on the DKC8-AA module interrupts the processor every 10 ms (100 HZ ± 0.01%) if interrupt enable is set. A skip instruction (CLSK) causes the program to skip an instruction if the clock flag is set.

A switch on the M8316 module allows the clock to be disabled.

6.1.4 Front Panel Control

The front panel control logic on the DKC8-AA module provides the interface between the Programmer's Console and the Omnibus. The front panel is connected to the DKC8-AA by two BC08S cables. Standard lengths are 1 foot (30.5 cm) and 12 feet (366 cm), but cables up to 15 feet (457 cm) are allowed when the panel is operated remotely.

The DKC8-AA contains the necessary control logic multiplexers, drivers, and receivers to load the extended memory and memory address registers and provide manual control of computer operation. The controls on the Programmer's Console are explained in Chapter 1. The detailed logic on the Programmer's Console and the logic on the DKC8-AA associated with the Programmer's Console are discussed in Paragraph 4.3.

6.2 SERIAL LINE UNIT

The SLU block diagram is shown in Figure 6-2. The SLU has two distinct functions: Receives parallel data (characters) from the AC and shifts them out to a serial device as serial data; and receive serial data from a serial device, changes it to parallel data and transfers it to the AC.

6.2.1 SLU Specifications

The SLU specifications are as follows:

Drive Capability:	20 mA serial	(Drivers/receivers will function properly at 110 baud with up to 5000 feet of 18 gauge or larger twisted pair cable.)
	EIA Serial	(Drivers/receivers will function properly with up to 50 feet of cable.)

SLU Specifications (Cont)

Baud Rates:

The following baud rates are switch selectable on the M8316 module:

50	1800
75	2000
110	2400
134.5	3600
150	4800
300	7200
600	9600
1200	

Transmit and receive baud rates must be the same.

Stop Bits:

One or two (switch selectable).

Parity:

Parity is enabled by installing a jumper. Even or odd parity is selectable using a second jumper.

Device Codes:

03 receive and 04 transmit. No other device codes are provided for.

Number of Bits per Character:

The number of bits per character is jumper selectable between 5 and 8. Jumpers NB1 and NB2 are used to select the number of bits per character as follows:

Number of Bits	NB1	NB2
5	IN	IN
6	OUT	IN
7	IN	OUT
8	OUT	OUT

The normal configuration is 8 bits per character.

Cables:

A BC05M-0-0 in lengths of 15, 25, or 50 feet connects to J3 on the M8316 module.

The end of the cable that connects to J3 on the M8316 module is a 6504-15 male Berg connector and the other end is a Mate-N-Lok female connector.

Modems:

The SLU will accommodate Bell 103A/E/F/G/H, 203/D, and 113B or equivalent type modems. A BC01V-25 cable must be purchased separately to make connection to the modem. The transmit and receive data leads, (Data terminal ready and request to send) are permanently enabled are activated by this cable. The modem system must be a full-duplex dedicated line type modem. Furthermore, the READER RUN feature, normally present on local terminals, cannot be used.

6.3 SLU FUNCTIONAL DESCRIPTION

The SLU uses a Universal Asynchronous Receiver/Transmitter through drivers and a cable to the external device. The UART performs serial to parallel (receive) and parallel to serial (transmit) conversion of data received from or sent to a serial device.

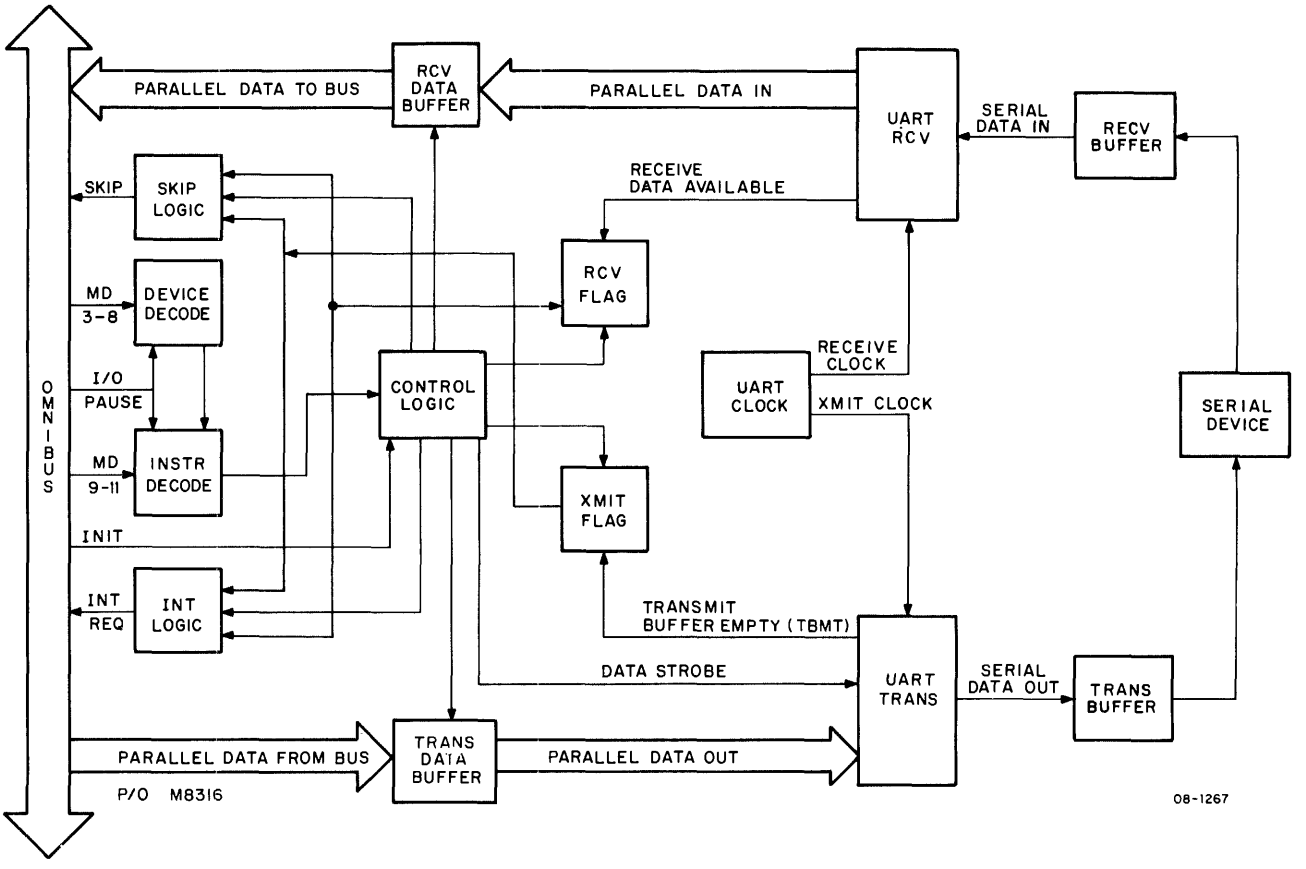


Figure 6-2 Serial Line Unit Block Diagram

Timing for the UART is derived from a 5.0688 MHz crystal oscillator and a network of frequency dividers. The frequency of the clock applied to the UART is determined by the Baud rate (its frequency is 16 times the Baud rate) which is switch selectable.

The SLU is operated via Programmed I/O. Instructions and data are received from the processor by way of the Omnibus. The programmed instructions are decoded by 2 instruction decoders which are enabled when I/O PAUSE L is asserted (low) on the Omnibus and either device code 03 or 04 is detected by the device select decoder. When this happens, Internal I/O L is also asserted (low).

The UART operation can best be understood by dividing the operation into two functions. A block diagram description of these functions is given in the following paragraphs.

6.3.1 Methods of Data Transfer

Data transfers between the AC and registers in the SLU may take place via Programmed I/O or Programmed Interrupts. The processor is interrupted by an INT RQST if the interrupt enable flag is set and the RECEIVE or XMIT flag sets. SKIP is asserted if the XMIT or RECEIVE flag sets while flags are being checked by the program.

6.3.2 Transmit Operation

Figure 6-3 is a block diagram of the UART transmit operation. The transmit portion of the UART receives an eight bit parallel character and changes it to 8 bits of serial data for transmission to a serial device. Bits 5, 6, and 7 are zeros if they are not used. The number of bits/characters is selected by installing jumpers (see Table 6-2).

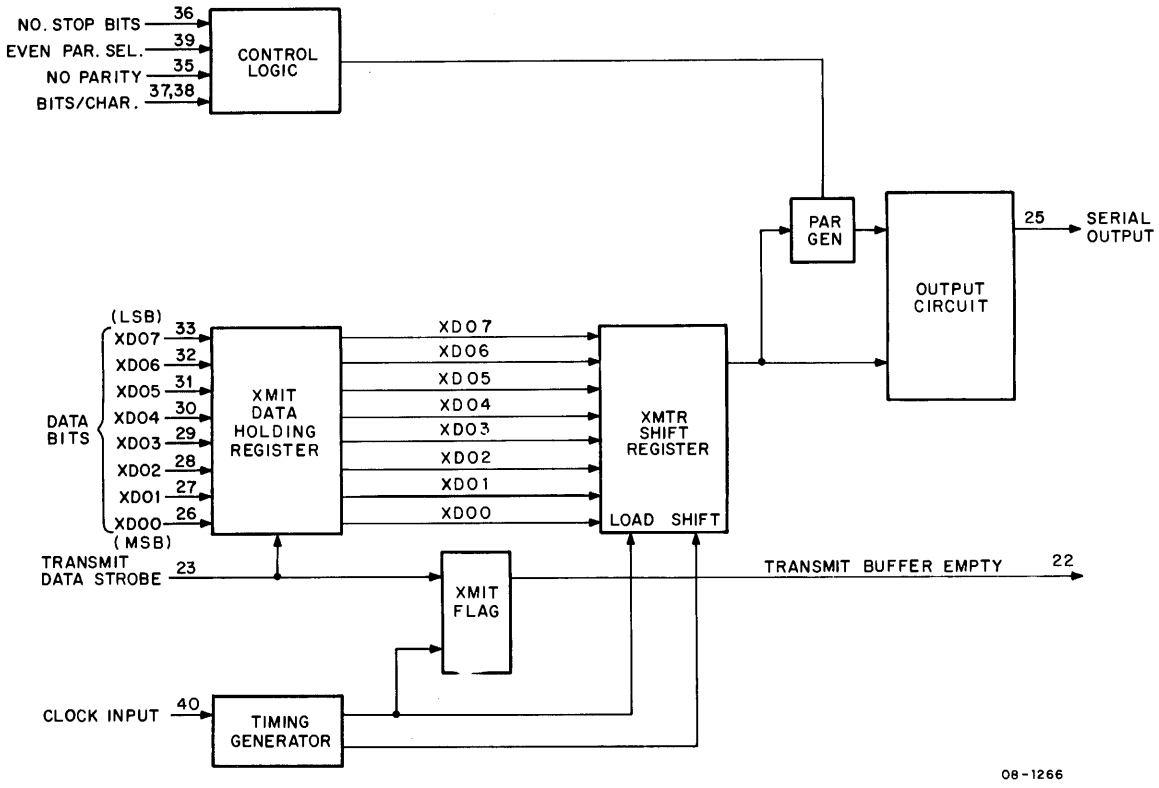


Figure 6-3 Transmitter Block Diagram (UART)

A transmit operation is started when the XMIT flag is set and parallel data is transferred from the AC to the DATA BUFFER register. A TRANSMIT DATA strobe is given loading the holding register. At this point TBMT is brought low by the UART. On the next transition of the transmit clock, the Holding register is transferred to the transmit shift register. TBMT is then allowed to go high setting the transmit flag. The transmit flag signals that the Holding register is empty and ready for another word. The UART then shifts out the word appending start and stop bits as required.

6.3.3 Receive Operation

A block diagram of the receive operation is shown in Figure 6-4. The receive portion of the UART will receive serial data from a serial device and change it to parallel data for transfer to the AC. Data from the device is assembled in the Receiver Shift register and transferred to the Data Holding register as parallel data. At this time, DATA AVAILABLE is asserted by the UART, the RECEIVE flag is set and the data should be transferred to the AC. Meanwhile, serial data from the device is available for transfer to the Data Holding register. The RECEIVE flag is cleared when the content of the Data Holding register is transferred to the AC.

6.3.4 SLU Timing Generator

Figure 6-5 is a block diagram of the SLU timing and baud rate generator. A 5.0688 MHz crystal oscillator and a programmable divider generate the clock signals required for the baud rates listed in Figure 6-5. The SLU clock signal is 16 times the selected baud rate. Different baud rates for transmit and receive are not allowed, thus the same clock is used for both transmit and receive operations. The baud rate is selected by 3 switches which supply inputs to the Baud rate selector.

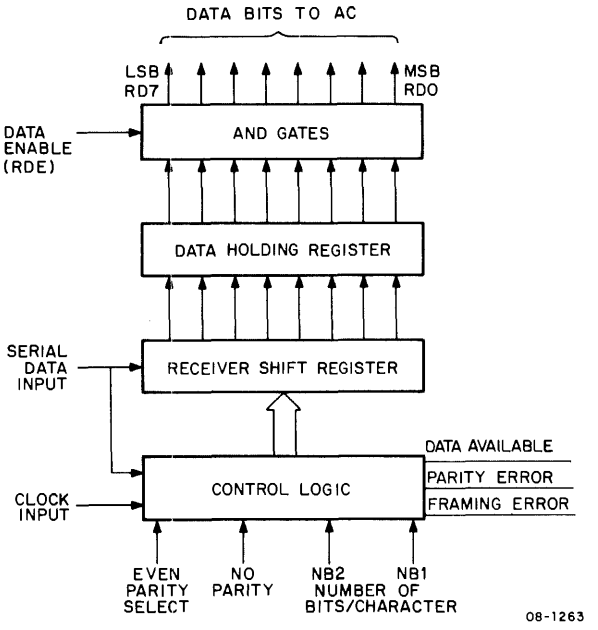
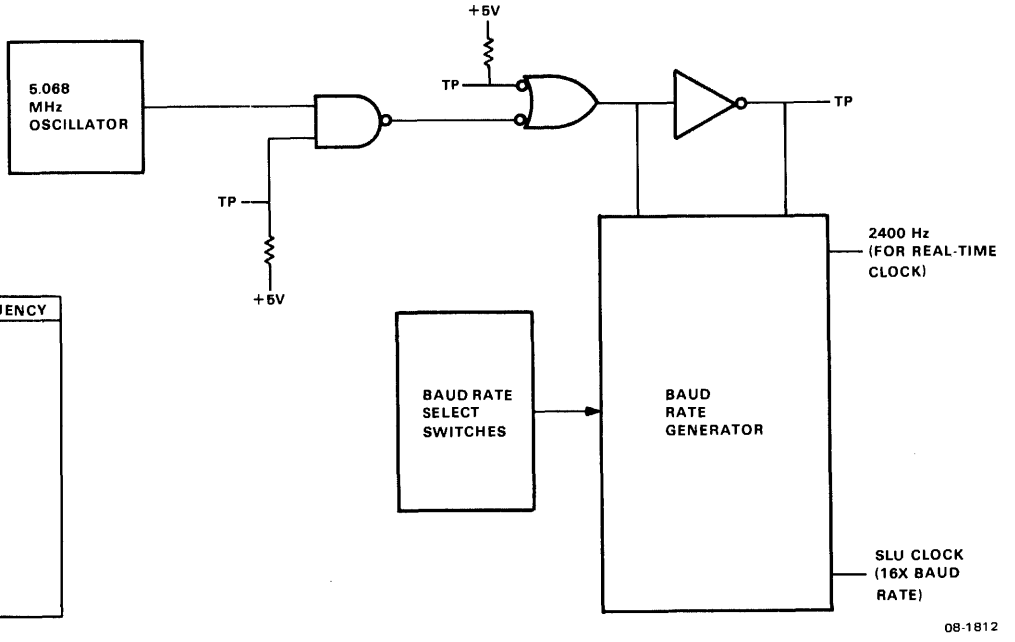


Figure 6-4 UART Receiver Block Diagram



BAUD RATE	CLOCK FREQUENCY (Hz)
50	800
75	1200
110	1760
134.5	2152
150	2400
300	4800
600	9600
1200	19.2K
1800	28.8K
2000	32K
2400	38.4K
3600	57.6K
4800	76.8K
7200	115.2K
9600	153.6K

Figure 6-5 Timing Generator Block Diagram

6.3.5 Parity Generation

Parity generation and checking may be enabled by grounding pin 32 on the UART chip. If this pin is not grounded (normal configuration) the UART will not check parity during receive or generate parity on transmit operations.

An Odd Parity Check is made if pin 39 on the UART is grounded and Even Parity Check is made if it is not.

6.3.6 Number of Bits Per Character

The number of bits per character may be 5, 6, 7, or 8 depending on jumper configuration of pins 37 and 38 of the UART (Table 6-2). The pins are grounded by using insulated wire jumpers to tie them to any point on the M8316 module which is grounded (drawing number D-CS-M8316-0-1).

6.4 SLU PROGRAMMING

The SLU IOT instructions are as follows:

Receive Instructions (Device Code 03)

Mnemonic	Octal Code	Function
KCF	6030	Clear receive flag, do not set reader run, do not request a new character from the reader if it is in operation, do not clear the AC. Reader run is automatically cleared by the new incoming character.
KSF	6031	Skip if the receive flag is set.
KCC	6032	Clear receive flag and AC, set reader run.
KRS	6034	Inclusive OR receive buffer into the AC.
KIE	6035	Load AC11 into interrupt enable for both receive and transmit. AC11 = 1. Enable interrupt AC11 = 0. Disable interrupt
KRB	6036	Combined KCC and KRS. Clear flag, load AC with contents of receive buffer, and set reader run.

Transmit Instructions (Device Code 04)

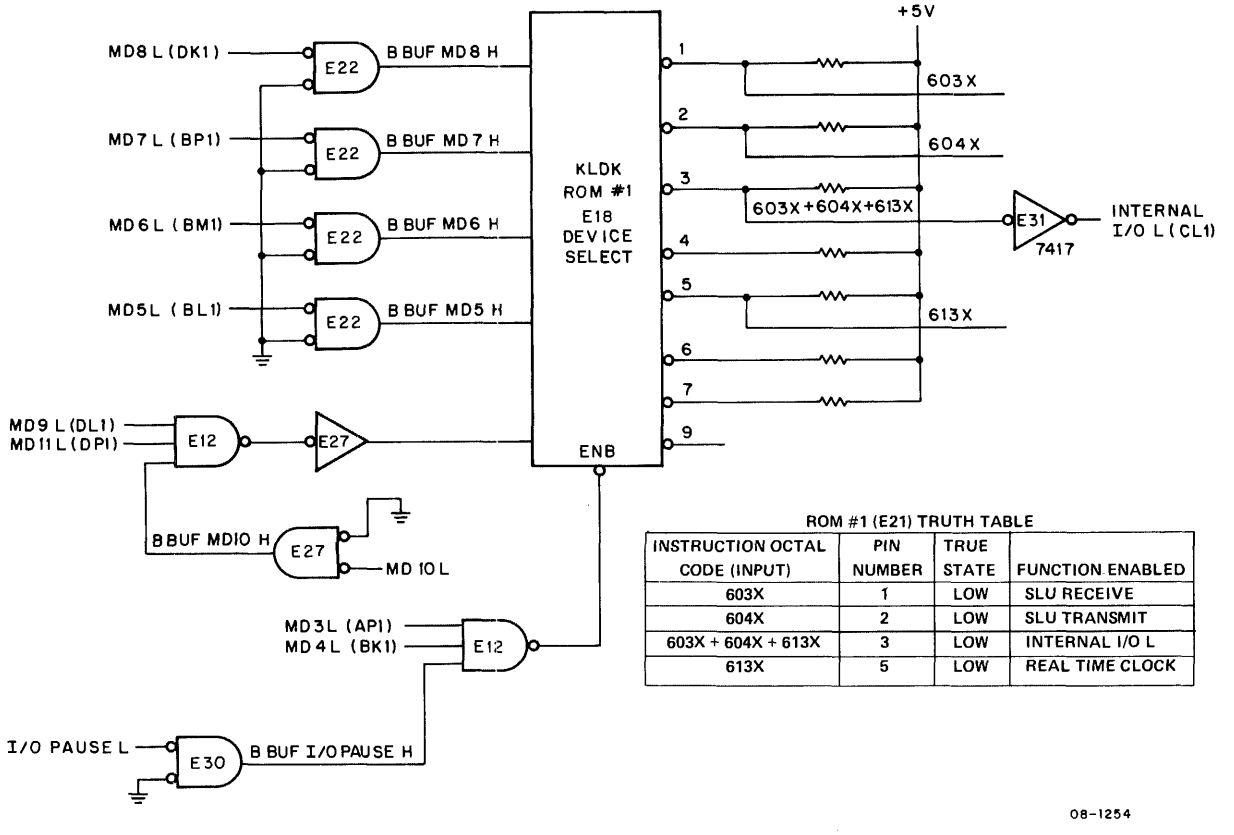
Mnemonic	Octal Code	Function
TFL	6040	Set transmit flag.
TSF	6041	Skip if the transmit flag is set.
TCF	6042	Clear transmit flag.
TPC	6044	Load AC into transmit buffer and transmit.
SPI	6045	Skip on transmit or receive flag if interrupt enable is set to a 1.
TLS	6046	Combined TCF and TPC commands.

6.5 SLU DETAILED LOGIC DESCRIPTION

The SLU Logic is divided into functional groups for discussion purposes. The block diagram in Figure 6-2 should be used to understand the interaction of the logic, the signal flow within the SLU and the input or output signals.

6.5.1 Device Select Logic

The device select logic for the SLU and the Real Time Clock are shown in Figure 6-6. MD3 and MD4 are gated by I/O PAUSE L to enable the device select ROM, when a 603X, 604X, or 613X instruction is decoded. The device select ROM asserts Internal I/O L for either of these instructions to cause the positive I/O interface to ignore these IOT instructions.



ROM #1 (E21) TRUTH TABLE

INSTRUCTION OCTAL CODE (INPUT)	PIN NUMBER	TRUE STATE	FUNCTION ENABLED
603X	1	LOW	SLU RECEIVE
604X	2	LOW	SLU TRANSMIT
603X + 604X + 613X	3	LOW	INTERNAL I/O L
613X	5	LOW	REAL TIME CLOCK

Figure 6-6 SLU and Real Time Clock Device Select Logic

The device select ROM also decodes MD5 – MD11 to generate three signals 603X, 604X, and 613X to enable the operation decoders for SLU and Real Time Clock. The truth table in Figure 6-6 gives the function enabled by the inputs to the device select ROM.

IOT instructions for the SLU are listed in Paragraph 6.4. ROM patterns for the SLU are contained in the M8316 engineering drawing in Appendix I.

6.5.2 SLU Operation Decoder

The SLU operation decoder is shown in Figure 6-7. The operation decoder consists of a ROM (E20) and a BCD to decimal decoder (E25) to decode MD9 – MD11. The BCD to decimal decoder is enabled by the signal 604X from the device select logic and decodes MD9 – MD11 to assert signals for the 6040, 6041, and 6045 instructions.

The ROM (E20) is addressed by MD9 – MD11, 603X, and 604X to decode the remainder of the SLU instructions (ROM No. 2 truth table in Figure 6-7).

The operation decoder supplies signals that represent the 603X and 604X instructions.

COL and C1L are asserted to control the direction of data transfer on the Data Bus (see Table 6-1).

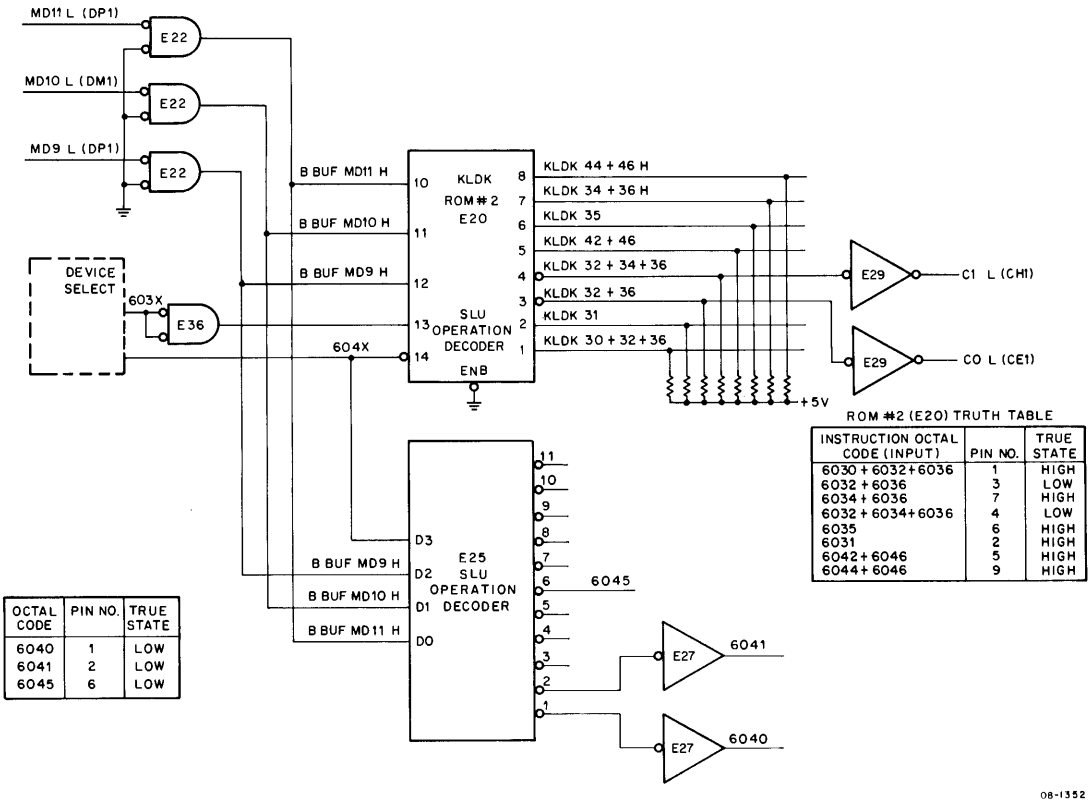


Figure 6-7 SLU Operation Decoder

Table 6-1
COL and C1L Levels for Data Bus Transfers

Instruction	COL	C1L	Direction of Transfer
6032	High	High	AC → Data Bus; 0 → AC
6034	High	Low	Data Bus → AC
6035	High	High	AC → Data Bus
6036	Low	Low	Data Bus → AC; 0 → AC
6044	High	High	AC → Data Bus
6046	High	High	AC → Data Bus

6.5.3 SLU Interrupt and Skip Logic

The interrupt and skip logic is used to interrupt the the program when a data transfer is required. To allow an interrupt, the INT EN flip-flop (E52) must be set by the 6035 instruction (Figure 6-8). The output of INT EN is gated with RCV FLAG or XMIT FLAG to assert INT RQST L when these flags are set. FCV FLAG is set when there is a character in the Receive Buffer register and XMIT FLAG is set when the transmit Buffer register is empty.

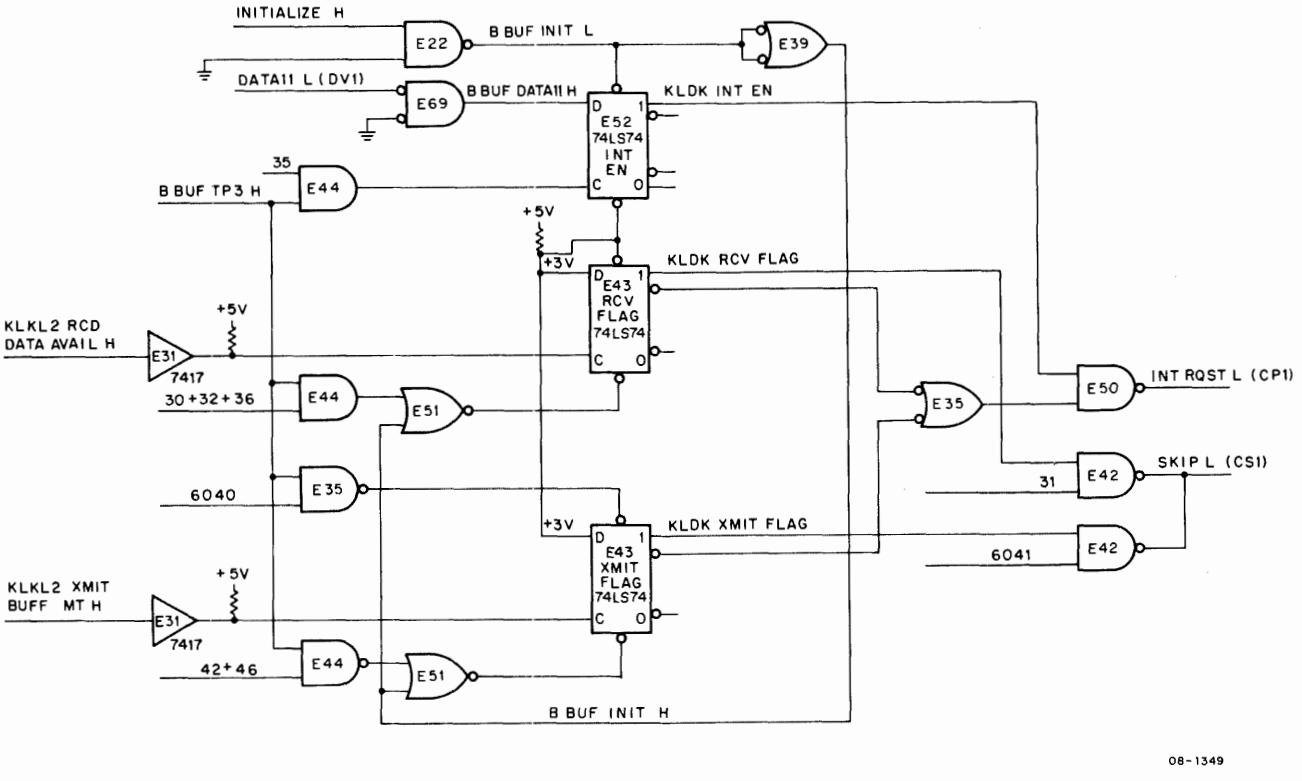


Figure 6-8 SLU Interrupt and Skip Logic

SKIP L is asserted when the RCV FLAG is set and a 6031 instruction is executed or when the XMIT FLAG is set and a 6041 instruction is executed. Assertion of SKIP L (low) causes the program to skip an instruction.

A more detailed description of the Interrupt and Skip logic can be found in Chapter 4.

6.5.4 SLU Timing Generator and Baud Rate Select Logic

The SLU Timing Generator is shown in Figure 6-9. The Timing Generator consists of a 5.0688 MHz oscillator and a dual baud rate generator. The SLU CLK signal is 16 times the baud rate selected by S1-1 through S1-4 (Figure 6-5). The SLU CLK is applied to the UART as both the receive and transmit clock (both are the same frequency). Thus, split baud rates are not available.

The dual baud rate generator is a programmable divider (see block diagram). The switches S1-1 to S1-4 will select the frequency for the SLU. See Table 6-2 for SLU baud rate switch settings. A second fixed frequency of 2400 Hz is also generated for use by the real time clock.

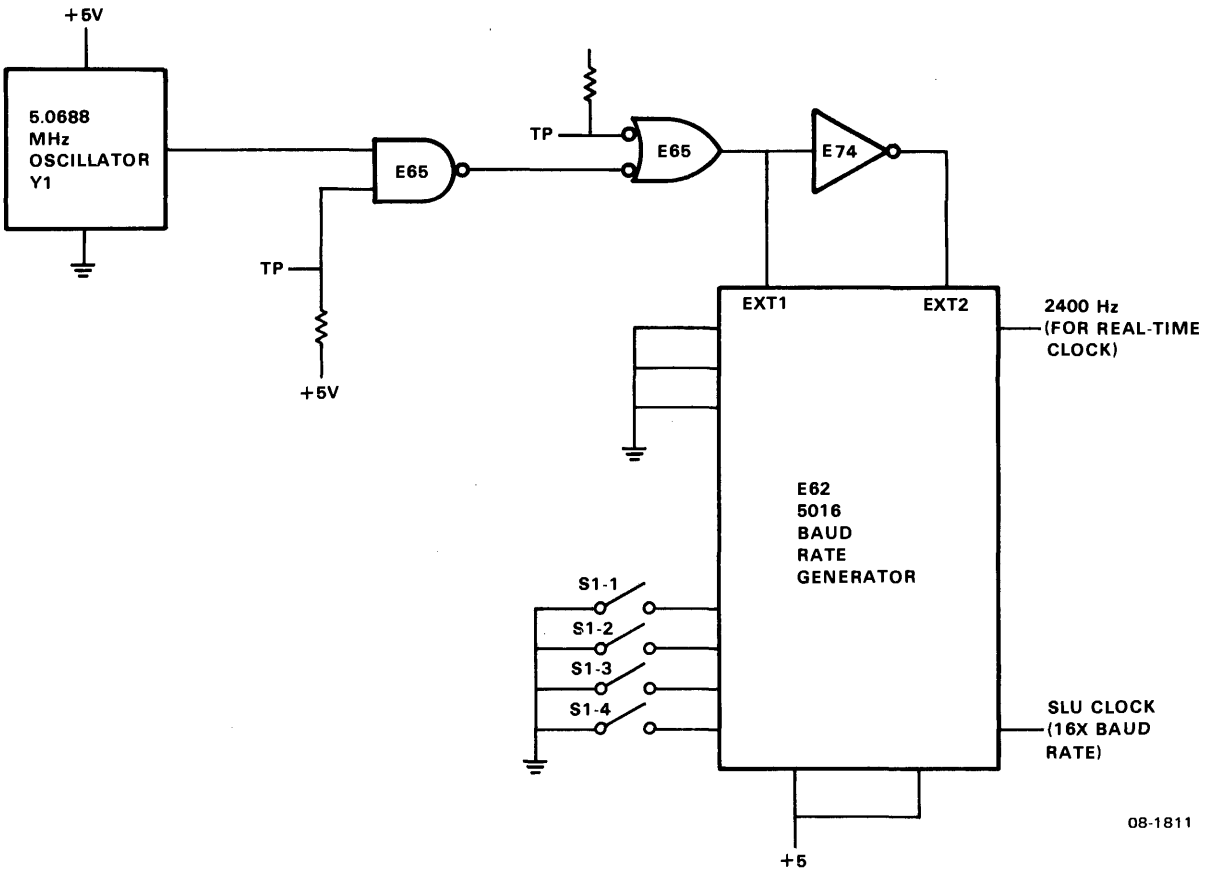


Figure 6-9 SLU Timing Generator and Baud Rate Select Logic

Table 6-2
D Etch SLU Baud Rate Select Chart

S1-4	S1-3	S1-2	S1-1	Baud Rate
ON	ON	ON	ON	50
ON	ON	ON	OFF	75
ON	ON	OFF	ON	110
ON	ON	OFF	OFF	134.5
ON	OFF	ON	ON	150
ON	OFF	ON	OFF	300
ON	OFF	OFF	ON	600
ON	OFF	OFF	OFF	1200
OFF	ON	ON	ON	1800
OFF	ON	ON	OFF	2000
OFF	ON	OFF	ON	2400
OFF	ON	OFF	OFF	3600
OFF	OFF	ON	ON	4800
OFF	OFF	ON	OFF	7200
OFF	OFF	OFF	ON	9600
*OFF	OFF	OFF	OFF	19.2K

*Serial line will *not* run at this baud rate. This setting is *not* to be used.

6.5.5 Universal Asynchronous Receiver/Transmitter (UART)

The UART (Figure 6-10) is a full duplex device with a receive and transmit section. The receiver section accepts serial binary characters from a serial device and converts them to a parallel format for transmission to the AC via the Data Bus. The transmitter section receives data in parallel format from the AC via the Data Bus and converts them to a serial data for output to a serial device. Table 6-3 lists the signals required to operate the UART in the SLU. The receiver block diagram (Figure 6-4) and transmitter block diagram (Figure 6-3) should be studied to understand the functional logic inside the UART.

6.5.5.1 UART Receive Operation – EIA or 20 mA serial data is received from a serial device (Figures 6-10 and 6-11) and converted to TTL levels (Paragraph 6.5.6). Each data character contains a start bit, 5, 6, 7, or 8 data bits and one or two stop bits (Figure 6-11). The number of data bits and stop bits are switch selectable (see Table 6-2). The stop bits are opposite in polarity to the start bits.

The converted serial input is used to supply an input to SERIAL IN on the UART. The signal is jumpered to pin E of J3 by installation of the proper cable for EIA or 20 mA operation.

The UART internally synchronizes the start bit with the clock input to ensure a full 16 clock period and keep the start bit independent of the time of data loading. The input bit is strobed at the center of the bit ±8%. A start bit that lasts for less than 1/2 of a bit time is rejected by the receiver.

When the receiver is in the idle state, it samples the serial input at the selected clock edges after the first low to high transition of the serial input. If the first sample is high, the receiver remains in the idle state and is ready to detect another low to high transition. If the sample is low, the receiver enters the data entry state.

There is no provision to detect parity errors in the received data, however data transmitted to a serial device may have an even or odd parity bit included in the data character (Table 6-2 and Figure 6-11).

The serial data is shifted into the UART a bit at a time and the occurrence of a stop bit indicates that the entire character has been received and shifted into the shift register. After the stop bit(s) has been sampled the receiver control logic parallel transfers the content of the Shift register to the Data Holding register (Figure 6-4) and asserts RCD DATA AVAIL H. RCD DATA AVAIL H sets the the RCV FLAG which pulls RESET AVAILABLE to clear Data Available and the processor will be interrupted to do a data transfer (Paragraph 6.5.3). Data is out on the Data Bus and transferred to the AC by the 6034 or 6036 instruction.

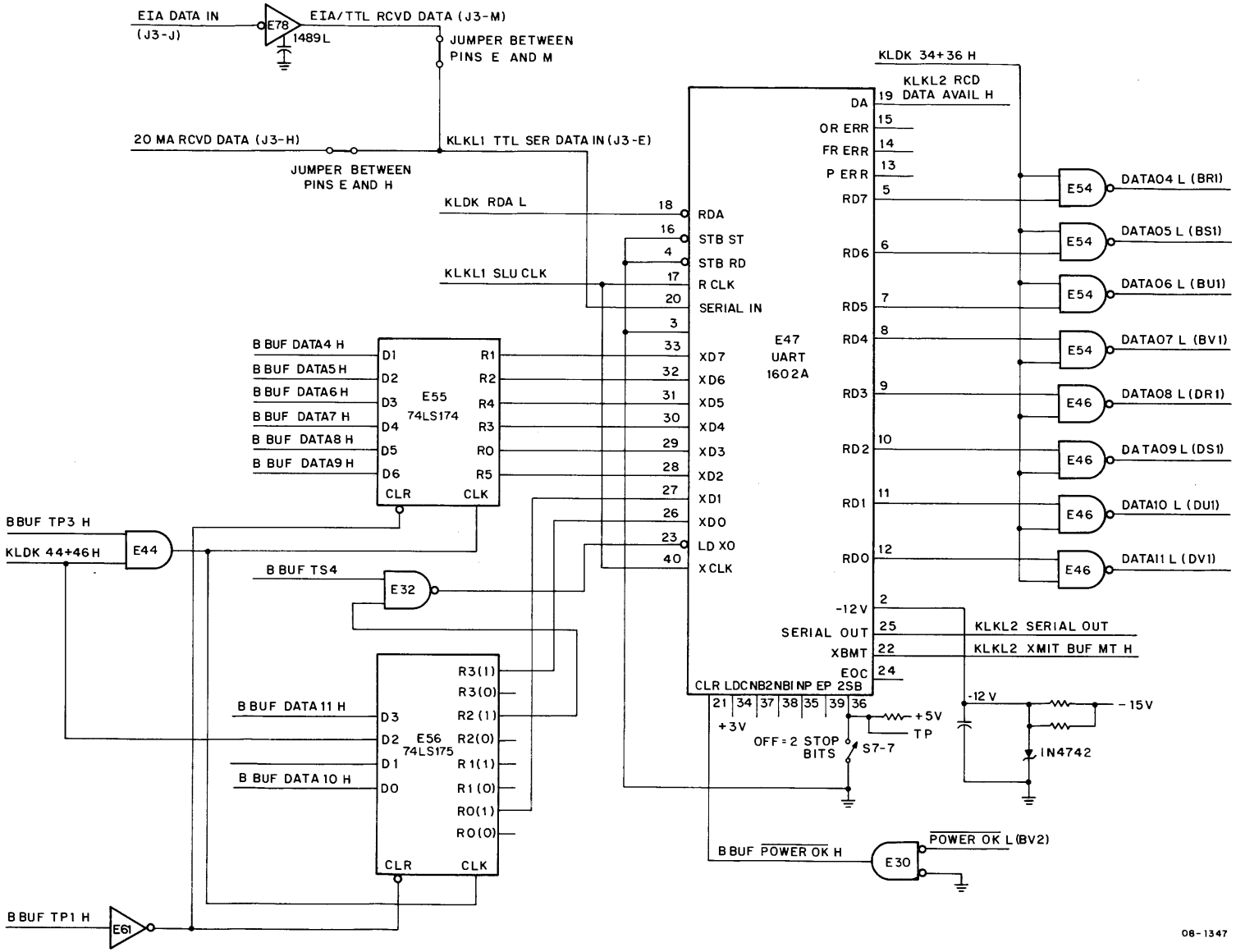


Figure 6-10 Format of Input/Output Character

Table 6-3
UART Signal Functions

Pin No.	Mnemonic	Name	Function
5–12	RD0–RD7	Received Data	Eight data out lines. RD7 (pin 5) is the MSB and RD0 (pin 12) is the LSB. When 5, 6, or 7 bit character is selected, the most significant unused bits are low. Character is right justified into the least significant bits.
13	PERR	Receive Parity	Not used.
14	FR ERR	Framing Error	Not used.
15	OR ERR	Overrun	Not used.
16	STB ST	Strobe Status	When asserted low, the transmit buffer output is applied to the output lines.
17	CLK	Receiver Clock	Input for an external clock whose frequency must be 16 times the desired receiver baud rate.
18	RDA	Reset Data Available	When low, resets the received DA (Data Available) line.
19	DA	Received Data Available	Goes high when an entire character has been received and transferred to the receiver Holding register.
20	SERIAL IN	Serial Input	Input for serial asynchronous data.
21	CLR	Clear (reset)	When power is turned on, this line is pulsed high by Power OK which resets all registers, sets serial output line high, and sets transmitter buffer empty line high.
22	XBMT	Transmitter Buffer Empty	Goes high when the transmitter Data Holding register may be loaded with another character.
23	LD XD	Data Strobe	Pulsed low to load the data bits into the transmitter Data Holding register during the positive-going trailing edge of the pulse.
24	EOC	End of Character	Not used.
25	SERIAL OUT	Serial Output	Output for transmitted character in serial asynchronous format. A mark is high and a space is low. Remains high when no data is being transmitted. Unused bits are held low out of the UART.
26–33	XD0–XD7	Data Input	Eight parallel Data In lines. XD7 (pin 33) is the MSB and XD0 (pin 26) is the LSB. If 5, 6, or 7 bit characters are selected, the least significant bits are used.
34	2 DC	Load Control	Not used.

Table 6-3 (Cont)
UART Signal Functions

Pin No.	Mnemonic	Name	Function
35	NP	No Parity	When high, eliminates the parity bit from the transmitted and received character and drives the received parity error line low. As a result, the receiver does not check parity on reception and during transmission the stop bits immediately follow the last data bit.
36	2 SB	Two Stop Bits	Selects the number of stop bits that immediately follow the data bits. A low inserts 1 stop bit and a high inserts 2 stop bits.
37, 38	NB2, NB1	Number of Bits per Character	Select 5, 6, 7, or 8 data bits per character as follows: **Bits/Character** — **NB2 (37)** — **NB1 (38)** 5 — L — L 6 — L — H 7 — H — L 8 — H — H
39	EP	Even Parity Select	Selects the type of parity to be added during transmission and checked during reception. A low selects odd parity and a high selects even parity.
40	X CLK	Transmitter Clock	Input for an external clock whose frequency must be 16 times the desired transmitter baud rate.

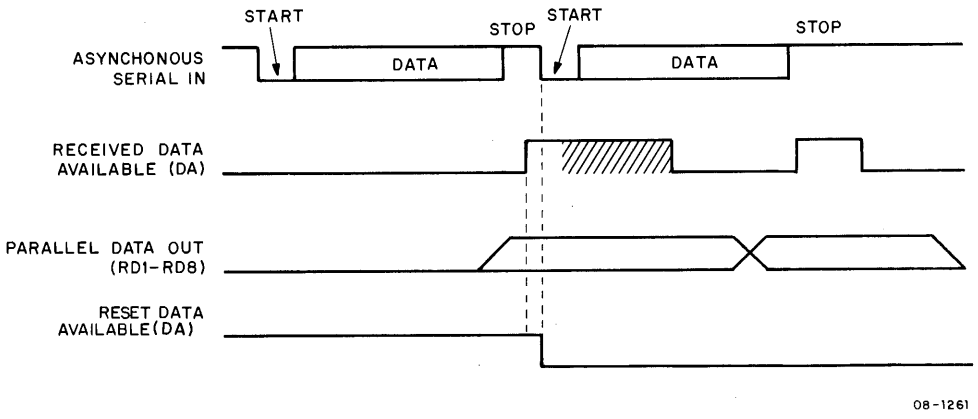


Figure 6-11 Receiver Timing Diagram

6.5.5.2 UART Transmit Operation – A transmit operation (Figure 6-10 and 6-12) is started when a parallel data character is transferred to the UART Data Holding register from the AC. The Data Buffer register (E55) is loaded by an 6044 or 6046 instruction at TP3H time. The data is then loaded into the Data Holding register during TS4. The 6046 instruction also clears the transmit flag.

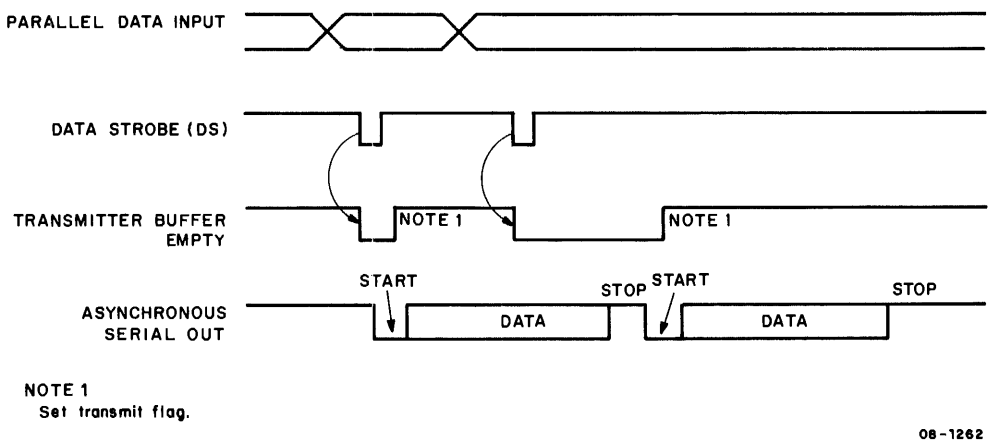


Figure 6-12 Transmitter Timing

The data is immediately transferred from the Data Holding register into the Shift register by the UART control logic. During this transfer the internal UART Control Logic will add Parity or no Parity, the stop bits, and provide for the correct number of data bits. The format is determined by the STOP BITS switch (S7-7) and jumpers installed on the UART pins (Table 6-2.) After the transfer is complete, XMIT BUF MT H is asserted to set the XMIT FLAG. At this time the program is interrupted for another data transfer (Paragraph 6.5.3).

The transmit flag is always cleared during a power up or initialize operation.

6.5.6 Level Converters

Level conversions are provided on both the receive and transmit lines between TTL levels of ground and +3 V to either EIA levels of ±12 V or 20 mA current loop of operation.

The receive converter logic is shown in Figure 6-13. The EIA DATA IN at J3 pin 5 is converted to TTL levels by E78 and then fed to pin M. A jumper on the cable for EIA devices feeds the signal to pin E and it is applied as input to the UART SERIAL IN pin.

In the 20 mA converter logic, Q7 and Q8 are normally turned off until the current goes above a threshold of 10 mA. A current greater than +10 mA turns Q7 on and a −10 mA turns Q8 on. When no signal is being received, Q7 and Q8 are turned off. The differential changes at pins K and S are sensed by Q7 and Q8, amplified by Q9 and Q10, and applied to the latch flip-flop. The latch flip-flop (E77) is used to eliminate noise on the receive line.

Switch S1-8 enables a filter when the ASR33 or ASR35 Teletype is the device connected to the SLU.

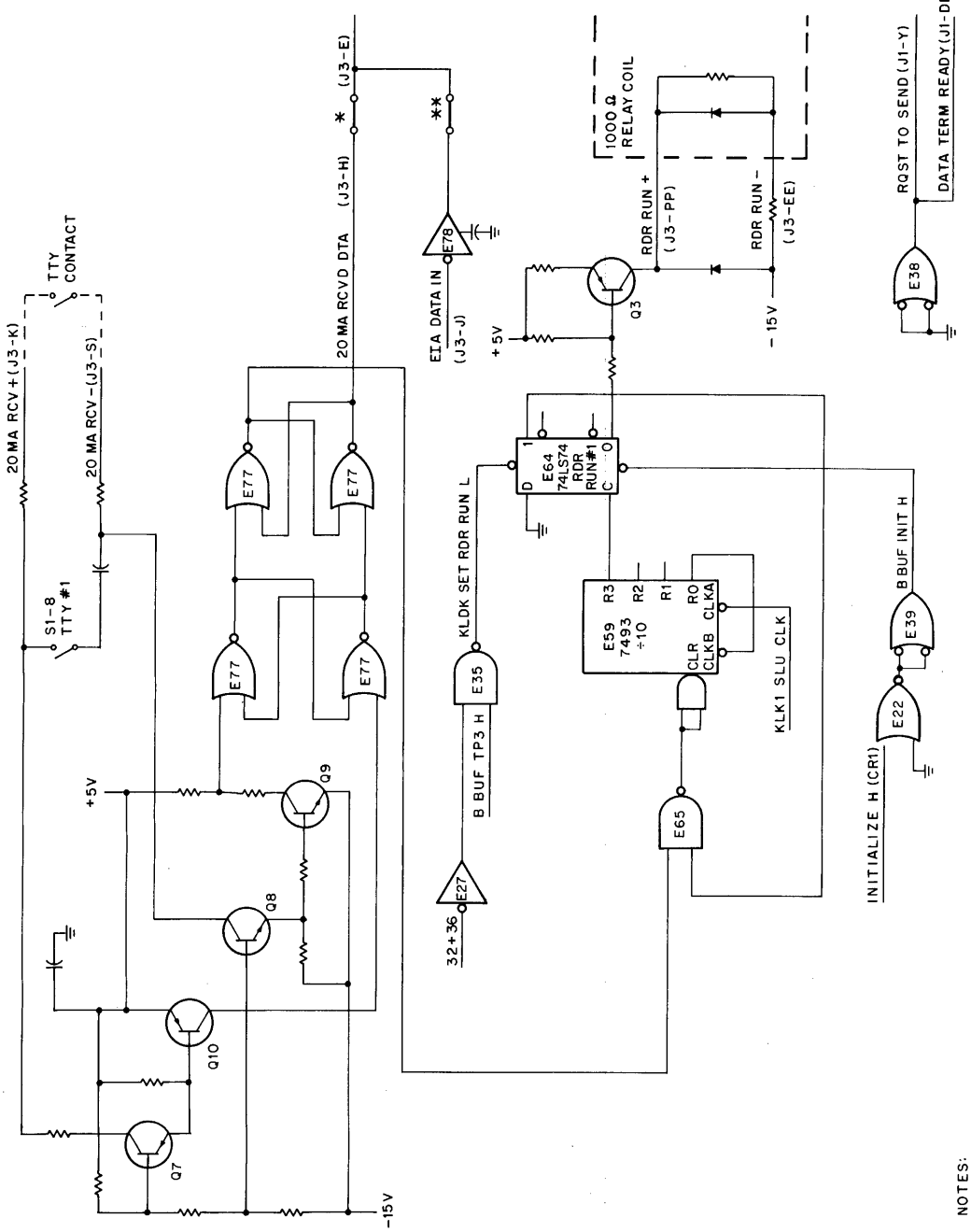
The 20 mA RCVD DTA data on pin H is jumpered to pin E by the cable used with 20 mA devices and it is applied to the SERIAL IN input on the UART.

The transmit level conversion for EIA data is done by E38 (Figure 6-14). E38 receives TTL data (0 and 3 V levels) from UART SERIAL OUT and changes it to −12 V levels.

In the TTL to 20 mA conversion logic, a low out of E63 produces a low at the base of Q4 (the series transistor) establishing a voltage divider from +5 to −15 V. This provides a bias to enable Q5 and Q6. The conduction of Q5 and Q6 establishes a differential current source for the 20 mA current loop through the external device.

6.5.7 Reader Run Logic

The RDR RUN flip-flop (Figure 6-13) is set when a 6032 or 6036 instruction is executed by the program. When RDR RUN is set, Q3 conducts and energizes the Reader Run relay in the external device.



NOTES:
* Jumper installed on cable for EIA DEVICES.
** Jumper installed on cable for 20ma DEVICES.

Figure 6-13 EIA and 20 mA to TTL Converters and Reader Run Logic

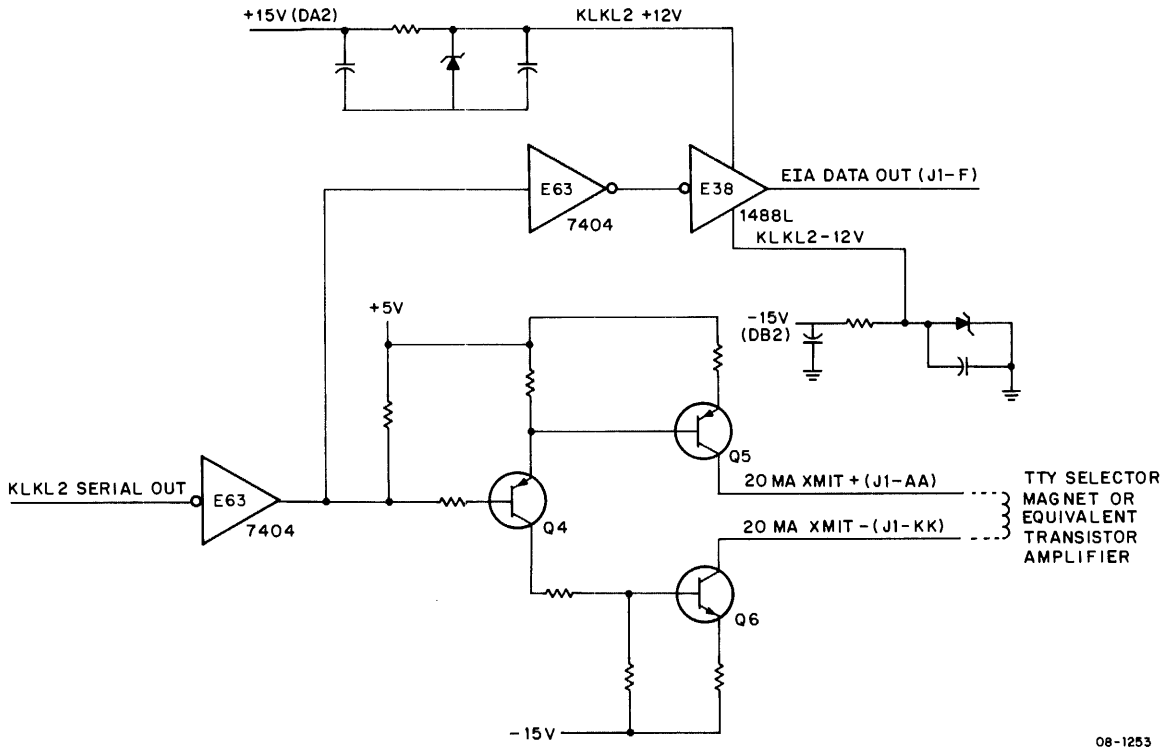


Figure 6-14 TTL to EIA and 20 mA Converters

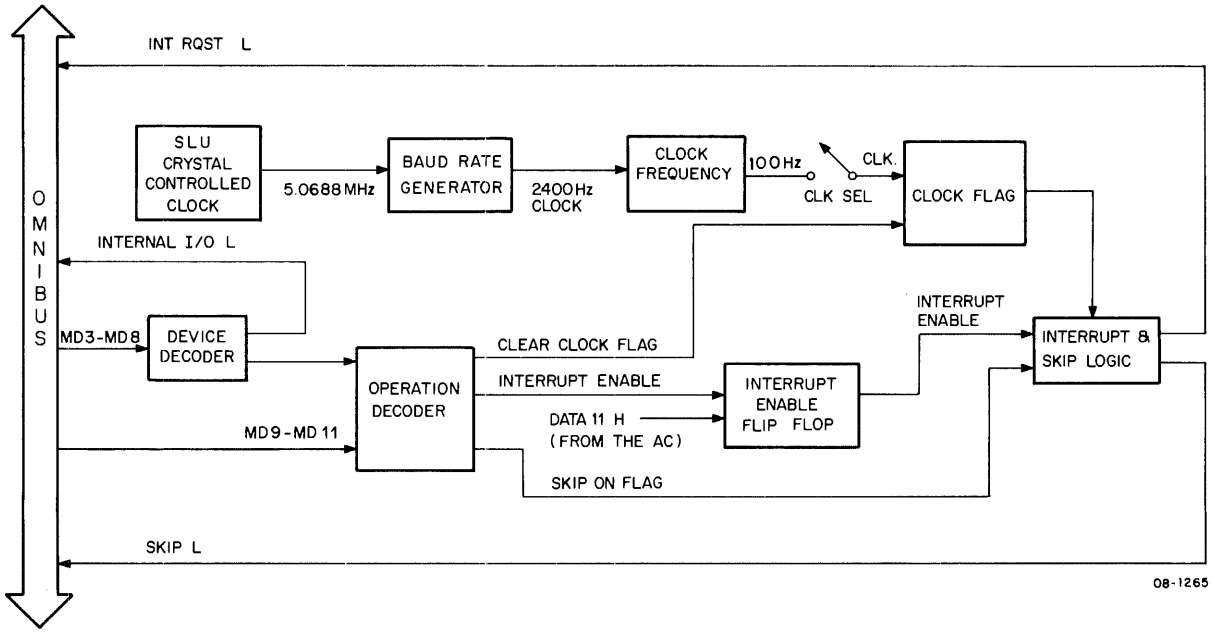


Figure 6-15 Real Time Crystal Clock Block Diagram

The divide by 10 counter (E59) provides for detection of noise spikes or random data on the receiver data line and the occurrence of a pulse that is shorter than 1/2 of a bit time.

The counter does not count until Reader Run sets, because AND gate E65 is disabled and a high is supplied to the CLR input of the counter. When RDR RUN sets, the start bit on the other input to NAND gate E65 enables the gate and removes the high input to CLR. The counter starts counting and after 8 clock pulses or 1/2 of a bit time, the RDR RUN flip-flop is cleared. This disables the AND gate and stops the counter.

6.5.8 Request to Send and Terminal Ready

For modem operation, the RQST TO SEND and DATA TERM READY signals are always asserted (high) by a ground applied to NOR gate E38 (Figure 6-13).

6.6 REAL TIME CLOCK

The Real Time Crystal Clock interrupts the processor every 10 ms if interrupt enable is set (100 Hz for ±0.01%). A Skip instruction causes the program to skip an instruction if the clock flag is set.

Figure 6-15 is a block diagram of the Real Time Crystal Clock. The 100 Hz clock signal is generated by a 5.0688 MHz crystal controlled clock and a group of frequency dividers. The CLK SEL switch enables the clock to be applied to the CLOCK FLAG, which sets each time a clock pulse is generated.

When the CLOCK FLAG sets, the program is interrupted by INT RQST L if interrupts are enabled, or by SKIP L if the program executes the Skip IOT.

6.7 REAL TIME CLOCK PROGRAMMING

The instructions used to program the Real Time Crystal Clock are as follows:

Mnemonic	Octal Code	Function
CLLE	6135	Load the interrupt enable from the AC11. AC11 = 1, set interrupt enable AC11 = 0, clear interrupt enable Interrupt enable is turned off when power is turned on and when the system is initialized by INIT on the Programmer's Console, or if the CAF instruction is executed.
CLCL	6136	Clear clock flag.
CLSK	6137	Skip on clock flag.

6.8 REAL TIME CLOCK DETAILED LOGIC DESCRIPTION

The Real Time Clock logic is divided into functional groups for discussion purposes. Figure 6-15 should be used to understand the relationship between the groups of logic and the flow of signals and data between them.

6.8.1 Device Select and Operation Decoder Logic

The device select logic for the Real Time Clock is the same as that for the SLU (Figure 6-6). When one of the Real Time Clock instructions is detected, the 613X signal (Figure 6-16) enables the clock operation decoder (E25). E25 is a BCD to decimal decoder which decodes MD<9:11> to determine what operation the Real Time Clock will do.

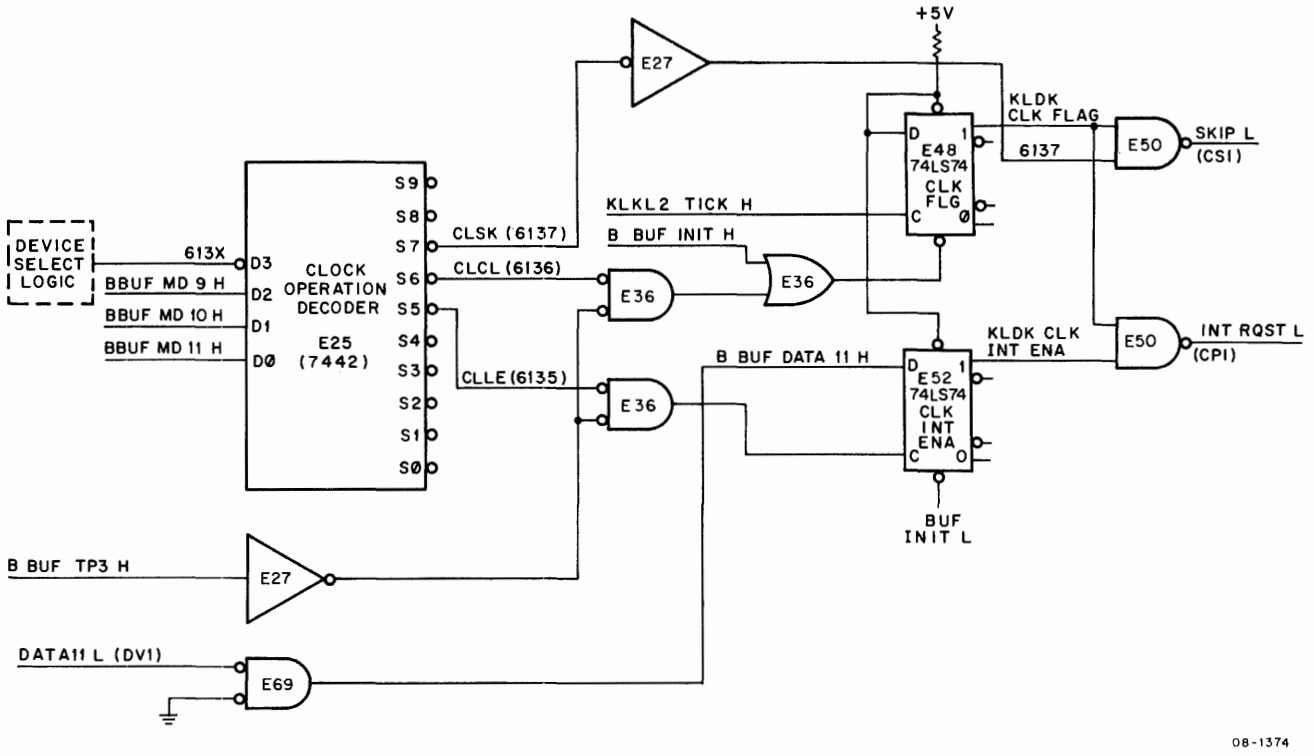


Figure 6-16 Real Time Clock IOT Decoder and Interrupt and Skip Logic

6.8.2 Real Time Clock Frequency Dividers

The Real Time Clock frequency dividers are shown in Figure 6-17. If TEST SWITCH (S1-6) is set to on to apply a ground to the CLR input of the divide by 12 counter (E37), the counter is enabled. E37 is a modified divide by 16 counter which has the divide by 2 output tied to the CLK BC input to cause a divide by 12 operation, and generation of a 200 Hz output. The 200 Hz signal is applied to (a divide by two counter) to generate the 100 Hz TICK H signal which is used to set the CLOCK FLAG (Figure 6-16) if S1-5 is set to ON.

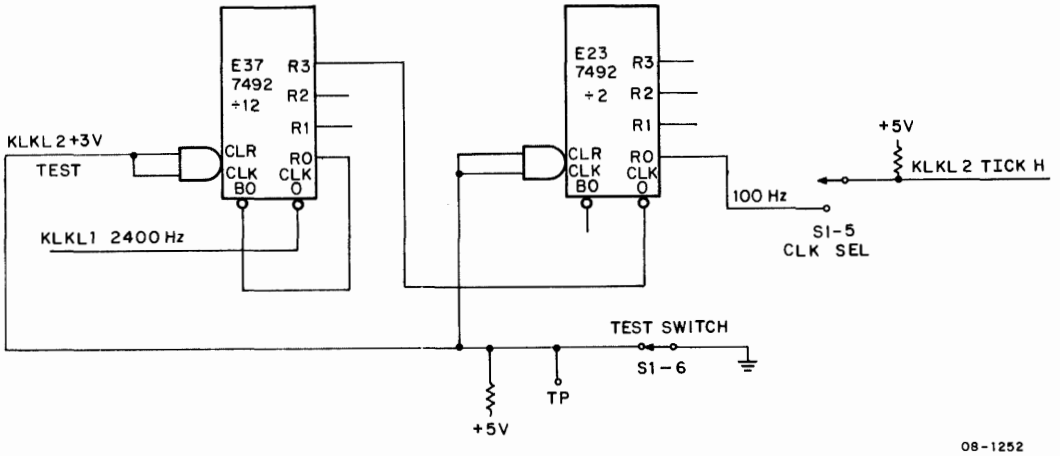


Figure 6-17 Real Time Clock Frequency Dividers

6.8.3 Real Time Clock Interrupt and Skip Logic

The interrupt and skip logic is used to interrupt the program at a 100 Hz rate.

INT RQST L is asserted when the CLOCK FLAG sets if the CLOCK INTERRUPT ENABLE flip-flop is set. CLOCK INTERRUPT ENABLE is set by DATA11 from the AC being a one when the 6135 instructions is executed by the program. SKIP L is asserted and the program skips an instruction if the CLOCK FLAG sets and 6137 instruction is executed by the program.

6.9 GENERAL PURPOSE PARALLEL I/O BLOCK DIAGRAM DESCRIPTION

The General Purpose Parallel I/O (Figure 6-18) allows the PDP-8/A to transmit or receive one 12-bit word at a time between user designed logic on single ended data lines or two PDP-8/A processors to transfer data to each other, provided each processor has a DKC8-AA I/O option board and the proper cables.

All data transfers are between the AC and an external device via programmed I/O. Data transfer rate is limited by program execution time to approximately 50K words/second.

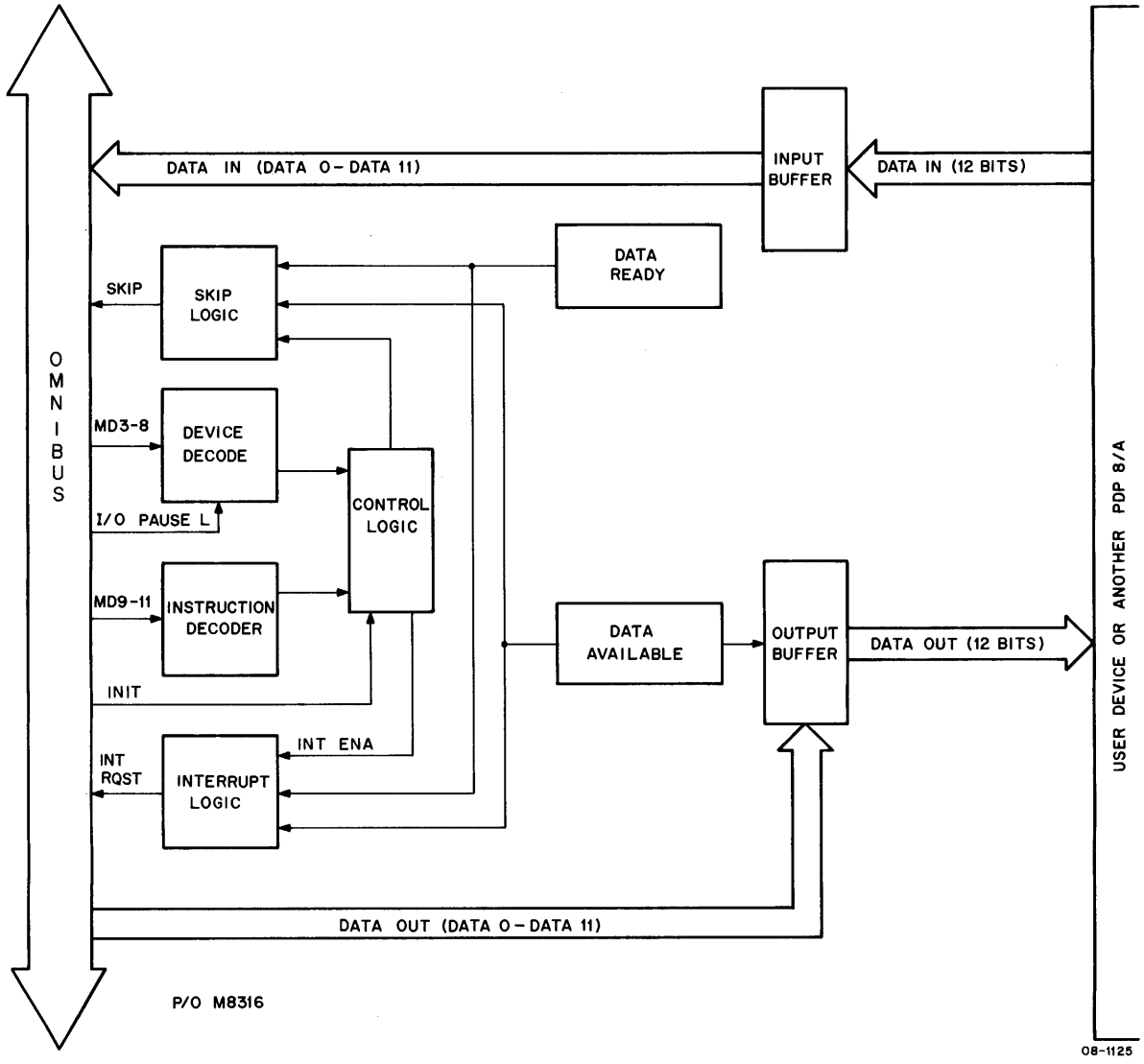


Figure 6-18 General Purpose Parallel I/O Block Diagram

FEATURES

Input/Output:	2 bits of parallel data input and output. Data is logic low true for both transmit and receive operations.
Drive Capability:	Each output drives up to 25 TTL unit loads. Data In presents 4 TTL unit loads to the driver circuit. Maximum cable length is 250 ft for transmit or receive.
Signal Levels:	Logic High is 4.0 V to 2.6 V. Logic Low is 0.0 V to 0.6 V. All signals are TTL compatible.
Cables:	All cables must be ordered separately. The BC08R cable should be used, the standard length is 10 ft, but other lengths up to 250 ft are available on special order. Two cables are needed if both transmit and receive functions are used. The BC80A-0-0 cable in lengths of 25, 50, and 100 ft are available for use with the LA180 printer. Plug the Parallel I/O into Digital standard logic blocks. The use of one or two M9100 cables is required. To transmit data between two PDP-8/A computers, use two BC08R cables. Each cable connects J5 of one DKC8-AA to J4 of the other. The cable must be turned over (connected backwards: pin A is plugged into the pin VV end of the connector) at one end of each cable. (Tables 6-4 and 6-5).

6.10 GENERAL PURPOSE PARALLEL I/O PROGRAMMING

The following instructions are used to program the General Purpose Parallel I/O:

Mnemonic	Octal Code	Function
DBST	6570	Skip on Data Accepted, clear Data Accepted and Data Available, if Data Accepted flag is set.
DBSK	6571	Skip on Data Ready flag.
DBRD	7572	Read data in to AC0-AC11.
DBCF	6573	Clear Data Ready flag, issue Data Accepted out pulse.
DBTD	6574	Load AC0-AC11 into buffer and transmit data out.
DBSE	6575	Set interrupt enable to a 1.
DBCE	6576	Reset interrupt enable to a 0.
DBSS	6577	Issue a strobe pulse.

6.11 DETAILED LOGIC DESCRIPTION

The General Purpose Parallel I/O logic is divided into functional groups for discussion purposes. The block diagram in Figure 6-18 should be used to understand the relationship between the groups of logic.

6.11.1 Device Select and Operations Decoder

The device select and operations decoder logic is shown in Figure 6-19. Bits MD3 – MD8 are gated by I/O PAUSE L when a 657X instruction is decoded to enable the operations decoder and assert INTERNAL I/O L. INTERNAL I/O L causes the positive I/O bus interface to ignore this instruction.

The operations decoder (E25) decodes MD9 – MD11 to determine what operation is to be performed by the parallel I/O. E25 is a BCD to decimal decoder which decodes the 3 bits and asserts one of the output pins to represent instructions 6571 through 6577. When a 6752 instruction is decoded, C0 L and C1 L are asserted (low) to allow data to be transferred from the Data Bus to the AC.

Table 6-4
J4 Input Signal Pin Assignments

Fingers M9100	J1	DKC8-AA J4 Pin No.	Signal Name	Comments
D1	SS	D	STROBE L	450 ns control pulse drives 10 unit loads.*
F1	PP	F	Not used	
J1	MM	J	Not used	
L1	KK	L	DATA IN 0 L	Most significant bit.
N1	HH	N	DATA IN 1 L	Input data low is true.**
R1	EE	R	DATA IN 2 L	
S1	CC	T	DATA IN 3 L	
V1	AA	V	Not used	
U1	Y	X	SET DATA READY L	Low when input data is valid.
U2	W	Z	DATA ACCEPTED OUT L	Low when input data is accepted. Drives 25 unit loads.*
C1	U	BB	Not used	
D2	S	DD	DATA IN 4 L	
F2	P	FF	DATA IN 5 L	
J2	M	JJ	DATA IN 6 L	
L2	K	LL	DATA IN 7 L	Input data, low is true.**
N2	H	NN	DATA IN 8 L	
R2	E	RR	DATA IN 9 L	
T2	C	TT	DATA IN 10 L	
V2	A	VV	DATA IN 11 L	Least significant bit.

All unspecified pins are ground.
*Unit load = 1.6 mA @ logic low and 0.04 mA @ a logic high.
**Presents 4 unit loads to the drive circuit.

Table 6-5
J5 Output Signal Pin Assignments

Fingers M9100	J1	DKC8-AA J5 Pin No.	Signal Name	Comments
D1	SS	D	Not used	
F1	PP	F	Not used	
J1	MM	J	Not used	
L1	KK	L	DATA OUT 0 L	Most significant bit.
N1	HH	N	DATA OUT 1 L	
R1	EE	R	DATA OUT 2 L	Output data, low is true.**
S1	CC	T	DATA OUT 3 L	
V1	AA	V	Not used	
U1	Y	X	DATA AVAILABLE L	Low when output data is valid.
U2	W	Z	DATA ACCEPTED IN L	Low when output data is accepted. Presents 4 unit loads to the driver circuit.*
C1	U	BB	Not used	
D2	S	DD	DATA OUT 4 L	
F2	P	FF	DATA OUT 5 L	
J2	M	JJ	DATA OUT 6 L	
L2	K	LL	DATA OUT 7 L	Output data, low when true.**
N2	H	NN	DATA OUT 8 L	
R2	E	RR	DATA OUT 9 L	
T2	C	TT	DATA OUT 10 L	
V2	A	VV	DATA OUT 11 L	Least significant bit.

Pins A, B, C, E, H, K, M, P, S, U, W, Y, AA, CC, EE, HH, KK, MM, PP, and SS are grounded.
*1 unit load.
**Each output can drive 25 unit loads.

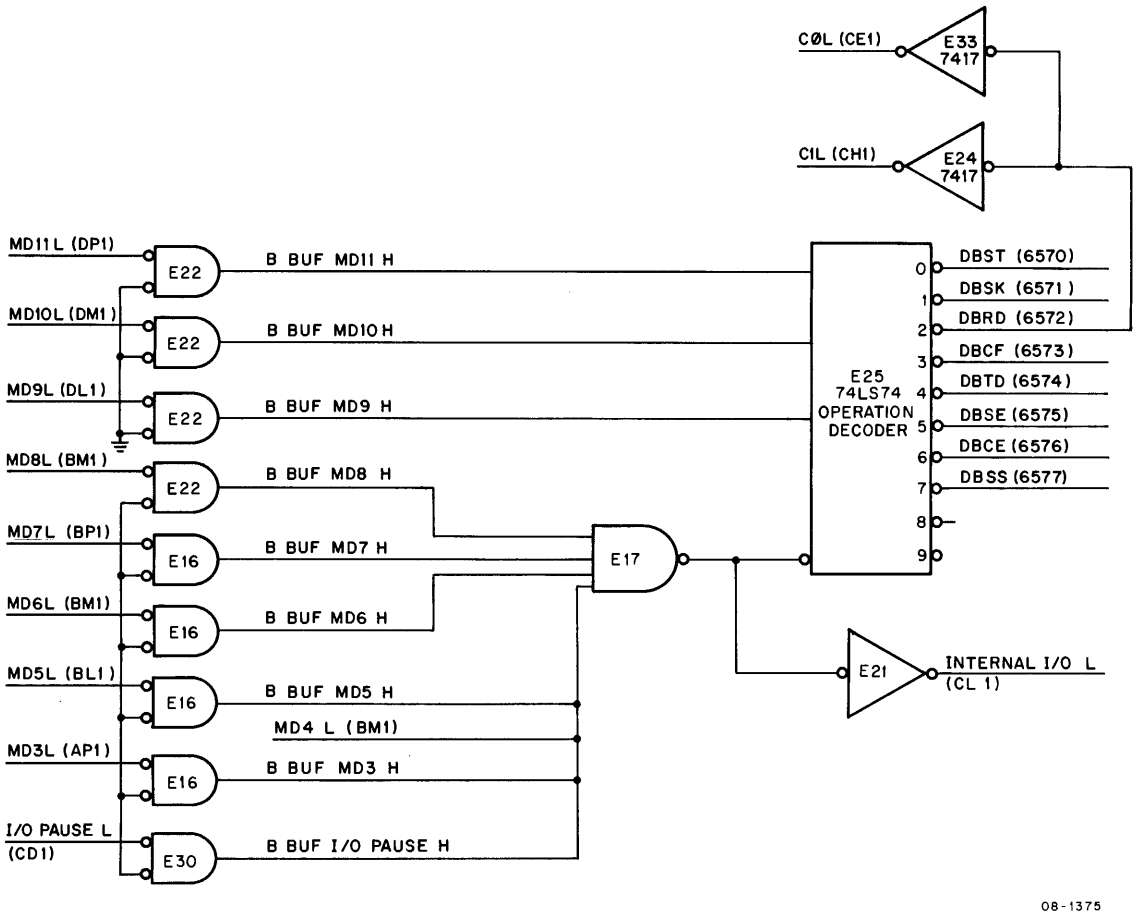


Figure 6-19 Parallel I/O Device Select and Operation Decoder

6.11.2 Interrupt and Skip Logic

The interrupt and skip logic is used to interrupt the program when a data transfer is required. To allow an interrupt to occur, INT ENA must be set by the 6575 instruction. The one output of INT ENA allows INT RQST L to be asserted when DATA READY or B DATA IN sets. SKIP L is asserted if the 6571 instruction is decoded and B DATA IN is set, or if the 6570 instruction is decoded and DATA READY is set. (See the transmit and receive operations in paragraph 6.11.3 for operation of these flags.)

6.11.3 Receive and Transmit Operations

The receive and transmit operations are described separately in the following paragraphs.

6.11.3.1 Transmit Operation – To transmit a 12-bit data word perform the following:

1. Load the output buffer by use of IOT 6574 (Figure 6-20). Data will be transferred from the data lines on the bus into the buffer at TP3 time.

2. At the trailing edge of TP3, DATA AVAILABLE becomes true (low) on the output cable (Figure 6-20). There is a switch on the M8316 that will cause DATA AVAILABLE to be negated (go high) on the leading edge of the next TS1 pulse, if this is desired. This yields a pulse of about 450 ns in duration on the DATA AVAILABLE signal line. The trailing edge of the pulse, on DATA AVAILABLE, could be used to strobe the output data of the M8316 into the user's register. If TS1 is not used to negate DATA AVAILABLE, IOT 6570 (DBST) should be used to negate DATA AVAILABLE.

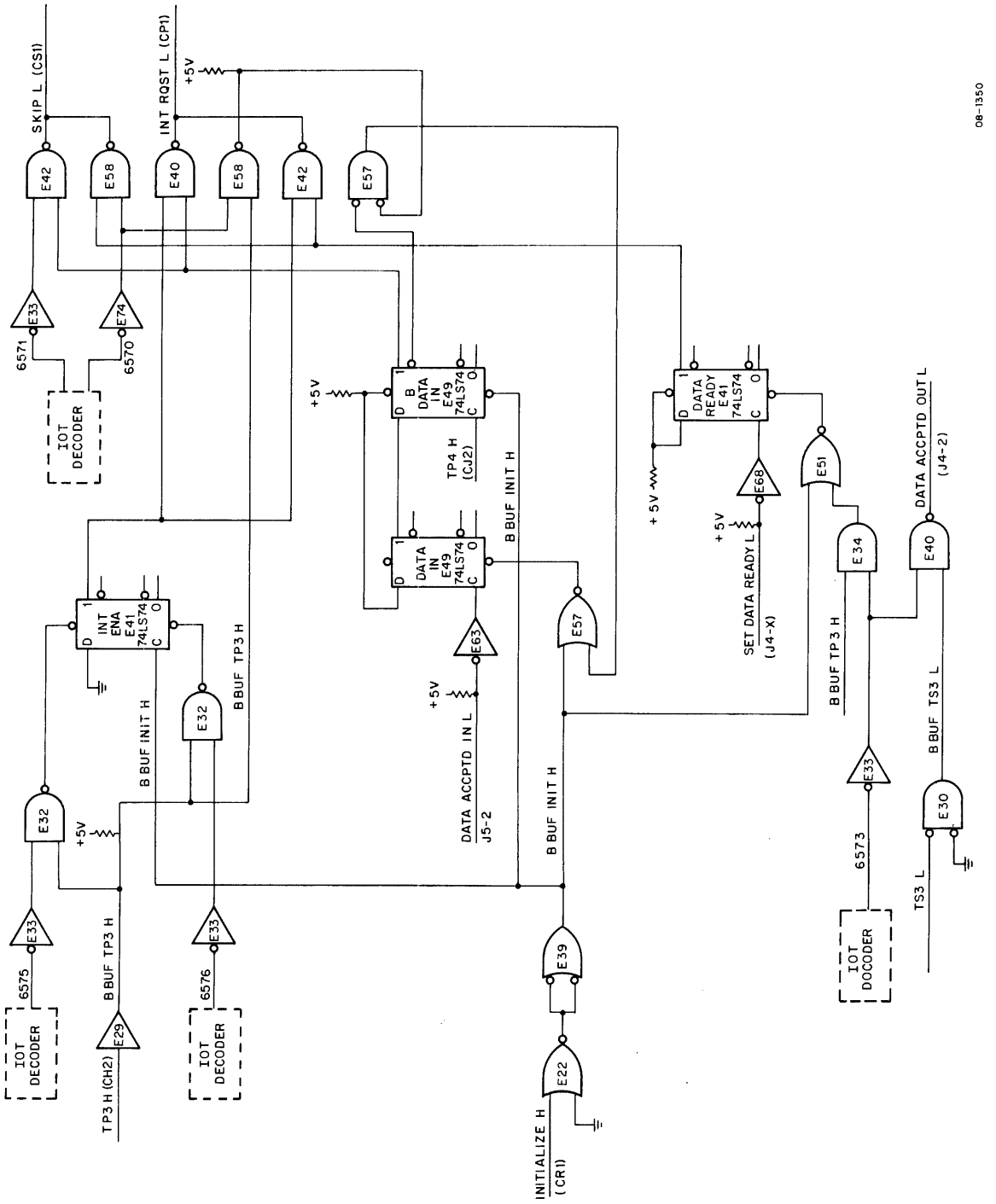


Figure 6-20 General Purpose Parallel I/O Interrupt and Skip Logic

3. The receiving device should then ground DATA ACCEPTED IN to signal the CPU that the transmitted data has been received.

4. Assuming interrupt enable is true, the DATA ACCEPTED flip-flop will assert INT RQST L on the bus. (Figure 6-20).

5. The CPU then executes IOT 6570 to test the DATA ACCEPTED flip-flop and to clear both DATA AVAILABLE and DATA ACCEPTED flip-flops. At TP3 of IOT 6570, DATA AVAILABLE will go high on the output cable. This signals the end of the transmit sequence.

6.11.3.2 Receive Operation – The receive sequence is as follows:

1. The external device places data in some type of latching register then grounds the SET DATA READY line on the input cable which raises the DATA READY flag. (Figure 6-20).

2. Assuming INTERRUPT ENABLE is true, INT RQST L will be asserted on the bus.

3. The CPU then executes the 6571 IOT to test the DATA READY flip-flop; then IOT 6572 should be issued to read the input data into AC0-11. (Figure 6-23).

4. The CPU should then execute IOT 6573 to clear DATA READY. This also sends a pulse out on the DATA ACCEPTED out line on the input cable. This signal should be used by the external device to negate the SET DATA READY signal.

6.11.4 Strobe

IOT 6577 (Figure 6-21) creates a pulse on the STROBE line that goes from the high to low state at TP3 of IOT 6577 and returns to the high state at the next TS1. This pulse may be used to start an event external to the CPU or it may signal the end of an event.

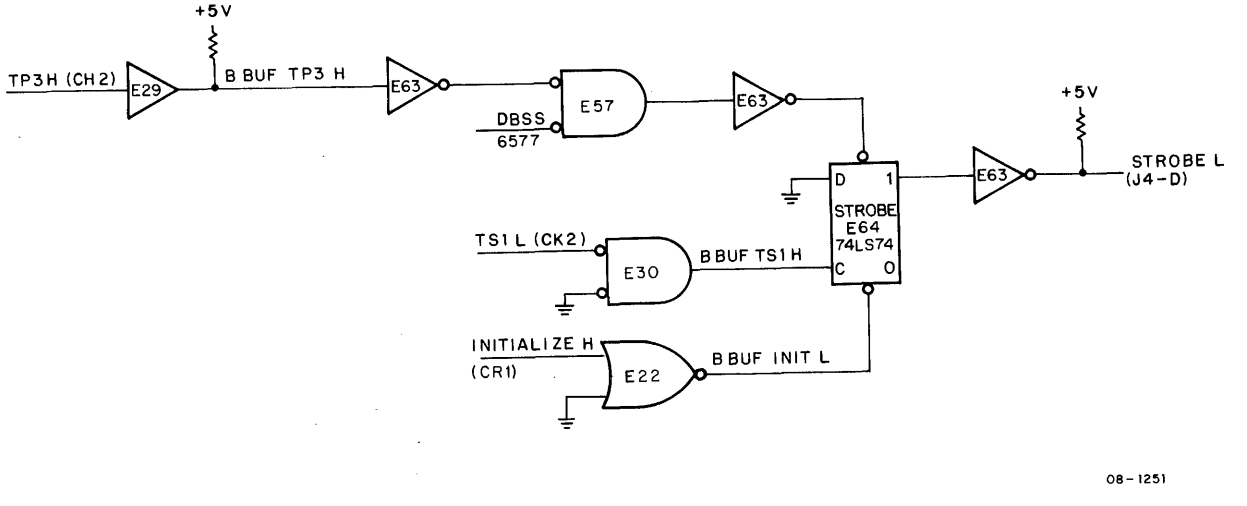


Figure 6-21 Parallel I/O Strobe Logic

6.11.5 Parallel I/O Output Register

The Parallel I/O output register (Figure 6-22) is loaded from the AC by a 6574 instruction and is loaded into the Transmit Buffer at TP3 time.

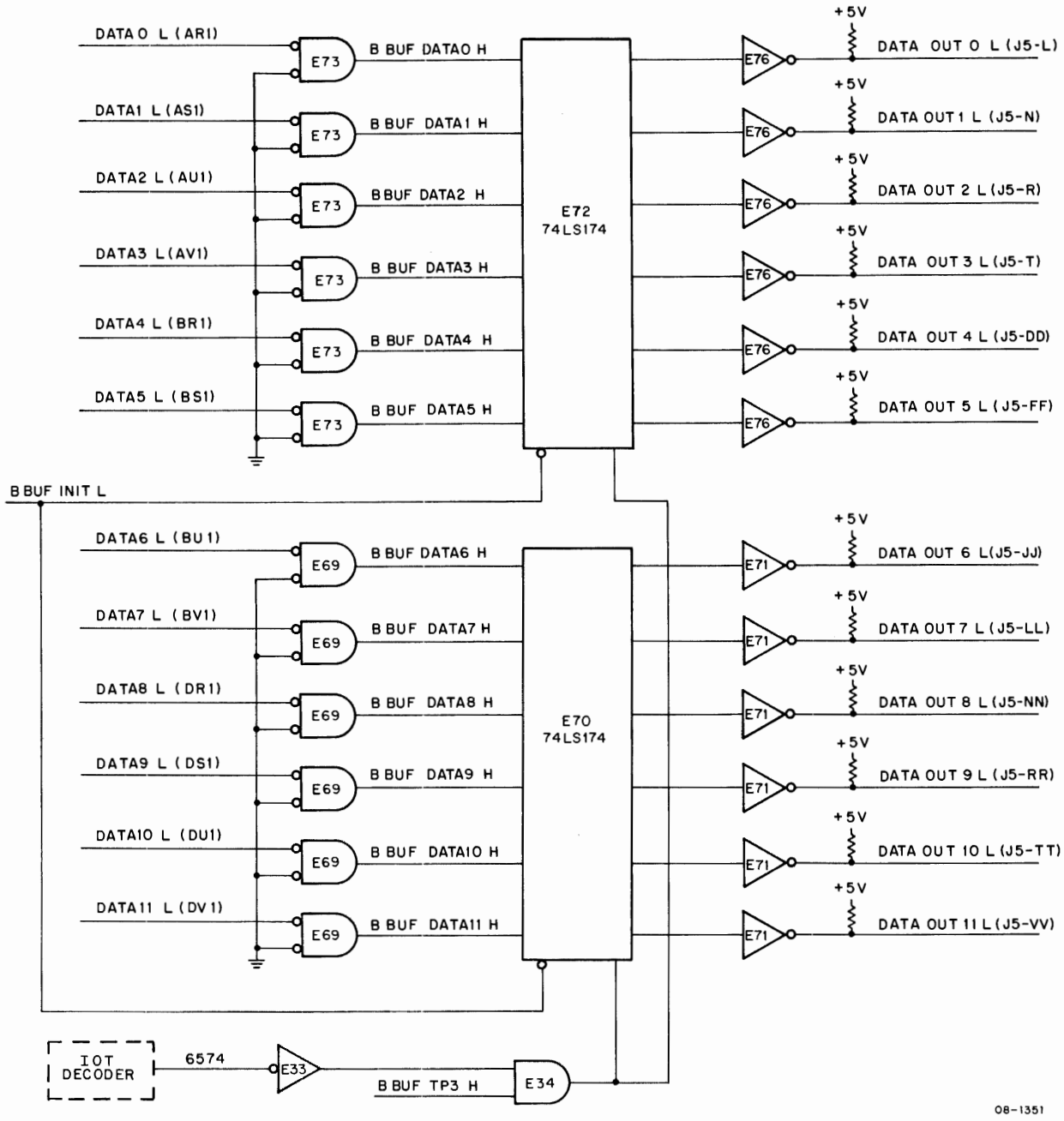


Figure 6-22 Parallel I/O Output Register

6.11.6 Parallel I/O Input Buffer and Data Gates

The information received from the device (Figure 6-23) is transferred to the AC via the Data Bus by the 6572 instruction. C0 L and C1 L (Figure 6-20) are asserted (low) to allow data to be transferred from the Data Bus to the AC.

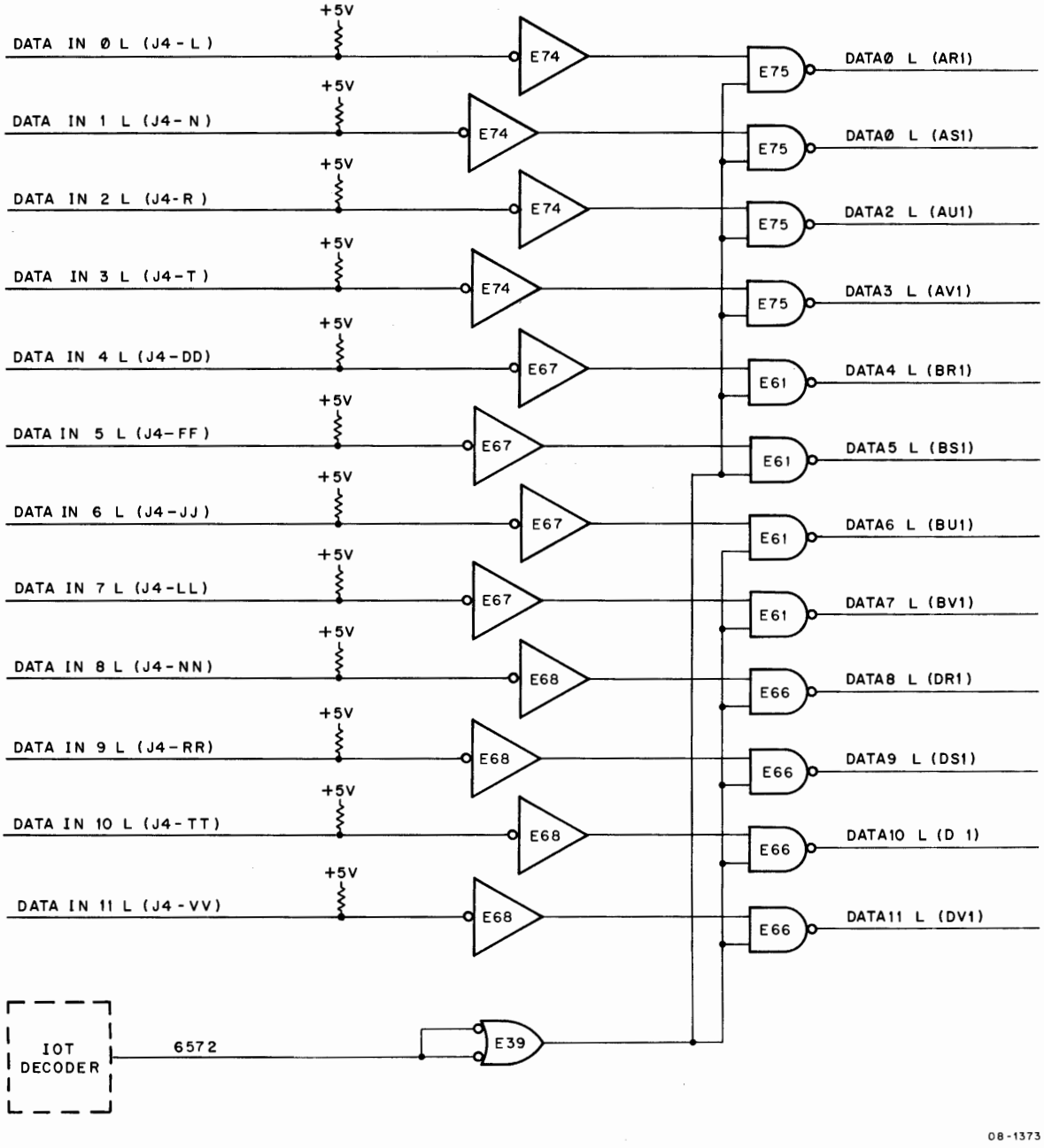


Figure 6-23 Parallel I/O Input Buffer and Data Gates

SECTION 2
KM8-A EXTENDED OPTION MODULE (M8317)

6.12 KM8-A EXTENDED OPTION BOARD (M8317)

The KM8-A extended option module (M8317) (Figure 6-24) is a hex size module which comprises four PDP-8/A options:

1. Memory Extension
2. Timeshare Control
3. Power Fail and Auto Restart
4. 128-Location Bootstrap Loader

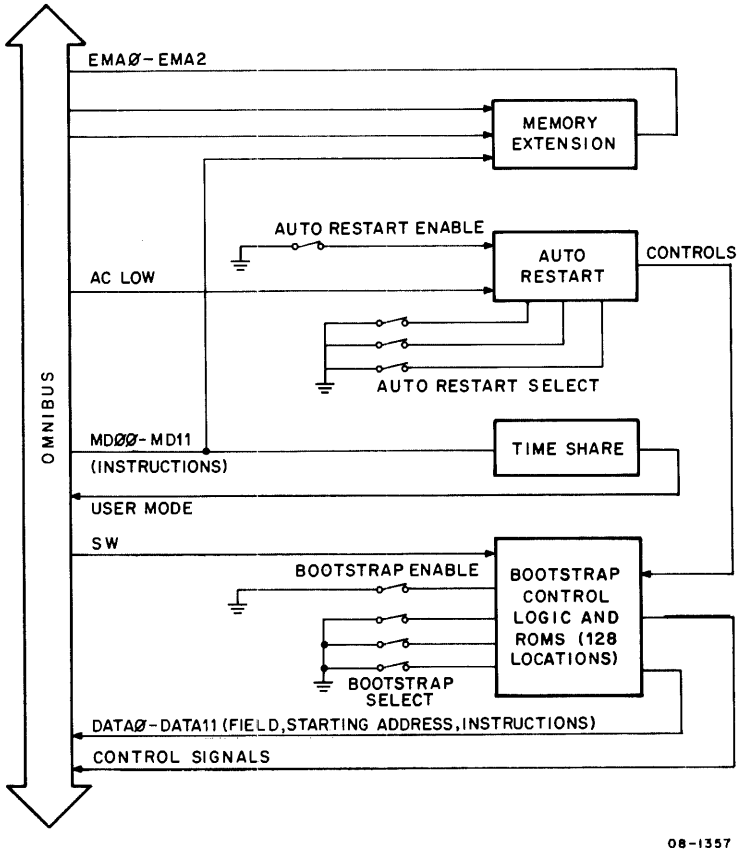


Figure 6-24 KM8-A Block Diagram

6.12.1 Memory Extension

The Memory Extension portion of the KM8-A extends the addressing capability of the PDP-8/A from 4096 words to 32,768 words.

6.12.2 Timeshare Option

The Timeshare portion of the KM8-A enables the PDP-8/A to operate in either the normal manner (Executive Mode) or User Mode. User Mode enables the computer to function in a timesharing environment, in which a user program is prevented from disturbing or interfering with another user program.

6.12.3 Power Fail/Auto Restart

The Power Fail/Auto Restart portion of the KM8-A interrupts the program when the power supply detects that the ac line voltage has fallen below a certain level (95 V ± 3% for 117 Vac operation). The power supply generates a signal AC LOW which causes the Power Fail/Auto Restart to interrupt the program as the AC is going away. The power supply negates the AC LOW signal when the AC line voltage rises above 105 V ± 3%.

6.12.4 Bootstrap Loader

The Bootstrap Loader portion of the KM8-A provides the logic to deposit into read/write memory one of several programs contained on two ROMS. These programs provide the necessary instructions to load programs from paper tape, disk, magnetic tape, etc, and to start the program at a specified location. Users may also purchase blank ROM chips and write their own programs in them.

6.13 MEMORY EXTENSION AND TIMESHARE DESCRIPTION

Memory Extension hardware is required when more than 4K of memory is to be addressed. Except for data break devices, the Memory Extension logic on the M8317 module is the only way to apply memory field addresses to the three Omnibus Extended Memory Address lines (EMA0-EMA2). Memory is divided into eight 4K fields – field 0(4K) to field 7(32K). Each 4K of memory receives and decodes the EMA0-EMA2 signals. This provides an addressing capability up to 32,768 memory locations. On systems with 4K or less of memory, EMA0-EMA2 are all high representing all zeros, and field 0 is the only field that can be addressed by the program. However data break devices supply their own field address bits and they can address fields 1 through 7 without installing the KM8-A option.

Timeshare hardware is required for all systems that use a timeshare system monitor. Timeshare may be enabled or disabled by a switch on the M8317 module.

6.14 MEMORY EXTENSION BLOCK DIAGRAM DESCRIPTION

The functional units that make the memory extension and timeshare option are explained in the following paragraphs (Figure 6-25). The flow diagram in the KM8-A print set in Appendix H should be referred to during this discussion.

6.14.1 Control Logic

The control logic for the memory extension and timeshare option consists of device selector logic, operation decoders, and the INT RQST and SKIP signal lines. IOT instructions for memory extension and timeshare must be executed by the program to start operation (Paragraph 6.15).

Data paths between the memory extension and time share option are via the DATA BUS. When the data field or instruction field are to be stored in memory, the data path is from the DATA BUS to the AC register. A DCA instruction is then used to store information in memory. The data paths between the memory extension/timeshare and the processor are via the MD lines (instructions) and DATA BUS (IF, DF, and USER MODE bits). When the program executes the CDF and CIF instructions the data field (CDF) and instruction field (IF) are carried on the MD lines.

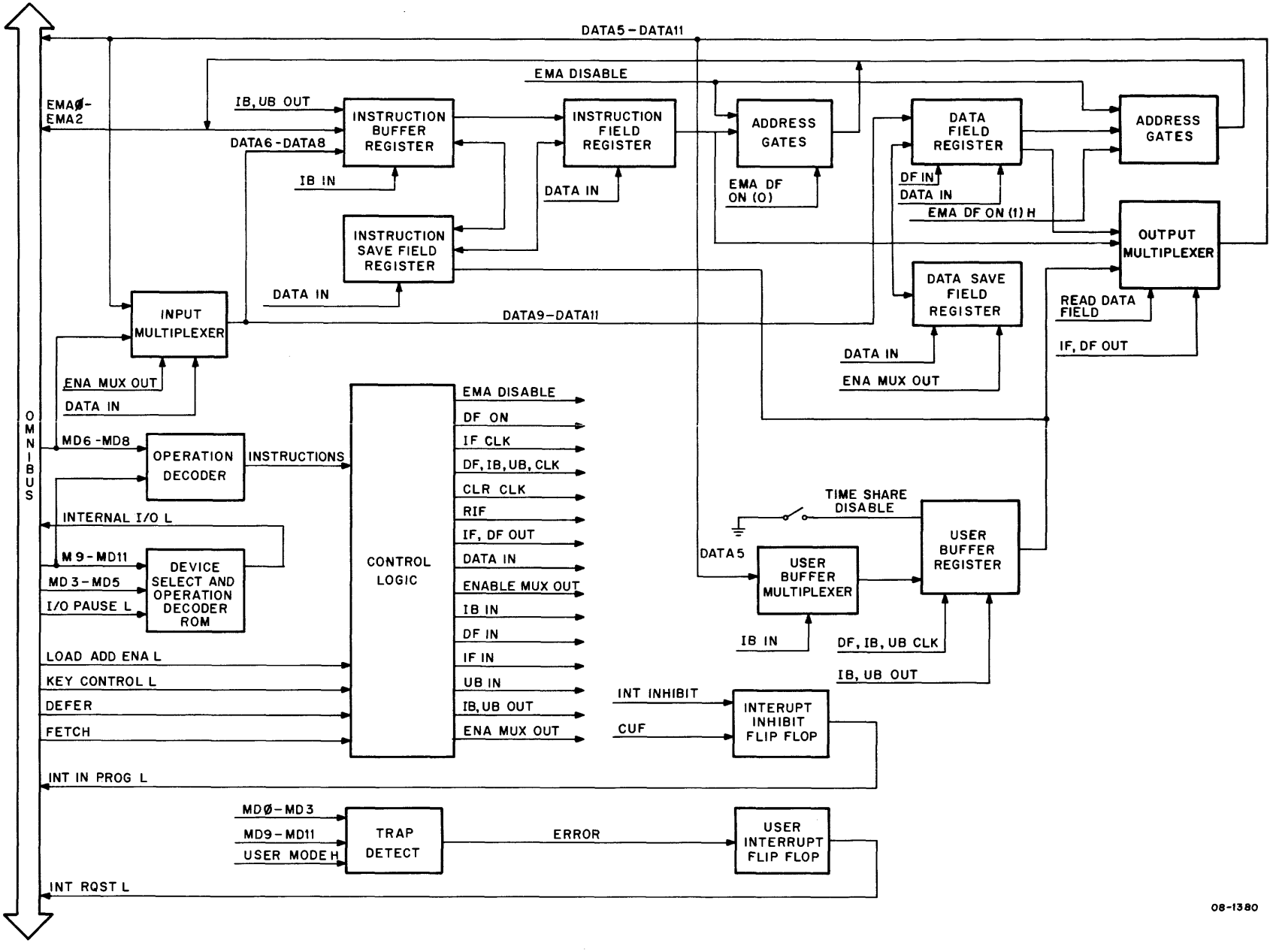


Figure 6-25 Memory Extension and Timeshare Block Diagram

6.14.2 Instruction Field Register (IF)

The IF is a three-bit register that is an extension of the PC. The contents of the IF determine the field from which all instructions are taken and the field from which operands are taken in directly-addressed Memory Reference Instructions. Pressing the console LXA switch transfers Entry Register bits 6 through 8 into the IF register. During a JMP or JMS instruction, the IF is set by a transfer of information from the Instruction Buffer register. If the instruction is a JMP, the IF is updated at the conclusion of the instruction. If the instruction is a JMS, the IF is updated just before the execute portion of the instruction saving the return address in the new field. When a program interrupt occurs, the contents of the IF is automatically stored in bits 0 through 2 of the Save Field register for restoration to the IF from the instruction buffer register at the conclusion of the program interrupt subroutine.

6.14.3 Data Field Register (DF)

This three-bit register determines the memory field from which operands are taken in indirectly-addressed Memory Reference Instructions. Pressing the console LXA switch transfers the Entry register bits 9 through 11 into the DF register. During a CDF instruction, the DF register is loaded from MD6-MD8 to establish a new data field. When a program interrupt occurs, the contents of the DF are automatically stored in bits 3-5 of the Save Field register. The DF is set by a transfer of information from Save Field register bits 3 through 5 by the RMF instruction. This action is required to restore the Data Field at the conclusion of the program interrupt subroutine.

6.14.4 Instruction Buffer Register (IB)

The IB is a three-bit input buffer for the Instruction Field register. All field number transfers into the Instruction Field register, except transfers from the operator's console switches, are made through the Instruction Buffer. The IB is set by pressing the console LXA switch in the same manner as the Instruction Field register. A CIF microinstruction loads the IB with the programmed field. An RMF microinstruction transfers Save Field register bits 0 through 2 into the IB to restore the instruction field that existed before a program interrupt.

6.14.5 Save Field Register (SF)

When a program interrupt occurs, this seven-bit register is loaded from the USER FIELD flip-flop, and the IF and DF registers. The SF register is loaded during the cycle in which the program count is stored at address 0000 of the JMS instruction forced by a program interrupt request, then the Instruction Field, Instruction Buffer, and Data Field registers are cleared. An RMF instruction can be given immediately before exit from the program interrupt subroutine to restore the Instruction Field and Data Field by transferring the SF into the IB and the DF registers. (Also, see GTF and RTF instructions.)

6.15 TIMESHARE CONTROL BLOCK DIAGRAM DESCRIPTION

The timeshare portion of the KM8-A module (Figure 6-25) operates in two modes defined by the USER Flag (UF) flip-flop in the User Buffer. When the UF flip-flop is in the logic 1 state, operation is in the User Mode and user program is running. When the UF flip-flop is in the logic 0 state, operation is in the Executive Mode and the timesharing system's monitor is in control of the central processor. Four instructions (CINT, SINT, CUF, and SUF) are used by the timesharing system's monitor in the executive mode and are never used by a user program. If a user program attempted to use one of these instructions, execution of the instruction would be blocked (see next paragraph). The timeshare option adds the necessary hardware to the PDP-8/A to implement these instructions.

In Executive Mode, the computer operates normally. When the computer is operated in User Mode, operation is normal except for IOT, HLT, LAS, and OSR instructions. When one of these instructions is encountered, the trap detect logic inhibits the normal instruction sequence (other than rewriting the instruction in memory), and generates an interrupt at the end of the current memory cycle. Any interrupt returns timeshare control to Executive Mode. The timesharing system's monitor program then analyzes the source of interrupt and takes appropriate action.

The timeshare option requires at least 8K of memory. A switch on the KM8-A module is used to enable the timeshare function.

6.16 MEMORY EXTENSION AND TIMESHARE PROGRAMMING

6.16.1 Memory Extension Programming

Instructions associated with the extended memory portion of the KM8-A option are as follows:

Mnemonic	Octal Code	Function
GTF	6004	Loads the contents of the SF register into AC5–11. Other AC bits are loaded with information from the CPU, i.e., link, interrupt bus, interrupt on.
RTF	6005	Loads the USER BUFFER flip-flop, the Instruction Buffer register, and the Data Field register with the contents of AC bits 5, 6–8, and inhibits processor interrupts until the next JMP or JMS instruction. At the conclusion of the JMP or JMS instruction, the contents of the USER BUFFER flip-flop and the Instruction Buffer register are transferred into the USER FIELD flip-flop and the Instruction Field register, respectively. AC0 is loaded into the Link. The INTERRUPT ON flip-flop in the CPU is unconditionally set by this instruction. AC5 0 — Clears User Flag AC6–AC8 — Instruction Field (0–7) AC9–AC11 — Data Field (0–7)
CDF	62N1	Loads the Data Field register with the program-selected field number N (N = 0 to 7). All subsequent memory requests for indirect operands are automatically switched to that Data Field.
CIF	62N2	Loads the Instruction Buffer register with the program-selected field number N (N = 0 to 7) and inhibits processor interrupts until the next JMP or JMS instruction. At the conclusion of a JMP instruction or at the beginning of the execute portion of a JMS instruction, the contents of the Instruction Buffer register is transferred into the Instruction Field register.
CDF CIF	62N3	Performs the combination of CDF and CIF operations.
RDF	6214	ORs the contents of the Data Field register into bits 6–8 of the AC. All other bits of the AC are unaffected.
RIF	6224	ORs the contents of the Instruction Field register into bits 6–8 of the AC. All other bits of the AC are unaffected.
RIB	6234	Inclusively ORs the contents of the Save Field register (which is loaded from the Instruction and Data Field during a program interrupt) into bits 6–8 and 9–11 of the AC, respectively. Thus, AC 6–11 contains the Instruction and Data Fields that were in use before the last program interrupt. AC 5 is loaded by the timeshare bit of the Save Field register. All other bits of the AC are unaffected.
RMF	6244	Restores the contents of the Save Field register (which is loaded from the Instruction and Data Field during a program interrupt) into the Instruction Buffer, the Data Field register, and the User Buffer (if timeshare option is enabled). This command is used upon exit from the program interrupt subroutine.

Instructions and data are accessed from the currently assigned instruction and data fields, which may be in the same or different memory fields. When indirect memory references are executed, the operand address refers first to the instruction field to obtain an effective address, which, in turn, refers to a location in the currently assigned data field. All instructions and operands are obtained from the field designated by the contents of the Instruction Field register, except indirectly-addressed operands, which are specified by the contents of the Data Field register. In other words, the DF is effective only in the EXECUTE cycle that directly follows the Defer cycle of a memory reference instruction as follows:

Indirect (Bit 3)	Page Bit (Bit 4)	Field In IF	Field In DF	Effective Address
0	0	m	n	The operand is in page 0 of field m at the address specified by bits 5 through 11.
0	1	m	n	The operand is in the current page of field m at the page address specified by bits 5 through 11 of the instruction.
1	0	m	n	The absolute address of the operand in field n is taken from the contents of field m. Page 0 at the page address specified by bits 5 through 11 of the instruction.
1	1	m	n	The absolute address of the operand in field n is taken from the contents of field m current page, at the page address specified by bits 5 through 11 of the instruction.

Each field of extended memory contains eight auto-index registers in addresses 10(8) through 17(8). For example, assume that a program in field 2 is running (IF = 2) and using operands in field 1 (DF = 1) when the instruction TAD I 10 is fetched. The Defer cycle is entered (bit 3 = 1), and the contents of location 10 in field 2 are read, incremented, and rewritten. If address 10 in field 2 originally contained 4321, it now contains 4322. In the execute cycle, the operand is fetched from location 4322 of field 1. Program control is transferred between memory fields by the CIF instruction. The instruction does not change the instruction field directly, because this would make it impossible to execute the next sequential instruction; instead, it loads the new instruction field in the IB for automatic transfer into the IF when either a JMP or JMS instruction is executed. The DF is unaffected by the JMP and JMS instructions.

The 12-bit program counter is set in the normal manner and, because the IF is an extension on the most significant end of the PC, the program sequence resumes in the new memory field following a JMP or JMS. Interrupts are inhibited after the CIF instruction until a JMP or JMS is executed.

NOTE

The IF is not incremented if the PC goes from 7777 to 0000. This feature protects the user from accidently entering a nonexistent field.

To call a subroutine that is out of the current field, the data field register is set to indicate the field of the calling JMS, which establishes the location of the operands as well as the identity of the return field. The instruction field is set to the field of the starting address of the subroutine.

When a program interrupt occurs, the current instruction and data field numbers are automatically stored in the 7-bit Save Field register; then the IF, IB, and DF, are cleared. The PC content is stored in location 0000 of field 0 and program control advances to location 0001 of field 0. At the end of the program interrupt subroutine, the RMF instruction restores the IF, IB, and DF from the contents of the SF. Alternatively, the GTF and RTF instructions may be used to handle the save field and link information.

6.16.2 Timeshare Programming

The instructions associated with the time share option are as follows:

Mnemonic	Octal Code	Function
CINT	6204	Clears the USER INTERRUPT flip-flop.
SINT	6254	When the USER INTERRUPT flip-flop is set the next sequential instruction is skipped.
CUF	6264	Clears the USER BUFFER flip-flop.
SUF	6274	Sets USER BUFFER flip-flop and inhibits processor interrupts until the next JMP or JMS instruction. At the conclusion of either of these instructions, the content of the USER BUFFER flip-flop is transferred into the USER FLAG flip-flop.

NOTE

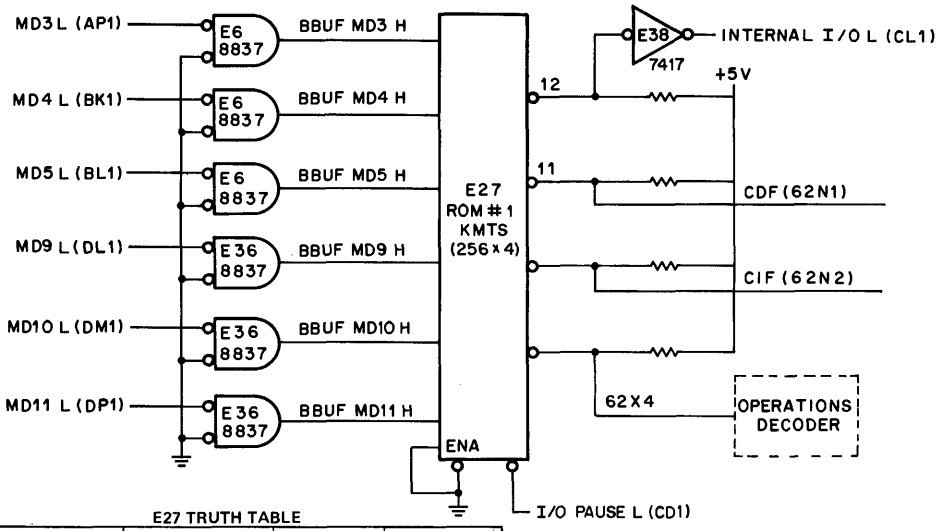
If the machine is stopped while in User mode, the user flag (UF) may only be cleared by negating POWER OK.

6.17 MEMORY EXTENSION AND TIMESHARE DETAILED LOGIC DESCRIPTION

The memory extension and timeshare block diagram in Figure 6-25 should be used to understand the interaction and signal flow between functional groups of logic. The logic can be considered to be divided into four groups: the control (located on the bottom left portion of the block diagram), the Instruction Field register (IF), the Data Field register (DF), and the Timeshare control logic. The only interface is the Omnibus. All signals entering and leaving the system, therefore, are directed to the Omnibus. Data is transferred between the processor and the KM8-A option via the Data Bus and between memory and the KM8-A via the MD lines. Data is transferred via the Data Bus to the console indicators during TS1 to tell the operator which instruction fields and data fields are being addressed by the program. When the data field and/or instruction field are to be stored in memory, the data path is from the Data Bus to the AC register. A DCA instruction is then used to store the information in memory.

6.17.1 Memory Extension/Timeshare Device Select

The device select logic for the memory extension and timeshare option is shown in Figure 6-26. ROM No. 1 (E27) is the device select decoder for the memory extension and timeshare options. The address bits MD3-MD5 and MD9-MD11 are enabled by I/O PAUSE L to select one of the ROM memory locations. INTERNAL I/O L is asserted anytime a 62XX instruction is decoded to direct the Positive I/O to ignore this IOT instruction (see E27 Truth Table in Figure 6-26).ROM No. 1 also decodes the CIF (62N1) and CDF (62N2) instructions to generate the necessary control signals for the execution of these instructions. The 62X4 output enables the operation decoder discussed in the next paragraph. The ROM pattern generated by this ROM is listed in the printset in Appendix H.



E27 TRUTH TABLE

OCTAL CODE	SIGNAL	PIN NUMBER	ASSERTED LEVEL
62N1	CDF	11	LOW
62N2	CIF	10	LOW
62N3	CDF,CIF	11 AND 10	LOW
62X4	62X4	9	LOW
62N1 + 62N2 + 62N3 + 62X4	INTERNAL I/O L	12	LOW

08-1356

Figure 6-26 Memory Extension and Timeshare Device Select Logic

6.17.2 Memory Extension and Timeshare Operation Decoder

The operation decoders are shown in Figure 6-27. There are two operations decoder: one for the 62X4 instructions and one for the 600X instructions.

E39, the operation decoder for the 62X4 instructions, is enabled by 62X4 for the device select logic. The operation decoder is a BCD to decimal decoder which decodes MD6-MD8 to generate the necessary control signals for the execution of these instructions. As an example, if the SUF (6274) instruction is executed by the program and MD6, MD7, and MD8 are all ones, pin 9 is asserted low to allow the execution of the SUF instruction. All other pins would be high.

C1 L is asserted by the RIB, RIF, and RDF instructions to allow data transfers from the Data Bus to the AC register.

MD3-MD8 are enabled by I/O PAUSE at E37 to enable the decoding of MD9-MD11 when an 600X instruction is executed by the program. The output of E37 enables E33 and E60 to decode MD9-MD11 and generate signals RTF and GTF.

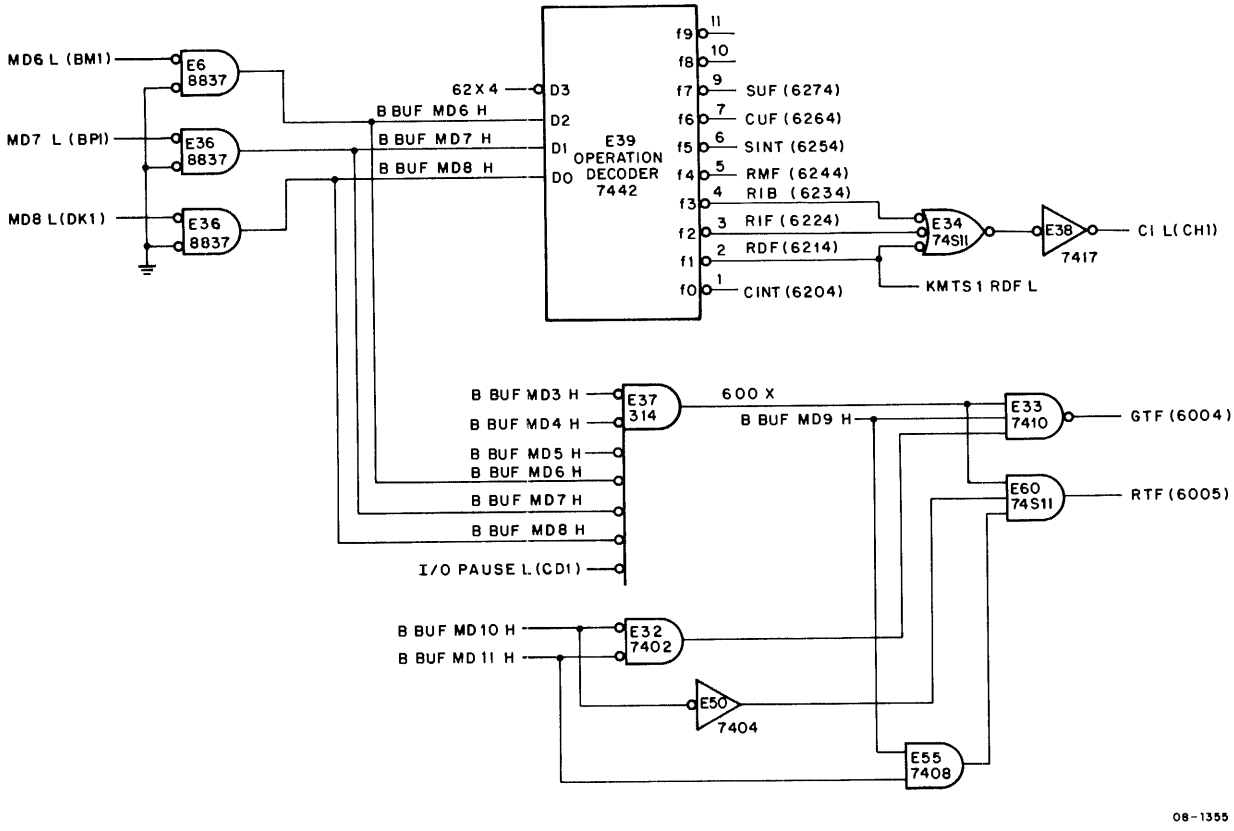


Figure 6-27 Memory Extension/Time Share Operation Decoder

6.17.3 Input Multiplexer

The Input Multiplexer shown in Figure 6-28 receives data from the Memory Data lines (MD6-MD8) and the Data Bus (DATA5-DATA11) and supplies an input to the UB, IF, and DF registers as follows:

RTF Instruction	DATA5 to UB register DATA6-DATA8 to IF register DATA9-DATA11 to DF register
CIF (62N1) Instruction	MD6-MD8 to IF register
CDF (62N2) Instruction	MD6-MD8 to DF register
CDF,CIF (62N3) Instruction	MD6-MD8 to IF and DF registers
	DATA6-DATA11 to IF and DF register when the LXA switch on the Programmer's Console is pressed. This asserts LOAD ADD EN L and KEY CONTROL L which enables E53.

The Multiplexers are 74S257 ICs with Tristate outputs which select one of the inputs (DATA5-DATA11 or MD6-MD8) as output to UB, IF, and DF registers. A low on the select input selects DATA5-DATA11 and a high selects MD6-MD8. ENA OUT must be low to enable either output to be used.

6.17.4 Instruction Field Register and Controls

The control logic associated with the IF register (Figure 6-29) controls data flow and provides the necessary gating and control signals to enable gating, clocking, loading, etc., of the IF, IB, UB, and IF Save Field registers. This logic loads either MD6-MD8 or DATA5-DATA8 (depending on the instruction) into the IB and UB registers for transfer to the IF register. If the RTF instruction is executed, the IB and UB registers are loaded from the Data Bus and interrupts are inhibited until the JMP or JMS instruction is executed. At the conclusion of the JMP or JMS instruction, the content of the IB and UB register is transferred to the IF register. If the CIF or CDF instructions are used MD6-MD8 are loaded into the IB register and transferred to the IF register at the conclusion of a JMP instruction or at the beginning of the execute cycle of a JMS instruction.

The IF in the Entry register on the Programmer's Console is transferred to the IB register via the Data Bus when LXA is pressed. This operation is enabled in the IF register control logic by LOAD ADD EN L and KEY CONTROL L which enables NAND gate E53. This operation loads the IB register, enables the IF Multiplexer, and loads the IF register. PULSE LA L clocks the data into the register.

The content of the IF register is transferred to the Save IF register at TP4 if BBUF INT IN PROG H is asserted high. This occurs anytime an interrupt occurs. Note that the CLR input of the IF register is clocked at the same time to clear the IF register. It is also cleared during power up when BBUF $\overline{\text{POWER OK}}$ H goes high.

To transfer the content of the Save IF register back to the IF register, the program must execute the RMF instruction at the conclusion of the interrupt service routine.

The RMF instruction enables the output of the Save IF register to the IB and UB register and it is clocked into the IB and UB register by BBUF TP3 H. The transfer from the IB and UB to the IF is made at the end of a JMP instruction or at the beginning of the execute cycle of a JMS instruction.

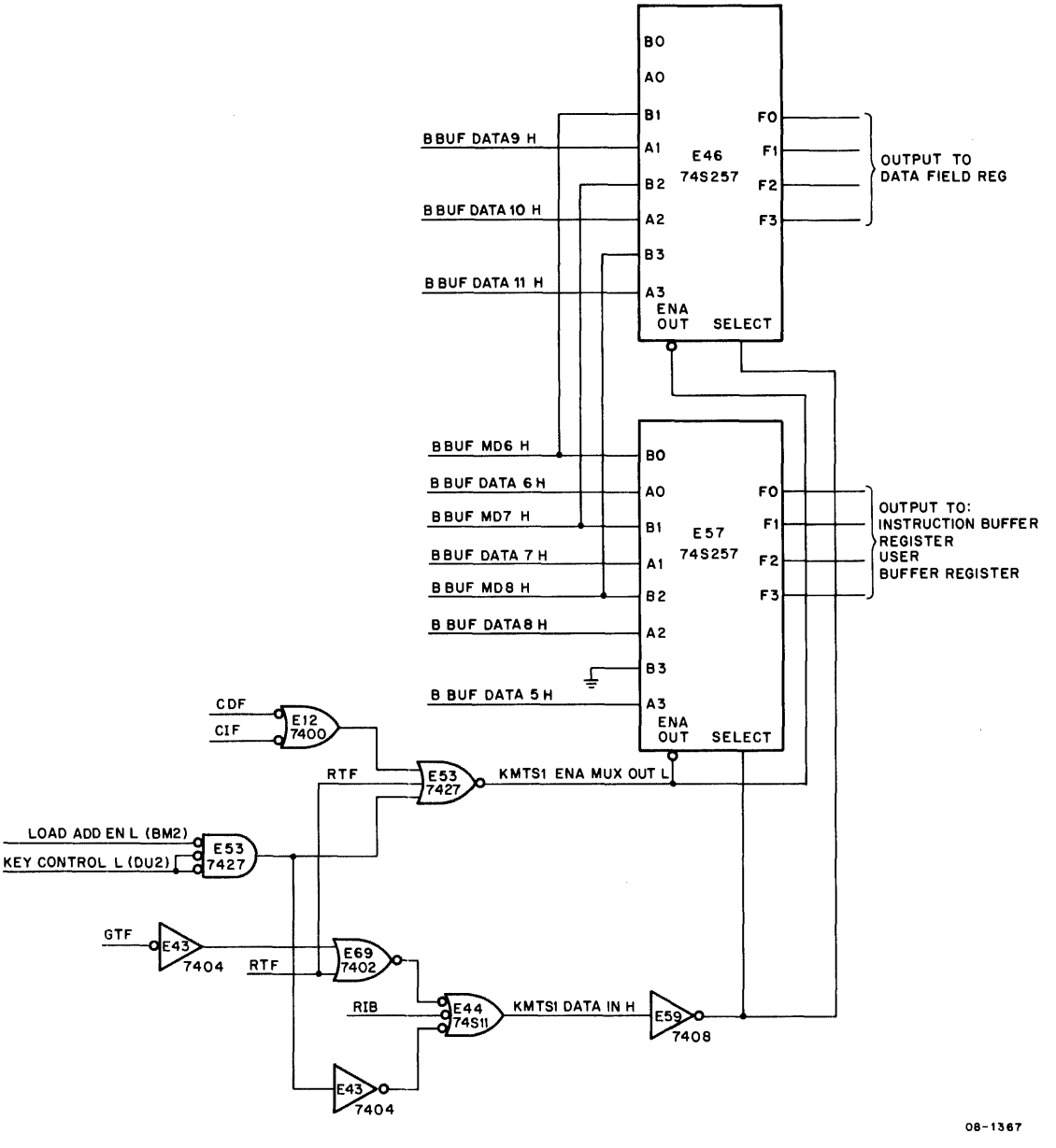


Figure 6-28 Input Multiplexer

The content of the IF register may be read into the AC for storage in memory by the RTF or RIF instruction. These instructions enable the IF multiplexer and the content of the IF register is applied to the output multiplexer (Paragraph 6.17.6) for transfer to the AC via the Data Bus.

The output of the IF register is enabled to the EMA lines (Figure 6-30) when DF ON and EMA DISABLE are both cleared. DF ON is set only in the Execute cycle that directly follows the Defer cycle of a memory reference instruction. EMA DISABLE is set only during a break cycle by CPMA DISA L and cleared by TP4 at the end of the break cycle. The break device supplies its own extended memory address during break cycles.

USER MODE H is asserted (low) when the User Flag in the IF register is set to a one. The user flag is set only when the computer operates as a timesharing system (see Paragraph 6.16.7).

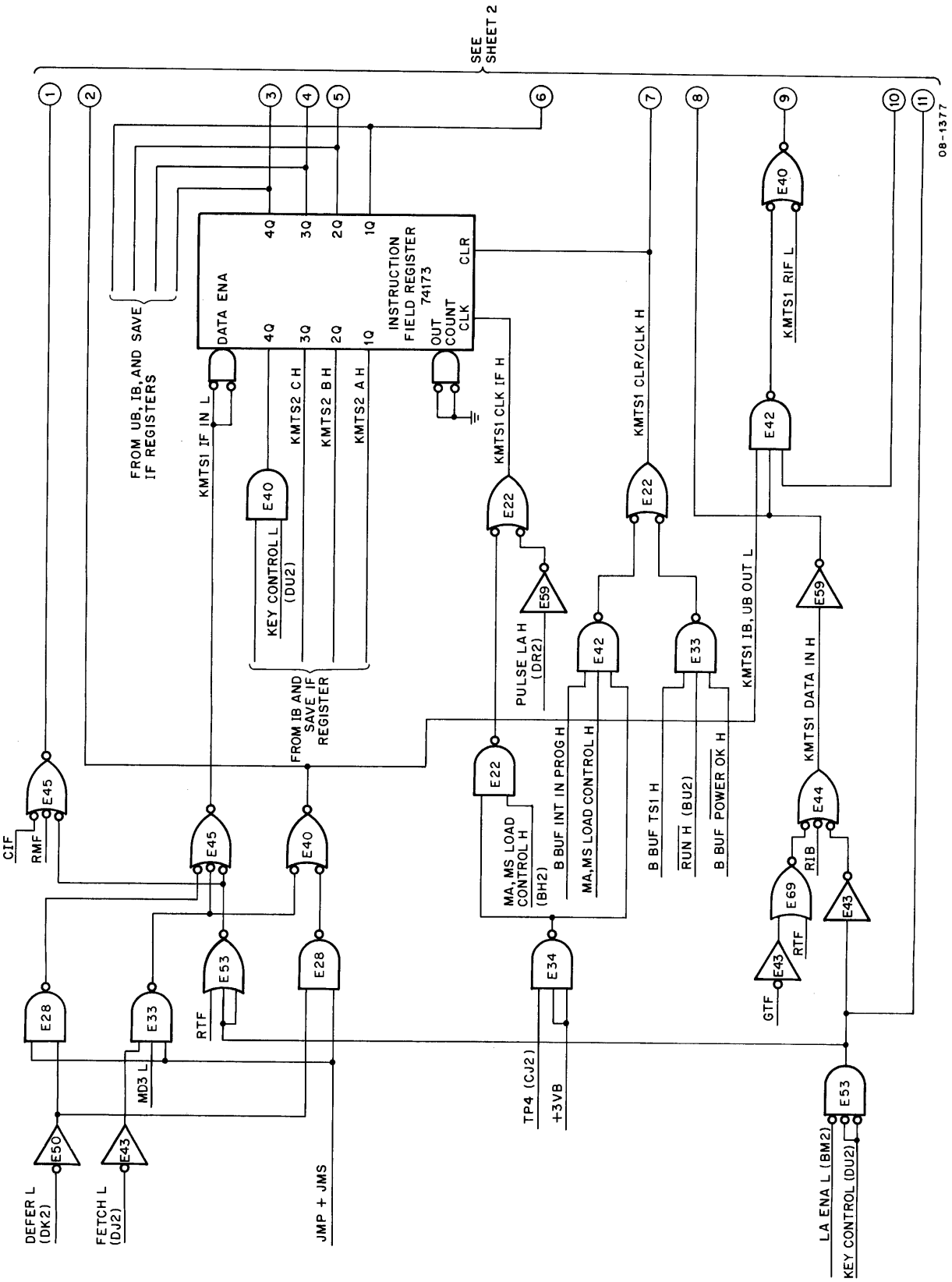


Figure 6-29 IF Register and Control Logic (Sheet 1 of 2)

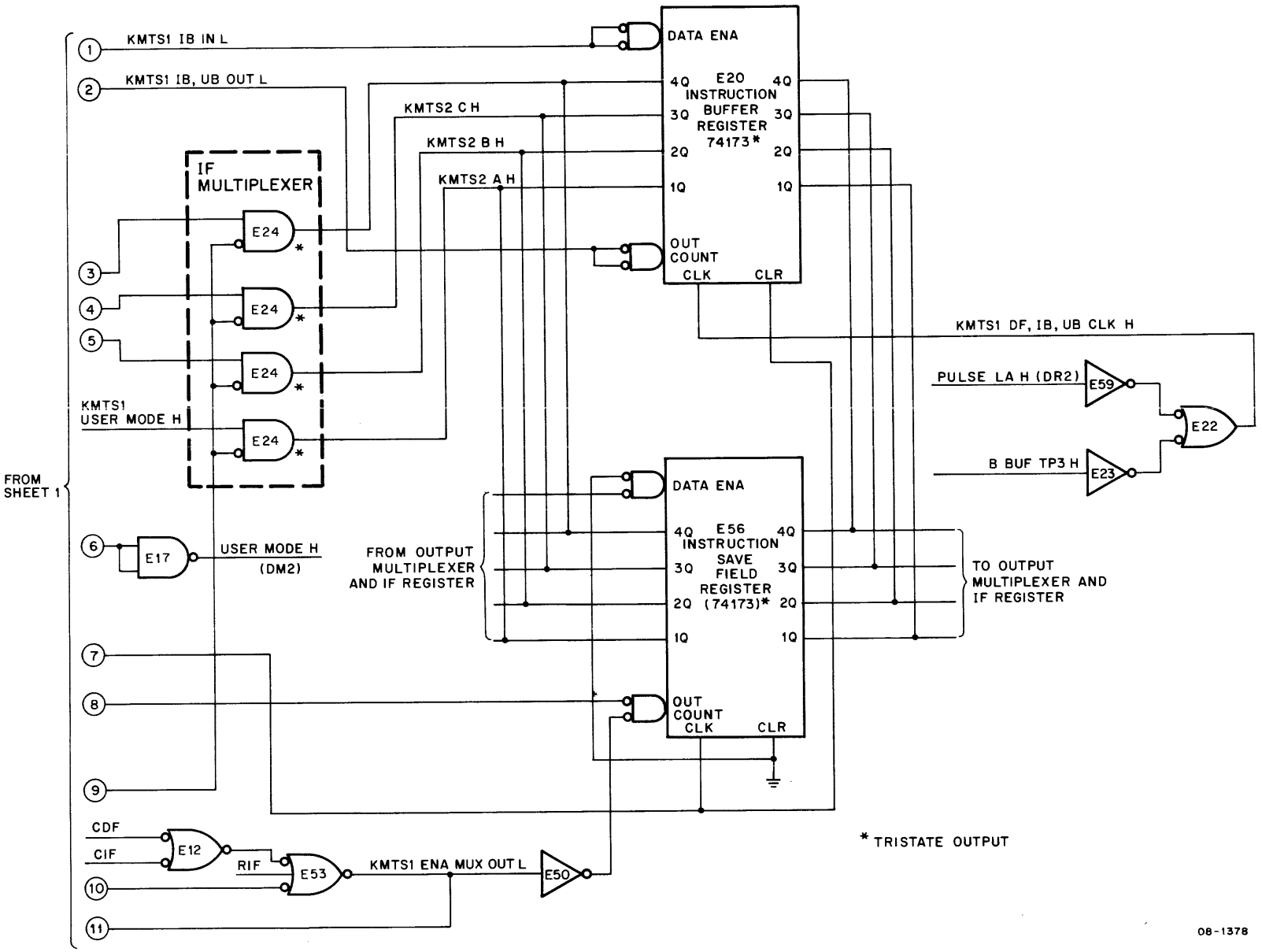


Figure 6-29 IF Register and Control Logic (Sheet 2 of 2)

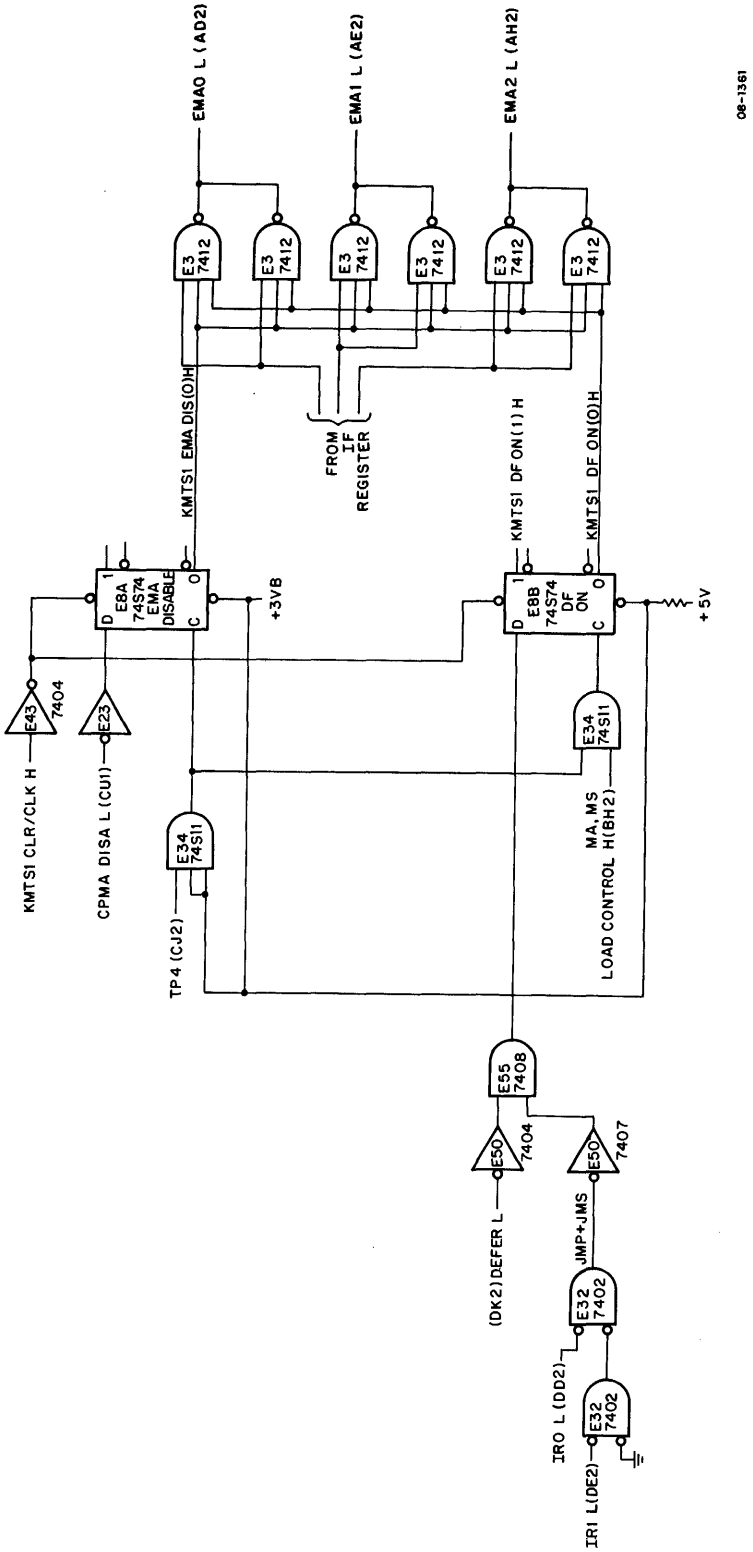


Figure 6-30 IF and DF Field Address Enable Logic

The IB, IF, and IF Save Field registers are 74173 ICs. Data is enabled into these registers by the two DATA ENA inputs and a low to high transition on the CLK input. Data is enabled out of these registers by two low inputs to DATA CONT. The registers are cleared by applying a high signal to the CLR input.

6.17.5 Data Field Register and Controls

The Data Field (DF) register (Figure 6-31) receives data from 3 sources:

1. The MD lines when the CDF or CDF, CIF instructions are executed,
2. The Data Bus when the RTF instruction is performed or LXA on the Programmer's Console is pressed,
3. The DF Save register when the IF and DF are restored at the end of a routine to service an interrupt. The content of the DF register is transferred to the DF Save register when an interrupt occurs.

When the RTF instruction is executed by the program, the DF register is loaded from the AC via the DATA BUS and the Input Multiplexer (Figure 6-28) and clocked into the DF register by BBUF TP3 H. When the CDF, CDF, or CIF instructions are used to load the DF register, it is loaded from MD6-MD8 via the input multiplexer. Data is enabled into the register by the CDF instruction and clocked into the register by BBUF TP3 H.

When LXA on the Programmer's Console is pressed, LA ENABLE L and KEY CONTROL L (E53) enables the Entry register data from the Data Bus via the input multiplexer to load the DF register. The input is clocked in by PULSE LA H.

The content of the DF register is transferred to the DF Save register anytime an interrupt request is made by a system device. When an interrupt request is made, BBUF INT IN PROG H is asserted (high), which clocks the content of the DF field register into the DF Save register. The DATA EN inputs are grounded on the DF Save register so it needs only a clock pulse to load the register.

The content of DF Save register is transferred back to the DF register by the RMF instruction which is executed at the end of an interrupt service routine.

The content of the DF register is enabled out to the EMA lines by KMTS1 DF ON(1) H during Execute cycles that directly follow a Defer cycle of a memory reference instruction (Figure 6-30). The other enabling signal KMTS1 EMA DIS(0) H, is always high except during data break cycles when the EMA DIS flip-flop (Figure 6-30) is set by CPMA DISABLE L.

6.17.6 Output Multiplexer

The Output Multiplexer (Figure 6-32) consists of two 8234 ICs which enable the output of the UB, IF, and DF registers to the Data Bus when instructions are executed to transfer their content to the AC. IND1 L and IND2 L enable the content of the IF, DF, and UB registers to be applied to the Data Bus during TS1 to display the IF, DF, and UB in the Status register (Figure 1-5).

6.17.7 Timeshare User Buffer Register and Control Logic

The User Buffer register is used only when the timesharing portion of the KM8-A is implemented (Figure 6-33). Timeshare is enabled by turning S2-1 on the KM8-A module off.

The User flag is set if DATA5 is a one or cleared if DATA5 is a zero when the RTF instruction is executed.

When the SUF instruction is executed, the User flag is set by MD8 as a one and it is cleared when the CUF instruction is executed by MD8 as a zero.

The state of the User flag is transferred to the IF registers at the same time and in the same way as the content of the IB register is transferred to the IF register (Paragraph 6.17.4).

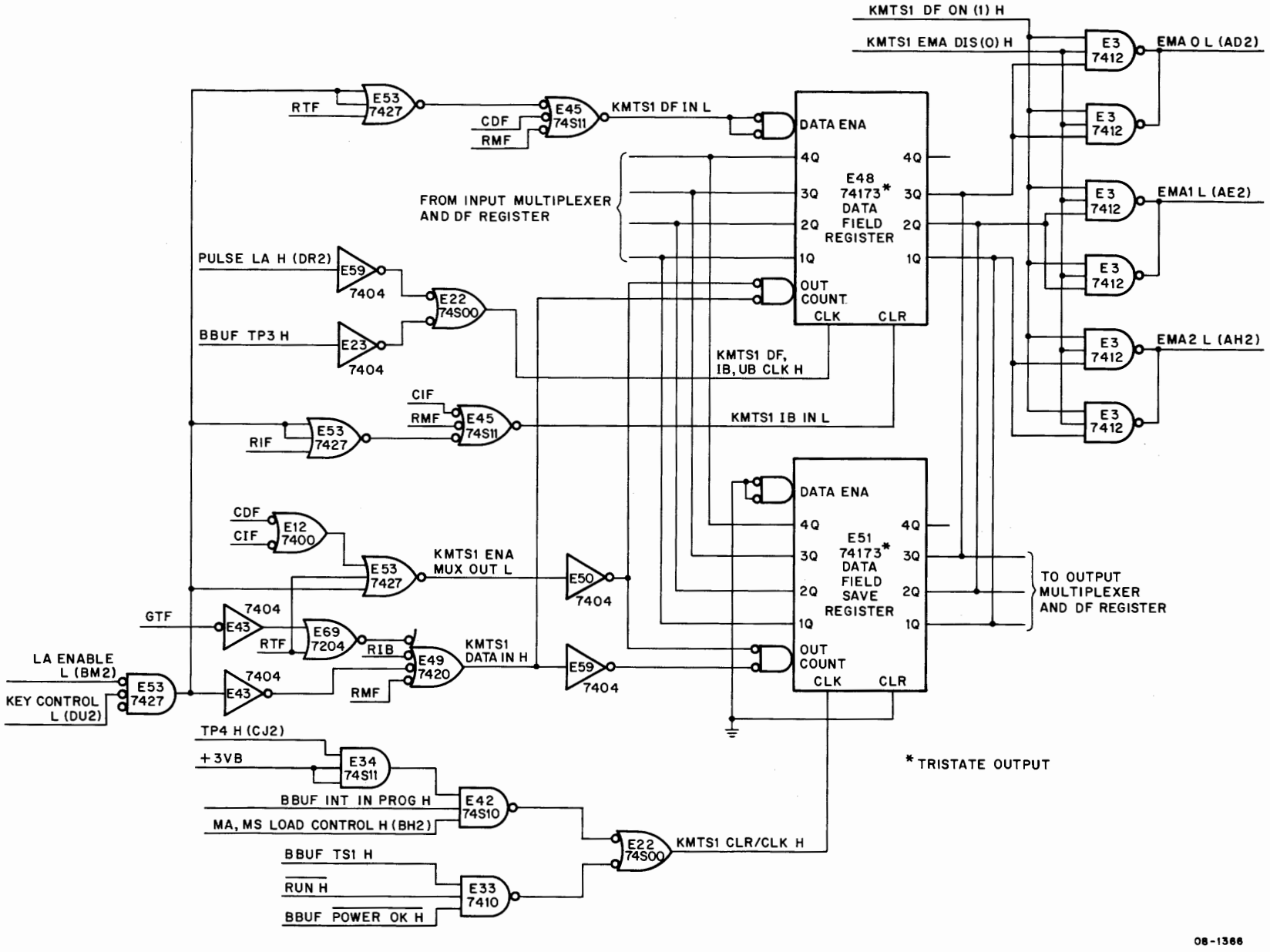


Figure 6-31 Data Field Register and Control Logic

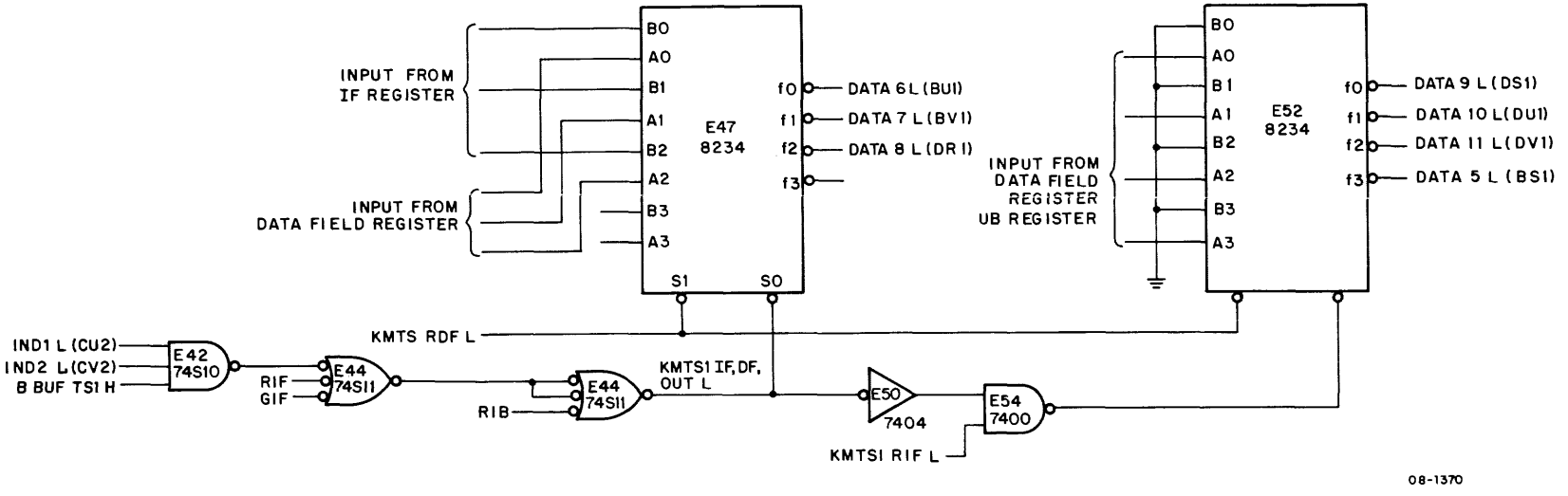


Figure 6-32 Output Multiplexer

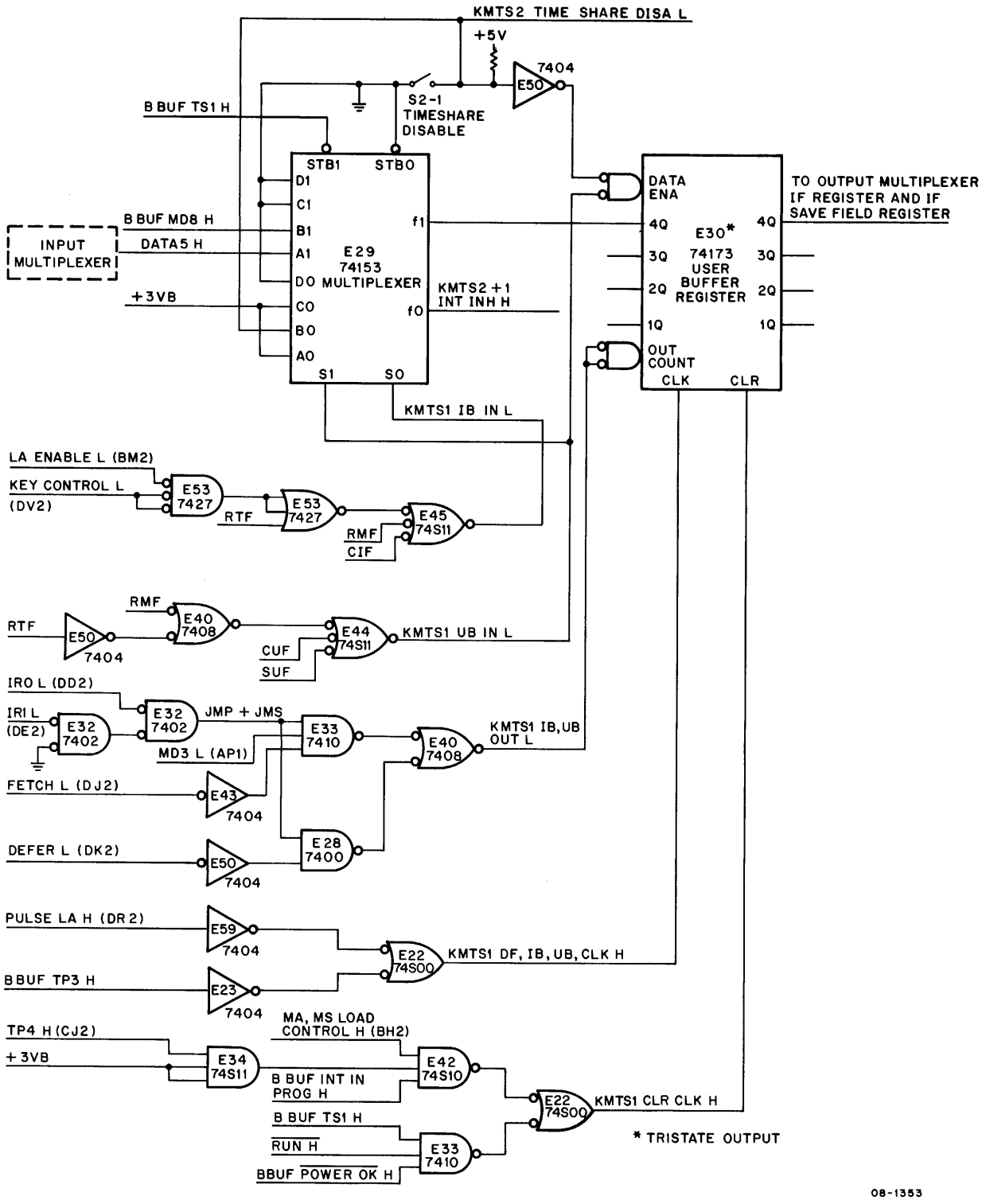


Figure 6-33 Time Share User Buffer Register and Control

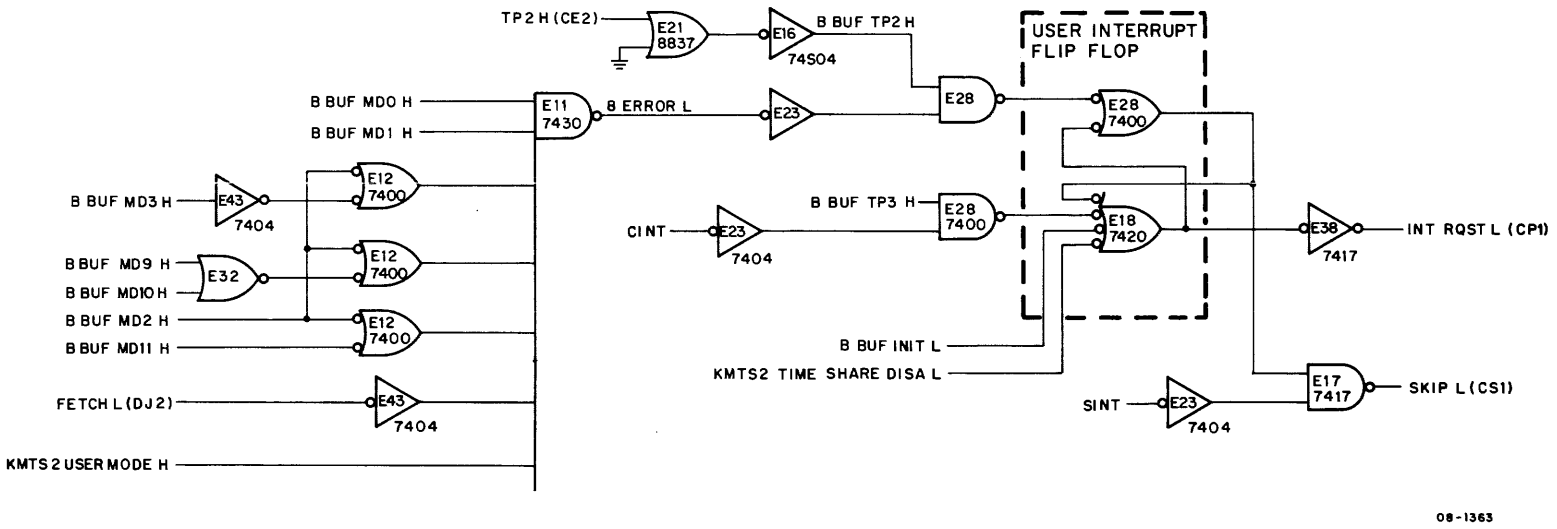


Figure 6-34 Trap Detect Logic

6.17.8 Trap Detect Logic

The purpose of the trap detect logic in Figure 6-34 is to generate an INT RQST if an IOT, HLT, LAS, or OSR instruction is executed by a user program while the computer is in the User Mode. NAND gate E11 is enabled by KMTS2 USER MODE H when S2-1 on is set to off. TP2 H is used to enable the input to INTERRUPT flip-flop so that an INT RQST will not be made until the completion of the current memory cycle. Any interrupt returns the computer to Executive Mode and the timesharing system monitor must determine what to do about the interrupt.

The SINT instruction asserts SKIP L if the USER INTERRUPT flip-flop is set. This instruction is used for flag checking routines.

The CINT instruction clears the USER INTERRUPT flip-flop.

6.17.9 Interrupt Inhibit Logic

The Interrupt Inhibit flip-flop in Figure 6-35 is set by KMTS2+1 INT INH H, which is asserted (high) if a CIF, CUF, SUF, RMF, or RTF instruction is executed by the program and S2-1 is off (see Figure 6-33). S2-1 is set to off to enable the Timeshare Mode. When the INTERRUPT INHIBIT flip-flop sets, INT IN PROG L is asserted (low) and the interrupt system is turned off. Interrupt Inhibit is cleared when a JMP or JMS instruction is executed at the end of an interrupt service routine. Also at this time the IF and DF registers are restored from the Save Field registers or loaded with a new field.

6.18 POWER FAIL/AUTO RESTART AND BOOTSTRAP LOADER

The Power Fail/Auto Restart and Bootstrap options are discussed in the following paragraphs.

6.18.1 Power Fail/Auto Restart Block Diagram Description

The power supply monitors the ac line voltage and detects when the ac line voltage has fallen below a certain level, (95 V ±3% for 117 Vac operation), and generates a logic signal AC LOW. This signal causes logic in the Power Fail/Auto Restart portion of the KM8-A extended option board to interrupt the program, which takes the necessary action as the ac power is going away (Figure 6-35). In MOS memory systems, the automatic switch-over to a battery supply that allows the system to continue operation for an additional 45 seconds minimum, will occur. If power is restored during this time, the system will automatically switch back to the regular power supply. In core memory systems, the program should store all active registers (AC, MQ, etc.) and stop the system when a low ac voltage is detected. The computer will restart and the program can restore the active registers when ac power goes above 105 Vac (117 Vac operation.)

Features

Restart Address:	One of four restart addresses may be selected, one at a time (4200, 2000, 0200, or 0000).
Auto Restart:	If Auto Restart is enabled, the PDP-8/A starts automatically when power is applied. This allows the user to apply power remotely and start the system without going to the PDP-8/A. (Auto-Start on the CPU must be disabled.)

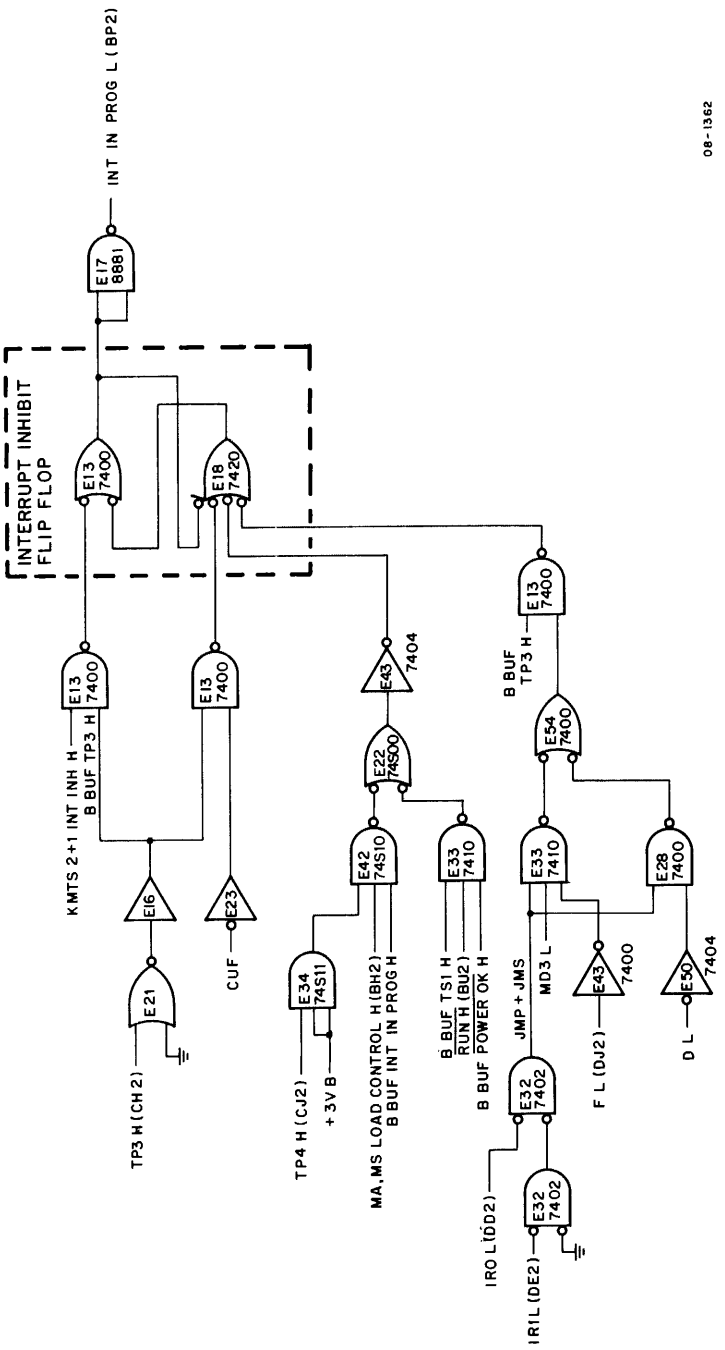


Figure 6-35 Interrupt Inhibit Logic

6.18.2 Power Fail/Auto Restart Programming (Figure 6-36)

The IOT instructions used with the Power Fail/Auto Restart option are as follows:

Mnemonic	Octal Code	Function
SPL	6102	Skip if the AC LOW flag is set or AC LOW signal is low. After detecting an AC LOW condition, flag should be cleared by a CAL instruction. Then test using the SPL instruction until ac goes above 105 V. Then test by an SPL instruction to skip on the level AC LOW being low. The INT RQST line will not be asserted after the flag has been cleared by CAL.
CAL	6103	Clear the AC LOW interrupt.
SBE	6101	Skip if the BATTERY EMPTY flag is set.

The device code for this option is fixed as 10.

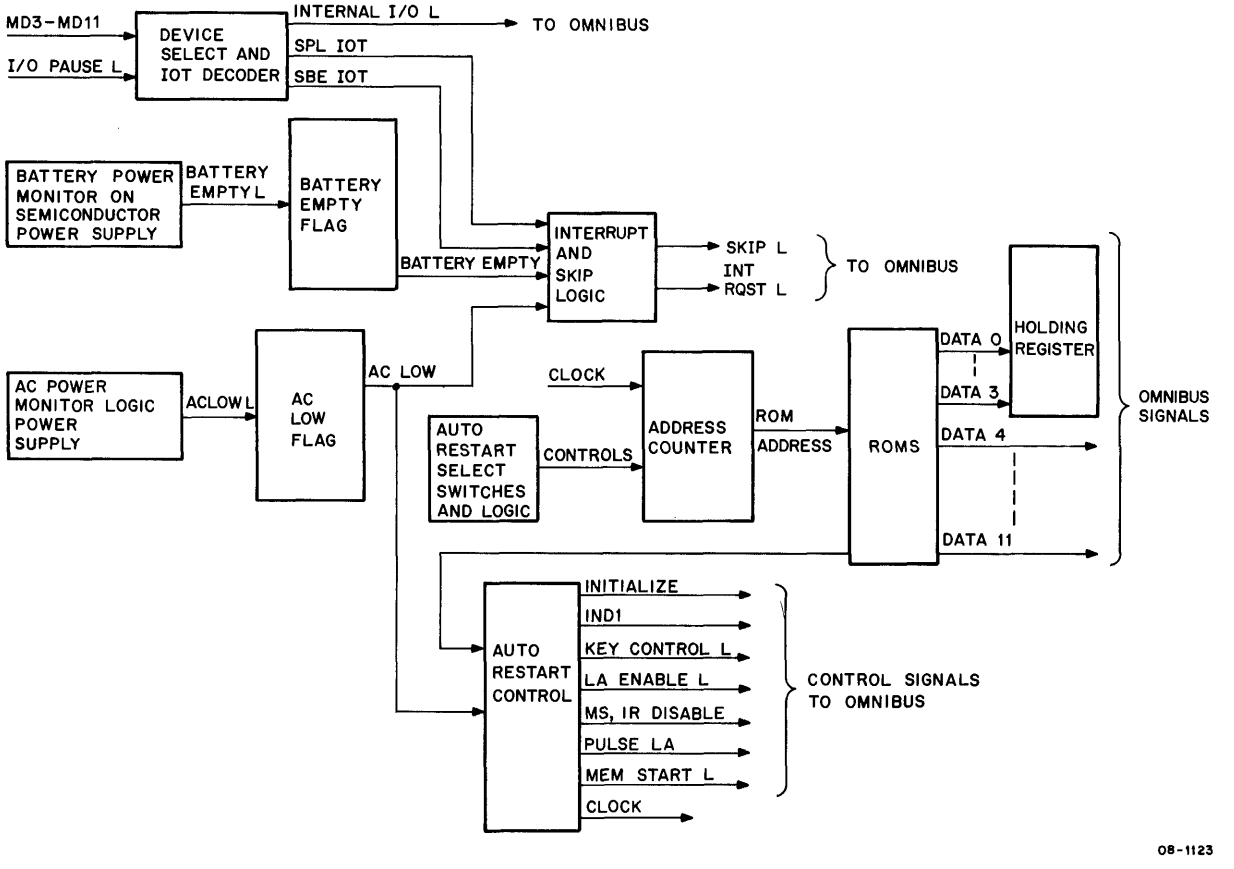


Figure 6-36 Power Fail and Auto Restart Block Diagram

6.18.3 Bootstrap Loader Block Diagram Description

The Bootstrap Loader (Figure 6-37) on the M8317 module provides the logic to deposit one of several programs that is contained in two ROMs on the M8317 module into read/write memory. These programs provide the necessary instructions to load programs from paper tape, disk, magnetic tape, etc., and to start the program at the specified location.

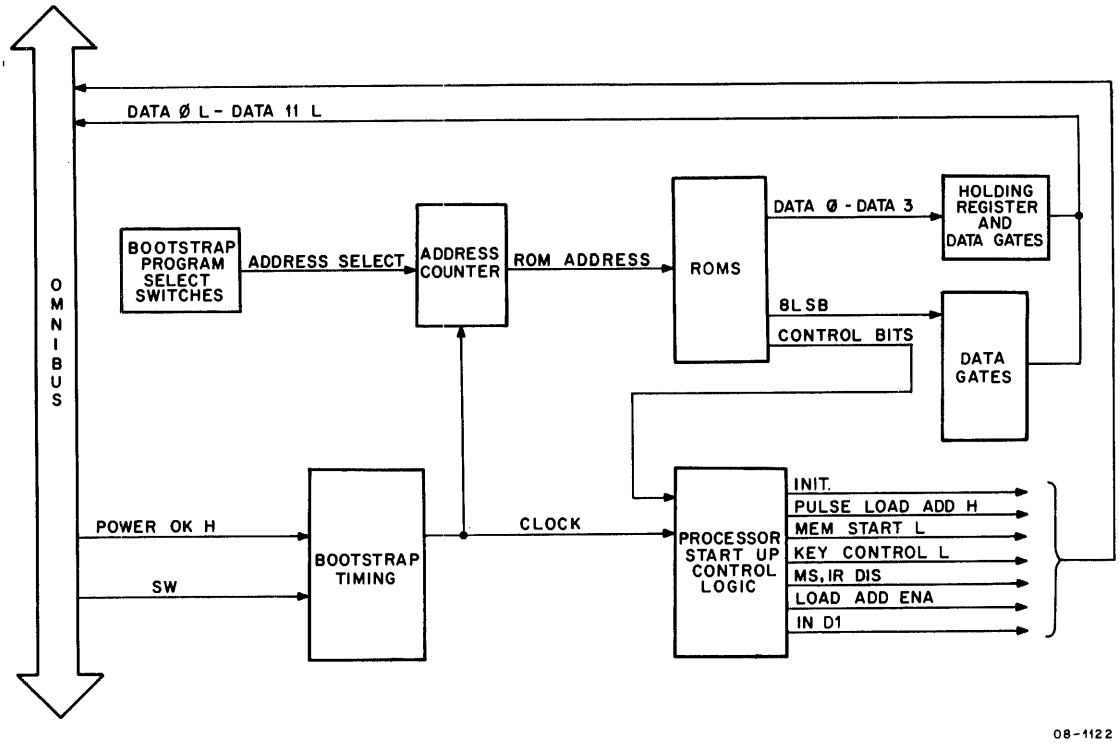


Figure 6-37 Bootstrap Loader Block Diagram

The Bootstrap Loader may be activated by pressing the BOOT switch on the Limited Function Panel or the optional Programmer's Console or from the transition of AC LOW from low to high. The computer must be halted for AC LOW to activate the bootstrap. Two switches on the M8317 module select the appropriate signal to activate the bootstrap.

The bootstrap can be started when the computer is turned on. This feature is enabled by a switch on the M8317 and allows the computer to be started remotely when the PDP-8/A is used as a peripheral.

6.19 BOOTSTRAP ROM ORGANIZATION AND PROGRAMMING

For those users who wish to write their own program into the bootstrap ROMs, the following procedures should be used.

6.19.1 ROM Organization

The two ROMs are connected as follows: the address lines are connected in parallel, i.e., two corresponding address lines of each ROM are connected together, and the outputs are arranged in serial fashion forming an 8-bit word, 4 outputs from each ROM. Because 12 bits are required for data/address information, two sequential addresses must be accessed from the ROMs to form a 16-bit word. Where the first 8 bits are temporarily stored in a register, then the next 8 bits are accessed from the ROMs. At this point, the control then decides what to do with 12 of the 16 bits. There are four possible actions that can take place at this time:

1. Load Address
2. Load Extended Address
3. Deposit
4. Start

The remaining 4 bits of the 16 actually tell the control which of the four actions are to take place. The 16-bit word should look like the word in Figure 6-38.

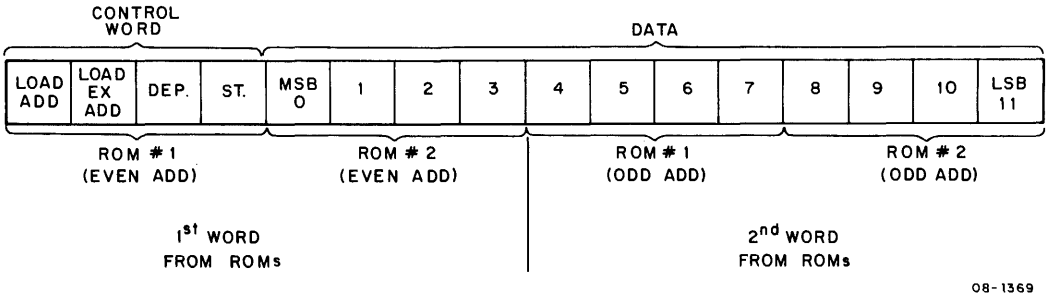


Figure 6-38 16 Bit Word ROM Format

The use of ROMs that have 256 addressable locations allows up to 128 words of ROM storage. These 128 locations may be used for bootstrap and/or auto-restart programs. Any auto-restart or bootstrap program may be located anywhere in the ROMs as long as the program starts in an even address in the ROM. If it is required that both bootstrap and auto-restart programs be accessible at the same time, activated by different signals, then of course the auto-restart program(s) must be located in addresses 0 through 15 in the ROMs. This is due to the addressing limits of the auto-restart select switches.

6.19.2 Auto-Restart/Bootstrap Sequence

The following events should take place when an auto-restart is initiated:

1. Load a 12 bit address
2. Load the extended address and start.

The following events should take place when the bootstrap is initiated:

1. Load a 12 bit initial address.
2. Load the Extended Address.
3. Deposit 12-bit data words, repeating as required by length of program, to be deposited.
4. Load a 12-bit starting address and start.

The decision to perform a bootstrap or an auto-restart is directed by a set of switches on the module. The bootstrap may be activated by the transition of the signal AC LOW from a logic low to a logical high or by a similar transition of the SW line on the Omnibus.

Auto-restart is only activated by AC LOW.

6.19.3 ROM Programming Examples

An auto-restart example is shown in Figure 6-39.

1. Load address 0200
2. Load field 0, start

Starting at ROM address 004.

	ROM NO. 1				ROM NO. 2				
Bit / Add	4	3	2	1	4	3	2	1	
4	1	0	0	0	0	0	0	0	Load Address 0200
5	1	0	0	0	0	0	0	0	
6	0	1	0	1	0	0	0	0	Load Ext. Add 0 and Start
7	0	0	0	0	0	0	0	0	

NOTE: Logic one (1) = + 3V

Figure 6-39 Auto Restart Example

6.19.4 Bootstrap Example (Figure 6-40)

1. Load address 0023
2. Load field 7
3. Deposit 2000
4. Deposit 6745
5. Deposit 0023
6. Deposit 7650
7. Deposit 5024
8. Deposit 6733
9. Deposit 5031
10. Load address 0024 and start

Starting at ROM address 124.

6.19.5 Obtaining Blank ROMs

Unprogrammed ROMs should be purchased by the user from Digital Equipment Corporation. The part number for an unprogrammed 256 X 4 ROM is 23-000A8.

	ROM NO. 1				ROM NO. 2				
Bit Add	4	3	2	1	4	3	2	1	
124	1	0	0	0	0	0	0	0	} Load Add 0023
125	0	0	0	1	0	0	1	1	
126	0	1	0	0	0	0	0	0	} Load Ext Add 7
127	0	0	1	1	1	0	0	0	
130	0	0	1	0	0	1	0	0	} Dep 2000
131	0	0	0	0	0	0	0	0	
132	0	0	1	0	1	1	0	1	} Dep 6745
133	1	1	1	0	0	1	0	1	
134	0	0	1	0	0	0	0	0	} Dep 0023
135	0	0	0	1	0	0	1	1	
136	0	0	1	0	1	1	1	1	} Dep 7650
137	1	0	1	0	1	0	0	0	
140	0	0	1	0	1	0	1	0	} Dep 5024
141	0	0	0	1	0	1	0	0	
142	0	0	1	0	1	1	0	1	} Dep 6733
143	1	1	0	1	1	0	1	1	
144	0	0	1	0	1	0	1	0	} Dep 5031
145	0	0	0	1	1	0	0	1	
146	1	0	0	1	0	0	0	0	} Load Add 24 & Start
147	0	0	0	1	0	1	0	0	

Figure 6-40 Bootstrap Example

6.20 ROM PROGRAM LISTING

All M8317 modules are shipped with the programs in either Table 6-6 or Table 6-7 stored in ROM No. 1 and ROM No. 2. The ROM patterns for these ROMs are listed in the KM8-A print set in Appendix H.

6.21 POWER FAIL/AUTO RESTART AND BOOTSTRAP OPERATION AND TIMING

6.21.1 Power Fail Operation

The power fail portion of the M8317 module initiates a controlled shutdown sequence when a power failure occurs. Circuits in the power supply monitor the ac voltage (Paragraph 7.2) and generate AC LOW L when the voltage falls below a predetermined level. In the 8A core memory systems, AC LOW L causes an INT RQST and the program must take the necessary action to store all active registers while the dc supply is adequate to maintain system operation. INT RQST is also asserted in these machines by ac power going low even though they switch to battery power. In the PDP-8/A Semiconductor memory system, operation is switched to battery power automatically when ac power fails. If ac power is not restored a fully loaded system will continue to run for up to 45 seconds. If ac power is restored, system operation is switched back to the regular power supply when they are in regulation. If power is not restored after a period of approximately 45 seconds, the BATTERY EMPTY signal is asserted and causes an INT RQST. At this time the program has 1 ms to do whatever is necessary to shut down the system before battery power is removed. When power is removed completely, the content of the MS8-A RAM is lost and programs in this memory must be reloaded.

Table 6-6
ROM No. 1 and ROM No. 2 Listings
(for ROMs Labeled 87A2 and 88A2)

ROM ADDRESS	MEMORY ADDRESS	CONTENTS (ROM and/or MEMORY)	COMMENTS
0	0000	0000	AUTO/RESTART
1			LOAD ADDRESS 0000
2	0000	0000	AUTO/RESTART
3			LOAD FIELD 0/START
4	0200	0200	AUTO/RESTART
5			LOAD ADDRESS 0200
6	0000	0000	AUTO-RESTART
7			LOAD FIELD 0/START
10	2000	2000	AUTO-RESTART
11			LOAD ADDRESS 2000
12	0000	0000	AUTO-RESTART
13			LOAD FIELD 0/START
14	4200	4200	AUTO-RESTART
15			LOAD ADDRESS 4200
16	0000	0000	AUTO-RESTART
17			LOAD FIELD 0/START
20	7737	7737	HIGH-LOW PAPERTAPE
21			LOAD ADDRESS 7737
22	0000	0000	LOAD FIELD 0
23			
24	7737	6014	DEPOSIT 6014
25			
26	7740	3376	DEPOSIT 3376
27			
30	7741	7326	DEPOSIT 7326
31			
32	7742	1337	DEPOSIT 1337
33			
34	7743	2376	DEPOSIT 2376
35			
36	7744	5341	DEPOSIT 5341
37			
40	7745	6011	DEPOSIT 6011
41			
42	7746	5356	DEPOSIT 5356
43			
44	7747	3361	DEPOSIT 3361
45			
46	7750	1361	DEPOSIT 1361
47			
50	7751	3371	DEPOSIT 3371
51			
52	7752	1345	DEPOSIT 1345
53			
54	7753	3357	DEPOSIT 3357
55			

Table 6-6 (Cont)
ROM No. 1 and ROM No. 2 Listings
(for ROMs Labeled 87A2 and 88A2)

ROM ADDRESS	MEMORY ADDRESS	CONTENTS (ROM and/or MEMORY)	COMMENTS
56	7754	1345	DEPOSIT 1345
57			
60	7755	3367	DEPOSIT 3367
61			
62	7756	6032	DEPOSIT 6032
63			
64	7757	6031	DEPOSIT 6031
65			
66	7760	5357	DEPOSIT 5357
67			
70	7761	6036	DEPOSIT 6036
71			
72	7762	7106	DEPOSIT 7106
73			
74	7763	7006	DEPOSIT 7006
75			
76	7764	7510	DEPOSIT 7510
77			
100	7765	5374	DEPOSIT 5374
101			
102	7766	7006	DEPOSIT 7006
103			
104	7767	6031	DEPOSIT 6031
105			
106	7770	5367	DEPOSIT 5367
107			
110	7771	6034	DEPOSIT 6034
111			
112	7772	7420	DEPOSIT 7420
113			
114	7773	3776	DEPOSIT 3776
115			
116	7774	3376	DEPOSIT 3376
117			
120	7775	5356	DEPOSIT 5356
121			
122	7737	7737	LOAD ADDRESS 7737/
123			START
124	0023	0023	RK8/E
125			LOAD ADDRESS 23
126	0000	0000	LOAD FIELD 0
127			
130	0023	2200	DEPOSIT 2200
131			
132	0024	6745	DEPOSIT 6745
133			

Table 6-6 (Cont)
ROM No. 1 and ROM No. 2 Listings
(for ROMs Labeled 87A2 and 88A2)

ROM ADDRESS	MEMORY ADDRESS	CONTENTS (ROM and/or MEMORY)	COMMENTS
134	0025	0023	DEPOSIT 0023
135			
136	0026	7640	DEPOSIT 7640
137			
140	0027	5024	DEPOSIT 5024
141			
142	0030	6743	DEPOSIT 6743
143			
144	0031	5031	DEPOSIT 5031
145			
146	0024	0024	LOAD ADDRESS 24/
147			START
150	7613	7613	TC08
151			LOAD ADDRESS 7613
152	0000	0000	LOAD FLD 0
153			
154	7613	6774	DEPOSIT 6774
155			
156	7614	1222	DEPOSIT 1222
157			
160	7615	6766	DEPOSIT 6766
161			
162	7616	6771	DEPOSIT 6771
163			
164	7617	5216	DEPOSIT 5216
165			
166	7620	1223	DEPOSIT 1223
167			
170	7621	5215	DEPOSIT 5215
171			
172	7622	0600	DEPOSIT 0600
173			
174	7623	0220	DEPOSIT 0220
175			
176	7754	7754	LOAD ADDRESS
177			7754
200	7754	7577	DEPOSIT 7577
201			
202	7755	7577	DEPOSIT 7577
203			
204	7613	7613	LOAD ADDRESS 7613/
205			START
206	7750	7750	RF08/DF32D
207			LOAD ADDRESS 7750
210	0000	0000	LOAD FIELD 0
211			

Table 6-6 (Cont)
ROM No. 1 and ROM No. 2 Listings
(for ROMs Labeled 87A2 and 88A2)

ROM ADDRESS	MEMORY ADDRESS	CONTENTS (ROM and/or MEMORY)	COMMENTS
212	7750	7600	DEPOSIT 7600
213			
214	7751	6603	DEPOSIT 6603
215			
216	7752	6622	DEPOSIT 6622
217			
220	7753	5352	DEPOSIT 5352
221			
222	7754	5752	DEPOSIT 5752
223			
224	7750	7750	LOAD ADDRESS 7750/
225			START
226	4000	4000	TA8/E
227			LOAD ADDRESS 4000
230	0000	0000	LOAD FIELD 0
231			
232	4000	1237	DEPOSIT 1237
233			
234	4001	1206	DEPOSIT 1206
235			
236	4002	6704	DEPOSIT 6704
237			
240	4003	6706	DEPOSIT 6706
241			
242	4004	6703	DEPOSIT 6703
243			
244	4005	5204	DEPOSIT 5204
245			
246	4006	7264	DEPOSIT 7264
247			
250	4007	6702	DEPOSIT 6702
251			
252	4010	7610	DEPOSIT 7610
253			
254	4011	3211	DEPOSIT 3211
255			
256	4012	3636	DEPOSIT 3636
257			
260	4013	1205	DEPOSIT 1205
261			
262	4014	6704	DEPOSIT 6704
263			
264	4015	6706	DEPOSIT 6706
265			
266	4016	6701	DEPOSIT 6701
267			

Table 6-6 (Cont)
ROM No. 1 and ROM No. 2 Listings
(for ROMs Labeled 87A2 and 88A2)

ROM ADDRESS	MEMORY ADDRESS	CONTENTS (ROM and/or MEMORY)	COMMENTS
270	4017	5216	DEPOSIT 5216
271			
272	4020	7002	DEPOSIT 7002
273			
274	4021	7430	DEPOSIT 7430
275			
276	4022	1636	DEPOSIT 1636
277			
300	4023	7022	DEPOSIT 7022
301			
302	4024	3636	DEPOSIT 3636
303			
304	4025	7420	DEPOSIT 7420
305			
306	4026	2236	DEPOSIT 2236
307			
310	4027	2235	DEPOSIT 2235
311			
312	4030	5215	DEPOSIT 5215
313			
314	4031	7346	DEPOSIT 7346
315			
316	4032	7002	DEPOSIT 7002
317			
320	4033	3235	DEPOSIT 3235
321			
322	4034	5201	DEPOSIT 5201
323			
324	4035	7737	DEPOSIT 7737
325			
326	4036	3557	DEPOSIT 3557
327			
330	4037	7730	DEPOSIT 7730
331			
332	4000	4000	LOAD ADDRESS 4000/
333			START
334 to 377	Spare Locations (36(10) ROM Address) (18(10) Words)		

Table 6-7
ROM No. 1 and ROM No. 2 Listings
(for ROMs Labeled 158A2 and 159A2)

ROM ADDRESS	MEMORY ADDRESS	CONTENTS (ROM and/or MEMORY)	COMMENTS
0	0000	0000	AUTO/RESTART
1			LOAD ADDRESS 0000
2	0000	0000	AUTO/RESTART
3			LOAD FIELD 0/START
4	0200	0200	AUTO/RESTART
5			LOAD ADDRESS 0200
6	0000	0000	AUTO-RESTART
7			LOAD FIELD 0/START
10	2000	2000	AUTO-RESTART
11			LOAD ADDRESS 2000
12	0000	0000	AUTO-RESTART
13			LOAD FIELD 0/START
14	4200	4200	AUTO-RESTART
15			LOAD ADDRESS 4200
16	0000	0000	AUTO-RESTART
17			LOAD FIELD 0/START
20	7737	7737	HIGH-LOW PAPERTAPE
21			LOAD ADDRESS 7737
22	0000	0000	LOAD FIELD 0
23			
24	7737	6014	DEPOSIT 6014
25			
26	7740	3376	DEPOSIT 3376
27			
30	7741	7326	DEPOSIT 7326
31			
32	7742	1337	DEPOSIT 1337
33			
34	7743	2376	DEPOSIT 2376
35			
36	7744	5341	DEPOSIT 5341
37			
40	7745	6011	DEPOSIT 6011
41			
42	7746	5356	DEPOSIT 5356
43			
44	7747	3361	DEPOSIT 3361
45			
46	7750	1361	DEPOSIT 1361
47			
50	7751	3371	DEPOSIT 3371
51			
52	7752	1345	DEPOSIT 1345
53			
54	7753	3357	DEPOSIT 3357
55			

Table 6-7 (Cont)
ROM No. 1 and ROM No. 2 Listings
(for ROMs Labeled 158A2 and 159A2)

ROM ADDRESS	MEMORY ADDRESS	CONTENTS (ROM and/or MEMORY)	COMMENTS
56	7754	1345	DEPOSIT 1345
57			
60	7755	3367	DEPOSIT 3367
61			
62	7756	6032	DEPOSIT 6032
63			
64	7757	6031	DEPOSIT 6031
65			
66	7760	5357	DEPOSIT 5357
67			
70	7761	6036	DEPOSIT 6036
71			
72	7762	7106	DEPOSIT 7106
73			
74	7763	7006	DEPOSIT 7006
75			
76	7764	7510	DEPOSIT 7510
77			
100	7765	5374	DEPOSIT 5374
101			
102	7766	7006	DEPOSIT 7006
103			
104	7767	6031	DEPOSIT 6031
105			
106	7770	5367	DEPOSIT 5367
107			
110	7771	6034	DEPOSIT 6034
111			
112	7772	7420	DEPOSIT 7420
113			
114	7773	3776	DEPOSIT 3776
115			
116	7774	3376	DEPOSIT 3376
117			
120	7775	5356	DEPOSIT 5356
121			
122	7737	7737	LOAD ADDRESS 7737/
123			START
124	0023	0023	RK8/E
125			LOAD ADDRESS 23
126	0000	0000	LOAD FIELD 0
127			
130	0023	2200	DEPOSIT 2200
131			
132	0024	6745	DEPOSIT 6745
133			

Table 6-7 (Cont)
ROM No. 1 and ROM No. 2 Listings
(for ROMs Labeled 158A2 and 159A2)

ROM ADDRESS	MEMORY ADDRESS	CONTENTS (ROM and/or MEMORY)	COMMENTS
134	0025	0023	DEPOSIT 0023
135			
136	0026	7640	DEPOSIT 7640
137			
140	0027	5024	DEPOSIT 5024
141			
142	0030	6743	DEPOSIT 6743
143			
144	0031	5031	DEPOSIT 5031
145			
146	0024	0024	LOAD ADDRESS 24/
147			START
150	0024	0024	RX8E
151			LOAD ADDRESS 0024
152	0000	0000	LOAD FIELD 0
153			
154	0024	7126	DEPOSIT 7126
155			
156	0025	1060	DEPOSIT 1060
157			
160	0026	6751	DEPOSIT 6751
161			
162	0027	7201	DEPOSIT 7201
163			
164	0030	4053	DEPOSIT 4053
165			
166	0031	4053	DEPOSIT 4053
167			
170	0032	7104	DEPOSIT 7104
171			
172	0033	6755	DEPOSIT 6755
173			
174	0034	5054	DEPOSIT 5054
175			
176	0035	6754	DEPOSIT 6754
177			
200	0036	7450	DEPOSIT 7450
201			
202	0037	7610	DEPOSIT 7610
203			
204	0040	5046	DEPOSIT 5046
205			
206	0041	1060	DEPOSIT 1060
207			
210	0042	7041	DEPOSIT 7041
211			

Table 6-7 (Cont)
ROM No. 1 and ROM No. 2 Listings
(for ROMs Labeled 158A2 and 159A2)

ROM ADDRESS	MEMORY ADDRESS	CONTENTS (ROM and/or MEMORY)	COMMENTS
212	0043	1061	DEPOSIT 1061
213			
214	0044	3060	DEPOSIT 3060
215			
216	0045	5024	DEPOSIT 5024
217			
220	0046	6751	DEPOSIT 6751
221			
222	0047	4053	DEPOSIT 4053
223			
224	0050	3002	DEPOSIT 3002
225			
226	0051	2050	DEPOSIT 2050
227			
230	0052	5047	DEPOSIT 5047
231			
232	0053	0000	DEPOSIT 0000
233			
234	0054	6753	DEPOSIT 6753
235			
236	0055	5033	DEPOSIT 5033
237			
240	0056	6752	DEPOSIT 6752
241			
242	0057	5453	DEPOSIT 5453
243			
244	0060	7024	DEPOSIT 7024
245			
246	0061	6030	DEPOSIT 6030
247			
250	0033	0033	LOAD ADDRESS 0033/
251			START
252	7750	7750	RF08/DF32D
253			LOAD ADDRESS 7750
254	0000	0000	LOAD FIELD 0
255			
256	7750	7600	DEPOSIT 7600
257			
260	7751	6603	DEPOSIT 6603
261			
262	7752	6622	DEPOSIT 6622
263			
264	7753	5352	DEPOSIT 5352
265			
266	7754	5752	DEPOSIT 5752
267			

Table 6-7 (Cont)
ROM No. 1 and ROM No. 2 Listings
(for ROMs Labeled 158A2 and 159A2)

ROM ADDRESS	MEMORY ADDRESS	CONTENTS (ROM and/or MEMORY)	COMMENTS
270	7750	7750	LOAD ADDRESS 7750/
271			START
272	4000	4000	TA8/E
273			LOAD ADDRESS 4000
274	0000	0000	LOAD FIELD 0
275			
276	4000	1237	DEPOSIT 1237
277			
300	4001	1206	DEPOSIT 1206
301			
302	4002	6704	DEPOSIT 6704
303			
304	4003	6706	DEPOSIT 6706
305			
306	4004	6703	DEPOSIT 6703
307			
310	4005	5204	DEPOSIT 5204
311			
312	4006	7264	DEPOSIT 7264
313			
314	4007	6702	DEPOSIT 6702
315			
316	4010	7610	DEPOSIT 7610
317			
320	4011	3211	DEPOSIT 3211
321			
322	4012	3636	DEPOSIT 3636
323			
324	4013	1205	DEPOSIT 1205
325			
326	4014	6704	DEPOSIT 6704
327			
330	4015	6706	DEPOSIT 6706
331			
332	4016	6701	DEPOSIT 6701
333			
334	4017	5216	DEPOSIT 5216
335			
336	4020	7002	DEPOSIT 7002
337			
340	4021	7430	DEPOSIT 7430
341			
342	4022	1636	DEPOSIT 1636
343			
344	4023	7022	DEPOSIT 7022
345			

Table 6-7 (Cont)
ROM No. 1 and ROM No. 2 Listings
(for ROMs Labeled 158A2 and 159A2)

ROM ADDRESS	MEMORY ADDRESS	CONTENTS (ROM and/or MEMORY)	COMMENTS
346	4024	3636	DEPOSIT 3636
347			
350	4025	7420	DEPOSIT 7420
351			
352	4026	2236	DEPOSIT 2236
353			
354	4027	2235	DEPOSIT 2235
355			
356	4030	5215	DEPOSIT 5215
357			
360	4031	7346	DEPOSIT 7346
361			
362	4032	7002	DEPOSIT 7002
363			
364	4033	3235	DEPOSIT 3235
365			
366	4034	5201	DEPOSIT 5201
367			
370	4035	7737	DEPOSIT 7737
371			
372	4036	3557	DEPOSIT 3557
373			
374	4037	7730	DEPOSIT 7730
375			
376	4000	4000	LOAD ADDRESS 4000/ START
377			

6.21.2 Auto-Restart Operation and Timing

The auto-restart portion of the M8317 module restarts the PDP-8/A after a power failure or when power is turned on locally or remotely. The program may be started at address 4200, 2000, 0200, or 0000. The address is switch selectable on the M8317 module.

The computer must start by executing the instruction stored in the starting location.

The CPMA register and the IF and DF registers in the memory extension portion of the M8317 module must be loaded with the starting address before CPU timing is allowed to start. Before start-up, all devices must be initialized and the Major State register must be manipulated so that it starts out in the Fetch major state. The auto-restart logic accomplishes this by asserting the Omnibus signals and performing transfers that normally occur from the Programmer's Console.

At the Programmer's Console, the start-up procedure is as follows:

1. Enter the Instruction Field and Data Field and press LXA (load DF and IF registers).
2. Enter starting address and press LA .
3. Press INIT and then RUN (Initialize and start from FETCH).

These operations are performed by the auto-restart portion of the KM8-AA.

The timing for this operation is shown in Figure 6-41. The detailed logic description of this operation is given in Paragraph 6.22.

The starting addresses (0000, 0200, 2000 and 4200) are stored in a 256 X 8 ROM along with the necessary control bits. The first ROM address to be accessed when the auto-restart operation begins is determined by switches on the M8317 module which preset the ROM address counter to this first address. The address counter is then incremented to read four ROM memory locations, which supply the field, the starting address and the necessary control signals required to load the field and starting address, initialize the processor, and start the program. Four of the 256 ROM locations are used for each of the starting addresses, a total of 16 addresses for the auto-restart operation. Except for the last 43 locations, the remainder of the ROM chip is used for bootstrap operation. (Refer to Table 6-6 and Figure 6-40).

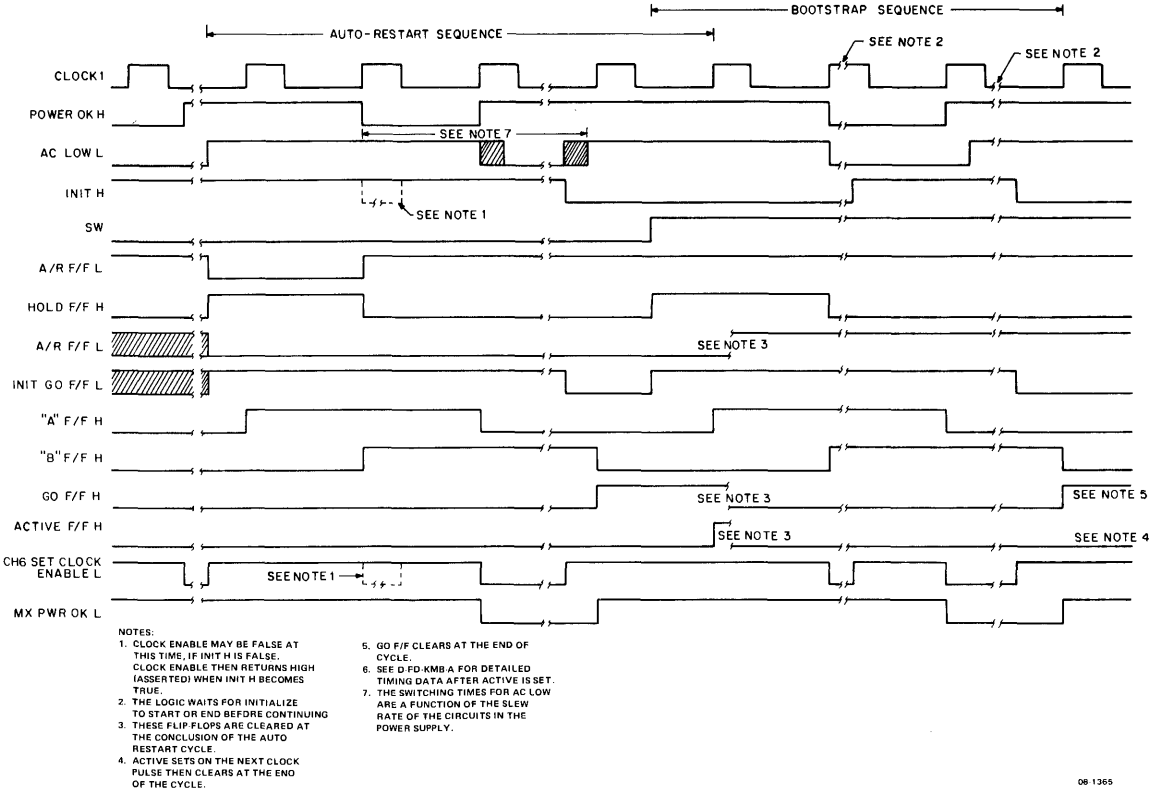


Figure 6-41 Auto Restart and Bootstrap Timing

6.21.3 Bootstrap Operation and Timing

The bootstrap operation portion of the M8317 logic is used to load short programs into memory which are used to load programs from system devices and to start the program at the specified location. A bootstrap operation is initiated by pressing BOOT on the Programmer's Console twice or by raising and lowering the BOOT switch on the Limited Function Panel.

When the Bootstrap operation is initiated the following occurs:

1. The CPU is initialized.
2. Load extended address and starting address to define the first address in which to deposit instructions.
3. Deposit instructions in sequential locations.
4. Load the starting address of the program just deposited.
5. Start the program.

In this operation the content specified locations in the 256 X 8 ROM is used to furnish the field, starting address, control signals, and programmed instructions required to transfer a program from a system device (Table 6-6). The specified location in ROM from which this information is obtained is determined by switches on the M8317 module.

The timing required for this operation is shown in Figures 6-41 and 6-42. The detailed logic description of this operation is given in Paragraph 6.22.

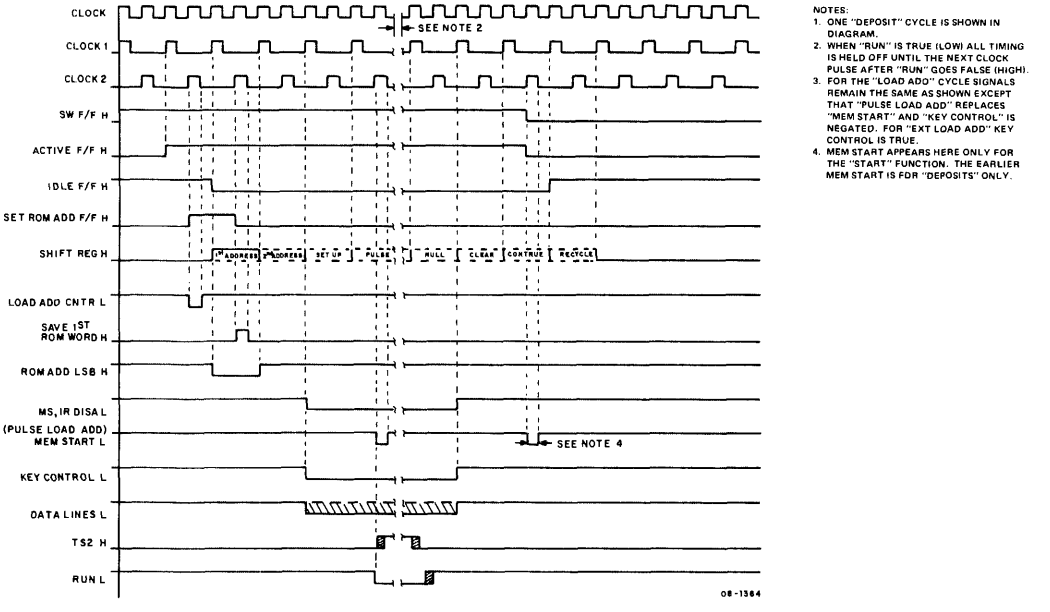


Figure 6-42 Bootstrap Timing

6.22 POWER FAIL/AUTO-RESTART AND BOOTSTRAP OPERATION DETAILED LOGIC DESCRIPTION

Some of the functional groups of logic on the M8317 are shared by the power fail/auto-restart and the bootstrap option. During this discussion it will be pointed out that when a functional group of logic applies to only one of the operations, or if it applies to more than one operation and its use. The block diagrams in Figures 6-36 and 6-37 should be used to determine which groups of logic are used by the individual operations and the interrelationship between the groups of logic as well as the signal flow.

6.22.1 Power Fail/Auto-Restart Device Select and Operation Decoder

The Power Fail/Auto-Restart device select and operation decoder logic is shown in Figure 6-43.

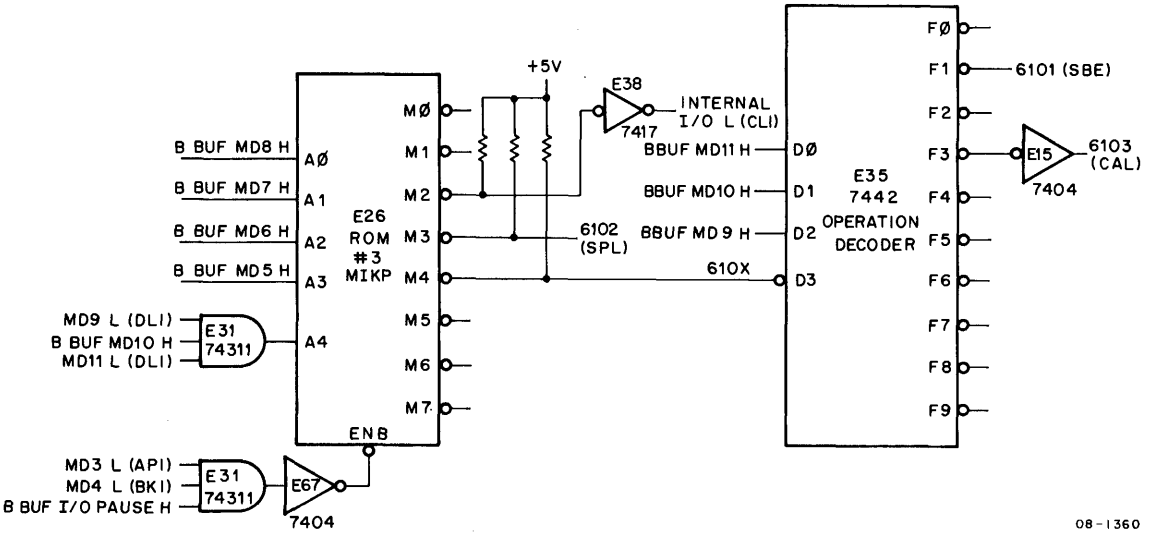


Figure 6-43 Power Fail Auto Restart Device Select and Operation Decoder

ROM No. 3, the device select decoder, is enabled by MD3 L, MD4 L and BBUF I/O PAUSE H when a 61XX instruction is executed by the program. When the ROM is enabled, it is addressed by BBUF MD5 H-BBUF MD8 H and the AND of MD9 L, BBUF MD10 H, and MD11 L. When a 610X instruction is executed by the program, the ROM address selected supplies an output which asserts INTERNAL I/O L and the 610X device select signal. INTERNAL I/O L is asserted to tell the KA8-E Positive I/O that the instruction is not to be decoded by the KA8-E. The 610X signal enables the operation decoder to decode the 6101 and 6103 instructions. When the program executes a 6102 (SPL) instruction the output of AND gate E31 adds an additional bit to the ROM address to select the location with an output which asserts INTERNAL I/O L and the 6102 signal line.

This causes the power fail/auto-restart option to execute the 6102 instruction.

The operation decoder is enabled by the 610X signal when a 610X instruction is decoded by the program. The operation decoder is a 7442 IC. The 7442 IC is a BCD to decimal decoder which decodes BBUF MD9-BBUF MD10 and asserts the necessary signals to execute the 6107 and 6103 instructions.

6.22.2 Power Fail Interrupt and Skip Logic

The power fail interrupt and skip logic is shown in Figure 6-44. There are two flags associated with SKIP L and INT RQST L – 1. The AC LOW flag, which is set by AC LOW L from the power supply when the ac voltage falls below a specified level, and 2. the BATTERY EMPTY flag, which sets when BATTERY EMPTY L is asserted by the power supply logic (applicable only to PDP-8/A Semiconductor computers). BATTERY EMPTY L is asserted prior to depletion of the battery so that the battery will never completely discharge. A fully loaded system runs approximately 45 seconds on battery power.

INT RQST L is asserted to interrupt the program if the BATTERY EMPTY or the AC LOW flags sets. The program must check the flags and determine which one caused the interrupt and what action is to be taken.

SKIP L is asserted to cause the program to skip an instruction if flag AC LOW is set or the AC LOW level is asserted and the 6102 instruction is executed or if BATTERY EMPTY is set and the 6101 instruction is executed. AC LOW flag is cleared by the 6103 instruction, but the program may still check the level by using the 6102 instruction.

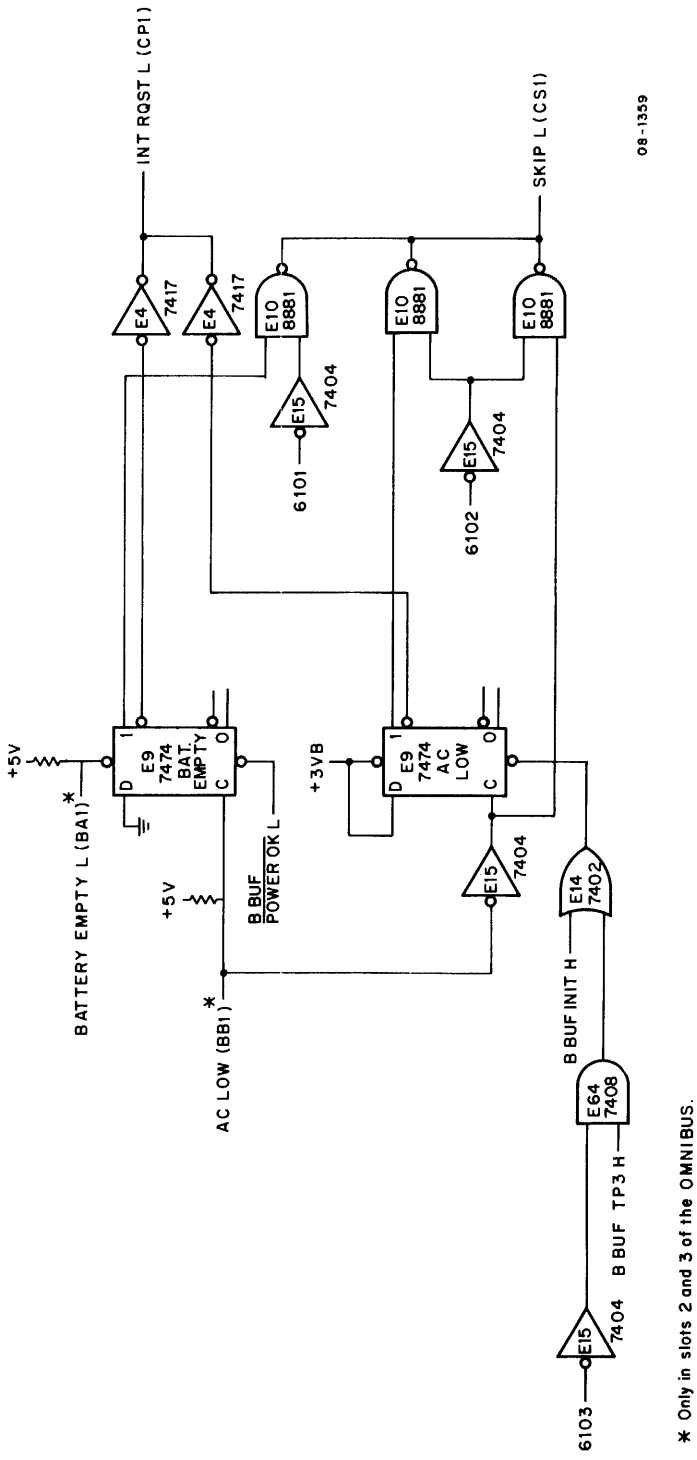


Figure 6-44 Bootstrap and Auto Start Clock

6.22.3 Bootstrap and Auto-Restart Timing Clock

The bootstrap and auto-restart clock logic in Figure 6-44 generates two clock signals, CLK1 and CLK2, which provide the timing pulses for the bootstrap and auto-restart operations. The MIKP1 CLK signal is generated by a 66 kHz (approximately) RC oscillator. The clock signal is disabled by holding ENA (E65) cleared, during initialization and power up operations or when the bootstrap and auto-restart logic is in an inactive state (ACTIVE flip-flop cleared and HOLD flip-flop set). The timing for the generation of CLK1 and CLK2 is shown in Figure 6-45. CLK1 and CLK2 pulse duration is approximately 7.5 μs; both input to the JK flip-flop (E90) so that it complements on trailing edge of each clock pulse. AND gates E86A and E86B are enabled on alternate clock pulses to generate two differentclocksignals at half the frequency of the MIKP1 CLK H signal.

6.22.4 Bootstrap Initialization Logic

The purpose of this logic is to initialize the CPU, Extended Memory Control and all peripherals, preset the ROM address counter to the address selected by the bootstrap select switches, set flip-flops to provide enabling signals for the bootstrap operation, and clear the control shift register.

If S1-8 is on the bootstrap operation (Figure 6-46) is initiated when SW makes a low to high transition to clock the HOLD flip flop causing it to set. If S1-4 is on HOLD will set only if the PDP-8/A is stopped. When HOLD sets, it enables the clock (Figures 6-45 and 6-46) and clears INIT GO. The first CLK1 pulse after HOLD is set, sets flip-flop A and B which enables AND gate E64. The high out of E64 turns Q1 on and the POWER OK H line is pulled low. Asserting POWER OK H allows the CPU to negate INITIALIZE H after 200 to 1000 ms. The negation of INITIALIZE H and having cleared flip-flop A sets INIT GO.

The next CLK pulse after flip-flop A is cleared clears flip-flop B, which sets the GO flip-flop. If S1-7 is open, NAND gate E60 is enabled when go sets to assert MIKP1 ENA BOOT ADD L. This enables the address selected by the bootstrap switches to preset the ROM address counters to the address of the first ROM location to be accessed during the bootstrap operation Paragraph 6.21.3). The address is loaded into the address counter by the assertion of MIKP1 ADD LOAD L during the next CLK2 pulse. ROM A SET is not cleared until ACT is set by the next CLK1 pulse so NAND gate E54 is enabled.

The next CLK1 pulse sets ACT, which in turn clears ROM A set and allows IDLE to clear on the next CLK1 pulse. ROM A is held cleared to disable NAND gate E54 and hold MIKP1 LOAD ADD L high to remove the input from the bootstrap select switches to the ROM address counters. At this time, the ROM address counters are preset to the address of the first ROM location to be accessed.

At this point, control of the bootstrap operation is taken over by the four control bits out of ROM No. 1 control counter (Paragraph 6.21.3).

6.22.5 Auto-Restart Initialization Logic

The purpose of this logic is to Initialize the CPU, the Extended Memory Control and all peripherals, preset the ROM Address counter to the address selected by the auto-restart switches, set the necessary flip-flops to provide enabling signals for the auto-restart operation, and clear the control shift register (Figure 6-47).

An auto-restart operation is initiated when AC LOW L is negated after power is turned on. The initialization and conditioning of the logic to enable an auto-restart operation is similar to the bootstrap operation so this description will not be repeated.

Having disabled NAND gate E54, and not running the CPU enables the data input to the AR flip-flop, and when AC LOW L is negated (high) the AR flip-flop sets. If S1-6 and S1-7 are ON (closed) the MIKP1 ENABLE RESTART ADD L is asserted to apply the address selected by the auto-restart switches to the address counter input. ROM A set is dc set by having cleared ACT during the initialization during power up. NAND gate E54 is enabled by CLK2 and MIKP1 ADD LOAD L presets the address counter with the address selected by the auto-restart switches. ROM A is cleared, and the next CLK2 pulse after IDLE is cleared as it was for the bootstrap operation (Paragraph 6.21.3).

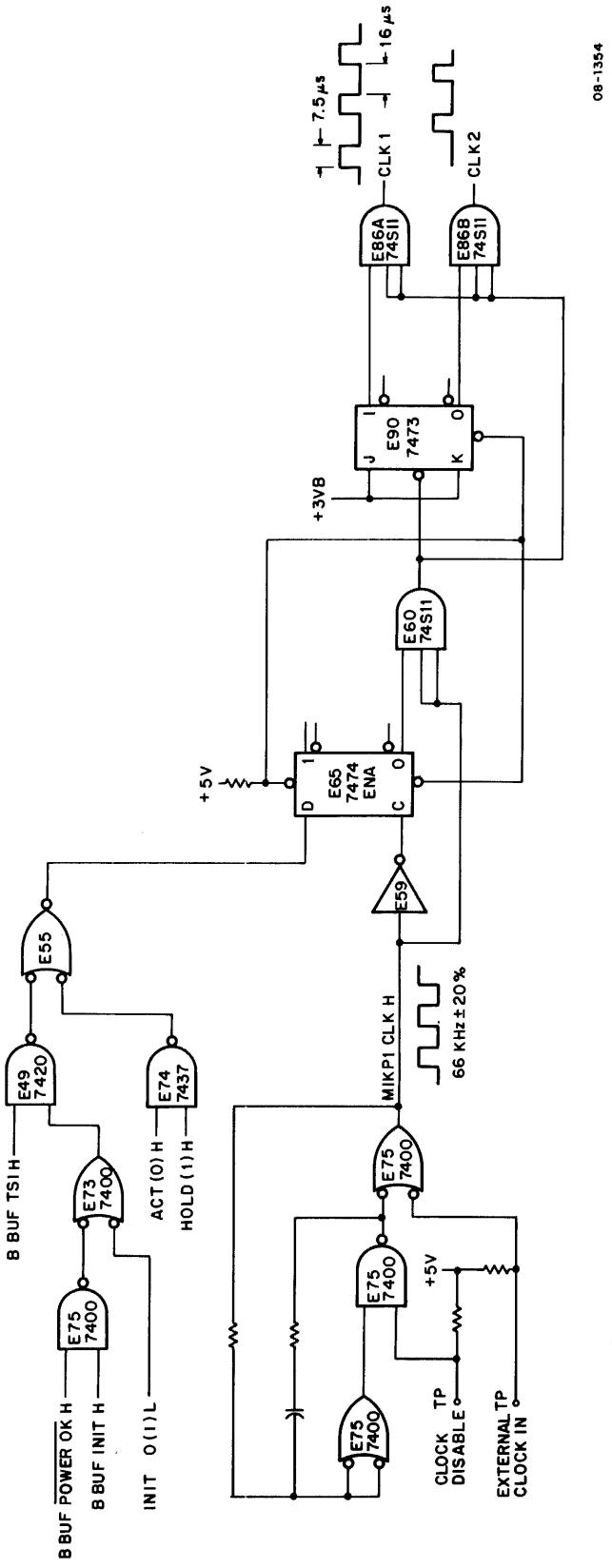


Figure 6-45 Bootstrap and Auto Start Clock

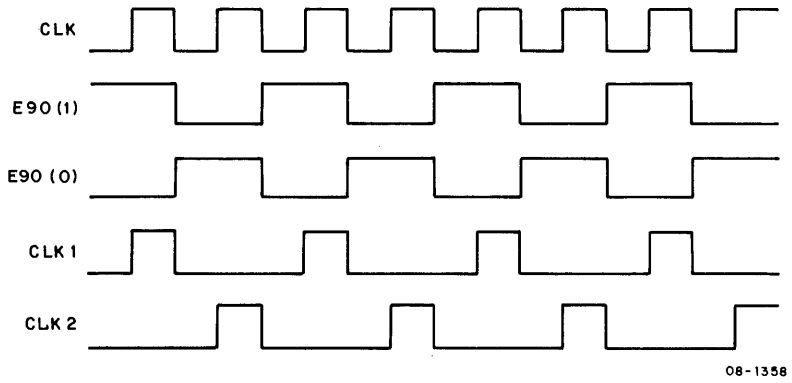


Figure 6-46 CLK1 and CLK2 Timing

6.22.6 Auto-Restart and Bootstrap Address Counters

The address counters in Figure 6-48 are preset to the first ROM address to be accessed when an auto-restart or bootstrap operation is started. The first address is always an even number. The 2 8266 IC's select either the condition of the bootstrap select switches or the auto-restart switches as input to the address counters. The address counter, consisting of two 74197 ICs is loaded when MIKP1 ADD LOAD L is asserted (see Figure 6-47). Incrementation of the counter takes place at the end of a control register cycle where CLK2 is ANDed with RECYCLE asserting MIKP1 INCRMT ADD counter L. The bootstrap and auto-restart switch settings are listed in Tables 2-10 through 2-13.

6.22.7 ROM Memory Control and Multiplexers

ROM Nos. 1 and 2, along with their associated multiplexers and control logic, are shown in Figure 6-49. The ROMs are addressed by the address counter and supply as output four control bits and a 12-bit word (Figure 6-38). The control bits are used to generate control signals which are used to load an extended memory address (field), load the memory address, or deposit a 12-bit word into read/write memory. The first 16-bit word read from memory also contains a bit which asserts MIKP2 START H. This signal is used to assert INITIALIZE H (Figure 6-49) during the first pass through the control shift register, and initialize the CPU, extended memory option, and all peripherals. The content of the two addressed locations in ROM Nos. 1 and 2 are transferred to the Data Bus during TS2 for deposit operations or by MIKP2 ENA DATA H to load the extended address or memory address.

MIKP2 ENA ADD DATA H is asserted by outputs of the control shift register (Figure 6-50) to enable the address data.

6.22.8 Bootstrap and Auto-Restart Operation Control Logic

The function of the control shift register and the associated logic is to assert the Omnibus signals required to address memory deposit information in a memory location and start the program. During auto-restart operations, a memory address is loaded into the memory address register and the program is started in field 0 at the selected address.

The control shift register is a 74164 IC used as an 8-bit shift register. A high on the two serial inputs allows the first bit to become a one on the first CLK1 pulse after ROM A sets. Subsequent clock 1 pulses will shift the 1 through the shift register and as it is shifted, the control signals on the output are asserted to assert the necessary Omnibus and control signals for the bootstrap and auto-restart operations. The timing required for these operations is shown in Figures 6-43 and 6-44. In subsequent passes the bit 1 in the shift register is set to 1 by RECYCLE out of the shift register.

A description of the Omnibus signal, asserted by the control signals out of the control shift register, is in Chapter 3.

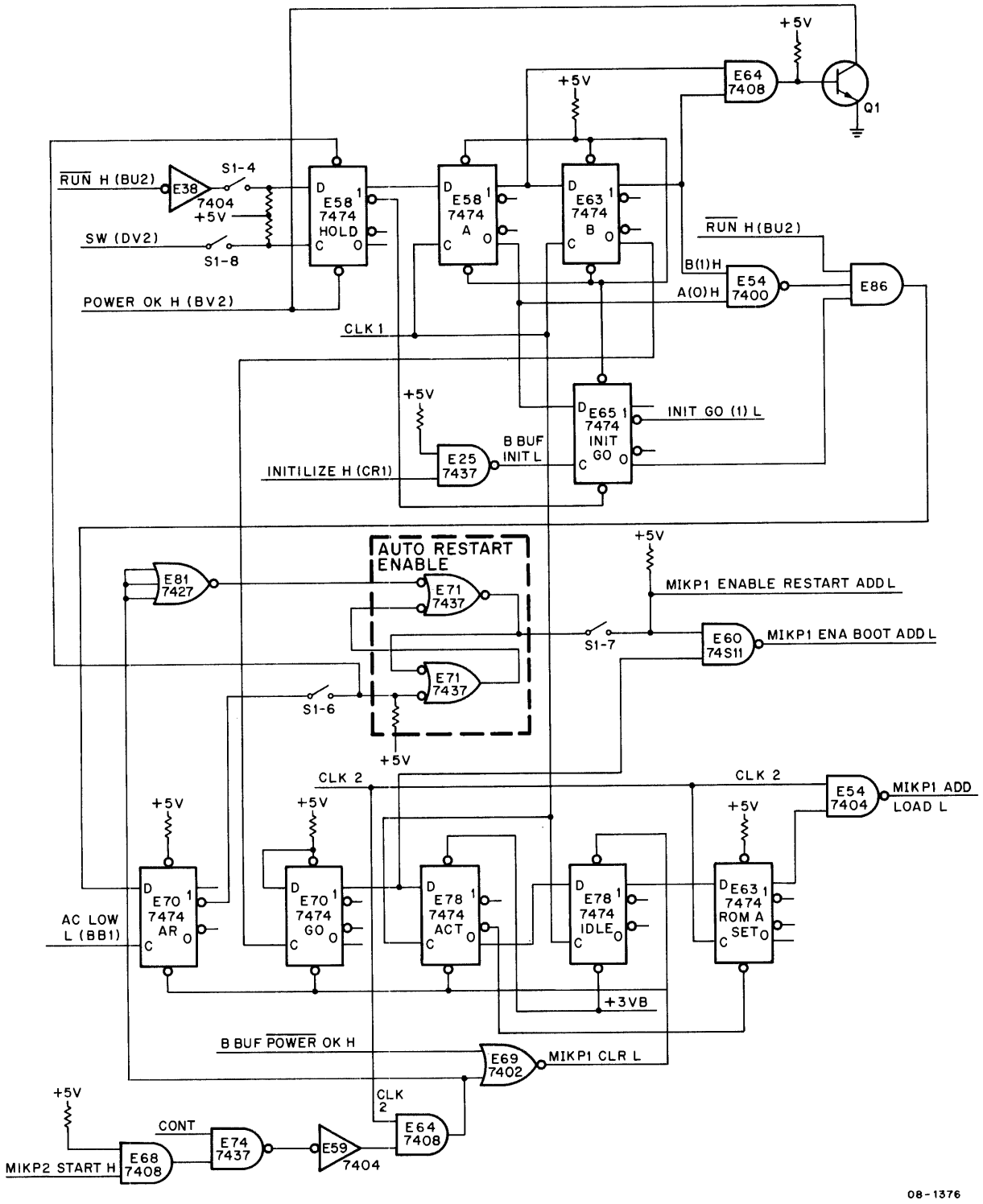


Figure 6-47 Auto Restart Initialization Logic

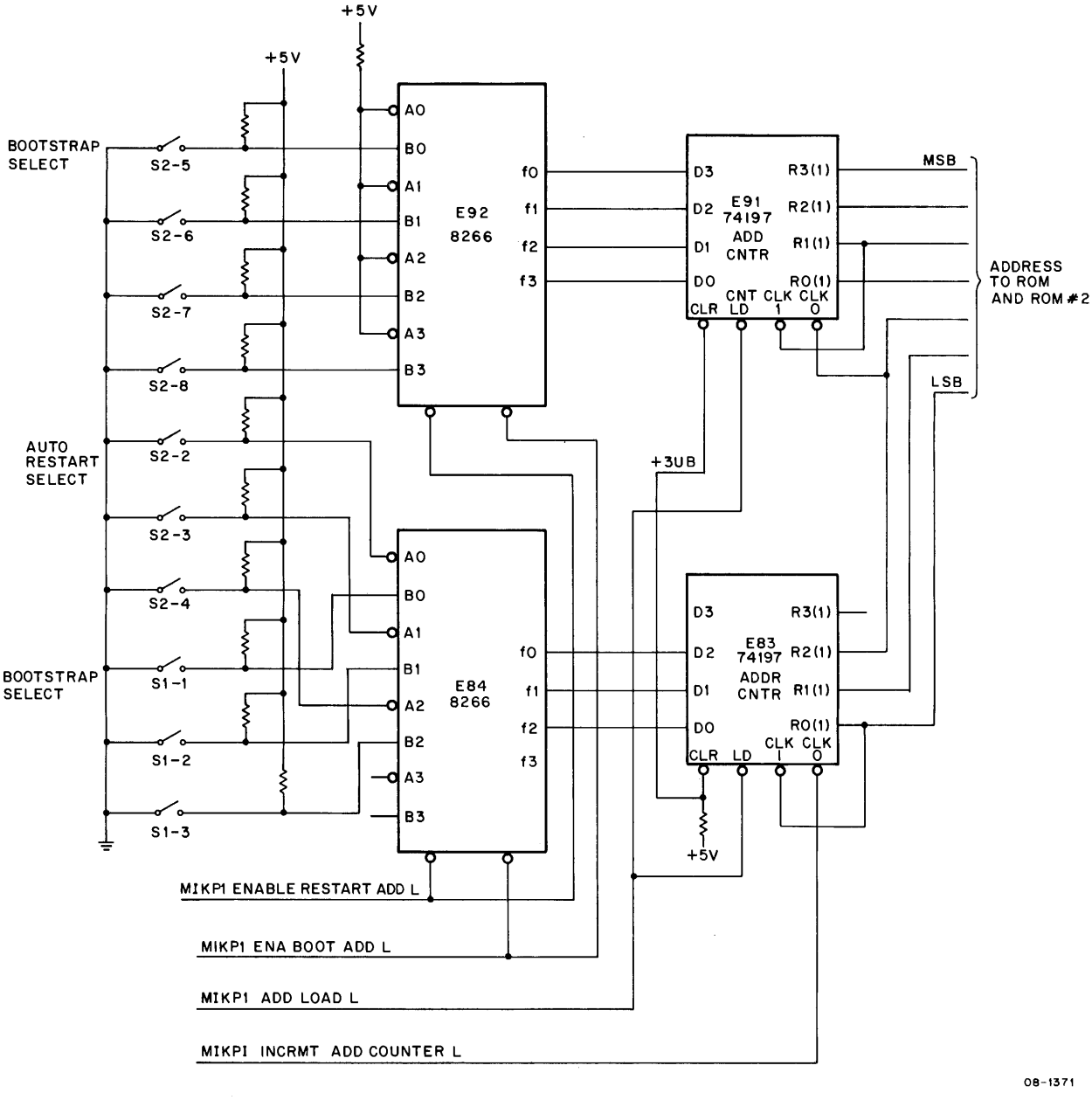


Figure 6-48 Auto Restart and Bootstrap ROM Address Counters

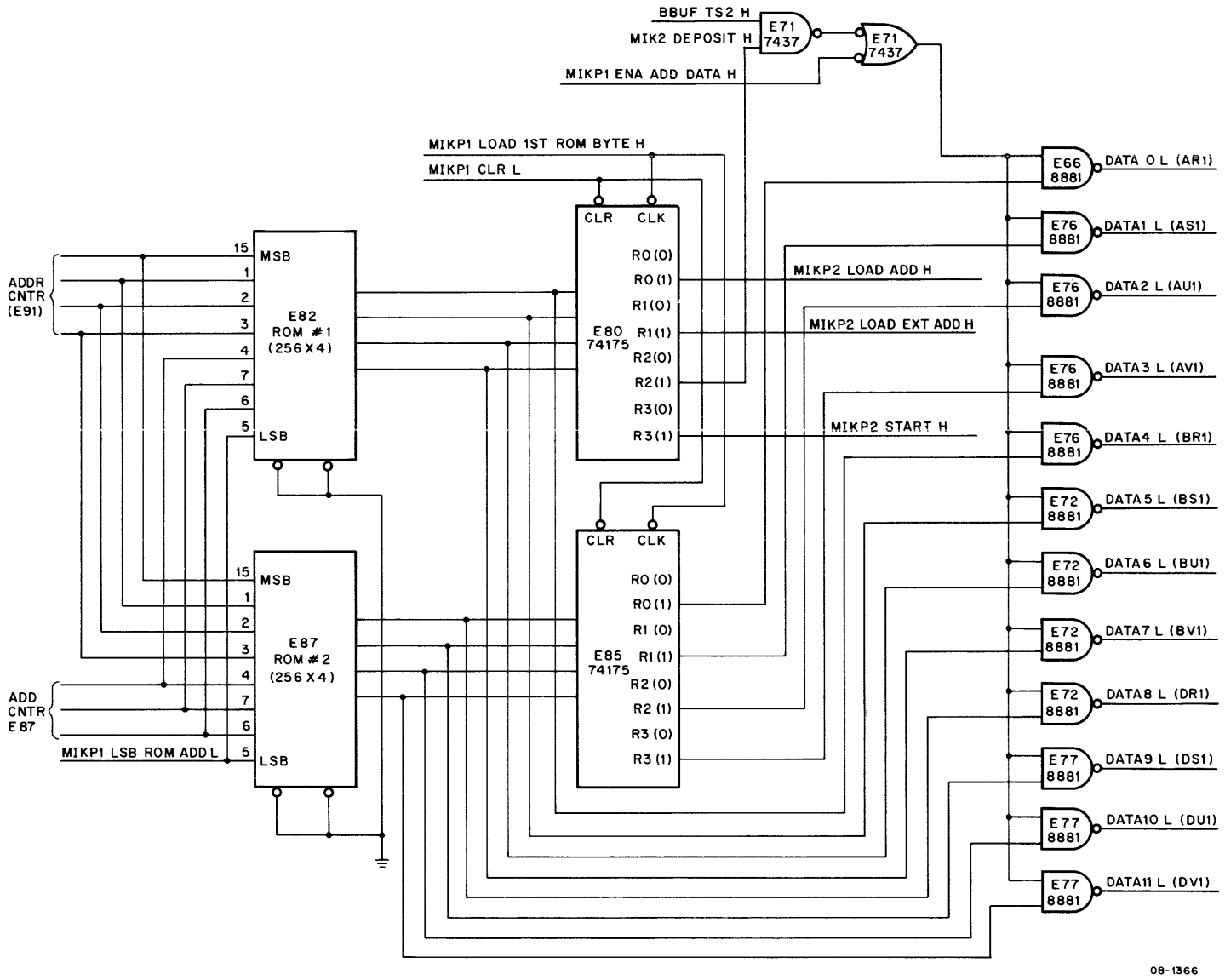


Figure 6-49 ROM Memory Control and MUX

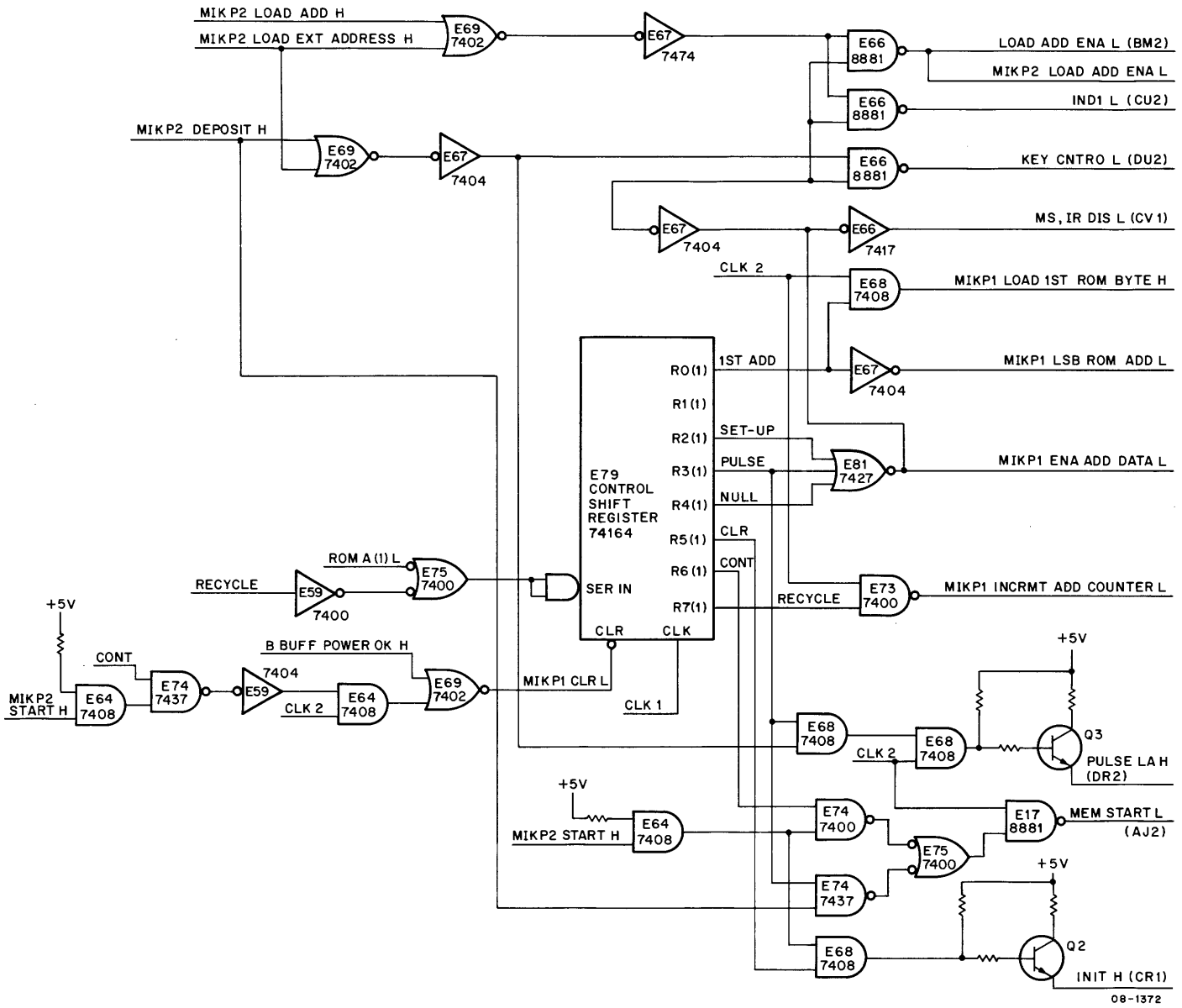


Figure 6-50 Bootstrap and Auto Restart Operation Control Logic

CHAPTER 7
POWER SUPPLY

7.1 GENERAL

There are two types of computers in the PDP-8/A family, namely, the PDP-8/A Semiconductor computer and the 8A-series of computers. A basic difference between these two types is their respective memories. The PDP-8/A uses semiconductor memories that have capacities ranging from 1K to 4K (a maximum capacity of 32K is possible). The 8A-series of computers uses expandable core memory of 8K or 16K. The PDP-8/A Semiconductor computer features battery backup to power the computer during momentary ac power interruptions.

Another difference between the two types of computers is the Omnibus assembly used with each. The PDP-8/A computer uses a 10-slot Omnibus (H9192) that accommodates both quad and hex modules (connectors E and F of the hex modules do not plug into the Omnibus), while the 8A computers use either a 12-slot Omnibus (H9194) or a 20-slot Omnibus (H9195). Both the 12-slot Omnibus and the 20-slot Omnibus have some slots that are reserved for hex modules whose E connector must plug into the Omnibus. Power for the PDP-8/A is provided by an H763 Power Supply assembly; this assembly includes a regulator pc board and a power pc board, both of which are inserted in the Omnibus. Power for the 8A computers is provided either by an H9300 chassis assembly or by a BA8-C chassis assembly, each of which includes a regulator pc board (pc boards, in the BA8-C) and the necessary Omnibus connector block(s). Table 7-1 summarizes the foregoing and also lists other assemblies that pertain to computer primary power.

Table 7-1
PDP-8/A Family, Primary Power Assemblies

Computer Type	Omnibus	Basic Power Assembly	Basic Power Assembly Includes
PDP-8/A	H9192	H763 Power Supply Assembly	G8016 Regulator Board Power Board Transformer Assembly Line Set Limited Function Panel
8A 8A400 8A600 8A800	H9194	H9300 Chassis Assembly	H9194 Connector Block Assembly G8018 Regulator Board Transformer Assembly Line Set Limited Function Panel
8A420 8A620 8A820	H9195	BA8-C Chassis Assembly	H9195 Omnibus Power Distribution Board Assembly (5412000) G8018 Regulator Board (2) Transformer Assembly Line Set Limited Function Panel

All the basic power assemblies are discussed in this chapter, Paragraph 7.2 covers the PDP-8/A Semiconductor assembly, Paragraph 7.3 covers the 8A400/600/800 assembly, and Paragraph 7.4 covers the 8A420/620/820 assembly.

7.2 PDP-8/A SEMICONDUCTOR BASIC POWER ASSEMBLY

The basic power assembly for the PDP-8/A consists of the G8016 regulator board, the power board, a transformer assembly, a line set, and a Limited Function Panel. Figure 7-1 illustrates the assembly interconnections. The Limited Function Panel has been described in Paragraph 4.3.1, the regulator board is described in Paragraph 7.2.2, and the power board is detailed in the following Paragraph 7.2.1.

7.2.1 Power Board

The power board circuits are shown in Figure 7-2 (only 117 V, 60 Hz operation is illustrated; fan connections are not shown). The primary winding of transformer T1 is connected across the ac line. The secondary voltage of T1 is rectified and filtered to produce the LINE LEVEL signal that is proportional to the line voltage. When the ON/OFF switch and the MASTER/SLAVE switch are in the positions shown, relay K1 is not energized. Hence, Line 1 is connected to the primary of the transformer assembly via one of the normally-closed (NC) contacts of K1. If the ON/OFF switch is moved to the OFF position, both the AC OFF L signal and the BATTERY OFF signal are grounded. Current flows through the coil of K1, and the relay contacts move to the normally-open (NO) position. The line voltage is removed from the transformer assembly and the power supply shuts down.

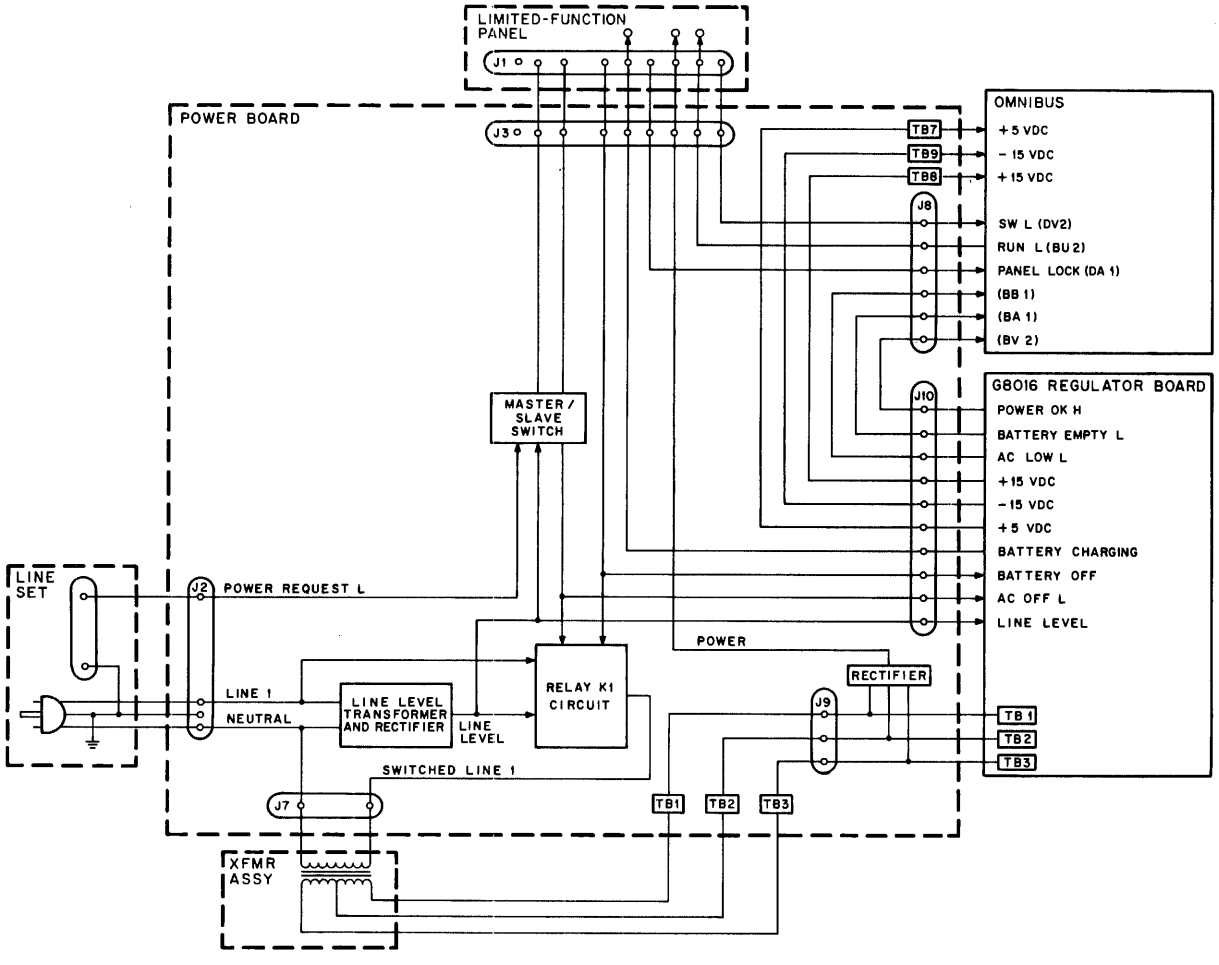


Figure 7-1 Interconnections, PDP-8/A Semiconductor Basic Power Assembly

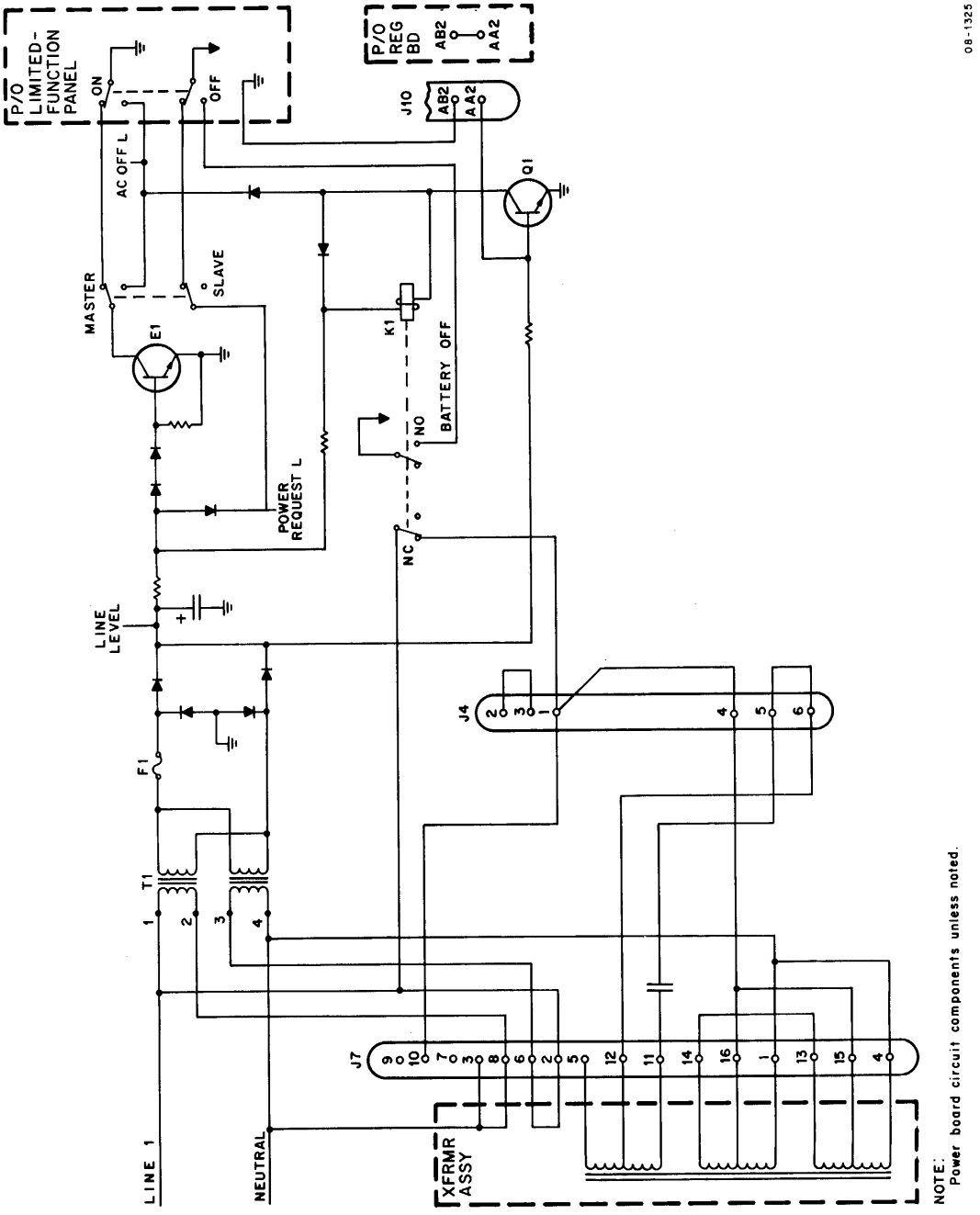


Figure 7-2 Power Board Circuits

If the MASTER/SLAVE switch is in the SLAVE position, K1 is not energized as long as the POWER REQUEST signal is grounded at the remote location. However, if the ground is removed from the POWER REQUEST line, transistor E1 conducts, grounding the AC OFF L signal and energizing the relay (BATTERY OFF is grounded via the relay NO contacts). Once again, the power supply shuts down. Note that when the ON/OFF switch is moved to the OFF position it causes the relay to energize, even though the SLAVE position has been selected.

No matter which switch is used to control line voltage, both AC OFF L and BATTERY OFF are asserted when the line voltage is purposely removed. The first signal, in addition to its relay-related function, causes the AC LOW L signal to be generated, while the second signal prevents the battery supply from operating (if the computer is equipped with a battery). If the line voltage fails, the AC LOW L signal is asserted by the AC LOW L circuit, but BATTERY OFF is not asserted; rather, the +5 V supply begins operating on battery power and does so until either the ac line voltage is restored or the batteries are nearly drained, whichever occurs first (Paragraph 7.2.2.7 relates the AC LOW L signal, battery power, and ac line voltage). If the ac line plug is pulled from the outlet while the switches are still in the ON positions, the supply will go on battery power before shutting off; obviously, one should not remove power in this way.

When the regulator board is not inserted in the power board connectors, transistor Q1 conducts, providing a path for relay coil current; thus, the relay is energized and ac line voltage is not connected to the transformer assembly. Pins AB2 and AA2 on the regulator board are connected; hence, when the board is inserted, pins AB2 and AA2 of J10 are connected and Q1 is turned off.

7.2.2 Regulator Board (G8016)

The G8016 regulator board is built on a quad module; the module can be inserted in pc board connectors mounted on the power board of the H763 assembly. The regulator board provides three dc voltages – +5 Vdc, +15 Vdc, and -15 Vdc. While the ferro-resonant transformer assembly (part of the H763 assembly) provides basic voltage regulation, a series regulator is used to generate the +5 Vdc voltage. The ±15 Vdc voltages are derived from the +5 Vdc circuit by an inverter circuit. The supplies have internal battery backup; automatic shift to battery-powered operation occurs when the ac line voltage falls below a selected level.

Figure 7-3 is a block diagram of the G8016 regulator board. A decision circuit in the +5 Vdc series regulator monitors the output of the ferro-resonant transformer secondary. If the voltage is above a specified level, the regulator operates under ac power; otherwise, battery power is selected.

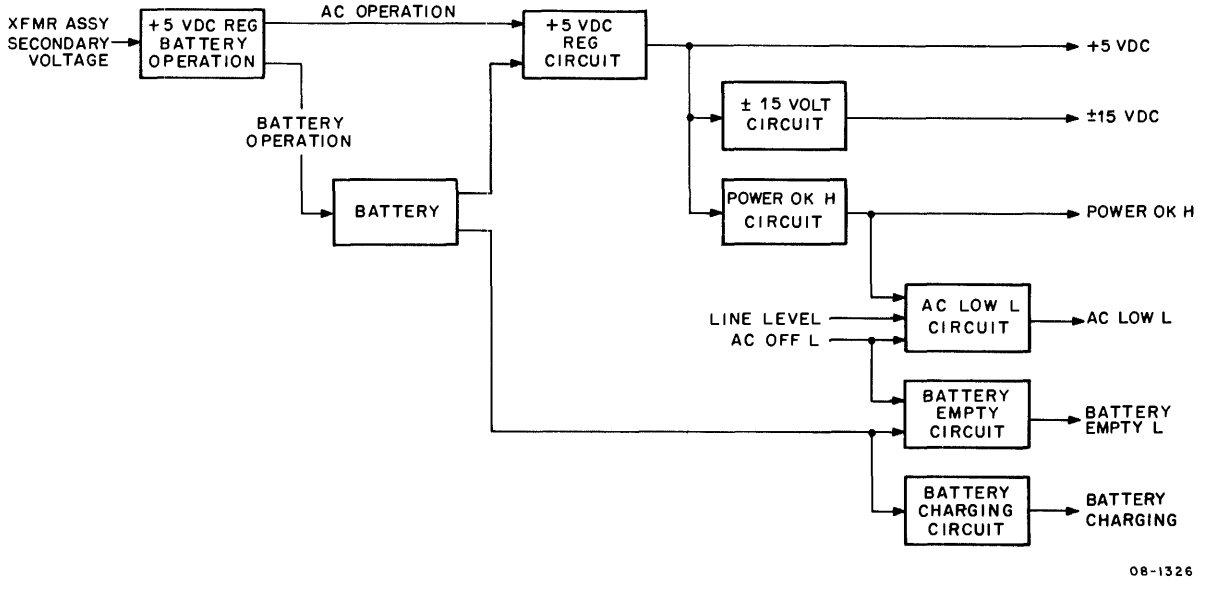


Figure 7-3 G8016 Regulator Block Diagram

The +5 V output is generated by the +5 V regulator circuit. This output is used to generate the 15 V outputs and is monitored by the POWER OK H circuit. As long as the +5 V output remains in regulation (within approximately 50 mV of the adjusted +5 V level), POWER OK H remains high. If the output goes out of regulation, POWER OK H goes low. POWER OK H being negated causes the CPU timing generator to halt and the AC LOW L signal to be asserted.

The AC LOW L circuit, besides responding to POWER OK H, monitors the AC OFF L signal, which is generated when the operator turns off power from a remote location or with the ON/OFF switch, and the LINE LEVEL signal, which is a measure of the ac line voltage.

If the supply shifts to battery-powered operation because of low line voltage, the battery empty circuit might generate the BATTERY EMPTY L signal. This would occur if the supply remains on battery power long enough for the batteries to discharge to a near empty state. The signal causes a program interrupt request to be generated by circuitry on option board 2 (M8317).

If the batteries have been used to operate the supply, they must be re-charged when ac-powered operation is resumed. The battery charging circuit operates in this situation, asserting the BATTERY CHARGING signal until the batteries are re-charged to 90% capacity.

7.2.2.1 +5 Vdc Regulator Circuit – The +5 Vdc regulator circuit is illustrated in Figure 7-4. The output voltage can be adjusted between 4.5 and 5.5 V by potentiometer R33. The supply regulates against line voltage variations and load variations and features both over-current and over-voltage protection. In addition, excessive heat sink temperature causes the circuit breaker, CB1, to open, shutting down the supply.

The rectifier diodes, D1 and D2, supply about +8 V dc to the emitter of the series pass transistor, Q11. This positive voltage allows Q12 to conduct, providing base drive for the pass transistor. Q12 regulates the amount of base drive supplied to Q11 by sampling the output voltage at the collector of Q11. If the output voltage, +5 Vdc, tends to decrease, the voltage at the base of Q15 goes less positive, causing Q15's collector current to decrease. This decrease raises the base potential of Q14, which then conducts less and provides less base current for Q13. Q13 draws less collector current; the base current of Q12 increases accordingly, resulting in increased drive for the pass transistor. The increased base drive reduces the effective series resistance; thus, the collector voltage of Q11 rises to counteract the original drop. If the +5 V output tends to increase, Q13 shunts more current away from the base of Q12, resulting in less base drive for the pass transistor and causing the voltage change to be opposed.

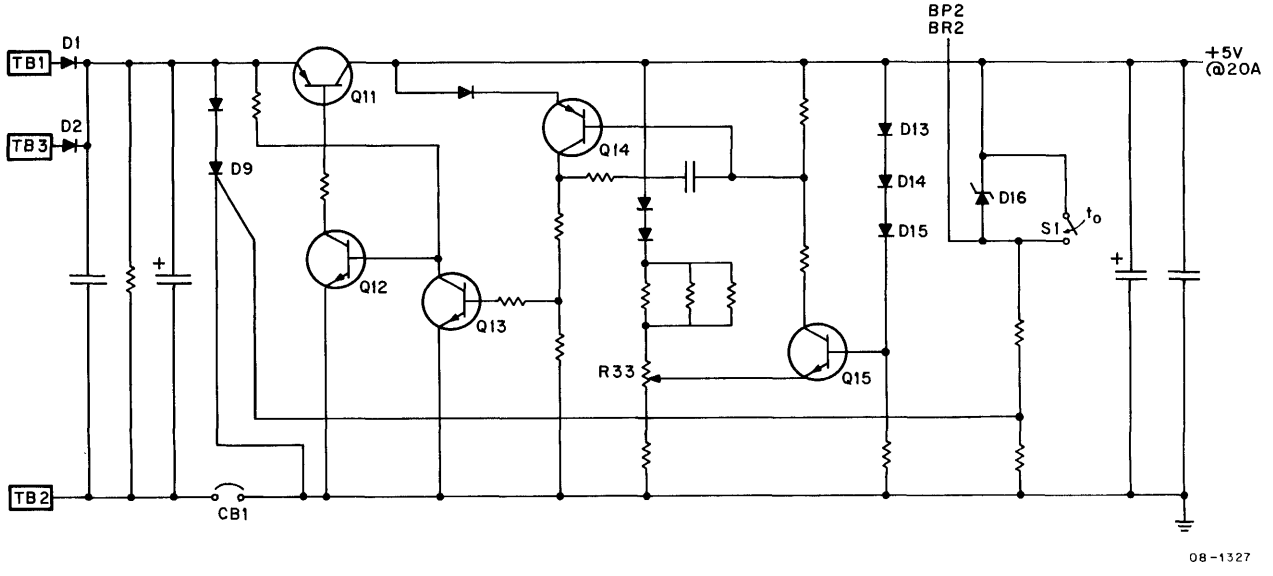


Figure 7-4 +5 Vdc Regulator Circuit

If the output current exceeds 30 ± 2 A, or if the +5 V supply is shorted to ground, CB1 opens, shutting down the supply. Over-voltage protection is provided by the SCR, D9, and Zener diode D16. When the +5 V output rises to between 5.7 and 6.3 V, the Zener diode conducts. The voltage applied to the gate of D9 causes the SCR to fire, shorting the input circuit and causing CB1 to open. Protection against excessive heat sink temperature is carried out in the same way, i.e., the SCR is fired by a gate voltage, causing CB1 to open. If the temperature rises above 230° F (110° C), thermal switch S1 closes, connecting the firing voltage to the SCR. The switch opens when the temperature cools to 194° F (90° C); however, the circuit breaker must be reset manually.

If the regulator board is moved out more than one-eighth of an inch from its full-seated position in the power board connectors, the +5 Vdc voltage is connected to pin BP2. The SCR is fired, opening the circuit breaker and shutting down the supply. Figure 7-5 illustrates part of edge connector B of the regulator board. The dotted lines represent pin BP2 of the power board connector, which is connected to +5 Vdc. As long as the regulator board is properly seated, the two pins do not make contact. If the regulator board is raised (in the arrow direction), BP2 on the regulator board connector makes contact with BP2 on the power board connector.

7.2.2.2 +5 Vdc Regulator Circuit, Battery Operation – Figure 7-6 shows the significant circuit components of the +5 V regulator circuit when that supply is operating with battery power. Transistor Q6 becomes the pass transistor, while control of the base drive for Q6 is effected by Q7 (Q7 and Q9 function analogously to Q12 and Q13 in Figure 7-4).

Battery operation commences when an ac line voltage failure occurs (Paragraph 7.2.2.7 relates battery operation to line failures). Zener diode D3, which conducts during normal ac line voltage operation, opens when the rectified voltage falls below that necessary to sustain conduction. When the diode opens, transistor Q1 stops conducting, removing the ground from the base of Q10 and allowing it to turn on. When Q10 conducts, Q8 also turns on and supplies collector current to Q9. Thus, Q9 can shunt more or less current from the base of Q7, depending on whether the +5 V output tends to increase or decrease, respectively.

The batteries can be damaged if they are allowed to discharge completely; consequently, transistors Q8 and Q10 turn off the supply before the discharge is complete. Q10 is biased so that it turns off when the +5 V output drops out of regulation due to a dying battery; Q8 does likewise, causing Q7 to do the same. Thus, the pass transistor stops conducting and the batteries cease to drain. The supply remains inactive until ac power is restored.

Battery operation of the supply must not begin when the ac power is turned off by the operator. The BATTERY OFF signal, grounded by the Limited Function Panel ON/OFF switch or by the power board relay, K1, is applied to the base of Q7. This ground ensures that both Q7 and Q6 remain non-conducting; thus, the batteries do not drain through Q6.

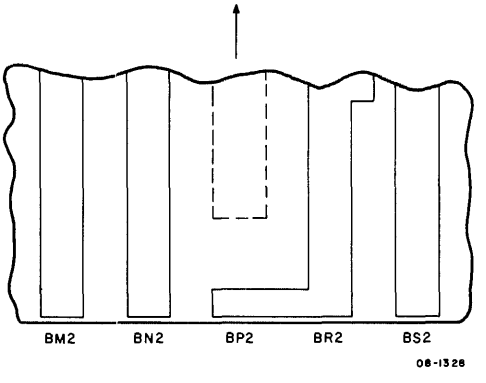


Figure 7-5 Regulator Board Edge Connector

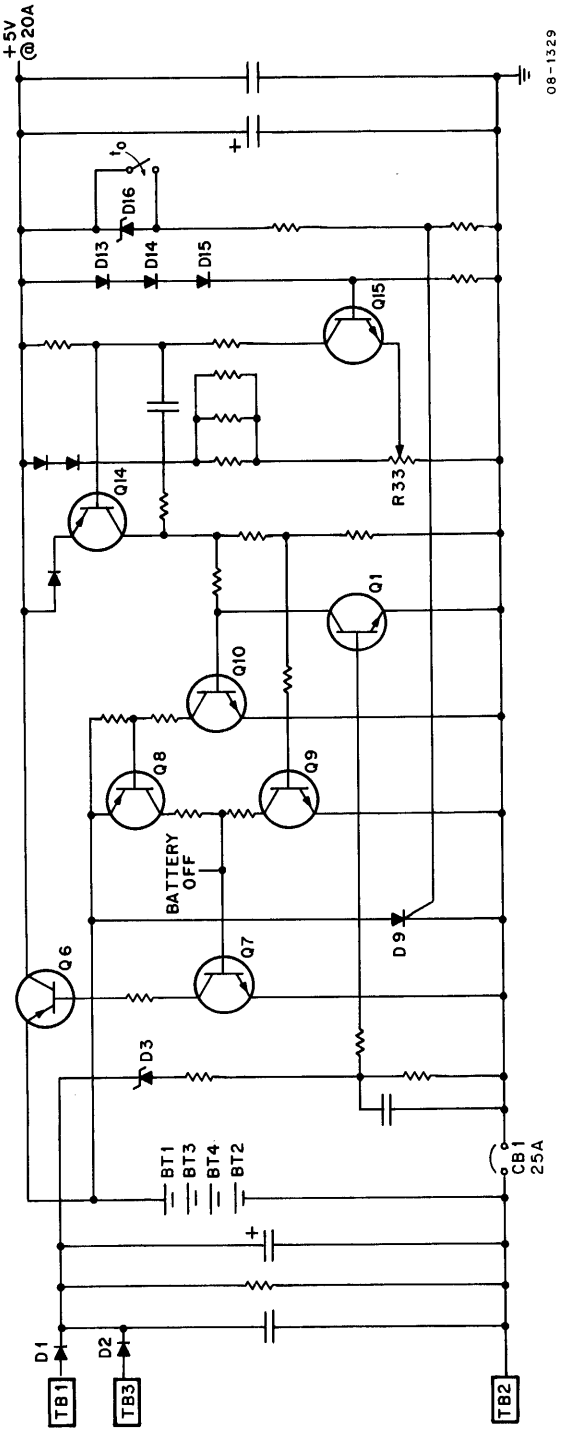


Figure 7-6 +5 Vdc Regulator Circuit, Battery Operation

7.2.2.3 Battery Empty Circuit – If the ac line voltage drops below a specified value, battery-powered operation begins. The batteries can sustain operation for a limited period of time; when this period is about to expire, the BATTERY EMPTY L signal is asserted. Interrupt logic on option board 2 generates an interrupt request and a program subroutine is entered to prepare for the imminent power shutdown. The battery empty circuit is shown in Figure 7-7.

Transistor Q18 measures the voltage across the battery series pass transistor Q6. As long as Q6 is not in saturation Q18 will conduct. When Q6 nears saturation (indicating battery failure is imminent) Q18 stops conducting and causes BATTERY EMPTY L to be asserted.

When the +5 V supply is in regulation, a positive voltage on the base of Q19 causes it to conduct. The base of Q17 becomes more positive and Q17 conducts, allowing Q16 to turn on (Q16 turns off when there is no +5 V, preventing discharge of the battery). The voltage present at the emitter of Q6 is applied through Q16 to the emitter of Q18. The base of Q18 is connected directly to the collector of Q6; thus, the emitter-base bias of Q18 is dependent upon the voltage across Q6, the battery regulator transistor. The values of resistors R42 and R43 are chosen so that as long as Q6 is not in saturation, Q18 will conduct. This will keep the base of Q20 positive, and Q20 will conduct, preventing the BATTERY EMPTY L signal from being asserted. When Q6 nears saturation, indicating the battery is nearly exhausted, Q18 will no longer have enough base current to conduct. When Q18 stops conducting so, too, will Q20; BATTERY EMPTY L will be asserted.

BATTERY EMPTY L is asserted immediately when the ON/OFF switch is turned to the OFF position, due to the AC OFF L input at the base of Q19. This input causes Q19, Q17, and Q16 to stop conducting, turning off Q18, and asserting BATTERY EMPTY L.

7.2.2.4 Battery Charging Circuit – The battery charging circuit is shown in Figure 7-8. The batteries are charged, if necessary, when ac power is applied after having been turned off for some reason. When the voltage supplied by the rectifier diodes, D1 and D2, reaches a level that is sufficient to cause Zener diode D3 to conduct, transistor Q5 turns on and draws current from the differential amplifier Q3/ Q4. The differential amplifier controls transistor Q2, which supplies charging current to the batteries through diode D4.

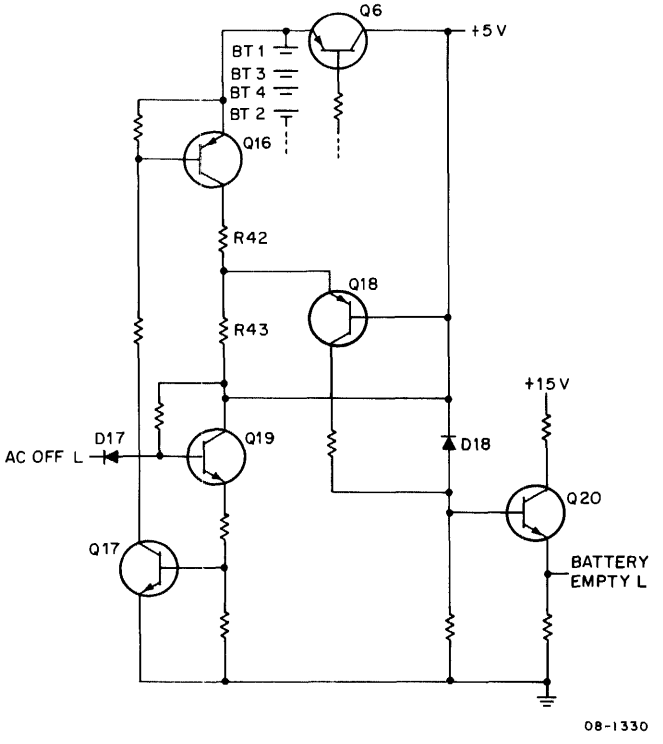


Figure 7-7 Battery Empty Circuit

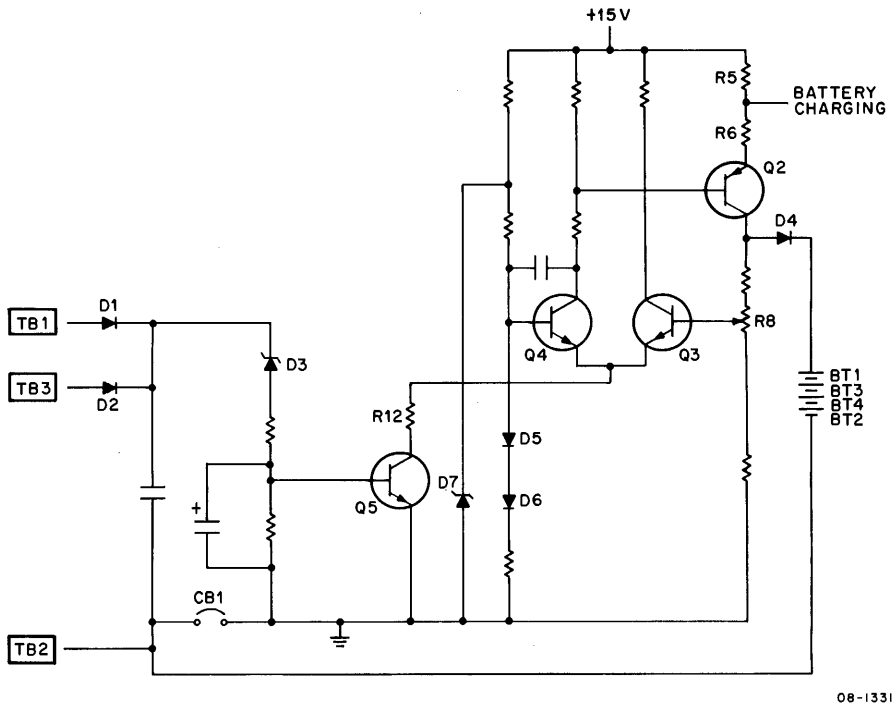


Figure 7-8 Battery Charging Circuit

The base of Q4 is held at a temperature variable reference voltage of approximately +2.4 V by Zener diode D7. Potentiometer R8 is adjusted so that the base of Q3 is at +2.4 V when the batteries are fully charged to +9.4 V. If the batteries need to be charged, the base of Q3 will be something less than +2.4 V; hence, Q4 conducts more heavily than Q3, lowering the base voltage of Q2. Q2 supplies charging current to the batteries until they are charged to the +9.4 V level. As the batteries are charging to this level, the differential amplifier is approaching the balanced state; Q4 is conducting less, Q3 is conducting more, and the base voltage of Q2 is increasing. At the equilibrium condition, Q2 supplies only enough current to maintain the condition of Q3; thus, the batteries stop charging. Diode D4 prevents the batteries from discharging through R8 to ground when the supply is turned off.

7.2.2.5 ±15 Vdc Circuit – The ±15 V supply, shown in Figure 7-9, is an inverter circuit that is driven by the +5 V regulated output voltage. The +5 V output is applied to the center tap of T1 and to the base of both Q26 and Q27. When the power is turned on and the +5 V output approaches its operating level, one of the two transistors will turn on before the other. If we assume that Q26 begins conducting first, then current begins to flow through the primary winding from pin 2 to pin 1. The magnetic field generated in the core induces a voltage in the feedback winding (pins 4-5). This induced voltage is of a polarity that supports the conduction of Q26, while ensuring that Q27 remains non-conducting. When the transformer saturates, the field in the feedback winding changes polarity, causing Q26 to turn off and Q27 to turn on. The current flowing in the primary from pin 2 to pin 3 induces a voltage in the feedback winding that supports the conduction of Q27. Once again, the field reverses when the transformer saturates; Q27 turns off and Q26 turns on. The transistors alternate in the on/off cycle as long as +5 V is applied to L1.

Each half of the secondary of T1 contains about three times the number of turns as does each primary winding. Consequently, each half of the secondary winding will have an alternating voltage of about 15 V induced in it. This alternating voltage is rectified to produce the ±15 Vdc supply voltages.

7.2.2.6 POWER OK H Circuit – The POWER OK H circuit (Figure 7-10) monitors the +5 Vdc regulated voltage, asserting the POWER OK H signal as long as the voltage remains in regulation. If the +5 Vdc output deteriorates, Q24 turns on, bringing POWER OK H near ground.

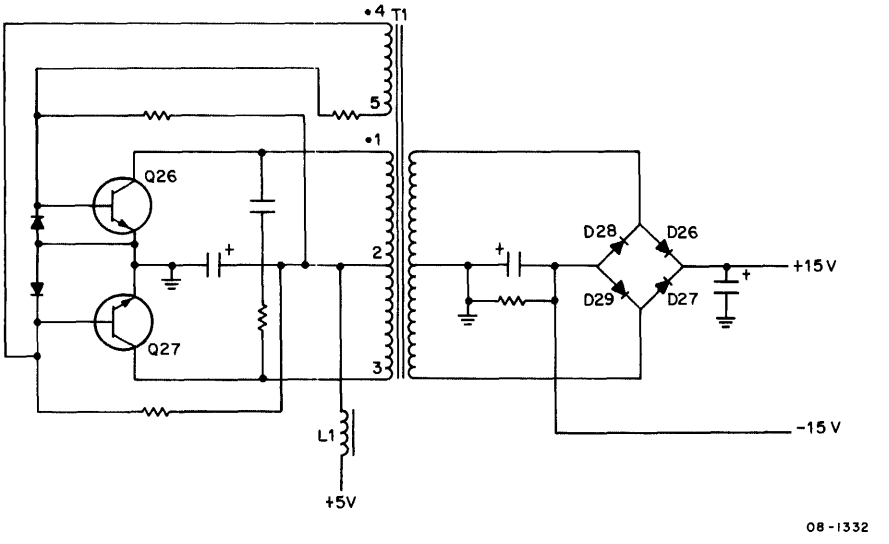


Figure 7-9 ±15 Vdc Power Supply

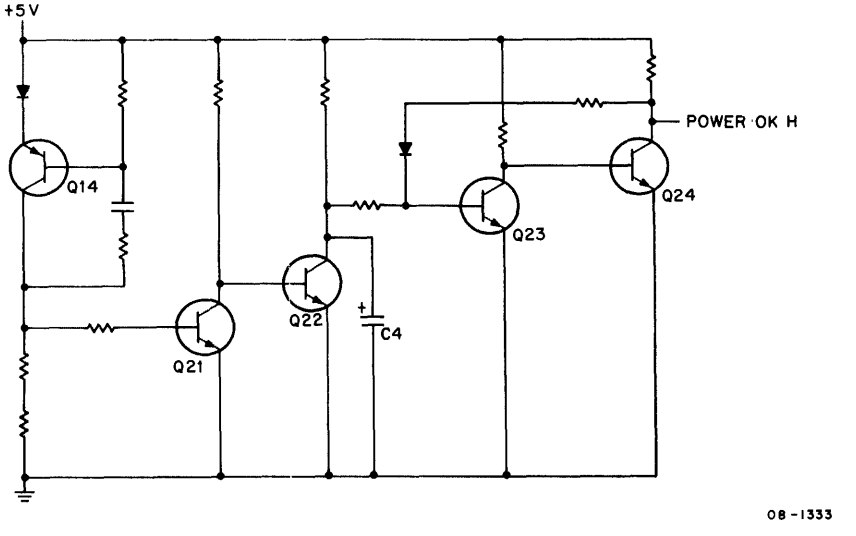


Figure 7-10 POWER OK L Circuit

When the supply is energized and the +5 Vdc voltage is present and in regulation, the collector of Q14 will be between 1.2 and 1.4 V. This voltage is applied to the base of Q21, causing it to conduct. Q22 does not conduct; thus, capacitor C4 charges to 15 V. 300 to 400 ms are required for C4 to charge to a value sufficient to allow Q23 to turn on. When Q23 conducts, Q24 turns off, allowing the POWER OK H signal to be asserted. This positive voltage feeds through D19 to capacitor C4, causing it to complete charging rapidly to prevent spikes on the POWER OK H signal.

If the input to the +5 V regulator drops below that required to maintain regulation, the collector of transistor Q14 will drop rapidly below 1 V. This will result in C4 discharging through Q22, turning off Q23 and causing Q24 to ground the POWER OK H signal.

7.2.2.7 AC LOW L Circuit – The AC LOW L circuit is shown in Figure 7-11. When the ac line voltage drops below a predetermined value, the AC LOW L signal is asserted. Interrupt logic on option board 2 uses the AC LOW L signal to generate a program interrupt. The program will test for the AC LOW L condition and proceed to a subroutine designed to handle the situation.

E1 is a differential amplifier that controls transistor Q25. Pin 3 of E1 is held at a reference voltage by Zener diode D22, while pin 2 is supplied with a voltage that is proportional to the ac line voltage. If the line voltage drops below 95 V (this level is determined by the setting of potentiometer R60), the LINE LEVEL signal causes the voltage at pin 2 of E1 to drop below that of pin 3. The output at pin 6 goes positive, turning on Q25 and grounding the AC LOW L signal.

If the line voltage begins to rise after a momentary failure, it must rise to some value higher than 95 V before pin 2 reaches a voltage sufficient to cause pin 6 to go low. This is because the resistance from pin 2 to ground is lowered when the AC LOW L signal is asserted. The level to which the line voltage must rise (105 V for a 117 V system) is set by potentiometer R63; when this level is reached, pin 6 goes low, turning off Q25 and negating AC LOW L.

Figure 7-12 shows a waveform that represents the RMS value of the ac line voltage as it might appear during a period of instability. When the RMS value drops below 95 V, the AC LOW L signal is asserted. If the voltage returns to 105 V, AC LOW L is negated. This minimum line voltage at which the supply will operate depends on the load requirements. When this minimum is reached, the supply begins to operate under battery power. The batteries support the supply for a period of time that also depends on load requirement (Figure 7-13 relates both minimum line voltage and battery support time to percent of full rated load).

Figure 7-12 illustrates the situation when the supply operates at 75% rated load. AC LOW L is asserted when the RMS line voltage drops below 95 V. When this happens, an interrupt request will be generated by option board 2, and a program subroutine will examine the situation. If the BATTERY EMPTY L signal is asserted while the AC LOW L signal is low, another interrupt request is generated; a program subroutine will prepare for the imminent power shut-down. However, if AC LOW L is negated without BATTERY EMPTY L having been asserted (i.e., either battery power did not cut in or the batteries did not discharge to the warning point), the system can return to normal operation.

When BATTERY EMPTY L is asserted, the supply can continue to operate on battery power for at least 1 ms. Then, the +5 Vdc output will drop out of regulation, the POWER OK H signal will be negated, and a power shut-down will follow. When ac power returns, the supply again operates, the batteries begin to charge, and POWER OK H is asserted. If the line voltage returns above 105 V, normal operation resumes.

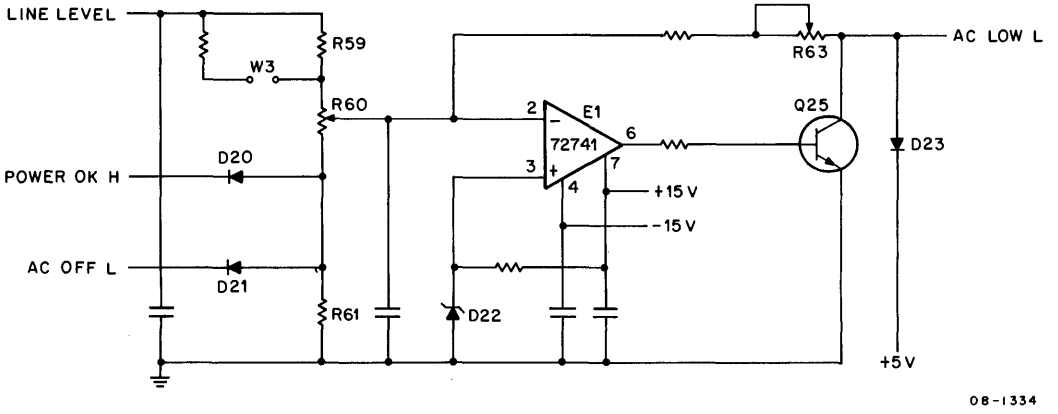


Figure 7-11 AC LOW L Circuit

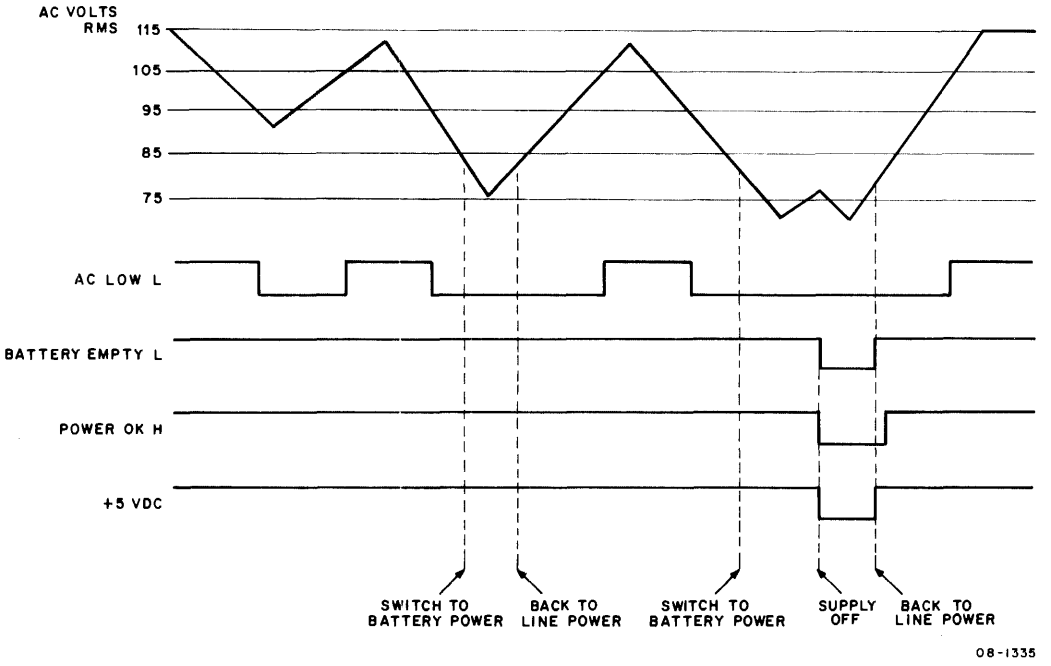


Figure 7-12 Voltage Monitor Waveforms

7.3 8A400/600/800 BASIC POWER ASSEMBLY

The basic power assembly for the 8A400/600/ and 800 computers consists of the H9194 Connector Block Assembly (the Omnibus), the G8018 Regulator board, a transformer assembly, a line set, and a Limited Function Panel.

Figure 7-14 illustrates the assembly interconnections. The Limited Function Panel has been discussed in Paragraph 4.3.1; the connector block assembly is described in Paragraph 7.3.1, the regulator board in Paragraph 7.3.2.

7.3.1 H9194 Connector Block Assembly

The Connector Block assembly circuits are shown in Figure 7-15 (only 117 V, 60 Hz operation is illustrated; fan connections are not shown). The primary winding of transformer T1 is rectified to produce the AC LEVEL signal that is used in the G8018 board POWER OK H circuit. This same secondary voltage is rectified and filtered, producing the LINE LEVEL signal, a dc level that is proportional to the ac line voltage amplitude.

When the ON/OFF switch and the MASTER/SLAVE switch are in the positions shown, relay K1 is not energized. Hence, the ac line is connected across each of the two primary windings of the transformer assembly via the normally-closed (NC) contacts of K1. If the ON/OFF switch is moved to the OFF position both the AC OFF L signal and the BATTERY OFF signal are grounded. Current flows through the coil of K1, and the relay contacts move to the normally-open (NO) position. The line voltage is removed from the transformer assembly and the power supply shuts down.

If the MASTER/SLAVE switch is in the SLAVE position, K1 is not energized as long as the POWER REQUEST signal is grounded at the remote location. However, if the ground is removed from the POWER REQUEST line, transistor E1 on the Limited Function Panel conducts, grounding the AC OFF L signal and energizing the relay. (BATTERY OFF L is grounded via the relay NO contacts). Once again, the power supply shuts down. Note that when the ON/OFF switch is moved to the OFF position, it causes the relay to energize even though the SLAVE position has been selected. No matter which switch is used to control line voltage, both AC OFF L and BATTERY OFF L are asserted when the line voltage is purposely removed. BATTERY OFF L causes the AC LOW L signal to be generated. If the line voltage fails, the AC LOW L signal is asserted in the AC LOW L circuit, but BATTERY OFF L is not asserted.

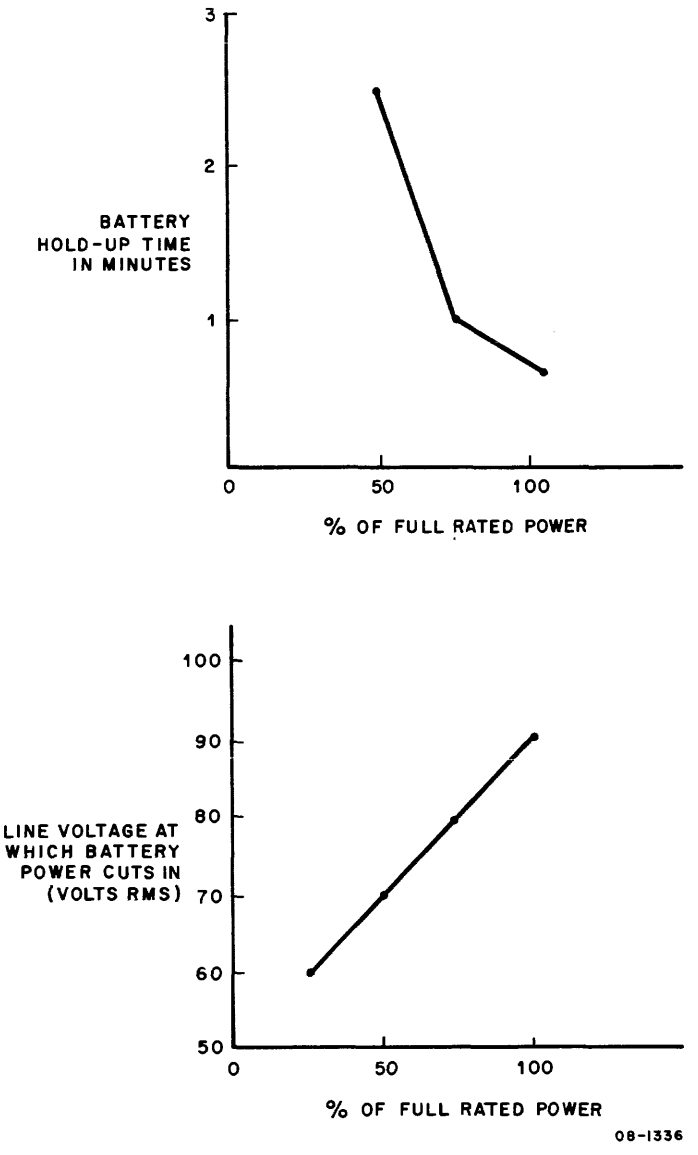


Figure 7-13 Battery Hold-up Time, Minimum Line Voltage vs% of Full-Rated Load

When the regulator board is not inserted in the connector block assembly, transistor E1A conducts, providing a path for relay coil current; thus, the relay is energized and ac line voltage is not connected to the transformer assembly. Pins AB2 and AA2 on the regulator board are connected; hence, when the board is inserted, pins AB2 and AA2 of J7 are connected and E1A is turned off.

The regulator board is protected from the effects of excessive temperature. Such temperature causes the thermostat to activate the emergency shut-down circuit. The thermostat switch t(0), on the regulator board closes when high temperature is detected. The LINE LEVEL signal applied to the base of E1C and E1B causes both transistors to conduct; relay K1 closes and the EMERGENCY SHUTDOWN L signal is generated, notifying the remote power control location of the shutdown.

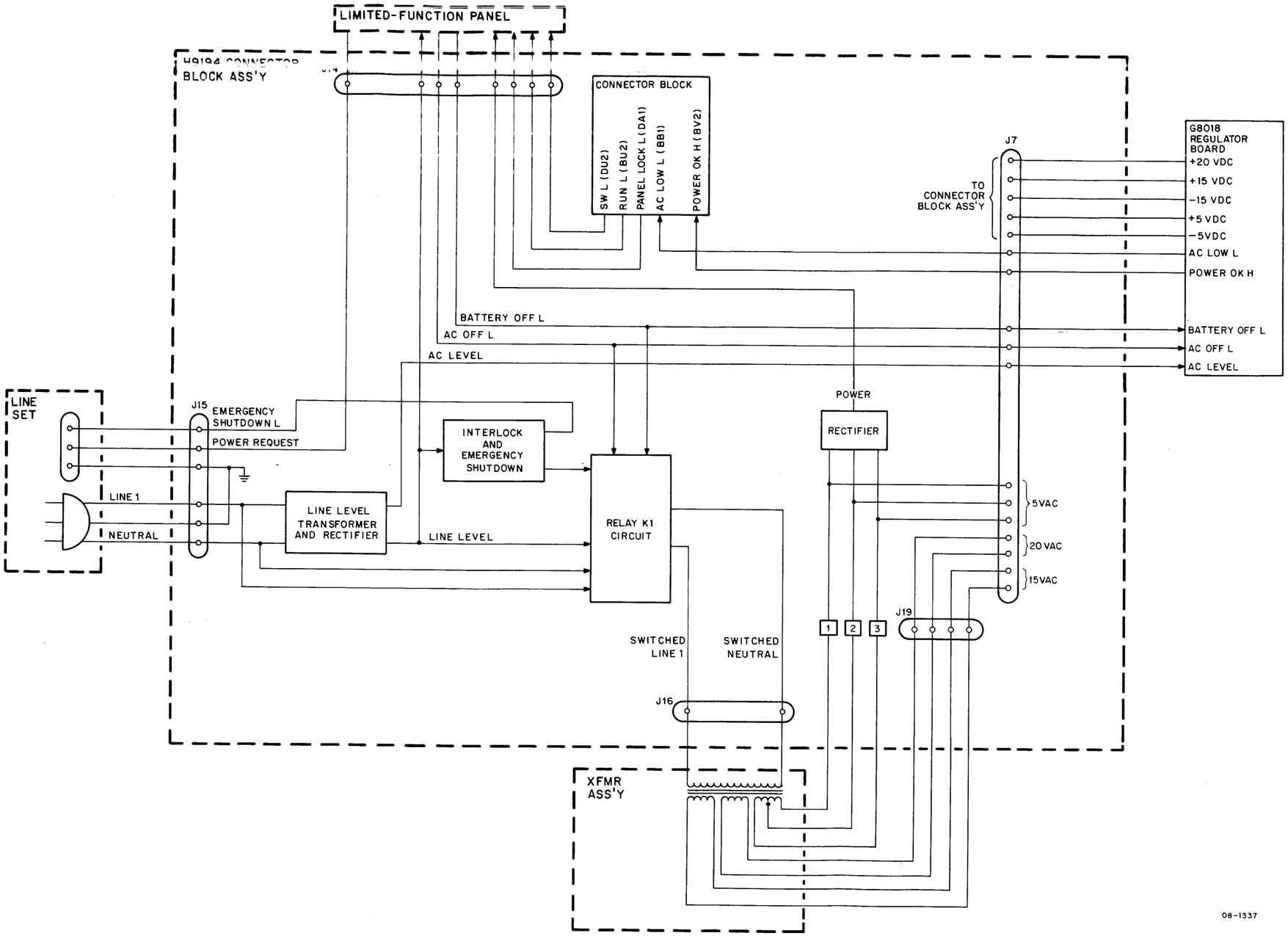


Figure 7-14 Interconnections, 8A400/600/800 Basic Power Assembly

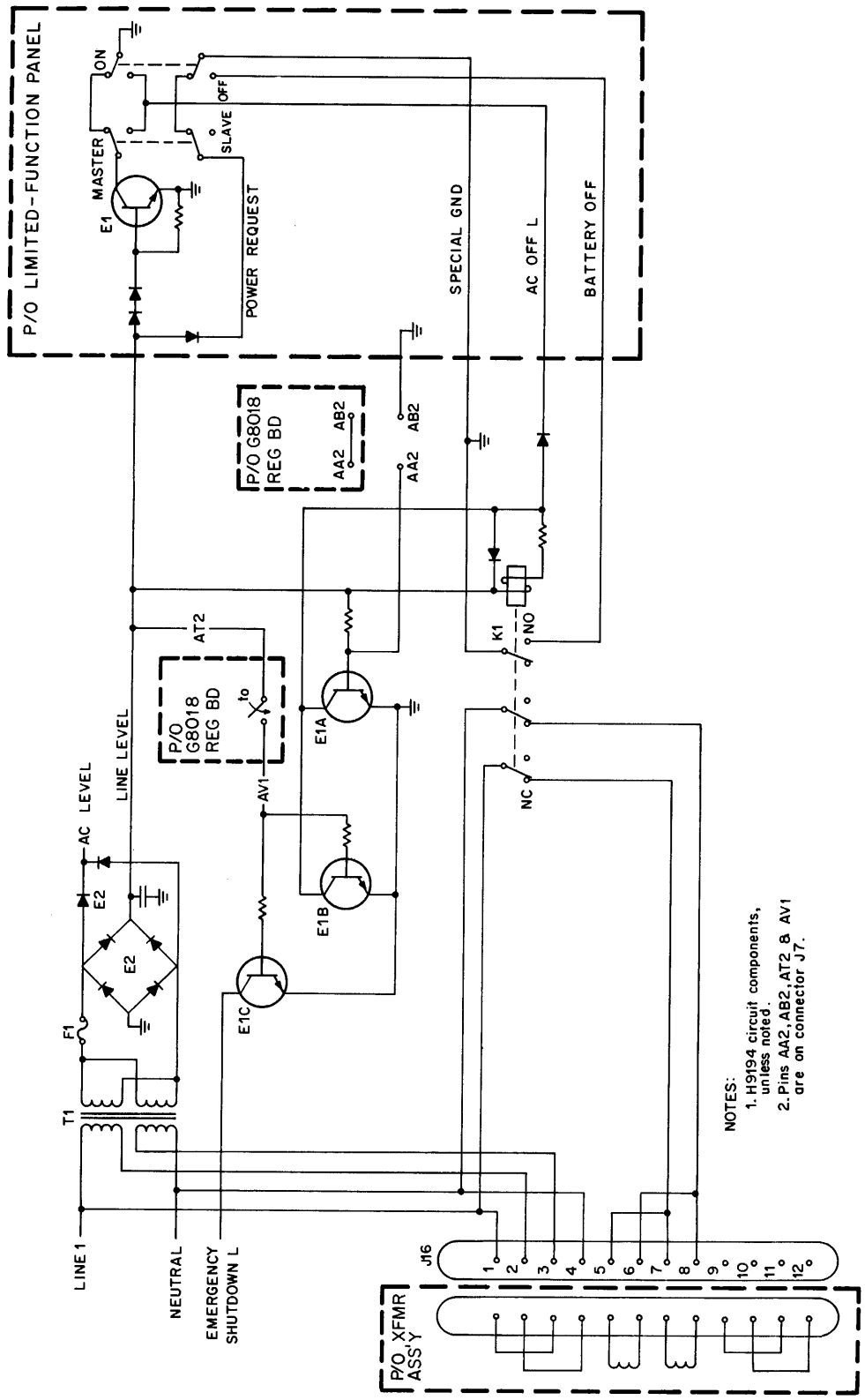


Figure 7-15 Connector Block Assembly Circuits

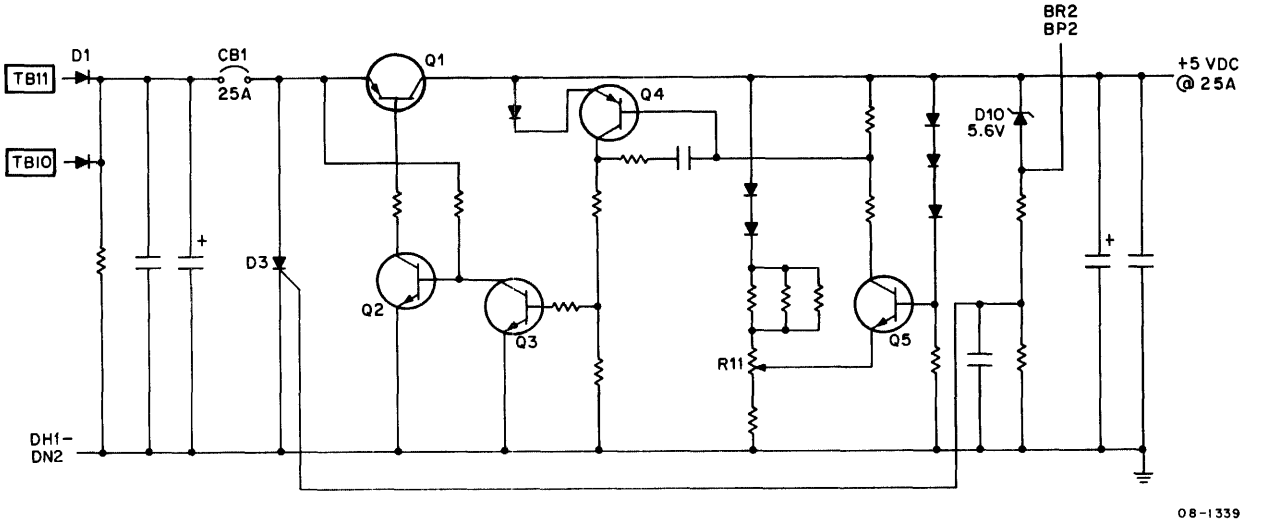


Figure 7-16 +5 Vdc Regulator Circuit

7.3.2 Regulator Board (G8018)

The G8018 regulator board provides dc voltages of +5 V, -5 V, +20 v, +15 V, and -15 V. Like the G8016, the G8018 has ac and dc voltage monitoring circuits that help to protect the operating program against voltage disturbances.

7.3.2.1 +5 Vdc Regulator Circuit – The +5 Vdc regulator circuit is shown in Figure 7-16. Except for the component designations and the position of the circuit breaker, the circuit is identical to the +5 Vdc regulator circuit on the G8016 board. Refer to Paragraph 7.2.2.1 for a description of the circuit operation.

7.3.2.2 -5 Vdc Regulator Circuit – Figure 7-17 illustrates the -5 Vdc regulator circuit. The circuit is a simple series regulator incorporating an operational amplifier in the voltage feedback path. The inverting input of the operational amplifier, E5, is connected to a voltage divider comprising precision resistors R32, R33, and R34. If the -5 Vdc output tends to vary relative to the +5 Vdc supply voltage, the operational amplifier output causes transistor Q20 to draw more or less base current from the pass transistor, Q8; thus, the pass transistor acts to force the output back to its equilibrium value.

The -5 Vdc circuit has no adjustment. The potentiometer in the +5 Vdc regulator circuit permits both supplies to be adjusted at the same time, the -5 Vdc output tracking the +5 Vdc output.

7.3.2.3 +20 Vdc Regulator Circuit – Figure 7-18 shows the +20 Vdc regulator circuit. A precision voltage regulator, E1, provides series regulation of the output voltage. E1 consists of a temperature-compensated reference amplifier, an error amplifier, a power series pass transistor, and current-limit circuitry. Pass transistor Q6 is included in the circuit to handle the current that exceeds the 150 mA capability of E1.

The +20 Vdc output is sampled by the voltage adjustment potentiometer, R22, and compared to the internally-generated reference voltage by E1. Any error voltage produced because of a change in the sampled output is amplified and applied to the internal pass transistor, which controls the base current of Q6. Thus, Q6 varies its degree of conduction to maintain the output voltage at a constant value.

The power resistor, R20, is connected to the current-limit circuitry of E1 to protect the internal pass transistor if the regulator output terminals are shorted. Zener diode D12 shorts the regulator input to ground, causing F1 to burn out, if the output voltage rises above approximately 22 Vdc.

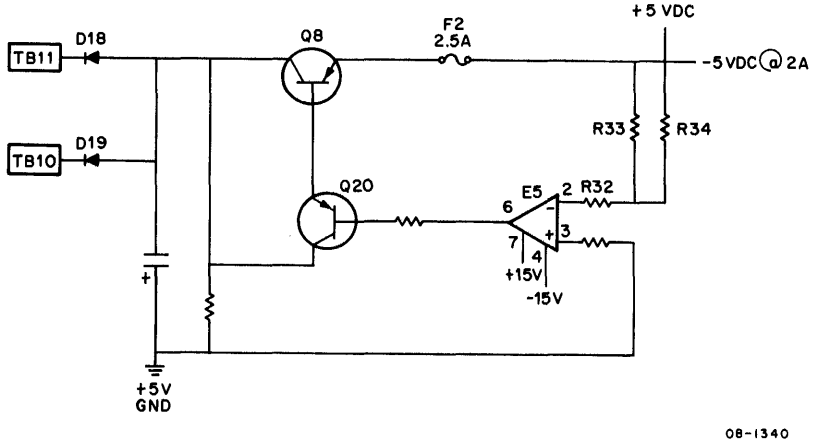


Figure 7-17 -5 Vdc Regulator Circuit

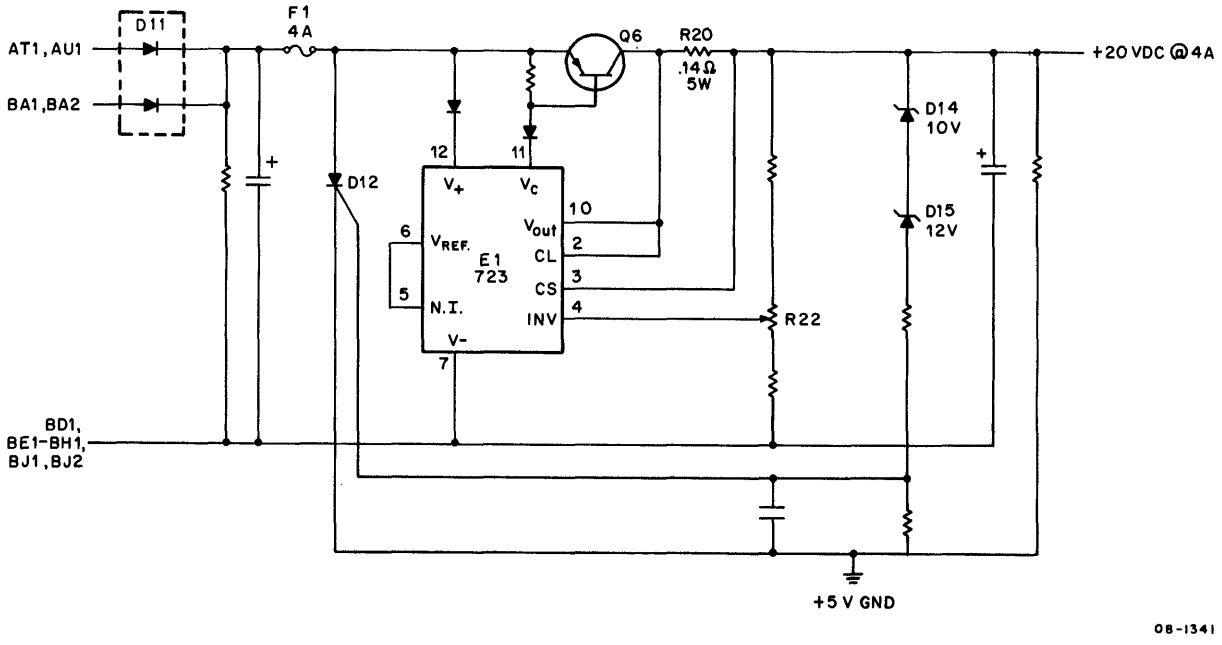


Figure 7-18 +20 Vdc Regulator Circuit

7.3.2.4 ±15 Vdc Circuit – The ±15 Vdc outputs are unregulated and are derived from a bridge rectifier, D16, illustrated in Figure 7-19. After being filtered, each voltage is referenced to +5 Vdc ground before being applied to the connector block assembly.

7.3.2.5 POWER OK H Circuit – The POWER OK H circuit (Figure 7-20) monitors the dc voltages, negating the POWER OK H signal whenever one or more voltages falls below a minimum value. When all dc voltages are at a satisfactory level, transistor Q16 conducts and LED D25 is illuminated. If a voltage deteriorates, Q15 turns on heavily, negating POWER OK H and turning off Q16.

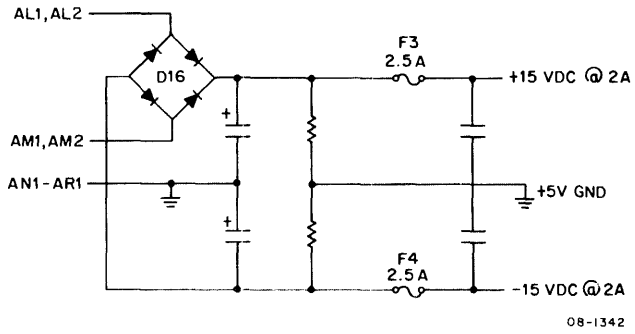


Figure 7-19 ±15 Vdc Circuit

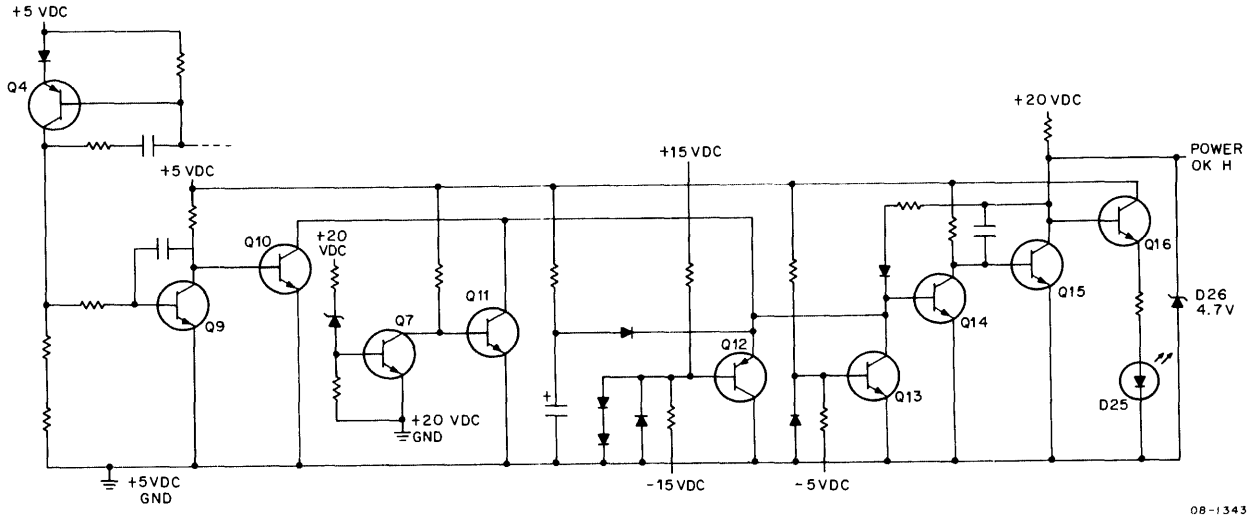


Figure 7-20 POWER OK H Circuit

If the +5 Vdc regulated voltage goes out of regulation, the collector of Q4 drops much more rapidly than does the +5 V output itself. Thus, the collector voltage of Q4 is monitored directly to provide faster response when the +5 Vdc output decreases. In such a situation, Q15 is turned on via a path that includes transistors Q9, Q10, and Q14.

The +20 Vdc output is monitored at the base of transistor Q7. When the base voltage drops because of a decrease in the +20 Vdc output, Q7 turns off, resulting in Q15 turning on and negating POWER OK H.

The +15 Vdc output is measured at the base of Q12. If the +15 Vdc voltage goes low, Q12 turns on, again resulting in Q15 turning on the POWER OK H signal near ground. The -15 Vdc output is monitored to bring indirectly. Since -15 Vdc is used by the voltage regulator integrated circuit in the -5 Vdc regulator circuit (Figure 7-17), a drop in the -15 Vdc output will affect the -5 Vdc output in the same way. Thus, Q13 turns on, resulting in POWER OK H being negated.

7.3.2.6 AC LOW L Circuit – The AC LOW L circuit is shown in Figure 7-21. The circuit asserts the AC LOW L signal in three situations: The ac line voltage drops below a predetermined value; the ON/OFF switch is turned to OFF, or the POWER REQUEST signal is negated; a dc voltage falls below a specified level. The AC LOW L signal is used in option board 2 to generate a program interrupt request and to initiate automatic program re-start when ac power is restored aftera failure.

The AC LEVEL signal (Figure 7-21) is proportional to the ac line voltage. The signal is applied through potentiometer R49 to the inverting input of an operational amplifier whose non-inverting input is held at a reference level by Zener diode D27. When pin 2 of E2 goes below the level of pin 3, output pin 6 goes positive. The situation is represented in Figure 7-22.

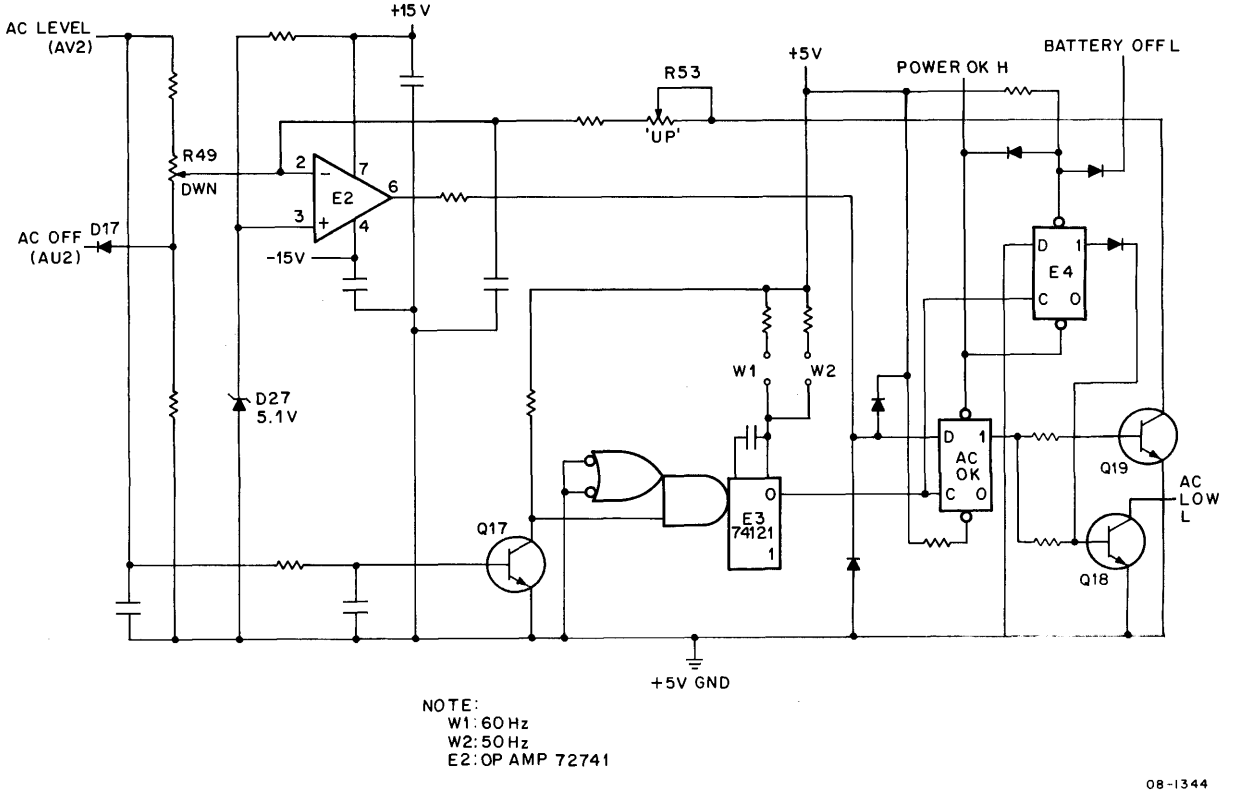


Figure 7-21 AC LOW L Circuit

The AC LEVEL signal is also applied to the base of transistor Q17, which turns off at the 0-crossing of the ac line voltage. When Q17 turns off, one-shot E3 is triggered on, remaining on for approximately 4 ms (60 Hz operation). When E3 turns off, the AC OK flip-flop is clocked. If the flip-flop's D-input is high when E3 turns off, the flip-flop is set, causing Q18 to assert the AC LOW L signal. When the line voltage rises after having fallen below the desired minimum (95 V in the 117 V system), it must rise to a level higher than this minimum due to the hysteresis effect produced by transistor Q19. If this higher level (105 V in the 117 V system) is exceeded, AC LOW L is negated and normal operation resumes.

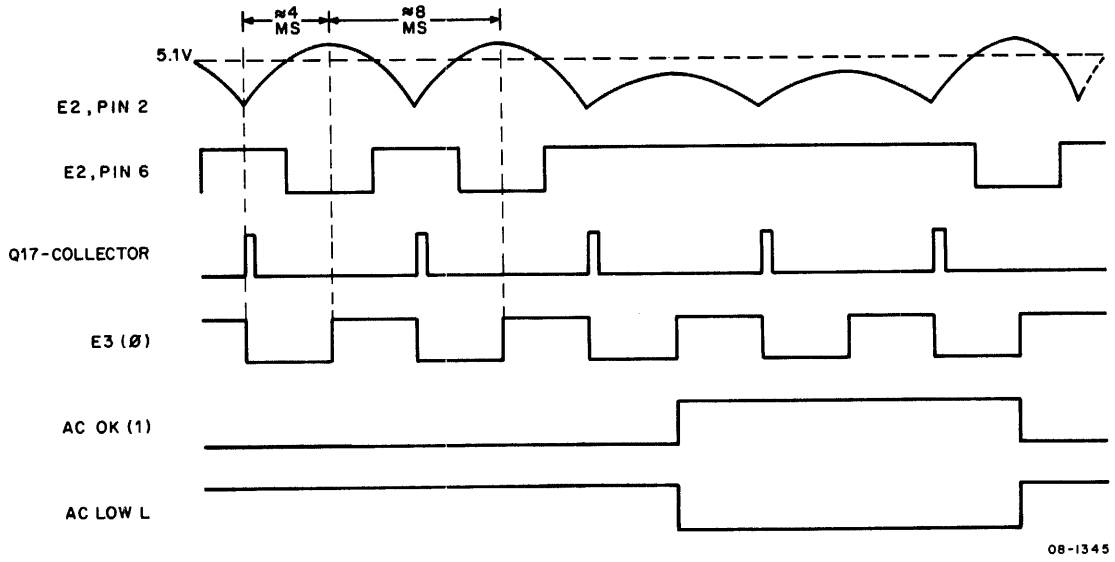


Figure 7-22 Timing, AC LOW L Circuit (60 Hz Operation)

7.4 8A420/620/820 BASIC POWER ASSEMBLY

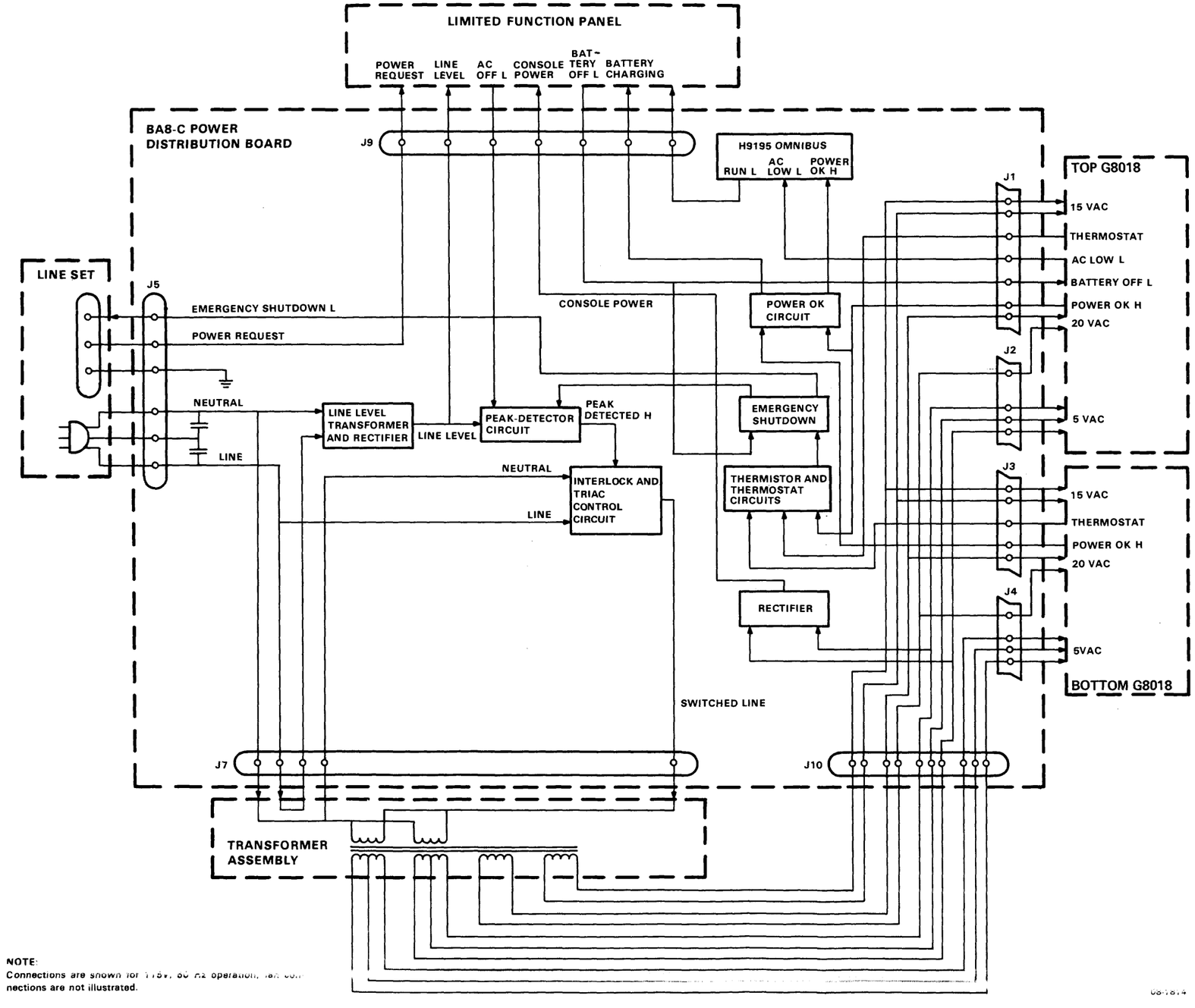
The basic power assembly for the 8A420/620/820 computers consists of the H9195 Omnibus, the 5412000 Power Distribution Board assembly, two G8018 Regulators, a transformer assembly, a line set, and a Limited Function Panel. Figure 7-23 illustrates the assembly interconnections. The 5412000 Power Distribution Board circuits are discussed in the balance of this paragraph. See Paragraphs 4.3.1 and 7.3.2, respectively, for descriptions of the Limited Function Panel and the G8018 Regulator Board circuits.

7.4.1 General

The Power Distribution Board features circuits that are designed to hold inrush current at power turn-on to a relatively low level (approximately 50 A). First, a Triac is included in the ac line to switch the line connection to the primary of the power transformer. Second, a voltage peak-detector circuit permits the Triac to switch on the ac line only when the inrush current is near its minimum value. Thus, the inrush current is reduced significantly from the values that would be observed with conventional relay-switching circuits.

Included on the Power Distribution Board are heat-sensing networks that operate with an emergency shutdown circuit; this combination turns off power when excessive temperature is detected on either G8018 regulator board or when any one of three fans is not providing sufficient cooling air to the chassis interior.

Another monitor circuit checks the POWER OK H signal from each G8018 regulator board. When both signals are asserted the circuit causes the POWER OK indicator on the Limited Function Panel to light, and POWER OK H on the Omnibus to go high.



NOTE:
Connections are shown for 115V, 60 Hz operation; 1ø. 50... nections are not illustrated.

Figure 7-23 Interconnections, 8A420/620/820 Basic Power Assembly

7.4.2 Interlock and Triac Control Circuit

Figure 7-24 shows the interlock scheme and illustrates the Triac control circuit. The Triac, D4, is in series with the LINE connection of the power transformer primary. The gate of the Triac (connected to TB2) is controlled by the Darlington-amplifier pair Q1/Q2. Q2 is an opto-coupled isolator that is turned on when the Peak Detector circuit generates the PEAK DETECTED H signal. This signal is generated when the input voltage is near its peak value; because there is a 90° phase difference between voltage and current in the power transformer ferro-resonant core, the peak value of voltage corresponds to the 0-value of current. Thus, PEAK DETECTED H is generated when the inrush current is near its minimum value. The diode portion of Q2 conducts, provided both G8018 boards, the fan harness, and the Limited Function Panel are in place. The transistor portion of Q2 is turned on by the emission from the diode; Q1 turns on, supplying gate current for the Triac, which conducts and, hence, connects the LINE to one side of the power transformer.

7.4.3 Line Level Transformer and Peak Detector

Figure 7-25 shows the Line Level transformer and the Peak Detector circuit. The line voltage is rectified to produce the LINE LEVEL signal. This signal is filtered and divided to produce a reference voltage at the base of Q4D. The non-filtered LINE LEVEL signal is applied to the base of Q4C. When the base of Q4C rises above the reference voltage, Q4C conducts, providing base current for Q5. When Q5 turns on, PEAK DETECTED H is asserted and the Triac control circuit connects the ac line to the power transformer.

If the ON/OFF switch on the Limited Function Panel is moved to the OFF position, AC OFF L is asserted, turning off Q4C; thus, PEAK DETECTED H is negated. The Triac stops conducting and line voltage is removed from the power transformer.

If the Emergency Shutdown circuit (Paragraph 7.4.4) should activate, transistor Q7 turns on and current flows in the relay coil. Hence, Q4A and Q6 turn on, removing the emitter-base forward bias from Q5; Q5 turns off, negating PEAK DETECTED H.

7.4.4 Thermistor/Thermostat and Emergency Shutdown

The circuits shown in Figure 7-26 produce an emergency shutdown of power when excessive heat is detected. Transistor Q4B is turned on if the thermostat on either or both G8018 boards activates or if one or more of the thermistors in the fan assembly overheats. Then, Q7 turns on and current passes through the coil of relay K1; the relay contact closure causes the EMERGENCY SHUTDOWN L signal to be generated.

As Figure 7-26 indicates, there are three thermistors in the fan assembly. They are mounted so that each receives cooling air from one of the fans. If the fans are providing a sufficient flow of air, the temperature of each thermistor is of such a value that V_{th} is less than V_{ref}. Thus, the output (at pin 2, pin 1, and pin 14) of each comparator of E1 is connected to ground and Q4B does not conduct (assuming that each thermostat remains inactive).

However, if the flow of air from one (or more) of the fans stops, the temperature of the thermistor associated with the fan rises. As the temperature increases, the thermistor resistance decreases and V_{th} increases. If V_{th} becomes greater than V_{ref}, the related comparator output goes high (the comparator output is an open-collector transistor); hence, the base of Q4B is pulled up toward the level of the POWER OK H signal, Q4B conducts, and EMERGENCY SHUTDOWN L is generated.

When the EMERGENCY SHUTDOWN L signal is asserted, the Triac is turned off and the ac line is disconnected from the primary of the power transformer (EMERGENCY SHUTDOWN L also notifies the remote power control location of the shutdown). However, the +12 Vdc voltage is still present; consequently, Q4B and Q7 remain on (Q4B is latched on by the voltage at the cathode of diode D2). Q4B and Q7 can be unlatched only if the ON/OFF switch on the Limited Function Panel is moved to the OFF position. This action generates the BATTERY OFF L signal, which causes output pin 13 of comparator E1 to be grounded. The ground on the base of Q4B turns Q4B and, in turn, Q7 off. Thus, the relay opens. When the cause of the shutdown is corrected and the ON/OFF switch is returned to the ON position, pin 13 of E1 goes high and the circuitry once again monitors the thermostats and thermistors.

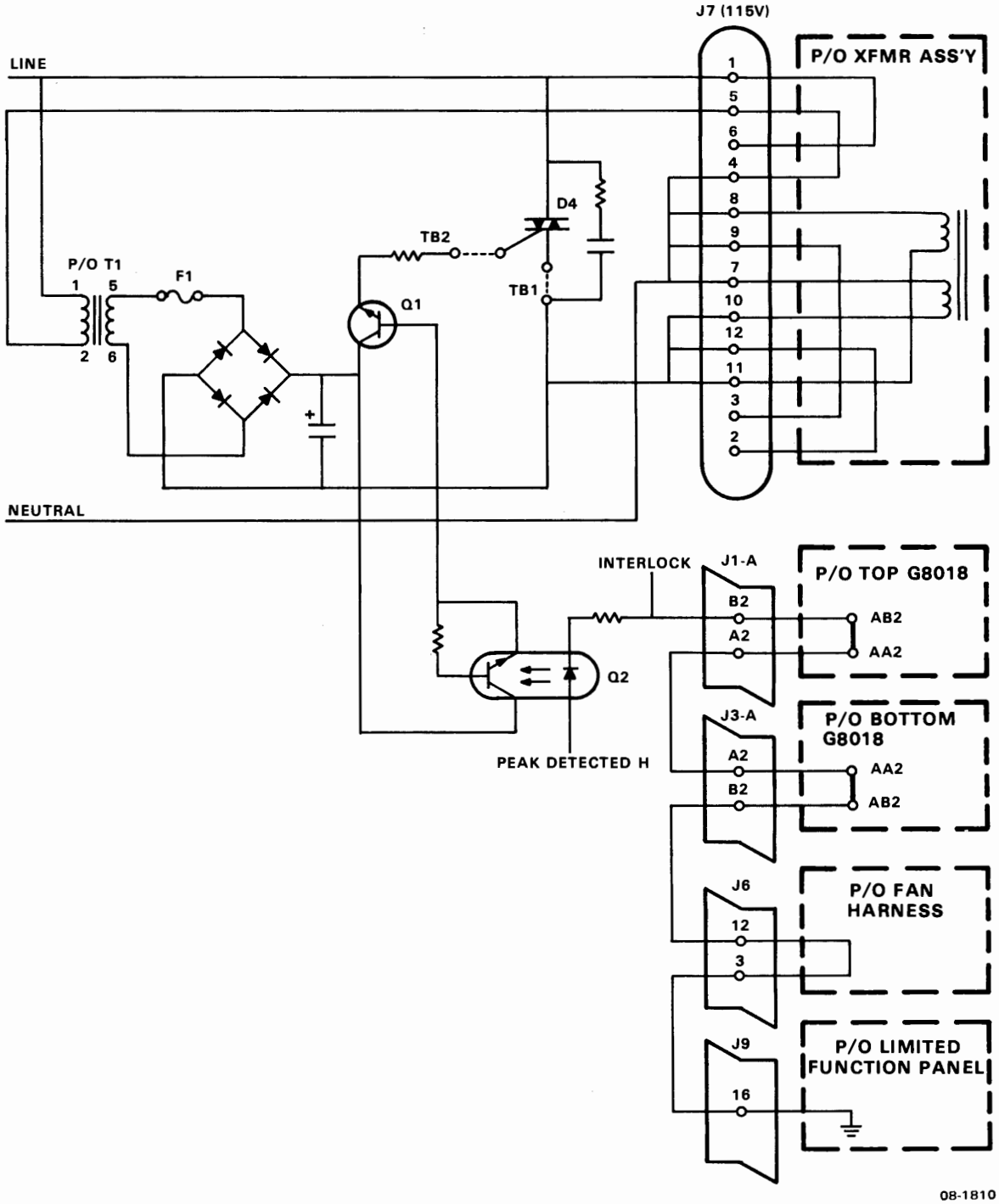


Figure 7-24 Interlock and Triac Control Circuit

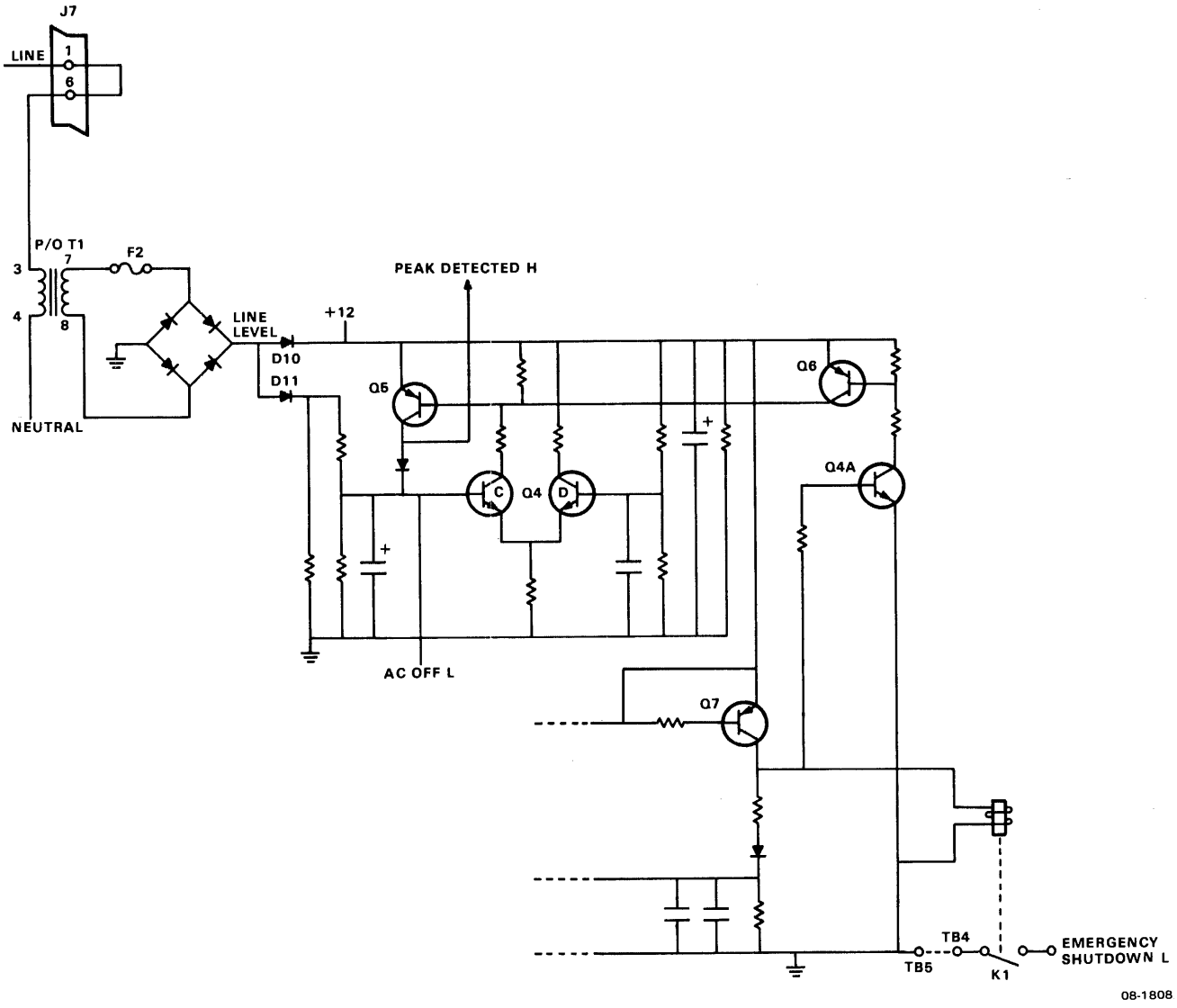


Figure 7-25 Line Level Transformer/Peak Detector

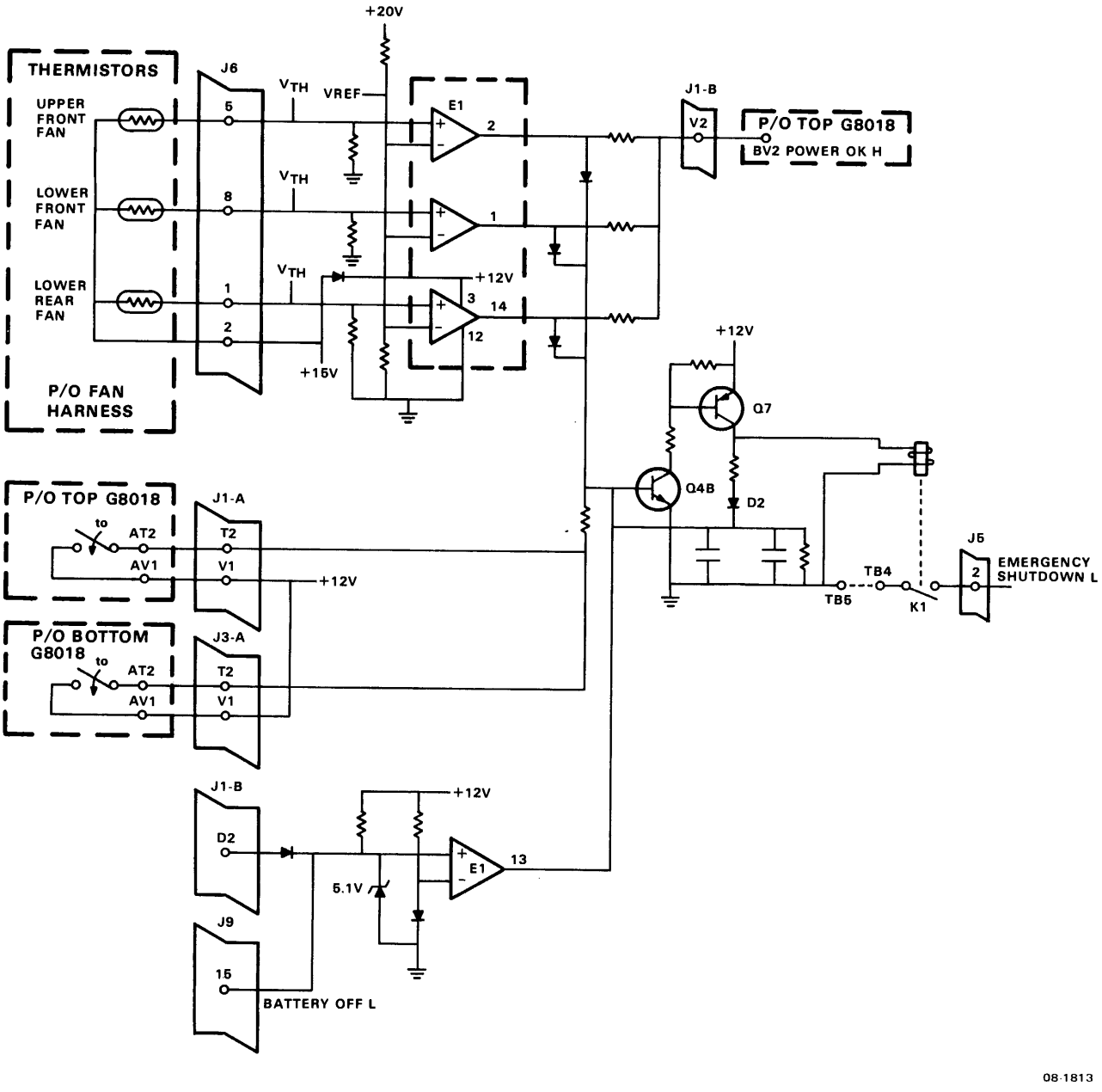
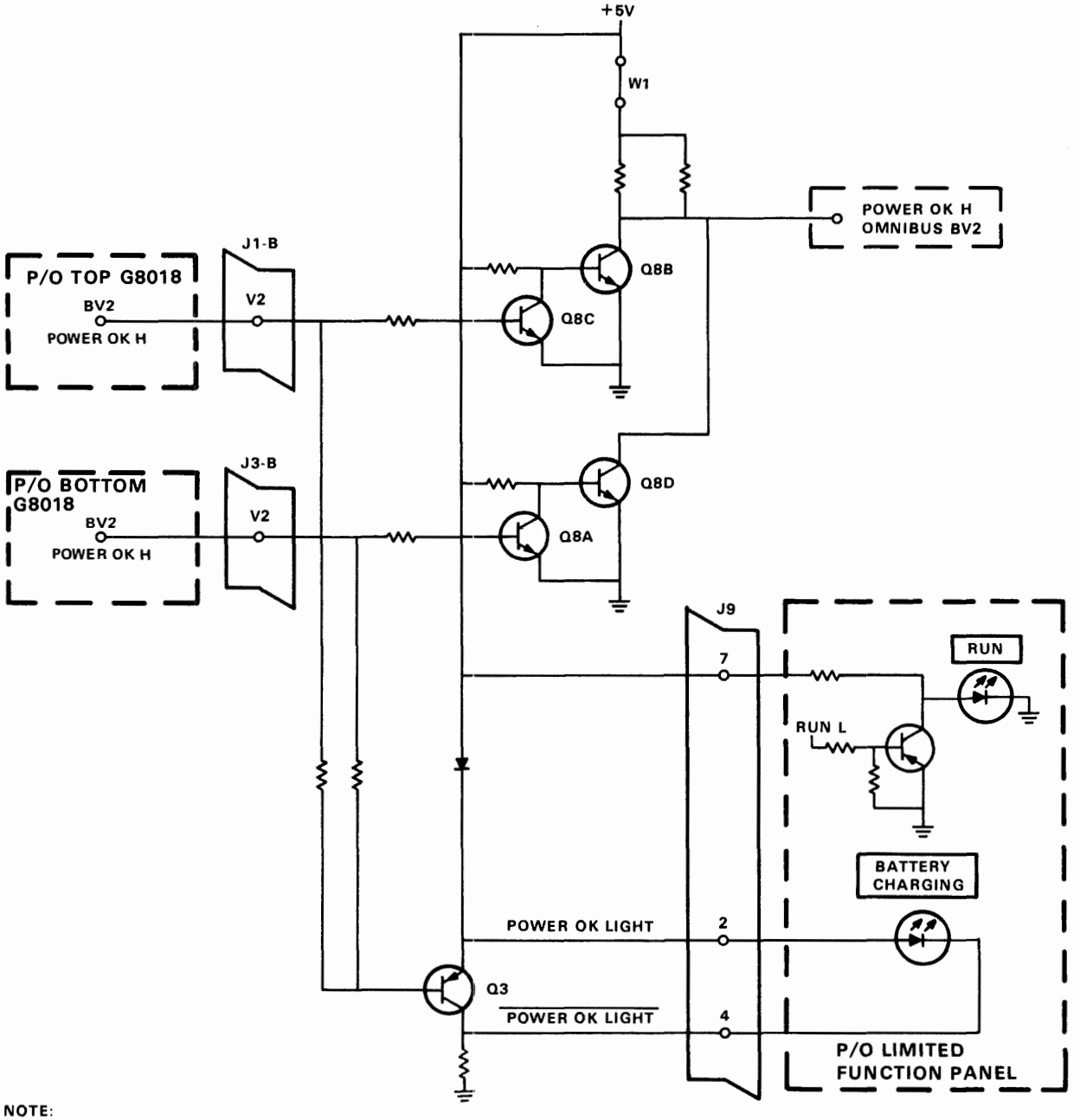


Figure 7-26 Thermistor/Thermostat and Emergency Shutdown

7.4.5 POWER OK H Circuit

The logic illustrated in Figure 7-27 monitors the POWER OK H signal generated on each G8018 regulator board. If both of these signals are high, the Omnibus POWER OK H signal is asserted, and the POWER OK light on the Limited Function Panel is lit. However, when either regulator board's POWER OK H signal is low, Omnibus POWER OK H will be taken to ground by transistor Q8B or Q8D; in addition, transistor Q3 will conduct and the POWER OK light will turn off.



NOTE:
The BA8-C can be used to expand a PDP8-E computer. Jumper W1 must be removed for such expansion. Refer to the 8A-Family Expansion Guide for particulars.

08-1809

Figure 7-27 POWER OK Circuit

CHAPTER 8
MAINTENANCE AND TROUBLESHOOTING

This chapter contains pertinent information about preventive maintenance, PDP-8/A troubleshooting techniques, and removal and replacement of modules.

CAUTION

ICs and individual components should not be replaced at the user's installation. Modules should be returned to DIGITAL for repair. Replacement of ICs and components on etched circuit boards require special equipment available at DIGITAL repair depots and at the factory.

8.1 MAINTENANCE AND TROUBLESHOOTING REQUIREMENTS

To maintain and troubleshoot the PDP-8/A, the user must obtain the necessary diagnostic programs and test equipment.

8.1.1 Diagnostic Programs

Diagnostics and supporting documentation are available from DIGITAL's Software Distribution Center. The PDP-8 Software Price List may be obtained by writing:

Digital Equipment Corporation
Software Distribution Center
146 Main Street
Maynard, Massachusetts 01754.

The price list also explains how to order.

The following software kits are available for testing the PDP-8/A:

PDP-8/A 4K Basic Software Kit (ZF006-RB)

MAINDEC-08-DJKKA-PB	PDP-8/A CPU Test
MAINDEC-08-DJKKA-D	PDP-8/A CPU Test Instructions
MAINDEC-08-DJMSA-PB	1-4K MS8-A MOS Memory Test
MAINDEC-08-DJMSA-D	1-4K MS8-A MOS Memory Test Instructions
MAINDEC-08-DJEXB-PB	2-32K Processor Exerciser
MAINDEC-08-DJEXB-D	2-32K Processor Exerciser Instructions
MAINDEC-08-DJMMA-PB	4-32K Memory Test
MAINDEC-08-DJMMA-D	4-32K Memory Test Instructions

PDP-8/A 1K and 2K Basic Software Kit (ZF007-RB)

MAINDEC-08-DJKKA-PM1	PDP-8/A CPU Test
MAINDEC-08-DJKKA-D	PDP-8/A CPU Test Instructions
MAINDEC-08-DJMSA-PM	1-4K MS8-A MOS Memory Test
MAINDEC-08-DJMSA-D	1-4K MS8-A MOS Memory Test Instructions
MAINDEC-08-DJEXA-PM	1-32K Random Memory Reference Instructions
MAINDEC-08-DJEXA-D	1-32K Random Memory Reference Instructions Exerciser Instructions
MAINDEC-08-DJEXB-PM	2-32K Processor Exerciser
MAINDEC-08-DJEXB-D	2-32K Processor Exerciser Instructions

1K and 2K DKC8-AA Option Software Kit (ZF207-RB)

MAINDEC-08-DJDKA-PM1	DKC8-AA Option Test 1
MAINDEC-08-DJDKA-PM2	DKC8-AA Option Test 2
MAINDEC-08-DJDKA-PM3	DKC8-AA Option Test 3
MAINDEC-08-DJDKA-PM4	DKC8-AA Option Test 4
MAINDEC-08-DJDKA-D	DKC8-AA Option Test Instructions

4K DKC8-AA Option Software Kit (ZF208-RB)

MAINDEC-08-DJDKA-PB1	DKC8-AA Option Test
MAINDEC-08-DJDKA-D	DKC8-AA Option Test Instructions

4K KM8-A Option Software Kit (ZF209-RB)

MAINDEC-08-DJKMA-PB1	KM8-A Option Test
MAINDEC-08-DJKMA-D	KM8-A Option Test Instructions

1K, 2K KM8-A Option Software Kit (ZF210-RB)

MAINDEC-08-DJKMA-PM1	KM8A Option Test 1
MAINDEC-08-DJKMA-PM2	KM8A Option Test 2
MAINDEC-08-DJKMA-PM4	KM8A Option Test 3
MAINDEC-08-DJKMA-D	KM8A Option Test Instructions

MR8-A ROM Software Kit (ZF211-RB)

MAINDEC-08-DJMRA-PM	MR8-A ROM Compare Test
MAINDEC-08-DJMRA-D	MR8-A ROM Compare Test Instructions

MR8-SA ROM Loader Software Kit (ZF204-RM)

MAINDEC-08-DJMRA-PB	MR8-A ROM Compare Test
MAINDEC-08-DJMRA-D	MR8-A ROM Compare Test Instructions
MAINDEC-08-DJMRB-PB	MR8-SA PROM Loader Program
MAINDEC-08-DJMRB-D	MR8-SA PROM Loader Program Instructions

MR8-FB 1K Software Kit (ZF196-RB)

MAINDEC-08-DHMRC-PB	MR8-FB PROM Compare Test
MAINDEC-08-DHMRC-D	MR8-FB PROM Compare Test Instructions
MAINDEC-08-DHMRE-PB	1K MR8-FB PROM Internal Test
MAINDEC-08-DHMRE-D	1K MR8-FB PROM Internal Test Instructions

The kits should be ordered by the kit number (i.e., ZF196-RB is the kit number for the 1K MR8-FB PROM.)

The information required to run the PDP-8/A diagnostics is provided in Chapter 2.

8.1.2 Equipment

Table 8-1 lists the equipment needed to run PDP-8/A diagnostics and test.

Table 8-1
Maintenance Equipment

Equipment	Specifications	Equivalent
Multimeter	10 kΩ/V minimum	Triplett Model 310
Jumper Wire		30-gauge with Termi Point Connections
Cable		BC08R-1
Quad Module Extender (1)		W987

8.2 PREVENTIVE MAINTENANCE INSPECTIONS

This paragraph provides information for performing preventive maintenance inspections. This information consists of visual, static, and dynamic tests that provide better equipment reliability. Preventive maintenance consists of procedures that are performed prior to the initial operation of the computer and periodically during its operating life. These procedures include visual inspections, cleaning, and operational testing. A log should be kept to record specific data that indicates the performance history and rate of deterioration; such a record can be used to determine the need and time for performing corrective maintenance on the system.

Scheduling of computer usage should always include specific time intervals that are set aside for scheduled maintenance purposes. Careful diagnostic testing programs can then reveal problems that may only occur intermittently during on-line operation.

8.2.1 Scheduled Maintenance

The PDP-8/A must receive certain routine maintenance attention to ensure maximum life and reliability. Digital Equipment Corporation suggests the maintenance defined in Table 8-2.

8.2.2 The Importance of a Preventive Maintenance Schedule

Computer downtime can be minimized by rigid adherence to a preventive maintenance schedule. A dirty air filter can cause machine failure through overheating. All filters should be cleaned periodically. The procedure for filter cleaning is described in Table 8-2.

8.3 PDP-8/A TROUBLESHOOTING

The PDP-8/A is constructed of highly reliable IC logic modules. Use of these circuits and a minimum amount of preventive maintenance ensures relatively little equipment downtime due to failure. If a malfunction occurs, users should analyze the condition and correct it by replacing the defective module.

Switches on modules that are used to replace another module should be set to correspond to the settings on the module that was removed. Chapter 2 lists the switch settings for all PDP-8/A modules.

8.3.1 Operator Errors

Operator errors are the cause of many computer malfunctions. When it has been determined that a module is malfunctioning, it is a good idea to check the switch positions on the module before replacing the module. Chapter 2 lists all the switch settings for the PDP-8/A modules and Table 2-16 lists basic symptoms and the corrective action required.

Table 8-2
Preventive Maintenance
(3 Months or 500 Hours)

Type	Action
Clean	Clean the exterior and interior of the computer cabinet, using a vacuum cleaner and/or clean cloths moistened in nonflammable solvent.
	Clean the air filter. Use a vacuum cleaner to remove accumulated dirt and dust, or wash with clean hot water and thoroughly dry before using.
Inspect	Visually inspect equipment for general condition. Repaint any scratched areas.
	Inspect all wiring and cables for cuts, breaks, fraying, wear, deterioration, kinks, strains, and mechanical security. Tape or replace any defective cable.
	Inspect the following for mechanical security: key switches, control knobs, lamps, connectors, transformers, fans, etc. Tighten or replace as required.
	Inspect all module mounting panels to ensure that each module is securely seated in its connector. Remove and clean any module that may have collected excess dirt or dust.
Perform	Run the necessary diagnostic programs to verify proper computer operation.
	Perform all preventive maintenance operations for each peripheral device included in the PDP-8/A System as directed in the individual maintenance instructions supplied with each peripheral device.
	Enter preventive maintenance results in log book.

8.3.2 Troubleshooting Procedures

When a malfunction is detected, gather all information available from other users who have encountered the problem and check the system log book for any previous reference to this problem. Make a note of indications on the Limited Function Panel and Programmer's Console before attempting to locate the module that is malfunctioning. This information is helpful for describing the malfunction in the log book or to your DIGITAL representative before he or she arrives on site.

Do not attempt to locate the defective module using complex software systems. Run the diagnostic programs following the procedures in Chapter 2 and select the simplest program that exhibits the error condition. Diagnostic programs are carefully written to include programs that assist the user when isolating the defective module.

For those modules connected to peripheral devices (i.e., DKC8-AA), disconnect the peripheral device if it is not necessary to run the diagnostic, and rerun the diagnostic.

8.3.3 Validation Tests

If a defective module is replaced by a new module, tag the defective module noting the nature of the failure.

To confirm that the new module resolved the problem, run all tests that originally exhibited the problem. If modules have been moved during the troubleshooting period, return all modules to their original positions before running the validation tests. Contact your DIGITAL field service office for the procedure required to repair your module.

8.3.4 Cable Problems

Malfunctions of modules that have cables connected to them, which are not corrected by replacing the modules, may be caused by defective cables. If the validation tests are run and the replacement module has not corrected the problem, it is a good idea to ensure that the cable is connected correctly. If the cable is connected correctly and the problem persists, remove and replace the cables.

8.3.5 Log Entry

A log book should be kept for each PDP-8/A System. Maintenance operations are not complete until all activities are recorded in the log book. Record all data indicating the symptoms given by the fault, the method of fault detection, the module at fault, and any comments that would be helpful to maintain the equipment in the future.

The log book should be maintained on a daily basis, recording all operator usage and preventive maintenance results.

8.3.6 Removal and Replacement of Modules

CAUTION

Power should be turned OFF before attempting to remove or install a module.

The Programmer's Console must be removed to gain access to PDP-8/A modules. To remove the Programmer's Console, grasp the console and pull it toward you. Do not remove any screws. There should be a table available on which to place the Programmer's Console when it is removed. If a table is not available, disconnect the two cables that are connected to the M8316 module.

To remove modules, unlock the locking handles on each side of the module by pulling them toward you. Slowly slide the module out of the cabinet, being careful not to change positions of switches on the module.

To replace a module, slide the module back into the slot from which it was removed and push the two locking handles back into the locked position.

To replace the Programmer's Console, reconnect the two cables to the M8316 module, line up the four latches with the holes, and push the panel into place.

8.3.7 Removal and Replacement of Regulator Board

The G8016 or G8018 Regulator Boards must be removed to replace fuses or to replace the regulator board.

To gain access to the regulator board in the PDP-8/A Semiconductor chassis or in the 8A400/600/800 chassis, turn power OFF and remove the Limited Function Panel by pulling it toward you. Disconnect the cable from the Limited Function Panel. Lay the Limited Function Panel out of the way. Use a flat-blade screwdriver to loosen the two fasteners holding the Regulator Board assembly. Pull the assembly toward you slowly, being careful not to damage connectors or components.

To replace the assembly slide it slowly back into the chassis, push the connector into the regulator board slot, and tighten the two fasteners. Reconnect the cable to the Limited Function Panel. Line up the four latches with the four holes and push the Function Panel back into place.

The Regulator Board assemblies in the 8A420/620/820 chassis are in the rear. After turning off the power, remove the rear cover by loosening the four fasteners that hold it to the frame. Each assembly is removed by loosening the two fasteners that secure it to the chassis and pulling the assembly from the regulator board connectors.

8.3.8 Removal and Replacement of LEDs on the Limited Function Panel

To replace the LED indicators on the Limited Function Panel, remove the Limited Function Panel as described in 8.3.7. After the Limited Function Panel is removed, remove the four screws that hold the printed circuit board on the Panel.

CAUTION

Soldering iron used to remove and replace LEDs should not exceed 40 W and should be free of dirt and burned resin.

Use a soldering iron and solder sucker to remove solder from pins of LED to be removed. Note the connection for the thickest pin on the LED so that the new LED can be installed with the pins connected to the correct polarity of voltage. Insert the new LED and solder the pins on the printed circuit board.

Replace the printed circuit board using the four screws to fasten it down.

Reconnect the Limited Function Panel cable and reinstall the Limited Function Panel.

8.3.9 Removal and Replacement of LEDs on the Programmer's Console

To remove LEDs on the Programmer's Console remove the Programmer's Console as explained in Paragraph 8.3.6. The cables must be disconnected from the M8316 module.

To remove the LEDs for the DISP and ADDR displays, take out the screws holding the two boards and remove the board. Remove the segmented display by grasping and pulling on it. Replace the segmented display with one that has the same part identification. Then replace the board and fasten with the screws that were taken out when the board was removed.

To remove the LED's for the status indicators (RUN, STATUS, MD etc.), remove the top board and bottom board by removing the screws that hold them. Remove the solder from the LED to be removed using a 40 W soldering iron and solder sucker. Remove the LED and note the connection for the thickest lead on the LED. Install the new LED with the thickest lead in the same hole on the circuit board that was occupied by the one removed. Solder the LED lead to the circuit board. Replace the bottom board and the top board.

Connect the cable on the Programmer's Console to the M8316 module and reinstall the Programmer's Console.

8.4 POWER SUPPLY ADJUSTMENTS

A W987 Module Extender board and an insulated adjusting tool are required to adjust the G8016 and G8018 Power Supply voltages.

8.4.1 G8016 Power Supply Adjustment

8.4.1.1 +5 V Adjustment (G8016) – To adjust the 5 V on the G8016 Regulator Board, install the W987 Module Extender in one of the Omnibus slots. Connect an accurate digital voltmeter between pin CA2 on the Module Extender board and any convenient ground. Use an insulated adjusting tool to adjust the +5 V supply adjustment (Figure 8-1) to read 5 V on the meter. After the power supply is adjusted, remove the meter leads and the Module Extender board.

8.4.2 G8018 Power Supply Adjustment

8.4.2.1 +5 V Power Supply Adjustment – To adjust the +5 V supply install the W987 Module Extender board in one of the Omnibus slots. Connect an accurate digital voltmeter between pin CA2 on the Module Extender board and any convenient ground. Use an insulated adjusting tool to adjust the +5 V supply adjustment (Figure 8-2) for 5 V. Remove the meter leads and the Module Extender after the power supply is adjusted.

8.4.2.2 +20 V Power Supply Adjustment – To adjust the +20 V supply, install the W987 Module Extender board in one of the core memory slots (Figure 3-1) with the D connector on the Module Extender in the E connector on the Omnibus. Connect a voltmeter between DA2 of the Module Extender board and some convenient ground. Use an insulated adjusting tool to adjust the +20 V (Figure 8-2) for 20.0 V. After the +20 V adjustemnt is made, remove the meter and the Module Extender board.

8.5 POWER FAIL/AUTO-RESTART LEVEL ADJUSTMENT (G8016 AND G8018)

NOTE

This is a factory adjustment and should not be performed in the field.

A Variac is required to adjust the Power Fail/Auto-Restart levels. The two potentiometers (up and down) are factory adjusted so AC LOW L is true when ac line drops below 95 Vac, and false when the ac line voltage goes above 105 Vac.

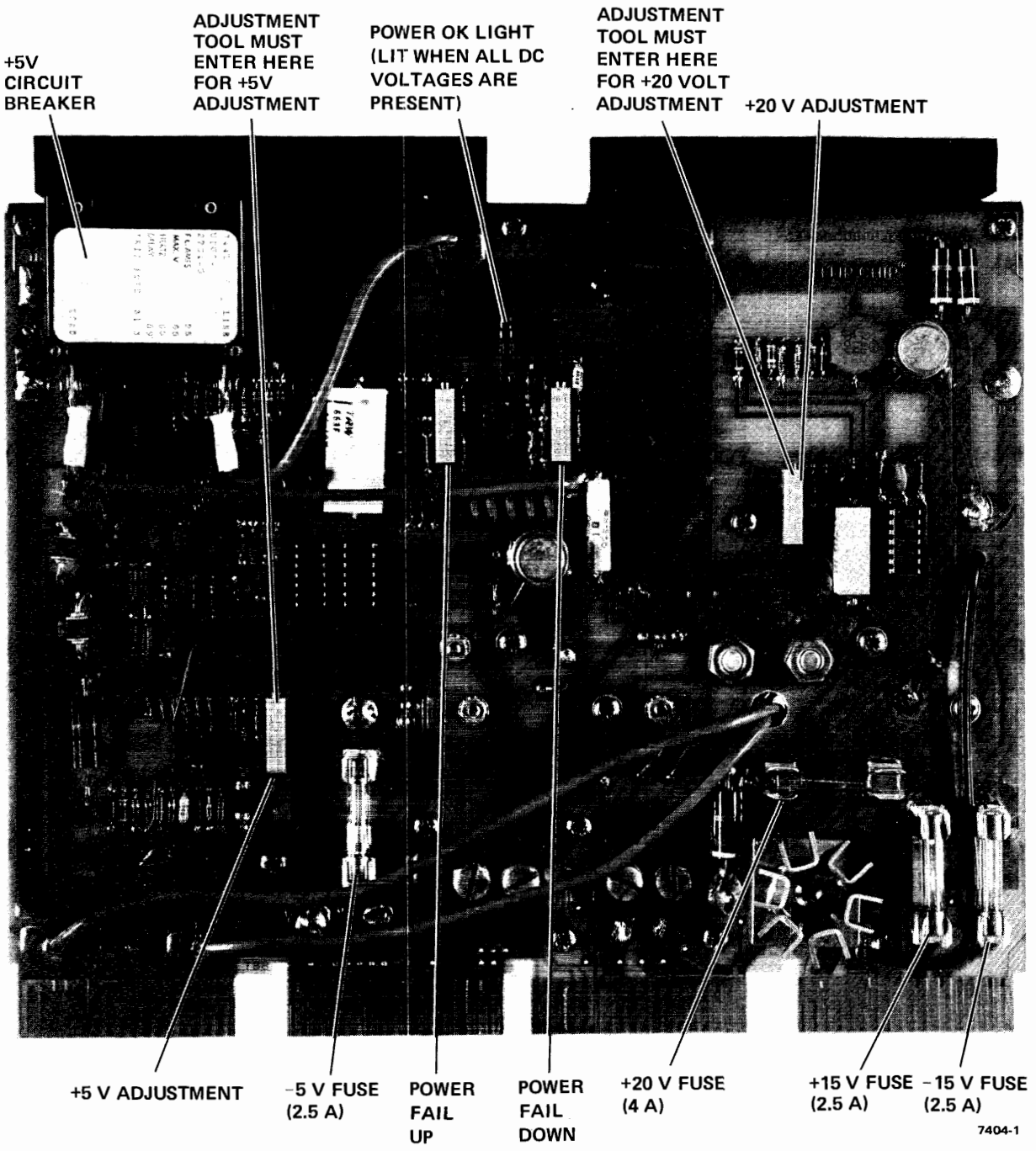


Figure 8-2 G8018 Regulator Board Adjustments

8.5.1 G8018 Power Fail/Auto-Restart Adjustment

To adjust the two levels, turn power OFF and connect a Variac to the 8A. Connect the Variac to the power source and turn 8A power ON. Install the module extender module in slot 2 or 3 of the Omnibus and monitor pin BB1. Adjust the Variac for approximately 80 Vac output, and verify that AC LOW on pin BB1 is low (true). Slowly adjust the Variac voltage toward 120 Vac; as the voltage reaches 105 Vac the AC LOW signal on BB1 should go high (+4 V). Adjust the UP potentiometer (Figure 8-2) until AC LOW makes a low to high transition at 105 Vac.

Now turn the Variac voltage down to 95 Vac and adjust the DOWN potentiometer so that AC LOW (pin BB1) makes a high to low transition at 95 Vac.

8.5.2 G8016 Power Fail/Auto-Restart Adjustment

To make the Power Fail/Auto-Restart adjustment on the G8016, turn power OFF and remove all modules. Remove the G8016 module, insert a W987 Extender Module into the regulator slot and mount the G8016 regulator in the extender module. Adjust the two levels using the same procedure as for the G8018 (Figure 8-1 shows the adjustment potentiometers). Remove the extender board and replace the regulator and all modules.

8.6 LINE VOLTAGE AND FREQUENCY COMBINATIONS

The PDP-8/A computers can operate with a line voltage of either 115 Vac or 230 Vac, and with a line frequency of either 50 Hz or 60 Hz. Table 8-3 lists the PDP-8/A computers and the part numbers of the line sets, fuses, and transformers that must be used with each line voltage/frequency combination. The operating voltage and frequency of each computer can be changed by replacing one line set/fuse/transformer combination with another. Specifics relating to each computer are given in the following sections.

Table 8-3
PDP-8/A Line Sets, Fuses, and Transformer Assemblies

Computer	Line Set		Fuse		Transformer Assembly P/N	
	P/N	Rated Operating Voltage and Current	P/N	Rating	50 Hz	60 Hz
8A400/600/800	7010915-03 7010915-04	115 Vac/8A 230 Vac/4A	9009698 9009699	250 V/8A 150 V/4A	7010935-02	7010935-01
8A420/620/820	7012375-00 7012375-01	115 Vac/15A 230 Vac/8A	9008279 9007999	250 V/12A 250 V/6A	7012373-01	7012373-00
PDP-8/A Semiconductor	7010041-01 7010041-02	115 Vac/4A 230 Vac/2A	9009699 9009697	250 V/4A 250 V/2A	7010040, with frequency jumper 7010042	

8.6.1 8A400/600/800

The transformer assembly (50 Hz or 60 Hz) includes two Mate-N-Lok connectors, three Quick Disconnect connectors, and one Ring Tongue terminal. For 115 Vac operation, plug transformer assembly connector P2 (12-pin) into J16 of the H9194 Connector Block assembly (Figure 8-3); for 230 Vac operation plug P2 into J17. For either voltage, plug P1 (6-pin) of the transformer assembly into J19 of the Connector Block assembly. For either voltage, connect the blue/black wire from the transformer assembly to the center lug (TB2) of the Connector Block assembly; attach the other two wires terminated by Quick Disconnect connectors to TB1 and TB3, either wire to either lug (the wire attached to the solderless connector is a ground connection).

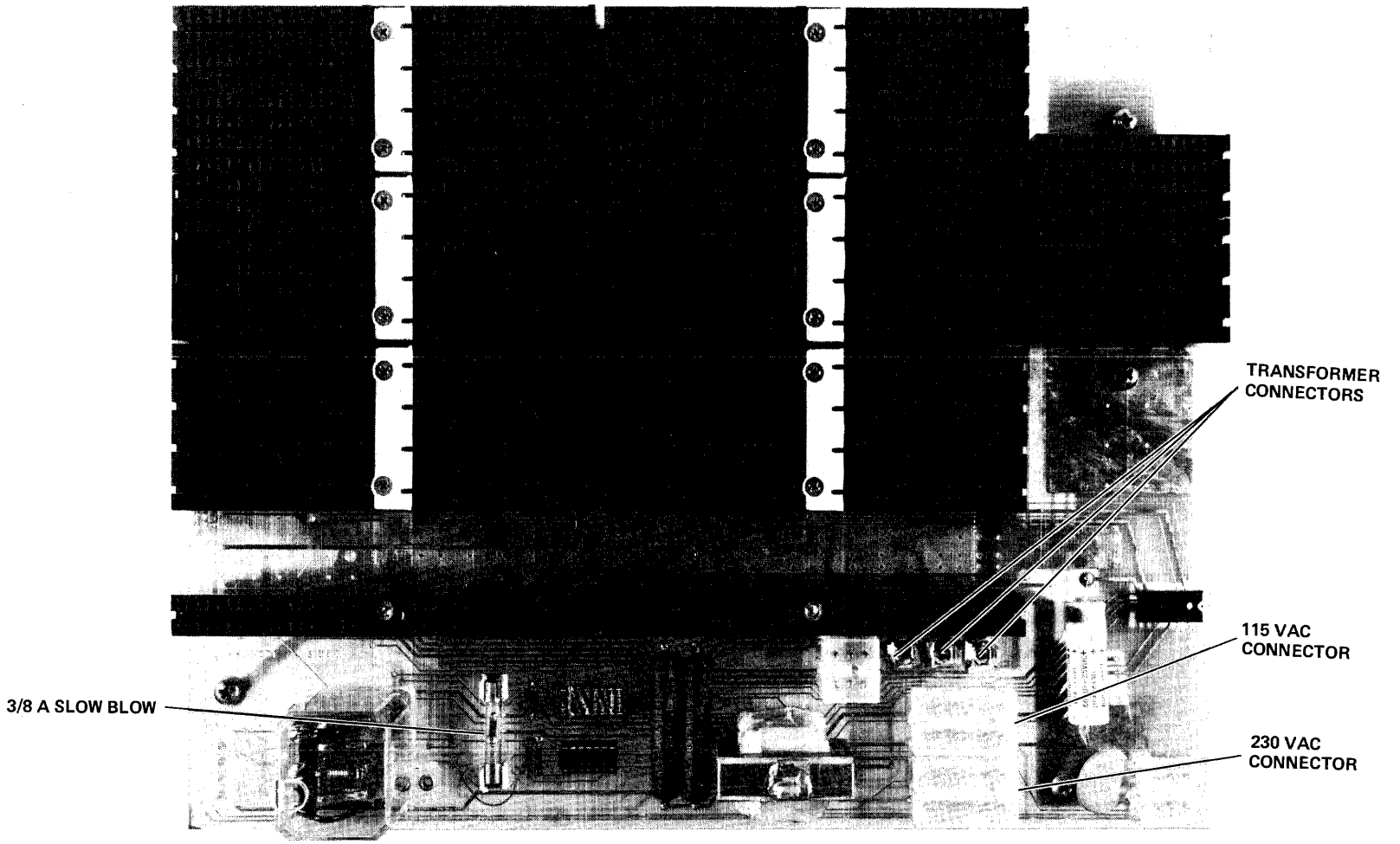


Figure 8-3 H9194 Connector Block Assembly

8.6.2 8A420/620/820

The transformer assembly (50 Hz or 60 Hz) includes a 12-pin Mate-N-Lok connector (P1), two Faston connectors, one Ring Tongue terminal (a ground connection), and a cable assembly terminated by twelve Ring Tongue terminals. For 115 Vac operation, plug P1 into J7 of the Power Distribution Board; for 230 Vac operation, plug P1 into J8. For either voltage, connect the two Faston connectors to the 12 microfarad, 660 V capacitor mounted above the transformer assembly. For either voltage, connect the twelve Ring Tongue terminals on the cable assembly to J10 of the Power Distribution board. Wire colors-pin numbers match as follows: Violet-12, violet-11, yellow-10, yellow-9, yellow/black-8, violet/black-7, blue-6, orange-5, blue/black-4, orange/black-3, blue-2, orange-1.

8.6.3 PDP-8/A Semiconductor

This computer uses the same transformer for either line frequency. For 115 Vac, plug P1 of the transformer assembly into J7 of the Power board (Figure 8-4); plug the frequency jumper into J4 of the Power board for 60 Hz operation and into J5 for 50 Hz operation. For 230 Vac, plug P1 into J6 of the Power board; plug the frequency jumper into J4 or J5, as before. Attach the Faston connectors to TB1–TB5 of the Power board as indicated in Figure 8-4.

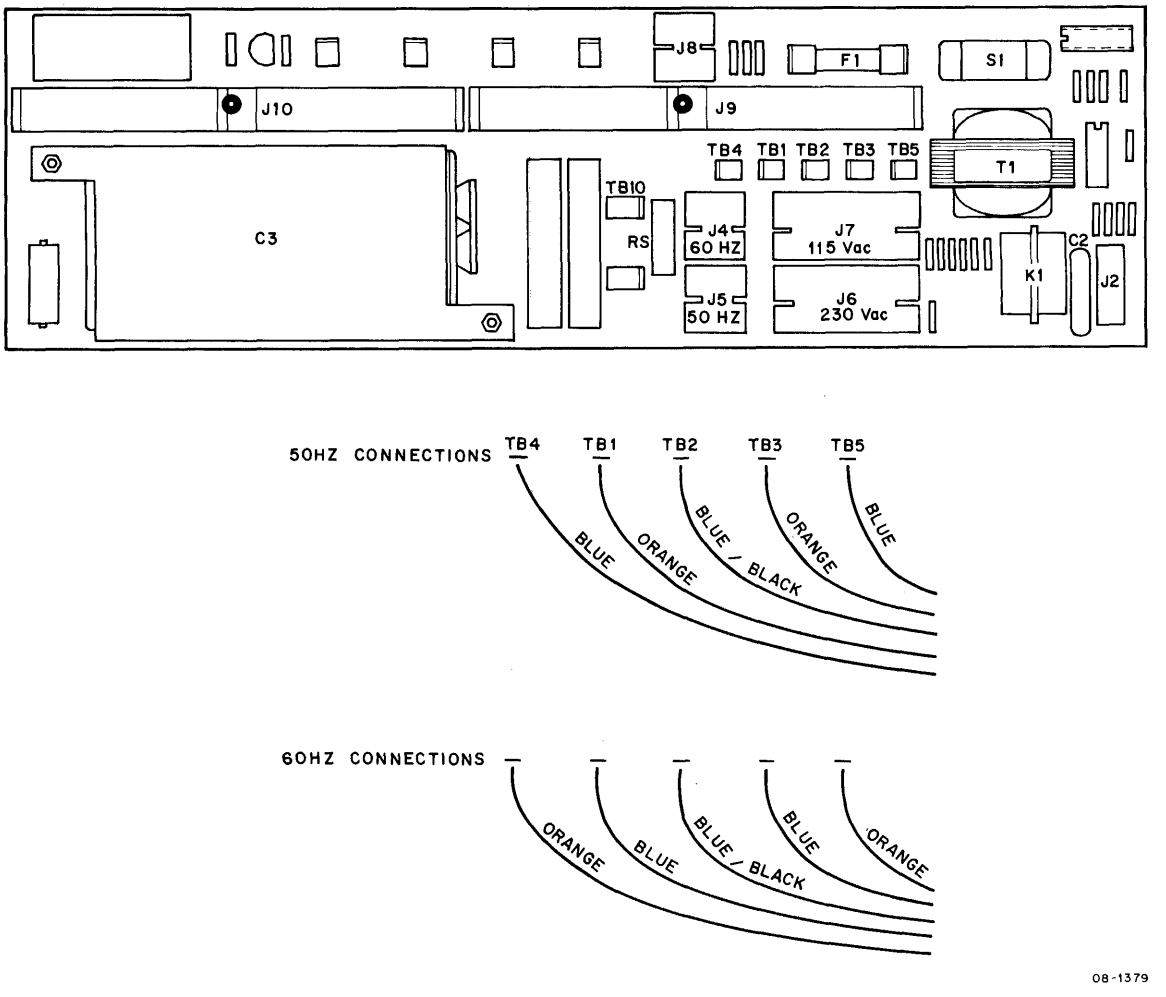


Figure 8-4 50 Hz and 60 Hz Connections on 10 Slot Machines

CHAPTER 9
SPARE PARTS

A list of recommended spares for the PDP-8/A is contained in Tables 9-1 (PDP-8/A Semiconductor) and 9-2 (8A).

Table 9-1
PDP-8/A Semiconductor Recommended Spare Parts

Designation (if any)	Name	Part Number	Quantity
KK8-A	Central Processor	M8315	1
DKC8-AA	I/O Option Module	M8316	1
KM8-AA	Extended Option Module	M8317	1
MS8-A	1K RAM Read/Write Memory	M8311YA	1
MS8-A	2K RAM Read/Write Memory	M8311YB	1
MS8-A	4K RAM Read/Write Memory	M8311YD	1
Regulator	Power Supply Regulator	G8016	1
	Console Logic	7010644	1
	Console Cable	BC08R-1	1
	Remote Console Cable	BC08R-15	1
	Cable Limited Function Console	7008612-IF	1
	2 A Slow Blow Fuse (230 V)	9009697	3
	4 A Slow Blow Fuse (115 V)	9009699	3
	3/8 A Slow Blow Fuse	9007207	3
	Diode Array	7010866	1
	Power Relay	1211138-01	1
	Battery	1211670	1

Table 9-2
8A Recommended Spare Parts

Designation (if any)	Name	Part Number	Quantity
KM8-E	Memory Extension and Time Share Option	M837	1
KK8-A	Central Processor	M8315	1
DKC8-AA	I/O Option Module	M8316	1
KM8-A	Extended Option Module	M8317	1
MM8-AA	8K Core Memory	G649	1
MM8-AB	16K Core Memory	G650	1
	Power Supply Regulator	G8018	1
	Console Cable	BC08R-1	1
	Remote Console Cable	BC08R-15	1
	Cable Limited Function Console	7008612-IF	1
	Console Logic	7010644	1
	4 A Slow Blow Fuse (230 V – H9300 Chassis Assembly)	9009699	3
	8 A Slow Blow Fuse (115 V – H9300 Chassis Assembly)	9009698	3
	3/8 A Slow Blow Fuse (H9300 Chassis Assembly)	9007207	3
	2.5 A Slow Blow Fuse (+15 V, -15 V, -5 V) (H9300 Chassis Assembly)	9008387	3
	4 A Fuse (+20 V)	9007219	3
	12 A Slow Blow Fuse (115 V – BA8-C Chassis Assembly)	9008279	3
	6 A Slow Blow Fuse (230 V – BA8-C Chassis Assembly)	9007999	3
	1/2 A Fuse (BA8-C Chassis Assembly)	9007208	5
	2.5 A Slow Blow Fuse (+15 V, -15 V, -5 V) (BA8-C Chassis Assembly)	9008387	5
	Diode Array	7010866	1
	Power Relay Assembly	1211138-01	1

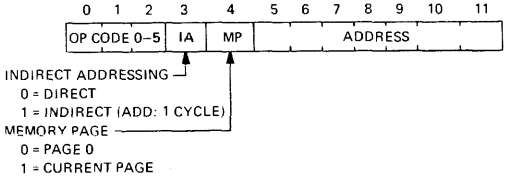
APPENDIX A
INSTRUCTION SUMMARY

CPU INSTRUCTION SUMMARY

CPU Instruction Summary

BASIC INSTRUCTIONS

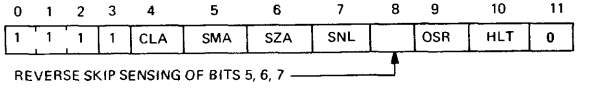
			Cycles
AND	0000	logical AND	2
TAD	1000	2's complement add	2
ISZ	2000	increment, and skip if zero	2
DCA	3000	deposit and clear AC	2
JMS	4000	jump to subroutine	2
JMP	5000	jump	1
IOT	6000	in/out transfer	-
OPR	7000	operate	1



Memory Reference Instruction Bit Assignments

GROUP 2 OPERATE MICROINSTRUCTIONS (1 CYCLE)

			Sequence
SMA	7500	skip on minus AC	1
SZA	7440	skip on zero AC	1
SPA	7510	skip on plus AC	1
SNA	7450	skip on on-zero AC	1
SNL	7420	skip on non-zero link	1
SZL	7430	skip on zero link	1
SKP	7410	skip unconditionally	1
OSR	7404	inclusive OR switch register with AC	3
HLT	7402	halts the program	3
CLA	7600	clear AC	2

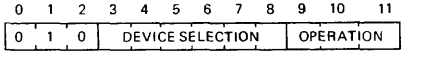


Logical Sequences:
1 (Bit 8 is Zero) – Either SMA or SZA or SNL
1 (Bit 8 is One) – Both SPA and SNA and SZL
2 – CLA
3 – OSR, HLT

Group 2 Operate Instruction Bit Assignments

INTERNAL IOT MICROINSTRUCTIONS
PROGRAM INTERRUPT AND FLAG (1 CYCLE)

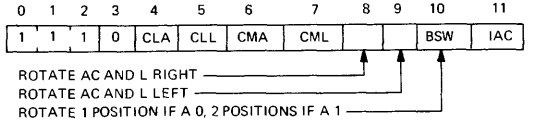
SKON	6000	skip if interrupt ON, and turn OFF
ION	6001	turn interrupt ON
IOF	6002	turn interrupt OFF
SRQ	6003	skip on interrupt request
GTF	6004	get interrupt flags
RTF	6005	restore interrupt flags
CAF	6007	clear all flags



IOT Instruction Bit Assignments

GROUP 1 OPERATE MICROINSTRUCTIONS (1 CYCLE)

			Sequence
NOP	7000	no operation	–
CLA	7200	clear AC	1
CLL	7100	clear link	1
CMA	7040	complement AC	2
CML	7020	complement link	2
RAR	7010	rotate AC and link right one	4
RAL	7004	rotate AC and link left one	4
RTR	7012	rotate AC and link right two	4
RTL	7006	rotate AC and link left two	4
IAC	7001	increment AC	3
BSW	7002	swap bytes in AC	4



Logical Sequences
1 – CLA CLL
2 – CMA CML
3 – IAC
4 – RAR, RAL, RTR, RTL, BSW

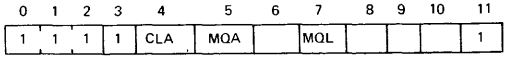
Group 1 Operate Instruction Bit Assignments

COMBINED OPERATE MICROINSTRUCTIONS (1 CYCLE)

CIA		7041	complement and increment AC
LAS		7604	load AC with switch register
STL		7120	set link (to 1)
GLK		7204	get link (put link in AC bit 11)
CLA	CLL	7300	clear AC and link
CLL	RAR	7110	shift positive number one right
CLL	RAL	7104	shift positive number one left
CLL	RTL	7106	clear link, rotate 2 left
CLL	RTR	7112	clear link, rotate 2 right
SZA	CLA	7640	skip if AC=0, then clear AC
SZA	SNL	7460	skip if AC=0 or link is 1, or both
SNA	CLA	7650	skip if AC≠0, then clear AC
SMA	CLA	7700	skip if AC<0, then clear AC
SMA	SZA	7540	skip if AC≤0
SMA	SNL	7520	skip if AC<0 or link is 1, or both
SPA	SNA	7550	skip if AC>0
SPA	SZL	7530	skip if AC≥0 and the link is 0
SPA	CLA	7710	skip if AC≥0, then clear AC
SNA	SZL	7470	skip if AC≠0 and link=0

MQ MICROINSTRUCTIONS (1 CYCLE)

NOP	7401	no operation
CLA	7601	clear AC
MQL	7421	load MQ from AC then clear AC
MQA	7501	inclusive OR the MQ with the AC
CAM	7621	clear AC and MQ
SWP	7521	swap AC and MQ
ACL	7701	load MQ into AC
CLA SWP	7721	load AC from MQ then clear MQ



Logical Sequence:
1–CLA
2–MQA, MQL
3–ALL OTHERS

MQ Microinstruction Bit Assignments

DKC8-AA I/O OPTION BOARD INSTRUCTIONS

Serial Line Unit IOT Instructions (1 Cycle)

Receive

KCF	6030	Clear Receive flag, do not set Reader Run.
KSF	6031	Skip if Receive flag is set.
KCC	6032	Clear Receive flag and AC, set Reader Run.
KRS	6034	Read Receive Buffer.
KIE	6035	Load AC11 into Interrupt Enable. AC11 = 1. Set interrupt Enable. AC11 = 0. Clear Interrupt Enable.
KRB	6036	Combined KCC & KRS.

Transmit

TFL	6040	Set Transmit Flag.
TSF	6041	Skip if Transmit flag is set.
TCF	6042	Clear Transmit flag.
TPC	6044	Load AC4-AC11 into transmit buffer and transmit.
SPI	6045	Skip if transmit or receive flag is set and if interrupt enable is set.
TLS	6046	Combined TCF and TPC commands.

General-Purpose Parallel I/O Instructions (1 Cycle)

DBST	6570	Skip on Data Accepted, clear Data Accepted and Data Available.
DBSK	6571	Skip on Data Ready flag.
DBRD	6572	Read Data In to AC0–AC11.
DBCF	6573	Clear Data Ready flag, issue Data Accepted Out pulse.
DBTD	6574	Load AC0–AC11 into buffer and transmit Data Out.
DBSE	6575	Set Interrupt Enable to a 1.
DBCE	6576	Reset Interrupt Enable to a 0.
DBSS	6577	Issue a Strobe pulse.

Real Time Crystal Clock Instructions (1 Cycle)

CLLE	6135	Load Interrupt Enable from AC11 AC11 = 1, set Interrupt Enable AC11 = 0, clear Interrupt Enable
CLCL	6136	Clear Clock flag.
CLSK	6137	Skip if Clock flag = 1.

KM8-A EXTENDED OPTION BOARD INSTRUCTIONS

Memory Extention Time Share Control Instructions (1 Cycle)

GTF	6004	Jam Transfer the status of the flags and link into AC0, AC2, and AC4–AC11. (0 = cleared, 1 = set) AC0 = Link AC2 = Interrupt Request AC4 = Interrupt Enable AC5-11 = User Mode and Save Field
RTF	6005	Transfer the contents of AC5, AC6–AC11 to the user buffer flip-flop, the instruction buffer and data field, and inhibit processor interrupts until the next JMP or JMS instruction. User Field flip-flop and the Instruction Field are loaded at the conclusion of the next JMP or JMS instruction. The CPU loads the contents of AC0 into the Link and enables the interrupt system in response to this IOT.
CDF	62N1	Load the Data Field register with the program selected number N (N = 0–7).
CIF	62N2	Load the Instruction Buffer with the program selected number N (N = 0–7) and inhibit program interrupts until the next JMP or JMS instruction.
CDF CIF	62N3	Load the Data Field and Instruction Buffer with program selected number N (N = 0–7). Combines CDF and CIF.
RDF	6214	OR's the content of the Data Field register with AC6–AC8.
RIF	6244	OR's the contents of the Instruction Field register with AC6–AC8.
RIB	6234	OR's the contents of the Save Field with AC6–AC8 and AC9–AC11. The time share bit of the Save Field is ORed into AC5.
RMF	6224	Restores the contents of the Save Field register into the Instruction Buffer, Data Field, and (if time share is enabled) user buffer.
CINT	6204	Clear User Interrupt flip-flop.

Memory Extension/Time Share Control Instructions (1 Cycle) (Cont)

SINT	6254	Skip if User Interrupt flip-flop is set.
CUF	6264	Clear User Buffer flip-flop (exit time share mode).
SUF	6274	Set User Buffer flip-flop (enter time share mode) following next JMP or JMS instruction.

Power Fail/Auto Restart (1 Cycle)

SPL	6102	Skip if AC Low flip-flop is set.
CAL	6103	Clear AC Low flip-flop.
SBE	6101	Skip if Battery Empty flip-flop is set.

PERIPHERAL AND OPTION INSTRUCTION SUMMARY

LE8-E Line Printer

Mnemonic Symbol	Octal Code	Operation
PSKF	6661	Skip on Character Flag
PCLF	6662	Clear the Character Flag
PSKE	6663	Skip on Error
PSTB	6664	Load Printer Buffer, Print on Full Buffer or Control Character
PSIE	6665	Set Program Interrupt Flag
PCLF, PSTB	6666	Clear Line Printer Flag, Load Character, and Print
PCIE	6667	Clear Program Interrupt Flag

XY8-E Incremental Plotter Control

Mnemonic Symbol	Octal Code	Operation
PLCE	6500	Clear Interrupt Enable
PLSF	6501	Skip on Plotter Flag
PLCF	6502	Clear Plotter Flag
PLPU	6503	Pen Up
PLLR	6504	Load Direction Register, Set Flag
PLPD	6505	Pen Down
PLCF, PLLR	6506	Clear Flag, Load Direction Register, Set Flag
PLSE	6507	Set Interrupt Enable

VC8-E CRT Display Control

Mnemonic Symbol	Octal Code	Operation
DILC	6050	Clears Enables, Flags and Delays
DICD	6051	Clears Done Flag
DISD	6052	Skip on Done Flag
DILX	6053	Load X Register
DILY	6054	Load Y Register
DIXY	6055	Clear Done Flag; Intensify; Set Done Flag
DILE	6056	Transfers AC to Enable Register
DIRE	6057	Transfers Display Enable/Status Register to AC

BB08-P General Purpose Interface Unit

Mnemonic Symbol	Octal Code	Operation
GTSF	6361	Skip on Transmit Flag
GCTF	6362	Clear Transmit Flag
	6564	(User-Assigned)
GRSF	6371	Skip on Receive Flag
GCRF	6372	Clear Receive Flag
GRDB	6374	Read Device Buffer

DR8-EA 12-Channel Buffered Digital I/O

Mnemonic Symbol	Octal Code	Operation
DBDI	65X0	Disable Interrupt
DBEI	65X1	Enable Interrupt
DBSK	65X2	Skip on Done Flag
DBCI	65X3	Clear Selective Input Register
DBRI	65X4	Transfer Input to AC
DBCO	65X5	Clear Selective Output Register
DBSO	65X6	Set Selective Output Register
DBRO	65X7	Transfer Output to AC

5X is the Device Code.

DP8-EA/EB Synchronous Modem Interface

Mnemonic Symbol	Octal Code	Operation
SGTT	6405	Transmit Go
SGRR	6404	Receive Go
SSCD	6400	Skip if Character Detected
SCSD	6406	Clear Sync Detect
SSRO	6402	Skip if Receive Word Count Overflow
SCSI	6401	Clear Synchronous Interface
SRTA	6407	Read Transfer Address Register
SLCC	6412	Load Control
SSRG	6410	Skip if Ring Flag
SSCA	6411	Skip if Carrier/AGC Flag
SRS2	6414	Read Status 2
SRS1	6415	Read Status 1
SLFL	6413	Load Field
SSBE	6416	Skip on Bus Error
SRCD	6417	Read Character Detected (if AC0=0) Maintenance Instruction (if AC0=1)
SSTO	6403	Skip if Transmit Word Count Overflows

DK8-EP Programmable Real Time Clock

Mnemonic Symbol	Octal Code	Operation
CLZE	6130	Clear Clock Enable Register per AC
CLSK	6131	Skip on Clock Interrupt
CLOE	6132	Set Clock Enable Register per AC
CLAB	6133	AC to Clock Buffer
CLEN	6134	Load Clock Enable Register
CLSA	6135	Clock Status to AC
CLBA	6136	Clock Buffer to AC
CLCA	6137	Clock Counter to AC

DK8-EC Crystal Clock

Mnemonic Symbol	Octal Code	Operation
CLEI	6131	Enable Interrupt
CLDI	6132	Disable Interrupt
CLSK	6133	Skip on Clock Flag and Clear Flag

KG8-EA Redundancy Check Option

Mnemonic Symbol	Octal Code	Operation
RCTV	6110	Test VRC and Skip
RCRL	6112	Read BCC Low
RCRH	6111	Read BCC High
RCCV	6113	Compute VRC
RCGB	6114	Generate BCC
RCLC	6115	Load Control
RCCB	6116	Clear BCC Accumulation

DB8-E Interprocessor Buffer

Mnemonic Symbol	Octal Code	Operation
DBRF	65X1	Skip if the receive set to a 1
DBRD	65X2	Read incoming data into the AC, clear receive flag
DBTF	65X3	Skip if the transmit flag is set to a 1
DBTD	65X4	Load the AC into the transmit buffer, transmit and set the transmit flag
DBEI	65X5	Enable the Interrupt Request line
DBDI	65X6	Disable the Interrupt Request Line
DBCD	65X7	Clear done flag

5X is the Device Code.

KL8-JA Terminal Control/Asynchronous Data Interface

Mnemonic Symbol	Octal Code	Operation
KCF	6030	Clear Receive Flag
KSF	6031	Skip on Keyboard Flag
KCC	6032	Clear Keyboard Flag and set Reader Run Flag
KRS	6033	Read Keyboard Status
KIE	6035 (AC11)	Set or clear Interrupt Enable AC11 = 1 set AC11 = 0 clear
KSE	6035 (AC10)	Set/Clear Status Enable AC10 = 1 Enable Status AC10 = 0 Disable Status
KRB	6036	Read Keyboard Buffer Combined KCC and KRS
TFL	6040	Set Transmit Flag
TSF	6041	Skip on Transmit Flag
TCV	6042	Clear Transmit Flag
TPC	6043	Load Print Buffer and Print
SPI	6045	Skip if Interrupt Enabled and Transmit or Receive Flag is set
TLS	6046	Print character. Combined TCF and TPC.

PC8-E Reader/Punch

Mnemonic Symbol	Octal Code	Operation
RPE	6010	Set Reader/Punch Interrupt Enable
RSF	6011	Skip on Reader Flag
RRB	6012	Read Reader Buffer
RFC	6014	Reader Fetch Character
RFC, RRB	6016	Read Buffer and Fetch New Character
PCE	6020	Clear Reader/Punch Interrupt Enable
PSF	6021	Skip on Punch Flag
PCF	6022	Clear Punch Flag
PPC	6024	Load Punch Buffer and Punch Character
PLS	6026	Load Punch Buffer Sequence

RK8-E Control and RK05 DECpack Drive

Mnemonic Symbol	Octal Code	Operation
DSKP	67X1	Disk skip on Flag
DCLR	67X2	Disk Clear
DLAG	67X3	Load Address and Go
DLCA	67X4	Load Current Address
DRST	67X5	Read Status Register
DLDC	67X6	Load Command Register
DMAN	67X7	Maintenance Instructions

7X is the Device Code.

TM8-E/F Control

Mnemonic Symbol	Octal Code	Operation
LWCR	6701	Load Word Count Register
CWCR	6702	Clear Word Count Register
LCAR	6703	Load Current Address Register
CCAR	6704	Clear Current Address Register
LCMR	6705	Load Command Register
LFGR	6706	Load Function Register
LDBR	6707	Load Data Buffer Register
RWCR	6711	Read Word Count Register
CLT	6712	Clear Transport
RCAR	6713	Read Current Address Register
RMSR	6714	Read Main Status Register
RCMR	6715	Read Command Register
RFSR	6716	Read Function Register & Status
RDBR	6717	Read Data Buffer
SKEF	6721	Skip if Error Flag
SKCB	6722	Skip if Not Busy
SKJD	6723	Skip if Job Done
SKTR	6724	Skip if Tape Ready
CLR	6725	Clear Controller and Master

TA8-E DECassette

Mnemonic Symbol	Octal Code	Operation
KCLR	67X0	Clear Status Register A and B
KSDR	67X1	Skip on Data Flag
KSEN	67X2	Skip on EOT/BOT, EOF, or Drive Empty
KSBF	67X3	Skip on Ready Flag
KLSA	67X4	Load Status A from the AC
KSAF	67X5	Skip on any flag or error
KGOA	67X6	Read Status A
KRSB	67X7	Read Status B

7X is the Device Code.

APPENDIX B
OMNIBUS SIGNAL LOCATOR

This Appendix contains a list of PDP-8/A signals and their corresponding Omnibus pin numbers. Figure B-1 illustrates these pin locations on the module.

Signal	Omnibus Pin	Signal	Omnibus Pin
+5 V	AA2	E L	DL2
	BA2	EMA0 L	AD2
	CA2	EMA1 L	AE2
MEM REFRESH (+5 V)	EH2	EMA2 L	AH2
	EJ2	F L	DJ2
+15 V	DA2	FSET L	DP2
-15 V	AB2	GROUND	AC1
	BB2	GROUND	AF1
	CB2	GROUND	AN1
	DB2	GROUND	AT1
+20 V	EA2	GROUND	AC2
	EE2	GROUND	AF2
	EX2	GROUND	AN2
	EP2	GROUND	AT2
-5 V	EM2	GROUND	BC1
BREAK CYCLE L	BL2	GROUND	BF1
BREAK DATA CONT L	BK2	GROUND	BN1
BRK IN PROG L	BE2	GROUND	BT1
BUS STROBE L	CK1	GROUND	BC2
C0 L	CE1	GROUND	BF2
C1 L	CH1	GROUND	BN2
C2 L	CJ1	GROUND	BT2
CPMA DISABLE L	CU1	GROUND	CC1
D L	DK2	GROUND	CF1
DATA0 L	AR1	GROUND	CN1
DATA1 L	AS1	GROUND	CT1
DATA2 L	AU1	GROUND	CC2
DATA3 L	AV1	GROUND	CF2
DATA4 L	BR1	GROUND	CN2
DATA5 L	BS1	GROUND	CT2
DATA6 L	BU1	GROUND	DC1
DATA7 L	BV1	GROUND	DF1
DATA8 L	DR1	GROUND	DN1
DATA9 L	DS1	GROUND	DT1
DATA10 L	DU1	GROUND	DC2
DATA11 L	DV1	GROUND	DF2

Signal	Omnibus Pin	Signal	Omnibus Pin
GROUND	DN2	MD10 L	DL1
GROUND	DT2	MD11 L	DM1
GROUND	EC1	MD DIR L	AK2
GROUND	EF1	MEM START L	AJ2
GROUND	EN1	MS, IR DISABLE L	CV1
GROUND	EC2	NOT LAST XFER L	CM1
GROUND	EF2	NTS STALL L	BR2
GROUND	EN2	OVERFLOW L	BJ2
GROUND	ET2	POWER OK H	BV2
IND1 L	CU2	PULSE LA H	DR2
IND2 L	CV2	RES	BS2
INHIBIT H	AP2	RETURN H	AR2
INITIALIZE H	CR1	ROM ADDRESS L	AU2
INT IN PROG H	BP2	RUN L	BU2
INT RQST L	CP1	SKIP L	CS1
INT STROBE H	BD2	SOURCE H	AL2
INTERNAL I/O L	CL1	STOP L	DS2
I/O PAUSE L	CD1	STROBE H	AM2
IR0 L	DD2	SW	DV2
IR1 L	DE2	TEST POINT	AA1
IR2 L	DH2	TEST POINT	AB1
KEY CONTROL L	DU2	TEST POINT	BA1
LA ENABLE L	BM2	TEST POINT	BB1
LINK DATA L	CR2	TEST POINT	CA1
LINK L	AV2	TEST POINT	CB1
LINK LOAD L	CS2	TEST POINT	DA1
MA0 L	AD1	TEST POINT	DB1
MA1 L	AE1	TEST POINT	EA1
MA2 L	AH1	TEST POINT	EB1
MA3 L	AJ1	TEST POINT	ED1
MA4 L	BD1	TEST POINT	EE1
MA5 L	BE1	TEST POINT	EH1
MA6 L	BH1	TEST POINT	EJ1
MA7 L	BJ1	TEST POINT	EK1
MA8 L	DD1	TEST POINT	EL1
MA9 L	DE1	TEST POINT	EM1
MA10 L	DH1	TEST POINT	EP1
MA11 L	DJ1	TEST POINT	ER1
MA, MS LOAD CONT L	BH2	TP1 H	CD2
MD0 L	AK1	TP2 H	CE2
MD1 L	AL1	TP3 H	CH2
MD2 L	AM1	TP4 H	CJ2
MD3 L	AP1	TS1 L	CK2
MD4 L	BK1	TS2 L	CL2
MD5 L	BL1	TS3 L	CM2
MD6 L	BM1	TS4 L	CP2
MD7 L	BP1	USER MODE L	DM2
MD8 L	DK1	WRITE H	AS2
MD9 L	DL1		

PIN	CONNECTOR, SIDE									
	E1	E2	D1	D2	C1	C2	B1	B2	A1	A2
A	TP	+20V	TP NOTE 5	+15V	TP NOTE 2	+5V	TP NOTE 3	+5V	TP NOTE 2	+5V
B	TP	NOT USED	TP	−15V	TP	−15	TP NOTE 4	−15V	TP	−15V
C	GND	GND	GND	GND	GND	GND	GND	GND	SP GND NOTE 1	GND
D	TP	NOT USED	MA8L	IRØL	I/O PAUSE L	TP1 H	MA4L	INT STROBE H	MAØ L	EMAØL
E	TP	+20V	MA9L	IR1L	CØL	TP2 H	MA5L	BRK IN PROG L	MA1L	EMA1L
F	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
H	TP	MEM REFRESH (+5V)	MA10L	IR2 L	C1L	TP3 H	MA6 L	MA,MS LOAD CONT L	MA2L	EMA2 L
J	TP	MEM REFRESH (+5V)	MA11L	FL	C2 L	TP4H	MA7L	OVERFLOW L	MA3 L	MEM START L
K	TP	+20V	MD8L	DL	BUS STROBE L	TS1 L	MD4 L	BREAK DATA CONT L	MDØ L	MD DIR L
L	TP	NOT USED	MD9L	EL	INTERNAL I/O L	TS2 L	MD5 L	BREAK CYCLE L	MD1L	SOURCE H
M	TP	−5V	MD10 L	USER MODE L	NOT LAST XFER L	TS3 L	MD6 L	LA ENABLE L	MD2 L	STROBE H
N	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
P	TP	+20V	MD11L	F SET L	INT ROST L	TS4 L	MD7L	INT IN PROG H	MD3 L	INHIBIT H
R	TP	NOT USED	DATA 8 L	PULSE LA H	INITIALIZE H	LINK DATA L	DATA 4 L	NTS STALL L	DATA ØL	RETURN H
S	NOT USED	NOT USED	DATA 9 L	STOP L	SKIP L	LINK LOAD L	DATA 5L	RES H	DATA 1L	WRITE H
T	JUMPER	GND	GND	GND	GND	GND	GND	GND	GND	GND
U	JUMPER	NOT USED	DATA 10 L	KEY CONTROL L	CPMA DISABLE L	IND 1 L	DATA 6 L	RUN L	DATA 2 L	ROM ADDRESS L
V	TP	NOT USED	DATA 11 L	SW	MS,IR DISABLE L	IND2 L	DATA 7L	POWER OK H	DATA 3 L	LINK L

Notes

1. This pin is connected to ground on the bus but serves as a logic signal within modules for testing.
2. Pins AA1 and CA1 in slot 1 supply +5 V to the CPU module.
3. Pin BA1 of slots 2 and 3 supplies BATTERY EMPTY to the option modules.
4. Pin BB1 of slots 2 and 3 supplies AC LOW to the option modules.
5. DA1 of slots 2 and 3 supplies PANEL LOCK to the option modules.

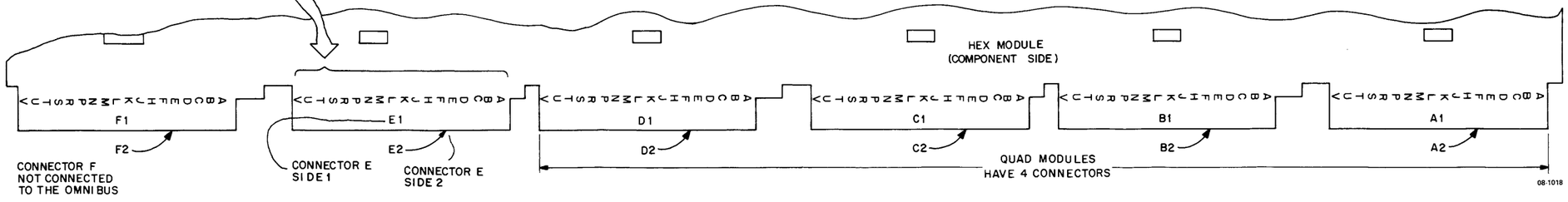


Figure B-1 Omnibus Signal Locator

APPENDIX C
MODULE ASSIGNMENT AND POWER REQUIREMENTS

Option	Description	Board Size	Slots Used	Assigned Slot No.	Current		
					+5 V	+15 V	-15 V
CM8-F	Card RDR Cont	Quad	1	4–20	0.55 A		
CR8-F	Card RDR Cont	Quad	1	4–20	0.55 A		
DB8-EA	Interproc Buffer	Quad	1	2–20	0.80 A		0.03 A
DK8-EC	RTC Crystal	Quad	1	2–20	0.34 A		
DK8-EP	RTC Prog	Quad	2	2–20	1.43 A		0.07 A
DKC8-A	Option 1	Hex	1	2–3	2.0 A	0.06 A	0.1 A
DP8-EA, -EB	Modem Interface	Quad	2	2–20	1.80 A	0.05 A	0.11 A
DR8-EA	Digital I/O	Quad	1	2–20	2.25 A		
KA8-E	Positive I/O	Quad	1	4–20	1.40 A		
KC8-AA, -AB	Prog Console	Pnl Mt	0	NA	2.5 A		
KD8-E	Data Break	Quad	1	4–20	1.2 A		
KG8-EA	Redundancy Check	Quad	1	4–20	0.94 A		
KK8-A	CPU	Hex	1	1	5.0 A		0.04 A
KL8-JA	Async Data Chart	Quad	1	2–20	1.1 A	0.05 A	0.10 A
KL8-M	Modem Control	Quad	1	2–20	0.40 A	0.04 A	0.04 A
KM8-A	Option 2	Hex	1	2–3	2.0 A		
KM8-E	Mem Ext and TS Cont	Quad	1	4–20	1.0 A		
LE8-XX	Line Printer Cont	Quad	1	2–20	0.35 A		
LS8-F	Line Printer Cont	Quad	1	2–20	0.40 A		
MM8-AA	8K Core, Operating	Hex	2	4–11	2.5 A		
MM8-AA	8K Core, Standby	Hex	2	4–11	2.5 A		
MM8-AB	16K Core, Operating	Hex	2	4–11	2.5 A		
MM8-AB	16K Core, Standby	Hex	2	4–11	2.5 A		
MR8-AA	1K ROM	Quad	1	2–20	2.0 A		
MR8-AB	2K ROM	Quad	1	2–20	3.0 A		
MR8-AC	3K ROM	Quad	1	2–20	4.0 A		
MR8-AD	4K ROM	Quad	1	2–20	5.0 A		
MR8-FB	1K PROM	Quad	1	2–20	3.8 A		0.35 A
MS8-AA	1K RAM	Quad	1	4–20	1.4 A		
MS8-AB	2K RAM	Quad	1	4–20	2.1 A		
MS8-AC	3K RAM	Quad	1	4–20	2.8 A		
MS8-AD	4K RAM	Quad	1	4–20	3.5 A		

Option	Description	Board Size	Slots Used	Assigned Slot No.	Current		
					+5 V	+15 V	-15 V
PC8-E, PR8-E	RDR/Punch Control	Quad	1	4–20	0.84 A		0.05 A
RX8-E	RX01 Control	Quad	1	4–20	1.5 A		
RK8-EA	RK05 Control	Quad	3	4–20	3.10 A		
TA8-AA	TU60 Control	Quad	1	2–20	2.80 A		
TA8-EA, -FA	TU10 Control	Quad	4	4–20	4.10 A		
VC8-E	Display Control	Quad	2	2–20	0.31 A		
VT8-E	Display Control	Quad	3	4–20	3.70 A	0.09 A	0.13 A
XY8-E	Plotter Control	Quad	1	4–20	0.42 A	0.01 A	0.03 A
KK8-E	M8300, Major Reg	Quad	1	18	1.7 A		
	M8310, Major Reg Cont	Quad	1	19	0.60 A		
	M8330, Timing Gen	Quad	1	20	1.2 A		
	M8320, Bus Load	Quad	1	1	1.0 A	1.0 A	0.53 A
AD8-A	A/D Conv	Quad	1	4–20			
FPP8-A	Floating Point	Hex	2	4–20	8.8 A		
KE8-E	M8340, EAE IR		1	19	1.6 A		
	M8341, EAE Reg		1	18			
KL8-A	MSLU	Hex	1	4–20	2.5 A	0.09 A	0.425 A
LA8-P	LA180 Cont	Quad	1	4–20	1.0 A		
MI8-E	Boot Loader	Quad	1	4–20	0.75 A		0.05 A
RK8-L	RK05 Cont	Quad	1	4–20	4.0 A		
TD8-E	TU56 Cont	Quad	1	4–20	1.3 A		
TM8-E	TU10 Cont	Quad	4	4–20	4.2 A		
VK8-A	Video Display Cont	Hex	1	4–20	2.8 A		

APPENDIX D
PROGRAM LOADING PROCEDURES

INTRODUCTION

This appendix provides the user with procedures to accomplish the following:

1. Turn the system on.
2. Load the Read In Mode (RIM) program. RIM must be in memory to load tapes from the high or low speed paper-tape readers.
3. Load the Binary (BIN) loader – The Binary loader is a program that is used to load the programs punched in BIN format on paper tapes into memory.
4. Load BIN paper tapes using the Binary loader.

NOTE

RIM and BIN paper-tape formats are discussed in Chapter 4 of the Introduction to Programming Handbook.

D.1 TURNING THE SYSTEM ON

Before using the computer system, it is good practice to initialize all units. Ensure that all switches and controls are as specified below:

1. Main power cord is properly plugged in.
2. Teletype is turned to ON-LINE.
3. Low-speed punch is OFF.
4. Low-speed reader is set to FREE.
5. Computer POWER ON.
6. Console LOCK OFF (set to down).
7. Ensure any peripherals supplied with the system are turned on. Refer to the maintenance manual supplied with the equipment for the startup procedures.

The system is now initialized and ready for use.

D.2 READ-IN MODE (RIM) LOADER

The RIM Loader is the very first program loaded into the computer; it is loaded by using the console switches or the BOOT switch. Operating the BOOT switch causes a RIM program, contained in a ROM ON on the extend option module to be deposited in memory. The RIM loader instructs the computer to receive and store in memory, data punched on paper tape in RIM coded format. (The RIM Loader is used to load the BIN loader described in the next paragraph.)

There are two RIM loader programs: one is used when the input is to be from the low-speed Teletype reader, and the other is used when input is to be from the high-speed paper-tape reader. The locations and corresponding instructions for both loaders are listed in Table D-1.

Table D-1
RIM Loader Programs

Location	Instruction	
	Low-Speed Reader	High-Speed Reader
7756	6032	6014
7757	6031	6011
7760	5357	5357
7761	6036	6016
7762	7106	7106
7763	7006	7006
7764	7510	7510
7765	5357	5374
7766	7006	7006
7767	6031	6011
7770	5367	5367
7771	6034	6016
7772	7420	7420
7773	3776	3776
7774	3376	3376
7775	5356	5357
7776	0000	0000
7777	0000	0000

The procedure for loading (keypadding) the RIM loader into memory using the Programmer's Console is as follows:

NOTE

On systems with an extended option module selected for paper tape bootstrap, the user can press BOOT on the Programmer's Console twice and the RIM program is loaded automatically. Then go on to the procedure to load the BINARY loader.

1. Press MD and then DISP to display the contents of the MD in the four character octal readout.

2. Enter the field that RIM is to be loaded into twice (i.e., if field 7 is being used, enter 77). Press LXA (load extended address).

3. Enter 7756 and then press LOAD ADDRESS (LA) to load the starting address.

4. Enter the first instruction from Table D-1 for the low-speed reader or high-speed reader, and press D NEXT.

5. Enter the remaining instructions from Table D-1; press D NEXT after each entry.

6. After all of the instructions have been entered, enter the starting address 7756 and press LA.

7. Check the entries you have made in the first 5 steps. To examine the first location, enter 7756 and then press E NEXT. The numbers displayed in the four character octal readout should correspond to the first number entered from Table D-1.

8. Press E NEXT and the second number from Table D-1 will be displayed. Check each instruction by observing the number. If any errors are found, enter the address and press LA and the correct number using the keypad switches and then press D NEXT.

9. After RIM has been loaded and checked, follow the instructions for loading the binary loader.

D.3 BINARY (BIN) LOADER

The BIN loader is a short utility program which instructs the computer to read binary coded data punched on paper tape and store it in memory. BIN is used primarily to load the programs furnished in the software package (excluding the loaders and certain subroutines) and the programmer's binary tapes.

BIN is furnished to the programmer on punched paper tape in RIM coded format. Therefore, RIM must be in memory before BIN can be loaded. The procedure for loading the binary loader is as follows:

1. Press MD and then DISP to display the contents MD lines in the four character octal readout.

2. Enter the memory field into which RIM was loaded followed by the field into which BIN is to be loaded, and then press LXA.

3. Enter 7756 and press LA. 7756 is the starting address of the RIM Loader program.

NOTE

Systems with high-speed readers perform steps 4 and 5; systems with low-speed readers perform steps 6 and 7.

4. Turn high-speed reader on.

5. Put the Binary loader tape in the right hand side of high-speed reader with the printed arrows up and pointing to the left (proceed to step 8).

6. Set the TTY to LINE.

7. Put the Binary loader tape in the low-speed reader with the printed arrows up and pointing toward you. Set the low-speed reader lever to START.

8. Press INIT and RUN. The tape should read in. If the tape does not read in, go back to step 1 to be certain an operator error was not the reason the tape did not read in.

9. If the tape reads in, press HLT/SS when trailer (single row of holes) passes under the read head.

10. Enter the field the Binary loader was loaded into and press LXA.

11. Enter 7777 and press LA.

12. Press E THIS.

13. The MD should read 5301. If it does not, go back to step 1 and repeat the procedure.

When stored in memory, BIN resides on the last page of core occupying absolute locations 7625 through 7752 and location 7777.

BIN was purposely placed on the last page of core so that it would always be available; most of the programs in DIGITAL's software package do not use the last page of memory. The programmer must be aware that if he or she writes a program that uses the last page of memory, BIN will be overwritten when the program runs on the computer. When this happens, the programmer must load RIM and then BIN before loading binary tape.

D.4 LOADING BINARY TAPES

The procedure for loading binary tapes is as follows:

1. Verify that the BINARY loader has been loaded.

2. Press AC and then DISP.

3. Enter the field into which the BINARY loader was loaded, and then enter the field into which binary tape is to be loaded. Press LXA.

4. Enter 7777 and press LA.

NOTE

Perform steps 5 and 6 for low-speed readers and steps 8, 9, and 10 for high-speed readers.

5. Turn TTY to line and put the tape in the low-speed reader, ensuring that the leader (code 200) is in the reader. The tape moves from back to front; the printed arrows on the tape should be up and pointing toward you.

6. Enter 7777 and press LSR.

7. Set low-speed reader to START. Proceed to step 11.

8. Turn high-speed reader on.

9. Enter 3777 and press LSR.

10. Put the tape in the high-speed reader, ensuring the leader (code 200) is in the reader. The tape moves from right to left; the printed arrows on the tape should be up and pointing left.

11. Press AC and then DISP.

12. Press INIT and then RUN.

13. The tape should read in and stop at the first trailer code (not the physical end of tape), with the AC equal to 0000. In case of difficulty, go back to step 1. Problems with reader motion are usually caused by not loading the BIN loader correctly. Checksum errors (AC not equal to 0) are often the result of worn tapes.

APPENDIX E
ASCII[1] CHARACTER CODES

Character	8-Bit Octal	6-Bit Octal	Decimal Equivalent (All Format)
A	301	01	96
B	302	02	160
C	303	03	224
D	304	04	288
E	305	05	352
F	306	06	416
G	307	07	480
H	310	10	544
I	311	11	608
J	312	12	672
K	313	13	736
L	314	14	800
M	315	15	864
N	316	16	928
O	317	17	992
P	320	20	1056
Q	321	21	1120
R	322	22	1184
S	323	23	1248
T	324	24	1312
U	325	25	1376
V	326	26	1440
W	327	27	1504
X	330	30	1568
Y	331	31	1632
Z	332	32	1696
0	260	60	-992
1	261	61	-928
2	262	62	-864
3	263	63	-800
4	264	64	-736
5	265	65	-672
6	266	66	-608
7	267	67	-54
8	270	70	-480
9	271	71	-416

[1]An abbreviation for American Standard Code for Information Interchange.

Character	8-Bit Octal	6-Bit Octal	Decimal Equivalent (All Format)
!	241	41	-1952
"	242	42	-1888
#	243	43	-1824
$	244	44	-1760
%	245	45	-1696
&	246	46	-1632
'	247	47	-1568
(	250	50	-1504
)	251	51	-1440
*	252	52	-1376
+	253	53	-1312
,	254	54	-1248
-	255	55	-1184
.	256	56	-1120
/	257	57	-1056
:	272	72	-352
;	273	73	-288
<	274	74	-224
=	275	75	-160
>	276	76	-96
?	277	77	-32
@	300		32
[	333	33	1760
\	334	34	1824
]	335	35	1888
↑(↑)[2]	336	36	1952
<(-)[2]	337	37	2016
Leader/Trailer	200		
LINE FEED	212		
Carriage RETURN	215		
SPACE	240	40	-2016
RUBOUT	377		
Blank	000		
BELL	207		
TAB	211		
FORM	214		

[2]The character in parenthesis is printed on some teletypes.

APPENDIX F
DEVICE CODES

The device codes for PDP-8/A options and peripherals are listed in Table F-1.

Table F-1
Device Codes

Option Designation	Option Name	Device Code
CM8-E	Optical Mark Card Reader	63,67
CR8-F	Card Reader	63,67
DB8-EA	Interprocessor Buffer	50,51,52,53,54,55,56,57*
DK8-EC	Crystal Clock	13
DK8-EP	Programmable Real Time Clock	13
DKC8-AA	I/O Option Board	
	Serial Line Unit	03 Receive,04 Transmit
	General Purpose Parallel I/O	57
	Real Time Crystal Clock	13
DP8-EA,EB	Synchronous Modem	40,41,42,43,45,46,47**
DR8-EA	12 Bit Digital I/O	50,51,52,53,54,55,56,57*
KA8-E	Positive I/O Bus Interface	The sum of the device codes for all external bus devices
KD8-E	Data Break Interface	None
KG8-EA	BCC Generator/Detector	11
KK8-A	Central Processor Unit (CPU)	None
KL8-JA	Asynchronous Device Interface	User defined in range 00-77 (2)
KL8-M	Modem Control used with KL8E or KL8J	
KM8-A	Extended Option Module	
	Memory Extension	00,20-27
	Time Share	20-27
	Power Fail	10
LE8-E	Line Printer Control	66
LS8-F	Line Printer Control	66
PC8-E, PR8-E	Paper Tape Reader/Punch	Reader 01 Punch 02
RK8-EA	RK05 Disk Control	74
TA8-AA	TU60 Cassette Tape Transport Control	70,71,72,73,74,75,76,77*
TM8-EA-FA	DECmagtape Control	70,71,72
TD8-E	DECtape Control	77,76,75,74*
VC8-E	Point Plot Display Control	05
VT8-E	High Speed Display Terminal and Control	Any device code not assigned (3)
XY8-E	XY Plotter Control	50
AD8-A	Analog/Digital converter	Any device code not assigned

*Any one
**Any two contiguous, even-odd, e.g., 40/41

APPENDIX G
MEMORY CYCLE TIME SUMMARY

Memory Configuration	Fetch Major State	All other
ROM only	1.5 μs	1.5 μs
ROM/RAM(ROM Cycle)	1.6 μs	1.6 μs
ROM/RAM	2.7 μs	3.1 μs
RAM only	2.4 μs	2.8 μs
MR8-FB PROM	3.4 μs	3.7 μs
Core Memory	1.5 μs	1.5 μs

APPENDIX H
ENGINEERING DRAWINGS

This appendix contains assembly drawings, schematic drawings, flow diagrams, and timing diagrams. They are arranged in the order indicated by the list that follows. Those that relate to a particular computer are listed with that computer, while those that apply to all computers are listed under "General."

PDP-8/A Semiconductor

Title	Drawing Number
PDP-8/A Unit Assembly	D-UA-PDP-8A-0-0
Connector Block Assembly	D-CS-H9192-0-1
Connector Block Assembly	D-AD-H9192-0-0
Power Supply Assembly	E-UA-H763-0-0
Limited Function Board	D-CS-5411168-0-1
Regulator Board G8016	D-CS-G8016-0-1
Power Board Assembly	D-CS-5410968-0-1
4K X 12 MOS Memory (MS8-A)	D-CS-M8311-0-1
ROM (MR8-A)	D-CS-M8312-0-1
PROM 1K (MR8-F)	D-CS-M8349-0-1

8A400/600/800

Chassis Assembly, H9300	D-UA-H9300-0-0
Connector Block Assembly	D-CS-H9194-0-1
Connector Block Assembly	D-AD-H9194-0-0
Limited Function Board	D-CS-5411507-0-1
Regulator Board 8 A Core	D-CS-G8018-0-1
Core Memory Stack, 8K	D-CS-5411531-0-1
Core Memory Stack, 16K	D-CS-5411531-YA-1
8K, 12-bit Base Board	D-CS-G649-0-1
16K, 12-bit Base Board	D-CS-G650-0-1

Unit Assembly, BA8-C	E-UA-BA8-C-0
BA8-C Power Distribution Board	D-CS-5412000-0-1
Wall Assembly, BA8-C Center	E-AD-7012561-0-0
Backplane, 20-slot	D-AD-H9195-0-0
Limited Function Board	D-CS-5411507-0-1 (See 8A400)
Regulator Board 8 A Core	D-CS-G8018-0-1 (See 8A400)
Core Memory Stack, 8K	D-CS-5411531-0-1 (See 8A400)
Core Memory Stack, 16K	D-CS-5411531-YA-1 (See 8A400)
8K, 12-bit Base Board	D-CS-G649-0-1 (See 8A400)
16K, 12-bit Base Board	D-CS-G650-0-1 (See 8A400)

General

Title	Drawing Number
Hex Omnibus CPU	D-CS-M8315-0-1
Flow Diagram M8315, FC1	D-FD-M8315-0-17
Flow Diagram M8315, FC2	D-FD-M8315-0-18
Flow Diagram M8315, FC3	D-FD-M8315-0-19
Flow Diagram M8315, FC4	D-FD-M8315-0-20
Flow Diagram M8315, FC5	D-FD-M8315-0-21
Flow Diagram M8315, FC6	D-FD-M8315-0-22
Flow Diagram M8315, FC7	D-FD-M8315-0-23
Flow Diagram M8315, FC8	D-FD-M8315-0-24
Flow Diagram M8315, FC9	D-FD-M8315-0-25
Flow Diagram M8315, FC10	D-FD-M8315-0-26
Flow Diagram M8315, Bus Timing	D-FD-M8315-0-27
8 A Internal Option 1	D-CS-M8316-0-1
Option Board 2	D-CS-M8317-0-1
Auto-Restart, Bootstrap Start-up Sequence	D-TD-KM8-A-4
Bootstrap Timing Diagram	D-TD-KM8-A-5
Flow Chart for Option Board 2, M8317	D-FD-KM8-A-6

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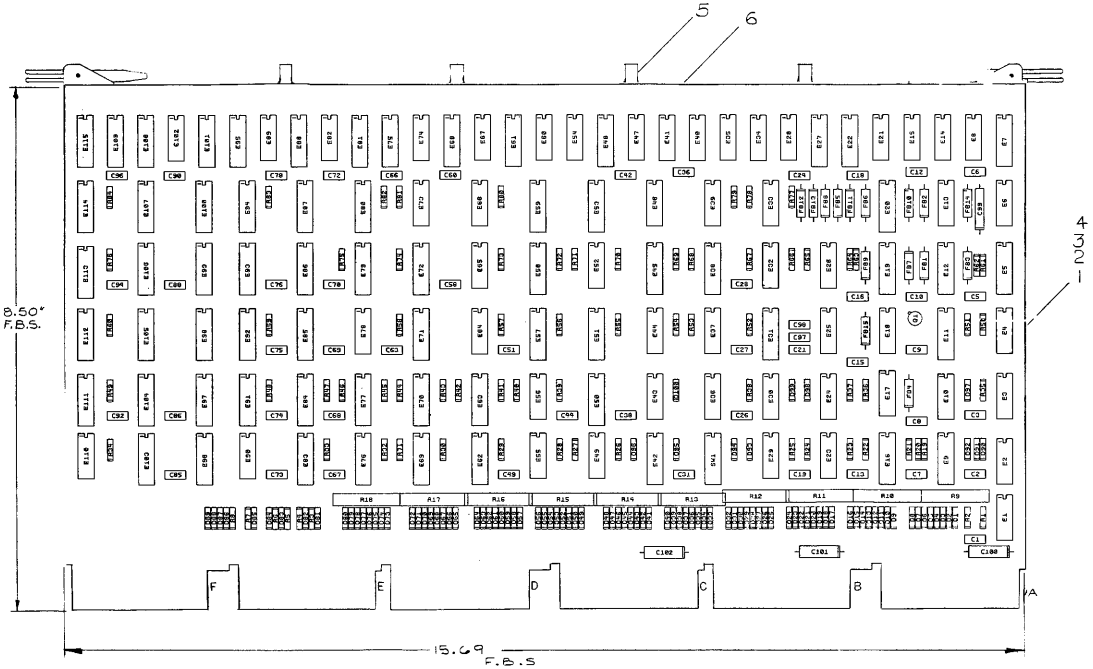
NOTES:

1. ALL UNLABELED DIODES ARE DEC TYPE D664
2. +3V, +3VA AND +3VB GENERATION ON SHEET # 8
3. ~~FOR ETCH CUTS REFER TO D-AH-M8315-0-5~~
4. ~~9 ETCH CUTS~~



GND. CONNECTION—PINS C,F,N,T ON CONNECTORS (A1, A2 / B1, B2 / C1, C2 / D1, D2) (AA1, AA2, BA2, CA1, CA2) +5V 6.8 µf .01 µf GND FOR ALL 6.8 µf & .01 µf CAPS

IC 74157	8	16
74S158	8	16
74163	8	16
74S175	8	16
74S194	8	16
380	1	8
8097	8	16
8235	8	16
8254	8	16
8271	8	16
8T10	8	16
256 BIT ROM	8	16
IC TYPE	GND	+5V

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

1024 BIT ROM	8	16
7442	8	16
7483	12	5
74120	8	16
74123	8	16
74S139	8	16
74151	8	16
74153	8	16
IC TYPE	GND	+5V

REF		DESCRIPTION	PART NO.	ITEM NO.
REF		X-Y COORDINATE HOLE LOCATION	K-CO-M8315-0-4	1
REF		ASSY/DRILLING HOLE LAYOUT	D-AH-M8315-0-5	2
REF		MODULE ECO HISTORY	8-MH-8315-0-6	3
1		ETCHED CIRCUIT BOARD	5010932	4
1		HEX BOARD HANDLE ASSY	1210711-2	5
12		EYELETS	9006732	6
3	C100 THRU C102	CAP 6.8uf 35V 10%	1005306	7
2	C97,C98	CAP .047uF 16V DISC	1009878	8
1	C99	CAP 15uf 20V 10%	1004812	9
48	C1 THRU C3,C5 THRU C10, C12,C13,C15,C16,C18,C19, C21,C24,C26,C27,C28,C31, C36,C38,C42,C44,C49,C51, C58,C60,C63,C66 THRU C70, C72 THRU C76,C79,C85,C86, C88,C90,C92,C94,C95	CAP .01uf 100V DISC	1001610-01	10
8	D86 THRU D92,D97	DIODE D662	1100113	11
92	D1 THRU D85,D93 THRU D96, D98 THRU D100	DIODE D664	1100114	12
1	SW1	DIP SWITCH PACKAGE	1211164-04	13
11	R2,R5,R6,R8,R19,R36,R62 THRU R66	RES 390 1/4W 5%	1300309	14
12	R1,R3,R4,R7,R20,R21,R23 THRU R26,R35,R37	RES 470 1/4W 5%	1300316	15
45	R22,R27,R29 THRU R34,R39 THRU R49,R52,R53,R55 THRU R60,R67 THRU R84	RES 1K 1/4W 5%	1300365	16
1	R28	RES 3.3K 1/4W 5%	1300439	17
1	R61	RES 22K 1/4W 5%	1301808	18
2	R50,R51	RES 27 1/4W 5%	1301522	19
5	R9,R10,R13,R14,R18	RES PACK 390 OHM	1312114-00	20
5	R11,R12,R15,R16,R17	RES PACK 470 OHM	1312114-01	21
2	R38,R54	RES 150 1/4W 5%	1300250	22
1	Q1	TRANSISTOR DEC 3009B	1503100	23
15	FB1 THRU FB15	FERRITE BEAD CHOKE	1611257-01	24
1	E2	20 MHZ X'TAL OSC	1811660-00	25
6	E1,E10,E17,E26,E29,E46	IC DEC 74S00	1910532	26
1	E33	IC DEC 7402	1909004	27
9	E3,E23,E25,E40,E56,E78, E82,E89	IC DEC 74S04	1910534	28
3	E47,E85,E74	IC DEC 7408	1910155	29
3	E24,E64,E90	IC DEC 74S10	1910536	30
2	E13,E28	IC DEC 74S11	1910537	31
1	E60	IC DEC 7412	1909955	32
3	E44,E49,E52	IC DEC 7417	1909929	33
2	E110,E102	IC DEC 74H21	1909058	34
1	E54	IC DEC 7430	1905578	35
3	E41,E43,E66	IC DEC 7432	1911521	36
1	E14	IC DEC 7437	1910091	37
2	E18,E32	IC DEC 74S40	1910541	38
1	E71	IC DEC 7442	1910046	39
2	E4, E6	IC DEC 74S51	1911712	40
4	E8,E75,E21,E34	IC DEC 74S74	1910544	41
3	E95,E101,E113	IC DEC 7483	1909932	42
3	E19,E22,E27	IC DEC 74120	1911314	43
1	E7	IC DEC 74123	1910436	44
2	E20,E58	IC DEC 74S139	1911678	45
2	E48,E59	IC DEC 74151	1909936	46
1	E45	IC DEC 74153	1909937	47

PARTS LIST

FIRST USED ON OPTION MODEL: -CS A

ETCH BOARD REV. E

REV	CHANGE NO.	CHK
C	M8315-00001	
D	M8315-00003	
E	M8315-00004	

DRN. L. KLOTZ 10/25/74
CHK'D 10/11/74
ENG.
PROJ. ENG.
PROD.
NEXT HIGHER ASSY A-PL-KK-A-0
SCALE
SHEET 1 OF 10

digital

TITLE: HEX OMNIBUS CPU

SIZE D | CODE CS | NUMBER M8315-0-1 | REV E

DST.

DEC NO. EIA NO. DEC NO. EIA NO.

SEMICONDUCTOR CONVERSION CHART

M8315-0-1 REV E

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1	E51	IC DEC 74157	1910655	48
7	E68,E79,E88,E95,E101,E109, E115	IC DEC 74S158	1910549	49
3	E75,E93,E94	IC DEC 74163	1911713	50
2	E5,E42	IC DEC 74S175	1910957	51
8	E9,E11,E12,E16,E81,E99,E100 E114	IC DEC 74S194	1910552	52
1	E38	IC DEC 380	1909405	53
2	E67,E73	IC DEC 8093	1910837	54
4	E77,E84,E104,E105	IC DEC 8097	1911527	55
3	E80,E86,E98	IC DEC 8234	1911315	56
3	E81,E87,E92	IC DEC 8235	1909835	57
1	E31	IC DEC 8271	1909615	58
5	E30,E35,E37,E39,E55	IC DEC 8881	1909705	59
11	E50,E62,E83,E91,E96,E97, E103,E106,E108,E111,E112	IC DEC 8T10	1911711	60
1	E69	256 BIT ROM (A)	23078A1	61
1	E57	256 BIT ROM (B)	23077A1	62
1	E70	256 BIT ROM (C)	23076A1	63
1	E72	256 BIT ROM (D)	23075A1	64
1	E76	256 BIT ROM (E)	23074A1	65
1	E83	256 BIT ROM (H)	23073A1	66
1	E38	256 BIT ROM (J)	23079A1	67
1	E53	1024 BIT ROM (F)	23080A2	68
~~C~~	~~WIRE~~	~~30AWG GREEN~~	~~9103740-05~~	~~69~~

SWITCH SELECTION CHART
(FOR AUTO RESTART LOCATION)

SW1–		
1	FIELD 7	
2	1000	ONLY ONE SWITCH MAY BE CLOSED AT A TIME
3	2000	
4	1000	
5	400	
6	200	
7	OFF (DISABLES AUTO RESTART)	
8	OFF FOR NORMAL OPERATION	

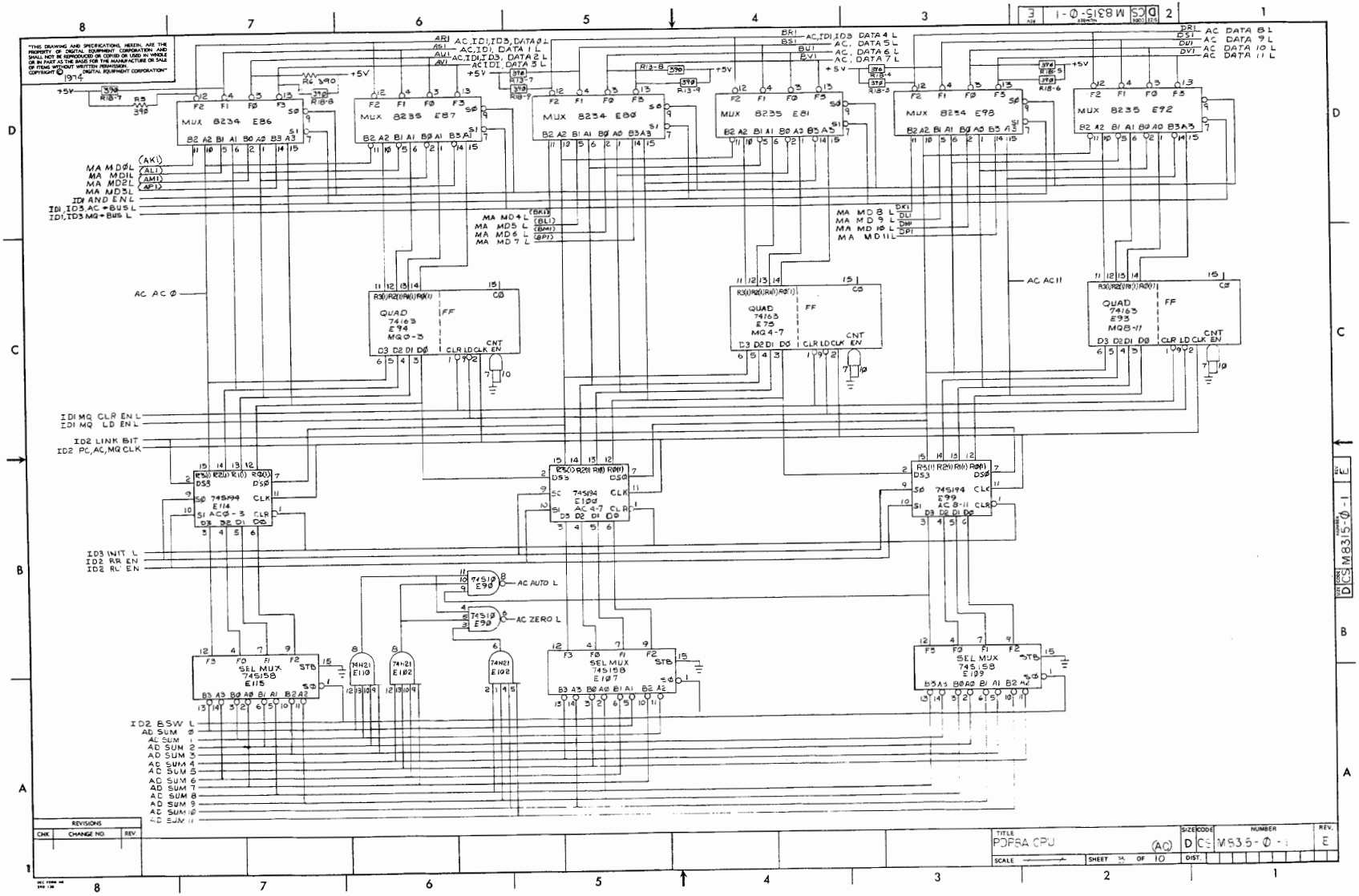
COMPONENT SUBSTITUTION CHART

PART CALLED FOR			SUBSTITUTE PART		
QTY	PART NO	DESC	QTY	PART NO	DESC.
1	1909485	IC 380	1	1910392	5380
			1	1909971	6380
			1	1910390	7380
			1	1911469	8640

REVISIONS

CHK	CHANGE NO	REV

TITLE: HEX OMNIBUS CPU
SIZE D | CODE DCS | NUMBER M8315-0-1 | REV E
SCALE | SHEET 2 OF 10 | DIST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MUX 8234 E86
MUX 8235 E87
MUX 8234 E80
MUX 8235 E81
MUX 8234 E98
MUX 8235 E92
QUAD 74163 E94 MQ0-3
QUAD 74163 E75 MQ4-7
QUAD 74163 E93 MQ8-11
SEL MUX 74S158 E115
SEL MUX 74S158 E107
SEL MUX 74S158 E109
74H21 E110
74H21 E102
74S10 E96
74S10 E90
AC AUTO L
AC ZERO L
MA MD0L
MA MD1L
MA MD2L
MA MD3L
MA MD4L
MA MD5L
MA MD6L
MA MD7L
MA MD8L
MA MD9L
MA MD10L
MA MD11L
AC AC0
AC AC11
ID1 MQ CLR EN L
ID1 MQ LD EN L
ID2 LINK BIT
ID2 PC,AC,MQ CLK
ID3 INIT L
ID2 RR EN
ID2 RL EN
ID2 BSW L
AD SUM 0
AD SUM 1
AD SUM 2
AD SUM 3
AD SUM 4
AD SUM 5
AD SUM 6
AD SUM 7
AD SUM 8
AD SUM 9
AD SUM 10
AD SUM 11
REVISIONS
CHK
CHANGE NO.
REV.
TITLE
PDP8A CPU (AC)
SIZE
CODE
NUMBER
REV.
D
CS
M835-0-1
E
SCALE
SHEET 14 OF 10
DIST.
DEC FORM NO 240 136

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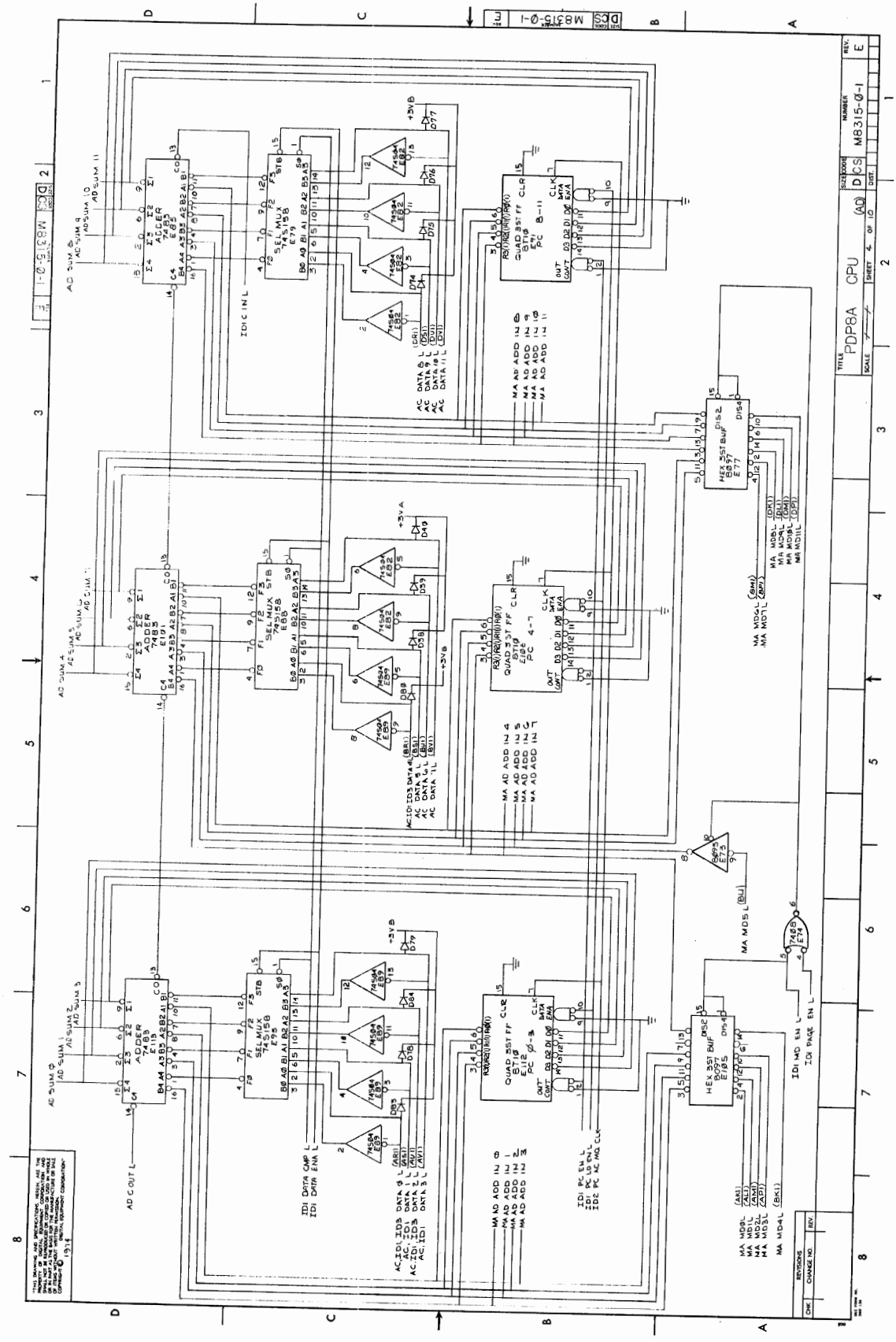

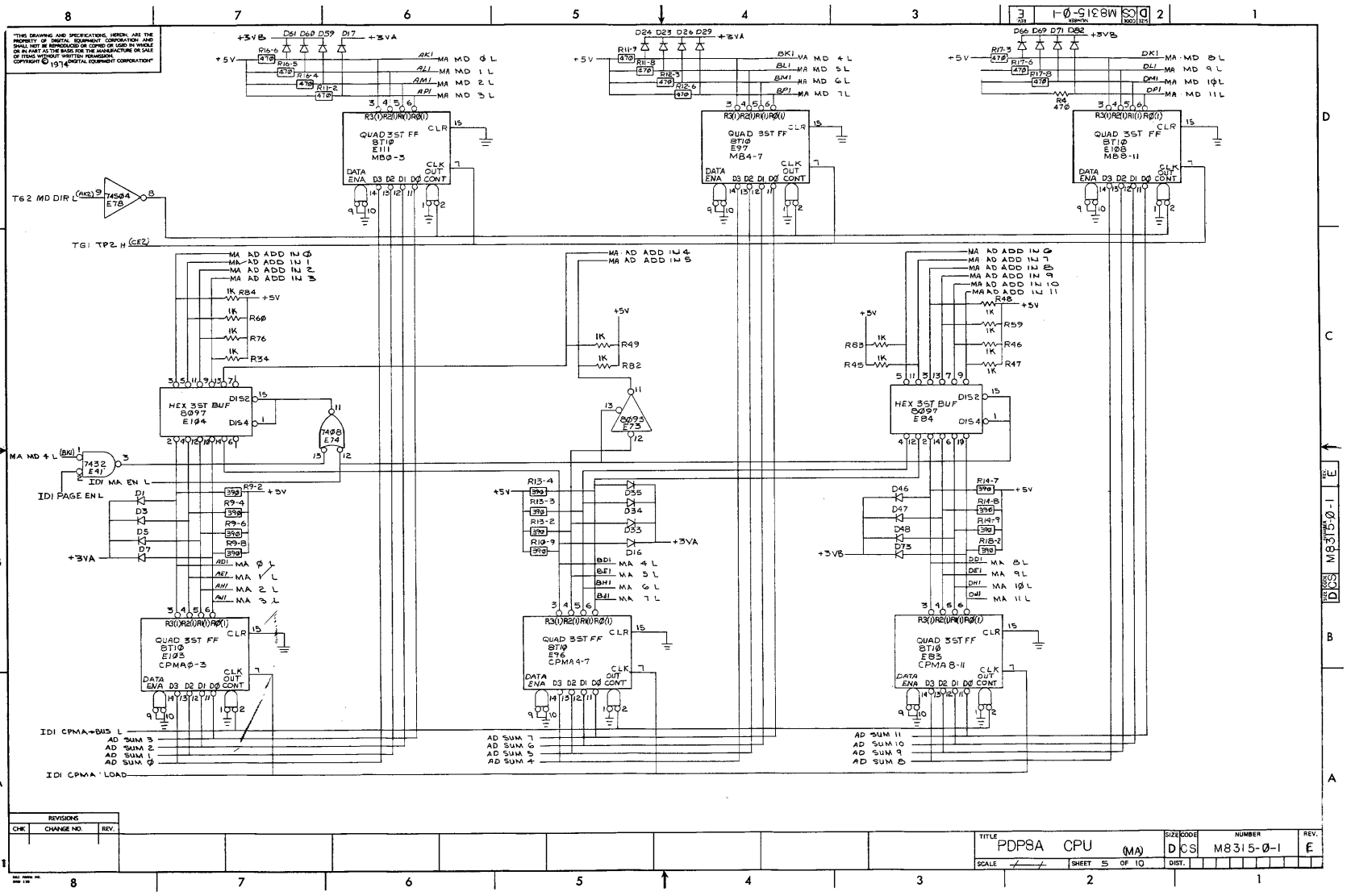
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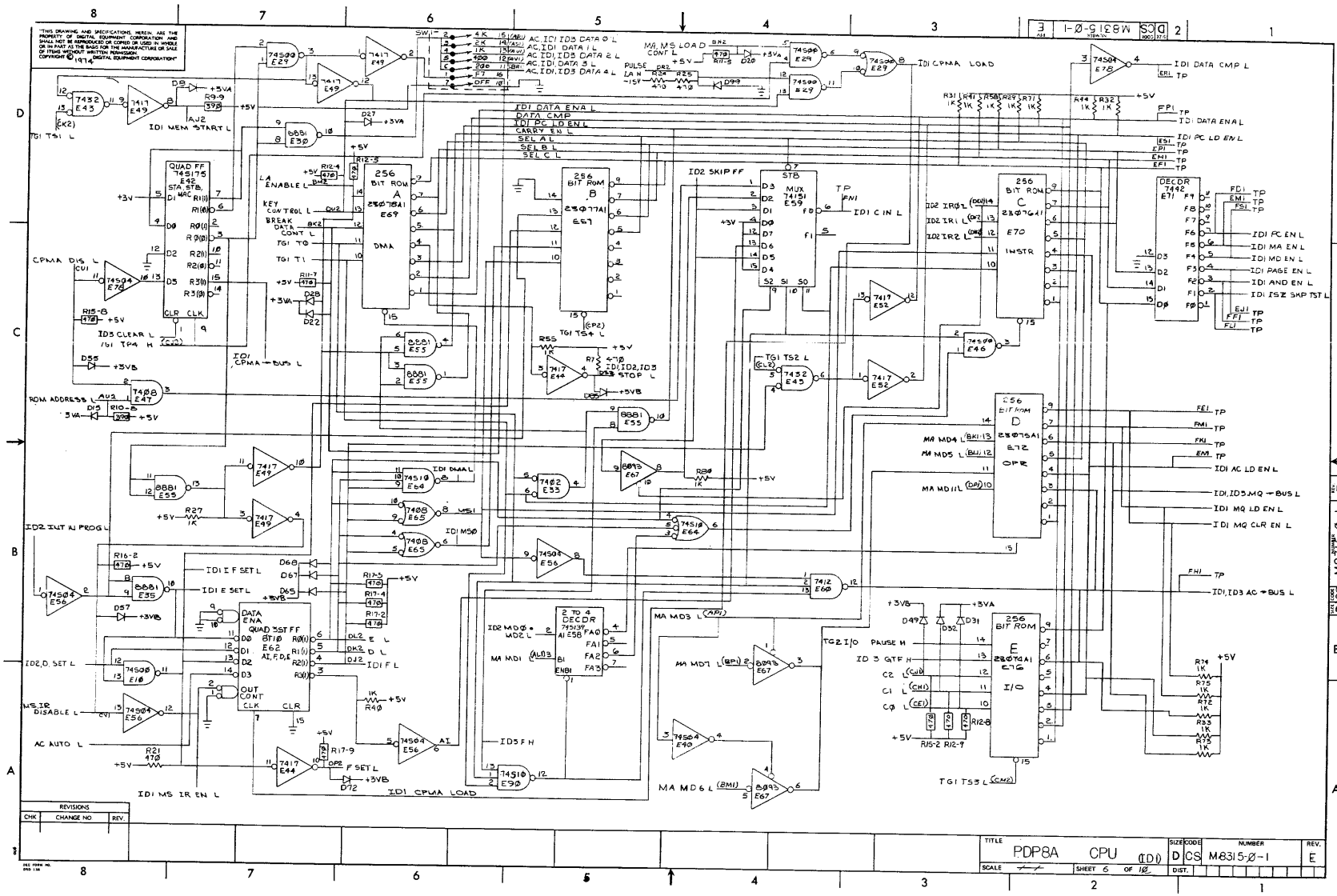
M8315-Ø-1
+3VB
+3VA
+5V
D61 D60 D59 D17
D24 D23 D26 D29
D66 D69 D71 D82
R16-6
R16-5
R16-4
R11-2
R11-9
R11-8
R12-3
R12-6
R17-9
R17-6
R17-3
R4
470
AK1 MA MD Ø L
AL1 MA MD 1 L
AM1 MA MD 2 L
AP1 MA MD 3 L
BK1 MA MD 4 L
BL1 MA MD 5 L
BM1 MA MD 6 L
BP1 MA MD 7 L
DK1 MA MD 8 L
DL1 MA MD 9 L
DM1 MA MD 10 L
DP1 MA MD 11 L
R3()R2()R1()R0()
QUAD 3ST FF
8T10
E111
MB0-3
E97
MB4-7
E105
MB8-11
CLR
CLK
DATA ENA D3 D2 D1 D0 CONT OUT
T62 MD DIR L (AK2)
74S04
E78
TG1 TP2 H (CE2)
MA AD ADD IN Ø
MA AD ADD IN 1
MA AD ADD IN 2
MA AD ADD IN 3
MA AD ADD IN 4
MA AD ADD IN 5
MA AD ADD IN 6
MA AD ADD IN 7
MA AD ADD IN 8
MA AD ADD IN 9
MA AD ADD IN 10
MA AD ADD IN 11
1K R84
1K R60
1K R76
1K R34
1K R49
1K R82
1K R48
1K R59
1K R46
1K R47
1K R83
1K R45
HEX 3ST BUF
8097
E104
E84
DIS2
DIS4
7408
E74
8095
E73
MA MD 4 L (BK1)
7432
E41
IDI MA EN L
IDI PAGE EN L
R9-2
R9-4
R9-6
R9-8
390
D1
D3
D5
D7
ADI MA Ø L
AEI MA 1 L
AHI MA 2 L
AMI MA 3 L
R13-4
R13-3
R13-2
R10-9
D35
D34
D33
D16
BDI MA 4 L
BEI MA 5 L
BHI MA 6 L
BMI MA 7 L
D46
D47
D48
D73
R14-7
R14-8
R14-9
R18-2
DDI MA 8 L
DEI MA 9 L
DHI MA 10 L
DMI MA 11 L
CPMAØ-3
CPMA4-7
CPMA8-11
IDI CPMA→BUS L
AD SUM 3
AD SUM 2
AD SUM 1
AD SUM Ø
AD SUM 7
AD SUM 6
AD SUM 5
AD SUM 4
AD SUM 11
AD SUM 10
AD SUM 9
AD SUM 8
IDI CPMA LOAD
REVISIONS
CHK
CHANGE NO.
REV.
TITLE
PDP8A CPU (MA)
SCALE
SHEET 5 OF 10
SIZE
CODE
D
CS
NUMBER
M8315-Ø-1
REV.
E
DIST.
H-7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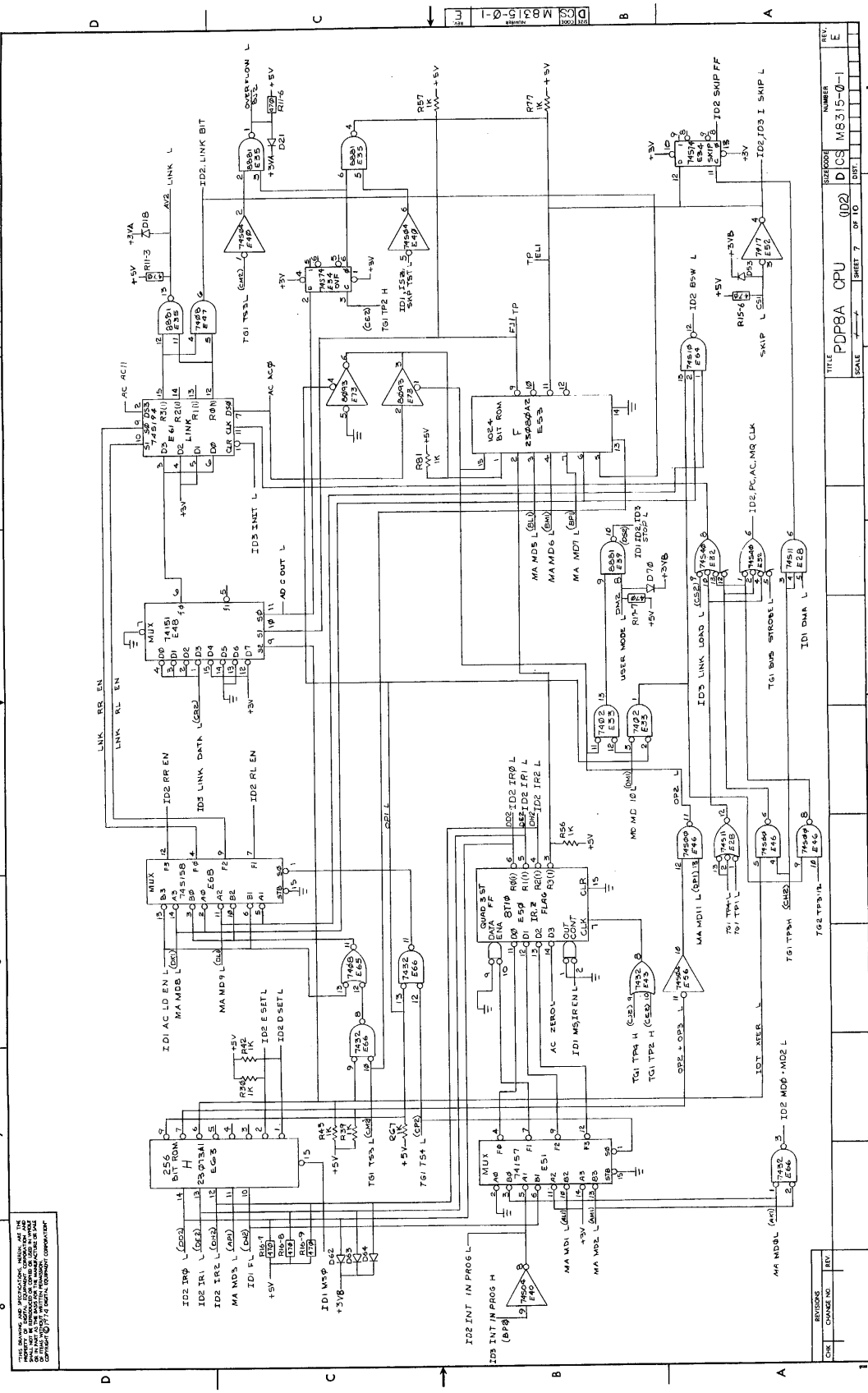
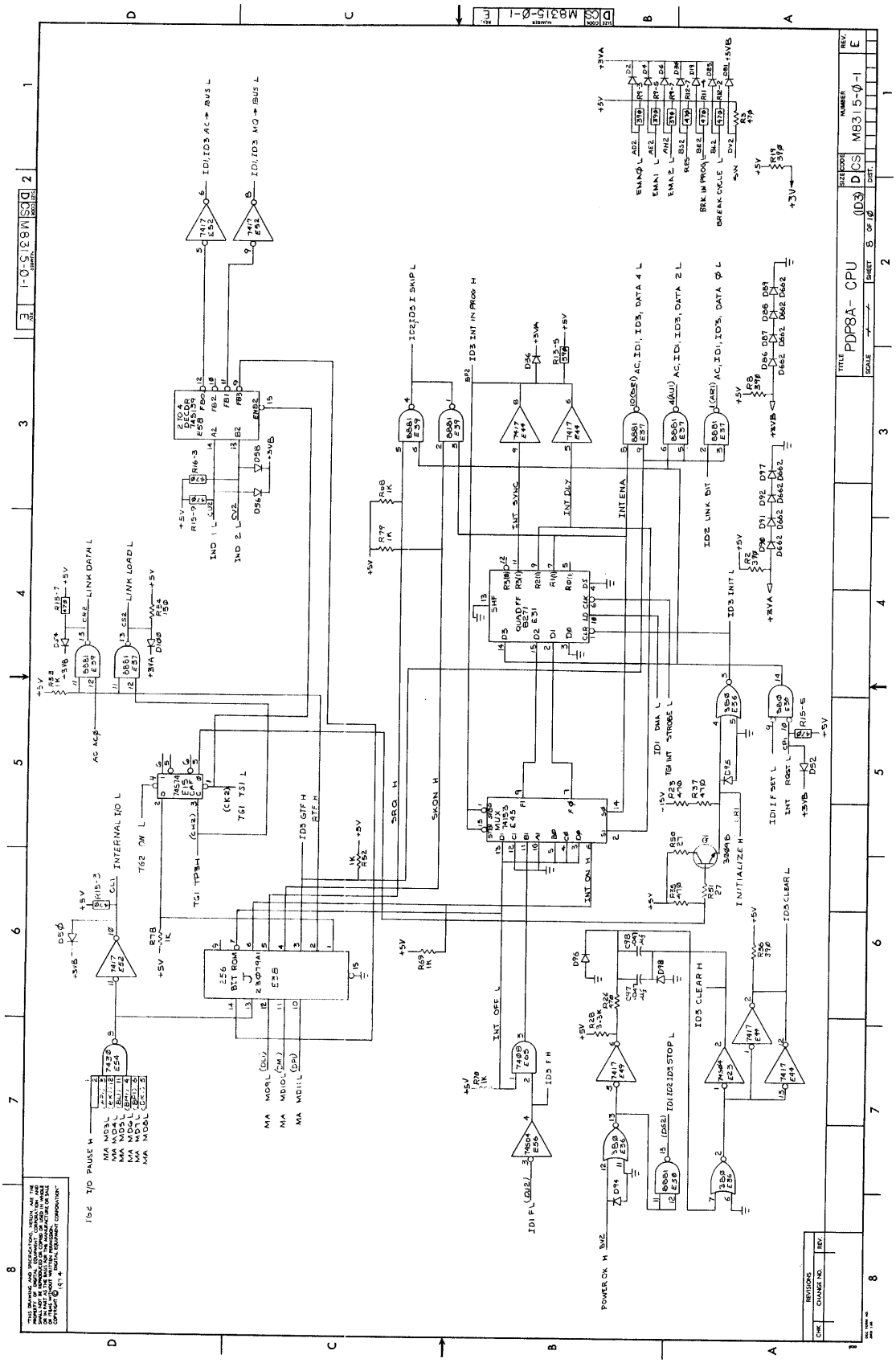
M8315-0-1
IDI DATA ENA L
DATA CMP
IDI PC LD EN L
CARRY EN L
SEL A L
SEL B L
SEL C L
IDI CPMA LOAD
IDI DATA CMP L
IDI MEM START L
IDI CPMA → BUS L
IDI MS IR EN L
IDI, ID3 MQ → BUS L
IDI MQ LD EN L
IDI MQ CLR EN L
IDI AC LD EN L
IDI PC EN L
IDI MA EN L
IDI MD EN L
IDI PAGE EN L
IDI AND EN L
IDI ISZ SKP TST L
IDI, ID3 AC → BUS L
IDI C IN L
IDI E SET L
IDI F SET L
ID3 CLEAR L
AC AUTO L
ROM ADDRESS 3
PDP8A CPU (IDI)
SHEET 6 OF 10
SIZE D
CODE DCS
NUMBER M8315-0-1
REV. E
REVISIONS
CHK
CHANGE NO.
REV.




TITLE PDP8A- CPU
(ID3)
SIZE D
NUMBER M8315-0-1
REV. E
SCALE
SHEET 8 OF 10
DIST.
M8315-0-1
INTERNAL I/O L
LINK DATA L
LINK LOAD L
I/O PAUSE H
INITIALIZE H
ID5 CLEAR H
ID5 CLEAR L
ID5 INIT L
ID5 INT IN PROG H
ID5 I SKIP L
ID5 LINK BIT
ID5 GFF H
ID5 FF H
ID1 DMA L
ID1 STROBE L
ID1 IOT STOP L
INT SYNC
INT DLY
INTENA
INT OFF L
SRQ H
SKON H
POWER ON H
BIT ROM
AC, ID1, ID3, DATA 4 L
AC, ID1, ID3, DATA 2 L
AC, ID1, ID3, DATA 0 L
BREAK CYCLE L
BRK IN PROG L
ENAC0 L
ENA1 L
ENA2 L
IOT PULSE H
IOT INT STROBE L
ID1 IF SET L
INT RQST L
ID1 FL (IO2)
ID1, ID3 AC → BUS L
ID1, ID3 MQ → BUS L
IND 1 L
IND 2 L
MA MD3 L
MA MD4 L
MA MD5 L
MA MD0 L
MA MD1 L
MA MD11 L
MD0 L (DLY)
MD10 L (2MC)
MD11 L (DF)
REVISIONS
CHG
CHANGE NO.
REV.
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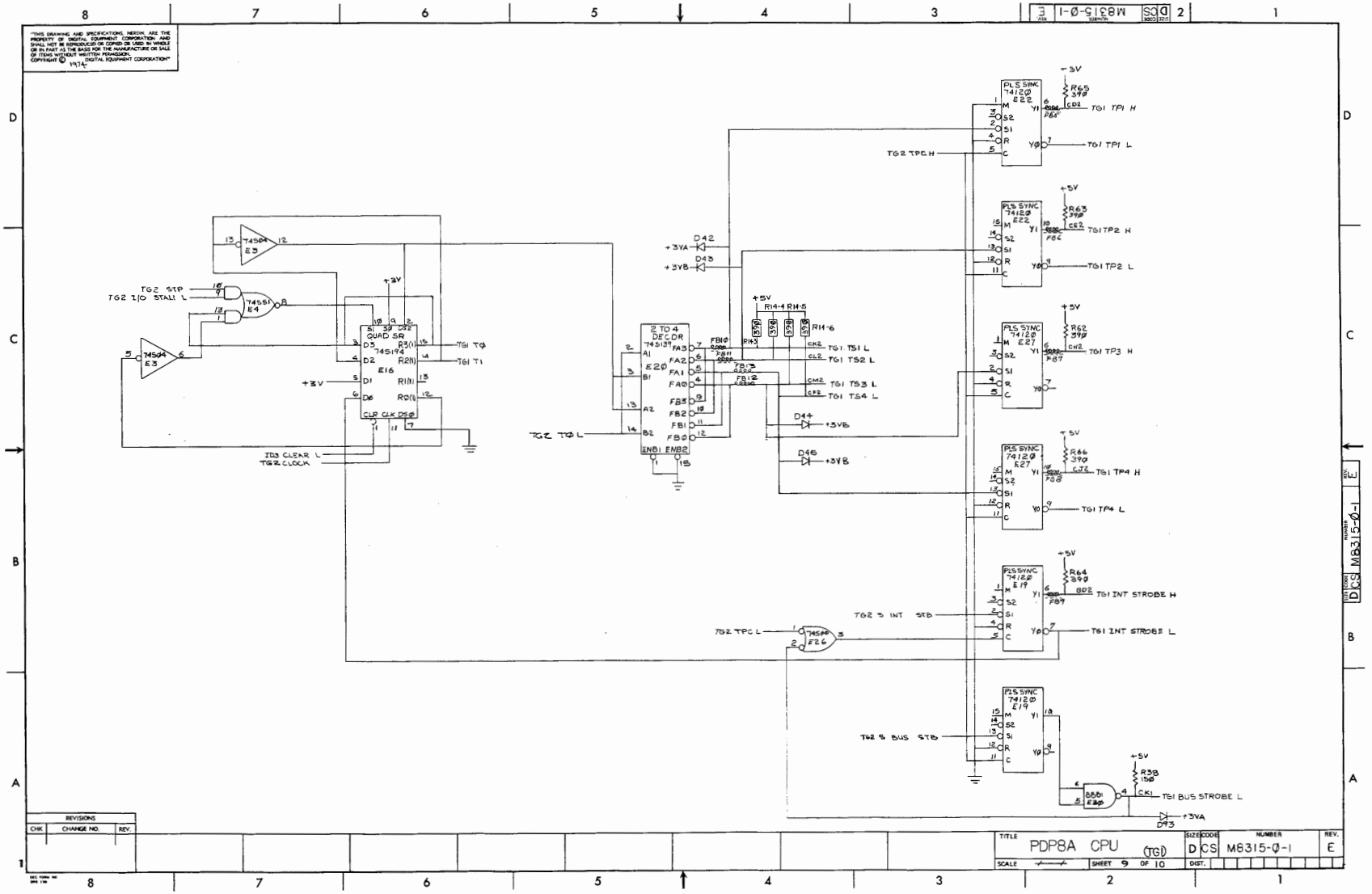
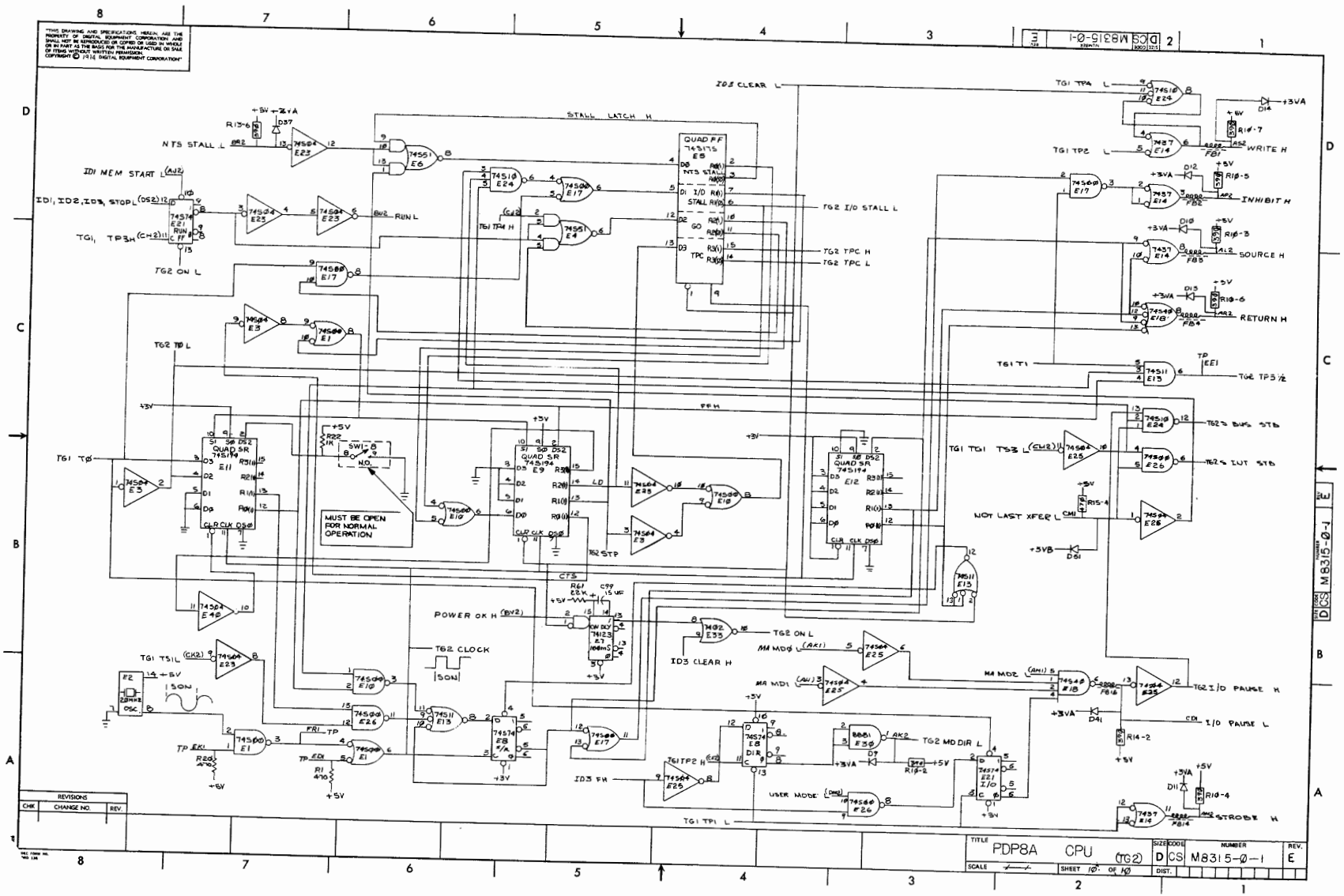

TG2 STP
TG2 I/O STALL L
TG2 TΦ
TG2 T1
TD3 CLEAR L
TG2 CLOCK
QUAD SR
74S194
DECDR
74S139
TG2 TΦ L
TG2 TPC H
TG2 TPC L
TG2 Ø INT STB
TG2 Ø BUS STB
TG1 TP1 H
TG1 TP1 L
TG1 TP2 H
TG1 TP2 L
TG1 TP3 H
TG1 TP4 H
TG1 TP4 L
TG1 INT STROBE H
TG1 INT STROBE L
TG1 BUS STROBE L
TG1 TS1 L
TG1 TS2 L
TG1 TS3 L
TG1 TS4 L
+5V
+3V
+3VA
+3VB
PLS SYNC
74120
REVISIONS
CHK
CHANGE NO.
REV.
TITLE
PDP8A CPU (TGI)
SIZE
CODE
NUMBER
REV.
D
CS
M8315-Ø-1
E
SCALE
SHEET 9 OF 10
DIST.

H-11


IDS CLEAR L
STALL LATCH H
NTS STALL L
IDI MEM START L
IDI, IDI2, IDI3, STOP L
TGI, TP3H
RUN L
TG2 ON L
TG2 TP0 L
TG1 TP0
TG1 TP4 H
TG2 I/O STALL L
TG2 TPC H
TG2 TPC L
TG1 TP4 L
WRITE H
INHIBIT H
SOURCE H
RETURN H
TG1 T1
TG2 TP3½
TG1 TG1 TS3 L
TG2 BUS STB
TG2 IOT STB
NOT LAST XFER L
MUST BE OPEN FOR NORMAL OPERATION
TG2 STP
CTS
POWER OK H
TG2 CLOCK
ID3 CLEAR H
MA MD0
MA MD1
MA MD2
TG2 I/O PAUSE H
I/O PAUSE L
TG2 MD DIR L
TG1 TP2 H
ID3 FH
USER MODE
STROBE H
TG1 TP1 L
TG1 TS1L
TP EK1
FRI TP
TG2 ON L
TG1 TØ
TG2 TØ L
FFH
+3V
+5V
+6V
+3VA
+3VB
QUAD FF 74S175 E8
QUAD SR 74S194 E9
QUAD SR 74S194 E11
QUAD SR 74S194 E12
SW1-8
NO.
20MHz OSC
E2
R61 22K
C99 .5 UF
100mS
74123 E7
74574 E8 F/A
74574 E21 I/O
8881 E36
74574 E8 DIR
74574 E21
74S00 E1
74S04 E3
74S08 E1
74S10 E24
74S11 E13
74S37 E14
74S40 E18
74S51 E4
74S64 E25
74S74 E21
74S86 E17
74S88 E17
74S89 E16
74S94 E23
74S94 E25
74S94 E40
74S95 E29
74S00 E10
74S00 E26
74S00 E16
74S64 E5
74S64 E28
74S64 E26
74S64 E35
74S64 E3
74S64 E9
74S64 E39
74S02 E35
74S11 E15
74S10 E26
74S08 E26
74S08 E18
74S64 E18
74S64 E29
74S64 E39
74S64 E9
74S64 E10
74S64 E11
74S64 E7
74S64 E8
74S64 E10
74S64 E1
74S64 E17
74S64 E1
74S64 E26
74S64 E1
74S64 E10
74S64 E13
74S64 E8
74S64 E26
74S64 E25
74S64 E26
74S64 E25
74S64 E18
74S64 E35
74S64 E25
74S64 E25
74S64 E26
74S64 E25
74S64 E26
74S64 E25
74S64 E26

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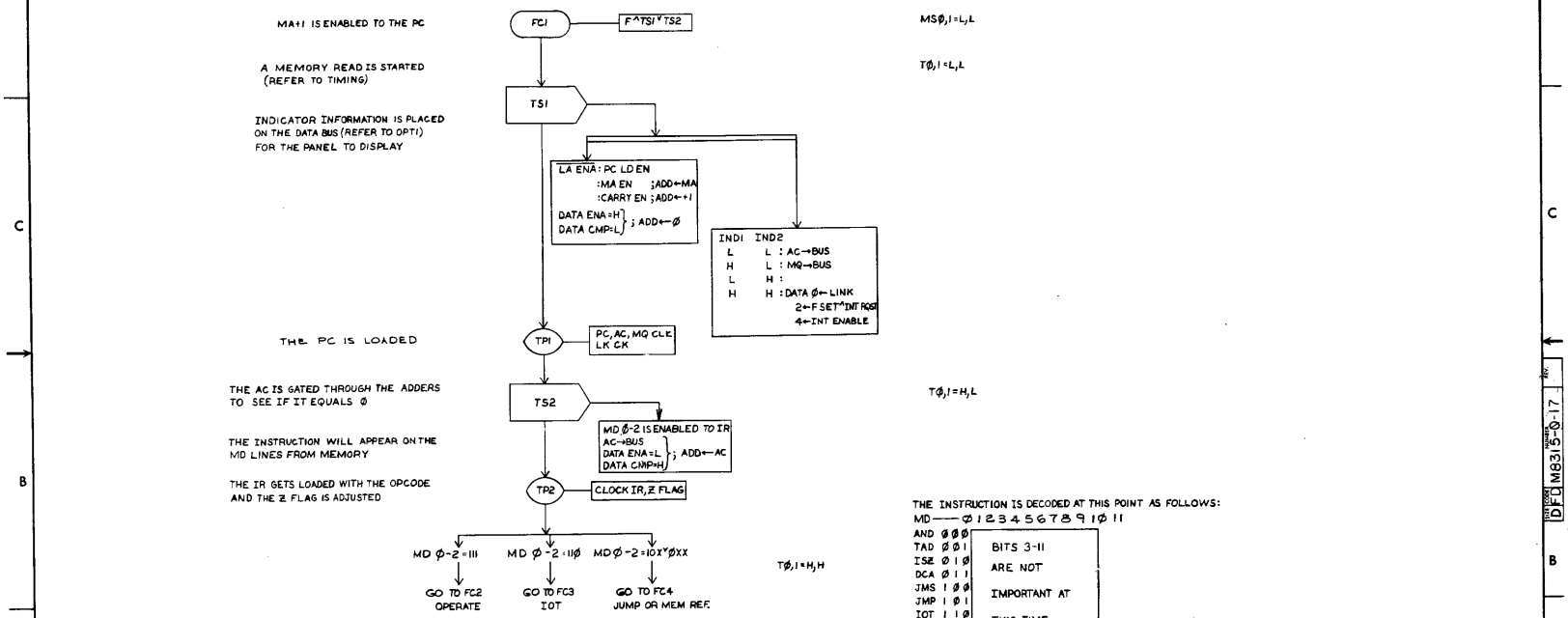


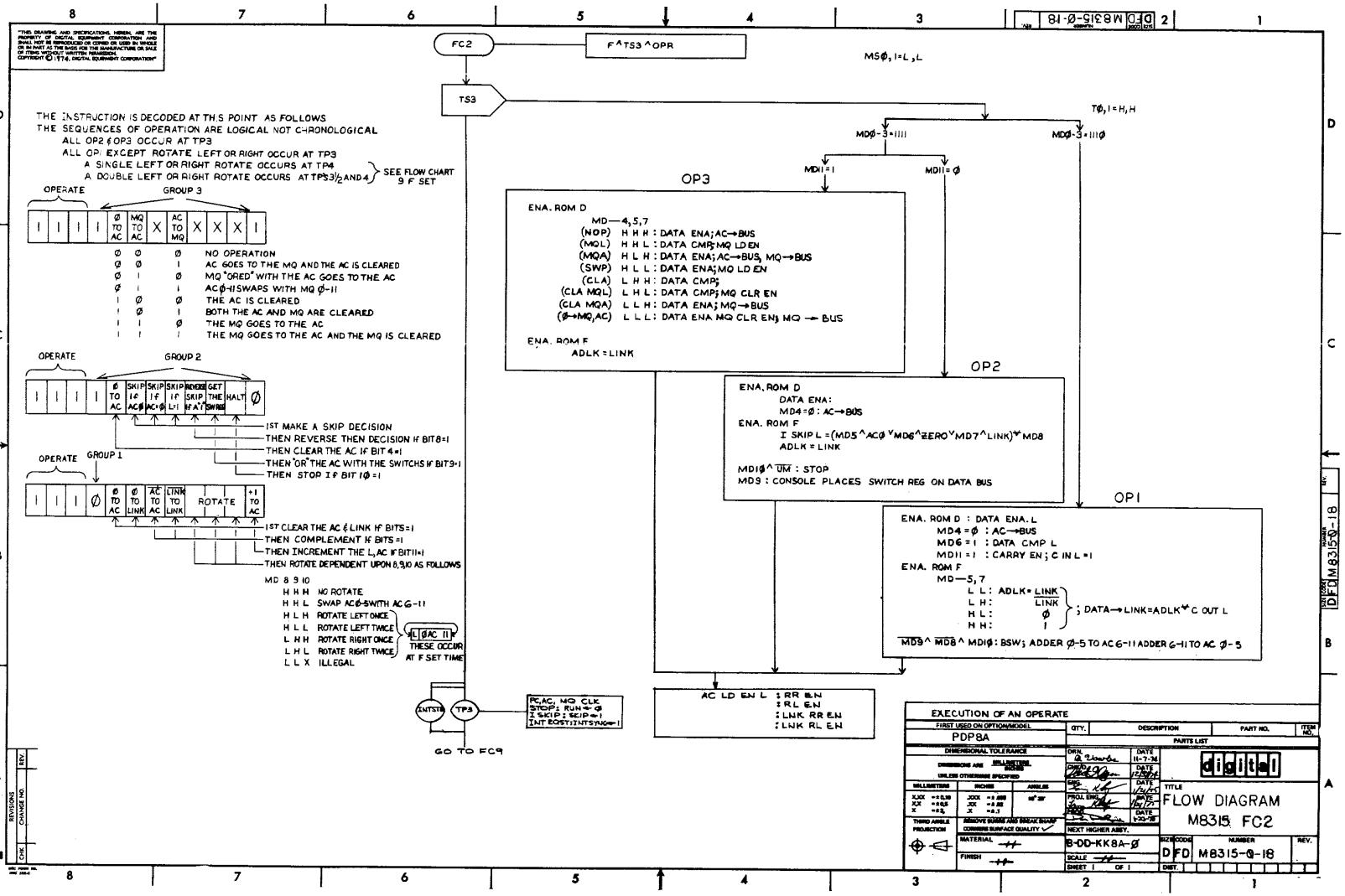
FETCH AND (TS1 or TS2) (GET AN INSTRUCTION)

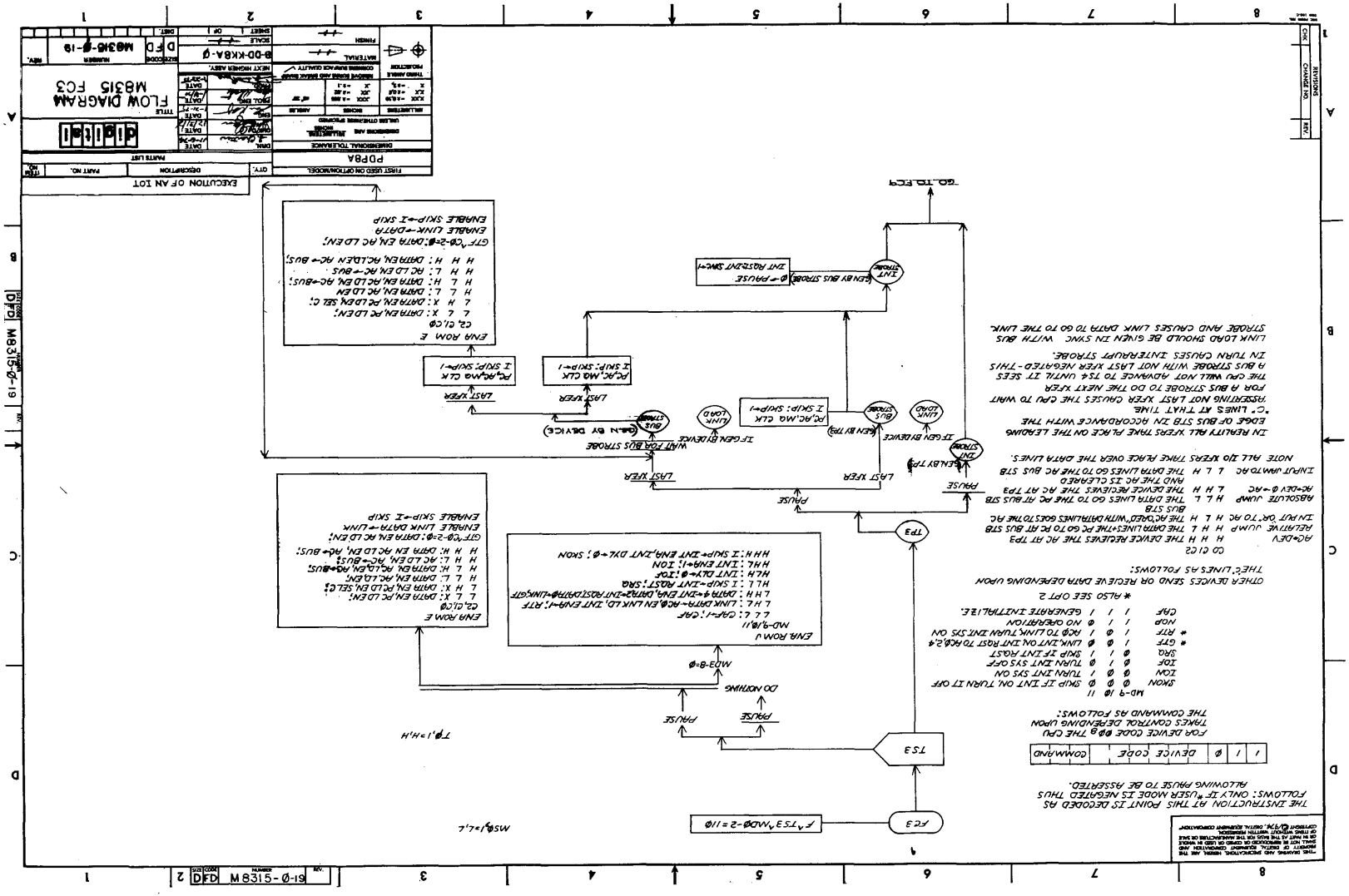
FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
PDP8A		PARTS LIST		

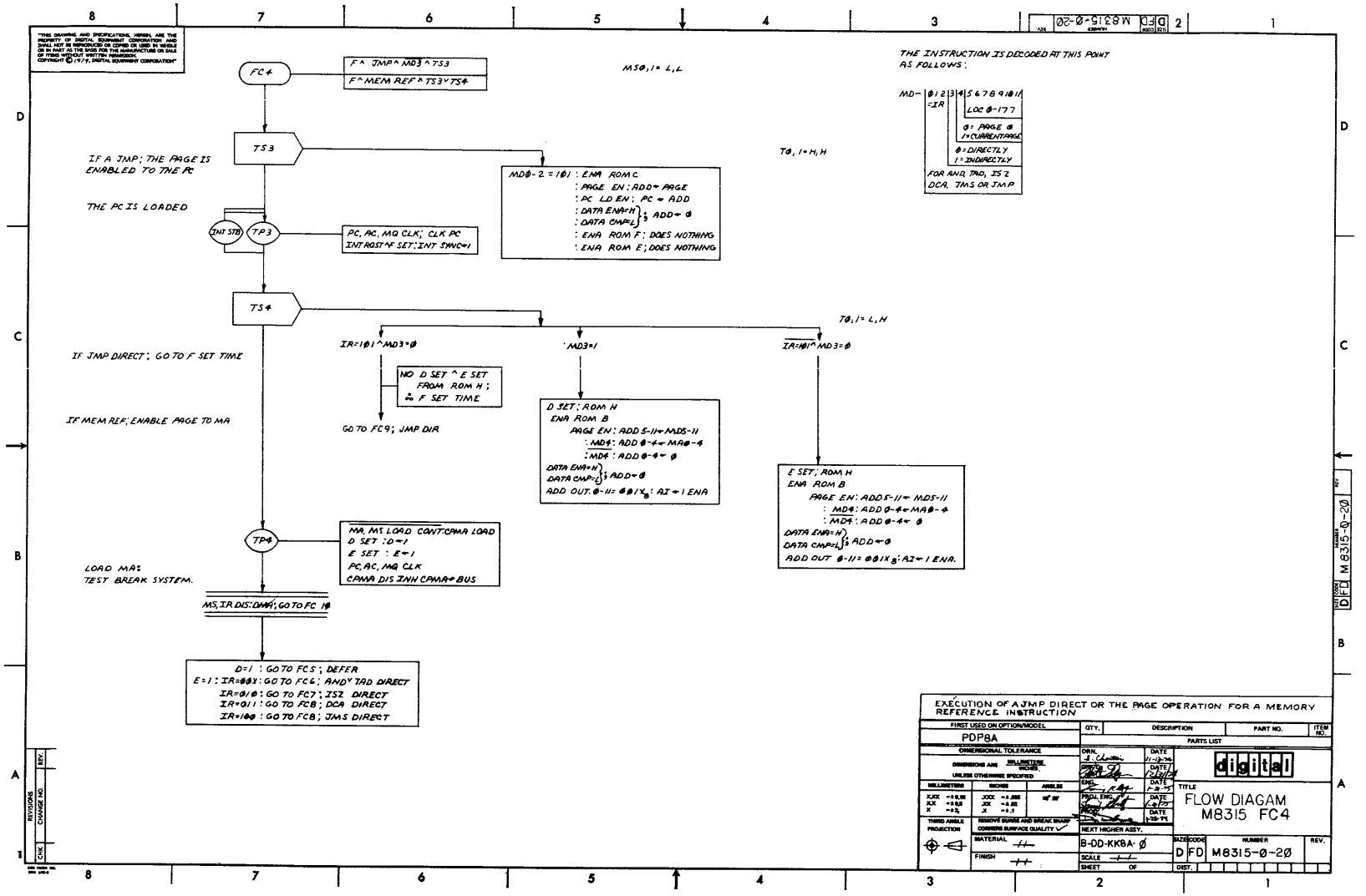
DIMENSIONAL TOLERANCE	DRN.	DATE 11-13-74	digital
DIMENSIONS ARE MILLIMETERS / INCHES UNLESS OTHERWISE SPECIFIED	CHK'D	DATE 12/9/74	
MILLIMETERS: X.XX ±0.13, X.X ±0.5, X ±2; INCHES: .XXX ±.005, .XX ±.02, X ±0.1; ANGLES ±30'	ENG.	DATE 1-24-75	TITLE FLOW DIAGRAM M8315 FC1
THIRD ANGLE PROJECTION	FIELD ENG.	DATE 1-24-75	
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY √	PROD.	DATE	
MATERIAL —	NEXT HIGHER ASSY. B-DD-KK8A-Ø		SIZE D CODE FD NUMBER M8315-Ø-17 REV.
FINISH —	SCALE — SHEET 1 OF 1		DIST.

REVISIONS: REV. | CHANGE NO. | CHK

DFD M8315-Ø-17


FC2
F^TS3^OPR
MSØ,1=L,L
TS3
TØ,1=H,H
MDØ-3=1111
MDØ-3=1110
MDII=1
MDII=Ø
OP3
ENA. ROM D
MD—4,5,7
(NOP) H H H : DATA ENA; AC→BUS
(MQL) H H L : DATA CMP; MQ LD EN
(MQA) H L H : DATA ENA; AC→BUS, MQ→BUS
(SWP) H L L : DATA ENA; MQ LD EN
(CLA) L H H : DATA CMP;
(CLA MQL) L H L : DATA CMP; MQ CLR EN
(CLA MQA) L L H : DATA ENA; MQ→BUS
(Ø→MQ,AC) L L L : DATA ENA MQ CLR EN; MQ → BUS
ENA. ROM F
ADLK = LINK
OP2
ENA. ROM D
DATA ENA:
MD4=Ø : AC→BUS
ENA. ROM F
I SKIP L = (MD5^ACØ^MD6^ZERO^MD7^LINK)^MD8
ADLK = LINK
MDIØ^UM : STOP
MD9 : CONSOLE PLACES SWITCH REG ON DATA BUS
OP1
ENA. ROM D : DATA ENA. L
MD4 = Ø : AC→BUS
MD6 = 1 : DATA CMP L
MDII = 1 : CARRY EN; C IN L = 1
ENA. ROM F
MD—5,7
L L : ADLK = LINK
L H : LINK
H L : Ø
H H : 1
; DATA→LINK=ADLK^C OUT L
MD9^MD8^MDIØ : BSW; ADDER Ø-5 TO AC 6-11 ADDER 6-11 TO AC Ø-5
THE INSTRUCTION IS DECODED AT THIS POINT AS FOLLOWS
THE SEQUENCES OF OPERATION ARE LOGICAL NOT CHRONOLOGICAL
ALL OP2 & OP3 OCCUR AT TP3
ALL OP1 EXCEPT ROTATE LEFT OR RIGHT OCCUR AT TP3
A SINGLE LEFT OR RIGHT ROTATE OCCURS AT TP4
A DOUBLE LEFT OR RIGHT ROTATE OCCURS AT TP3½ AND 4
SEE FLOW CHART 9 F SET
OPERATE
GROUP 3
Ø TO AC
MQ TO AC
AC TO MQ
Ø Ø Ø NO OPERATION
Ø Ø 1 AC GOES TO THE MQ AND THE AC IS CLEARED
Ø 1 Ø MQ "ORED" WITH THE AC GOES TO THE AC
Ø 1 1 AC Ø-11 SWAPS WITH MQ Ø-11
1 Ø Ø THE AC IS CLEARED
1 Ø 1 BOTH THE AC AND MQ ARE CLEARED
1 1 Ø THE MQ GOES TO THE AC
1 1 1 THE MQ GOES TO THE AC AND THE MQ IS CLEARED
OPERATE
GROUP 2
Ø TO AC
SKIP IF ACØ
SKIP IF AC<Ø
SKIP IF L=1
REVERSE SKIP IF A=1
GET THE SWREG
HALT
Ø
1ST MAKE A SKIP DECISION
THEN REVERSE THEN DECISION IF BIT 8=1
THEN CLEAR THE AC IF BIT 4=1
THEN "OR" THE AC WITH THE SWITCHES IF BIT 9=1
THEN STOP IF BIT 10=1
OPERATE
GROUP 1
Ø TO AC
Ø TO LINK
AC TO AC
LINK TO LINK
ROTATE
+1 TO AC
1ST CLEAR THE AC & LINK IF BITS=1
THEN COMPLEMENT IF BITS=1
THEN INCREMENT THE L,AC IF BIT11=1
THEN ROTATE DEPENDENT UPON 8,9,10 AS FOLLOWS
MD 8 9 10
H H H NO ROTATE
H H L SWAP ACØ-5 WITH AC 6-11
H L H ROTATE LEFT ONCE
H L L ROTATE LEFT TWICE
L H H ROTATE RIGHT ONCE
L H L ROTATE RIGHT TWICE
L L X ILLEGAL
L, ØAC 11
THESE OCCUR AT F SET TIME
INTSTB
TP3
PC,AC, MQ CLK
STOP: RUN←Ø
I SKIP : SKIP←1
INT ENBST: INTSYNC←1
GO TO FC9
AC LD EN L : RR EN
: RL EN
: LNK RR EN
: LNK RL EN
EXECUTION OF AN OPERATE
FIRST USED ON OPTION/MODEL
PDP8A
QTY.
DESCRIPTION
PART NO.
ITEM NO.
PARTS LIST
DIMENSIONAL TOLERANCE
DIMENSIONS ARE MILLIMETERS INCHES
UNLESS OTHERWISE SPECIFIED
MILLIMETERS
INCHES
ANGLES
THIRD ANGLE PROJECTION
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY
MATERIAL
FINISH
NEXT HIGHER ASSY.
8-DD-KK8A-Ø
SIZE
CODE
NUMBER
REV.
D
FD
M8315-Ø-18
SCALE
SHEET 1 OF 1
DIST.
DRN. Q. Wanke
DATE 11-7-74
CHKD.
DATE 12/2/74
ENG.
DATE 12/6/74
PROJ. ENG.
DATE 12/9/74
MFG.
DATE 1-20-75
digital
TITLE
FLOW DIAGRAM
M8315 FC2
DFD M8315-Ø-18
REVISIONS
REV.
CHANGE NO.
CHK.


M8315-Ø-19
DFD
PDP8A
DIGITAL
FLOW DIAGRAM M8315 FC3
M8315-Ø-19
B-DD-KK8A-Ø
EXECUTION OF AN IOT
PARTS LIST
THE INSTRUCTION AT THIS POINT IS DECODED AS FOLLOWS; ONLY IF *USER MODE IS NEGATED THUS ALLOWING PAUSE TO BE ASSERTED.
FOR DEVICE CODE ØØ THE CPU TAKES CONTROL DEPENDING UPON THE COMMAND AS FOLLOWS:
MD-9 10 11
SKON Ø Ø Ø SKIP IF INT ON, TURN IT OFF
ION Ø Ø 1 TURN INT SYS ON
IOF Ø Ø 1 TURN INT SYS OFF
SRQ Ø 1 1 SKIP IF INT RQST
* GTF 1 Ø Ø LINK,INT ON, INT RQST TO AC0,2,4
* RTF 1 Ø 1 ADD TO LINK,TURN INT SYS ON
NOP 1 1 Ø NO OPERATION
CAF 1 1 1 GENERATE INITIALIZE.
* ALSO SEE OPT 2
OTHER DEVICES SEND OR RECEIVE DATA DEPENDING UPON THEIR LINES AS FOLLOWS:
IOT Ø1Ø2
AC←DEV H H H THE DEVICE REQUESTS THE AC AT TP3
RELATIVE JUMP H H L THE DATA LINES GO TO PC AT BUS STB
IN PUT 'OR' TO AC H L H THE AC 'ORED' WITH DATA LINES GOES TO THE AC BUS STB
ABSOLUTE JUMP H L L THE DATA LINES GO TO THE PC AT BUS STB
PC←DEV Ø→AC L H H THE DEVICE RECEIVES THE AC AT TP3
AND THE AC IS CLEARED
INPUT JUMP TO AC L L H THE DATA LINES GO TO THE AC BUS STB
NOTE ALL IOT XFERS TAKE PLACE OVER THE DATA LINES.
IN REALITY ALL XFERS TAKE PLACE ON THE LEADING EDGE OF BUS STB IN ACCORDANCE WITH THE "C" LINES AT THAT TIME.
ASSERTING NOT LAST XFER CAUSES THE CPU TO WAIT FOR A BUS STROBE TO DO THE NEXT XFER
THE CPU WILL NOT ADVANCE TO TS4 UNTIL IT SEES A BUS STROBE WITH NOT LAST XFER NEGATED - THIS IN TURN CAUSES INTERRUPT STROBE.
LINK LOAD SHOULD BE GIVEN IN SYNC WITH BUS STROBE AND CAUSES LINK DATA TO GO TO THE LINK
GO TO FC9
INT STROBE
GEN BY BUS STROBE Ø→PAUSE
INT RQST2 FF SET→1
TS3
FC3
F'TS3'*MAD Ø-2 = 1/Ø
MSØ/→4,4
TP3
PAUSE
DO NOTHING
MD3-8→Ø
ENA ROM J
MD-9,10,11
LINK DATA→AC Ø,EN LNK,LD, INT ENA→1; RTF
Ø H H : DATA 4→INT ENA, DATA2→INT RQST, DATA Ø→LINK; GTF
H L L : I SKIP→INT RQST; SRQ
H L H : INT CLK→Ø ; IOF
H H L : INT ENA→1; ION
H H H : I SKIP→INT ENA, INT DX←Ø ; SKON
ENA ROM E
C2, CLC Ø
L L X: DATA EN, PC LD EN;
L H X: DATA EN, PC LD EN, SEL C1;
H L L: DATA EN, AC LD EN
H L H: DATA EN, AC LD EN, AC←BUS1;
H H L: AC LD EN, AC←BUS1
H H H: DATA EN AC LD EN, AC←BUS1;
GTF'Ø-2=Ø: DATA EN, IR LD EN;
ENABLE LINK DATA→LINK
ENABLE SKIP←I SKIP
LAST XFER
WAIT FOR BUS STROBE
GEN BY DEVICE
IF GEN BY DEVICE
GEN BY TP3
PC, MA CLK I SKIP: SKIP←1
PC, AC, MA CLK I SKIP: SKIP←1
ENA ROM E
C2, CLC Ø
L L X: DATA EN, PC LD EN;
L X X: DATA EN, PC LD EN, SEL C1;
H L L: DATA EN, AC LD EN
H L H: DATA EN, AC LD EN, AC←BUS1;
H H L: AC LD EN, AC←BUS1
H H H: DATA EN, AC LD EN, MD←BUS1;
GTF'Ø-2=Ø: DATA EN, IR LD EN;
ENABLE LINK DATA→LINK
ENABLE SKIP←I SKIP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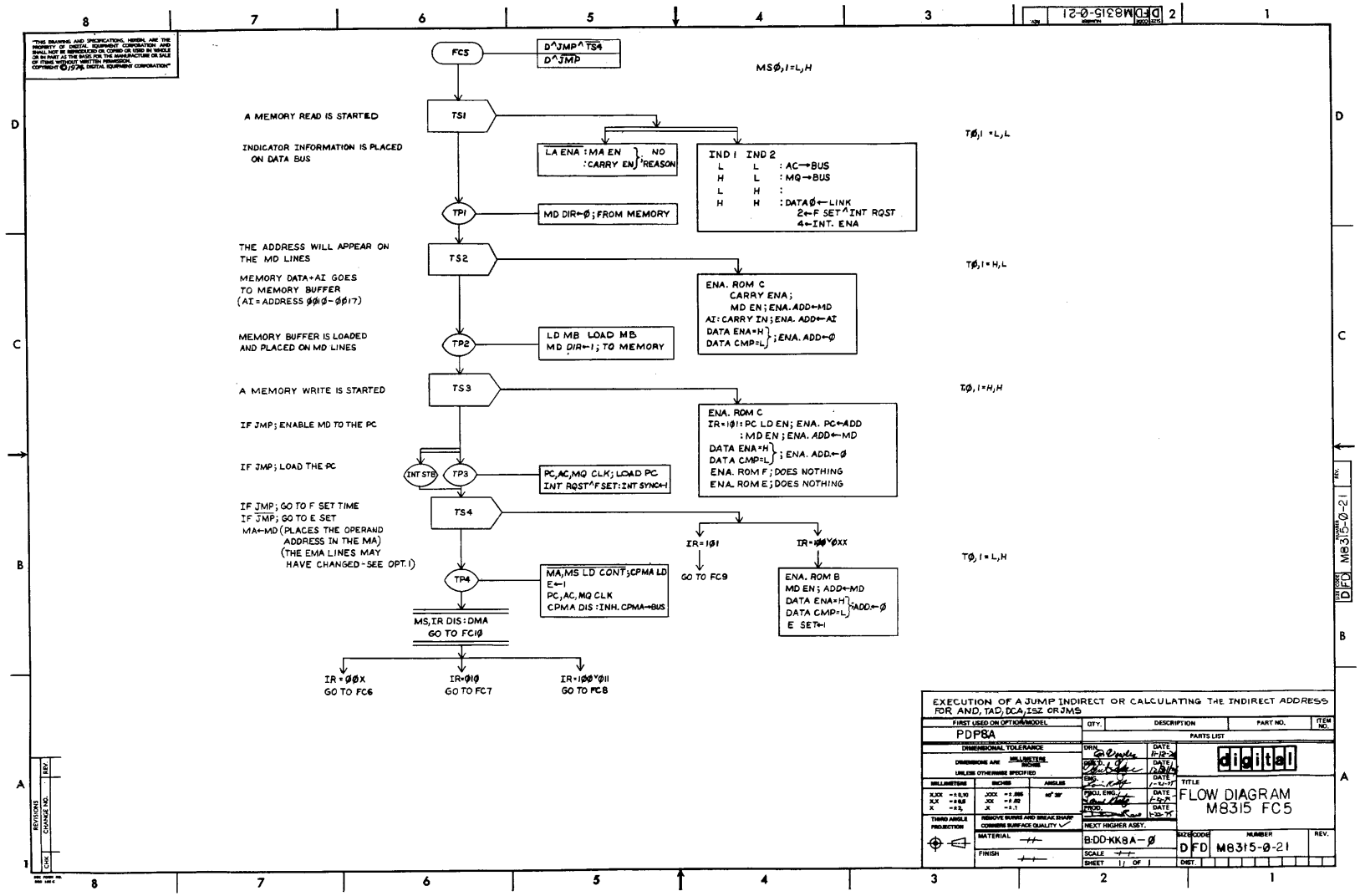
FC4
F^ JMP^MD3^TS3
F^MEM REF^TS3∨TS4
M5Ø,1= L,L
THE INSTRUCTION IS DECODED AT THIS POINT AS FOLLOWS:
MD- =IR
Ø 1 2 3 4 5 6 7 8 9 10 11
LOC Ø-177
Ø= PAGE Ø
1=CURRENT PAGE
Ø=DIRECTLY
1=INDIRECTLY
FOR AND, TAD, ISZ DCA, JMS OR JMP
TS3
IF A JMP; THE PAGE IS ENABLED TO THE PC
THE PC IS LOADED
T Ø, I= H, H
MDØ-2 = 1Ø1 : ENA ROM C
: PAGE EN; ADD← PAGE
: PC LD EN; PC ← ADD
: DATA ENA=H } ; ADD← Ø
: DATA CMP=L }
: ENA ROM F; DOES NOTHING
: ENA ROM E; DOES NOTHING
INT STB
TP3
PC, AC, MQ CLK; CLK PC
INT RQST^F SET; INT SWC=1
TS4
T Ø, I= L, H
IR=1Ø1^MD3=Ø
MD3=1
IR=1Ø1^MD3=Ø
IF JMP DIRECT; GO TO F SET TIME
NO D SET ^ E SET FROM ROM H; ∴ F SET TIME
GO TO FC9; JMP DIR
IF MEM REF; ENABLE PAGE TO MA
D SET; ROM H
ENA ROM B
PAGE EN: ADD 5-11← MD5-11
: MD4: ADD Ø-4← MAØ-4
: MD4: ADD Ø-4← Ø
DATA ENA=H } ; ADD← Ø
DATA CMP=L }
ADD OUT Ø-11= ØØ1X2: AI← 1 ENA
E SET; ROM H
ENA ROM B
PAGE EN: ADD 5-11← MD5-11
: MD4: ADD Ø-4← MAØ-4
: MD4: ADD Ø-4← Ø
DATA ENA=H } ; ADD← Ø
DATA CMP=L }
ADD OUT Ø-11= ØØ1X2: AI← 1 ENA.
TP4
MA, MS LOAD CONT; CPMA LOAD
D SET: D← 1
E SET: E← 1
PC, AC, MQ CLK
CPMA, DIS INH CPMA← BUS
LOAD MA:
TEST BREAK SYSTEM.
MS, IR DIS; CPMA; GO TO FC 1Ø
D=1 : GO TO FC5; DEFER
E=1 : IR=ØØX: GO TO FC6; AND, TAD DIRECT
IR=Ø1Ø: GO TO FC7; ISZ DIRECT
IR=Ø11: GO TO FC8; DCA DIRECT
IR=1ØØ: GO TO FC8; JMS DIRECT
REVISIONS
REV.
CHANGE NO.
CHK
EXECUTION OF A JMP DIRECT OR THE PAGE OPERATION FOR A MEMORY REFERENCE INSTRUCTION
FIRST USED ON OPTION/MODEL
PDP8A
QTY.
DESCRIPTION
PART NO.
ITEM NO.
PARTS LIST
DIMENSIONAL TOLERANCE
DIMENSIONS ARE MILLIMETRE INCHES
UNLESS OTHERWISE SPECIFIED
MILLIMETERS
INCHES
ANGLES
XXX ±0.13
XX ±0.25
X ±0.5
XXX ±.005
XX ±.01
X ±.02
THIRD ANGLE PROJECTION
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY
NEXT HIGHER ASSY.
MATERIAL
FINISH
B-DD-KK8A-Ø
SCALE
SHEET OF
DRN. J. Clinton 11-12-70
DSGN
ENG. 1-8-71
PROJ. ENG. 1-20-71
DATE
digital
TITLE
FLOW DIAGAM M8315 FC4
SIZE CODE
D FD
NUMBER
M8315-Ø-2Ø
REV.
DIST.



EXECUTION OF A JUMP INDIRECT OR CALCULATING THE INDIRECT ADDRESS FOR AND, TAD, DCA, ISZ OR JMS

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
PDP8A		PARTS LIST		

DIMENSIONAL TOLERANCE
DIMENSIONS ARE MILLIMETERS / INCHES
UNLESS OTHERWISE SPECIFIED

MILLIMETERS	INCHES	ANGLES
XXX = ±0.10	.XXX = ±.005	±0° 30'
XX = ±0.8	.XX = ±.02	
X = ±0.5	.X = ±.1	

THIRD ANGLE PROJECTION

REMOVE BURRS AND BREAK SHARP
CONFIRM SURFACE QUALITY ✓
MATERIAL —
FINISH —

DRN. Ed Snyder DATE 11-12-74
DES. J. Clark DATE 12-2-74
ENG. DATE 1-2-75
PROJ. ENG. DATE 1-24-75
PROD. DATE 1-30-75
NEXT HIGHER ASSY.
B-DD-KK8A-Ø
SCALE —
SHEET 1 OF 1

digital

TITLE: FLOW DIAGRAM M8315 FC5

SIZE D | CODE DFD | NUMBER M8315-Ø-21 | REV.
DIST.

REVISIONS: REV. | CHANGE NO. | CHK

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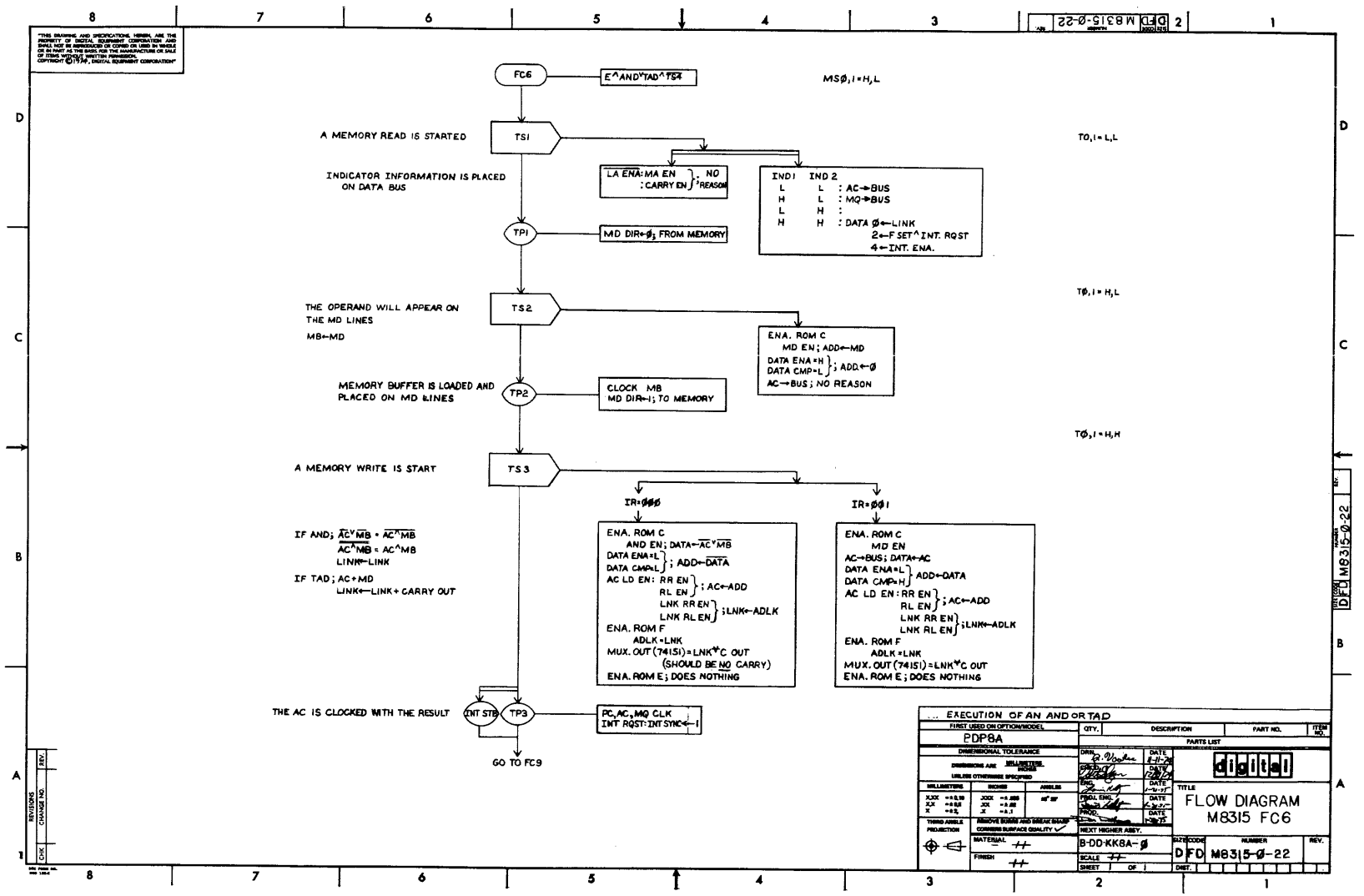

EXECUTION OF AN AND OR TAD

FIRST USED ON OPTION/MODEL	PDP8A
DRN	B. Woodbury 8-11-76
CHK	Gordon Bell 8-11-76
ENG	1-14-77
PROJ. ENG.	4-27-77
PROG.	12-27-76
NEXT HIGHER ASSY.	B-DD-KK8A-Ø
MATERIAL	—
FINISH	—
SCALE	—
SHEET 1 OF 1	
SIZE	D
CODE	DFD
NUMBER	M8315-Ø-22
REV.	

digital

TITLE: FLOW DIAGRAM M8315 FC6

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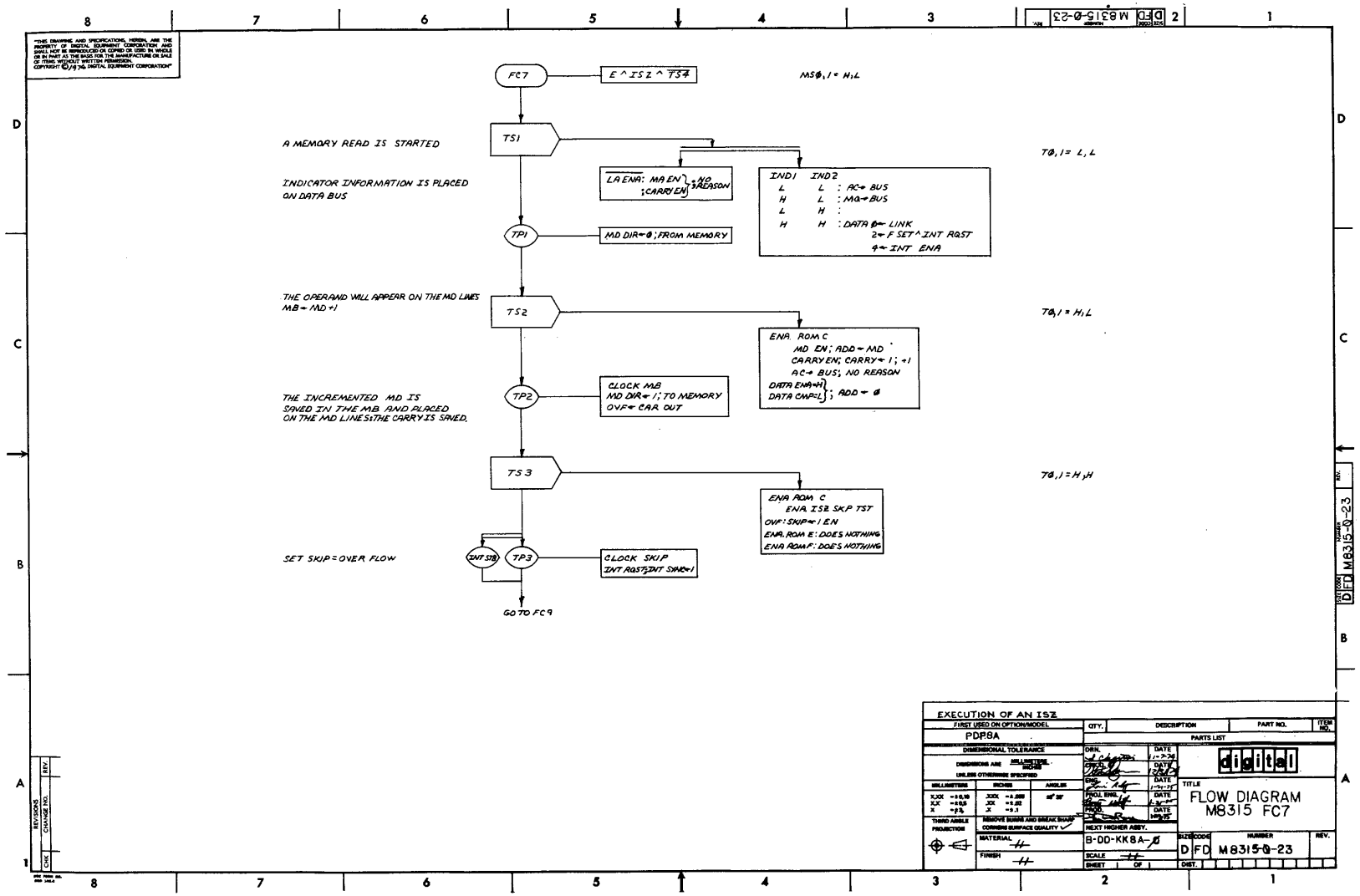
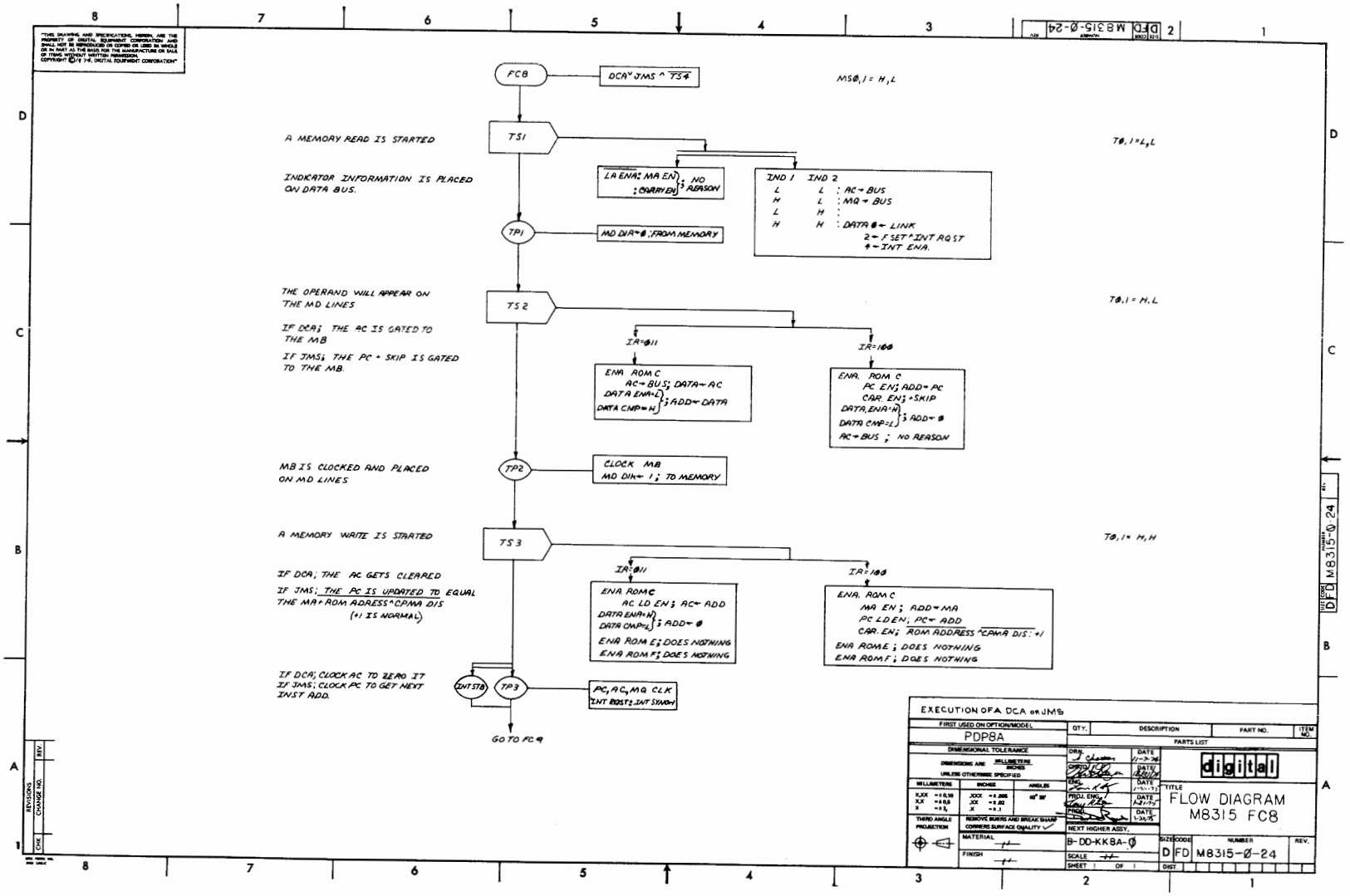

FC7
E ^ ISZ ^ TS4
MSØ,1 = H,L
TS1
A MEMORY READ IS STARTED
INDICATOR INFORMATION IS PLACED ON DATA BUS
LA ENA: MA EN; CARRY EN; NO SAE REASON
IND1 IND2
L L : AC → BUS
H L : MQ → BUS
L H :
H H : DATA Ø → LINK
2 → F SET ^ INT RQST
4 → INT ENA
TØ,1 = L,L
TP1
MD DIR → Ø; FROM MEMORY
TS2
THE OPERAND WILL APPEAR ON THE MD LINES
MB → MD + 1
ENA ROM C
MD EN; ADD → MD
CARRY EN; CARRY → 1; +1
AC → BUS; NO REASON
DATA ENA → H
DATA CMPL → L; ADD → Ø
TØ,1 = H,L
TP2
THE INCREMENTED MD IS SAVED IN THE MB AND PLACED ON THE MD LINES; THE CARRY IS SAVED.
CLOCK MB
MD DIR → 1; TO MEMORY
OVF → CAR OUT
TS3
ENA ROM C
ENA ISZ SKP TST
OVF: SKIP → 1 EN
ENA ROM E: DOES NOTHING
ENA ROM F: DOES NOTHING
TØ,1 = H,H
INT STB
TP3
SET SKIP = OVER FLOW
CLOCK SKIP
INT RQST; INT SAVE → 1
GO TO FC9
EXECUTION OF AN ISZ
FIRST USED ON OPTION/MODEL
PDP8A
PARTS LIST
QTY. DESCRIPTION PART NO. ITEM NO.
digital
TITLE
FLOW DIAGRAM
M8315 FC7
NEXT HIGHER ASSY.
B-DD-KK8A-Ø
SIZE CODE NUMBER REV.
D FD M8315-Ø-23
SCALE
SHEET OF
DIST.
REVISIONS
REV.
CHANGE NO.
CHK
M8315-Ø-23



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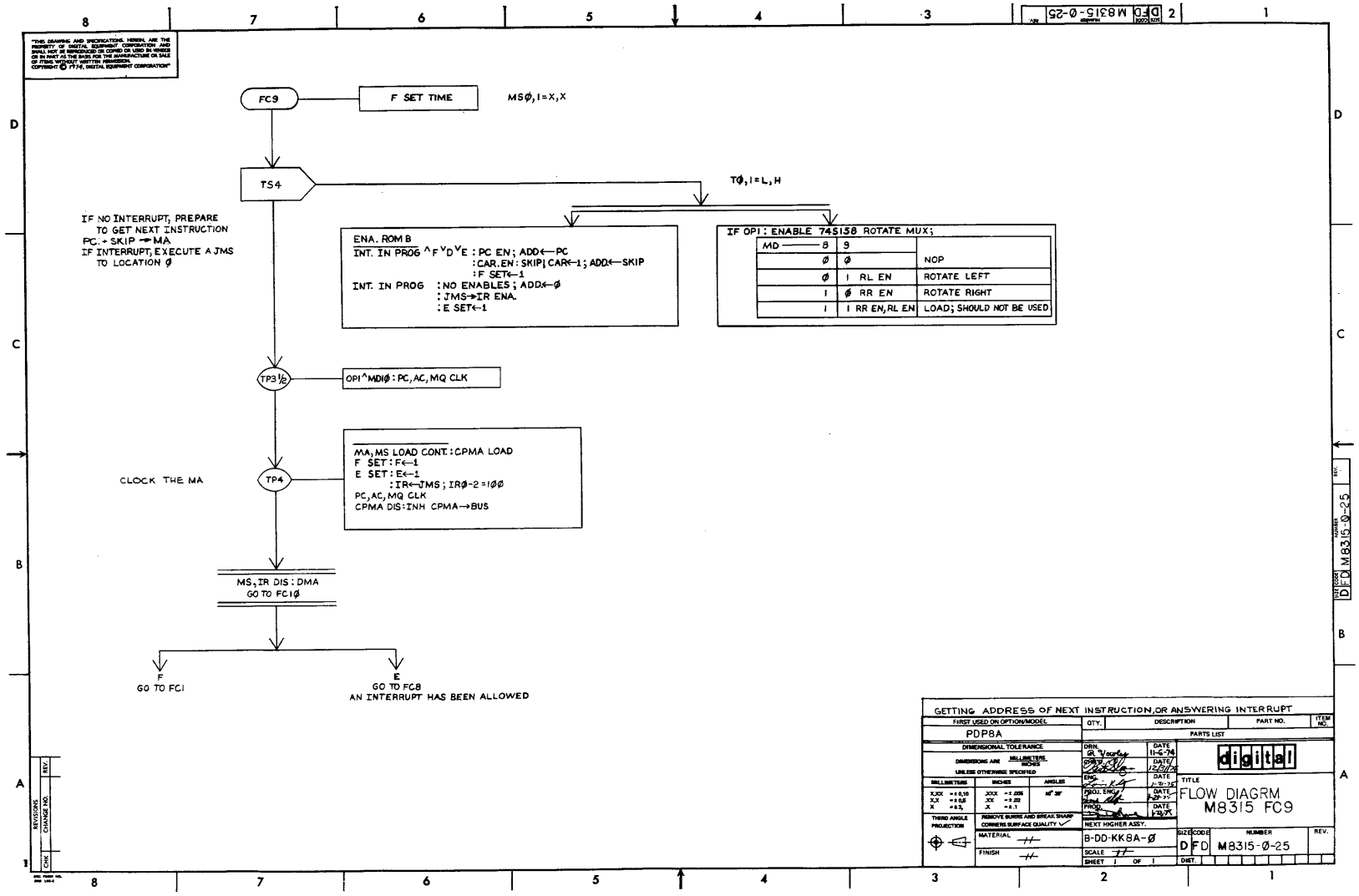


GETTING ADDRESS OF NEXT INSTRUCTION, OR ANSWERING INTERRUPT

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
PDP8A		PARTS LIST		

DIMENSIONAL TOLERANCE
DIMENSIONS ARE MILLIMETERS / INCHES
UNLESS OTHERWISE SPECIFIED

MILLIMETERS	INCHES	ANGLES
XXX ± 0.10	XXX ± .005	½° 30'
XX ± 0.5	XX ± .02	
X ± 0.2	X ± 0.1	

THIRD ANGLE PROJECTION
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓
MATERIAL —
FINISH —

DRN.	GL Vosley	DATE 11-6-74
DSN.		DATE 12/11/74
ENG.		DATE 1-24-75
PROJ. ENG.		DATE 1-24-75
PROD.		DATE 1-24-75

NEXT HIGHER ASSY. B-DD-KK8A-Ø
SCALE FT
SHEET 1 OF 1

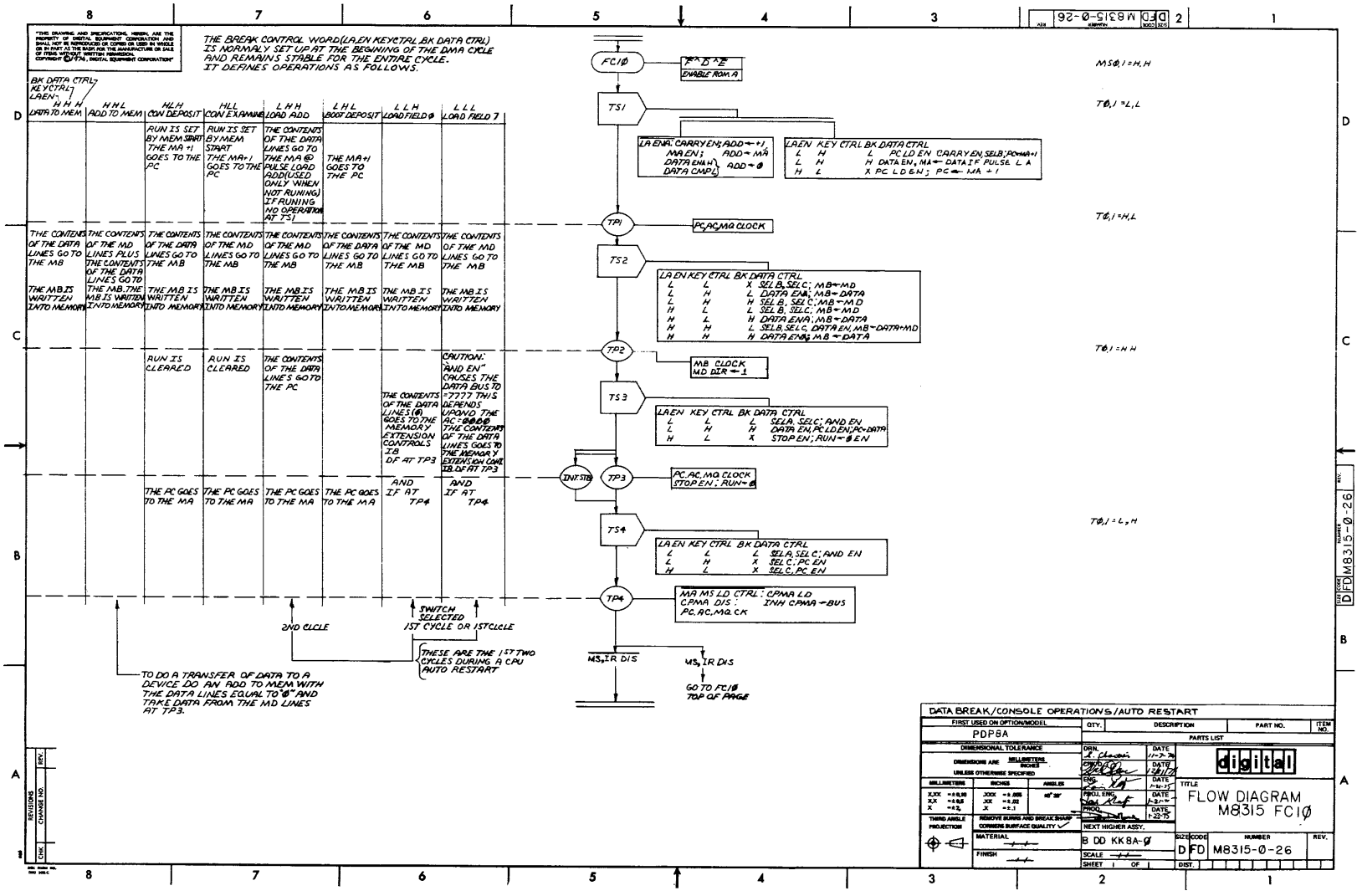
digital

TITLE FLOW DIAGRM M8315 FC9

SIZE D | CODE FD | NUMBER M8315-Ø-25 | REV.
DIST.

REVISIONS: REV. | CHANGE NO. | CHK

DFD M8315-0-25 REV.


THE BREAK CONTROL WORD (LA EN KEY CTRL BK DATA CTRL) IS NORMALLY SET UP AT THE BEGINNING OF THE DMA CYCLE AND REMAINS STABLE FOR THE ENTIRE CYCLE. IT DEFINES OPERATIONS AS FOLLOWS.
BK DATA CTRL / KEY CTRL / LA EN
H H H DATA TO MEM
H H L ADD TO MEM
H L H CON DEPOSIT
H L L CON EXAMINE
L H H LOAD ADD
L H L BOOT DEPOSIT
L L H LOAD FIELD Ø
L L L LOAD FIELD 1
RUN IS SET BY MEM START THE MA+1 GOES TO THE PC
RUN IS SET BY MEM START THE MA+1 GOES TO THE PC
THE CONTENTS OF THE DATA LINES GO TO THE MA @ PULSE LOAD ADD (USED ONLY WHEN NOT RUNING) IF RUNING NO OPERATION AT TS1
THE MA+1 GOES TO THE PC
THE CONTENTS OF THE DATA LINES GO TO THE MB
THE CONTENTS OF THE MD LINES GO TO THE MB
THE CONTENTS OF THE MD LINES GO TO THE MB
THE CONTENTS OF THE DATA LINES GO TO THE MB
THE CONTENTS OF THE MD LINES PLUS THE CONTENTS OF THE DATA LINES GO TO THE MB. THE MB IS WRITTEN INTO MEMORY
THE MB IS WRITTEN INTO MEMORY
THE MB IS WRITTEN INTO MEMORY
THE MB IS WRITTEN INTO MEMORY
THE MB IS WRITTEN INTO MEMORY
THE MB IS WRITTEN INTO MEMORY
THE MB IS WRITTEN INTO MEMORY
RUN IS CLEARED
RUN IS CLEARED
THE CONTENTS OF THE DATA LINES GO TO THE PC
THE CONTENTS OF THE DATA LINES (Ø) GOES TO THE MEMORY EXTENSION CONTROLS IB DF AT TP3
CAUTION: "AND EN" CAUSES THE DATA BUS TO "7777" THIS DEPENDS UPON WHAT THE AC "ØØØØ" THE CONTENTS OF THE DATA LINES GOES TO THE MEMORY EXTENSION CONT. IB DF AT TP3
THE PC GOES TO THE MA
THE PC GOES TO THE MA
THE PC GOES TO THE MA
THE PC GOES TO THE MA
AND IF AT TP4
AND IF AT TP4
FC1Ø
ENABLE ROM A
TS1
LA ENA: CARRY EN; ADD ← +1
MA EN ↑ ADD ← MA
DATA ENA H ↑
DATA CMPL ↓ ADD ← Ø
LA EN KEY CTRL BK DATA CTRL
L H L PC LD EN CARRY EN SELB; PC ← MA + 1
L H H DATA EN; MA ← DATA IF PULSE L A
H L X PC LD EN; PC ← MA + 1
TP1
PC AC MQ CLOCK
TS2
LA EN KEY CTRL BK DATA CTRL
L L X SEL B, SEL C; MB ← MB
L H L DATA ENA; MB ← DATA
L H H SEL B, SEL C; MB ← MD
H L L SEL B, SEL C; MB ← MD
H L H DATA ENA; MB ← DATA
H H L SEL B, SEL C, DATA EN, MB ← DATA + MD
H H H DATA ENA; MB ← DATA
TP2
MB CLOCK
MD DIR ← 1
TS3
LA EN KEY CTRL BK DATA CTRL
L L L SEL A, SEL C; AND EN
L H H DATA EN, PC LD EN; PC ← DATA
H L X STOP EN; RUN ← Ø EN
INT STB
TP3
PC AC MQ CLOCK
STOP EN; RUN ← Ø
TS4
LA EN KEY CTRL BK DATA CTRL
L L L SEL A, SEL C; AND EN
L H X SEL C; PC EN
H L X SEL C; PC EN
TP4
MA MS LD CTRL: CPMA LD
CPMA DIS: INH CPMA → BUS
PC AC MQ CK
MS, IR DIS
US, IR DIS
GO TO FC1Ø TOP OF PAGE
MS Ø, 1 = H, H
T Ø, 1 = L, L
T Ø, 1 = H, L
T Ø, 1 = H H
T Ø, 1 = L, H
SWITCH SELECTED 1ST CYCLE OR 1ST CYCLE
2ND CYCLE
THESE ARE THE 1ST TWO CYCLES DURING A CPU AUTO RESTART
TO DO A TRANSFER OF DATA TO A DEVICE DO AN ADD TO MEM WITH THE DATA LINES EQUAL TO "Ø" AND TAKE DATA FROM THE MD LINES AT TP3.
DATA BREAK/CONSOLE OPERATIONS/AUTO RESTART
FIRST USED ON OPTION/MODEL
PDP8A
QTY.
DESCRIPTION
PART NO.
ITEM NO.
PARTS LIST
DIMENSIONAL TOLERANCE
DIMENSIONS ARE MILLIMETERS / INCHES
UNLESS OTHERWISE SPECIFIED
MILLIMETERS
INCHES
ANGLES
THIRD ANGLE PROJECTION
REMOVE BURRS AND BREAK SHARP
CORNERS SURFACE QUALITY
MATERIAL
FINISH
NEXT HIGHER ASSY.
B DD KK8A-Ø
SCALE
SHEET 1 OF
DRN.
CHK'D
ENG.
PROJ. ENG.
PROD.
DATE
digital
TITLE
FLOW DIAGRAM
M8315 FC1Ø
SIZE
CODE
NUMBER
REV.
D FD M8315-0-26
DIST.
REVISIONS
REV.
CHANGE NO.
CHK
D FD M8315-0-26

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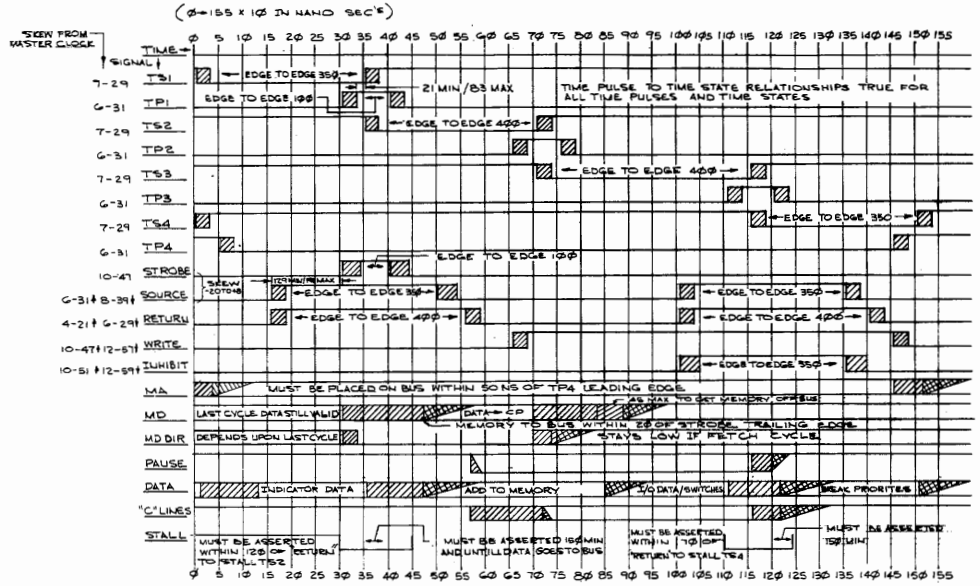


8A DATA PATH FUNCTION & TIMING

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
PDP8A		PARTS LIST		

DIMENSIONAL TOLERANCE
DIMENSIONS ARE MILLIMETERS / INCHES
UNLESS OTHERWISE SPECIFIED

MILLIMETERS	INCHES	ANGLES
X.XX ±0.13	.XXX ±.005	±0° 30'
.XX ±0.05	.XX ±.02	
.X ±0.1	.X ±.1	

THIRD ANGLE PROJECTION

REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓

MATERIAL —

FINISH —

	NAME	DATE
DRAWN	Wayne Hyatt	11/24/74
CHECK	Bill Gay	12/6/74
ENG.		1-24-75
PROJ. ENG.	Rod Hoag	1-27-75
PROG.		1-29-75

NEXT HIGHER ASSY.

B-DD-KK8A-Ø

SCALE —

SHEET 1 OF 2

digital

TITLE
FLOW DIAGRAM
M8315 BUS TIMING

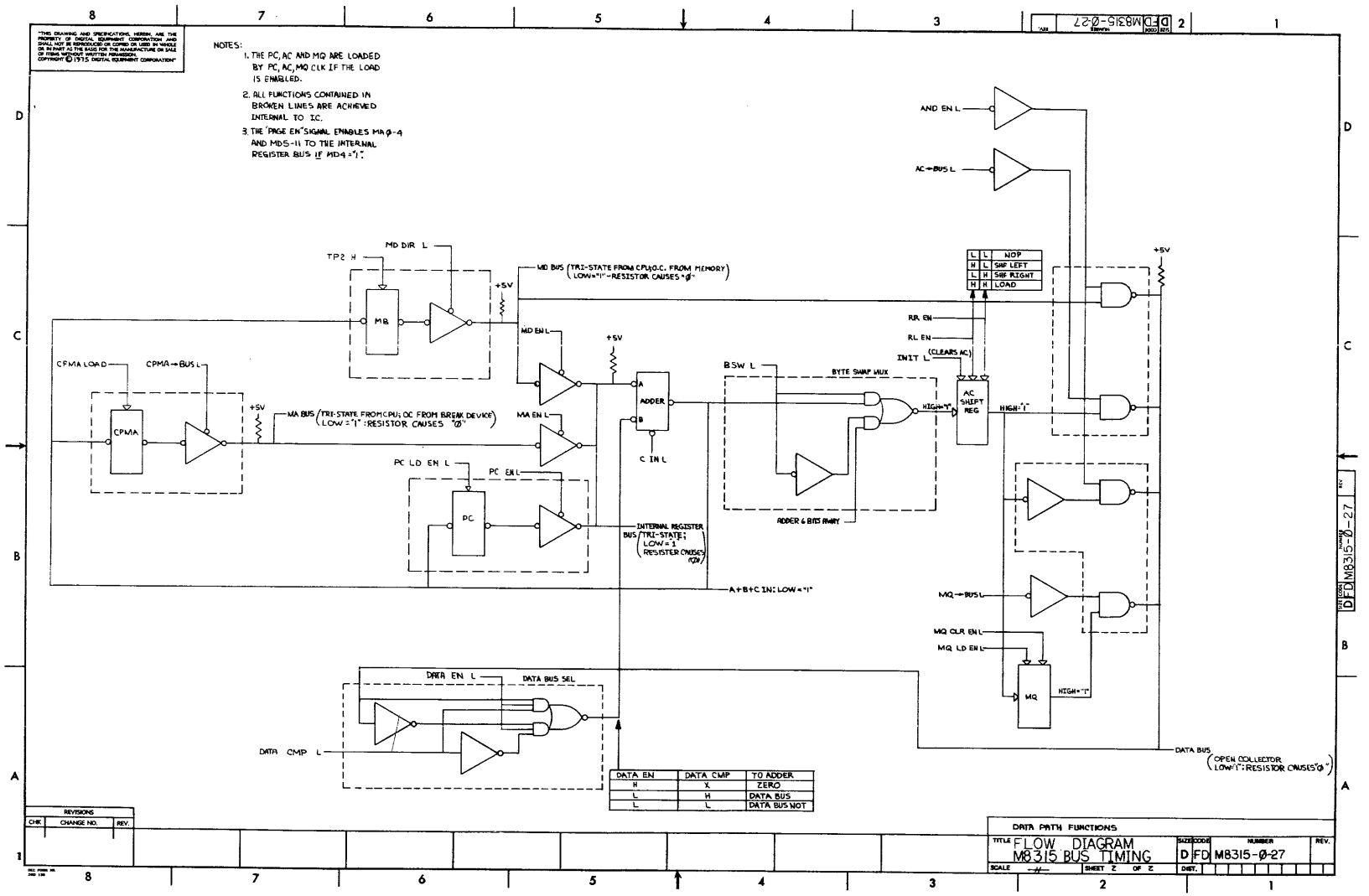
SIZE	CODE	NUMBER	REV.
D	FD	M8315-Ø-27	

DIST.

REVISIONS

REV.	CHANGE NO.	CHK.

SIZE CODE D FD M8315-0-27 REV.


NOTES:
1. THE PC, AC AND MQ ARE LOADED BY PC, AC, MQ CLK IF THE LOAD IS ENABLED.
2. ALL FUNCTIONS CONTAINED IN BROKEN LINES ARE ACHIEVED INTERNAL TO IC.
3. THE "PAGE EN" SIGNAL ENABLES MA 0-4 AND MD 5-11 TO THE INTERNAL REGISTER BUS IF MD 4 = "1".
MD DIR L
TP2 H
MB
MD BUS (TRI-STATE FROM CPU; O.C. FROM MEMORY) LOW = "1" - RESISTOR CAUSES "0"
MD EN L
+5V
CPMA LOAD
CPMA → BUS L
CPMA
MA BUS (TRI-STATE FROM CPU; OC FROM BREAK DEVICE) LOW = "1" : RESISTOR CAUSES "0"
MA EN L
PC LD EN L
PC EN L
PC
ADDER
A
B
C IN L
A+B+C IN: LOW = "1"
INTERNAL REGISTER BUS (TRI-STATE; LOW = 1 RESISTOR CAUSES "0")
BSW L
BYTE SWAP MUX
ADDER & BITS AWRY
HIGH = "1"
AC SHIFT REG
L L NOP
H L SHF LEFT
L H SHF RIGHT
H H LOAD
RR EN
RL EN
INIT L
(CLEARS AC)
AND EN L
AC → BUS L
MQ → BUS L
MQ CLR EN L
MQ LD EN L
MQ
DATA EN L
DATA BUS SEL
DATA CMP L
DATA BUS
(OPEN COLLECTOR LOW "1": RESISTOR CAUSES "0")
DATA EN | DATA CMP | TO ADDER
H | X | ZERO
L | H | DATA BUS
L | L | DATA BUS NOT
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REVISIONS
CHK | CHANGE NO. | REV.
DATA PATH FUNCTIONS
TITLE FLOW DIAGRAM M8315 BUS TIMING
SIZE D | CODE FD | NUMBER M8315-0-27 | REV.
SCALE -H- | SHEET 2 OF 2 | DIST.
DFD M8315-0-27

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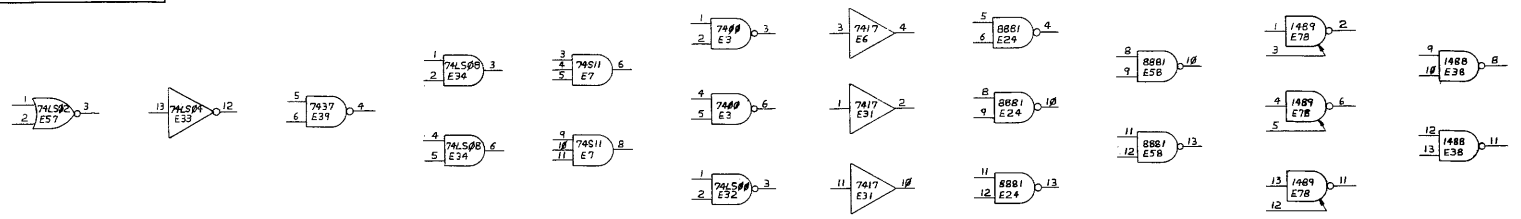
SPARES



M8316 SWITCH SETTINGS

S1-1, S1-2, S1-3, S1-4 } SERIAL LINE BAUD RATE (SEE CHART)

S1-5 ON = REAL TIME CLOCK ENABLED
OFF = REAL TIME CLOCK DISABLED

S1-6 ON = TEST SWITCH (ALWAYS ON)

S1-7 ON = 1 STOP BIT IN SLU CHARACTER
OFF = 2 STOP BITS IN SLU CHARACTER

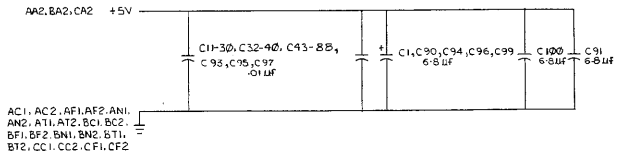
S1-8 ON = ASR/KSR 33 DR35 FILTER IN (ACROSS SLU 20 MA RECV LEADS)
OFF = FILTER OUT

S1-9 ON = TS1 CLEARS "DATA AVAIL" F/F IN PARALLEL I/O SECTION
OFF = "DATA AVAIL" NOT CLEARED BY TS1

SLU BAUD RATE SELECT CHART

	SI-4	SI-3	SI-2	SI-1	BAUD RATE
	ON	ON	ON	ON	50 BAUD
	ON	ON	ON	OFF	75 BAUD
	ON	ON	OFF	ON	110 BAUD
	ON	ON	OFF	OFF	134.5 BAUD
	ON	OFF	ON	ON	150 BAUD
	ON	OFF	ON	OFF	300 BAUD
	ON	OFF	OFF	ON	600 BAUD
	ON	OFF	OFF	OFF	1200 BAUD
	OFF	ON	ON	ON	1800 BAUD
	OFF	ON	ON	OFF	2000 BAUD
	OFF	ON	OFF	ON	2400 BAUD
	OFF	ON	OFF	OFF	3600 BAUD
	OFF	OFF	ON	ON	4800 BAUD
	OFF	OFF	ON	OFF	7200 BAUD
	OFF	OFF	OFF	ON	9600 BAUD
*	OFF	OFF	OFF	OFF	19.2K BAUD

* SERIAL LINE WILL NOT RUN AT THIS BAUD RATE.
THIS SETTING IS NOT TO BE USED



COMPONENT SUBSTITUTION CHART

PART CALLED P/N	DESCRIPTION	SUBSTITUTE PART P/N	DESCRIPTION
1001610-01	0.01 uF DISC.	1001610-00	0.01 uF GLASS
1909705	8881	1909973	97401
1911469	8640	1910392	5380
		1909971	6380
		1910390	7380
		1911113	11380
1912824	74LS74	1905547	7474
1912799	74LS00	1905575	7400
1912807	74LS10	1905576	7410
1912815	74LS30	1905578	7430
1912801	74LS02	1909004	7402
1912803	74LS04	1909686	7404
1912819	74LS42	1910046	7442
1912805	74LS08	1910155	7408
1912853	74LS175	1910651	74175
1912697	74LS174	1910652	74174

REVISIONS	REV.
CHANGE NO.	
ORIGINATED	H
CHK.	

DRN. Hoggmeier 3-9-76
CHK'D Hoggmeier 3-30-76
ENG. 7-2-76
PROJ. ENG. 7-2-76
PROD. 7-2-76
NEXT HIGHER ASSY. D-UA-M8316-0-0
SCALE —
SHEET 1 OF 8

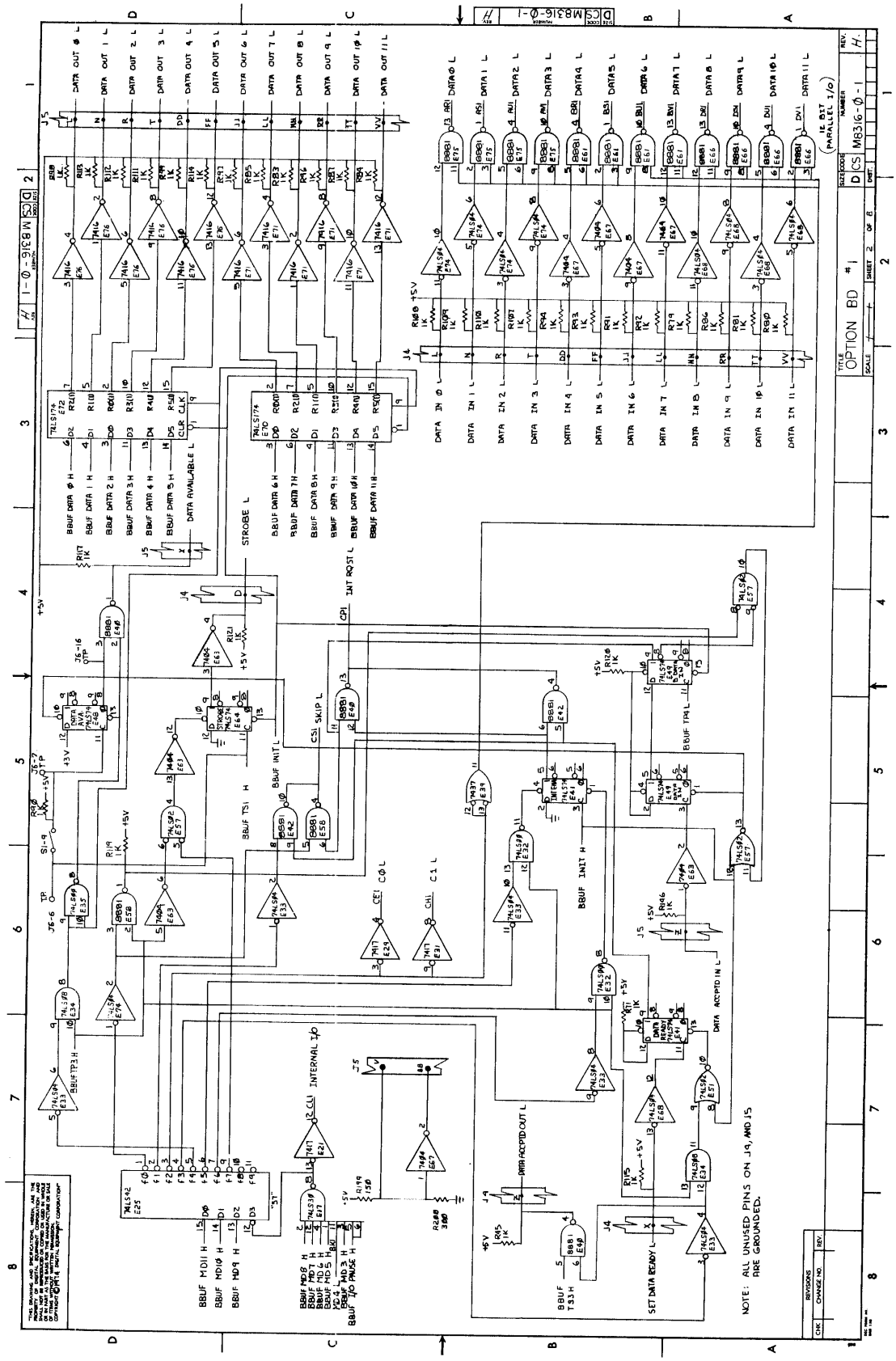
FIRST USED ON DKC 8A

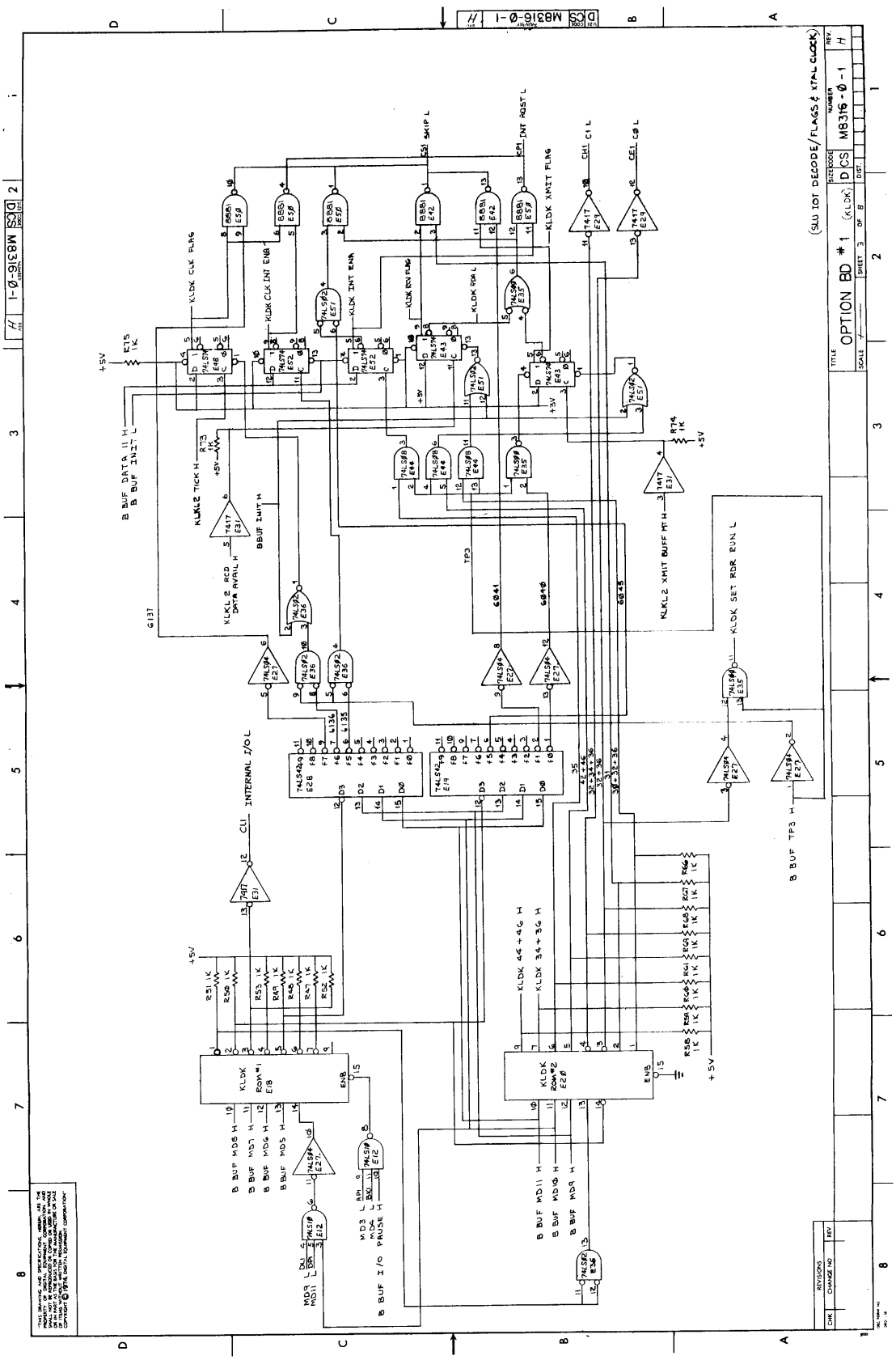
digital

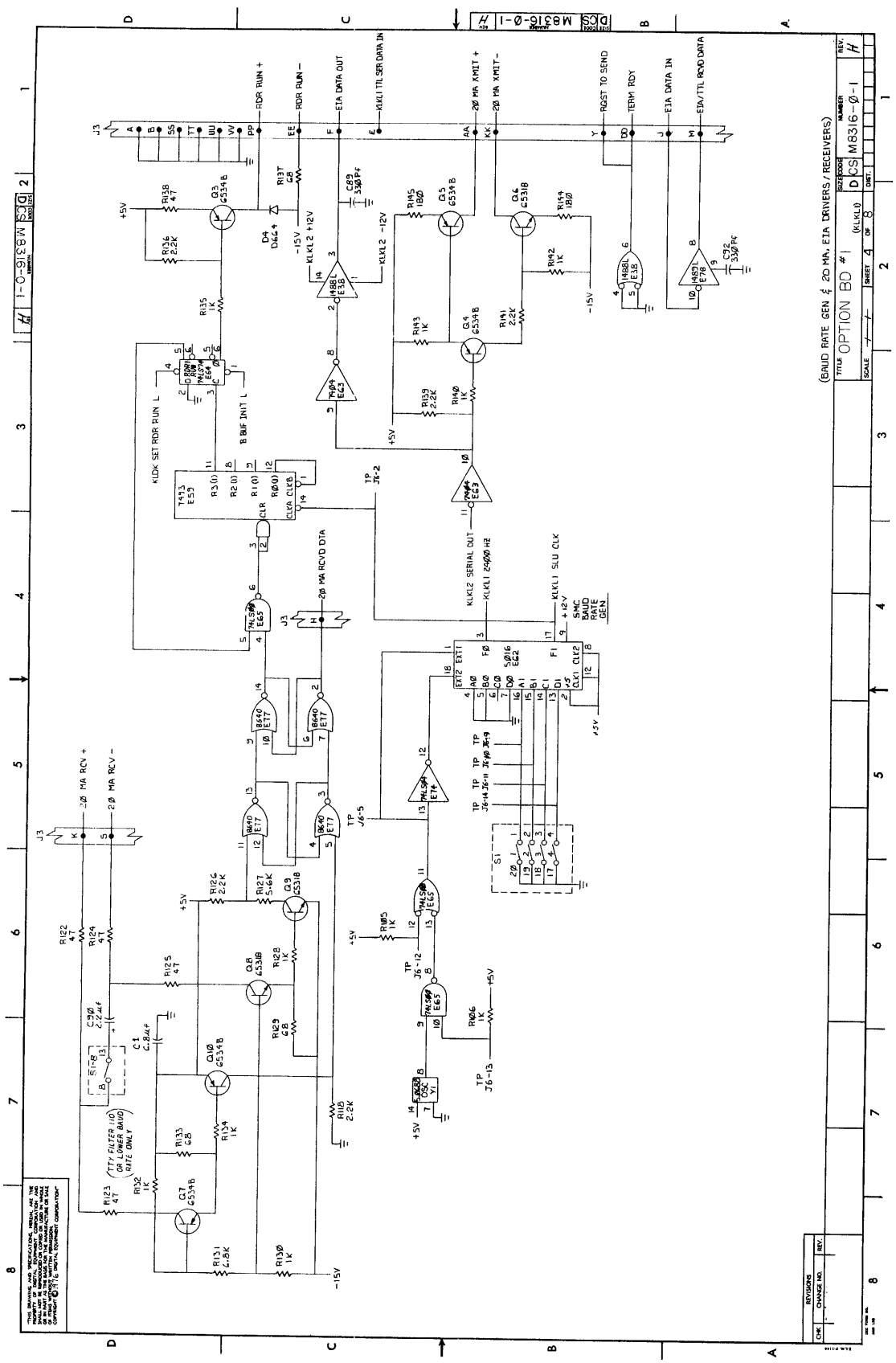
TITLE OPTION BD #1

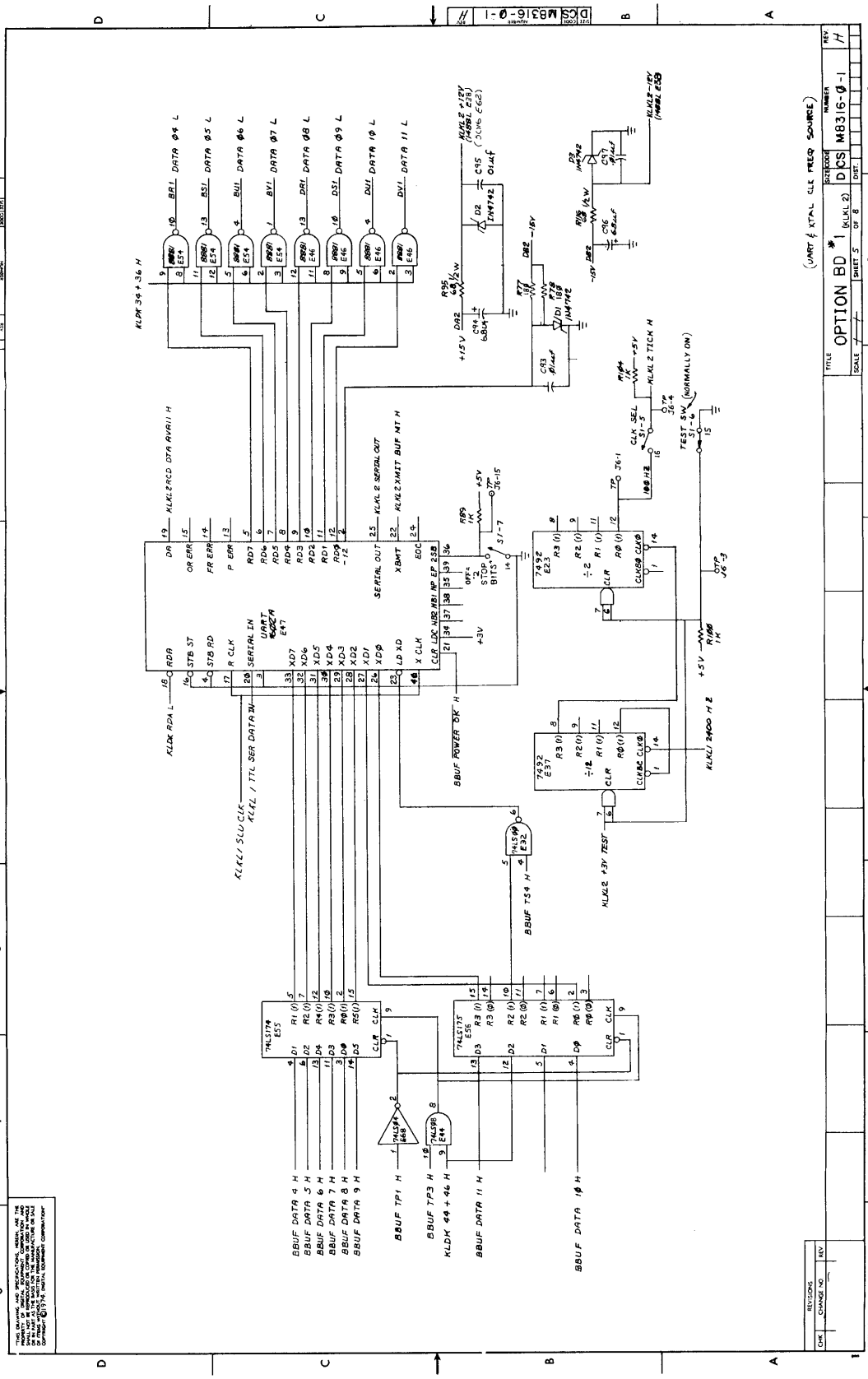
SIZE D CODE CS NUMBER M8316-0-1 REV. H
DIST.

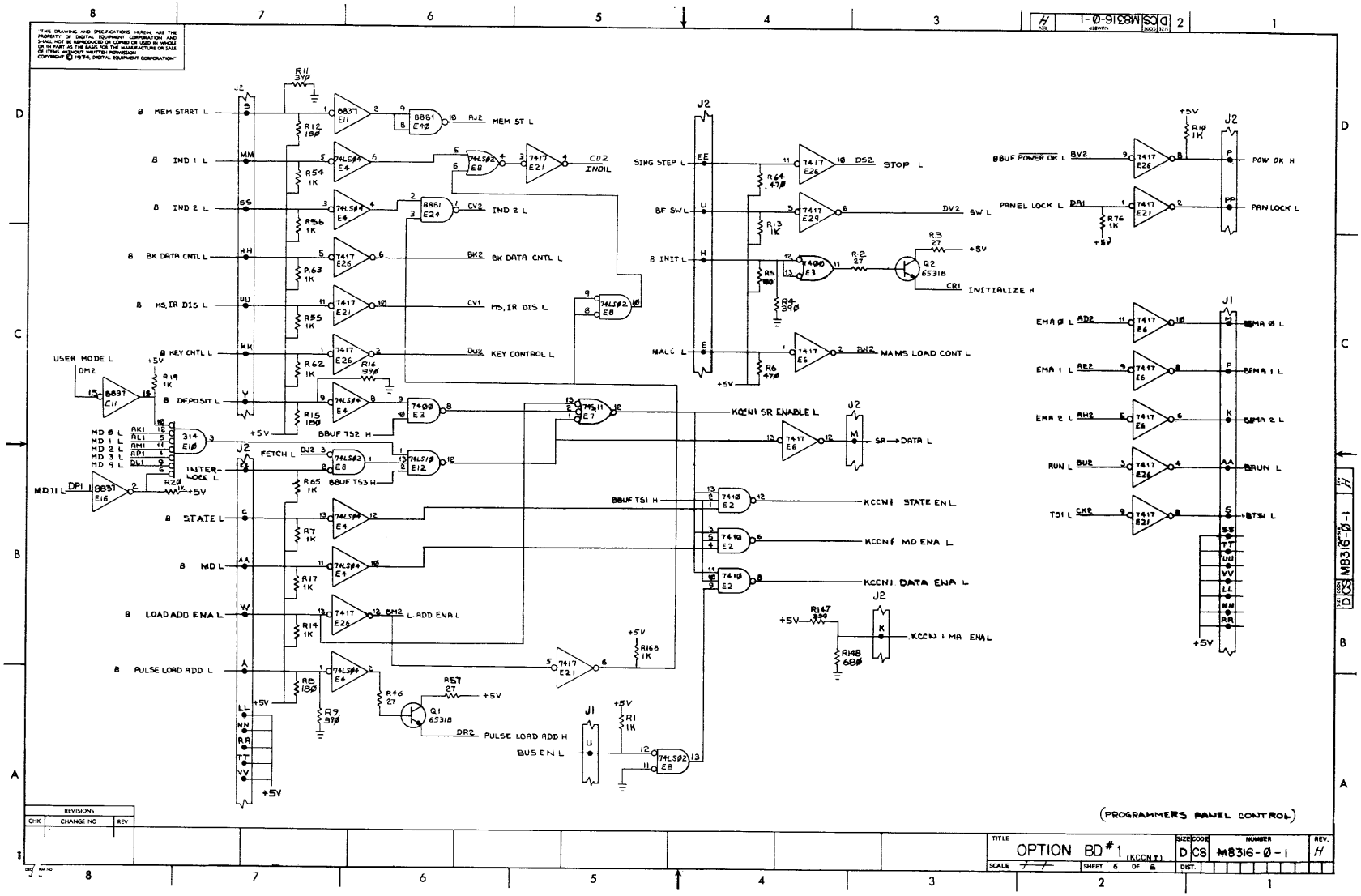
DEC FORM NO. BMY 1102-0


OPTION BD #1
DCS M8316-0-1
IE BST (PARALLEL I/O)
NOTE: ALL UNUSED PINS ON J9, AND J5 ARE GROUNDED.
DATA OUT 0 L
DATA OUT 1 L
DATA OUT 2 L
DATA OUT 3 L
DATA OUT 4 L
DATA OUT 5 L
DATA OUT 6 L
DATA OUT 7 L
DATA OUT 8 L
DATA OUT 9 L
DATA OUT 10 L
DATA OUT 11 L
DATA IN 0 L
DATA IN 1 L
DATA IN 2 L
DATA IN 3 L
DATA IN 4 L
DATA IN 5 L
DATA IN 6 L
DATA IN 7 L
DATA IN 8 L
DATA IN 9 L
DATA IN 10 L
DATA IN 11 L
STROBE L
DATA AVAILABLE L
INT RQST L
DATA ACCEPTD IN L
DATA ACCEPTD OUT L
SET DATA READY L
BBUF INIT H
BBUF INIT L
BBUF TP3 H
BBUF TP4 H
BBUF TP1 H
BBUF TP2 H
BBUF TP3 H
BBUF TP4 H
INTERNAL TP
+5V
+3V


OPTION BD #1 (KLDK)
M8316-0-1
SIZE DCS
SHEET 3 OF 8
SCALE
REVISIONS
CHK
CHANGE NO
REV
(SLU IOT DECODE/FLAGS & XTAL CLOCK)
KLDK CLK FLAG
KLDK CLK INT ENA
KLDK INT ENA
KLDK RDR FLAG
KLDK RDR L
KLDK XMIT FLAG
SKIP L
INT RQST L
CI1 L
CE1 L
+5V
B BUF DATA 11 H
B BUF INIT L
KLKL2 TICK H
BBUF INIT H
KLKL2 RCD DATA AVAIL H
KLKL2 XMIT BUFF MT H
KLDK SET RDR RUN L
TP3
INTERNAL I/O
CLU
KLDK 44-46 H
KLDK 34-36 H
B BUF TP3 H
B BUF MD8 H
B BUF MD7 H
B BUF MD6 H
B BUF MD5 H
B BUF MD11 H
B BUF MD10 H
B BUF MD9 H
B BUF I/O PRUSE H
MD3 L
MD4 L
MDR L
MD11 L
KLDK ROM #1 E18
KLDK ROM #2 E20
ENB
R51 1K
R50 1K
R53 1K
R49 1K
R48 1K
R54 1K
R52 1K
R55 1K
R56 1K
R57 1K
R58 1K
R59 1K
R60 1K
R61 1K
R62 1K
R63 1K
R64 1K
R65 1K
R66 1K
R67 1K
R68 1K
R69 1K
R70 1K
R71 1K
R72 1K
R73 1K
R74 1K
R75 1K


M8316-0-1
RDR RUN +
RDR RUN –
EIA DATA OUT
KLKLI TTL SER DATA IN
20 MA XMIT +
20 MA XMIT –
RQST TO SEND
TERM RDY
EIA DATA IN
EIA/TTL RCVD DATA
(BAUD RATE GEN & 20 MA, EIA DRIVERS/RECEIVERS)
OPTION BD #1
M8316-0-1
KLOK SET RDR RUN L
B BUF INIT L
20 MA RCVD DTA
KLKL2 SERIAL OUT
KLKLI 2400 HZ
KLKLI SLU CLK
SMC BAUD RATE GEN
20 MA RCV +
20 MA RCV –
TTY FILTER (10 CHAR LOWER BAUD RATE ONLY)
+5V
–15V
+12V
–12V

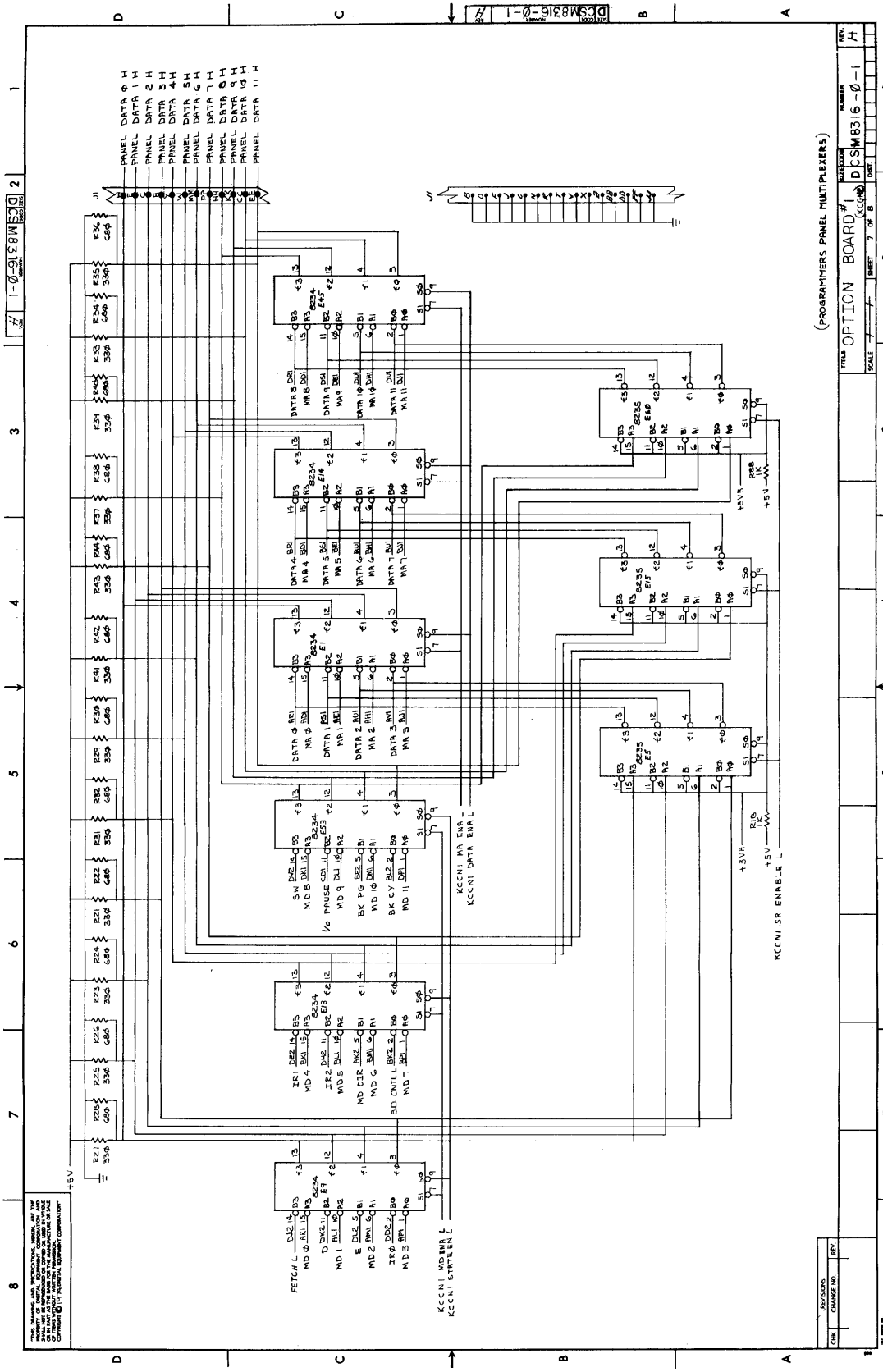

OPTION BD #1 (KLKL 2)
M8316-0-1
(UART & XTAL CLK FREQ SOURCE)
KLPX 34 + 36 H
KLKL2 RCD DTA AVAIL H
KLDK RDA L
KLKL / TTL SER DATA IN
KLKL / SLO CLK
KLKL2 SERIAL OUT
KLKL2 XMIT BUF MT H
BBUF POWER OK H
BBUF TP1 H
BBUF TP3 H
KLDK 44 + 46 H
BBUF TS4 H
KLKL2 +3V TEST
KLKL 2400 H Z
KLKL2 TICK H
TEST SW (NORMALLY ON)
BBUF DATA 4 H
BBUF DATA 5 H
BBUF DATA 6 H
BBUF DATA 7 H
BBUF DATA 8 H
BBUF DATA 9 H
BBUF DATA 11 H
BBUF DATA 10 H
DATA 04 L
DATA 05 L
DATA 06 L
DATA 07 L
DATA 08 L
DATA 09 L
DATA 10 L
DATA 11 L

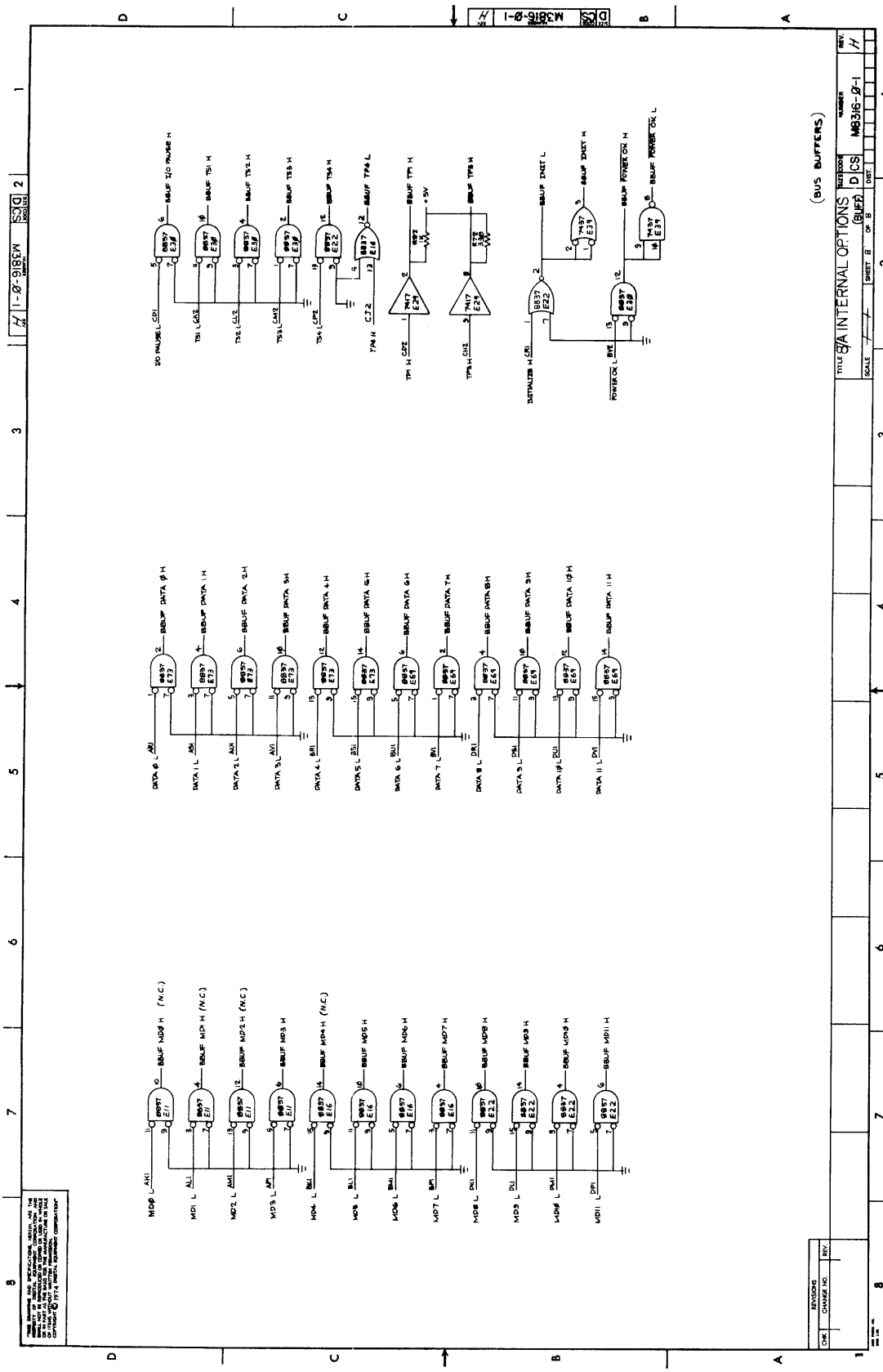


H-30

REVISIONS		
CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV.
OPTION BD # 1 (KCCN 1)	D	CS	M8316-Ø-1	H
SCALE	SHEET 6 OF 8		DIST.	


OPTION BOARD #1
(PROGRAMMERS PANEL MULTIPLEXERS)
DCSM8316-0-1
KCCNI MA ENA L
KCCNI DATA ENA L
KCCNI MD ENA L
KCCNI STATE EN L
KCCNI SR ENABLE L
FETCH L
PANEL DATA 0 H
PANEL DATA 1 H
PANEL DATA 2 H
PANEL DATA 3 H
PANEL DATA 4 H
PANEL DATA 5 H
PANEL DATA 6 H
PANEL DATA 7 H
PANEL DATA 8 H
PANEL DATA 9 H
PANEL DATA 10 H
PANEL DATA 11 H


M8316-0-1
(BUS BUFFERS)
8A INTERNAL OPTIONS (BUFF)
M8316-0-1
SIZE D
SCALE
SHEET 8 OF 8
REVISIONS
CHK
CHANGE NO.
REV.

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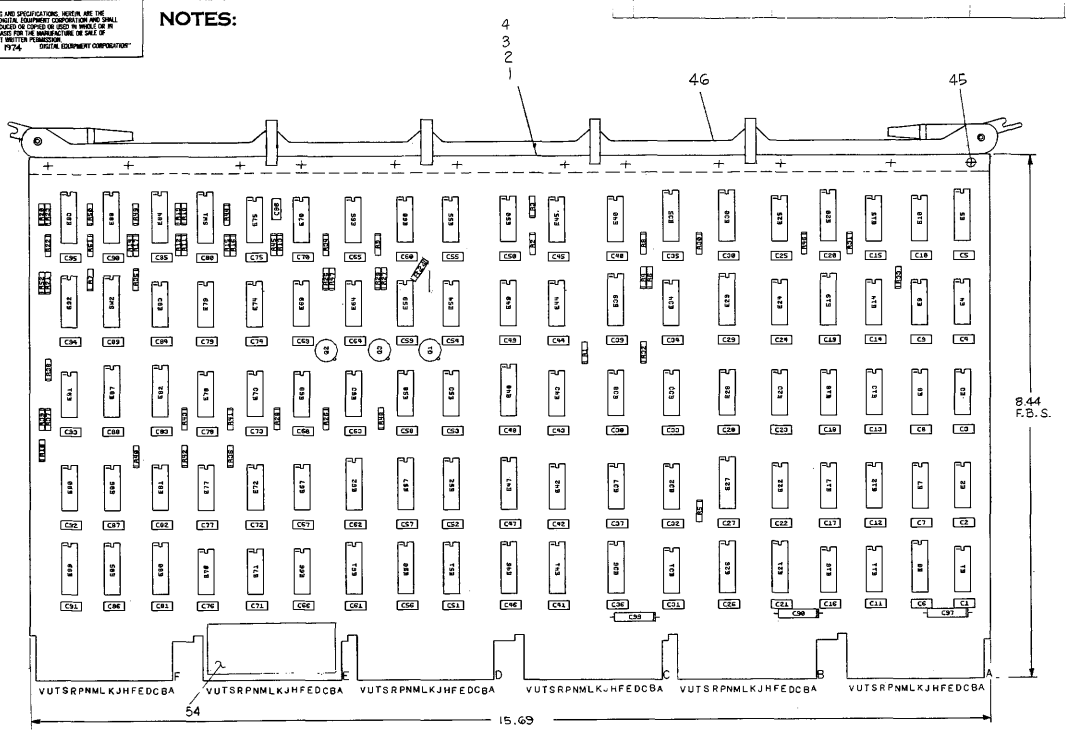
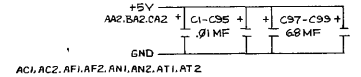
NOTES:





AC1, AC2, AF1, AF2, AN1, AN2, AT1, AT2
BC1, BC2, BF1, BF2, BN1, BN2, BT1, BT2
CC1, CC2, CF1, CF2, CN1, CN2, CT1, CT2
DC1, DC2, DF1, DF2, DN1, DN2, DT1, DT2

IC 7442	8	16
IC 314	1	8
IC 8234	8	16
IC 74173	8	16
IC 74153	8	16
IC 74S257	8	16
IC 8837	8	16
IC 7473	11	4
IC 8266	8	16
IC 74175	8	16
IC TYPE	GND	+5V

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

REV.	ORIGINATED	CHANGE NO.	CHK
K	1-SEP-76	M8317-00006	
J	30-JUN-76	M8317-00005	
H	13-JAN-76	M8317-00004	
F	11-SEP-75	M8317-00003	
E	10-DEC-74	M8317-00002	
D	27-NOV-74	M8317-00001	
C			

DEC NO.	EIA NO.	DEC NO.	EIA NO.

SEMICONDUCTOR CONVERSION CHART

REF		DESCRIPTION	PART NO.	ITEM NO.
REF		X-Y COORDINATE HOLE LOCATION	K-CO-M8317-0-4	1
REF		ASSY/DRILLING HOLE LAYOUT	D-AH-M8317-0-5	2
REF		MODULE ECO HISTORY	B-MH-M8317-0-6	3
1		ETCHED CIRCUIT BOARD	5010938	4
1	C96	CAP 5000 PF 100V DISC	1981765	5
95	C1-C95	CAP .01 MF 100V 20%	1991618-01	6
3	C97-C99	CAP 6.8 MF 35V 10%	1995386	7
2	SW1, SW2	DIP SWITCH	1211164-04	8
46	R1-R23,R26,R28-R43,R46, R49-R52 R24	RES. 1K 1/4W 5%	1398365	9
1	R44	RES. 100 OHM 1/4W 5%	1398229	10
4	R25,R27,R47,R48	RES. 27 OHM 1/4W 5%	1391522	11
				12
3	Q1,Q2,Q3	TRANSISTOR DEC3009B	1503100	13
6	E9,50,63,65,78,79	I.C. 7474	1985547	14
6	E12,13,28,54,73,75	I.C. 7408	1985575	15
1	E33	I.C. 7418	1985576	16
2	E18,E49	I.C. 7420	1985577	17
1	E11	I.C. 7430	1985578	18
1	E80	I.C. 7473	1985587	19
3	E14,E32,E69	I.C. 7402	1989004	20
6	E31,34,44,45,80,85	I.C. 74S11	1910537	21
2	E46,E57	I.C. 74S257	1911641	22
1	E8	I.C. 74S74	1910544	23
6	E10,17,66,72,76,77	I.C. 8881	1989705	24
2	E4,E38	I.C. 7417	1989929	25
2	E84,E92	I.C. 8266	1989934	26
1	E29	I.C. 74153	1989937	27
1	E22	I.C. 74S00	1910532	28
2	E83,E91	I.C. 74197	1910035	29
1	E79	I.C. 74164	1910841	30
2	E35,E39	I.C. 7442	1910846	31
3	E25,E71,E74	I.C. 7437	1910891	32
4	E40,E55,E64,E68	I.C. 7408	1910155	33
1	E37	I.C. 314	1909704	34
2	E60,E85	I.C. 74175	1910651	35
1	E24	I.C. 8093	1910837	36
2	E53,E81	I.C. 7427	1910878	37
2	E47,E52	I.C. 8234	1911315	38
6	E19,20,30,48,51,56	I.C. 74173	1911338	39
8	E15,E23,E43,E58,E59,E67	I.C. 7404	1909686	40
1	E82 SEE NOTE 2	I.C. MIKP ROM #1 (256 X 4)	23-156A2	41
1	E87 SEE NOTE 2	I.C. MIKP ROM #2 (256 X 4)	23-L59A2	42
1	E26	I.C. MIKP ROM #3 (32 X 8)	23-086A1	43
1	E27	I.C. KMTS ROM #1 (256 X 4)	23-086A2	44
12		EYELET, HANDLE	9008732	45
1		HANDLE ASSY	1210711-2	46
4	E1,E2,E3,E7	I.C. 7412	1909955	47
6	E21,E36,E41,E61,E62,E6	I.C. 8837	1911116	48
1	E16	I.C. 74S04	1910534	49
1	E42	I.C. 74S10	1910536	50
4	E82,E87,E88,E93	SOCKET, 16 PIN	1211813	51
1	R45	RES. 220 1/4W 5%	1300271	52
A/R		WIRE #30 AWG,	9N-05740-55	53
.05		DECAL	7415856	54

PARTS LIST

FIRST USED ON OPTION MODEL: KM8-A
ETCH BOARD REV: D

		DATE
DRN.	E Sobking	6-27-74
DES.	Bob Kopec	10-10-74
ENGR.	Larry Marble	10-10-74
PROJ. ENG.	Larry Marble	10-10-74
ENGR.	[illegible]	10-10-74

NEXT HIGHER ASSY: B-DD-KM8-A
SCALE: NONE
SHEET 1 OF 7

digital

TITLE: OPTION BOARD #2

SIZE D | CODE CS | NUMBER M8317-0-1 | REV. K

DIST.

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BOOTSTRAP/AUTO RESTART FUNCTIONAL SWITCH SETTINGS

DESIRED FUNCTION	ACTIVATING SIGNAL	S1-4	S1-5	S1-6	S1-7	S1-8	S2-1
BOOTSTRAP ENABLED	"BOOT" SW	*		OFF	OFF	ON	N/A
AUTO-RESTART DISABLED	N/A						
BOOTSTRAP ENABLED	"BOOT" SW	*		ON	ON	ON	N/A
AUTO-RESTART ENABLED	"AC LOW"						
BOOTSTRAP DISABLED	N/A	*	SPARE	ON	ON	OFF	N/A
AUTO-RESTART ENABLED	"AC LOW"						
BOOTSTRAP ENABLED	"AC LOW"	*		ON	OFF	OFF	N/A
AUTO-RESTART DISABLED	N/A						
BOOTSTRAP ENABLED	"AC LOW" OR "BOOT" SW	*		ON	OFF	ON	N/A
AUTO-RESTART DISABLED	N/A						
TIME SHARE DISABLED	N/A	N/A	N/A	N/A	N/A	N/A	ON
TIME SHARE ENABLED	N/A	N/A	N/A	N/A	N/A	N/A	OFF

NOTES:

* S1-4 "OFF" - BOOTSTRAP CAN BE ACTIVATED BY "BOOT" SW EITHER IN THE "RUN" OR "RUN" STATE
S1-4 "ON" - BOOTSTRAP CAN ONLY BE ACTIVATED BY "BOOT" SW IN THE "RUN" STATE

1. "AC LOW" WILL CAUSE AUTO-RESTART OR BOOTSTRAP, DEPENDING ON SWITCH SETTINGS, TO OCCUR ONLY IN THE "RUN" OR STOPPED STATE
   S1-6,7,8 "OFF" - BOOTSTRAP & AUTO-RESTART DISABLED
2. E82 & E8T ARE NOT ON THE YA VARIATION. ALL OTHER PARTS REMAIN THE SAME
3. IF AUTO-RESTART IS ENABLED, THE AUTO-START FEATURE OF THE CPU (M8315) MUST BE DISABLED

BOOTSTRAP SELECT SWITCH SETTINGS

PROGRAM	S2-5	S2-6	S2-7	S2-8	S1-1	S1-2	S1-3	ROM ST ADD	MEM ADD START
HI-LO PT RDR	ON	ON	ON	OFF	ON	ON	ON	2Ø	7734
RK8E	ON	OFF	ON	OFF	ON	OFF	ON	124	24
RX8E	ON	OFF	OFF	ON	OFF	ON	ON	164	33
RF88/DF32D	OFF	ON	OFF	ON	OFF	ON	OFF	252	7754
TA8E	OFF	ON	OFF	OFF	OFF	ON	OFF	272	4ØØØ

3. BOOTSTRAP SELECT SWITCHES ARE DEFINED AS FOLLOWS:
   (a) ROM ADDRESS RANGE: Ø-377
   (b) ON = LOGIC Ø OR LOW; OFF = LOGIC 1 OR HIGH
   (c) ORDER OF SIGNIFICANCE
   $S_B5 = 2^7 = 200$ (MSB)
   $S_B6 = 2^6 = 100$
   $S_B7 = 2^5 = 40$
   $S_B8 = 2^4 = 20$
   $S_11 = 2^3 = 10$
   $S_12 = 2^2 = 4$
   $S_13 = 2^1 = 2$

   THE LSB OF ADDRESS IS CONTROLLED BY THE BOOTSTRAP/AUTO-RESTART LOGIC

AUTO-RESTART SELECT SWITCH SETTINGS

RESTART ADDRESS	S2-2	S2-3	S2-4
Ø	OFF	OFF	OFF
2ØØ	OFF	ON	OFF
4ØØ	ON	OFF	OFF
6ØØ	ON	ON	OFF

4. AUTO-RESTART SELECT SWITCHES ARE DEFINED AS FOLLOWS:
   (a) ROM ADDRESS RANGE: Ø-16
   (b) ON = LOGIC 1 OR LOW; OFF = LOGIC Ø OR HIGH
   (c) ORDER OF SIGNIFICANCE
   $S_B2 = 2^3 = 10$
   $S_B3 = 2^2 = 4$
   $S_B4 = 2^1 = 2$

COMPONENT SUBSTITUTION CHART

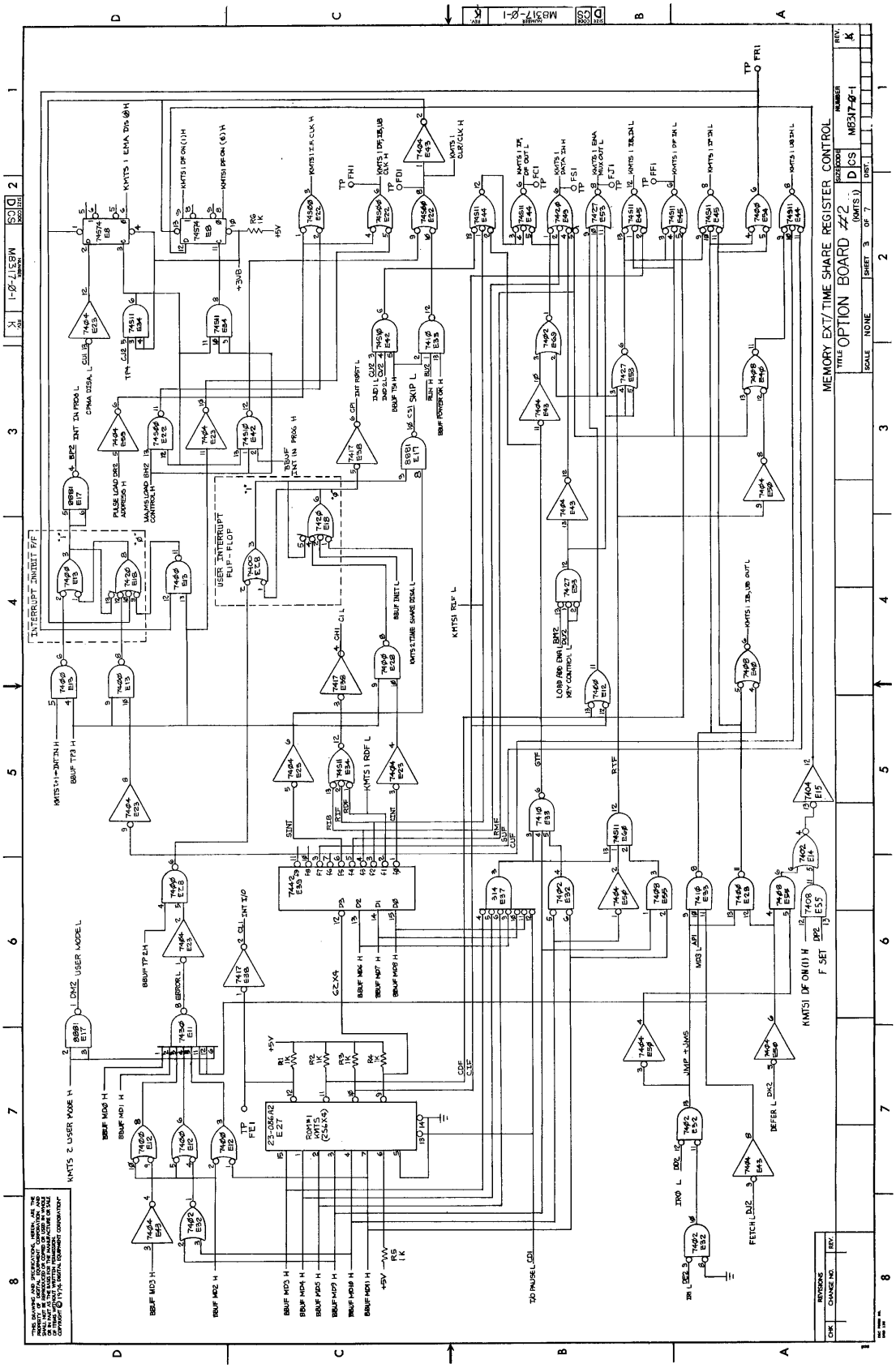
PART CALLED FOR			SUBSTITUTE PART		
QTY	PART NO.	DESCRIPTION	QTY	PART NO.	DESCRIPTION
95	1001610-01	.01 UFD DISC	95	1001610-00	.01 UFD GMSE
3	1503100	DEC 30098	3	1509338	DEC 6531
6	1911330	74173	6	1911711	8T10
1	1909704	314	1	1910391	5314
			1	1909972	6314
			1	1910389	7314
6	1909705	8881	6	1909973	97401

REVISIONS		
CHK	CHANGE NO.	REV.

QTY	REF. DESIGNATION	DESCRIPTION	PART NO.	ITEM NO

TITLE: OPTION BOARD #2
SIZE: D | CODE: CS | NUMBER: M8317-Ø-1 | REV: K
SCALE: NONE | SHEET 2 OF 7 | DIST.

M8317-Ø-1 K SOD


MEMORY EXT/TIME SHARE REGISTER CONTROL
TITLE OPTION BOARD #2 (KMTS 1)
SIZE CODE DWG NO. MB317-0-1
SCALE NONE SHEET 3 OF 7 DWG.
REV. K
INTERRUPT INHIBIT F/F
USER INTERRUPT FLIP-FLOP
KMTS 1 EMA DIS (8) H
KMTS 1 DF ON (1) H
KMTS 1 DF ON (8) H
KMTS 1 CLR/CLK H
KMTS 1 DF, DF OUT L
KMTS 1 DATA IN H
KMTS 1 EMA INHIBIT L
KMTS 1 DF IN L
KMTS 1 DF IN L
KMTS 1 USER MODE L
KMTS 1 USER MODE H
KMTS 1 DF ON (1) H
F SET
DEFER L
FETCH L
IOD PULSE L
IOI L
JUMP + JAMS
KMTS 1 RDF L
KMTS & TIME SHARE DISAL L
USER INT REQ L
INT IN PROG H
PULSE LOAD DRS ADDRESS H
JAMS LOAD BR12 CONTROL H
CPMA DISA L
SKIP L
KEY CONTROL
LOAD ADR ENA L
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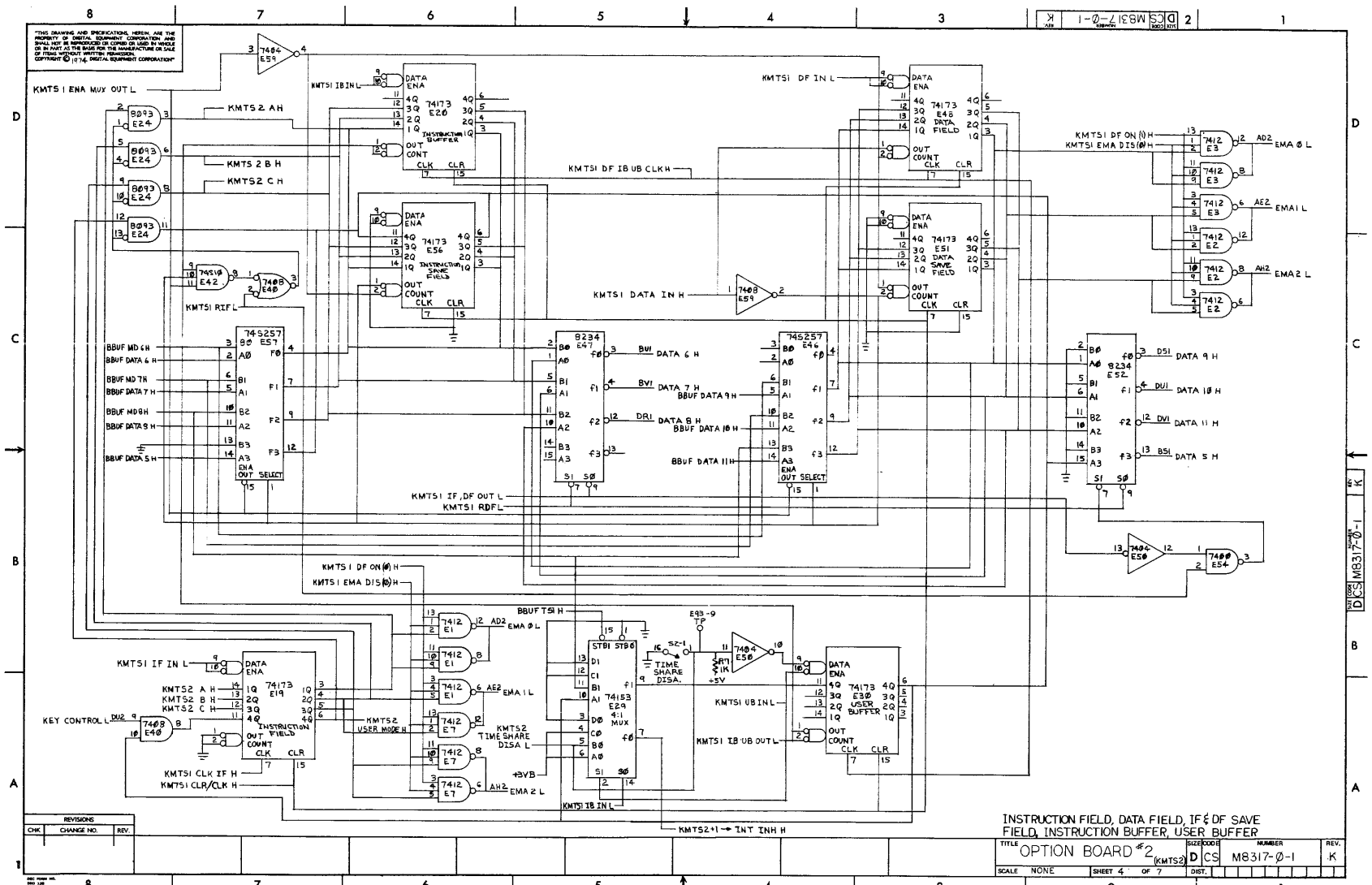
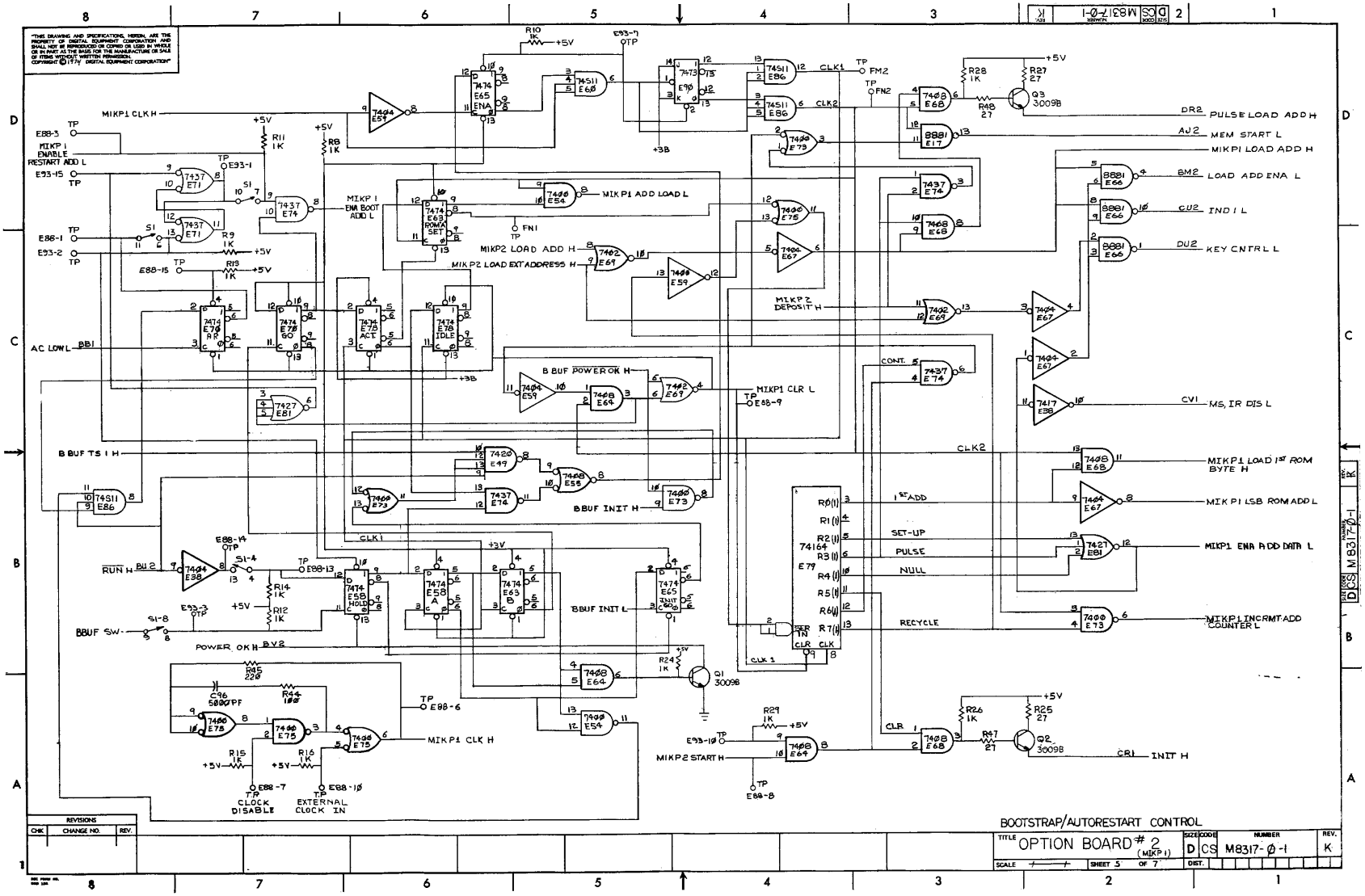
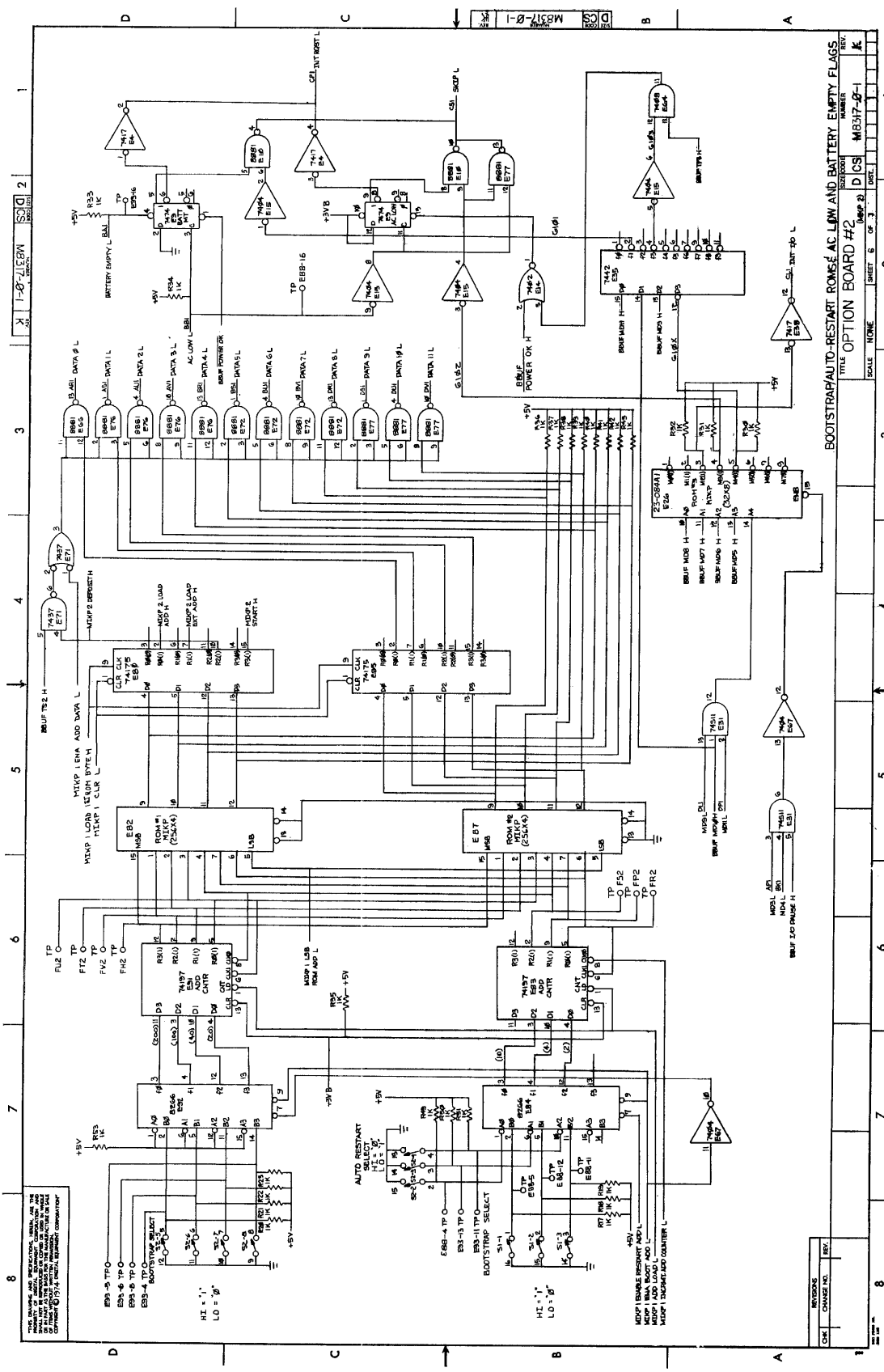

KMTS1 ENA MUX OUT L
KMTS2 A H
KMTS2 B H
KMTS2 C H
KMTS1 IB IN L
KMTS1 DF IN L
KMTS1 DF IB UB CLK H
KMTS1 DATA IN H
KMTS1 R1F L
KMTS1 IF,DF OUT L
KMTS1 RDF L
KMTS1 DF ON (1) H
KMTS1 EMA DIS (0) H
KMTS1 IF IN L
KEY CONTROL L
KMTS1 CLK IF H
KMTS1 CLR/CLK H
KMTS2 USER MODE H
KMTS2 TIME SHARE DISA L
KMTS1 UB IN L
KMTS1 IB UB OUT L
KMTS1 IB IN L
BBUF TS1 H
+3VB
KMTS2+1 → INT INH H
BBUF MD 6 H
BBUF DATA 6 H
BBUF MD 7 H
BBUF DATA 7 H
BBUF MD 8 H
BBUF DATA 8 H
BBUF DATA 5 H
DATA 6 H
DATA 7 H
BBUF DATA 9 H
DATA 8 H
BBUF DATA 10 H
BBUF DATA 11 H
DATA 9 H
DATA 10 H
DATA 11 H
DATA 5 H
EMA Ø L
EMA 1 L
EMA 2 L
TIME SHARE DISA.
INSTRUCTION BUFFER
INSTRUCTION SAVE FIELD
USER BUFFER
INSTRUCTION FIELD, DATA FIELD, IF & DF SAVE FIELD, INSTRUCTION BUFFER, USER BUFFER
OPTION BOARD #2 (KMTS2)
SIZE D
CODE CS
NUMBER M8317-Ø-1
REV. K
SCALE NONE
SHEET 4 OF 7
DIST.


MIKP1 CLK H
MIKP1 ENABLE RESTART ADD L
MIKP1 ENA BOOT ADD L
MIKP2 LOAD ADD H
MIKP2 LOAD EXT ADDRESS H
MIKP1 ADD LOAD L
MIKP2 DEPOSIT H
AC LOW L
B BUF TS 1 H
B BUF POWER OK H
MIKP1 CLR L
B BUF INIT H
B BUF INIT L
RUN H
BBUF SW
POWER OK H
CLK1
CLK2
SET-UP
PULSE
NULL
RECYCLE
1ST ADD
MIKP1 CLK H
MIKP2 START H
CLOCK DISABLE
EXTERNAL CLOCK IN
DR2 PULSE LOAD ADD H
AU2 MEM START L
MIKP1 LOAD ADD H
BM2 LOAD ADD ENA L
CU2 IND I L
DU2 KEY CNTRL L
CVI MS, IR DIS L
MIKP1 LOAD 1ST ROM BYTE H
MIKP1 LSB ROM ADD L
MIKP1 ENA ADD DATA L
MIKP1 INCRMT ADD COUNTER L
CRI INIT H
BOOTSTRAP/AUTORESTART CONTROL
OPTION BOARD # 2 (MIKP1)
M8317-Ø-1


BOOTSTRAP/AUTO-RESTART ROM'S AC LOW AND BATTERY EMPTY FLAGS
OPTION BOARD #2
M8317-0-1
DCS
AUTO RESTART SELECT
BOOTSTRAP SELECT
BATTERY EMPTY L
AC LOW L
BBUF POWER OK H
MIKP I ENA ADD DATA L
MIKP I LOAD 1ST/2ND BYTE H
MIKP I CLR L
MDVP I ENABLE RESTART ADD L
MDVP I BOOT ADD L
MDVP I RESTART ADD L
MDVP I TADPAK ADD COUNTER L

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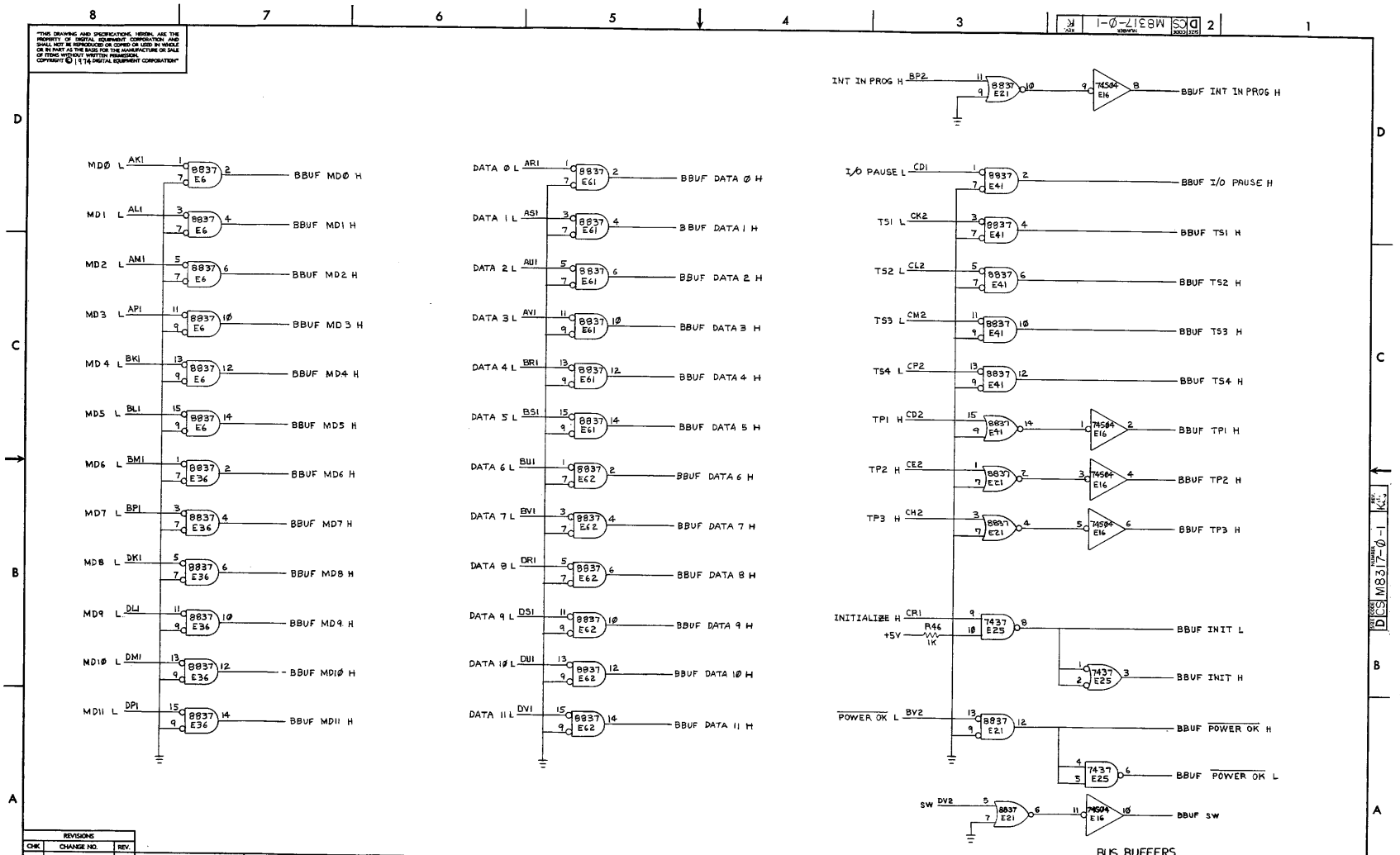
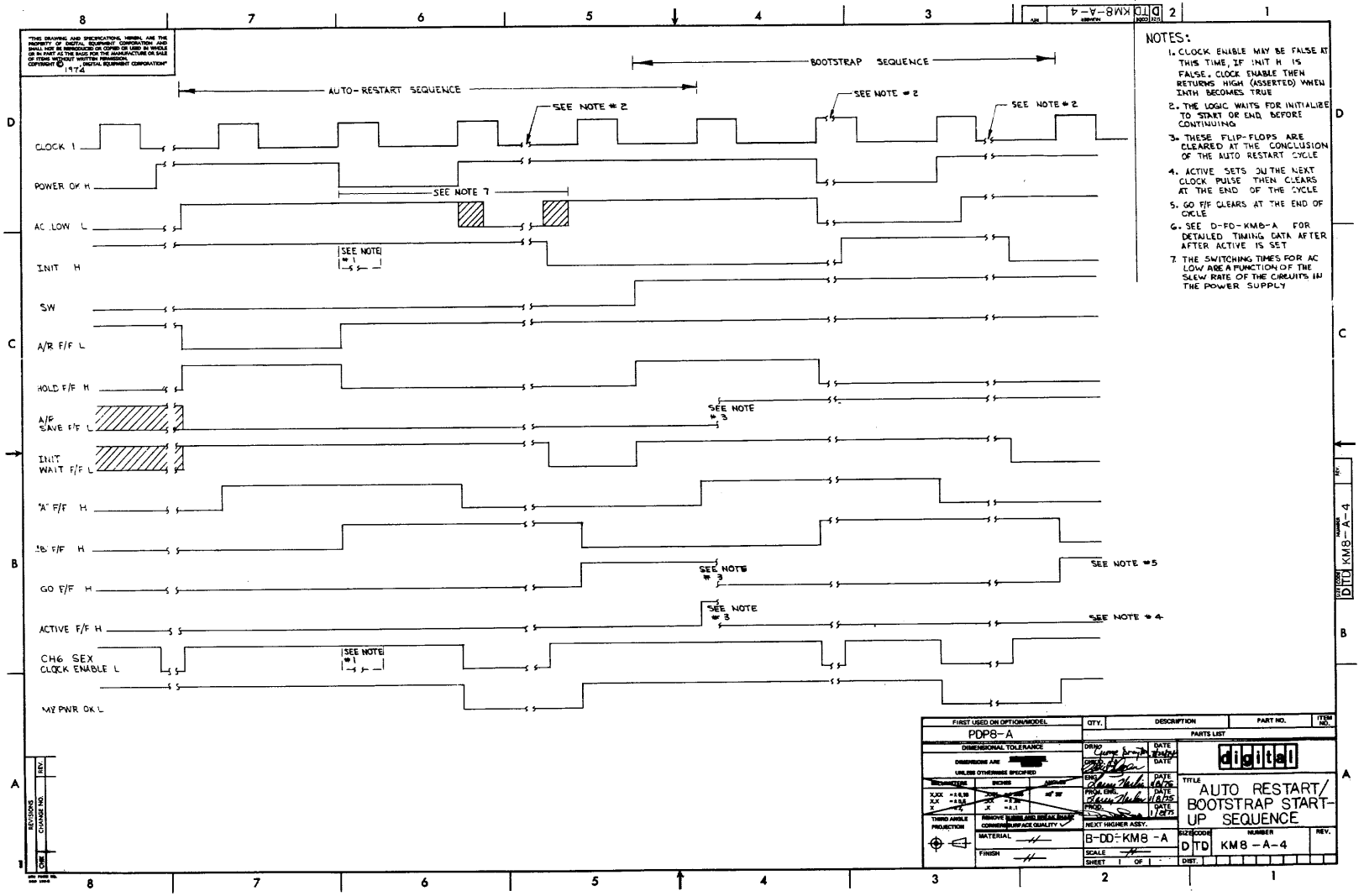


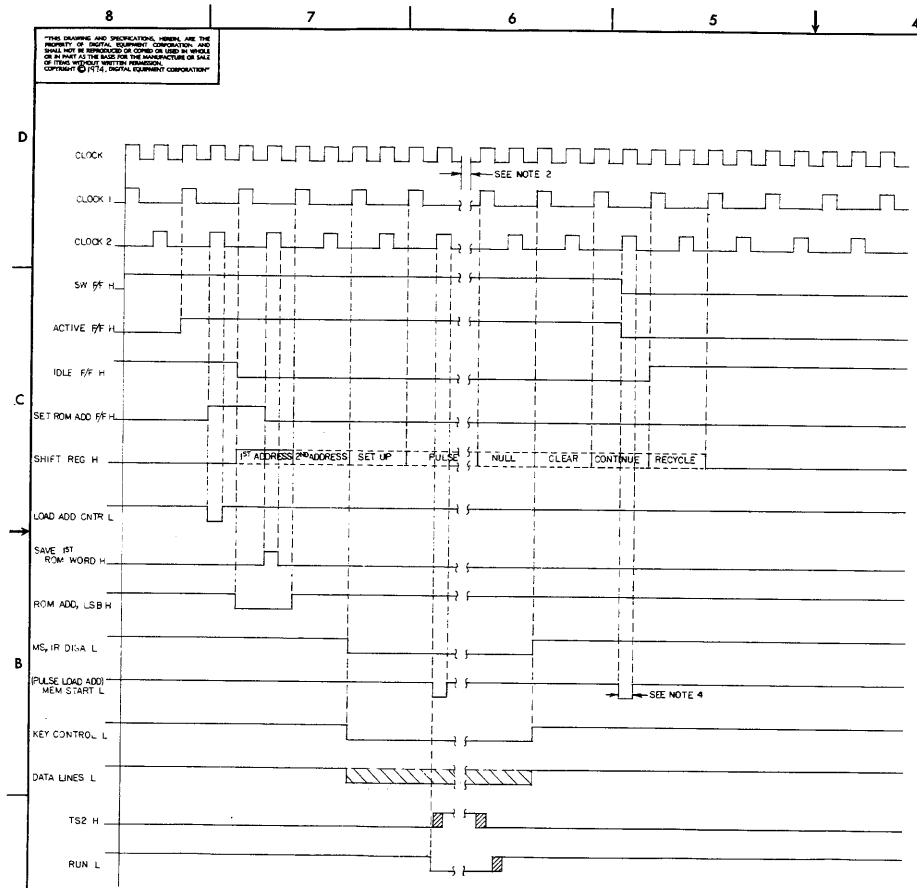
BUS BUFFERS

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
8/A INTERNAL OPTION #2 (BBUF)	D	CS	M8317-Ø-1	K

SCALE NONE · SHEET 7 OF 7 · DIST.


BOOTSTRAP SEQUENCE
AUTO-RESTART SEQUENCE
SEE NOTE # 2
SEE NOTE # 2
SEE NOTE # 2
CLOCK 1
POWER OK H
SEE NOTE 7
AC LOW L
SEE NOTE #1
INIT H
SW
A/R F/F L
HOLD F/F H
SEE NOTE #3
A/F SAVE F/F L
INIT WAIT F/F L
"A" F/F H
"B" F/F H
SEE NOTE #3
SEE NOTE #5
GO F/F H
SEE NOTE #3
SEE NOTE #4
ACTIVE F/F H
SEE NOTE #1
CH6 SEX CLOCK ENABLE L
MY PWR OK L
NOTES:
1. CLOCK ENABLE MAY BE FALSE AT THIS TIME, IF INIT H IS FALSE. CLOCK ENABLE THEN RETURNS HIGH (ASSERTED) WHEN INTH BECOMES TRUE
2. THE LOGIC WAITS FOR INITIALIZE TO START OR END BEFORE CONTINUING
3. THESE FLIP-FLOPS ARE CLEARED AT THE CONCLUSION OF THE AUTO RESTART CYCLE
4. ACTIVE SETS ON THE NEXT CLOCK PULSE THEN CLEARS AT THE END OF THE CYCLE
5. GO F/F CLEARS AT THE END OF CYCLE
6. SEE D-FD-KM8-A FOR DETAILED TIMING DATA AFTER AFTER ACTIVE IS SET
7. THE SWITCHING TIMES FOR AC LOW ARE A FUNCTION OF THE SLEW RATE OF THE CIRCUITS IN THE POWER SUPPLY
FIRST USED ON OPTION/MODEL
PDP8-A
QTY.
DESCRIPTION
PART NO.
ITEM NO.
PARTS LIST
DIMENSIONAL TOLERANCE
UNLESS OTHERWISE SPECIFIED
DRWN
ENG
PROJ. ENG.
PROJ. MGR.
DATE
NEXT HIGHER ASSY.
B-DD-KM8-A
MATERIAL
FINISH
SCALE
SHEET
OF
digital
TITLE
AUTO RESTART/ BOOTSTRAP START-UP SEQUENCE
SIZE/CODE
D TD
NUMBER
KM8-A-4
REV.
DIST.
REVISIONS
CHANGE NO.
REV.
CHK
KM8-A-4



NOTES:

1. ONE "DEPOSIT" CYCLE IS SHOWN IN DIAGRAM.
2. WHEN "RUN" IS TRUE (LOW) ALL TIMING IS HELD OFF UNTIL THE NEXT CLOCK PULSE AFTER "RUN" GOES FALSE (HIGH).
3. FOR THE "LOAD ADD" CYCLE SIGNALS REMAIN THE SAME AS SHOWN EXCEPT THAT "PULSE LOAD ADD" REPLACES "MEM START" AND "KEY CONTROL" IS NEGATED. FOR "EXT LOAD ADD" KEY CONTROL IS TRUE.
4. MEM START APPEARS HERE ONLY FOR THE "START" FUNCTION. THE EARLIER MEM START IS FOR "DEPOSITS" ONLY.

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
PDP8--A		PARTS LIST		

DIMENSIONAL TOLERANCE
DIMENSIONS ARE MILLIMETERS / INCHES UNLESS OTHERWISE SPECIFIED

MILLIMETERS	INCHES	ANGLES
X.XX ±0.10	.XXX ±.005	±0° 30'
X.X ±0.5	.XX ±.02	
X ±1.	.X ±.1	

THIRD ANGLE PROJECTION
REMOVE BURRS AND BREAK SHARP CORNERS/SURFACE QUALITY ✓
MATERIAL —
FINISH —

DRN. M W Pate 7-30-75
CHK'D Tom Vaan 7-30-75
ENGR Jerry Hosler 8-8-75
PROJ. ENG. Jerry Hosler 8-8-75
PROD.T [illegible] 8-8-75

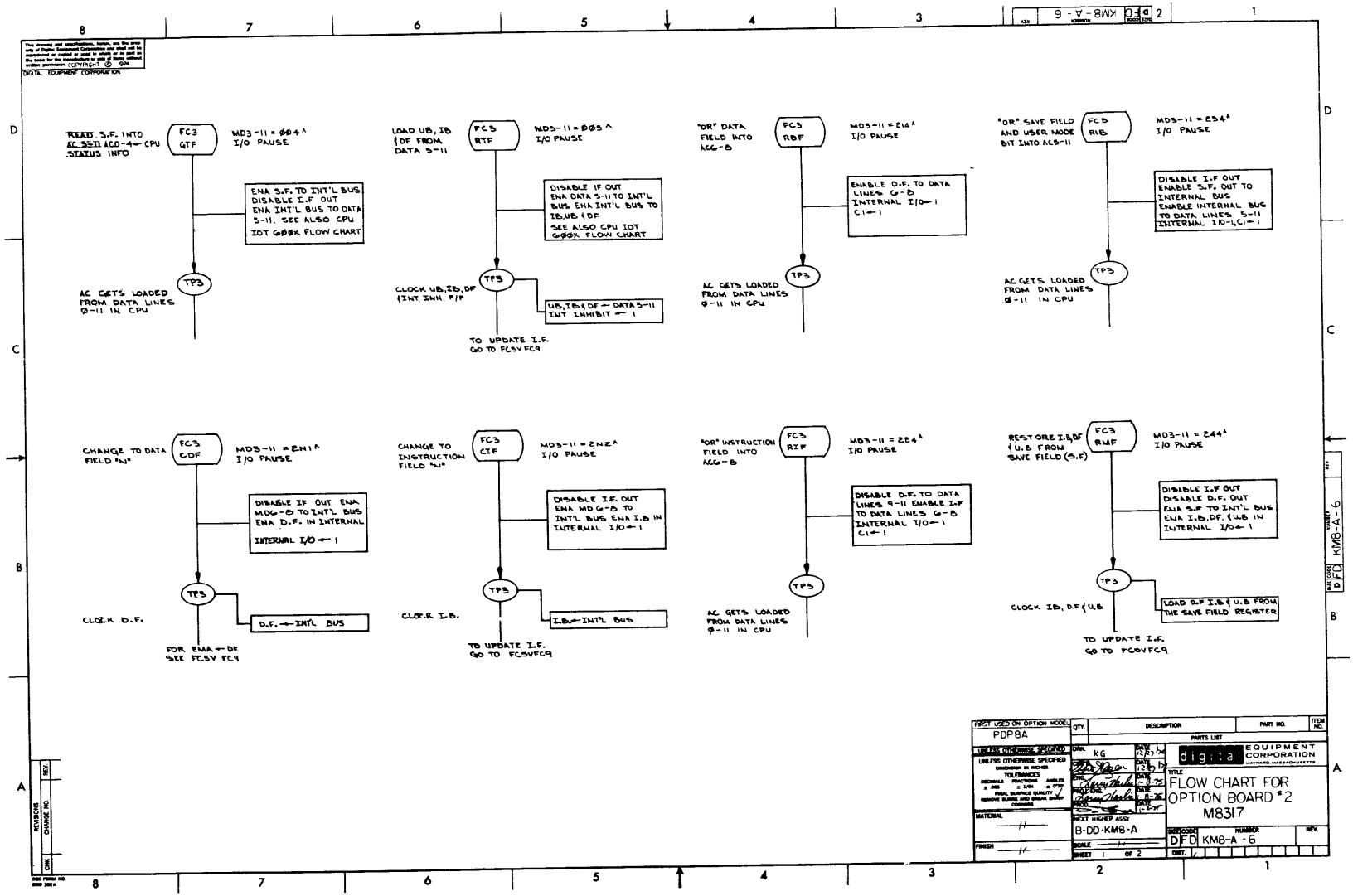
digital

TITLE: BOOTSTRAP TIMING DIAGRAM

NEXT HIGHER ASSY. B-DD-KM8-A
SCALE NONE
SIZE D | CODE TD | NUMBER KM8-A-5 | REV.
SHEET 1 OF 1 | DIST

REVISIONS	REV.	CHANGE NO.	CHK

D TD KM8-A-5


READ S.F. INTO AC 5-11 ACD-4← CPU STATUS INFO
FC3 GTF
MD3-11 = 0004^ I/O PAUSE
ENA S.F. TO INT'L BUS DISABLE I.F OUT ENA INT'L BUS TO DATA 5-11. SEE ALSO CPU IOT GGGX FLOW CHART
TP3
AC GETS LOADED FROM DATA LINES 0-11 IN CPU
LOAD UB, IB & DF FROM DATA 5-11
FC3 RTF
MD3-11 = 0005 ^ I/O PAUSE
DISABLE IF OUT ENA DATA 5-11 TO INT'L BUS ENA INT'L BUS TO IB, UB & DF SEE ALSO CPU IOT GGGX FLOW CHART
CLOCK UB, IB, DF & INT. INH. F/F
UB, IB & DF ← DATA 5-11 INT INHIBIT ← 1
TO UPDATE I.F. GO TO FC5VFC9
"OR" DATA FIELD INTO AC6-8
FC3 RDF
MD3-11 = 0014^ I/O PAUSE
ENABLE D.F. TO DATA LINES 6-8 INTERNAL I/O←1 C1←1
AC GETS LOADED FROM DATA LINES 0-11 IN CPU
"OR" SAVE FIELD AND USER MODE BIT INTO AC5-11
FC3 RIB
MD3-11 = 0024^ I/O PAUSE
DISABLE I.F OUT ENABLE S.F. OUT TO INTERNAL BUS ENABLE INTERNAL BUS TO DATA LINES 5-11 INTERNAL I/O←1, C1←1
AC GETS LOADED FROM DATA LINES 0-11 IN CPU
CHANGE TO DATA FIELD "N"
FC3 CDF
MD3-11 = 2N1^ I/O PAUSE
DISABLE IF OUT ENA MD6-8 TO INT'L BUS ENA D.F. IN INTERNAL INTERNAL I/O ← 1
CLOCK D.F.
D.F. → INT'L BUS
FOR ENA ← DF SEE FC5V FC9
CHANGE TO INSTRUCTION FIELD "N"
FC3 CIF
MD3-11 = 2N2^ I/O PAUSE
DISABLE I.F. OUT ENA MD 6-8 TO INT'L BUS ENA I.B IN INTERNAL I/O←1
CLOCK I.B.
I.B → INT'L BUS
TO UPDATE I.F. GO TO FC5VFC9
"OR" INSTRUCTION FIELD INTO AC6-8
FC3 RIF
MD3-11 = 2204^ I/O PAUSE
DISABLE D.F. TO DATA LINES 9-11 ENABLE I.F TO DATA LINES 6-8 INTERNAL I/O←1 C1←1
AC GETS LOADED FROM DATA LINES 0-11 IN CPU
RESTORE I.B, DF & U.B FROM SAVE FIELD (S.F)
FC3 RMF
MD3-11 = 2244^ I/O PAUSE
DISABLE I.F OUT DISABLE D.F. OUT ENA S.F TO INT'L BUS ENA I.B, DF, & UB IN INTERNAL I/O←1
CLOCK IB, DF & UB
LOAD D.F I.B & U.B FROM THE SAVE FIELD REGISTER
TO UPDATE I.F. GO TO FC5VFC9
FIRST USED ON OPTION MODEL: PDP8A
UNLESS OTHERWISE SPECIFIED
TOLERANCES
MATERIAL
FINISH
DRAWN K6 12/23/74
CHECKED 12/27/74
ENGR 1-6-75
PROJECT 1-6-75
MGR 1-6-75
NEXT HIGHER ASSY B-DD-KM8-A
SCALE
SHEET 1 OF 2
digital EQUIPMENT CORPORATION
TITLE FLOW CHART FOR OPTION BOARD #2 M8317
SIZE CODE D FD NUMBER KM8-A-6 REV.
DIST
REVISIONS REV. DWN CHANGE NO.
KM8-A-6

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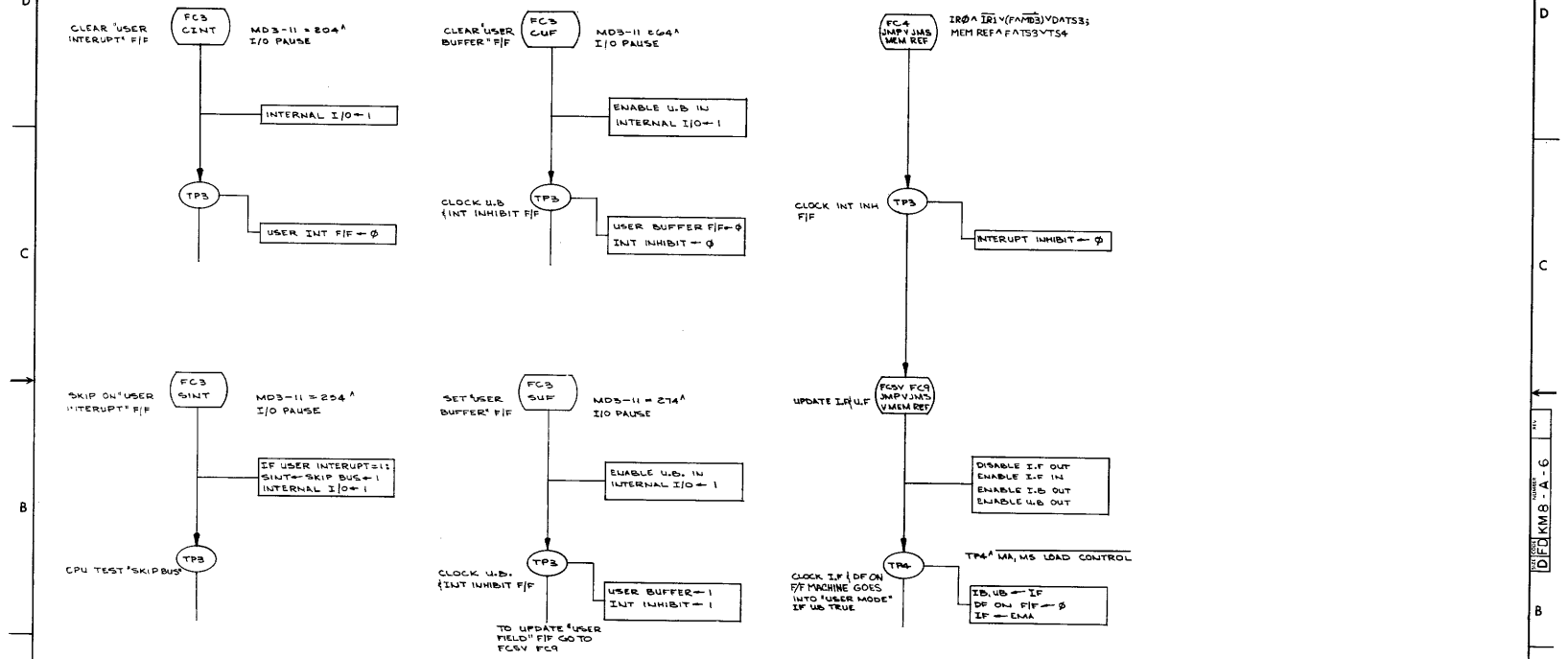
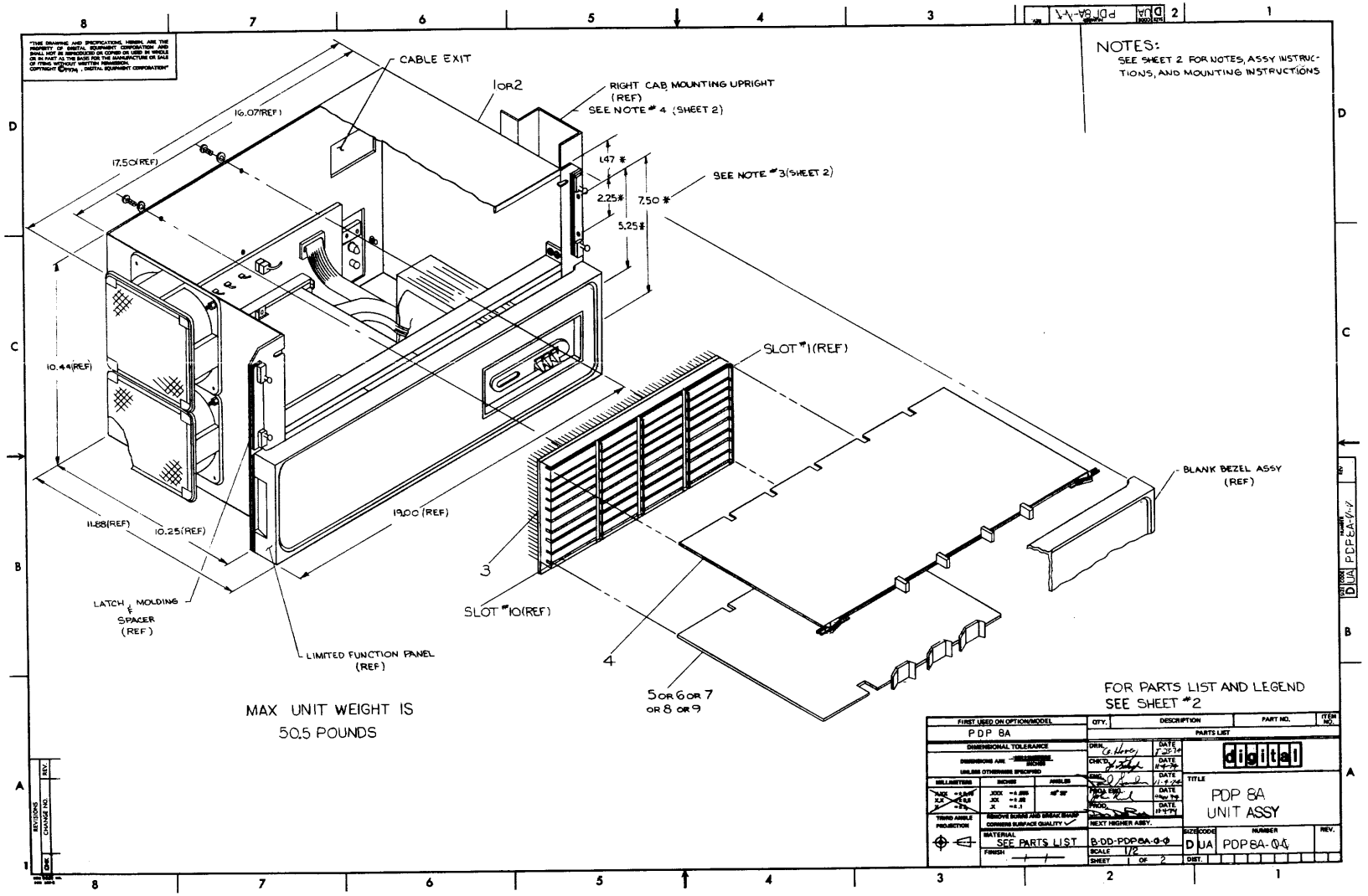


REVISIONS		
CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV.
FLOW CHART FOR OPTION BOARD #2 M8317	D	FD	KM8-A-6	
SCALE — SHEET 2 OF 2	DIST.			


CABLE EXIT
1 OR 2
RIGHT CAB MOUNTING UPRIGHT (REF)
SEE NOTE #4 (SHEET 2)
16.07(REF)
17.50(REF)
1.47 *
2.25*
7.50 *
5.25*
SEE NOTE #3(SHEET 2)
10.44(REF)
SLOT #1(REF)
BLANK BEZEL ASSY (REF)
11.88(REF)
10.25(REF)
19.00 (REF)
3
SLOT #10(REF)
LATCH & MOLDING SPACER (REF)
LIMITED FUNCTION PANEL (REF)
4
5 OR 6 OR 7 OR 8 OR 9
MAX UNIT WEIGHT IS 50.5 POUNDS
NOTES:
SEE SHEET 2 FOR NOTES, ASSY INSTRUCTIONS, AND MOUNTING INSTRUCTIONS
FOR PARTS LIST AND LEGEND SEE SHEET #2
PDP 8A
UNIT ASSY
digital
SEE PARTS LIST
B-DD-PDP8A-0-0
PDP8A-0-0
SCALE 1/2
SHEET 1 OF 2

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MODULE ASSIGNMENTS & POWER REQUIREMENTS

OPTION	DESCRIPTION	BOARD SIZE	NO. SLOTS USED	ASSIGNED SLOT NO.	CURRENT +5V	CURRENT +15V	CURRENT -15V
CM8-F	CARD RDR CONT.	QUAD	1	4-10	.55A	—	—
CR8-F	CARD RDR CONT.	↕	↕	4-10	.55A	—	—
DB8-EA	INTERPROC. BUFFER	↕	↕	2-10	.80A	—	.03A
DK8-EC	RTC, CRYSTAL	↕	1	2-10	.34A	—	—
DK8-EP	RTC, PROG.	QUAD	2	2-10	1.43A	—	.07A
DKC-AA	OPTION #1	HEX	1	2-3	2.0A	—	—
DP8-EA,-EB	MODEM INTERFACE	QUAD	2	2-10	1.80A	.05A	.11A
DR8-EA	DIGITAL I/O	QUAD	1	2-10	2.25A	—	—
KA8-E	POSITIVE I/O	QUAD	1	4-10	1.44A	—	—
KC8-AA,-AB	PROG. CONSOLE	PNL. MT.	0	N.A.	2.5A	—	—
KD8-E	DATA BREAK	QUAD	1	4-10	1.2A	—	—
KG8-EA	REDUNDANCY CHECK	QUAD	1	4-10	.94A	—	—
KK8-A	C.P.U.	HEX	1	1	5.0A	—	—
KL8-JA	ASYNC. DATA CONT	QUAD	1	2-10	1.1A	.05A	.10A
KL8-M	MODEM CONTROL	QUAD	1	2-10	.40A	.04A	.04A
KM8-A	OPTION #2	HEX	1	2-3	2.0A	—	—
LE8-XX	LINE PRINTER CONT.	QUAD	1	2-10	.35A	—	—
LS8-F	LINE PRINTER CONT.	↕	1	2-10	.40A	—	—
MR8-AA	1K ROM	↕	1	2-10	2.0A	—	—
MR8-AB	2K ROM	↕	1	2-10	↕	—	—
MR8-AC	3K ROM	↕	1	2-10	↕	—	—
MR8-AD	4K ROM	↕	1	2-10	5.0A	—	—
MR8-FB	1K PROM	↕	1	2-10	3.0A	↕	.35A
MS8-AA	1K RAM	↕	1	4-10	2.0A	—	—
MS8-AB	2K RAM	↕	1	4-10	↕	—	—
MS8-AC	3K RAM	↕	1	4-10	↕	—	—
MS8-AD	4K RAM	↕	1	4-10	3.2A	—	—
PC8-E, PR8-E	RDR/PUNCH CONTROL	↕	1	4-10	.84A	↕	.05A
RK8-EA	RK05 CONTROL	↕	3	4-10	3.10A	—	—
TA8-AA	TU60 CONTROL	↕	1	2-10	2.80A	—	—
TM8-EA,-FA	TU10 CONTROL	↕	4	4-10	4.18A	—	—
VC8-E	DISPLAY CONTROL	↕	2	2-10	.31A	—	—
VT8-E	DISPLAY CONTROL	↕	3	4-10	3.70A	.09A	.13A
XY8-E	PLOTTER CONTROL	QUAD	1	4-10	.42A	.01A	.03A

AVAILABLE PDP8A CURRENT = 20 AMPS OF +5V.
1 AMP OF +15V & -15V SHARED

FOR IN HOUSE USE ONLY

LEGEND

NUMBER	VARIATION
PDP8A-AA	115V, NO MEMORY
PDP8A-AB	230V, NO MEMORY
PDP8A-AC	115V, 1K RAM
PDP8A-AD	230V, 1K RAM
PDP8A-AE	115V, 2K RAM
PDP8A-AF	230V, 2K RAM
PDP8A-AH	115V, 3K RAM
PDP8A-AJ	230V, 3K RAM
PDP8A-AK	115V, 4K RAM
PDP8A-AL	230V, 4K RAM
PDP8A-FA	115V, 1K PROM
PDP8A-FB	230V, 1K PROM

ASSEMBLY INSTRUCTIONS

1. OPERATIONS TO BE PERFORMED PER HARDWARE STANDARDS (SP 7665099-0-0) AND/OR DEC WORKMANSHIP STANDARDS.
2. INSTALL THE CONNECTOR BLOCK ASSY. (ITEM #3) INTO THE POWER SUPPLY ASSY (ITEM #1 OR #2) WITH HARDWARE ATTACHED.
3. PLUG THE SIGNAL JUMPER, FROM J8 OF THE POWER BD, INTO J9 OF THE CONNECTOR BLOCK ASSY. (ITEM #3)
4. PLUG THE 12 AWG JUMPERS FROM THE POWER BD INTO THE CONNECTOR BLOCK ASSY 4 PLACES. -15V TO -15V, +15V TO +15V, +5V TO +5V AND GRD TO GRD.
5. INSTALL THE MODULES PER PARTS LIST VARIATIONS BELOW.

MOUNTING INSTRUCTIONS

1. REMOVE THE BLANK BEZEL ASSY.
2. REMOVE THE LIMITED FUNCTION PANEL AND DISCONNECT THE CABLE FROM THE LIMITED FUNCTION BD.
3. REMOVE THE LATCH MOLDING AND SPACERS 4 PLACES.
4. REMOVE THE SPEED NUT FROM THE CHASSIS AND INSTALL ON CABINET POST 8 PLACES PER MOUNTING DIMENSIONS ON SHEET #1.
5. IT MAY BE NECESSARY TO REMOVE THE FILTER RETAINER AND THE FILTER IN ORDER TO MOUNT THE BOX IN A CABINET.
6. WITH THE BOX IN PLACE, IN THE CABINET, REPLACE THE LATCH MOLDING AND SPACERS SO AS TO SECURE THE BOX TO THE CABINET.
7. PLUG THE CABLE INTO THE LIMITED FUNCTION BD AND REPLACE LIMITED FUNCTION PANEL.
8. REPLACE THE BLANK BEZEL ASSY
9. REINSTALL THE FILTER RETAINER AND THE FILTER.

NOTES:

1. ALL PDP8A POWER SUPPLY DC OUTPUTS ARE PROVIDED TO DRIVE LOGIC INTERNAL TO THE BASIC MACHINE ENCLOSURE. DIGITAL WILL NOT BE RESPONSIBLE FOR THE PERFORMANCE OF THE PDP8A IF ANY D.C. POWER IS TAKEN OUTSIDE THE MACHINE.
2. ENVIRONMENTAL CONDITIONS FOR PDP8A ARE SPECIFIED IN DEC STD 102 CLASS "C" ENVIRONMENT.
3. ASTERIK(*) DENOTES MTG DIM
4. THE DIM FROM CENTER LINE OF RIGHT CAB UPRIGHT MOUNTING HOLE TO LEFT CAB UPRIGHT MOUNTING HOLE CENTER LINE IS 18.31
5. FOR VOLTAGE AND FREQUENCY CONVERSION SEE DEC DRAWING E-UA-H763-0-0

PDP8A-FB	PDP8A-FA	PDP8A-AL	PDP8A-AK	PDP8A-AJ	PDP8A-AH	PDP8A-AF	PDP8A-AE	PDP8A-AD	PDP8A-AC	PDP8A-AB	PDP8A-AA	DESCRIPTION	PART NO.	ITEM NO.
QTY	QTY	QTY	QTY	QTY	QTY	QTY	QTY	QTY	QTY	QTY	QTY			
0.9	0.9	0.9	0.9	0.9	0.5	0.9	0.9	0.9	0.9	0.9	0.9	PACKAGING INSTRUCTIONS CUSHIONED CARTON	A-SP-3700172-0-0	12
1	1	1	1	1	1	1	1	1	1	1	1	PACKAGING INSTRUCTIONS INNER CARTON	A-SP-3700170-0-0	11
1	1	1	1	1	1	1	1	1	1	0	0	SHIPPING LIST	A-PL-PDP8A-0-2	10
1	1	0	0	0	0	0	0	0	0	0	0	1K PROM, MB349	A-PL-MR8-FB-0	9
0	0	1	1	0	0	0	0	0	0	0	0	4K RAM, MB311-YD	A-PL-MS8-AD-0	8
0	0	0	0	1	1	0	0	0	0	0	0	3K RAM, MB311-YC	A-PL-MS8-AC-0	7
0	0	0	0	0	0	1	1	0	0	0	0	2K RAM, MB311-YB	A-PL-MS8-AB-0	6
0	0	0	0	0	0	0	0	1	1	0	0	1K RAM, MB311-YA	A-PL-MS8-AA-0	5
1	1	1	1	1	1	1	1	1	1	1	1	CPU, MB315	A-PL-KK8-A-0	4
1	1	1	1	1	1	1	1	1	1	1	1	CONNECTOR BLOCK ASSY	D-CS-H9192-0-1	3
1	0	1	0	1	0	1	0	1	0	1	0	POWER SUPPLY ASSY 230V	D-UA-H763-B-0	2
0	1	0	1	0	1	0	1	0	1	0	1	POWER SUPPLY ASSY 115V	D-UA-H763-A-0	1

REVISIONS		
CHK	CHANGE NO	REV

TITLE: PDP8A UNIT ASSY
SIZE: D | CODE: UA | NUMBER: PDP8A-0-0 | REV:
SCALE: — | SHEET 2 OF 2 | DIST:

DEC FORM NO. SMD 121

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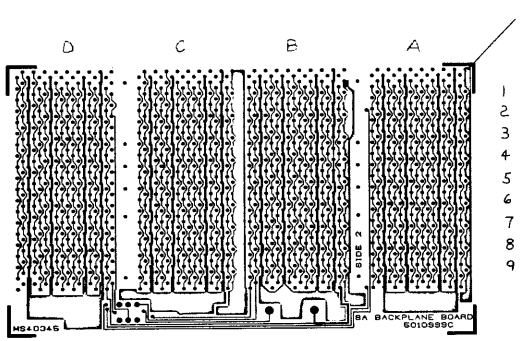
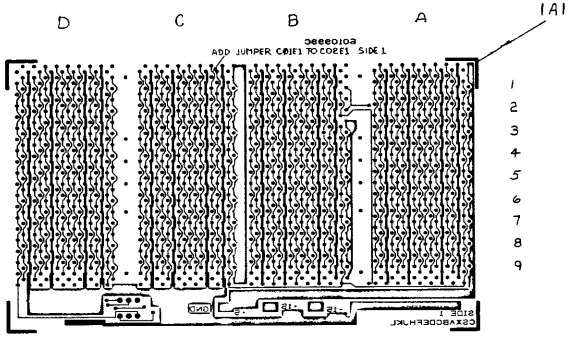
NOTES:



SOLDER SIDE
(SIDE 2)



BLOCK SIDE
(SIDE #1)
AS SEEN THRU SIDE #2

IC TYPE	GND	+5V

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

REF				
REF		X-Y COORDINATE HOLE LOCATION	K-CO-H9192-0-4	1
REF		ASSY/DRILLING HOLE LAYOUT	D-AH-H9192-0-5	2
REF		MODULE ECO HISTORY	B-MH-H9192-0-6	3
REF		ETCHED CIRCUIT BOARD	5010999	4
REF		CONN BLOCK ASSY	D-AD-H9192-0-0	5
1	1.0"	WIRE, KYNAR #30 AWG	9105740	6

QTY	REF. DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

FIRST USED ON OPTION MODEL: PDP8A

ETCH BOARD REV. C

ORIGINATED: DRWG NO. REV.

CHK REVISIONS

DEC NO.	EIA NO.	DEC NO.	EIA NO.

SEMICONDUCTOR CONVERSION CHART

DRN E. Wilson 7/31/74
CHK [illegible] 7/31/74
ENG [illegible] 11/1/74
PROJ ENG. [illegible] 11/5/74
PROD. [illegible] 11/21/74

NEXT HIGHER ASSY D-AD-H9192-0

SCALE NONE

SHEET 1 OF 2

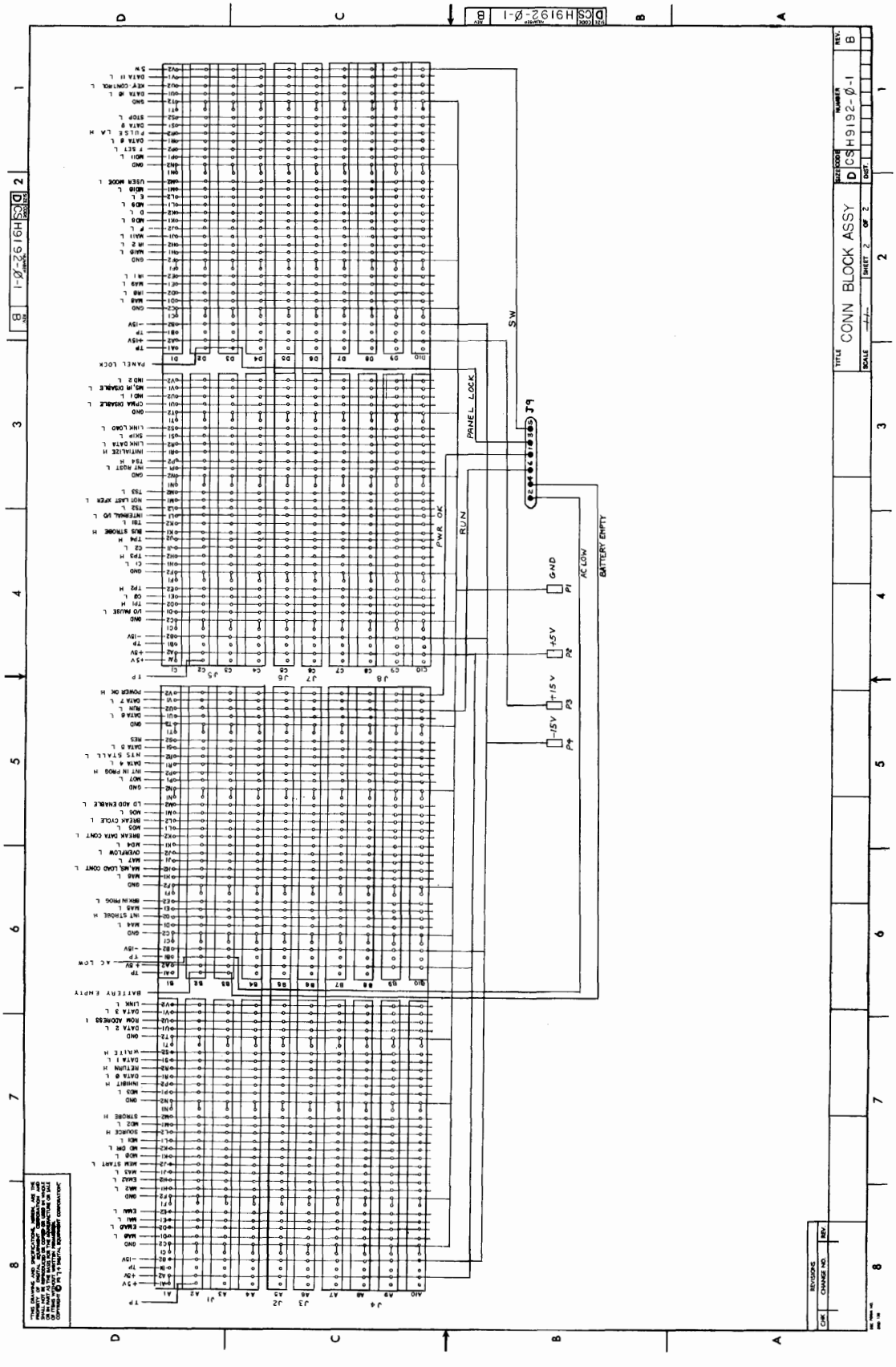
digital

TITLE: CONN BLOCK ASSY

SIZE D | CODE CS | NUMBER H9192-0-1 | REV. B

DIST.

REV B 1-0-2616H SO a


CONN BLOCK ASSY
DCSH9192-Ø-1
B
SIZE
D
CODE
CS
SHEET 2 OF 2
SCALE
REVISIONS
CHK
CHANGE NO.
REV
PANEL LOCK
S.W
RUN
PWR OK
BATTERY EMPTY
AC LOW
GND
+5V
-15V
+15V
-15V
P1
P2
P3
P4
J9
J1
J2
J3
J4
J5
J6
J7
J8

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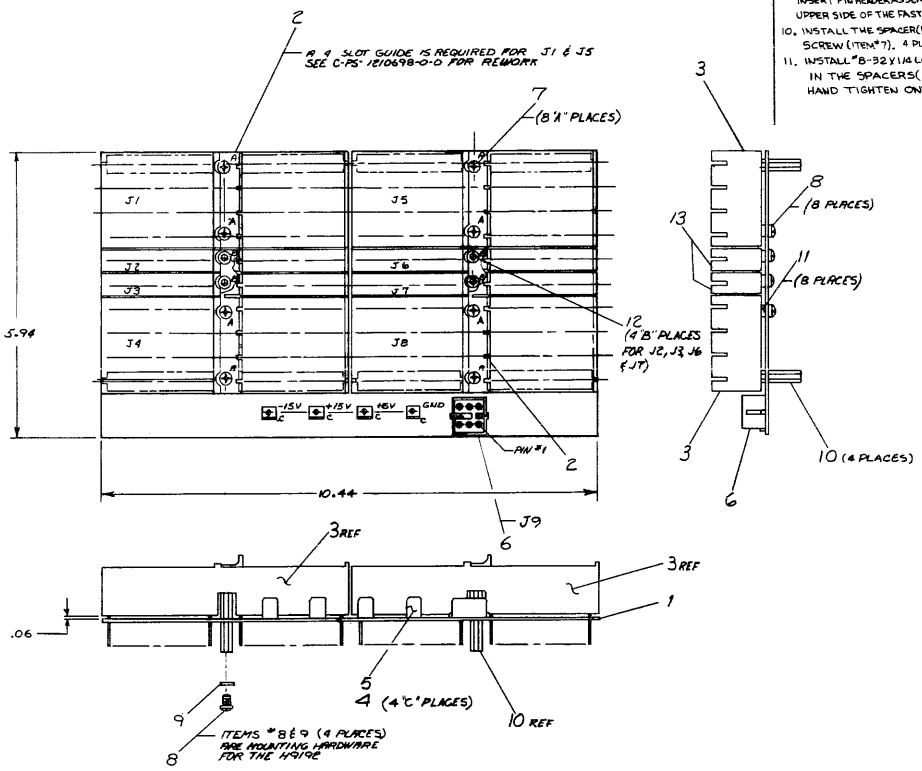


9. TOUCH UP PER ENG SPEC SP-7665510-0-0. HAND INSERT PIN HEADER ASSEMBLY (ITEM "6) AND SOLDER UPPER SIDE OF THE FAST ON TABS (ITEM "4) 4 'C' PLACES.
10. INSTALL THE SPACER (ITEM "10) USING SELF TAPPING SCREW (ITEM "7). 4 PLACES
11. INSTALL "8-32 X 1/4 LG SCREW AND "8 L' WASHER IN THE SPACERS (ITEM "10) 4 PLACES. HAND TIGHTEN ONLY

NOTES: ASSEMBLY INSTRUCTIONS

1. OPERATIONS TO BE PERFORMED PER HARD-WARE STANDARD SP-7665099-0 AND/OR DEC WORKMANSHIP STANDARD.
2. ATTACH THE FAST ON TABS (ITEM "4) TO THE ETCH CIRCUIT BOARD (ITEM "1) WITH THE EYELETS (ITEM "5) 4 'C' PLACES.
3. ATTACH THE SPACERS (ITEM "11) TO THE CONNECTOR BLOCKS (ITEM "13) WITH THE "8-32 X 1/2 LG. SOCKET HD SCREWS (ITEM "12) 4 'B' PLACES.
4. REWORK THE CARD GUIDES (ITEM "2) FOR J1 AND J5 BY CUTTING PER C-PS-1210698-0-0
5. ATTACH THE CARD GUIDES (ITEM "2) TO THE CONNECTOR BLOCKS (ITEM "3) USING ONE (1) SELF TAPPING SCREW (ITEM "7) AND ONE (1) SPACER (ITEM "11) PER CONNECTOR BLOCK AS SHOWN ON DRAWING. DO NOT INSTALL SPACER (ITEM "10) AT THIS TIME.
6. ATTACH THE CONNECTOR BLOCKS (ITEM "3 AND "13) TO THE ETCH CIRCUIT BD (ITEM "1) WITH "8-32 X 1/4 LG SCREW (ITEM "8).
7. FLOW SOLDER ASSEMBLY PER SP-7665159-0-0
8. DEGREASE

REF	OMNIBUS SPEC.		18
REF	MODULE HISTORY ECO	B-MH-H9192-0-0	17
REF	ASSY/DRILLING HOLE LAYOUT	D-AH-H9192-0-0	16
REF	X-Y COORDINATE HOLE LOCATION	K-CO-H9192-0-0	15
REF	CIRCUIT SCHEMATIC	D-CS-H9192-0-0	14
4	CONN BLOCK (72 PIN)	1211425	13
4	SCR, SOC HD CAP "8-32 X 1.50	9006338-08	12
8	SPACER "8-32 X .25 AF X .36 LG	9009602	11
4	SPACER "8-32 X .25 AF X 1.25 LG	9009603	10
4	WASHER, INT TOOTH LOCK "8	9006631	9
12	SCR, PHL PAN HD "8-32 X .25 LG	9006035-01	8
8	SCR, SELF TAPPING "8-32 X .81	9009070-00	7
1	PIN HEADER ASSY, 6 CKT	1211392-06	6
4	EYELET	9009000	5
4	FAST ON TAB	9008219	4
4	CONNECTOR BLOCK (100 PIN)	1210258	3
4	GUIDE CARD CENTER	1210698	2
1	ETCHED CIRCUIT BOARD	5040999	1
QTY.	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

FIRST USED ON OPTION/MODEL: PDP8A

DIMENSIONAL TOLERANCE
DIMENSIONS ARE INCHES
UNLESS OTHERWISE SPECIFIED

FRACTIONS	INCHES	ANGLES
X.XX ±.01	.XXX ±.005	±0° 30'
X.X ±.03	.XX ±.01	
X ±.1	.X ±.1	

THIRD ANGLE PROJECTION

REMOVE BURRS AND BREAK SHARP CORNERS
SURFACE QUALITY

MATERIAL
FINISH

DRN: R. Nichols DATE 8-8-78
DES: [illegible] DATE 10-21-78
CH: [illegible] DATE 10-21-78
ENGR: [illegible] DATE 10-21-78
PROD: [illegible] DATE 10-21-78
QA: [illegible] DATE 10-21-78

NEXT HIGHER ASSY. B-DD-H9192-0

SCALE 1/1
SHEET 1 OF 1

digital

TITLE: CONN BLOCK ASSY

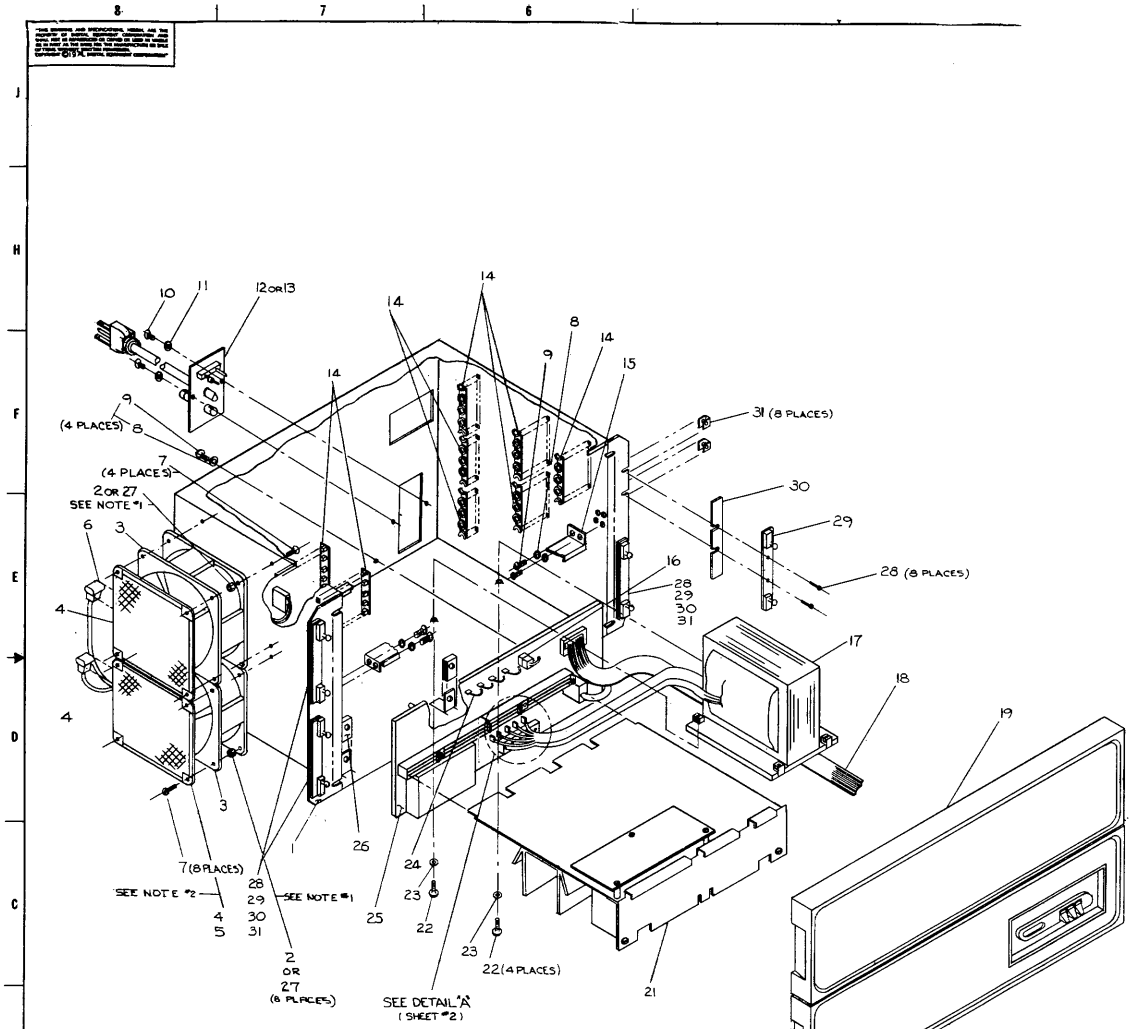
SIZE D | CODE AD | NUMBER H9192-0 -0 | REV.

DIST.

DAD H9192-0-0

REVISIONS

REV.	CHANGE NO.	CHK



NUMBER	VARIATION
H763-A	115V (SEE PARTS LIST)
H763-B	230VOLT (SEE PARTS LIST)

NOTES:

1. MOUNTING HARDWARE VARIATIONS FOR FAN (ITEM #3) ARE AS FOLLOWS

FAN (ITEM #3)	MOUNTING HARDWARE ITEM NO.	DESCRIPTION
IMC	7	SCR FLAT HD #6-32 X 5/8 LG
	27	MOUNTING CLIP
ROTRON	7	SCR FLAT HD #6-32 X 5/8 LG
	2	NUT, KEP #6-32

2. ATTACH FILTER RETAINER SO THAT FILTER CAN BE INSERTED FROM REAR OF BOX.
3. SEE SHEET #2 FOR ASSY INSTRUCTIONS.

8	8	NUT, SPEED #10-32	9007786	31
4	4	SPACER	BMD-1407789-0-0	30
4	4	LATCH MOLDING	12.09224	29
8	8	SCR PH, FLAT HD #10-32 X 3/4	9006075-2	28
12	12	MOUNTING CLIP	9009165	27
2	2	RECEPTACLE 1/4 TURN	9003896	26
1	1	POWER SW	DCS-5407568-01	25
4	4	JUMPER, #12 AWG	B-1A-7000044-0-0	24
4	4	WASHER, LOCK INT TOOTH #10	9006635	23
4	4	SCR PH, PAN HD #10-32 X 1/2 LG	9006073-1	22
1	1	REGULATOR BD ASSY	D-C3-68076-0-1	21
1	1	PANEL, LIMITED FUNCTION	D-AD-7000119-0-0	20
1	1	BLANK, BEZEL, ASSY	D-AD-7009718-0-0	19
1	1	CABLE, KEYBOARD (18")	C-1A-7006612-1F	18
1	1	X-FMR ASSY	D-1A-7000040-0-0	17
1	1	JUMPER, SIGNAL	C-1A-7000043-0-0	16
1	1	BRACKET, MODULE SUPPORT	C-MD-7412100-0-0	15
8	8	CARD GUIDE	12.11630-0-0	14
1	—	LINE SET ASSY (230V)	D-AD-7010041-02-0	13
—	1	LINE SET ASSY (115V)	D-AD-7010041-01-0	12
2	2	WASHER, LOCK EXT TOOTH #6	9007649	11
2	2	SCR PH, PAN HD #6-32 X 1/4 LG	9006020-1	10
8	8	SCR PH, PAN HD #8-32 X 1/4 LG	9006035-1	9
8	8	WASHER, LOCK INT TOOTH #8	9006634	8
12	12	SCR PH, FLAT HD #6-32 X 3/8 LG	9006025-2	7
1	1	HARNESS, FAN	D-1A-7007755-0-0	6
2	2	FILTER	12.12106	5
2	2	RETAINER, FILTER	12.12059	4
2	2	FAN	12.09403-01	3
20	20	NUT, KEP #6-32	9006360	2
1	1	CHASSIS	E-1A-7007754-0-0	1

H763-B	H763-A	QTY.	QTY.	DESCRIPTION	PART NO.	ITEM NO.

FIRST USED ON OPTION/MODEL: PDP 8A

PARTS LIST

DIMENSIONAL TOLERANCE UNLESS OTHERWISE SPECIFIED

DRN G. Henry 6/8/76
CHK [illegible] 6/8/76
QUAL [illegible] 6/8/76
PROJ ENG [illegible] 6/8/76
MFG ENG [illegible] 6/8/76
NEXT HIGHER ASSY

digital

TITLE: POWER SUPPLY ASSY

MATERIAL: SEE PARTS LIST
FINISH

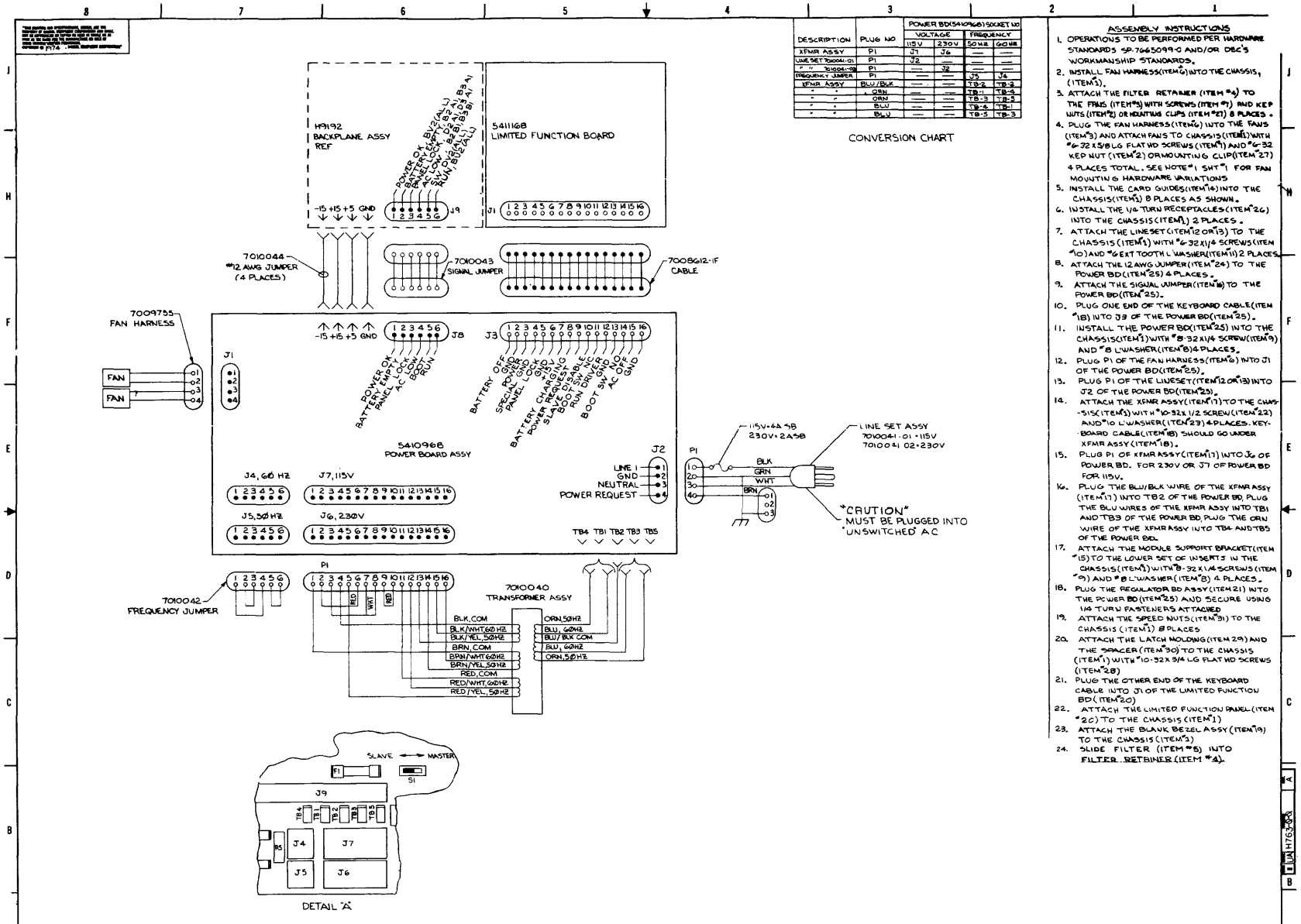
D-UA-PDP8A-E-0

SIZE E | CODE UA | NUMBER H763-0-0 | REV A

SCALE 1/2
SHEET 1 OF 2

DIST

UA H763-0-0 A



DESCRIPTION	PLUG NO	POWER BD(5410968) SOCKET NO			
		VOLTAGE		FREQUENCY	
		115V	230V	50 HZ	60 HZ
XFMR ASSY	P1	J1	J6	—	—
LINE SET 7010041-01	P1	J2	—	—	—
" " 7010041-02	P1	—	J2	—	—
FREQUENCY JUMPER	P1	—	—	J5	J4
XFMR ASSY	BLU/BLK	—	—	TB-2	TB-3
" "	ORN	—	—	TB-1	TB-4
" "	ORN	—	—	TB-3	TB-5
" "	BLU	—	—	TB-4	TB-1
" "	BLU	—	—	TB-5	TB-3

CONVERSION CHART

ASSEMBLY INSTRUCTIONS

1. OPERATIONS TO BE PERFORMED PER HARDWARE STANDARDS SP-7665099-0 AND/OR DEC'S WORKMANSHIP STANDARDS.
2. INSTALL FAN HARNESS(ITEM"6) INTO THE CHASSIS, (ITEM"1).
3. ATTACH THE FILTER RETAINER (ITEM"4) TO THE FANS (ITEM"3) WITH SCREWS (ITEM"7) AND KEP NUTS (ITEM"2) OR MOUNTING CLIPS (ITEM"27) 8 PLACES.
4. PLUG THE FAN HARNESS (ITEM"6) INTO THE FANS (ITEM"3) AND ATTACH FANS TO CHASSIS (ITEM"1) WITH "6-32 X 5/8 LG FLAT HD SCREWS (ITEM"7) AND "6-32 KEP NUT (ITEM"2) OR MOUNTING CLIP (ITEM"27) 4 PLACES TOTAL. SEE NOTE"1 SHT"1 FOR FAN MOUNTING HARDWARE VARIATIONS
5. INSTALL THE CARD GUIDES (ITEM"14) INTO THE CHASSIS (ITEM"1) 8 PLACES AS SHOWN.
6. INSTALL THE 1/4 TURN RECEPTACLES (ITEM"26) INTO THE CHASSIS (ITEM"1) 2 PLACES.
7. ATTACH THE LINESET (ITEM"12 OR"13) TO THE CHASSIS (ITEM"1) WITH "6-32 X 1/4 SCREWS (ITEM"10) AND "6 EXT TOOTH L WASHER (ITEM"11) 2 PLACES.
8. ATTACH THE 12 AWG JUMPER (ITEM"24) TO THE POWER BD (ITEM"25) 4 PLACES.
9. ATTACH THE SIGNAL JUMPER (ITEM"18) TO THE POWER BD (ITEM"25).
10. PLUG ONE END OF THE KEYBOARD CABLE (ITEM"18) INTO J3 OF THE POWER BD (ITEM"25).
11. INSTALL THE POWER BD (ITEM"25) INTO THE CHASSIS (ITEM"1) WITH "8-32 X 1/4 SCREW (ITEM"9) AND "8 L WASHER (ITEM"8) 4 PLACES.
12. PLUG P1 OF THE FAN HARNESS (ITEM"6) INTO J1 OF THE POWER BD (ITEM"25).
13. PLUG P1 OF THE LINESET (ITEM"12 OR"13) INTO J2 OF THE POWER BD (ITEM"25).
14. ATTACH THE XFMR ASSY (ITEM"17) TO THE CHASSIS (ITEM"1) WITH "10-32 X 1/2 SCREW (ITEM"22) AND "10 L WASHER (ITEM"23) 4 PLACES. KEYBOARD CABLE (ITEM"18) SHOULD GO UNDER XFMR ASSY (ITEM"18).
15. PLUG P1 OF XFMR ASSY (ITEM"17) INTO J6 OF POWER BD. FOR 230V OR J7 OF POWER BD FOR 115V.
16. PLUG THE BLU/BLK WIRE OF THE XFMR ASSY (ITEM"17) INTO TB2 OF THE POWER BD, PLUG THE BLU WIRES OF THE XFMR ASSY INTO TB1 AND TB3 OF THE POWER BD, PLUG THE ORN WIRE OF THE XFMR ASSY INTO TB4 AND TB5 OF THE POWER BD.
17. ATTACH THE MODULE SUPPORT BRACKET (ITEM"15) TO THE LOWER SET OF INSERTS IN THE CHASSIS (ITEM"1) WITH "8-32 X 1/4 SCREWS (ITEM"9) AND "8 L WASHER (ITEM"8) 4 PLACES.
18. PLUG THE REGULATOR BD ASSY (ITEM 21) INTO THE POWER BD (ITEM"25) AND SECURE USING 1/4 TURN FASTENERS ATTACHED.
19. ATTACH THE SPEED NUTS (ITEM"31) TO THE CHASSIS (ITEM"1) 8 PLACES
20. ATTACH THE LATCH MOLDING (ITEM 29) AND THE SPACER (ITEM"30) TO THE CHASSIS (ITEM"1) WITH "10-32 X 3/4 LG FLAT HD SCREWS (ITEM"28)
21. PLUG THE OTHER END OF THE KEYBOARD CABLE INTO J1 OF THE LIMITED FUNCTION BD (ITEM"20)
22. ATTACH THE LIMITED FUNCTION PANEL (ITEM"20) TO THE CHASSIS (ITEM"1)
23. ATTACH THE BLANK BEZEL ASSY (ITEM"19) TO THE CHASSIS (ITEM"1)
24. SLIDE FILTER (ITEM"5) INTO FILTER RETAINER (ITEM"4).

REVISIONS		
CHR	CHANGE NO.	REV.
V. Wong 7-24-78		
V. Wong 10-17-78		

TITLE	SIZE/CODE	NUMBER	REV.
POWER SUPPLY ASSY	E U4	H763-G-G	A
SCALE —	SHEET 2 OF 2	DIST	

MADE IN U.S.A.

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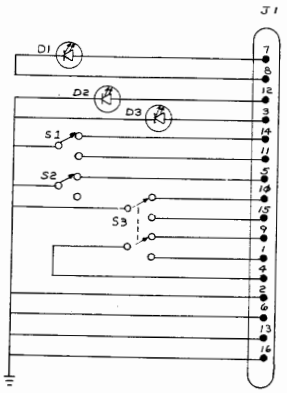
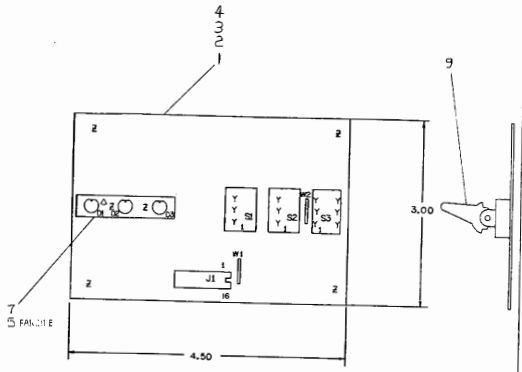
NOTES:





REF				
REF		XY COORDINATION HOLE LOCATION	K-CO-5411168-0-1	1
REF		ASSY/DRILLING HOLE LAYOUT	D-AH-5411168-0-1	2
REF		MODULE ECO HISTORY	B-MH-5411168-0-1	3
1		ETCHED CIRCUIT BOARD	5011167	4
2		SCR, SELF TAPPING, #6-32 X 1/4	9008230-01	5
1	S3	SWITCH, TOGGLE DPDT	1212010	6
1		LED HOLDER, TRIPLE	1210940-01	7
2	S1, S2	SWITCH, TOGGLE SPDT	1210840-00	8
3		KNOB, DARK GRAY (#47)	1210786-01	9
1	J1	SOCKET, IC., 16 POSITION	1211813 -02	10
3	D1, D2, D3	DIODE, LIGHT-EMITTING	1110324 -00	11
2	W1, W2	JUMPER, INSULATED	9009185	12

QTY	REF. DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

IC TYPE	GND	+5V
GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE		

IC PIN LOCATIONS

DEC NO.	EIA NO.	DEC NO.	EIA NO.

SEMICONDUCTOR CONVERSION CHART

REV.	CHANGE NO.	CHK	REVISIONS
A	ORIGINATED		

J. Gardner 6/4/74
P. GARDNER 6-3-74
J. Burgess 6-3-74
5411168-0001
5411168-0-1

FIRST USED ON OPTION MODEL: H763

ETCH BOARD REV. A

DRN. Erikson	DATE 5/21/74	
CHK'D P. Gaynard	DATE 5-29-74	
ENG.	DATE 6-6-74	
MANUFG.	DATE 6-6-74	
QUAL. ENG.	DATE 6-6-74	
APPD.	DATE 7-6-74	

NEXT HIGHER ASSY: D-AD-7010039-0-0

SCALE: NONE

SHEET 1 OF 1

digital

TITLE: LIMITED FUNCTION BOARD

SIZE	CODE	NUMBER	REV.
D	CS	5411168-0-1	A

DIST.

SUB PROD D CS 5411168-0-1 REV A

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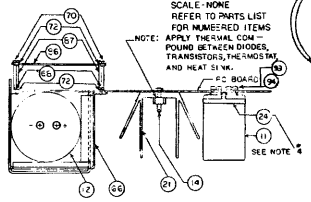
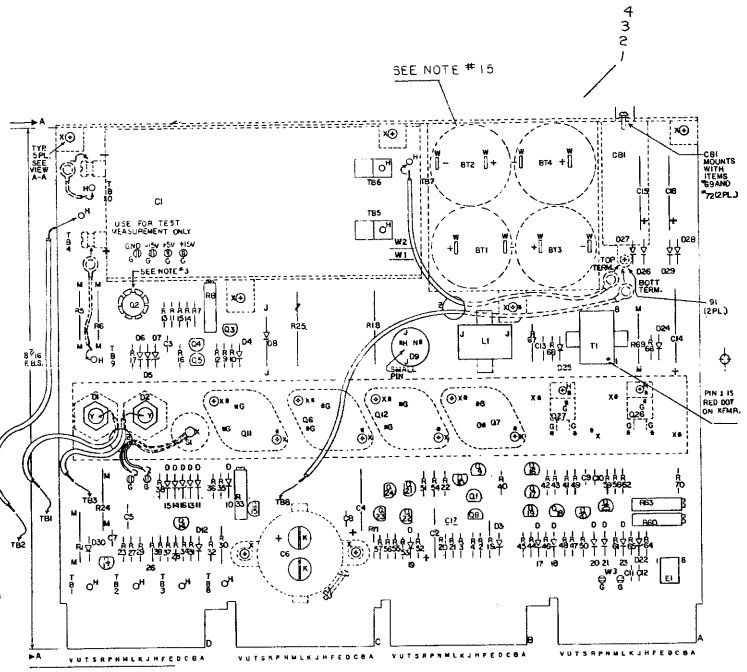
NOTES:

1. TRANSISTOR DEC 2N5302, 1510196 MAY BE USED AS A SECOND SOURCE FOR ITEM # 62 TRANSISTOR DEC D44H8 15111654.
2. ALL COMPONENTS SHOWN BY A BROKEN LINE MOUNT ON SIDE 2.
3. TRANSISTOR PAD MOUNTS UNDER Q2, AND HEAT SINK MOUNTS ON Q2. REFER TO PARTS LIST, ITEM #25 AND #77.
4. ITEM #24 BRKT IS MOUNTED ON BOARD WITH ITEM #68, 73, AND #81 (2 PL).
5. Q6, Q7, Q11, AND Q12 ARE MOUNTED WITH ITEM #73, 78 AND #81 (8 PL).
6. S1 MOUNTS WITH ITEM #73 AND #81 (1 PLACE).
7. Q26 AND Q27 ARE MOUNTED WITH ITEM #67, #71 AND #74 (2 PLACES).
9. PINSCAL IS MADE IN REVERSE, SIDE 1 IS LIGHT, SIDE 2 IS DARK.
10. INSERT JUMPER W3 FOR 220V OPERATION.
11. JUMPERS W1, W2 SHOULD BE INSTALLED AFTER TEST.
12. D1 & D2, TORQUE TO 20 LB-IN.
13. S1, Q26, & Q27 TORQUE TO 10 LB-IN
14. Q4, 7, 11, & 12 TORQUE TO 14 LB-IN
15. FOR HANDLING AND SOLDERING REQUIREMENTS OF 12116.70 LEAD ACID BATTERIES (ITEM #13) SEE A-SP-7665252-0-0





REF				
REF		X-Y COORDINATE HOLE LOCATION	K-CO-G8Ø16-Ø-4	1
REF		ASSY/DRILLING HOLE LAYOUT	D-AH-G8Ø16-Ø-5	2
REF		MODULE ECO HISTORY	B-MH-G8Ø16-Ø-6	3
1		ETCHED CIRCUIT BOARD	D-TA-SXD984-0-0	4
2	C5,C13	CAP .1 UF 100V 20% DISC	1000030	5
1	C4	CAP 180 UF 6V 20% STANT	1000086	6
5	C3,C9,C10,C11,C12	CAP .01 UF 100V 20% DISC	1001610-01	7
3	C14,C15,C16	CAP 100 UF 25V -10% + 75% ELECT	1002781	8
1	C2	CAP 22 UF 6V 10% STANT	1005636	9
2	C7,C8	CAP .22 UF 50V -20% + 80% CER	1010274-00	10
1	C6	CAP 6000 UF 10V -10% + 75% ELECT	1010704	11
1	C1	CAP .1F 10V	1011578	12
7	D5,D6,D11,D12,D13,D14,D15	DIODE D882	1100113	13
2	D1,D2	DIODE IN1183	1111609	14
10	D10,D17,D18,D19,D20,D21, D23,D24,D25,D30	DIODE D872	1105275	15
5	D4,D26,D27,D28,D29	DIODE IN4004	1105798	16
1	D8	DIODE WR752	1110615	17
2	D7,D22	DIODE IN751A ZENER	1110994	18
2	D3,D16	DIODE SCREENED 5.7V 2% ZENER	1111205	19
1	S1	THERMOSTAT	1211682	20
1		HEAT SINK	12-FIB14	21
1	CB1	CIRCUIT BREAKER 25A	1211673	22
4	BT1,BT2,BT3,BT4	BATTERIES D-CELL	1211070	23
1		BRACKET	1210428	24
1		HEAT SINK T-05 TRANSISTOR MOUNTED	1211543	25
3	R5,R6,R69	RES 10 1W 5%	1300171	26
2	R29,R42	RES. 47 1/4W 5%	1300202	27
1	R1	RES. 100 1W 5%	1300232	28
7	R71,R4,R22,R28,R38,R50,R57,	RES. 100 1/4W 5%	1300228	29
2	R12,R47	RES. 120 1/4W 5%	1300247	30
2	R27,R43	RES. 150 1/4W 5%	1300250	31
4	R10,R17,R28,R54	RES. 220 1/4W 5%	1300271	32
5	R3,R15,R37,R64, R36	RES. 330 1/4W 5%	1300295	33
13	R11,R13,R20,R21,R35, R40,R41,R48,R52,R55,R66, R68,R70	RES. 1K 1/4W 5%	1300365	34
2	R14,R56	RES. 1.5K 1/4W 5%	1300391	35
6	R23,R44,R45,R46,R51,R65	RES. 3.3K 1/4W 5%	1300439	36
1	R38	RES. 10 1/4W 5%	1301317	37
1	R49	RES. 180 1/4W 5%	1301322	38
1	R2	RES. 82 1/4W 5%	1301477	39
1	R19	RES. 56 1/4W 5%	1301602	40
2	R16,R62	RES. 511 1/4W 1% MF	1302411	41
1	R24	RES. 56 2W 5%	1302838	42
1	R34	RES. 100 1/8W 1% MF	1302858	43
1	R7	RES. 1.21K 1/8W 1% MF	1302871	44
1	R31	RES. 196 1/4W 1% MF	1302956	45
1	R59	RES. 464 1/4W 1% MF	1303047	46
2	R18,R25	RES. 1 5W 10% WW	1303385	47
1	R32	RES. 1.96K 1/4W 1% ME	1304833	48
2	R9,R61	RES. 383 1/4W 1% MF	1305125	49
1	R53	RES. 27K 1/4W 5%	1305346	50
3	R8,R33,R60	RES. 100 3/4W 10% POT 76 PR	1309143-04	51
1	R63	RES. 5K 3/4W 10% POT 76 PR	1309143-09	52
QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.

72741	4	7
IC TYPE	GND	+5V

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

REV	CHANGE NO	REVISIONS	CHK	DATE
C	G8Ø14-ØØØØ1	ORIG RELEASED	A.DELUCA	10-27-76

FIRST USED ON OPTION MODEL: PDP8A

ETCH BOARD REV: E

NEXT HIGHER ASSY: B-DD-PDP8A-Ø

SCALE:

SHEET 1 OF 3

DEC NO. / EIA NO. / DEC NO. / EIA NO.

SEMICONDUCTOR CONVERSION CHART

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE: H763 REGULATOR BOARD

SIZE: D | CODE | NUMBER: DCSG8Ø16-Ø-1 | REV: E

DIST:

DCSG8Ø16-Ø-1 E

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WIRE TABLE

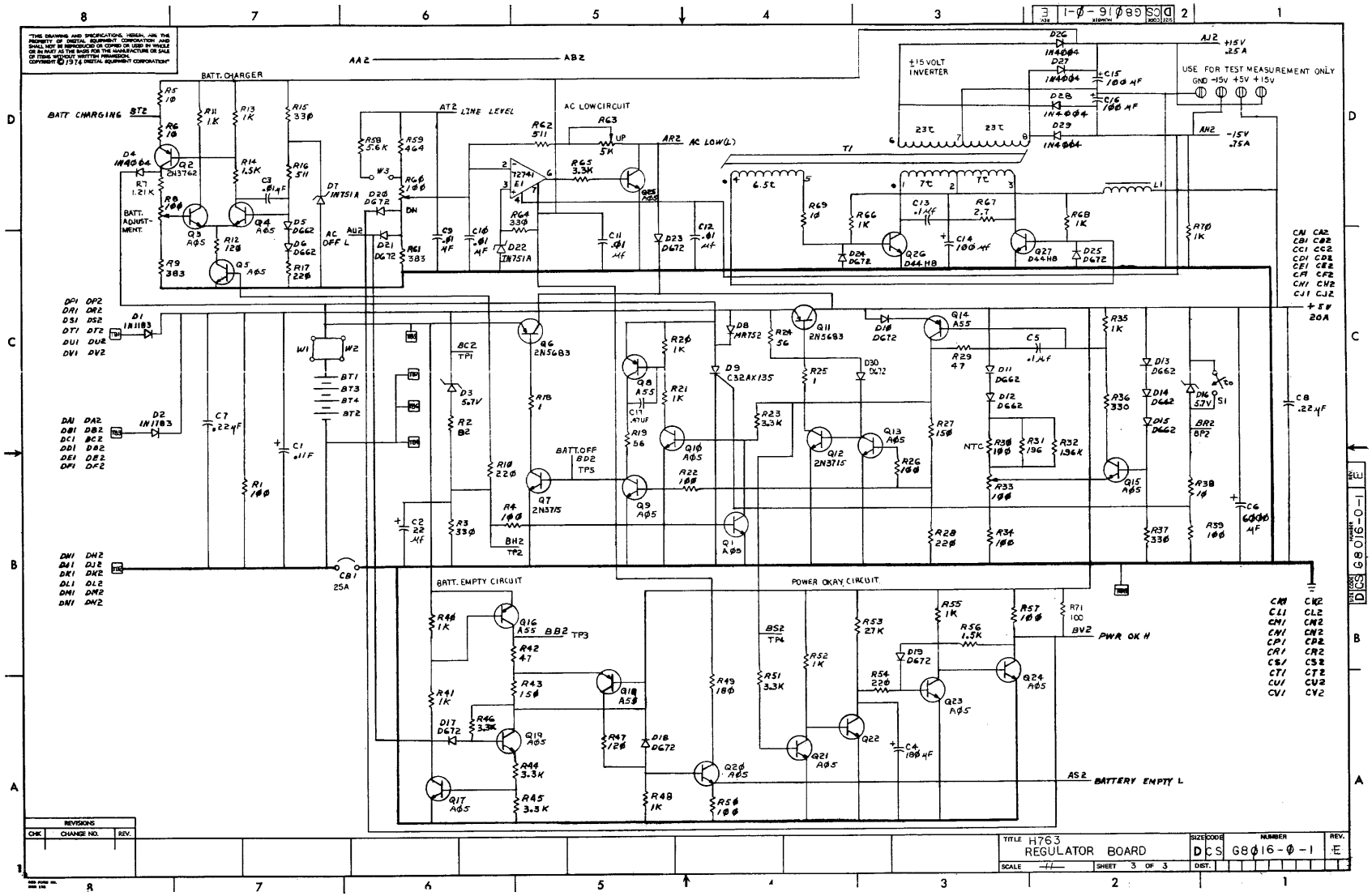
PART NO.	FROM	TO	TERMINATION	WIRE LENGTH
91-07380-22	T81	D1	SOLDER AT D1 END. SOLDER AT T81 END	5.00
91-07380-22	T83	D2	SOLDER AT D2 END. TAB AT T83 END	5.00
91-07380-00	T82	T84	SOLDER AT T82 END SOLDER AT T84 END	7.00
91-07380-00	+ TERMINAL OF C1	TB9 HOLE	SOLDER WIRE AT HOLE END TB9. SOLDERLESS CONNECTOR AT C1 END 90-07926	2.50
91-07380-00	- TERMINAL OF C1	TB10 HOLE	SOLDER WIRE AT HOLE END TB10 SOLDERLESS CONNECTOR AT C1 END 90-07926	1.25
91-07380-00	T87 TOP TERMINAL OF CB1		SOLDER AT T87 END. SOLDERLESS CONNECTOR AT CB1 END 90-07926	7.00
91-07380-00	T88 BOTTOM TERMINAL OF CB1		SOLDER AT T88 END. SOLDERLESS CONNECTOR AT CB1 END 90-07926	11.25
91-07350-22	S1 SPLIT LUG		SOLDER AT SPLIT LUG END	4.00
	S1 SPLIT LUG		SOLDER AT S1 END	4.00

QTY	REF DESIGNATION	DESCRIPTION	PART NO	ITEM
1	R30	RES. 100 1/2W NTC	1341760	53
1	R87	RES. 2.7 1/2W 10%	1389440	54
2	Q7,Q12	TRANS. DEC 2N3715	1503068	55
1	Q2	TRANS. 2N3762	1509649-01	56
18	Q1,Q3,Q4,Q5,Q9,Q10,Q13, Q15,Q17,Q19,Q20,Q21,Q22, Q23,Q24,Q25	TRANS. DEC A05	1510705	57
J	RS8	RES. 5.6K, 1/4W, 5%	1301874	58
4	Q8,Q14,Q16,Q18	TRANS. DEC A55	1510706	59
1	D9	DIODE SCR C32AX135	1510928	60
2	Q6,Q11	TRANS. 2N5683	1511647	61
2	Q26,Q27	TRANS. D44H8	1510707-01	62
1	T1	TRANSFORMER	1611758	63
1	L1	CHOKE	1611759	64
1	E1	I.C. DEC 72741	1910298	65
1		BRACKET REG. B.D.	7411478	66
2		SCREW 4-40 x .50 PH	9006013-1	67
4		SCREW 6-32 x .25 PH	9006020-1	68
2		SCREW 6-32 x .31 PH	9006021-1	69
3		SCREW 6-32 x .75 PH	9006026-1	70
2		KEPNUT 4-40	9006557	71
7		WASHER #6- INTERNAL	9006633	72
9		WASHER #8- FLAT	9006656	73
2		WASHER #4- FLAT	9006	74
8		SPLIT LUGS	9006735	75
2	TB5,TB6	TAB FAST-ON (OFF SET)	9007112	76
1		TRANSIT PAD #10134	9007200	77
8		SCREW .6-32 X .56 PH	9007793-1	78
REF		G8016 REG. BOARD SPEC	G8016-0-8	79
4		SOLDERLESS CONNECTOR	9007926	80
11		KEPNUT 6-32	9008185	81
A/R		WIRE #12 AWG	9107380-00	82
A/R		WIRE #12 AWG	9107380-22	83
A/R	W3	BUS WIRE #22 AWG (SEE NOTE #10)	9107560-01	84
A/R	W1,W2	REEL JUMPER (SEE NOTE #11)	9107560	85
1		SHIELD BATTERY	7411693-0-0	86
3		SPACER #6 .38 LG.	9006801	87
2	TB5 TB6	EYELET	9009000	88
8	TB1,TB2,TB3, TB4, TB7,TB8,TB9, TB10	EYELET GS4-3	9007836	89
A/R		WIRE #22 AWG	9107350-22	90
2		WASHER #8 INTERNAL	9006634	91
A/R		THERMO COMPOUND	9008268	92
2		SCREW 10-32 X .31	9004030-01	93
2		WASHER #10 INTERNAL	9006635	94
1	C17	CAP .47UF 25V -20% CER.	1010275	95
				96
1		DECAL	A-DC-7413109-0-0	97
REF		FINAL INSP. PROC. FOR G8016	TA-SP-G8016-0-9	98
REF		POWER SUPPLY TESTER	B-DD-G8016-TA-	99
1		PACKAGING INSTRUCTION	A-SP-3700175-0-0	100

REVISIONS		
CHK	CHANGE NO.	REV

TITLE	SIZE	CODE	NUMBER	REV.
H763 REGULATOR BOARD	D	DCS	G8016-0-1	E
SCALE	SHEET 2 OF 3		DIST.	

DEC FORM 40
DRD 1/8


BATT. CHARGER
BATT CHARGING BT2
BATT. ADJUSTMENT
AC OFF L
AC LOW CIRCUIT
LINE LEVEL
AC LOW(L)
±15 VOLT INVERTER
USE FOR TEST MEASUREMENT ONLY
GND -15V +5V +15V
+15V .25A
-15V .25A
+5V 20A
BATT. EMPTY CIRCUIT
POWER OKAY CIRCUIT
BATT.OFF BD2 TP5
BATTERY EMPTY L
PWR OK H
CB1 25A
TITLE H763 REGULATOR BOARD
SIZE CODE DCS
NUMBER G8016-0-1
REV. E
SCALE —H—
SHEET 3 OF 3
DIST.
REVISIONS
CHK CHANGE NO. REV.

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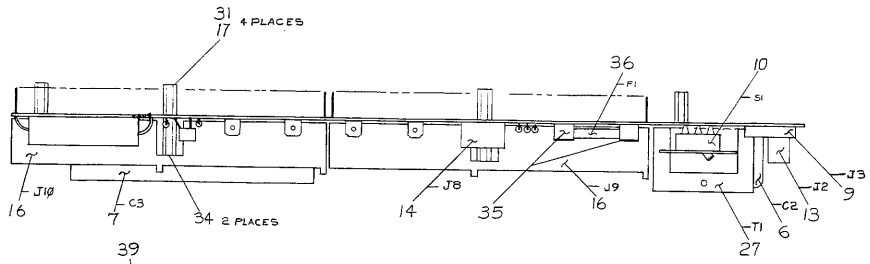
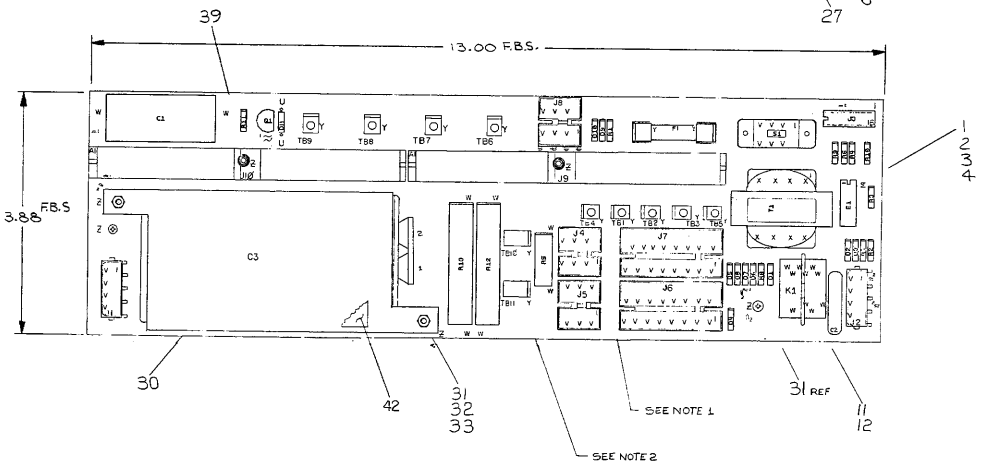
NOTES:

1. FREQUENCY JUMPER (ITEM "28") MUST BE CONNECTED TO J4 OR J5 BEFORE BOARD CAN BE TESTED
2. JUMPERS (ITEM "29") MUST BE CONNECTED (TB11 TO C3-1 & TBIØ TO C3-2) BEFORE CAN BE OPERATIVE.





IC TYPE	GND	+5V

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

REF		DESCRIPTION	PART NO.	ITEM NO.
REF		X-Y COORDINATE HOLE LOCATION	K-CO-5410968-0-1	1
REF		ASSY. DRILLING HOLE LAYOUT	D-MH-5410968-0-1	2
REF		MODULE ECO HISTORY	B-MH-5410968-0-1	3
1		ETCHED CIRCUIT BOARD	5010967	4
1	C1	CAP. 500 UF 25V	1000087	5
1	C2	CAP 2X .02 UF 1000V	1010767	6
1	C3	CAP 3.0 UF, 660V	1011729	7
10	D2 THRU D11	DIODE DG72	1105275	8
1	J3	SOCKET 16 PIN	1211813-02	9
1	S1	SWITCH, SLIDE DPSP	1210919	10
1	K1	RELAY 2 POLE 12V	1211138-01	11
1		SOCKET, RELAY	1211139	12
2	J1, J2	CONN, MATE-N-LOCK 9 PIN	1211342-04	13
3	J8, J4, J5	CONN, MATE-N-LOCK 6 PIN	1211342-06	14
2	J6, J7	CONN, MATE-N-LOCK 16 PIN	1211342-16	15
2	J10 J9	CONN BLOCK 72 PIN, SLOTTED	1211425-00	16
4		SPACER #8-32 x .62 LG x .25 AF	9009629	17
1	R1	RES 470, 1/4W, 5%	1300316	18
3	R2, R3, R4	RES 1.5K, 1/4W, 5%	1300391	19
1	R5	RES 47, 2W, 10%	1301655	20
3	R6, R7, R8	RES 820, 1/4W, 5%	1301775	21
2	R9, R10	RES 270, 1/4W, 5%	1301972	22
2	R12, R13	RES 20, 10W	1305416	23
1	R11	RES 2.2K, 1/4W, 5%	1300417	24
1	Q1	TRANSISTOR MIA940S	1510705	25
1	E1	NPN QUAD CURR DRIVER 4011	1511102-00	26
1	T1	TRANSFORMER	1611646	27
1		JUMPER FREQUENCY	7010042-00	28
2		JUMPER	7010044-00	29
1		BRACKET, CAPACITOR	7411988	30
4		SCR PH PAN HD #8-32 x 9/16	9006036-01	31
2		NUT, KEPS #8-32	9006563-00	32
2		LOCKWASHER INT TOOTH #8	9006634-00	33
2		SPACER #8-32 X .562 LG X 1/4 AF.	9009602-00	34
2		CLIP, FUSE	9007203	35
1	F1	FUSE 1/4 A. S.B.	9007206	36
11	TB1 - TB11	TAB, FASTON	9008219	37
13		EYELET	9009000-00	38
2		SCR SOCKET HD #8-32 x 1.25	9008471-08	39
A/R		WIRE #30 KYNAR	9105740	40
1	D1	DIODE IN 4004	1105796	41
1		DECAL	A-DC-7412194-0-0	42

FIRST USED ON OPTION MODEL: H763

PARTS LIST

ETCH BOARD REV. C

DEC NO.	EIA NO.	DEC NO.	EIA NO.
		DG72	1N3653

SEMICONDUCTOR CONVERSION CHART

REV.	CHANGE NO.	REVISIONS	CHK
D	SK16686-10001	ORIGINATED	
E	SK16686-10001		
F			

P. GARDNER 7/16/73
F. Gardner 5-22-74 DRN
A. DELUCA 6-19-74 ENG
A. DeLuca 6-19-74 PROJ. ENG
K. MALAGHER 12-27-74 MFG
K. Malagher 12-27-74 QA
5410968-0002 F

DRN: K. Boyd DATE 7-30-74
CHK: [signature] DATE 8/5/74
ENG: [signature] DATE 8-11-74
PROJ. ENG: [signature] DATE 8-8-74
MFG: [signature] DATE 8-12-74
QA: [signature] DATE 8-12-74
NEXT HIGHER ASSY: E-UA-H763-0-0
SCALE: —
SHEET 1 OF 2

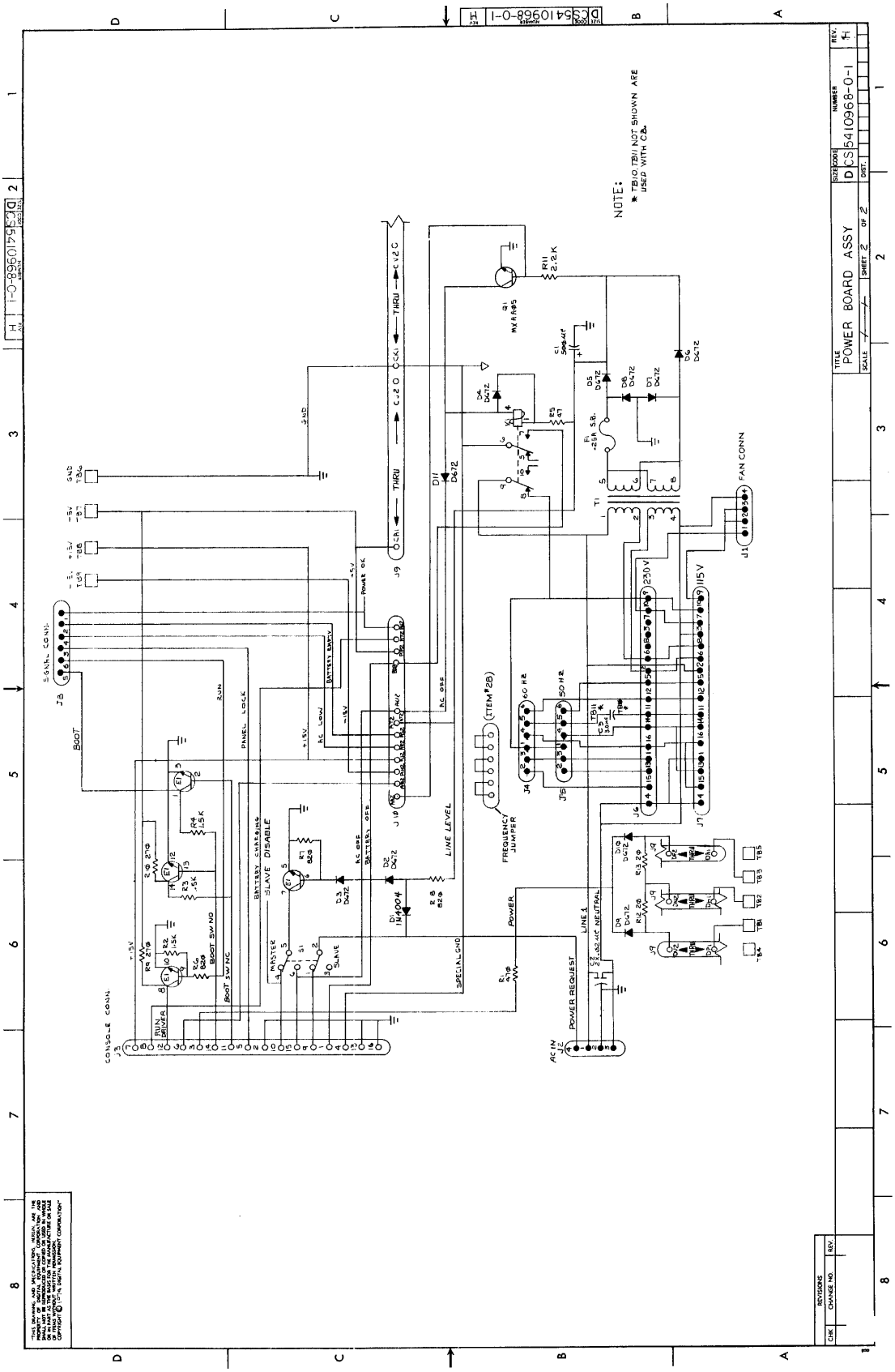
digital

TITLE: POWER BOARD ASSY

SIZE D | CODE CS | NUMBER 5410968-0-1 | REV. H

DIST.

SIZE D CS 5410968-0-1 REV H


POWER BOARD ASSY
DCS410968-0-1
NOTE:
* TB10, TB11 NOT SHOWN ARE USED WITH CB
CONSOLE CONN.
J3
SIGN. CONN.
J8
FAN CONN
J11
POWER REQUEST
AC IN
J2
FREQUENCY JUMPER
(ITEM #28)
BOOT SW NC
BOOT SW NO
SLAVE DISABLE
LINE LEVEL
THRU
230V
115V
50 HZ
60 HZ

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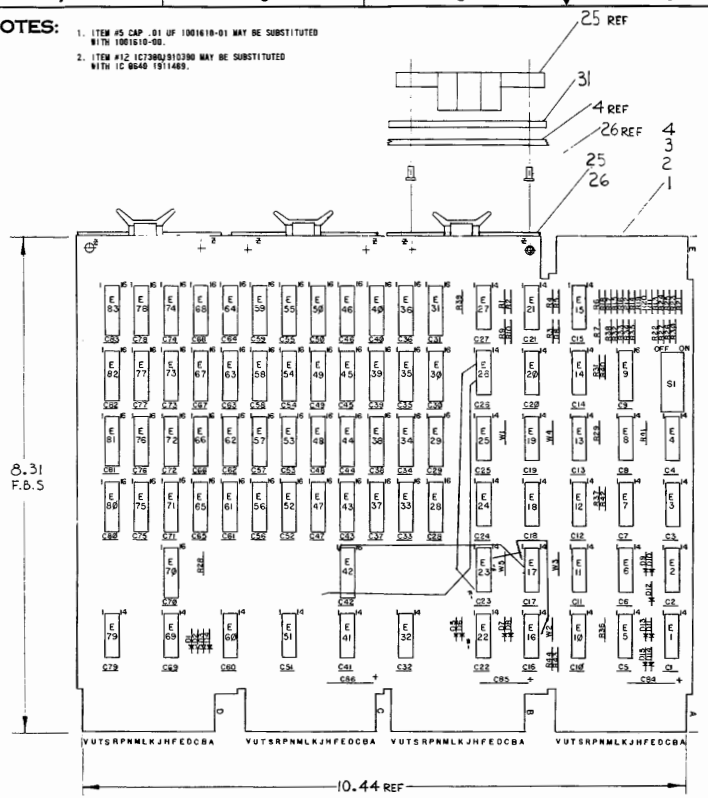
NOTES:

1. ITEM #5 CAP .01 UF 1001610-01 MAY BE SUBSTITUTED WITH 1001610-00.
2. ITEM #12 IC7380J/S10390 MAY BE SUBSTITUTED WITH IC 8648 1911469.



M8311-YA	M8311-YB	M8311-YC	M8311-YD	M8311-YE	M8311-YF	M8311-YH	M8311-YJ			
REF	REF	REF	REF	REF	REF	REF	REF		X-Y COORDINATE HOLE LOCATION	K-CO-M8311-0-4	1
REF	REF	REF	REF	REF	REF	REF	REF		ASSY/DRILLING HOLE LAYOUT	D-AH-M8311-0-5	2
REF	REF	REF	REF	REF	REF	REF	REF		MODULE ECO HISTORY	B-MH-M8311-0-6	3
1	1	1	1	1	1	1	1		ETCHED CIRCUIT BOARD	5010586	4
-	-	71	-	-	-	71	-	C1-C27,C29-C32,C34-C36,C38,C42,C44-C46,C48-C51,C53-C55,C57-C60,C62-C64,C66-C70,C72-C74,C76-C79,C81-C83			
-	59	-	-	-	59	-	-	C1-C27,C30-C32,C35,C36,C39,C40,C41,C42,C45,C46,C49,C50,C51,C54,C55,C58,C59,C60,C63,C64,C67-C70,C73,C74,C77,C78,C79,C82,C83			
47	-	-	-	47	-	-	-	C1-C27,C31,C32,C36,C40-C42,C46,C50,C51,C55,C59,C60,C64,C68-C70,C74,C78,C79,C83	CAP .01 UF 100V 20% (SEE NOTE #1)	1001610-01	5
			83				83	C1-C83			
15	15	15	15	15	15	15	15	D1-D15	DIODE D664	1100114	6
11	11	11	11	11	11	11	11	R1-R10,R36	RES, 180 1/4W 5%	1301322	7
5	5	5	5	5	5	5	5	R39-R43	RES, 220 1/4W 5%	1300271	8
13	13	13	13	13	13	13	13	R11-R20,R38,R31,R37	RES, 2.2K 1/4W 5%	1300417	9
1	1	1	1	1	1	1	1	S1	SWITCH 10 POS	1211184-06	10
1	1	1	1	1	1	1	1	E7	IC 7402	1909004	11
6	6	6	6	6	6	6	6	E22,E23,E41,E68,E79,E1	IC 7380 (SEE NOTE #2)	1910390	12
4	4	4	4	4	4	4	4	E5,E32,E51,E69	IC 8881	1909705	13
3	3	3	3	3	3	3	3	E4,E6,E17	IC 7400	1905575	14
1	1	1	1	1	1	1	1	E19	IC 7410	1905576	15
1	1	1	1	1	1	1	1	E2	IC 8242	1909712	16
1	1	1	1	1	1	1	1	E13	IC 74164	1910041	17
1	1	1	1	1	1	1	1	E10	IC 7490	1910155	18
5	5	5	5	5	5	5	5	E8,E18,E15,E21,E27	IC 7437	1910091	19
4	4	4	4	4	4	4	4	E3,E14,E28,E26	IC 7384	1910393	20
4	4	4	4	4	4	4	4	E11,E12,E16,E24	IC 7474	1905547	21
2	2	2	2	2	2	2	2	E42,E70	IC 74174	1910652	22
-	-	-	48	-	-	-	-	E28-E31,E33-E40,E43-E50,E52,E59,E61-E68,E71-E78,E80-E83			
-	-	36	-	-	-	-	-	E29-E31,E34-E36,E38-E40,E44,E46,E48-E50,E53-E55,E57-E59,E62-E64,E66-E68,E72-E74,E76-E78,E81-E83	IC DEC 2102-0	2111318-0C	23
-	24	-	-	-	-	-	-	E30,E31,E35,E36,E39,E40,E45,E46,E49,E50,E54,E55,E58,E59,E63,E64,E67,E68,E73,E74,E77,E78,E82,E83			
12	-	-	-	-	-	-	-	E31,E36,E40,E46,E50,E55,E56,E64,E68,E74,E78,E83			
-	-	-	-	-	-	-	48	E28-E31,E33,E40,E43-E50,E52-E59,E61-E68,E71-E78,E80-E83			
-	-	-	-	-	-	36	-	E29-E31,E34-E38,E38-E40,E44-E46,E48-E50,E53-E55,E57-E59,E62-E64,E66-E68,E72-E74,E76-E78,E81-E83	IC DEC 2102-1	2111318-01	24
QTY	QTY	QTY	QTY	QTY	QTY	QTY	QTY	QTY	REF. DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.

FIRST USED ON OPTION MODEL: PDP8A

PARTS LIST

ETCH BOARD REV. E

8223	8	16
2102	9	18
74174	8	16
7384	1	8
7380	1	8
IC TYPE	GND	+5V

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

REV	CHANGE NO.	ORIGINATED	CHK
D			
E		M8311-0000	
F			

R. Hayes 10/23/74
B. TARPLEY 7/24/74
B. TARPLEY 8-6-74

DEC NO. | EIA NO. | DEC NO. | EIA NO.

SEMICONDUCTOR CONVERSION CHART

DRN: George Long 6/26/74
CHK'D: [illegible] 6/27/74
ENGR: [illegible] 6/27/74
PROJ. ENG: [illegible] 7/1/74
MFG: [illegible] 7/1/74
NEXT HIGHER ASSY: D-DD-PDP8A-0
SCALE: NONE
SHEET 1 OF 6

digital

TITLE: 4K X 12 MOS. MEMORY

SIZE D | CODE CS | NUMBER M8311-0-1 | REV. F

DIST.

DCS M8311-0-1 REV F

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M8311-YA	M8311-YB	M8311-YC	M8311-YD	M8311-YE	M8311-YF	M8311-YH	M8311-YJ	REF DESIGNATION	DESCRIPTION	PART NO	ITEM NO
QTY	QTY	QTY	QTY	QTY	QTY	QTY	QTY				
-	-	-	-	-	24	-	-	E30,E31,E35,E36,E39,E40,E45,E46,E49,E50,E54,E55,E58,E59,E63,E64,E67,E68,E73,E74,E77,E78,E82,E83.	IC DEC 2102-1	2111318-0-1	24
-	-	-	-	12	-	-	-	E31,E36,E40,E46,E50,E55,E59,E64,E68,E74,E78,E83			
3	3	3	3	3	3	3	3		HANDLE FLIP CHIP MAGENTA	9008337-06	25
6	6	6	6	6	6	6	6		EYELET GS4-7	9008750	26
1	1	1	1	1	1	1	1	E9	IC DEC 8223 OR EQUIVALENT	23003A1	27
5	5	5	5	5	5	5	5	W1-W5	INSULATED JUMPER	9006105	28
3	3	3	3	3	3	3	3	C64, C65, C66	CAP .68 MF 35V, 10% TAPT	1005306	29
14	14	14	14	14	14	14	14	R21-R29, R32-R35, R38	RES. 3.3K 1/4W 5%	1300439	30
3	3	3	3	3	3	3	3		SPACER (CABLE CLAMP)	1202704	31
1	1	1	1	1	1	1	1	R44	RES. 3ΩΩ 1/4W 5%	1300308	32
1	1	1	1	1	1	1	1	E25	CRYSTAL OSCILLATOR 18 MHZ	1011660-01	33

SWITCH DEFINITIONS

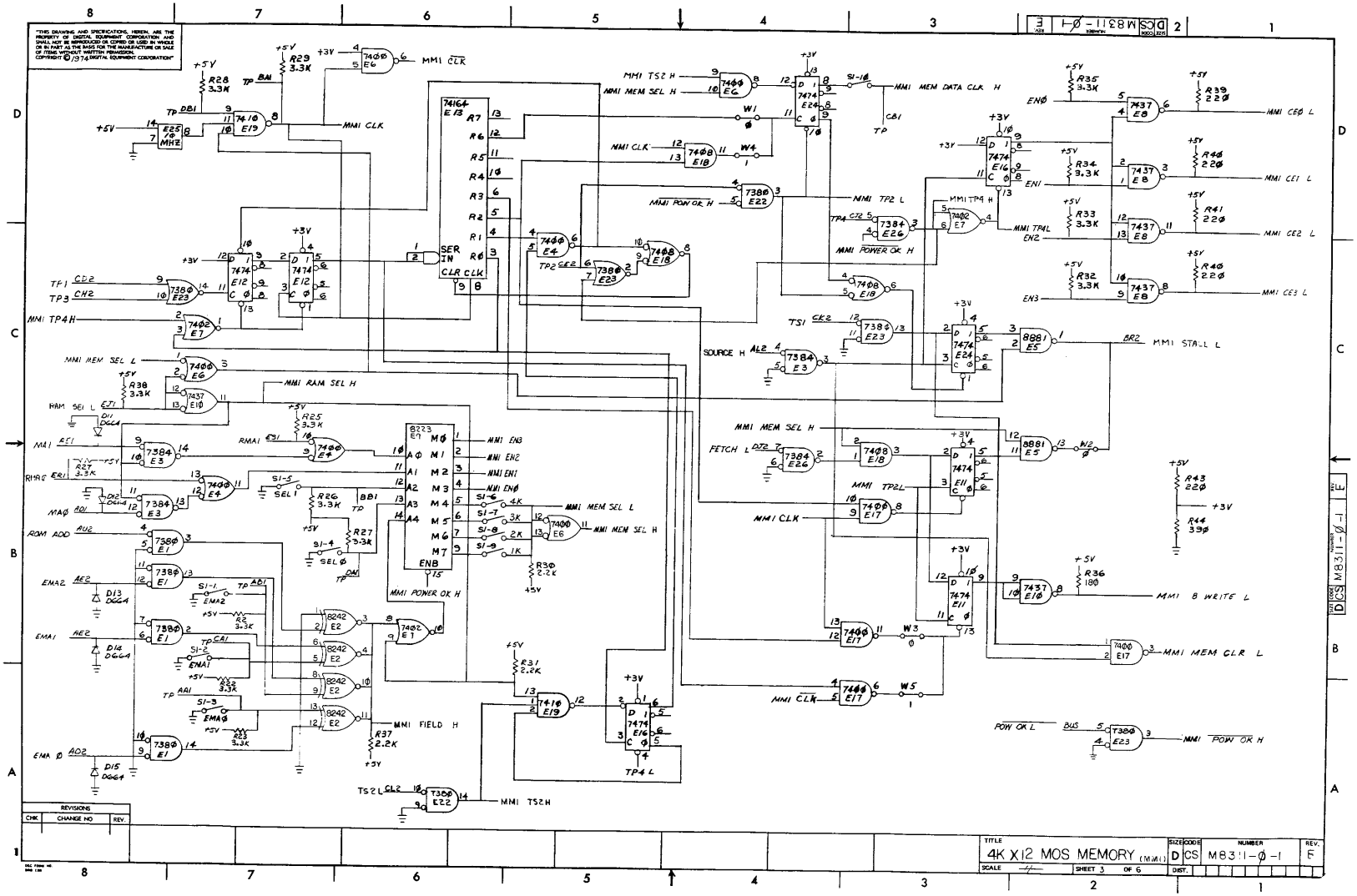
SW1-1	EMA2	FIELD SELECTION 'ON' IS Ø
SW1-2	EMA1	
SW1-3	EMAØ	
SW1-4	SELØ	STARTING ADDRESS SELECT 'ON' IS Ø
SW1-5	SEL1	
SW1-6	4K	MEMORY SIZE SELECT CORRECT SIZE-'ON' OTHERS - 'OFF'
SW1-7	3K	
SW1-8	2K	
SW1-9	1K	
SW1-10		USED FOR TEST ONLY, ALWAYS 'ON'

JUMPER CONFIGURATION

YA, YB, YC AND YD — W1, W2, W3 ARE IN	W4 AND W5 ARE OUT
YE, YF, YH AND YJ — W4 AND W5 ARE IN	W1, W2 AND W3 ARE OUT

REVISIONS		
CHK	CHANGE NO	REV

TITLE 4K X 12 MOS MEMORY
SIZE D CODE CS NUMBER M8311-Ø-1 REV. F
SCALE NONE SHEET 2 OF 6 DIST.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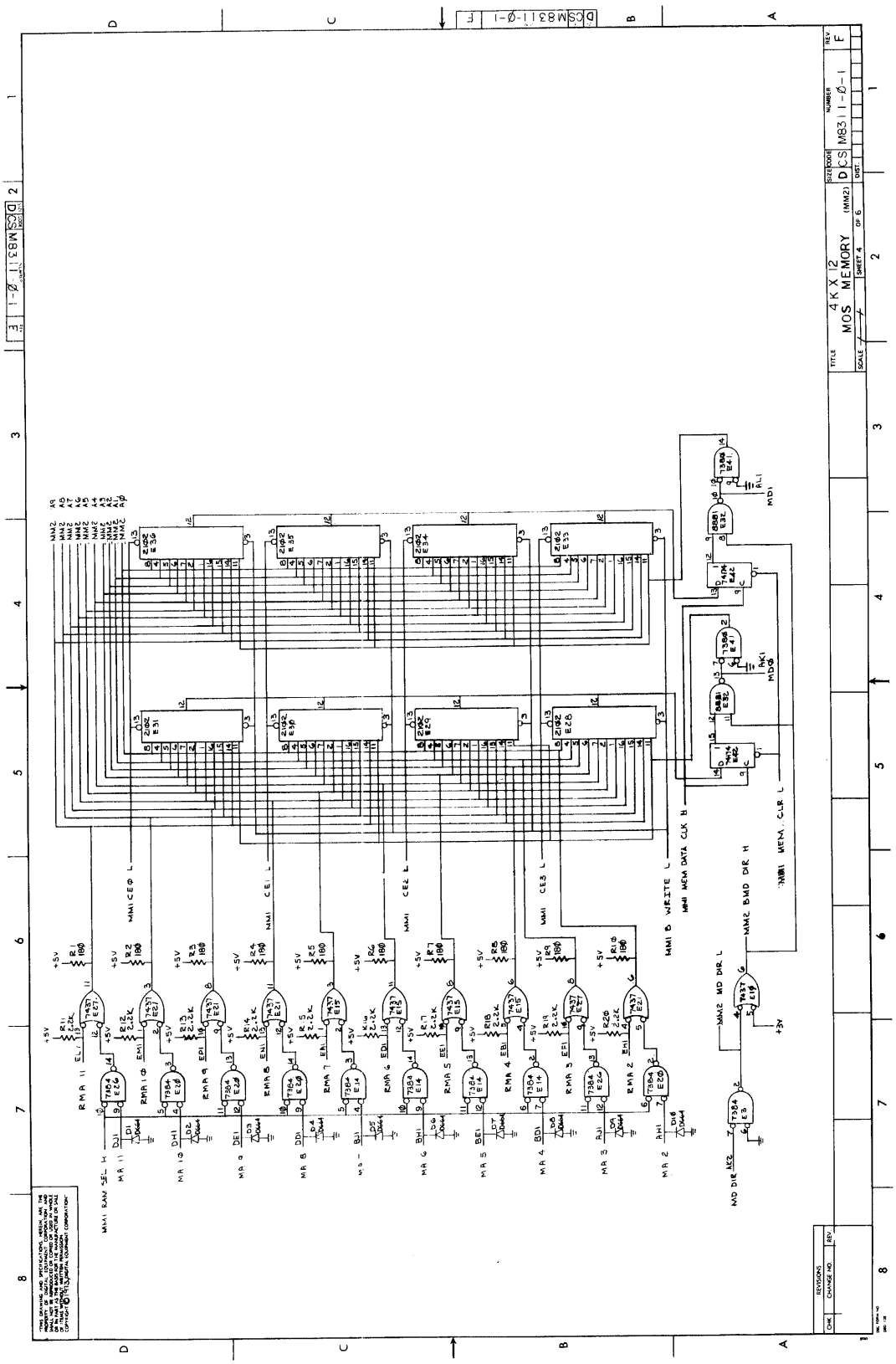
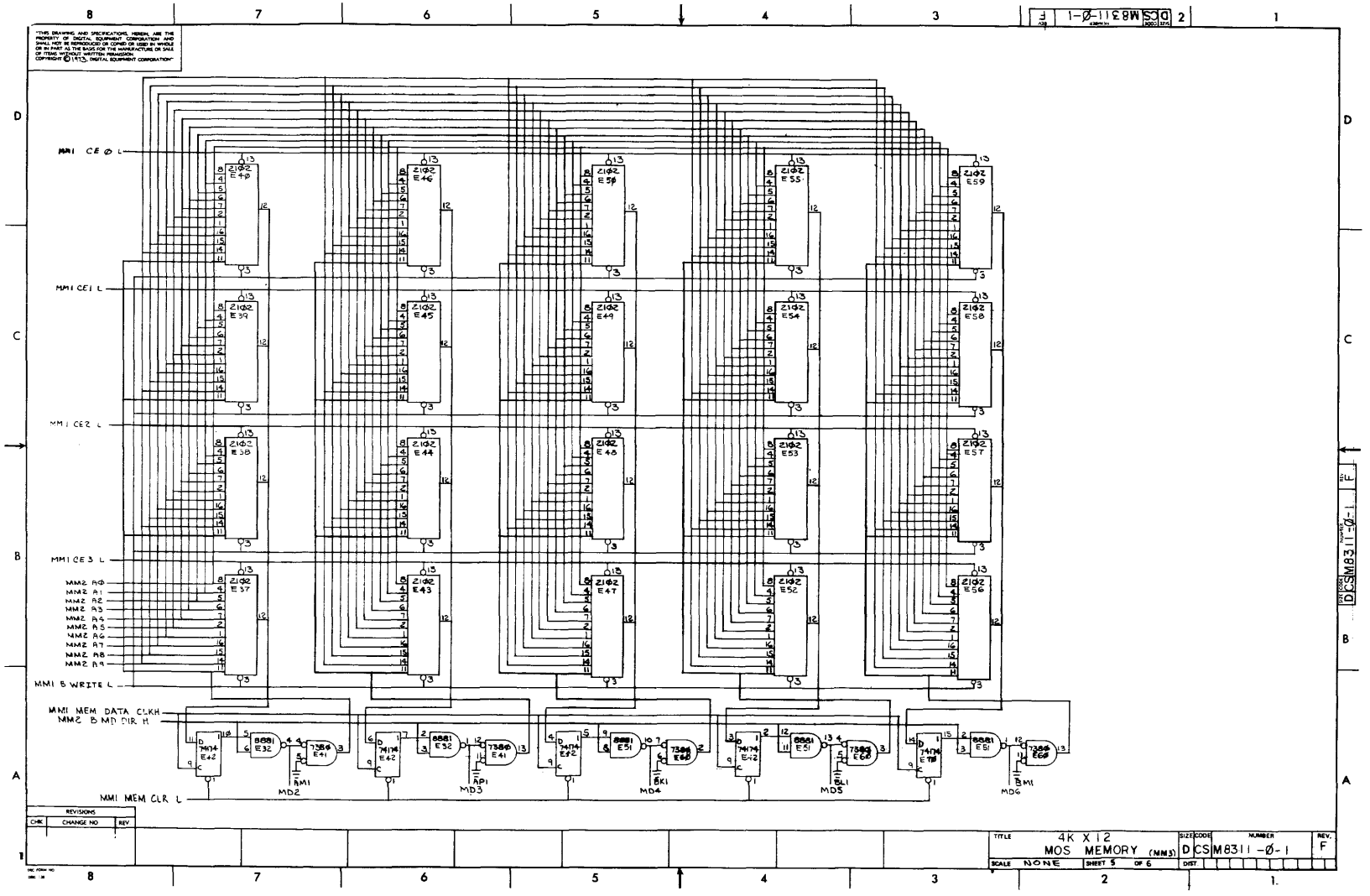
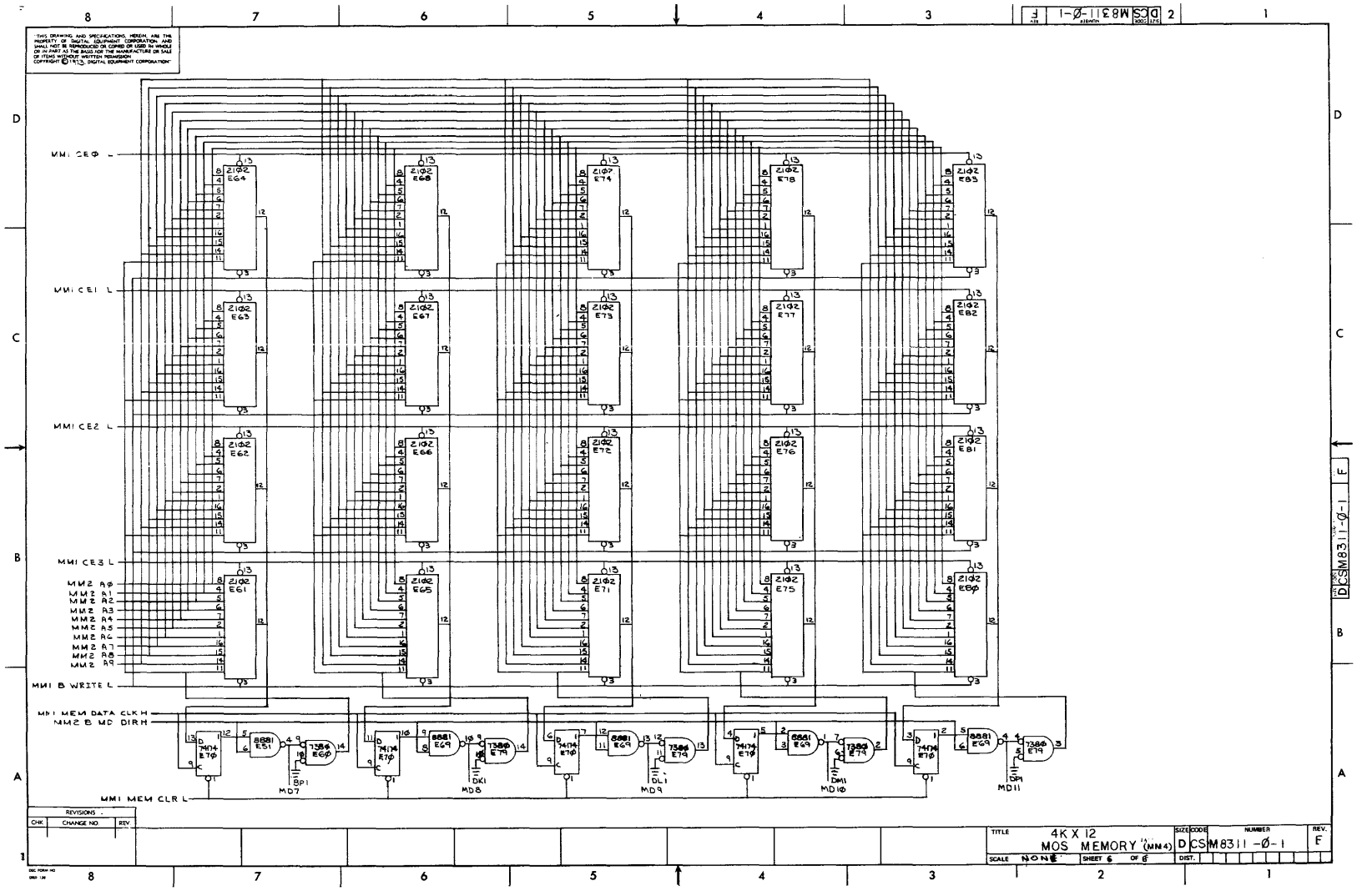
MMI CLR
MMI CLK
MMI TS2 H
MMI MEM SEL H
MMI MEM DATA CLK H
MMI POWER OK H
MMI TP2 L
MMI TP4 H
MMI TP4 L
MMI RAM SEL H
MMI MEM SEL L
MMI FIELD H
MMI TS2 H
MMI EN3
MMI EN2
MMI EN1
MMI EN0
MMI CE0 L
MMI CE1 L
MMI CE2 L
MMI CE3 L
MMI STALL L
MMI MEM CLR L
MMI B WRITE L
MMI POW OR H
SOURCE H
FETCH L
POW OR L
TP4 L
4K X 12 MOS MEMORY (MMI)
M8311-Ø-1
SHEET 3 OF 6
REVISIONS
CHK
CHANGE NO
REV.

H-69


4K X 12
MOS MEMORY
(MM2)
DCSM8311-0-1
MMI MEM. CLR L
MMI MEM DATA CLK H
MMI WRITE L
MM2 MD DIR L
MM2 BMD DIR H
MMI RAM SEL H
MMI CE0 L
MMI CE1 L
MMI CE2 L
MMI CE3 L


MM1 CE Ø L
MM1 CE1 L
MM1 CE2 L
MM1 CE3 L
MM2 A0
MM2 A1
MM2 A2
MM2 A3
MM2 A4
MM2 A5
MM2 A6
MM2 A7
MM2 A8
MM2 A9
MM1 B WRITE L
MM1 MEM DATA CLKH
MM2 B MD DIR H
MM1 MEM CLR L
MD2
MD3
MD4
MD5
MD6
TITLE 4K X 12 MOS MEMORY (MM3)
SIZE CODE DCSM8311-Ø-1
REV. F
SCALE NONE
SHEET 5 OF 6
DIST
REVISIONS
CHK
CHANGE NO
REV
DCSM8311-Ø-1


MM1 CEΦ L
MM1 CE1 L
MM1 CE2 L
MM1 CE3 L
MM2 A0
MM2 A1
MM2 A2
MM2 A3
MM2 A4
MM2 A5
MM2 A6
MM2 A7
MM2 A8
MM2 A9
MM1 B WRITE L
MM1 MEM DATA CLK H
MM2 B MD DIR H
MM1 MEM CLR L
MD7
MD8
MD9
MD10
MD11
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REVISIONS
CHK
CHANGE NO.
REV.
TITLE 4K X 12 MOS MEMORY (MM4)
SIZE D
CODE
NUMBER DCSM8311-Ø-1
REV. F
SCALE NONE
SHEET 6 OF 6
DIST.
DCSM8311-Ø-1 F

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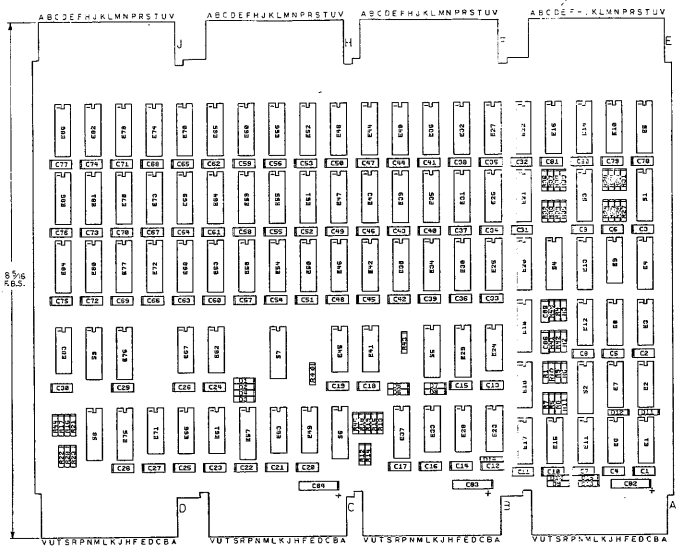
NOTES:

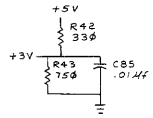
1. ITEM #7 CAP .01uF 1001610-01 MAY BE SUBSTITUTED WITH 1001610-00.
2. ALL PROMS IN MODULE MUST BE THE SAME DASH VARIATION

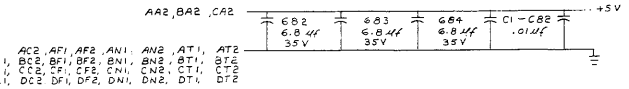
ROM SWITCH SETTINGS

SW	1	2	3	4	5	6	7	8	FUNCTION
S1	1	1	1	1	1	1	1	1	PROGRAM
S2	1	–	–	Ø	–	–	1	–	1K
S2	Ø	–	–	Ø	–	–	1	–	2K
S2	Ø	–	–	1	–	–	Ø	–	3K
S2	Ø	–	–	Ø	–	–	Ø	–	4K
S2	–	–	Ø	–	–	Ø	Ø	–	FIELD Ø
S2	–	–	Ø	–	–	1	Ø	–	FIELD 1
S2	–	–	1	–	–	Ø	Ø	–	FIELD 2
S2	–	–	1	–	–	1	Ø	–	FIELD 3
S2	–	–	Ø	–	–	Ø	1	–	FIELD 4
S2	–	–	Ø	–	–	1	1	–	FIELD 5
S2	–	–	1	–	–	Ø	1	–	FIELD 6
S2	–	–	1	–	–	1	1	–	FIELD 7
S2	–	Ø	–	Ø	–	–	–	–	256X4 PROM
S3	1	1	1	1	1	1	1	1	PROGRAM
S4	1	1	1	1	Ø	1	–	–	PROGRAM
S4	–	–	–	–	–	–	1	Ø	ROM ONLY
S4	–	–	–	–	–	–	Ø	1	ROM/RAM
S5	1	1	1	1	1	1	1	1	PROGRAM
S6	Ø	Ø	1	1	1	1	1	1	PROGRAM
S7	1	1	1	1	1	1	1	1	PROGRAM
S8	1	1	1	1	1	1	1	1	PROGRAM
S9	1	1	1	1	1	1	1	1	PROGRAM

1=ON Ø=OFF







DEC 1024 BIT OPEN COLLECTOR PROM	8	16
11380	1	8
74175	8	16
74153	8	16
7442	8	16
IC TYPE	GND	+5V

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

M8312-YA M8312-YB M8312-YE M8312-YD

REF	REF	REF	REF				
REF	REF	REF	REF		X-Y COORDINATE HOLE LOCATION	K-CO-M8312-B-4	1
REF	REF	REF	REF		ASSY/DRILLING HOLE LAYOUT	D-AH-M8312-B-5	2
REF	REF	REF	REF		MODULE ECO HISTORY	B-MH-M8312-B-6	3
1	1	1	1		ETCHED BOARD	5010598	4
3	3	3	3	C82,C83,C84	CAP 6.8 UF, 35V, 10% STANT	1005306	5
15	15	15	15	D1-D15	DIODE D664	1100114	6
-	-	-	81	C1 THRU C81			
-	-	66	–	C1 THRU C65,C78,C79,C80	CAP .01UF, 100V 10% DISC	1001610-01	7
-	55	-	-	C1 THRU C53,C78,C79	(SEE NOTE 1)		
42	-	-	-	C1 THRU C41,C78			
1	1	1	1	C85,	CAP 68 PF 100V 5%	1000014	8
31	31	31	31	R1 THRU R11,R24 THRU R39, R43-R46	RES. 1K 1/4W 5%	1300365	9
12	12	12	12	R12 THRU R23	RES. 680 1/4W 5%	1301424	10
1	1	1	1	R40	RES. 15K 1/4W 5%	1300496	11
1	1	1	1	E24	I.C. DEC 7474	1905547	12
1	1	1	1	E9	I.C. DEC 74H40	1905586	13
1	1	1	1	E8	I.C. DEC 74H00	1909056	14
4	4	4	4	E15,E28,E49,E66	I.C. DEC 8881	1909705	15
2	2	2	2	E7,E12	I.C. DEC 8242	1909712	16
2	2	2	2	E4,E13	I.C. DEC 74153	1909937	17
2	2	2	2	E29,E76	I.C. DEC 7442	1910046	18
6	6	6	6	E18,E41,E45,E62,E67,E83	I.C. DEC 7437	1910091	19
2	2	2	2	E2,E3	I C DEC 74H50	1909060	20
2	2	2	2	E11,E17	I.C DEC 11380	1911113	21
3	3	3	3	E37,E57,E75	I.C. DEC 74175	1910651	22
3	3	3	3	E33,E53,E71	I.C. DEC 7400	1905575	23
1	1	1	1	E19	I.C. DEC 74123	1910436	24
1	1	1	1	R42	RES 27K 1/4W 5%	1305346-00	25
9	9	9	9	S1 THRU S9	SWITCH PACK	1211164-04	26
4	4	4	4	E1,E6,E23,E61	I.C. DEC 5384	1910394	27
1	1	1	1	C86	CAP 47MMF 100V 5%	1000011-00	28
13	-	-	-	E5,E20-E22,E25-E27,E30-E32,E34-E36			
-	26	-	-	E5,E10,E20-E22,E25-E27,E30-E32,E34-E36,E38-E40,E42-E44,E46-E48,E50-E52			
-	-	39	-	E5,E10,E14,E20-E22,E25-E27,E30-E32,E34-E36,E38-E40,E42-E44,E46-E48,E50-E52,E54-E56,E58-E60,E63-E65,E68-E70	I.C. DEC 1024 PROM REFER TO NOTE 2	2300088	29
-	-	-	52	E5,E10,E14,E16,E20-E22,E25-E27,E30-E32,E34-E36,E38-E40,E42-E44,E46-E48,E50-E52,E54-E56,E58-E60,E63-E65,E68-E70,E72-E74,E77-E79,E80,E82,E84-E86			
13	-	-	-				
-	26	-	-				
-	-	52	-		SOCKET I C.	1211813-0	30
-	-	-	52				
1	1	1	1	R41	RES. 8.2K 1/4W 5%	1303179-00	31
A/R	A/R	A/R	A/R		WIRE INSULATED KYNAR 30 AWG.	9105740-	32
QTY	QTY	QTY	QTY	REF. DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.

FIRST USED ON OPTION MODEL: PDP8A

PARTS LIST

ETCH BOARD REV. D

DEC NO.	EIA NO.	DEC NO.	EIA NO.

SEMICONDUCTOR CONVERSION CHART

REV.	CHANGE NO.	CHK
D	ORIGINATED	R. REGAN
E	M836E-00001	

DRN	C. Wilson	6/7/74
CHK	T. Shaw	6/7/74
ENG	D. Kaufman	6/10/74
PROD ENG		
		6/10/74
	D. Delaney	6/10/74

NEXT HIGHER ASSY: 8-DC-PDP8A-C

SCALE: NONE

SHEET 1 OF 6

digital

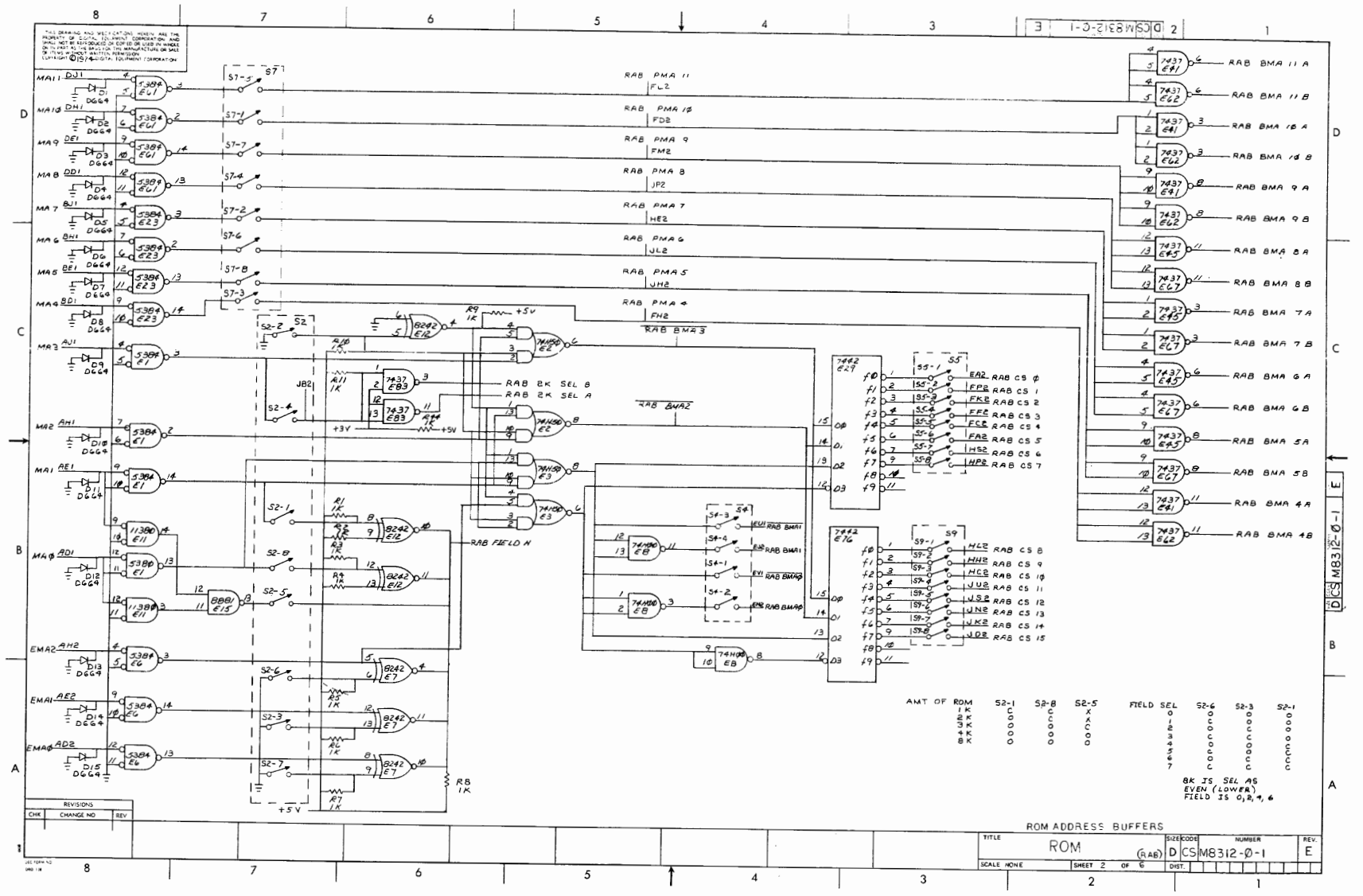
TITLE: ROM

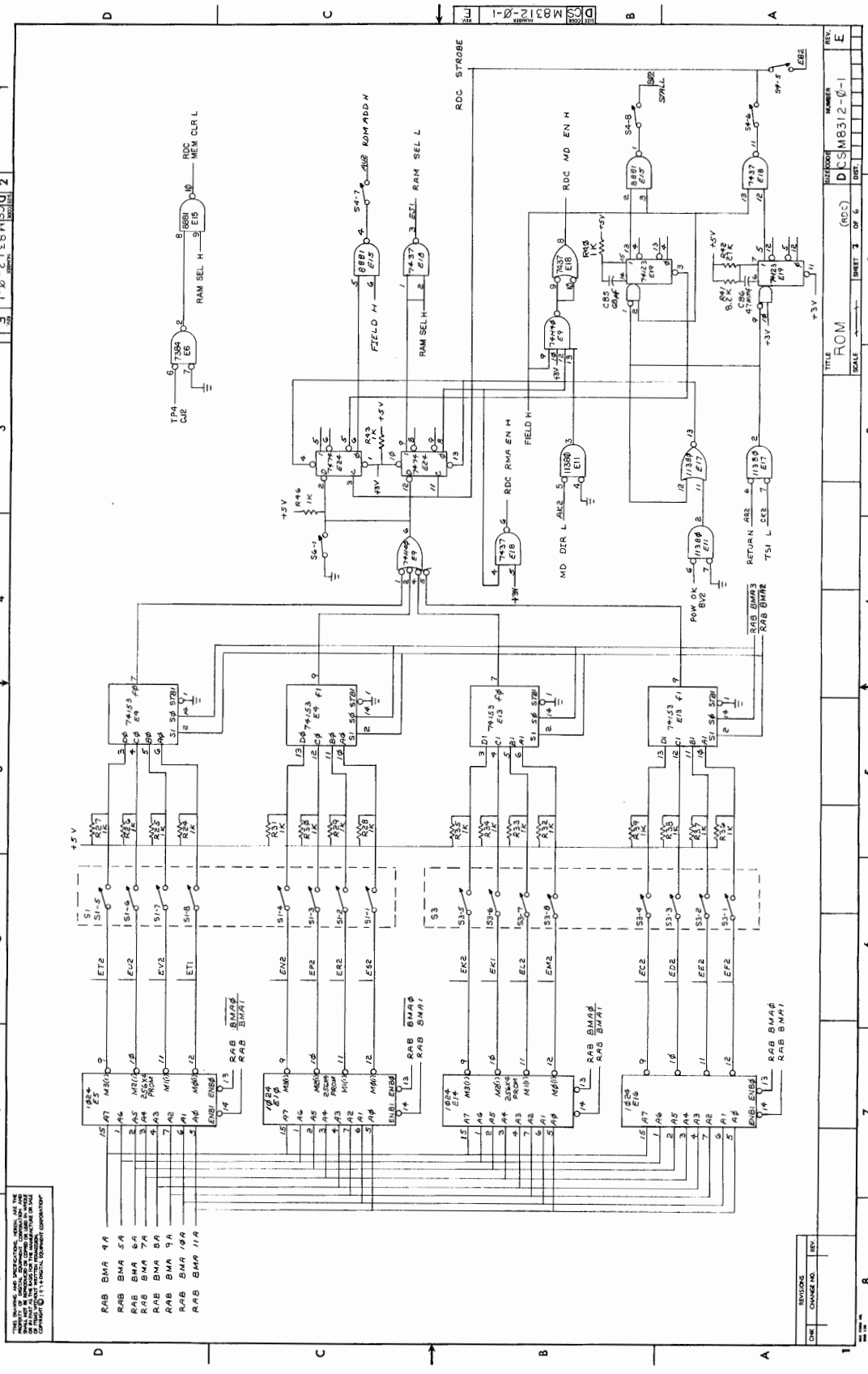
SIZE D | CODE CS | NUMBER M8312-Ø-1 | REV. E

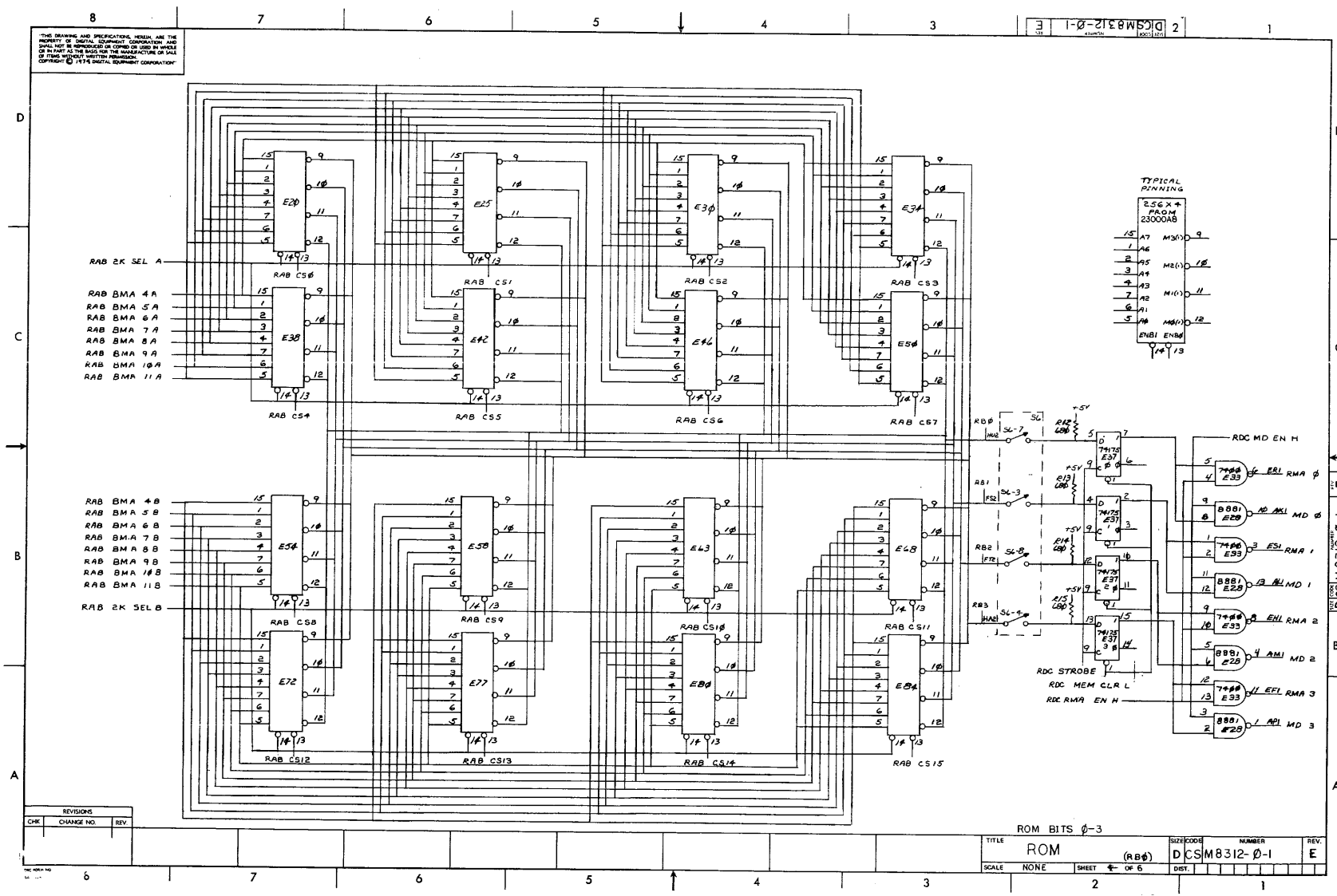
DIST.

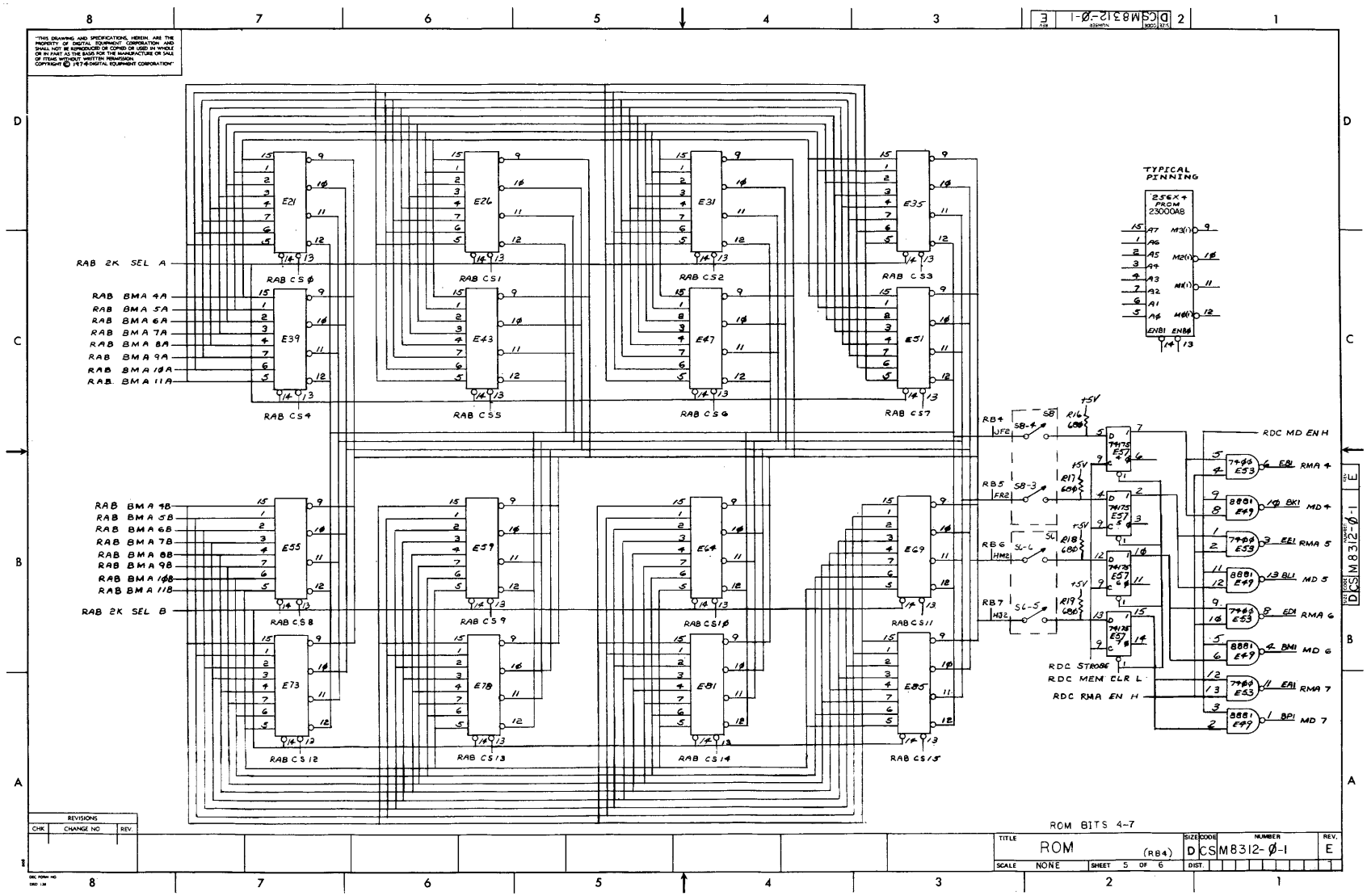
DRAWING NUMBER: D CS M8312-Ø-1 REV E

NEXT ASSY USED ON: D CS M8312-Ø-1


RAB PMA 11
RAB PMA 10
RAB PMA 9
RAB PMA 8
RAB PMA 7
RAB PMA 6
RAB PMA 5
RAB PMA 4
RAB BMA3
RAB 2K SEL B
RAB 2K SEL A
RAB BMA2
RAB FIELD N
RAB BMA 11 A
RAB BMA 11 B
RAB BMA 10 A
RAB BMA 10 B
RAB BMA 9 A
RAB BMA 9 B
RAB BMA 8 A
RAB BMA 8 B
RAB BMA 7 A
RAB BMA 7 B
RAB BMA 6 A
RAB BMA 6 B
RAB BMA 5 A
RAB BMA 5 B
RAB BMA 4 A
RAB BMA 4 B
RAB CS 0
RAB CS 1
RAB CS 2
RAB CS 3
RAB CS 4
RAB CS 5
RAB CS 6
RAB CS 7
RAB CS 8
RAB CS 9
RAB CS 10
RAB CS 11
RAB CS 12
RAB CS 13
RAB CS 14
RAB CS 15
AMT OF ROM
FIELD SEL
8K IS SEL AS EVEN (LOWER) FIELD IS 0,2,4,6
ROM ADDRESS BUFFERS
ROM (RAB)
D CS M8312-0-1
E
SCALE NONE
SHEET 2 OF 6




RAB 2K SEL A
RAB BMA 4A
RAB BMA 5A
RAB BMA 6A
RAB BMA 7A
RAB BMA 8A
RAB BMA 9A
RAB BMA 10A
RAB BMA 11A
RAB 2K SEL B
RAB BMA 4B
RAB BMA 5B
RAB BMA 6B
RAB BMA 7B
RAB BMA 8B
RAB BMA 9B
RAB BMA 10B
RAB BMA 11B
RAB CS0
RAB CS1
RAB CS2
RAB CS3
RAB CS4
RAB CS5
RAB CS6
RAB CS7
RAB CS8
RAB CS9
RAB CS10
RAB CS11
RAB CS12
RAB CS13
RAB CS14
RAB CS15
TYPICAL PINNING
2.56 X 4 PROM 23000AB
RDC MD EN H
RDC STROBE
RDC MEM CLR L
RDC RMA EN H
RMA Ø
MD Ø
RMA 1
MD 1
RMA 2
MD 2
RMA 3
MD 3
ROM BITS Ø-3
ROM
(RBØ)
NONE
DCSM8312-Ø-1
E



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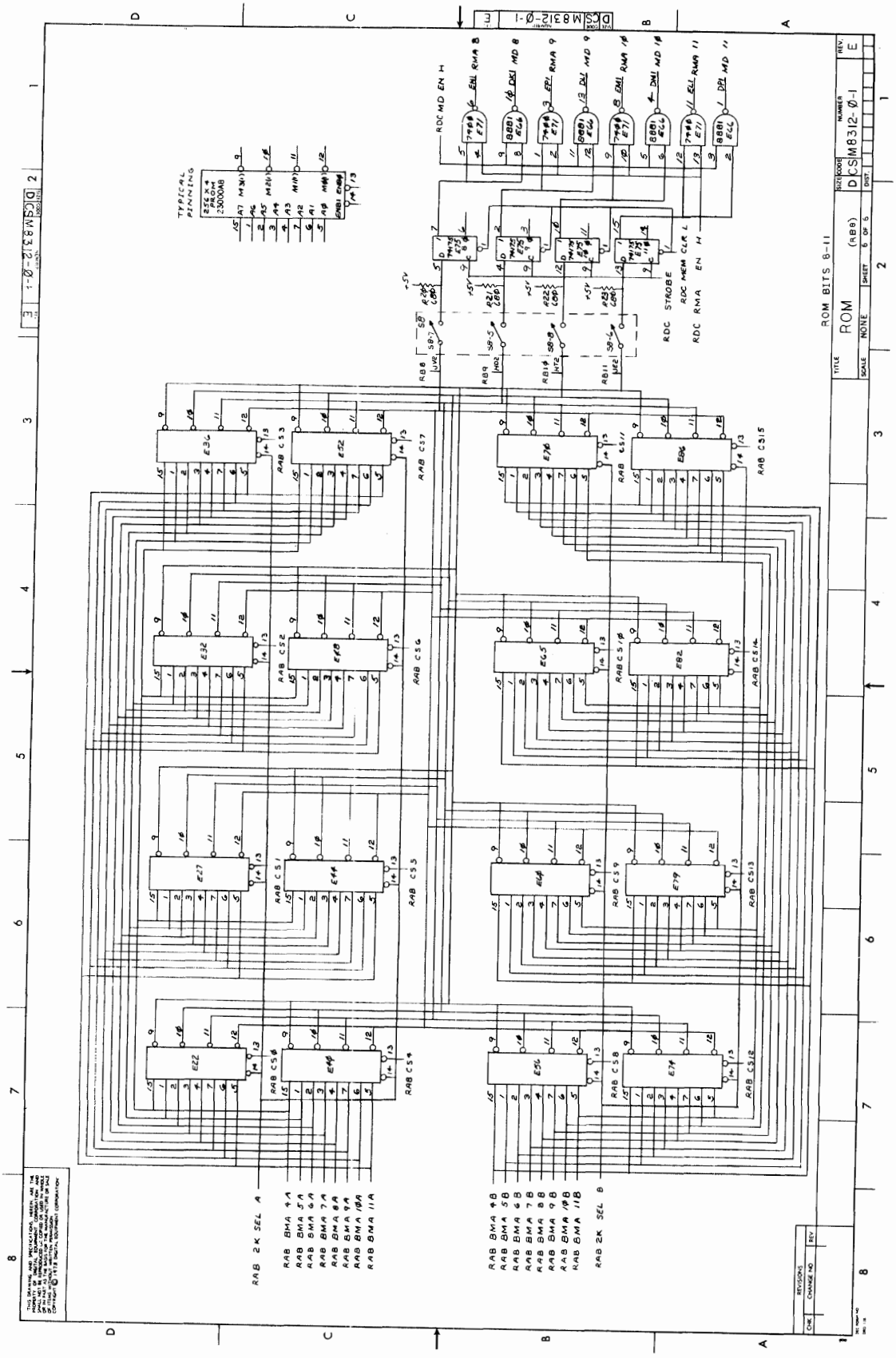
REVISIONS		
CHK	CHANGE NO	REV.

ROM BITS 4-7

TITLE		SIZE	CODE	NUMBER	REV.
ROM (RB4)		D	DCSM8312-Ø-1		E
SCALE NONE	SHEET 5 OF 6	DIST.			

DRC FORM NO
DSD 138

DCSM8312-Ø-1 E


ROM
DCSM8312-0-I
ROM BITS 8-11
ROC MD EN H
ROC STROBE
ROC MEM CLR L
ROC RMA EN H
RAB 2K SEL A
RAB 2K SEL B

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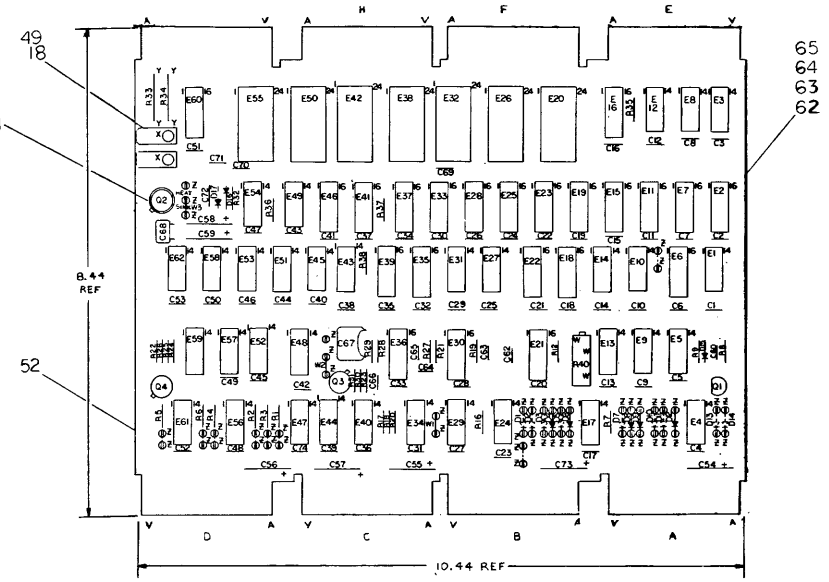
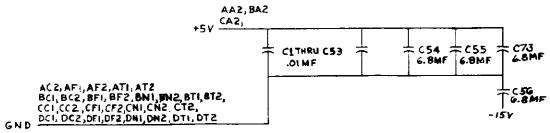
NOTES:

1. JUMPERS IN FOR Ø OUT FOR 1
2. DIODES ON OUTPUT OF INVERTERS ARE IN FOR 1
   DIODES ON INPUT OF INVERTERS ARE IN FOR Ø
   SOME DIODES ARE INSTALLED IN PRODUCTION TO FACILITATE CHECKOUT. A CUSTOMER WILL RE-ARRANGE DIODES TO HIS REQUIREMENTS
3. DELAY OUTPUT IS ADJUSTED TO 2 2 S + 50 NS.
4. DIODES AND JUMPERS SHOWN IN DOTTED LINES ARE NOT PUT ON THE BOARD DURING MANUFACTURE. THEY ARE ADDED DURING CHECKOUT AS REQUIRED. SOLID LINE JUMPERS ARE PUT IN WHEN BOARD IS ASSEMBLED.
5. UNLESS OTHER WISE NOTED RESISTANCE IS IN OHMS 1/4W 5%.
6. YA1 JUMPER (ROM ADDRESS) IS ONLY INSTALLED IF THE PROM ADDRESSES OVERLAY CORE MEMORY ADDRESSES.
7. UNLESS OTHER WISE SPECIFIED ALL DELAY TIMES ARE ± 20%.





DEC 1702A	–	12
DEC 5380	1	8
DEC T384	1	8
DEC 74151	8	16
DEC 74123	8	16
DEC 74157	8	16
DEC 74174	8	16
DEC 74200	8	16
IC TYPE	GND	+ 5V

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY. EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

M8349-YA	M8349-YC	M8349-YD	ITEM NO.	QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.
				1	C84	CAP 68 PF 100V 5% DM	1988014	5
				1	C65	.047 CAP.	1009678	6
2	6	3	7	SEE Y VARIATION CHART		IC DEC 1702 A	2304144	7
				1	C88	CAP 1000 PF 100V 5% DM	1988942	8
				1	C57	CAP 30 MF 10V MF S.TANT	1988976	9
				55	C1-C53, C89, C70, C71, C72, C74	CAP .01 MF 100V Z5U DISC	1009610	10
				1	C80	CAP 300 PF 100V 5% DM	1009631	11
				1	C87	CAP 2700 PF 100V 5% DM	1009637	12
				2	C83, C86	CAP 27 PF 100V 5% DM	1009739	13
				6	C54, C55, C56, C58, C59, C73	CAP 6.8 MF 35V 10% S TANT	1985308	14
				1	D15	DIODE D862	1100113	15
				6	D1&, D4, D6, D8, D9, D12.	DIODE D664	1100114	16
				1	D17	DIODE 1N753A	1100880	17
				2		FASTON TABS	9007112	18
				2	R8, R29	RES 100 OHMS 1/4W 5%	1300229	19
				1	R32	RES 220 OHMS 1/4W 5%	1300271	20
				2	R24, R28	RES 470 OHMS 1/4W 5%	1300316	21
				6	R7, R16, R17, R22, R26, R30	RES 1K OHMS 1/4W 5%	1300365	22
				1	R35	RES 1.5K OHMS 1/4W 5%	1300391	23
				1	R31	RES 2 2K OHMS 1/4W 5%	1300417	24
				1	R10	RES 3K OHMS 1/4W 5%	1300432	25
				1	R9	RES 3.3K OHMS 1/4W 5%	1300438	26
				7	R1-R6, R12	RES 4 7K OHMS 1/4W 5%	1300447	27
				3	R19, R21, R23	RES 10K OHMS 1/4W 5%	1300479	28
				2	R20, R37	RES 15K OHMS 1/4W 5%	1300498	29
								30
				2	R25, R26	RES 27 OHMS 1/4W 10%	1301428	31
				1	R27	RES 22K OHMS 1/4W 5%	1301498	32
				1	R33	RES 270 OHMS 1/4W 5%	1301572	33
								34
				2	R33, R34	RES 4.7 OHMS 1W 5%	1304883	35
				2	Q3, Q4	TRANSISTOR 2N3638	1503108	36
				1	Q1	TRANSISTOR 65310	1500338	37
				1	Q2	TRANSISTOR 3762	1500848	38
				2	E29, E58	I.C. DEC 7474	1988547	39
				1	E57	I.C. DEC 7480	1988575	40
				2	E48, E58	I.C. DEC 7402	1988804	41
				1	E12	I.C. DEC 74H00	1900858	42
				1	E13	I.C. DEC 74H10	1900857	43
				2	E9, E52	I.C. DEC 74H11	1988267	44
				7	E14, E31, E44, E45, E47, E56, E61	I.C. DEC 8881	1909705	45
				3	E1, E17, E40	I.C. DEC 74H04	1988831	46
Ø	Ø	Ø	1	SEE Y VARIATION CHART		I.C. DEC 74151	1988826	47
				3	E49, E53, E54	I.C. DEC 7408	1910155	48
				2		EYELETS-(65-4-7)	9006732	49
				5	E34, E52, E3, E5, E8	I.C. DEC 5380 (CAN USE 11580)	1910382 (1911113)	50
3	3	3	6	SEE Y VARIATION CHART		I.C. DEC 5384 (CAN USE 384)	1910394 (1909486)	51
			56			SPLIT LUGS -(4-7)	9006735	52
				3	E21, E30, E36	I.C. DEC 74123	1988436	53
				2	E22, E38	I.C. DEC 74174	1988882	54
				3	W1, W2, W3	BUS WIRE #22 AWG	9107560-01	55

FIRST USED ON OPTION MODEL: MR8-F

PARTS LIST

ETCH BOARD REV: C

DEC NO.	EIA NO.
3762	NONE
6531B	NONE
1N757A	NONE
D664	1N3606
D662	1N645

SEMICONDUCTOR CONVERSION CHART

REV	CHNG NO.	REVISIONS
A	1	ORIGINATED M8349-00008 R. REGAN 2-2-73
B		M8349-00006 R. REGAN 2-27-73
C		M8349-00005 R. REGAN 1-6-75
D		M8349-00004 D. ADAMS 1-3-75
E		M8349-00003 D. ADAMS 12-12-73
F		M8349-00008 D. ADAMS 1-6-75

ORIGINATED: M8349-00008 B

DRWN	R. Regan	DATE 3-1-73
CHK		DATE
ENGR		DATE
MFG		DATE
QA		DATE

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: PROM IK

NEXT HIGHER ASSY: C-UA-MR8-F-Ø

SCALE: NONE

SIZE: D | CODE: DCS | NUMBER: M8349-Ø-1 | REV: F

SHEET 1 OF 7

DEC FORM NO. LMD 1304

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QTY	QTY	QTY	QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.
Ø	Ø	Ø	12	SEE Y VARIATION CHART	I.C. DEC 74200 (3105)	1910818-2	58
			4	E8,E10,E35,E88	I.C. DEC 74157	1910855	57
			1	.082	CAP SUPP 100V 5%	1000025	58
							59
			1	.048	RES. 10K POT 3/4 W 10%	1309143-10	60
			1		HEAT SINK: TRANSISTOR	1210001	61
			REF		X-Y COORDINATE HOLE LOCATION	K-CO-M8349-Ø-4	62
			REF		ASSY/DRILLING HOLE LAYOUT	D-AH-M8349-Ø-5	63
			REF		ECO MODULE HISTORY	B-MH-M8349-Ø-6	64
			1		ETCH CIRCUIT BOARD	5010426	65

M8349-YA / M8349-YC / M8349-YD

Y VARIATION CHART

COMPONENTS	M8349 YA	M8349 YC	M8349 YD	M8349
I.C. DEC 1702A	E26,E50	E26,E32,E38 E42,E50,E55	E26,E32,E50	E20,E26,E32, E38,E42,E50, E55
I.C. DEC 5384	E4,E24,E51	E4,E24,E51	E4,E24,E51	E4,E10,E24, E27,E43,E51
JUMPER YA1 SEE NOTE 6	IN	IN	IN	OUT
JUMPER YA2	IN	IN	IN	OUT
I.C. DEC 74151	O	O	O	E16
I.C. DEC 74200	O	O	O	E2 E7 E11 E15 E19 E23 E25 E28 E33 E37 E41 E46

* DIODE & JUMPER SETTINGS FOR ADDRESS DEFINITIONS

MEMORY FIELD SELECT	DIODE D3	D4	D5	D6	D9	D10
Ø	I	–	I	–	–	I
1	–	I	I	–	–	I
2	I	–	I	–	I	–
3	–	I	I	–	I	–
4	I	–	–	I	–	I
5	–	I	–	I	–	I
6	I	–	–	I	I	–
7	–	I	–	I	I	–

FIRST MEMORY ADDRESS	DIODE D7	D8	D11	D12
0000	–	I	–	I
2000	I	–	–	I
4000	–	I	I	–
6000	I	–	I	–

STARTING MEMORY ADDRESS	JUMPERS BELOW R1	R2	R3
0000	I	I	I
0200	I	I	–
2000	I	–	I
2200	I	–	–
4000	–	I	I
4200	–	I	–
6000	–	–	I
6200	–	–	–

* "I" = DIODE OR JUMPER IN
"–" = DIODE OR JUMPER OUT

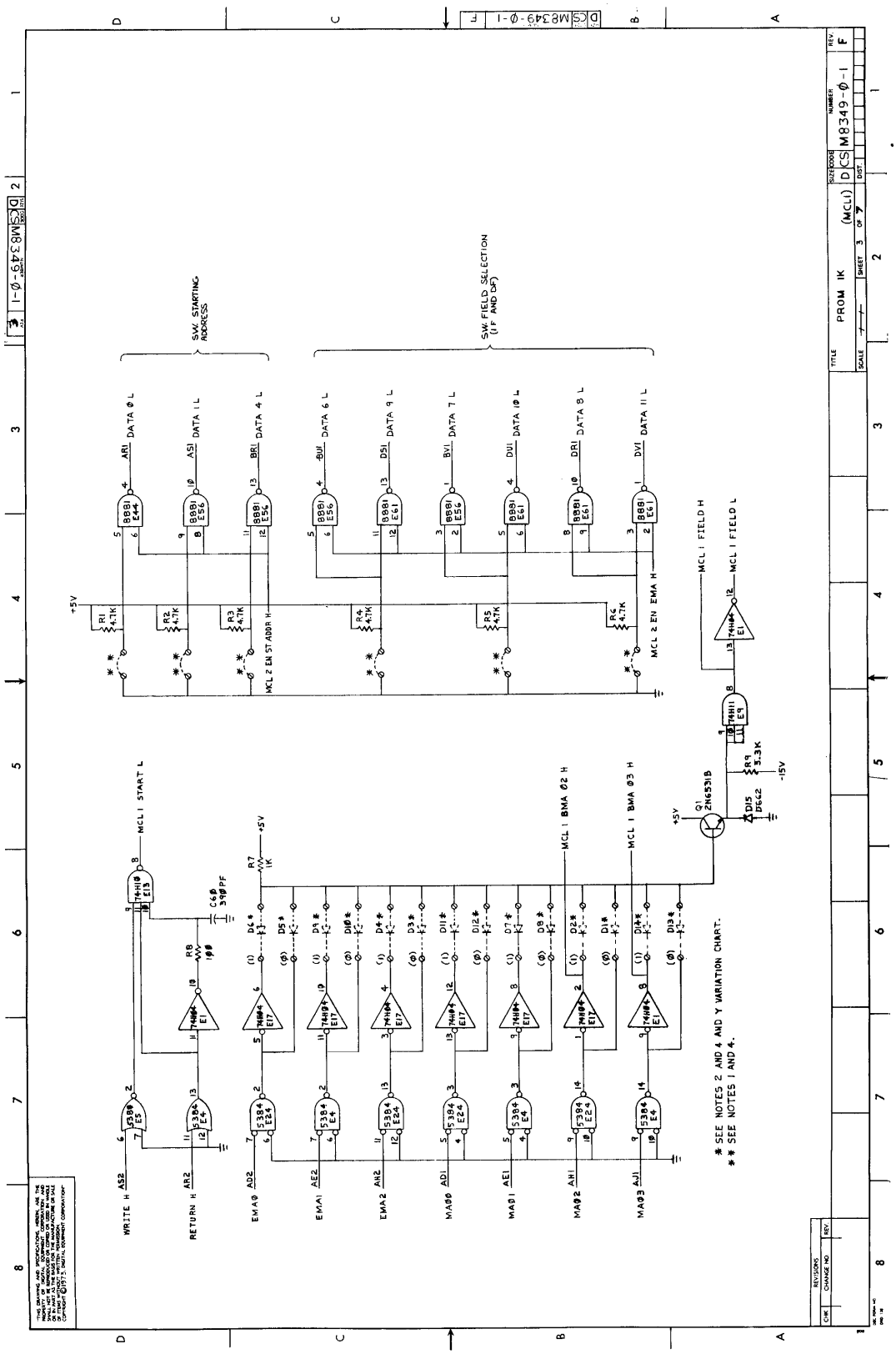
'SW' OR 'BOOT' FIELD SELECT	JUMPER BELOW R4	R5	R6
Ø	I	I	I
1	I	I	–
2	I	–	I
3	I	–	–
4	–	I	I
5	–	I	–
6	–	–	I
7	–	–	–

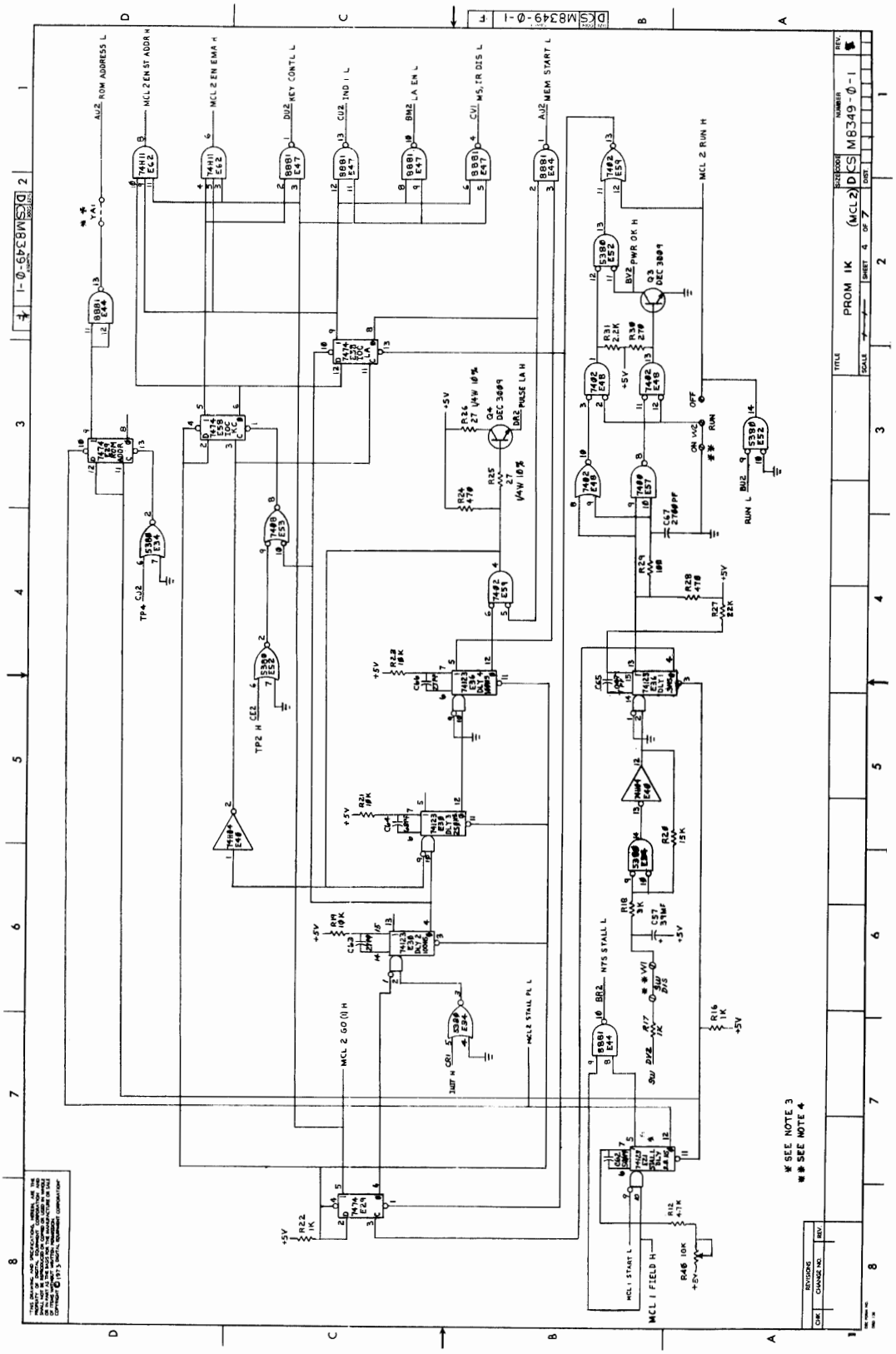
REVISIONS		
CHK	CHANGE NO.	REV

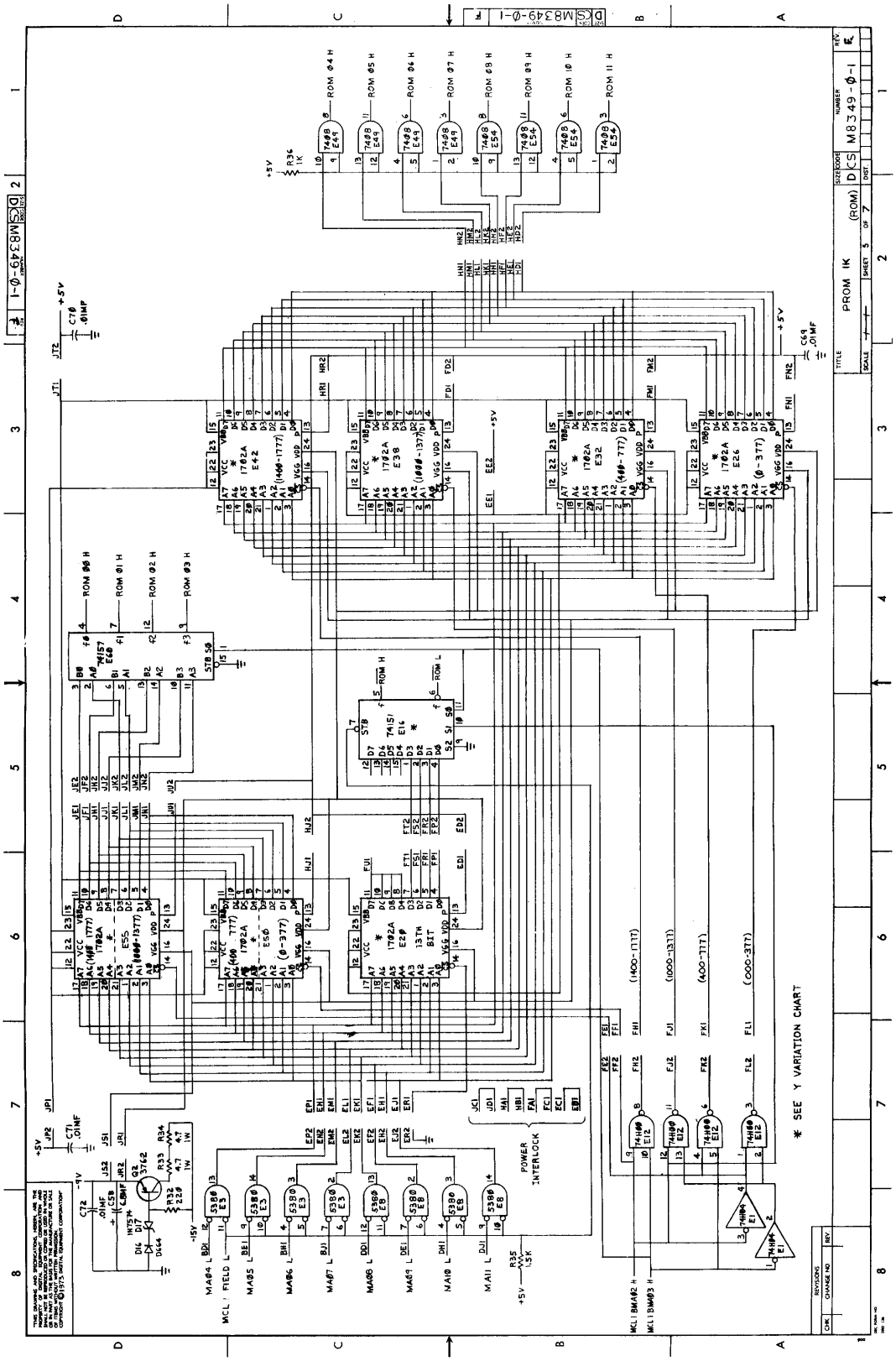
TITLE	SIZE	CODE	NUMBER	REV.
PROM IK	D	CS	M8349-Ø-1	F
SCALE	SHEET 2 OF 7		DIST.	

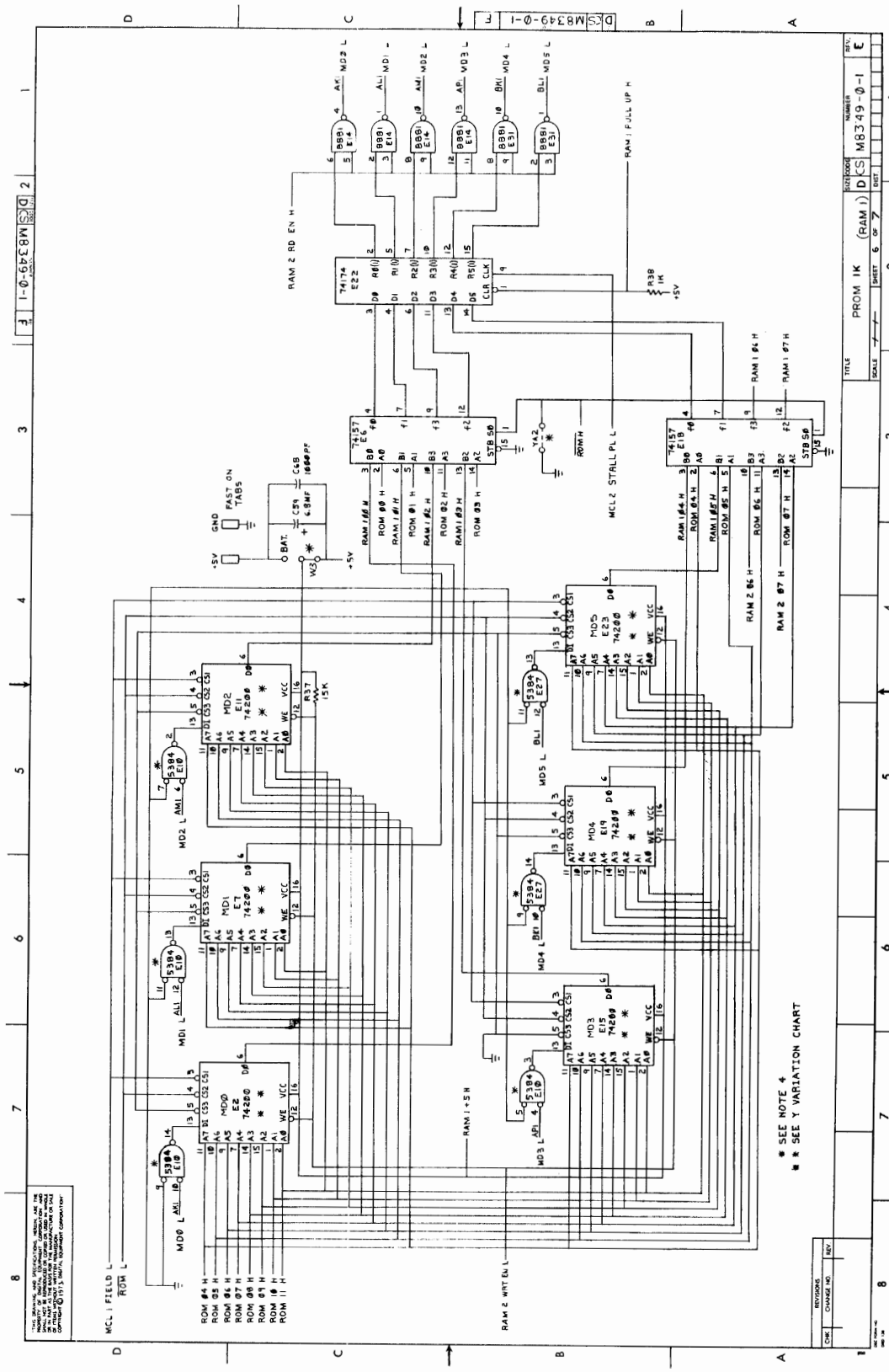
DEC FORM 140 DMD 137

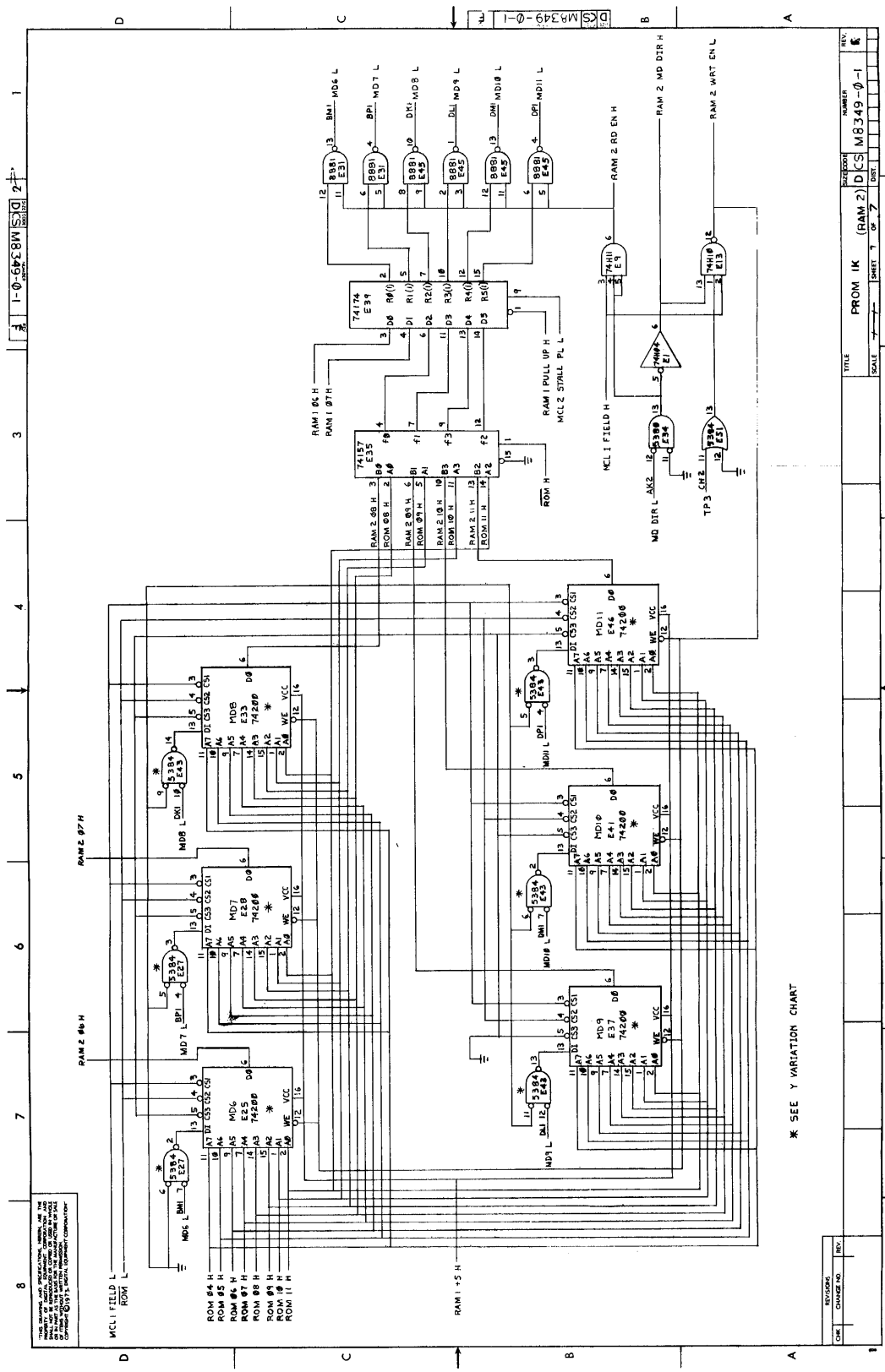
DCS M8349-Ø-1 F

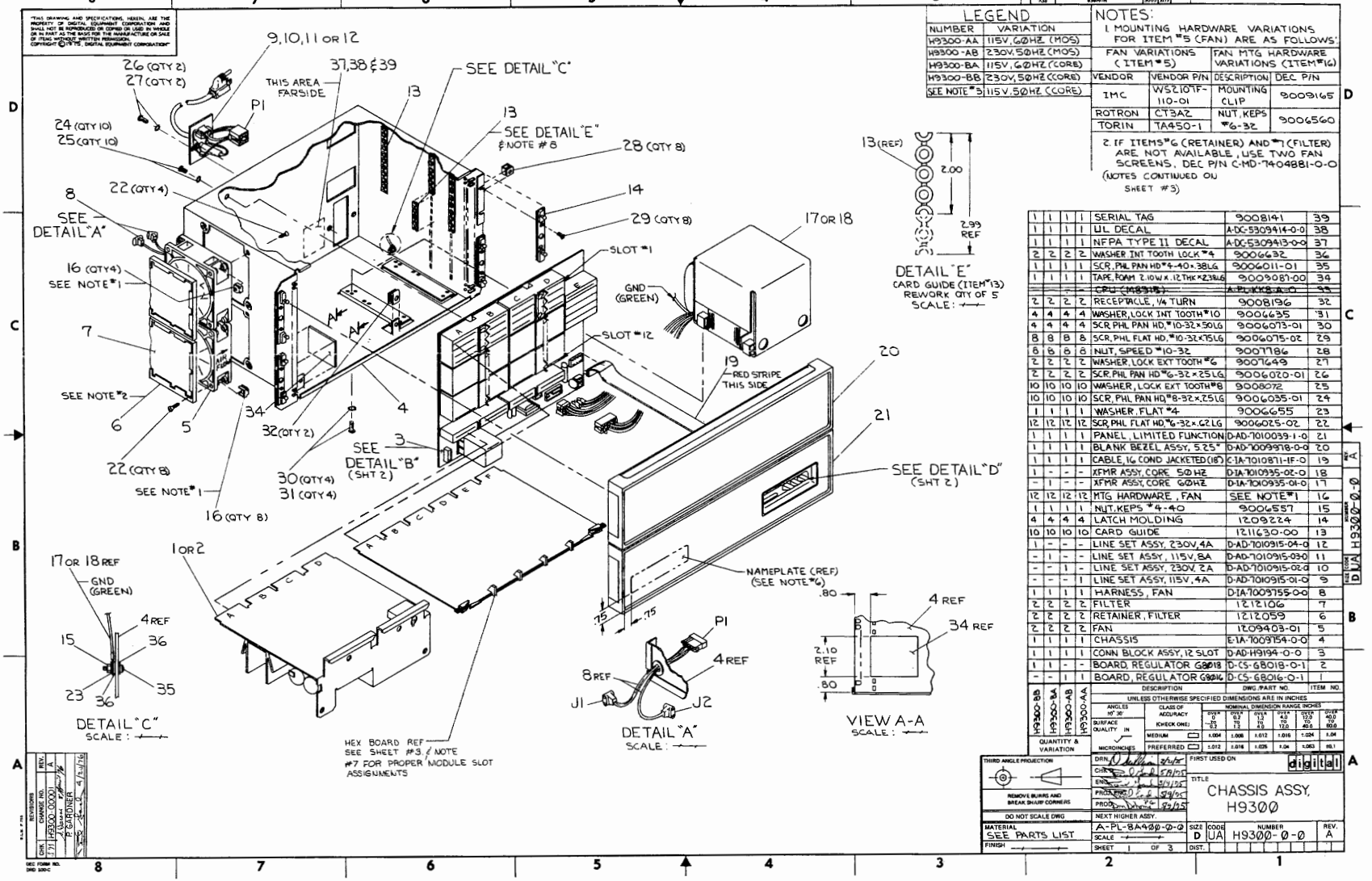

SW. STARTING ADDRESS
SW. FIELD SELECTION (1F AND DF)
DATA Ø L
DATA 1 L
DATA 4 L
DATA 6 L
DATA 9 L
DATA 7 L
DATA 10 L
DATA 8 L
DATA 11 L
MCL 2 EN ST ADDR H
MCL 2 EN EMA H
MCL 1 FIELD H
MCL 1 FIELD L
MCL 1 START L
MCL 1 BMA Ø2 H
MCL 1 BMA Ø3 H
WRITE H AS2
RETURN H AR2
EMAØ AD2
EMA1 AE2
EMA2 AH2
MAØØ AD1
MAØ1 AE1
MAØ2 AH1
MAØ3 AJ1
Q1 2N6531B
D15 D622
* SEE NOTES 2 AND 4 AND Y VARIATION CHART.
** SEE NOTES 1 AND 4.
PROM IK (MCLI)
M8349-Ø-1


PROM 1K (MCL2)
MCL 2 RUN H
MCL 2 GO (1) H
MCL 1 FIELD H
MCL 1 START L
MCL 2 STALL PL L
N75 STALL L
MEM START L
PULSE LA H
PWR OK H
RUN L
ROM ADDRESS L
KEY CONTL L
IND 1 L
LA EN L
MS,TR DIS L
MCL 2 EN ST ADDR H
MCL 2 EN EMA H
* SEE NOTE 3
** SEE NOTE 4


PROM 1K (ROM)
M8349-0-1
* SEE Y VARIATION CHART
POWER INTERLOCK


PROM 1K (RAM 1)
D CS M8349-0-1
* SEE NOTE 4
* * SEE Y VARIATION CHART
MCL 1 FIELD L
ROM L
RAM 2 WRT EN L
RAM 2 RD EN H
RAM 1 FULL UP H
MCL 2 STALL PL L
RAM 1 #4 H
RAM 1 #7 H
RAM 2 #7 H
MD0 L AKI
MD1 L ALI
MD2 L AMI
MD3 L API
MD4 L BKI
MD5 L BLI
MD0 E2
MD1 E7
MD2 E11
MD3 E15
MD4 E19
MD5 E23
74200
74174 E22
74157 E6
74157 E18
5384 E10
5384 E27
8881 E14
8881 E31
STB S0
R37 15K
R38 1K +5V
C68 1000PF
C59 6.8MF
W3
Y42
-5V
GND
FAST ON TABS
BAT.
+5V
ROM 00 H
ROM 01 H
ROM 02 H
ROM 03 H
ROM 04 H
ROM 05 H
ROM 06 H
ROM 07 H
RAM 1 #0 H
RAM 1 #1 H
RAM 1 #2 H
RAM 1 #3 H
RAM 1 #4 H
RAM 1 #5 H
RAM 1 #6 H
RAM 1 #7 H
ROM 04 H
ROM 05 H
ROM 06 H
ROM 07 H
ROM 08 H
ROM 09 H
ROM 10 H
ROM 11 H
REVISIONS
CHK
CHANGE NO.
REV
TITLE
SCALE
SIZE/CODE
NUMBER
SHEET 6 OF 7
DIST
REV. E


PROM IK (RAM 2)
DCS M8349-0-1
* SEE Y VARIATION CHART
RAM 2 MD DIR H
RAM 2 WRT EN L
RAM 2 RD EN H
MCL 1 FIELD H
MD DIR L
RAM 1 PULL UP H
MCL 2 STALL PL L
RAM 1 Ø6 H
RAM 1 Ø7 H
ROM H
RAM 2 Ø7 H
RAM 2 Ø6 H
RAM 1 +5 H
MCL 1 FIELD L
ROM L
MD6 L
MD7 L
MD8 L
MD9 L
MD10 L
MD11 L



LEGEND	
NUMBER	VARIATION
H9300-AA	115V, 60HZ (MOS)
H9300-AB	230V, 50HZ (MOS)
H9300-BA	115V, 60HZ (CORE)
H9300-BB	230V, 50HZ (CORE)
SEE NOTE #5	115V, 50HZ (CORE)

NOTES:

1. MOUNTING HARDWARE VARIATIONS FOR ITEM #5 (FAN) ARE AS FOLLOWS:

FAN VARIATIONS (ITEM #5)		FAN MTG HARDWARE VARIATIONS (ITEM #16)	
VENDOR	VENDOR P/N	DESCRIPTION	DEC P/N
IMC	WS2101F-110-01	MOUNTING CLIP	9009165
ROTRON	CT3A2	NUT, KEPS #6-32	9006560
TORIN	TA450-1		

2. IF ITEMS #6 (RETAINER) AND #7 (FILTER) ARE NOT AVAILABLE, USE TWO FAN SCREENS, DEC P/N CMD-7404881-0-0

(NOTES CONTINUED ON SHEET #3)

1	1	1	1	SERIAL TAG	9008141	39
1	1	1	1	UL DECAL	A-DC-5309414-0-0	38
1	1	1	1	NFPA TYPE 11 DECAL	A-DC-5309413-0-0	37
2	2	2	2	WASHER INT TOOTH LOCK #4	9006632	36
1	1	1	1	SCR, PHL PAN HD #4-40×.38LG	9006011-01	35
1	1	1	1	TAPE, FOAM 2.10W×.12THK×23LG	9009081-00	34
-	-	-	-	CPU (M8318)	A-PL-KA8A-0-0	33
2	2	2	2	RECEPTACLE, 1/4 TURN	9008196	32
4	4	4	4	WASHER, LOCK INT TOOTH #10	9006635	31
4	4	4	4	SCR, PHL PAN HD, #10-32×.50LG	9006073-01	30
8	8	8	8	SCR, PHL FLAT HD, #10-32×.75LG	9006075-02	29
8	8	8	8	NUT, SPEED #10-32	9007786	28
2	2	2	2	WASHER, LOCK EXT TOOTH #6	9007649	27
2	2	2	2	SCR, PHL PAN HD #6-32×.25LG	9006020-01	26
10	10	10	10	WASHER, LOCK EXT TOOTH #8	9008072	25
10	10	10	10	SCR, PHL PAN HD #8-32×.75LG	9006035-01	24
1	1	1	1	WASHER, FLAT #4	9006655	23
12	12	12	12	SCR, PHL FLAT HD, #6-32×.62LG	9006025-02	22
1	1	1	1	PANEL, LIMITED FUNCTION	D-AD-7010039-1-0	21
1	1	1	1	BLANK BEZEL ASSY, 5.25"	D-AD-7009918-0-0	20
1	1	1	1	CABLE, 16 COND JACKETED (18")	C-IA-7010871-1F-0	19
1	-	-	-	XFMR ASSY, CORE, 50 HZ	D-IA-7010935-02-0	18
-	1	-	-	XFMR ASSY, CORE, 60HZ	D-IA-7010935-01-0	17
12	12	12	12	MTG HARDWARE, FAN	SEE NOTE #1	16
1	1	1	1	NUT, KEPS #4-40	9006557	15
4	4	4	4	LATCH MOLDING	12.09224	14
10	10	10	10	CARD GUIDE	12.11630-00	13
1	-	-	-	LINE SET ASSY, 230V, 4A	D-AD-7010915-04-0	12
-	1	-	-	LINE SET ASSY, 115V, 8A	D-AD-7010915-03-0	11
-	-	1	-	LINE SET ASSY, 230V, 2A	D-AD-7010915-02-0	10
-	-	-	1	LINE SET ASSY, 115V, 4A	D-AD-7010915-01-0	9
1	1	1	1	HARNESS, FAN	D-IA-7009155-00-0	8
2	2	2	2	FILTER	12.12106	7
2	2	2	2	RETAINER, FILTER	12.12059	6
2	2	2	2	FAN	12.09403-01	5
1	1	1	1	CHASSIS	E-IA-7009154-0-0	4
1	1	1	1	CONN BLOCK ASSY, 12 SLOT	D-AD-H9194-0-0	3
1	1	-	-	BOARD, REGULATOR G8018	D-CS-68018-0-1	2
-	-	1	1	BOARD, REGULATOR G8016	D-CS-68016-0-1	1
H9300-BB	H9300-AA	H9300-BA	H9300-AB	DESCRIPTION	DWG./PART NO.	ITEM NO.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

QUANTITY & VARIATION	ANGLES ±0° 30'	CLASS OF ACCURACY (CHECK ONE)	NOMINAL DIMENSION RANGE INCHES					
			OVER 0 TO 0.7	OVER 0.7 TO 1.2	OVER 1.2 TO 2.0	OVER 2.0 TO 4.0	OVER 4.0 TO 12.0	OVER 12.0 TO 40.0
	SURFACE QUALITY IN MICROINCHES	MEDIUM	±.004	±.008	±.012	±.016	±.024	±.04
		PREFERRED	±.012	±.016	±.025	±.04	±.063	±0.1

THIRD ANGLE PROJECTION

REMOVE BURRS AND BREAK SHARP CORNERS

DO NOT SCALE DWG

MATERIAL: SEE PARTS LIST

FINISH

DRN. D. Sullivan 8/4/75

CHK. [illegible] 8/19/75

ENGR. [illegible] 8/19/75

PROJ. ENGR. [illegible] 8/19/75

PROD. [illegible] 8/19/75

FIRST USED ON: digital

TITLE: CHASSIS ASSY, H9300

NEXT HIGHER ASSY.: A-PL-8A900-0-0

SIZE: D | CODE: UA | NUMBER: H9300-0-0 | REV.: A

SCALE: | SHEET 1 OF 3 | DIST.

REVISIONS			
DIR.	CHANGE NO.	REV.	
1711	H9300-0000	A	4/24/76

DEC FORM NO. DRD 320-C

H9300-0-0 REV A

FILE CODE D UA

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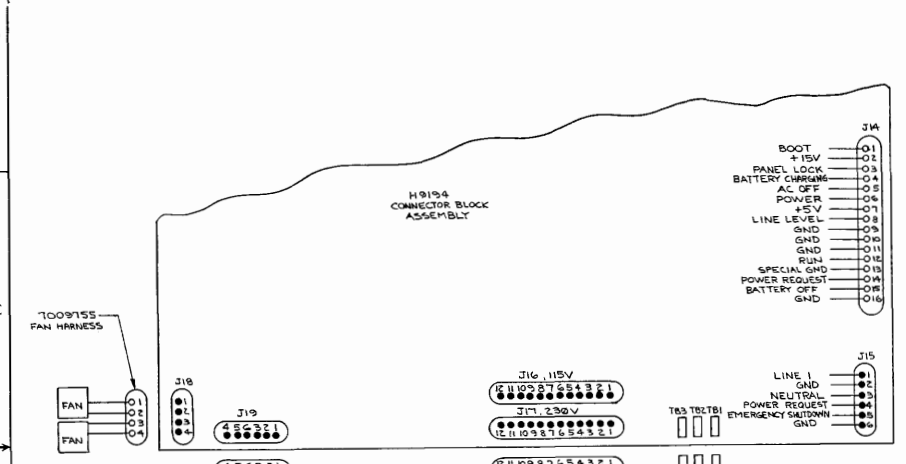

ASSEMBLY INSTRUTIONS

1. OPERATIONS TO BE PERFORMED PER HARDWARE STANDARDS SP-7685099-0 AND/OR DEC WORKMANSHIP STANDARDS.
2. ATTACH FOAM TAPE (ITEM #34) TO CHASSIS (ITEM #4) AS SHOWN IN VIEW A-A.
3. INSTALL FAN HARNESS (ITEM #8) INTO CHASSIS AS SHOWN IN DETAIL "A".
4. ATTACH FILTER RETAINERS (ITEM #6) TO THE TWO FANS (ITEM #5) WITH #6-32 X .62 FLAT HEAD SCREW (ITEM #22) AND THE APPROPRIATE MOUNTING HARDWARE (SEE NOTES #1 & 2) FOUR PLACES EACH FAN.
5. PLUG FAN HARNESS CONNECTORS J1 & J2 (SEE DETAIL "A") ON TO THE FAN TERMINALS.
6. ATTACH FANS TO CHASSIS WITH #6-32 X .62 FLAT HEAD SCREWS (ITEM #22) AND THE APPROPRIATE MOUNTING HARDWARE (SEE NOTE #1) TWO PLACES EACH FAN.
7. REWORK FIVE CARD GUIDES (ITEM #13) AS SHOWN ON DETAIL "E".
8. INSTALL FULL LENGTH CARD GUIDES (ITEM #13) AND REWORKED CARD GUIDES AS SHOWN (10 PLACES).
9. INSTALL THE 1/4 TURN RECEPTACLES (ITEM #32) ON THE TWO TABS ON THE BOTTOM OF THE CHASSIS.
10. ATTACH THE H9194 CONNECTOR BLOCK ASSEMBLY (ITEM #3) TO THE REAR OF THE CHASSIS WITH #8-32 X .25 PAN HEAD SCREWS (ITEM #24) AND #8 EXTERNAL TOOTH LOCK WASHERS (ITEM #25) TEN PLACES.
11. PLUG P1 OF THE FAN HARNESS (4 PIN CONNECTOR) INTO J18 OF THE H9194 (SEE DETAIL "B", SHEET 2)
12. ATTACH THE LINE SET (ITEM #9,10,11 OR 12) TO THE REAR OF THE CHASSIS WITH TWO #6-32 X .25 LG PAN HEAD SCREWS (ITEM #26) AND TWO #6 EXTERNAL TOOTH LOCKWASHERS (ITEM #27) AS SHOWN.
13. PLUG P1 (6 PIN CONNECTOR) OF THE LINE SET INTO J15 OF THE H9194 (SEE.DETAIL "B").
14. PLUG ONE END OF THE 16 CONDUCTOR CABLE (ITEM #19) INTO J14 OF THE H9194 AS SHOWN.
15. SET THE TRANSFORMER ASSEMBLY (ITEM #17 OR 18) IN THE CHASSIS AND FASTEN THE GREEN WIRE TO THE CHASSIS WITH ONE #4-40 X .38 SCREW (ITEM #35) TWO #4 INTERNAL TOOTH LOCK WASHERS (ITEM #36) ONE FLAT WASHER (ITEM #23) AND ONE #4-40 KEP NUT (ITEM #15) AS SHOWN IN DETAIL "C".
16. PLACE THE TRANSFORMER ASSEMBLY IN POSITION (THE 16 CONDUCTOR CABLE SHOULD BE ROUTED UNDERNEATH THE TRANSFORMER) AND ATTACH TO THE CHASSIS WITH FOUR #10-32 X .50 PAN HEAD SCREWS (ITEM #30) AND #10 INTERNAL TOOTH LOCK WASHERS (ITEM #31) AS SHOWN.
17. PLUG P2 OF THE TRANSFORMER ASSEMBLY (12 PIN CONNECTOR) INTO EITHER J16 (115V) OR J17 (230V) OF THE H9194 (SEE DETAIL "B")
18. CONNECT THE THREE LARGE WIRES ON THE TRANSFORMER ASSEMBLY TO THE TABS TB1, TB2 AND TB3 (SEE DETAIL #B) ON THE H9194. THE BLU/BLK WIRE IS ALWAYS CONNECTED TO THE CENTER TAB (TB2).
19. PLUG P1 OF THE TRANSFORMER ASSEMBLY (6 PIN CONNECTOR) INTO J19 OF THE H9194 (SEE DETAIL #B).
20. PLUG THE G8018 REGULATOR BOARD (ITEM #2) INTO THE H9194 AS SHOWN, AND SECURE IN PLACE WITH THE TWO ATTACHED 1/4 TURN FASTENERS.
21. ATTACH THE LATCH HOLDINGS (ITEM #14) TO THE CHASSIS WITH #10-32 X .75 FLAT HEAD SCREWS (ITEM #29) AND SPEED NUTS (ITEM #28).
22. PLUG THE OTHER END OF THE 16 CONDUCTOR CABLE INTO J1 OF THE LIMITED FUNCTION PANEL (ITEM #21) SEE DETAIL #C.
23. ATTACH THE LIMITED FUNCTION PANEL TO THE CHASSIS.
24. ATTACH THE BLANK BEZEL ASSEMBLY (ITEM #20) TO THE CHASSIS.
25. SLIDE FILTERS (ITEM #7) INTO FILTER RETAINERS.

REVISIONS		
CHK	CHANGE NO.	REV

TITLE	SIZE	CODE	NUMBER	REV.
CHASSIS ASSY, H9300	D	UA	H9300-0-0	A
SCALE	SHEET 2 OF 3		DIST.	

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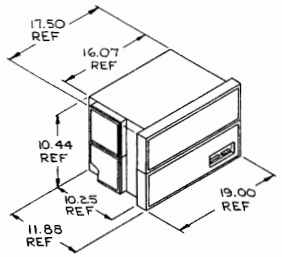
MODULE ASSIGNMENTS AND POWER REQUIREMENTS (SEE NOTES #7/8)

OPTION	DESCRIPTION	BOARD SIZE	NO. SLOTS USED	ASSIGNED SLOT NO.	CURRENT +5V	CURRENT +15V	CURRENT -15V
CRB-F	CARD RDR CONT.	QUAD	1	4 - 12	.55A	—	—
CRB-F	CARD RDR CONT.	↓	↓	4 - 12	.55A	—	—
DBB-EA	INTERPROC. BUFFER			2 - 12	.88A	—	.83A
DKB-EC	RTC, CRYSTAL		1	2 - 12	.34A	—	—
DKB-EP	RTC, PROG.	QUAD	2	2 - 12	1.43A	—	.07A
DKCB-A	OPTION #1	HEX	1	2 - 3	2.0A	.06A	.10A
DPB-EA,-EB	MODEM INTERFACE	QUAD	2	2 - 12	1.08A	.05A	.11A
DRB-EA	DIGITAL I/O	QUAD	1	2 - 12	2.25A	—	—
KAB-E	POSITIVE I/O	QUAD	1	4 - 12	1.48A	—	—
KCB-AA,-AB	PROG. CONSOLE	PNL. MT.	0	N.A.	2.5A	—	—
KDB-E	DATA BREAK	QUAD	1	4 - 12	1.2A	—	—
KGB-EA	REDUNDANCY CHECK	QUAD	1	4 - 12	.94A	—	—
KKB-A	C.P.U.	HEX	1	1	5.0A	—	.84A
KLB-JA	ASYNC. DATA CONT	QUAD	1	2 - 12	1.1A	.05A	.18A
KLB-M	MODEM CONTROL	QUAD	1	2 - 12	.48A	.04A	.84A
KMB-A	OPTION #2	HEX	1	2 - 3	2.0A	—	—
KMB-E	MEM. EXT. & T.S. CONT.	QUAD	1	4 - 12	1.0A	—	—
LEB-II	LINE PRINTER CONT.	QUAD	1	2 - 12	.35A	—	—
LSB-F	LINE PRINTER CONT.	QUAD	1	2 - 12	.48A	—	—
MMB-AA	8K CORE, OPERATING	HEX	2	4 - 8	2.5A	—	—
MMB-AA	8K CORE, STANDBY	HEX	2	4 - 8	2.5A	—	—
MMB-AB	16K CORE, OPERATING	HEX	2	4 - 8	2.5A	—	—
MMB-AB	16K CORE, STANDBY	HEX	2	4 - 8	2.5A	—	—
MRB-AA	1K ROM	QUAD	1	2 - 12	2.0A	—	—
MRB-AB	2K ROM	↓	1	2 - 12	3.0A	—	—
MRB-AC	3K ROM		1	2 - 12	4.0A	—	—
MRB-AD	4K ROM		1	2 - 12	5.0A	—	—
MRB-FB	1K PROM		1	2 - 12	3.0A	—	.35A
MSB-AA	1K RAM		1	4 - 12	1.4A	—	—
MSB-AB	2K RAM		1	4 - 12	2.1A	—	—
MSB-AC	3K RAM		1	4 - 12	2.8A	—	—
MSB-AD	4K RAM		1	4 - 12	3.5A	—	—
PCB-E,PRB-E	RDR/PUNCH CONTROL		1	4 - 12	.84A	—	.85A
RXB-E	RX01 CONTROL		1	4 - 8	1.5 A	—	—
RKB-EA	RK05 CONTROL		3	4 - 12	3.10A	—	—
TAB-AA	TU58 CONTROL		1	2 - 12	2.88A	—	—
TMB-EA,-FA	TU10 CONTROL		4	4 - 12	4.18A	—	—
VCB-E	DISPLAY CONTROL		2	2 - 12	.31A	—	—
VTB-E	DISPLAY CONTROL	↓	3	4 - 12	3.78A	.09A	.13A
XYB-E	PLOTTER CONTROL	QUAD	1	4 - 12	.42A	.01A	.93A
KKB-E	M8300, MAJOR REG.	QUAD	1	12	1.7	—	—
	M8310, MAJOR REG. CONT	QUAD	1	11	.6	—	—
	M8330, TIMING GEN	QUAD	1	10	1.2	—	—
	M8320, BUS LOAD	QUAD	1	1	1.0	1.0	.53

AVAILABLE CURRENT -H9300-AA,AB / -H9300-BA,BB: +5V 20A / 25A; +15 2A ← 1A SHARED → -15V 2A



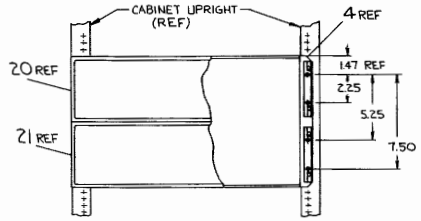
MAX. UNIT WEIGHT = 55 LB.

MOUNTING INSTRUCTIONS

1. SEE DETAIL "D" FOR MTG DIM
2. THE DIM FROM CENTER LINE OF RIGHT CAB UPRIGHT MOUNTING HOLE TO LEFT CAB UPRIGHT MOUNTING HOLE CENTER LINE IS 18.31.
3. REMOVE THE BLANK BEZEL ASSY.
4. REMOVE THE LIMITED FUNCTION PANEL AND DISCONNECT THE CABLE FROM THE LIMITED FUNCTION BD.
5. REMOVE THE LATCH MOULDING (4 PLACES).
6. REMOVE THE SPEED NUT, AND INSTALL ON CABINET POST, 8 PLACES PER MOUNTING DIMENSIONS.
7. IT MAY BE NECESSARY TO REMOVE THE FILTER RETAINER AND THE FILTER IN ORDER TO MOUNT THE BOX IN A CABINET
8. WITH THE BOX IN PLACE, IN THE CABINET, REPLACE THE LATCH MOLDING AND SPACERS SO AS TO SECURE THE BOX TO THE CABINET.
9. PLUG THE CABLE INTO THE LIMITED FUNCTION BD AND REPLACE LIMITED FUNCTION PANEL.
10. REPLACE THE BLANK BEZEL ASSY; REINSTALL THE FILTER RETAINER AND THE FILTER.

NOTES:

3. TO CREATE A 115V 50 HZ CORE VARIATION USE THE H9300-BB REPLACE THE LINE SET (ITEM #12) WITH A 115V 50HZ 8A LINE SET (DEC P/N 0-AD-7910915-03) AND PLUG P2 (12 PIN CONN) OF THE TRANSFORMER ASSEMBLY, INTO J16 (115V) OF THE H9194
4. ALL H9300 POWER SUPPLY DC OUTPUTS ARE PROVIDED TO DRIVE LOGIC INTERNAL TO THE BASIC MACHINE ENCLOSURE. DIGITAL WILL NOT BE RESPONSIBLE FOR THE PERFORMANCE OF THE H9300 IF ANY DC POWER IS TAKEN OUTSIDE THE MACHINE.
5. ENVIRONMENTAL CONDITIONS FOR H9300 ARE SPECIFIED IN DEC STD 102 CLASS "C" ENVIRONMENT.
6. THIS ITEM (NAMEPLATE) IS SHOWN FOR REFERENCE ONLY. IT WILL BE ADDED ON A HIGHER LEVEL ASSEMBLY.
7. INSTALL MODULES AS FOLLOWS:
   PLACEMENT OF HEX MODULES IS FROM SLOT #1 (TOP OF BACKPLANE) DOWN ↓
   PLACEMENT OF QUAD MODULES IS FROM SLOT #12 (BOTTOM OF BACKPLANE) UP ↑
8. CARD GUIDES (ITEM #13) ARE PROVIDED FOR SLOTS #1-10. WHEN A QUAD MODULE WITH AN H851, OR H8511, CONNECTOR BLOCK (MRB-A, MSB-A, ETC) ON THE "E" SET OF FINGERS IS INSTALLED, IT IS NESSESARY TO CLIP OFF THE FRONT-LEFT CARD GUIDE IN THOSE SLOTS SO THAT THE CONNECTOR BLOCK MAY BE PROPERLY SEATED (REF DETAIL "E" FOR AN EXAMPLE OF CARD GUIDE REWORK).



DETAIL "D"
SCALE: —

REVISIONS		
CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV.
CHASSIS ASSY, H9300	D	UA	H9300-0-0	A
SCALE —	SHEET 3 OF 3		DIST.	

H-78

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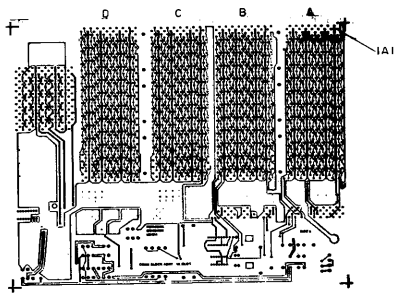
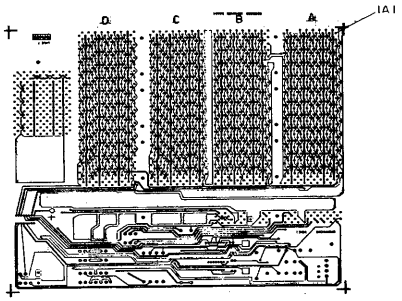
NOTES:



SOLDER SIDE
(SIDE 2)



BLOCK SIDE
(SIDE 1)
AS SEEN THRU SIDE 2

REF			
REF		X-Y- COORDINATE HOLE LOCATION	K-CO-H9194-0-4	1
REF		ASSY/DRILLING HOLE LAYOUT	E-AH-H9194-0-5	2
REF		MODULE ECO HISTORY	B-MH-H9194-0-6	3
REF		ETCHED CIRCUIT BOARD	5041505	4
REF		CONNECTOR BLOCK ASSY	D-AD-H9194-0-0	5

QTY	REF. DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

FIRST USED ON OPTION MODEL: PDP8A

ETCH BOARD REV. B

IC TYPE	GND	+5V
GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE		

IC PIN LOCATIONS

REV.	CHANGE NO.	CHK
B	RETRACING	
C	ORIGINATED	

DRN Robert Hyman 3-3-75
CHK'D Robert Hyman 3-5-75
ENGR'G [illegible] 3/4/75
PROJECT [illegible] 3/4/75
PROD. [illegible] 3/4/75
NEXT HIGHER ASSY H9300
SCALE
SHEET 1 OF 2

digital

TITLE: CONNECTOR BLOCK ASSY

SIZE D | CODE CS | NUMBER H9194-0-1 | REV. C

DIST.

SEMICONDUCTOR CONVERSION CHART

DEC NO.	EIA NO.	DEC NO.	EIA NO.

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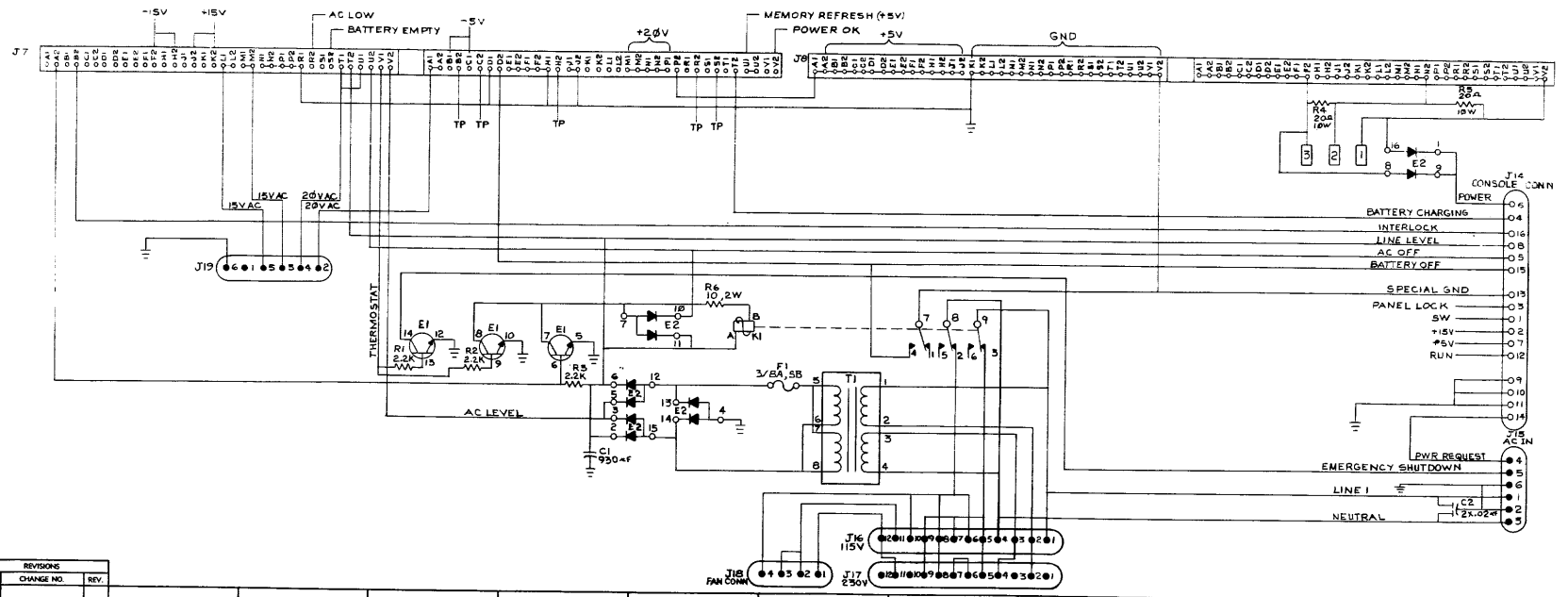
PIN	A1	A2	B1	B2	C1	C2	D1	D2	E1	E2
A	AØ1=+5V ALL OTHERS=TP	+5V	BØ2≠BØ3=BATTERY EMPTY, ALL OTHERS=TP	+5V	CØ1=+5V ALL OUTHERS=TP	+5V	DØ2≠DØ3=PANEL LOCK, ALL OTHERS=TP	+15V	TEST POINT	+2ØV
B	TEST POINT	-15V	BØ2≠BØ3=AC LOW, ALL OTHERS=TP	-15V	TEST POINT	-15V	TEST POINT	-15V	TEST POINT	UNUSED
C	GROUND	GROUND	GROUND	GROUND	GROUND	GROUND	GROUND	GROUND	GROUND	GROUND
D	MAØ L	EMAØ L	MA4 L	INT STROBE H	I/O PAUSE L	TP1 H	MA8 L	IRØ L	TEST POINT	UNUSED
E	MA1 L	EMA1 L	MA5 L	BREAK IN PROG L	CØ L	TP2 H	MA9 L	IR1 L	TEST POINT	+2ØV
F	GROUND	GROUND	GROUND	GROUND	GROUND	GROUND	GROUND	GROUND	GROUND	GROUND
H	MA2 L	EMA2 L	MA6 L	NA, MS LOAD CONT L	C1 L	TP3 H	MAIØ L	IR2 L	TEST POINT	MEMORY REFRESH
J	MA3 L	MEM START L	MA7 L	OVERFLOW L	C2 L	TP4 H	MA11 L	F L	TEST POINT	MEMORY REFRESH
K	MDØ L	MD DIR L	MD4 L	BREAK DATA CONT L	BUS STROBE H	TS1 L	MD8 L	D L	TEST POINT	+2ØV
L	MD1 L	SOURCE H	MD5 L	BREAK CYCLE L	INTERNAL I/O L	TS2 L	MD9 L	E L	TEST POINT	UNUSED
M	MD2 L	STROBE H	MD6 L	LOAD ADD ENABLE L	NOT LAST XFER L	TS3 L	MDIØ L	USE MODE L	TEST POINT	-5V
N	GROUND	GROUND	GROUND	GROUND	GROUND	GROUND	GROUND	GROUND	GROUND	GROUND
P	MD3 L	INHIBIT H	MD7 L	INT IN PROG H	INT REQUEST L	TS4 L	MD11 L	F SET L	TEST POINT	+2ØV
R	DATA ØL	RETURN H	DATA 4 L	NTS STALL L	INITIALIZE H	LINK DATA L	DATA 8 L	PULSE LAH	TEST POINT	UNUSED
S	DATA 1 L	WRITE H	DATA 5 L	RES	SKIP L	LINK LOAD L	DATA 9 L	STOP L	UNUSED	UNUSED
T	GROUND	GROUND	GROUND	GROUND	GROUND	GROUND	GROUND	GROUND	JUMPER	GROUND
U	DATA 2 L	ROM ADDRESS L	DATA 6 L	RUN L	CPMA DISABLE L	IND 1 L	DATA IØ L	KEY CONTROL L		UNUSED
V	DATA 3 L	LINK L	DATA 7 L	POWER OK H	MS. IP DISABLE L	IND 2 L	DATA 11 L	SW	UNUSED	UNUSED



REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
CONN BLOCK ASSY	D	CS	H9194-Ø-1	C
SCALE -/-	SHEET 2 OF 2	DIST.		

H-80

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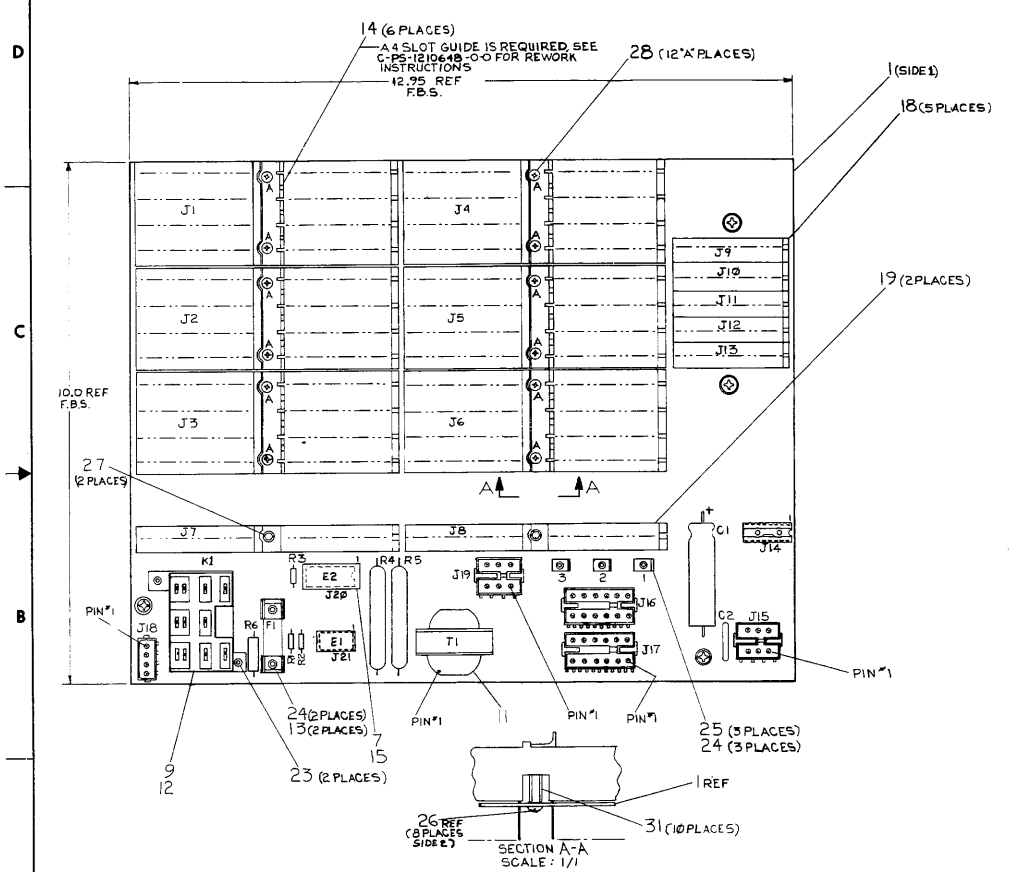

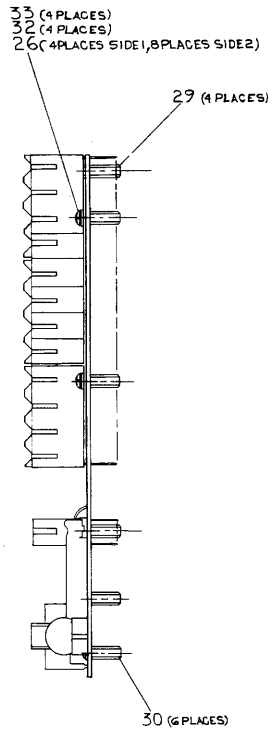

REF				
REF		"OMNIBUS" SPEC	A-SP-OMNIB-US	39
REF		MODULE ECO HISTORY	B-MH-H9194-0-6	38
REF		ASSY/DRILLING HOLE LAYOUT	D-AH-H9194-0-5	37
REF		X-Y COORDINATE HOLE LOCATION	K-CO-H9194-0-4	36
REF		CIRCUIT SCHEMATIC	D-CS-H9194-0-1	35
A/R		WIRE, 24 AWG. GREEN	9107688-55	34
4		WASHER, FLAT #8	9006660	33
4		WASHER, INTL TOOTH #8	9006634	32
10		SPACER, #8-32x.25AFx.56	9009602	31
6		SPACER, #8-32x.25AFx.62	9009629	30
4		SPACER, #8-32x.25AFx1.25	9009603	29
12		SCR, SLFTPG #8-32x.81	9009070	28
2		SCR, SOC. HD #8-32x1.25	9008471	27
12		SCR, PHL PAN HD #8-32x.25	9006035-01	26
3		TERMINAL, SINGLE MALE TAB	9008219	25
5		EYELET	9009000	24
2		EYELET	9006746	23
1	J18	CONN, P.C.. .4 PIN	1211342-04	22
2	J15 J19	CONN, PC 6 PIN	1211342-06	21
2	J16 J17	CONN, PC . 12 PIN	1211342-12	20
2	J7, J8	CONN BLK, 72 PIN SLTD	1211425	19
5	J9 → J13	CONN BLK, 36 PIN SLTD	1211029	18
6	J1 → J6	CONN BLK, 288 PIN SLTD	1210258	17
1	J21	SOCKET, IC, 14 PIN	1211813-01	16
2	J14, J20	SOCKET, IC, 16 PIN	1211813-02	15
6		CARD GUIDE, CENTER	1210698	14
2		CLIP, FUSE	9007203	13
1		SOCKET, RELAY	1210684	12
1	T1	TRANSFORMER	1611646	11
1	F1	FUSE, 3/8 A, S.B	9007207	10
1	K1	RELAY, 3 POLE, 6V, 10 AMP	1210683-01	9
1	E1	QUAD CORE DRIVER 4011	1511102	8
1	E2	DIODE ARRAY	C-1A-7010866-0-0	7
1	R6	RES. 10 Ω, 2W, 10 %	1300172	6
2	R4, R5	RES. 20 Ω, 1ØW, 1 %	1305416	5
3	R1, R2, R3	RES, 2.2K 1/4W, 5 %	1300417	4
1	C2	CAP. .02 µf, 1000V, DUAL DISC	1010767	3
1	C1	CAP. 930 µf, 30V	1010509-00	2
1		ETCHED CIRCUIT BOARD	50115Ø5	1

REF DES	DESCRIPTION	DWG./PART NO.	ITEM NO.

QUANTITY & VARIATION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

ANGLES ± 30'	CLASS OF ACCURACY (CHECK ONE)	NOMINAL DIMENSION RANGE INCHES					
		OVER 0 TO 0.3	OVER .3 TO 1.2	OVER 1.2 TO 4.0	OVER 4.0 TO 12.0	OVER 12.0 TO 40.0	OVER 40.0 TO 80.0
SURFACE QUALITY IN MICRONINCHES	MEDIUM	±.004	±.008	±.012	±.016	±.024	±.04
	PREFERRED	±.012	±.016	±.025	±.04	±.063	±0.1

THIRD ANGLE PROJECTION

REMOVE BURRS AND BREAK SHARP CORNERS

DO NOT SCALE DWG.

DRN	1/28/75
CHK	2-8-75
ENG	2-21-75
PROJ ENG	2-27-75
PROD	3-27-75
NEXT HIGHER ASSY.	
MATERIAL	6-DD-H9194-0
SCALE	1/1
SHEET	1 OF 1
FIRST USED ON	H9300
TITLE	CONNECTOR BLOCK ASS'Y
SIZE	D
CODE	DAD
NUMBER	H9194-0-0
REV.	C
DIST.	

digital

REVISIONS		
DIR.	CHANGE NO.	REV.
H9194-00001		C

DEC FORM NO. DRD 100-C

8 7 6 5 4 3 2 1

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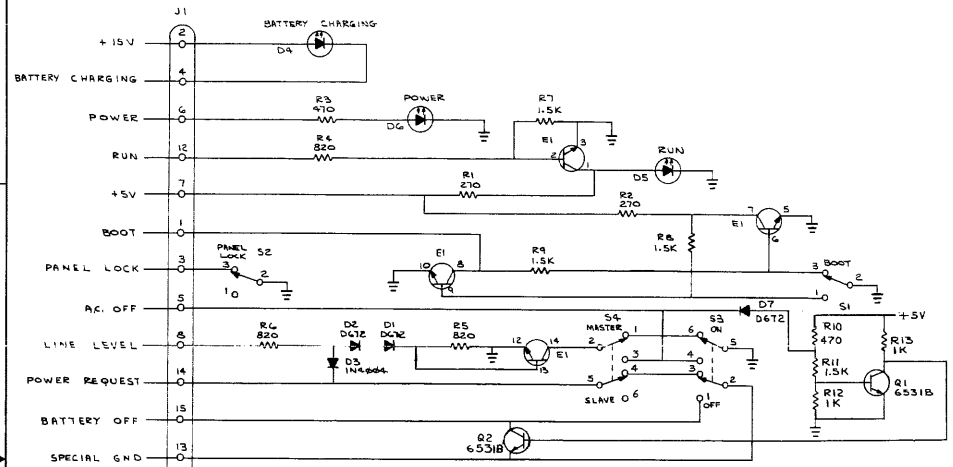
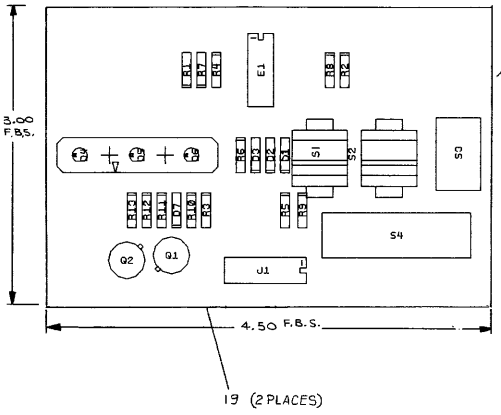
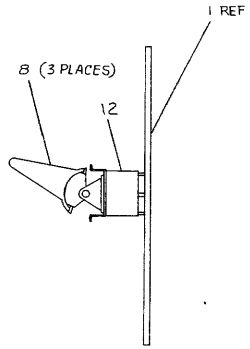
NOTES:







IC TYPE	GND	+5V

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

REF			
REF		X-Y COORDINATE HOLE LOCATION	K-CO-5411507-0-1
REF		ASSY/DRILLING HOLE LAYOUT	D-AH-5411507-0-1
REF		MODULE ECO HISTORY	B-MH-5411507-0-1
1		ETCHED CIRCUIT BOARD	5011506
3	D1, D2, D7	DIODE, D6T2	1105275
1	D3	DIODE, 1N4004	1105796
3	D4, D5, D6	DIODE, LIGHT EMITTING	1110324
3		KNOB, DARK GRAY (#47)	1210786-01
2	S1, S2	SWITCH, TOGGLE, SP.D.T.	1210840
1	S4	SWITCH, SLIDE, DP.S.T.	1210919
1	LH1	LED HOLDER, TRIPLE	1210940-02
1	S3	SWITCH, TOGGLE, D.P.D.T	1212010
2	R3, R10	RES. 470, ¼W 5%	1300316
4	R7, R8, R9, R11	RES. 1.5K, ¼W 5%	1300391
3	R4, R5, R6	RES 820, ¼W, 5%	1301775
2	R1, R2	RES 270, ¼W, 5%	1301972
1	E1	QUAD CORE DRIVER, 4011	1511102-00
1	J1	SOCKET, 16 PIN	1211813-02
2		SCR, SLOTTED PAN HD, SELF TAP #6-.25	9008230-01
2	R12, R13	RES. 1K, ¼W 5%	1300365
2	Q1, Q2	TRAN. DEC 6531B	1509338

QTY	REF. DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

FIRST USED ON OPTION MODEL: H9300

ETCH BOARD REV. B

REV	CHANGE NO.	CHK	REVISIONS
C	5011507-00003	P. GARDNER	2/17/76
B	5411507-00002	P. GARDNER	12-29-75
A	5411507-00001	R. LANDNER	6-2-75

DEC NO.	EIA NO.	DEC NO.	EIA NO.

SEMICONDUCTOR CONVERSION CHART

DRN.	K. Davis	DATE 1-27-75
CHKD.	Robert Hayward	DATE 1-29-75
ENG.		DATE 2-20-75
REQ. ENG.		DATE 2-27-75
PROG.		DATE 3-3-75
NEXT HIGHER ASSY	D-AD-7810033-0-0	
SCALE		
SHEET	1 OF 1	

digital

TITLE: LIMITED FUNCTION BOARD

SIZE D | CODE CS | NUMBER 5411507-0-1 | REV. C

DIST.

5411507-0-1

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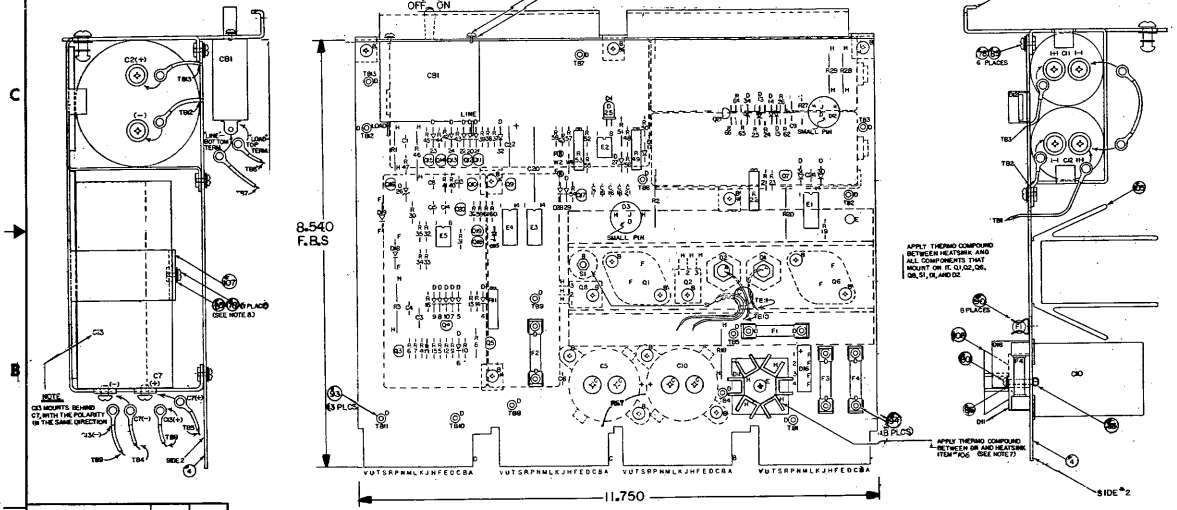
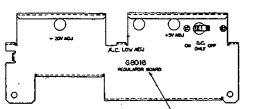
NOTES:
1. * INDICATES HOLES OFF GRID (4 PLACES)
2. ALL COMPONENTS SHOWN BY BROKEN LINES MOUNT ON SIDE *2
3. S1 MOUNTS WITH ITEMS *84 & *88 (1 PLACE)
4. FOR 50HZ OPERATION REMOVE W1 AND INSERT W2 BUSS WIRE, 22 AWG, PART NO. 9107560-01
5. Q1,Q2,Q6 & Q8 MOUNT WITH ITEMS *82,*84, & *88
6. C5 & C10 MOUNT WITH ITEMS *102,*79,*84, 85 & *113
7. PLACE ITEM *89 BETWEEN D11 AND PC BOARD SECURE WITH ITEMS *80 *83 & *86. (1 PLACE)
8. C7 & C13 ARE HELD IN PLACE WITH ITEM *107 (CAPACITOR CLAMP) AND SECURED WITH ITEMS *78 & *85
9. REFER TO PARTS LIST FOR IDENTIFICATION OF ALL NUMBERED ITEMS
10. D1 & D2 TORQUE TO 20 LB-INS
Q1 & Q6 TORQUE TO 14 LB-INS
Q2 Q8 & S1 TORQUE TO 10 LB-INS

WIRE TABLE

PART NO.	FROM	TO	TERMINATION	WIRE LENGTH
9-07380-00	TB1	C5(+)END	SOLDER WIRE AT TB1 END. ATTACH SOLDERLESS CONNECTOR(90-07380) AT C5(+) END.	7
9-07380-00	TB2	C13(-)END	SOLDER WIRE AT TB2 END. ATTACH SOLDERLESS CONNECTOR(90-07380) AT C13(-) END.	1 1/4
9-07380-22	TB3	C13(+)END	SOLDER WIRE AT TB3 END. ATTACH SOLDERLESS CONNECTOR(90-07380) AT C13(+) END.	1 1/4
9-07380-00	TB4	C7(-)END	SOLDER WIRE AT TB4 END. ATTACH SOLDERLESS CONNECTOR(90-07380) AT C7(-) END.	8 1/2
9-07380-22	TB5	C7(+)END	SOLDER WIRE AT TB5 END. ATTACH SOLDERLESS CONNECTOR(90-07380) AT C7(+) END.	7 1/2
9-07380-22	TB6	CR1(LOAD) TERMINAL	SOLDER WIRE AT TB6 END. ATTACH SOLDERLESS CONNECTOR(90-07380) AT CR1 LOAD TERMINAL	6
9-07380-22	TB7	CR1 (LINE) TERMINAL	SOLDER WIRE AT TB7 END. ATTACH SOLDERLESS CONNECTOR(90-07380) AT CR1 LINE TERMINAL	4 1/2
9-07380-00	TB8	CR1(+)END	SOLDER WIRE AT TB8 END. ATTACH SOLDERLESS CONNECTOR(90-07380) AT CR1(+) END.	1 1/2
9-07380-22	TB9	C2(-)END	SOLDER WIRE AT TB9 END. ATTACH SOLDERLESS CONNECTOR(90-07380) AT C2(-) END.	2 1/2
9-07350-22	S1	P.C. BOARD AS SHOWN BELOW		6"

PART NO.	FROM	TO	TERMINATION	WIRE LENGTH
9-07380-22	TB10	D2	SOLDER WIRE AT TB10 END. SOLDER WIRE AT D2 END.	8 3/8
9-07380-22	TB11	D1	SOLDER WIRE AT TB11 END.	10
9-07380-00	TB12	C2(+)END	SOLDER WIRE AT TB12 END. ATTACH SOLDERLESS CONNECTOR (90-07380) AT C2(-) END.	1 1/4
9-07380-22	TB13	C2(+)END	SOLDER WIRE AT TB13 END. ATTACH SOLDERLESS CONNECTOR (90-07380) AT C2(+) END.	1 1/4
9-07560-05	CR1(-) END	C2(-) END	ATTACH SOLDERLESS CONNECTOR AND WIRE TO CR1(-)END. ATTACH SOLDERLESS CONNECTOR(90-07380) AT C2(-) END.	7/8





QTY	REF. DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.
REF		X-Y COORDINATE HOLE LOCATION	2-CO-G8818-A4	1
REF		DRILLING HOLE LAYOUT	5-NC-G8818-0-5	2
REF		MODULE ECO HISTORY	5-NC-G8818-0-6	3
1		ETCHED CIRCUIT BOARD	5011494	4
2	C3,C9	CAP .1uf 100V 80%/0	1000030	5
1	C80	CAP .47 uf 100V 10 %/0	1000090	6
9	C4,C14,C15,C16,C17 C18, C19, C21, C24	CAP .01uf 100V 80%/0	1001610-01	7
1	C7	CAP 18,000 uf 40V -10%TO+75%	1009966	8
8	C11, C12	CAP 10,800 uf 80V -10%TO+100%	1010185	9
1	C13	CAP 18,000 uf 10V -10%TO+100%	1010197	10
2	C1, C6	CAP .12 uf 50V -20%TO+80%	1012274	11
1	C10	CAP 4500 uf 85V -10%TO+75%	1010703	12
1	C5	CAP 6000 uf 10V -10%TO+75%	1010704	13
1	C2	CAP, 1.1F, 10V -10% TO +75%	1011578	14
2	C8, C23	CAP 680 PF 100 V .5 %/0	1000826	15
1	C22	CAP 39 uf 10 V 10 %/0	1000076	16
5	D5, D6, D7, D8, D9	DIODE 0662	1100113	17
1	D14	DIODE IN7584 10V 5 %/0	1100185	18
1	D10	DIODE 57V12R SCREENED	1111203	19
1	D26	DIODE IN4732 4.7 V 5 %/0	1103718	20
1	D13	DIODE IN9698 18V 5 %/0	1109988	21
1	D16	DIODE MDA970-3 200V	1100908	22
1	DS5	DIODE LED MV5054-1	1110326	23
1	D11	DIODE MSS8518 800V	1110714	24
2	D18, D19	DIODE ME752	1110615	25
1	D15	DIODE IN759A 12V 5 %/0	1110836	26
1	D27,	DIODE IN5314 5.1V 5 %/0	1110994	27
2	D1, D2	DIODE IN1183	1111609	28
2	R7, R25	RES 47 1/4 W 5%/0	1300202	29
2	R8, R17	RES 100 1/4 W 5 %/0	1300229	30
1	R1,	RES 100 1 W 5 %/0	1300232	31
1	R6.	RES 150 1/4 W 5 %/0	1300250	32
2	R5, R19	RES 220 1/4 W 5 %/0	1300271	33
6	R13, R15, R43, R54, R60, R61	RES 330 1/4 W 5 %/0	1300295	34
1	R51	RES 330 1/2 W 5 %/0	1300296	35
1	R29	RES 390 1/4 W 5 %/0	1300309	36
2	R28, R39	RES 470 1/4 W 5 %/0	1300319	37

PARTS LIST

IC TYPE	GND	+5V
GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE		

IC PIN LOCATIONS

DEC NO.	ECA NO.	DEC NO.	ECA NO.

SEMICONDUCTOR CONVERSION CHART

REV.	DESCRIPTION	DATE	APPROVED
J	ECO G8818-00005	6-18-74	W. DASH
H	ECO G8818-00004	1-14-74	A. DELUCA
F	ECO G8818-00003	7-9-75	A. DELUCA
E	ECO G8818-00002	2-21-75	A. DELUCA
D	ECO G8818-00001	5-13-75	A. DELUCA
C	ECO G8818-00000	5-30-75	A. DELUCA
B	ECO G8818-00000	7-9-75	A. DELUCA
A	ECO G8818-00000	7-9-75	A. DELUCA

FIRST USED ON OPTION MODEL

ETCH BOARD REV. D

NEXT HIGHER ASSY

SCALE

SHEET 1 OF 1

digital

TITLE: REGULATOR BOARD 8A CORE

SIZE D | CODE | NUMBER DCS G8818-0-1 | REV. J

DIST.

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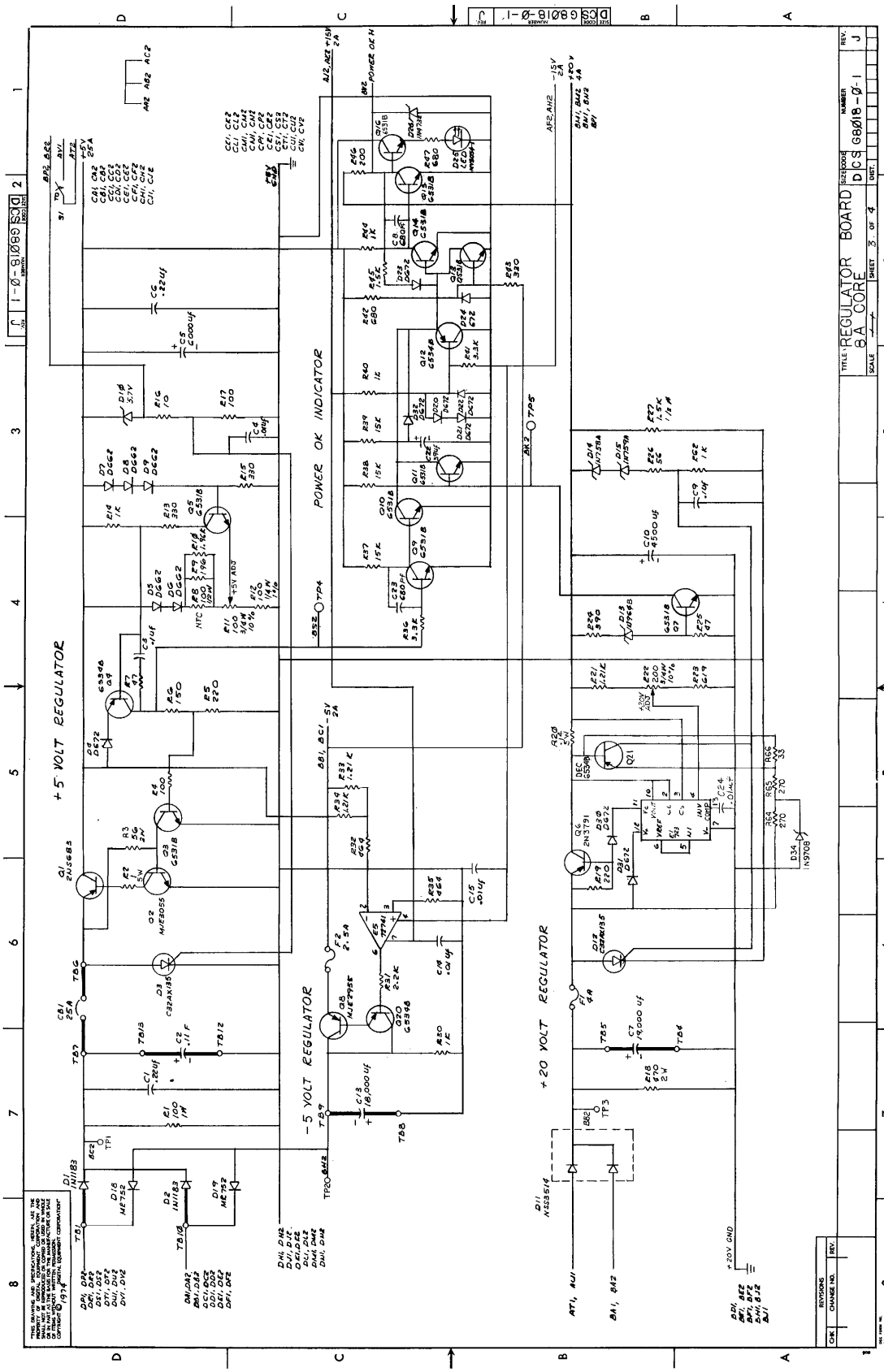
QTY	REF DESIGNATION	DESCRIPTION	PART NO	NEW NO
				81
6		SCREW 6-32 X .56	9007793-1	82
1		KEPNUT 8-38	9006963	83
11		KEPNUT 6-32	9008185	84
13		WASHER #6 INTERNAL	9006688	85
1		WASHER #8 INTERNAL	9006634	86
				87
13		WASHER #6 FLAT	9006656	88
1		WASHER #8 FLAT NYLON(NHM)	9006713-00	89
8		FUSE CLIPS	9007203	90
1	F1	FUSE 4A	9007219	91
3	F2, F3, F4	FUSE 2.6A	9008387	92
13	TB1-TB13	EYELET 654-3	9007836	93
8		EYELET	9009000	94
A/R	W1	WIRE JUMPER	9009185	95
A/R		WIRE #22 AWG	9107380-22	96
A/R		WIRE #18 AWG (BLK)	9107380-00	97
A/R		WIRE #18 AWG (RED)	9107380-22	98
1	R22	RES 200 3/4 W 10%	1309143-05	99
A/R		WIRE BUSS #14 AWG	9107550-05	101
2		BRACKET	1210978	102
1	CB1	CIRCUIT BREAKER	1211673	103
1	S1	THERMOSTAT	1211682	104
1		HEAT SINK T-05 (TRANS MOUNTED)	1212322	105
1		HEAT SINK (BRIDGE RECT) 695-148	1210907	106
1		CLAMP CAP	7413208	107
1		BRACKET REG BOARD	7413241	108
2		LUGS SPLIT	9006735	109
11		CONN SOLDERLESS	9007926-01	110
2		CONN SOLDERLESS	9007928	111
A/R		COMPOUND THERMO	9008268	112
4	C5, C10	WASHER #6 NYLON	9006707	113
13	D4, D17, D20, D21, D23 D24, D28 - D32, D22 D35	DIODE 0672	1105875	114
A/R		WIRE, 30 AWG, GREEN	9105740-05	115
1		DECAL	A-DC-7413498-0-0	116
2	R64, R65	RES 270 1/4W 5%	1301972	117
1	R66	RES 33 1/4W 5%	1300197	118
				119
1	D34	DIODE IN 9708	1110856	120
1		PACKAGING INSTRUCTIONS	A-SP-3700175-00	121

QTY	REF DESIGNATION	DESCRIPTION	PART NO	NEW NO
8	R14, R30, R40, R44, R55, R57, R62 R65	RES 1K 1/4W 5%	1300665	38
1	R45	RES 1.82K 1/8 W 5%	1300391	39
1	R27	RES 1.5K 1/8W 5%	1300394	40
2	C36, R61	RES 3.3K 1/4W 5%	1300429	41
1	R56	RES 4.7K 1/4W 5%	1300447	42
1	R16	RES 10 1/4W 5%	1301317	43
2	R42, R47	RES 680 1/4W 5%	1301424	44
1	R46	RES 200 2W 5%	1301494	45
1	R52	RES 511 1/4 W 1%	1302411	46
1	R26	RES 56 1/4W 5%	1302602	47
1	R3	RES 56 2W 5%	1302836	48
1	R12	RES 100 1/2W 1%	1302868	49
4	R21, R33, R34, R63	RES 1.21K 1/4W 1%	1302871	50
1	R9	RES 196 1/4W 1%	1302956	51
3	R37, R35, R50	RES 464 1/4W 1%	1303097	52
1	R18	RES 470 2W 5%	1303062	53
1	R57	RES 12.1K 1/4W 1%	1303313	54
1	R2	RES 1 5W 10%	1303365	55
1	R10	RES 1.96K 1/4W 1%	1306833	56
3	R37, R38, R39	RES 15K 1/4W 5%	1300496	57
1	R51	RES 2.2K 1/4W 5%	1300417	58
1	R48	RES 383 1/4 W 1%	1305185	59
1	R23	RES 619 1/8 W 1%	1305186	60
1	R11	RES 100 3/4W 10%	1309145-04	61
1	R49	RES 500 3/4 W 10%	1309182-06	62
1	R53	RES 5K 3/8W 10%	1309183-09	63
1	R58	RES 14.7K 1/4W 1%	1802981	64
1	R20	RES .1Ω 5W 1%	1310189	65
1	R8	RES 100 1/2W, NTC	1311760	66
1	E4	IC DEC 7474	1905547	67
1	E3	IC DEC 74121	1910230	68
2	E2, E5	IC DEC 72741	1910398	69
1	E1	IC DEC 723	1910415	70
4	Q4, Q12, Q20, Q21	TRANS DEC 65368	1503409-01	71
1	Q6	TRANS DEC 2N3791	1509581	72
1	Q2	TRANS MJE 3055	1510555	73
1	Q5	TRANS MJE 8955	1510556	74
2	D3, D12	TRANS C32A K/35 SCR	1510928	75
1	Q1	TRANS 2N5655	1511647	76
13	Q3, Q5, Q7, Q9 Q10, Q11, Q13-Q19	TRANS DEC 65316	1509338	77
7		SCREW 6-32 X .25	9006020-1	78
6		SCREW 8-32 X .31	9006021-1	79
1		SCREW 8-32 X .75	9006061-1	80

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE REGULATOR BOARD 8A CORE
SIZE D | CODE CS | NUMBER G8018-Ø-1 | REV. J
SCALE | SHEET 2 OF 9 | DIST.

H-84


+5 VOLT REGULATOR
POWER OK INDICATOR
-5 VOLT REGULATOR
+20 VOLT REGULATOR
TITLE REGULATOR BOARD 8A CORE
SIZE CODE DCS G8018-0-1
SHEET 3 OF 4
REV. J
REVISIONS
CHANGE NO.
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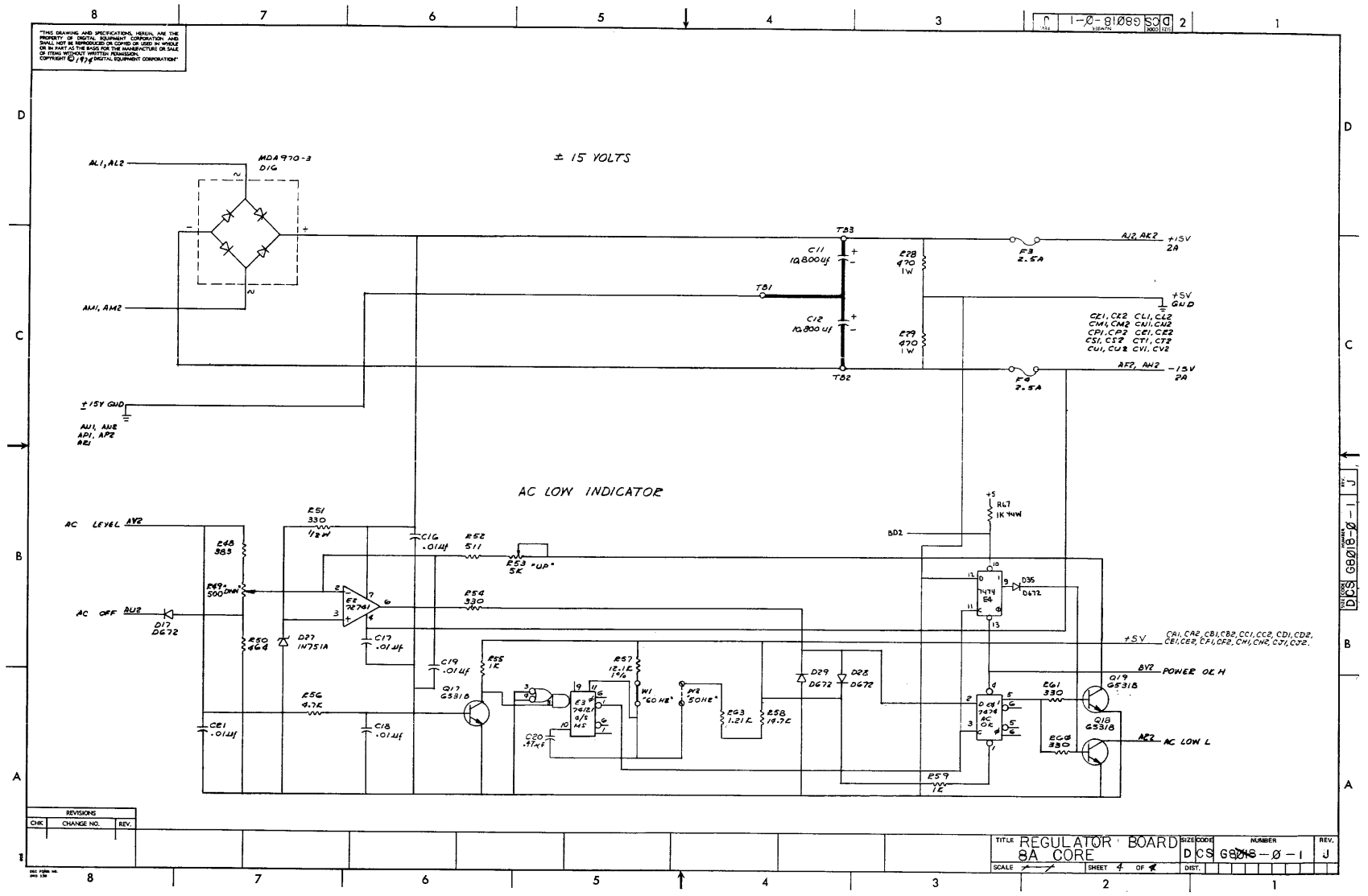
± 15 VOLTS
AL1, AL2
MDA970-3
DIG
AM1, AM2
±15V GND
AH1, AH2
AP1, AP2
AR1
TB3
TB1
TB2
C11
10,800uf
C12
10,800 uf
R28
470
1W
R29
470
1W
F3
2.5A
F4
2.5A
AL2, AK2 +15V
2A
+5V
GND
CE1, CE2 CL1, CL2
CM1, CM2 CU1, CU2
CP1, CP2 CE1, CE2
CS1, CS2 CT1, CT2
CU1, CU2 CV1, CV2
AF2, AH2 -15V
2A
AC LOW INDICATOR
AC LEVEL AV2
AC OFF BU2
D17
DG72
R48
383
R49
500 OHM
R50
464
D27
1N751A
R51
330
1/2W
C16
.01uf
R52
511
R53
5K "UP"
R54
330
C17
.01uf
C19
.01uf
R55
1K
Q17
G5318
R56
4.7K
CE1
.01uf
C18
.01uf
R57
12.1K
1%
W1
"60 HZ"
W2
"50 HZ"
R58
19.7K
R59
1K
C20
.47uf
R63
1.21K
D29
DG72
D28
DG72
BD2
+5
R47
1K 1%W
D35
DG72
+5V
CA1, CA2, CB1, CB2, CC1, CC2, CD1, CD2,
CE1, CE2, CF1, CF2, CH1, CH2, CJ1, CJ2.
BY2 POWER OK H
Q19
G5318
R61
330
Q18
G5318
R60
330
AF2 AC LOW L
R59
1K
REVISIONS
CHK
CHANGE NO.
REV.
TITLE REGULATOR BOARD 8A CORE
SIZE CODE DCS
NUMBER G8018-Ø-1
REV. J
SCALE
SHEET 4 OF 4
DIST.

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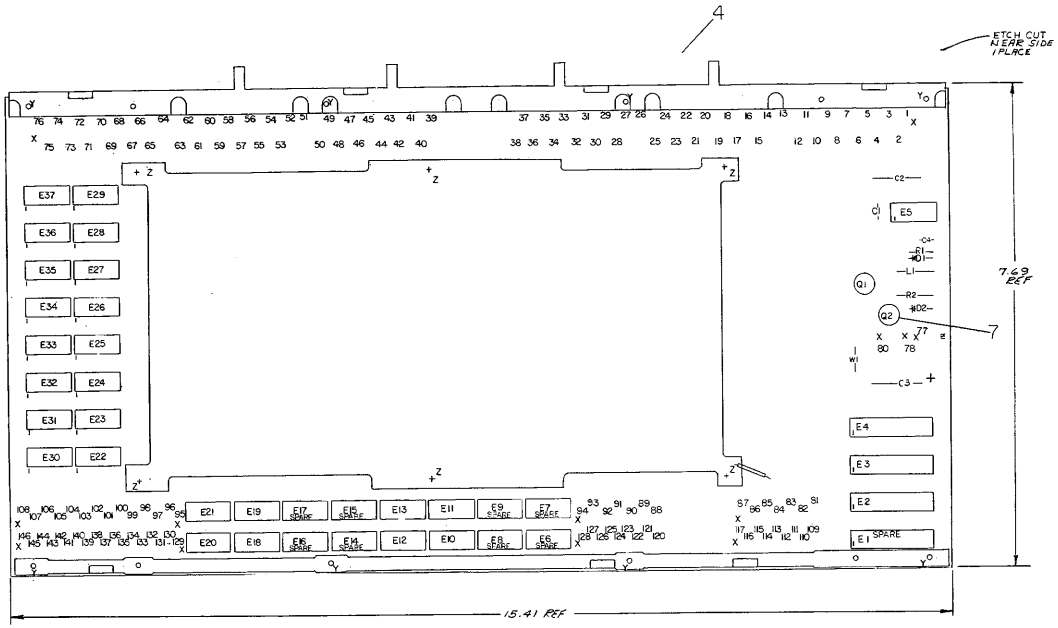
NOTES:

1. E1, E6 THRU E9, AND E14 THRU E17 ARE SPARES.
2. OMIT PINS, 79, 118, 119



REF		DESCRIPTION	PART NO.	ITEM NO.
REF		X-Y COORDINATE HOLE LOCATION	6.CO-5411531-0-4	1
REF		ASSY/DRILLING HOLE LAYOUT	D-AH-5411531-0-5	2
REF		MODULE ECO HISTORY	B-MH-5411531-0-0	3
1		ETCHED CIRCUIT BOARD	3010986-00	4
1	C1	CAP .01 µF 100V 20%	1001610-00	5
2	C2, C3	CAP 6.8 µF 35V 10% S.TANT	1005306-00	6
3		TRANSIPRO	9007201-00	7
2	D1, D2	DIODE D672	1105275-00	8
				9
1	R2	RES 39 1/2W 5%	1302336-00	10
3	E2, E3, E4	RES PACK (8-220 CKTS 1% COM)	1311742-00	11
2	Q1, Q2,	TRANS 3734	1510062-00	12
1	L1	INDUCTOR, DD100	1610662-00	13
1	E5	I.C. 7412B	1912068-00	14
24	E10 — E13, E18 - E37	I.C 2501	1910010-00	15
99	J1, J18, J99, J85-J108, J113-J117, J120-J196 J1-J3, J7-J9, J13-J16, J20-J22, J26-J29, J33-J35, J39-J41, J45-J47, J51-J54, J58-J60, J64-J67 J71-J3	CONTACT, MALE SEE NOTE 2	12/1727-00	16
1	W1	JUMPER	9009180-00	17
1	R3	RES 100 1/4 W 5%	1300229-00	18
1	C4	CAP 1000 PF	1000042-00	19

QTY	REF. DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.

74128	7	14
IC TYPE	GND	+5V

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

FIRST USED ON OPTION MODEL: PDP-8A-MEM

ETCH BOARD REV. B

PARTS LIST

REV.	CHANGE NO.	DEC NO.	EIA NO.	DEC NO.	EIA NO.
A	0001				

C. GRANTER 5411531

SEMICONDUCTOR CONVERSION CHART

DRN. [illegible] DATE 12/14/74
CHKD. [illegible] DATE 12/16/74
ENG. DATE
PROJ. ENG. DATE 12/16/74
PROD. DATE 12/16/74
NEXT HIGHER ASSY
SCALE
SHEET 1 OF 4

digital

TITLE: CORE MEMORY STACK 8K

SIZE D | CODE CS | NUMBER 5411531-0-1 | REV. A

DIST.

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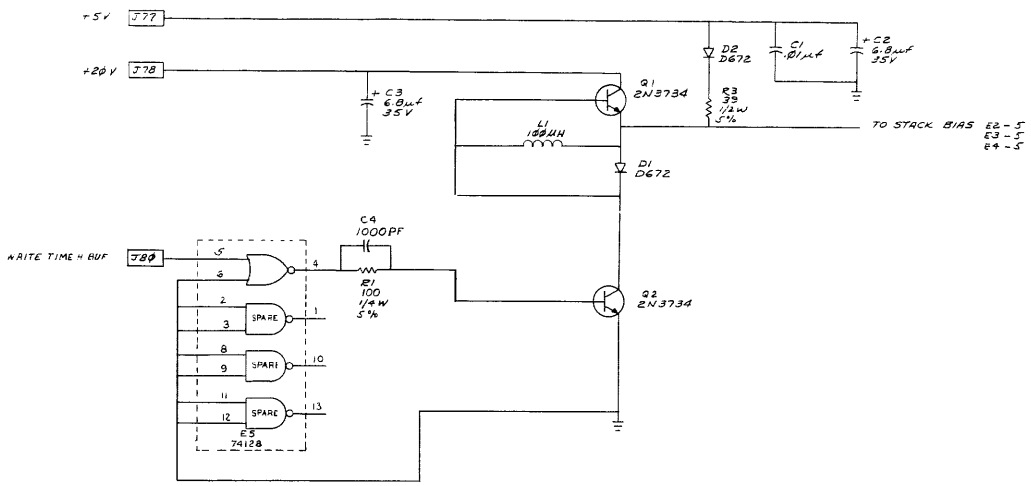

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
CORE MEMORY STACK 8K	D	CS	5411531-0-1	A
SCALE	SHEET 2 OF 4	DIST.		

DCS 5411531-0-1 A

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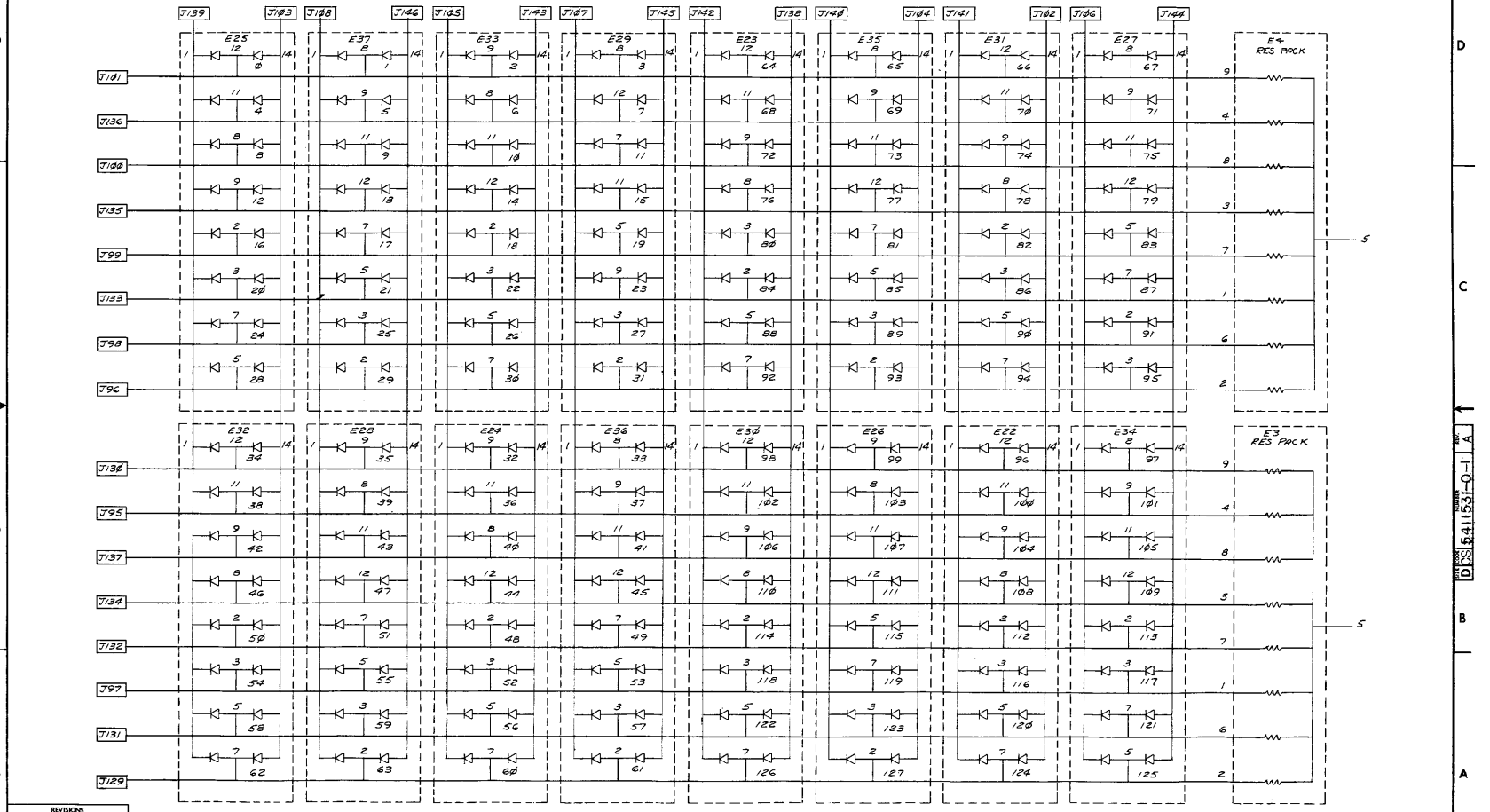

("X" DRIVE DIMENSION DIODE MATRIX)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
CORE MEMORY STACK 8K	D	CS	5411531-0-1	A
SCALE —	SHEET 3 OF 4	DIST.		

5411531-0-1

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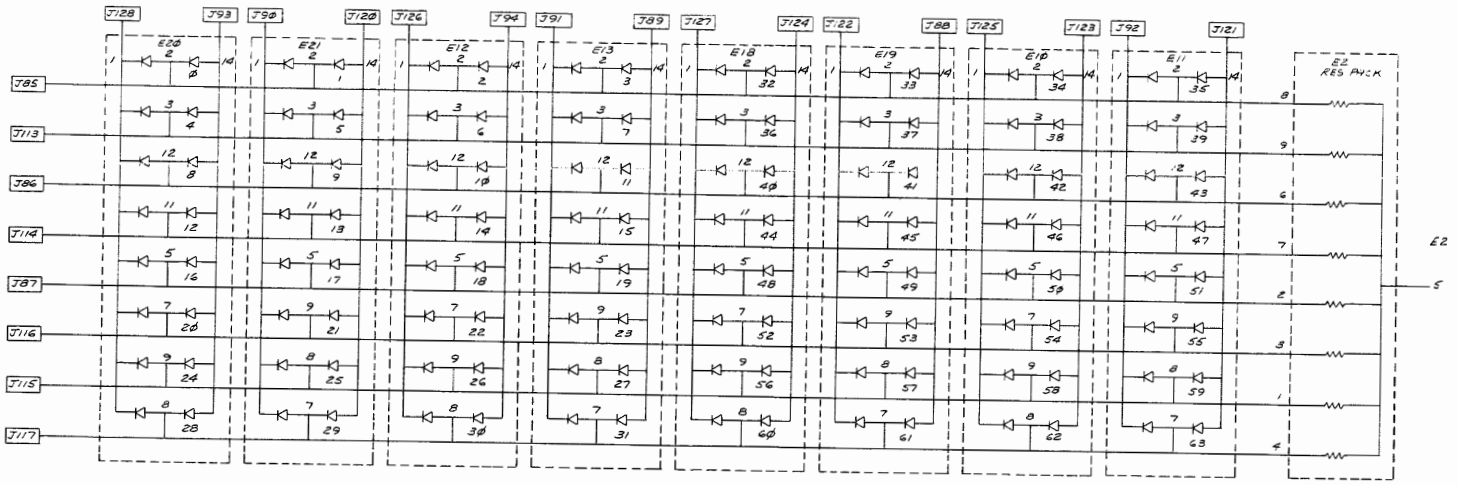

"Y" DRIVE DIMENSION DIODE MATRIX)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
CORE MEMORY STACK 8K	D	DCS	5411531-0-1	A
SCALE	SHEET 4 OF 4	DIST.		

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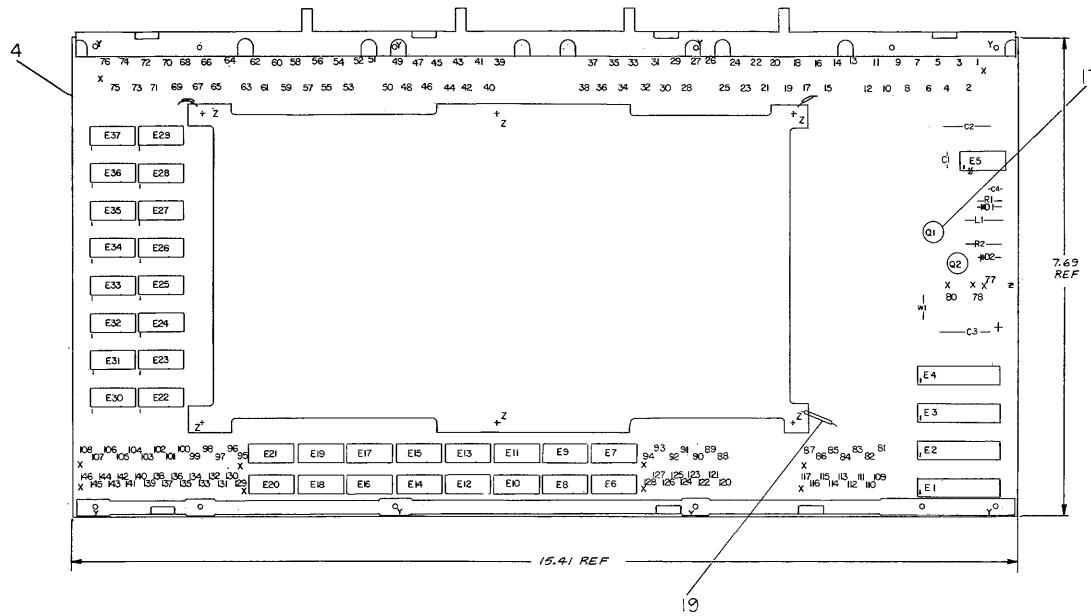
NOTES:

1. OMIT PINS 79, 118, 119.
2. ITEM 5 MUST BE 10-01610-00 NO SUBSTITUTIONS ALLOWED.
3. HEIGHT TOLERANCE MUST BE WATCHED ON ITEM 7 (1000 PF) NOT TO EXCEED .312.



REF				
REF		X-Y COORDINATE HOLE LOCATION	K-CO-5411531-YA-A	1
REF		ASSY/DRILLING HOLE LAYOUT	D-AN-5411531-YA-5	2
REF		MODULE ECO HISTORY	B-MM-5411531-YA-6	3
1		ETCHED CIRCUIT BOARD	5010986-00	4
1	C1	CAP .01UF 100V	1001610-00	5
2	C2,C3	CAP 6.8UF 35V 10% S.TANT	1005306-00	6
1	C4	CAP 1000PF 100V D MICA	1000042-00	7
2	D1, D2	DIODE D672	1105275-00	8
1	R1	RES 100 1/4W 5%	1300229-00	9
1	R2	RES 39 1/2W 5%	1302336-00	10
4	E1-E4	RES PACK	1311742-00	11
2	Q1-Q2	TRANS 2N3734	1510062-00	12
1	L1	INDUCTOR, DD100	1610662-00	13
1	E5	I.C. 74128	1912068-00	14
32	E6-E37	I.C. 2501	1910010-00	15
183	J1-J78, J80-J117, J120-J146	CONTACT MALE (SEE NOTE 1)	1211727-00	16
2		TRANSIPAD	9007201-00	17
1	W1	JUMPER, INSULATED	9009185-00	18
A/R		WIRE, JUMPER	9105790-55	19

QTY	REF. DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

2501	—	—
IC TYPE	GND	+5V

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

FIRST USED ON OPTION MODEL: MM8-AB

ETCH BOARD REV. 8

CHANGE NO.	REV.
DEC NO.	EIA NO.
DEC NO.	EIA NO.

SEMICONDUCTOR CONVERSION CHART

DRN. [signature] DATE 3/18/75
CHK'D [signature] DATE 3/27/75
PROJ. ENGR. [signature] DATE 7-21-75
PROJ. LDR. [signature] DATE 10-6-75
NEXT HIGHER ASSY

digital

TITLE: CORE MEMORY STACK 16K

SIZE D | CODE CS | NUMBER 5411531-YA-1 | REV. A

SCALE — SHEET 1 OF 4 DIST.

SIZE D | CODE CS | NUMBER 5411531-YA-1 | REV. A

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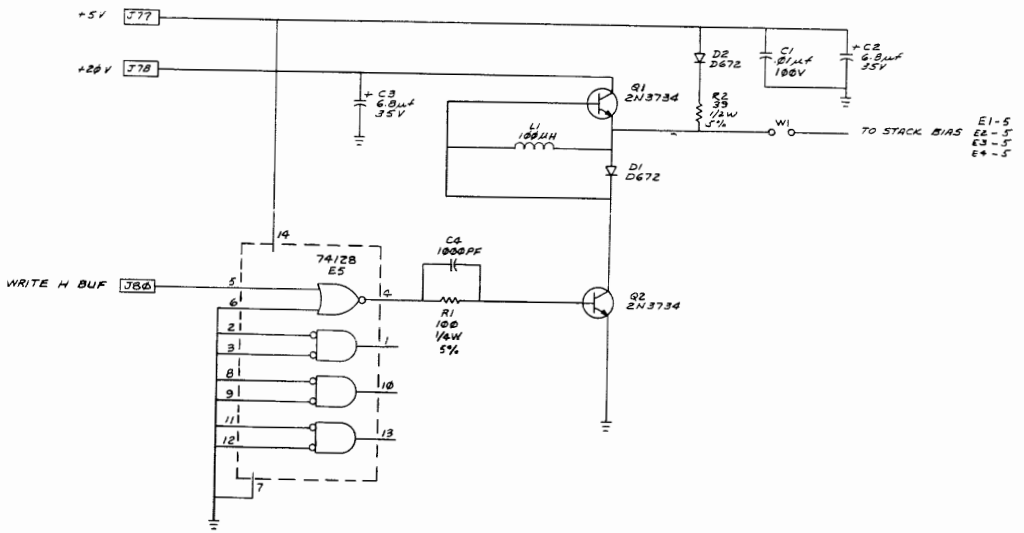
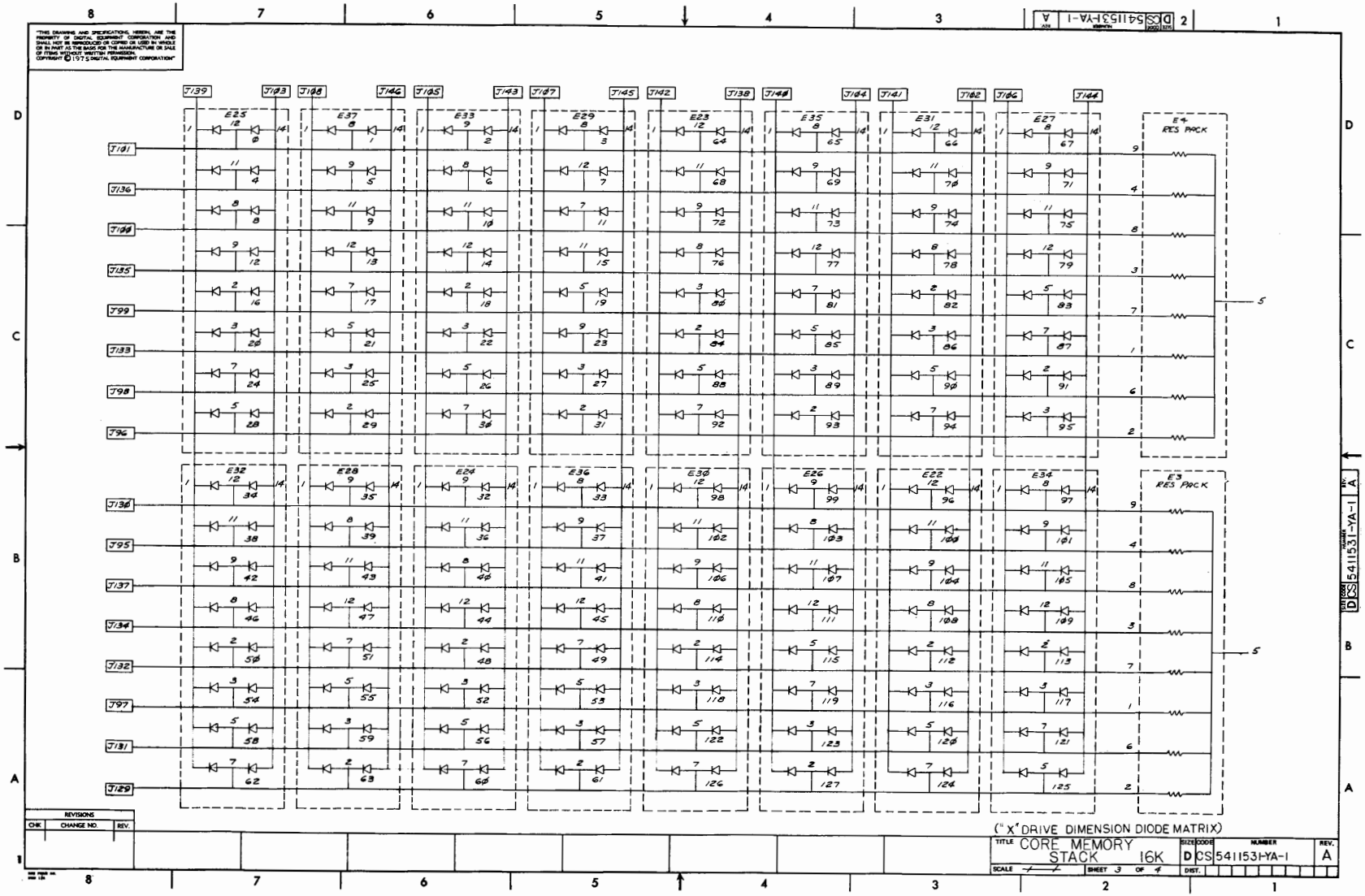


REVISIONS		
CHK	CHANGE NO.	REV.

TITLE CORE MEMORY STACK 16K
SIZE D CODE DCS NUMBER 5411531-YA-1 REV. A
SCALE SHEET 2 OF 4 DIST.

DIGITAL DCS 5411531-YA-1 REV A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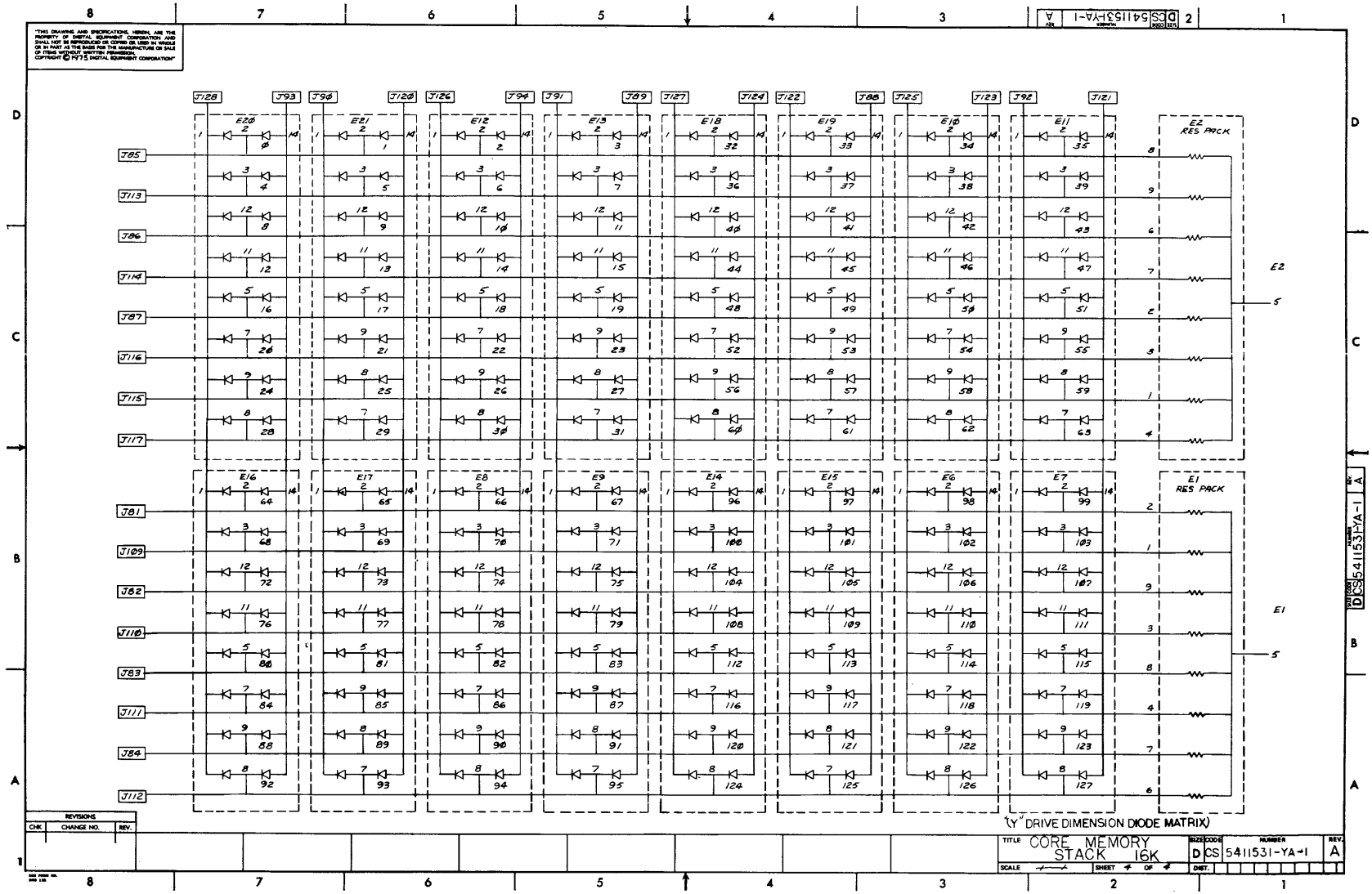
J139 J103 J108 J146 J105 J143 J107 J145 J142 J138 J140 J104 J141 J102 J106 J144
J101 J136 J100 J135 J99 J133 J98 J96
J130 J95 J137 J134 J132 J97 J131 J129
E25 E37 E33 E29 E23 E35 E31 E27
E32 E28 E24 E36 E30 E26 E22 E34
E4 RES PACK
E3 RES PACK
("X" DRIVE DIMENSION DIODE MATRIX)
REVISIONS
CHK CHANGE NO. REV.
TITLE CORE MEMORY STACK 16K
SIZE CODE DCS5411531-YA-1 REV. A
SCALE SHEET 3 OF 4
DIST.
DCS5411531-YA-1 A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DCS5411531-YA-1 A
J128 J93 J96 J120 J126 J94 J91 J89 J127 J124 J122 J88 J125 J123 J92 J121
J85 J113 J86 J114 J87 J116 J115 J117
J81 J109 J82 J110 J83 J111 J84 J112
E20 E21 E12 E13 E18 E19 E10 E11
E16 E17 E8 E9 E14 E15 E6 E7
E2 RES PACK
E1 RES PACK
E2
E1
"Y" DRIVE DIMENSION DIODE MATRIX)
REVISIONS
CHK CHANGE NO. REV.
TITLE CORE MEMORY STACK 16K
SIZE D CODE CS NUMBER 5411531-YA-1 REV. A
SCALE SHEET 4 OF 4 DIST.
DCS5411531-YA-1 REV. A

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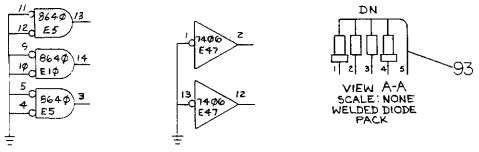
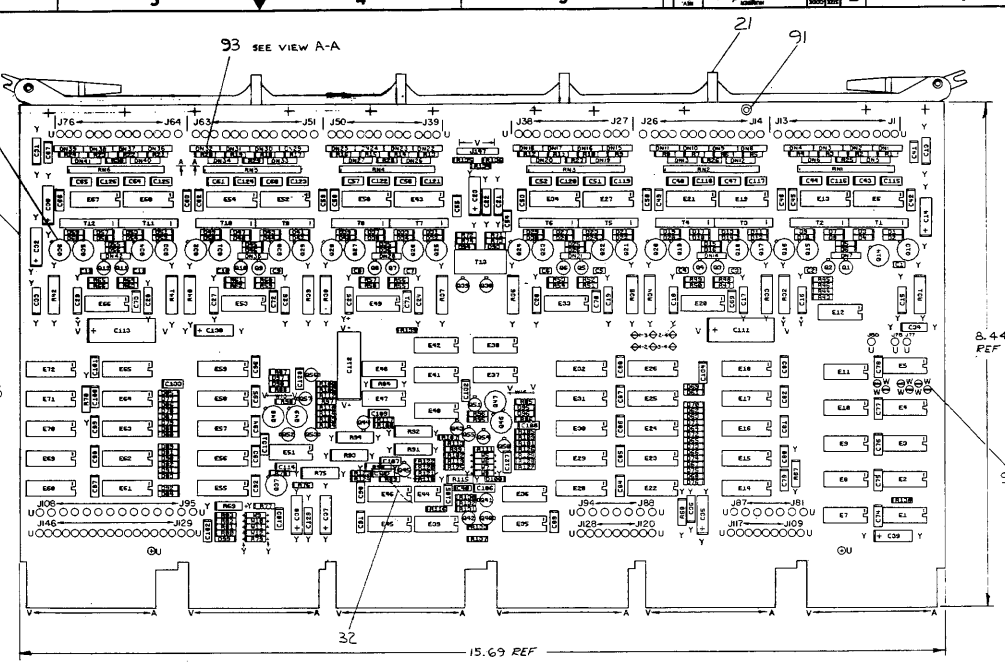
NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   a. RESISTORS ARE 1/4W, ±5%
   b. CAPACITORS ARE 50V
   c. DIODES ARE D672
2. ALL RECEPTACLES ARE INDICATED WITH J NO'S.
3. COMP. C68, C104 NOT USED
4. DEFINITION OF MEMORY SELECTION JUMPERS

WITH JUMPERS IN LOCATIONS	MEMORY IS DECODED FOR ADDRESSESS	MEMORY BANK SELECTED
1&1	Ø TO 16K	1ST 16K
2&2	16K TO 32K	2ND 16K
3&3	32K TO 48K	3RD 16K
4&4	48K TO 64K	4TH 16K





+5V AA2, BA2
J77 AC2, AF1, AF2, AH1, AH2, AT1, AT2, BC1, BC2, BF1, BF2, BH2, BT1, BT2, CC1, CC2, CF1, CF2, CH1, CH2, CT1, CT2, EC2, EF2, DC2, DF1, DF2, DH1, DH2, DT1, DC1, DT2, EH2, ET2
C69 THRU C79, C81, C89, C84, C86, C88 THRU C92, C94, C96, C97, C99, C101, C132, C133, C139 .01 µF
C34 .47 µF
C35 8 µF 25V
C39 8 µF 25V
C130 8 µF 25V

+20V XY EA2
J78
C112 47 µF 30V
C80, C82, C85, C87, C93, C95, C98, C100 .01 µF
C36 .47 µF
C37 8 µF 25V

+20V VZ EE2, EK2, EP2
C38 8 µF 25V

75325		8	9	16
7520	8	9	16	
8640		1	8	
7442		8	16	
72741		4		7
7384		1	8	
IC TYPE	-5V	GND	+5V	+20V

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

QTY	REF. DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

FIRST USED ON OPTION MODEL: MM8-AB

ETCH BOARD REV: C

CHANGE NO. REVISIONS	REV.	DWN	CHK	DATE	ENG	DATE	PROJ. ENG	DATE	PROD. ENG	DATE	PROJ.	NEXT HIGHER ASSY	SCALE	SHEET 1 OF 12
DEC NO.	EIA NO.	DEC NO.	EIA NO.											

SEMICONDUCTOR CONVERSION CHART

digital

TITLE 16K, 12 BIT (BI) BASE BOARD

SIZE D | CODE CS | NUMBER G650-Ø-1 | REV B | DIST.

G650-Ø-1

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PARTS LIST

QTY	REF DESIGNATIONS	DESCRIPTION	PART NO	ITEM NO
REF		X-Y COORDINATE HOLE LOCATION	K-CO-G649-0-4	1
REF		ASSY/DRILLING HOLE LAYOUT	D-AH-G649-0-5	2
REF		MODULE ECO HISTORY	B-MH-G649-0-6	3
1		ETCHED CIRCUIT BOARD	5011016	4
1	C119	CAP .47 PF 100V 5% DM	1000011-00	5
12	C60,C62,C64,C66,C68,C70, C72,C74,C76,C78,C80,C82	CAP 100 PF 100V 5% DM	1000016-00	6
1	C108	CAP 56 PF 100V 5% DM	1000012-00	7
1	C109	CAP 2.2 PF 100V 5% DM	1005820-00	8
15	C96,C97,C98,C99,C101-C105, C110,C113,C130,C131 C132 C129	CAP .47 μF 50V	1012312-00	9
1	R94	RES 261 1/4W 1%	1302873-00	10
12	C83-C94	CAP 3300 PF 50V 10%	1011740-01	11
1	C117	CAP .022 μF 50V 10%	1011683-00	12
1	R114	RES 1K 1/2W 1%	1300381-00	13
1	D138	DIODE IN750A 4.7V ZENER	1100124-00	14
137	D1-D136, D139	DIODE D672	1105275-00	15
1	D137	DIODE IN759A 12V ZENER	1110836-00	16
1		HANDLE, REWORK	7418182-0-0	17
99	(SEE NOTE 2)	RECEPTACLE	12.11728-00	18
12	R1-R12	RES 33 1/4W 5%	1300197-00	19
1	R91	RES 100 1/4W 5%	1300229-00	20
1	R77	RES 220 1/4W 5%	1312123-00	21
3	R49-R51	RES 300 1/2W 5%	1300291-00	22
1	R86	RES 330 1/2W 5%	1300296-00	23
1	R80	RES 1K 1/4W 1%	1303114-00	24
2	R62,R98	RES 3.3K 1/4W 5%	1300439-00	25
4	R52,R53, R102,R103	RES 10K 1/4W 5%	1300479-00	26
1	R97	RES 750 1/4W 1%	1302955-00	27
4	R67,R88,R95,R116	RES 1.2K 1/4W 5%	1301320-00	28
1	R69	RES 35.7K 1/8W 1%	1303421-00	29
1	R65	RES 220 1/4W 5%	1300271-00	30
4	R64,R82,R84,R93	RES 2K 1/4W 1%	1302715-00	31
6	R60,R61,R66,R96, R104,R105	RES 75 1/4W 1%	1303064-00	32
1	R59	RES 1.21K 1/4W 1%	1302871-00	33
1	R117	RES 82K 1/4W 5%	1303219-00	34
1	R58	RES 825 1/4W 1%	1305143-00	35
2	R106,R107	RES 14.7K 1/4W 1%	1302941-00	36
1	R87	RES 5.11K 1/4W 1%	1304854-00	37
12	R25-R36	RES 4.7K 1/4W 5%	1300447-00	38
1	R109	RES 19.6K 1/4W 1%	1309419-00	39
1	R71	RES 137K 1/4W 1%	1305422-00	40
5	R55,R56,R66,R81,R89	RES 562 1/4W 1%	1304693-00	41
4	R54,R57,R99,R100	RES 383 1/4W 1%	1305125-00	42
2	R70,R111	RES 68.1K 1/4W 1%	1305252-00	43
1	R112	RES 121K 1/4W 1%	1305255-00	44
1	R110	RES 34.8K 1/4W 1%	1303156-00	45
2	R63,R85	RES 4.99K 1/4W 1%	1305324-00	46
1	R92	RES 1K 1% THERMISTOR	1310071-00	47
12	R37-R48	RES 22 2W 1%	1312502-01	48
6	R13-R18	RES PACK 10/100 1/8W 1% CNTS	1311741-00	49

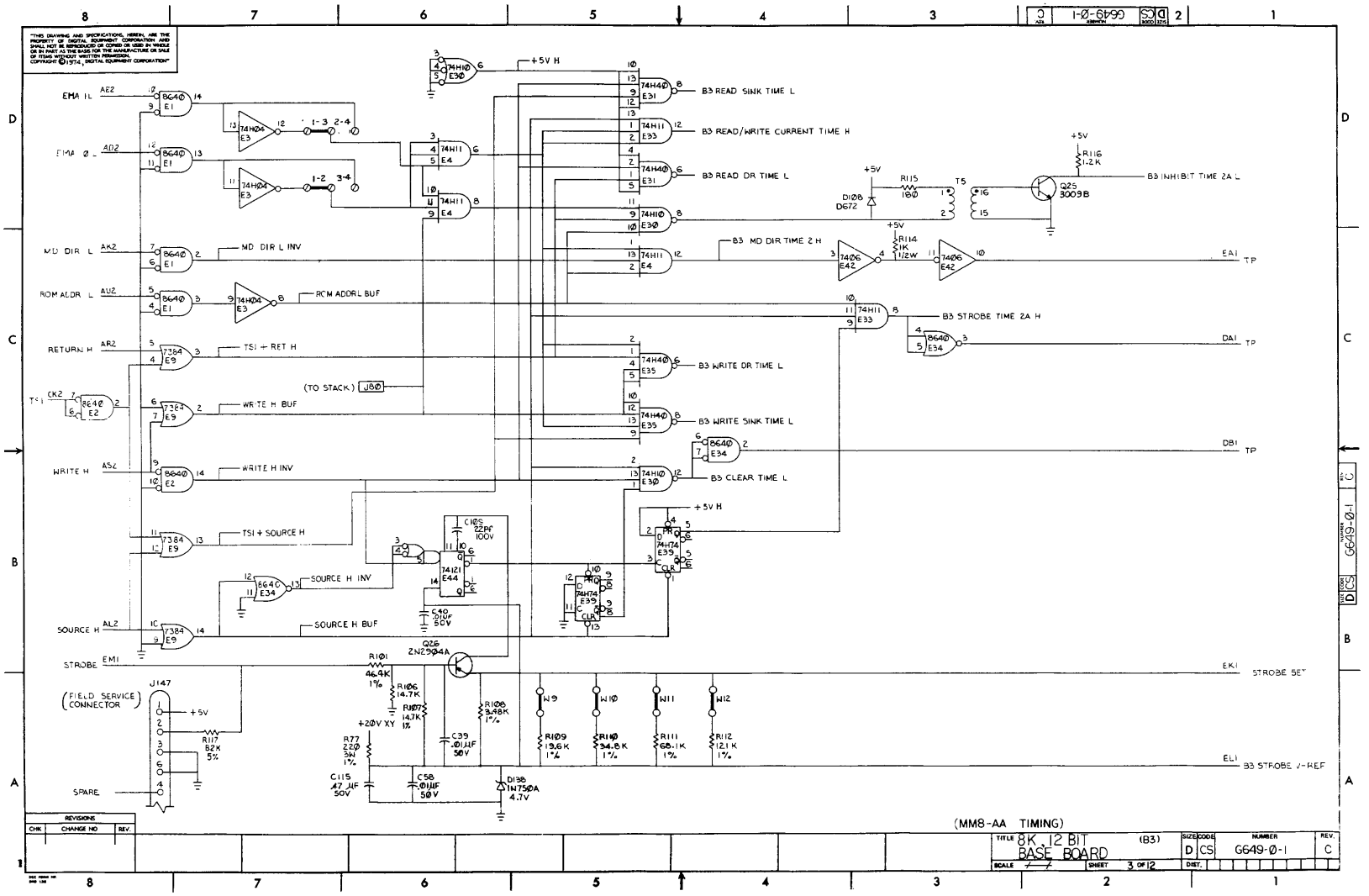
PARTS LIST

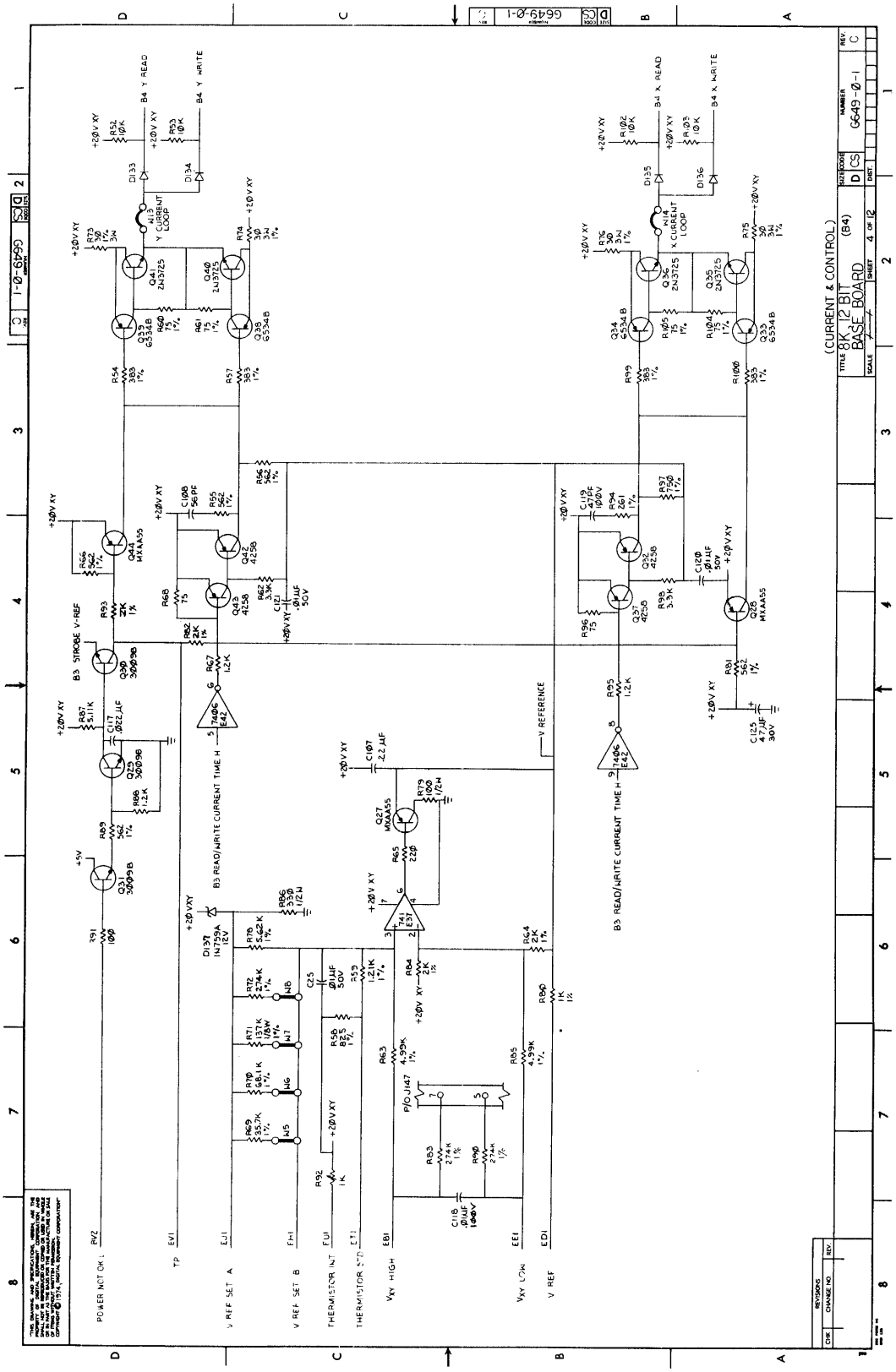
QTY	REF DESIGNATIONS	DESCRIPTION	PART NO	ITEM NO
4	R73-R76	RES 30 3W 1%	1311737-00	50
1	R79	RES 100 1/2W 5%	1300228-00	51
1	R115	RES 180 1/4W 5%	1301322-00	52
1	R113	RES 2.61K 1/4W 1%	1303303-00	53
1	Q26	TRANSISTOR 2N2904A	1501913-00	54
4	Q29-Q31, Q25	TRANSISTOR 3009B	1503100-00	55
4	Q33,Q34,Q38,Q39	TRANSISTOR 6534B	1503409-01	56
4	Q32,Q37,Q42,Q43	TRANSISTOR 4258	1505321-00	57
12	Q1-Q12	TRANSISTOR 6531B	1509338-00	58
2	W1,W2	BUS WIRE #22AWG	9107560-01	59
3	Q27,Q28,Q44	TRANSISTOR MXAA55	1510706-00	60
16	Q13-Q24,Q35,Q36,Q40,Q41	TRANSISTOR 2N3725	1510959-00	61
1	T5	TRANSFORMER 1:1	1609996-00	62
4	T1-T4	TRANSFORMER 2:1	1611756-00	63
2	E31,E35	IC 74H40	1905586-00	64
1	E30	IC 74H10	1909057-00	65
2	E4,E33	IC 74H11	1909267-00	66
1	E9	IC 7384	1910393-00	67
1	E35	IC 74H74	1909667-00	68
3	E7,E28,E40	IC 8881	1905705-00	69
1	E3	IC 74H04	1909931-00	70
5	E20,E26,E51,E58,E64	IC 7442	1910046-00	71
1	E44	IC 74121	1910230-00	72
1	E37	IC 741	1910298-00	73
1	E42	IC 7406	1910741-00	74
20	E16-E19,E22-E25,E47-E50, E54-E57,E60-E63	IC 75325	1910960-00	75
10	E1,E2,E5,E8,E10,E11, E29,E34,E36,E41	IC 8640	1911469-00	76
12	E6,E12,E14,E15,E21,E27, E30,E43,E45,E46,E53,E59	IC 7520	1911748-00	77
3	E13,E32,E52	IC 74128	1912068-00	78
6		EYELET (TERMINAL POSTS)	9006735-00	79
8	W5-W12	MACHINE INSERTED JUMPERS	9009185-00	80
2	W13,W14	INSULATED WIRE #22 AWG	1700035-00	81
1	J147	CONNECTOR 7 PIN	12.12104-00	82
12		EYELET	9006732-00	83
6	R19-R24	RES 10K 1/4W 1%	1303312-00	84
52	C1-C6,C9,C10,C13-C20, C23-C36,C37-C44,C47, C48,C51-C58,C118, C120-C123,C128	CAP .01μF 100V	1001610-01	85
13	C7,C8,C11,C12,C21,C22, C35,C36,C45,C46,C49, C50,C107	CAP .22μF 50V	1010274-00	86
1	R72	RES 274K 1/4W 1%	1305131-00	87
1	R108	RES 3.48K 1/4W 1%	1305114-00	88
A/R	W15-W18	WIRE #30 AWG SOLID GREEN	9105740-55	89
1	R101	RES 46.4K 1/4W 1%	1303311-00	90
1	R78	RES 5.62K 1/4W 1%	1305128-00	91
18		TRANSIPAD	9007201-00	92
-		"		93
10	C111-114, C100, C116, C127, C126, C124	CAP. 8UF 25V	1012084-01	94
3	C125, C95, C106	47UF 30V	1012219	95

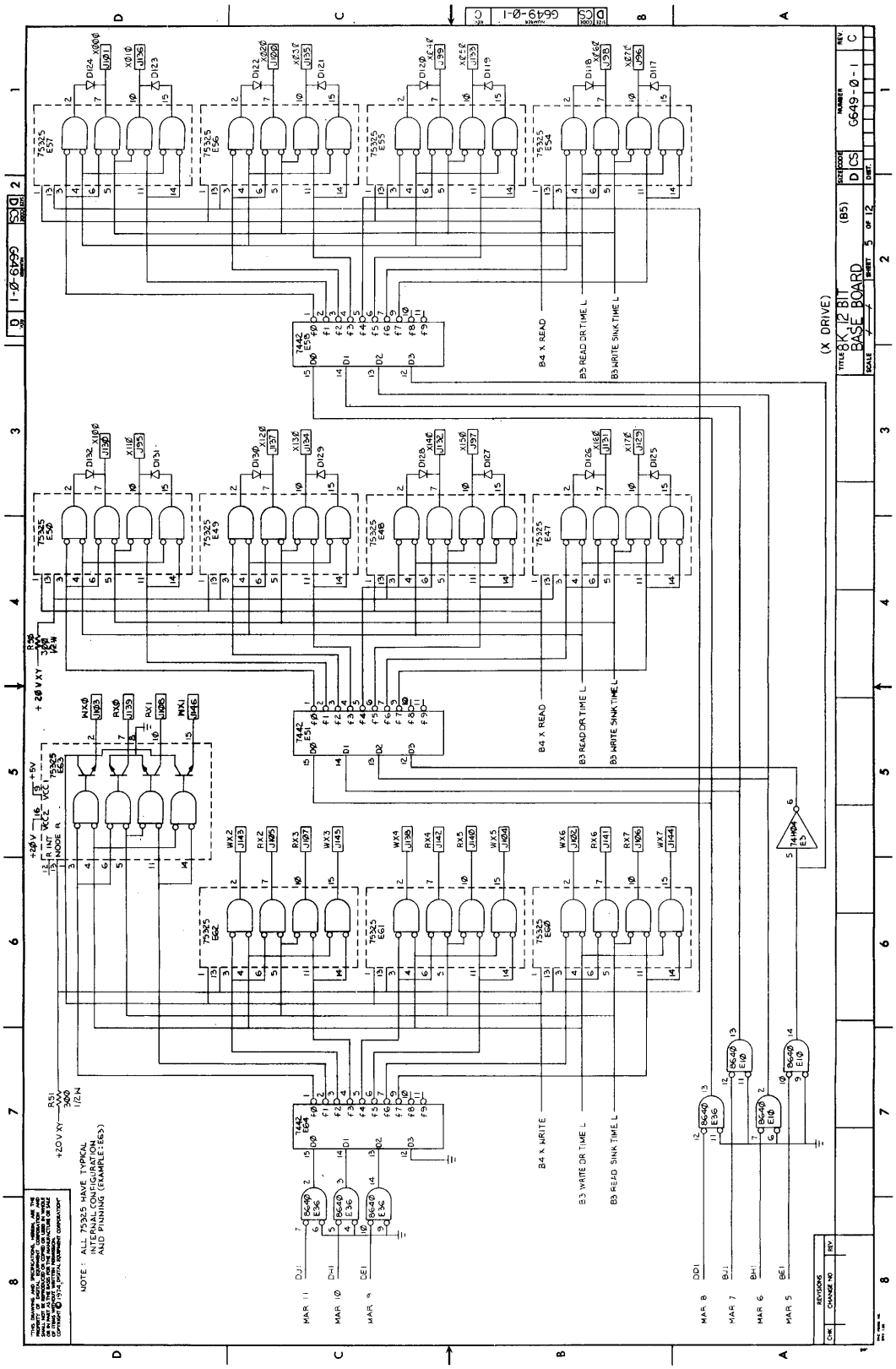
REVISIONS		
CHK	CHANGE NO	REV

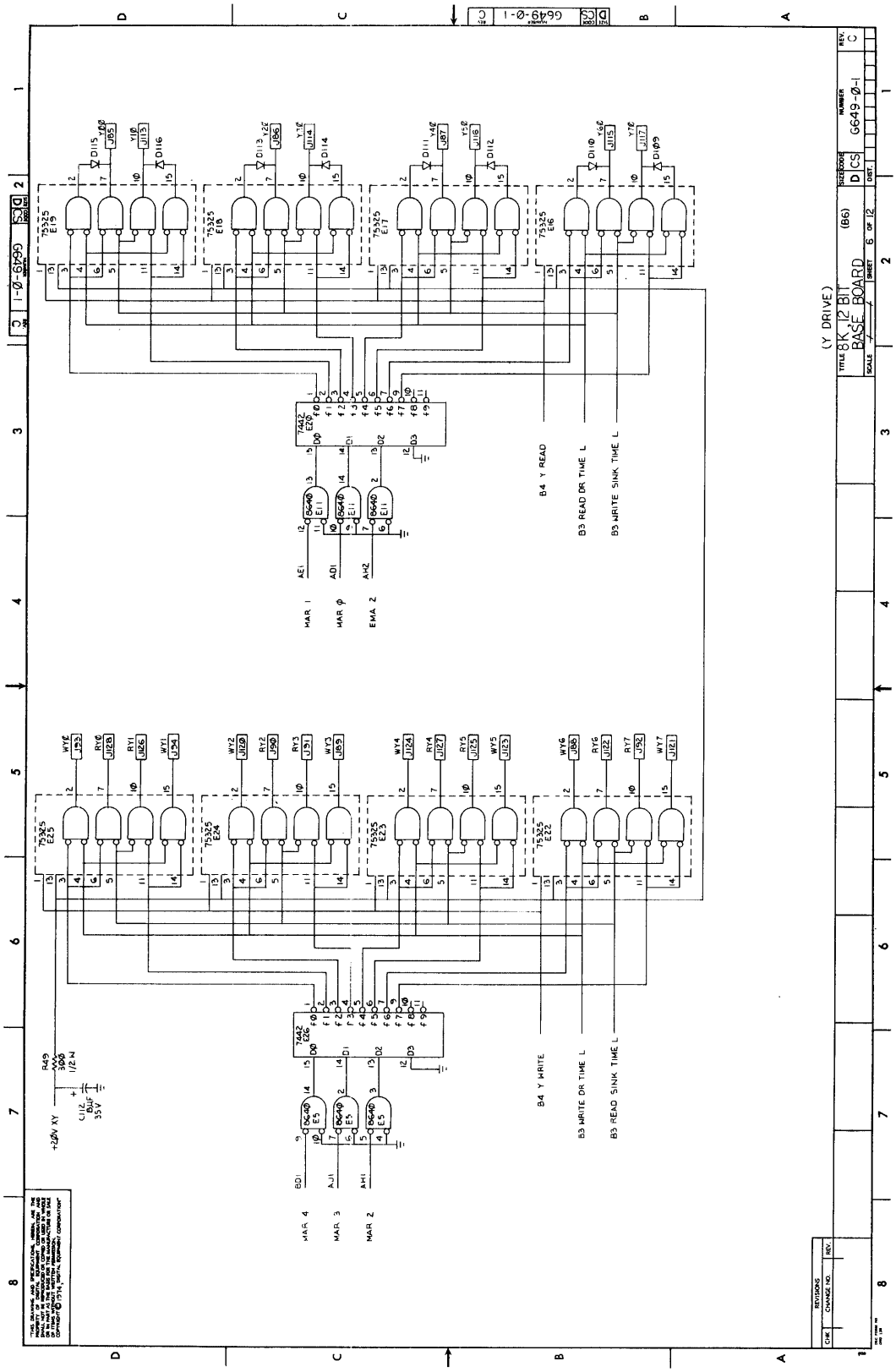
TITLE	SIZE	CODE	NUMBER	REV.
8K, 12 BIT BASE BOARD (B2)	D	CS	G649-0-1	C
SCALE —	SHEET 2 OF 12	DIST		

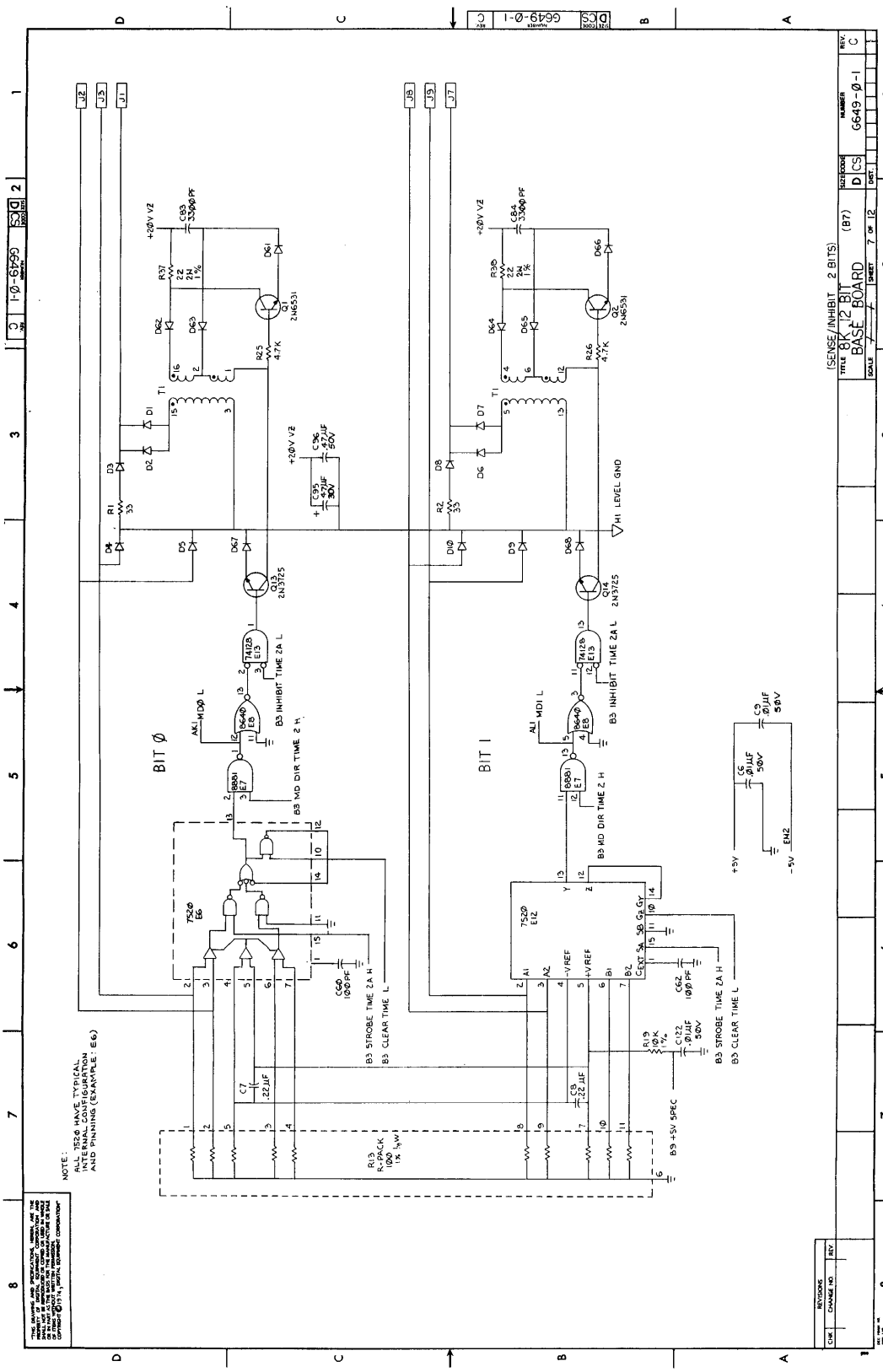
G649-0-1 C DCS

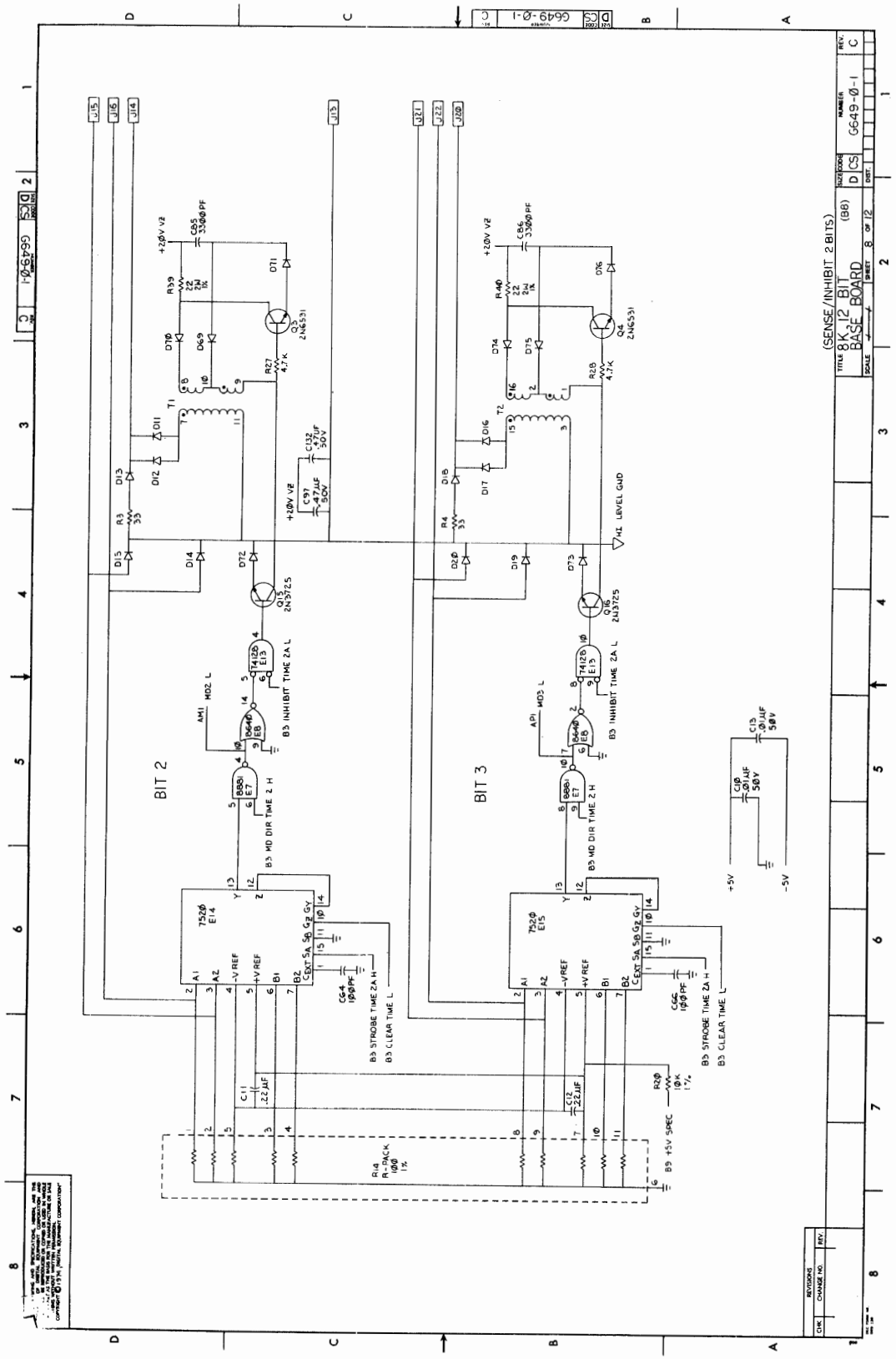

B3 READ SINK TIME L
B3 READ/WRITE CURRENT TIME H
B3 READ DR TIME L
B3 INHIBIT TIME 2A L
B3 MD DIR TIME 2 H
B3 STROBE TIME 2A H
B3 WRITE DR TIME L
B3 WRITE SINK TIME L
B3 CLEAR TIME L
B3 STROBE /-REF
MD DIR L INV
ROM ADDR BUF
TSI ← RET H
WRITE H BUF
WRITE H INV
TSI → SOURCE H
SOURCE H INV
SOURCE H BUF
STROBE SET
(TO STACK) J80
(FIELD SERVICE CONNECTOR)
SPARE
+5V H
+5V
+20V XY
(MM8-AA TIMING)
8K, 12 BIT BASE BOARD (B3)
G649-0-1

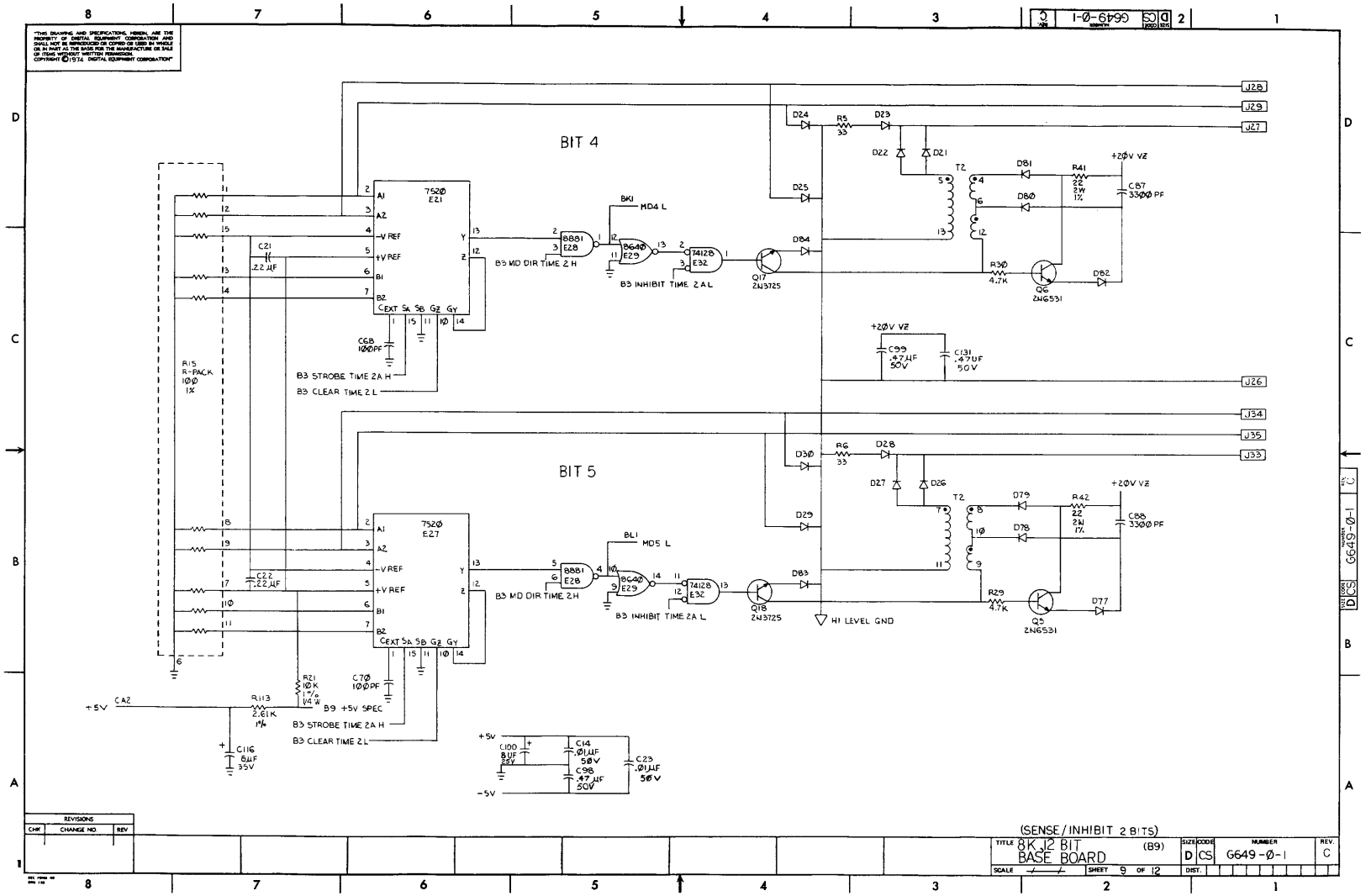

(CURRENT & CONTROL)
TITLE 8K 12 BIT
BASE BOARD
(B4)
SIZE D
CS
NUMBER 6649-0-1
REV. C
SCALE
SHEET 4 OF 12
DIST.
B4 Y READ
B4 Y WRITE
B4 X READ
B4 X WRITE
Y CURRENT LOOP
X CURRENT LOOP
B3 STROBE V-REF
B3 READ/WRITE CURRENT TIME H
V REFERENCE
POWER NOT OK
V REF SET A
V REF SET B
THERMISTOR INT
THERMISTOR EXT
VXY HIGH
VXY LOW
V REF
TP
+20V XY
+5V
-20V XY
6649-0-1

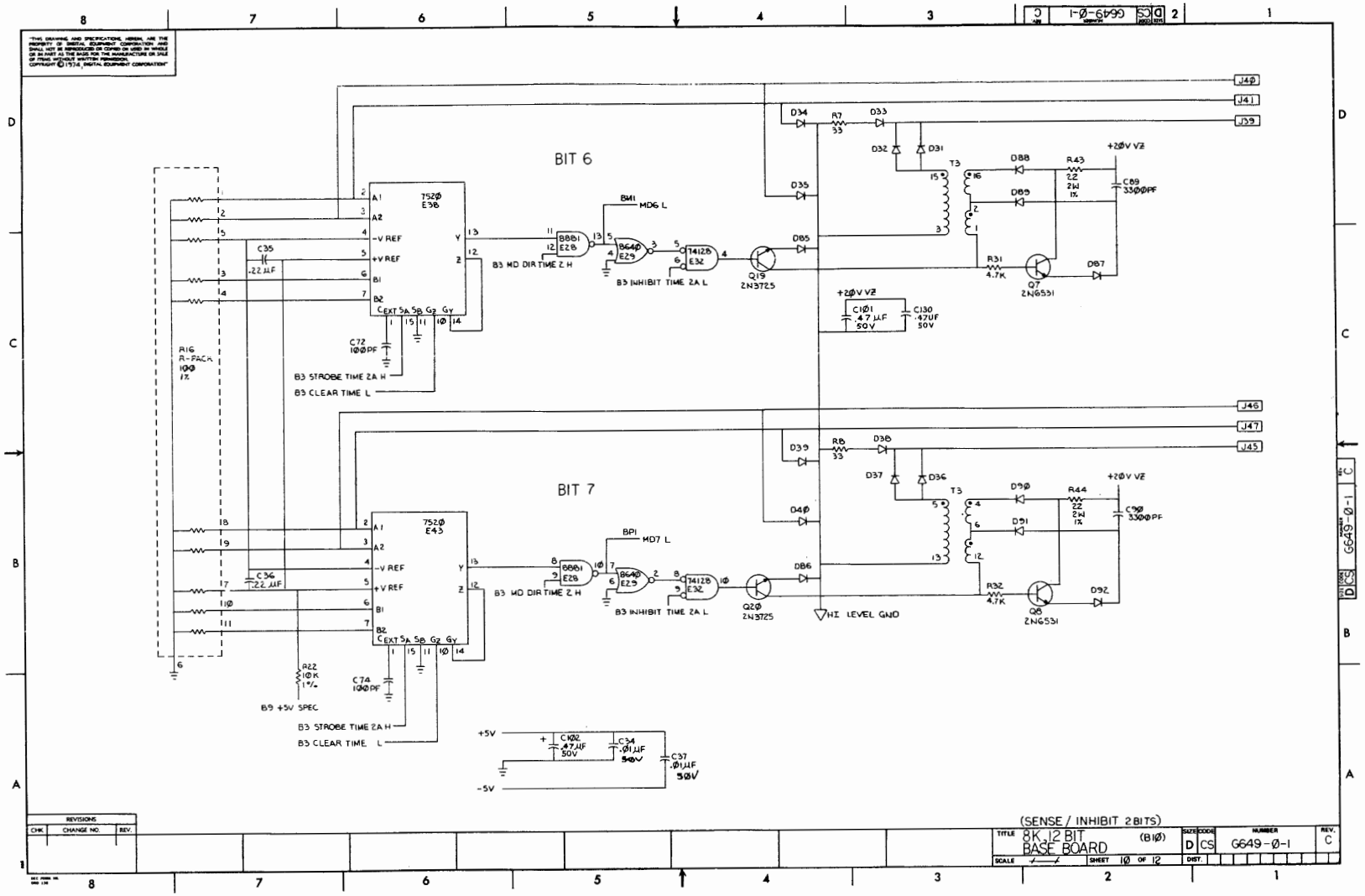

8K, 12 BIT
BASE BOARD
(X DRIVE)
(BS)
SIZE D
DWG NO 6649-0-1
REV C
SHEET 5 OF 12
6649-0-1
NOTE: ALL 75325 HAVE TYPICAL INTERNAL CONFIGURATION AND PINNING (EXAMPLE: E63)
+20 V XY
+5V
B4 X READ
B3 READ DR TIME L
B3 WRITE SINK TIME L
B4 X WRITE
B3 WRITE DR TIME L
B3 READ SINK TIME L
MAR 11
MAR 10
MAR 9
MAR 8
MAR 7
MAR 6
MAR 5

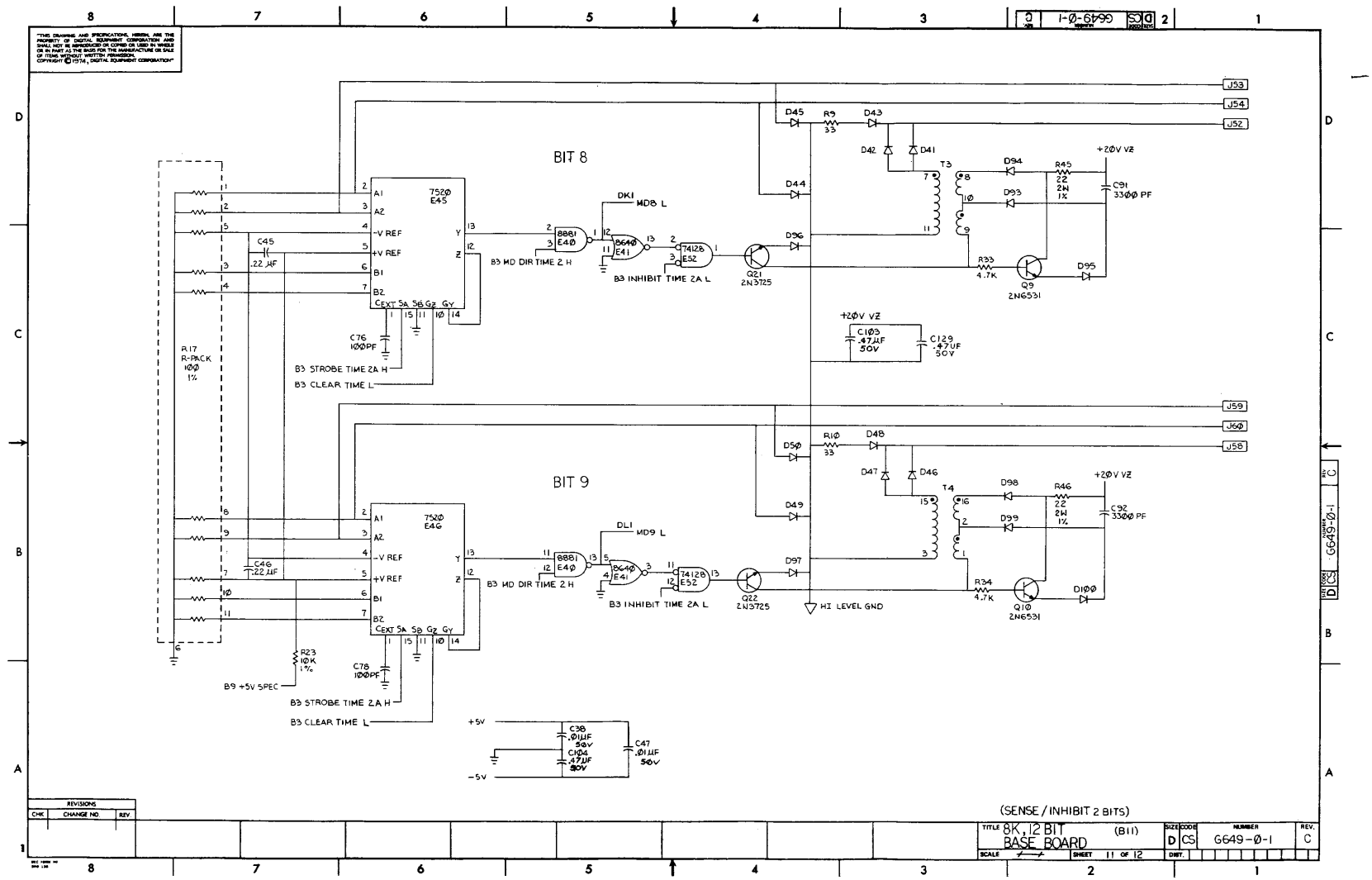

(Y DRIVE)
8K 12 BIT
BASE BOARD
G649-0-1
B4 Y READ
B3 READ DR TIME L
B3 WRITE SINK TIME L
B4 Y WRITE
B3 WRITE DR TIME L
B3 READ SINK TIME L
MAR 1
MAR 0
EMA 2
MAR 4
MAR 3
MAR 2
+24V XY

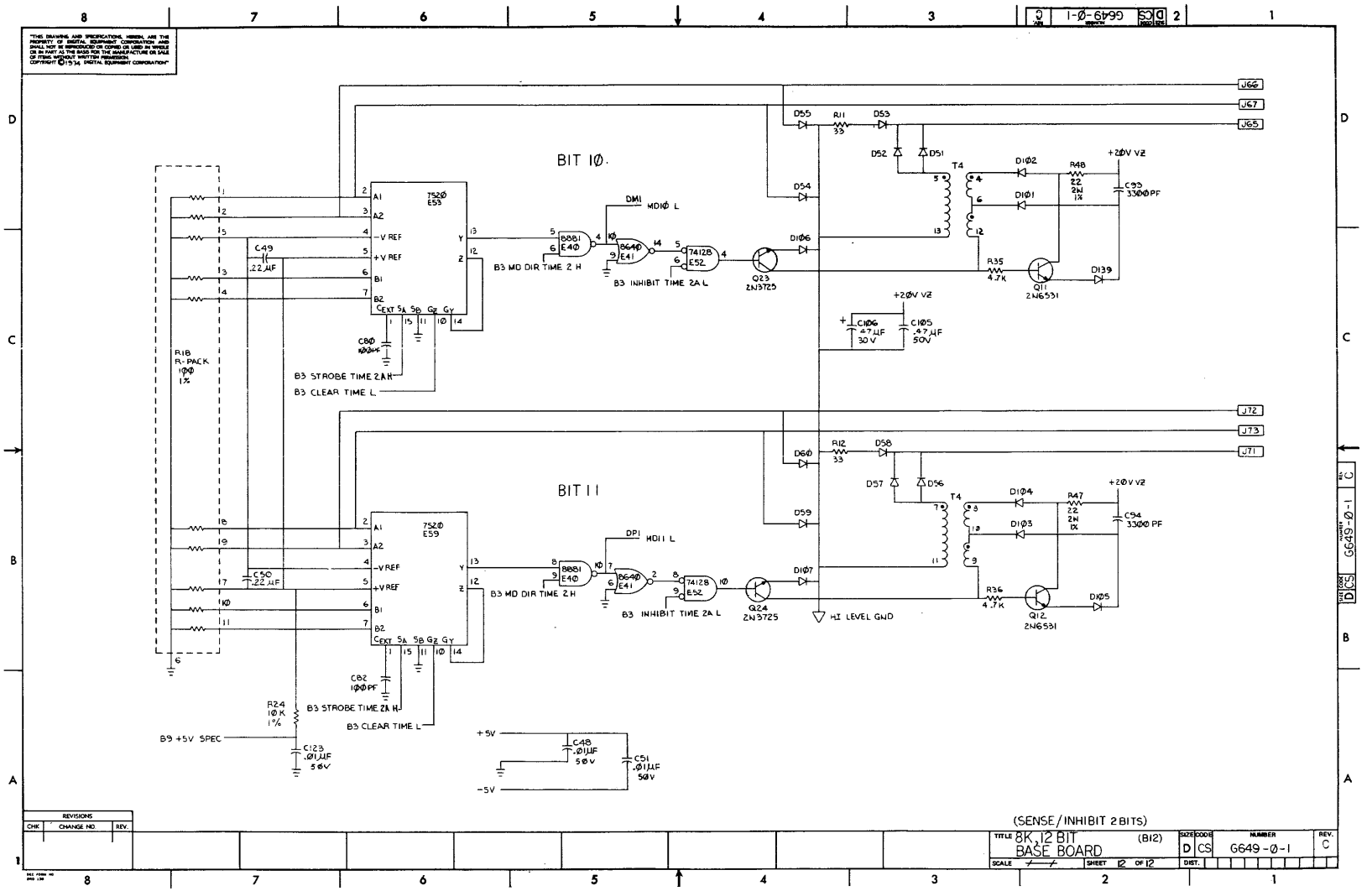

BIT Ø
BIT 1
(SENSE/INHIBIT 2 BITS)
8K 12 BIT BASE BOARD
G649-Ø-1
B3 INHIBIT TIME 2A L
B3 MD DIR TIME 2 H
B3 STROBE TIME 2A H
B3 CLEAR TIME L
B3 +5V SPEC
HI LEVEL GND
+20V VZ
+5V
-5V
NOTE:
ALL 1520 HAVE TYPICAL
INTERNAL CONFIGURATION
AND PINNING (EXAMPLE E6)


BIT 2
BIT 3
(SENSE/INHIBIT 2 BITS)
8K 12 BIT BASE BOARD
(88)
6649-0-1
B3 INHIBIT TIME 2A L
B3 MD DIR TIME 2 H
B3 STROBE TIME 2A H
B3 CLEAR TIME L
B9 +5V SPEC
H1 LEVEL GND
+20V V2
-5V
+5V


BIT 4
BIT 5
7520 E21
7520 E27
8881 E28
8640 E29
74128 E32
B3 MD DIR TIME 2 H
B3 INHIBIT TIME 2 A L
B3 STROBE TIME 2A H
B3 CLEAR TIME 2 L
B3 +5V SPEC
MD4 L
MD5 L
Q17 2N3725
Q18 2N3725
Q6 2N6531
Q5 2N6531
+20V VZ
HI LEVEL GND
(SENSE/INHIBIT 2 BITS)
8K J2 BIT BASE BOARD (B9)
G649-0-1
SIZE D
CODE CS
REV C
SHEET 9 OF 12


BIT 6
BIT 7
752Ø E38
752Ø E43
8881 E28
8640 E29
74128 E32
B3 MD DIR TIME 2 H
B3 INHIBIT TIME 2A L
B3 STROBE TIME 2A H
B3 CLEAR TIME L
B3 +5V SPEC
HI LEVEL GND
+2ØV VZ
R16 R-PACK 100 1%
C35 .22 µF
C36 .22 µF
C72 1ØØPF
C74 1ØØPF
C101 .47 µF 50V
C130 .47UF 50V
C102 .47µF 50V
C34 .Ø1µF 50V
C37 .Ø1µF 50V
Q19 2N3725
Q20 2N3725
Q7 2N6551
Q8 2N6551
R31 4.7K
R32 4.7K
R43 22 2W 1%
R44 22 2W 1%
C89 33ØØPF
C90 33ØØPF
R22 1ØK 1%
+5V
-5V
J40
J41
J39
J46
J47
J45
MD6 L
MD7 L
(SENSE / INHIBIT 2 BITS)
8K 12 BIT BASE BOARD (BIØ)
G649-Ø-1
SHEET 1Ø OF 12


BIT 8
BIT 9
J53
J54
J52
J59
J60
J58
D45
R9
33
D43
D42
D41
T3
D94
R45
22
2W
1%
C91
3300 PF
+20V VZ
D93
D44
D36
R33
4.7K
Q9
2N6531
D95
Q21
2N3725
C45
.22 µF
7520
E45
A1
A2
-V REF
+V REF
B1
B2
CEXT SA SB GZ GY
C76
100PF
B3 STROBE TIME 2A H
B3 CLEAR TIME L
R17
R-PACK
100
1%
DK1
MD8 L
8881
E40
8640
E41
74128
E52
B3 MD DIR TIME 2 H
B3 INHIBIT TIME 2A L
C103
.47µF
50V
C129
.47UF
50V
R10
33
D48
D47
D46
T4
D98
R46
22
2W
1%
C92
3300 PF
D50
D49
D97
D99
D100
R34
4.7K
Q10
2N6531
Q22
2N3725
C46
.22 µF
7520
E46
DL1
MD9 L
HI LEVEL GND
R23
10K
1%
B9 +5V SPEC
C78
100PF
+5V
-5V
C38
.01µF
50V
C104
.47µF
50V
C47
.01µF
50V
(SENSE / INHIBIT 2 BITS)
REVISIONS
CHK
CHANGE NO.
REV.
8K, 12 BIT (B11)
BASE BOARD
SIZE
CODE
NUMBER
REV.
D
CS
G649-0-1
C
SCALE
SHEET 11 OF 12
DIST.
DIGITAL
DCS - G649-0-1


BIT 10.
BIT 11
(SENSE/INHIBIT 2 BITS)
B3 STROBE TIME 2A H
B3 CLEAR TIME L
B3 MD DIR TIME 2 H
B3 INHIBIT TIME 2A L
B3 +5V SPEC
HI LEVEL GND
+20V VZ
-5V
R18 R-PACK 10Ø 1%
R24 10K 1%
C49 .22 µF
C50 .22 µF
C82 100PF
C123 .01 µF 50V
C48 .01µF 50V
C51 .01µF 50V
C106 47 µF 30V
C105 .47 µF 50V
C93 330ØPF
C94 330Ø PF
R48 22 2W 1%
R47 22 2W 1%
R35 4.7K
R36 4.7K
R11 33
R12 33
Q23 2N3725
Q24 2N3725
Q11 2N6531
Q12 2N6531
D139
D105
D107
D106
D104
D103
D102
D101
D100
D55
D53
D52
D51
D54
D58
D57
D56
D60
D59
J66
J67
J65
J72
J73
J71
T4
7520 E53
8881 E40
8640 E41
74128 E52
REVISIONS
CHK
CHANGE NO.
REV.
TITLE 8K, 12 BIT BASE BOARD (812)
SIZE D
CODE CS
NUMBER G649-Ø-1
REV. C
SCALE
SHEET 12 OF 12
DIST.

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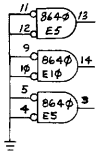
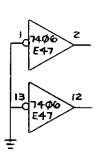
NOTES:

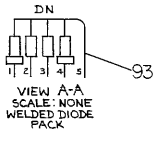
1. UNLESS OTHERWISE SPECIFIED:
   a. RESISTORS ARE 1/4W, ±5%
   b. CAPACITORS ARE 50V
   c. DIODES ARE D672
2. ALL RECEPTACLES ARE INDICATED WITH J NO'S.
3. COMP. C68, C104 NOT USED
4. DEFINITION OF MEMORY SELECTION JUMPERS

WITH JUMPERS IN LOCATIONS	MEMORY IS DECODED FOR ADDRESSES	MEMORY BANK SELECTED
1-1	Ø TO 16K	1ST 16K
2-2	16K TO 32K	2ND 16K
3-3	32K TO 48K	3RD 16K
4-4	48K TO 64K	4TH 16K

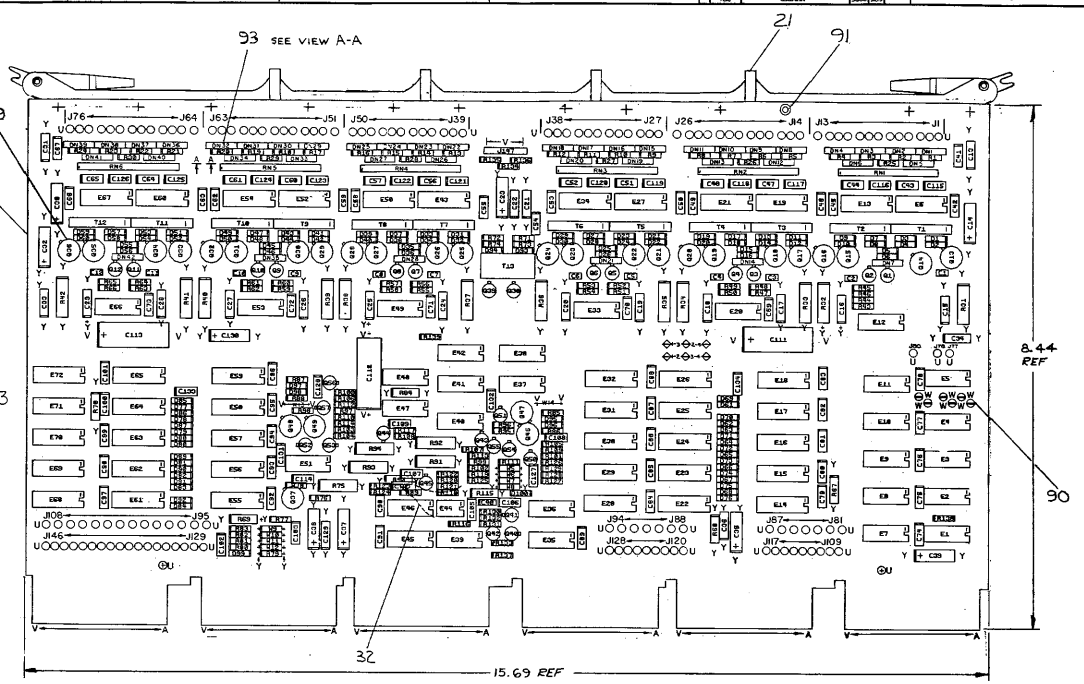


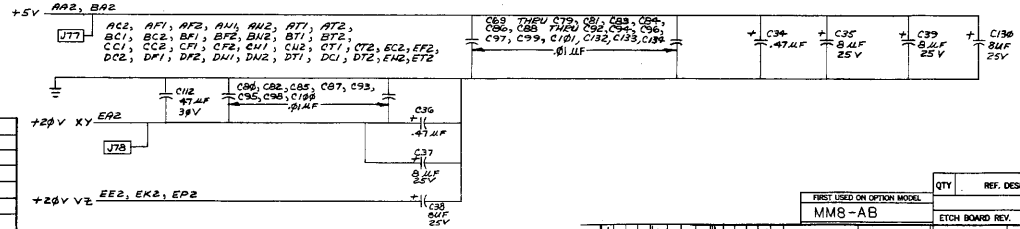
SPARES





VIEW A-A
SCALE: NONE
WELDED DIODE PACK





7532		8	9	16
7520	8	9	16	
8640		1	8	
7442		8	16	
72741		4		7
7384		1	8	
IC TYPE	-5V	GND	+5V	+20V

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

REV	CHANGE NO.	DESCRIPTION	DATE	APPROVED
C	G650-00001	C. GRANGER	7-25-75	
D	G650-00002	C. GRANGER	7-15-75	
E	G650-00003	C. GRANGER	7-31-75	

FIRST USED ON OPTION MODEL	ETCH BOARD REV.
MM8-AB	C

DEC NO.	EIA NO.	DEC NO.	EIA NO.

SEMICONDUCTOR CONVERSION CHART

QTY	REF. DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

DRD		DATE 7/17/75
CHK'D		DATE 8/1/75
ENGR		DATE 7/17/75
PROJ ENGR		DATE 7/10-24
PROD		DATE 7/10-24
NEXT HIGHER ASSY		
SCALE		
SHEET	1 OF 12	

digital

TITLE 16K, 12 BIT (81) BASE BOARD

SIZE	CODE	NUMBER	REV.
D	CS	G650-Ø-1	E

DIST.

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PARTS LIST				
QTY	REF DESIGNATIONS	DESCRIPTION	PART NO.	ITEM NO.
		X-Y COORDINATE HOLE LOCATION	K-CO-G650-0-4	1
		ASSY/DRILLING HOLE LAYOUT	D-MM-G650-0-5	2
		MODULE ECO HISTORY	B-MM-G650-0-6	3
		ETCHED CIRCUIT BOARD	5011418	4
1	C114	CAP 22PF 100V	1005820-00	5
1	C128	CAP 47PF 100V	1000011-00	6
1	C127	CAP 56PF 100V	1000012-00	7
12	C115-C126	CAP 100PF 50V	1000016-00	8
12	C1-C12	CAP 3300PF 50V	1011740-01	9
57	C81,C82,C85,C86,C89,C90 C93,C94,C95,C96,C97,C98 C63,C66,C67,C69-C103,C111 C105-C107,C112,C133,C134	CAP .01UF 50V	1001610-00	10
1	C40	CAP .022UF 50V	1011683-00	11
15	C43,C44,C47,C48,C51, C52,C56,C57,C60,C61, C64,C65,C108,C131,C109	CAP .22UF 50V	1010274-00	12
20	C13,C15-C22,C24-C29, C31,C33,C34,C36,C129	CAP .47UF 50V	1012312-00	13
9	C14,C23,C30,C32,C35 C37,C38,C39,C130	CAP 8UF 25V	1012084-01	14
3	C111-C113	CAP 47UF 30V	1012219-0-0	15
98	D1-D38	DIODE D672	1105275-00	16
1	D99	DIODE IN750A 4.7V ZENER	1100124-00	17
1	D100	DIODE IN759A 12V ZENER	1110836-00	18
42	DN1-DN42	DIODE ASSY	7010918-00	19
143	J1-J78, J80-J117, J120-J146	RECEPTACLE	1211728-00	20
		HANDLE, REWORK	7413182-00	21
1	J147	CONNECTOR 7 PIN	1212104-00	22
1	R90	RES 100 1/2W 5%	1300228-00	23
1	R133	RES 100 1/4W 5%	1300229-00	24
4	R67-R70	RES 300 1/2W 5%	1300291-00	25
1	R115	RES 330 1/2W 5%	1300296-00	26
1	R84	RES 1K 1/2W 1%	1300381-00	27
2	R111, R112	RES 3.3K 1/4W 5%	1300439-00	28
2	R85, R87	RES 10K 1/4W 5%	1300479-00	29
6	R73, R74, R113, R114, R122, R132,	RES 1.2K 1/4W 5%	1301320-00	30
2	R71, R72	RES 180 1/4W 5%	1301322-00	31
A/R		WIRE, #30 AWG SOLID GREEN	9105740-55	32
5	R116, R117, R118, R121, R138	RES 2K 1/4W 1%	1302715-00	33
1	R119	RES 825 1/4W 1%	1305143-00	34
2	R77, R78	RES 14.7K 1/4W 1%	1302941-00	35
1	R109	RES 1K 1/4W 1%	1303114-00	36
2	R86, R88	RES 3.48K 1/4W 1%	1305114-00	37
6	R95-R100	RES 75 1/4W 1%	1303064-00	38
1	R82	RES 34.8K 1/4W 1%	1303156-00	39
1	R139	RES 82K 1/4W 5%	1303219-00	40
5	R131, R107, R108, R106, R110	RES 562 1/4W 1%	1304693-00	41
1	R130	RES 5.11K 1/4W 1%	1304854-00	42
4	R101-R104	RES 383 1/4W 1%	1305125-00	43
2	R81, R128	RES 68.1K 1/4W 1%	1305252-00	44
1	R80	RES 121K 1/4W 1%	1305255-00	45
2	R123, R124	RES 4.99K 1/4W 1%	1305324-00	46
1	R83	RES 13.6K 1/4W 1%	1309419-00	47
1	R137	RES 1K THERMISTOR	1310071-00	48
4	R91-R94	RES 30 3W 1%	1311737-00	49

PARTS LIST				
QTY	REF DESIGNATIONS	DESCRIPTION	PART NO.	ITEM NO.
12	R31-R42	RES 22Ω, 2% FUSIBLE	1312502-01	50
6	RN1-RN6	RES R PACK 1/8W 1%	1311741-00	51
1	R75	RES 220 3W 1%	1312123-00	52
2	R120, R83	RES 1.21K 1/4W 1%	1302871-00	53
3	R126, R134, R135	RES 274K 1/4W 1%	1305131-00	54
1	R127	RES 137K 1/4W 1%	1305422-00	55
1	R129	RES 35.7K 1/4W 1%	1305421-00	56
1	R136	RES 2.37K 1/4W 1%	1310632-00	57
6	R25-R30	RES 10K 1/4W 1%	1303312-00	58
24	R43-R66	RES 4.7K 1/4W 5%	1300447-00	59
1	R76	RES 46.4K 1/4W 1%	1303311-00	60
1	R125	RES 5.62K 1/4W 1%	1305128-00	61
24	R1-R24	RES 33 1/4W 5%	1300197-00	62
28	Q13-Q26, Q46-Q49	TRANSISTOR 2N3725	1510959-00	63
1	Q27	TRANSISTOR 2N2904A	1501913-00	64
5	Q38-Q42	TRANSISTOR 3009B	1503100-00	65
4	Q50-Q53	TRANSISTOR 6534B	1503409-01	66
4	Q54-Q57	TRANSISTOR 4258	1505321-00	67
12	Q1-Q12	TRANSISTOR 6531B	1509338-00	68
3	Q43-Q45	TRANSISTOR MXAA55	1510706-00	69
1	T13	TRANSFORMER 1:1	1609996-00	70
12	T1-T12	TRANSFORMER 2:1	1612119-00	71
2	E37, E38	IC 74H40	1905586-00	72
1	E42	IC 74H10	1909057-00	73
2	E4, E41	IC 74H11	1909267-00	74
1	E48	IC 74H74	1909667-00	75
3	E7, E35, E45	IC 8881	1909705-00	76
6	E18, E26, E32, E59 E65, E72	IC 7442	1910046-00	77
1	E51	IC 74121	1910230-00	78
1	E44	IC 72741	1910298-00	79
2	E3, E9	IC 7384	1910393-00	80
1	E47	IC 7406	1910741-00	81
24	E10-E17, E22-E25 E28-E31, E55-E58 E61-E64, E68-E71	IC 75325	1910960-00	82
10	E1, E2, E5, E8, E10, E11 E36, E39, E40, E46	IC 8640	1911469-00	83
12	E6, E13, E19, E21, E27 E34, E43, E50, E52, E54 E60, E67	IC 7520	1911748-00	84
6	E12, E20, E33, E49 E53, E66	IC 74128	1912068-00	85
A/R	W1-W4	BUS WIRE #22 AWG	9107560-01	86
8	W5-W12	MACHINE INSERTED JUMPER	9009185-00	87
A/R	W13, W14	INSULATED WIRE #22 AWG	1700035-00	88
29		TRANSIPAD	9007201-00	89
6		EYELET (TERMINAL POSTS)	9006735-00	90
12		EYELET	9006732-00	91
1	R105	RES 464 1/4W 1%	1303067-00	92
84		DIODE ASSEMBLY SPACER	9107771-00	93
1	R79	RES 3.83K 1/4W 1%	1309413-00	94

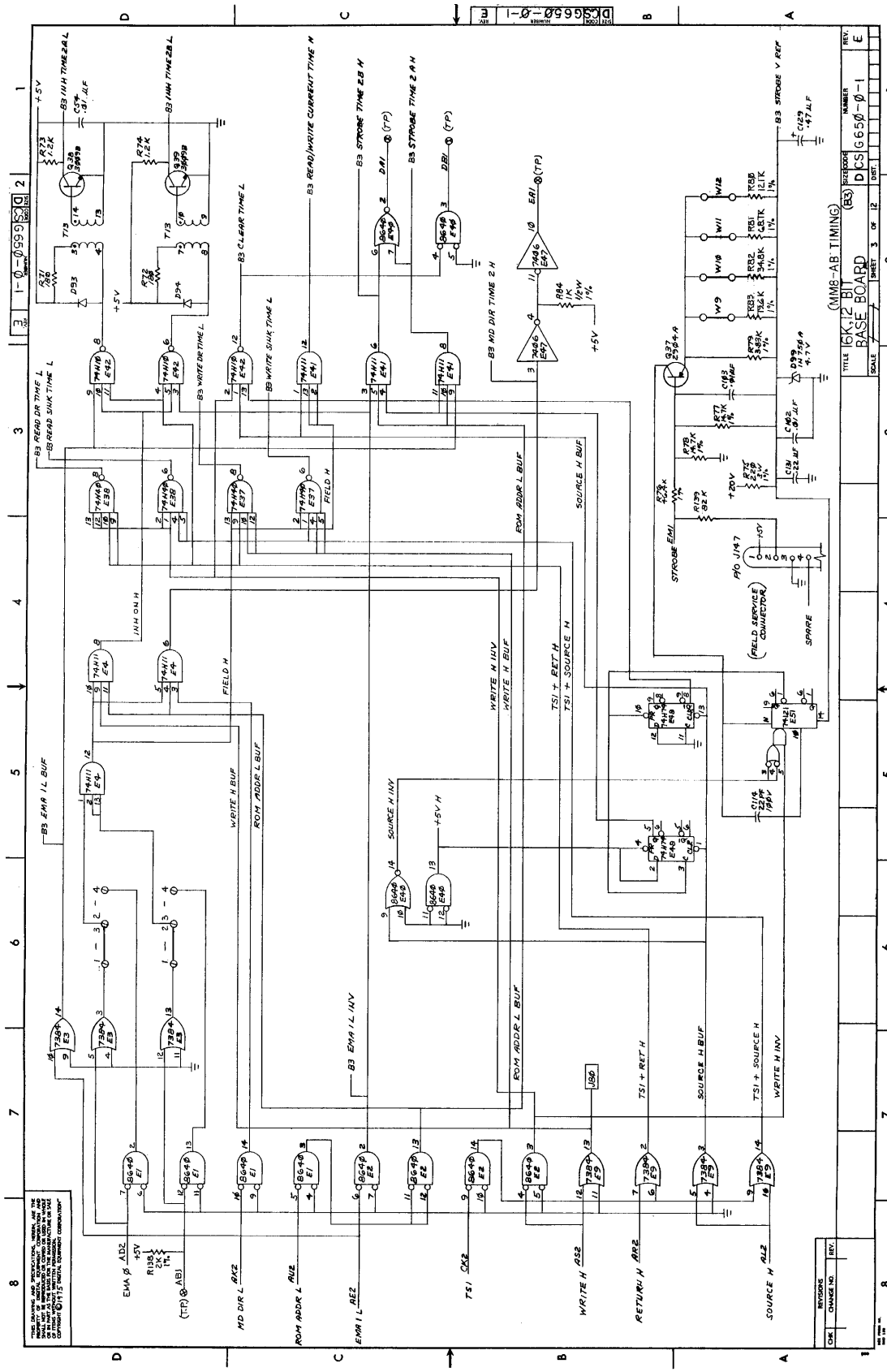
REVISIONS		
CHK	CHANGE NO.	REV.

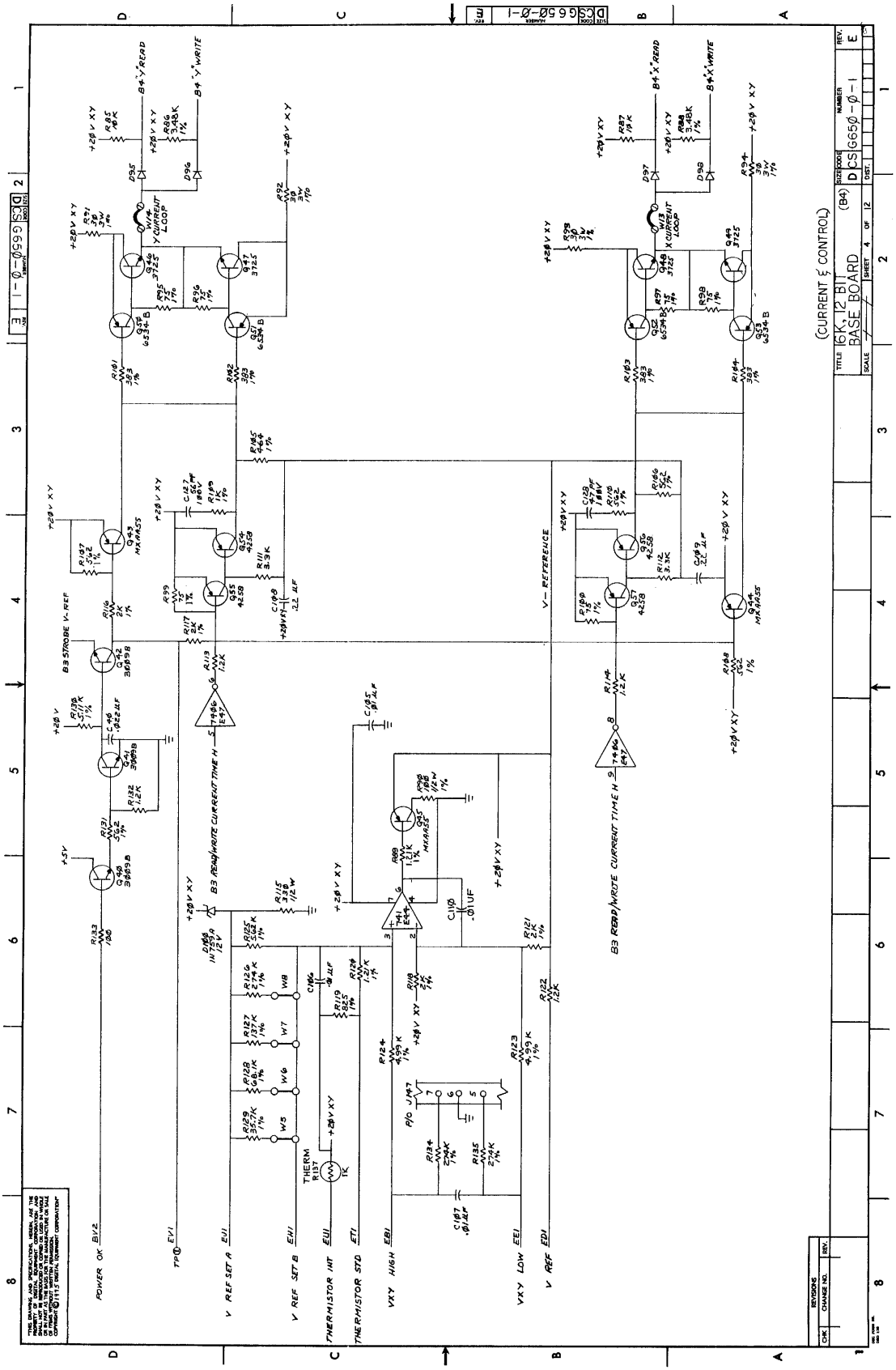
TITLE	16K, 12 BIT BASE BOARD	(B2)	SIZE	CODE	NUMBER	REV.
SCALE		SHEET 2 OF 12	D	CS	G650-0-1	E
			DIST.			

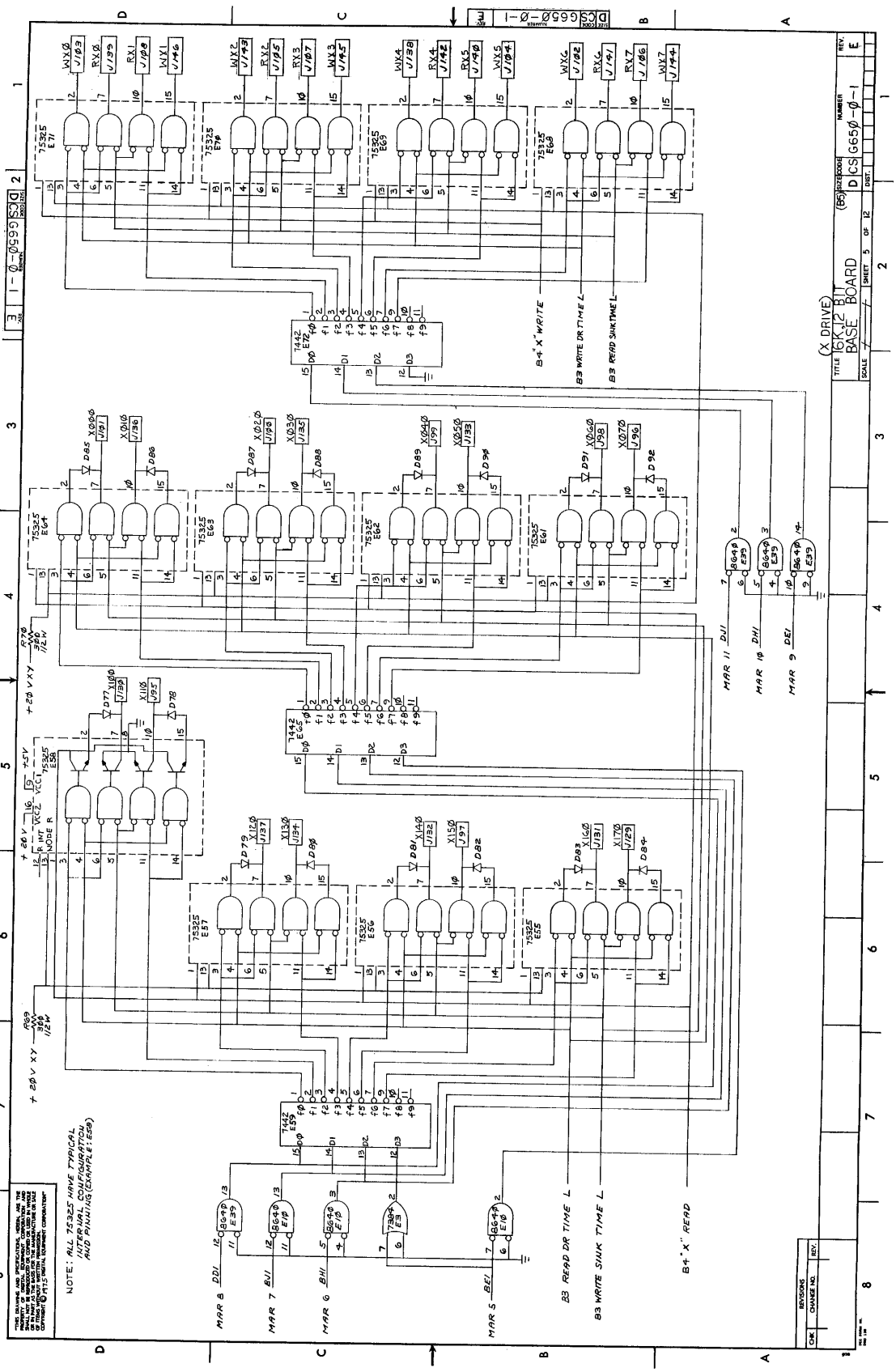
DEC FORM NO. 0140 130

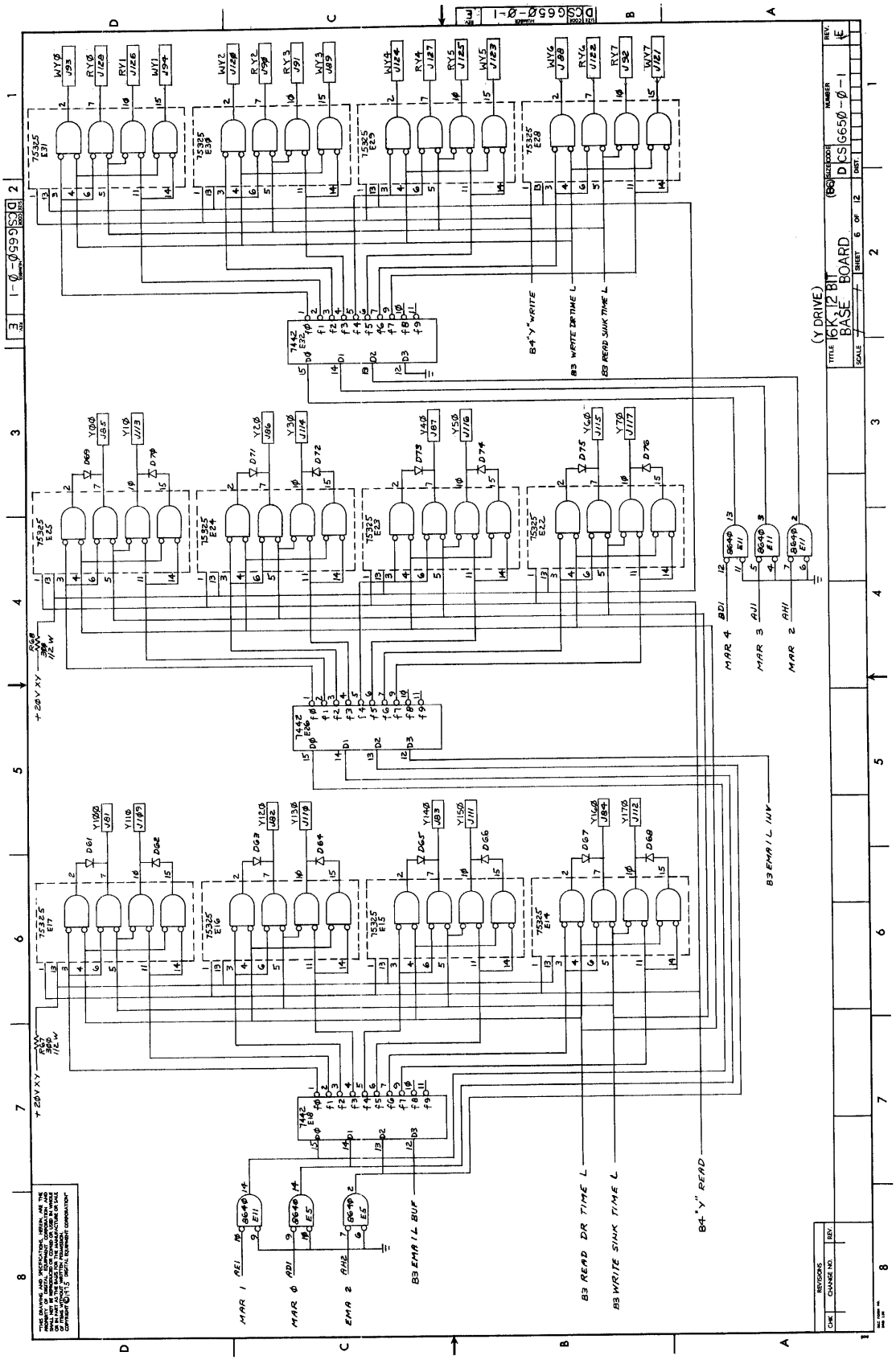
H-108

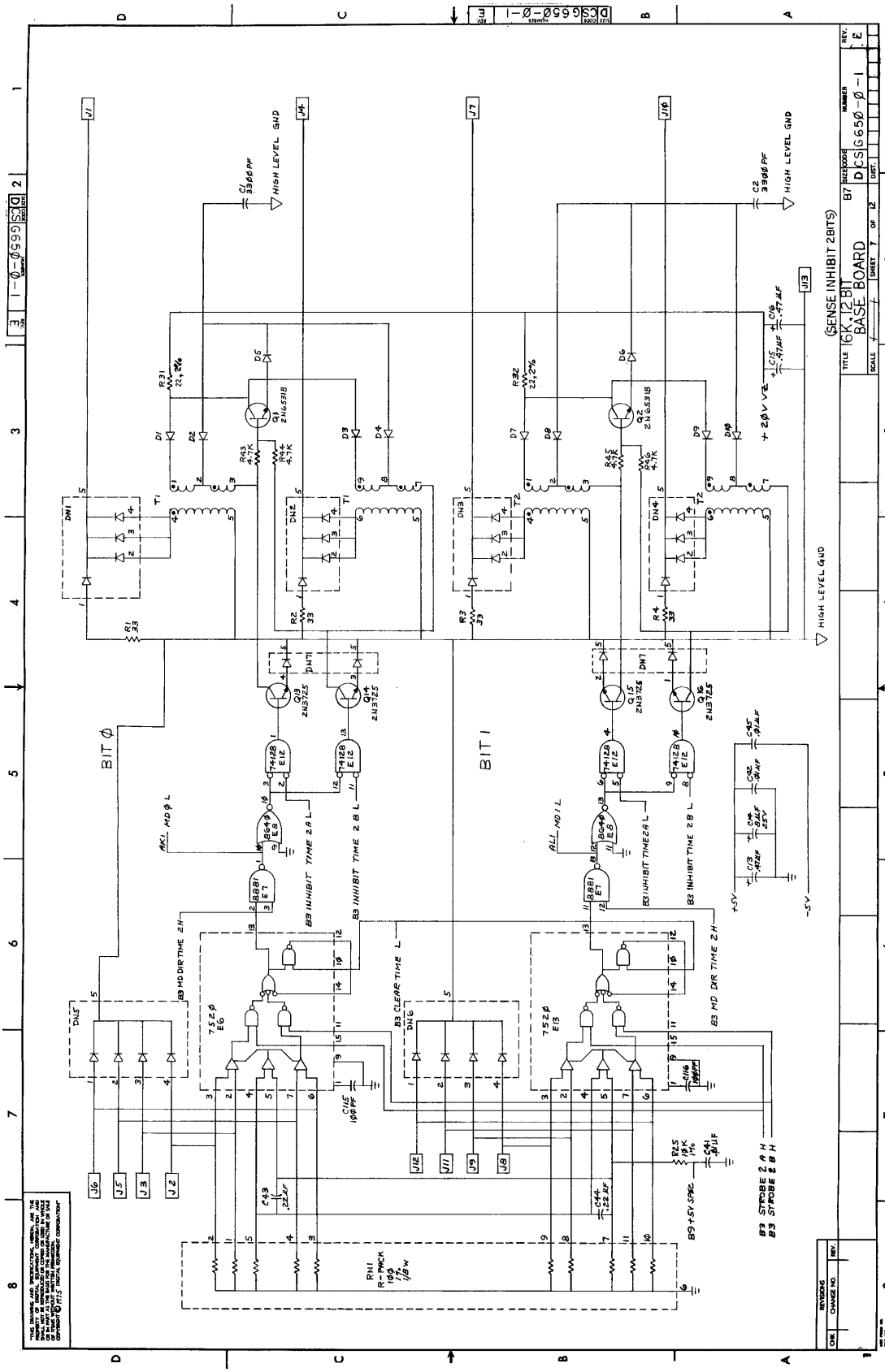
8 7 6 5 4 3 2 1

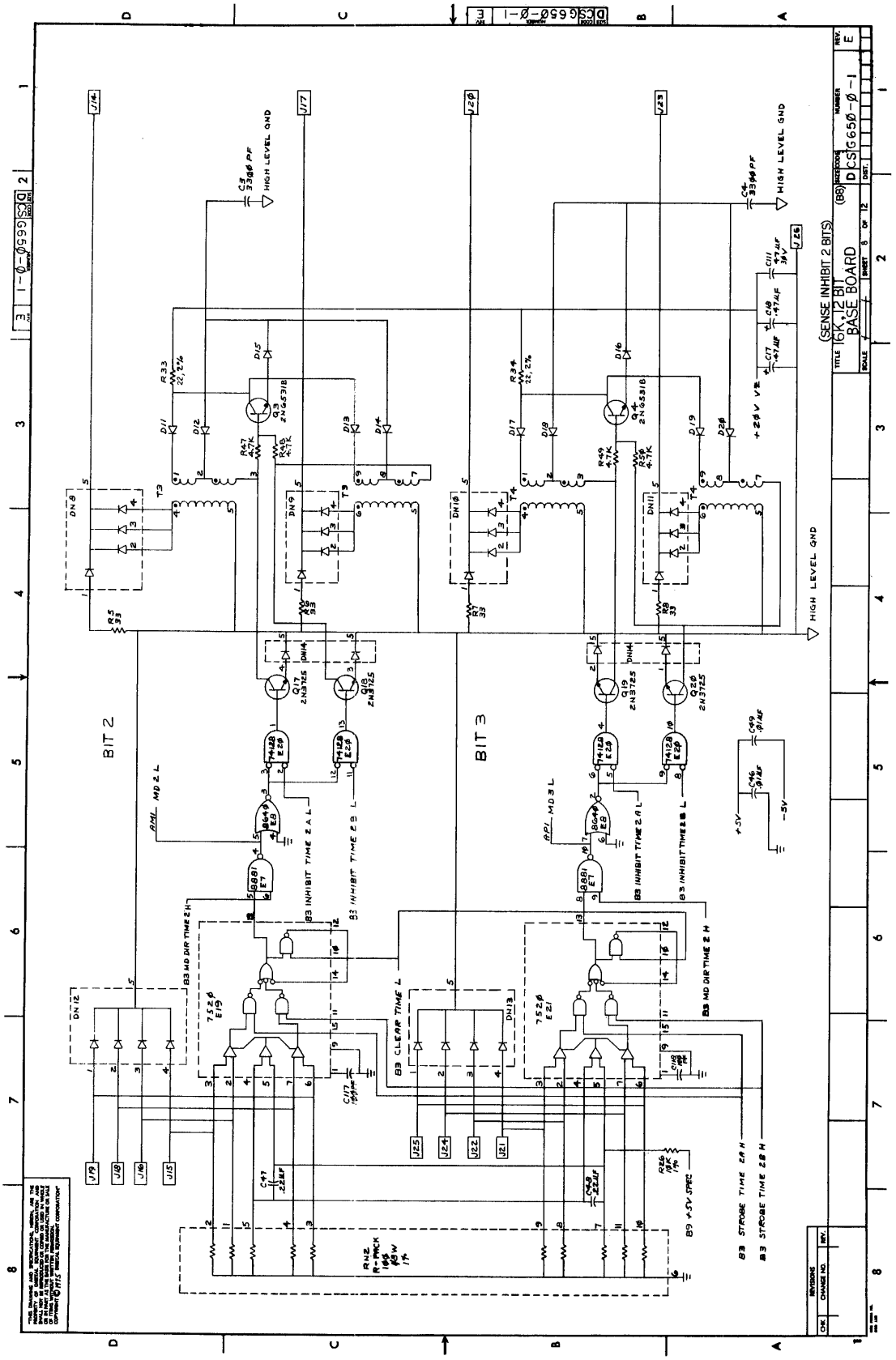


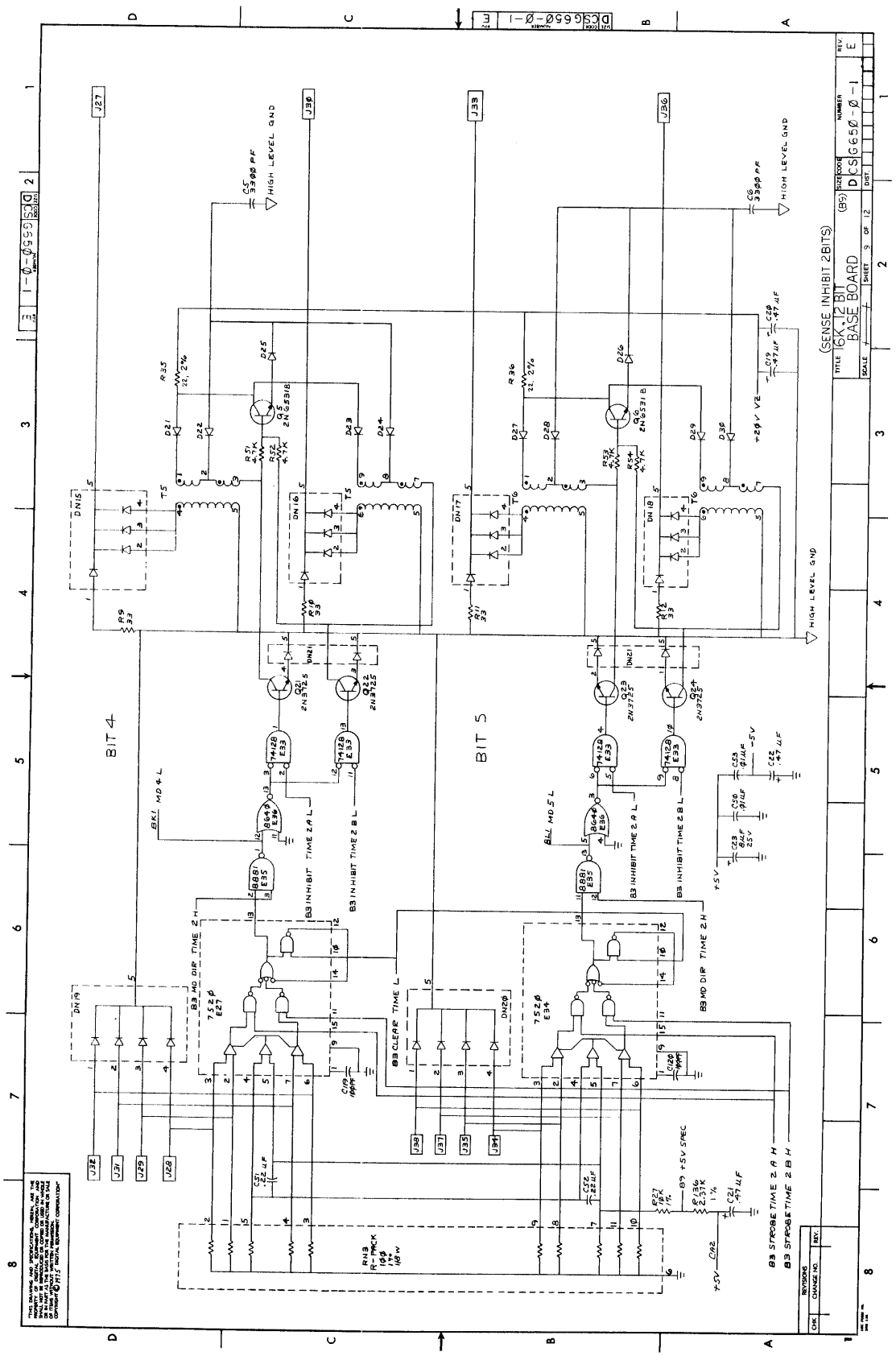

(CURRENT & CONTROL)
16K, 12 BIT
BASE BOARD
DCS(66)60-0-1
B3 READ/WRITE CURRENT TIME H
B3 STROBE V-REF
V- REFERENCE
POWER OK BV2
V REF SET A EVI
V REF SET B EHI
THERMISTOR INT EUI
THERMISTOR STD ETI
VXY HIGH EBI
VXY LOW EEI
V REF EDI
THERM R131
+5V
+15V
+29V XY
-15V

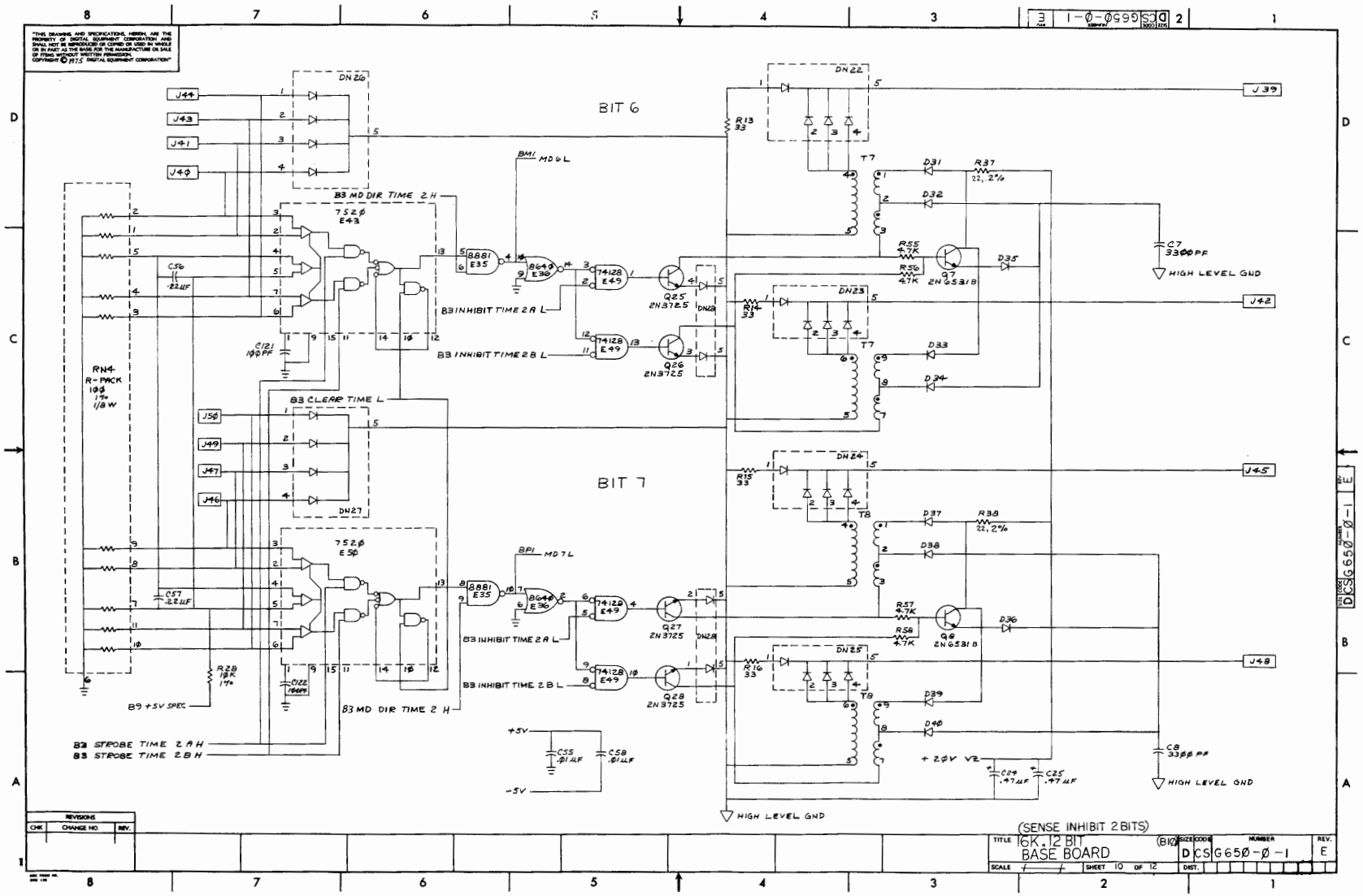

(X DRIVE)
16K 12 BIT
BASE BOARD
DCS 6650-0-1
NOTE: ALL 75325 HAVE TYPICAL
INTERNAL CONFIGURATION
AND PINNING (EXAMPLE: E58)
B4 "X" WRITE
B3 WRITE DR TIME L
B3 READ SHK TIME L
B4 "X" READ
B3 READ DR TIME L
B3 WRITE SHK TIME L
MAR 11 DJ1
MAR 10 DH1
MAR 9 DE1
MAR 8 DD1
MAR 7 BJ1
MAR 6 BH1
MAR 5 BE1
+20 V XY
+5V
+24 V
R NOT
NODE R

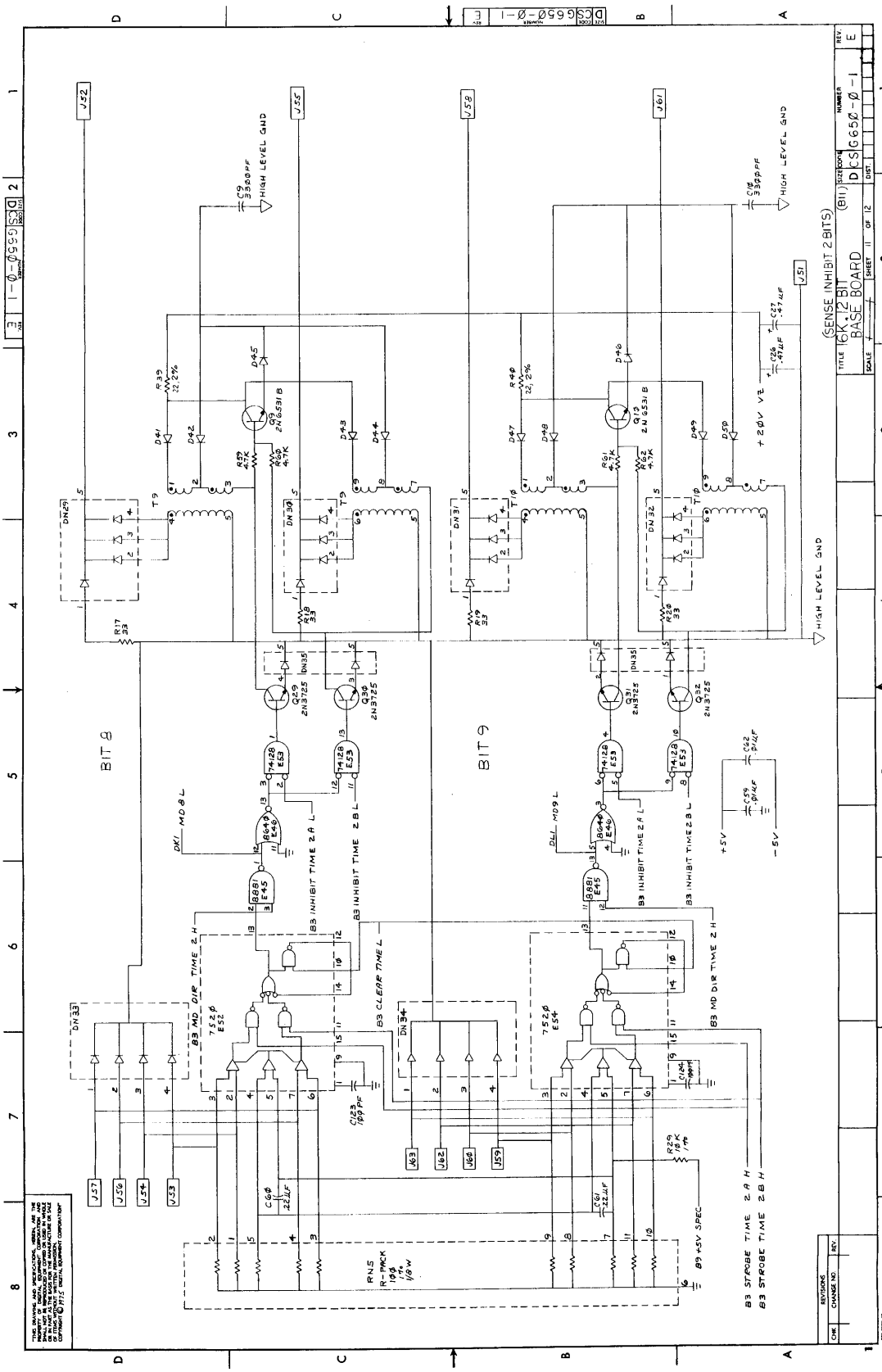

(Y DRIVE)
16K, 12 BIT
BASE BOARD
DCSG650-0-1
B4 "Y" WRITE
B3 WRITE DR TIME L
B3 READ SINK TIME L
B3 EMA I L BUF
B3 READ DR TIME L
B3 WRITE SINK TIME L
B4 "Y" READ
MAR 1
MAR 0
EMA 2
MAR 4
MAR 3
MAR 2
+26V XY

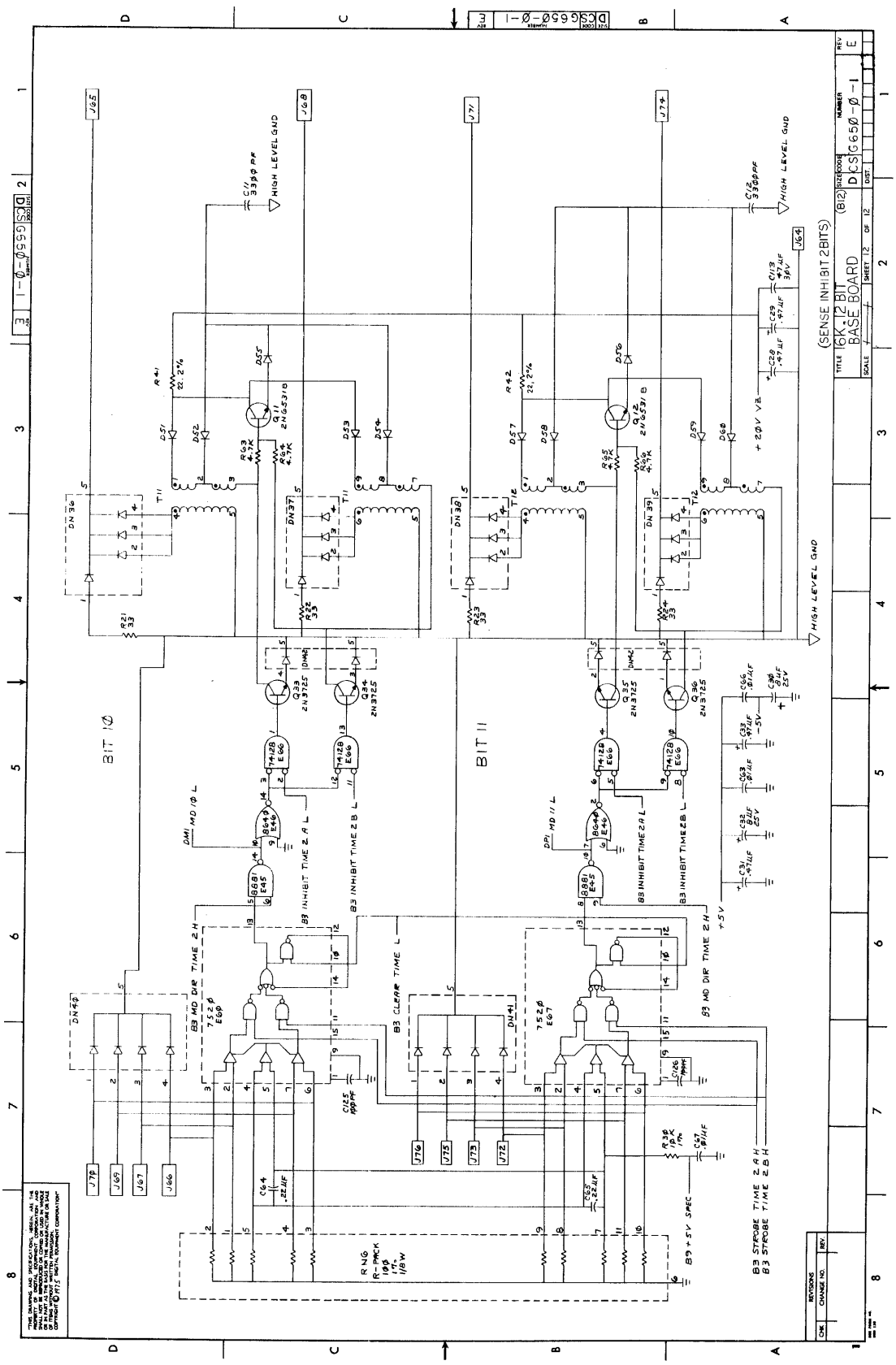

BIT Ø
BIT 1
(SENSE INHIBIT 2BITS)
16K, 12 BIT
BASE BOARD
DCSG650-Ø-1
HIGH LEVEL GND
+ 2Ø V VR
+5V
-5V
B3 INHIBIT TIME 2Ø L
B3 INHIBIT TIME 2Ø L
B3 INHIBIT TIME 2Ø L
B2 INHIBIT TIME 2Ø L
B3 MD DIR TIME 2H
B3 MD DIR TIME 2H
B3 CLEAR TIME L
MD Ø L
ALL MD 1 L
B3 STROBE 2 A H
B3 STROBE 2 B H
B9 +5V SPEC
RNI
R-PACK
16Ø
1/8W

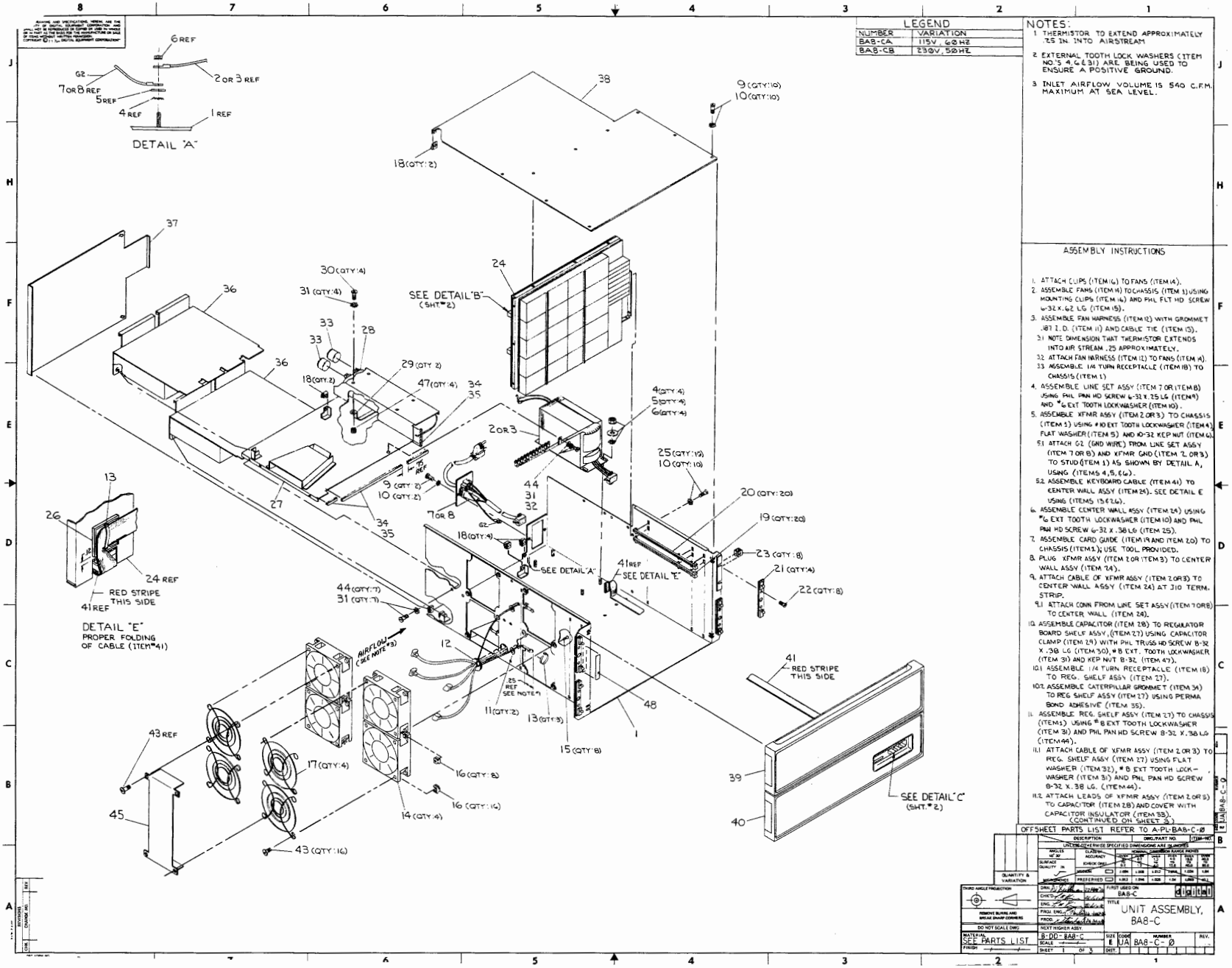

BIT 2
BIT 3
(SENSE INHIBIT 2 BITS)
16K, 12 BIT
BASE BOARD
DCSG650-0-1
HIGH LEVEL GND
+5V
-5V
B3 INHIBIT TIME 2 A L
B3 INHIBIT TIME 2 B L
B3 MD DIR TIME 2 H
B3 CLEAR TIME L
B3 STROBE TIME 2 A H
B3 STROBE TIME 2 B H
B9 +5V SPEC


(SENSE INHIBIT 2BITS)
16K-12 BIT
BASE BOARD
DCSG650-0-1
BIT 4
BIT 5
B3 INHIBIT TIME 2 A L
B3 INHIBIT TIME 2 B L
B3 MD DIR TIME 2 H
B3 CLEAR TIME L
B3 STROBE TIME 2 A H
B3 STROBE TIME 2 B H
HIGH LEVEL GND
+5V SPEC
-5V


BIT 6
BIT 7
J44
J43
J41
J40
J56
J49
J47
J46
DN26
DN27
B3 MD DIR TIME 2 H
B3 CLEAR TIME L
B3 INHIBIT TIME 2A L
B3 INHIBIT TIME 2B L
BMI MD 6 L
BPI MD 7 L
RN4
R-PACK
10Ω
1%
1/8 W
C56 .22 μF
C121 100 PF
C57 .22 μF
C122 100 PF
R28 18K 1%
B9 +5V SPEC
B2 STROBE TIME 2A H
B3 STROBE TIME 2B H
+5V
-5V
C55 .01 μF
C58 .01 μF
DN22
DN23
DN24
DN25
R13 33
R14 33
R15 33
R16 33
J39
J42
J45
J48
T7
T8
T9
D31
D32
D33
D34
D35
D36
D37
D38
D39
D40
R37 22, 2%
R38 22, 2%
R55 4.7K
R56 4.7K
R57 4.7K
R58 4.7K
Q7 2N6531B
Q8 2N6531B
Q25 2N3725
Q26 2N3725
Q27 2N3725
Q28 2N3725
C7 3300 PF
C8 3300 PF
HIGH LEVEL GND
+20V V2
C24 .47 μF
C25 .47 μF
8881 E35
8640 E36
74128 E49
7520 E43
7520 E50
DN28
(SENSE INHIBIT 2 BITS)
6K, 12 BIT BASE BOARD
(BI)
D CS G650-0-1
E
SHEET 10 OF 12
REVISIONS
CHK
CHANGE NO.
REV.


BIT 8
BIT 9
(SENSE INHIBIT 2 BITS)
16K 2 BIT
BASE BOARD
DCSG650-0-1
HIGH LEVEL GND
+20V VR
+5V
-5V
B3 INHIBIT TIME 2 A L
B3 INHIBIT TIME 2 B L
B3 CLEAR TIME L
B3 MD DIR TIME 2 H
B3 STROBE TIME 2 A H
B3 STROBE TIME 2 B H
B9 +5V SPEC
R.N.S.
R-PACK
10Ω
1/8 W


BIT 10
BIT 11
(SENSE INHIBIT 2 BITS)
16K, 12 BIT
BASE BOARD
DCSG650-0-1
HIGH LEVEL GND
+20V
+5V
B3 MD DIR TIME 2 H
B3 CLEAR TIME L
B3 INHIBIT TIME 2 A L
B3 INHIBIT TIME 2 B L
B3 STROBE TIME 2 A H
B3 STROBE TIME 2 B H
B3 +5V SPEC
R NG
R-PACK
10Ω
1%
1/8W



LEGEND	
NUMBER	VARIATION
BA8-CA	115V, 60 HZ
BA8-CB	230V, 50 HZ

NOTES:
1. THERMISTOR TO EXTEND APPROXIMATELY .25 IN. INTO AIRSTREAM
2. EXTERNAL TOOTH LOCK WASHERS (ITEM NO'S 4 & 6) ARE BEING USED TO ENSURE A POSITIVE GROUND.
3. INLET AIRFLOW VOLUME IS 540 C.F.M. MAXIMUM AT SEA LEVEL.

ASSEMBLY INSTRUCTIONS

1. ATTACH CLIPS (ITEM 4) TO FANS (ITEM 14).
2. ASSEMBLE FANS (ITEM 14) TO CHASSIS (ITEM 1) USING MOUNTING CLIPS (ITEM 4) AND PHL FLT HD SCREW 6-32 X .62 LG (ITEM 15).
3. ASSEMBLE FAN HARNESS (ITEM 12) WITH GROMMET .187 I.D. (ITEM 11) AND CABLE TIE (ITEM 13).
3.1 NOTE DIMENSION THAT THERMISTOR EXTENDS INTO AIR STREAM .25 APPROXIMATELY.
3.2 ATTACH FAN HARNESS (ITEM 12) TO FANS (ITEM 14).
3.3 ASSEMBLE 1/4 TURN RECEPTACLE (ITEM 18) TO CHASSIS (ITEM 1)
4. ASSEMBLE LINE SET ASSY (ITEM 7 OR ITEM 8) USING PHL PAN HD SCREW 6-32 X .25 LG (ITEM 9) AND #6 EXT TOOTH LOCKWASHER (ITEM 10).
5. ASSEMBLE XFMR ASSY (ITEM 2 OR 3) TO CHASSIS (ITEM 1) USING #10 EXT TOOTH LOCKWASHER (ITEM 4), FLAT WASHER (ITEM 5) AND 10-32 KEP NUT (ITEM 6).
5.1 ATTACH G2 (GND WIRE) FROM LINE SET ASSY (ITEM 7 OR 8) AND XFMR GND (ITEM 2, OR 3) TO STUD (ITEM 1) AS SHOWN BY DETAIL A, USING (ITEMS 4, 5, & 6).
5.2 ASSEMBLE KEYBOARD CABLE (ITEM 41) TO CENTER WALL ASSY (ITEM 24). SEE DETAIL E USING (ITEMS 13 & 24).
6. ASSEMBLE CENTER WALL ASSY (ITEM 24) USING #6 EXT TOOTH LOCKWASHER (ITEM 10) AND PHL PAN HD SCREW 6-32 X .38 LG (ITEM 25).
7. ASSEMBLE CARD GUIDE (ITEM 19 AND ITEM 20) TO CHASSIS (ITEM 1). USE TOOL PROVIDED.
8. PLUG XFMR ASSY (ITEM 2 OR ITEM 3) TO CENTER WALL ASSY (ITEM 24).
9. ATTACH CABLE OF XFMR ASSY (ITEM 2 OR 3) TO CENTER WALL ASSY (ITEM 24) AT J10 TERM. STRIP.
9.1 ATTACH CONN FROM LINE SET ASSY (ITEM 7 OR 8) TO CENTER WALL (ITEM 24).
10. ASSEMBLE CAPACITOR (ITEM 28) TO REGULATOR BOARD SHELF ASSY. (ITEM 27) USING CAPACITOR CLAMP (ITEM 29) WITH PHL TRUSS HD SCREW 8-32 X .38 LG (ITEM 30), #8 EXT. TOOTH LOCKWASHER (ITEM 31) AND KEP NUT 8-32 (ITEM 47).
10.1 ASSEMBLE 1/4 TURN RECEPTACLE (ITEM 18) TO REG. SHELF ASSY (ITEM 27).
10.2 ASSEMBLE CATERPILLAR GROMMET (ITEM 34) TO REG SHELF ASSY (ITEM 27) USING PERMA BOND ADHESIVE (ITEM 35).
11. ASSEMBLE REG. SHELF ASSY (ITEM 27) TO CHASSIS (ITEM 1) USING #8 EXT TOOTH LOCKWASHER (ITEM 31) AND PHL PAN HD SCREW 8-32 X .38 LG (ITEM 44).
11.1 ATTACH CABLE OF XFMR ASSY (ITEM 2 OR 3) TO REG. SHELF ASSY (ITEM 27) USING FLAT WASHER (ITEM 32), #8 EXT TOOTH LOCK-WASHER (ITEM 31) AND PHL PAN HD SCREW 8-32 X .38 LG. (ITEM 44).
11.2 ATTACH LEADS OF XFMR ASSY (ITEM 2 OR 3) TO CAPACITOR (ITEM 28) AND COVER WITH CAPACITOR INSULATOR (ITEM 33).
(CONTINUED ON SHEET 3)

OFFSHEET PARTS LIST REFER TO A-PL-BA8-C-Ø

| | | |

MODULE ASSIGNMENT AND POWER REQUIREMENTS

OPTION	DESCRIPTION	BOARD SIZE	NO. SLOTS USED	ASSIGNED SLOT NO.	CURRENT +5V	+15V	-15V
CM8-F	CARD RDR CONT.	QUAD	1	4 – 20	55A	—	—
CR8-F	CARD RDR CONT.		1	4 – 20	55A	—	—
DB8-EA	INTERPROC. BUFFER		1	2 – 20	.80A	—	.03A
DK8-EC	RTC. CRYSTAL		1	2 – 20	.34A	—	—
DK8-EP	RTC. PROG.	QUAD	2	2 – 20	1.43A	—	.07A
DKC8-A	OPTION*1	HEX	1	2 – 3	2.0A	.06A	1A
DP8-EA-EB	MODEM INTERFACE	QUAD	2	2 – 20	1.80A	.05A	11A
DR8-EA	DIGITAL I/O	QUAD	1	2 – 20	2.25A	—	—
KA8-E	POSITIVE I/O	QUAD	1	4 – 20	1.40A	—	—
KC8-AA,-AB	PROG. CONSOLE	PNL. MT.	0	N.A	2.5A	—	—
KD8-E	DATA BREAK	QUAD	1	4 – 20	1.2A	—	—
KG8-EA	REDUNDANCY CHECK	QUAD	1	4 – 20	.94A	—	—
KK8-A	C.P.U.	HEX	1	1	5.0A	—	.04A
KL8-JA	ASYNC. DATA CONT.	QUAD	1	2 – 20	1.1A	.05A	10A
KL8-M	MODEM CONTROL	QUAD	1	2 – 20	.40A	.04A	.04A
KM8-AA OR-AB	OPTION*2	HEX	1	2 – 3	2.0A	—	—
KM8-E	MEM.EXT. & T.S. CONT.	QUAD	1	4 – 20	1.0A	—	—
LE8-XX	LPØ5 CONTROL	QUAD	1	2 – 20	.35A	—	—
LS8-F	LSØ1 CONTROL	QUAD	1	2 – 20	.40A	—	—
MM8-AA	8K CORE, OPERATING	HEX	2	4 – 11	2.5A	—	—
MM8-AA	8K CORE, STANDBY	HEX	2	4 – 11	2.5A	—	—
MM8-AB	16K CORE, OPERATING	HEX	2	4 – 11	2.5A	—	—
MM8-AB	16K CORE, STANDBY	HEX	2	4 – 11	2.5A	—	—
MR8-AA	1K ROM	QUAD	1	2 – 20	2.0A	—	—
MR8-AB	2K ROM		1	2 – 20	3.0A	—	—
MR8-AC	3K ROM		1	2 – 20	4.0A	—	—
MR8-AD	4K ROM		1	2 – 20	5.0A	—	—
MR8-FB	1K PROM		1	2 – 20	3.8A	—	.35A
MS8-AA	1K RAM		1	4 – 20	1.4A	—	—
MS8-AB	2K RAM		1	4 – 20	2.1A	—	—
MS8-AC	3K RAM		1	4 – 20	2.8A	—	—
MS8-AD	4K RAM		1	4 – 20	3.5A	—	—
PC8-E,PR8-E	PC04 CONTROL		1	4 – 20	.84A	—	Ø5A
RX8-E	RXØ1 CONTROL		1	4 – 20	1.5A	—	—
RK8-EA	RKØ5 CONTROL		3	4 – 20	3.ØA	—	—
TA8-AA	TUGØ CONTROL		1	2 – 20	2.8ØA	—	—
TM8-EA,-FA	TUIØ CONTROL		4	4 – 20	4.ØA	—	—
VC8-E	DISPLAY CONTROL		2	2 – 20	.31A	—	—
VT8-E	DISPLAY CONTROL		3	4 – 20	3.70A	.09A	.13A
XY8-E	PLOTTER CONTROL		1	4 – 20	42A	ØIA	.03A
KK8-E	M83ØØ, MAJOR REG.		1	*18	1.7A	—	—
	M83IØ, MAJOR REG. CONT.		1	*19	.6ØA	—	—
	M8330, TIMING GEN.		1	*20	1.2A	—	—
	M8320, BUS LOAD		1	1	1.0A	1ØA	.53A
AD8-A	A/D CONV.	QUAD	1	4 – 20	3.25A	—	—
FPP8-A	FLOATING POINT	HEX	2	4 – 20	.88A	—	—
KE8-E	M8340, EAE IR		1	*19	1.6A	—	—
	M8341, EAE REG		1	*18	—	—	—
KL8-A	MSLU	HEX	1	4 – 20	2.5A	Ø9A	.425A
LA8-P	LAI80 CONT.	QUAD	1	4 – 20	1.0A	—	—
MI8-E	BOOT LOADER	QUAD	1	4 – 20	.75A	—	.05A
RK8-L	RKØ5 CONT.	QUAD	2	4 – 20	3.5A	—	—
TD8-E	TU56 CONT.	QUAD	1	4 – 20	1.3A	—	—
VK8-A	VIDEO DISPLAY CONT.	HEX	1	4 – 20	2.8A	—	—

* WITH KE8-E OPTION, M83ØØ & M83IØ MUST BE MOVED TO SLOTS 16 & 17 RESPECTIVELY. THE KE8-E OPTION PLUGS INTO SLOTS 18 & 19 (M8341 & M8340)

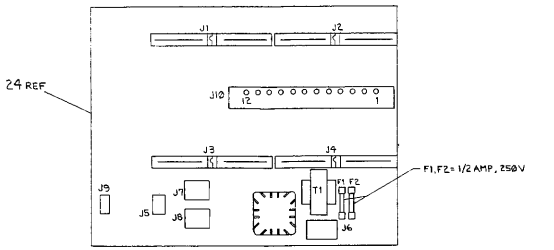
AVAILABLE CURRENT:

SLOTS* 1 THRU 10

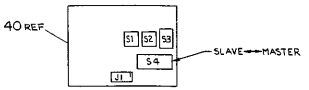
+5V	-15V	+15V
25A (MAX.)	2A (MAX.)	2A (MAX.)

SLOTS* 11 THRU 20

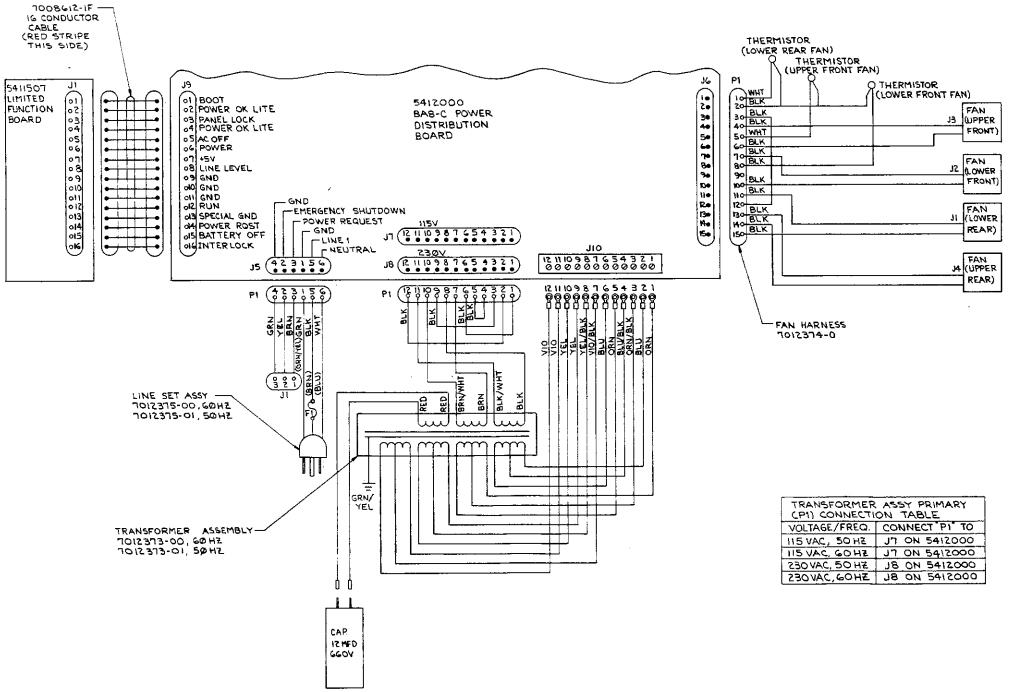
+5V	-15V	+15V
25A (MAX.)	2A (MAX.)	2A (MAX.)



DETAIL "B"
JACK LOCATIONS ON POWER DISTRIBUTION BOARD OF CENTER WALL ASSEMBLY (ITEM#24)



DETAIL "C"
SWITCH LOCATIONS ON LIMITED FUNCTION BOARD OF PANEL ASSY (ITEM#40)



TRANSFORMER ASSY PRIMARY (P1) CONNECTION TABLE

VOLTAGE/FREQ.	CONNECT "P1" TO
115 VAC, 50 HZ	J7 ON 5412000
115 VAC, 60 HZ	J7 ON 5412000
230 VAC, 50 HZ	J8 ON 5412000
230 VAC, 60 HZ	J8 ON 5412000

REVISIONS

DATE	CHANGE NO.	ECO

TITLE: UNIT ASSEMBLY, BA8-C
SIZE/CODE: E UA
NUMBER: BA8-C-Ø
REV.
SCALE
SHEET 2 OF 3
DIST.

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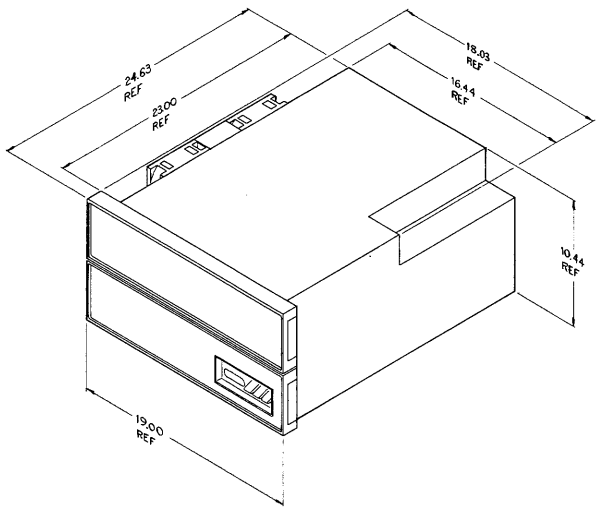
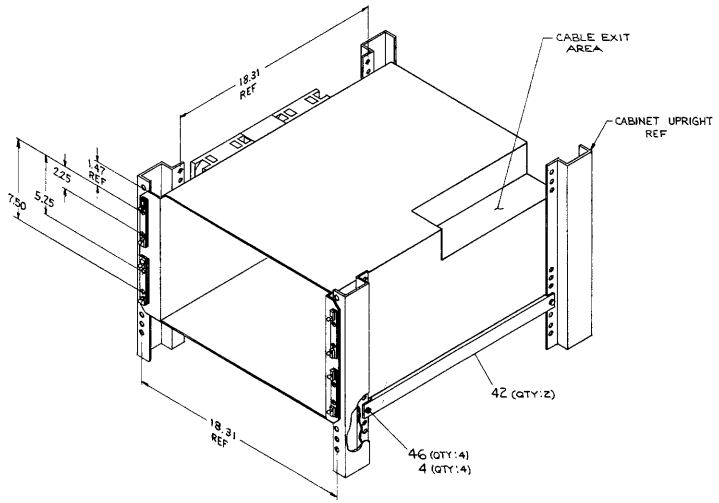


MAX. UNIT WEIGHT = 117 LBS.

MOUNTING INSTRUCTIONS

1. SEE DETAIL "D" FOR MOUNTING DIMENSIONS.
2. REMOVE THE BLANK BEZEL ASSEMBLY OR PROGRAMMER'S PANEL.
3. REMOVE THE LIMITED FUNCTION PANEL AND DISCONNECT THE CABLE FROM THE LIMITED FUNCTION BOARD.
4. REMOVE THE LATCH MOLDING (4 PLCS)
5. REMOVE THE SPEED NUT, AND INSTALL ON CAB UPRIGHT. EIGHT PLACES PER MOUNTING DIMENSIONS.
6. IT MAY BE NECESSARY TO REMOVE THE FINGER GUARDS (4) AND HARNESS COVER IN ORDER TO MOUNT BOX IN CAB.
7. ATTACH MOUNTING RAILS USING SCREWS AND LOCK WASHERS TO LEFT AND RIGHT SIDE OF CABINET AS PER DETAIL "D"
8. WITH THE BOX IN PLACE, IN THE CABINET, REPLACE THE LATCH MOLDING, SO AS TO SECURE THE BOX TO THE CABINET.
9. PLUG THE CABLE INTO THE LIMITED FUNCTION PANEL AND REPLACE THE PANEL.
10. REPLACE BLANK BEZEL OR PROGRAMMER'S PANEL
11. RE-INSTALL FINGER GUARDS AND HARNESS COVER.



DETAIL "D"
MOUNTING DIMENSIONS

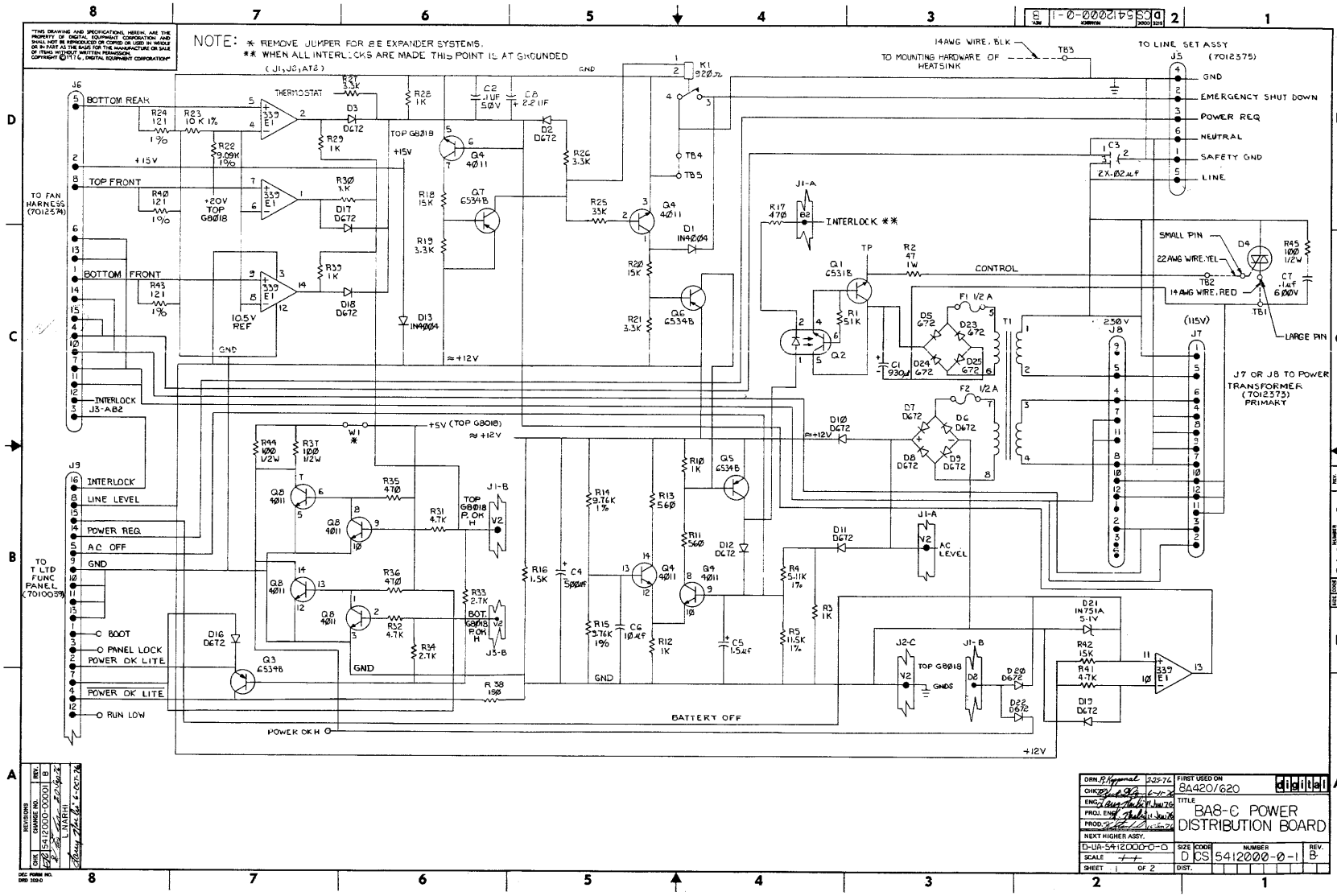
ASSEMBLY INSTRUCTIONS CONTINUED

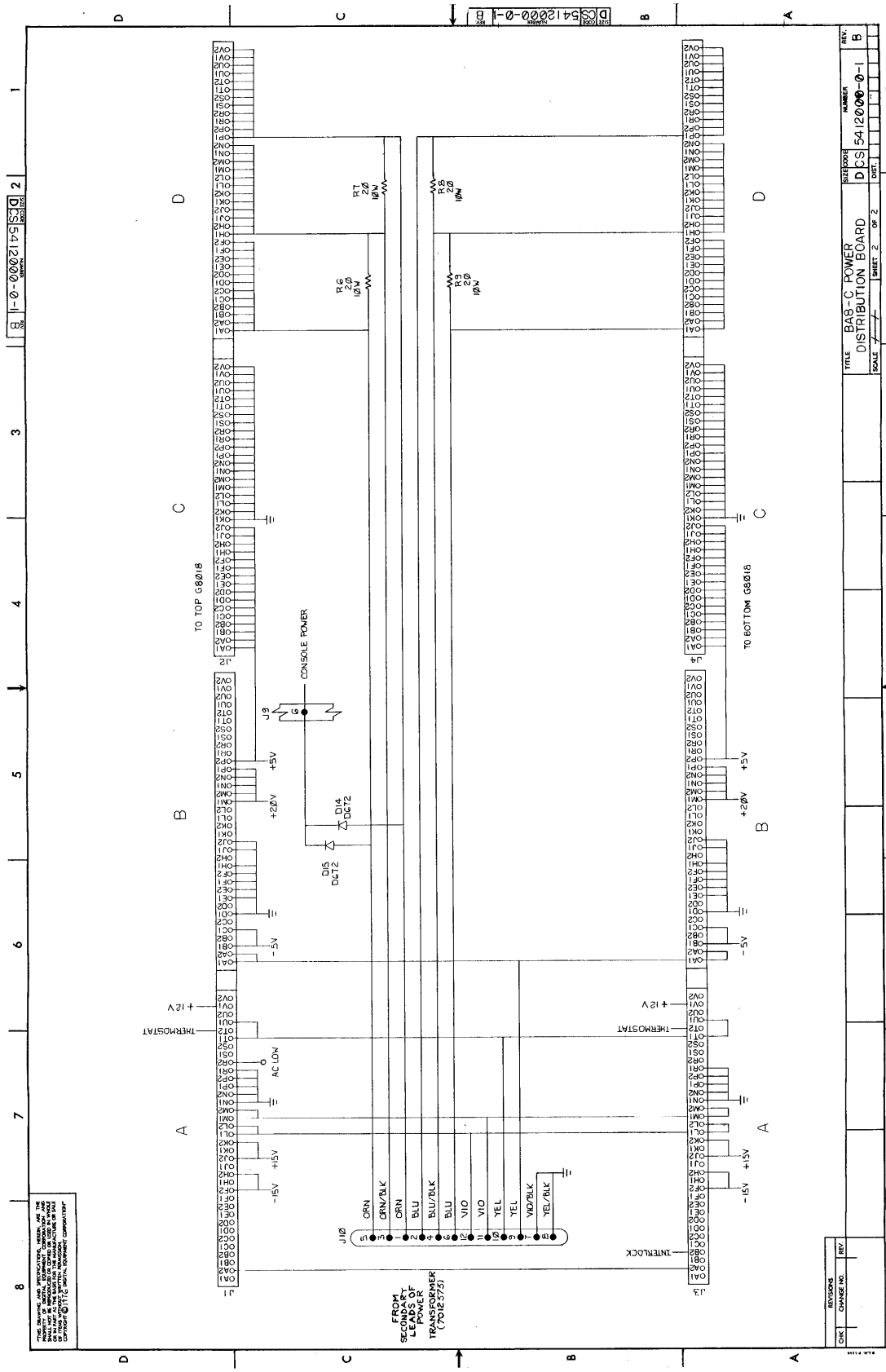
12. INSERT LOWER G80IB (ITEM 34) TO CHASSIS (ITEM 1) AND CENTER WALL ASSY (ITEM 24).
12.1 INSERT UPPER G80IB (ITEM 34) TO REG SHELF ASSY (ITEM 27) AND CENTER WALL ASSY (ITEM 24).
13. ADD 1/4 TURN RECEPTACLE (ITEM 18) TO TOP COVER (ITEM 38).
14. ASSEMBLE TOP COVER (ITEM 38) TO CHASSIS (ITEM 1) USING #6 EXT TOOTH LOCKWASHER (ITEM 10) AND PHL PAN HD SCREW 6-32 X .25 LG (ITEM 9).
15. ASSEMBLE REAR COVER (ITEM 37) TO CHASSIS (ITEM 1).
16. ASSEMBLE LATCH MOLDING (ITEM 21) TO CHASSIS (ITEM 1) USING 10-32 SPEED NUT (ITEM 23) AND PHL FLAT HD SCREW 10-32 X .75 LG (ITEM 22).
17. ATTACH KEYBOARD CABLE (ITEM 41) TO LIMITED FUNCTION PANEL (ITEM 40).
18. ATTACH 5 1/4 BLANK BEZEL ASSY (ITEM 39) TO CHASSIS (ITEM 1).
19. ASSEMBLE HARNESS COVER (ITEM 45) AND FINGER GUARD (ITEM 17) TO FANS (ITEM 19) USING MOUNTING CLIP (ITEM 16) AND PHL PAN HD SCREW 6-32 X .62 LG (ITEM 43).

REVISIONS		
CHR	CHANGE NO	REV

TITLE	SIZE/CODE	NUMBER	REV.
UNIT ASSEMBLY, BA8-C	E UA	BA8-C-Ø	
SCALE	SHEET 3 OF 3	DIST.	

BA8-C-Ø


NOTE: * REMOVE JUMPER FOR 8E EXPANDER SYSTEMS.
** WHEN ALL INTERLOCKS ARE MADE THIS POINT IS AT GROUNDED (J1,J2,AT2)
14AWG WIRE, BLK
TO MOUNTING HARDWARE OF HEATSINK
TO LINE SET ASSY (7012375)
GND
EMERGENCY SHUT DOWN
POWER REQ
NEUTRAL
SAFETY GND
LINE
2X-02uF
THERMOSTAT
BOTTOM REAR
TOP FRONT
BOTTOM FRONT
INTERLOCK J3-A82
TO FAN HARNESS (7012574)
+15V
+5V (TOP G8018)
≈+12V
+12V
10.5V REF
+20V TOP G8018
INTERLOCK **
CONTROL
SMALL PIN
22AWG WIRE, YEL
14AWG WIRE, RED
LARGE PIN
230V
(115V)
J7 OR J8 TO POWER TRANSFORMER (7012572) PRIMARY
INTERLOCK
LINE LEVEL
POWER REQ
A.C. OFF
GND
TO T LTD FUNC PANEL (7010039)
C BOOT
PANEL LOCK
POWER OK LITE
POWER OK LITE
RUN LOW
POWER OK H
BATTERY OFF
AC LEVEL
TOP G8018 P. OK H
BOT. G8018 P.OK H
TOP G8018 GNDS
DRN. R.Kopperud 3-25-74
CHK. 4-1-74
ENG. 4-1-74
PROJ. ENG. 4-Jun-74
PROD. 4-Jun-74
NEXT HIGHER ASSY. D-UA-5412000-0-0
SCALE —
SHEET 1 OF 2
FIRST USED ON BA420/620
TITLE BA8-C POWER DISTRIBUTION BOARD
SIZE D CODE DCS NUMBER 5412000-0-1 REV. B
DIST.
REVISIONS REV. B CHANGE NO. 5412000-00001 CHK. 27-MAR-74


TO TOP G8018
TO BOTTOM G8018
CONSOLE POWER
J9
D14
D15
D6T2
+5V
+20V
-5V
+12V
THERMOSTAT
AC LOW
+15V
-15V
INTERLOCK
J10
ORN
ORN/BLK
BLU
BLU/BLK
VIO
YEL
VIO/BLK
YEL/BLK
FROM SECONDARY LEADS OF POWER TRANSFORMER (70125735)
R6 2Ω 10W
R7 2Ω 10W
R8 2Ω 10W
R9 2Ω 10W
J1
J2
J3
J4
TITLE BA8-C POWER DISTRIBUTION BOARD
SIZE D
CODE DCS
NUMBER 5412000-0-1
REV. B
SCALE
SHEET 2 OF 2
DIST.
REVISIONS
CHK
CHANGE NO.
REV.
5412000-0-1 B
DCS 5412000-0-1 B

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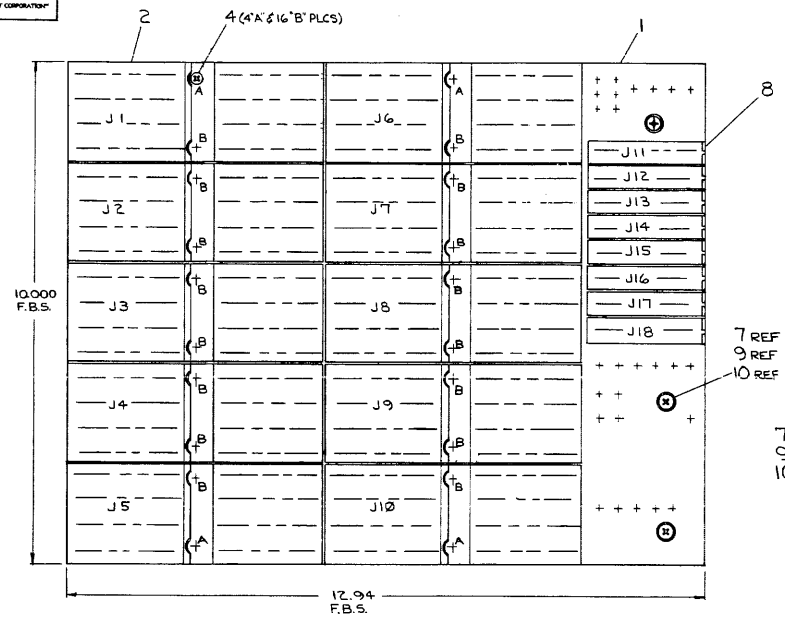

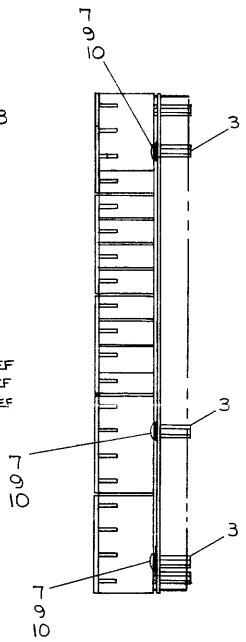

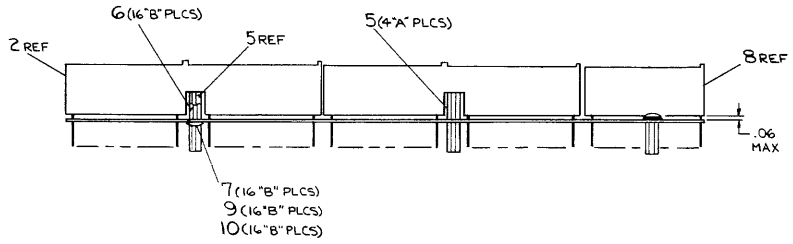

NOTES:

OFFSHEET PARTS LIST REFER TO B-PL-H9195-0-0

DESCRIPTION	DWG./PART NO. / ITEM NO.
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	
ANGLES ±0° 30'	NOMINAL DIMENSION RANGE INCHES
CLASS OF ACCURACY (CHECK ONE)	OVER 0 TO 4.0 / OVER 4.0 TO 12.0 / OVER 12.0 TO 40.0 / OVER 40.0 TO 80.0
SURFACE QUALITY IN MICROINCHES	MEDIUM ☐ ±.004 ±.008 ±.063 ±.016 ±.024 ±.04
	PREFERRED ☐ ±.012 ±.016 ±.025 ±.04 ±.063 ±0.1
QUANTITY & VARIATION	
THIRD ANGLE PROJECTION	DRN. / CHK. / ENG. / PROJ. ENG. / PROD.
REMOVE BURRS AND BREAK SHARP CORNERS	NEXT HIGHER ASSY.
DO NOT SCALE DWG	
MATERIAL SEE PARTS LIST	E-UA-BA8-C-0
FINISH	SCALE
	SHEET 1 OF

FIRST USED ON BA8-C

digital

TITLE BACKPLANE, 20 SLOT

SIZE D | CODE UA | NUMBER H9195-0-0 | REV. D | DIST.

REVISIONS	REV.	CHANGE NO.	CHK

DEC FORM M3 DWG 100-C

PDP-8A MINIPROCESSOR
USERS MANUAL
EK-8A002-MM-002

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