

PDP-15 SYSTEMS
MX15
MEMORY BUS MULTIPLEXER
MAINTENANCE MANUAL
VOLUME 2

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DIGITAL	COMPUTER LAB

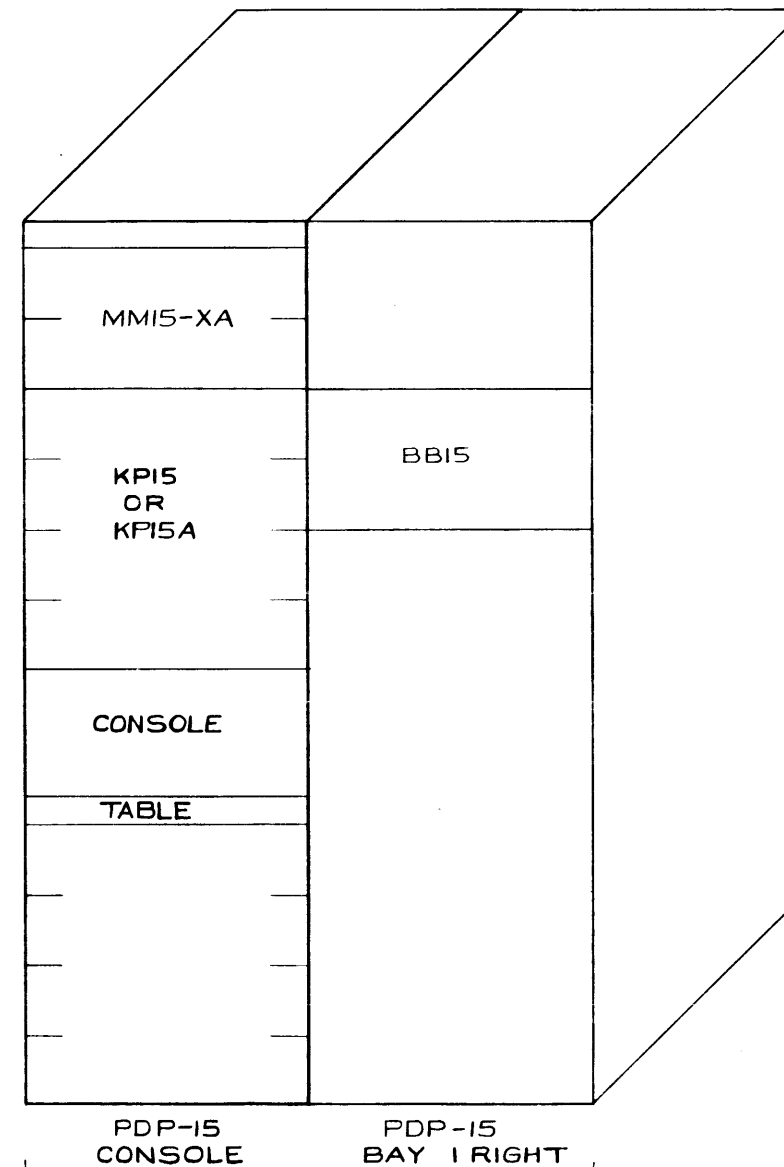
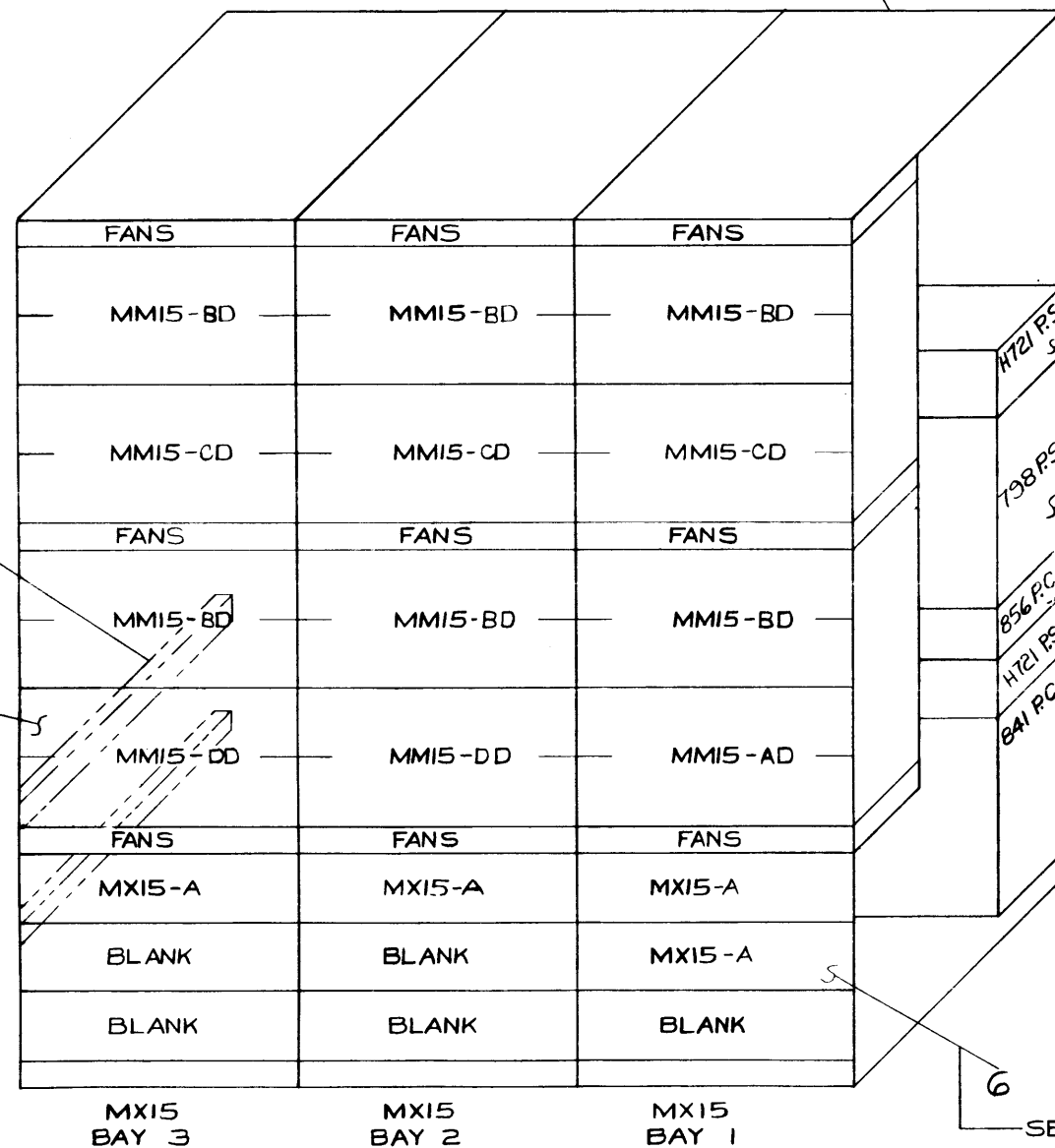
ENGINEERING DRAWINGS

Engineering Drawing List	
Drawing No.	Title
D-AD-7006863-0-0	MX15 Maximum Configuration
D-UA-MX15-0-0	MX15 Assembly
D-BS-MX15-A-12	Priority Logic Input Port 1
D-BS-MX15-A-13	Priority Logic Input Port 2
D-BS-MX15-A-14	Priority Logic Input Port 3
D-BS-MX15-A-15	MDL 03, 04 Drivers, M REQ Logic
D-BS-MX15-A-16	Control Lines
D-BS-MX15-A-17	MDL 0-8
D-BS-MX15-A-18	MDL 9-17, Parity
D-BS-MX15-A-19	Inhibit Logic
D-IC-MX15-A-20	Memory Port Out
D-IC-MX15-A-21	Memory Port 1
D-IC-MX15-A-22	Memory Port 2
D-IC-MX15-A-23	Memory Port 3
D-AD-7006862-0-0	Wired Assembly (MX15-A)
D-UA-841-B-0	Power Control 841-B, 841-C
D-CS-H721-0-1	H721 Power Supply Circuit Schematic
B-CS-798-0-1	798 Dual 15-Volt Power Supply Schematic
15-0409	856 Power Control

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NOTES:

1. WHEN A MM15 IS INCLUDED IN A BAY, THE ADDITION OF A 798 P.S. AND AN 856 P.C. IS REQUIRED. WHEN ADDING A SECOND MM15 TO THE BAY, THE ADDITION OF A SECOND H721 P.S. AND A SECOND POWER DISTRIBUTION BAR IS REQUIRED.
2. ONLY BAY 1 CAN HAVE 2 MX15-A WIRED ASSEMBLIES.
3. FOR DRAWING INDEX LIST, REFER TO: D-DI-7006863-0-1.



SHOWN FOR
REFERENCE ONLY

REV	DATE	DESCRIPTION
1	3/10/70	INITIAL DESIGN
2	5/15/70	REVISION
3	5/15/70	REVISION
4	5/15/70	REVISION
5	5/15/70	REVISION

FIRST USED ON OPTION/MODEL
MX15

DO NOT SCALE DRAWING UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES TOLERANCES DECIMALS FRACTIONS ANGLES ± .005 ± 1/64 ± 0°30' FINAL SURFACE QUALITY REMOVE BURRS AND BREAK SHARP CORNERS	DATE 3/10/70 DATE 5/15/70 DATE 5/15/70 DATE 5/15/70 DATE 5/15/70
MATERIAL SEE PARTS LIST	PROJ. ENG. J. C. HAY PROJ. 3/10/70
FINISH	SCALE 1 OF 4 SHEET 1 OF 4

QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST			
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS			
TITLE MX15 MAXIMUM CONFIGURATION			
SIZE CODE	NUMBER	REV	
DAD	7006863-0-0	A	
DIST.			

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NOTES FOR CABLING:

1. IN MX15 PORT LOCATIONS ARE AS FOLLOWS:

PORT 1 (HIGHEST PRIORITY)

A26-A27

B26-B27

PORT 2 (MIDDLE PRIORITY)

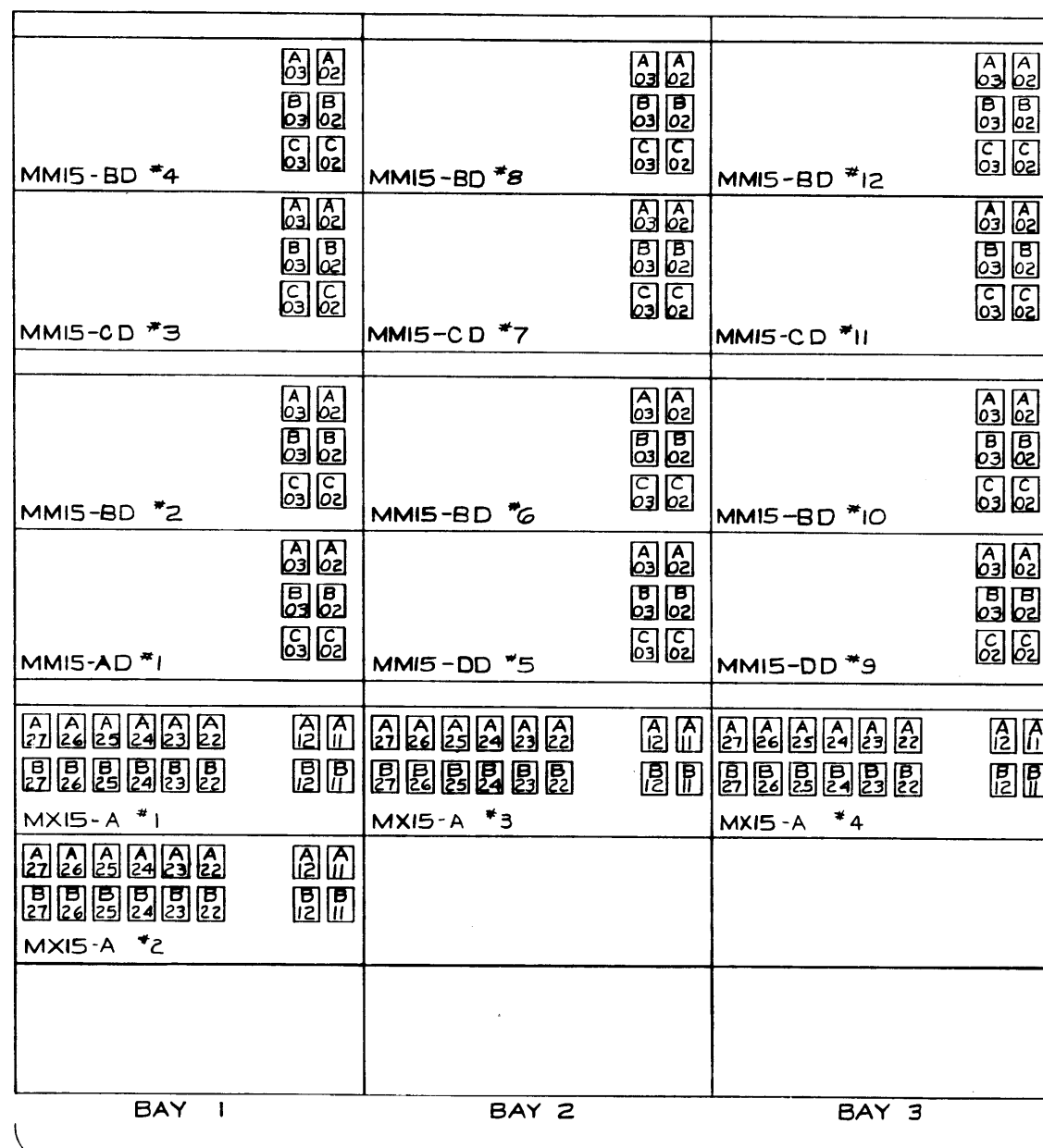
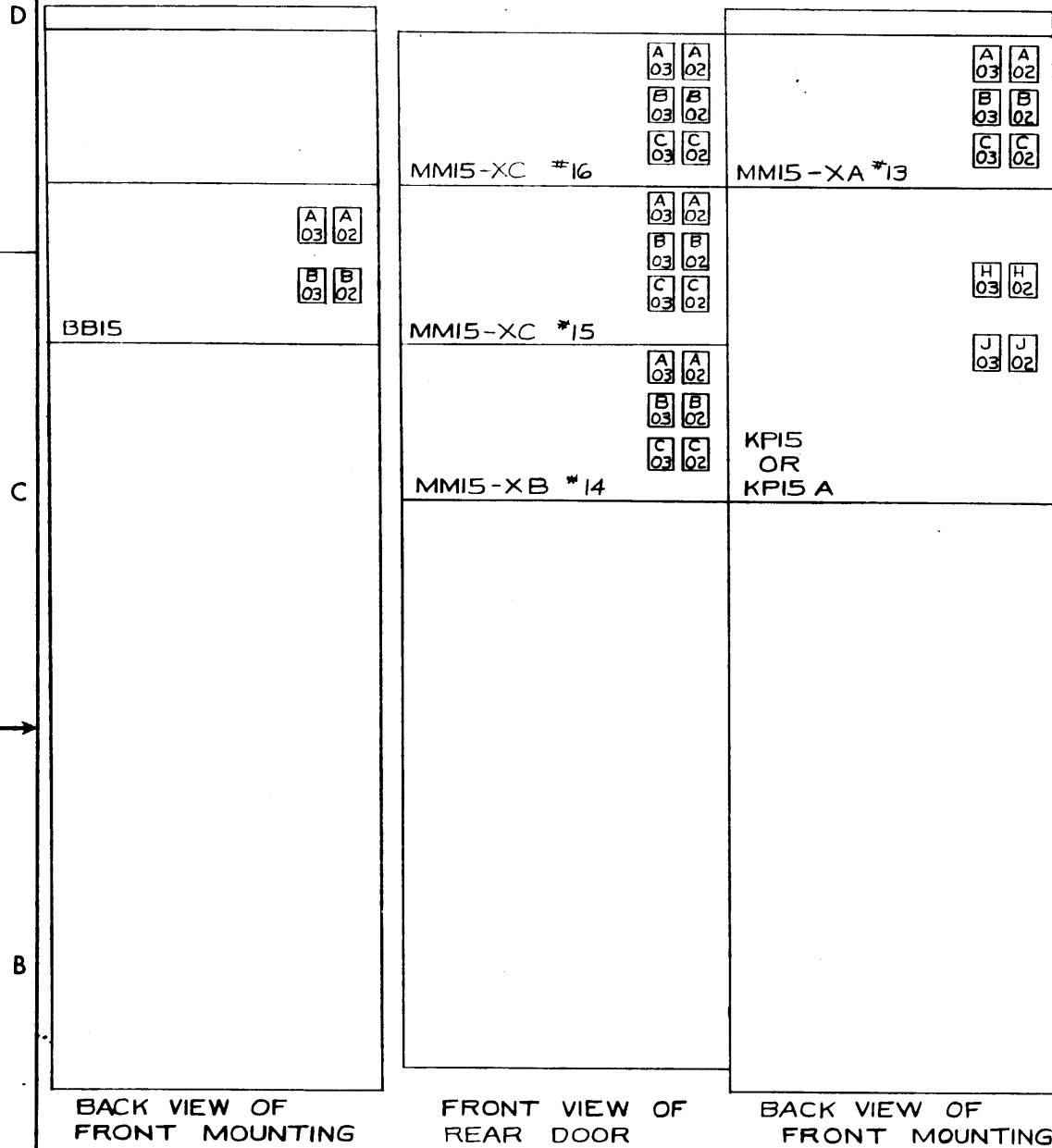
A24-A25

B24-B25

PORT 3 (LOWEST PRIORITY)

A22-A23

B22-B23



PDP-15
BAY 1 RIGHT
(SHOWN FOR
REFERENCE ONLY)

PDP-15
CONSOLE
(SHOWN FOR
REFERENCE ONLY)

MX15
BACK VIEW OF
FRONT MOUNTING

FIRST USED ON OPTION/MODEL
MX15

DO NOT SCALE DRAWING
UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS FRACTIONS ANGLES
± .005 ± 1/64 ± 0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP
CORNERS

DRN. *W. McCarthy* DATE *3/3/70*
CHK'D. *W. McCarthy* DATE *3/3/70*
ENG. *W. McCarthy* DATE *3/3/70*
PROJ. ENG. *W. McCarthy* DATE *3/3/70*
PROP. *W. McCarthy* DATE *3/3/70*

PARTS LIST
digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS
TITLE
MX15
MAXIMUM
CONFIGURATION

SIZE CODE NUMBER REV.
DAD 0006863-0-0 A
SHEET 2 OF 4
DIST.

CABLE NUMBERS

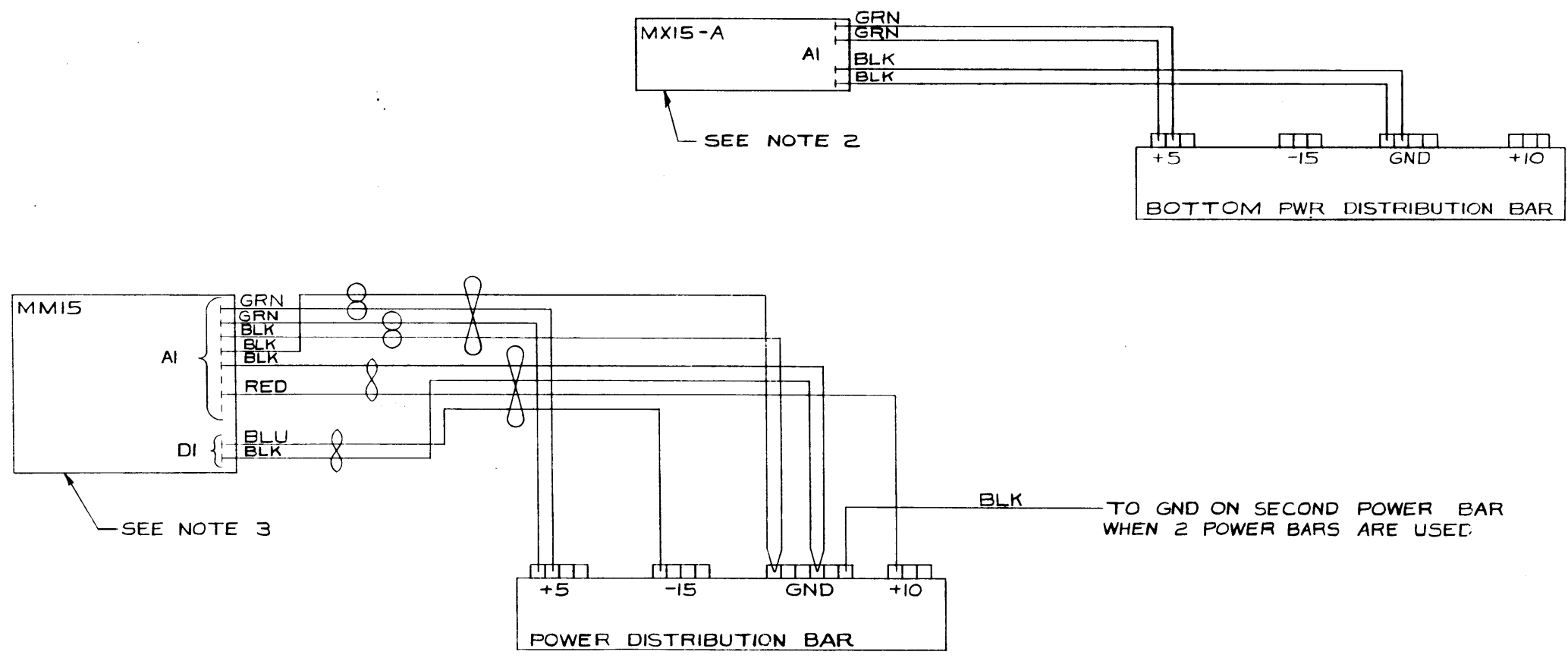
ITEM NO	CABLE	DEC PART NO
7	A	7006094-1
8	B	BC08B-1
9	C	BC08B-2
10	D	BC08B-3
11	E	BC08B-7
12	F	7006414-1
13	H	7006414-2
14	J	7006437-2
15	K	7006437-6
16	L	7006437-10
-	M	BC08B-6
-	N	7005890

[illegible]

QTY.		DESCRIPTION		PART NO.		ITEM NO.	
		PARTS LIST					
FIRST USED ON OPTION/MODEL MX15		DO NOT SCALE DRAWING UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES TOLERANCES DECIMALS FRACTIONS ANGLES ± .005 ± 1/64 ± 0°30' FINAL SURFACE QUALITY 1 REMOVE BURRS AND BREAK SHARP CORNERS		DRN <i>W.E. McCarthy</i> DATE <i>4/6/72</i> CHK'D <i>W.E. McCarthy</i> DATE <i>5/14/72</i> ENG <i>W.E. McCarthy</i> DATE <i>5/15/72</i> PROJ. ENG. <i>W.E. McCarthy</i> DATE <i>5/15/72</i> PROD. <i>W.E. McCarthy</i> DATE <i>5/15/72</i>		digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS	
		MATERIAL <i>+</i> <i>+</i> <i>+</i>		NEXT HIGHER ASSY		TITLE MX15 MAXIMUM CONFIGURATION	
FINISH <i>+</i> <i>+</i> <i>+</i>		SCALE <i>+</i> <i>+</i> <i>+</i>		SIZE CODE DAD		NUMBER 7006863-0-0	
		SHEET <i>3</i> OF <i>4</i>		DIST. <i>G</i>		REV. A	

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- NOTES FOR PWR WIRING:
1. ALL WIRING IS #14 GAUGE EXCEPT WHERE SPECIFIED.
 2. THIS WIRING IS FOR THE FIRST BAY, THE SECOND MX15.
 3. EACH BAY CAN HAVE UP TO 4 MM15'S AND 2 POWER DISTRIBUTION BARS. THE FIRST MM15 SHOULD BE WIRED TO THE BOTTOM POWER DISTRIBUTION BAR. WHEN INSTALLING A SECOND MM15, THE ADDITION OF A SECOND POWER DISTRIBUTION BAR IS REQUIRED. THE SECOND, THIRD, AND FOURTH MM15'S WILL BE WIRED TO THE TOP (SECOND) POWER DISTRIBUTION BAR. THE WIRING FROM EACH MM15 TO ITS APPROPRIATE POWER DISTRIBUTION BAR IS IDENTICAL.



DC WIRING

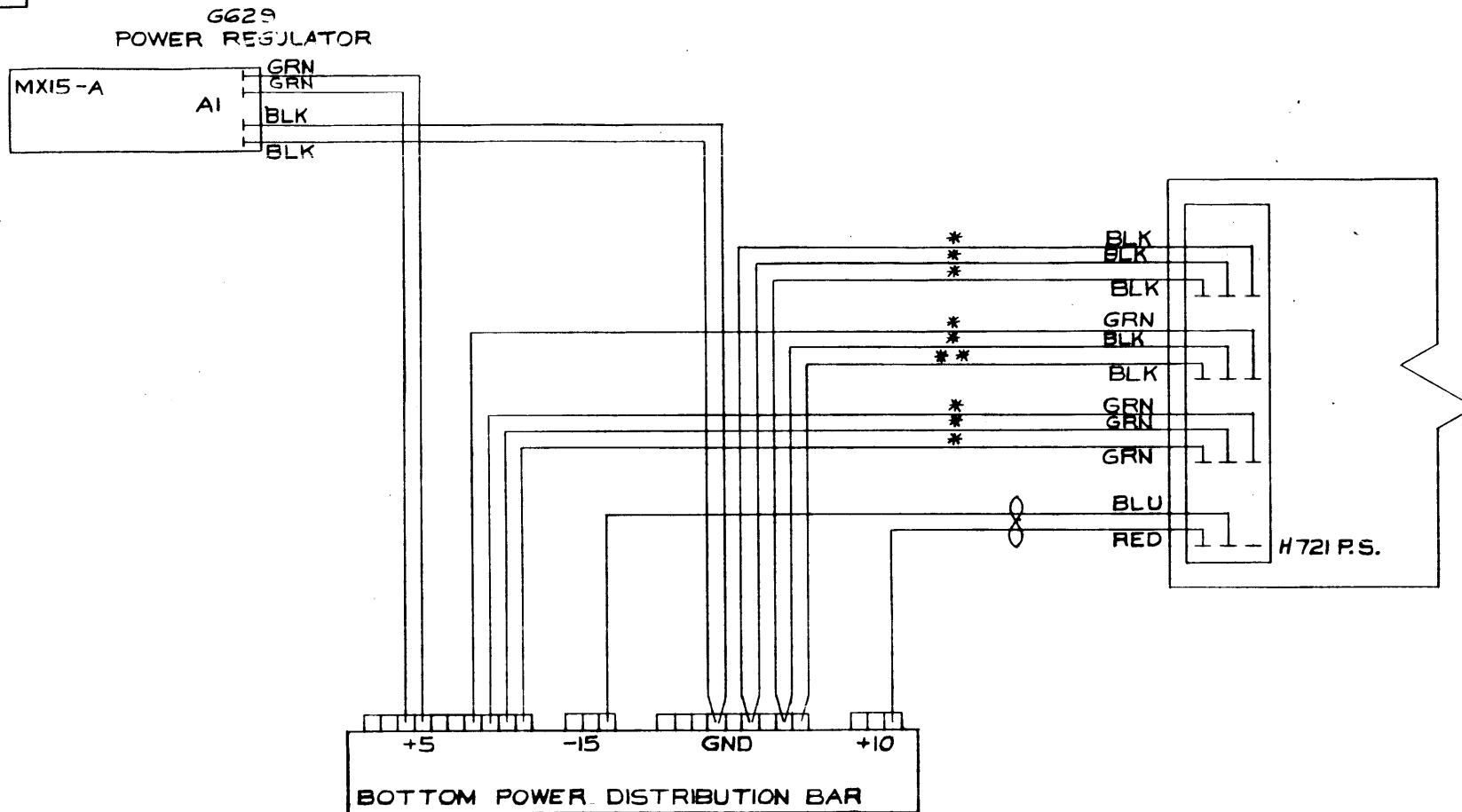
FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
MX15				
PARTS LIST				
UNLESS OTHERWISE SPECIFIED				
UNLESS OTHERWISE SPECIFIED				
DIMENSION IN INCHES				
TOLERANCES				
DECIMALS FRACTIONS ANGLES				
+ .005 ± .005 ± .010				
FINAL SURFACE QUALITY				
REMOVE BLURS AND BREAK SHARP CORNERS				
MATERIAL				
FINISH				
SCALE				
SHEET OF				
DATE				
BY				
CHECKED				
APPROVED				
DIGITAL EQUIPMENT CORPORATION				
TITLE				
MX15				
MAXIMUM				
CONFIGURATION				
SIZE/CODE/NUMBER				
D				
DIST.				



1. ALL WIRING IS *14 GAUGE EXCEPT WHERE SPECIFIED.
2. IF TOPHT21 POWER SUPPLY IS NOT USED, JUMP S1 TOGETHER WITH MALE FASTON CONNECTOR (ITEM *10).
3. * TWIST GRN/BLK TWP WITH GRN/BLK TWP.
** TWIST WITH RED/BLU TWP.
4. ALL POWER SUPPLY WIRING (AC-DC) WILL BE WIRED TO MAXIMUM CONFIGURATION.
5. FOR LOCATION OF UNITS SHOWN IN PHANTOM LINES REFER TO D-AD-7006863-O-O.
6. ADD ALL -30 V DC WIRING AT ONE TIME.

FIRST USED ON ITEM NO.		QTY.	DESCRIPTION	PART NO.	ITEM NO.
MX15			PARTS LIST		
UNLESS OTHERWISE SPECIFIED		DRN. <i>McCarthy</i>	DATE <i>3/21/70</i>	 DIGITAL EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS	
UNLESS OTHERWISE SPECIFIED		CHUD.	DATE		
DIMENSION IN INCHES		ENG. <i>McCarthy</i>	DATE		
TOLERANCES		PROJ. ENG.	DATE		
DECIMALS FRACTIONS ANGLES		PROD.	DATE	MX15 ASSEMBLY	
± .005 ± .164 ± °30					
FINAL SURFACE QUALITY					
REMOVE BURRS AND BREAK SHARP CORNERS					
MATERIAL		TOLERANCES		SIZE CODE NUMBER REV.	
FINISH		SCALE		DUJAMX15 C C 13	
		SHEET OF 1		DIST.	

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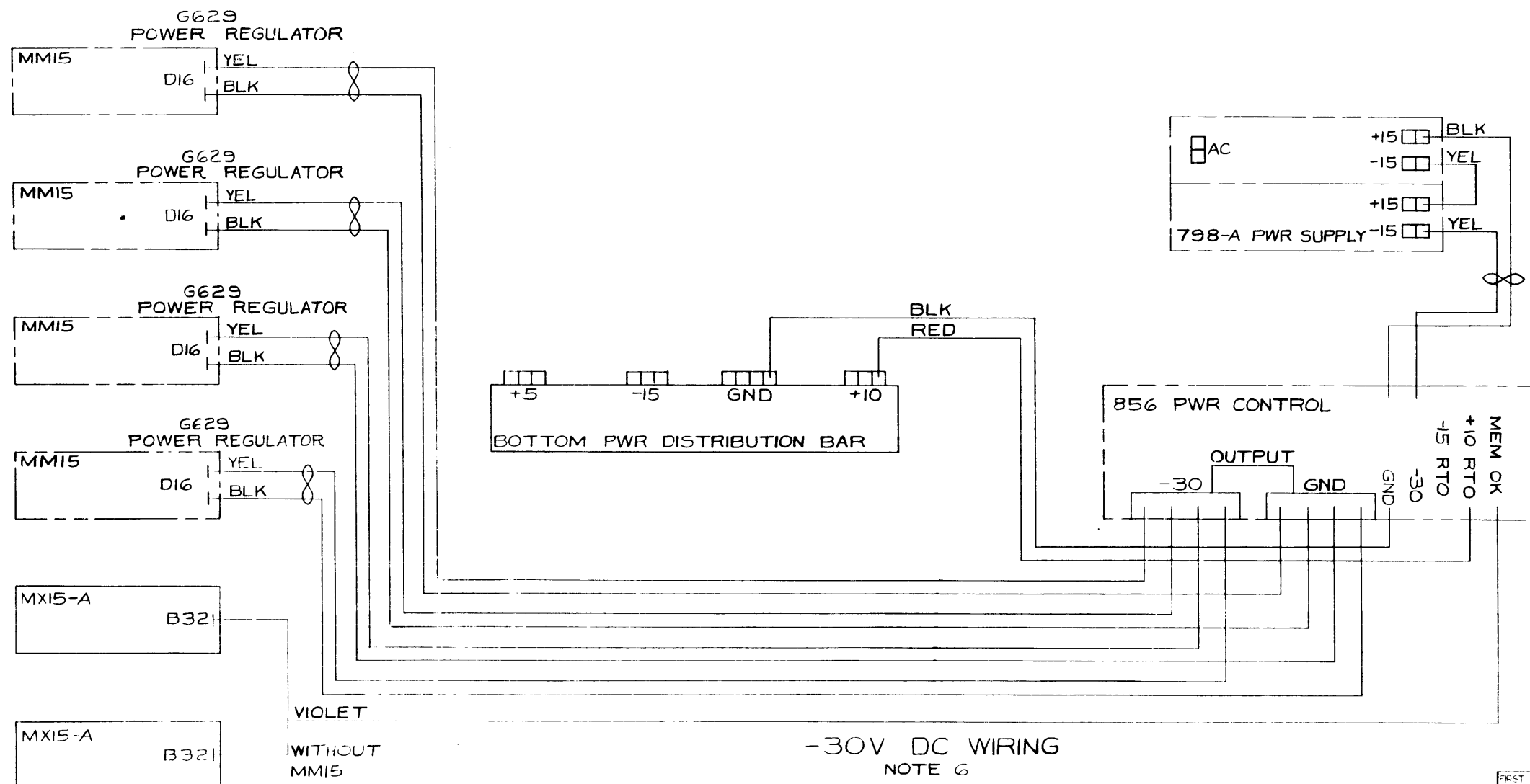
DC WIRING

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO	ITEM NO.
MX15				
UNLESS OTHERWISE SPECIFIED				
UNLESS OTHERWISE SPECIFIED				
DIMENSION IN INCHES				
TOLERANCES				
DECIMALS FRACTIONS ANGLES				
± .005 ± 1/64 ± 0°30'				
FINAL SURFACE QUALITY				
REMOVE BURRS AND BREAK SHARP CORNERS				
MATERIAL				
NEXT HIGHER ASSY				
D-AD-7006863-0-0				
FINISH				
SCALE 1 1				
SHEET 3 OF 4				
SIZE CODE				
NUMBER				
DUA MX15-0-0				
REV				
B				

digital EQUIPMENT CORPORATION
WAYNARD MASSACHUSETTS

MX15
ASSEMBLY

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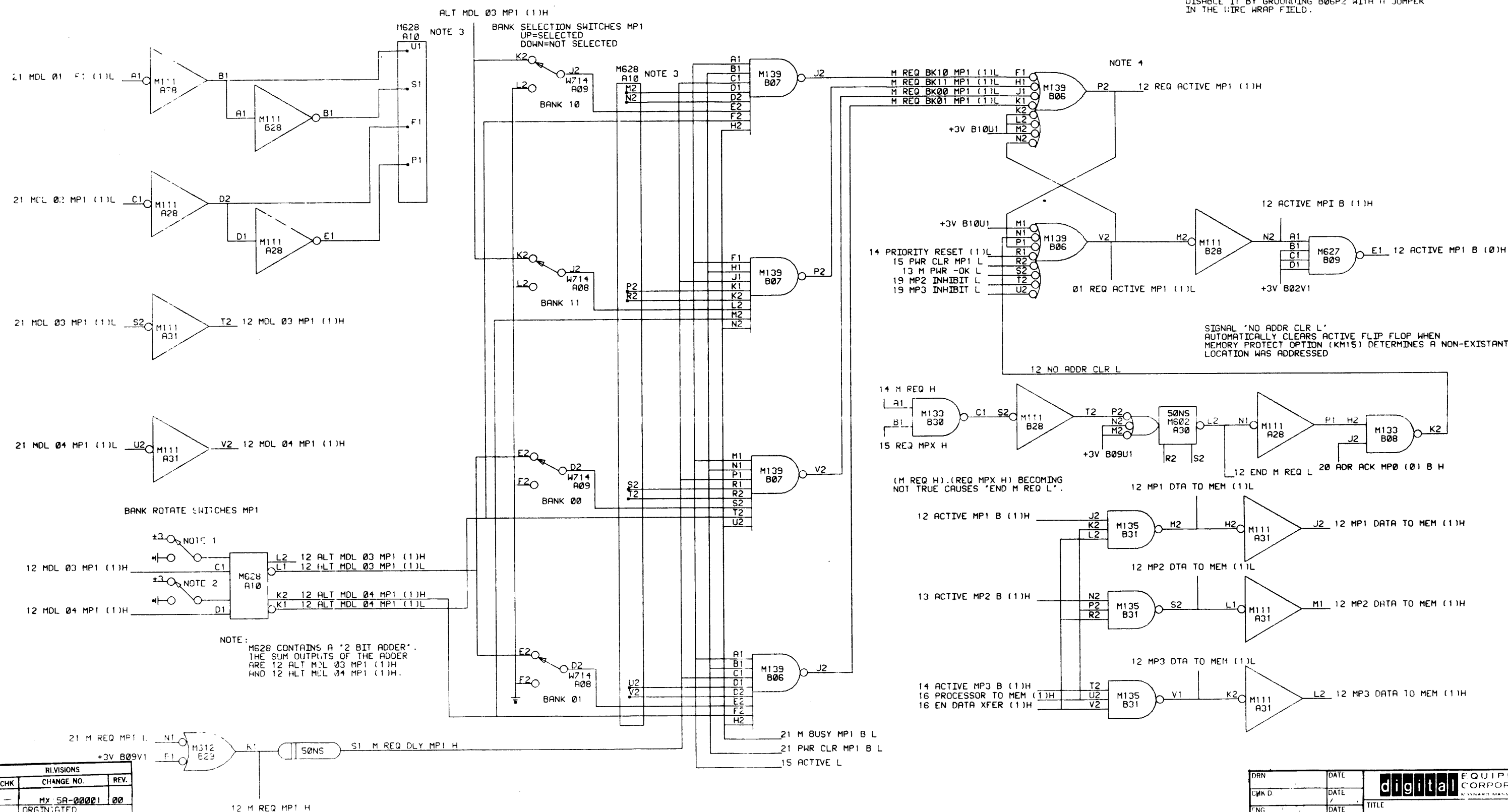


FIRST USED ON: MODEL		QTY.	DESCRIPTION	PART NO.	ITEM NO.
MX15					
UNLESS OTHERWISE SPECIFIED		DRN	DATE	PARTS LIST	
UNLESS OTHERWISE SPECIFIED		CHK'D	DATE	digital EQUIPMENT CORPORATION	
DIMENSION IN INCHES		ENG	DATE	TITLE	
TOLERANCES		PROJ. ENG	DATE	MX15	
DECIMALS FRACTIONS ANGLES		PROD.	DATE	ASSEMBLY	
= .005 = 1/64 = 0°30'				SIZE CODE	
FINAL SURFACE QUALITY				NUMBER	
REMOVE BURRS AND BREAK SHARP CORNERS				REV	
MATERIAL				SCALE	
FINISH				SHEET	

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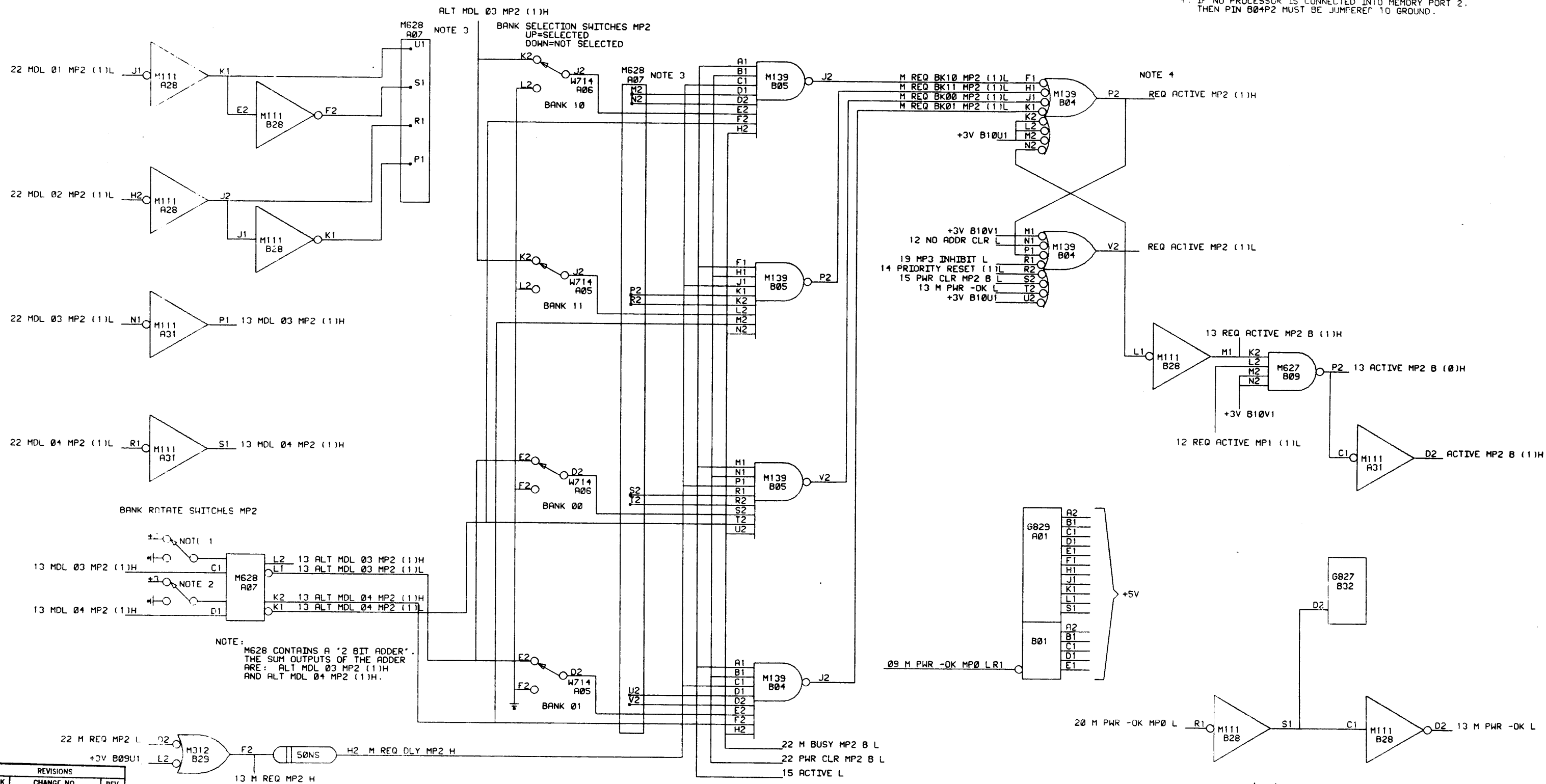
NOTES :

1. IN UP POSITION THIS ADDS (1) TO ADDRESS BIT 03 [16K].
2. IN UP POSITION THIS ADDS (1) TO ADDRESS BIT 04 [8K].
3. JUMPER: THE M528 MODULE CONNECTS THE PROPER POLARITY OF BLOCK ADDRESS BITS [MOL0] AND [MOL2] TO THE M139 ADDRESS DECODE GATES.
4. IF NO DEVICE IS CONNECTED INTO MEMORY PORT 1, DISABLE IT BY GROUNDING 806P2 WITH A JUMPER IN THE WIRE WRAP FIELD.

[illegible]

DRN	DATE	digital EQUIPMENT CORPORATION 34 VINLAND MASSACHUSETTS			
CWK D.	DATE	TITLE PRIORITY LOGIC INPUT PORT 1			
ENG	DATE				
PROJ. ENG.	DATE				
PROQ	DATE				
FIRST USED ON MX15					
SCALE		SIZE	CODE	NUMBER	REV.
SHEET	OF	1	BS	MX15-A-12	00
		DIST			

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[illegible]

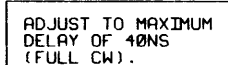
DRAWN	DATE	 DIGITAL EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS			
CHK'D	DATE	TITLE			
ENG	DATE	PRIORITY LOGIC INPUT			
PROJ. ENG.	DATE	PORT 2			
PROD.	DATE				
FIRST USED ON					
MX15					
SCALE		SIZE	CODE	NUMBER	REV.
		D	BS	MX15-A-13	00
SHEET	1	OF	1	DIST	

1. FOR EQUAL PRIORITY JUMPER A28V2 TO A30H2
2. IF NO PROCESSOR IS CONNECTED TO MEMORY PORT 3
PIN B02P2 MUST BE GROUND WITH A JUMPER
3. IN UP POSITION THIS ADDS (1) TO ADDRESS BIT 03 [16K].
4. IN UP POSITION THIS ADDS (1) TO ADDRESS BIT 04 [128K].
5. JUMPERS IN THE M628 MODULE CONNECTS THE POWER POLARITY
OF BLOCK ADDRESS BITS [MDL01 AND MDL02] TO THE M139
ADDRESS DECODE GATES.



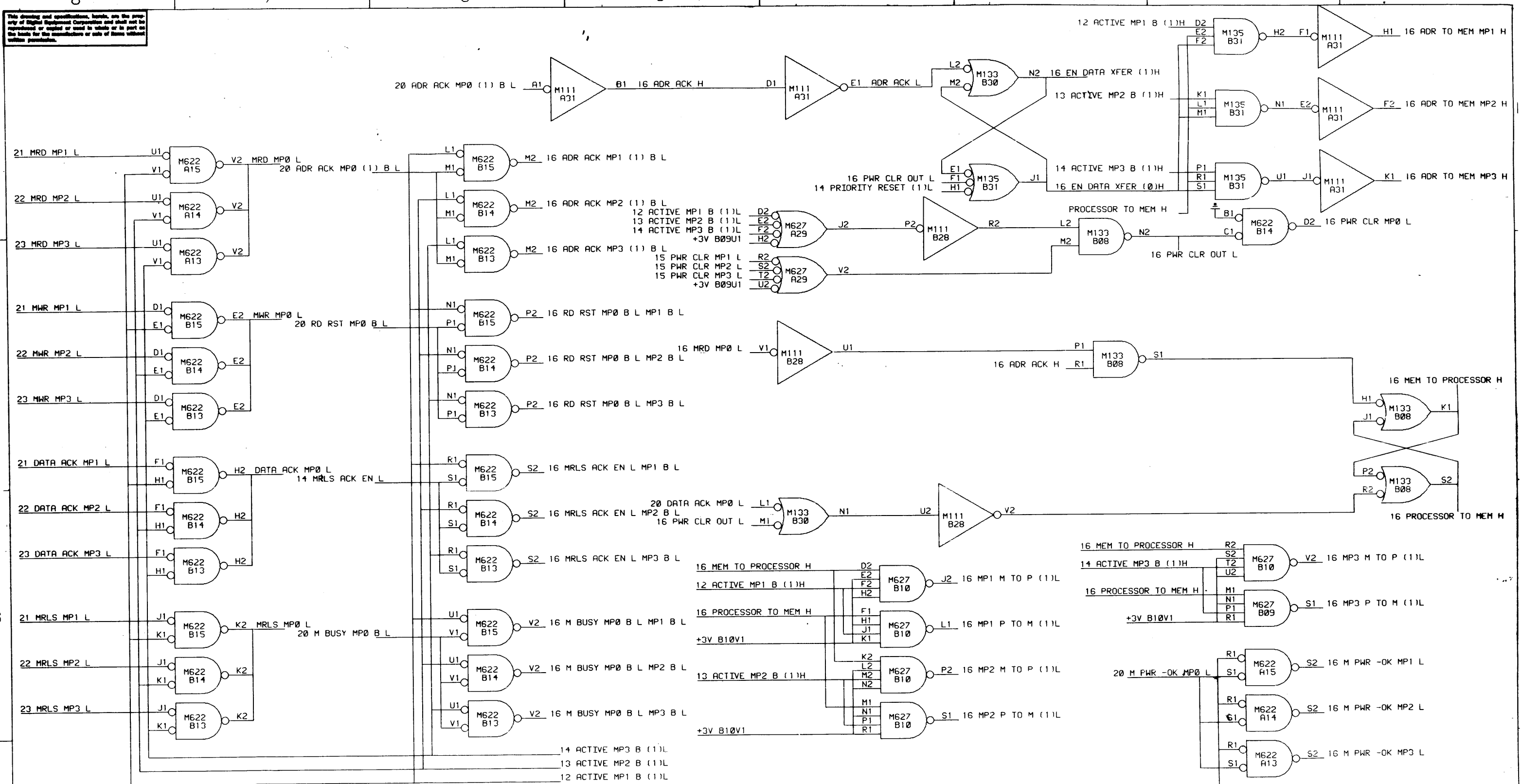
DNR.		DATE	10-29-78	digital	EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
K WALSH		DATE	10-30-78	TITLE	PRIORITY LOGIC INPUT PORT 3
CHK'D.		DATE	10-30-78		
G HAVILAND		DATE	10-30-78		
ENG.		DATE	10-30-78		
B C GRAY		DATE	10-30-78		
PROJ. ENG.		DATE	10-30-78		
R D BIRD		DATE	10-30-78		
PROD.		DATE	10-30-78		
J R BUNLY		DATE	10-30-78		
FIRST USED ON					
NEXT		SHEET	OF	CODE	NUMBER
SCALE				D BS	MX15-A-14
SHEET	1	OF	1	DISP.	

1



DRN.	DATE	 DIGITAL EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS									
CHP.D.	DATE										
ENG.	DATE	TITLE MDL 03.04 DRIVERS. MREQ LOGIC									
PROJ. ENG.	DATE										
PROJ.	DATE	<table><tr><th>SIZE</th><th>CODE</th><th>NUMBER</th><th>REV.</th></tr><tr><td>D</td><td>BS</td><td>MX15-A-15</td><td>00</td></tr></table>		SIZE	CODE	NUMBER	REV.	D	BS	MX15-A-15	00
SIZE	CODE			NUMBER	REV.						
D	BS	MX15-A-15	00								
FIRST USED ON	DATE	DIST.									
MX15											
SCALE											
SHEET 1	OF 1										

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[illegible]

DRN.	DATE	 digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS											
CHK'D.	DATE												
ENG.	DATE	TITLE CONTROL LINES											
PROJ. ENG.	DATE												
PROD.	DATE												
FIRST USED ON	DATE												
MX15				SIZE CODE		NUMBER		REV.					
				D BS		MX15-A-16		00					
SCALE													
SHEET	1	OF		1									
				DIST.									

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D

C

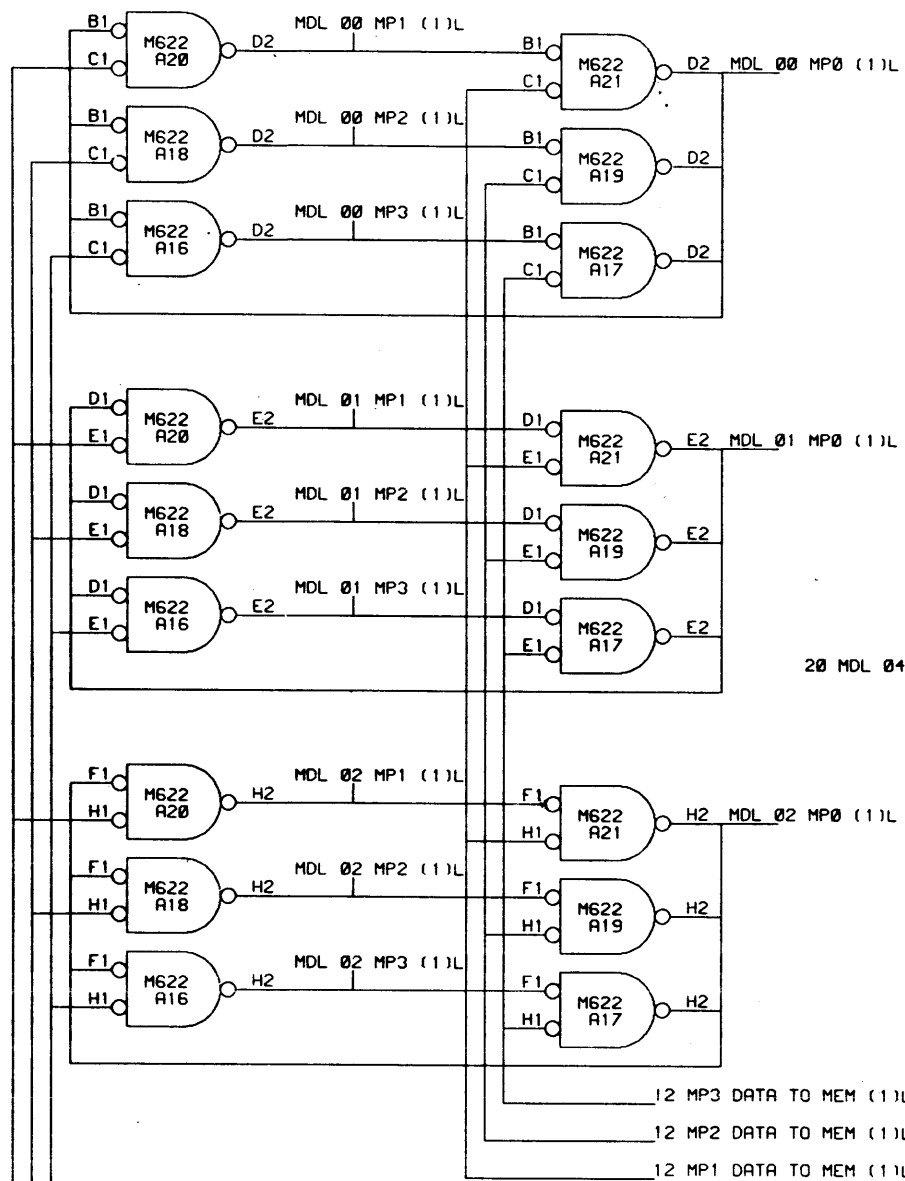
B

18

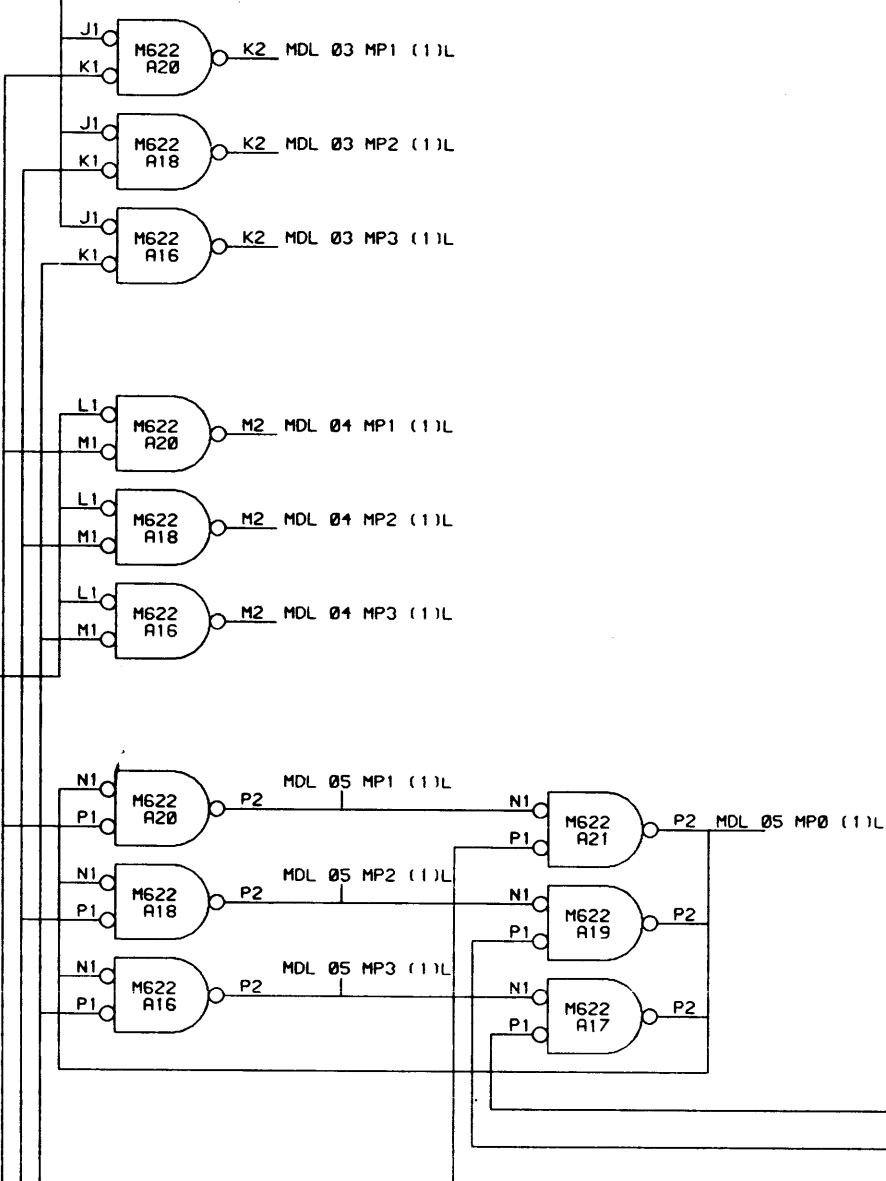
A

REVISIONS		
CHK	CHANGE NO.	REV.
—	MX15A-00001	00
ORIGINATED		

20 MDL 03 MP0 (1)L



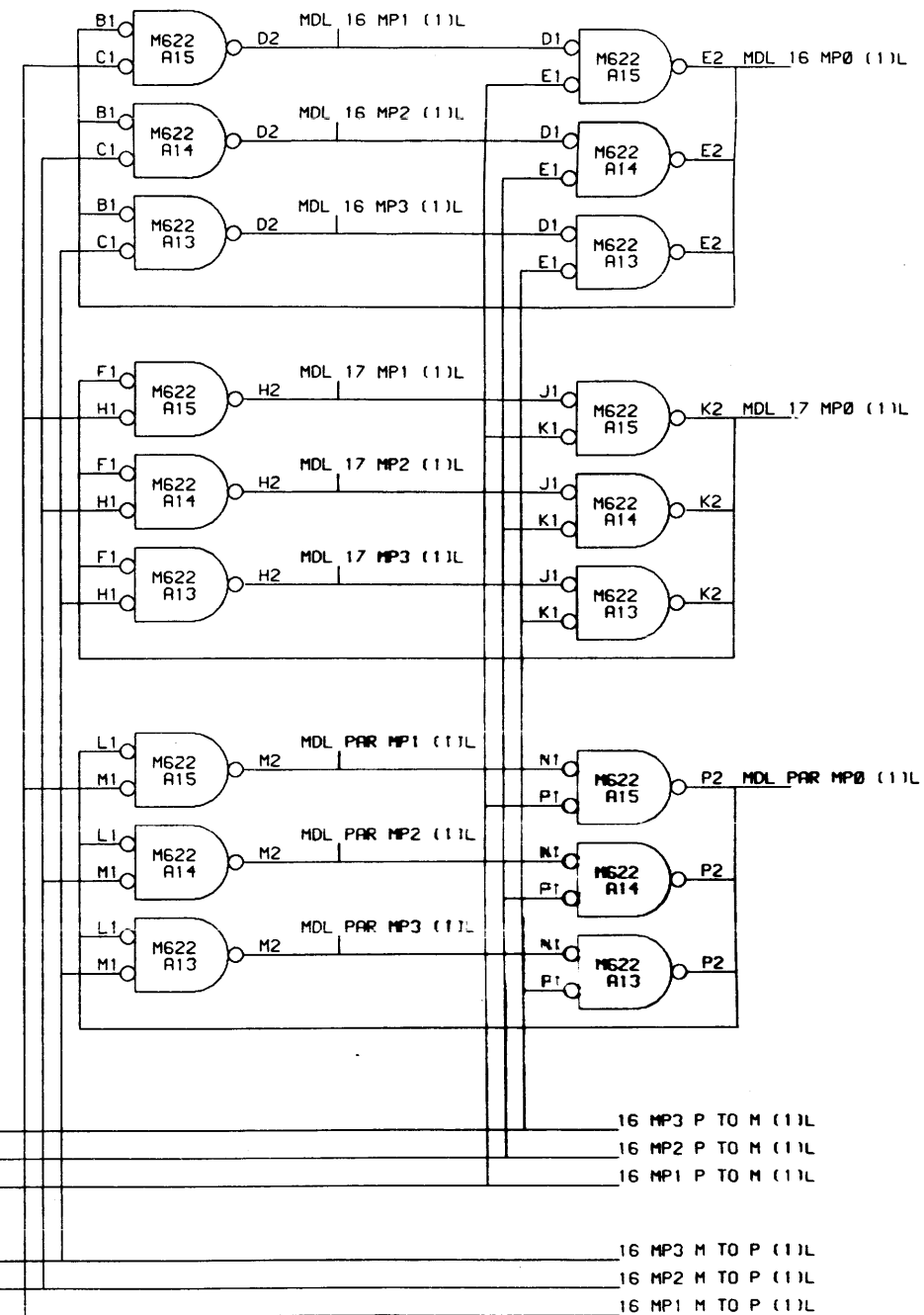
20 MDL 04 MP0 (1)L



NOTE:
1. ALL SIGNALS WITH NAMES
"MDL** MP**" ARE BI-DIRECTIONAL

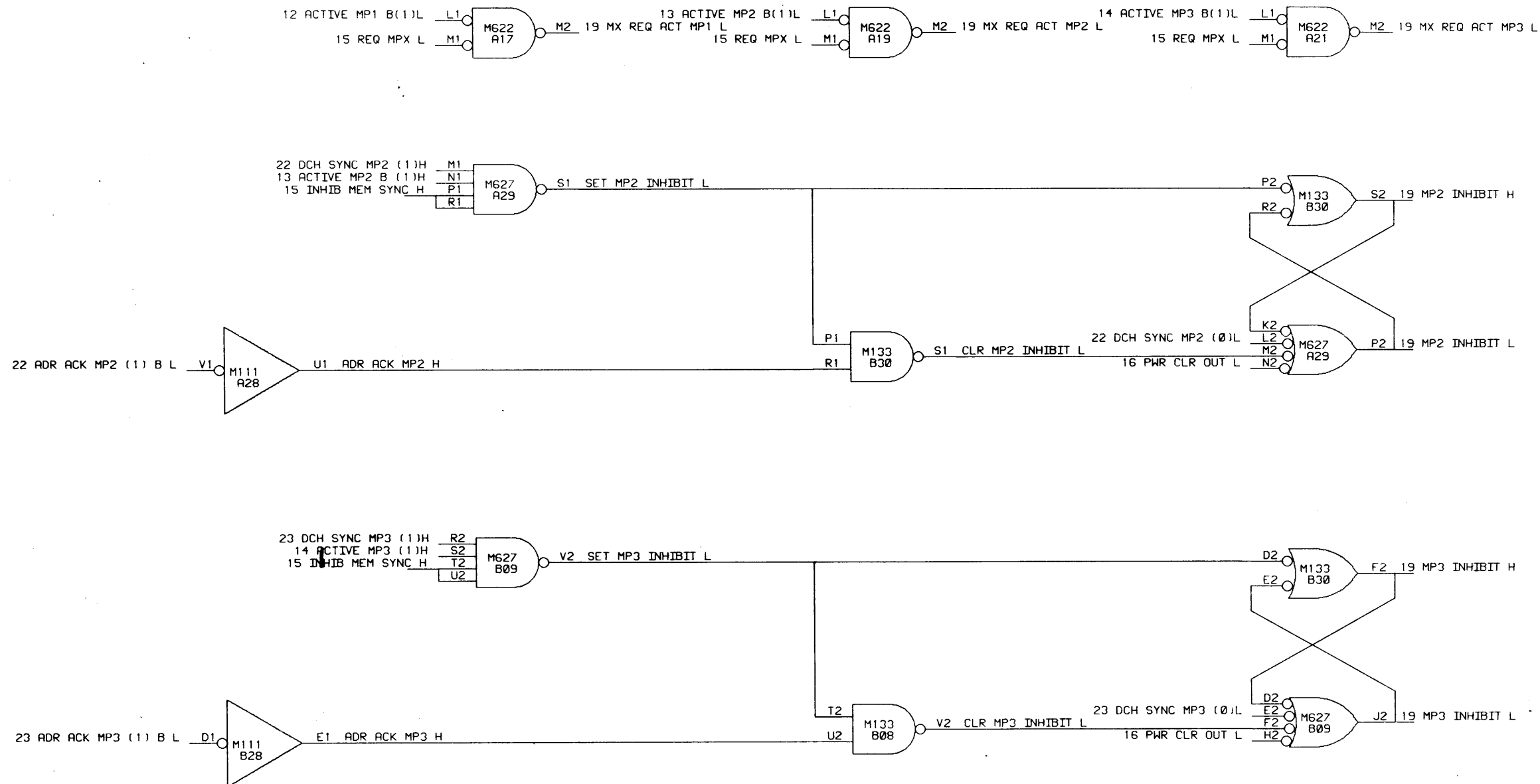
DRN.	DATE	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS		
CHN'D.	DATE			
ENG.	DATE			
PROJ. ENG.	DATE			
PROG.	DATE			
FIRST USED ON		TITLE		
MX15		MDL 0 THROUGH 8		
SCALE		SIZE/CODE	NUMBER	REV.
SHEET 1 OF 1	DIST.	D BS	MX15-A-17	00

17



DRN.	DATE	 digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS	TITLE									
CHMD.	DATE											
ENG.	DATE											
PROJ. ENG.	DATE											
PROM.	DATE											
FIRST USED ON			MDL 9-17 PARITY									
MX15		SIZE	CODE	NUMBER						REV.		
SCALE		D	BS	MX15-A-18						00		
SHEET 1 OF 1		DIST.										

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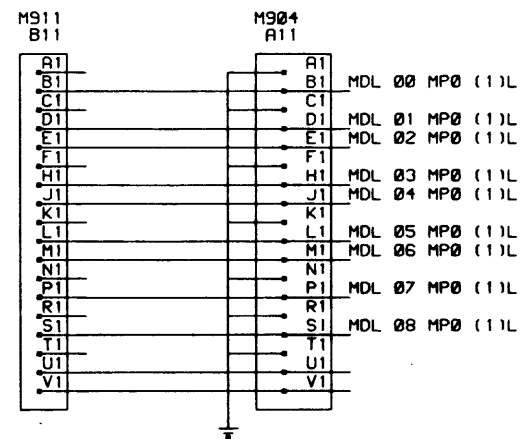
REVISIONS		
CHK	CHANGE NO.	REV.
	MX15A-00001	00
	ORIGINATED	
TC	MX15A-00003	A

DRN.	DATE	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS	
CHK'D.	DATE		
ENG.	DATE	TITLE INHIBIT LOGIC	
PROJ. ENG.	DATE		
PROD.	DATE	FIRST USED ON MX15	
SCALE		SIZE CODE D BS	NUMBER MX15-A-19
SHEET	OF	DIST.	REV. A

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- NOTE:
1. UP TO FOUR MM15'S MAY BE DAISY-CHAINED TO THE "MEMORY PORT OUT".
 2. ALL "MDL" SIGNALS ARE BI-DIRECTIONAL.
 3. SIGNALS WITH AN "*" FOLLOWING THE NAME ORIGINATE IN THE MM15 MEMORY SYSTEM.
 4. ACTUAL CABLE GROUND WIRES ARE CONFIGURED FOR MINIMUM NOISE PICKUP AND HENCE DEVIATE FROM THIS DIAGRAM. FOR ACTUAL GROUND RUNS, SEE "MX15 WIRE LIST".

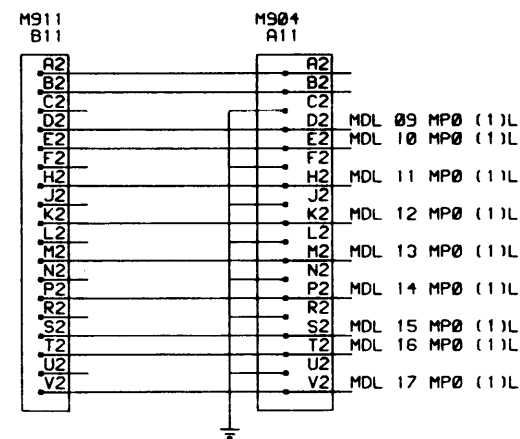
TO MM15
MODULE SLOT
A02 OR B02



CORRESPONDING MM15 SIGNAL NAMES

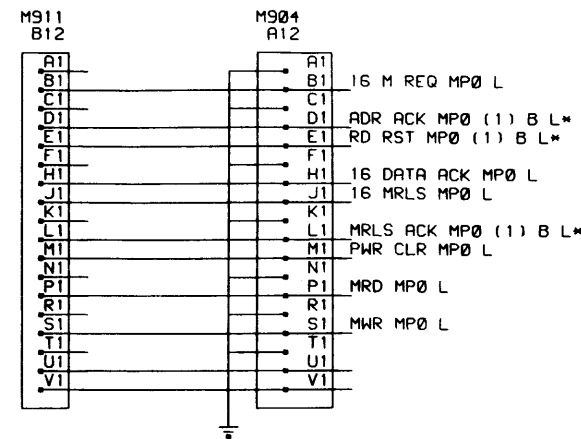
(MM16+19 MDL 00 (1)L)
(MM16+19 MDL 01 (1)L)
(MM16+19 MDL 02 (1)L)
(MM16+19 MDL 03 (1)L)
(MM16+19 MDL 04 (1)L)
(MM16+19 MDL 05 (1)L)
(MM16+19 MDL 06 (1)L)
(MM16+19 MDL 07 (1)L)
(MM16+19 MDL 08 (1)L)

TO MM15
MODULE SLOT
A02 OR B02



(MM16+19 MDL 09 (1)L)
(MM16+19 MDL 10 (1)L)
(MM16+19 MDL 11 (1)L)
(MM16+19 MDL 12 (1)L)
(MM16+19 MDL 13 (1)L)
(MM16+19 MDL 14 (1)L)
(MM16+19 MDL 15 (1)L)
(MM16+19 MDL 16 (1)L)
(MM16+19 MDL 17 (1)L)

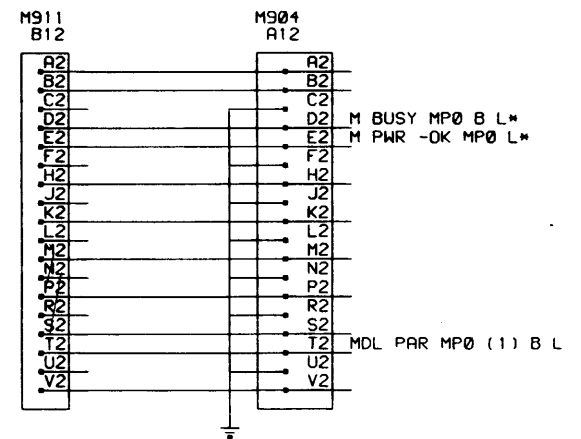
TO MM15
MODULE SLOT
A03 OR B03



CORRESPONDING MM15 SIGNAL NAMES

(MM19 MREQ L)
(MM16 ADR ACK (1) B L)
(MM16 RD RST (1) B L)
(MM19 DATA ACK L)
(MM19 MRLS L)
(MM16 MRLS ACK (1) B L)
(MM19 PWR CLR L)
(MM19 MRD L)
(MM19 MWR L)

TO MM15
MODULE SLOT
A03 OR B03



(MM16 M BUSY (B) L)
(MM20 M PWR -OK L)
(MM19+24 MDL PAR (1) B L)

REVISIONS		
CHK	CHANGE NO.	REV.
	MX15A-00001	00
ORIGINATED		

DRN.	DATE	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
CHK'D.	DATE	
ENG.	DATE	
PROJ. ENG.	DATE	
PROD.	DATE	
FIRST USED ON		TITLE
MX15		MEMORY PORT OUT
SCALE	SIZE CODE	NUMBER
SHEET 1 OF 1	D IC	MX15-R-20
	DIST.	REV. 00

D

C

B

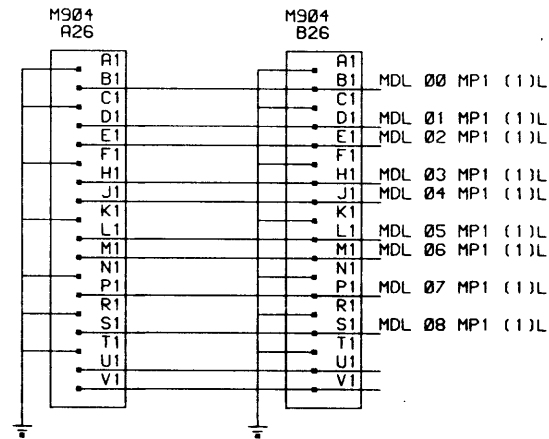
22

A

- NOTE:
1. 'MEMORY PORT 1' IS THE HIGHEST PRIORITY PORT INPUT. IT WILL NORMALLY BE CONNECTED TO THE KP15-A I/O PROCESSOR MEMORY BUS IF A KP15-A IS USED. IF A DMA CHANNEL (DIRECT MEMORY ACCESS) IS PROVIDED, IT WOULD BE CONNECTED TO MEMORY PORT 1.
 2. ALL 'MDL' SIGNALS ARE BI-DIRECTIONAL.
 3. SIGNALS WITH AN '*' FOLLOWING THE NAME ORIGINATE IN THE MM15 MEMORY SYSTEM.
 4. ACTUAL CABLE GROUND WIRES ARE CONFIGURED FOR MINIMUM NOISE PICKUP AND HENCE DEVIATE FROM THIS DIAGRAM. FOR ACTUAL GROUND RUNS, SEE 'MX15 WIRE LIST'.

TO KP15
MODULE SLOT
J02 OR TO
PREVIOUS MX15

TO NEXT MX15
OR TERMINATE
WITH M902

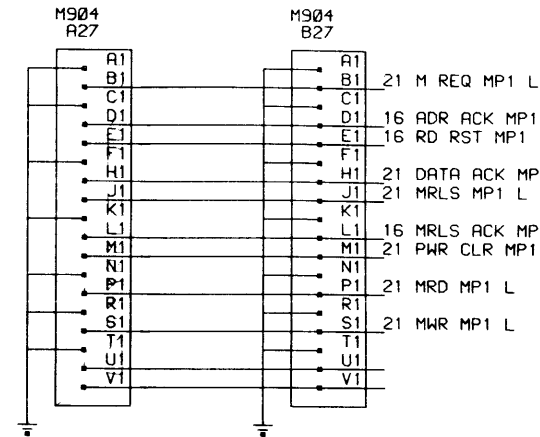


CORRESPONDING KP15 SIGNALS

(KP27 MDL 00 L)
(KP27 MDL 01 L)
(KP27 MDL 02 L)
(KP27 MDL 03 L)
(KP27 MDL 04 L)
(KP27 MDL 05 L)
(KP27 MDL 06 L)
(KP27 MDL 07 L)
(KP27 MDL 08 L)

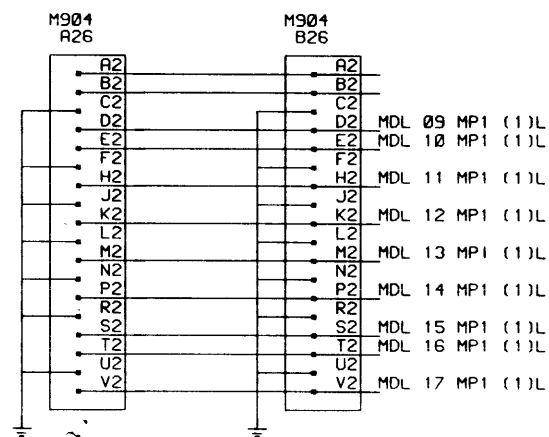
TO KP15
MODULE SLOT
J03 OR TO
PREVIOUS MX15

TO NEXT MX15
OR TERMINATE
WITH M902

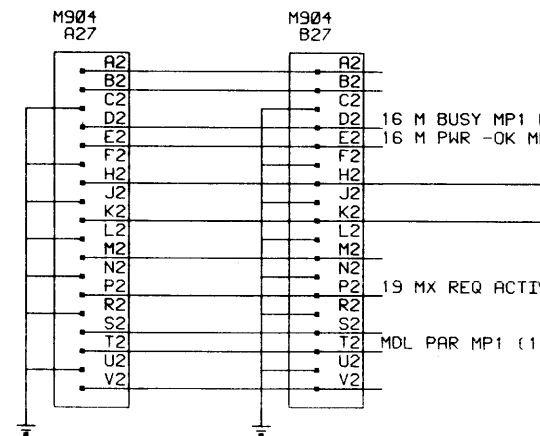


CORRESPONDING KP15 SIGNALS

(KP32 MREQ L)
(KP27 ADR ACK B (1)L)
(KP27 RD RST B (1)L)
(KP32 DATA ACK L)
(KP32 MRLS L)
(KP27 MRLS ACK (B) L)
(KP20 PWR CLR L)
(KP32 MRD L)
(KP32 MWR L)



(KP27 MDL 09 L)
(KP27 MDL 10 L)
(KP27 MDL 11 L)
(KP27 MDL 12 L)
(KP27 MDL 13 L)
(KP27 MDL 14 L)
(KP27 MDL 15 L)
(KP27 MDL 16 L)
(KP27 MDL 17 L)



(KP27 SEQ (1)L)
(KP57 POWER OK H)
(KP27 TRAP L)
(KP31 DEFER H)

REVISIONS		
CHK	CHANGE NO.	REV.
	MX15A-00001	00
ORIGINATED		
TC	MX15A-00003	A
RC Day 2/7/70		

DRN.	DATE	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
CHK'D.	DATE	
ENG.	DATE	
PROJ. ENG.	DATE	
PROD.	DATE	
FIRST USED ON		TITLE
MX15		MEMORY PORT 1
SCALE	SIZE/CODE	NUMBER
SHEET 1 OF 1	D IC	MX15-A-21
	DIST.	REV. A

8

7

6

5

4

3

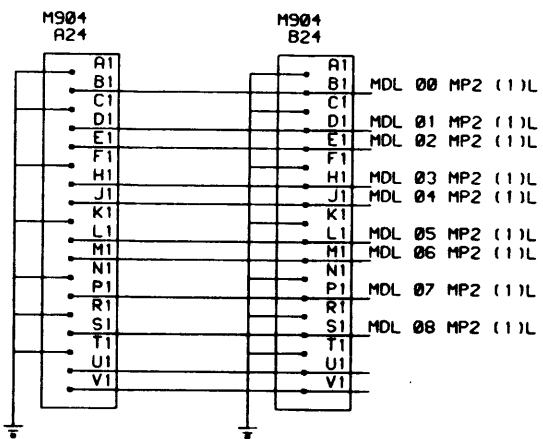
2

1

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TO KP15
MODULE SLOT
J02 OR TO
PREVIOUS MX15

TO NEXT MX15
OR TERMINATE
WITH M902

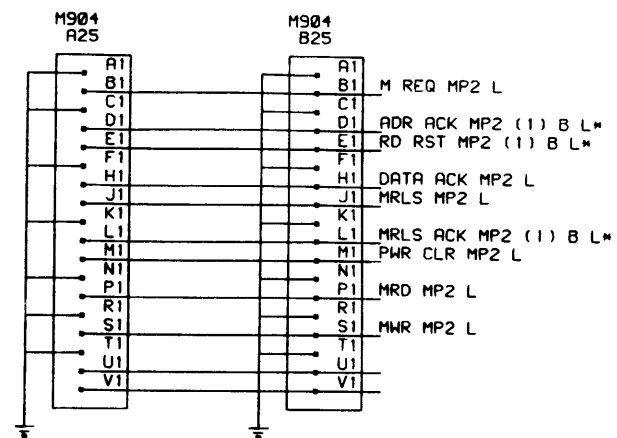


CORRESPONDING KP15 SIGNALS

(KP27 MDL 00 L)
(KP27 MDL 01 L)
(KP27 MDL 02 L)
(KP27 MDL 03 L)
(KP27 MDL 04 L)
(KP27 MDL 05 L)
(KP27 MDL 06 L)
(KP27 MDL 07 L)
(KP27 MDL 08 L)

TO KP15
MODULE SLOT
J03 OR TO
PREVIOUS MX15

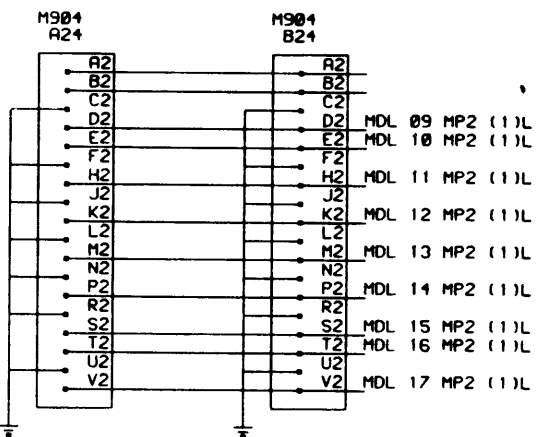
TO NEXT MX15
OR TERMINATE
WITH M902



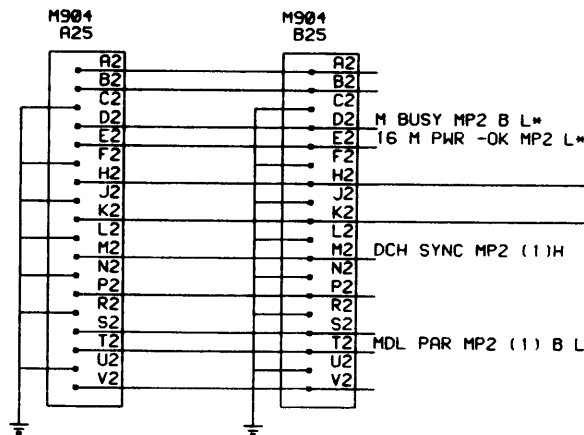
CORRESPONDING KP15 SIGNALS

(KP32 MREQ L)
(KP27 ADR ACK B (1)L)
(KP27 RD RST B (1)L)
(KP32 DATA ACK L)
(KP32 MRLS L)
(KP27 MRLS ACK (B) L)
(KP20 PWR CLR L)
(KP32 MRD L)
(KP32 MWR L)

- NOTE:
1. "MEMORY PORT 2" IS THE SECOND HIGHEST PRIORITY INPUT PORT.
 2. ALL "MDL" SIGNALS ARE BI-DIRECTIONAL.
 3. SIGNALS WITH AN "M" FOLLOWING THE NAME ORIGINATE IN THE MM15 MEMORY SYSTEM.
 4. ACTUAL CABLE GROUND WIRES ARE CONFIGURED FOR MINIMUM NOISE PICKUP AND HENCE DEVIATE FROM THIS DIAGRAM. FOR ACTUAL GROUND RUNS, SEE "MX15 WIRE LIST".



(KP27 MDL 09 L)
(KP27 MDL 10 L)
(KP27 MDL 11 L)
(KP27 MDL 12 L)
(KP27 MDL 13 L)
(KP27 MDL 14 L)
(KP27 MDL 15 L)
(KP27 MDL 16 L)
(KP27 MDL 17 L)



(KP27 SEQ (1)L)
(KP57 POWER OK H)
(KP27 TRAP L)
(KP31 DEFER H)
(KP51 DCH SYNC B L)

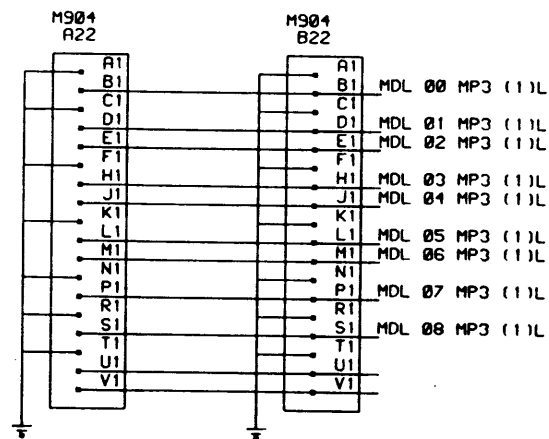
REVISIONS		
CHK	CHANGE NO.	REV.
	MX15A-00001	00
ORIGINATED		

DRAWN	DATE	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS		
CHK'D	DATE			
ENG	DATE			
PROJ. ENG	DATE			
PROJ. MGR	DATE			
FIRST USED ON		TITLE		
MX15		MEMORY PORT 2		
SCALE		SIZE CODE	NUMBER	REV.
SHEET 1 OF 1		D. IC	MX15-A-22	00

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TO KP15
MODULE SLOT
J02 OR TO
PREVIOUS MX15

TO NEXT MX15
OR TERMINATE
WITH M902

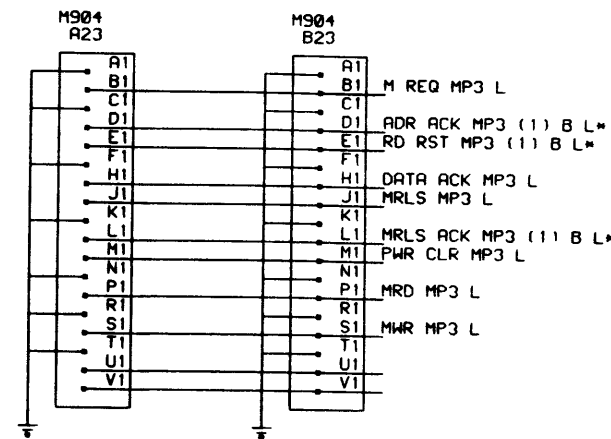


CORRESPONDING KP15 SIGNALS

(KP27 MDL 00 L)
(KP27 MDL 01 L)
(KP27 MDL 02 L)
(KP27 MDL 03 L)
(KP27 MDL 04 L)
(KP27 MDL 05 L)
(KP27 MDL 06 L)
(KP27 MDL 07 L)
(KP27 MDL 08 L)

TO KP15
MODULE SLOT
J03 OR TO
PREVIOUS MX15

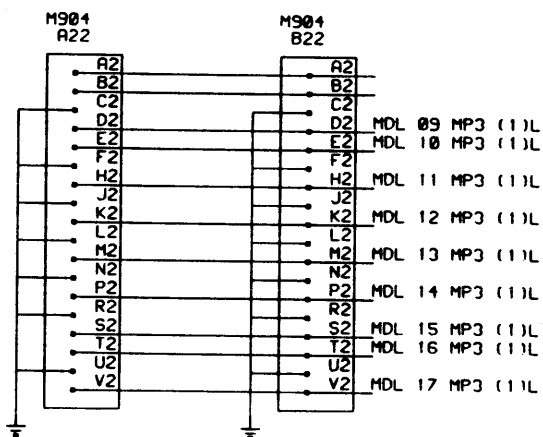
TO NEXT MX15
OR TERMINATE
WITH M902



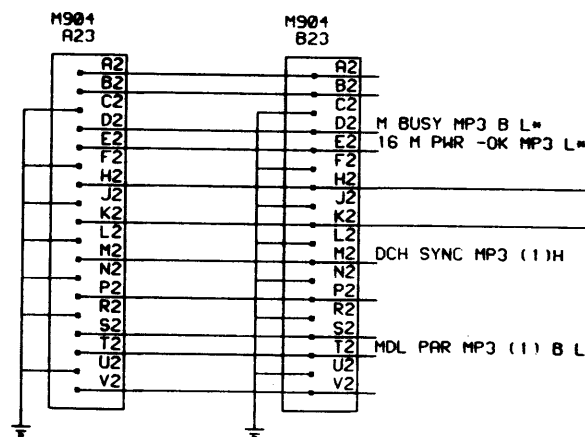
CORRESPONDING KP15 SIGNALS

(KP32 MREQ L)
(KP27 ADR ACK B (1)L)
(KP27 RD RST B (1)L)
(KP32 DATA ACK L)
(KP32 MRLS L)
(KP27 MRLS ACK (B) L)
(KP20 PWR CLR L)
(KP32 MRD L)
(KP32 MWR L)

- NOTE:
1. MEMORY PORT 3 IS THE LOWEST PRIORITY INPUT PORT.
 2. ALL "MDL" SIGNALS ARE BI-DIRECTIONAL.
 3. SIGNAL WITH AN "*" FOLLOWING THE NAME ORIGINATE IN THE MMIS MEMORY SYSTEM.
 4. ACTUAL CABLE GROUND WIRES ARE CONFIGURED FOR MINIMUM NOISE PICKUP AND HENCE DEVIATE FROM THIS DIAGRAM. FOR ACTUAL GROUND RUNS, SEE "MX15 WIRE LIST".



(KP27 MDL 09 L)
(KP27 MDL 10 L)
(KP27 MDL 11 L)
(KP27 MDL 12 L)
(KP27 MDL 13 L)
(KP27 MDL 14 L)
(KP27 MDL 15 L)
(KP27 MDL 16 L)
(KP27 MDL 17 L)



(KP27 SEQ (1)L)
(KP57 POWER OK H)
(KP27 TRAP L)
(KP31 DEFER H)
(KP51 DCH SYNC B L)

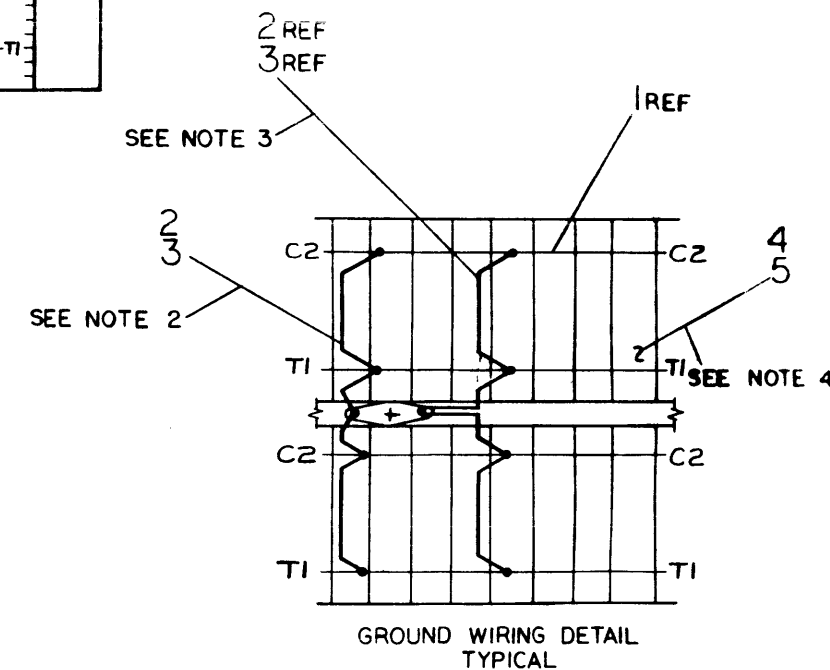
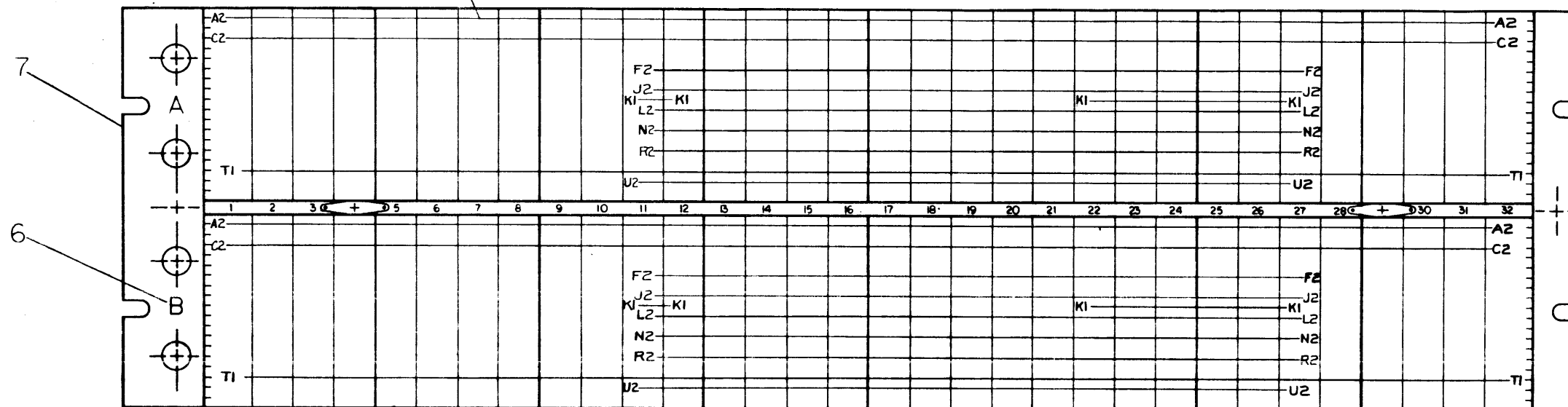
REVISIONS		
CHK	CHANGE NO.	REV.
--	MX15A-00001	00
ORIGINATED		

DRN. <i>John Wiley</i>	DATE <i>10/20/70</i>	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
CHFD. <i>W. H. Wiley</i>	DATE <i>10/20/70</i>	
ENG. <i>W. H. Wiley</i>	DATE <i>10/20/70</i>	
PROJ. ENG. <i>W. H. Wiley</i>	DATE <i>10/20/70</i>	
PROD. <i>W. H. Wiley</i>	DATE <i>10/20/70</i>	
FIRST USED ON		TITLE MEMORY PORT 3
MX15		SIZE/CODE D IC
SCALE		NUMBER MX15-A-23
SHEET 1 OF 1		REV. 00

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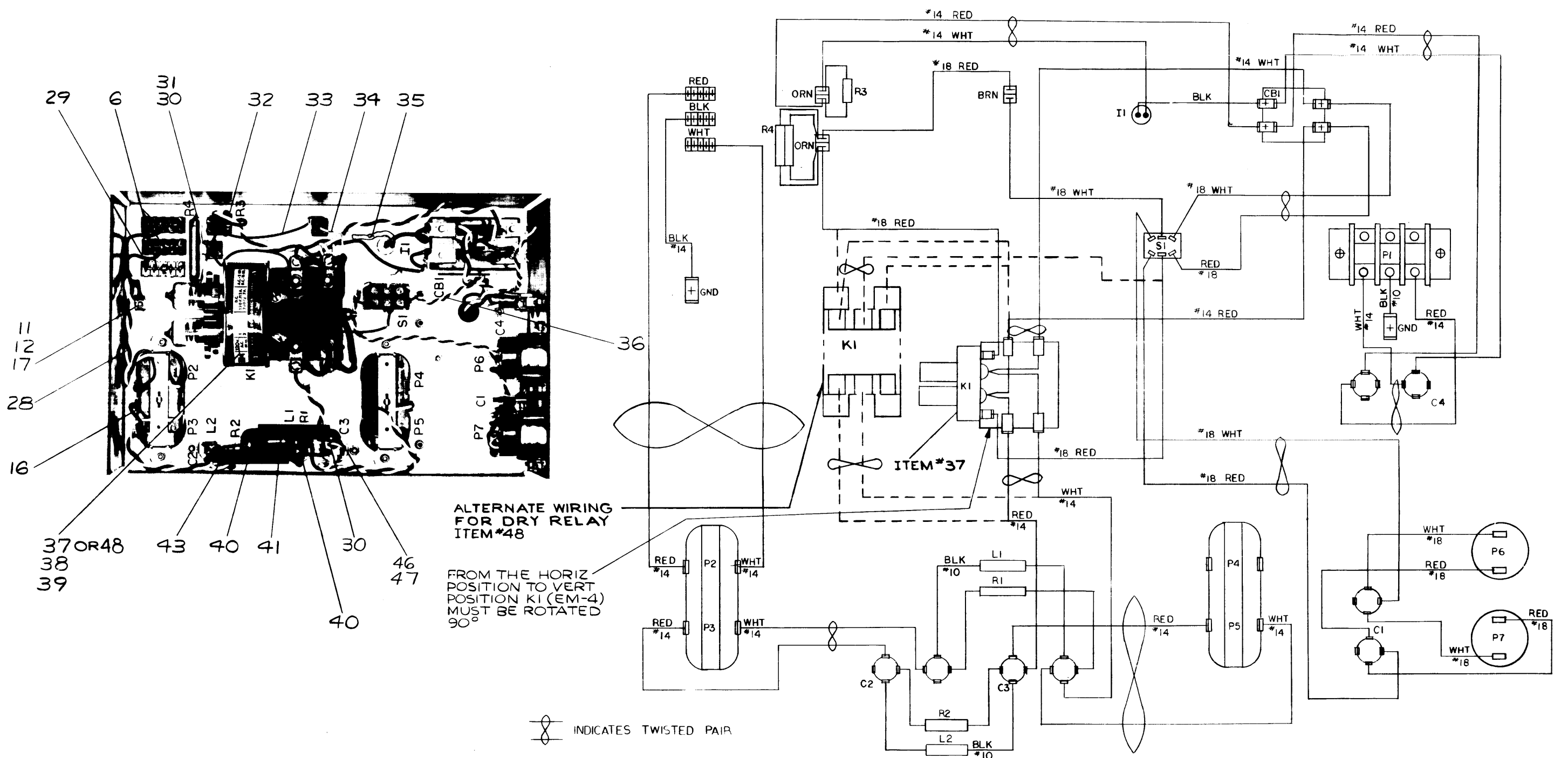
NOTES:

1. CONNECTIONS ON ITEM NUMBER 1 & 2 TO BE LOCATED AND SOLDERED AT MINIMUM PRACTICAL HEIGHT ABOVE BLOCKS.
2. ALL CONNECTOR BLOCKS TO BE GROUNDED TO GROUND LUGS AS SHOWN, 2 PLACES.
3. JUMPER GROUND BUSSING AS SHOWN, 8 PLACES.
4. USE YELLOW WIRE (ITEM #4) FOR MACHINE WRAPPED AND BLUE WIRE (ITEM #5) FOR HAND WRAPPED WIRING.



FIRST USED ON OPTION/MODEL		QTY.	DESCRIPTION	PART NO.
MX15 - A				
DO NOT SCALE DRAWING		DRN. W.F. McCarthy	DATE 4/28/70	
UNLESS OTHERWISE SPECIFIED		CHKD. W.F. McCarthy	DATE 5/12/70	
DIMENSION IN INCHES		ENG. J. B. McCarthy	DATE 5/12/70	
TOLERANCES		PROJ. ENG. J. B. McCarthy	DATE 5/12/70	
DECIMALS FRACTIONS ANGLES		PROP. J. B. McCarthy	DATE 5/12/70	
± .005 ± 1/64 ± 0°30'				
FINAL SURFACE QUALITY				
REMOVE BURRS AND BREAK SHARP CORNERS				
MATERIAL		NEXT HIGHER ASSY		
		D-UA-MX15-0-0		
FINISH		SCALE NONE	SIZE/CODE	NUMBER
		SHEET 1 OF 1	D AD 7006862-0-0	REV.

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WIRING DIAGRAM

REV.	CHANGE NO.	REVISION

FIRST USED ON OPTION 7 MODEL:		QTY.	DESCRIPTION	PART NO.	ITEM NO.
UNLESS OTHERWISE SPECIFIED		PARTS LIST			
UNLESS OTHERWISE SPECIFIED		digital EQUIPMENT CORPORATION MAINTARD MASSACHUSETTS			
DIMENSION IN INCHES		TITLE			
TOLERANCES		POWER CONTROL			
DECIMALS FRACTIONS ANGLES		841-B			
± .005 ± 1/64 ± 0/30		841-C			
FINAL SURFACE QUALITY		SIZE CODE NUMBER REV.			
REMOVE BURRS AND BREAK CHAMF CORNERS		DUA 841-B Ø			
MATERIAL		SHEET OF			
FINISH					

NOTE - DOTTED
LINES FOR
HIOVAC INPUT

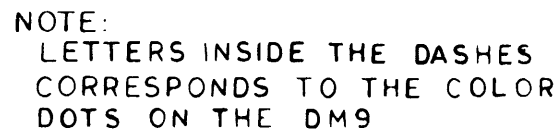


INPUT CONNECTION CHART			
INPUT	CONNECTION	JUMPER	TO
220 VAC	TB2-1 AND TB2-2	TB1-4	TB1-5
		TB1-3	TB1-2
		TB1-1	TB1-3
110 VAC	TB2-1 AND TB2-2	TB1-2	TB1-4
		TB1-5	TB1-3
		TB1-3	TB1-5

COMPONENT CHART				VENDOR
CKT. REF	DESCRIPTION			PART NO.
A1	P. C. CARD ASS'Y.			618 1979
B1	FAN			312 0020
C100	CAPACITOR	12,000 MFD @ 30 VDC		304 2159
C102, 201	CAPACITOR	100 MFD @ 25 VDC		304 1282
C103, 202	CAPACITOR	0.0068 MFD @ 100 VDC		304 0992
C200	CAPACITOR	19,000 MFD @ 40 VDC		304 2170
C307, 308	CAPACITOR	1.0 MFD @ 50 VDC		304 1106
C306	CAPACITOR	0.001 MFD @ 100 VDC		304 0714
C300, 301	CAPACITOR	50,000 MFD @ 25 VDC		304 2153
C302	CAPACITOR	500 MFD @ 25 VDC		304 1383
C303	CAPACITOR	0.0022 MFD @ 100 VDC		304 1048
C304	CAPACITOR	0.68 MFD @ 35 VDC		304 1332
C305	CAPACITOR	390 MFD @ 10VDC		304 1397
T1	TRANSFORMER			602 2264
CR100, 101	DIODE	BRIDGE		337 1558
CR200, 201	"	"		"
CR300, 301	DIODE	1N645		337 1363
CR302, 303	DIODE	1N1185A		337 1329
F100	FUSE	3A AGC		315 0049
F200	FUSE	5A AGC		315 0242
F300	FUSE	25A AGC		315 0093
F400	FUSE	12A ABC		315 0218
Q302	TRANSISTOR	2N3055		370 0202
Q100, 200	TRANSISTOR	2N1613		370 0072
Q301	"	"		"
Q101, 201	TRANSISTOR	2N3054		370 0223
Q303-310	TRANSISTOR	2N3055		370 0219
Q102, 103	"	"		"
Q202, 203	"	"		"
Q300	S. C. R.	C30U		337 1560
R100, 106	RESISTOR	2600 5 W. 1%		340 1732
R101	RESISTOR	5600 1 W. 5%		340 0619
R102, 201	RESISTOR	15000 1 W. 5%		340 0629
R103	RESISTOR	6800 1/2 W. 1%		340 6111
R104, 204	POT.	5000 3/4 W. ±10%		341 0656
R303, 308	"	" " " "		"
R105, 205	RESISTOR	9090 1/2 W. 1%		340 6279
R200	RESISTOR	3000 10 W. 5%		340 1902
R202	RESISTOR	2.7K 1 W. 5%		340 0635
R203	RESISTOR	16900 1/2 W. 1%		340 6278
R300, 311	RESISTOR	1000 10 W. 5%		340 1900
R301	RESISTOR	620 2 W. 5%		340 0819
R302	RESISTOR	7500 1/2 W. 1%		340 6113
R304	RESISTOR	22100 1/2 W. 1%		340 6236
R305	RESISTOR	2K 1/2 W. 5%		340 0160
R306	RESISTOR	1K 1/2 W. 5%		340 0153
R307	RESISTOR	6800 1/2 W. 5%		340 0149
R309	POT.	500 3/4 W. ±20%		341 0657
R310	RESISTOR	0.0250 25 W. ±3%		340 2966
S1	THERMOSTAT			366 0430
VR100, 200	ZENER	1N751A		337 1072
VR300	"	"		"
VR301	I.C. REG.	UA723C		371 3001
VR302	ZENER	1N749A		337 1241

FIRST USED ON OPTION/MOD PDP-15		QTY.	DESCRIPTION		PART NO.		ITEM NO.
UNLESS OTHERWISE SPECIFIED		DRW	PARTS LIST				
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES		CHK'D	DATE		digital EQUIPMENT CORPORATION WATYARD, MASSACHUSETTS		
TOLERANCES DECIMALS FRACTIONS ANGLES ± .005 ± 1/64 ± 0°30'		ENG	DATE		TITLE		
FINAL SURFACE QUALITY REMOVE BURRS AND BREAK SHARP CORNERS		PROJ. ENG.	DATE		H721		
MATERIAL		PROD.	DATE		CIRCUIT SCHEMATIC		
		NEXT HIGHEST ASSY					
FINISH		SCALE		SIZE	CODE	NUMBER	REV.
		SHEET OF		D	C	H721-0-1	
				DIST.			

SIZE	B	CS	798-0-1	REV. A
CODE			NUMBER	



X HEYMAN MFG CO TAB-
TERMINAL IN PLASTIC BUSHINGS
 CINCH JONES TERMINAL STRIP

REVISIONS		
CHK	CHG NO.	REV
<i>end</i>	798- 05501	A

DRN. P. LOR	DATE 10-1-68
CHK'D E. M. Lewis	DATE 10-16-68
ENG. J. L. Lewis	DATE 10-22-68
PROD J. L. Lewis	DATE 10-22-68

[illegible]

digital
EQUIPMENT
CORPORATION
MAYNARD, MASSACHUSETTS

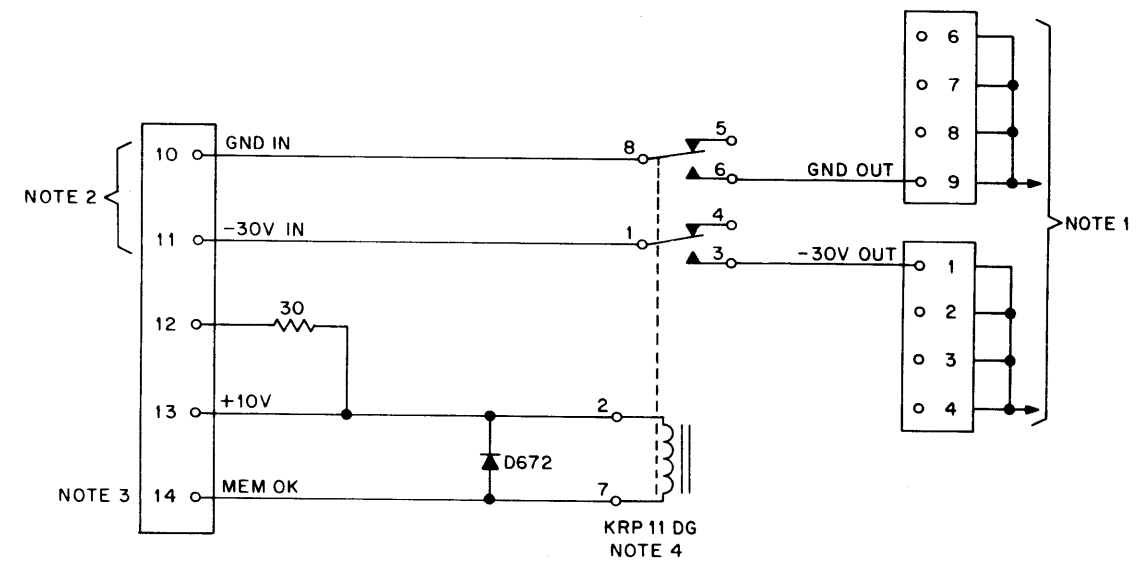
TITLE DUAL 15 VOLT
POWER SUPPLY 798

SIZE B	CODE CS	NUMBER 798-0-	REV A
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[illegible]

DEC FORM NO.
DRB 102

PINK	DATE	7-1	1961	1136
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NOTES:

1. -30V GOES TO G825 OF MEMORY GND ALSO GOES TO MEMORY
2. THE SOURCE COMES FROM 798 POWER SUPPLY.
3. WHEN THIS POINT IS SWITCHED FROM GND - THERE IS A PROBLEM IN MEM WHICH THIS GUARDS.
4. KRP11 DG - THE RELAY IS A DPDT WITH A COIL VOLTAGE OF 12 VDC. THE SUFFIX (G) MEANS SILVER-CADMIUM CONTACTS RATED 10 AMPS.