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MS11-M MOS memory user guide

digital

EK-MS11M-UG-001

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user guide

digital equipment corporation • maynard, massachusetts

1st Edition, May 1979

Printed in U.S.A.

This document was set on DIGITAL's DECset-8000 computerized typesetting system.

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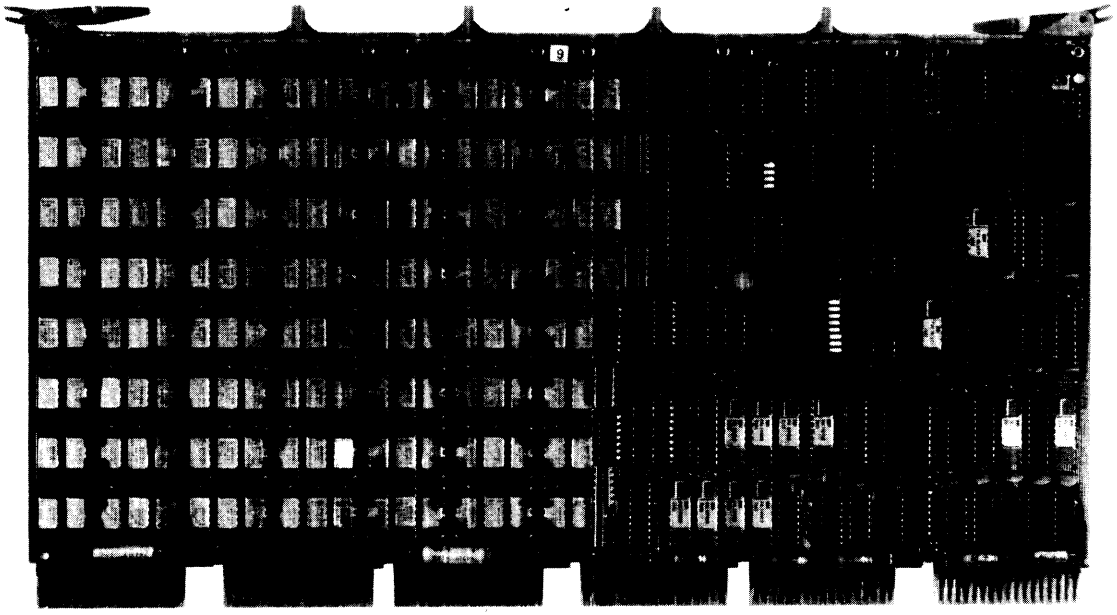

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MS11-M MOS Memory

CHAPTER 1
CHARACTERISTICS AND SPECIFICATIONS

1.1 INTRODUCTION

The MS11-M is a metal oxide semiconductor (MOS), random access memory (RAM), designed to be used with the PDP-11 Unibus or extended Unibus. The memory assumes the role of a slave device to the PDP-11 processor or to any peripheral device designated bus master. The MS11-M utilizes an error correction code (ECC) to increase the reliability of the memory. There are two versions of the MS11-M: the MS11-MA (M8722-AA) which provides 64K × 16-bit data storage; and the MS11-MB (M8722-BA) which provides 128K × 16-bit data storage. Note that the two versions are differentiated by the total memory capacity available on the module.

1.2 GENERAL DESCRIPTION

The MS11-M consists of a single hex-height module (M8722) that contains the Unibus/extended Unibus interface, timing and control logic, error correcting code (ECC) logic, and a MOS storage array. The module also contains circuitry for ECC-initialization and memory refresh, and a control and status register (CSR).

The memory starting address can be set at any 64K boundary within the 128K Unibus address space or 2048K extended Unibus address space. (The extended Unibus contains 22 address lines as opposed to 18 Unibus address lines.) The MS11-M reserves the top 4K of the Unibus or extended Unibus address space for the I/O peripheral page. The MS11-M also allows address interleaving between two memory modules that have the same storage capacity.

The MOS storage array is configured in 39-bit words which consist of 2 16-bit PDP-11 words and 7 check bits generated by the ECC logic. The error correction code allows the MS11-M to detect a single-bit or double-bit error within the 39-bit word, and to correct a single-bit data error. A double-bit error is not corrected by the MS11-M and can cause a parity error trap. A single-bit error is transparent to the Unibus/extended Unibus.

The memory storage elements are 16384 × 1-bit, MOS dynamic RAM devices. The MOS storage array contains 39 of these devices for each 32K bank of PDP-11 memory; e.g., a 128K memory contains 156 storage devices, a 64K memory contains 78 storage devices. The MOS storage devices are periodically refreshed by specially-timed, refresh cycles, executed by the MS11-M so that the data and check bits remain valid.

Since the MOS storage devices are volatile (data is not retained when power is lost), a battery backup unit is available as an option to support the MOS power supply regulator(s). Therefore, dc power is available to MOS memory only for a limited time during an ac power failure. The MS11-M memory module has inputs for ±12 V power and two sources of +5 V power, designated +5 VBB and +5 V. The ±12 V and +5 VBB module inputs are battery supported during an ac power failure; the +5 V input is not battery supported. The power distribution lines on the module are arranged to accommodate the use of the battery backup option. In the battery support mode, power is used only to refresh the MOS storage array so that battery backup time and therefore data retention time are maximized. A green LED on the module stays on as long as power is applied to the +5 VBB input.

If +5 VBB (and therefore data) was lost during an ac power failure, the MS11-M performs an error correction initialize (ECC INIT) operation after the power-up. For an ECC INIT operation, logical 0s and the corresponding check bit pattern are written twice into all 39-bit word locations in the MOS storage array. Signal AC LO is asserted by the memory while the ECC INIT operation is in progress.

The control and status register (CSR) in the MS11-M allows program control of certain ECC functions and stores diagnostic information if an error has occurred. The CSR has its own address in the I/O peripheral page, and can be read or written into by any device designated as bus master, even during a memory refresh cycle.

Although the MOS storage array is configured in 39-bit words, the bus master sees the MS11-M as a standard 16-bit memory. The memory response to the four types of data transfers (DATI, DATIP, DATO, and DATOB) is discussed in the following paragraphs.

1.2.1 DATI or DATIP Data Transfer

Memory responds to a DATI or DATIP data transfer by performing a read cycle. (A DATIP data transfer is interpreted as a DATI.) The 39-bit word which contains the requested data is retrieved from the MOS storage array, and 7 check bits are calculated based on the 32 retrieved data bits. The newly calculated check bits are then compared to the seven retrieved check bits, creating seven syndrome bits. A logical 1 in the syndrome bit pattern indicates an error in the 39-bit word; an odd number of logical 1s indicates a single-bit error while an even number of logical 1s indicates a double-bit error. If no error is detected, the memory places the requested 16-bit data on the Unibus/extended Unibus and asserts the SSYN signal.

If a single-bit error is detected during a read cycle, the MS11-M initiates the following action:

1. A single-bit error within the 32 data bits is corrected
2. Bit 4 in the CSR is set to 1
3. A partial address of the requested data is recorded in the CSR, if CSR bit 15 is cleared to 0
4. The requested 16-bit data and the SSYN signal are asserted on the Unibus/extended Unibus after a delay of approximately 70 ns. Therefore, the memory access time is increased due to a single-bit error.

Note that the syndrome bits are used to determine if the single-bit error is contained in the retrieved data or check bits, and to isolate a bad data bit. A check bit error is not corrected; however, the other single-bit error reactions are the same.

If a double-bit error is detected it is not corrected. However, the memory initiates the following actions:

1. Bit 15 in the CSR is set to 1
2. A red LED on the module turns on, providing a visual indication of a double-bit (uncorrectable) error
3. A partial address of the requested data is recorded in the CSR. Any address information relating to a previous error is destroyed
4. If bit 0 in the CSR is set, the memory asserts BUS PBL which warns the processor that a double-bit (uncorrectable) error has occurred.

5. The requested 16-bit data and the SSYN signal are asserted on the Unibus/extended Unibus after a delay of approximately 70 ns. Therefore, the memory access time is increased due to a double-bit error.

1.2.2 DATO or DATOB Data Transfer

Memory responds to a DATO or DATOB data transfer by performing a read-modify-write (RMW) cycle. During the first portion of the RMW cycle the data byte(s) supplied by the bus master are latched-in from the Unibus/extended Unibus and the SSYN signal is asserted. The 39-bit word which includes the desired PDP-11 location is then retrieved from the MOS storage array. Based on the 32 retrieved data bits, 7 check bits are calculated and then compared to the retrieved check bits, creating 7 syndrome bits. The syndrome bits are examined to determine if the 39-bit word contains a single-bit or double-bit error. A single-bit error in the data is corrected, but a double-bit error in the 39-bit word is not corrected.

The manipulation of data during the remaining portion of the RMW cycle is the same for a no error or corrected error condition. The 39-bit word is modified by merging the data byte(s) supplied by the bus master with the old data bytes from the storage array. Check bits are generated based on the four data bytes, and the modified 39-bit word is then written into the MOS storage array. For a DATO data transfer, the modifed 39-bit word contains 2 new bytes, two old bytes, and seven new check bits. For a DATOB, the modified word contains one new byte, three old bytes and seven new check bits.

If a double-bit error is detected during the first portion of the RMW cycle, the four bytes of old data and the old check bits are rewritten into the MOS storage array. Therefore, the double-bit error is preserved and will be flagged if the 39-bit word is retrieved during a DATI or DATIP data transfer. The data supplied by the bus master is lost.

1.3 SPECIFICATIONS

1.3.1 Functional Specifications

Capacity

MS11-MA	65,536(64K) words	16-bit PDP-11 words
MS11-MB	131,072(128K) words	

Refresh Timing

Cycle time	620 ns (typical), 675 ns (maximum)	
Repetition rate	One cycle every:	12.5 microseconds (typical) 11.25 microseconds (fastest) 13.75 microseconds (slowest)

NOTE

Refresh cycle time is defined as the time interval between the assertion of REF REQ (1) H and the negation of MBSY L. These signals are internal to the memory module.

ECC INIT Time — 451 ms (maximum)

NOTE

ECC INIT time is defined as the time interval between the negation of DC LO (at the output of the memory receiver) and the negation of AC LO (on the Unibus/extended Unibus) by the memory.

Access and Cycle Times (Table 1-1)

Table 1-1 Access and Cycle Times

Data Transfer	Access Time (ns)		Cycle Time (ns)	
	Typical	Maximum	Typical	Maximum
DATI/DATIP (Memory)	490(560 w/err)	525(600 w/err)	450	500
DATO/DATOB (Memory)	220	250	950	1000
DATI/DATIP (CSR)	115	150	-	-
DATO/DATOB (CSR)	115	150	-	-

NOTES

1. Access time - The time interval between memory reception of MSYN (at the input of the bus receiver) and the assertion of SSYN on the Unibus/extended Unibus.

   Cycle time - The time interval between memory reception of MSYN (at the output of the bus receiver) and the negation of MBSY L. Signal MBSY L is internal to the memory module.

2. If the memory is accessed by a bus master during a refresh cycle, the data transfer is delayed until the refresh cycle is completed. In the worst case, memory access and cycle times are increased by the entire refresh time; 620 ns (typical), 675 ns (maximum). Access to the CSR is not affected by a refresh cycle.

1.3.2 Electrical Specifications

Voltage Requirements +5 V ±5%, max ripple = 0.2 V p-p
+5 VBB ±5%, max ripple = 0.2 V p-p
+12 V ±5%, max ripple = 1 V p-p
-12 V ±10%, max ripple = 1 V p-p

Current and Power Requirements (Tables 1-2 and 1-3)

Table 1-2 Current Requirements

Memory Option	+5 V		+5 VBB		-12 V		+12 V			
							Standby		Active	
	Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	Max
MS11-MA	3.8 A	4.8 A	1.2 A	1.5 A	25 mA	50 mA	0.15 A	0.2 A	0.55 A	0.8 A
MS11-MB	3.8 A	4.8 A	1.2 A	1.5 A	30 mA	50 mA	0.3 A	0.4 A	0.7 A	1.0 A

NOTES

1. The total module consumption of +5 V current during normal operation is equal to the sum of the +5 V and +5 VBB ratings.

2. The standby and active ratings for +5 V, +5 VBB and −12 V are the same. The current drawn from the +12 V supply varies directly with the frequency of operation; e.g., the stated +12 V active ratings are obtained at a 1 microsecond repetition rate. Interleaving can almost double the current drawn from the +12 V supply depending on bus overhead (e.g., two interleaved MS11-MB modules can collectively consume up to 4 A as opposed to 2 A for the noninterleaved case).

Table 1-3 Total Module Power Requirements

Memory Option	Standby		Active		Battery Backup Mode	
	Typ	Max	Typ	Max	Typ	Max
MS11-MA	27.1 W	34.5 W	31.9 W	41.7 W	8.1 W	10.5 W
MS11-MB	28.9 W	36.9 W	33.7 W	44.1 W	9.9 W	12.9 W

1.3.3 Physical and Environmental Specifications

Module designation

MS11-MA M8722-AA
MS11-MB M8722-BA
} All versions are hex-height multilayer, 21.6 × 38.1 cm (8.5 × 15 inches)

Operating temperature — 5 to 50° C (41° to 122° F)

Humidity — 10 to 95% (noncondensing)

1.4 RELATED DOCUMENTS

Additional reference information can be found in the documents listed below.

Title	Document No.	Availability
PDP-11 Peripherals Handbook	EB-05961	Hardcopy only
PDP-11/04/34/45/55/60 Processor Handbook	EB-09340	Hardcopy only
PDP-11/44 User's Guide	EK-11044-UG	Hardcopy only

These documents can be ordered from:

Digital Equipment Corporation
444 Whitney Street
Northboro, MA 01532

Attn: Communication Services (NR2/M15)
Customer Services Section

For information concerning Microfiche Libraries, contact:

Digital Equipment Corporation
Micropublishing Group
PK3-2/T12
Maynard, MA 01754

CHAPTER 2
INSTALLATION AND PROGRAMMING

2.1 GENERAL

This chapter presents the information necessary for installation and programming of the MS11-M and applies to both versions of the memory. Installation procedures include: switch/jumper settings, backplane placement, power voltage checks, and MAINDEC testing. Programming information includes a discussion of bit assignments in the control and status register (CSR).

2.2 INSTALLATION

2.2.1 Switch and Jumper Configurations

The MS11-M contains two jumpers and two switchpacks; one switchpack contains four switches (S1-1 through S1-4) and the other contains eight switches (S2-1 through S2-8). The location of the jumpers and switches is shown in Figure 2-1. The switches are used to specify the memory starting address, interleaved or noninterleaved operation, and the CSR address. Unibus or extended Unibus operation is specified by jumper W1. Jumper W2 is related to the storage capacity of the memory and should not be tampered with in the field.

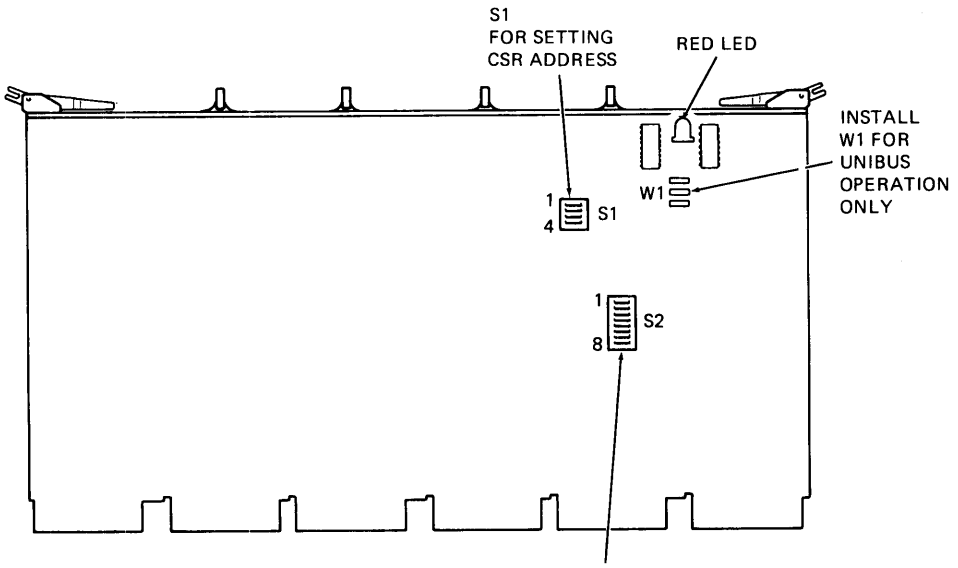
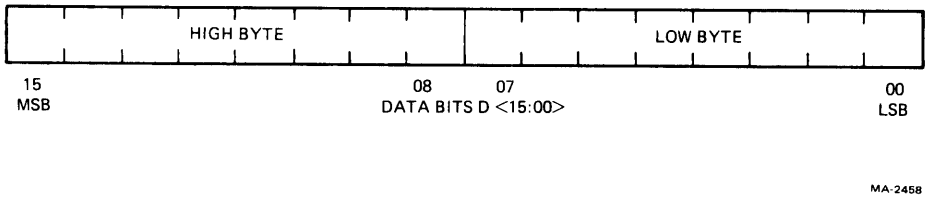


Figure 2-1 Switch and Jumper Locations

2.2.1.1 Memory Addressing

PDP-11 Memory Conventions - The MS11-M can be used with the PDP-11 Unibus or extended Unibus. Memory in these computer systems provides storage for 16-bit data words, each containing two 8-bit bytes. These bytes are identified as low or high, as shown below.



Each byte is addressable and has its own address location; low bytes are even-numbered and high bytes are odd-numbered. Words are addressed by even numbered locations only, and the high (odd) byte for each word is automatically included.

Via the Unibus, 131,072 (128K) words or 262,144 (256K) bytes can be addressed; 2,097,152 (2048K) words or 4,194,034 (4096K) bytes can be addressed via the extended Unibus. Each byte location in Unibus memory is specified by a 6-digit octal number, but with the extended Unibus, 8-digit octal numbers are used. The address range is 000000–777777 on the Unibus and 00000000–17777777 on the extended Unibus (Figure 2-2).

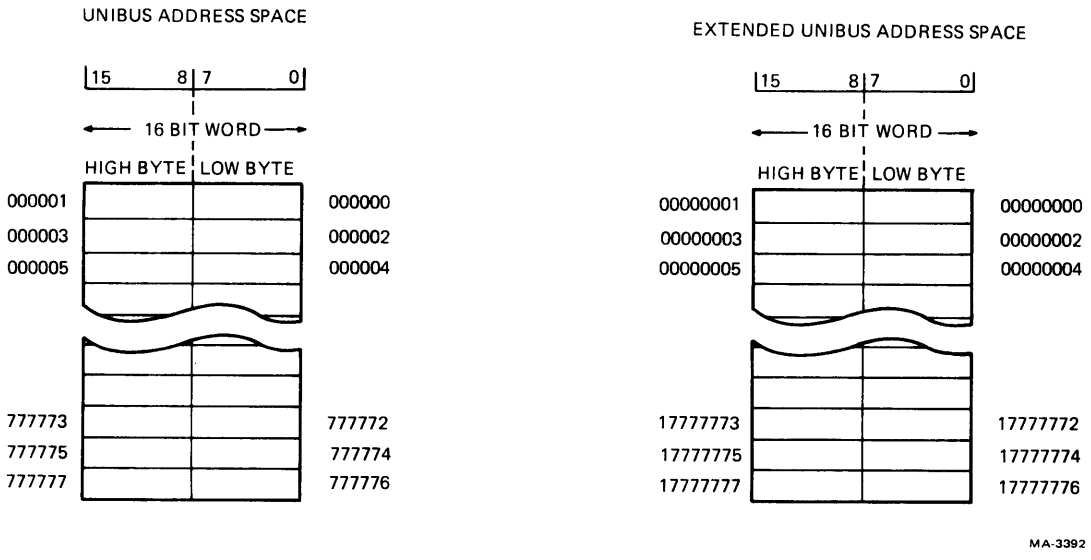
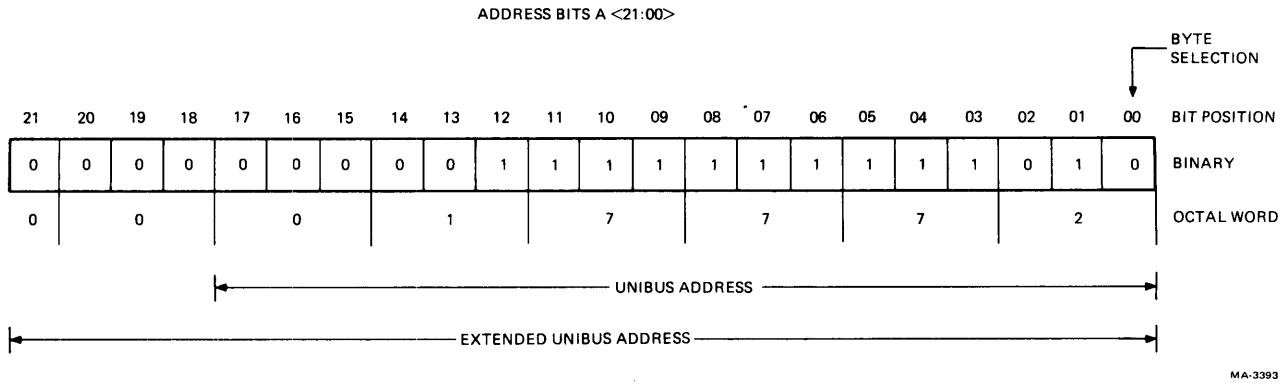


Figure 2-2 Bus Accessible Data Locations

The memory address decoding logic responds to the binary equivalent of the octal address. The binary equivalent of 00017772 is shown below. The MS11-M decodes an 18-bit address (A17–A00) on the Unibus or a 22-bit address (A21-A00) on the extended Unibus.



The address space on a bus occupied by a memory module is determined by the memory starting address, storage capacity, and interleaving information. A unique starting address is selected by switches on the MS11-M which correspond to address bits A21–A17 on the extended Unibus or A17 on the Unibus. For noninterleaved operation, the block of addresses occupied by each module is continuous. Table 2-1 lists the noninterleaved, octal address ranges of the MS11-M versions and the associated address bits which determine the word location within the module. Address bit A00 is used to select a data byte during a DATOB bus cycle.

Table 2-1 MS11-M Address Ranges (Noninterleaved)

Memory Designation	Storage Capacity	Octal Address Range (Noninterleaved)	Associated Address Bits
MS11-MA	65,536 words (131,072 bytes)	00000000–00377777	A16-A00
MS11-MB	131,072 words (262,144 bytes)	00000000–00777777	A17-A00

Memory Starting Address Selection – The memory starting address is the lowest bus address to which the MS11-M responds in the noninterleaved mode. The starting address must be assigned to a 64K boundary within the 128K Unibus address space or 2048K extended Unibus address space. The starting address is assigned by manually setting five switches, S2-1 through S2-5, to the appropriate positions for the desired location (Table 2-2).

Table 2-2 Starting Address Configurations

Starting Address		Switch Positions				
Decimal	Octal	S2-5 (A21)	S2-4 (A20)	S2-3 (A19)	S2-2 (A18)	S2-1 (A17)
0K	00000000	ON	ON	ON	ON	ON
64K	00400000	ON	ON	ON	ON	OFF
128K	01000000	ON	ON	ON	OFF	ON
192K	01400000	ON	ON	ON	OFF	OFF
256K	02000000	ON	ON	OFF	ON	ON
320K	02400000	ON	ON	OFF	ON	OFF
384K	03000000	ON	ON	OFF	OFF	ON
448K	03400000	ON	ON	OFF	OFF	OFF
512K	04000000	ON	OFF	ON	ON	ON
576K	04400000	ON	OFF	ON	ON	OFF
640K	05000000	ON	OFF	ON	OFF	ON
704K	05400000	ON	OFF	ON	OFF	OFF
768K	06000000	ON	OFF	OFF	ON	ON
832K	06400000	ON	OFF	OFF	ON	OFF
896K	07000000	ON	OFF	OFF	OFF	ON
960K	07400000	ON	OFF	OFF	OFF	OFF
1024K	10000000	OFF	ON	ON	ON	ON
1088K	10400000	OFF	ON	ON	ON	OFF
1152K	11000000	OFF	ON	ON	OFF	ON
1216K	11400000	OFF	ON	ON	OFF	OFF
1280K	12000000	OFF	ON	OFF	ON	ON
1344K	12400000	OFF	ON	OFF	ON	OFF
1408K	13000000	OFF	ON	OFF	OFF	ON
1472K	13400000	OFF	ON	OFF	OFF	OFF
1536K	14000000	OFF	OFF	ON	ON	ON
1600K	14400000	OFF	OFF	ON	ON	OFF
1664K	15000000	OFF	OFF	ON	OFF	ON
1728K	15400000	OFF	OFF	ON	OFF	OFF
1792K	16000000	OFF	OFF	OFF	ON	ON
1856K	16400000	OFF	OFF	OFF	ON	OFF
1920K	17000000	OFF	OFF	OFF	OFF	ON
1984K	17400000	OFF	OFF	OFF	OFF	OFF

Switches S2-1 through S2-5 correspond to address bits A17-A21 respectively on the extended Unibus. A switch in the OFF position corresponds to a logical 1.

NOTE
Switches S2-2 through S2-5 should be set to the ON position if the MS11-M is used with the PDP-11 Unibus.

Unibus or extended Unibus operation of the MS11-M is selected by jumper W1:

W1 OUT	Specifies extended Unibus operation
W1 IN	Specifies Unibus operation

Interleave/Noninterleave Selection – A continuous (noninterleaved) address block can be assigned to each MS11-M module, or an address block can be interleaved between two MS11-M modules that have the same storage capacity. Figure 2-3 shows two 128K memories in the interleaved mode and the corresponding noninterleaved mode.

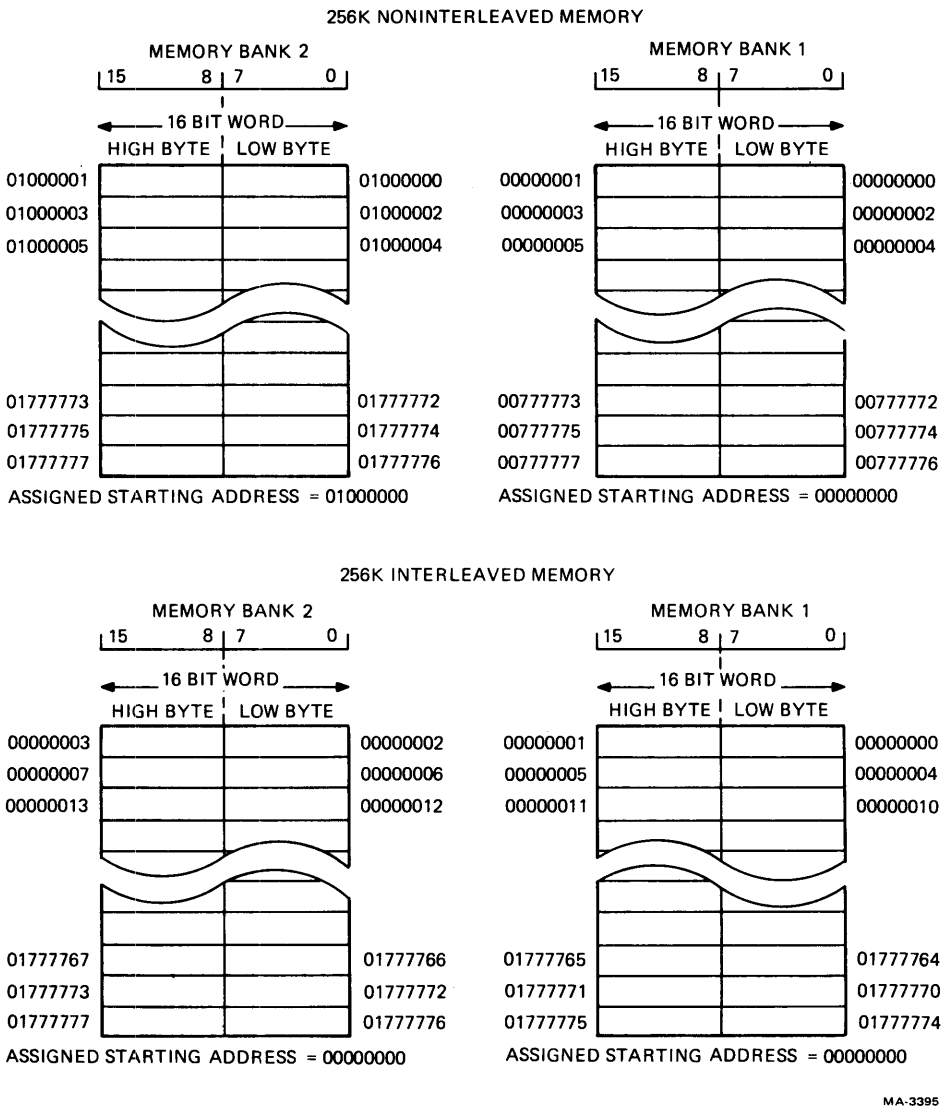


Figure 2-3 Interleaved Versus Noninterleaved Memory Organization of Two 128K Memory Banks

For noninterleaved operation of a 128K or 64K memory, switches S2-6 through S2-8 should be OFF and each module should be assigned a unique starting address (Table 2-2).

Except for the address ranges involved, interleaved operation for two 64K memories is the same as for two 128K memories. When two 128K modules are interleaved, one memory is assigned all the even addressed words within a 256K block of word addresses; the second memory is assigned all the odd addressed words in the same block. Address bit A01 is used to determine if a word is even or odd addressed. If consecutively addressed words are accessed by the bus master for a DATO or DATOB data transfer, the two memories are accessed alternately so the memory cycles can overlap. Therefore, the bus master sees a reduction in memory cycle time (averaged over a number of DATO or DATOB data transfers).

To specify interleaved operation, switches S2-6 through S2-8 should be set to the appropriate positions on each module (Table 2-3), and both modules should be assigned the same starting address (Table 2-2). The assigned starting address for two interleaved 128K (64K) modules is the lowest address in the 256K (128K) block.

Table 2-3 Interleave Mode Selection

Switch Positions			Mode
S2-6	S2-7	S2-8	
OFF	OFF	OFF	Noninterleaved memory
ON	ON	OFF	One interleaved memory; contains the even addressed words (A01=0)
ON	OFF	ON	Second interleaved memory; contains the odd addressed words (A01=1)

NOTE
The five remaining switch configurations that are not listed should never be used.

For interleaved operation on the extended Unibus, address bits A18-A02 determine the word location within a 128K module; A17-A02 are used for a 64K module. Address bit A00 is used to select a data byte during a DATOB bus cycle. Note that on the Unibus only two 64K modules can be interleaved.

2.2.1.2 CSR Address Selection – The control and status register (CSR) can be read or written into via the Unibus/extended Unibus, even during a memory refresh cycle. Address decoding logic in the MS11-M specifies the CSR address in the range 772100–772136 for Unibus operation or 17772100–17772136 for extended Unibus operation. Four switches, S1-1 through S1-4, select the exact CSR address (Table 2-4). Switches S1-1 through S1-4 correspond to address bits A04-A01 respectively; a switch in the OFF position corresponds to a logical 1. The CSR is always accessed as an entire data word since bit A00 is not decoded by the CSR address logic.

The CSR address has no relevance to the memory starting address, storage capacity, or interleave mode of the MS11-M. However, for organizational purposes only, it may be helpful to assign the CSR address in accordance with the assigned memory starting address (e.g., assign the lowest CSR address to the module which has the lowest memory starting address). Between two interleaved modules, assign the lower CSR address to the module that contains the even addressed words (Table 2-3).

Table 2-4 CSR Address Selection

		Switch Positions			
Unibus Address	Extended Unibus Address	S1-1 (A04)	S1-2 (A03)	S1-3 (A02)	S1-4 (A01)
772100	17772100	ON	ON	ON	ON
772102	17772102	ON	ON	ON	OFF
772104	17772104	ON	ON	OFF	ON
772106	17772106	ON	ON	OFF	OFF
772110	17772110	ON	OFF	ON	ON
772112	17772112	ON	OFF	ON	OFF
772114	17772114	ON	OFF	OFF	ON
722116	17772116	ON	OFF	OFF	OFF
772120	17772120	OFF	ON	ON	ON
772122	17772122	OFF	ON	ON	OFF
772124	17772124	OFF	ON	OFF	ON
772126	17772126	OFF	ON	OFF	OFF
772130	17772130	OFF	OFF	ON	ON
772132	17772132	OFF	OFF	ON	OFF
772134	17772134	OFF	OFF	OFF	ON
772136	17772136	OFF	OFF	OFF	OFF

2.2.2 Backplane Placement

The MS11-M is compatible with the PDP-11 Unibus or the extended Unibus (EUB) which is the main memory bus in the PDP-11/44.

When used with the PDP-11/44, the MS11-M should be inserted into any one of slots 9 through 12 in the processor backplane (part no. 70-16502-00). Slots 9 through 12, sections A and B, contain the extended Unibus.

For Unibus operation, the MS11-M should be inserted into any slot in a backplane that contains modified Unibus connectors in sections A and B. For example:

DD11-D	Slots 2 through 8
DD11-C	Slots 2 and 3

The MS11-M and other memory types (except the MS11-L) are mutually exclusive with respect to the backplane since the MS11-M requires ±12 V power. The backplane connections used by the MS11-M are listed in Table 2-5.

2.2.3 Power Voltage Check

Once primary power has been turned on, the dc power voltages listed below should be checked at the backplane.

Voltage and Tolerance	Backplane Pin(s)
+5 V ±5%, max ripple = 0.2 V p-p	AA2, BA2, CA2
+5 VBB ±5%, max ripple = 0.2 V p-p	BD1
+12 V ±5%, max ripple = 1 V p-p	AR1
-12 V ±10%, max ripple = 1 V p-p	AS1

2.2.4 MAINDEC Testing

The MS11-L/M Memory Exerciser (MAINDEC-11-CZMSD) diagnostic program should be used with the MS11-M memory module. To verify proper operation of the memory, run two passes of the diagnostic. No double errors are permitted. Also, verify that the program printout agrees with the total memory in the system.

2.3 CSR BIT ASSIGNMENT

The control and status register (CSR) in the MS11-M allows program control of certain ECC functions and contains diagnostic information if an error has occurred. The CSR is assigned an address and can be accessed by a bus master via the Unibus/extended Unibus, even during a memory refresh cycle. Some CSR bits are cleared by the assertion of BUS INIT L. This signal is asserted for a short time after system power has come up or in response to a reset instruction. The CSR bit assignments are illustrated in Figure 2-4 and are described as follows:

Bit 0 Uncorrectable Error Indication Enable	This bit, when set to 1, allows the assertion of BUS PB L when BUS SSYN L is asserted, if an uncorrectable error is detected during a memory read cycle (e.g., with error correction enabled, BUS PB L is asserted for a double-bit error. With error correction disabled, BUS PB L is asserted for a single-bit or double-bit error). Bit 0 can be read or loaded by the program (read/write bit) and is cleared by BUS INIT L.

Table 2-5 MS11-M Pin Out

	A		B		C		D		E		F	
	1	2	1	2	1	2	1	2	1	2	1	2
A	INIT L	+5 V	-	+5 V	NPG IN H]	+5 V	-	-	-	-	-	-
B	-	-	+5 V Battery	-	NPG OUT H]	-	-	-	-	-	-	-
C	D00 L	GND	-	GND	-	-	-	GND	-	-	-	-
D	D02 L	D01 L	+5 V Battery	-	-	-	-	-	-	-	-	-
E	D04 L	D03 L	A19 L	A18 L	-5 V TP	-	-	-	-	-	-	-
F	D06 L	D05 L	AC LO L	DC LO L	-	-	-	-	-	-	-	-
H	D08 L	D07 L	A01 L	A00 L	-	-	-	-	-	-	-	-
J	D10 L	D09 L	A03 L	A02 L	-	-	-	-	-	-	-	-
K	D12 L	D11 L	A05 L	A04 L	-	-	-	BUS G7 SO H]	-	-	-	-
L	D14 L	D13 L	A07 L	A06 L	-	-	-	BUS G7 OUT H]	-	-	-	-
M	-	D15 L	A09 L	A08 L	-	-	-	BUS G6 SO H]	-	-	-	-
N	A21 L	PB L	A11 L	A10 L	-	-	-	BUS G6 OUT H]	-	-	-	-
P	A20 L	-	A13 L	A12 L	-	-	-	BUS G5 SO H]	-	-	-	-
R	+12 V Battery	-	A15 L	A14 L	-	-	-	BUS G5 OUT H]	-	-	-	-
S	-12 V Battery	- -	A17 L	A16 L	-	-	INH REFL TP	BUS G4 SO H]	-	-	-	-
T	GND	-	GND	C1 L	-	-	GND	BUS G4 OUT H]	-	-	-	-
U	+12 V Battery	-	SSYN L	C0 L	-	-	-	-	-	-	-	-
V	-	-	MSYN L	-	-	-	-	-	-	-	-	-

NOTES

1. **Pins AN1, AP1, BE1, and BE2 are used for address lines A21L through A18L in extended Unibus operation. In Unibus operation, the signals on these pins are ignored by the MS11-M (receivers disabled).**

2. **Pins marked by] are tied together on the module to provide grant continuity.**

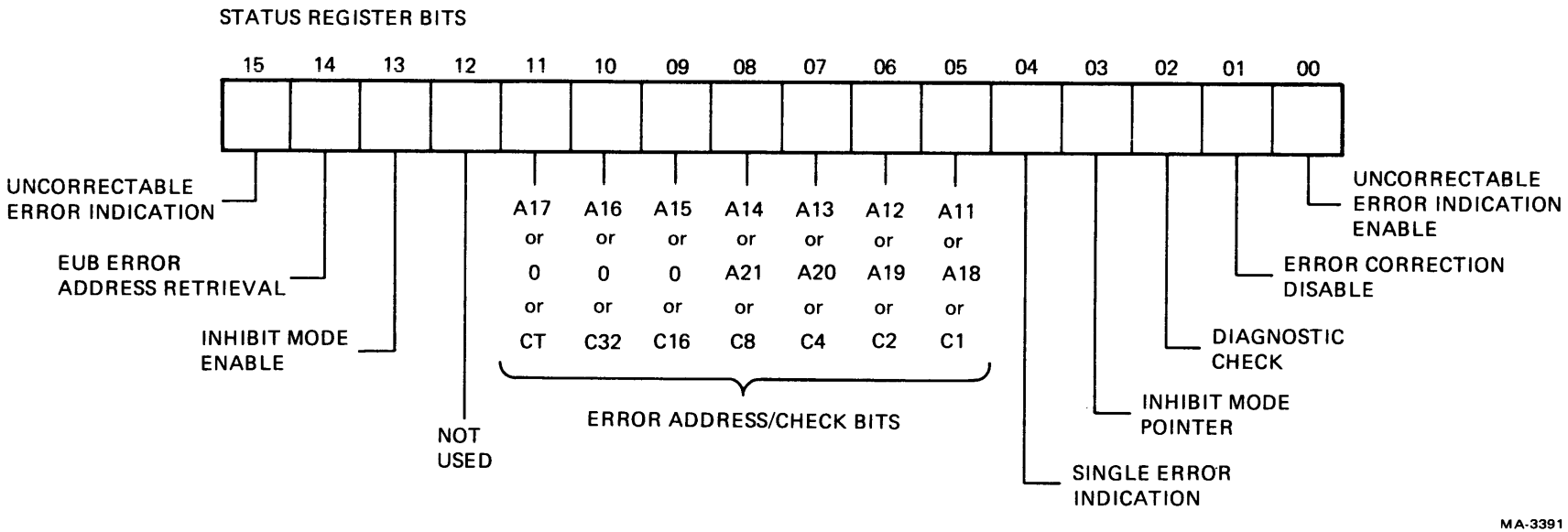


Figure 2-4 CSR Bit Allocation

Bit 1
Error Correction
Disable

This bit, when set to 1, disables single-bit error correction. During a memory read cycle, a single-bit error is treated as an uncorrectable (double-bit) error and is also identified as a single-bit error in the CSR. A double-bit error, detected during a memory read-modify-write (RMW) cycle, does not prevent the modification of the 39-bit word retrieved from the storage array. Therefore, data supplied by the bus master and the generated check bits are allowed to be written into the MOS storage array along with old data. Bit 1 is a read/write bit and is cleared by BUS INIT L.

Bit 2
Diagnostic
Check

This bit, when set to 1, allows the transfer of information between the CSR and MOS RAM chips used for check bit storage. During a memory RMW cycle, data in CSR bits 11-5 is written into the MOS storage array instead of the generated check bits of a 39-bit word. During a memory read cycle, check bits retrieved from the MOS storage array are loaded into CSR bits 11-5. Bit 2 does not affect the detection of a single-bit or double-bit error although a detected double-bit error is ignored by the MS11-M during a RMW cycle. Bit 2 is a read/write bit and is cleared by BUS INIT L.

Bit 3
Inhibit Mode
Pointer

This bit, in conjunction with CSR bit 13, selects a 16K × 16-bit section of memory that is not affected by CSR bits 1 and 2. Therefore, a 16K area of memory can be protected from manipulation in the error correction disable or diagnostic check mode. With bit 13 set to 1 and bit 3 cleared to 0, the first 16K of memory is protected. With bits 13 and 3 set to 1, the second 16K bank is protected. Bit 3 has no effect if bit 13 is cleared to 0. Bit 3 is a read/write bit and is cleared by BUS INIT L.

NOTE

Between two interleaved memory modules, the first 16K of address space is protected if bit 13 is set and bit 3 is cleared on both modules. The second 16K is protected if bits 13 and 3 are set.

Bit 4
Single Error
Indication

This bit, when a 1, indicates the detection of a single-bit error during a memory read cycle. Bit 4 is not affected by any other CSR bit (i.e., bit 1-error correction disable). Bit 4 is a read/write bit and is cleared by BUS INIT L.

Bits 11-5
Error Address and
Check Bit Storage

Error Address Storage - These bits store a partial address of the accessed memory location, recorded on the detection of a single-bit or double-bit error during a memory read cycle. In Unibus operation, address bits A17-A11 are stored in CSR bits 11-5 respectively, specifying the data location to a 1K segment of memory. In extended Unibus operation, address bits A21-A11 are recorded; however, the address bits that appear in bits 11-5 are determined by bit 14.

NOTE

With error correction enabled (bit 1=0), a single-bit error address is not recorded if bit 15 is a 1, indicating that a double-bit error has occurred.

Check Bit Storage – When bit 2 equals 1, CSR bits 11–5 store the check bits read from the storage array, or information to be written into the storage array as the check bits of a 39-bit word. The check bits and error address are recorded if an error is detected during a memory read cycle in the diagnostic mode (bit 2=1). The recorded check bits appear in bits 11–5 while bit 2 is still set to 1. The error address can be retrieved once bit 2 is cleared to 0.

CSR bits 11–5 are not cleared by BUS INIT L.

Bit 12 — This bit is not used and is read as a logical 0.

Bit 13
Inhibit Mode
Enable — This bit, when set to 1, enables bit 3 to inhibit either the first or second 16K portion of memory from ever going into the error correction disable or diagnostic check mode. Bit 13 is a read/write bit and is cleared by BUS INIT L.

Bit 14
EUB Error
Address Retrieval — In normal operation, this bit, when set to 1, causes the MS11-M to place A21–A18 of a recorded error address into CSR bits 8–5; logical 0s are placed in bits 11–9. Address bits A17-A11 are placed in bits 11–5 when bit 14 is cleared to 0, if bit 15 or 4 is a 1. Bit 14 has no effect when the memory is in the diagnostic mode (bit 2=1). In extended Unibus operation, bit 14 is a read/write bit and is cleared by BUS INIT L. In Unibus operation, bit 14 is a read-only bit and is always a 0.

Bit 15
Uncorrectable Error
Indication — This bit, when a 1, indicates the detection of an uncorrectable error during a memory read cycle and also turns on a red LED on the module. Bit 15 is just a flag. This bit is a read/write bit and is cleared by BUS INIT L.

2.3.1 Notes on CSR Usage

For two interleaved memory modules, CSR bits 14, 13, 3, 2, 1, and 0 on both modules should be set to the same value (i.e., bit 1 on both modules is cleared to 0). The values of these bits can be set independently for each module in the noninterleaved mode. For normal operation in the interleaved or noninterleaved mode, CSR bit 0 should be set to 1 and bits 14, 13, 3, 2, and 1 should be cleared to 0.

Bit 1 (error correction disable) is usually set to 1 for diagnostic purposes, allowing data to be read or written into memory without interference from the error correction logic. With bit 1 set to 1, a soft double error in memory can be cleared by writing new data into one or both PDP-11 memory locations of the bad 39-bit word. Note that a soft double error may be caused by the occurence of one hard error and one soft error, or two soft errors within a 39-bit word (a hard double error cannot be cleared).

Bit 2 (diagnostic check mode) allows check bits in the MOS storage array to be read via the CSR. Right after a DATI bus cycle to memory (with bit 2=1), the CSR should be read with a DATI cycle to examine the check bits retrieved from the storage array. Note that a DATO cycle to the CSR destroys the retrieved check bits but an error address recorded in the CSR is preserved.

The diagnostic check mode also provides a means of testing the error correction logic by allowing the check bit pattern in a 39-bit word to be altered via the CSR. The desired check bit pattern should be written into CSR bits 11–5 and bit 2 should be set to 1 with a DATO cycle to the CSR. A DATO cycle to memory should then be performed. Writing the appropriate check bit pattern in the storage array should cause the detection and correction of a single-bit error during a subsequent memory read cycle. (Refer to the *MS11-M Technical Manual.*)

Bits 1 and 2 in the CSR will not affect the segment of memory specified by bit 3, if bit 13 is set to 1. The system diagnostic can reside in the protected portion of memory. The diagnostic can then disable error correction and/or run the diagnostic check mode on the rest of the memory module, without itself being vulnerable to single-bit errors.

With bit 15 or 4 set to 1 and bits 14 and 2 cleared to 0, retrieve the EUB error address (A21–A11) as follows:

1. Read the CSR with a DATI bus cycle to obtain A17-A11
2. Write a logical 1 into CSR bit 14 with a DATO bus cycle
3. Read the CSR with a DATI bus cycle to obtain A21-A18.

When the memory is not in the diagnostic mode (CSR bit 2=0), data previously loaded into CSR bits 11-5 cannot be read when bit 15, 14, or 4 is a logical 1.

MS11-M MOS MEMORY
USER GUIDE
EK-MS11M-UG-001

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