APPLICATION		REVISIONS			
NEXT ASSY	USED ON	APPROVED	DATE	DESCRIPTION	REV
		Lubeck	11-3-81	RELEASE PER PCO 24174	A

INSTALLATION GUIDE

NS23M

256K BYTE MEMORY

REV																											
SHEET																											
REVISION STATUS OF SHEETS	REV	A	A	A	A	A	A	A	A	A	A																
	SHEET	1	2	3	4	5	6	7	8	9	10																

	BY PAUL LUBECK DATE 11-3-81	TITLE INSTALLATION GUIDE NS23M 256K BYTE MEMORY
	CHK	
	APPD Paul Lubeck 11-3-81	
	APPD	

National Semiconductor Corporation
2900 Semiconductor Drive, Santa Clara, Calif. 95051

SIZE	DWG NO	REV
A	409103882-001	A

SHEET 1 OF 10

4200008

APPENDIX D

NATIONAL SEMICONDUCTOR NS253M

INSTALLATION GUIDE

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TABLE OF CONTENTS

TABLES AND FIGURES

National Semiconductor Corporation
2900 Semiconductor Drive, Santa Clara, Calif. 95051

SIZE A | DWG.NO. 409103882-001 | A
SCALE _____ | SHEET 2 OF ____

4230007

CHAPTER I
INSTALLATION AND MAINTENANCE

1.1 INTRODUCTION

This section will provide the information necessary to install the NS23M, install or remove any of the options, and maintain the memory. Table 1.1 lists the configuration jumpers and a description of each, Table 1.2 lists the switches and their functions and Figure 1.1 shows the placement of the jumpers and switches.

W1*	I = 200 ns DRAM R = 150 ns DRAM
W2*	I = 150 ns DRAM R = 200 ns DRAM
W3*	I = Test Only R = Standard Configuration
W4*	I = Standard Configuration R = Test Only
W5*	I = 32K DRAM R = 16K or 64K DRAM
W6*	I = 64K DRAM R = 16K or 32K DRAM
W7*	I = 16K DRAM R = 32K or 64K DRAM
W8*	I = Test Only R = Standard Configuration
W9*	I = Standard Configuration R = Test Only
W10	I = Internal Refresh R = External Refresh
W11	I = External Refresh R = Internal Refresh
W12*	I = 16K or 64K DRAM R = 32K DRAM

Table 1.1
Jumper Definition

Table 1.1 (Continued)

W13*	I = 32K DRAM - Upper R = 16K or 32K Lower or 64K DRAM
W14*	I = 32K DRAM - Lower R = 16K, 32K Upper or 64K DRAM
W15	I = 18 Bit Address Bus R = 22 Bit Address Bus
W16	I = External Refresh to MEMSEL R = External Refresh isolated from MEMSEL
W17*	I = 150 ns DRAM R = 200 ns DRAM
W18*	I = 200 ns DRAM R = 150 ns DRAM
W19	I = +5v Battery Back-up R = +5v Standard
W20	I = +5v Standard R = +5v Battery Back-up

* Factory Configuration - Do not Alter!

DIP SWITCH 1

S1-1	Starting Address Select LSB
S1-2	Starting Address Select
S1-3	|
S1-4	|
S1-5	|
S1-6	|
S1-7	|
S1-8	|
S1-9	Starting Address Select MSB
S1-10	2K/4K I/O Space

Table 1.2
Switch Definitions

National Semiconductor Corporation 2900 Semiconductor Drive, Santa Clara, Calif. 95051	SIZE A	DWG.NO. 409103882-001	A
	SCALE	SHEET 4 OF	

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Table 1.2 (Continued)

DIP SWITCH 2

S2-1	Memory Size LSB
S2-2	Memory Size
S2-3	Memory Size
S2-4	Memory Size MSB

1.2 UNPACKING AND INSPECTION

Follow the steps listed below to unpack and inspect the NS23M memory module:

1. Remove all packing material from shipping container.

2. Remove memory board from its container.

3. Inspect the board for damage, checking for bent parts, damaged IC's, broken wires or connectors, broken switches, etc. If any damage is found, do not attempt to install the memory.

1.3 ADDRESS RANGE SELECTION

The address range is set by assigning a bus type, selecting the proper I/O space, assigning a starting address and memory size. Refer to Table 1.3 for bus type selection, Table 1.4 and 1.5 for starting address selection, Table 1.6 for I/O space selection, and Table 1.7 for memory size selection.

Bus Type	Install/ Remove
18 Bit Address Bus	Install Jumper W15
22 Bit Address Bus	Remove Jumper W15

Table 1.3 Bus Type Selection

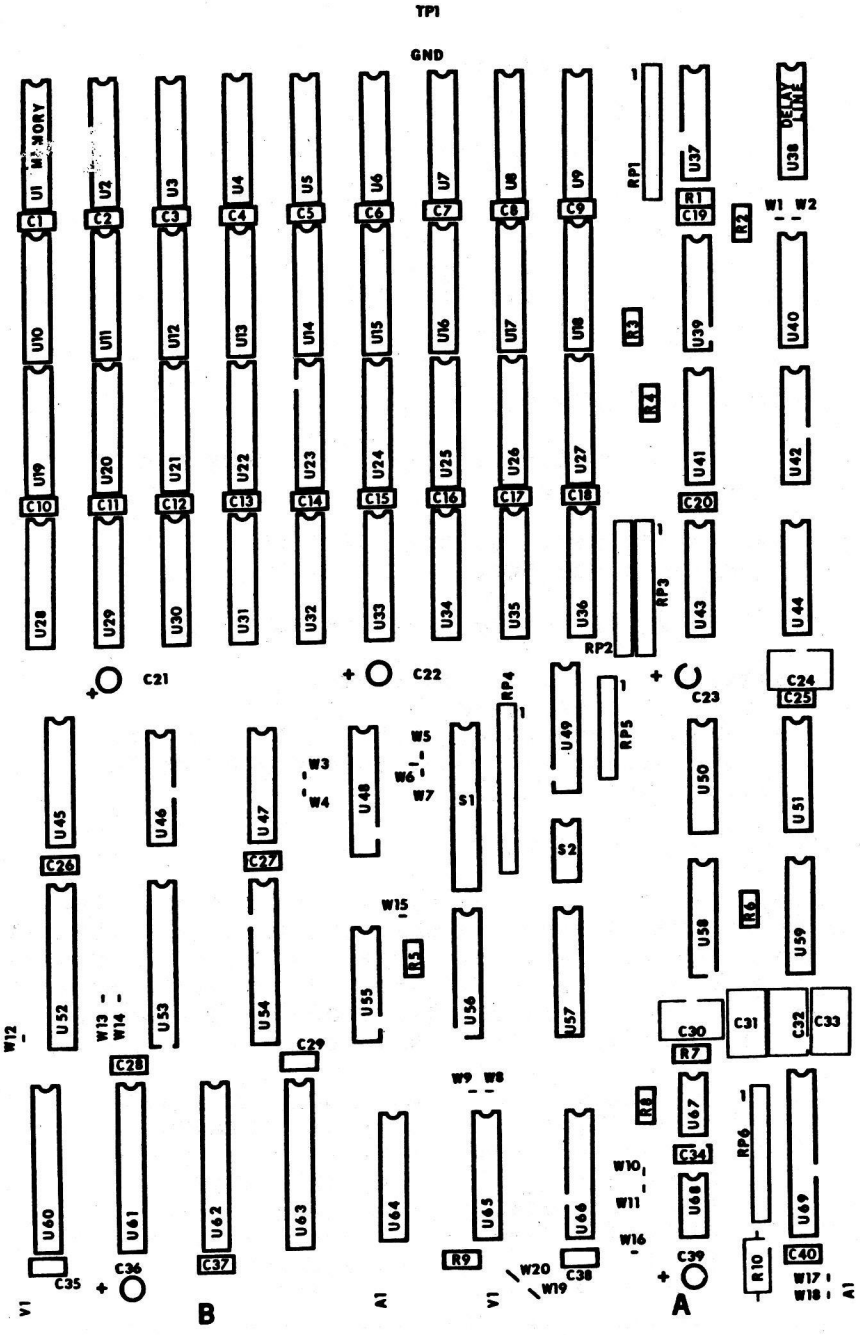

Figure 1.1 Jumper and Switch Placement

National Semiconductor Corporation 2900 Semiconductor Drive, Santa Clara, Calif. 95051	SIZE A	DWG. NO. 409103882-001	A
	SCALE _____	SHEET 6 OF _____	

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STARTING ADDRESS*	SWITCH SETTINGS** S1-5	S1-4	S1-3	S1-2	S1-1
0K	0	0	0	0	0
4K	0	0	0	0	1
8K	0	0	0	1	0
12K	0	0	0	1	1
16K	0	0	1	0	0
20K	0	0	1	0	1
24K	0	0	1	1	0
28K	0	0	1	1	1
32K	0	1	0	0	0
36K	0	1	0	0	1
40K	0	1	0	1	0
44K	0	1	0	1	1
48K	0	1	1	0	0
52K	0	1	1	0	1
56K	0	1	1	1	0
60K	0	1	1	1	1
64K	1	0	0	0	0
68K	1	0	0	0	1
72K	1	0	0	1	0
76K	1	0	0	1	1
80K	1	0	1	0	0
84K	1	0	1	0	1
88K	1	0	1	1	0
92K	1	0	1	1	1
96K	1	1	0	0	0
100K	1	1	0	0	1
104K	1	1	0	1	0
108K	1	1	0	1	1
112K	1	1	1	0	0
116K	1	1	1	0	1
120K	1	1	1	1	0
124K	1	1	1	1	1

* In 4K word increments

** 0 = Open (OFF)
1 = CLOSED (ON)

Table 1.4 - STARTING ADDRESS SELECTION

National Semiconductor Corporation
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SIZE A | DWG.NO. 409103882-001 | A

SCALE _____ | SHEET 7 OF ____

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ADDRESS RANGE	S1-9	S1-8	S1-7	S1-6
0K-128	0	0	0	0
128K-256K	0	0	0	1
256K-384K	0	0	1	0
384K-512K	0	0	1	1
512K-640K	0	1	0	0
640K-768K	0	1	0	1
768K-896K	0	1	1	0
896K-1024K	0	1	1	1
1024K-1152K	1	0	0	0
1152K-1280K	1	0	0	1
1280K-1408K	1	0	1	0
1408K-1536K	1	0	1	1
1536K-1664K	1	1	0	0
1664K-1792K	1	1	0	1
1792K-1920K	1	1	1	0
1920K-2048K	1	1	1	1

* To use addresses above 128K, 22 bit addressing must be used. In this case, the starting address will be the sum of the adddress in Table 1.5 and the lower limit of the range in Table 1.6.

** 0 = OPEN (OFF)
1 = CLOSED (ON)

Table 1.5. - ADDRESS RANGE SELECTION

I/O SPACE	S1-10
2K I/O	Close
4K I/O	Open

Table 1.6 I/O Space Selection

Memory Size*	Switch Settings S2-4	S2-3	S2-2	S2-1
8K	0	0	0	0
16K	0	0	0	1
24K	0	0	1	0
32K	0	0	1	1
40K	0	1	0	0
48K	0	1	0	1
56K	0	1	1	0
64K	0	1	1	1
72K	1	0	0	0
80K	1	0	0	1
88K	1	0	1	0
96K	1	0	1	1
104K	1	1	0	0
112K	1	1	0	1
120K	1	1	1	0
128K	1	1	1	1

0 = open
1 = closed

* In K words, K = 1024

Table 1.7 Memory Size

1.4 BATTERY BACK-UP

The NS23M has a separated power plane so that battery back-up may be used if desired. The module requires +5 volts only and has the battery back-up input at pin AVI. To implement battery back-up remove jumper W20 and install W19. W20 may originally be in etch which means it must be cut. The battery back-up must be able to supply 1A at +5 volts d.c. to the memory module.

1.5 INTERNAL/EXTERNAL REFRESH

Refresh may be supplied from either an internal or external source. If supplied from an external source, a refresh cycle will be initiated on a low to high voltage transition and may be either synchronous or asynchronous. To maintain valid data, 256 refresh cycles must be completed every 4 ms. This can be accomplished by initiating one cycle every 15 +/- 1us. Figure 1.2 shows the suggested external refresh timing.

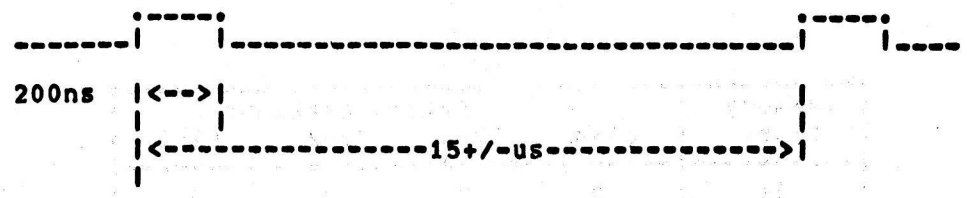


Figure 1.2 External Refresh Timing

1.6 INSTALLATION

The NS23M may be installed in any backplane wired for Q-Bus. Listed below are some guidelines:

A. Standard LSI-11 Backplanes

The NS23M Memory Card is designed to plug directly into Standard H9270 ("Quad") LSI-11 backplane/card guide assembly, and the DDV11-B ("Hex") expansion unit, the H9273-A Backplane and the H9281 backplane.

B. Precautions

In the H9270 backplane, slot one is reserved for the LSI-11 processor. The Memory Card may be inserted into any slot in this backplane with the exception of slot number one.

If the DDV11 expansion backplane is utilized, the memory card must be inserted into the A,B connectors or the C,D connectors of the backplane.

Install the card with components facing row 1, apply power and run system diagnostics. Never install or remove modules from the backplane while power is applied.

2.0 MAINTENANCE

No routine maintenance is required on the NS23M. If problems are encountered check the following:

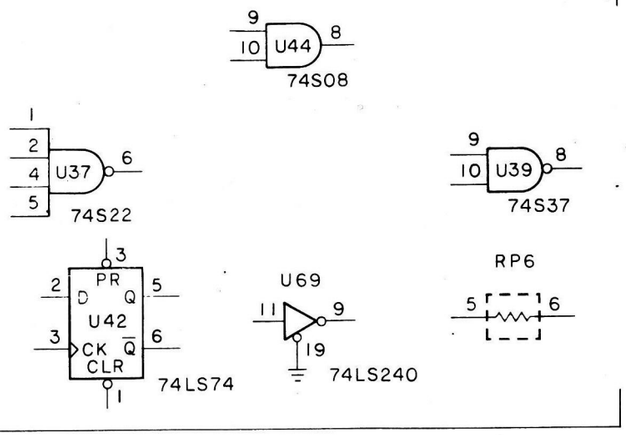
- Is the system configured properly? Is the bus priority daisy chain maintained?
- Are all switches and jumpers configured properly?
- Are the board edge contacts clean and is the board completely seated?
- Is DC power present at the backplane?

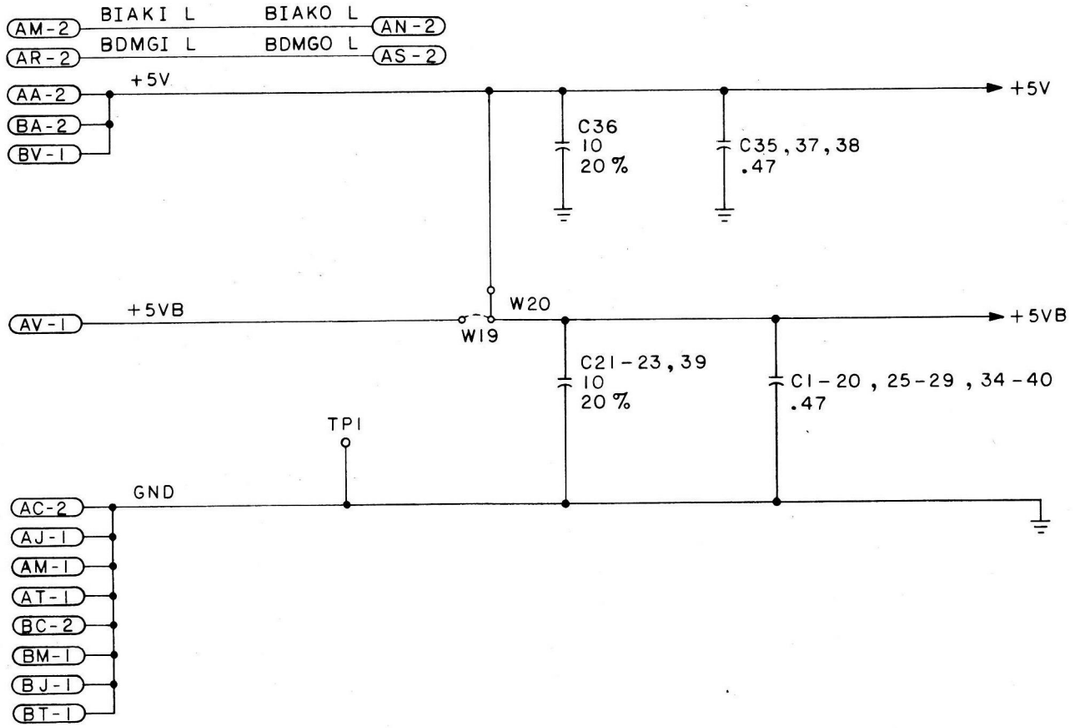
REFERENCE DESIGNATION	
LAST USED	NOT USED
C40	
R12	
RP6	
S2	
TP1	
U69	
W20	

REVISIONS			
REV	DATE	ECO NO.	APPVD
A	10-11-79	PCO 24165	
B	11-11-80	PCO 24173	
C	11-11-81	PCO 24188	
D	12-7-	PCO 24201	
E	6-3-82	PCO 24285	

VOLTAGE CHART				
TYPE	+5V	+5VB	GND	REFERENCE DESIGNATION
74LS00		14	7	U40
74S00		14	7	U47, 59
74S08		14	7	U44, 55
74S22		14	7	U37
74S32		14	7	U43
74S37		14	7	U39, 41
74S74		14	7	U58
74S132		14	7	U51
74S135		16	8	U45
74S175		16	8	U48
74LS240		20	10	U69
74S260		14	7	U50
74S283		16	8	U49, 56, 57
74S373		20	10	U52, 53, 54
74S393		14	7	U46
75452B		8	4	U68
2908	20		5,16	U60, 61, 62, 63
8641	16		8	U64, 65, 66
LM555		8	1	U67
DELAY LINE, 200NS			1,14	U38
74LS74		14	7	U42

SPARE GATES





NOTES UNLESS OTHERWISE SPECIFIED:

1. RESISTANCE VALUES ARE IN OHMS, 1/8W, 5%.
2. CAPACITANCE VALUES ARE IN MICROFARADS, 25V. $^{+80}_{-20}$ %.
3. □ INDICATES +5V ONLY.
4. ALL RESISTOR PACKS (RP) ARE 22 OHMS.

MATERIAL		DR BY W. Yaba	6-3-81
		CHK BY	
FINISH		ME	
		EE	
		PE	
TOLERANCE: ANG. — 2 PL — 3 PL —		UNLESS OTHER SPECIFIED: DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES. REMOVE BURRS AND SHARP EDGES BREAK SHARP CORNERS .015 MAX	
NEXT ASSY	USED ON		

National Semiconductor Corporation
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SCHEMATIC DIAGRAM
NS23M

SIZE D | DR NO 870103882 001

SCALE NONE | SHEET 1 OF 5

REVISIONS			
REV	DATE	ECO NO	APPVD
		SEE SHEET 1	

AP-2 BBS7 L
AJ-2 BSYNC L
BA-1 BDCOK H
AK-2 BWTBT L
U65 8641 BUS4 BUS1 BUS3 BUS2 OUT4 IN4 OUT1 IN1 OUT3 IN3 OUT2 IN2 DIS A DIS B
U50 74S260
U37 74S22
U51 74S132
U39 74LS00
R1 2.7K
R2 3.9K
R3 27
C24 47PF 500V 5%
+5VB
BS7 A SH 4
+SYNC B SH 3,4
-BE C SH 3,4
U37 74S22
U41 74S37
U38 140 160 IN 200 20 120 60 180
U69 74LS240 W18 W17
U68 75452
R10 470
R11 330
R12 100
C31 47PF
DRCP D SH 3
U44 74S08
W2 W1
SH 4 AD -SEL
U58 74S74 PR D Q CLR
U43 74S32
U42 74LS74
U39
RP1 -CAS E SH 5
REFH F SH 3
U69 74LS240
RP6 100
C33 220PF 500V 5%
C32 220PF 500V 5%
R6 1K
R8 27K
R7 68K
C30 100PF 500V 5%
C34 .1
U67 LM555 DSC THR TRG CV R OUT
W10 W11
W16
AR-1 EXT REFH/MEMSEL
R9 1K
+5V
SH 4 AF LA Ø
U40 74LS00
U41 74S37
RP4
RP6
U59 74S00
U69 74LS240
U68 75452
-RAS Ø H SH 5
-RAS 1 J SH 5
R4 15
-RON K SH 3
-RAON L SH 3
-CAON M SH 3
-WE BØ N SH 5
-WE B1 P SH 5
BRPLY L AF-2
PU R SH 3,4
SH 4 AB DOUT
SH 4 AC DIN
SH 4 AE +RSEL

SIZE	DR NO	
D	870103882	001
SCALE NONE	SHEET 2 OF 5	

REVISIONS			
REV	DATE	ECO NO	APPVD
		SEE SHEET 1	

SH 2 R PU
SH 5 AK DFM PØ
SH 5 AJ DFM P1
SH 4 AB DOUT
SH 2 C -BE
SH 2 D DRCP
SH 5 AH D ØØ-D 15
SH 4 AL DAL 16

(AU-2) BDAL ØØ
(AV-2) BDAL 01
(BE-2) BDAL Ø2
(BF-2) BDAL Ø3
(BH-2) BDAL Ø4
(BJ-2) BDAL Ø5
(BK-2) BDAL Ø6
(BL-2) BDAL Ø7
(BM-2) BDAL Ø8
(BN-2) BDAL Ø9
(BP-2) BDAL 1Ø
(BR-2) BDAL 11
(BS-2) BDAL 12
(BT-2) BDAL 13
(BU-2) BDAL 14
(BV-2) BDAL 15

SH 2 K -RON
SH 2 F REFH
SH 2 B +SYNC
SH 2 L -RAON
SH 2 M -CAON

U63, U62, U61, U60 — 2908 — DRCP BE RLE OE — A3 BUS3 A2 BUS2 A1 BUS1 AØ BUSØ — R3 R2 R1 RØ — ODD
D ØØ D Ø1 D Ø2 D Ø3 D Ø4 D Ø5 D Ø6 D Ø7 D Ø8 D Ø9 D 1Ø D 11 D 12 D 13 D 14 D 15

DAL ØØ DAL Ø1 DAL Ø2 DAL Ø3 DAL Ø4 DAL Ø5 DAL Ø6 DAL Ø7 DAL Ø8 DAL Ø9 DAL 1Ø DAL 11 DAL 12 DAL 13 DAL 14 DAL 15

U47 74S00 — U45 74S135 — U46 74LS393 — U53, U54, U52 74S373 — OC G D Q

W9 W8 W4 W3 W12 W13 W14

D 17 S SH 4
D 16 T SH 4
DTM PØ U SH 5
DTM P1 V SH 5
DAL ØØ X SH 4
ATM Ø – ATM 7 Y SH 5
DAL ØØ – DAL 15 Z SH 5
DAL 13 – DAL 15 AA SH 4
DAL 12 W SH 4

RP2 4 ATM Ø
RP3 7 ATM 1
RP3 6 ATM 2
RP3 2 ATM 3
RP3 4 ATM 4
RP2 6 ATM 5
RP2 2 ATM 6
RP2 7 ATM 7

SIZE	DR NO	
D	870103882	001
SCALE NONE	SHEET 3 OF 5	

REVISIONS			
REV	DATE	ECO NO.	APPVD
		SEE SHEET 1	

SH 3 AA DAL 13-DAL 15

DAL 13
DAL 14
DAL 15

+5VB RP4 1K S1 74S32 U43

SH 2 C -BE

DIS A DIS B
BUS1 BUS2 BUS4 BUS3 U66 8641
OUT1 IN1 OUT2 IN2 OUT4 IN4 OUT3 IN3

AC-1 BDAL 16
AD-1 BDAL 17
AE-2 BDIN L
AH-2 BDOUT L

DAL 16
DAL 17
DOUT
DIN

SH 3 S D 17
SH 3 T D 16

U57 74S283 (C0, A1 B1 A2 B2 A3 B3 A4 B4, Σ1 Σ2 Σ3 Σ4, C4)

4 NA 14
1 NA 15
13 NA 16
10 NA 17

S2 RP5 1K +5VB

U49 74S283

DOUT SH 2,3 (AB)
DIN SH 2 (AC)
DAL 16 SH 3 (AL)

+ = > MAXIMUM ADDRESS

BC-1 BDAL 18
BD-1 BDAL 19
BE-1 BDAL 20
BF-1 BDAL 21

U64 8641 U55 74S08

DAL 18
DAL 19
DAL 20
DAL 21

U56 74S283

4 NA 18
1 NA 19
13 NA 20
10 NA 21

74S32 U43 74S260 U50 74S00 U47

-SEL SH 2 (AD)

+ = > MINIMUM ADDRESS

+5VB R5 1K W15

SH 3 W DAL 12
SH 2 A BS7
SH 2 B +SYNC
SH 2 R PU
SH 3 X DAL ØØ

S1 RP5 1K 74S08 U44

U48 74S175 (CLR CLK, 3D 4D 2D 1D, 3Q 3Q̄ 4Q 4Q̄ 2Q 2Q̄ 1Q 1Q̄)

16K 32K W5 W7 W6 64K

+RSEL SH 2 (AE)
LA Ø SH 2 (AF)

SIZE	DR NO	
D	870103882	001
SCALE NONE	SHEET 4 OF 5	

REVISIONS			
REV	DATE	ECO NO	APPVD
		SEE SHEET 1	

SH 3 Z DAL ØØ - DAL 15

SH 3 V DTM P1

SH 3 U DTM PØ

SH 2 N -WE BØ

SH 2 P -WE B1

SH 2 H -RAS Ø

SH 2 E -CAS

SH 2 J -RAS 1

SH 3 Y ATM Ø - ATM 7

ATM Ø	4	5
ATM 1	7	6
ATM 2	12	11
ATM 3	10	13
ATM 4	9	15
ATM 5	5	7
ATM 6	6	12
ATM 7	11	10
	13	9
	15	4

DAL Ø1 DAL Ø3 DAL Ø5 DAL Ø7 DAL Ø9 DAL 11 DAL 13 DAL 15 DAL ØØ DAL Ø2 DAL Ø4 DAL Ø6 DAL Ø8 DAL 1Ø DAL 12 DAL 14

U1 U2 U3 U4 U5 U6 U7 U8 U9 U10 U11 U12 U13 U14 U15 U16 U17 U18

U19 U20 U21 U22 U23 U24 U25 U26 U27 U28 U29 U30 U31 U32 U33 U34 U35 U36

D Ø1 D Ø3 D Ø5 D Ø7 D Ø9 D 11 D 13 D 15 D ØØ D Ø2 D Ø4 D Ø6 D Ø8 D 1Ø D 12 D 14

D ØØ - D 15 AH SH 3

DFM P1 AJ SH 3

DFM PØ AK SH 3

64K RAM TYP X36

NC	1	16	GND
DI	2	15	-CAS
-WE	3	14	DO
-RAS	4	13	A 6
A Ø	5	12	A 3
A 2	6	11	A 4
A 1	7	10	A 5
(+5V) V_{CC}	8	9	A 7

SIZE	DR NO	
D	870103882	001
SCALE NONE	SHEET 5 OF 5	