EK-780EH-RM-001

MS780-E/F and MS780-H/J Memory Options Maintenance Advisory

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CHAPTER 1
INTRODUCTION

1.1 DESCRIPTION

The MS780-E/F and MS780-H/J are new memory options for the VAX-11/780 or VAX-11/785. The MS780-E/F uses 64K MOS RAM chips to increase the amount of memory available on a single array module to one megabyte. The MS780-H/J uses 256K MOS RAM chips to increase the amount of memory available on a single array module to four megabytes. The MS780-E/H replaces the MS780-C memory and is made up of an SBI interface and two memory controllers, each of which can access up to eight arrays. A single backplane can accommodate 16 arrays, and the memory can be expanded to two full MS780-E/H assemblies. An assembly or memory subsystem consists of a backplane, an SBI interface board (M8376), two controllers (M8375), and an even number of M8373 array boards for the MS780-E or M8374 array boards for the MS780-H.

The memory is internally interleaved (normal) when there are two controllers in the MS780-E/H assembly. It is noninterleaved when there is only one controller. When internally interleaved, the assembly is expanded in two-megabyte (MS780-E) or eight-megabyte (MS780-H) increments. A single megabyte in the MS780-E or four megabytes in the MS780-H can be added only when the memory is noninterleaved and there is only one controller in the assembly.

External interleaving is possible with a memory of the same type and size, and when both memories have only one controller. External interleaving is software controlled; the other forms of interleaving are hardware controlled. The MS780-E or MS780-H cannot be interleaved with an MS780-C memory.

More than one type of memory can be on a system; however, mixed types cannot be interleaved with one another. Each type must have separate address spaces.

The MS780-F refers to array expansion of the MS780-E, and MS780-J refers to array expansion of the MS780-H.

1.2 FEATURES

1.2.1 MS780-E Memory Option

1. Memory Type: 64K MOS N channel RAM.
2. Memory size:
   a. One megabytes per array
   b. Up to 16 arrays per MS780-E assembly
   c. Up to two MS780-E assemblies per CPU (VMS now supports only two)
3. Error correction (ECC):
   a. Single-bit error correction
   b. Double-bit error detection
4. Memory configurations:

a.	MS780-EA	4-Mbyte system expansion, controllers, and power
b.	MS780-EB	240 V, 50 Hz version of MS780-EA
c.	MS780-EC	2-Mbyte system expansion, controllers, and power
d.	MS780-ED	240 V, 50 Hz version of MS780-EC
e.	MS780-FA	2-Mbyte expansion
f.	MS780-FB	4-Mbyte expansion
g.	MS780-FC	6-Mbyte expansion
h.	MS780-FD	1-Mbyte expansion
i.	MS780-FF	10-Mbyte expansion

1.2.2 MS78Ø-H Memory Option

1. Memory Type: 256K MOS N channel RAM.
2. Memory size:
   a. Four megabytes per array
   b. Up to 16 arrays per MS78Ø-H assembly
   c. Up to two MS78Ø-H assemblies per CPU (VMS now supports only two)
3. Error correction (ECC):
   a. Single-bit error correction
   b. Double-bit error detection
4. Memory configurations:

a.	MS78Ø-HA	16-Mbyte system expansion, controllers, and power
b.	MS78Ø-HB	24Ø V, 5Ø Hz version of MS78Ø-HA
c.	MS78Ø-HC	8-Mbyte system expansion, controllers, and power
d.	MS78Ø-HD	24Ø V, 5Ø Hz version of MS78Ø-HC
e.	MS78Ø-JA	8-Mbyte expansion
f.	MS78Ø-JB	16-Mbyte expansion
g.	MS78Ø-JC	32-Mbyte expansion
h.	MS78Ø-JD	4-Mbyte expansion
i.	MS78Ø-JF	4Ø-Mbyte expansion

1.3 PHYSICAL TOPOLOGY

1. Board locations (refer to Figure 1-1).
2. MS780-E/H assembly location (refer to Figure 1-2).
3. Power connections (refer to Figure 1-3).

ARRAY NUMBER		MODULE UTILIZATION MS780 E/F, H/J		
7	20	M8373/M8374	1MB/4MB	*
6	19	M8373/M8374	1MB/4MB	*
5	18	M8373/M8374	1MB/4MB	*
4	17	M8373/M8374	1MB/4MB	*
3	16	M8373/M8374	1MB/4MB	*
2	15	M8373/M8374	1MB/4MB	*
1	14	M8373/M8374	1MB/4MB	*
0	13	M8373/M8374	1MB/4MB	
	12	M8375	UPPER CONTROLLER	
	11	M8376	SBI INTERFACE	
	10	M8375	LOWER CONTROLLER	
0	9	M8373/M8374	1MB/4MB	
1	8	M8373/M8374	1MB/4MB	*
2	7	M8373/M8374	1MB/4MB	*
3	6	M8373/M8374	1MB/4MB	*
4	5	M8373/M8374	1MB/4MB	*
5	4	M8373/M8374	1MB/4MB	*
6	3	M8373/M8374	1MB/4MB	*
7	2	M8373/M8374	1MB/4MB	*
	1	M9040	SBI TERMINATOR	*

* OPTIONAL IF NOT INSTALLED
USE BLANK MODULE 7014103

PART NO. 3614746-01

MKV84-2600

Figure 1-1 Module Location Diagram

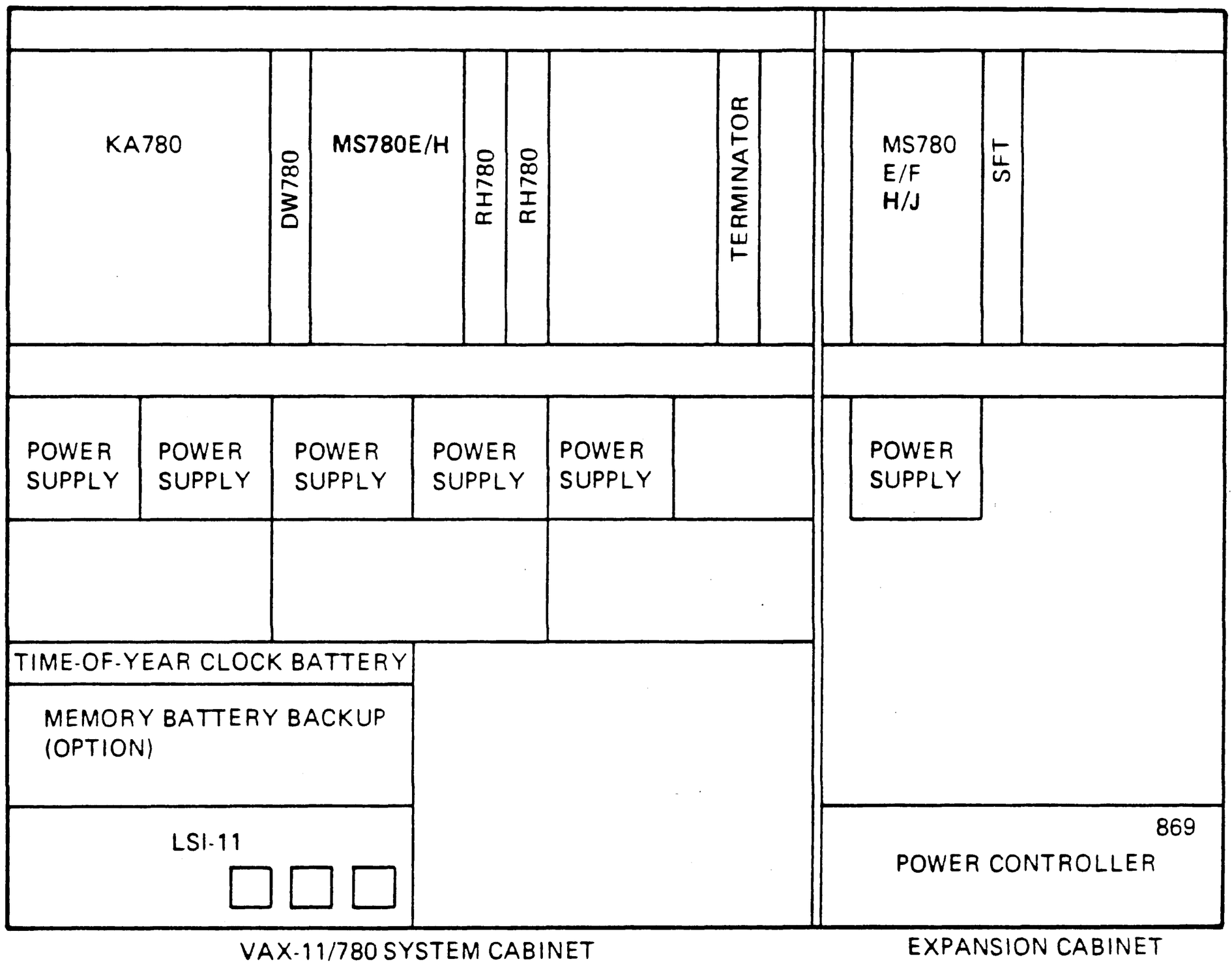

Figure 1-2 MS780-E/H Assembly Locations

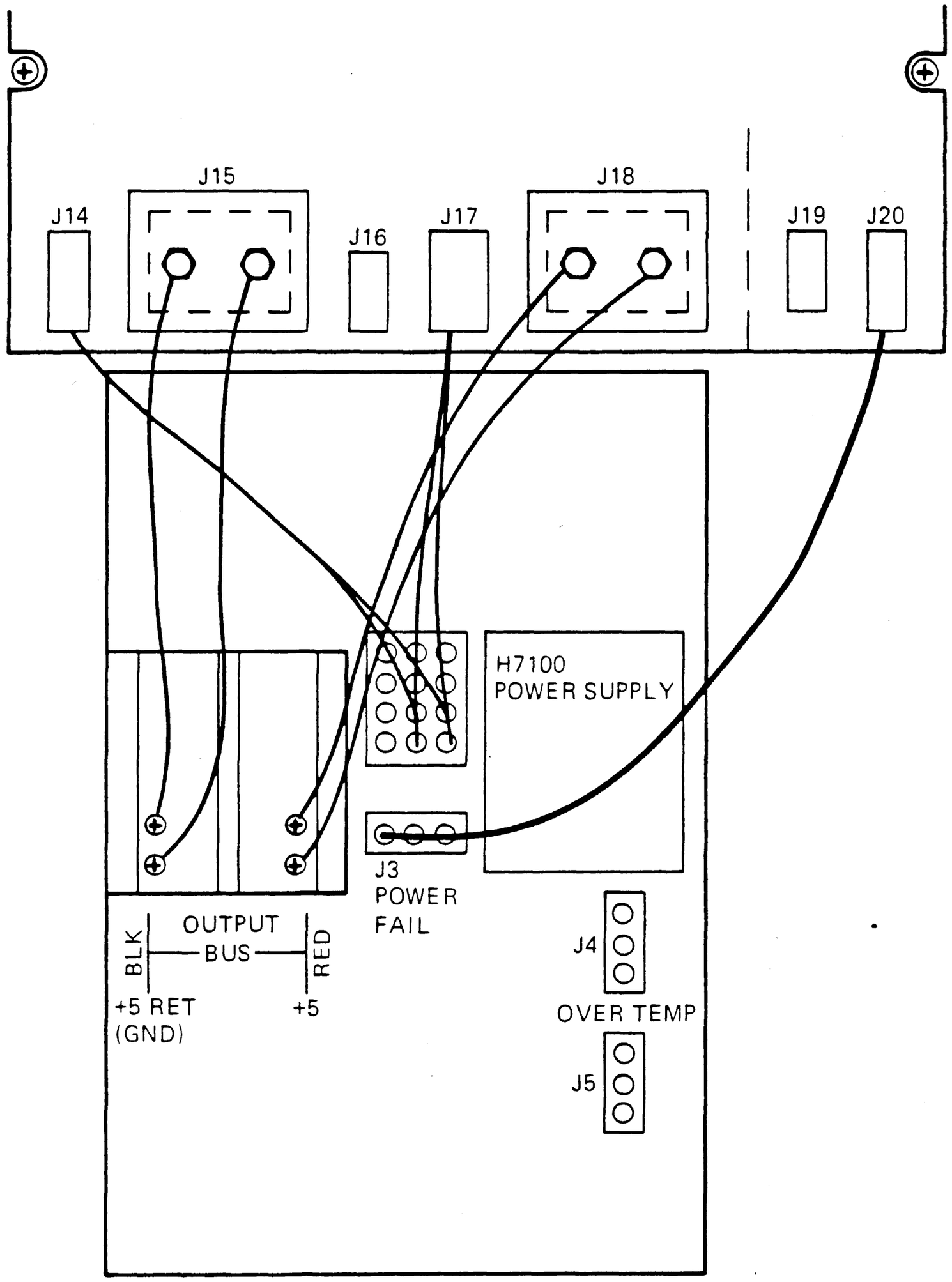

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Figure 1-3 Power Connections

1.4 MODULES

1. SBI interface (M8376) -- One SBI interface board per assembly. This board handles the interactions between the SBI and the memory. It contains:

   a. Decode logic

   b. Two configuration registers (A and B)

   c. Data latches (registers E and F)

   d. Arbitration logic

   e. Control logic

   f. DBUS (data) from the SBI interface to the memory controller

   g. ABUS (address) from SBI interface to memory controller

2. Memory controllers (M8275) -- There are two memory controllers per assembly, each of which can access up to eight memory arrays. Each controller contains:

   a. Input/output buffer data latches

   b. Command/address buffer latches

   c. ECC logic

   d. Two configurations registers (C and D)

   e. Refresh and initialization logic

   f. Controller microsequencer

   g. DBUS (data) from the memory controller to the SBI interface

   h. MBUS (data) from the memory controller to memory arrays

   i. ABUS (address) continuation to memory arrays

CAUTION

DO NOT place a controller module (M8375) in slot 11, the location for the SBI interface module. If this is done, -5V will be applied to a chip on the controller module and may short out the chip.

3. MS78Ø-E Array modules (M8373) -- Each array module is arranged in a matrix of 256K address bits by 39 data bits to produce a one-megabyte array using 64K RAMs. The 39 bits are made up of a 32-bit longword and 7 ECC bits. Logic on the array module consists of:

   a. Address MUX

   b. Input data buffers

   c. Output data MUX

   d. MBUS (data) from array to memory controller

4. MS78Ø-H Array modules (M8374) -- Each array module is arranged in a matrix of one megabyte address bits by 39 data bits to produce a four-megabyte array using 256K RAMs. The 39 bits are made up of a 32-bit longword and 7 ECC bits. Logic on the array module consists of:

   a. Address MUX

   b. Input data buffers

   c. Output data MUX

   d. MBUS (data) from array to memory controller

1.5 MISCONFIGURATION LED

There is an LED on the SBI interface module that lights if there is a misconfiguration. The LED lights when any of the following conditions are met:

1. The number of arrays to which each of the two controllers have access is not the same. For example, if the lower controller has access to four megabytes, the upper controller must also have access to four megabytes.
2. The arrays are not in consecutive slots.
3. The arrays have different RAM types.

1.6 SOFTWARE REQUIREMENTS

1. VMS Version 3.2 or higher for the MS78Ø-E and 4.Ø or higher for the MS78Ø-H.

2. VMB.EXE Version 3 or higher (shipped with VMS Version 3.Ø (33 blocks)).

1.7 MAINTENANCE PHILOSOPHY

The MS78Ø-E/H maintenance philosophy is the same as that for the VAX-11/78Ø itself, which is module replacement. The microdiagnostic should provide problem isolation to the board level.

Should a memory controller failure occur, the MS78Ø-E/H is capable of running in a degraded mode with one controller and its arrays.

Because the memory detects and corrects single-bit errors, array modules with such errors should not be replaced until a double-bit error occurs.

1.8 THROUGHPUT AND ACCESS TIMES

Table 1-1 lists the access times and throughput for the memory system for each command type.

A distinction is made between Byte Writes and Full Writes (for both longword and quadword Writes); they involve different procedures at the memory controller level and below, and therefore have different cycle lengths.

In addition, Read accesses that result in single-bit errors are followed by a correction routine that extends their access and cycle times. Categories of Read cycles with correctable errors are included in the table.

Access time is defined from the SBI point of view. It is the interval (in increments of 2ØØ-ns SBI cycles) from the command/address beginning transmission on the SBI (bus TØ time) to the time that requested data is enabled onto the bus (also TØ).

Cycle time is the interval between commands of the same type, repeated at the maximum rate the memory system can sustain without returning a BUSY to any requester. In interleaved modes, it is assumed that the command stream accesses both controllers with approximately equal probability, with no more than three consecutive commands to the same controller. This takes full advantage of the system's interleave capability.

Table 1-1 Access and Cycle Times (in SBI Cycles)

Command	No Error	Single Error		Single Error in Each Read
		1st Word	2nd Word	
Longword Read				
Access	3	4	-	
Cycle (Interleaved)	2*	2.5	-	
Cycle (Noninterleaved)	2	5	-	
Extended Read				
Access	3,4	4,5	3,5	4,6
Cycle (Interleaved)	3*	3.5	3	4
Cycle (Noninterleaved)	3*	7	6	8
Longword Write (Byte)				
Access	-	-	-	
Cycle (Interleaved)	2*	2.5	-	
Cycle (Noninterleaved)	4	5	-	
Longword Write (Full)				
Access	-	-	-	
Cycle (Interleaved)	2*	-	-	
Cycle (Noninterleaved)	3	-	-	
Extended Write (Byte)				
Access	-	-	-	5
Cycle (Interleaved)	3*	3.5	3.5	4
Cycle (Noninterleaved)	6	7	7	8
Extended Write (Full)				
Access	-	-	-	
Cycle (Interleaved)	3*	-	-	
Cycle (Noninterleaved)	4	-	-	

* SBI-limited. At these cycle times, memory throughput is limited to the maximum rate the SBI can sustain.

CHAPTER 2
MEMORY ADDRESS SPACE

The 28-bit SBI address field defines 268,435,456 longword addresses, which are divided into two sections by the most significant bit. The lower half is reserved for memory and the upper half is reserved for I/O space. For memory alone, this represents over 134 million longwords, or 512 Mbytes.

The user has access to the physical address space by using the 30-bit byte address space available at the console. Since NEXUS addresses are longword addresses, the system converts the physical byte address (30-bit) to the SBI longword address (28-bit).

From the console, addresses from 00000000 to 1FFFFFFF are legal physical addresses to memory. Addresses from 20000000 up are I/O space.

For information on the relationship between the physical byte address and the SBI longword address, see Chapter 16, Synchronous Backplane Interconnect, in the VAX Hardware Handbook (EB-17281).

CHAPTER 3
CONFIGURATION REGISTERS

The MS780-E/H memory uses six addressable registers (refer to Figure 3-1). They are addressed by six consecutive longword addresses (hex console addresses) beginning at:

1. 20002000 if the memory is backplane-jumpered to TR1.
2. 20004000 if the memory is backplane-jumpered to TR2.
3. 20006000 if the memory is backplane-jumpered to TR3.
4. 20008000 if the memory is backplane-jumpered to TR4.

Register A is located on the SBI interface board (M8376). Its primary function is fault and status information. It also reports memory size, RAM type, and interleave mode.

Register B is partially on the interface and partly on the controller boards. The upper half, on the interface, stores the starting address of the system and is on battery-backup, so a warm start should not require rewriting. The lower half is duplicated on each controller. Writing the bits in the lower half of the register causes the bits to be written on both controllers.

Register C, on the lower controller (0), and Register D, on the upper controller (1), are identical in bit assignments and are for ECC status and diagnostics.

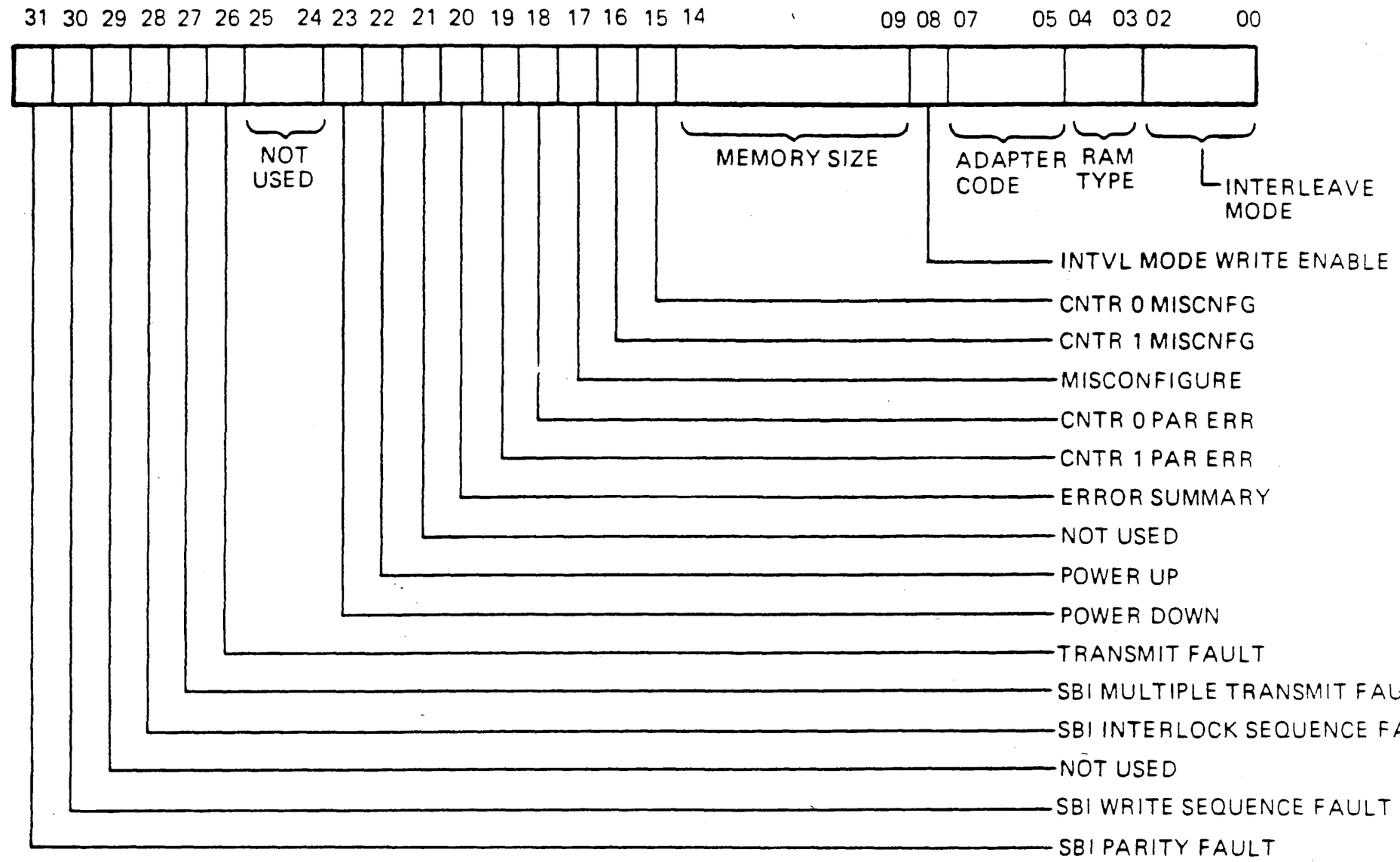
Registers E and F are two longword data latches on the SBI interface which store, respectively, the lower and upper longword of a quadword write data. These two registers can be written to and read from to verify SBI transfers.

The following is a list of the registers and their addresses, assuming that the TR level of the MS780-E is 1.

Register	Address
A	20002000
B	20002004
C	20002008
D	2000200C
E	20002010, 20002018, 2000201C
F	20002014

not used they are spare

REGISTER A 2000X000



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REGISTER B 2000X004

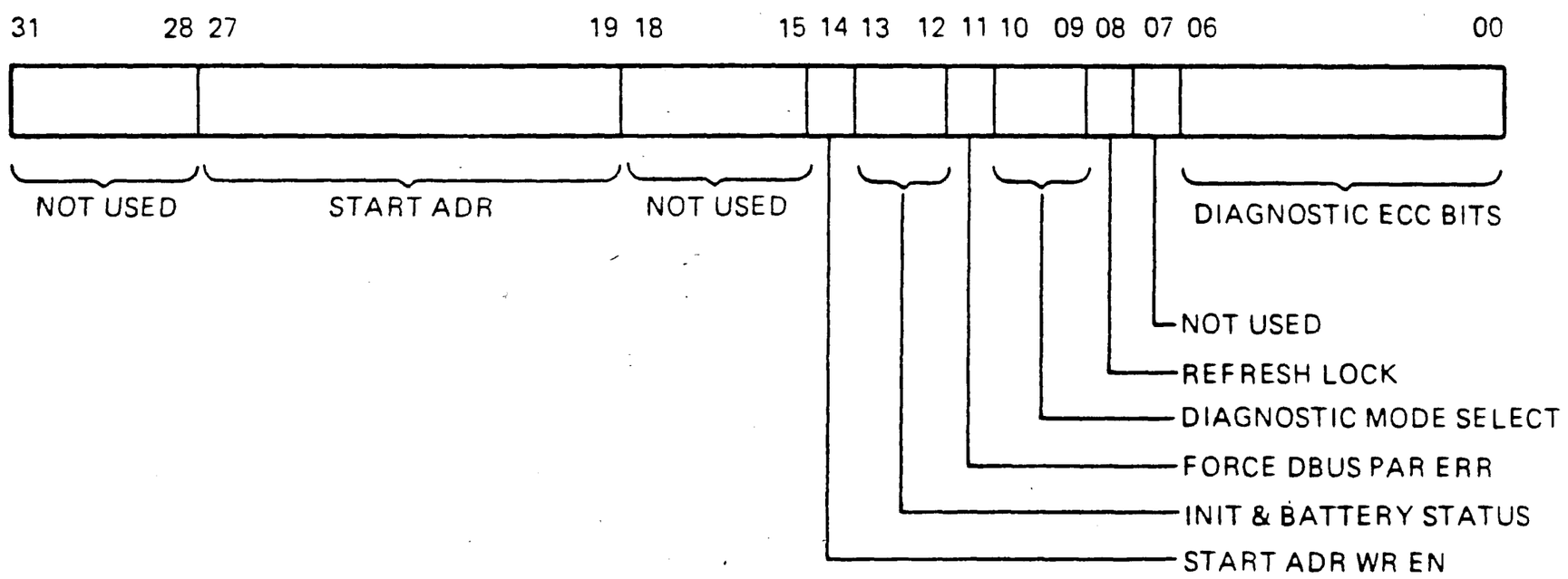

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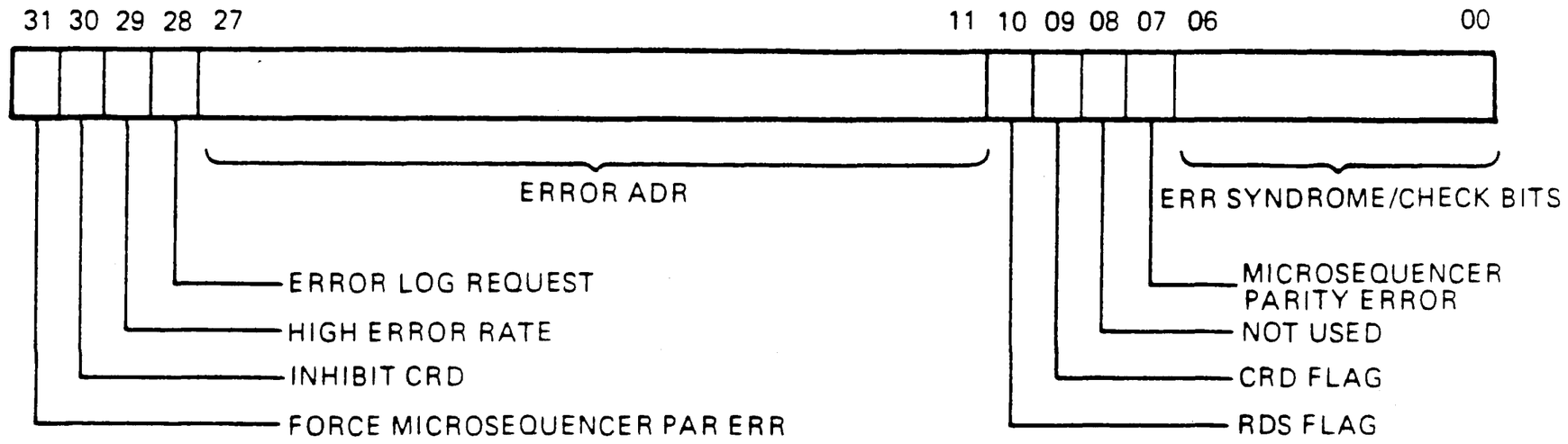
Figure 3-1 Configuration Registers (Sheet 1 of 2)

On Error Log:— { C = Lower arrays.
D = UPPER arrays.

REGISTERS C AND D 2000X008 AND 2000X00C



REGISTERS E AND F 2000X010 AND 2000X014

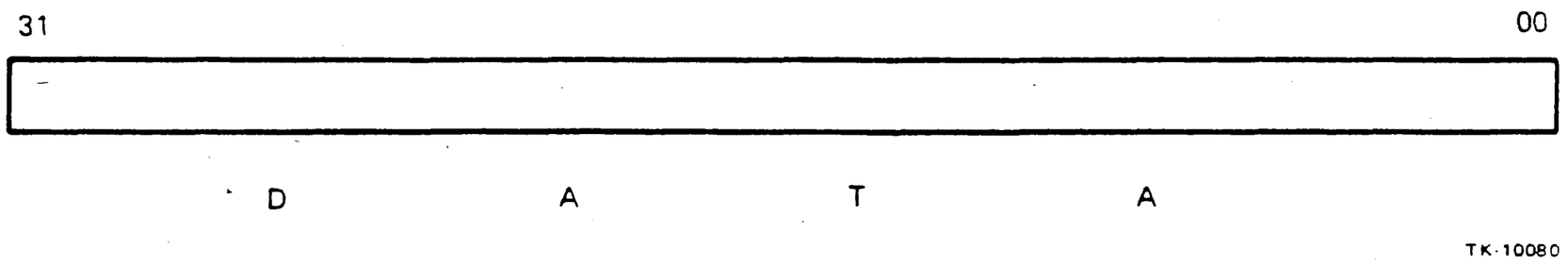


Figure 3-1 Configuration Registers (Sheet 2 of 2)

3.1 REGISTER A

Same as M-5780-C.

Table 3-1 lists the bit functions and their meanings.

Table 3-1 Register A Bit Functions

Bits	Function	Description/Interpretation When Set
31	SBI Parity Fault	An SBI information path parity error has occurred. Read-only.
30	SBI Write Sequence Fault	Failure of a Write command to be followed immediately by a Write Data Format command. Read-only.
29	(not used)	Reads as zero.
28	SBI Interlock Sequence Fault	An Interlock Write command was not preceded by an Interlock Read command. Read-only.
27	SBI Multiple Transmit Fault	Received ID is not the same as the sent ID. Read-only.
26	Transmit Fault	Memory was the transmitter when the error occurred. Read-only.
25,24	(not used)	Read as zeros.
23	Power Down	A power-down sequence is underway. Clear when bit 22 is set. Read/write 1 to clear.
22	Power Up	A power-up sequence is underway. Clear when bit 23 is set. Read/write 1 to clear.
21	(not used)	Reads as zero.
20	Error Summary	Set if any of the following are set: 1. Internal parity errors (Reg. A bits 19, 18; Reg. C bit 7). 2. Misconfigure warning (Reg. A bits 17, 16, 15). 3. Error log request (Reg. C bit 28). Cleared only when all the above bits are clear.

Table 3-1 Register A Bit Functions (Cont)

Bits	Function	Description/Interpretation When Set
19	CNTR 1 PAR ERR	Read data from the upper controller to interface had parity error. Bad data is sent on SBI with corrected parity and RDS tag (double-bit errors). Read/write 1 to clear.
18	CNTR Ø PAR ERR	Same as bit 19 but for the lower controller.
17	Misconfigure	In internally interleaved mode, set by an unequal number of arrays with each controller.
16	CNTR 1 MISCNFG	Misconfiguration in upper controller memory. Illegal array arrangement (no arrays or no controller). Read-only.
15	CNTR Ø MISCNFG	Same as bit 16 but for the lower controller.
14:9	Memory Size	Memory system capacity from 1 megabyte (ØØØØØØ) to 64 megabytes (111111). Capacity is a function of RAM size, interleave mode, and the number of array boards. Count is binary.
8	Interleave Mode Write Enable	When set, permits write to bits <2:Ø> which establish interleave mode. Write-only. Reads as Ø.
7:5	Adapter Code	Fixed set of bits identifying the MS78Ø-E subsystem. Bits 7:5 read as Ø11. Read-only.
4:3	RAM Type	Identifies sizes of RAMs on arrays.
	Bits 4 3	
	Ø Ø	Misconfigured; no array boards in backplane.
	Ø 1	64K RAMs (1-Mbyte arrays).
	1 Ø	256K RAMs (4-Mbyte arrays) (future).
	1 1	Misconfigured; both array types in backplane.

Table 3-1 Register A Bit Functions (Cont)

Bits	Function	Description/Interpretation When Set
2:Ø	Interleave	Mode indicated according to the following:
	Bits 2 1 Ø	
	Ø Ø Ø	Noninterleaved lower controller (hardware).
	Ø 1 Ø	Noninterleaved upper controller (hardware).
	Ø Ø 1	External interleaved lower controller (software).
	Ø 1 1	External interleaved upper controller (software).
	1 Ø Ø	Internal two-way interleaved (hardware).

Upon power-up, these bits are set according to the hardware configuration appropriate to the number and position of memory controllers present. Bits are read/write (write-only if bit Ø8 is set). If there are two MS78Ø-Es, bit ØØ must be set by the software for external interleaving. Bits Ø1 and Ø2 must not be changed; if they are changed, a misconfiguration error will result.

3.2 REGISTER B

Same as MS780-C

Table 3-2 lists the bit functions and their meanings.

Table 3-2 Register B Bit Functions

Bits	Function	Description/Interpretation When Set
31:28	(not used)	Read as zeros.
27:19	START ADDR	Specifies the memory system starting address in 1-Mbyte increments. VMS software controlled. Read/write. Write when bit 14 is set.
18:15	(not used)	Read as zeros.
14	START ADR WR EN	Enables writing to bits 27:19. Write-only.

Starting address of this memory

Table 3-2 Register B Bit Functions (Cont)

Bits	Function	Description/Interpretation When Set
13:12	INIT and Battery Status	Indicates if memory is coming up from a cold start and is initializing the memory, or if valid data is preserved in the memory arrays.
	Bits 13 12	
	Ø Ø	Initialization in progress (memory written with zeros and BUSY to any SBI commands).
	Ø 1	Memory contains valid data.
	1 Ø	Invalid combination.
	1 1	Initialization completed, no valid data in memory.
11	Force DBUS PAR ERR	When set, Read Data from the controllers to the SBI interface has an error and a Read Data Substitute is forced. Register access is unaffected. Read/write.
1Ø:9	Diagnostic Mode Select	There are three diagnostic modes that exercise various controller functions and four data paths and their latches. Read/write.
	Bits 1Ø 9	
	Ø Ø	Normal operation.
	Ø 1	Diag. Mode 1 -- Verifies check bit generation logic and controller data path.
	1 Ø	Diag. Mode 2 -- Verifies ECC logic.
	1 1	Diag. Mode 3 -- Verifies check bit MOS RAMs.
8	Refresh Lock	Controller cannot execute read/write cycles when set.
7	(not used)	Reads as zero.
6:Ø	Diagnostic ECC Bits	Loaded with substitute ECC bits in conjunction with diagnostic modes.

3.3 REGISTERS C AND D

These registers are the same. Register C is on the lower controller (slot 1Ø) and Register D is on the upper controller (slot 12). The function of these registers is primarily for error logging.

Table 3-3 lists the bit functions and their meanings.

Table 3-3 Registers C and D Bit Functions

Bit	Function	Description/Interpretation When Set
31	Force Microsequencer PAR ERR	Causes the wrong parity across the 56 PROM bits of the microsequencer data field. Sets bit 7. Read/write.
3Ø	Inhibit CRD	Prevents single-bit errors from sending CRD with read data on the SBI. Error log requests (bit 28) and CRD error (bit 9) are still set by a single-bit error.
29	High Error Rate	Indicates a second error has been detected before the first was serviced and cleared.
28	Error Log Request	Notification of an error on a memory read. Details of the error are logged in other bits.
27:11	Error ADR	Memory address to the page level of the error. Valid only if bit 28 is set. Read-only.
	Bits: 27	Controller Select
	26:24	Array Select
	23:22	Array Bank Select
	21:11	RAM Page Address (256K RAMs) (future)
	or 19:11	RAM Page Address (64K RAMs)
1Ø	RDS Flag	Multiple-bit error detected. Read/write 1 to clear.
9	CRD Flag	Single-bit error detected and corrected. Read/write 1 to clear.

Table 3-3 Registers C and D Bit Functions (Cont)

Bit	Function	Description/Interpretation When Set
8	(not used)	Reads as zero.
7	Microsequencer PAR ERR	Detected parity error across the 56-bit PROM data. Read/write 1 to clear.
6:Ø	ERR Syndrome/ Check Bits	Stores 7-bit error syndrome or 7 check bits, depending on the diagnostic mode set in Register B. Read-only.

3.4 REGISTERS E AND F

These are the two data latches on the SBI interface board and may be addressed as registers for diagnostic purposes. After they have been written to, they may be read from, causing data to be output onto the internal DBUS (data bus also called the BUS IF) and sent back onto the SBI through the SBI transceivers. This procedure accomplishes a data wraparound within the interface. No controllers need be present.

3.5 PHANTOM REGISTERS

There are two phantom registers, or two legal addresses, above Registers E and F that may be written to or read from without affecting memory arrays and result in normal interface bus cycles. Their presence is the result of the fact that three bits were needed to allow legal access to six registers (A through F). When three bits are used, eight addresses became available, and since having two more legal addresses does no harm, they are included. These two phantom addresses are valid for Register E but not for Register F.

CHAPTER 4
SYSTEM BLOCK DIAGRAM

4.1 BASIC ARRAY CYCLE

Figures 4-1, 4-2, and 4-3 are block diagrams of the MS780-E/H subsystem, showing the major signal pathways and functional circuit blocks. A more thorough description of their operation may be found in the MS780-E and MS780-H Memory Subsystems Technical Description (EK-780EH-TD).

The SBI interface receives commands through its Interface 8646 SBI transceivers. Command and address information is latched and decoded to determine its applicability to the memory system. (These commands are transferred by the information field of the SBI, B <31:00>). Command and address information is stored in the one-deep command/address latch if it is empty. Tests (valid array address, valid tag and function, and good parity) are then performed, and if all tests are positive, the latch is closed (considered full) and MEM GO is asserted to the controller from the MEM GO logic.

Each controller has a capacity for two-deep storage of command/address information and associated data. If neither buffer is full, MEM GO causes the designated controller to start a memory cycle immediately at the addressed array board. If one is full (a cycle is underway), the command is loaded into the other, and the SBI interface is again ready for new commands. If both are full, the interface waits with the latched command until the controller becomes available. It refuses new commands on the SBI, sending back a BUSY confirmation.

The controller accepts new commands with CONTROLLER GOT IT, clearing MEM GO and reopening the SBI interface command/address latch. All memory cycles start as a read of the selected array.

If the command is a Write, the correct write pulse (or pulses for a quadword write) is generated by the controller, and the data word plus ECC bits are stored in the array RAMs.

If the command is a Read, the data and ECC bits are returned from the selected array and checked for errors in the controller error detection logic. Good data is passed to the data output latch on the controller.

SYSTEM BLOCK DIAGRAM

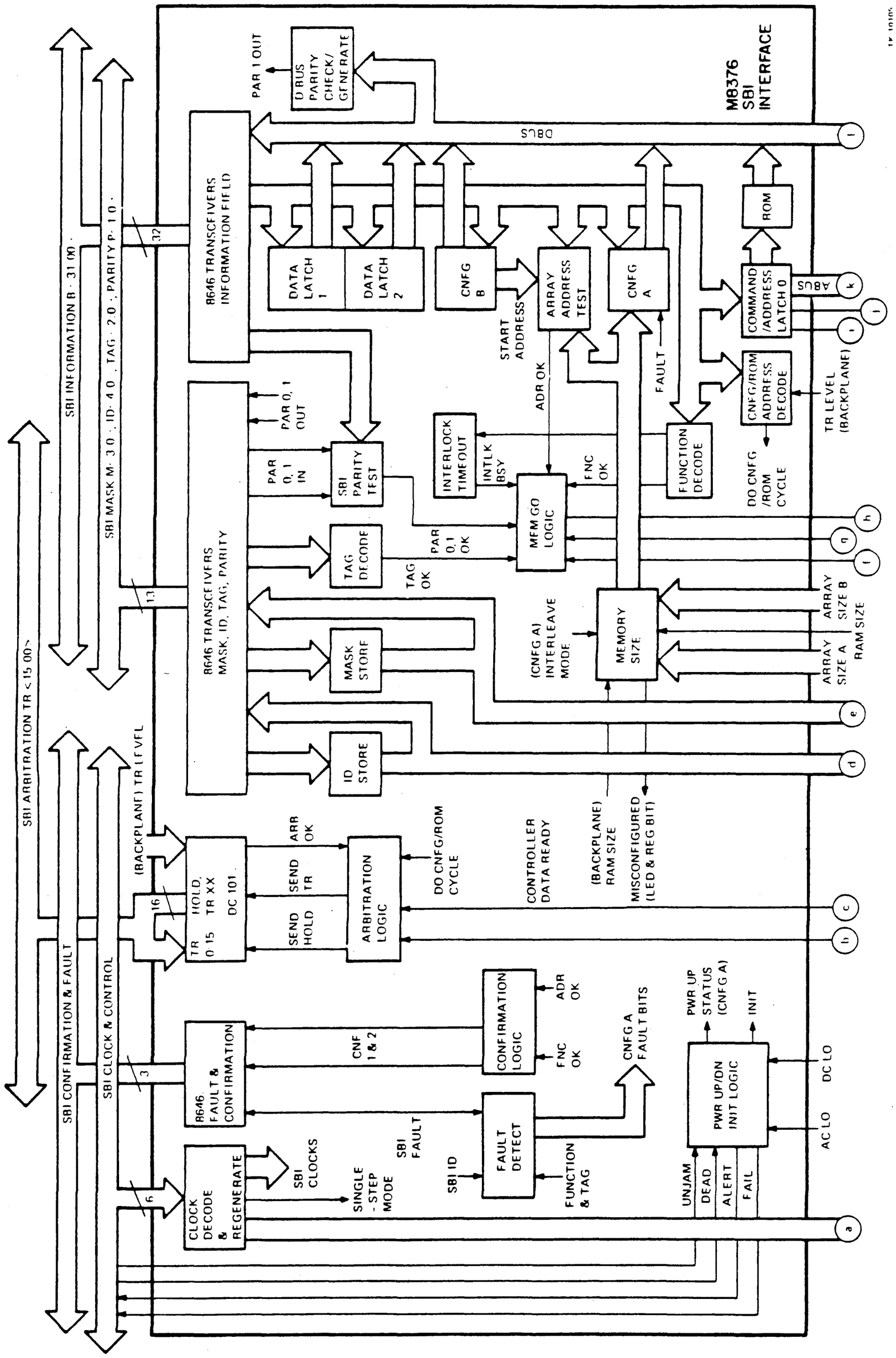


Figure 4-1 MS780-E/H Block Diagram (Sheet 1 of 3)

SYSTEM BLOCK DIAGRAM

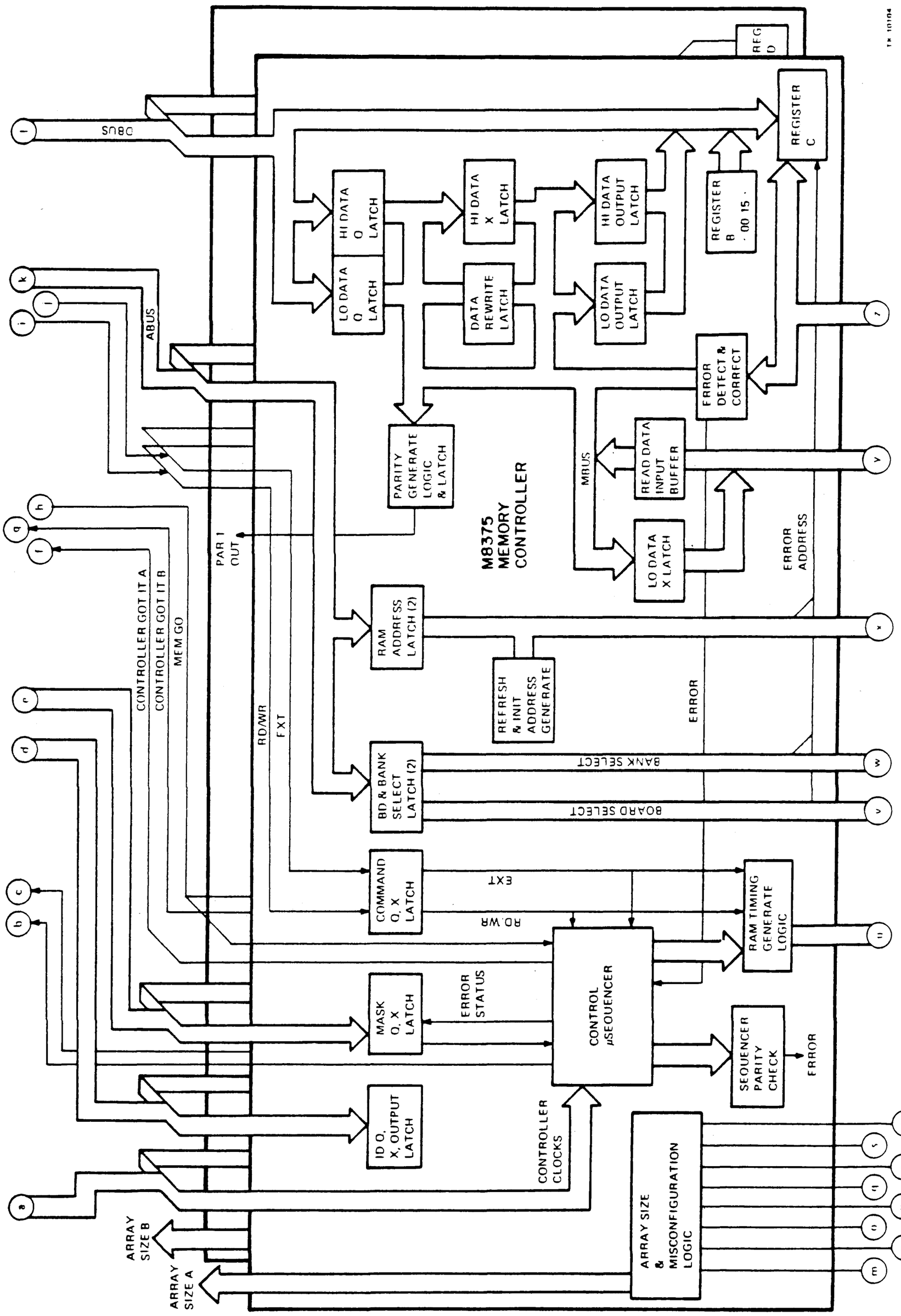


Figure 4-1 MS780-E/H Block Diagram (Sheet 2 of 3)

SYSTEM BLOCK DIAGRAM

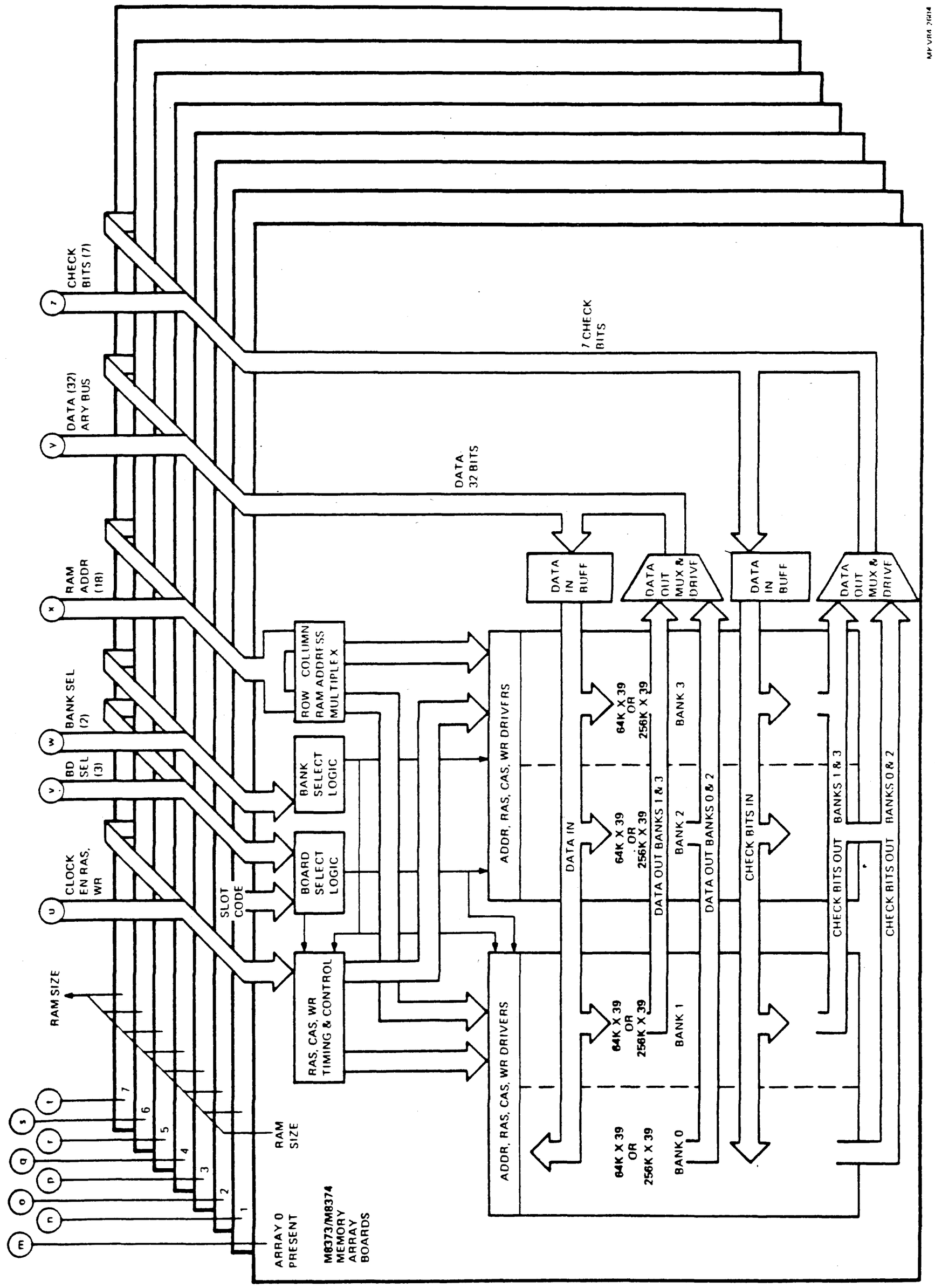


Figure 4-1 MS780-E/H Block Diagram (Sheet 3 of 3)

SYSTEM BLOCK DIAGRAM

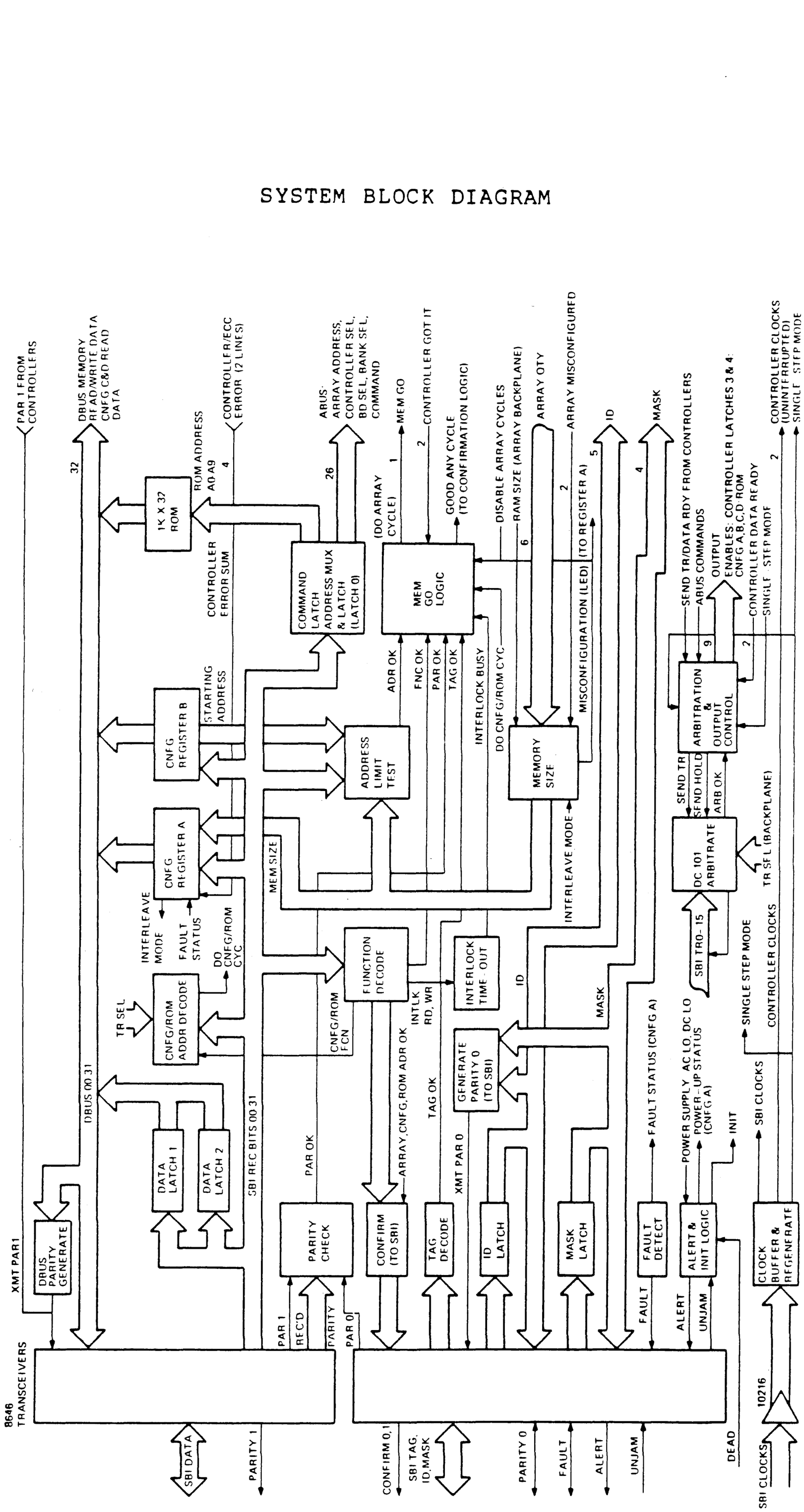


Figure 4-2 SBI Interface Block Diagram

SYSTEM BLOCK DIAGRAM

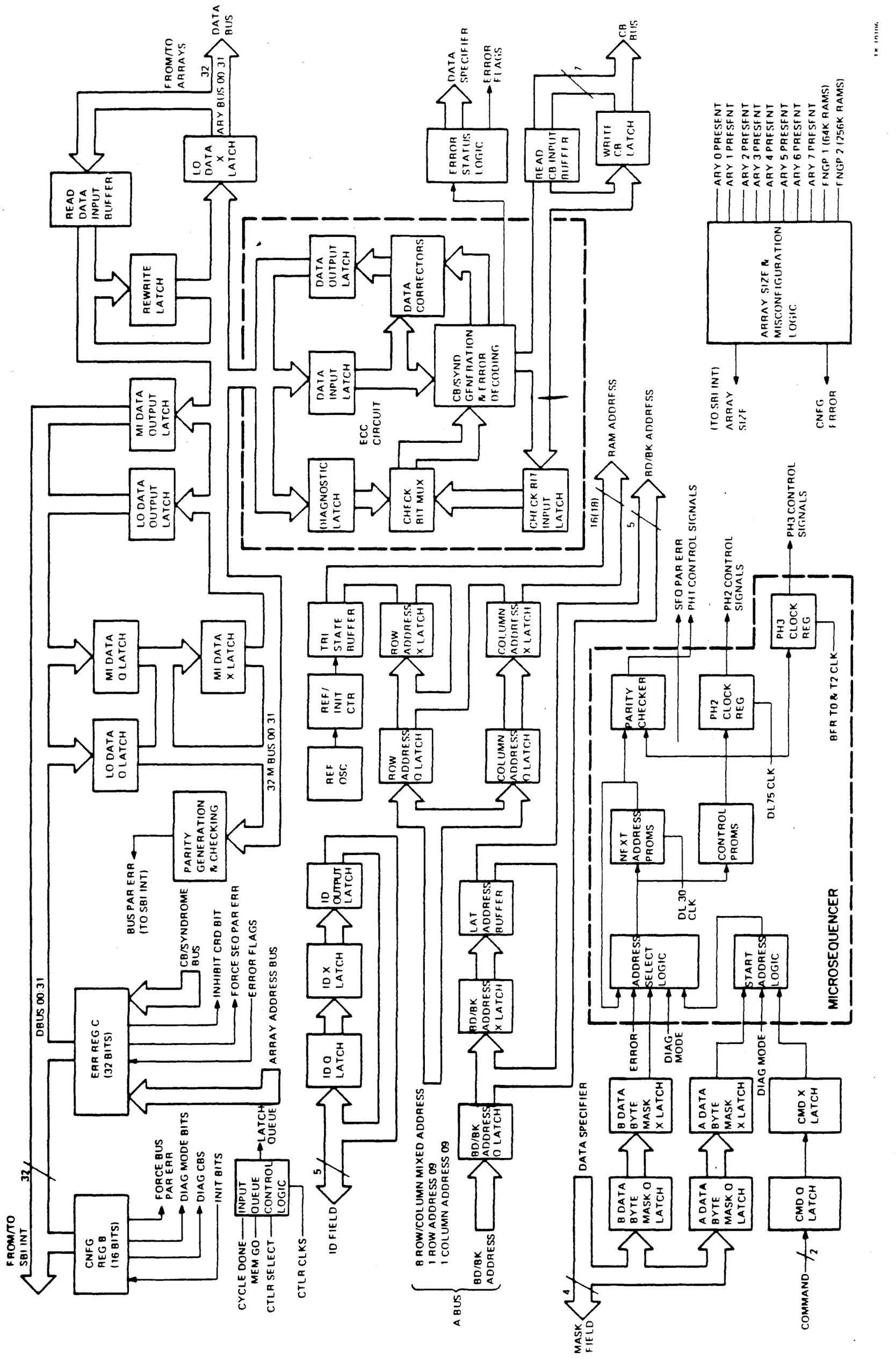


Figure 4-3 Memory Controller Block Diagram

In the meantime, the SBI interface has been arbitrating for SBI time on the assumption that data is on its way from the arrays. When two conditions are satisfied (ARB OK is received from the DC1Ø1 arbitration chip and DATA RDY is returned from the controller), the controller data out latch is enabled and the data is passed on to the SBI at the next cycle.

4.2 CONFIGURATION REGISTER AND ROM CYCLES

The SBI interface also contains logic to check the received address for access to ROM or configuration register space (REG/ROM ADDRESS DECODE). When a valid Read command has been decoded, the selected register or ROM output is enabled and the requested data is made available to the 8646 bus transceivers. Arbitration is simultaneously underway. When ARB OK comes back, the data can be transmitted on the SBI during the next cycle. Valid Write commands can load new data into the registers.

4.3 SUBSYSTEM CONTROL AND DATA PATHWAYS

The three basic elements of the memory subsystem communicate with one another largely over three buses: ABUS, DBUS, and ARY BUS.

Between the SBI interface and the two memory controllers, the ABUS sends all command/address information to the controllers for array reads and writes. This is primarily a one-directional bus, which is always enabled for maximum speed in initiating memory cycles. Within the ABUS, the command takes only two lines: RD/WR and EXT (Extended Cycle Type). In conjunction with MEM GO and the mask bits, these define the varieties of cycles the controllers are to perform. The other 24 ABUS lines are for address: 18 for RAM address, two for bank select, three for board select, and one for controller select. (Some of these lines will be implemented when and if 256K RAMs are used.)

All data transfers between the SBI interface and the controllers and within the SBI interface (REG/ROM accesses) make use of the 32-bit DBUS. This bidirectional bus sends data one way or the other depending on the phase of the SBI clocks:

1. From TØ to T2, the path from the interface to the controllers can be enabled.

2. From T2 to TØ, controller outputs can be enabled to send data back to the Interface 8646 inputs for transmission on the SBI. Register and ROM outputs are also enabled in the T2 to TØ time slot.

SYSTEM BLOCK DIAGRAM

Between a controller and its eight (maximum) arrays, the bidirectional data path is designated as ARY BUS. It is 39 bits wide (32 data and 7 ECC bits). Within the controller, the internal data path is known as MBUS, which is also 39 bits wide. On Write cycles, one of the controller input data latches is the source of 32-bit data to the MBUS. On the MBUS, there is also ECC logic which generates the seven check bits based on that data. The MBUS passes them to the array on the check-bit portion of the MBUS. On Read cycles, one array is enabled and sources 39 bits back to its controller. The ECC logic examines the MBUS data again, tests the returned check bits, and rules on the data integrity. Good data passes from the MBUS back to the DBUS through the data output latches for transmission to the SBI.

Address and control lines to arrays from the controller are one-directional and are always enabled. Each array sources two signals used by the controller and the SBI interface: MEMORY PRESENT and RAM SIZE (64K or 256K). These signals identify which array slots are occupied and permit calculation of the total memory size for the SBI interface address test logic.

CHAPTER 5
POWER SUPPLY REQUIREMENTS

The MS78Ø-E/H requires a new power supply with an additional +5V power regulator that replaces the +12V regulator used in operating the MS78Ø-C memory. The resulting power supply has three +5V voltage regulators, two of which produce 25 amps and are battery backed up and one which produces 5Ø amps and is not backed up.

The memory array requires only +5V power for operation. To minimize the power required from the battery backup supply, the +5V voltage plane has been partitioned into two separate planes called +5VB and +5V. Only the +5VB needs to be battery backed up to maintain data integrity in the event of power failure.

Table 5-1 lists the power requirements for this array in the active and standby states. The active state is defined as the fastest possible operation which is continuously accessing with 6ØØ-ns cycles. The standby state is defined as operation with refresh cycles that occur only once per 12.5 usec.

Table 5-1 Memory Array Power Requirements

		Active		Standby	
		Typical	Maximum	Typical	Maximum
MS78Ø-H	+5VB	2.5ØA	3.7ØA	1.33A	1.75A
MS78Ø-H	+5V	Ø.75A	Ø.9ØA	Ø.75A	Ø.9ØA
MS78Ø-E	+5VB	2.Ø9A	3.29A	1.21A	1.63A
MS78Ø-E	+5V	Ø.75A	Ø.9ØA	Ø.75A	Ø.9ØA

The tolerance on both +5V supplies is +5%. This includes ripple voltage as well as dc variations.

CHAPTER 6
DIAGNOSTICS

The only diagnostic designed explicitly for the MS78Ø-E/F and the MS78Ø-H/J memory is ESKAR, or Micro3. It is run like any other microdiagnostic.

Below is an example of running Micro2 and Micro3.

Micro2 does not test the MS78Ø-E and so produces the following:

```
>>>T
ZZ-ESKAB V14.Ø
3D,3E,
CPU TR = ØØØØØØ1Ø
MS78Ø-E 64K CHIP AT TR ØØØØØØØ1        (Micro2 recognizes MS78Ø-E
  MAX ADDRESS+1= ØØ2ØØØØØ              memories but fails when it
DW78Ø AT TR ØØØØØØØ3                   tries to test them.)
RH78Ø AT TR ØØØØØØØ8
RH78Ø AT TR ØØØØØØØ9
NO MEMORY CNTRLLRS
DEP CNTRLLR ADDR IN RCØ AND TY LO

?ERROR: 11CA  TEST: Ø17D  SUBTEST: ØØØ1

TRACE: ØØ,
FALLING MODULES: M8214,                (Not a module in the
                                       MS78Ø-E/H.)
MIC>
```

DIAGNOSTICS

Running Micro3 with the MS780-E produces the following results:

```
>>>T
ZZ-ESKAB  V14.0

ESKAR-V2.0
3D,3E,
CPU TR - 00000010
MS780E 64K CHIP AT TR 00000001
  LOWER CNTRLLR  MAX ADDRESS+1= 00100000
  UPPER CNTRLLR  MAX ADDRESS+1= 00100000
DW780 AT TR 00000003
RH780 AT TR 00000008
RH780 AT TR 00000009
3F,40,41,42,43,44,45,46,47,48,49,4A,4B,4C,4D,4E,4F,50,51,52
MS780-EF IO BASE ADDRESS = 20002000
LOWER CONTROLLER MAX ADDR + 1 = 00100000
  BOARD NUMBER = 00000000
     NUMBER OF CRD ERRORS = 00000000
MS780-EF IO BASE ADDRESS = 20002000
UPPER CONTROLLER MAX ADDR + 1 = 00100000
  BROAD NUMBER = 00000000
     NUMBER OF CRD ERRORS = 00000000
53,
MS780-E 64K CHIP AT TR 00000001
  M8376  ROMS OK
54,55,56,57,58,59,
STARTING FPA TESTS
5A,5B,5C,5D,5E,5F,60,61,62,63,64,65,66,
END OF PASS 0001

MIC>
```

Upon detection of an error, Micro3 prints the number of the failing module.

Running Micro3 with the MS780-H produces the following results:

```
>>>T
ZZ-ESKAB  V14.0

ESKAR-V2.0   (ETKAR-V3.0 FOR THE VAX 11/785)
3D,3E,
CPU TR - 00000010
MS780H 256K CHIP AT TR 00000001
  LOWER CNTRLLR MAX ADDRESS+1= 00400000
  UPPER CNTRLLR MAX ADDRESS+1= 00400000
DW780 AT TR 00000003
RH780 AT TR 00000008
RH780 AT TR 00000009
3F,40,41,42,43,44,45,46,47,48,49,4A,4B,4C,4D,4E,4F,50,51,52
MS780-E/H IO BASE ADDRESS = 20002000
LOWER CONTROLLER MAX ADDR + 1 = 00400000
  BOARD NUMBER = 00000000
     NUMBER OF CRD ERRORS = 00000000
MS780-E/H IO BASE ADDRESS = 20002000
UPPER CONTROLLER MAX ADDR + 1 = 00400000
  BOARD NUMBER = 00000000
     NUMBER OF CRD ERRORS = 00000000
53,
MS780-H 256K CHIP AT TR 00000001
  M8376  ROMS OK
54,55,56,57,58,59,
STARTING FPA TESTS
5A,5B,5C,5D,5E,5F,60,61,62,63,64,65,66,
END OF PASS 001

MIC>
```

Upon detection of an error, Micro3 prints the number(s) of the modules that could produce such an error.

NOTE ETKAR is V3.0 and ESKAR is V2.0.

DIAGNOSTICS

There are a number of simple things that can be done on the system to verify or detect problems.

NOTE

Before performing these exercises, be sure to turn cache off by typing >>>D 1D 18000. If this is not done, Read commands will read cache, not memory.

1. Read and write to registers on the SBI interface (M8376):

   For example, reading and writing the data latches on the SBI interface board (Registers E and F) test a significant amount of logic on that board. This may be done with or without the controller boards present. Below is an example with no controllers:

```
>>>E 20002000/N:3

        P  20002000  00108E68  !REG A
        P  20002004  0000FFFF  !REG B
        P  20002008  00FFFFFF  !REG C
        P  2000200C  00FFFFFF  !REG D

>>>D/Q 20002010 0                    !0 DEPOSITED IN DATA LATCHES

>>>E/N:5 20002000                    !EXAMINE REGS A - F

        P  20002000  00108E68  !BITS SET - ERROR SUMMARY,
                               !MISCONFIGURATION
        P  20002004  00000000
        P  20002008  00000000
        P  2000200C  00000000
        P  20002010  00000000  !DATA LATCH (REG E)
        P  20002014  00000000  !DATA LATCH (REG F)
```

2. Read and write to registers on the controllers (M8375):

   Register C (lower controller slot 10) and Register D (upper controller slot 12) have a few bits that can be written, but their primary function is to record errors associated with the arrays each controller addresses. A better test of its logic is to read and write to the memory arrays.

3. Read and write to memory arrays:

   Here is a way to test mask functions and extended writes and reads. For example:

```
>>>E Ø
        P   ØØØØØØØØ   ØØØØØØØØ
>>>D/B Ø F
>>>E Ø
        P   ØØØØØØØØ   ØØØØØØØF
>>>D/B 1 F
>>>E Ø
        P   ØØØØØØØØ   ØØØØFØFF
>>>D/W 2 FØFØ
>>>E Ø
        P   ØØØØØØØØ   FØFØFØFF
>>>D/L Ø Ø
>>>E Ø
        P   ØØØØØØØØ   ØØØØØØØØ
>>>D/Q Ø FFFFFFFFFFFFFFFF
>>>E/Q Ø
        P   ØØØØØØØØ   FFFFFFFFFFFFFFFF
```

   Effectively, these exercises have tested most of the logic used in the memory. Errors will be apparent.

4. Moving controllers:

If Micro3 identifies a controller problem (M8375), the problem can be followed by exchanging the positions of the two controllers, rerunning the diagnostic, and verifying that the failing controller is indeed the failing module. For example, move the board in slot 1Ø to slot 12 and place the board in slot 12 in slot 1Ø. Then rerun the diagnostic. The failing module should have moved, eliminating the possibility of a problem other than on the module.

APPENDIX A
DIAGNOSTIC USE OF REGISTERS, MODULE LEVEL FAULT ISOLATION

This appendix describes various diagnostic modes available for use. This information is being supplied to allow exploration of other more sophisticated methods of diagnosis.

A.1 REGISTER A

Register A bit 20 is the error summary bit requested by VMS. It is the ORed result of internal parity errors (Register A bits 19 and 18 plus Register B bit 15 plus Register C bit 7), misconfiguration warnings (Register A bits 17, 16, and 15), and error log request (Register C bit 28). Bit 20 cannot be directly cleared because all contributors must be individually cleared for bit 20 to read a zero.

A.2 REGISTER B

START ADDress is present in Register B bits 27:19 during powerup. The start address may be respecified by loading bits 27:19 with another address. The MS780-E minimum starting address increment is one megabyte. The MS780-H minimum starting address increment is four megabytes. Bits 15:00 of Register B are on the memory controllers. Any bit asserted represents an OR of that bit contained in both memory subsystems. A Write to these bits writes both controllers. FORCE DBUS PAR ERR (bit 11), when written, is asserted on all three boards. On subsequent Read cycles, the addressed controller returns bad parity with Read data for transmission to the RDS tag. It should also set Register A bits 19 or 18, depending on which controller was addressed.

APPENDIX A

Bits 10:09 set up diagnostic modes for controller and memory array testing.

1. Diagnostic Mode 0 -- Bit 10 = 0, bit 9 = 0: Normal operation.

2. Diagnostic Mode 1 -- Bit 10 = 0, bit 9 = 1: Verifies the check bit generation logic. A Write to memory arrays is performed normally, but the check bits, in addition to being stored on the array with data, are also written into Register C bits 06:00. A subsequent Read to Register C can recover the seven check bits and verify the generating logic. Reads and Byte Writes are normal.

3. Diagnostic Mode 2 -- Bit 10 = 1, bit 9 = 0: Tests the error correction logic. Writes are performed normally; Read commands take the 32 data bits from memory but, instead of using the seven check bits stored with the data, substitutes seven bits of Register B (06:00). By loading these to appropriate values for a known 32-bit longword stored in memory, the substituted bits can cause a single-bit error determination by the ECC logic and a correction cycle, complementing the selected bit. The altered longword is sent onto the SBI with a CRD flag, and can be checked to see that the expected bit has been flipped.

4. Diagnostic Mode 3 -- Bit 10 = 1, bit 9 = 1: ECC bypass. Writes are normal. On Reads, data passes through the controller without the normal error checking and correction. This gives direct access to data as it is on the arrays. In addition, the check bits stored with the longword are written into Register C bits 06:00 on every Read. This permits the diagnostic to effectively examine the full 39 bits as they are stored on the arrays.

Register B bit 8 is a refresh lock bit. While it is set, the controller is perpetually busy with refresh cycles and cannot execute a commanded Read or Write. In this state, a pair of extended Write cycles loads up the full set of input data latches of the controller. The latches are tested by loading them as described, and then clearing the refresh lock bit. The Writes should then take place and a set of Read commands to the same addresses verifies that the data is intact.

APPENDIX A

The controller data rewrite latch is exercised by commanding an extended Byte Write (mask not equal to 1111 on both longwords). The data already at the addressed location which is to be retained (not written over) passes through the rewrite latch before being rewritten. The locations (two longwords) should be prewritten so that known data is returned and can be checked by Read commands later. Finally extended Read commands fill both data out latches and should be used to test them.

A.3 REGISTERS C AND D

Attempted access to Register C or D that is incompatible with interleave mode, possibly to a nonexistent controller, results in a normal register cycle for both Read and Write commands. Data returned on a Read is not valid. This is also true for the two phantom register locations above Registers E and F.

In Registers C and D, bit 31 forces a controller microsequencer parity error, if set. This should result in bit 7 of the same register being set as well as the Register A error summary bit.

Bit 3Ø, if set, prevents single-bit errors from sending the CRD flag with Read data on the SBI. The error log request (bit 28) and the CRD error (bit 9) are still set, however. High Error Rate (bit 29) is set if a new single- or multiple-bit error occurs before the previous one has been cleared.

Error Log Request (bit 28) is set by any Read cycle with detectable data errors. Although Byte Writes involve a memory Read, they do not set this bit, the RDS flag (bit 1Ø), or the CRD flag (bit 9). In the event of a single-bit error detected during a Byte Write, the error is corrected but no record is kept. A multiple-bit error results in the bad data, including check bits, being rewritten into memory exactly as it was read out. A subsequent Read to the location discovers the error and logs it properly.

Error Address (bits 27:11) are loaded following single- or multiple-bit errors. If it was filled with the location of a single-bit error and a multiple-bit error follows before the first was logged, the multiple-error address overwrites the original address. Any other sequence of two errors keeps the original address. The contents of the error address field are not valid unless bit 1Ø (RDS) or bit 9 (CRD) is set.

MS780-E/F AND MS780-H/J
MEMORY OPTIONS MAINTENANCE
ADVISORY

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