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Q-BUS I/O-MODULES

IDV1S-A, IDV1S-B, IDV1S-C, IDV1S-D,
IAV1S-A, IAV1S-AA, IAV1S-B. IAV1S-C,
IAV1S-CA MODULES

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NOTEBOOK SECTION

4.3. - 35

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DRAWING SET NUMBER

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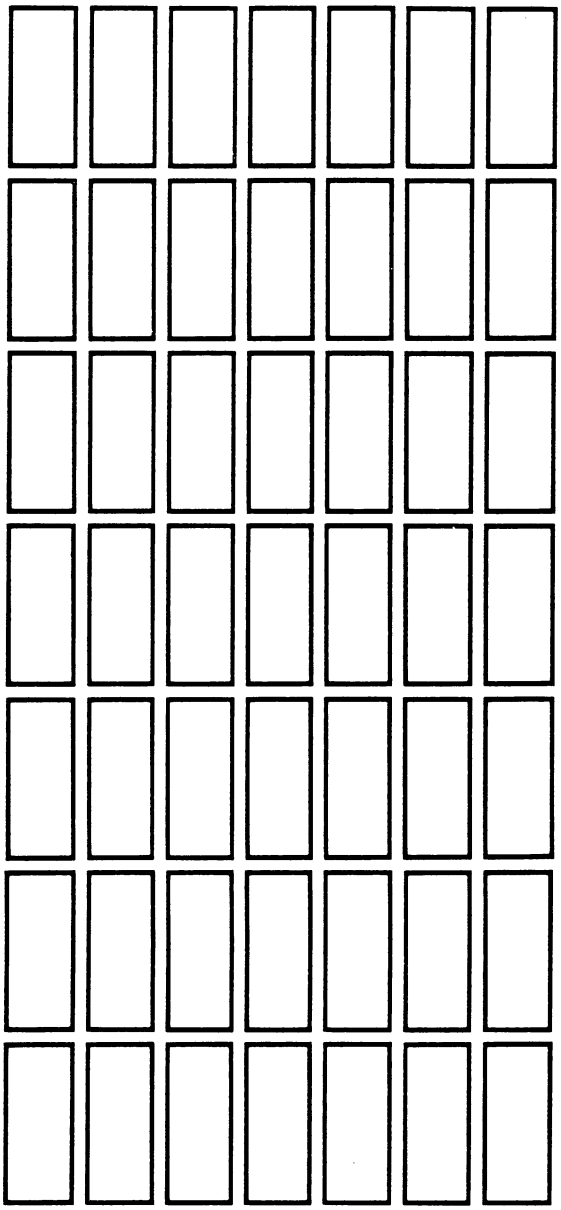

Q-BUS I/O-MODULES

IDV1S-A, IDV1S-B, IDV1S-C, IDV1S-D,
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DECsystem-10	Professional	VMS
DECSYSTEM-20	Rainbow	VT
DECUS	RSTS	Work Processor

CONTENTS

FIGURES

TABLES

Warning!
To prevent electrical shock or energy hazards, interface only with SELV(safety extra low voltage) equipment(IEC435).

Warnung!
Um einen elektrischen Schlag zu vermeiden, sind nur Sicherheits-Kleinspannungsstromkreise (SELV) anzuschließen(IEC435).

Avertissement!
Pour éviter on choc électrique ou des dangers de transfer d'énergie mettre en contacte seulement avec les circuits à TBTS (très basse tension de securité)IEC435.

Atención peligro!
Para impedir un choque electrico solo se debe conectar circuitos de baja tension seguum norma IEC435.

Varoitus!
Sähköiskujen välttämiseksi liitä ainoastaan turvallisuuspienjännite (SELV) laitteita (IEC435).

Varning!
För att undvika elektrisk chock eller annan fara så får endast SELV (Säker extra låg spänning) utrustning anslutas (IEC435).

Waarschuwing!
Om een elektrische schok te vermijden, alleen aan veiligheids lage spanning stroomcircuik (SELV) aanslniken (IEC435).

Attenzione!
Per prevenire scosse elettriche o pericoli di fulminazione si raccomanda di utilizzare solamente apparecchiature o strumenti a bassissima tensione di sicurezza (IEC435).

Advarsel!
For at forebygge personskade eller anden skade, må der kun tilsluttes ekstra isoleret lavspændings-udstyr.

Advarsel!
For aa hindre elektrisk sjokk eller annen skade, tilknytt dette utstyret kun mot utstyr med ekstra lav spenning. (IEC435 / spenning lavere enn 42.4 Volt)

CHAPTER 1

MODULE SET OVERVIEW

1.1 GENERAL

This manual includes information on a series of boards that are I/O options for MicroVAX and MicroPDP11 Q-bus processors, based on BA200-series system enclosures. Each board may be used by itself on the Q-bus, but typically each is used with one or more of the other boards to create a small I/O system.

These boards are especially appropriate for use in electrically noisy environment, since most I/O circuits are electrically isolated from the computer power. This allows a high common mode voltage for the field signals.

The family includes the following modules:

IDV1S-A	16-BIT OPTO ISOLATED INPUT	(M5026-P0)
IDV1S-B	16-BIT OPTO ISOLATED OUTPUT	(M6029-P0)
IDV1S-C	16-BIT RELAY OUTPUT	(M8005-P0)
IAV1S-B	4-CH ISOLATED D/A CONVERTER	(A6007-P0)
IAV1S-A	4/12 CHANNEL A/D CONVERTER	(A410-P0)
IAV1S-AA	16 CHANNEL A/D CONVERTER	(A410-PA)
IAV1S-C	16-CHANNEL FLYING CAP. MULTIPLEXER	(A029-P0)
IAV1S-CA	16 CHANNEL EXPANSION MULTIPLEXER	(A029-PA)
IDV1S-D	FIVE CHANNEL COUNTER MODULE	(M7197-P0)

The IAV1S-C/CA is an add-on option to the IAV1S-A/AA A/D converter. The 16 channels of the IAV1S-A can be expanded with several IAV1S-C multiplexer boards for a higher number of analogue inputs.

NOTE

The IxV1S module family for the BA200 series Q-bus enclosure is software and functionally compatible to the IxV11 module family for standard Q-bus enclosures, but have different I/O-connectors.

RELATED LITERATURE

The following manuals provide Q22-bus signal specifications and provide added information on other Q-bus options respectively:

- BA2xx Enclosers
- Microcomputer Products Handbook
- Microsystems Handbook
- MicroVAX CPU Module User's Guide
- MicroVAX II Technical Manual
- MicroVAX Systems Maintenance Guide

These manuals are available through your local DIGITAL sales office.

FCC/FTZ USER STATEMENT

This equipment generates, uses, and may emit radio frequency energy. The equipment has been type tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of FCC rules, which are designed to provide reasonable protection against such radio frequency interference. Operation of this equipment in a residential area may cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

1.2 ADDRESS AND VECTOR ALLOCATION

To facilitate the use of the boards described in this manual, the registers of all the boards are structured in the same manner and arranged in the same sequence.

Per module, there are always four word addresses from the I/O address range reserved even if only two are required (e.g. the digital output boards).

The first register is always the Mode Register (MOD), which is used by the test software and by the software handler to recognize the type and function of the boards.

ADDRESS RANGE

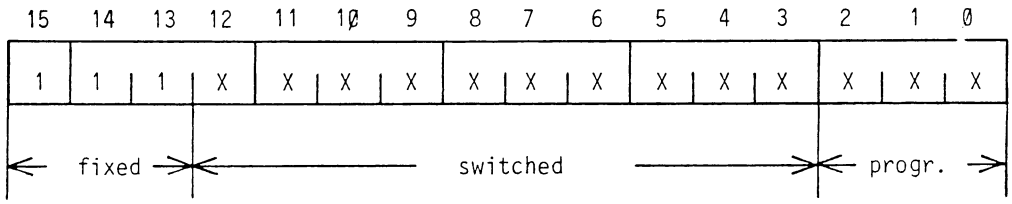
The device address is to be set by switches within a range of 160000 octal to 177770 octal.

The I/O boards described here should be configured with their addresses in the following standard device address range:

modules without interrupt 171000 to 171370
modules with interrupt 171400 to 171770

Each range covers an address possiblity of 32(dec.) boards when four registers are reserved per module (Figure 1-1).

Address Selection



Standard Addresses: 171000 to 171370 (without interrupt)
171400 to 171770 (with interrupt)

Figure 1-1: Address Selection

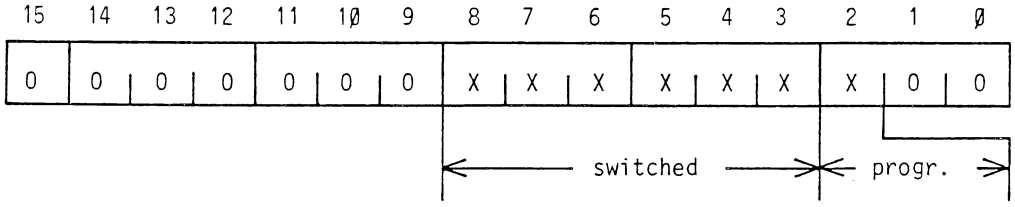
VECTOR RANGE

The interrupt vector address is set by switches within the range of 0 to 770 octal in increments of 10 octal.

Those modules with interrupt capability should be located in the standard address range from 171400 to 171770. If the vector bits 3 to 8 are switched to the same position as the address bits, a vector range of 400 to 770 octal is available (Figure 1-1).

This vector range means 64 (decimal) vectors and 32 (decimal) modules, because two vectors are reserved for every module with interrupt capability.

Vector Selection



Standard Vectors: 400 to 770

Figure 1-2: Vector Selection

NOTES

- The recommendations for address and vector ranges and the factory configured addresses and vectors in this manual refer to XXDP-diagnostic (MicroPDP11) requirements of the IxV1S module set. The addresses assigned by the XXDP diagnostic should be used for RSX11 handler software too.

- The MDM diagnostic on MicroVAX needs other addresses and vectors which have to be assigned in the floating device address range if auto-configuration is used to run the diagnostic. See the standard address configuration rules or use a configuration program to assign the correct floating device addresses. The same addresses and vectors which are assigned for MDM diagnostic should then be used for the VMS handler.

- The IDV1S-B, IDV1S-C, IAV1S-B modules do not have interrupt vectors, but it may be necessary to select dummy vectors for the device handlers or for MDM diagnostic.

1.3 MODULE IDENTIFICATION

The module set can be identified by the software. Every module type can be recognized by an 8 bit code in the high-byte of the Mode Register (MOD).

This identification is used in the diagnostic and driver software to identify the function and register structure of each module.

The identification code (octal) is divided into the following function groups:

a. 000 to 037 Digital Input Modules

b. 040 to 077 Digital Output Modules

c. 100 to 107 "OR"-ed with 110 to 170 Analogue Input Controller connected to Analogue Input Multiplexer Board

d. 200 to 207 Analogue Output Controller

e. 300 to 377 Special Modules (five channel counter)

The identification codes of the module family described here are listed in the following table.

An installation protocol of the modules present can be obtained with the test program, provided that the standard address range, which is described in chapter 1.2, is used.

Identif. Code (oct.)	Module Designation	Description
004	M5026-P0	IDV1S-A 16 Bit Opto Isolated Input
040	M6029-P0	IDV1S-B 16 Bit Opto Isolated Output
042	M8005-P0	IDV1S-C 16 Bit Relay Output
100*	A410-P0	IAV1S-A 4/12 Channel A/D Converter
100*	A410-PA	IAV1S-AA 16 Channel A/D Converter
110*	A029-P0	IAV1S-C 16 Ch. Flying Cap Multiplexer
110*	A029-PA	IAV1S-CA 16 Channel Expansion Multiplexer
200	A6007-P0	IAV1S-B 4 Ch. Isolated D/A Converter
300	M7197-P0	IDV1S-D Five Channel Counter Module

Table 1-1: Module Identification Codes

NOTE

* the -PA versions are variations of the -P0 modules and thus they have the same identifier code.

1.4 COMMON INSTALLATION PARAMETERS

All modules described in this manual have the following common parameters for both installation and use.

1.4.1 Module Format

The module size is a quad-high module format with a flush bulkhead handle for the BA200 series Q-bus system enclosures. The module handle provides Electro-Magnetic Conduction (EMC) shielding that complies with FCC regulations.

1.4.2 BA200-series System Enclosure

The IXV1S modules have to be installed in BA200 series enclosure. The enclosure has a 6-slot or 12-slot Q-bus backplane and one or two modular power supplies.
The backplane implements the Q22-bus on AB rows of each slot. The CD interconnect is implemented in all 12 slots. MicroVAX systems use the DC rows of slots 1 through 3 for their high-speed memory interconnects.

1.4.3 Installation and Configuration Rules

The installation and configuration of the modules have to be made according to the standard rules for BA200 series enclosures and Q-bus backplanes.
Installation instructions e.g. can be found in the DEC manuals MicroVAX CPU Module User Guide and Microsystems Handbook.
Detailled information about the installation of the individual modules can be found in the particular module description in this manual in the chapter "Installation".

NOTE

The IxV1S modules are flash handle modules. When you use a flash handle module next to a recessed handle module, you must install a metal filler plate between the modules to meet FCC regulation. The filler plate part number is 70-24071-01.

1.4.4 Installation Checkout on Micro-PDP11

All modules can be tested with the same diagnostic program CZIXV?? (except the IDV1S-D which has to be tested with the diagnostic CZIDV??). The following program sections can be used to check for correct installation of one or several of the modules.

- Print Configuration Table
  The printout can be checked with Table 1-1 in chapter 1-3 of this description.

- Internal Logic Test
  This test checks the internal registers of the selected modules. This will also test modules with interrupts if there are any installed.

Further test possibilities are given in chapter 1-5 and in the diagnostic listing.

1.4.5 Installation and Checkout on MicroVAX

Following MDM diagnostics can be used for the individual module types:

GGSKMIDA for IDV1S-A (see Note)
GGSKMIDB for IDV1S-B
GGSKMIDC for IDV1S-C
GGSKMIDD for IDV1S-D
GGSKMIAA for IAV1S-A, IAV1S-AA
GGSKMIAA for IAV1S-C, IAV1S-CA
GGSKMIAB for IAV1S-B

The diagnostics are divided into several groups and will lead the user through operation.

NOTE

The options in the diagnostic are named IxV11. The IxV1S options are the BA200 series enclosures versions and software compatible to the IxV11.

1.4.6 User I/O-Connector

The user I/O-connector is integrated in the module handle. Each module has the same 50-pin D-type subminiature male connector (plug). See figure 1-3 I/O-Connector Dimensioning. The module connector has a slide latch assembly to lock the cable connector.

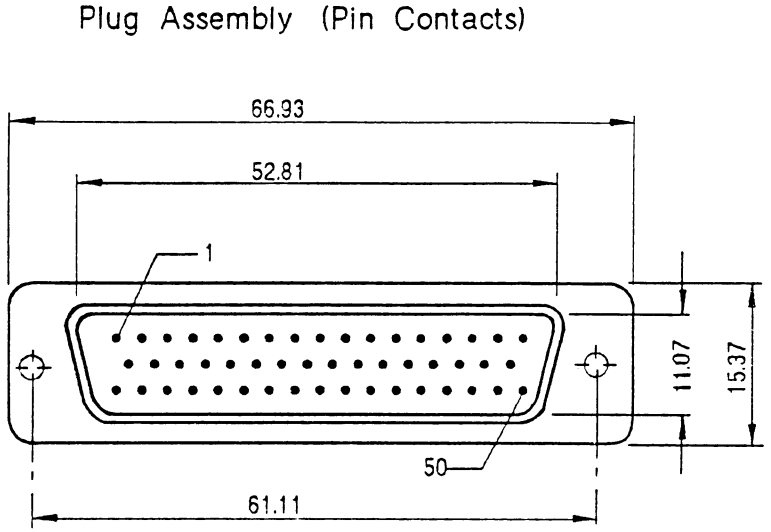


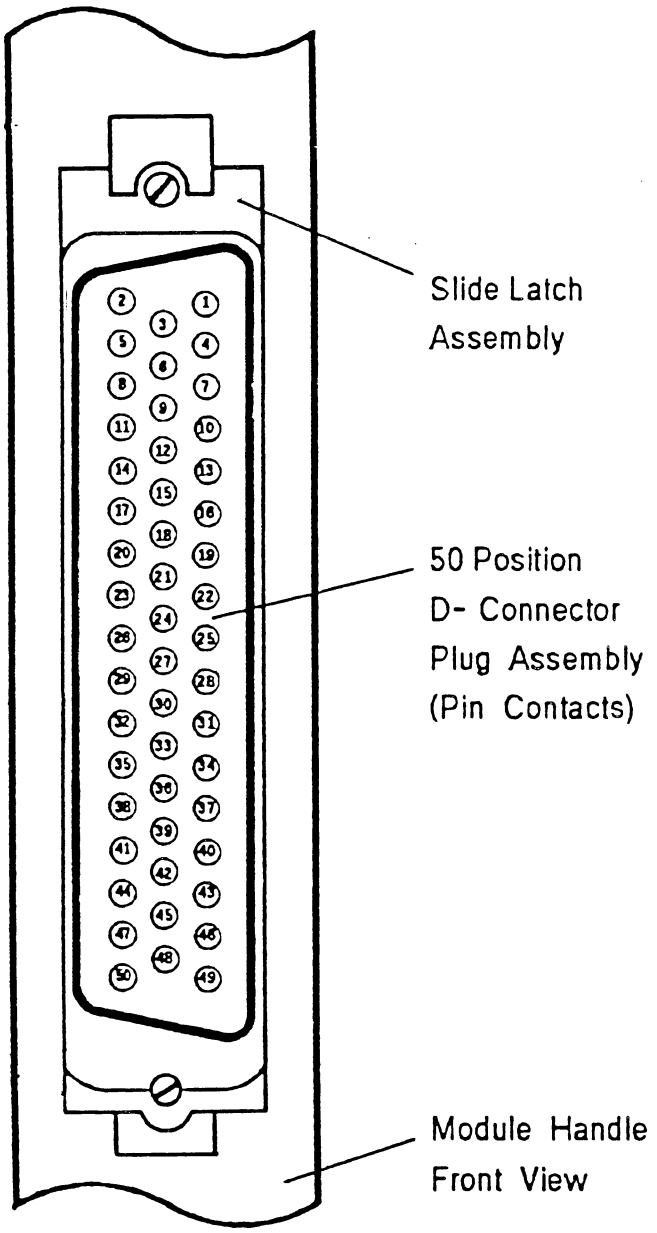
Figure 1-3: I/O-Connector Dimensioning

The maximum preferred cable connector depth from the surface of the module handle is 40.6 mm. A cable connector depth greater than those will abut on the inside of the system enclosure, preventing skins/doors from closing. For example, the shielded cable clamp assemblies from ITT/Cannon DD115386-92 or DD19977-4 or equivalent can be used.

Versions of the 50-pin I/O-connector are available for flat cable or discrete wire connection. For FCC requirements the user cable and the connector have to be shielded. The wire shield has to be connected to the connector Gnd/handle Gnd.

Users which need single wire connections can use the H3031-A screw terminal. To connect this screw terminal to a IxV1S module, the adapter cable 2G-E10JA-0E (0.5 m length) or equivalent have to be used. The pin arrangement on the screw terminal is identical to those of the internal board connector, see Figure 1-3.

In Figure 1-3 "I/O-Connector Pin Arrangement", the module I/O-connector plug assembly is shown form handle front view. A receptacle assembly (cable connector) is mirror image.



Pin Assignments for Reference

I/O-Connector	Internal Board Connector
1	A
2	B
3	C
4	D
5	E
6	F
7	H
8	J
9	K
10	L
11	M
12	N
13	P
14	R
15	S
16	T
17	U
18	V
19	W
20	X
21	Y
22	Z
23	AA
24	BB
25	CC
26	DD
27	EE
28	FF
29	HH
30	JJ
31	KK
32	LL
33	MM
34	NN
35	PP
36	RR
37	SS
38	TT
39	UU
40	VV
41	not used
42	
43	
44	
45	
46	
47	
48	
49	
50	

Figure 1-4: I/O-Connector Pin Arrangement

1.4.7 Environment (per DEC Standard 102, Class C)

Operating Temperature	+5 to 50 degrees celsius *
Relative Humidity	10% to 90% noncondensing.
Airflow	Sufficient airflow must be provided to limit the temperature rise across the module to: <10 degrees celsius for inlet temperature below 55 deg. celsius

* Lower the maximum temperature by 1 degree celsius for every 1000 feet (300 m) of altitude above 8000 feet (2400 m). Normally, the modules should be mounted in a DEC standard enclosure, which is fitted with fans.

NOTE

These are the design limits. Lower temperature limits will serve to increase the lifetime of the module.

1.5 MAINTENANCE

This chapter refers to the IxV11-module set diagnostics. The IxV11 is the standard Q-bus enclosure version. The IxV1S is the module set for BA200 series enclosures. Both module families are software compatible.

NOTE

The testconnectors which are used for the IxV11-modules and described in Appendix B have to be used for the IxV1S-modules too, but the adapter cable 2G-E10SA-0L (see Appendix B) is needed to install the testconnectors on IxV1S modules.

1.5.1 Module Family Diagnostic for LSI 11 - Processors

The module set described is tested by the diagnostic CZIXV?? "IDV11/IAV11 I/O Module Family" DIAG (except the Five Channel Counter Module M7197, in which case the Five Channel Counter DIAG CZIDV?? has to be used). Each module contains one LED, which is on when the module is being tested.
There are four diagnostic program sections which may be used for field tests.

- Print Configuration Table
  With this routine, one module or a set of modules can be identified with the device address, the module identification code and its selected operation mode. The standard address range should be used on this test.

- Internal Logic Test
  This test section performs detailed tests on each separately accessible part of the device.

- Device I/O Tests
  Some test equipment is necessary in this test section. The "Digital I/O Test Connector" for the digital I/O modules, the "Analogue Input Test Connector" for the analogue input modules or one of the "Analogue Output testconnectors" for the analogue output modules. The test connectors are described in Appendix B "Field Test Equipment".

- I/O Line Check
  Specifically selectable tests allow the user to read or write the user interface of the chosen device. User lines can be set or monitored for the digital I/O modules. This test can be used to calibrate the analogue I/O modules. Calibration procedures of the analogue modules are described in the individual module descriptions.

The use of the diagnostic and a test description are included in the diagnostic listing.

1.5.2 Module Diagnostics for MicroVAX-Processors

The different modules can be tested with following MDM diagnostics:

GGSKMIDA for IDV1S-A
GGSKMIDB for IDV1S-B
GGSKMIDC for IDV1S-C
GGSKMIDD for IDV1S-D
GGSKMIAA for IAV1S-A, IAV1S-AA
GGSKMIAA for IAV1S-C, IAV1S-CA
GGSKMIAB for IAV1S-B

The diagnostic programs are equally structured. The tests are divided into six groups:

- the Configuration Procedure
  that verifies that the addressed module is the correct device for the selected program

- the Verify Mode Functional Tests
  which are testing the module-functionality without manual intervention of the operator

- the Verify Mode Exerciser
  which is using all verify mode functional tests together

- the Service Mode Functional Tests
  which are testing the modules completely and require to connect test equipment, as described in Appendix B

- the Service Mode Exerciser
  which simulates the intense use of the module under normal system conditions

- the Service Mode Utilities
  which allow the operator to test module functions in a dialog mode

NOTE

To run MDM diagnostic in onto configuration, other addresses and vectors have to be assigned as used in this manual, see chapter 1.2.

1.5.3 Maintenance Philosophy

Module replacement is the suggested maintenance technique. The recommended spare parts are the complete boards (see Appendix "Shipping List").

NOTE

Before starting any system checkout that may affect field signals produced by the I/O modules, for example running the diagnostics, contact the customer and take appropriate safety precautions.

CHAPTER 2

IDV1S-A 16 BIT OPTO ISOLATED INPUT (M5026-P0)

2.1 GENERAL DESCRIPTION

The IDV1S-A is an isolated digital input module (M5026-P0) for the Q-bus. It accepts up to 16 single optically isolated inputs used for monitoring voltages where noise immunity or common mode rejection is important. The 16 bit data are read by programs and transferred to the processor or memory.

The input line bit 15 is selectable for interrupt by program and generates an interrupt at the leading edge (ON-going signal) and/or at the trailing edge (OFF-going signal).

The standard input range is 24 to 42 Vdc. In this range, the input switching delay can be changed by a programmable contact bounce eliminator to three different values.

In addition, a programmable low level input range for low speed, low power 5 Vdc signals and usable for TTL or MOS inputs is selectable.

IDV1S-A FEATURES

- 16 single optically isolated inputs
- interrupt capability on input line bit 15
- interrupt generating signal edge is programmable
- programmable contact bounce eliminator
- standard input range from 24 to 42 Vdc
- programmable low level range for 5 Vdc signals
- module identification code readable by program

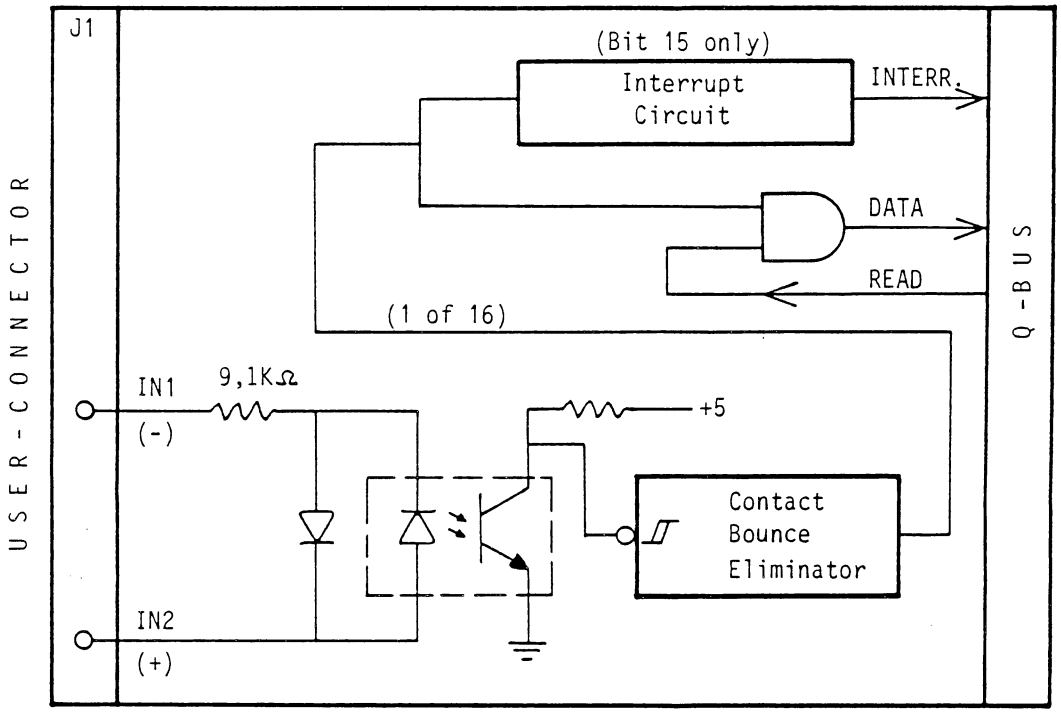


Figure 2-1: IDV1S-A Simple Block Diagram (M5026-P0)

2.2 SPECIFICATION

Module Designation	M5026-P0
Identification	004 octal (identification code when reading the MOD register)
Module Size	Quad high Module (for BA200 enclosures)
Power Requirements	5,0 Vdc at 720mA ±5%
Bus Load	1 DC-Load; 2 AC-Load

INPUT CIRCUITS

No. of Digital Inputs	16 two wire optocoupler inputs
Standard Input Range	24 to 42 Vdc at 2,6 to 5,2mA; ON voltage 11V minimum; OFF voltage 4,2V maximum; Max. input voltage 42V
Contact Bounce Eliminator (Software selectable)	Default debounce delay is 5 millisec ±30%; programmable to 500 microsec ±60% or 10 msec ±20%
Low Level Input Range (Software selectable)	Min ON-voltage is 4,2 Vdc at 0,46mA; max. input frequency is 50Hz on 50% duty cycle; Max. input voltage 42V
Hysteresis	Approx. 0,55V for both input ranges
Isolation Voltage	Inputs to Computer Gnd 1000 Vdc or peak ac
Interchannel Isolation	250 Vdc or peak ac

BUS INTERFACE

Register Addressing	Switch selectable over the 4K I/O address range; occupies a 4 word address with one word unused
Interrupt Vector	Switch selectable from 000 to 770 octal
Priority Level	BR4 (jumper selectable level 5 or 6)

2.3 INSTALLATION

2.3.1 Site Considerations

The IDV1S-A has two bus interface connectors that plug into a Q-bus slot. These connectors have signals which are defined in the Q-bus specification. The interrupt priority of the module is determined by the position on the Bus (position dependent configuration). The closer a device is located to the processor, the higher its priority.

2.3.2 Interconnections

Interfacing the IDV1S-A to the user's device is done via the 50 pin D-type male connector. A 50 conductor flat cable or a user made twisted pair cable may be used for field connection. The pin assignment and the signal description can be found in chapter 2.5.
General informations about the user I/O-connector and the physical requirements are given in Chapter 1.4.6.

2.3.3 Initial Operation

Selecting the IDV1S-A Device Address

The device address is the I/O address assigned to the MOD-register. The device address is selected via a 10-pole switch (Figure 2-4). The switches allow the device to be set within a range of 160000 octal to 177770 octal. The standard address range for this module is from 171400 to 171770 in increments of 10 octal (Figure 2-2).

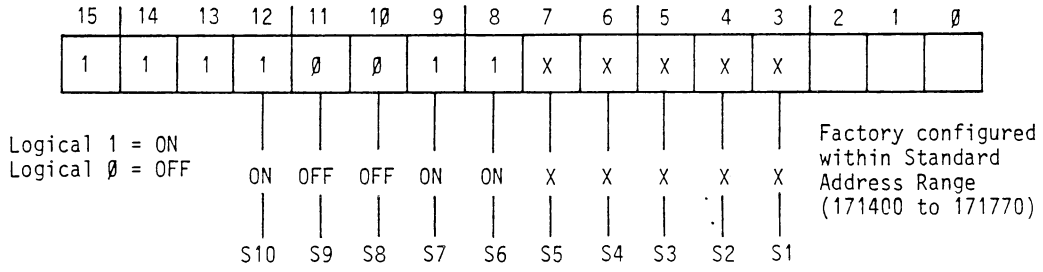


Figure 2-2: Selecting IDV1S-A Device Address

Selecting the IDV1S-A Interrupt Vector Address

The IDV1S-A is capable of generating one interrupt vector. The interrupt vector address can be set via a 6-pole switch (Figure 2-4) within the range of 0 to 770 octal in increments of 10 octal.

For standard vectors, the vector switches 1 to 6 (Figure 2-3) should have the same position as the address switches 1 to 6 (Figure 2-2). This means that the address and vector are identical for address bits 3 to 8.

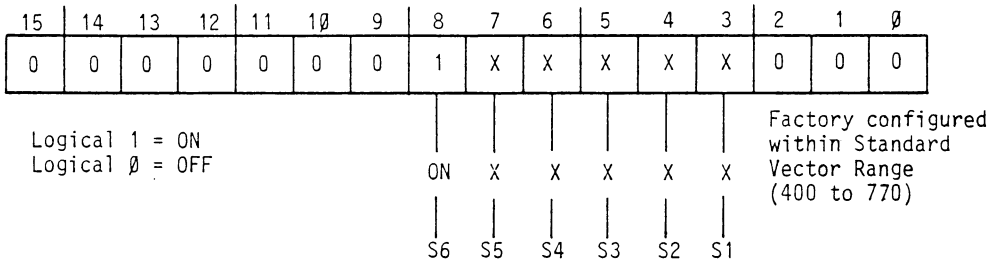


Figure 2-3: Selecting IDV1S-A Interrupt Vector

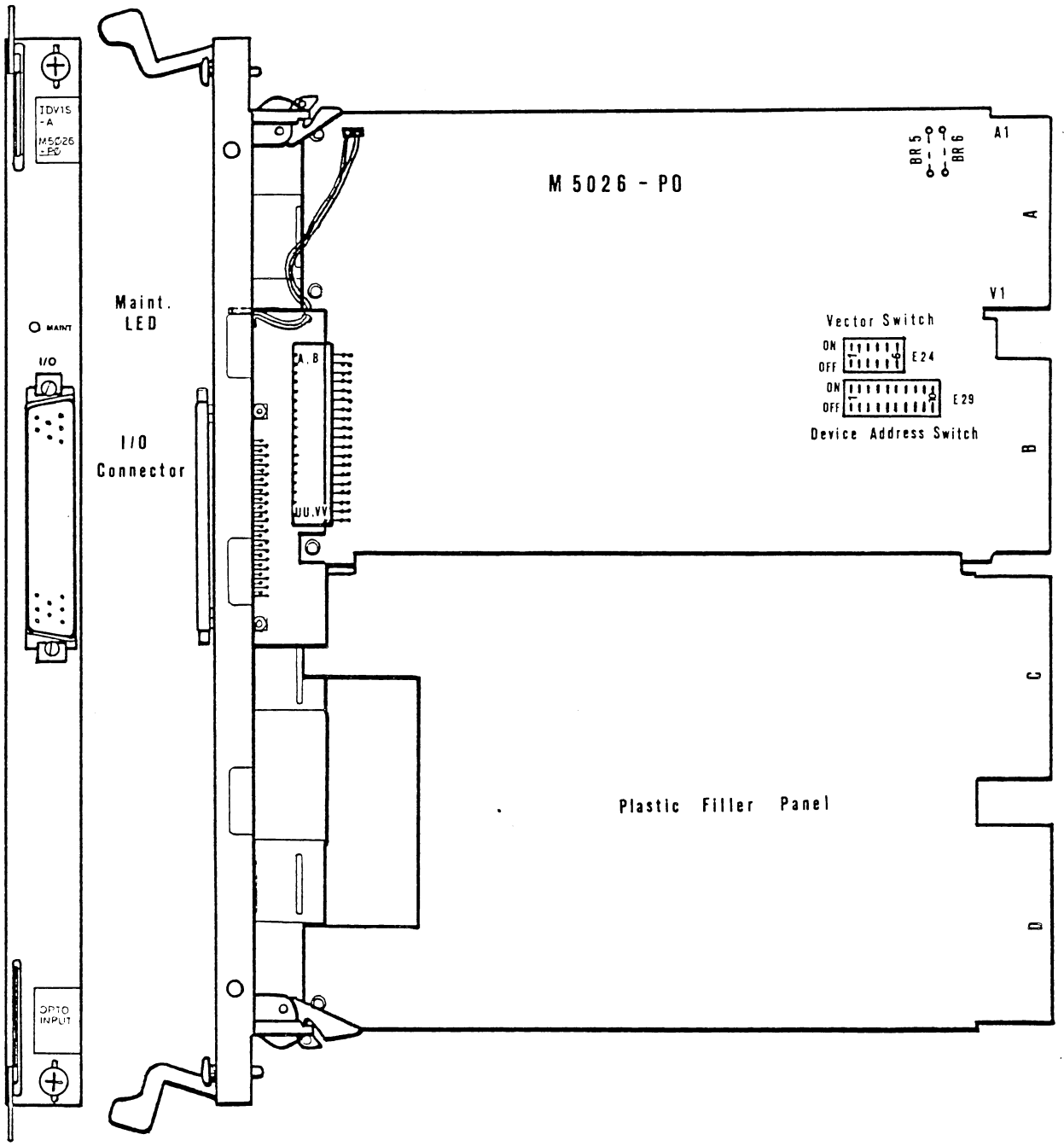


Figure 2-4: IDV1S-A Physical Layout M5026-P0

Selecting the Interrupt Request Level

The standard interrupt request level is 4 (BIRQ4). A higher request level, BIRQ5 or BIRQ6, can be selected via the jumpers BR5 or BR6.

Whenever the BIRQ4 on the module is changed to a higher level, no other modules, which have a lower request level, should be installed on the bus closer to the processor. The interrupt priority of the IDV1S-A is position dependent and does not monitor higher request levels.

2.4 OPERATION AND PROGRAMMING

2.4.1 General

This chapter presents a detailed description of the IDV1S-A registers (see figure 2-5). Four consecutive bus addresses are assigned to the register set.

171XX0	Mode Register	(MOD)
171XX2	Input Data Buffer	(DAT)
171XX4	Control Status Register	(CSR)
171XX6	unused	-

They can be read or loaded using any instruction which refers to their address.

Initialization

The mnemonic INIT refers to the initialization signal issued by the processor. Initialization is caused by one of the following:

- issuing a programmed RESET instruction
- depressing the start switch on the processor console
- the occurrence of a power-up or power-down sequence

The MOD and CSR registers are then initialized.

Operation Modes

All variable operation modes of the IDV1S-A, e.g. the low level input range, contact debouncing and the interrupt generating signal edge, are program selectable. They are described in the CSR-bit description and in chapter 2.5.

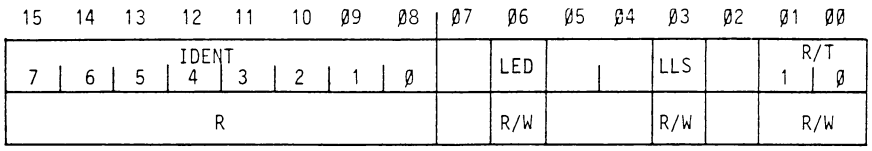
2.4.2 Mode Register (MOD)

The MOD register is generally used to identify the module with its identification code and to select operation modes. If this register is not used by the user program, the module has standard parameters as shown in the following bit description.

Bit	Name	Description
15 to 8	IDENT 7 to IDENT 0 (read only)	Identification Bits 7-0 The module is identified by these bits. The M5026 has the code 004 octal (in high byte).
3	LLS (read/write)	Low Level Input Range Select Setting this bit enables the 16 input lines to the 5 volt input range. Otherwise the standard input range of 24 to 42Vdc is selected.
1 0	RT1 RT0 (read/write)	Input Response Time, for the contact bounce eliminator circuits of the 16 input lines. bin. 0 not selectable 1 response time 500 microsec 2 response time 5 millisec 3 response time 10 millisec After INIT the bit RT1 (5 millisec) is selected.
6	LED	LED indication for test purposes.

Table 2-1: IDV1S-A MOD Register Bit Assignments

MOD 171XX0 - Mode Register



NOTE: R = Read Only
W = Write Only
R/W = Read/Write
R/WZ = read/write to zero with a "1"

All bits not described are unused
and read or written as zero

Figure 2-5: IDV1S-A Mode Register

2.4.3 Input Data Buffer (DAT)

The input data buffer is a 16-bit read only register that monitors the data of the input lines 0 to 15.

DAT 171XX2 - Input Data Buffer

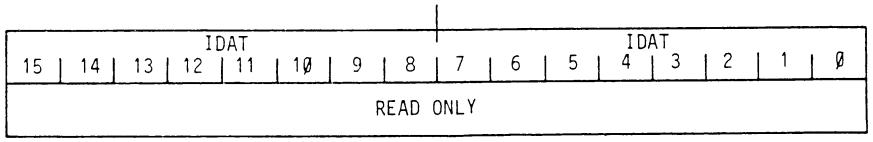


Figure 2-6: IDV1S-A Input Data Buffer

2.4.4 Control and Status Register (CSR)

The input line 15 (IN15) enabled using bit 14 (EI) in the CSR-register to generate an interrupt. Line 15 is also monitored in the input data buffer bit 15.

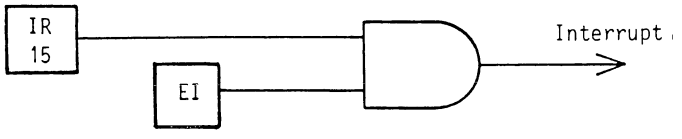
Bit	Name	Description
15	IR15 (read/write to zero)	Interrupt request from the input line 15. IR15 is set on the edge of the input signal according to the state of the bits ELE15 and ETE15. IR15 produces an interrupt on vector XX0 when EI is set.
14	EI (read/write)	Enable Interrupt for IR15.
13	ELE 15 (read/write)	Enable the Leading Edge (ON-going signal) from input line 15 to set IR15.
12	ETE 15 (read/write)	Enable the Trailing Edge (OFF-going signal) from input line 15 to set IR15.
8	TST IR (write only)	Test the Interrupt Request Bit IR15. Writing the TST IR sets the Bit IR15 to test the internal Interrupt Function.

Table 2-2: CSR Register Bit Assignment

CSR 171XX4 - Control Status Register

IR 15	EI	ELE 15	ETE 15				TST IR								
R/WZ	R/W						W								

Interrupt Generation



NOTE: R = Read Only
W = Write Only
R/W = Read/Write
R/WZ = read/write to zero with a "1"
All bits not described are unused and read or written as zero.

Figure 2-7: IDV1S-A Control Status Register / Interrupt Generation

2.5 FUNCTIONAL DESCRIPTION

2.5.1 Theory of Operation

Figure 2-1 shows a simple block diagram of the IDV1S-A. The board is addressed via the bus address lines. It has switches to select its device address and interrupt vector address according to the rules in chapter 2.3.

The 16 digital input data are entered through connector J1. They can be read by program via the input data buffer (DAT).

Each input enters via an optical isolator. Following each isolator is a contact bounce eliminator circuit to provide a high noise immunity.

2.5.2 Mode of Operation

Standard Input Range

The standard input range for all 16 digital inputs is 24 to 42 Vdc. This range is selected after INIT.

Low Level Input Range

This range can be selected by program with the mode register bit LLS (Bit 3). It is possible to use low voltage and low power signal sources, e.g. TTL and MOS at this input mode. However, the signals may only have a very low frequency. See chapter 2.2 "Specification".

Contact Bounce Eliminator

The contact bounce eliminator circuit takes an input signal from a bouncing contact and generates a clean digital signal four clock periods after the input is stabilized. The clock for operation is derived from a programmable R-C oscillator. The R-C oscillator can be programmed via the MOD-register bits RT0 and RT1 for the bounce delays 500 microsecs, 5 millisecs and 10 millisec. After INIT, the 5 msec delay is selected.

Interrupt on Input Line 15

The input line 15 can be programmed with the CSR register bits ELE 15 and ETE 15, such that an input change is stored in a flip-flop (CSR bit IR15) as follows:

ELE15 enable the leading edge or ON-going signal to set IR15.
ETE15 enable the trailing edge or OFF-going signal to set IR15.

An interrupt only occurs via bit IR15 when IE (CSR bit 14) is set.

2.5.3 User Input Signals

The IDV1S-A has a 50-pin D-type male connector for user inputs. A flat cable or a user made twisted pair cable could be used for field connection.

For a logical "1" input, the minus voltage has to be supplied at the INX/1 input pin and + voltage at the INX/2 input pin to drive the light emitting diode of the optocoupler.

For the correct electrical signal requirements, see chapter 2.2 "Specification".

NOTE

The +5V output on Pin 2 and 38 are normally used for DIGITAL manufacturing purposes.

I/O Connector Pin	Signal Name	I/O Connector Pin	Signal Name
1		2	+5V (Maint.)
3		4	IN0/1 (- Bit 0)
5	IN0/2 (+ Bit 0)	6	IN1/1
7	IN1/2	8	IN2/1
9	IN2/2	10	IN3/1
11	IN3/2	12	IN4/1
13	IN4/2	14	IN5/1
15	IN5/2	16	IN6/1
17	IN6/2	18	IN7/1
19	IN7/2	20	IN8/1
21	IN8/2	22	IN9/1
23	IN9/2	24	IN10/1
25	IN10/2	26	IN11/1
27	IN11/2	28	IN12/1
29	IN12/2	30	IN13/1
31	IN13/2	32	IN14/1
33	IN14/2	34	IN15/1 (-Bit 15)
35	IN15/2(+ Bit 15)	36	
37		38	+5Vdc Out(Manuf.
39		40	Gnd only)
41		42	
43		44	
45		46	
47		48	
49		50	

Table 2-3: IDV1S-A Connector J1 Pin Assignment (M5026-P0)

2.5.4 Interfacing to the IDV1S-A

In the following, some typical user circuits which drive the IDV1S-A inputs are shown:

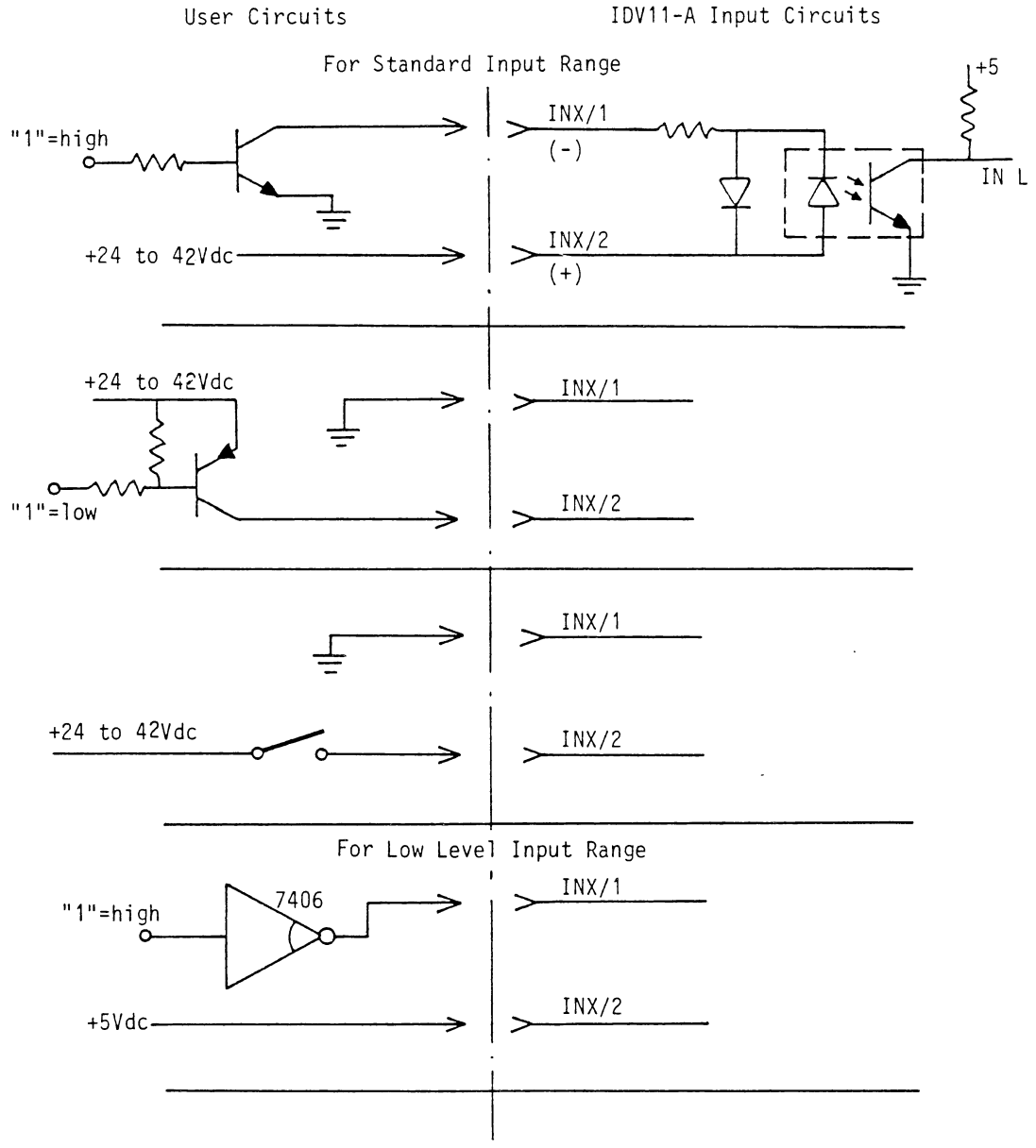


Figure 2-8: IDV1S-A Application Circuits (M5026-P0)

CHAPTER 3

IDV1S-B 16-BIT OPTO ISOLATED OUTPUT (M6029-P0)

3.1 GENERAL DESCRIPTION

The IDV1S-B is an isolated digital output module (M6029-P0) for the Q-bus. It provides 16 single optically isolated dc outputs. The latched field outputs are two-wire open-collector/ open-emitter switches used for controlling relays, indicators, semiconductor switches etc., where isolation from the controlled process must be maintained.

The 16-bit output data are written by program in word or byte and the output data register can be read back.

IDV1S-B FEATURES

- 16 single optically isolated outputs
- two wire connection per output
- capable of driving up to max. 42 Vdc at 130mA
- read/write output data register
- module identification code readable by program

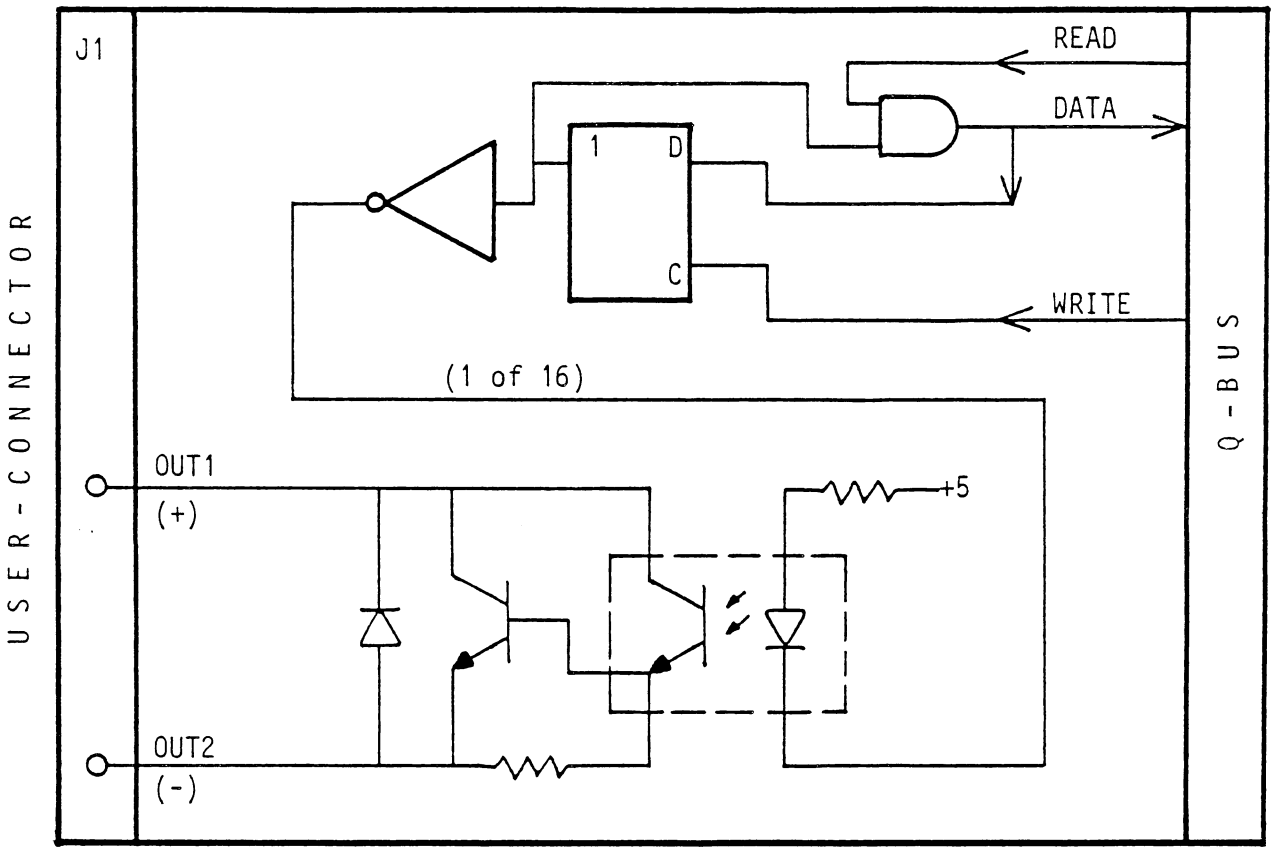


Figure 3-1: IDV1S-B Simple Block Diagram (M6029-P0)

3.2 SPECIFICATION

Module Designation	M6029-P0
Identification	040 octal (software identification code when reading the MOD register)
Module Size	Quad high Module (for BA200 enclosures)
Power	5,0 Vdc at 440mA ±5%
Bus Load	1 DC-load; 1,4 AC-load

OUTPUT CIRCUITS

No. of Outputs	16 two-wire darlington opto-coupler dc outputs
Output Voltage	42 Vdc
Max. Output Current*	130mA (Ptot = 150 milliwatts)
Saturation Voltage	Vce (sat) = Typical 0,85V at Ic 50mA (max. 1 V)
Switching Speeds	ON-Time typ. 6 microsecs OFF-Time typ. 120 microsecs (at Vce = 5V, Rl = 100 ohm)
Isolation Voltage	Output to Computer Gnd 1000 Vdc or peak AC
Interchannel Isolation	250 Vdc or peak AC
Logic "1" Output	Transistor ON (conducting)

* Derate 2 mW/ degrees centrigrade above 25 degrees centigrade ambient

BUS INTERFACE

Register Addressing	Switch selectable over the 4K I/O address range, occupies a four word address with two words unused

3.3 INSTALLATION

3.3.1 Site Consideration

The IDV1S-B has two bus interface connectors that plug into a Q-bus slot. These connectors have signals defined by the Q-bus specification. The module can be plugged into any slot of a Q-bus backplane according to the rules of the Q-bus system configuration.

3.3.2 Interconnection

Interfacing the IDV1S-B to the user's device is done via the 50-pin D-type male connector. A 50-conductor flat cable or a user made twisted pair cable may be used for field connection. The pin assignmnent and the signal description are shown in chapter 3.5.
General information about the user I/O-connector and the physical requirements are given in chapter 1.4.6.

3.3.3 Initial Operation

Selecting the IDV1S-B Device Address

The device address is the I/O address assigned to the MOD-register. The device address is selected via a 10-pole switch (see figure 3-3). The switches allow the device address to be set within a range of 160000 octal to 177770 octal. The standard address range for this module is from 171000 to 171370 octal in increments of 10 octal.

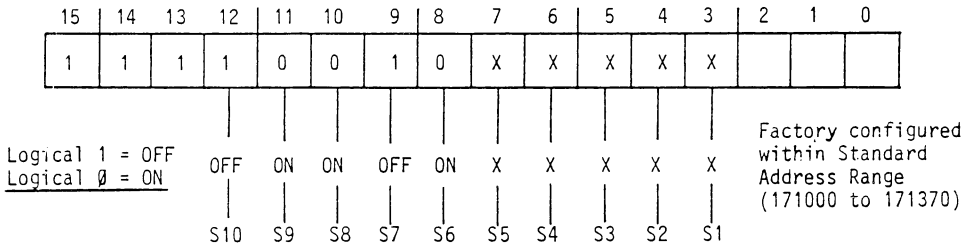


Figure 3-2: Selecting IDV1S-B Device Address

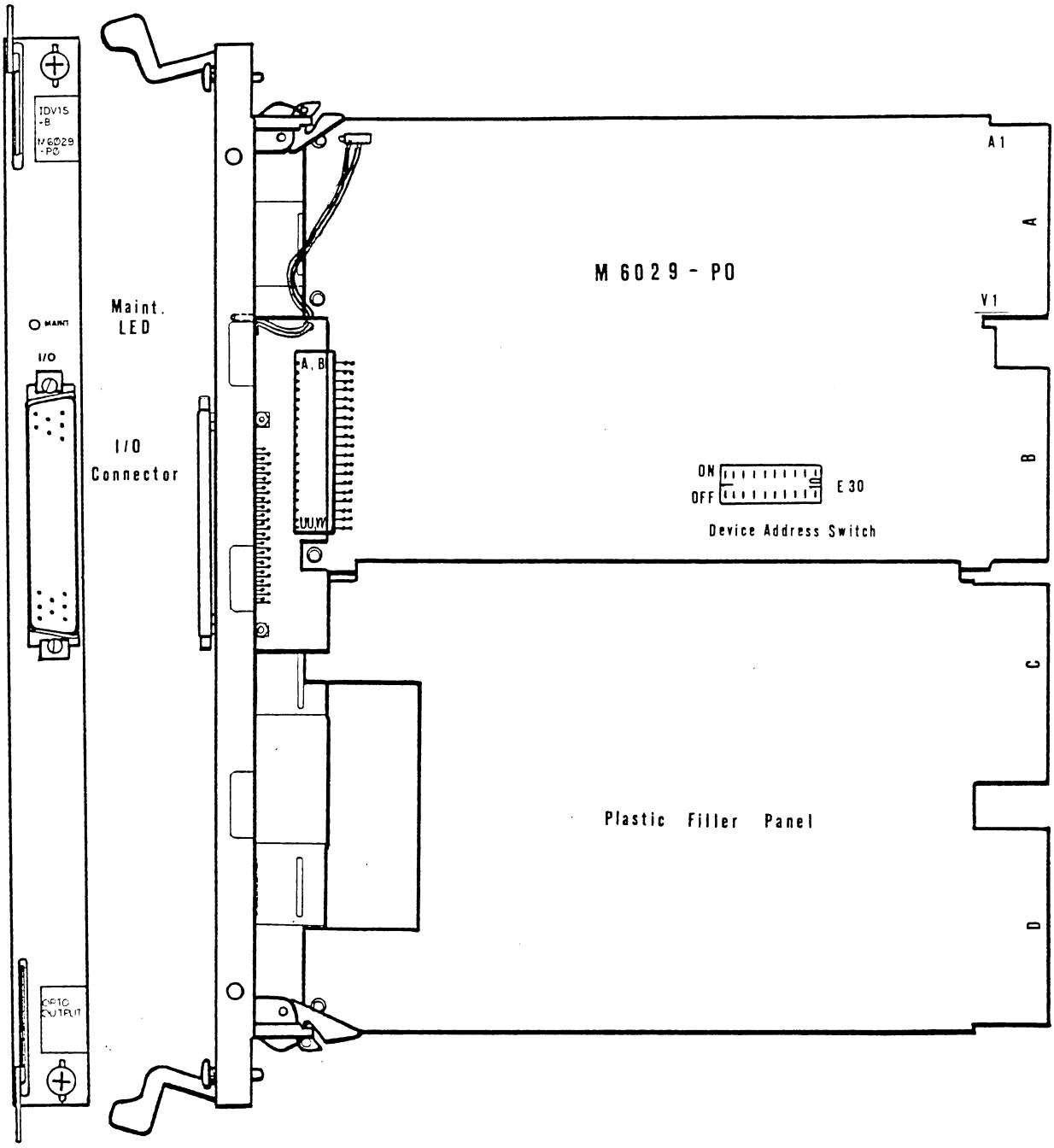


Figure 3-3: IDV1S-B Physical Layout M6029-P0

3.4 OPERATION AND PROGRAMMING

3.4.1 General

This chapter presents a detailed description of the IDV1S-B resgisters (see figure 3-4). Four consecutive bus addresses are assigned to the register set.

171XX0	Mode Register	(MOD)
171XX2	Output Data Register	(DAT)
171XX4	unused	
171XX6	unused	

They can be read or loaded using any instruction that refers to their address.

Initialization

The mnemonic INIT refers to the initialization signal issued by the processor. Initialization is caused by one of the following:

- issuing a programmed RESET instruction
- depressing the start switch on the processor console
- the occurrence of a power-up or power-down sequence

The MOD and the DAT register are then initialized. All 16 output lines are set to logical "0" (transistor OFF).

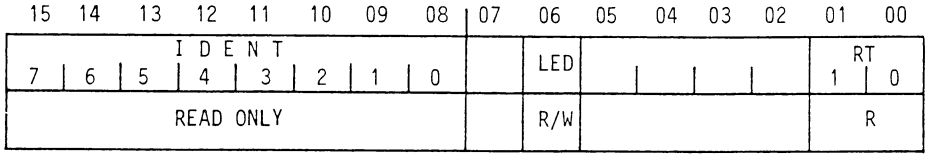
3.4.2 Mode Register (MOD)

The MOD register is generally used to identify the module with its identification code and for maintenance purposes.

Bit	Name	Description
15 to 8	IDENT 7 to IDENT 0 (read only)	Identification Bits 7-0. The module is identified by these bits. The M6029 has the code 040 octal (in high byte).
6	LED (read/write)	LED indication for test purposes.
1	RT 1	Response Time Bits 0-1
0	RT 0 (read only)	Switching time of the 16 output circuits (diagnostic feature). RT0 is always set since the ON or OFF time could be up to 500 micro-sec. RT1 is always zero.

Table 3-1: IDV1S-B MOD-Register Bit Assignments

MOD 171XX0 - Mode Register



NOTE: R = Read Only
W = Write Only
R/W = Read/Write
All bits not described are unused and read or write as zero

Figure 3-4: IDV1S-B Mode Register

3.4.3 Output Data Register (DAT)

The output data register is a 16-bit read/write register. It can be written by word or byte. The read back data only shows the contents of the DAT and not the status of the output circuits.

DAT 171XX2 - Output Data Register

ODAT								ODAT							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
READ/WRITE								READ/WRITE							

Figure 3-5: IDV1S-B Output Data Register

3.5 FUNCTIONAL DESCRIPTION

3.5.1 Theory of Operation

Figure 3-1 shows a simple block diagram of the IDV1S-B. It is addressed via the Q-bus address lines. The board has a 10-pole DIL switch to select its device address according to the rules in chapter 3.3.

The output data are loaded in the 16-bit output register (DAT). The DAT outputs drive the darlington optocouplers. The collector and emitter of the darlington switches goes to the field connector J1. Each of these switches is protected from inductive spikes by a clamp diode across its output.

The output data remain unchanged unless the processor outputs new data to the DAT-register.

3.5.2 User Output Signals

The IDV1S-B has a 50-pin D-type male connector for the output signals to the user. A flat cable or a user made twisted pair cable may be used for field connection.

A logical "1" output means the darlington output switch is ON (conducting).

For the correct electrical signal requirements, see chapter 3.2 "Specification".

NOTE

The +5V output on Pin 38 is normally used for DIGITAL manufacturing purposes.

I/O Connector. Pin	Signal Name	I/O Connector. Pin	Signal Name
1	Gnd	2	
3		4	OUT0/1 (+ Bit 0)
5	OUT0/2 (- Bit 0)	6	OUT1/1
7	OUT1/2	8	OUT2/1
9	OUT2/2	10	OUT3/1
11	OUT3/2	12	OUT4/1
13	OUT4/2	14	OUT5/1
15	OUT5/2	16	OUT6/1
17	OUT6/2	18	OUT7/1
19	OUT7/2	20	OUT8/1
21	OUT8/2	22	OUT9/1
23	OUT9/2	24	OUT10/1
25	OUT10/2	26	OUT11/1
27	OUT11/2	28	OUT12/1
29	OUT12/2	30	OUT13/1
31	OUT13/2	32	OUT14/1
33	OUT14/2	34	OUT15/1(+ Bit 15)
35	OUT15/2(-Bit 15)	36	
37		38	+5Vdc Out (Manuf.
39		40	Gnd only)
41		42	
43		44	
45		46	
47		48	
49		50	

Table 3-2: IDV1S-B Connector J1 Pin Assignment M6029-P0

3.5.3 Interfacing to the IDV1S-B

In the following, some typical user circuits, which can be driven from the IDV1S-B outputs, are shown.

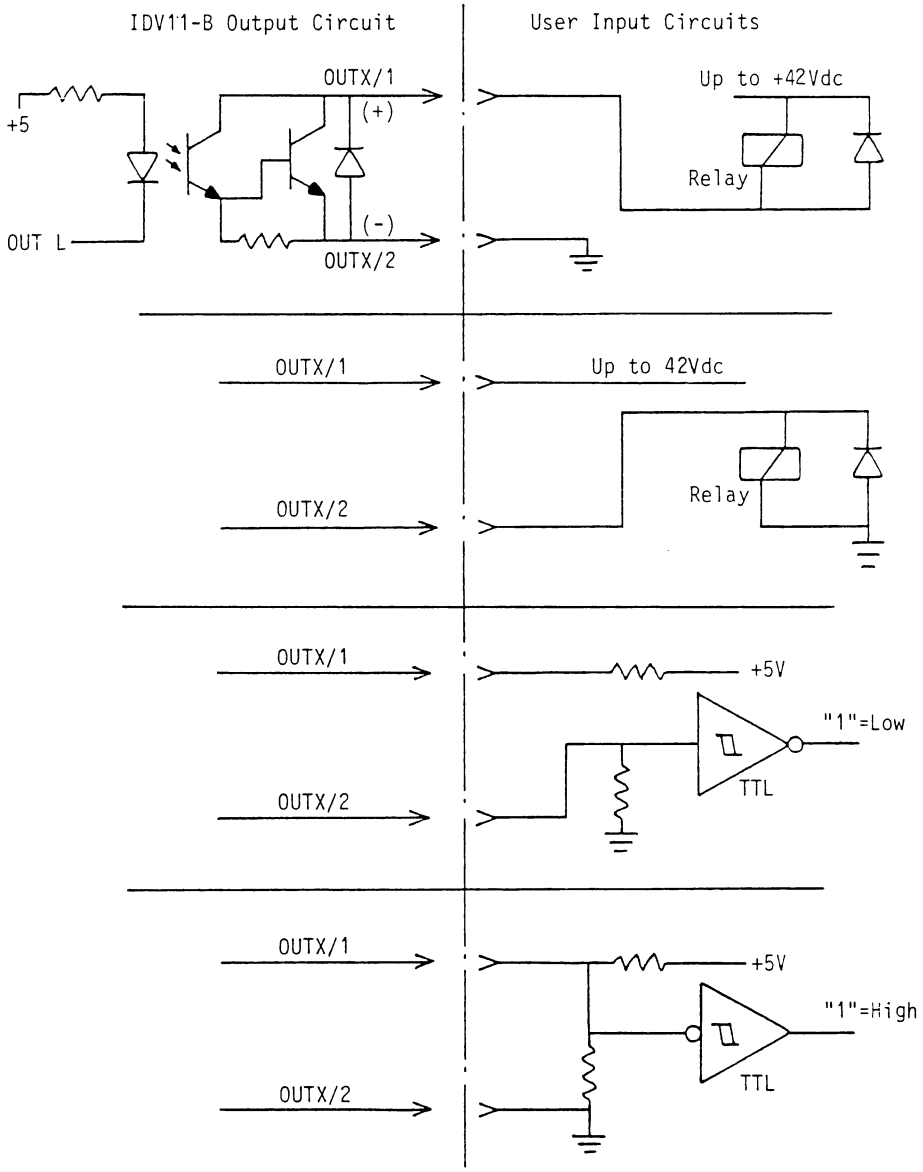


Figure 3-6: IDV1S-B Application Circuits M6029-P0

CHAPTER 4

IDV1S-C 16-BIT RELAY OUTPUT (M8005-P0)

4.1 GENERAL DESCRIPTION

The IDV1S-C is a relay output module (M8005-P0) for the Q-bus. It provides 16 latched reed contact outputs. The outputs are two-wire normally open contacts, used for controlling solenoids, relays, indicators, etc., where isolation from the controlled process must be maintained.

The 16-bit output data are written by program in word or byte and the output data register can be read back.

IDV1S-C FEATURES:

- 16 normally open reed contact outputs
- two-wire connection per output
- capable of driving up to 42 volt dc (or peak ac) 1A; Pmax. 30W/42VA
- contact protection
- read/write output data register
- module identification code readable by program

4.2 SPECIFICATION

Module Designation	M8005-P0
Identification	042 octal (identification code when reading the MOD register
Module Size	Quad high Module (for BA200 enclosures)
Power	5,0 Vdc ±5% at 760mA
Bus Load	1 DC-Load; 2,1 AC-Load

OUTPUT CHARACTERISTICS

No. of Outputs	16 two-wire reed contact outputs
Contact Form	SPST normally open Contact with contact protection
Contact Resistance	Typ. 0,2 ohm across the output pins
Switching Voltage	42 volt dc (or peak ac) maximum
Switching Current	1 A maximum; Note: above 0,2A, life expectancy is derated.
Maximum Wattage	30W (dc) or 42VA (ac)
Response Time	Typ. 1 millisec
Life Expectancy	>100 000 000 operations at 0,2A/12V
Isolation Voltage	Output to computer Gnd 1000 Vdc or peak ac
Interchannel Isolation	250 Vdc or peak ac
Switching Rate	400 Hz maximum
Logic "1" Output	Contact closed

BUS INTERFACE

Register Addressing	Switch selectable over 4K I/O area, 4 word addresses of which two words are unused

4.3 INSTALLATION

4.3.1 Site Consideration

The IDV1S-C has two bus interface connectors that plug into a Q-bus slot. These connectors have signals defined by the Q-bus specification. The module can be plugged into any slot of a Q-bus backplane according to the rules of the Q-bus system configuration.

4.3.2 Interconnection

Interfacing the IDV1S-C to the users's device is done via the 50-pin D-type male connector. A 50-conductor flat cable or a user made twisted pair cable may be used for field connection. The pin assignment and the signal description are shown in chapter 4.5.
General information about the user I/O-connector and the physical requirements are given in chapter 1.4.6.

4.3.3 Initial Operation

Selecting the IDV1S-C Device Address

The device address is the I/O address assigned to the MOD-register. The device address is selected via a 10-pole switch (see figure 4-3). The switches allow the device address to be set within a range of 160000 octal to 177770 octal. The standard address range for this module is from 171000 to 171370 octal in increments of 10 octal (see Figure 4-2).

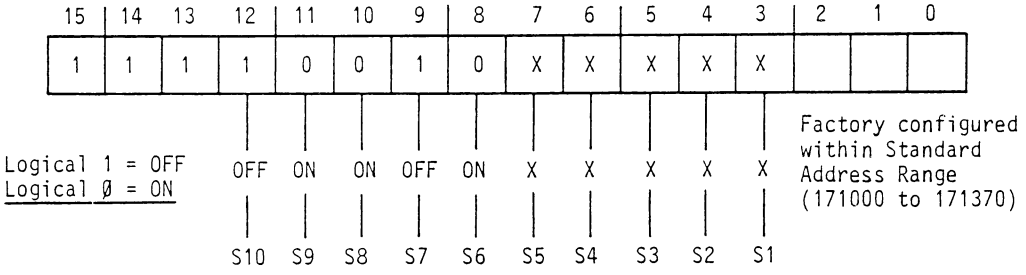


Figure 4-2: Selecting IDV1S-C Device Address

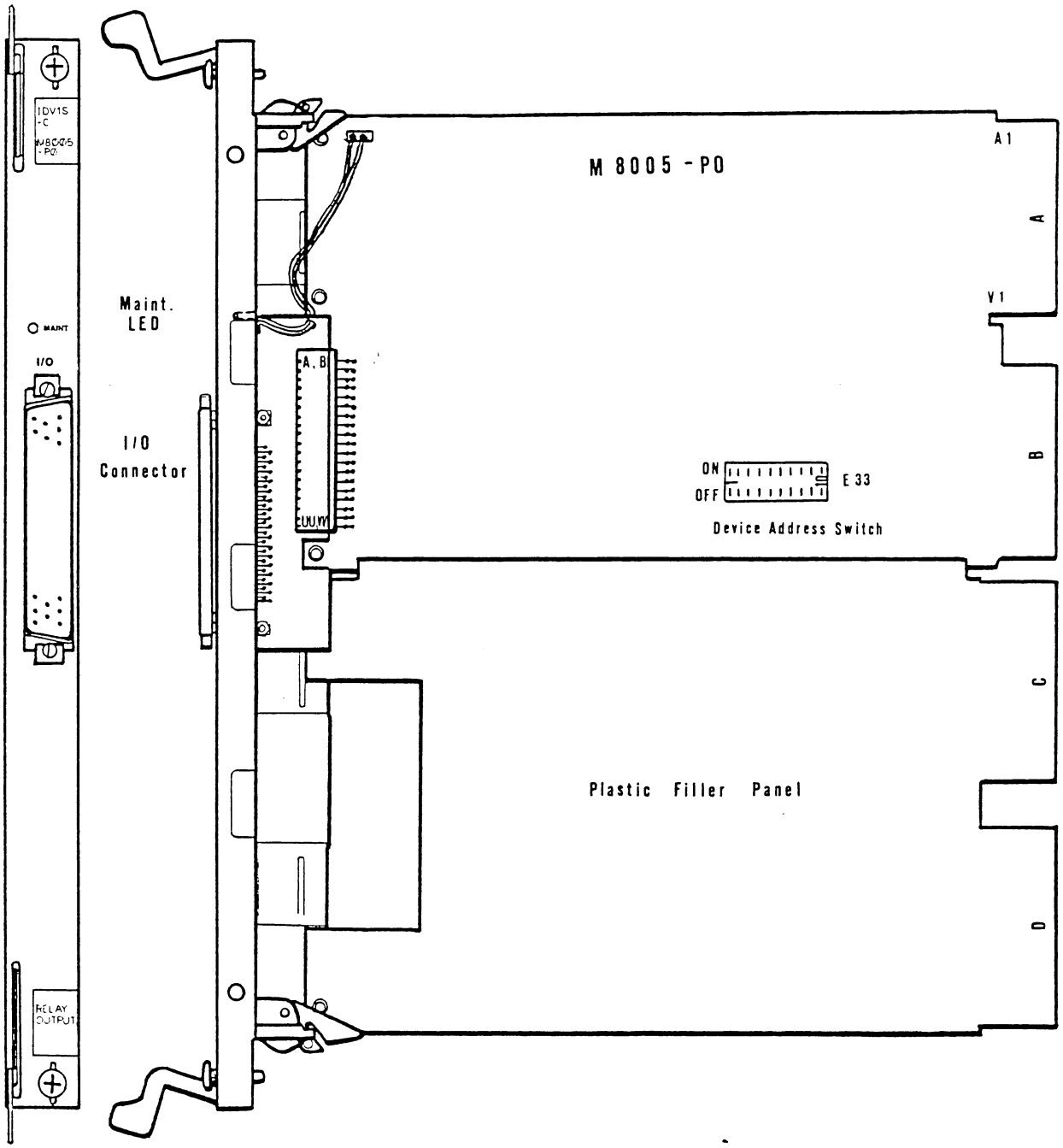


Figure 4-3: IDV1S-C Physical Layout M8005-P0

4.4 OPERATION AND PROGRAMMING

4.4.1 General

This chapter presents a detailed description of the IDV1S-C registers (see figures 4-4 to 4-6). Four consecutive bus addresses are assigned to the register set.

171XX0	Mode Register	(MOD)
171XX2	Output Data Register	(DAT)
171XX4	unused	
171XX6	unused	

They can be read or loaded using any instruction that refers to their address.

Initialization

The mnemonic INIT refers to the initialization signal issued by the processor. Initialization is caused by one of the following:

- issuing a programmed RESET instruction
- depressing the start switch on the processor console
- the occurrence of a power-up or power-down sequence

The MOD and the DAT register are then initialized. All 16 output lines are set to logical "0" (contact open).

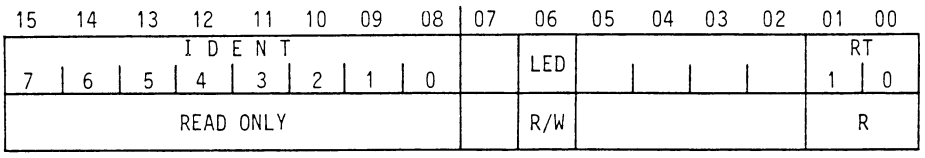
4.4.2 Mode Register (MOD)

The MOD register is generally used to identify the module with its identification code and for maintenance purposes.

Bit	Name	Description
15 to 8	IDENT 7 to IDENT 0 (read only)	Identification Bits 7-0. The module is identified by these bits. The M8005 has the code 042 octal (in high byte).
6	LED (read/write)	LED indication for test purposes.
1	RT 1	Response Time Bits 0,1
0	RT 0 (read only)	Switching time of the 16 output circuits (diagnostic feature). RT1 is always set since the ON or OFF switching time could be up to 5 msec. RT0 is always zero.

Table 4-1: IDV1S-C MOD-Register Bit Assignments

MOD 171XX0 - Mode Register



NOTE: R = Read Only
W = Write Only
R/W = Read/Write
All bits not described are unused and read or write as zero

Figure 4-4: IDV1S-C Mode Register

4.4.3 Output Data Register (DAT)

The output data register is a 16-bit read/write register. It can be written by word or byte. The read back data only shows the contents of the DAT and not the status of the output circuits.

DAT 171XX2 - Output Data Register

ODAT								ODAT							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
READ/WRITE								READ/WRITE							

Figure 4-5: IDV1S-C Output Data Register

4.5 FUNCTIONAL DESCRIPTION

4.5.1 Theory of Operation

Figure 4-1 shows a simple block diagram of the IDV1S-C. It is addressed via the LSI-11 bus address lines. The board has a 10-pole DIL switch to select its device address according to the rules in chapter 4.3.

The output data are loaded in the 16-bit output register (DAT). The DAT outputs drive the relay coil. Both sides of the SPST-NO read contacts go to the field connector J1. Each of these contacts is protected from inductive loads by a RC-network across its output.

The output data remain unchanged unless the processor outputs new data to the DAT register.

4.5.2 User Output Signals

The IDV1S-C has a 50-pin D-type male connector for the output signals to the user. A flat cable or a user made twisted pair cable could be used for field connection.

A logical "1" output means the reed contact is closed.

For the correct electrical signal requirements, see chapter 4.2 "Specification".

NOTE

The +5V output on Pin 38 is normally used for DIGITAL manufacturing purposes.

I/O Connector Pin	Signal Name	I/O Connector Pin	Signal Name
1	Gnd	2	
3		4	OUT0/1 (Bit 0)
5	OUT0/2 (Bit 0)	6	OUT1/1
7	OUT1/2	8	OUT2/1
9	OUT2/2	10	OUT3/1
11	OUT3/2	12	OUT4/1
13	OUT4/2	14	OUT5/1
15	OUT5/2	16	OUT6/1
17	OUT6/2	18	OUT7/1
19	OUT7/2	20	OUT8/1
21	OUT8/2	22	OUT9/1
23	OUT9/2	24	OUT10/1
25	OUT10/2	26	OUT11/1
27	OUT11/2	28	OUT12/1
29	OUT12/2	30	OUT13/1
31	OUT13/2	32	OUT14/1
33	OUT14/2	34	OUT15/1 (Bit 15)
35	OUT15/2 (Bit 15)	36	
37		38	+5Vdc Out (Manuf.
39		40	Gnd only)
41		42	
43		44	
45		46	
47		48	
49		50	

Table 4-2: IDV1S-C Connector J1 Pin Assignment M8005-P0

4.5.3 Interfacing to the IDV1S-C

In the following, some typical user circuits, which can be driven from the IDV1S-C outputs, are shown.

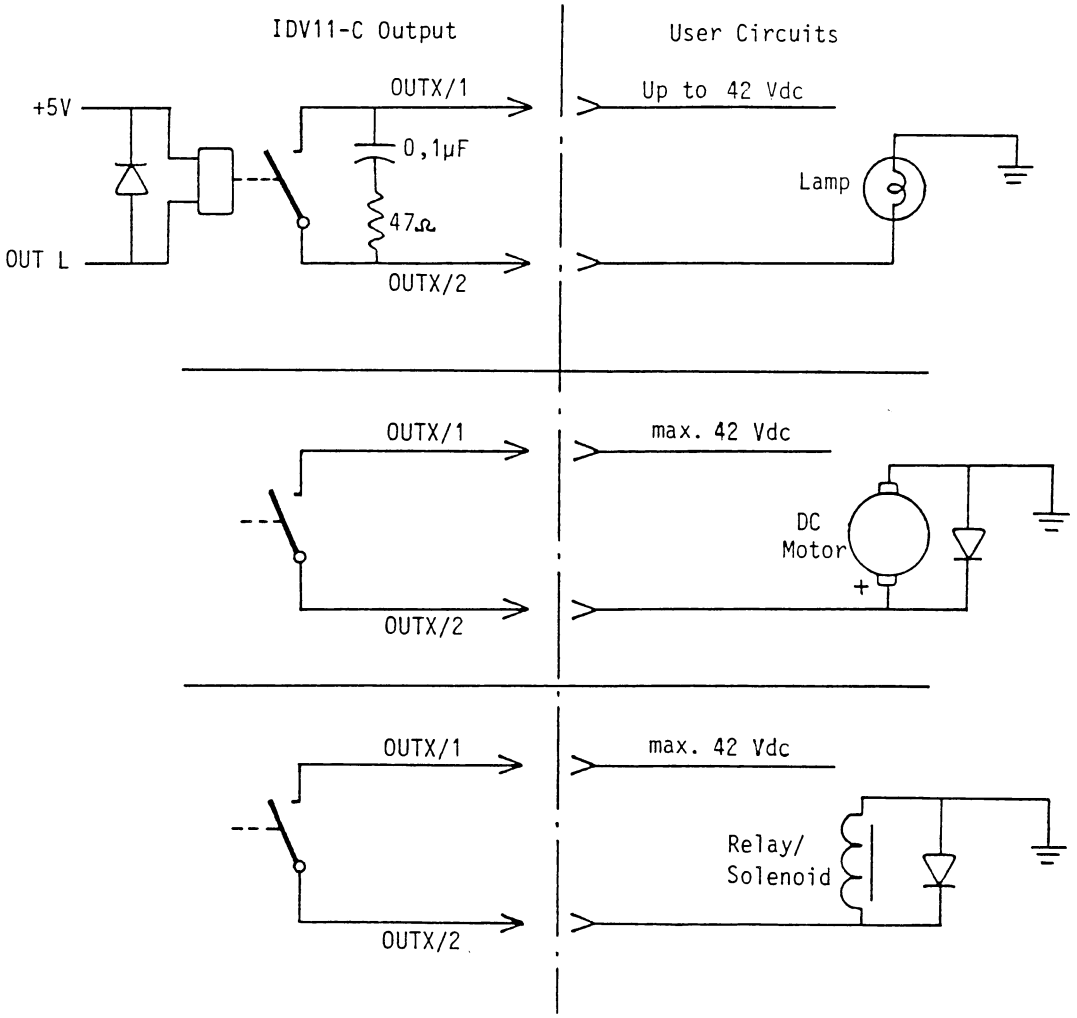


Figure 4-6: IDV1S-C Application Circuits (M8005-P0)

CHAPTER 5

IAV1S-B 4-CHANNEL ISOLATED D/A CONVERTER (A6007-P0)

5.1 GENERAL DESCRIPTION

The IAV1S-B is a four channel group isolated digital to analogue converter module (A6007-P0) for the Q-bus.

It offers a choice of voltage and current outputs. The current outputs are self-powered and selectable by a mode-plug for 0-20mA or 4-20mA.

Each DAC has a double buffer register that provides 12-bit input data resolution. The DAC registers are written by program in word format.

The double buffer DAC registers can be simultaneously latched to the DAC's with an external control signal, if the process requires this.

The digital data and the control signals are transmitted to the four DAC's through optical couplers that isolate the analogue circuits from the computer. The analogue power for the DAC circuits is produced by an isolated DC/DC converter (see figure 5-1 IAV1S-B Block Diagram).

IAV1S-B Features

- Four group isolated D/A converters
- 12 bit resolution
- Voltage output 0 to +10V
- Current output, selectable for 0 to 20mA or 4 to 20mA
- Software identification of open 20mA outputs
- Input signal for simultaneous latching of the DAC registers
- Module identification code readable by program

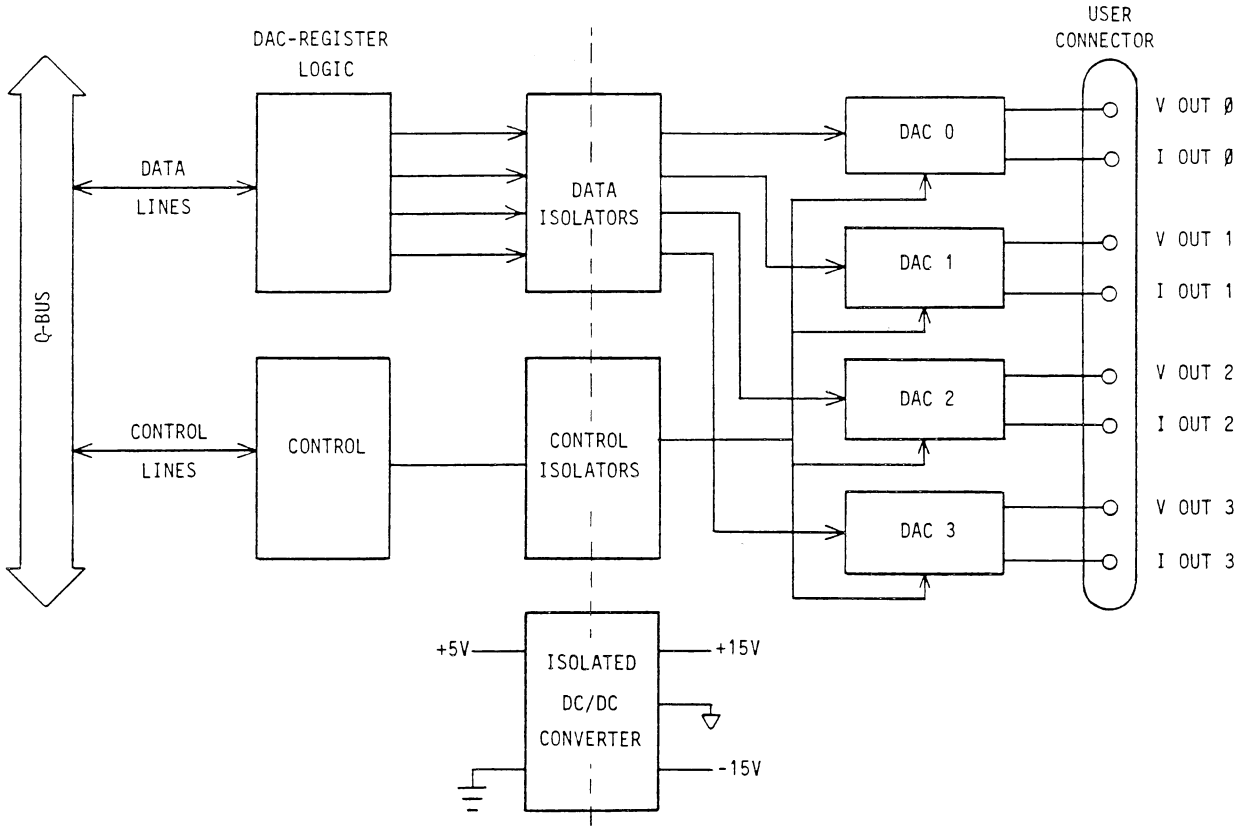


Figure 5-1: IAV1S-B Simple Block Diagram (A6007-P0)

5.2 SPECIFICATION

Module Designation	A6007-P0
Identification	200 octal, (identification code when reading the MOD register)
Size	Quad high Module (for BA200 enclosure)
Power	+5Vdc ±5% at 1,5A
Bus Load	1 DC-Load; 1,4 AC-Load

OPERATIONAL

No of Analogue Outputs	4 (group isolated)
Resolution	12-Bit (1 part in 4096)
DAC Digital Inputs	12-Bits binary encoded
DAC Digital Storage	Write Only Register in Word Operation
Response Time	between 1 and 150 microsecs (serial load sequence of DAC)
Isolation Voltage	Analogue Outputs to Computer Gnd 500 Vdc

CURRENT OUTPUT CHARACTERISTICS

Range (plug selectable)	4 to 20mA; LSB = 3,9 microamp 0 to 20mA; LSB = 4,88 microamp
Offset	Adjustable per channel
Maximum Load Resistance	500 Ohm
Gain Accuracy	Adjustable per channel
Gain Temp. Coefficient	30 ppm of FSR/degree celsius
Offset Temp. Coefficient	0,4 microamps/degree celsius
Integral Non-linearity	± 2 LSB maximum
Differential Non-linearity	± 2 LSB maximum

Monotonicity	12 Bits
Slew Rate	1,2 milliamps/microsec

VOLTAGE OUTPUT CHARACTERISTICS

Range	0 to +10V
LSB	2,4 mV
Maximum Output Current	5mA (short circuit protected to Ground)
Gain Accuracy	Adjustable per channel
Offset	Adjustable per channel
Gain Temperature Coefficient	30 ppm of FSR/Degrees celsius
Integral Non-linearity	± 1,5 LSB maximum
Differential Non-linearity	± 1,5 LSB maximum
Monotonicity	12 Bits
Slew Rate	0,6 V/microsec

BUS INTERFACE

Register Addressing	Switch selectable over 4K - I/O address area, occupies 4 word addresses with 1 word unused.

5.3 INSTALLATION

5.3.1 Site Consideration

The IAV1S-B has two bus interface connectors that plug into Q-bus slot. These connectors have signals defined by a Q-bus specification. The module can be plugged into any slot of a Q-bus backplane according to the rules of the Q-bus system configuration.

5.3.2 Interconnection

Interfacing the IAV1S-B to the user's device is done via the 50-pin D-type male connector. A 50-conductor flat cable or a user made twisted pair cable may be used for field connection. The pin assignment and the signal description are shown in chapter 5.5.
General information about the user I/O-connector and the physical requirements are given in chapter 1.4.6.

5.3.3 Initial Operation

Selecting the IAV1S-B Device Address

The device address is the I/O address assigned to the MOD-register. The device address is selected via a 10-pole switch (see figure 5-3). The switches allow the device address within a range of 160000 octal to 177770 octal to be set.

The standard address range for this module is recommended from 171000 to 171370 in increments of 10 octal (see Figure 5-2).

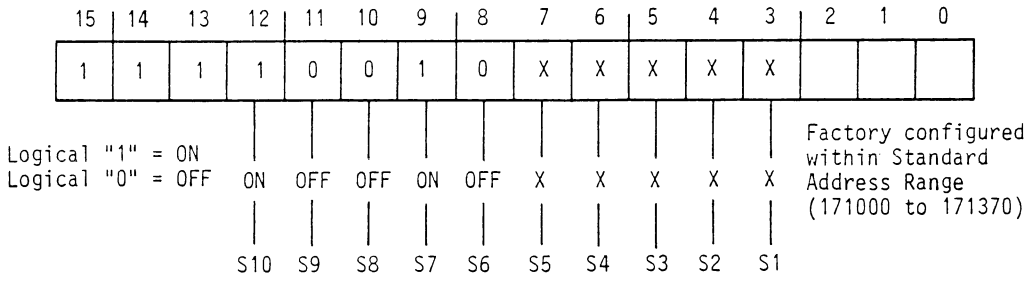


Figure 5-2: Selecting IAV1S-B Device Address

Selecting the Current Output Modes

The current output mode for all four DAC's is selected by a 20-pin DIL plug.

Pin 1 plug to pin 1 socket = 4 to 20mA output
Pin 1 plug to pin 11 socket = 0 to 20mA output

The IAV1S-B is normally shipped with the calibration of 0 to 20mA outputs. If the voltage or the 4 to 20mA outputs are used, a new calibration is necessary. See chapter 5.5.3.

The state of this plug can be identified by software in the MOD-register.

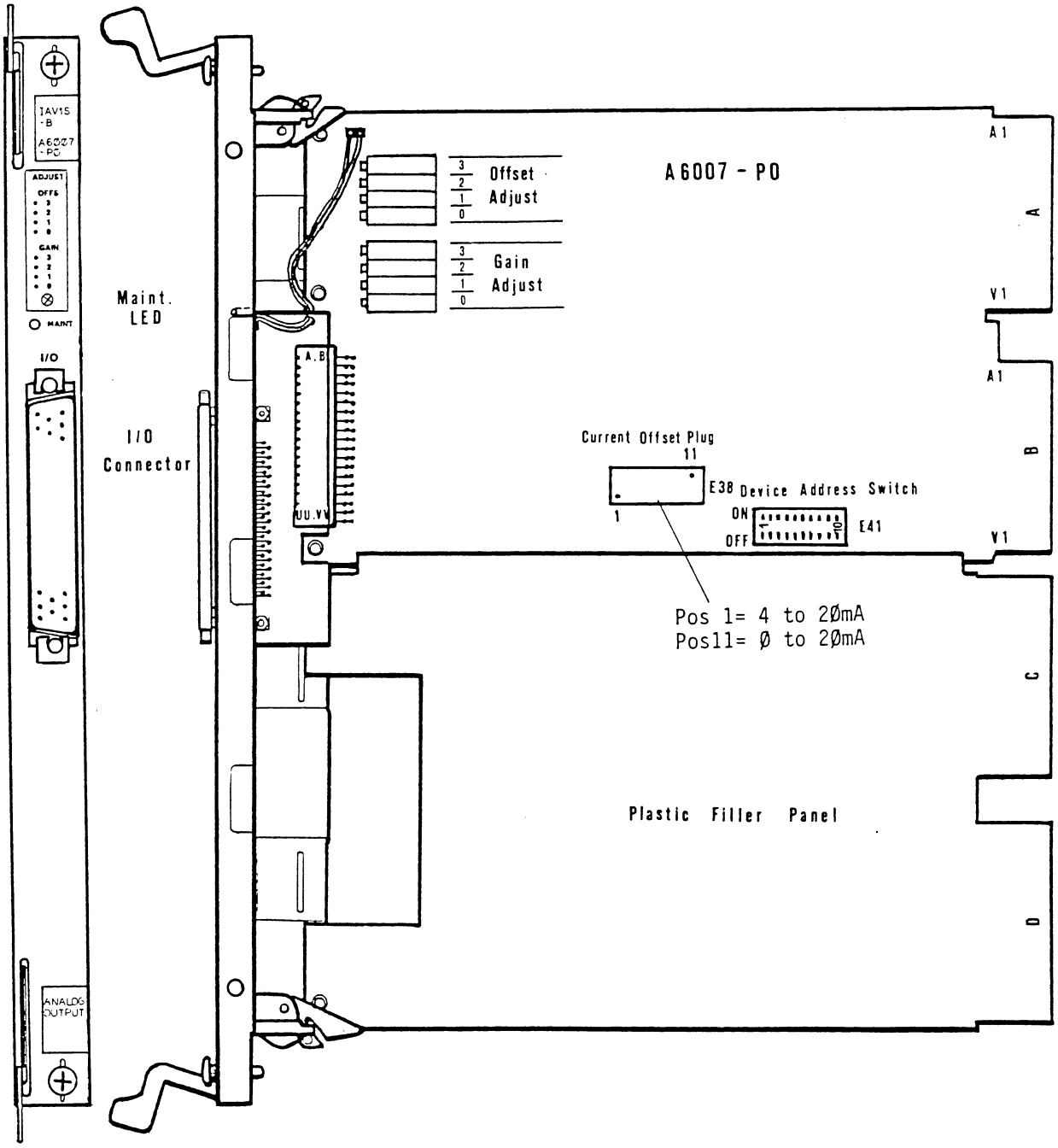


Figure 5-3: IAV1S-B Physical Layout (A6007-P0)

5.4 OPERATION AND PROGRAMMING

5.4.1 General

This chapter presents a detailed description of the IAV1S-B register (see figures 5-4 to 5-6). Four consecutive bus addresses are assigned to the register set.

171XX0	Mode Register	(MOD)
171XX2	DAC Data Register	(DAT)
171XX4	Control Status Register	(CSR)
171XX6	unused	

These can be read or loaded using any instruction that refers to their addresses.

Initialization

The mnemonic INIT refers to the initialization signal issued by the processor. Initialization is caused by one of the following:

- issuing a programmed RESET instruction
- depressing the start switch on the processor console
- the occurrence of a power-up or power-down sequence

The MOD, DAT and CSR registers are then initialized.

Operation Modes:

The current output mode of the four DAC's is the only mode which can be changed by a DIL-plug on the module. The current outputs can be selected between 0 to 20mA and 4 to 20mA.

The position of the current mode plug is readable in the MOD register. When the COFS-bit (current output offset) is set, the 4 to 20mA output range is selected.

Execution of a D/A Conversion

A digital-to-analogue conversion is performed for each DAC in the following steps:

- Check that the READY flag is set
- Load the channel address bit CH0,1 for the desired DAC
- Write the DAC data to the DAT register

The DAC data are now transferred by an internal load cycle to the DAC circuit. During this time of between 1 and 150 microsecs, the READY is cleared and the DAT register cannot be loaded again.

5.4.2 Mode Register (MOD)

The MOD register is generally used to identify the module with its identification code and for maintenance purposes.

Bit	Name	Description
15 to 8	IDENT 7 to IDENT 0 (read only)	Identification Bits 7-0. The module is identified by these bits. The A6007 has the code 200 octal (in high byte).
6	LED (read/write)	LED indication for test purposes.
3	COFS (read only)	Current Output Offset This bit reads the position of the current output configuration plug. If COFS is set, the 4 to 20mA output range of all four DAC's is selected. Otherwise the 0 to 20mA range is on.

Table 5-1: IAV1S-B MOD Register Bit Assignments

MOD 171XX0 - Mode Register

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
IDENT									LED			COFS			
7	6	5	4	3	2	1	0								
READ ONLY									R/W			R			

NOTE: R = Read Only
W = Write Only
R/W = Read/Write
All bits not described are unused and read or write as zero

Figure 5-4: IAV1S-B Mode Register

5.4.3 DAC Data Register (DAT)

The DAT register is a 12-bit write only register. It can only be loaded by word instruction. After loading the DAT register, the data is transferred to DAC circuits by an internal load sequence. The data code for the DAC's is binary code. Refer to the Coding Table in chapter 5.5.

DAT 171XX2 - DAC Data Register

	(MSB) DA DAT (LSB)										
	11	10	09	08	07	06	05	04	03	02	01	00
	WRITE ONLY											

NOTE: R = Read Only
W = Write Only
R/W = Read/Write
All bits not described are unused and read or write as zero

Figure 5-5: IAV1S-B DAC Data Register

5.4.4 Control Status Register (CSR)

The CSR is a 16-bit read/write register. It can be written in word or byte format. The bit definitions are described in Table 5-2.

Bit	Name	Description
15	CHAVAI (read only)	Channel Available. This bit is set when the channel addressed by the CHA-bits is in the system.
9	CHA 1	Channel Address
8	CHA 0 (read/write)	Binary addressing of the DAC's which should be loaded via the DAT-register.
7	READY (read only)	Ready to write the DAT-register READY is cleared for between 1 and 150 microsecs after the DAT has been loaded. The next write to the DAT can be done when the READY is set again.
5	OPL (read only)	Open Line at 20mA Outputs OPL is set when the addressed channel is not connected. This means that the 20mA output line is broken or not used. In the 0 to 20mA output range, OPL is only detected if the output is greater than 5 LSB.
4	FNCT (read/write)	The Function Bit is present as TTL output signal. It has non-internal meaning. This bit is unused and for future expansion.

Table 5-2: IAV1S-B CSR Register Bit Assignment

CSR 171XX4 - Control Status Register

CH AVAI								CH 1	CH 0	READY		OPL	FNCT				
R								R/W		R		R	R/W				

NOTE: R = Read Only
W = Write Only
R/W = Read/Write

All bits not described are unused
and read or write as zero

Figure 5-6: IAV1S-B Control Status Register

5.5 FUNCTIONAL DESCRIPTION

5.5.1 Theory of Operation

Figure 5-1 shows a simple block diagram of the IAV1S-B. It is addressed via the LSI-11 bus address lines. The board has a 10-pole DIL switch to select its device address according to the rules in chapter 5.3.

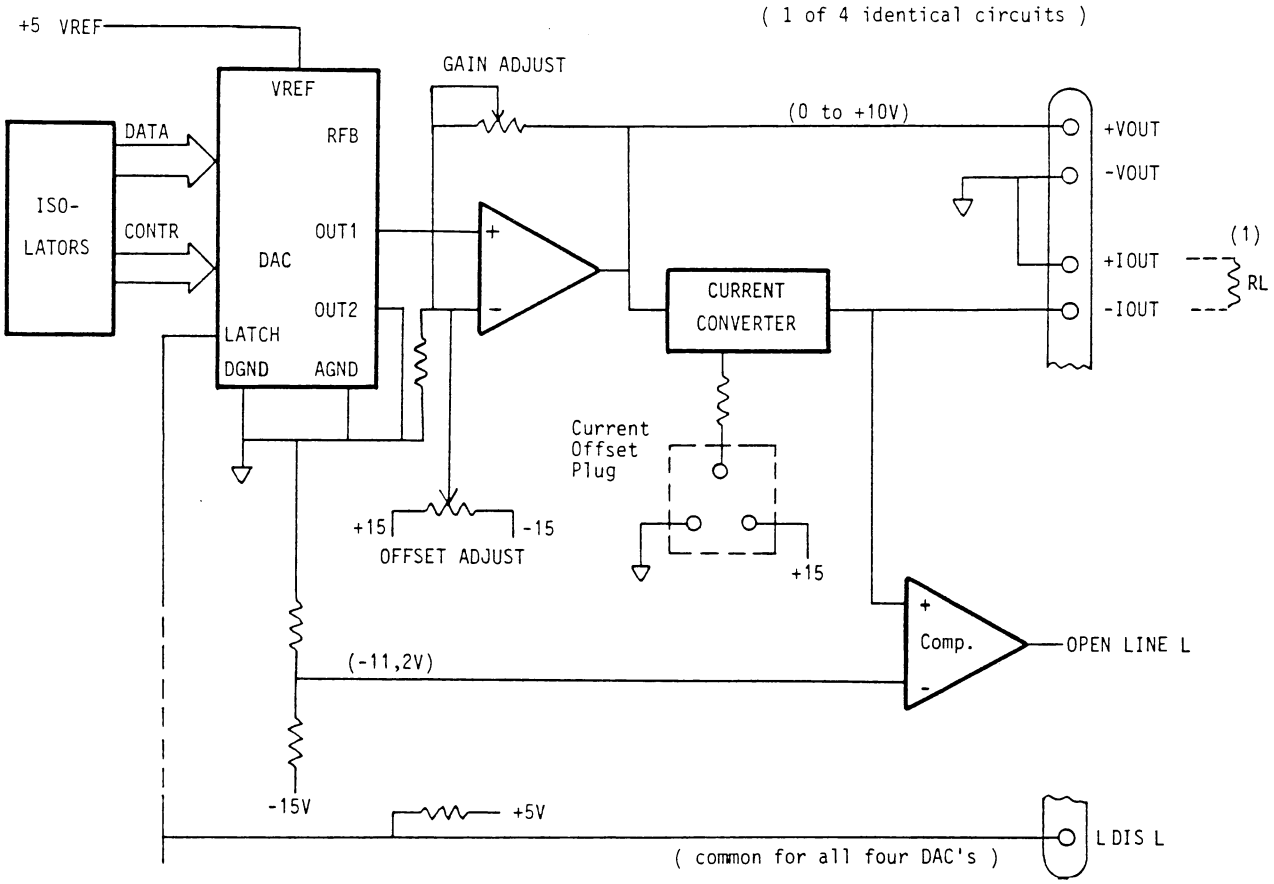
The four DAC's are monolithic 12-bit multiplying D/A converters, which are isolated from the computer with opto couplers and a DC/DC converter.

The DAC-data are stored in four 12-bit registers on the computer side. These registers are permanently updated to the internal double buffer registers of the DAC-IC's by a sequential register load logic.

Each DAC-IC is loaded in two steps. First the 8 MSB's are loaded to the DAC input latch and after loading the other 4 LSB's, all 12 bits are gated to the DAC holding register.

A comparator on each DAC-current output circuit monitors the -IOUT line. The comparator gives an "Open Line" signal to CSR-register when the voltage at this output is greater than -11,2V (see figure 5-7). To detect open lines in the 0 to 20mA Output Range, at least 5 LSB must be set.

The four DAC circuits have separate voltage and current outputs, but they cannot be used at the same time. The calibration per channel can only be done either for voltage or for current outputs, but not for both.



NOTE (1): RL max for the current outputs is 500 ohm.
The equivalent voltage is then 10V at 20mA.

Figure 5-7: IAV1S-B DAC-Circuit (A6007-P0)

5.5.2 Mode of Operation

Current Output Modes

The current outputs for all four DAC's can be selected by a 20-pin DIL plug in two modes.

Pin 1 plug to pin 1 socket = 4 to 20mA output
Pin 1 plug to pin 11 socket = 0 to 20mA output

The current offset plug is always installed on the board (see figure 5-3) and its position is readable by the COFS-bit in the MOD register.

DAC Register Latch Control

With the input signal Latch Disable (L DIS L), all four DAC-IC's holding registers can be latched simultaneously.

Normally, the L DIS L-signal is not used and not connected by the user and the DAC holding register is directly loaded by the programmed load instruction.

If the external L DIS L signal is connected and changed from low to high (min 150 microsecs), the contents of the four DAC input latches are loaded simultaneously into the DAC's, and therefore the DAC outputs will be changed at the same time.

D/A Converter Coding

The DAC registers are loaded with 12-bit (4096 states) binary code.

The analogue outputs operate in unipolar operation with the ranges listed in the following coding tables.

Scale	Full Scale Range			Binary Coding MSB LSB
	0 to +10V	0 to 20mA	4 to 20mA	
FS-1LSB	9.9976	19.995	19.996	111 111 111 111
3/4 FS	7.5000	15.000	16.000	110 000 000 000
1/2 FS	5.0000	10.000	12.000	100 000 000 000
1/4 FS	2.5000	05.000	08.000	010 000 000 000
1 LSB	0.0024	00.005	04.004	000 000 000 001
ZERO	0.0000	00.000	04.000	000 000 000 000

Current to voltage Conversion with RL 500 ohm (1)					
0 to 20mA		0 to -10V	4 to 20mA		-2 to -10V
19.995		9.9976	19.996		9.998
15.000		7.5000	16.000		8.000
10.000	->	5.0000	12.000	->	6.000
05.000		2.5000	08.000		4.000
00.005		0.0024	04.004		2.002
00.000		0.0000	04.000		2.000

NOTE (1): This table shows the equivalent voltage when the current outputs are supplied with 500 ohm resistors, as described in chapter 5.5.3 "Calibration".

Table 5-3: IAV1S-B D/A Coding Tables

5.5.3 Calibration

It is only possible to calibrate either the voltage output or the current output. The IAV1S-B is normally shipped with the calibration of 0 to 20mA outputs. If the user wants to change the 0 to 20mA current output to 4 to 20mA or to voltage output, a new calibration is necessary. The calibration is done with the diagnostic software, see example in the diagnostic software description.

The trim potentiometers for the calibration adjustment of the 4 channels can be found in the installation section, Figure 5-3 IAV1S-B Physical Layout (A6007).

Calibration Equipment

- Digital voltmeter to measure the voltage and current outputs. The DVM should have an accuracy of 0,01%.
- Test connector assembly (see Appendix B) or a Precision 500 ohm resistor (preferably a 0,01% resistor with the DEC part number 13-09985-00).

Principle of Calibration

Voltage Output Adjustment

Step 1: Load the DAC with all 12 bits at 0. Adjust the offset trimpot until the digital voltmeter indicates 0,000V.

Step 2: Load the DAC with all 12 bits at 1. Adjust the GAIN trimpot until the digital voltmeter shows +9,997V (FS-1LSB).

Current Output Adjustment

Attach the 500 ohm resistor together with the digital voltmeter on to the current outputs (+IOUT/-IOUT) of the channel which is to be calibrated.

Step 1: Load the DAC with all 12 bits at 0 and adjust the offset trimpot as follows:

a. 4 to 20mA output : Offset adjust to 4.000mA or -2.000V

b. 0 to 20mA output : Offset adjust between 0.000mA and 0.002mA or between 0.000V and -0.001V

Step 2: Load the DAC with all 12 bits at "1" and adjust the GAIN trimpot as follows:

a. 4 to 20mA output : GAIN adjust to 19.996mA or -9.998V

b. 0 to 20mA output : GAIN adjust to 19,995mA or -9,997V

5.5.4 Analogue Output Signals

The IAV1S-B analogue output voltage and current signals leave the board via a 50-pin D-type male connector. A flat cable or a user made twisted pair cable could be used for field connection.

Each DAC has a separate current and voltage output and a corresponding analogue ground pin. For the correct electrical analogue output signal requirements, see chapter 5.2 "Specification".
The input signal Latch Disable (L DIS L) is powered from the isolated analogue power. If this signal is used, its corresponding return line is ANA Gnd.
The Function (FNCT L) output is a TTL-output which is set from the FNCT-bit in the CSR register. This line is not field supported, it is only used for test purposes.
The digital +5V output on pin 38 is protected by a 1A pico fuse and is normally used for DIGITAL manufacturing purposes only.

I/O Conn. Pin	Signal Name	I/O Conn. Pin	Signal Name
1		2	
3		4	+VOUT0) + Voltage
5	-VOUT0) Analogue Gnd	6	+VOUT1 > Outputs
7	-VOUT1 > for Voltage	8	+VOUT2) CH0 to CH3
9	-VOUT2) Outputs	10	+VOUT3)
11	-VOUT3)	12	
13		14	
15		16	
17		18	
19		20	+IOUT0) Analogue Gnd
21	-IOUT0) - Current	22	+IOUT1 > for Current
23	-IOUT1 > Outputs	24	+IOUT2) Outputs
25	-IOUT2) CH0 to CH3	26	+IOUT3)
27	-IOUT3)	28	
29		30	
31		32	
33		34	
35		36	ANA Gnd
37	L DIS L	38	DIG +5V Out (manuf. only)
39	FNCT L	40	Gnd
41		42	
43		44	
45		46	
47		48	
49		50	

Table 5-4: IAV1S-B Connector J1 Pin Assignment A6007-P0

5.5.5 Interfacing to the IAV1S-B

In the following, some typical analogue instrument inputs are shown which may be connected to the IAV1S-B analogue outputs.

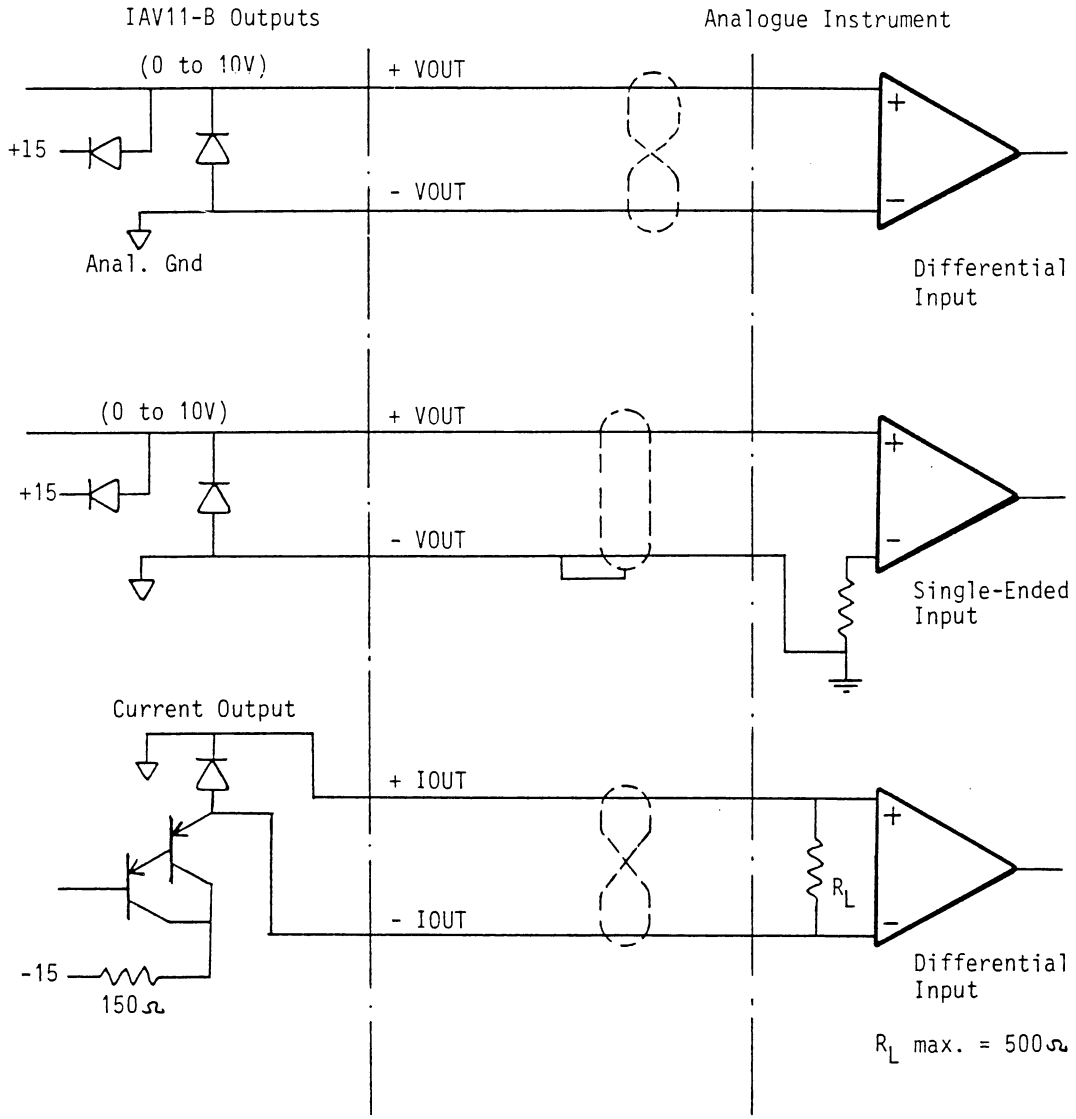


Figure 5-8: Connection the IAV1S-B, (A6007-P0)

CHAPTER 6

IAV1S-A/AA 16 CHANNEL A/D CONVERTER (A410-P0/PA)

6.1 GENERAL DESCRIPTION

The IAV1S-A/AA are 16 channel analogue-to-digital converter modules for the Q-bus. The two board versions are:

IAV1S-A 4/12 Channel A/D-Converter (A410-P0)

12 channel single-ended inputs with analogue semiconductor multiplexers. 4 channel isolated, differential flying capacitor inputs, which are used for analogue field signals where a high degree of isolation from common mode voltages must be maintained. The 4 channel flying capacitor inputs are selected by a reed-relay multiplexer.

IAV1S-AA 16 Channel A/D-Converter (A410-PA)

The IAV1S-AA has only 16 single-ended inputs with semiconductor multiplexer, like the 12 channels of IAV1S-A.

The IAV1S-A or IAV1S-AA are expandable by multiplexer boards, such as the IAV1S-C or IAV1S-CA expansion multiplexer boards, up to 128 channels in any combination.

Analogue to digital conversions are started by program command or an external trigger. After the conversion on the selected channel is done, the DONE-flag is set and an interrupt occurs.

NOTE

All general information in this description refers to the IAV1S-A, but is also valid for the IAV1S-AA, if not otherwise noted.

FEATURES

o For IAV1S-A only

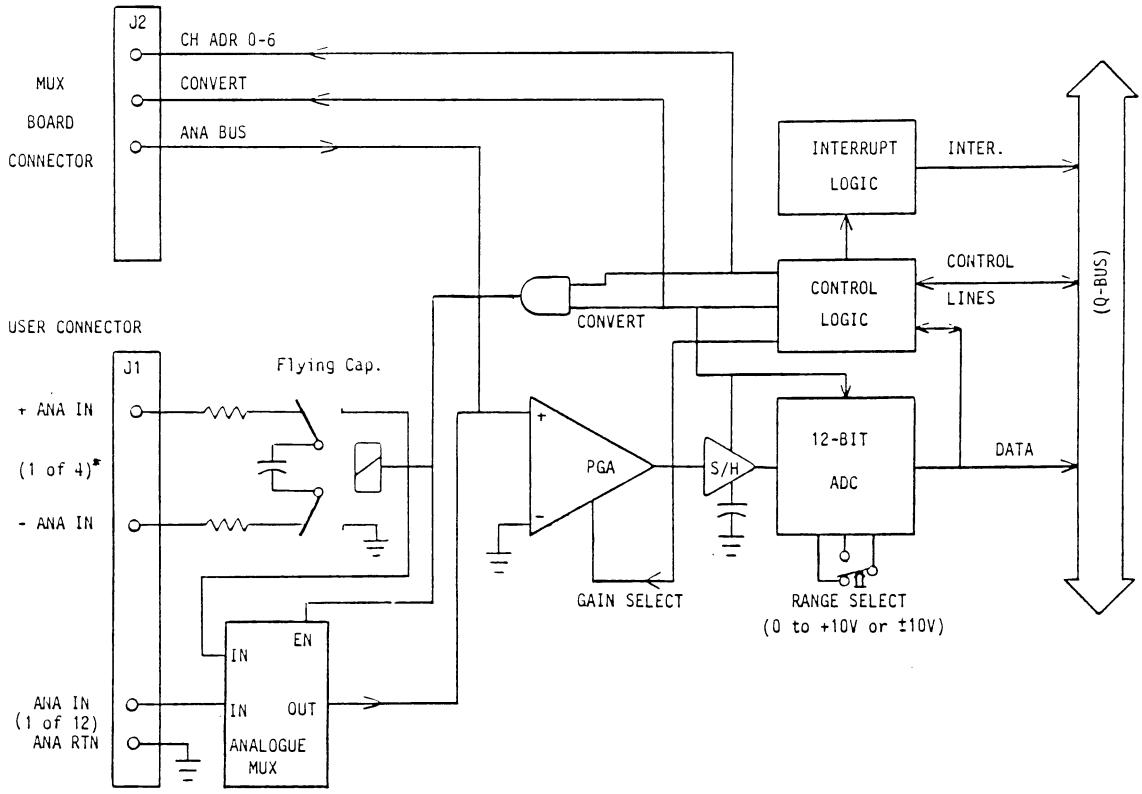
- 4 potentially free, true differential flying capacitor input channels
- 12 single-ended solid state input channels

o For IAV1S-AA only

- 16 channel single-ended solid state analogue inputs non-isolated

o For both versions

- 12-bit resolution
- Unipolar (0 to +10V) or bipolar (±10V) input range
- 8 software programmable gains of 1, 2, 5, 10, 20, 50, 100, 200
- External trigger input
- Expandable by multiplexer boards up to maximum of 128 channels
- Module identification code readable by program
- both A/D-converter versions can be installed in any combination with the IAV1S-C and IAV1S-CA multiplexer versions



* NOTE: In the IAV1S-AA version (A410-PA) these 4 channels (channel 0 to 3) have only semiconductor multiplexer inputs, like the other 12 channels.

Figure 6-1: IAV1S-A Simple Block Diagram A410-P0

6.2 SPECIFICATION

Parameter	IAV1S-A	IAV1S-AA
GENERAL:		
Module Designation	A410-P0	A410-PA
Identification	100 octal (software identification when reading the MOD register)	
Board Size	Quad high Module (for BA200 enclosures)	
Power	+5Vdc ± 5% at 1,3A	+5Vdc ± 5% at 1,25A
Bus Load	1 DC-load; 1,6 AC-load	
OPERATIONAL:		
No. of Analogue Channels	4 potentially free, true differential flying cap. inputs 12 solid state single ended inputs	16 solid state single-ended inputs (non isolated)
Expansion Capabilities	Connector for Mux-Board allows up to 112 extended channels	
Resolution	12-Bit	
A/D Output Coding (switch selected)	Unipolar 0 to +10V; binary code Bipolar ±10V; offset binary code	
Conversion Time	Flying cap. chan. 8,5 msec. per channel (115 Hz)	N.A.
	Solid State Channels: typ. 40microsec. at gain 1 to 10 typ. 100microsec. at gain 20 to 200	
Software Programmable Gains	1, 2, 5, 10, 20, 50, 100, 200,	

Parameter	IAV1S-A	IAV1S-AA
ANALOGUE INPUT CHARACTERISTICS:		
System Accuracy (Bipolar Mode)	Gain 1 to 10 ± 1 LSB Gain 20 to 100 ± 2 LSB Gain 200 ± 5 LSB In unipolar mode the system accuracy deviates between gain 10 and 200 by 1 to 2 LSB from values given for bipolar mode. Note, that the above are specified for a system calibration at gain 1.	
Linearity	± 1 LSB at gain 1	
Input Impedance	> 50 megohm	
Gain Temperature Coefficient	max. 50 ppm/degree celsius	
Offset Temperature Coefficient	max. 20 ppm/degree celsius	
Warm-up Time	≥ 10 minutes	
Input Protection	up to ± 25V at power ON and ± 15V at power OFF	
* Input Filter	First order low pass filter, cut off frequency 2,95 Hz	N.A.
* Common Mode and Crosstalk Rejec.	100 dB typ. at 50 Hz	N.A.
* Isolation Voltage	Inputs to Comp. Gnd 1000 Vdc or peak AC	N.A.
* Interchannel Isolation	250 Vdc or peak AC	N.A.

* NOTE: Flying Capacitors inputs Channels 0 to 3 only !

Parameter	IAV1S-A	IAV1S-AA
BUS INTERFACE:		
Register Addressing	Switch selectable over the 4 k I/O address erea. Four word address with one word unused.	
Interrupt Vector	Switch selectable from 000 to 770 octal Done = XX0; Error = XX4	
Priority Level	BR4; Jumper selectable to 5 or 6	

6.3 INSTALLATION

6.3.1 Site Considerations

The IAV1S-A/AA has two bus interface connectors that plug into a Q-bus slot. These connectors have signals defined by the Q-bus specification. The interrupt priority of the module is determined by the position on the Bus (Position Dependent Configuration). The closer a device is to the processor, the higher its priority.

6.3.2 Interconnection

Interfacing the IAV1S-A/AA to the user's device is done via the 50-pin D-type male connector. A 50-conductor flat cable or a user made twisted pair cable may be used for field connection. The pin assignment and the signal description are shown in chapter 6.5.
General information about the user I/O-connector and the physical requirements are given in chapter 1.4.6.
Connection of a IAV1S-C/CA multiplexer board to the IAV1S-A/AA is done via the 26 pin connector J2 and a T-type flat cable, as described in the multiplexer description.

6.3.3 Initial Operation

Selecting the IAV1S-A/AA Device Address

The device address is the I/O address assigned to the MOD-register. The device address is selected via a 10-pole switch (Figure 6-4). The switches allow the device address to be set within a range of 160000 octal to 177770 octal.
The standard address range for this module is from 171400 to 171770 in increments of 10 octal.

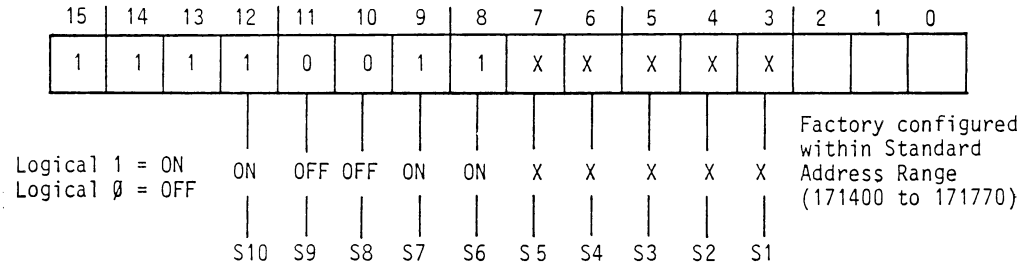


Figure 6-2: Selecting IAV1S-A/AA Device Address

Selecting the IAV1S-A/AA Interrupt Vector Address

The IAV1S-A is capable of generating two interrupt vectors (DONE and ERR INTERRUPT). The interrupt vector address can be set via a 6-pole switch (Figure 6-4) within the range of 0 to 770 octal in increments of 10 octal.

For standard vector, the vector switches 1 to 6 (Figure 6-3) should have the same position as the address switches 1 to 6 (Figure 6-2). This means that the address and the vector are identical at the address bits 3 to 8.

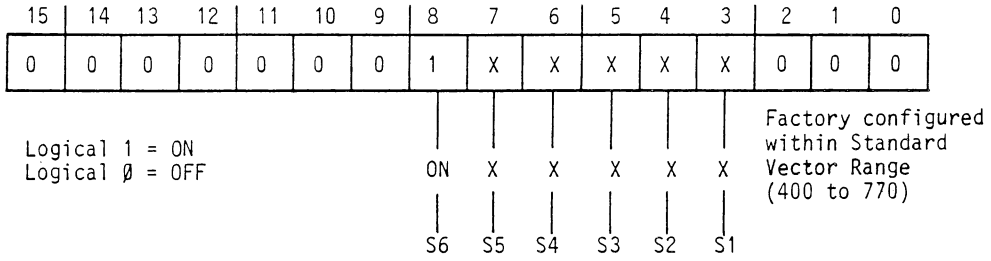


Figure 6-3: Selecting IAV1S-A/AA Interrupt Vector

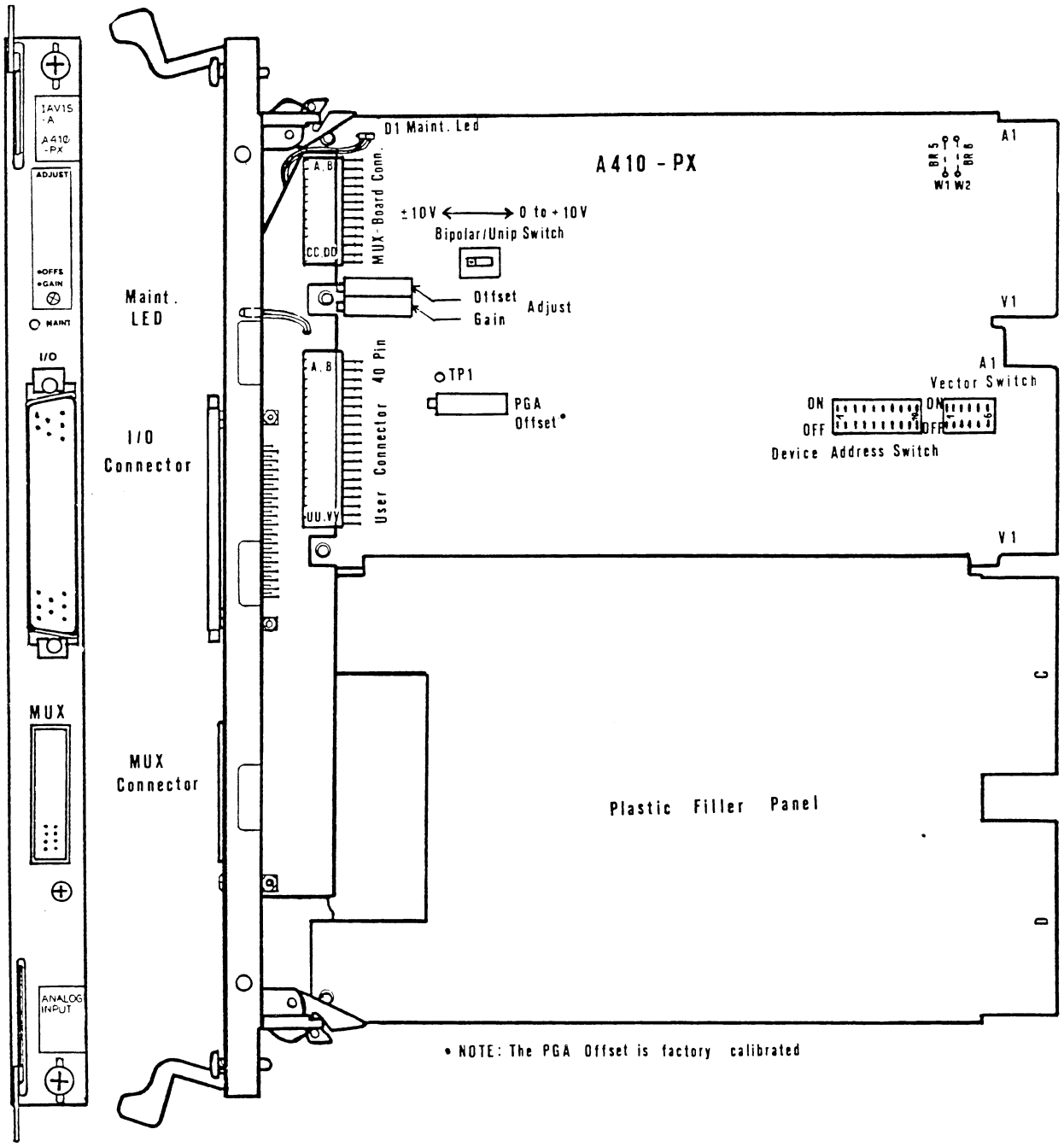


Figure 6-4: IAV1S-A/AA Physical Layout (A410-P0/PA)

Selecting the Interrupt Request Level

The standard interrupt request level is 4 (BIRQ4). A higher request level, BIRQ5 or BIRQ6 can be selected via the jumpers BR5 or BR6.

Whenever the BIRQ4 on the module is changed to a higher level, no other modules should be installed on the bus closer to the processor which have a lower request level. The interrupt priority of the IAV1S-A/AA is position dependent and it does not monitor higher request levels.

Selecting the Analogue Input Range

The unipolar (0 to +10V) and the bipolar (±10V) input range may be selected by a single DIL-switch, see figure 6-4.

The IAV1S-A is normally shipped and calibrated in the Bipolar Input Range. The switch position for the input range can be read by the program in the MOD-register bit 4 (BIP). If BIP is set, the bipolar range is selected.

However, if the input range has to be changed, a new calibration is necessary. See chapter 6.5.3 "Calibration".

6.4 OPERATION AND PROGRAMMING

6.4.1 General

This chapter presents a detailed description of the IAV1S-A registers (see Figure 6-5). Four consecutive bus addresses are assigned to the register set.

171XX0	Mode Register	(MOD)
171XX2	ADC-Data Register	(DAT)
171XX4	Control Status Register	(CSR)
171XX6	unused	

They can read or written using any instruction that refers to their address.

Initialization

The mnemonic INIT refers to the initialization signal issued by the processor. Initialization is caused by one of the following:

- issuing a programmed RESET instruction
- depressing the start switch on the processor console
- the occurrence of a power-up or power-down sequence

The MOD and CSR registers are then initialized.

Operation Modes

The unipolar (0 to +10V) and bipolar (±10V) analogue input range is the only mode which can be changed by a single DIL switch on the module.

The position of the input range switch is readable in the MOD-register. Normally, the IAV1S-A is shipped and calibrated in the bipolar input range.

Execution of a A/D Conversion

An analogue to digital conversion is performed in the following steps:

- Check that the DONE flag is not set.
- Load the channel address and the gain for the desired channel in the CSR register.
- Set the A/D START bit for internal start or the EET bit for the external trigger in the SCR register.
- At the end of the conversion, the DONE flag is set and the converter data can be read from the DAT register.

If Interrupt Enable (IE) is set, an interrupt occurs by setting the DONE flag. Reading the DAT register clears DONE and a new conversion can be started.

6.4.2 Mode Register (MOD)

The MOD register is generally used to identify the module with its identification code and for maintenance purposes.

Bit	Name	Description
15 to 8	IDENT 7 to IDENT 0 (read only)	Identification Bits 7-0 The module is identified by these bits. The A410 module has the code 100 octal (in high byte).
6	LED (read/write)	LED indication for test purposes
4	BIP (read only)	Bipolar Input Range This bit monitors the position of the Bipolar/Unipolar Switch on the board. If BIP is set, the bipolar range (±10V) is selected.

Table 6-1: IAV1S-A/AA MOD Register Bit Assignments

MOD 171XX0 - Mode Register

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
IDENT									LED		BIP				
7	6	5	4	3	2	1	0								
R									R/W		R				

NOTE: R = read only
W = write only
R/W = read/write
All bits not described are unused and read or written as zero.

Figure 6-5: IAV1S-A/AA Mode Register

6.4.3 ADC-Data Register (DAT)

The DAT register is a 12-bit read only register. It contains the converted data after an analogue-to-digital conversion has been performed. Reading the DAT register clears the DONE and ERR-flags in the CSR register. The data code for the ADC is binary code in unipolar range (0 to 10V) and offset binary code in bipolar range (±10V). Refer to the coding table chapter 6.5.

DAT 171XX2 - ADC Data Register

	(MSB) AD DAT (LSB)											
	11	10	09	08	07	06	05	04	03	02	01	00
	READ ONLY											

NOTE: R = read only
W = write only
R/W = read/write

All bits not described are unused and read or written as zero.

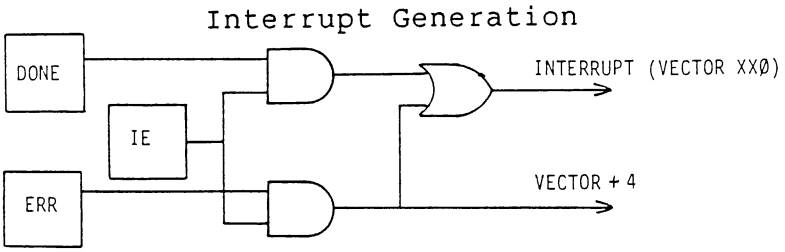
Figure 6-6: IAV1S-A/AA ADC Data Register

6.4.4 Control Status Register (CSR)

The CSR is a 16-bit read/write register. It can be written in word or byte format. The definitions are described in table 6-2.

CSR 171XX4 - Control Status Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Ø
CH AVAI	CHA 6	5	4	3	2	1	0	DONE	IE	ERR	EET	GAIN 2	1	0	A/D START
R	R/W							R	R/W	R	R/W	R/W			W



NOTE: R = read only
W = write only
R/W = read/write

All bits not described are unused and read or written as zero.

Figure 6-7: IAV1S-A/AA Control Status Register / Interrupt Generation

Bit	Name	Description
15	CHAVAI (read only)	Channel available. This bit is set when the addressed channel is in the system (diagnostic feature).
14 to 8	CHA 6 to CHA 0 (read/write)	Channel Address Bits 6-0 Address of the channel which should do a A/D conversion.
7	DONE (read only)	A/D Conversion Done DONE is set at the end of a conversion. It is cleared when the DAT register is read or by INIT.
6	IE (read/write)	Interrupt Enable for DONE and ERROR-flags
5	ERR (read only)	Error This bit is set when an internal or external start to a A/D conversion is made and following conditions are present: - DONE-flag is set - an A/D conversion is currently taking place. ERR is cleared when the DAT register is read.
4	EET (read/write)	Enable External Trigger EET enables the EXTRIG-Input signal to start the A/D conversion. EXTRIG-input is then wired-OR to the A/D START bit. EET is also a TTL output signal.
3 2 1	GAIN 2 GAIN 1 GAIN 0 (read/write)	These bits show the Gain for the currently addressed channels. Binary coded from 0-7 for the levels 1, 2, 5, 10, 20, 50, 100 and 200.
0	A/D START (write only)	A/D Conversion Start This bit can start a conversion provided that DONE is not present.

Table 6-2: IAV1S-A/AA CSR Register Bit Assignment

6.5 FUNCTIONAL DESCRIPTION

6.5.1 Theory Of Operation

Figure 6-1 shows a simple block diagram of the IAV1S-A/AA. It is addressed via the Q-bus address lines. The board has switches to select its device address and interrupt vector address according to the rules in chapter 6.3.

The 16 analogue input channels are entered through connector J1. The channels 0 to 3 are isolated by flying capacitor inputs with a relay multiplexer at the IAV1S-A/AA version only. A semiconductor analogue multiplexer is used for all other non-isolated channels.

The selected analogue input signal goes to the internal analogue bus and to a digitally programmable gain amplifier. A sample and hold amplifier samples this signal a definate time and switches to hold-state during the conversion cycle of the A/D converter (see figure 6-8). The ADC is a 12-bit successive approximation analogue to digital converter in a 28 pin DIP package.

6.5.2 Mode Of Operation

Unipolar/Bipolar Input Range

The full scale input range is selectable by a DIL-switch to unipolar 0 to +10V or bipolar $\pm$10V input voltage. The Uni/Bi-switch position can be read by the BIP-bit in the MOD register. Changing the input range requires a new calibration.

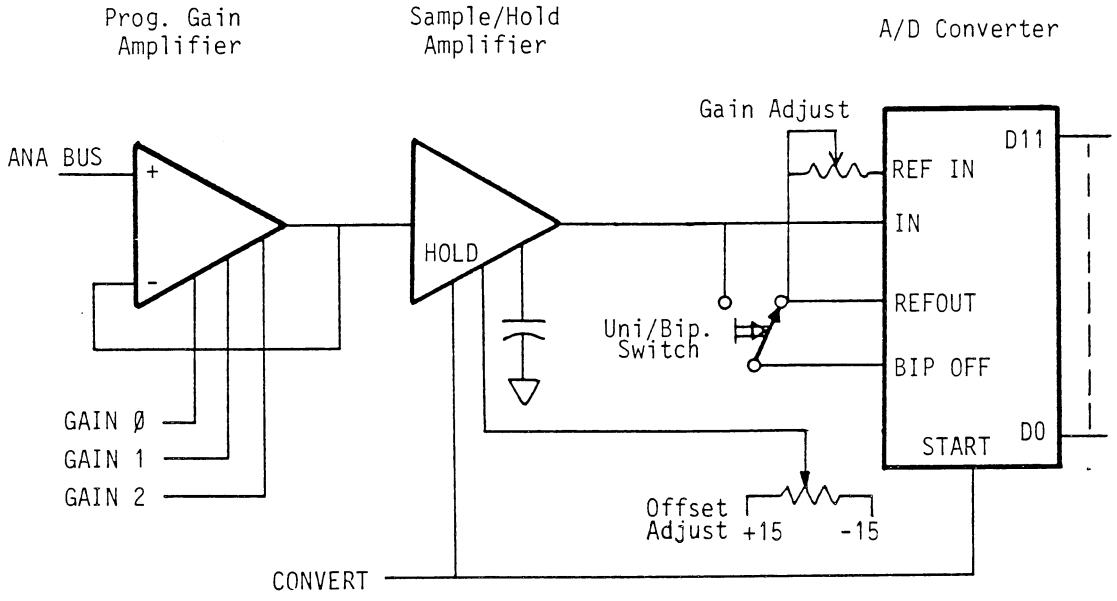


Figure 6-8: IAV1S-A/AA ADC Circuit (A410-P0/PA)

Programmable Gain

The gain can be programmed with three bits in the CSR register for the levels 1, 2, 5, 10, 20, 50, 100 and 200. A higher gain takes a longer conversion time. For details, see specification.

The different conversion times required at flying capacitor or semiconductor multiplexers or at higher gains is controlled by the IAV1S-A hardware.

A/D Converter Coding

The A/D converter produces the 12-bit (4096 states) binary codes which are listed in the following tables.

Unipolar Operation Code

	Scale	Range 0 to +10V	Binary Coding MSB LSB			
Full Pos.	+FS-1LSB	+9.9976	111	111	111	111
	+3/4 FS	+7.5000	110	000	000	000
	+1/2 FS	+5.0000	100	000	000	000
	+1/4 FS	+2.5000	010	000	000	000
	+1 LSB	+0.0024	000	000	000	001
Zero	ZERO	0.0000	000	000	000	000

Bipolar Operation Code

	Scale	Range ±10V	Offset Binary Coding MSB LSB			
Full Pos.	+FS-1LSB	+9.9951	111	111	111	111
	+3/4 FS	+7.5000	111	000	000	000
	+1/2 FS	+5.0000	110	000	000	000
	+1 LSB	+0.0049	100	000	000	001
Zero	ZERO	0.0000	100	000	000	000
	-1 LSB	-0.0049	011	111	111	111
	-1/2 FS	-5.0000	010	000	000	000
	-FS+1LSB	-9.9951	000	000	000	001
Full Nega.	-FS	-10.0000	000	000	000	000

A/D Converter Input Ranges

Gain Bits 2.1.0 (binary)	Gain	Full Scale Range Unipolar	Bipolar	mV/LSB Unipolar	Bipolar
0	1	0 to +10V	+- 10V	2.4414	4.8828
1	2	0 to +5V	+- 5V	1.2207	2.4414
2	5	0 to +2V	+- 2V	0.4882	0.9765
3	10	0 to +1V	+- 1V	0.2441	0.4882
4	20	0 to +0.5V	+- 0.5V	0.1220	0.2441
5	50	0 to +0.2V	+- 0.2V	0.0488	0.0976
6	100	0 to +0.1V	+- 0.1V	0.0244	0.0488
7	200	0 to +0.05V	+- 0.05V	0.0122	0.0244

Table 6-3: IAV1S-A/AA ADC Coding Tables

6.5.3 A/D Converter Calibration

The IAV1S-A/AA is normally shipped and calibrated for the bipolar input range. If the input range is changed to unipolar, a new calibration is necessary. The calibration is done with the diagnostic software. There are two tests available, the "Dynamic" and the "Calibration" test. The latter contains operator instructions (see the example in the diagnostic software listing).

Calibration Equipment

- Precision voltage reference source with an accuracy of 0,01%
- The analogue input test connector (see Appendix B) can be used.

Starting the Calibration

Put the precision voltage reference source at one or more of the analogue inputs. Use gain 1 only for the following procedures.

A warm-up time of $\geq$10 minutes is required.

Bipolar Adjustment

Step 1: Offset Adjust
Enter -9.9951V (-FS+1LSB). Adjust the offset trimpot so that the printout of the conversions is mainly on -9.9951V or 0001 octal code.

Step 2: Gain Adjust
Enter +9.9902V (FS-2LSB). Adjust the gain trimpot so that the printout of the conversions is mainly on +9.9902V or 7776 octal code.

Unipolar Adjustment

Step 1: Offset Adjust
Enter +0.0024V (1LSB). Adjust the offset trimpot so that the printout of the conversion is mainly on +0.0024V or 0001 octal code.

Step 2: Gain Adjust
Enter +9.9952V (+FS-2LSB). Adjust the gain trimpot so that the printout of the conversion is mainly on +9.9952V or 7776 octal code.

NOTE: If the ADC is used at one gain only, it can be calibrated more precisely if the steps of the calibration procedure are done in this gain. The table "A/D Converter Input Ranges" can be used to calculate the full scale range and the LSB value for this calibration.

Precalibration of the PGA Offset (for factory use only)

Connect the Analogue Bus on the MUX-connector to Analogue Ground (Pin BB to Pin AA) and adjust the voltage at TP1 with RV3 to 0 volts ±10 microvolt. The program must be stopped during this calibration.

6.5.4 Analogue Input And Control Signals

The analogue input signals enter the board through the 50-pin male connector J1. A flat cable or a user made twisted pair cable could be used for field connection.

At the IAV1S-A 4 channel isolated, differential flying capacitor and 12 channel semiconductor single-ended inputs can be connected to input connector J1. The IAV1S-AA has only 16 channel semiconductor single-ended inputs.

The flying capacitor channels (channel 0 to 3) at the IAV1S-A are differential inputs. They have one side of the generating source connected to the positive (+IN) and the other side to negative (-IN) input pins as shown in Figure 6-10.

The single-ended inputs have one side of the user's analogue source connected to the semiconductor analogue multiplexer input (IN) and the other side connected to analogue return (ANA RTN) as shown in Figure 6-9.

For correct electrical analogue input signal requirements, see chapter 6.2 "Specification".

Control Signals

The external trigger input signal (EXT TRIG L) is a TTL input which generates a conversion start at the trailing edge of a low pulse if the enable external trigger bit (EET) in the CSR register is set. EXT TRIG L is then a wired-or to the internal start function.

The external trigger enable (EET L) is a TTL outpt signal. It monitors the EET-bit in the SCR register. When the EET-bit is set, the EET L output signal has a low level.

The +5V output on Pin 38 is protected by a 1A pico fuse and is normally used for DIGITAL manufacturing purposes only.

The signals in the MUX-board connector J2 are not for user applications. J2 is only used to connect standard analogue MUX-boards, such as the IAV1S-C.

I/O Conn. Pin	Signal Name	I/O Conn. Pin	Signal Name
1		2	
3		4	+IN0(+Ana Inp. Ch 0)
5	-IN0(-Ana Inp. Ch 0)	6	+IN1
7	-IN1	8	+IN2
9	-IN2	10	+IN3(+Ana Inp. Ch 3)
11	-IN3(-Ana Inp. Ch 3)	12	IN4(Ana Inp. Ch 4)
13	RTN4(Ana Ret Ch 4)	14	IN5
15	RTN5	16	IN6
17	RTN6	18	IN7
19	RTN7	20	IN8
21	RTN8	22	IN9
23	RTN9	24	IN10
25	RTN10	26	IN11
27	RTN11	28	IN12
29	RTN12	30	IN13
31	RTN13	32	IN14
33	RTN14	34	IN15(Ana Inp. Ch 15)
35	RTN15(Ana Ret Ch 15)	36	Gnd
37	EET L	38	+5V Out(Manuf. only)
39	EX TRIG L	40	Gnd
41		42	
43		44	
45		46	
47		48	
49		50	

Table 6-4: IAV1S-A Connector J1 Pin Assignment A410-P0

I/O Conn. Pin	Signal Name	I/O Conn. Pin	Signal Name
1		2	
3		4	IN0 (Ch 0)
5	RTN0 (Ch 0)	6	IN1
7	RTN1 A	8	IN2 A
9	RTN2 N	10	IN3 N
11	RTN3 A	12	IN4 A
13	RTN4 L	14	IN5 L
15	RTN5 O	16	IN6 O
17	RTN6 G	18	IN7 G
19	RTN7	20	IN8
21	RTN8 R	22	IN9 I
23	RTN9 E	24	IN10 N
25	RTN10 T	26	IN11 P
27	RTN11 U	28	IN12 U
29	RTN12 R	30	IN13 T
31	RTN13 N	32	IN14
33	RTN14	34	IN15 (Ch 15)
35	RTN15 (Ch 15)	36	Gnd
37	EET L	38	+5V Out (Manuf. only)
39	EX TRIG L	40	Gnd
41		42	
43		44	
45		46	
47		48	
49		50	

Table 6-5: IAV1S-AA Connector J1 Pin Assignment A410-PA

6.5.5 Interfacing To The IAV1S-A/AA

Single-Ended Inputs

Single-ended inputs may be of two types, grounded or floating.

A grounded input signal is referenced to the ground of the instrument that is producing the signal (figure 6-9). Since the instrument may be located some distance from the computer, there may be some voltage difference between the instrument ground and the computer ground. The voltage seen by the IAV1S-A is the sum of this unwanted ground difference voltage and the desired signal voltage.

A floating signal voltage is measured with respect to a point that is not connected to ground. Examples of this type of analogue input are shown in figure 6-9.

The return line of a floating signal must be connected to the IAV1S-A analogue return (ANA RTN).

There is a return connection provided for each channel. Refer to the Input Connector Table.

Differential Inputs

Figure 6-8 illustrates the differential input mode. The same noise voltage exists in the power distribution ground system, except that the generation device ground is connected directly to the negative input of the receiving differential amplifier. Because the instantaneous noise voltage is common to the + and - inputs, it is cancelled out of the final amplifier output.

Shielded Input Lines

The effects of electrostatic coupling on the input signals can be decreased by using shielded input cables. This is important if the device or source has high impedance. To prevent the shield from developing a ground loop and conducting current, connect it to ground at the source end only.

Twisted-Pair Input Lines

The effects of magnetic coupling on the input signals can be decreased for floating single-ended or differential inputs by using twisted-pair input cables. The inductive noise on the two lines match, making the combined effect zero at the input to the IAV1S-A.

With ground-referenced, single-ended inputs, the use of twisted-pair inputs has no effect.

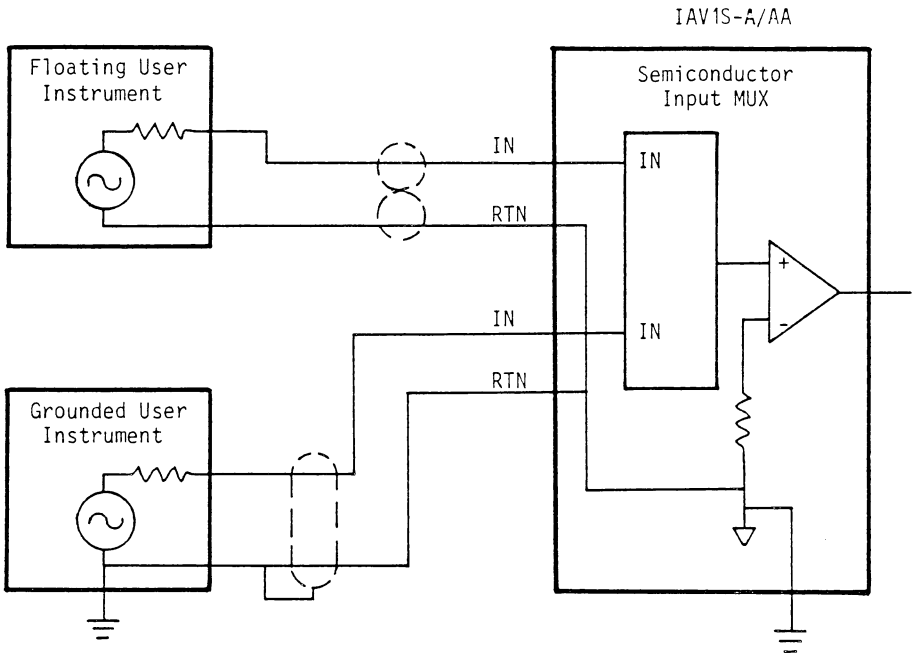


Figure 6-9: Single-Ended Analogue Input

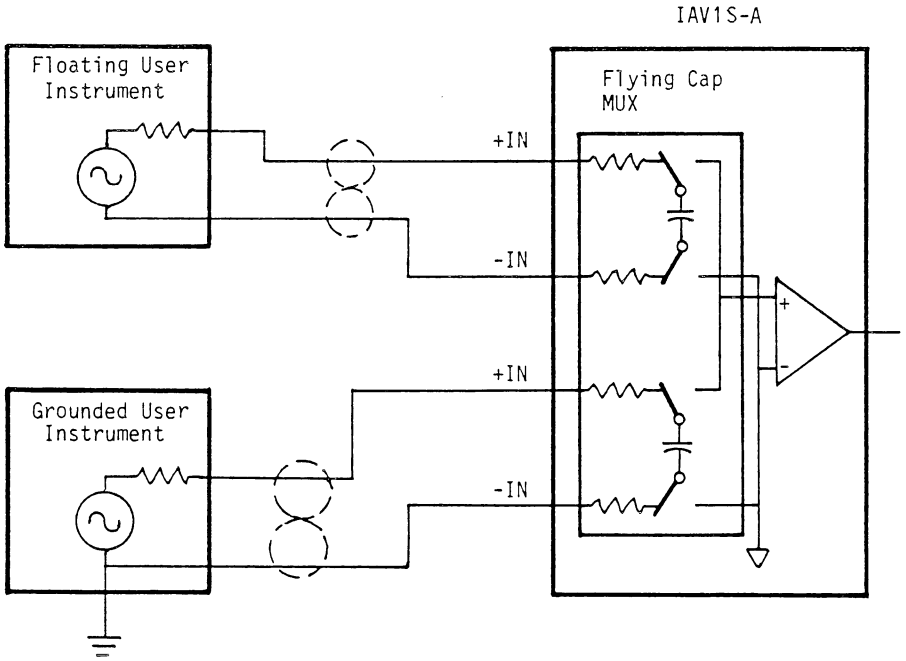


Figure 6-10: Isolated Differential Input

CHAPTER 7

IAV1S-C/CA 16 CHANNEL EXPANSION MULTIPLEXER (A029-P0/PA)

7.1 GENERAL DESCRIPTION

The IAV1S-C/CA are expansion multiplexer boards with 16 channel analogue inputs for Q-bus systems.

The two board versions are:

IAV1S-C 16 Channel Flying Cap. Exp. MUX (A029-P0)

The IAV1S-C is a 16 channel flying capacitor multiplexer board. It is used where a high degree of isolation of the field signals from common mode voltage must be maintained.

IAV1S-CA 16 Channel Expansion Multiplexer (A029-PA)

The IAV1S-CA is a 16 channel semiconductor multiplexer board. It is used where a large number of low cost analogue inputs have to be maintained in the field.

Both multiplexer versions have the same PC-board and are software-and input connector compatible. The IAV1S-C and IAV1S-CA can be installed in any combination with the IAV1S-A or IAV1S-AA A/D-Converters.

Up to seven multiplexer boards can be connected to the A/D-Converter via a T-type flat cable assembly.

NOTE

All general information in this description refers to the IAV1S-C, but is also valid for the IAV1S-CA version, if not explicitly differentiated. The same applies to IAV1S-A.

FEATURES

o For IAV1S-C only

- 16 channel true differential, potential free, flying capacitor analogue inputs.
- The relays are decoupled from the analogue bus by semiconductor multiplexers to increase the system reliability.

o For IAV1S-CA only

- 16 channel single-ended solid state analogue inputs (non-isolated).

o For both versions

- Input Range ±10V
- Up to seven IAV1S-C's can be connected to an IAV1S-A A/D converter for expansion up to 128 channels.
- The 16 channel address bank of each IAV1S-C/CA is selectable by switches.
- Only +5V power is used from the Q-bus backplane.
- Module identification readable by program.
- both multiplexer board versions can be installed in any combination with the IAV1S-A A/D-Converter versions.

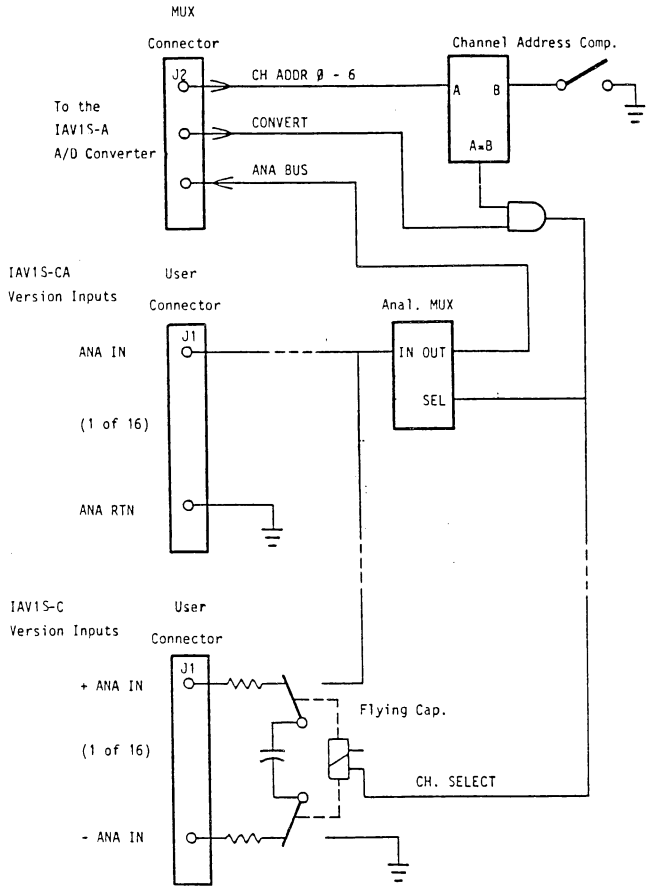


Figure 7-1: IAV1S-C/CA Simple Block Diagram

7.2 SPECIFICATION

PARAMETER	IAV1S-C	IAV1S-CA
GENERAL:		
Module Designation	A029-P0	A029-PA
Identification	10 octal (this code is or'd in the A/D-Converter Identification Code)	
Board Size	Quad high Module (for BA200 enclosures)	
Prerequisite	One T-type 26 Conductor Flat Cable	
Power	+ 5 Vdc ± 5% at 200 mA	+ 5 Vdc ± 5% at 80 mA
Bus Load	No Bus Load (power only)	
OPERATIONAL:		
No. of Analogue Inp.	16 potential free flying capacitor inputs	16 single-ended inputs (non-isolated)
Expansion Capabilities	Up to seven A029-P0/A029-PA multiplexer boards may be connected to the A410-P0/A410-PA A/D-Converter modules	
Conversion Time	typ. 8,5 millisec.	typ 40 microsec.

PARAMETER	IAV1S-C	IAV1S-CA
INPUT CHARACTERISTICS:		
Input Range	± 10V	± 10V
System Accuracy *	0,03% FSR	0.02% FSR
Input Filter	First order low pass filter, cut off frequency 2,95 Hz	N.A.
Isolation Voltage	Inputs to Computer Gnd 1000 Vdc or peak AC	N.A.
Interchannel Isolation	250 Vdc. or peak AC	N.A.
Input Protection	Up to ± 25V across the ± inp. pins per channel	max. ± 25V at power ON, and ± 15V at power OFF
Common Mode and Crosstalk Rejection Ratio	typ. 100 dB at 50 Hz	N.A.

N.A. means Not Applicable

* NOTE: Refer to the IAV1S-A/AA A/D-Converter specification (A410-P0/PA) for the accuracy at higher gains. The system performance can decrease at gains above 10, up to 2 LSB if several multiplexer boards are installed.

7.3 INSTALLATION

7.3.1 Site Considerations

The IAV1S-C has two interface connectors that plug into a Q-bus slot.

The module is only supplied with +5V power from the backplane.

The Q-bus interrupt and DMA-grant daisy-chain lines are hardwired on the module.

7.3.2 Interconnection

Interfacing the IAV1S-C to the user's device is done via the 50-pin D-type male connector J1. A flat cable or a user made twisted pair cable could be used for field connection. The pin assignment and the signal description are shown in chapter 7.5. General information about the user I/O-connector and the physical requirements are given in chapter 1.4.6.

Connecting the IAV1S-C to the IAV1S-A A/D converter module or to another multiplexer board is done via the 26-pin connector J2 and a T-type flat cable as shown in Figure 7-2. The cable is always connected from pin A to pin A between the connectors.

Note that IAV1S-C's should always be installed in the same backplane where the IAV1S-A (A/D converter) is located. Special MUX interconnection cables should be made as short as possible.

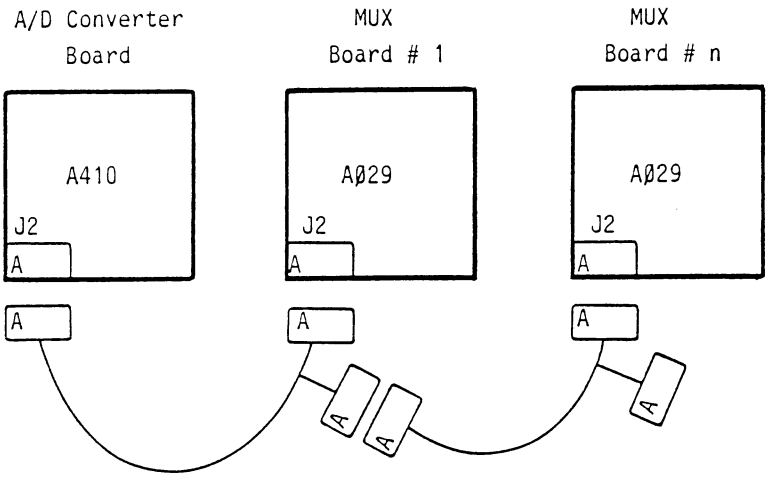


Figure 7-2: Connecting the MUX Cable

7.3.3 Initial Operation

Each IAV1S-C has 16 input channels which are accessed by a multiplexer.

The channels are addressed by the address bits CHA6 to CHA0 in the IAV1S-A A/D converter. This is a channel address range of 128 decimal channels. Channel 0 to 15 is always used by the A/D converter board. The following 7 address banks of 16 channels each can be selected by a DIL-switch on the IAV1S-C board (see figures 7-3 and 7-4).

The selected channel address banks should correspond from the second bank upwards, so that a closed address range from channel 0 to channel n is possible.

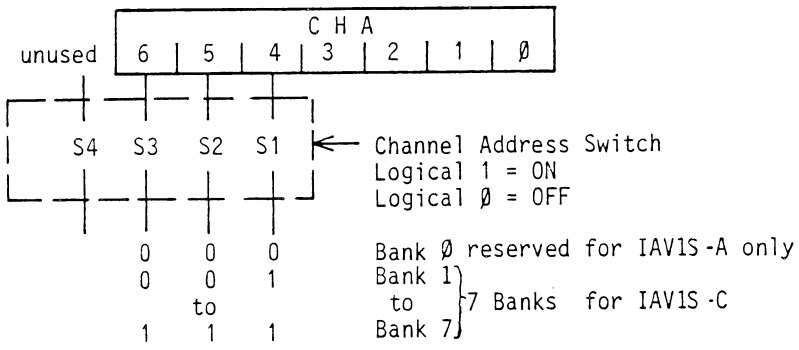


Figure 7-3: Selecting IAV1S-C Channel Address

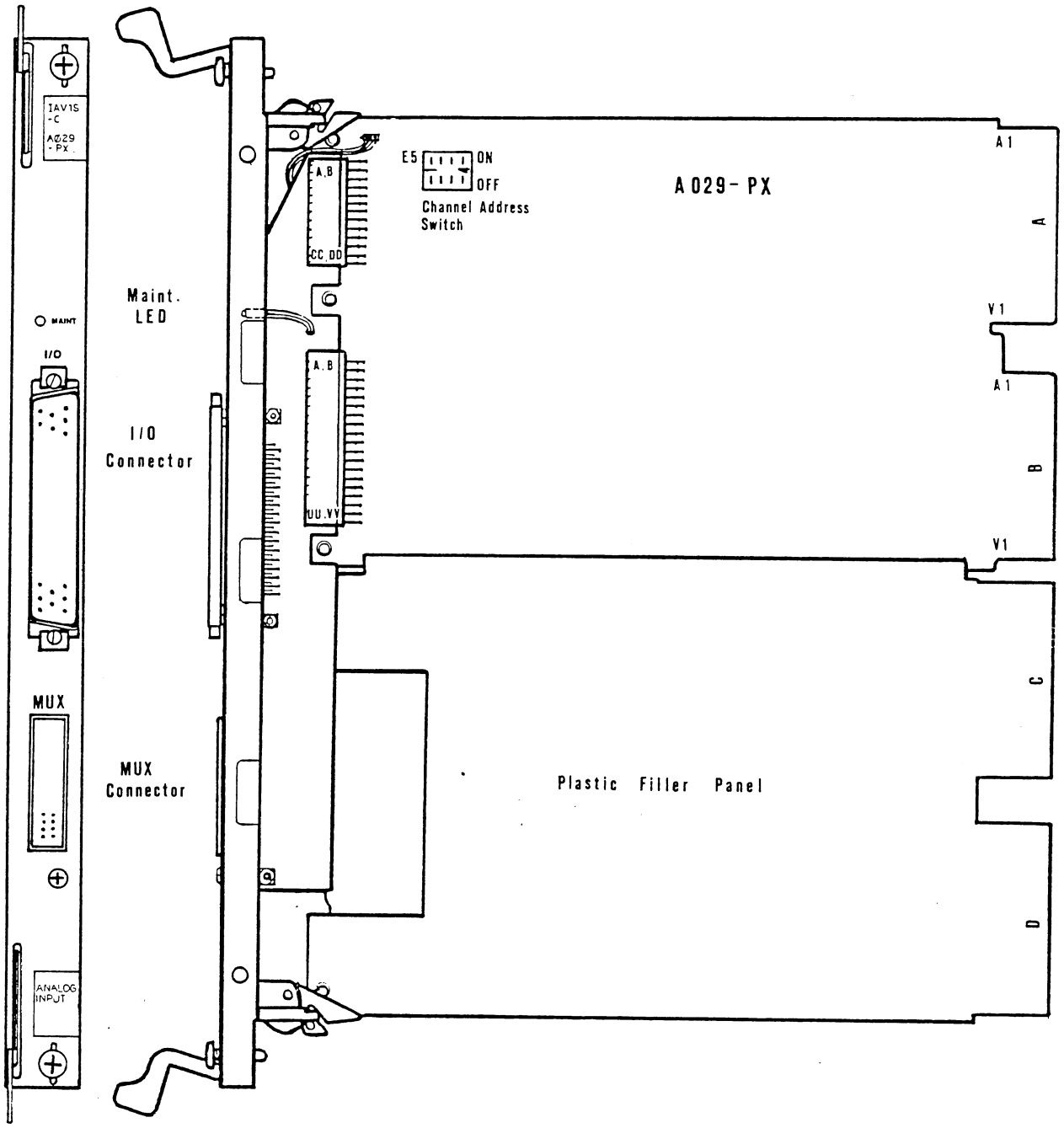


Figure 7-4: IAV1S-C/CA Physical Layout A029-P0/PA

7.4 OPERATION AND PROGRAMMING

7.4.1 General

The IAV1S-C 16 channel expansion multiplexer is an add-on option to the IAV1S-C A/D converter.

The IAV1S-C has no internal registers. Its analogue input channels are controlled by the register set in the IAV1S-A A/D converter.

The IAV1S-C (Board A029) is selected by the channel address bits CHA6 to CHA0. This gives a channel address range of 128 (decimal). The first 16 channel address bank (CH0 to CH15) is used by the IAV1S-A. The next 7 address banks of 16 channels each may be used for one or more IAV1S-C MUX-boards.

7.4.2 Programming The IAV1S-C

Each IAV1S-C can be selected by a DIL switch for the following channel addresses:

```
Bank 0 : Ch 0 to Ch 15 reserved for IAV1S-A only
Bank 1 : Ch 16  to Ch 31    )
Bank 2 : Ch 32  to Ch 47    )  The IAV1S-C can expand
Bank 3 : Ch 48  to Ch 63    )  the first 16 channels of
Bank 4 : Ch 64  to Ch 79     > the IAV1S-A A/D converter
Bank 5 : Ch 80  to Ch 95    )  module in this order.
Bank 6 : Ch 96  to Ch 111   )
Bank 7 : Ch 112 to Ch 127   )
```

Programming the IAV1S-C is done by the register set of the IAV1S-A A/D converter module. Refer to chapter 6.4. "Operation and Programming" of the IAV1S-A Option Description.

When a channel address from a IAV1S-C MUX board is set in CSR register, the CH AVAI bit indicates if this channel or channel bank is in the system.

Reading the MOD registers indicates which MUX board type (MUX board identification code) is installed at the desired channel address. The IAV1S-C has an identification code of 10 octal. This code is OR'd to the IAV1S-A identification code by reading the MOD register (result 110 octal).

7.5 FUNCTIONAL DESCRIPTION

7.5.1 Theory Of Operation

Figure 7-1 shows a simple block diagram of the IAV1S-C. It has to be connected via the MUX connector J2 to the IAV1S-A A/D converter.

The IAV1S-C channels are selected by the channel address bits CHA6 to CHA0 in the CSR register of the IAV1S-A.

The 16 analogue input channels are entered through connector J1. The inputs of the IAV1S-C (A029) are flying capacitor inputs which are switched by a reed relay multiplexer. These relays are additionally decoupled from the A/D converter analogue bus by semiconductor multiplexers. The inputs of the IAV1S-CA (A029-PA) have only semiconductor multiplexers.

The analogue input signal goes to the analogue bus and is converted according to the selected gain or input range by the IAV1S-A to a 12 bit binary word.

7.5.2 Analogue Input Signals

The analogue input signals enter the module through a 50-pin male connector. A flat cable or a user made twisted-pair cable could be used for field connection.

All analogue inputs of the IAV1S-C (A029-P0) are isolated differential inputs. They have one side of the generating source connected to the positive (+IN) and the other to the negative (-IN) input pins. For correct electrical analogue input signal requirements, see chapter 7-2 "Specification".

The inputs of the IAV1S-CA are single-ended nonisolated inputs. They have one side of the generating source connected to the ANA IN and the other (Gnd on grounded instruments) to the ANA RTN pins.

Note: Both multiplexer versions have the same pin assignment for the 16 channels on the input connectors J1, see Tables 7-1 and 7-2. In application, an IAV1S-CA can be installed for an IAV1S-C if interchannel isolation, common mode voltage rejection and isolation from computer Gnd is not required.

I/O Connector Pin	Signal Name	I/O Connector Pin	Signal Name
1		2	
3		4	+IN 0 (Ch 0)
5	-IN 0 (Ch 0)	6	+IN 1 +
7	-IN 1 -	8	+IN 2 A
9	-IN 2 A	10	+IN 3 N
11	-IN 3 N	12	+IN 4 A
13	-IN 4 A	14	+IN 5 L
15	-IN 5 L	16	+IN 6 O
17	-IN 6 O	18	+IN 7 G
19	-IN 7 G	20	+IN 8
21	-IN 8	22	+IN 9 I
23	-IN 9 I	24	+IN 10 N
25	-IN 10 N	26	+IN 11 P
27	-IN 11 P	28	+IN 12 U
29	-IN 12 U	30	+IN 13 T
31	-IN 13 T	32	+IN 14 S
33	-IN 14 S	34	+IN 15 (Ch 15)
35	-IN 15 (Ch 15)	36	
37		38	
39		40	
41		42	
43		44	
45		46	
47		48	
49		50	

Table 7-1: IAV1S-C Connector J1 Pin Assignment (A029-P0)

I/O Conn. Pin	Signal Name	I/O Conn. Pin	Signal Name
1		2	
3		4	ANA IN 0 (Ana Inp. Ch 0)
5	ANA RTN 0 (Ana Ret.Ch 0)	6	ANA IN 1
7	ANA RTN 1	8	ANA IN 2
9	ANA RTN 2	10	ANA IN 3
11	ANA RTN 3	12	ANA IN 4
13	ANA RTN 4	14	ANA IN 5
15	ANA RTN 5	16	ANA IN 6
17	ANA RTN 6	18	ANA IN 7
19	ANA RTN 7	20	ANA IN 8
21	ANA RTN 8	22	ANA IN 9
23	ANA RTN 9	24	ANA IN 10
25	ANA RTN 10	26	ANA IN 11
27	ANA RTN 11	28	ANA IN 12
29	ANA RTN 12	30	ANA IN 13
31	ANA RTN 13	32	ANA IN 14
33	ANA RTN 14	34	ANA IN 15(Ana Inp Ch 15)
35	ANA RTN 15(Ana Ret. Ch 15)	36	
37		38	
39		40	
41		42	
43		44	
45		46	
47		48	
49		50	

Table 7-2: IAV1S-CA Connector J1 Pin Assignment (A029-PA)

7.5.3 Interfacing To The IAV1S-C/CA

The IAV1S-C or IAV1S-CA multiplexer boards have the same analogue inputs as the IAV1S-A A/D-Converter board, which is necessary to use the multiplexers.

Some guide lines how to interface the analogue inputs are given in Chapter 6 "Interfacing to the IAV1S-A" in the IAV1S-A description.

Refer to Differential Inputs for IAV1S-C
Refer to Single-Ended Inputs for IAV1S-CA

CHAPTER 8

IDV1S-D FIVE CHANNEL COUNTER (M7197-P0)

8.1 GENERAL DESCRIPTION

The IDV1S-D counter module (M7197-P0) consists of five 16-bit-counters, which can be programmed to count up or down in binary code. Counter channels may be concatenated to form an effective counter width of up to 80 bits. Both hardware and software gating of each counter is available. The count inputs may be controlled by either external signals or internal programming.

Outputs of each counter provide pulses or levels to external pins and may be enabled to generate internal interrupts to the Q-Bus (e.g. in the case of counter-overflow). A programmable time reference may be used for external internally timing control and can be selected as the count source for each counter.

All inputs are available with industrial opto isolation for two voltage ranges, for reliable industrial needs and TTL compatibility for high speed lab application.

A variety of SW programmable operating modes allow, for example, any inputs to be selected to any counter, active H or L levels to be selected, the rising or falling edge of signals to be selected.

IDV1S-D FEATURES

- 5 independent 16 bit counters
- external and SW controlled gating for each counter
- 5 source and 5 gate opto isolated input signals, which are high or low level input range switch selectable
- 5 source and 5 gate non-isolated high frequency input signals at TTL level
- 5 non-isolated TTL output signals (over/underflow)
- 1 programmable non-isolated TTL output signal (frequency)
- interrupt capability for counter under/overflow
- programmable up/down counting in binary code
- internal oscillator frequency source
- internal concatenating of five 16-bit counters up to one 80-bit counter
- high flexibility in selecting gate and count sources, active signal level or edge

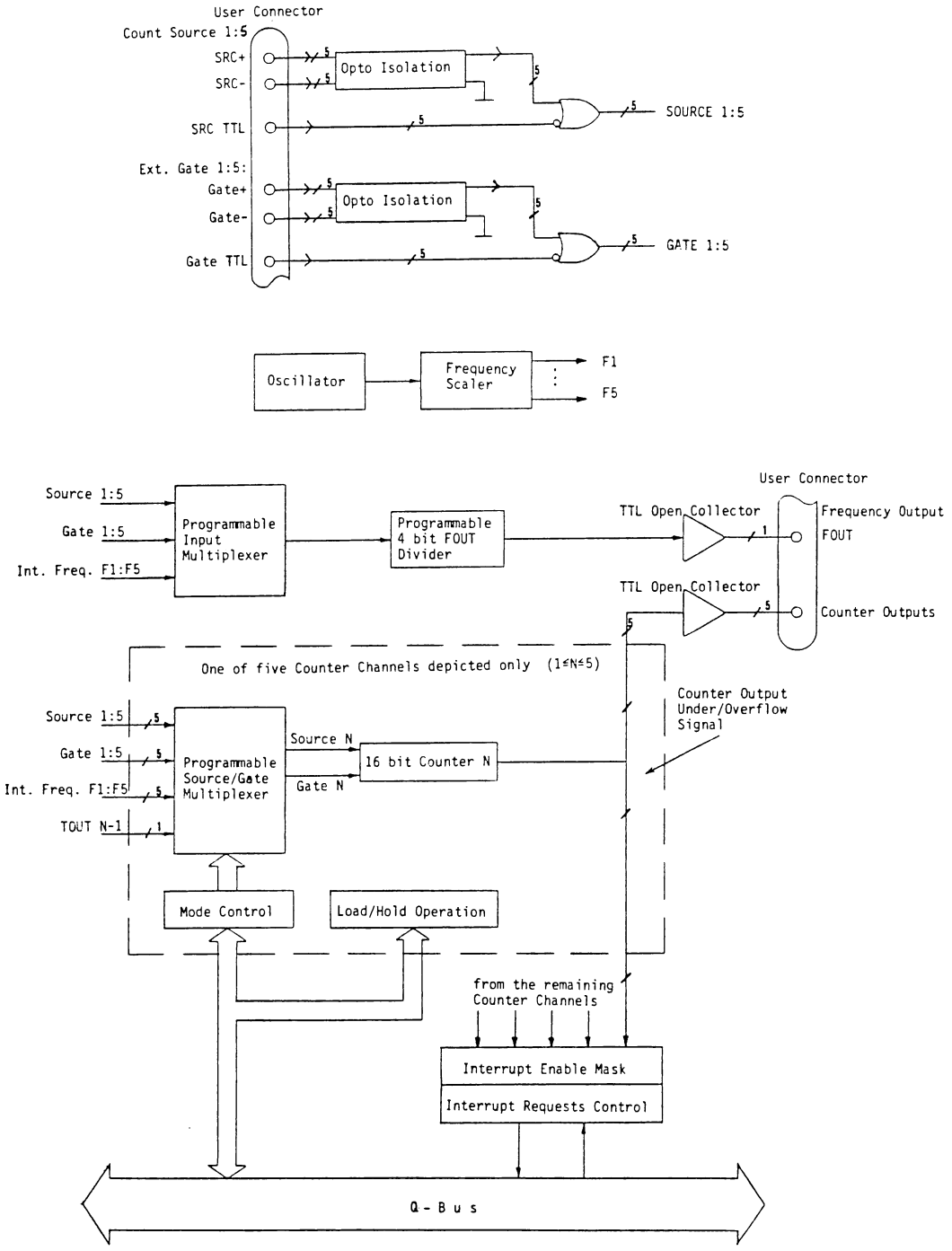


Figure 8-1: IDV1S-D Simplified Block Diagram (M7197-P0)

8.2 SPECIFICATION

GENERAL

Module Designation:	M7197-P0
Identification:	300 octal (identification code when reading SUR Register)
Module Size:	Quad high Module (for BA200 enclosures)
Power Requirements:	5,0 Vdc ±5% at 900mA
Bus Load:	1 DC Load 2 AC Loads

BUS INTERFACE

Register Addressing:	Switch selectable over 4K word I/O address range; occupies a 4 word address
Interrupt Vector:	Switch selectable from 000 to 770 octal
Priority Level:	BR4 (jumper selectable levels 5 and 6) support only position dependent configurations

OPERATIONAL

Modes

(Individually programmable for each of the five counter channels).

- Count:

Range: 0-65535 (16 bit for each counter channel,concatenated up to 80 bits by using additional counter channels).

Features:
- up/down programmable
- one of 16 input sources is software selectable for each channel
- start/stop by software or by external gate signal (active gate level (high or low) and gate source selectable)
- overflow and underflow detection
- automatic reload on counter over or underflow

maximum frequency of input source depends on the selected external input.

- Time:

- internal time reference (5 MHz) provides timing capability with an accuracy of ± 1 count $\pm$ timebase error (<100 PPM)
- start/stop by software or by external gate signal (level and gate source selectable)
- overflow and underflow detection
- automatic reload on counter over or underflow

External Input Signals

1. 10 opto isolated general purpose input signals (SOURCE 1 - 5, GATE 1 - 5) for use as count source and/or gate source.

   Specified Input Voltage (active high level):

   Low Level Range: 12 to 24 Vdc at 8 to 18mA
   High Level Range: 20 to 42 Vdc at 7 to 19mA

   The voltage input range is individually selectable by dedicated switches for each Source/Gate input (refer to Chapter 8.3.3).

   * Isolation Voltage — Inputs to Computer Gnd 200 Vdc or peak ac

   * Interchannel Isolation — 200 Vdc or peak ac

     However, due to the I/O user connector, both isolation voltages are limited to 300 Vdc or peak ac.

   Max. Input Frequency — 150 KHz for 24V input voltage (for further voltages, refer to Figure 8-2)

   * NOTE:
   The IDV1S-D has a filtered user I/O-connector to go conform with FTZ requirements.

   Connector Electrical Specifications:

Operation Voltage (Isolation Voltage)	200 Vdc or peak AC
Dielectric with standing Voltage	600 Vdc or peak AC
Capacity per Filter	375 pF $\pm$ 20%

Figure 8-2 shows the minimum input pulse duration time (maximum input frequency) for both input voltage ranges.

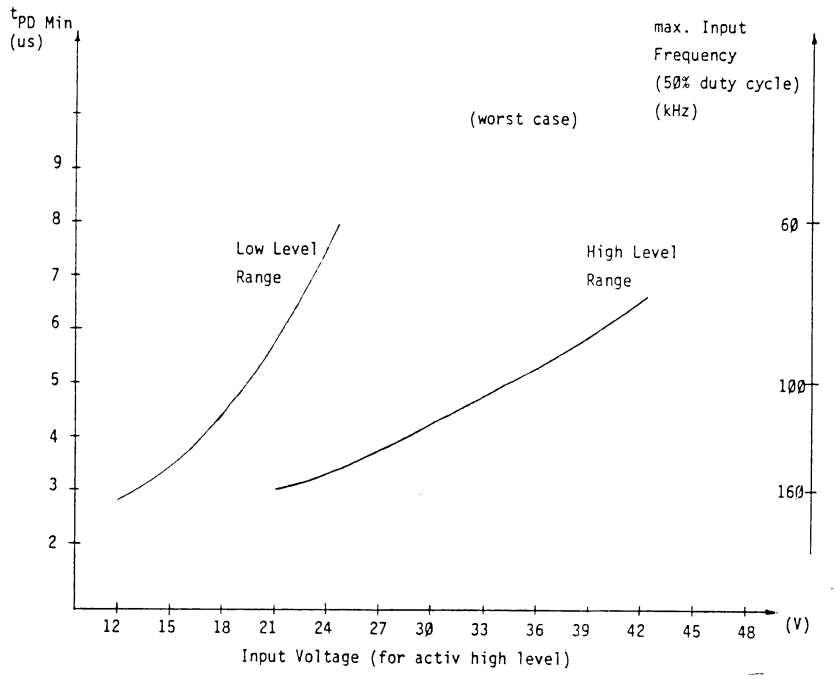


Figure 8-2: Minimum Input Pulse Duration Time

2. 10 non-isolated input signals (SOURCE TTL 1 - 5, GATE TTL 1 - 5), each a logical OR conjuction to one of the 10 opto isolated general purpose input signals.

Input Level:	TTL level, inverted signal levels as isolated inputs.
Minimum Input Pulse Duration Time:	700 ns
(Max. Input Frequency:	7.0 MHz at 50% duty cycle)

External Output Signals

5 general purpose output signals (OUT 1 - 5), referring to the corresponding counter overflow output in order to generate special timing signals (pulses, square wave, etc.).

1 general purpose timing reference signal (FOUT), programmable by the Frequency Output Control Register (refer to Figure 8-7).

For all output signals:
- non-isolated
- TTL level
- activ low
- open collector

8.3 INSTALLATION

8.3.1 Site Considerations

The IDV1S-D has two bus interface connectors that plug into a Q-bus slot. The signals are totally compatible with the Q-bus specification. The interrupt priority of the module is determined by the position on the Bus (position dependent configuration). The closer a device is located to the processor, the higher its priority.

8.3.2 INTERCONNECTIONS

Interfacing the IDV1S-D to the user's device is done via the 50 pin D-type male connector. A flat cable or a twisted pair cable may be used for field connection. The pin assignment and the signal description can be found in Table 8-6 (see chapter 8.5.2).
General information about the user I/O-connector and the physical requirements are given in chapter 1.4.6.

8.3.3 Initial Operation

Selecting the IDV1S-D Device Address

The device address is the I/O address assigned to the MOD-register. The device address is selected via a 10-pole switch (Figure 8-5). The switches allow the device to be set within a range of 160000 octal to 177770 octal. The standard address range for this module is from 171400 to 171770 in increments of 10 octal (Figure 8-3).

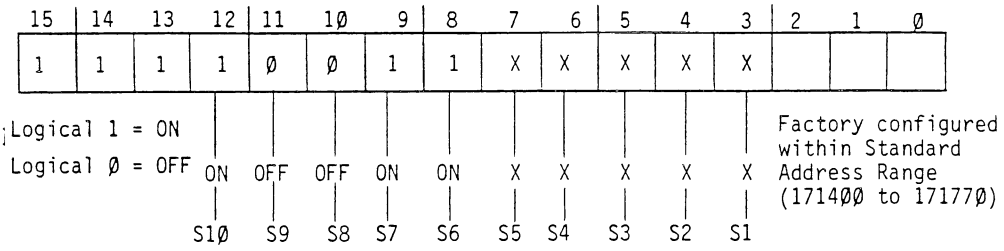


Figure 8-3: Selecting IDV1S-D Device Address

Selecting the IDV1S-D Interrupt Vector Address

The IDV1S-D is capable of generating one interrupt vector. The interrupt vector address can be set via a 6-pole switch (Figure 8-5) within the range of 0 to 770 octal in increments of 10 octal.

For standard vectors, the vector switches 1 to 6 (Figure 8-4) should have the same position as the address switches 1 to 6 (Figure 8-3). This means that the address and vector are identical for address bits 3 to 8.

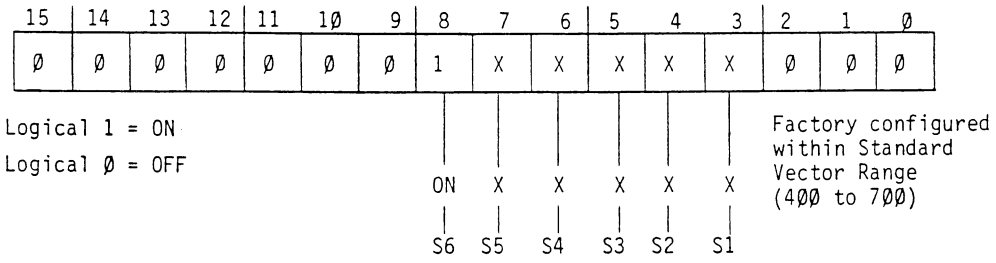


Figure 8-4: Selecting the IDV1S-D Interrupt Vector

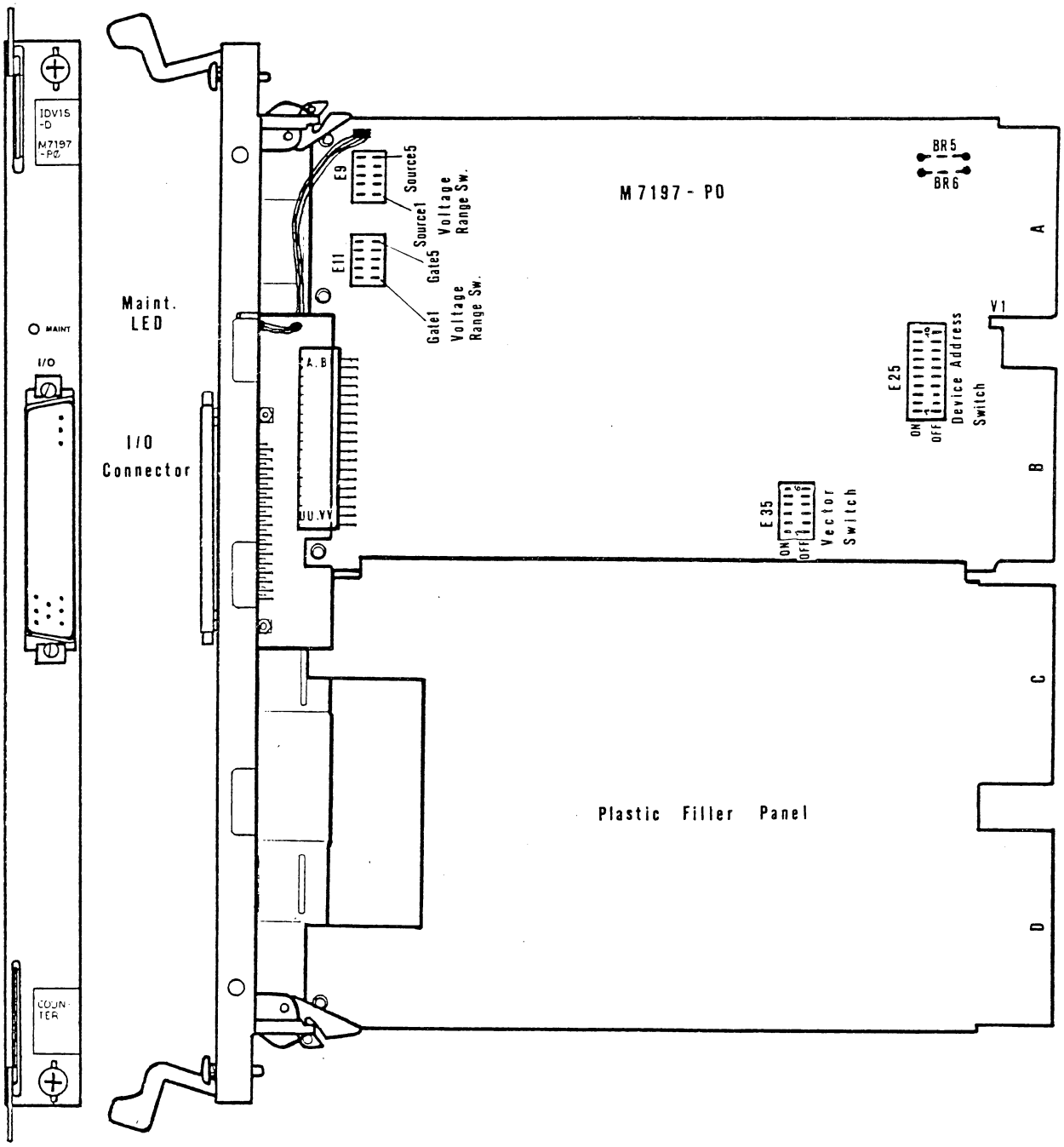


Figure 8-5: IDV1S-D Physical Layout M7197-P0

Selecting the Interrupt Request Level

The standard interrupt request level is 4 (BIRQ4). A higher request level, BIRQ5 or BIRQ6, can be selected via the jumpers BR5 or BR6 (Figure 8-5). In addition, the IDV1S-D should not be installed closer to the processor unit than any module with a higher interrupt level than itself. Whenever the BIRQ4 on the module is changed to a higher level, no other modules, which have a lower request level, should be installed on the bus closer to the processor.

Selecting the Voltage Range of External Isolated Inputs

Each isolated input signal (SRC 1 - 5, Gate 1 - 5) has one switch dedicated to it (see Figure 8-5) to select either the low level or the high level input voltage range (switch no. 1 corresponds to channel no. 1, switch no. 2 to channel no. 2, etc.). The "OFF" switch position selects the high level input voltage range (20 to 42 V). The "ON" switch position selects the low level input voltage range (12 to 24 V).

8.4 OPERATION AND PROGRAMMING

8.4.1 General

For operation, four registers are available, as listed below.

Address	Register	
171XX0	Mode Register	(MOD)
171XX2	Status and Command Register	(SCR)
171XX4	Counter Control Register	(CCR)
171XX6	Interrupt Register	(INR)

Table 8-1: Counter Register Set

INITIALIZATION

The MOD and INR register are initialized by INIT. The mnemonic INIT refers to the initialization signal issued by the processor. Initialization is caused by one of the following.

- Issuing a programmed RESET instruction
- Depressing the start switch on the processor console
- The occurrence of a power-up or power-down sequence

In order to initialize the SCR and CCR registers (and their subregisters, see Figure 8-13) a master reset command sequence has to be applied. For a detailed description, see chapter 8.4.2.1.2).

8.4.1.1 Mode Register (MOD)

The Mode Register (MOD) is generally used to identify the module by its identification code. In addition, a LED indication can be used for test purposes.

MNEMONIC	Bit	Function
IDENT 7 to IDENT 0	15 to 8	Identification Bits 7 - 0 The module is identified by theses bits (read only bits). M7197 has the code 300 octal.
LED	6	If this bit is set, a LED residing on the module will indicate a special mode (i.e. test purpose) to the user. The LED is cleared by INIT.

Table 8-2: MOD Bit Assignment

MOD - Mode Register

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IDENT								not used	LED	not used					
171XX0	7	6	5	4	3	2	1	0								
	1	1	0	0	0	0	0	0	1	R/W	1	1	1	1	1	1

R = Read Only Bit
R/W = Read/Write Bit

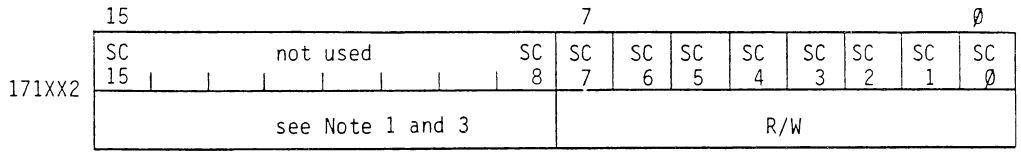
Figure 8-6: IDV1S-D Mode Register

8.4.1.2 Status And Command Register (SCR)

The 8 bit SCR Status and Command Register is a multifunctional register: commands are interpreted when writing into this register, status bits are shown when reading.

For a detailed description of this register, refer to paragraph 8.4.2.1.

SCR Status and Command Register



R = Read Only Bit
R/W = Read/Write Bit

Figure 8-7: IDV1S-D SCR Status and Command Register

Note 1: The SCR is not cleared by INIT. Bits 8 to 15 are not used. They should only be written to one and may be read as one or zero.

Note 2: In order to avoid programming errors, the following operations are not allowed for Status and Command register (SCR) and for the Counter Control register (CCR):

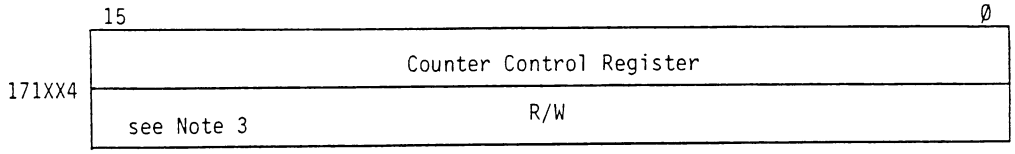
- Write Byte Instructions
- Read Modify Write Instructions (Bit Set, Bit Test, etc.)

8.4.1.3 Counter Control Register (CCR)

The Counter Control register of the Counter Module is an addressing window referring to sixteen subordinate registers: Mode registers 1-5, Load registers 1-5, Hold registers 1-5 (one set of registers for each counter channel) and to the Frequency Output Control register (independent for all counter channels). Note that the CCR is not cleared by INIT.

For detailed information of these registers refer to paragraph 8.4.2.2.

CCR - Counter Control Register



R = Read Only Bit
R/W = Read/Write Bit

Figure 8-8: IDV1S-D Counter Control Register

Note: In order to avoid programming errors, the following operations are not allowed for Status and Command register (SCR) and for the Counter Control register (CCR):

- Write Byte Instructions
- Read Modify Write Instructions (Bit Set, Bit Test, etc.)

8.4.1.4 Interrupt Register (INR)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
171XX6	MAS EN	1	1	EN 5	EN 4	EN 3	EN 2	EN 1	1	1	1	IR 5	IR 4	IR 3	IR 2	IR 1
	R/W	not used		R/W					not used			R/W			see Note 2	

R = Read Only Bit
R/W = Read/Write Bit

Figure 8-9: IDV1S-D Register Assignment

Note: The bits IR1 - 5 can only be written to zero; writing to one is not possible.

INR Interrupt Register

MNEMONIC	BIT	FUNCTION
IR1 IR2 IR3 IR4 IR5	00 01 02 03 04	"Interrupt Request Bits" One of these bits is set by the high to low transition of the corresponding counter output signal (OUT 1-5) (i.e. in case of counter under/overflow). Note that the INT bit is only set if the corresponding Enable Bit (EN1-5) is also set. Note that in order to get the interrupt functionality for counter under/overflow the counter output signal OUT N has to be achieved by setting the appropriate bits of the counter mode register (CM 0 - 2, see Figure 8-10), i.e. to "activate low OUT pulse" (CM 0 - 2 =001). The Interrupt request bit can be cleared under program control by writing to zero (hardwired implemented bit clear functionality). Writing a one has no influence as no cleared bit will be set.
EN1 EN2 EN3 EN4 EN5	08 09 10 11 12	"Interrupt Enable Bit" These bits can be set and cleared by program. Only if the Enable Bit is set, can the corresponding IR Bit be set. Previous counter over/underflows will not set the IR bit when setting the enable bit.
MAS EN	15	"Master Enable" Setting an interrupt request bit will only generate an Q-Bus interrupt if the Master Enable bit is set. This bit is cleared by the first interrupt generated to the bus (interrupt granted signal) and has to be set again (interrupt service routine) before further bus interrupt requests can be generated. It has no influence on the dedicated channel interrupt request bits (IR 1-5). In order to ensure that no interrupt requests are lost, a bus interrupt is generated even if an IR bit has been set before the MAS EN bit is set. NOTE: All bits are cleared by INIT

Table 8-3: INT Bit Assignment

8.4.2 Programming The Counter Module

Figure 8-10 is a more detailed diagram of the counter registers and the subordinate registers of the Status and Command register and of the Counter Control register.

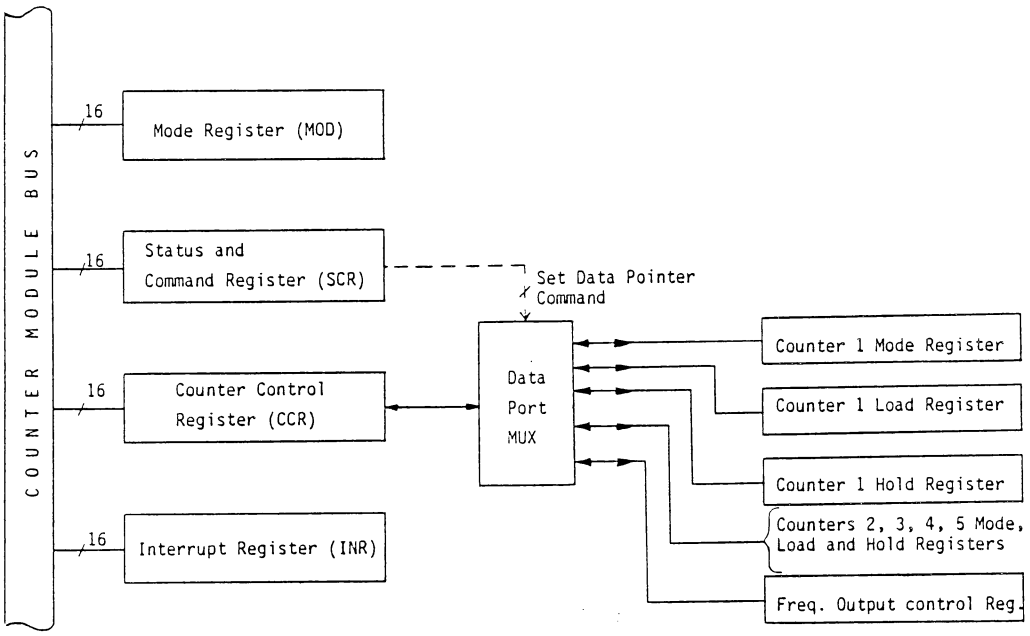


Figure 8-10: Diagram of all Subordinate Registers

As shown above, the Counter Control Register (CCR) refers to 16 sub-registers (a Load, a Hold and a Mode register for each channel plus one Frequency Output Control Register). The sub-register, reflected in the CCR, is defined by a 'Set Data Pointer' command, which has to be entered into the Status and Command register before accessing the CCR (see Paragraph 8.4.2.1.2).

8.4.2.1 Status And Command Register (SCR)

8.4.2.1.1 Status Assignment

By reading the Status and Command Register, the Status bits shown in Figure 8-11 are displayed:

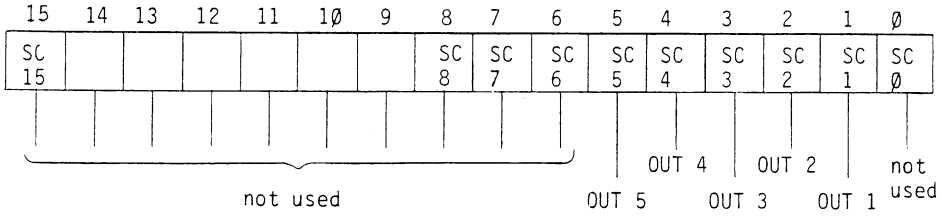


Figure 8-11: Status Register Bit Assignments

The bits SC1-5 reflect the over/underflow output signal of each counter channel (OUT1-5). Note that these bits are set to one while the corresponding output signal is in the active low state. The state of these bits changes immediately with the change of the counter outputs. They have a different function to the bits IR1-5 of the Interrupt register (INR) where an active state is stored until they are written to zero by the software (or cleared by INIT). All bits not used (0, 6-15) may be read as one or zero.

8.4.2.1.2 Command Interpretation

Table 8-4 shows all the useful commands that can be written under program control to the Status and Control register. No other codes should be used to avoid uncalculated operations.

SC 7	SC 6	SC 5	SC 4	SC 3	SC 2	SC 1	SC Ø	COMMAND DESCRIPTION
Ø	Ø	Ø	X5	X4	X3	X2	X1	Set Data Pointer to one CCR Subregister
Ø	Ø	1	S5	S4	S3	S2	S1	Arm counting for all selected counters
Ø	1	Ø	S5	S4	S3	S2	S1	Load contents of Load Register into all selected counters
1	Ø	Ø	S5	S4	S3	S2	S1	Disarm and Save all selected counters
1	Ø	1	S5	S4	S3	S2	S1	Save all selected counters
1	1	Ø	S5	S4	S3	S2	S1	Disarm all selected counters
1	1	1	Ø	1	N4	N2	N1	Set TOUT bit N (ØØ1 N 1Ø1)
1	1	1	Ø	Ø	N4	N2	N1	Clear TOUT bit N (ØØ1 N 1Ø1)
1	1	1	1	Ø	N4	N2	N1	Step counter N (ØØ1 N 1Ø1)
1	1	1	Ø	1	Ø	Ø	Ø	Initialisation Command 1
1	1	1	Ø	1	1	1	1	Initialisation Command 2
1	1	1	1	1	1	1	1	Master Reset

Table 8-4: Command Summary

Five of the above listed command types are used for direct software control of the counting process and they each contain a 5-bit S field. Each bit in the S field corresponds to one of the five counter channels (S1=Counter 1, S2=Counter 2, etc.). When an S bit is one, the specified operation corresponds to the selected counter channel (a zero in the S field has no influence), so one command can influence several counter channels. Simultaneous actions on multiple counter channels are allowed, so a software synchronisation can be achieved.

Note, that the bits 8 to 15 of the SCR register should be set to one for all commands written to the Status and Command Register (see Figure 8-10)

Arm Counter, Disarm Counter

A counter must be armed before counting can commence. If no gate is selected (refer to the mode description, chapter 8.4.2.2), the counter starts counting until the Disarm command occurs. If a gate is selected, the counter has to be armed and the gate condition must be valid before the counter starts.

When a Disarm command is entered while the counter under/overflow output Out N (N = channel number) is in the active state, the counter will not be affected until OUT N becomes inactive (OUT N becomes inactive with the next active edge of the count source). This ensures that the counter never latches up in the OUT N active state.

Load Counter

The Load Command is used to load the selected counter with the contents of the corresponding Load register (a sub-register of the CCR, see Figure 8-10). The Load command should only be used when the counter is disarmed.

Disarm and Save Counter

The Disarm and Save command will disarm the counter and immediately save the counter value into the Hold register (a sub-register of the CCR, see Figure 8-10).

Save Command

By applying the SAVE command, the contents of the appropriate counter channel (as specified in the S field) is transferred into the associated hold register. The transfer takes place without interfering with any counting that may be underway. This command allows an accumulated count to be preserved, so that it can be read by the host at some later time.

Set Output

The Set Output command sets the counter output signal OUT n in an active state (active low TTL level; corresponding SC bit of the SCR register is set). Note that the Set Output command can only be used if TOUT toggle is selected in the Counter Mode register (see Figure 8-13).

Clear Output

Clear Output command clears the OUT N signal in an inactive state (TTL high level; the corresponding SC bit of the SCR register is cleared). Note that the Clear Output command can only be used if TOUT toggle is selected in the Counter Mode register (see Figure 8-13).

Step Counter

The selected counter is incremented or decremented by one depending on its operating configuration. The Step command will take effect even on a disarmed counter.

Initialisation Command 1 & Initialisation Command 2

Both commands should always be entered after power-up and after using the Master Reset command before starting the programming of the Counter Module.

Master Reset

The Master Reset command has the same function as a power-up reset. It disarms all counters, enters zero in the Master Mode, Load and Hold registers and enters 005400 (octal) in the Counter Mode registers.

Following either a power up or software reset, the Initialisation Commands 1 and 2 should be entered. The Load command should be applied to all the counters to clear any that are in the OUT N active state. Please note, that a Master Reset selects down counting (all Mode registers are set to 005400 (octal)), so before entering a Load command to all counter channels, either the Load registers have to be loaded with a value other than zero, or the counter mode has to be changed to up counting; otherwise unerratic errors would occur, as zero is not allowed to be loaded into a down counter (refer to paragraph 8.4.2.2 Load Register). The Set Data Pointer command should also be set to a legal value in order to set the internal data pointer, since reset does not initiate it.

The command sequence listed below shows one possible reset routine

```
RESET     MOV      #177777, SCR    ;Master Reset
          MOV      #177750, SCR    ;Initialization Command 1
          MOV      #177757, SCR    ;Initialization Command 2
          MOV      #177401, SCR    ;Set Data Pointer to Mode
                                    Register of Channel 1
          MOV      #5450,   CCR    ;Select "Upcounting" for
                                    Channel 1
          MOV      #177402, SCR    ;The same for Channel 2 to 5
          MOV      #5450,   CCR    ;
          MOV      #177403, SCR    ;
          MOV      #5450,   CCR    ;
          MOV      #177404, SCR    ;
          MOV      #5450,   CCR    ;
          MOV      #177405, SCR    ;
          MOV      #5450,   CCR    ;
          MOV      #177537, SCR    ;Move all Counter Channels to
                                    ;a legal value
```

Note that an active INIT signal on the Q-Bus generates no Master Reset command to the Counter module.

Set Data Pointer

This command is used to control the Data Port multiplexer (see Figure 8-7), by selecting the internal register which is to be accessible through the Counter Control register (CCR).

Table 8-5 shows how to use the Set Data Pointer command.

Command Bits					Selected CCR Sub-register
X5	X4	X3	X2	X1	
0	0	0	0	1	Channel 1 Mode Register
0	0	0	1	0	Channel 2 Mode Register
0	0	0	1	1	Channel 3 Mode Register
0	0	1	0	0	Channel 4 Mode Register
0	0	1	0	1	Channel 5 Mode Register
0	1	0	0	1	Channel 1 Load Register
0	1	0	1	0	Channel 2 Load Register
0	1	0	1	1	Channel 3 Load Register
0	1	1	0	0	Channel 4 Load Register
0	1	1	0	1	Channel 5 Load Register
1	0	0	0	1	Channel 1 Hold Register
1	0	0	1	0	Channel 2 Hold Register
1	0	0	1	1	Channel 3 Hold Register
1	0	1	0	0	Channel 4 Hold Register
1	0	1	0	1	Channel 5 Hold Register
1	0	1	1	1	Frequency Output Control Register

Table 8-5: Data Pointer Command

By using one of the Data Printer commands listed in Table 8-6, a sub-register of the Counter Control register (CCR, refer to 8.4.2.2) is preaddressed for a direct access through the Counter Control Register (CCR).

Note that in order to correctly address the subordinate register of the Counter Control register, the contents of the Data Pointer register have to be updated immediately before each access to the Data and Mode register. This includes a reloading of the Data Pointer Command even if the same subregister in the Data and Mode register is addressed again.

8.4.2.2 Counter Control Register (CCR)

As already mentioned, each counter channel consists of a 16-bit Load register, a 16-bit Hold register and a 16-bit Mode register. These registers and the Frequency Output Control register are reflected in the Data and Mode register (see Figure 8-7), preaddressed by the Command and Status Register (Set Data Pointer command).

Load Register

The Load register is used to control the effective period of the general counter. Any 16-bit value may be written into the load register but it is not recommended that it be loaded with zero or one if down counting is selected (for up counting, it should not be loaded with 177777). The contents of the Load register are transferred into the counter by the Load command (refer to chapter 8.4.2.1.2 "Command Interpretation"). The contents is reloaded into the counter on each counter under/overflow.

Hold Register

The 16-bit Hold register can be used to store accumulated counter values for later transfers to the host processor. Transfers of the counter contents into the Hold register are done by using the DISARM AND SAVE or the SAVE command (see Table 8-4 Command Summary).

Frequency Output Control Register

The 16-bit Frequency Output Control register is an additional register controlling the FOUT reference signal which is provided to the user cable for external timing control. The bits MM4 to MM7 of the Frequency Output Control register (see Figure 8-9) select between fifteen different sources (F1-F5 : internal timing signal defined by the internal 5 MHz clock, SRC1-SRC5 : input sources of the five counter channels, GATE1-GATE5 : gate inputs of the five counter channels), the bits MM8 to MM11 specify the dividing ratio for the 4-bit FOUT Divider and bit MM12 disables the FOUT signal if it is set.

After power up, all the bits of the Time Reference register are set to zero (FOUT is On, F1 = 5 MHz divided by 16 is selected).

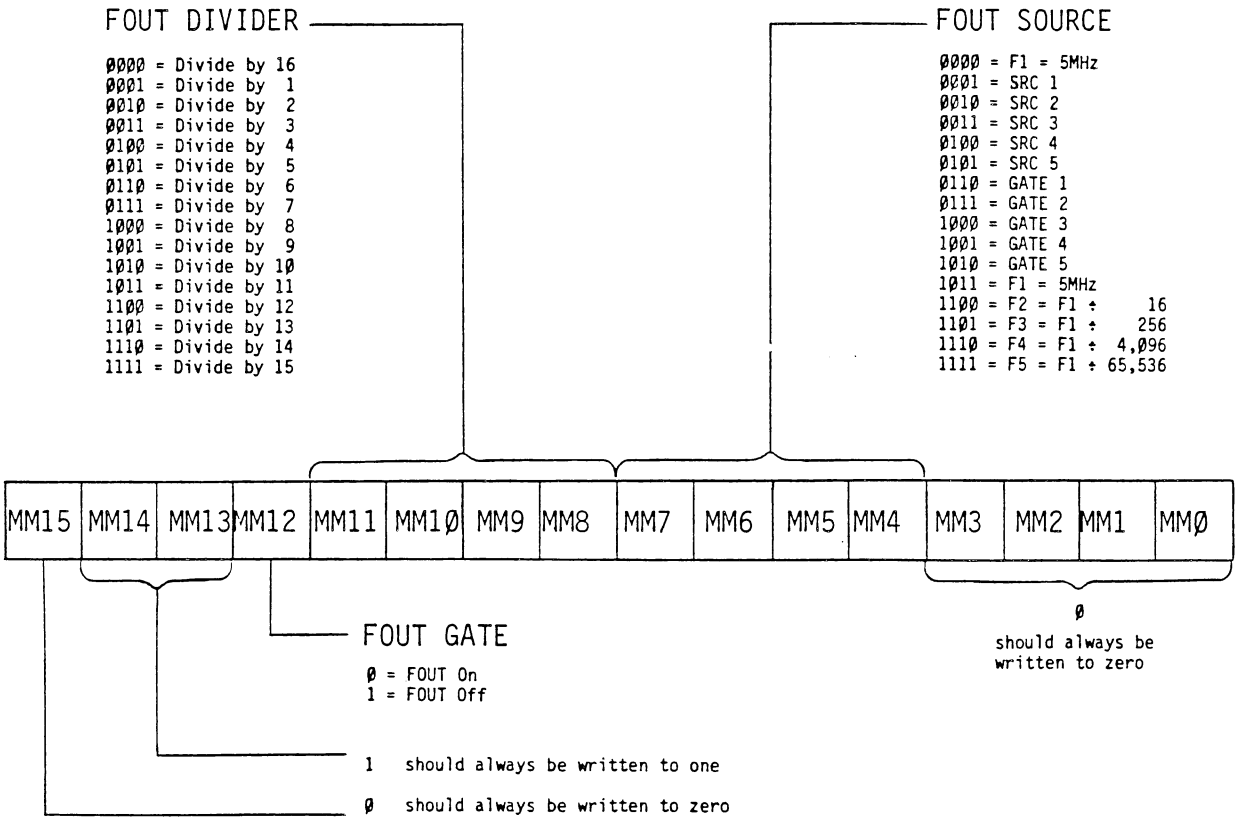


Figure 8-12: Frequency Output Control Register Bit Assignments

Mode Register

The 16-bit read/write Channel Mode register controls the gating, counting, output and source select functions of one counter channel.

The counter mode of each channel is defined by the corresponding Counter Mode register (see Figure 8-13).

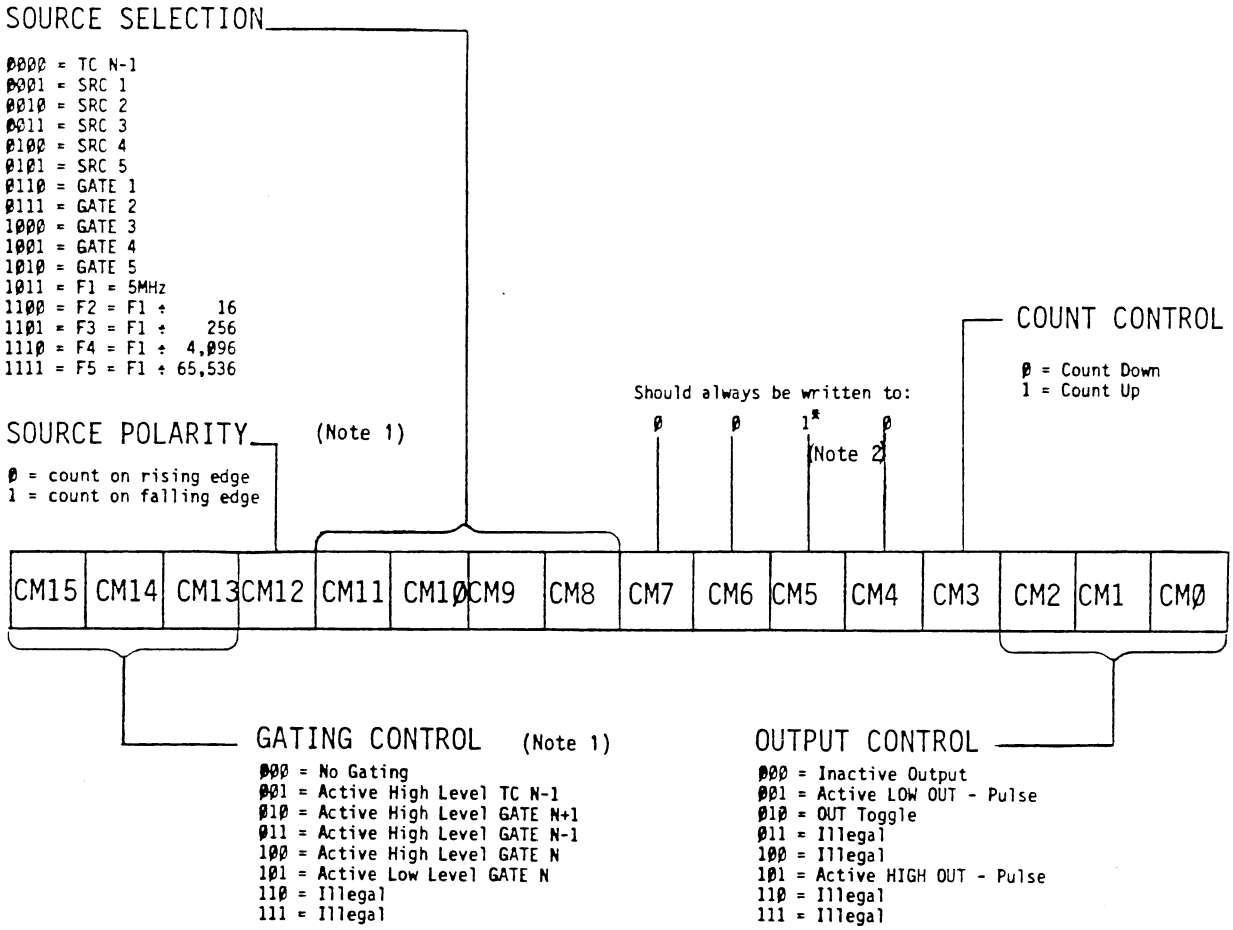


Figure 8-13: Channel Mode Register Bit Assignments

Notes 1. Active level assignment corresponds to isolated input signal, the levels of nonisolated inputs are inverted.

2. The CM5 bit is cleared after power up and should be written to one when defining the counter mode.

The Channel Mode register should only be loaded when the counter channel is disarmed, otherwise erratic counter operations may result.

- Output Control

The counter mode bits CM0 to CM2 specify the output control configuration (refer to Figures 8-13 and 8-14).

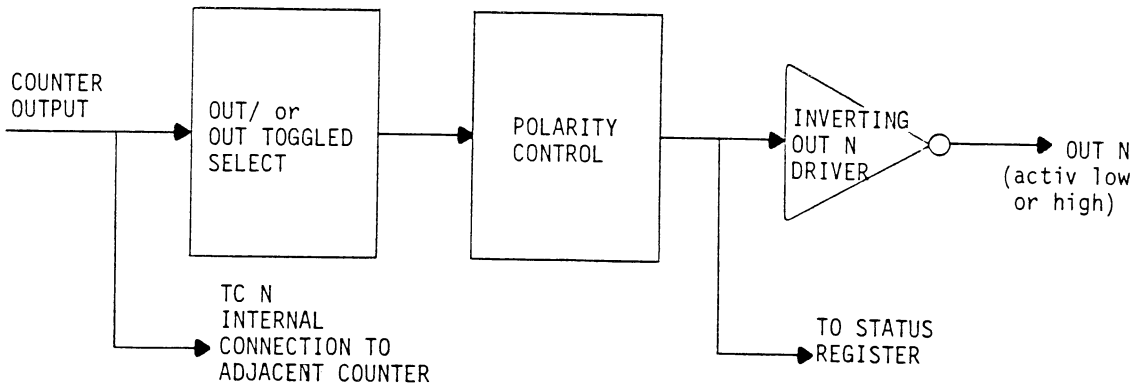


Figure 8-14: Output Control Logic

One available output mode is called OUT Pulse. The timer output OUT becomes active (low or high may be selected) at the next count when the counter is at 0001 for down counting or 177777 (octal) for up-counting. The OUT N pulse width is defined by the period of counting source. Figure 8-15 shows this timing assuming an active high source polarity, counter armed, counter decrementing and a reload value of K (K is the contents of the Load register and is reloaded after each counter overflow).

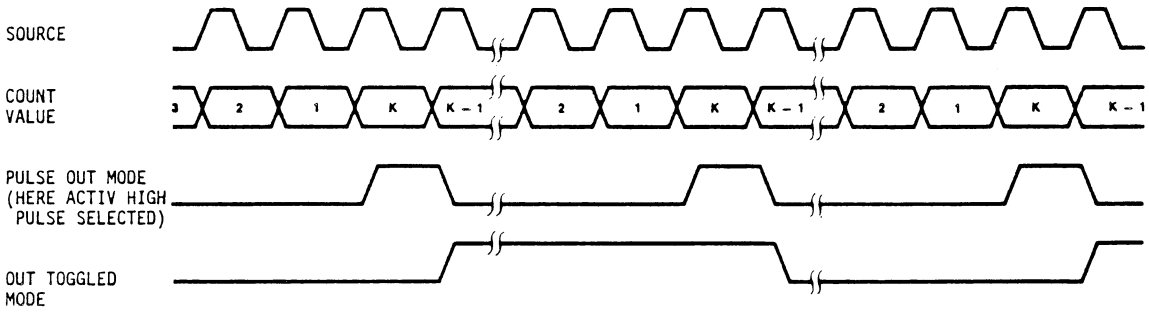


Figure 8-15: Counter Output Waveforms

The other output form, OUT N toggled, uses the trailing edge of OUT N to toggle a flip-flop to generate an output level instead of a pulse.

Note that if the reload value K is 1 for down-counting or 177777 (octal) for counting up, the OUT N signal will drive active regardless of whether the counter is disarmed or gated off. As long as this value is reloaded by the Load register, OUT N remains active.

Note that the corresponding Status bit of the SCR register is set while the OUT signal is in an active low state, and that it is zero while the OUT signal is in the high state.

Please remember that the counter is always in a repetition mode, a counter once armed (and gated on) will never stop and will always be reloaded from the Load register on counter overflow (reaching the value of 0001 or 177777 (octal)) until the counter is disarmed or gated off.

- Count Control

Bit CM3 is used to select up and down counting (down mode is selected after power-up).

- Source Count Selection

Channel Mode bits CM8 to CM11 specify the source used as input to the counter. Bit CM12 controls the polarity for all sources. One of sixteen count sources can be selected: five internal frequencies are available (defined by the 5MHz internal time base), five different input signals (SRC1-5) and five gate signals (Gate 1-5), supplied from the user connector. The 16th available input is an internal timer-output signal (TC N-1) from the adjacent lower-numbered counter (the counter 5 output wraps around to the counter 1 input). This option allows internal concatenating up to 80 bits. The internal TC signal provides the inverted level of the external OUT signal for use as source (or gate) input.

- Gating Control

Bits CM13 to CM15 specify the hardware gating options: If "no gating" is selected, the counter will proceed unconditionally as long as armed. A level active gate allows counting only when the gate is in the active level. If the gate becomes inactive, the counter stops and will start at the same count value when the gate is active again. Up to three gate inputs are available for one counter (not at the same time), but only one can be used for low level active. Note, active level assignment corresponds to the isolated input signal, the levels of the non-isolated inputs are inverted.

A 001 code in this field selects the internal timer output of the adjacent lower numbered counter as a gate (TC N-1 always has the opposite level to that of the external OUT signal, refer to Figure 8-14). This code can be used to generate a counting "window" by the adjacent lower numbered counter channel (TC5 is wrapped around to channel 1).

8.4.2.3 Application Examples

8.4.2.3.1 Event Counting

The following describes a counter set-up for generating an interrupt to the host processor after counting a defined number of external pulses. In this example, counter channel 1 should generate an interrupt after five pulses have been counted on Source 1.

The disarmed counter channel 1 (e.g. after a Master Reset Sequence, refer to paragraph 8.4.2.1.2) is initialised by loading the Channel 1 Mode register with 000441 (octal) to down counting of the rising edge of Source 1 with no gating or active low pulse selected. The Load 1 register is written to 5, then the channel 1 interrupt request is enabled by setting the EN1-bit and MAS EN-bit in the INR. After entering the load command for channel 1 (177501 octal) in the SCR, the Load register value of 5 is transferred to the counter channel. By entering the Arm command for channel 1 (177441 octal) in the SCR, channel 1 starts down-counting the rising edges of Source 1. After four pulses from Source 1, the counter value of 1 is reached. With the next source edge, instead of counting down to zero (no legal value for down-counting), the counter reloads the value of the load register (in this case 5) and generates one active low OUT pulse for the period of one count. With the high to low transition of the OUT signal (counter underflow from one to five), the IR1 bit in the Interrupt register (INR) is set and

an interrupt request is generated to the LSI bus. The counter continues counting until it is disarmed. To avoid further interrupts on counter underflows, the counter module automatically clears the Master Enable bit in the INR. However, in the interrupt service routine, the counter channel should be disarmed and the IR1 bit in the INR cleared.

8.4.2.3.2 Pulse Duration Measurement

To allow time measurement of an external pulse, one counter channel can be set up to count the internal reference clock (e.g. 5 MHz), which is gated by the external pulse signal. For example, the Mode register of channel 1, which counts 5 MHz while the signal on Gate 2 input is in an active high state, has to be loaded with 105450 (octal) and the Load register set to zero. After applying the Load and the Arm command to this channel, the counter starts up counting immediately with the low to high transition of the Gate 2 input. The counter channel stops counting when the Gate 2 input becomes inactive (high to low transition of the external pulse). The count value (number of 5 MHz clock edges) is shown in the Channel 1 Hold register after applying either the Hold or the Hold and Disarm command to the counter channel. Note that the counter continues counting if further pulses on the gate input occur and if no Disarm command is issued to the counter channel.

However, before disarming the counter and reading the count value, an interrupt is required to recognize the end of the gate pulse (high to low transition). This interrupt can be generated by using an additional counter channel (e.g. channel 2), and by counting the falling edges of Gate 2 input or when the system is initialised to down counting, preloaded with 1 and interrupt enabled on counter underflow. Basically, this channel operates in the same manner as the event counting application described in paragraph 8.4.2.3.1 except that a preload by writing the Load register to one is not allowed for down counting. Therefore, the Load register has to be loaded with the value of two and a Step command has to be applied between the Load and Arm commands, stepping the counter value down from 2 to 1. The next active input edge (here the falling edge at the end of the pulse on Gate 2) causes an underflow on channel 2 (reload to the load value of 2) and an interrupt then identifies the end of the gate input pulse. In response to the interrupt, the host processor has to disarm both channels, reading the Hold register value after applying the Hold command to channel 1 and getting the final result by dividing the counter 1 Hold value by 5MHz.

8.4.2.3.3 Output Signal Generation

In addition to using the FOUT signal for generating output frequencies (defined by the Frequence Output Control Register), any of the counter overflow outputs OUT N are able to generate output pulses at defined time intervals. Counting one of the five internal reference frequencies (F1 - F5) and loading the counter channel with the preloaded value of 'n' (down counting selected) would generate an active high or active low output pulse on the OUT signal (depending on whether the active high or active low TOUT pulse mode is selected in the Counter Mode register).

8.4.2.3.4 Frequence Output Generation

Frequence Generation on the FOUT signal is controlled by the Frequence Output Control register. To get a quarz controlled output frequence, one of the internal reference frequencies available F1 - F5 should be used as FOUT SOURCE (refer to Figure 8-12). Due to the fact that the FOUT divider can only be programmed to values between 1 and 16, only a limited range of FOUT frequencies is available for the user.

8.4.2.3.5 Pulse Output Generation

In addition to the FOUT signal, the counter over/underflow output signals OUT 1 - 5 can be used for timing control purposes of external user devices. A counter channel, preloaded with the value of 'n' and programmed to down counting, would underflow every 'n' clock edge. Depending on the output control mode defined in the Channel Mode register (refer to Figure 8-13) on counter underflow, the OUT signal would becomes active high or active low for one clock cycle (depending on whether the active high OUT pulse or active low OUT pulse is selected); e.g. for the count source of F2=5 MHz divided by 1b and with a load of 100 (decimal), an OUT pulse of 1.6 microseconds would be generated every 160 microseconds. In selection of the OUT toggle mode for the Channel Output control, the level of the output is changed every underflow, so that an output frequency with 50% duty cycle is generated (in this example with a period cycle of 320 microseconds).

Please note, that only the active low OUT pulse mode is supported by the software driver for the IDV1S-D.

8.4.2.3.6 UP/DOWN Counting

Normally, up/down counting should be no problem for the channel module: one counter is initialized for down counting and armed. For changing count direction, use the bit CM3 in the Channel Mode register. First, the counter channel has to be disarmed, the CM3 bit has to be changed and the counter has to be armed again. This method has the disadvantage that it is controlled by software and so no accurate gating can be simulated.

For an introduction to the highly versatile use of the counter mode, the application should be shown with the up/down mode controlled by the hardware gate (see Figure 8-16).

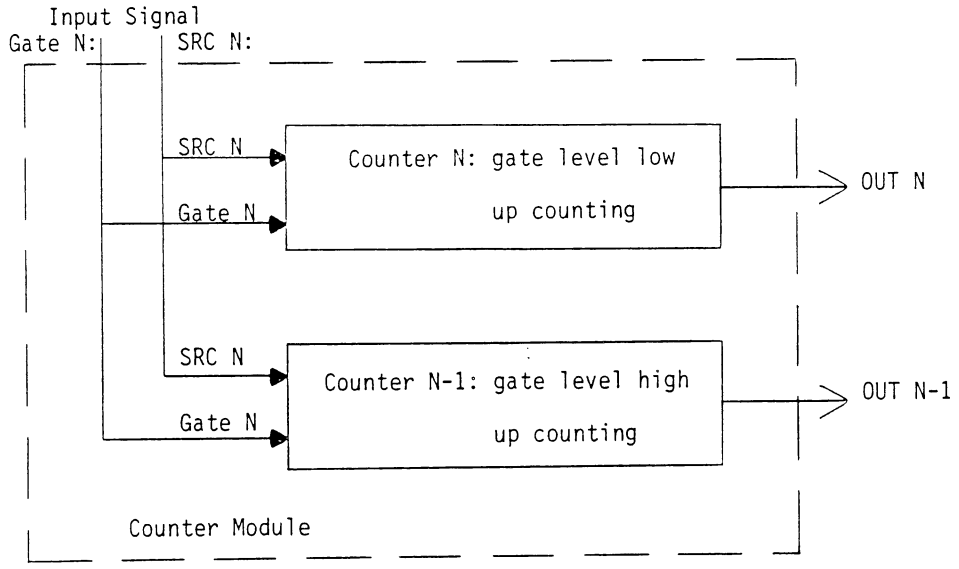


Figure 8-16: UP/DOWN Counting Controlled By Gate-Signal

In this application, using two counter channels, both up-counting, only one counter is active depending on the level of the gate signal. To get the same count value as in an application with one counter working up and down, the difference of the contents of both counters has to be calculated by software. The advantage of this arrangement is the direct control of the up/down mode by a hardware gate, so no input counts can be lost.

Note that there are problems when one gate edge and one active input signal edge occur at the same time, because one input edge may count both counters or none, so the count may be counted twice or lost. To avoid this problem, the arrangement can be changed so that only one counter is gated, the second should always count. The final result can be calculated by subtracting the double value of the gated counter from the value of the non-gated counter. In this case, no count is lost because one counter is always counting and the second counter may get the raising edge of the input signal or not, so the insecurity in the counting value is only one (allowed by input and gate edge at the same time) instead of two by gating two counters.

If the count value of these pseudo up/down counters exceeds the 16-bit range, the counters may be concatenated up to 32-bits or may be extended by a software counter (software counts the number of interrupts that occur on counter overflow).

8.4.2.3.7 Concatenated Counter Channel

Concatenated counter channels are typically used either to count a high number of events (which exceed the 16 bit range) or to enable a high resolution for time measurement or output signal generation.

To simplify concatenation, the counter module provides an internal TC signal from the low order counter, which can be selected as count source (or as gate control signal) in the high order counter's Counter Mode register.

Thus, although any two counter channels can be concatenated with external strapping (note the level of the TC and OUT signal, see Figure 8-1Ø). Usually, adjacent counter channels are used to enable the use of this internal TC signal.

In count up concatenation, both the high and low ordered counter's Load registers should be cleared to zero. The low order counter channel will start counting from 0 and increment through 177777 (octal). On the next active source edge, the TC output of the low order counter channel becomes active and increments the high order counter channel (the low order counter channel reloads 0 from Load register).

This counter configuration is shown in Figure 8-17.

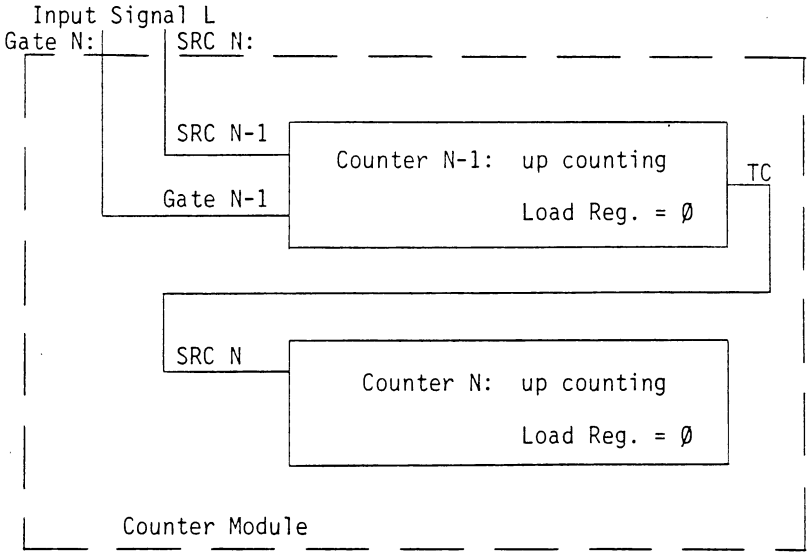


Figure 8-17: Concatenation Counter

8.5 FUNCTIONAL DESCRIPTION

8.5.1 Theory Of Operation

This chapter provides a more detailed description of the Five Channel Counter module. The block diagram, shown in Figure 8-15 gives a brief technical overview of the counter components. The engineering drawing set should be available to the reader for detailed consideration of each component described in the next paragraphs.

Counter Chip

The kernel of the Five Channel Counter Module is the AM 9513A System Timing Controller. This VLSI counter chip includes the logic groups of counters 1-5, 8-bit Command register, bus buffer and Mux, 16-bit Counter Frequency Scaler and the 4-bit FOUT Divider. Programming of the timer chip is done by using the data and control port (referring to the registers SCR and CCR), which consists of 16 data bits and the timing control signals CS, C/D, RD and WR.

The counter chip is provided with a 5MHz clock signal, in order to get time measurement capability. The time reference is generated by a 10MHz crystal (divided by two to get 5 MHz clock source). The same crystal controls the Read/Write control logic and a Glitch rejection logic. Due to the fact that the OUT 1 - 5 signals (output signal of the AM 9513A corresponding to the counter over/underflow detection on each channel) may generate signal spikes when programming the AM9513A chip. A synchron implemented glitch rejection logic is added to each OUT signal, in order not to generate undesired interrupt request (if enabled).

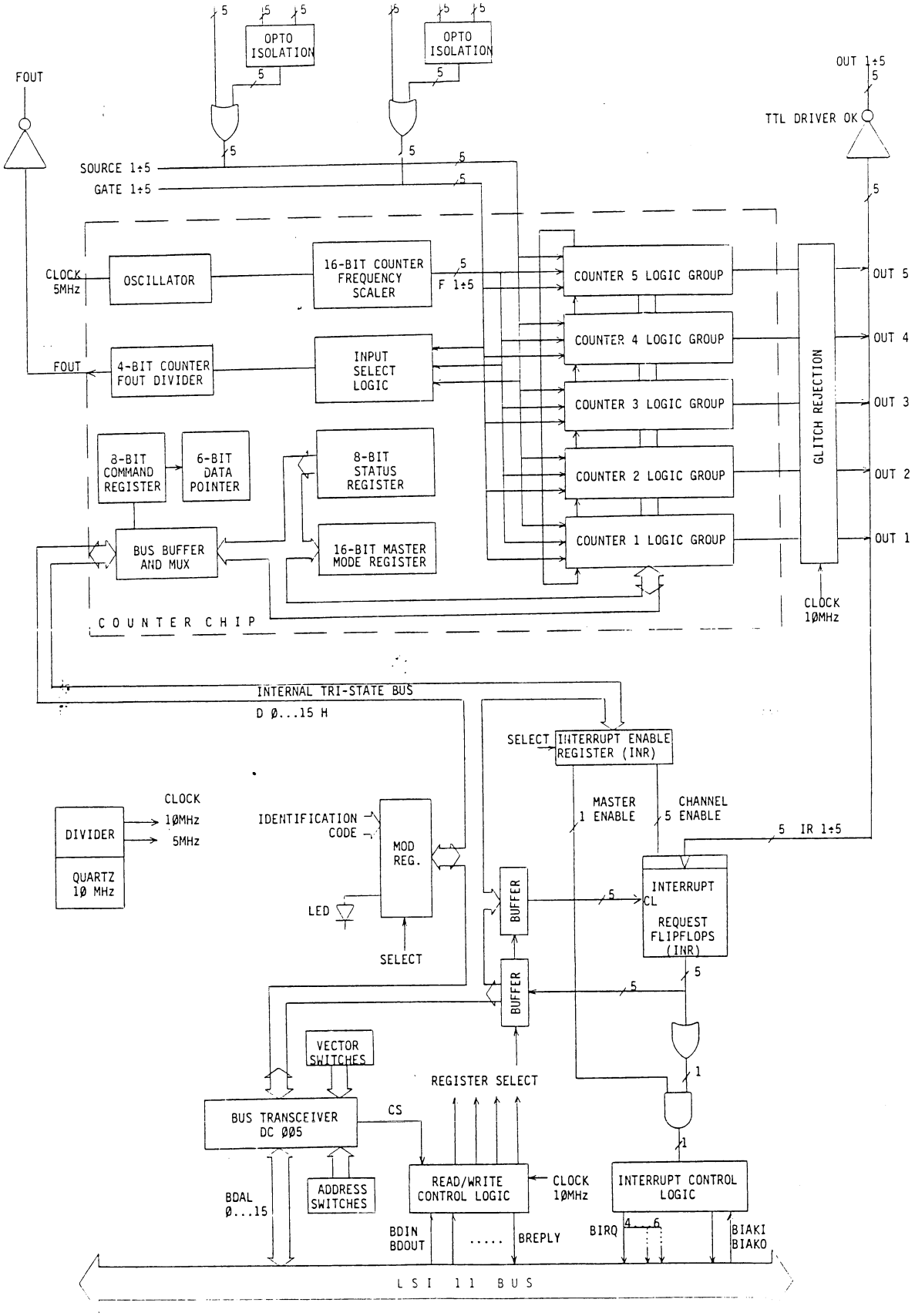


Figure 8-18: IDV1S-D Simple Block Diagram (7197-P0)

Q - Bus Interface

Interfacing the internal Tri-state bus D0-15 (the AM 9513A counter chip requires access by a Tri-state bus) to the Q-bus data/address BDAL 00-15 is done by four DC005 chips, which in addition compares the bus address to the switch selected module address. The interrupt vector (switch defined) is also provided on the LSI bus.

Additional read/write control logic (LSI/MSI implementation) provides timing control for read/write access to the module. In order to meet the AM 9513A timing requirements, the REPLY signal (read/write acknowledge) is delayed by a clocked delay element (implemented as part of the "Glitch Rejection" logic).

Interrupt Capability

Each of the five output signals OUT 1 - 5 (over/underflow signal for each counter channel) clocks one interrupt request (IR) flipflop. The IR flipflops are set only if the corresponding bit in the interrupt enable register is valid. If one or more IR flipflops are set, a Q-bus interrupt will be generated. The prerequisite "Master Enable" bit in the interrupt register is set. The interrupt control logic handles the Q-bus interrupt sequence and if interrupt is granted it resets the master enable bit, so further interrupts are disabled until the interrupt service routine enables them by setting the master enable bit again. Every internal pending interrupt request (one IR flipflop is set) immediately generates a Q-bus interrupt request when setting the master enable bit. It is recommended that the interrupt service routine scans every internal pending interrupt request (INR register) before enabling new Q-bus interrupt requests (set master enable bit).

User Signal Interface

Each counter input signal (Source 1 to 5, Gate 1 to 5) is supplied by a NAND Schmitt Trigger gate, a logical conjunction of the non-isolated and the isolated user input signal.

The opto coupler providing isolated input signal is calculated for a wide input range, which has, additionally, two input ranges which can be switched. A minimum input current of 6,7mA is required in order to switch a maximum collector current of 0,8mA, so the maximum input voltage is limited by the power dissipation of 0,4 watt for each input resistor.

8.5.2 User Input Signals

The IDV1S-D has a 50-pin D-type male connector for user inputs. A flat cable or a user made twisted pair cable should be used for field connection.

Table 8-6 shows the pin assignment of the User Connector

I/O Conn. Pin	Signal Name	I/O Conn. Pin	Signal Name
1	SOURCE 1 +	2	SOURCE 1 -
3	SOURCE 2 +	4	SOURCE 2 -
5	SOURCE 3 +	6	SOURCE 3 -
7	SOURCE 4 +	8	SOURCE 4 -
9	SOURCE 5 +	10	SOURCE 5 -
11	GATE 1 +	12	GATE 1 -
13	GATE 2 +	14	GATE 2 -
15	GATE 3 +	16	GATE 3 -
17	GATE 4 +	18	GATE 4 -
19	GATE 5 +	20	GATE 5 -
21	GND	22	GND
23	SOURCE TTL 1	24	GATE TTL 1
25	SOURCE TTL 2	26	GATE TTL 2
27	SOURCE TTL 3	28	GATE TTL 3
29	SOURCE TTL 4	30	GATE TTL 4
31	SOURCE TTL 5	32	GATE TTL 5
33	OUT 1	34	OUT 2
35	OUT 3	36	OUT 4
37	OUT 5	38	FOUT
39	GND	40	GND
41		42	
43		44	
45		46	
47		48	
49		50	

Table 8-6 IDV1S-D Connector J1 Pin Asssignment (M7197-P0)

APPENDIX A

Q-BUS I/O MODULE SET OPTION LIST

The following Shipping List shows which components are included in each option.

Ordering can be done by option name or as single parts only.

The test equipment is not a part of the option or module shipments, but can be ordered by the user separately.

DIGITAL EQUIPMENT CORPORATION

SHIPPING LIST

ITEM NO.	DWG NO. / PART NO.	DESCRIPTION	QUANTITY / VARIATION											
			IDV1S-A	IDV1S-B	IDV1S-C	IDV1S-D	IAV1S-A	IAV1S-AA	IAV1S-B	IAV1S-C	IAV1S-CA	IADV1-MA		
1	M5026-P0	16 Bit Opto Isolated Input Module	1											
2	M6029-P0	16 Bit Opto Isolated Output Module		1										
3	M8005-P0	16 Bit Relay Output Module			1									
4	M7197-P0	5 Channel Counter Module				1								
5	A410-P0	4/12 Channel Counter Module					1							
6	A410-PA	16 Channel A/D Converter Module						1						
7	A6007-P0	4 Channel Isolated D/A Converter Module							1					
8	A029-P0	16 Channel Flying Cap. Exp. MUX Module								1				
9	A029-PA	16 Channel Expansion MUX Module									1			
10	2G-E091A-00	MUX Board T-Type Expansion Cable								1	1			
11	YG-C04UC-00	Q-Bus I/O Modules Option Description	1	1	1	1	1	1	1	1	1			
12	DD-M5026-P0	Drawing for IDV1S-A0	1											
13	DD-M6029-P0	Drawing for IDV1S-B0		1										
14	DD-M8005-P0	Drawing for IDV1S-C0			1									
15	DD-M7197-P0	Drawing for IDV1S-D0				1								
16	DD-0A410-P0	Drawing for IAV1S-A0					1							
17	DD-0A410-PA	Drawing for IAV1S-AA						1						
18	DD-A6007-P0	Drawing for IAV1S-B0							1					
19	DD-IAV1S-C0	Drawing for IAV1S-C0								1				
20	DD-IAV1S-CA	Drawing for IAV1S-CA									1			
21	2G-M002A	Digital I/O Board Test Connector										1		
22	2G-M003A	Analogue Input Test Connector										1		

TITLE Q-BUS I/O MODULE SET

SHEET 1 OF 2

REV. A

DIGITAL EQUIPMENT CORPORATION

SHIPPING LIST

ITEM NO.	DWG NO. / PART NO.	DESCRIPTION	QUANTITY / VARIATION											
			IDV1S-A	IDV1S-B	IDV1S-C	IDV1S-D	IAV1S-A	IAV1S-AA	IAV1S-B	IAV1S-C	IAV1S-CA	IADV1-MA		
23	2G-M00AA	Analogue Current Output Test Connector										1		
24	2G-M009A	Analogue Voltage Output Test Connector										1		
25	2G-M00BA	Five Channel Counter Test Connector										1		
26	2G-E10SA-0L	Adaptor Cable for Testconnectors										1		
27	2G-E010JA-00	Adaptor Cable for Screw Terminal (0.5m) see Note 1)												
28	H3031-B	Screw Terminal 2 x 40 Points see Note 1)												
29	* ZNA06-C5	MDM Diagnostic (MicroVAXII) TK50												
30	* ZNA06-C3	MDM Diagnostic (MicroVAXII) RX50												
31	* ZYA05-P5	XXDP+ Diagnostic (PDP) TK50												
32	* ZYA05-P3	XXDP+ Diagnostic (PDP) RX50												
33														
34														
35														
		Notes: 1) as required (can be ordered from CSS)												
		* Supplied by SDC												

TITLE Q-BUS I/O MODULE SET

SHEET 2 OF 2

REV. A

APPENDIX B

FIELD TEST EQUIPMENT

For the IXV11 and IXV1S industrial I/O module sets, some test equipment is available for easier checkout of the module I/O circuits in the field. This test equipment may be used with or without the diagnostic tests.

The following equipment will be needed to carry out a calibration adjustment using the diagnostic program.

- For the digital-to-analog-converter options.

  Digital voltmeter (DVM), accuracy 0.01%

- For the analog-to-digital-converter option.

  High-quality dc-voltage source, 0 to 10V, accuracy 0.01%

The diagnostic programs available from SDC for testing the IxV11- and IxV1S-modules are:

Part Number	Name	Processor	Medium
ZYA05-P5	XXDP+	PDP	TK50
ZYA05-P3	XXDP+	PDP	RX50
ZNA01-C5	MDM	MicroVAXII	TK50
ZNA01-C3	MDM	MicroVAXII	RX50

The following test connectors can also be used on IxV11-modules when bulkhead panels are installed and on IxV1S-modules (BA200 series enclosure versions) which have only a 50 pin D-connector. For both the adaptercable 2G-E10SA-0L has to be used which reconverts from the 50 pole D-type connector to the 40 pole module connector standard of the test connectors (see figure below).

List of Test Connectors

Part Number	Test Connector Type
2G-M002A	Digital-I/O test
2G-M003A	Analog-input test
2G-M009A	Analog-voltage-output test
2G-M00AA	Analog-current-output test
2G-M00BA	5-channel-counter test

TEST CONNECTOR ADAPTER CABLE

The adapter cable 2G-E10SA-0L is needed to install the testconnectors (described in Appendix B) on the IxV1S module family or on IxV11-modules with 50-pole male D-connector Bulkhead Panels.
The adapter cable reconverts the 50-pole D-connector to the 40-pole module connector standard of the test connectors.

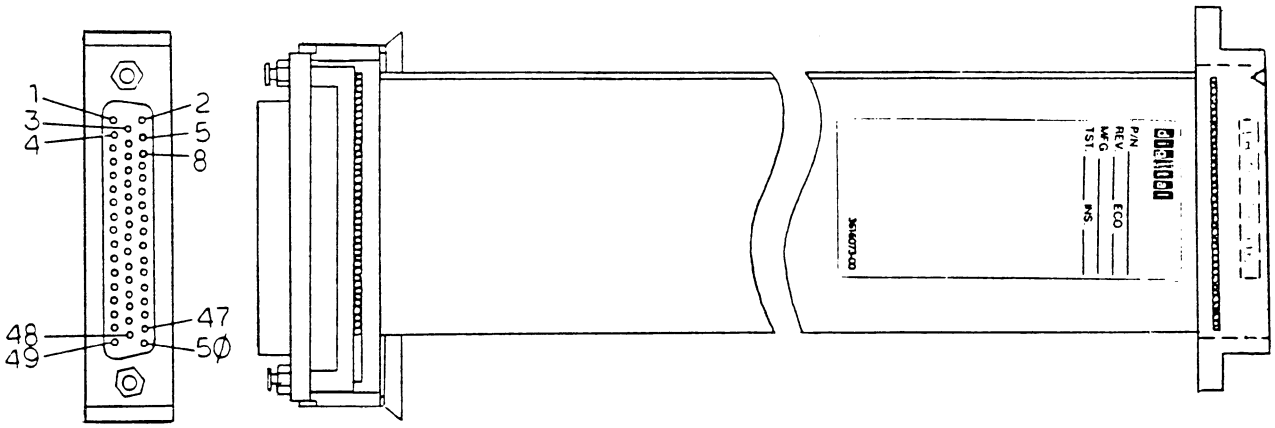


Figure B-1: Test Connector Adapter Cable

DIGITAL I/O TEST CONNECTOR

This test connector may be plugged directly in the I/O connector J1 of the digital I/O modules M5026-P0, M6029-P0 and M8005-P0.

The function of the test connector is automatically configured for input or output modules when the connector is installed.

With output modules, the LED's 0 to 15 monitor the desired bits in the modules' output data register (DAT) and the output circuit. If a bit in the DAT register is set to "1", the same LED has to light up.

With input modules, the LED's 0 to 15 can be switched by the on-board switch (see figure B-1) for even inputs and for odd inputs. Reading the input data register should give the same data pattern.

The digital I/O test connector only checks the principal functions of the digital I/O circuits, but not the whole electrical circuit specification.

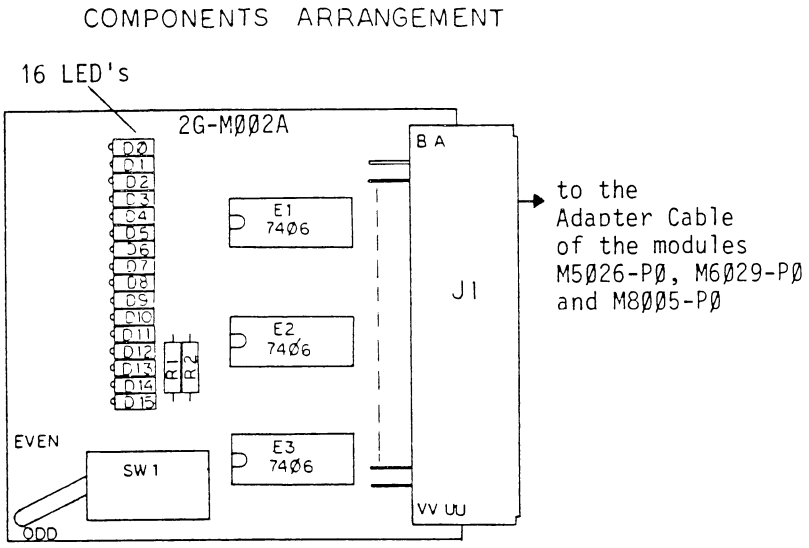


Figure B-2: Digital I/O Test Connector

The test connector is supplied with +5Vdc from the testing module. Therefore, the I/O circuits are only checked with 5 volt.

ANALOGUE INPUT TEST CONNECTOR

This test connector may be used for the analogue input modules A410-P0 and A029-P0 (and its variations) to supply the 16 channels with an external calibration source.

There are 3 pins on the connector printed circuit board (see figure B-2), where the calibration source can be connected.

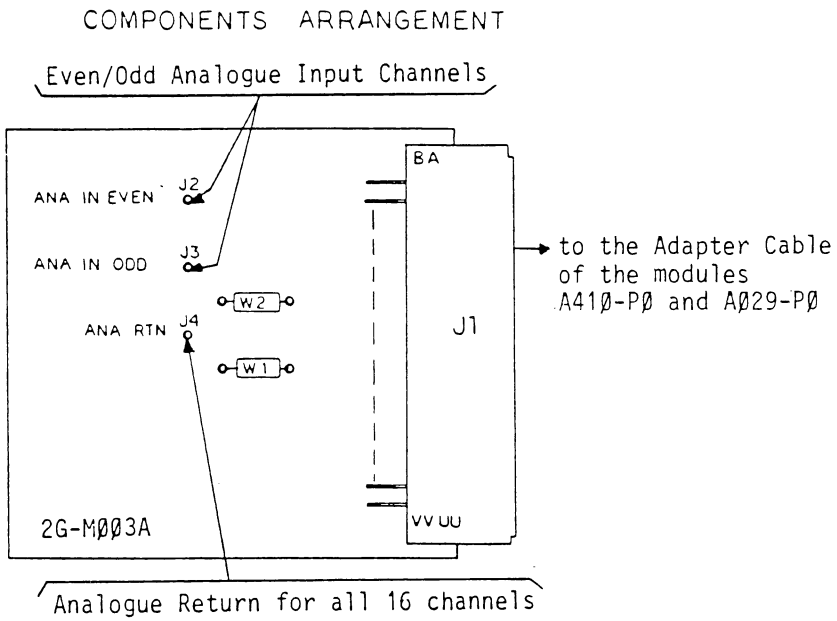


Figure B-3: Analogue Input Test Connector

ANALOGUE OUTPUT TEST CONNECTORS

There are two test connectors for the analogue output module A6007-P0. These connectors may be used for easier connection of a digital voltmeter for module checkout or calibration.

The voltage output test connector has to be used to check the 0 to 10V output.

The current output test connector has to be used to check the 0 to 20mA or 4 to 20mA outputs.

NOTE

The four analogue outputs can only be calibrated and used for one of the three output ranges: either for 0 to +10V, 0 to 20mA or 4 to 20mA.

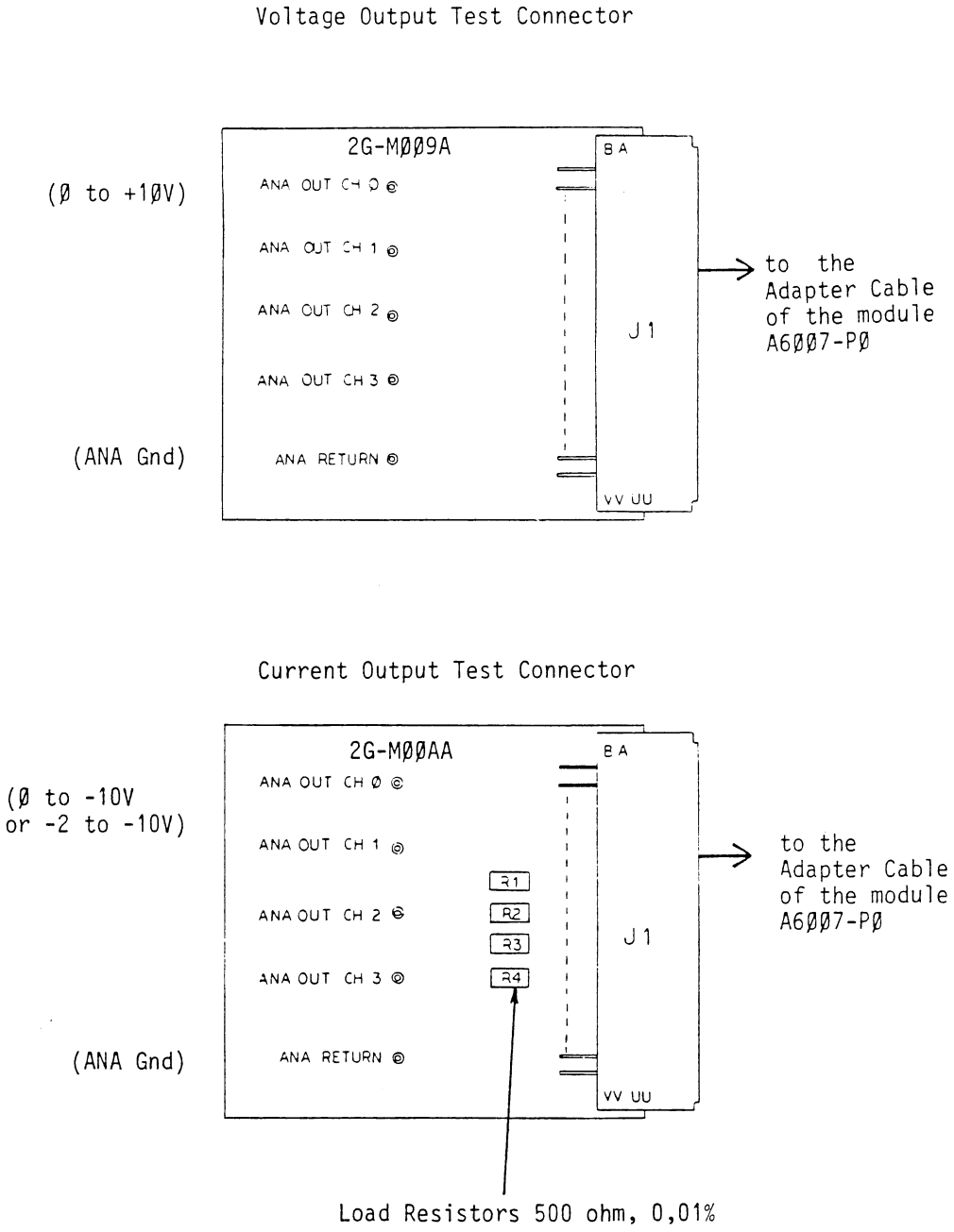


Figure B-4: Analogue Output Test Connectors

FIVE CHANNEL COUNTER TEST CONNECTOR

This test connector is intended to be used for the Five Channel Counter Module (M7197-P0) in order to perform loopback diagnostic tests.

Note that the test connector is a prerequisite for testing the counter module with the diagnostic; without the test connector plug, only a sub-set of the module functionality can be tested.

For correct operation, the loopback connector has be supplied with an external voltage of 21V to 24V.

NOTE

The counter test connector 2G-M00BA has to be installed upside down. The "SIDE2" of the connector PC-board must be pointing upwards.

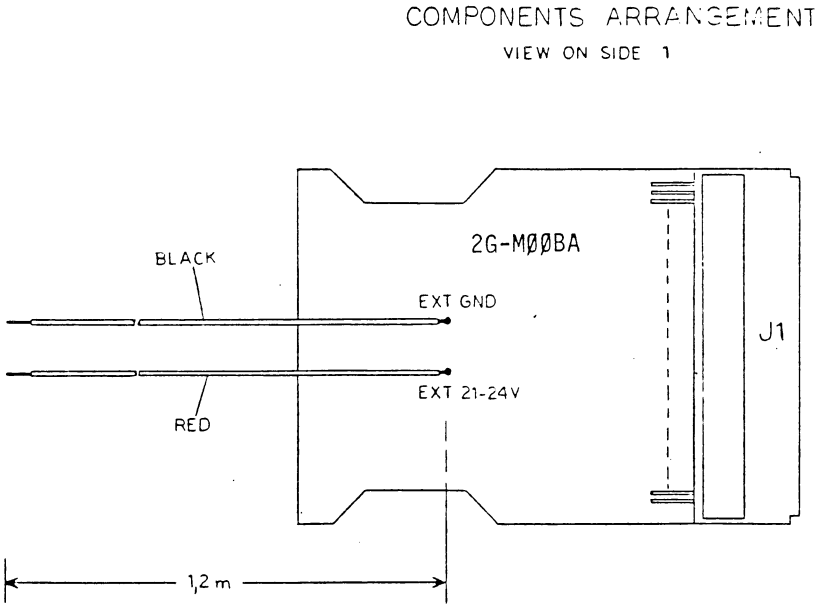


Figure B-5: Five Channel Counter Test Connector

Q-BUS I/O-MODULES
IDV1S-A,IDV1S-B,IDV1S-C,IDV1S-D,
IAV1S-A,IAV1S-AA, IAV1S-B,IAV1S-C,
IAV1S-CA MODULES
YG-C04UC-00

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