digital EQUIPMENT CORPORATION
MAYNARD MASSACHUSETTS

DRAWING DIRECTORY

CUSTOMER PRINT SET INDEX

THIS IS PRINT SET

SEQUENCE

PRINT SET #1

DRAWING DIRECTORY	B-DD-DL11-Ø
ASYNCHRONOUS LINE INTERFACE	C-UA-DL11-Ø-Ø
ASYNCHRONOUS LINE INTERFACE (PL)	A-PL-DL11-Ø-Ø
ASYNCHRONOUS LINE INTERFACE	E-CS-M78ØØ-Ø-1
CABLE ASSEMBLY (KL8/E)	D-IA-7008360-Ø-Ø
SOFTWARE LIST	A-SL-DL11-Ø-4
ACCESSORY LIST	A-AL-DL11-Ø-5
INSTALLATION PROCEDURE	A-SP-DL11-Ø-2

PRINT SET #2

DRAWING DIRECTORY	B-DD-DL11-Ø
ASYNCHRONOUS LINE INTERFACE	C-UA-DL11-Ø-Ø
ASYNCHRONOUS LINE INTERFACE (PL)	A-PL-DL11-Ø-Ø
ASYNCHRONOUS LINE INTERFACE	E-CS-M78ØØ-Ø-1
CABLE, MODEM BCØ5C	D-UA-BCØ5C-Ø-Ø
FILTER NETWORK	B-CS-G8ØØØ-Ø-1
MODEM TEST CONN	D-CS-H315-Ø-1
SOFTWARE LIST	A-SL-DL11-Ø-4
ACCESSORY LIST	A-AL-DL11-Ø-5
INSTALLATION PROCEDURE	A-SP-DL11-Ø-2

SEQUENCE

PRINT SET #3

DRAWING DIRECTORY	B-DD-DL11-0
ASYNCHRONOUS LINE INTERFACE	C-UA-DL11-0-0
ASYNCHRONOUS LINE INTERFACE (PL)	A-PL-DL11-0-0
ASYNCHRONOUS LINE INTERFACE	E-CS-M7800-0-1
CABLE, MODEM BC05C	D-UA-BC05C-0-0
CABLE ASSEMBLY (KL8/E)	D-IA-7008360-0-0
MODEM TEST CONN.	D-CS-H315-0-1
INSTALLATION PROCEDURE	A-SP-DL11-Ø-2

UNIT VARIATIONS

VARIATION	TITLE	PRINT SET TYPE DL11-1	PRINT SET TYPE DL11-2
DL11-A	ASYNC LINE INTERFACE, CURRENT LOOP	1	0
DL11-B	ASYNC LINE INTERFACE, EIA	0	1
DL11-C	ASYNC LINE INTERFACE, CURRENT LOOP	1	0
DL11-D	ASYNC LINE INTERFACE, EIA	0	1
DL11-E	ASYNC LINE INTERFACE, DATA SET	0	1

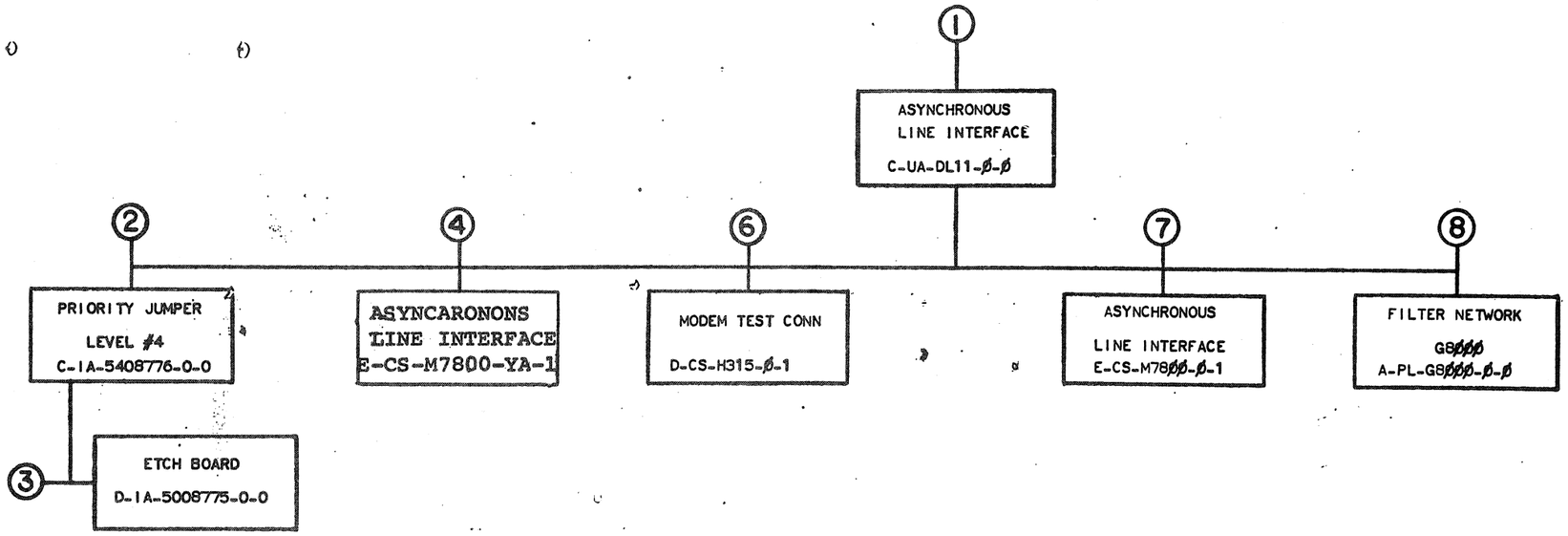
REVISIONS			
DATE	CHG. NO.	REV	
8 MAY	DL11-00001	A	M. Davis 7-17-72 P. JANSON P.E. Jansen 7-17-72
28	DL11-00002	B	M. Davis 11-30-72 P. JANSON P.E. Jansen 12-5-72
28	DL11-00003	C	Bradley 12-20-72 JANSON P.E. Jansen 1-2-72
9 M	DL11-00004	D	G. Blodgett 3-28-73 JANSON P.E. Jansen 4-6-73
9 M	DL11-00005	E	G. Blodgett 7-31-73 L. CONDON Barry Condon 8/8/73
28	DL11-00006	F	J. Chartier 9-21-73 CONDON [illegible] 10/9/73

USED ON OPTION/MODEL

DRN. M. Pierce	DATE 4-28-72	TITLE	
CHK'D. [illegible]	DATE 5/9/72	ASYNCHRONOUS LINE INTERFACE	
PROJ ENG. P.E. Jansen	DATE 5/11/72		
PROD. [illegible]	DATE 5-15-72	SIZE B	CODE DD
FIELD SERV. [illegible]	DATE [illegible]	NUMBER DL11-Ø	REV F
SHEET 1 OF 3		DIST	

DRB 106

DEC 16-(325)-1062-1-N871



TLE ASYNCHRONOUS LINE INTERFACE	SHEET 2 OF 3	SIZE B	CODE DD	NUMBER DLII - Ø	REV F

ELECTRICAL

CUSTOMER PRINT SET DL11-1	DL11-2	DL11-3	DEPOT SET	FIND NO.	DRAWING NO.	REV	NO OF SHT	DESCRIPTION	OPTION NO.
X	X	X		1.	C-UA-DL11-Ø-Ø	D	1	ASYNCHRONOUS LINE INTERFACE	
X	X	X			A-PL-DL11-Ø-Ø	D	1	ASYNCHRONOUS LINE INTERFACE (PL)	
	X	X			D-UA-BCØ5C-Ø-Ø	#	1	CABEE, MODEM, BCØ5C	
X		X			D-IA-7008360-0-0	#	1	CABLE, ASSEMBLY (KL8/E)	
					A-SP-DL11-Ø-1	*	11	ENGINEERING SPECIFICATION	
X	X	X			A-SP-DL11-Ø-2	D	8	INSTALLATION PROCEDURE	
					A-SP-DL11-Ø-3	A	7	TEST PRODEDURE	
X	X				A-SL-DL11-Ø-4	*	1	SOFTWARE LIST	
X	X				A-AL-DL11-Ø-5	C	1	ACCESSORY LIST	
				2.	C-IA-5408776-0-0		1	PRIORITY JUMPER LEVEL #4	
					B-CS-5408776-0-1		1	CIRCUIT SCHEMATIC	
					K-CO-5408776-0-4		1	X-Y COORDINATE HOLE LOC	
					B-MH-5408776-0-6		1	MODULE ECO HISTORY	
				3.	C-AH-5408776-0-5		1	ASSY/DRILLING HOLE LAYOUT	
X				4	E-CS-M7800-YA-1	#	6	ASYNCHRONOUS LINE INTERFACE	
					K-CO-M7800-YA-4		1	X-Y COORDINATE HOLE LOCATION	
					D-AH-M7800-YA-5		1	ASSY DRILLING HOLE LAYOUT	
					B-MH-M7800-YA-6		1	MODULE ECO HISTORY	
	X	X		6.	D-CS-H315-Ø-1	#	1	MODEM TEST CONN	
					K-CO-H315-Ø-4		1	X-Y COORDINATE HOLE LOC	
					D-AH-H315-Ø-5		1	ASSY DRILLING HOLE LAYOUT	
					B-MH-H315-Ø-6		1	MODULE ECO HISTORY	
X	X	X		7.	E-CS-M78ØØ-Ø-1	#	7	ASYNCHRONOUS LINE INTERFACE	
					K-CO-M78ØØ-Ø-4		1	X-Y COORDINATE HOLE LOC	
					D-AH-M78ØØ-Ø-5		1	ASSY/DRILLING HOLE LAYOUT	
					B-MH-M78ØØ-Ø-6		1	MODULE ECO HISTORY	
				8.	A-PL-G8ØØØ-Ø-Ø		1	FILTER NETWORK	
	X				B-CS-G8ØØØ-Ø-1	#	1	CIRCUIT SCHEMATIC	
					K-CO-G8ØØØ-Ø-4		1	X-Y COORINATE HOLE LOC	
					C-AH-G8ØØØ-Ø-5		1	ASSY/DRILLING HOLE LAYOUT	
					B-MH-G8ØØØ-Ø-6		1	MODULE ECO HISTORY	

MECHANICAL

CUSTOMER PRINT SET DL11-1	DL11-2	DL11-3	DEPOT SET	FIND NO.	DRAWING NO.	REV	NO OF SHT	DESCRIPTION	OPTION NO.
				1.	C-UA-DL..-Ø-Ø	D	1	ASYNCHRONOUS LINE INTERFACE	
					A-PL-DL11-Ø-Ø	D	1	ASYNCHRONOUS LINE INTERFACE (PL)	
					D-UA-BCØ5C-Ø-Ø		1	CABLE, MODEM BCØ5C	
					D-IA-7008360-0-0		1	CABLE ASSEMBLY (KL8/E)	
				2.	C-IA-5408776-0-0		1	PRIORITY JUMPER LEVEL #4	
					K-CO-5408776-0-4		1	X-Y COORDINATE HOLE LOC	
					B-MH-5408776-0-6		1	ASSY/DRILLING HOLE LAYOUT	
				3.	D-IA-5008775-0-0		1	ETCH BOARD	
					C-AH-5408776-0-5		1	ASSY/DRILLING HOLE LAYOUT	
				6.	D-CS-H315-Ø-1		1	MODEM TEST CONN	
					K-CO-H315-Ø-4		1	X-Y COORDINATE HOLE LOC	
					C-AH-H315-Ø-5		1	ASSY/DRILLING HOLE LAYOUT	
					B-MH-H315-Ø-6		1	MODULE ECO HISTORY	
				7.	E-CS-M78ØØ-Ø-1		7	ASYNCHRONOUS LINE INTERFACE	
					K-CO-M78ØØ-Ø-4		1	X-Y COORDINATE HOLE LOC	
					D-AH-M78ØØ-Ø-5		1	ASSY/DRILLING HOLE LAYOUT	
					B-MH-M78ØØ-Ø-6		1	MODULE ECO HISTORY	
				8.	A-PL-G8ØØØ-Ø-Ø		1	FILTER NETWORK	
					K-CO-G8ØØØ-Ø-4		1	X-Y COORDINATE HOLE LOC	
					C-AH-G8ØØØ-Ø-5		1	ASSY/DRILLING HOLE LAYOUT	
					B-MH-G8ØØØ-Ø-6		1	MODULE ECO HISTORY	

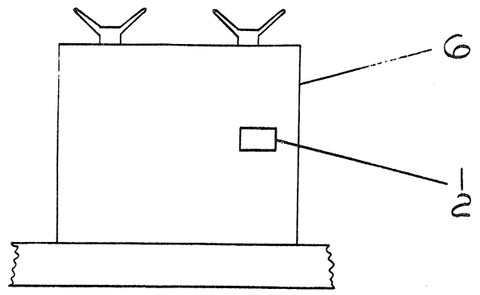
TITLE	SIZE	CODE	NUMBER	REV
ASYNCHRONOUS LINE INTERFACE	B	DD	DL11-Ø	F

SHEET 3 OF 3

DRB 108

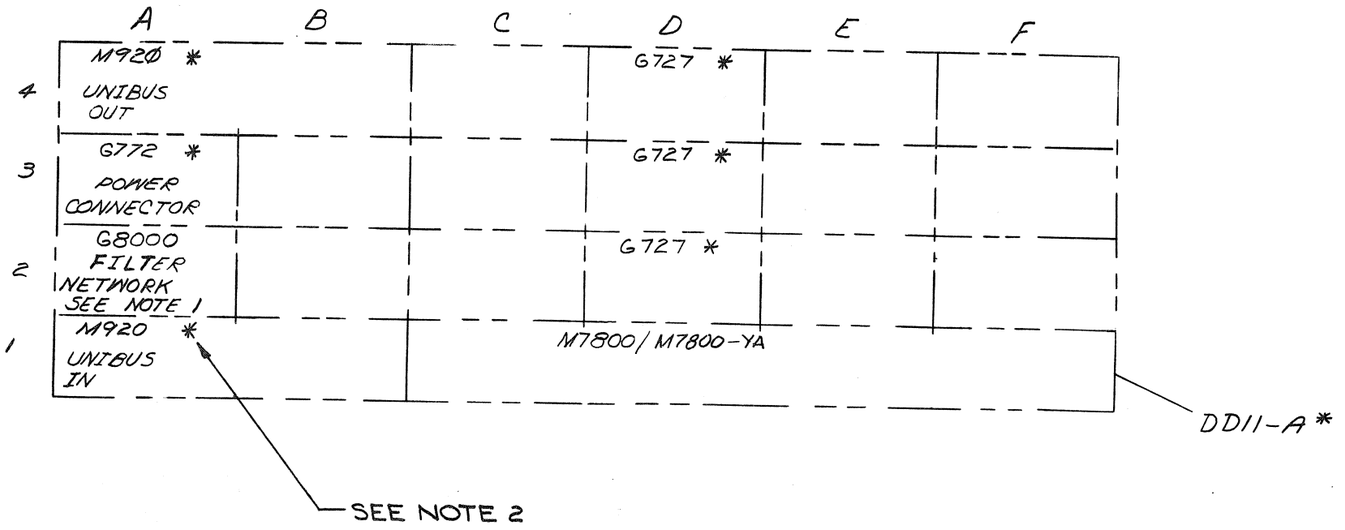
DEC 16—(325)—1062—2—N871

G



NOTES:

1. G8000 IS REQUIRED ONLY IN PDP 11 SYSTEMS WHERE +15V IS NOT AVAILABLE. THE INSTALATION REQUIRES 2 WIRES TO BE ADDED.
   A03V2 - A02V2
   A02N2 - CXXU1
   WHERE (XX) IS THE SLOT NUMBER CONTAINING THE DL11.
2. ITEMS INDICATED WITH ASTERICK (*) ARE SHOWN FOR REFERENCE ONLY AND ARE NOT PART OF THIS UNIT.



REVISIONS												
CHK	CHANGE NO.	REV.										
PM	DL11-00001	A	M. Jacobi 2-18-72	R. JANSON								
PM	DL11-00002	B	D.E. Jenson 7-17-72	D.E. Jenson 11-6-72	JANSON							
PM	DL11-00005	C	D.E. Jenson 10-5-72	D. Gardner 7-31-73	L. CONDON							
PM	DL11-00006	D	J. Chartier 9-21-73	CONDON								

DEC FORM NO. DRC 100-A

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
PDP-11		PARTS LIST		

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES

DECIMALS	ANGLES
.XXX = .005 .XX = .02 .X = .1	±0° 30'

REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓

MATERIAL

FINISH

DRN. M Brien	DATE 3/18/72	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
CHK'D. L. Frazier	DATE 4-24-72	
ENG. D E Jenson	DATE 5-11-72	
PROJ ENG. D E Jenson	DATE 5-11-72	TITLE: ASYNCHRONOUS LINE INTERFACE
PROD. J Mackey	DATE 5-15-72	

NEXT HIGHER ASSY. B-OD-DL11-Ø

SCALE NONE

SHEET OF

SIZE	CODE	NUMBER	REV.
C	UA	DL11-Ø-Ø	D

DIST. G

SIZE C | CODE UA | NUMBER DL11-Ø-Ø | REV. D

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

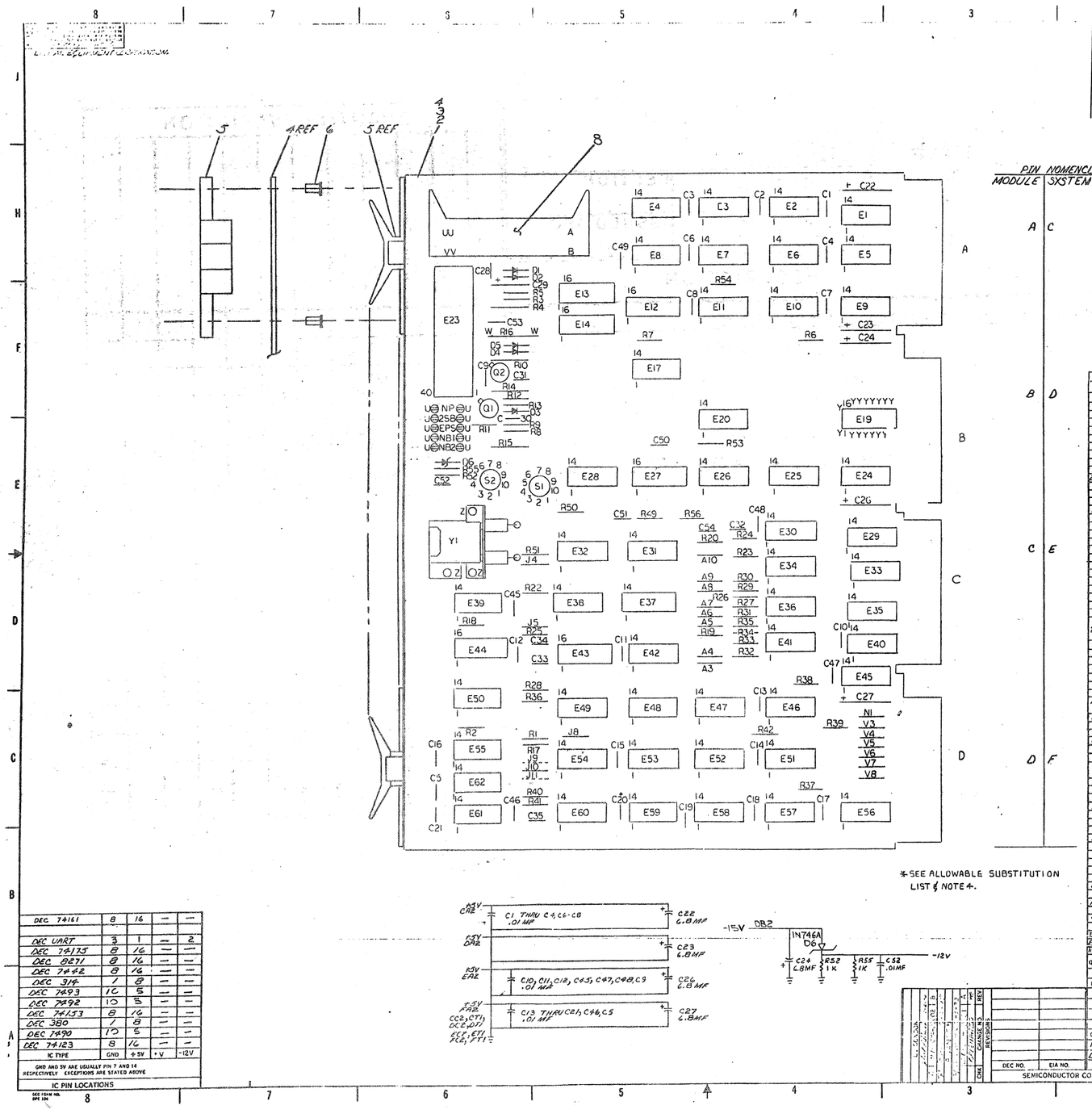
PARTS LIST

MADE BY M. PIERCE	CHECKED J. FERGUSON	SECTION
DATE 4/27/72	DATE 4/27/72	1
ENG P. E. Jonson	PROD J. McGuire	ISSUED SECT.
DATE 5/11/72	DATE 5/15/72	1

ITEM NO.	DWG NO. / PART NO.	DESCRIPTION	QUANTITY/VARIATION DL11-A	DL11-B	DL11-C	DL11-D	DL11-E	
1	C-IA-5408776-0-0	PRIORITY JUMPER LEVEL #4	1	1	1	1	1	
~~2~~	~~C-IA-5408778-0-0~~	~~PRIORITY JUMPER LEVEL #5~~	~~-~~	~~-~~	~~-~~	~~-~~	~~1~~	
3	D-UA-BCØ5C-25	CABLE, MODEM BCØ5C	-	1	-	1	1	
4	D-IA-7008360-0-0	CABLE ASSEMBLY (KL8E)	1	-	1	-	-	
5	D-CS-H315-Ø-1	MODEM TEST CONNECTOR	-	-	-	-	A/R	See Note 2
6	E-CS-M7800-Ø-1	ASYNCHRONOUS LINE INTERFACE	-	1	-	1	1	
7	A-PL-G8ØØØ-Ø-Ø	FILTER NETWORK	-	A/R	-	A/R	A/R	See Note 1
8		CRYSTAL	A/R	A/R	A/R	A/R	A/R	See Note 3
9	E-CS-M7800-YA-1	ASYNCHRONOUS LINE INTERFACE	1	-	1	-	-	
	NOTES: 1.	G8000 IS REQUIRED ONLY IN PDP 11						
		SYSTEMS WHERE +15V IS NOT						
		AVAILABLE. ONE PER DD11-A.						
	2.	ONE H315 PER PDP11 SYSTEM						
	3.	CRYSTAL FREQUENCY DEFINED BY CUSTOMER						
		SPECIFIED BAUD RATE						
	4.	APPLY TAPE TO TOP SURFACES OF CRYSTAL						
		AND MOUNTING BRACKETS TO INSULATE FROM						
		ADJACENT MODULES.						
10	9008269	TRANSPARENT VINYL TAPE	A/R					

TITLE	ASSY NO.	SIZE	CODE	NUMBER	REV.	ECO NO.
ASYNCHRONOUS LINE INTERFACE	C-UA-DL11-Ø-Ø	A	PL	DL11-Ø-Ø	D	DL11-00006
	SHEET 1 OF 1	DIST.	G			

DEC FORM DEC 16-(325)-1031-N870
DRA 110



*SEE ALLOWABLE SUBSTITUTION LIST & NOTE 4.

NOTES:

1.) PIN NOTATION THROUGHOUT IS ORDERED UPON MODULE PLACEMENT IN THE SYSTEM UNIT. MODULE REFERENCE ALONE IS OBTAINED BY CONVERTING THE FIRST LETTER ACCORDING TO THE PIN NOMENCLATURE CHART AT THE LEFT.

2.) JUMPERS TO BE USED AT CONNECTIONS A3-A10, J4-J6, J8-J10, V3-V3, AND N1.

3.) LETTERS ENCLOSED IN PARENTHESIS REFER TO PINS ON THE BERG CONNECTOR. EXAMPLE: (X).

4.) ON ITEM NO.23, ALL 7 CHIPS MUST BE EITHER DEC 380's OR ITS SUBSTITUTE 11380 ICs'. A DEC 380 AND 11380 MIXTURE OF THESE 7 CHIPS IS NOT ALLOWED. E28 MUST BE A DEC 380. (ITEM NO.68).

PIN NOMENCLATURE	
MODULE	SYSTEM UNIT
A	C
B	D

ALLOWABLE SUBSTITUTION LIST

ORIG. PART NO	SUBSTITUTE PART DESCRIPTION	PART NO.	ITEM NO.
1909485	IC 11380	1911113	23

QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.
1	E28	IC DEC 380	1909485	68
1	R3	RES 750Ω 1/4W 5%	1301401	67
1	R28	RES 390Ω 1/4W 5%	1300397	66
1	D9	DIODE 1N746A	1104860	65
2	Q1,Q2	TRANSISTOR 2N3415	1903409-00	64
1	C52	CAP 100PF 100V 5% MICA	1000016	63
1	C54	CAP 560PF 100V 5% MICA	1000025	62
2	C50,C51	CAP .047MF CERAMIC	1009978	61
1	E27	IC DEC 74161	1910650	60
1	C34,C35	CAP 330PF 100V 5% DIPPED MICA	1000029	59
1	C32	CAP 82PF 100V 5% DIPPED MICA	1000029	58
1	C31	CAP 100PF 100V 5% DIPPED MICA	1000032	57
29	A1,A2,A3,A4,A5,A6,A7,A8,A9,A10,C30,A5-B4,C52	CAP .01UF 100V 20% CERAMIC DISC	1001610	56
1	C28	CAP .47UF 35V 10% TANT	1003925	55
6	C22-C23,C25,C27	CAP 6.8 UF 35V 20% TANT	1000067	54
1	C33	CAP 150PF 100V 5% DIPPED MICA	1000079	53
2	R14,R15	RES 1.5K 1/2W 5%	1300399	52
6	R23,R24,R10, R52,R55	RES 1K 1/4W 5%	1300365	51
1	R31	RES 49.9Ω 1/2W 5%	1300202	50
1	R30	RES 68Ω 1/2W 10%	1300220	49
1	R29	RES 82Ω 1/4W 5%	1301877	48
1	R34	RES 100Ω 1/4W 5%	1300239	47
1	R11	RES 130Ω 1/4W 5%	1300330	46
1	R22	RES 180Ω 1/4W 5%	1301322	45
1	E53	RES 220Ω 1/4W 5%	1300271	44
5	D1-D5	DIODE FR-LA 201 1001A	1104714	43
3	R9,R8,R51	RES 470Ω 1/4W 5%	1300396	42
1	R2	RES 560Ω 1/2W 5%	1300338	41
3		NUT HEX 4-40	9006555	40
1	R16	RES 1.2K 1/4W 5%	1302985	39
26	R1,R2,R6,R7,R11-R21, R45,R47-R53,R54, R49, R50, R12, R55, R56	RES 10K 1/4W 5%	1300479	38
2	R9, R12	RES 1.3K 1/4W 5%	1300391	37
1	E29	IC DEC UART	1910939	36
3	E35, E37, E41, E62	IC DEC 7474	1903549	35
2	E34, E41	IC DEC 8242	1909712	34
3	E38, E49, E59	IC DEC 7408	1910153	33
1		SCA PWR SUP PWR *2-5CX-25E(S)	9-CCCDN-1	32
5	E20, E26	IC DEC 7490	1909031	31
11	E1, E2, E3, E7-E9, E11, E30, E47, E51, E52	IC DEC 8881	1909705	30
8		AI/SAT 8200 PS-1	1912812	29
1	E39	IC DEC 74123	1910436	28
3	E31, E37, E38	IC DEC 74174	1909687	27
3	E33, E36, E42	IC DEC 7400	1903579	26
1	E40	IC DEC 7473	1909789	25
2	E50, E33	IC DEC 7402	1909004	24
7	E5, E6, E33, E35, E40, E45, E46.	IC DEC 380	1909485-8	23
1	E16	IC DEC 74133	1909937	22
1	E60	IC DEC 74H04	1909951	21
1	E25	IC DEC 7492	1909059	20
4	E4, E17, E58, E59	IC DEC 7404	1909026	19
1	E24	IC DEC 7493	1909054	18
1	E32	IC DEC 7410	1903376	17
1	E19	IC DEC 374	1909724	16
1	E21	IC DEC 7442	1910056	15
1	E22	IC DEC 8277	1909643	14
2	E18, E18	IC DEC 74175	1910651	13
1		CRYSTAL HOLDER	3303823	12
1		CRYSTAL HOLDER	3303154	11
1	E19	IC SOCKET	1200830	10
2	S1, S2	SWITCH, STABLE ROLE, 10 POS	1200754	9
1		40 PIN CONNECTOR BERG	1207941	8
10		SPLIT LUGS	9006733	7
8		FASTENER #6SS-7 E.B.STHYRON	9906733	6
9		HANDLE, FLIP-CHIP, MAGENTA	3008337-04	5
1		ETCHED CIRCUIT BOARD	3009979	4
REF		MODULE ECO HISTORY		3
REF		ASSY/UTILITY HOLE LAYOUT		2
REF		X-Y COORDINATE HOLE		1

PARTS LIST

ETCH BOARD REV E

IC TYPE	GND	+5V	+V	-12V
DEC 74161	8	16	—	—
DEC UART	3	1	—	2
DEC 74175	8	16	—	—
DEC 8271	8	16	—	—
DEC 7442	8	16	—	—
DEC 374	1	8	—	—
DEC 7493	10	5	—	—
DEC 7492	10	5	—	—
DEC 74153	8	16	—	—
DEC 380	1	8	—	—
DEC 7490	10	5	—	—
DEC 74123	8	16	—	—

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

SEC TOP# NO. SPC 106

+5V C1 THRU C4, C6-C8 .01 MF

+5V DB2

C22 6.8MF

C23 6.8MF

C26 6.8MF

C27 6.8MF

+5V E28 C2, C7, C11, C12, C16, C21 E1, E17, E61

C10, C11, C18, C43, C47, C48, C9 .01 MF

C13 THRU C21, C46, C5 .01 MF

-15V DB2

1N746A D6

C24 6.8MF

R52 1K

R55 1K

C52 .01MF

-12V

DEC NO.	EIA NO.
GS345	MPS6534
1N746A	1N4734A
D44	1N3606
DEC NO.	EIA NO.

SEMICONDUCTOR CONVERSION CHART

NEXT HIGHER ASSY

DRAWN

CHK'D

ENG

MFG

DATE

EQUIPMENT CORPORATION

TITLE ASYNCHRONOUS LINE INTERFACE

CAGE CODE E | NUMBER CS M7680 -YA-1 | REV A1

SHEET 1 OF 6

ESM7680-YA-1 B

DL-2 BINIT H
DL1 BUS INIT L
DL-2 BINIT L

DL-2 BD07 H
DL-2 BD06 H
DL-2 BD05 H
DL-2 BD04 H
DL-2 BD03 H
DL-2 BD02 H
DL-2 BD01 H
DL-2 BD00 H

DL-4 RD7 H
DL-4 RD6 H
DL-4 RD5 H
DL-4 RD4 H
DL-4 RD3 H
DL-4 RD2 H
DL-4 RD1 H
DL-4 RD0 H
DL-5 RBUF TO BUS H

DL-4 XMIT READY H
DL-4 XMIT INT ENB (1)H
DL-4 MAINT (1)H
DL-4 BREAK (1)H
DL-5 XCSR TO BUS H

DL-4 RCVR DONE H
DL-4 RCVR INT ENB (1)H
DL-4 DATASET INT ENB (1)H
DL-4 SEC XMIT (1)H (CK)
DL-4 REQ TO SEND (1)H (CM)
DL-4 DATA TERMINAL READY (1)H (CF)

CM2 BUS D07 L
CV2 BUS D06 L
CP2 BUS D05 L
CN2 BUS D04 L
CT2 BUS D03 L
CU2 BUS D02 L
CR2 BUS D01 L
C32 BUS D00 L

+5V
R1 10K
J8
DL-5 RBUF TO BUS L

DL-4 OR ERR H
DL-4 FR ERR H
DL-4 P ERR H

+5V
R2 10K
J7
DL-5 RCSR TO BUS L

ERROR H

DL-5 RCSR TO BUS H
DL-4 RCVR BUSY (1)H

CD2 BUS D15 L
CE2 BUS D14 L
CF2 BUS D13 L
CH2 BUS D12 L
CH1 BUS D11 L
CJ2 BUS D10 L

REVISIONS		
CHK.	ECO NO.	REV.

FIRST USED ON OPTION/MODEL	DL11
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES	
DECIMALS	.XXX = .005 .XX = .02 .X = .1
ANGLES	±0° 30'
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓	
MATERIAL	
FINISH	

QTY.	DESCRIPTION	PART NO.	ITEM NO.
	PARTS LIST		

DRN. DATE 10/5/72
CHK. DATE 10/5/72
ENG. DATE 11/6/72
PROJ ENG. DATE 11/6/72
PROD. DATE 11/6/72
NEXT HIGHER ASSY.
SCALE
SHEET 2 OF 6

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE ASYNCHRONOUS LINE INTERFACE (BUS RECEIVERS & DRIVERS) DL-2

SIZE	CODE	NUMBER	REV.
D	CS	M7800-YA-1	B

DIST.

Y1	844.8 KHZ		1.0368 MHZ		1.152 MHZ		4.608MHZ	
SWITCH POS.	BAUD	μSEC	BAUD	μSEC	BAUD	μSEC	BAUD	μSEC
1	36.7	1700	44.8	1342	50	1250	200	312
2	55	1135	67.3	928	75	833	300	208
3	110	567	134.5	464	150	417	600	104
4	220	284	269	232	300	208	1200	52
5	440	142	538	116	600	104	2400	26
6	880	71	1076	58	1200	52	4800	13
7	1320	47.4	1614	38.7	1800	34.6	7200	8.7
8	1760	35.5	2152	29	2400	26	9600	6.5
9	BERG CLOCK INPUT- COMMON TO RCVR AND XMIT							
10	EXTERNAL CLOCK INPUT- RCVR; DSI; XMIT DRI							

DL-3 BG IN H DV2 01 — DL-6 BG OUT H DV2 03 — BUS BG4 OUT H DT2 04 — BUS BG4 IN H DB2 05 — BUS BG5 OUT H DR2 06 — BUS BG5 IN H DP2 07 — BUS BG6 OUT H DN2 08

PRIORITY PLUG E19

09 DM2 BUS BR4 L
10 DD2 BUS BR7 L
11 DK2 BUS BG7 IN H
12 DJ2 DL-6 REQUEST L
13 DH2 BUS BR5 L
14 DF2 BUS BR5 L
15 DE2 BUS BR6 L
16 DD2 BUS BR7 L

DR1 EXT XMIT INPUT
DL-3 XMIT CLK H
(CC) BERG CLOCK INPUT
DSI EXT RCVR INPUT
DL-3 RCVR CLK H

DB1 TTL RDR ENB L
DL-4 RDR ENB (1)H
R8 1.5K R9 470 R11 150 Q1 6534D D3 D084 C38 .01μFD
READER RELAY (PP)
R10 68Ω -15V (EE)

DC1 TTL SERIAL OUT L
R12 1.5K R13 470 C31 1000 pf C53 100pF Q2 6534D D4 D084 D5 D084 R14 1.5K R15 1.5K R16 75Ω
20 MA TRANSMIT (BB) (KK)
+5 (TT) (A) (B) (VV) (UU)

R49 10K R50 10K C50 .047μFD C51 .047μFD Y1 R51 47Ø
380 E28 380 E28
+5V R3 750 R5 82 D1 D664 (H) TO BERG INTERLOCK
20 MA RECEIVE (K) C28 .01 UFD C29 .47UFD C49 .01UFD D2 D664 (S) R4 560 -15V

7414 E25 — CLR — CLKBC CLKØ — R3(1) R2(1) R1(1) R0(1)
7493 E23 — CLR — CLKBC CLKØ — R3(1) R2(1) R1(1) R0(1)
7493 E24 — CLR — CLKBC CLKØ — R3(1) R2(1) R1(1) R0(1)
74153 E12 — DI CI BI AI DØ CØ BØ AØ — FI FØ — SI SØ
74161 E27 — CLR — D3 D2 D1 D0 — R3(1) R2(1) R1(1) R0(1) — CARRY
380 E28
7413 E10 — 06
R6 10K R54 10K R56 10K

BERG CLOCK INPUT(CC)
BERG SERIAL IN L (E)
TTL SERIAL IN L DA1
DL-4 MAINT (1)H
BERG CLK ENB L(HH)
DL-4 SERIAL OUT H
09 FRI DL-3 RCLK H
07 FSI DL-3 SI H

Net Maint bit ser. out connected to ser. in.

NOTES:
1. LETTERS ENCLOSED IN PARENTHESIS REFER TO PINS ON THE BERG CONNECTOR. EXAMPLE (X)
2. NUMBERS WITHIN TRIANGLES REFER TO PINS ON THE FEMALE MATE-N-LOCK CONNECTOR WHEN USING THE 7008360 CABLE, THIS CABLE ALSO CONNECTS BERG PINS H TO E.

REVISIONS		
CHK.	CHANGE NO.	REV.

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
DL11		PARTS LIST		

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES
DECIMALS .XXX = .005 .XX = .02 .X = .1 ANGLES ±0° 30'
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓
MATERIAL
FINISH

DRAWN — DATE 11/6/72
CHKD. — DATE
ENG. — DATE
PROGRAM — DATE 11/6/72
PROD — DATE 11/6/72
NEXT HIGHER ASSY.
SCALE
SHEET 3 OF 6

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS 01754

TITLE ASYNCHRONOUS LINE INTERFACE (CLOCK & CURRENT LOOPS) DL-3

SIZE	CODE	NUMBER	REV.
D	CS	M78ØØ-YA-1	B

DIST.

DL-2 BINIT L

DL-5 SEL 2 L

7408 E31

UART E23

DL-2 BD07 H
DL-2 BD06 H
DL-2 BD05 H
DL-2 BD04 H
DL-2 BD03 H
DL-2 BD02 H
DL-2 BD01 H
DL-2 BD00 H
DL-5 LD XD L
X CLK H

CLR R DONE
STB STATUS
STB RD
R CLK
SERIAL IN
XD7
XD6
XD5
XD4
XD3
XD2
XD1
XD0
LD XD
X CLK
DU1 40

R DONE
OR ERR
FR ERR
P ERR
RD7
RD6
RD5
RD4
RD3
RD2
RD1
RD0
SERIAL OUT
XRDY
EOC

DL-4 OR ERR H
DL-4 FR ERR H
DL-4 P ERR H
DL-4 RD7 H
DL-4 RD6 H
DL-4 RD5 H
DL-4 RD4 H
DL-4 RD3 H
DL-4 RD2 H
DL-4 RD1 H
DL-4 RD0 H

CLR LDC NB2 NB1 NP EP 288

+5V R17 10K

7474 E38 — DL-4 RCVR BUSY (1)H

7408 E15

DL-2 BINIT H

7402 E50

8271 E44

CLR LD CLK D8

FSI DL-3 SI H

7408 E58 — 7408 E58 — 7408 E42

DL-3 RCLK H FRI

7474 E55

7404 E38 — 7404 E36 — DL-4 SERIAL OUT H

7474 E61

7404 E17

R53 220

C54 560 pf

7408 E20

SET 9 — CLR — CLKBC — CLKØ

7408 E54 — 7408 E59 — J9 — J11 — J10

DL-3 XMIT CLK H

74175 E14

DL-2 BD02 H
DL-2 BD00 H
DL-2 BD06 H
DL-2 BD04 H

D3 D2 D1 D0 — CLR CLK

R3(1) R3(0) R2(1) R2(0) R1(1) R1(0) R0(1) R0(0)

DL-4 MA INT (1)H
DL-4 BREAK (0)H
DL-4 XMIT INT ENB (1)H

DL-5 BUS TO XCSR H

7404 E36 — DL-4 BREAK (1)H

+5K R18 10K — J5

7408 E31 — DL-4 XMIT INT H

DL-4 XMIT READY H

DL-4 RCVR DONE H

7408 E42 — 7408 E42 — 7408 E42 — DL-4 RCVR INT H

+5V R19 10K — J6

7474 E62

74175 E19

DL-2 BD05 H
DL-2 BD02 H
DL-2 BD06 H
DL-2 BD03 H

DL-4 DATASET INT ENB (1)H
DL-4 REQ TO SEND (1)H
DL-4 REQ TO SEND (0)H
DL-4 RCVR INT ENB (1)H
DL-4 SEC XMIT (1)H
DL-4 SEC XMIT (0)H

+5V R20 10K — J3

DL-4 DATA LEADS ONLY L

J4

DTR 7474 E32 — DL-2 BD01 H — DL-4 DATA TERMINAL READY (1)H — DL-4 DATA TERMINAL READY (0)H

+5V R22 10K

RDR ENB 7474 E32 — DL-2 BD00 H — DL-4 RDR ENB (1) H

DL-5 BUS TO RCSR H

REVISIONS		
CHK.	CHANGE NO.	REV.

FIRST USED ON OPTION/MODEL: DL11	QTY.	DESCRIPTION	PART NO.	ITEM NO.
		PARTS LIST		

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES
DECIMALS: .XXX = .005, .XX = .02, .X = .1
ANGLES: ±0° 30'
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓
MATERIAL
FINISH

DRN. — DATE
CHK'D — DATE 10/12/72
ENG. — DATE
PROJ. ENG. — DATE
PROD. — DATE

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: ASYNCHRONOUS LINE INTERFACE (UART & STATUS) DL-4

NEXT HIGHER ASSY.
SCALE
SHEET 1 OF 6

SIZE D | CODE CS | NUMBER M7800-YA-1 | REV. B

DIST.

BUS A11 L
BUS A13 L
BUS A14 L
BUS A15 L
BUS A16 L
BUS A17 L
BUS A12 L
314 E29
BUS MSYN L
388 E33
7418 E34
8881 E38
+5V R23 1K
R24 180
C32 470 pf
E-J1 BUS SSYN L
7464 E39
EL2 REG SEL H
+5V R27 10K
R28 1K
A10
A9
A8
A7
A6
A5
A4
A3
8242 E36
8242 E41
8243 E41
8242 E37
BUS A18 L EP1
BUS A17 L EP2
BUS A16 L EU1
BUS A15 L EV1
BUS A14 L EU2
BUS A13 L EV2
BUS A01 L EH1
BUS A02 L EF1
BUS A03 L EH2
BUS C1 L EF2
BUS C0 L E-J2
388 E40
388 E45
388 E48
388 E50
388 E36
7442 E37
D3 D
D2 C
D1 B
D0 A
+5V R29 1BK
R25 10K
C33 150 pf
50ns
74123 E43
EBL DL-5 LD XD L
DL-5 BUS TO XBUF L
DL-5 BUS TO XCSR H
DL-5 BUS TO RCSR H
DL-5 XCSR TO BUS H
DL-5 RBUF TO BUS L
DL-5 RBUF TO BUS H
DL-5 RCSR TO BUS H
C34 330 pf
100ns
DL-5 SEL 2 L
DL-5 BUS TO RBUF L
DL-5 RCSR TO BUS L

NOTE 1: THE "A" LINES ARE TO BE JUMPERED FOR A 0.

REVISIONS		
CHK.	CHANGE NO.	REV.

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	FIND NO.
DL11		PARTS LIST		

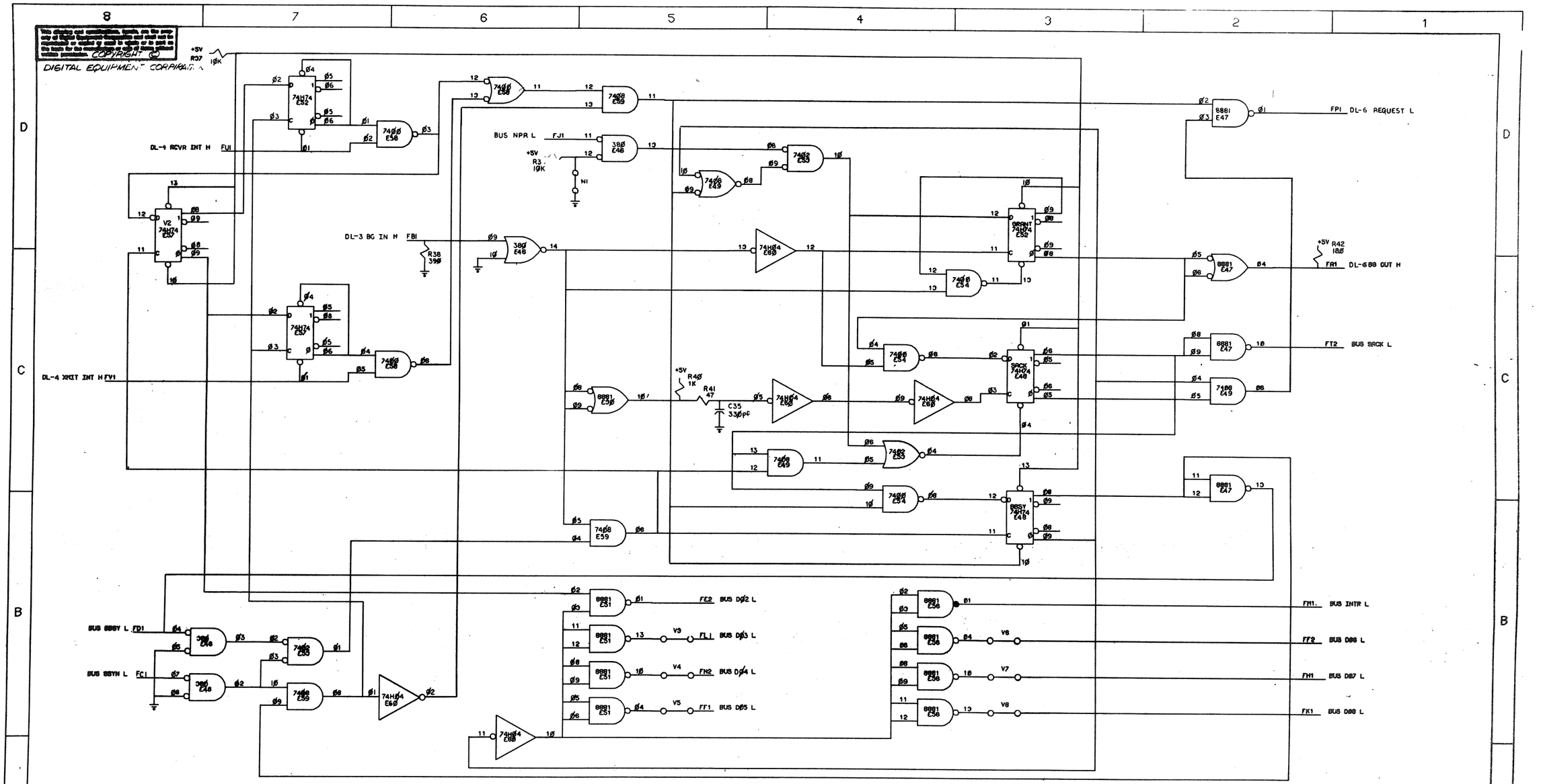
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES
DECIMALS .XXX = .005 .XX = .02 .X = .1
ANGLES ±0° 30'
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓
MATERIAL —
FINISH —

DRN. DATE 10/72
DSGN. DATE 10/72
ENGR. DATE 11/72
PROJ. ENG. DATE 11/72
MOD. DATE 11/6/72
NEXT HIGHER ASSY. —
SCALE —
SHEET 5 OF 6

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE ASYNCHRONOUS LINE INTERFACE (ADDRESS SELECTION) DL-5

SIZE B | CODE DCS | NUMBER M7800-YA-1 | REV B | DIST.



NOTE: THE "V" LINES ARE TO BE JUMPERED FOR A 1.

REVISIONS		
CHK.	CHANGE NO.	REV.

FIRST USED ON OPTION/MODEL: DL11	QTY.	DESCRIPTION	PART NO.
		PARTS LIST	

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES
DECIMALS: .XXX = .005, .XX = .02, .X = .1 — ANGLES: ±0° 30'
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓
MATERIAL
FINISH

DRN. — DATE
CHK'D. — DATE
ENG. — DATE
PROJ. ENG. — DATE
PROD. — DATE
NEXT HIGHER ASSY.
SCALE
SHEET 6 OF 6

digital EQUIPMENT CORPORATION

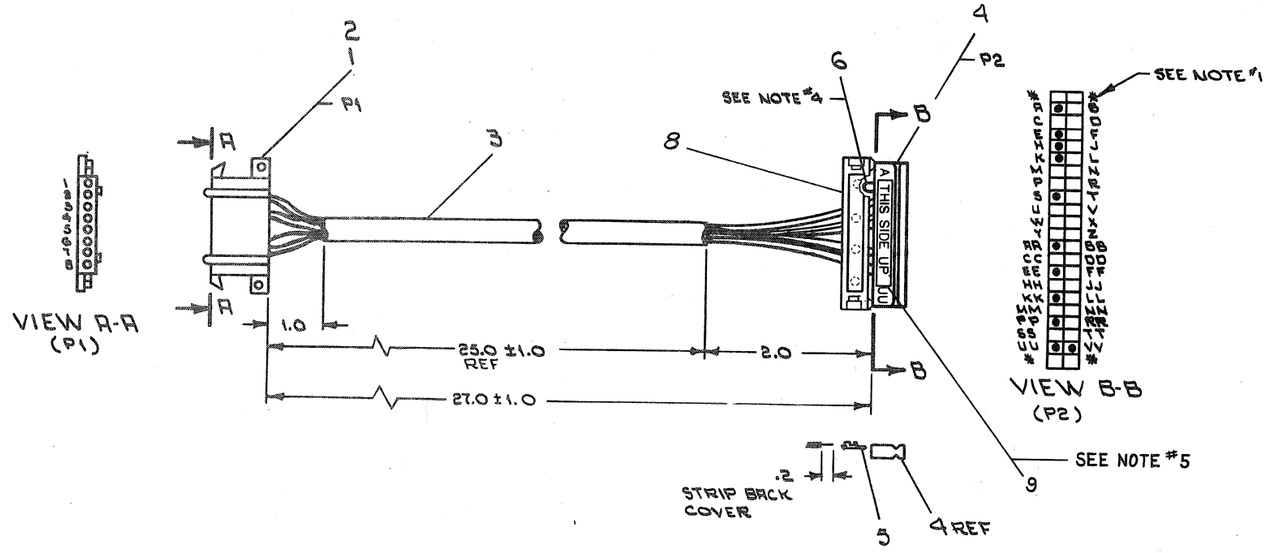
TITLE ASYNCHRONOUS LINE INTERFACE (INTERRUPT CONTROL) DL-6

CODE D CS — NUMBER M7800-YA-1 — REV. B

DIST.

WIRE TABLE								
ITEM NO.	DESCRIPTION AWG	COLOR	PAIR NO.	FROM CONNECTION	FROM WITH	TO CONNECTION	TO WITH
3	22	BLK	1	P1-2	2	P2-KK	5
3		RED		P1-3	2	P2-S	
3,7		SHIELD		SEE NOTE #2	—	P2-A(NOTE #3)	
3		BLK	2	P1-4	2	P2-EE	
3		WHT		P1-5	2	P2-RR	
3,7		SHIELD		SEE NOTE #2	—	P2-LL(NOTE #3)	
3		BLK	3	P1-6	2	P2-PP	
3		GRN		P1-7	2	P2-K	
3,7		SHIELD		SEE NOTE #2	—	P2-VV(NOTE #3)	
6	22	BLK	—	P2-E	5	P2-H	5

NOTES:
1. * ASTERISKS INDICATE CAVITIES NOT USED OR DESIGNATED BY LETTERS.
2. DRAIN WIRES TO BE CUT BACK TO OUTER INSULATION ON P1 END OF CABLE ONLY. SHIELDS TO BE CUT BACK TO OUTER INSULATION ON BOTH ENDS OF CABLES.
3. DRAIN WIRES ON P2 END OF CABLE TO BE EACH ENCLOSED WITH ITEM #7 (TUBING) FROM END OF CABLE JACKET TO POINT WHERE THEY ENTER P2 CONNECTOR.
4. ITEM #6 (WIRE) TO BE APPROXIMATELY ONE(1) INCH LONG.
5. PLACE ITEM #9 ("THIS SIDE UP" STICKER) ON LETTERED SIDE OF ITEM #4 (BERG HOUSING) AS SHOWN.



ITEM NO.	DESCRIPTION	PART NO.	QTY.
1	LABEL, THIS SIDE UP	3611567	9
1	STRAIN RELIEF	1211166	8
A/R	TUB. #18 TEF. THINWALL WHT	9107278-11	7
A/R	WIRE #22 AWG STRD TEF BLK	9107550-00	6
11	SOCKET, CRIMP # 47216	1210089-07	5
1	HOUSING, BERG #65043-015	1210918-15	4
A/R	CABLE, BELDEN #8777-3PR SHLD	9107723-0	3
6	CONTACT MATE-N-LOCK (FEMALE)	1209379	2
1	CONN. MATE-N-LOCK (FEMALE)	1209340-00	1

PARTS LIST

REVISIONS			
CHK	CHANGE NO.	REV.	
	KL8E-00002	A	
	KL8E-00006	B	
	7008360-00001	C	
	7008360-00002	D	

FIRST USED ON OPTION/MODEL: PDP-8E

DO NOT SCALE DRAWING
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES
TOLERANCES
ANGLES ± 0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS
MATERIAL: SEE PARTS LIST
FINISH

DRN.	T.J. LeRoy	DATE 14APR'71
CHK'D.		DATE 4-6-71
ENG.		DATE 4-6-71
PROJ. ENG.		DATE 4-8-71
PROD.		DATE 4/20/71

NEXT HIGHER ASSY: A-ML-KL8-E-0
SCALE: NONE
SHEET 1 OF

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: CABLE ASSEMBLY (KL8E)

SIZE D | CODE IA | NUMBER 7008360-0-0 | REV D
DIST.

REVISIONS

CHK	CHANGE NO.	REV.	
	KL8E-00002	A	N. NAKAHARA 5/13/71
	KL8E-00006	B	E. CLARK 5-17-73
	7008360-00001	C	E. ALLain 10-29-73
	7008360-00002	D	B. REGAN 3-27-74

B. REGAN 3/2/74

FORM NO. 0

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

SOFTWARE LIST

MADE BY EMPellegrini DATE 8/29/72	CHECKED P. Janson DATE 8-30-72	SECTION
ENG P. Janson DATE 8/29/72	PROD J. Tinkham DATE 8-31-72	ISSUED SECT.

LEGEND

D	DOCUMENT
DN	DOCUMENT CHANGE NOTICE
PA	PAPER TAPE ASCII
PB	PAPER TAPE BINARY
PM	PAPER TAPE READ-IN-MODE

ITEM NO.	DWG NO. / PART NO.	DESCRIPTION	QUANTITY/VARIATION DL11-A	DL11-B	DL11-C	DL11-D	DL11-E			KIT CHECK BY ____ DATE ____	INSTALLATION CHECK BY ____ DATE ____
1	LIBKIT-11-KL11-Ø4	KL11 MAINDEC	1	1	0	0	0				
2	LIBKIT-11-DL11C-A-K	DL11 MAINDEC	0	0	1	1	0				
3	LIBKIT-11-DL11E-A-K	DL11 MAINDEC	0	0	0	0	1				

TITLE: DL11 SOFTWARE LIST	ASSY. NO.	SIZE A	CODE SL	NUMBER DL11-0-4	REV.	ECO NO
	SHEET 1 OF 1	DIST.				

DEC FORM NO. DEC 16-(327)-1049-N471
DRA 120

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

ACCESSORY LIST

MADE BY	E. Pellegrini	CHECKED P. Janson	SECTION
DATE	June 26, 1972	DATE 8-8-72	
ENG	Paul Janson	PROD J. Thibeau	ISSUED SECT.
DATE	June 26, 1972	DATE 8-8-72	

LEGEND

D DOCUMENT
DN DOCUMENT CHANGE NOTICE
PA PAPER TAPE ASCII
PB PAPER TAPE BINARY
PM PAPER TAPE READ-IN-MODE

ITEM NO.	DWG NO./PART NO.	DESCRIPTION	QUANTITY/VARIATION								
			DL11-A	DL11-B	DL11-C	DL11-D	DL11-E			KIT CHECK BY ____ DATE ____	INSTALLATION CHECK BY ____ DATE ____
1	M7800	ASYNCHRONOUS LINE INTERFACE (EIA)	0	1	0	1	1				
2	G8000	FILTER NETWORK	0	A/R	0	A/R	A/R				
3	M7800-YA	ASYNCHRONOUS LINE INTERFACE (CURRENT LOOP)	1	0	1	0	0				
4	5408776	PRIORITY JUMPER LEVEL #4	1	1	1	1	1				
5	BC05-C-25	MODEM CABLE	0	1	0	1	1				
6	7008360	TTY CABLE	1	0	1	0	0				
7	-	CRYSTAL	1	1	1	1	1				
8	-	DL11 ENGINEERING DRAWINGS	1	1	1	1	1				
9	DEC-11-HDLAA-A-D	DL11 ASYNCHRONOUS LINE INTERFACE MANUAL	1	1	1	1	1				
10	LIBKIT-11-KL11-04	KL11 MAINDEC	1	1	0	0	0				
11	LIBKIT-11-DL11C-A-K	DL11 MAINDEC	0	0	1	1	0				
12	LIBKIT-11-DL11E-A-K	DL11 MAINDEC	0	0	0	0	1				
13	H315	MODEM TEST CONNECTOR	0	0	0	0	A/R				

NOTES: 1. G8000 IS REQUIRED ONLY IN PDP-11 SYSTEMS WHERE +15V IS NOT AVAILABLE. ONE PER DD11-A.

2. CRYSTAL FREQUENCY DEFINED BY CUSTOMER SPECIFIED BAUD RATE.
3. ONE H315 PER PDP11 SYSTEM
4. INSURE THAT TRANSPARENT VINYL TAPE HAS BEEN APPLIED TO THE TOP SURFACE OF THE CRYSTAL AND MOUNTING BRACKET.

TITLE	ASSY. NO.	SIZE	CODE	NUMBER	REV.	ECO NO
DL11 CHECK LIST	SHEET 1 OF 1	A	AL	DL11-0-5	C	DL11-00005
		DIST.				

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

DATE 6/21/72

TITLE DL11 INSTALLATION PROCEDURE

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
C	CHANGE PER ECO	DL11-4	JANSON	3/73	P. Janson	4-6-73
D	CHANGE PER ECO	DL11-5	CONDON	7/73	L. Condon	8/[illegible]/73

ENG	APPD	SIZE	CODE	NUMBER	REV
Paul E. Janson	Paul E. Janson	A	SP	DL11 0-2	D

DEC FORM NO. DRA 107A

ENGINEERING SPECIFICATION digital CONTINUATION SHEET

TITLE DL11 INSTALLATION PROCEDURE

DL11 INSTALLATION PROCEDURE:

Installation of the M7800 module or its variation as a DL11-A through DL11-E option consists of the following preparations:

1. Jumper insertion/deletion for selection of operation mode (A, B, C, D, or E).
2. Register address assignment.
3. Vector address assignment.
4. Priority assignment.
5. Special NPR jumper insertion/deletion.
6. Selection of data format (data bits, stop bits, parity).
7. Selection of crystal for baud rate.
8. Installation of G8000 in systems where +15v is not available.
9. Filter capacitor selection for high baud rate current-loop.
A. OPERATION MODE:

The following describes the jumpers associated with controlling the mode of operation (A,B,C,D, or E):

J1. Ties EIA driver to REQUEST-TO-SEND lead (pin 4) of dataset cable. IN for DL11-B,D, and E; does not affect DL11-A and C. Drawing DL-7.

J2. Ties EIA driver, normally used for the REQUEST-TO-SEND lead, to FORCE BUSY lead (pin 25) for use with Bell 103E. This is a customer option. If not specified, jumper is OUT for all DL11's. Drawing DL-7.

J3. When inserted, allows REQUEST-TO-SEND lead (pin 4) to be controlled by bit 2 of the receiver status register. OUT for DL11-B and D; IN for DL11-E; does not affect DL11-A and C. Drawing DL-4.

J4. When inserted, forces "DATA LEADS ONLY" mode of EIA operation. Turns DATA TERMINAL READY (pin 20) and REQUEST-TO-SEND (pin 4) on. IN for DL11-B and D; OUT for DL11-E; does not affect DL11-A and C. Drawing DL-4.

J5. When inserted, allows the BREAK bit to function. OUT for DL11-A and B; IN for DL11-C,D, and E. Drawing DL-4.

J6. When inserted, allows DSET INT to cause interrupts. OUT for DL11-A,B,C and D; IN for DL11-E. Drawing DL-4.

J7. When inserted, allows dataset control bits to be read as part of the receiver status register.

SIZE	CODE	NUMBER	REV
A	SP	DL11-0-2	D

DEC FORM NO DRA 108 DEC 16-(381)-1022-N370

J7. (con't)

OUT for DL11-A,B,C and D; IN for DL11-E. Drawing DL-2.

J8. When inserted, allows error bits to be read as part of the receiver data register. OUT for DL11-A and B; IN for DL11-C,D and E. Drawing DL-2.

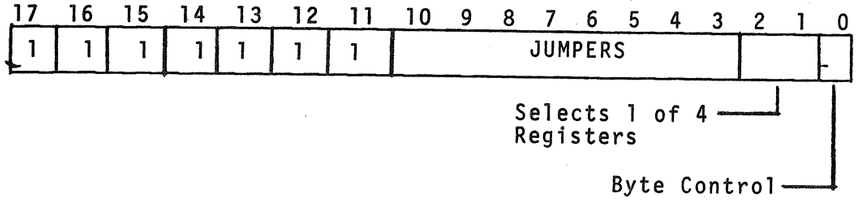
Summary of mode control jumpers:

JUMPER	A	B	C	D	E	DRAWING
J1	*	IN	*	IN	IN	DL-7
J2	OUT	OUT	OUT	OUT	OUT	DL-7
J3	*	OUT	*	OUT	IN	DL-4
J4	*	IN	*	IN	OUT	DL-4
J5	OUT	OUT	IN	IN	IN	DL-4
J6	OUT	OUT	OUT	OUT	IN	DL-4
J7	OUT	OUT	OUT	OUT	IN	DL-2
J8	OUT	OUT	IN	IN	IN	DL-2

*= don't care

B. REGISTER ADDRESS ASSIGNMENTS:

The DL11 can respond to addresses with the following format:



Bits 10 through 3 are controlled by jumpers A1Ø to A3. A jumper inserted indicates a zero.

For the DL11-A and B used as the console device, address 777560 is assigned. For additional units, assign 776XX0, where XX=50 for the first additional unit and XX=67 for the 16th unit.

For the DL11-C,D and E assign address 77XXX0, where XXX=561 for the first line, and XXX=617 for the 31st line. Assign all C's first, then D's, and then E's.

C. VECTOR ADDRESS ASSIGNMENT:

Jumpers V8 through V3 control the interrupt vector. A jumper inserted provides a vector bit of one. Vectors can be produced in the form XXØ and XX4, where XX ranges from ØØ to 77.

For the DL11-A and B used as a console device the vector address is 060/064. For additional units, vectors are floating.

For the DL11-C,D, and E vector addresses are floating. Assign all C's first, then D's, then E's.

D. PRIORITY ASSIGNMENT:

Interrupt priority is established by inserting a "priority plug" in the socket at IC location E19. For DL11-A,B,C, D and E use level 4.

SUMMARY OF REGISTER, VECTOR AND PRIORITY ASSIGNMENTS:

	ADDRESS	VECTOR	PRIORITY
DL11-A,B CONSOLE	777560 777562 777564 777566	60/64	BR4
DL11-A,B ADDITIONAL UNITS	776XXØ 776XX2 776XX4 776XX6	Floating	BR4

Where XX= 50 for line #1
and XX= 67 for line #16

	ADDRESS	VECTOR	PRIORITY
DL11-C,D,E	77XXXØ 77XXX2 77XXX4 77XXX6	Floating	4

Where XXX= 561 for line #1
and XXX= 617 for line #31

E. SPECIAL NPR JUMPER:

Jumper N1, shown on drawing DL-6, controls the response of the interrupt circuit to an NPR request. The jumper should normally be IN, except for 11/20 and 11/15 systems without the KH11 option.

F. SELECTION OF DATA FORMAT:

1. Data Bits

Split lug pairs NB2 and NB1 control the number of data bits in the serial character as follows:

NB2	NB1	# OF DATA BITS
OUT	OUT	8
OUT	IN	7
IN	OUT	6
IN	IN	5

2. Parity

Parity is controlled by split lug pairs NP and EPS as follows:

NP	EPS	PARITY
OUT	OUT	OFF
OUT	IN	OFF
IN	OUT	EVEN
IN	IN	ODD

3. Stop Bits

Split lug pair 2SB and jumpers J9, J10 and J11 control the number of stop bits in the serial character as follows:

2SB	J9	J10	J11	# OF STOP BITS
OUT	OUT	IN	OUT	2
IN	OUT	IN	OUT	1
IN	OUT	OUT	IN	1.5 for TI, GI, and SCM UARTS
IN	IN	OUT	OUT	1.5 for WD UARTS

G. CRYSTAL SELECTION:

The clocking scheme of the DL11 consists of a single crystal oscillator feeding a divider network, with two 10-position switches tapping various points to feed into the UART's

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transmitter and receiver sections. Thus, for a given crystal frequency, 8 baud rates are independently selectable for transmit and receive. The two addition switch positions select external clocks.

SPEED GROUP		1	2	3	4
		CRYSTAL (HZ)			
POSITION	FACTOR	844.8K	1.03296M	1.152M	4.608M
1*	23040	36.7	44.8	50	200
2	15360	55	67.3	75	300
3	7680	110	134.5	150	600
4	3840	220	269	300	1200
5	1920	440	538	600	2400
6	960	880	1076	1200	4800
7	640	1320	1614	1800	7200
8	480	1760	2152	2400	9600

*Most counter-clock wise position.

To determine a crystal frequency for a non-standard baud rate, pick the position of the closest baud rate in the 1.152MHz column, and then multiply the non-standard baud rate by the factor for that position. For example, if the customer specifies 1050 baud, this is closest to 1200 baud, position 6.

1050 X 960 = 10080000 = 1.008MHz.

The crystal frequency should not fall outside the range of the standard crystals.

DEC part numbers for the standard crystals are as follows:

844.8 KHz	18-10245-1*
1.03296 MHz	18-05501-6
1.152 MHz	18-05501-5
4.608 MHz	18-05501-7

*Use A or C cut crystals only. Do not use crystals marked NE-6D.

When ordering a special crystal, refer to purchase specification 18-05501 for crystal specification.

Insure that transparent vinyl tape (9008269) is applied to the top surfaces of the crystal and mounting brackets to insulate from adjacent modules.

H. G8000 INSTALLATION:

For DL11-B, D, and E a positive voltage is required between 9 and 15 volts to operate the EIA drivers. For PDP-11/20 and PDP-11/15 systems with the H720 power supply, a G8000 module must be installed to provide this voltage. Using a filter network, this module converts the full-wave rectified "+8V" signal to a positive DC voltage.

1. Install G8000 into slot AØ2 of DD11-A.
2. Wire AØ3V2 to AØ2V2.
3. Wire AØ2N2 to CXXU1 where XX is the slot location of the M7800.

Refer to diagram 1.

I. FILTER CAPACITOR SELECTION:

For DL11-A's and DL11-C's, which operate with 20ma current loops, capacitors are used to filter the receive line and slow the switching time of the transmit line. To avoid excessive distortion above 150 baud, the capacitance in each of these two circuits must be reduced. This is accomplished by clipping C29 (.47 mfd) and C31 (1000 pf), both shown on drawing DL-3.

J. DL11-B,D,E in Systems with +15V available using DD11-A

There is a special situation of using a DD11-A to mount a DL11-B, D, Or E in systems with +15V available. These systems have +15V available and it appears at pin AØ3V2 of the DD11-A when using power harness such as 7009177, 7008855, or 7008909. In this situation, no G8000 is necessary, and +15V can be wired directly from AØ3V2 to CXXU1, where XX is the slot number of the DL11. NOTE: this does not apply to DL11-A or C or DD11-B.

K. When using the DL11-B,D,E in an 11/05 processor pin CXXU1 has +15V available on it so no G8000 or no jumpers are required.

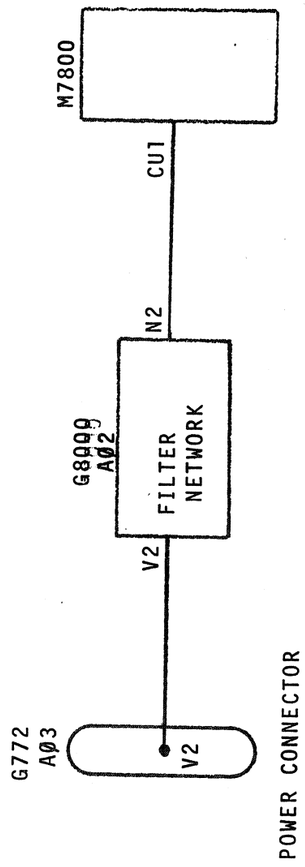

DIAGRAM 1. G8000 INSTALLATION