

DRAWING DIRECTORY

CUSTOMER PRINT SET INDEX

THIS IS PRINT SET

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SEQUENCE

SEQUENCE

PRINT SET #1

DRAWING DIRECTORY	B-DD-DL11-0
ASYNCHRONOUS LINE INTERFACE	C-UA-DL11-0-0
ASYNCHRONOUS LINE INTERFACE (PL)	A-PL-DL11-0-0
ASYNCHRONOUS LINE INTERFACE	E-CS-M7800YA+1
CABLE ASSEMBLY (KLS/E)	D-1A-7008360-0-0
SOFTWARE LIST	A-SL-DL11-0-4
ACCESSORY LIST	A-AL-DL11-0-5
INSTALLATION PROCEDURE	A-SP-DL11-0-2

PRINT SET #3

DRAWING DIRECTORY B-DD-DLII-0
 ASYNCHRONOUS LINE
 INTERFACE C-UA-DLII-0-0
 ASYNCHRONOUS LINE
 INTERFACE (PL) A-PL-DLII-0-0
 ASYNCHRONOUS LINE
 INTERFACE E-CS-M7800-0-1
 CABLE, MODEM BC05C D-UA-BC05C-0-0
 CABLE ASSEMBLY (KL8IE) D-1A-7008360-0-0
 MODEM TEST CONN. D-CS-H315-0-1
 INSTALLATION PROCEDURE A-SP-DLII-0-2

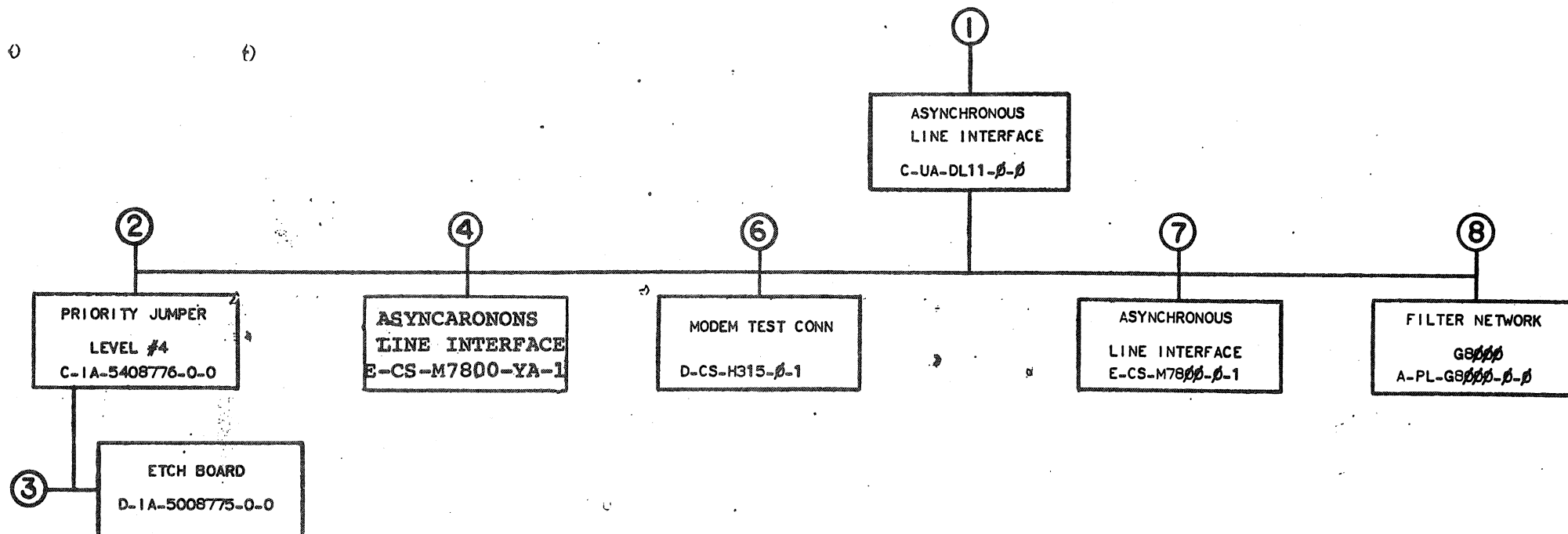
PRINT SET #2

DRAWING DIRECTORY	B-DD-DL11-Ø
ASYNCHRONOUS LINE INTERFACE	C-UA-DL11-Ø-Ø
ASYNCHRONOUS LINE INTERFACE (PL)	A-PL-DL11-Ø-Ø
ASYNCHRONOUS LINE INTERFACE	E-CS-M7ØØ-Ø-1
CABLE, MODEM BCØ5C	D-UA-BCØ5C-Ø-Ø
FILTER NETWORK	B-CS-G8ØØØ-Ø-1
MODEM TEST CONN	D-CS-H315-Ø-1
SOFTWARE LIST	A-SL-DL11-Ø-4
ACCESSORY LIST	A-AL-DL11-Ø-5
INSTALLATION PROCEDURE	A-SP-DL11-Ø-2

UNIT VARIATIONS

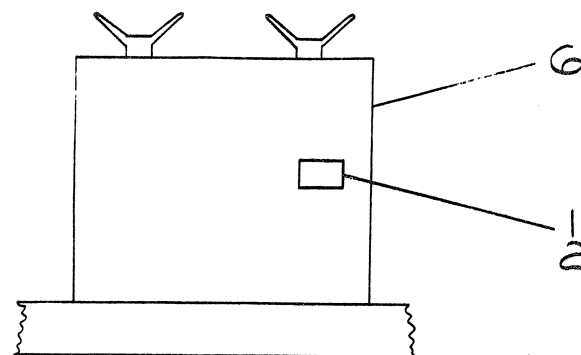
PRINT SET TYPE

[illegible][illegible]



FILE	ASYNCHRONOUS LINE INTERFACE	SHEET 2 OF 3	SIZE CODE B DD	NUMBER DL11 - Ø	REV F
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NOTES:

- G 8000 IS REQUIRED ONLY IN PDP 11 SYSTEMS WHERE +15V IS NOT AVAILABLE. THE INSTALLATION REQUIRES 2 WIRES TO BE ADDED.
A03V2 - A02V2
A02N2 - CXXU1
WHERE (XX) IS THE SLOT NUMBER CONTAINING THE DL11.
- ITEMS INDICATED WITH ASTERICK (*) ARE SHOWN FOR REFERENCE ONLY AND ARE NOT PART OF THIS UNIT.

	A	B	C	D	E	F
4	M920 * UNIBUS OUT			G727 *		
3	G772 * POWER CONNECTOR			G727 *		
2	G8000 FILTER NETWORK SEE NOTE 1			G727 *		
1	M920 * UNIBUS IN			M7800/M7800-YA		

DD11-A *

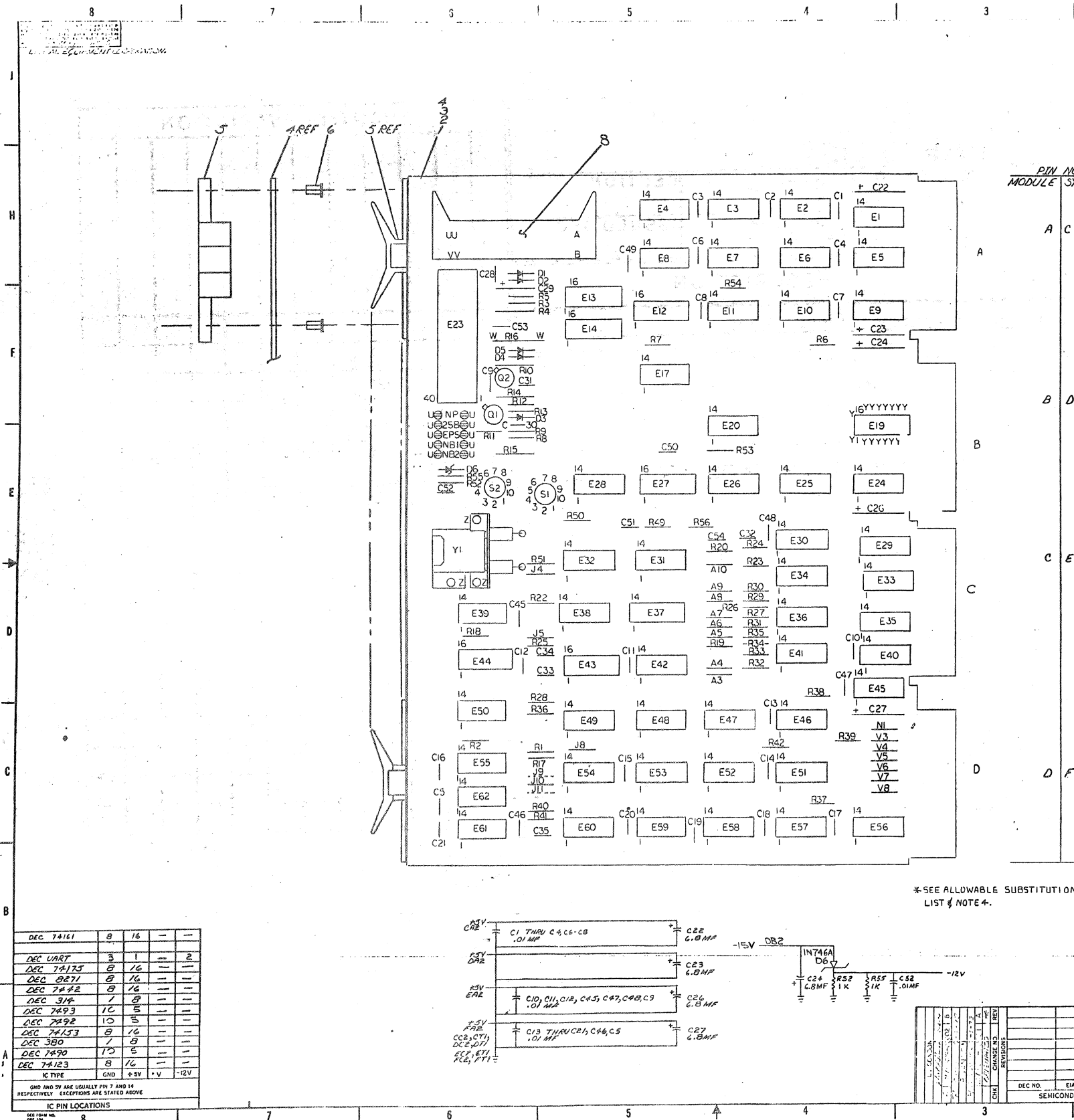
SEE NOTE 2

REV.	CHANGE NO.	REV.
A	DL11-00001	
B	DL11-00002	
C	DL11-00005	
D	DL11-00006	

DEC FORM NO.
DRC 100-A

FIRST USED ON OPTION/MODEL PDP-11	QTY.	DESCRIPTION	PART NO.	ITEM NO.
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES				
DECIMALS	ANGLES			
.XXX = .005	± 0° 30'			
.XX = .02				
.X = .1				
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY	✓			
MATERIAL	NEXT HIGHER ASSY.			
FINISH	SCALE NONE			
SHEET		OF		DIST.
B-DD-DL11-0		C UA DL11-0-0		REV. D

DIGITAL EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS			QUANTITY / VARIATION													
PARTS LIST			DL11-A	DL11-B	DL11-C	DL11-D	DL11-E									
MADE BY M. PIERCE		CHECKED J. FERGUSON	SECTION													
DATE 4/27/72		DATE 4/27/72	1													
ENG <i>P. E. Janson</i>		PROD <i>J. Mac Sique</i>	ISSUED SECT.													
DATE 5/11/72		DATE 5/15/72	1													
ITEM NO.	DWG NO. / PART NO.	DESCRIPTION	DL11-A	DL11-B	DL11-C	DL11-D	DL11-E									
1	C-IA-5408776-0-0	PRIORITY JUMPER LEVEL #4	1	1	1	1	1									
2	C-IA-5408778-0-0	PRIORITY JUMPER LEVEL #5	-	-	-	-	-									
3	D-UA-BC05C-25	CABLE, MODEM BC05C	-	1	-	1	1									
4	D-IA-7008360-0-0	CABLE ASSEMBLY (KL8E)	1	-	1	-	-									
5	D-CS-H315-0-1	MODEM TEST CONNECTOR	-	-	-	-	A/R	See Note 2								
6	E-CS-M7800-0-1	ASYNCHRONOUS LINE INTERFACE	-	1	-	1	1									
7	A-PL-G8000-0-0	FILTER NETWORK	-	A/R	-	A/R	A/R	See Note 1								
8		CRYSTAL	A/R	A/R	A/R	A/R	A/R	See Note 3								
9	E-CS-M7800-YA-1	ASYNCHRONOUS LINE INTERFACE	1	-	1	-	-									
NOTES:																
1. G8000 IS REQUIRED ONLY IN PDP 11																
SYSTEMS WHERE +15V IS NOT																
AVAILABLE. ONE PER DD11-A.																
2. ONE H315 PER PDP11 SYSTEM																
3. CRYSTAL FREQUENCY DEFINED BY CUSTOMER																
SPECIFIED BAUD RATE																
4. APPLY TAPE TO TOP SURFACES OF CRYSTAL																
AND MOUNTING BRACKETS TO INSULATE FROM																
ADJACENT MODULES.																
10	9008269	TRANSPARENT VINYL TAPE	A/R													
TITLE																
ASYNCHRONOUS																
LINE INTERFACE																
ASSY NO.																
C-UA-DL11-0-0																
SHEET 1 OF 1																
SIZE CODE																
A PL																
NUMBER																
DL11-0-0																
REV.																
D																
ECO NO.																
DL11-00006																



NOTES:
1.) PIN NOTATION THROUGHOUT IS ORDERED UPON MODULE PLACEMENT IN THE SYSTEM UNIT. MODULE REFERENCE ALONE IS OBTAINED BY CONVERTING THE FIRST LETTER ACCORDING TO THE PIN NOMENCLATURE CHART AT THE LEFT.
2.) JUMPERS TO BE USED AT CONNECTIONS A3-A10, J4-J6, J8-J10, V3-V5, AND N1.
3.) LETTERS ENCLOSED IN PARENTHESIS REFER TO PINS ON THE BERG CONNECTOR. EXAMPLE: (X1).
4.) ON ITEM NO. 23, ALL 7 CHIPS MUST BE EITHER DEC 380'S OR ITS SUBSTITUTE 11360 IC'S. A DEC 380 AND 11360 MIXTURE OF THESE 7 CHIPS IS NOT ALLOWED. E28 MUST BE A DEC 380. (ITEM NO. 6B).

PIN NOMENCLATURE
MODULE SYSTEM UNIT

ALLOWABLE SUBSTITUTION LIST			
ORIG. PART NO.	SUBSTITUTE DESCRIPTION	PART NO.	ITEM NO.
1909485	IC 11380	1911113	23

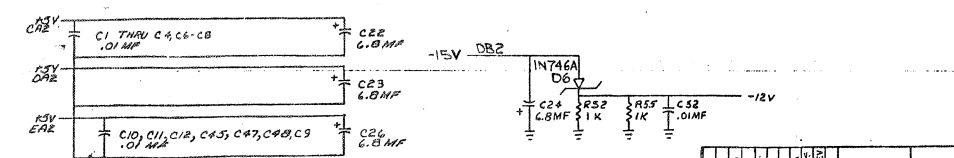
ITEM NO.	DESCRIPTION	PART NO.	ITEM NO.
1	E28	IC DEC 380	1909485
1	R3	RES 750 OHM 1/4W 5%	1301401
1	R38	RES 390 OHM 1/4W 5%	1300107
1	D6	DIODE 1N24GA	1104860
2	Q1, Q2	TRANSISTOR GE 34C	1503401-00
1	C1	CAP 100PF 100V 5% TANT	1000005
1	C2	CAP 500PF 100V 5% TANT	1000005
2	C50, C51	CAP .047MF CERAMIC	1004678
1	E27	IC DEC 74161	1906550
1	C35	OP 330PF 100V 5% DIFFER. MICA	1000003
1	C36	OP 330PF 100V 5% DIFFER. MICA	1000003
1	C37	OP 330PF 100V 5% DIFFER. MICA	1000003
1	C38	OP 330PF 100V 5% DIFFER. MICA	1000003
1	C39	OP 330PF 100V 5% DIFFER. MICA	1000003
1	C40	OP 330PF 100V 5% DIFFER. MICA	1000003
1	C41	OP 330PF 100V 5% DIFFER. MICA	1000003
1	C42	OP 330PF 100V 5% DIFFER. MICA	1000003
1	C43	OP 330PF 100V 5% DIFFER. MICA	1000003
1	C44	OP 330PF 100V 5% DIFFER. MICA	1000003
1	C45	OP 330PF 100V 5% DIFFER. MICA	1000003
1	C46	OP 330PF 100V 5% DIFFER. MICA	1000003
1	C47	OP 330PF 100V 5% DIFFER. MICA	1000003
1	C48	OP 330PF 100V 5% DIFFER. MICA	1000003
1	C49	OP 330PF 100V 5% DIFFER. MICA	1000003
1	C50	OP 330PF 100V 5% DIFFER. MICA	1000003
1	C51	OP 330PF 100V 5% DIFFER. MICA	1000003
1	C52	OP 330PF 100V 5% DIFFER. MICA	1000003
1	C53	OP 330PF 100V 5% DIFFER. MICA	1000003
1	C54	OP 330PF 100V 5% DIFFER. MICA	1000003
1	C55	OP 330PF 100V 5% DIFFER. MICA	1000003
1	C56	OP 330PF 100V 5% DIFFER. MICA	1000003
1	C57	OP 330PF 100V 5% DIFFER. MICA	1000003
1	C58	OP 330PF 100V 5% DIFFER. MICA	1000003
1	C59	OP 330PF 100V 5% DIFFER. MICA	1000003
1	C60	OP 330PF 100V 5% DIFFER. MICA	1000003
1	C61	OP 330PF 100V 5% DIFFER. MICA	1000003
1	C62	OP 330PF 100V 5% DIFFER. MICA	1000003
1	C63	OP 330PF 100V 5% DIFFER. MICA	1000003
1	C64	OP 330PF 100V 5% DIFFER. MICA	1000003
1	C65	OP 330PF 100V 5% DIFFER. MICA	1000003
1	C66	OP 330PF 100V 5% DIFFER. MICA	1000003
1	C67	OP 330PF 100V 5% DIFFER. MICA	1000003
1	C68	OP 330PF 100V 5% DIFFER. MICA	1000003
1	C69	OP 330PF 100V 5% DIFFER. MICA	1000003
1	C70	OP 330PF 100V 5% DIFFER. MICA	1000003
1	C71	OP 330PF 100V 5% DIFFER. MICA	1000003
1	C72	OP 330PF 100V 5% DIFFER. MICA	1000003
1	C73	OP 330PF 100V 5% DIFFER. MICA	1000003
1	C74	OP 330PF 100V 5% DIFFER. MICA	1000003
1	C75	OP 330PF 100V 5% DIFFER. MICA	1000003
1	C76	OP 330PF 100V 5% DIFFER. MICA	1000003
1	C77	OP 330PF 100V 5% DIFFER. MICA	1000003
1	C78	OP 330PF 100V 5% DIFFER. MICA	1000003
1	C79	OP 330PF 100V 5% DIFFER. MICA	1000003
1	C80	OP 330PF 100V 5% DIFFER. MICA	1000003
1	C81	OP 330PF 100V 5% DIFFER. MICA	1000003
1	C82	OP 330PF 100V 5% DIFFER. MICA	1000003
1	C83	OP 330PF 100V 5% DIFFER. MICA	1000003
1	C84	OP 330PF 100V 5% DIFFER. MICA	1000003
1	C85	OP 330PF 100V 5% DIFFER. MICA	1000003
1	C86	OP 330PF 100V 5% DIFFER. MICA	1000003
1	C87	OP 330PF 100V 5% DIFFER. MICA	1000003
1	C88	OP 330PF 100V 5% DIFFER. MICA	1000003
1	C89	OP 330PF 100V 5% DIFFER. MICA	1000003
1	C90	OP 330PF 100V 5% DIFFER. MICA	1000003
1	C91	OP 330PF 100V 5% DIFFER. MICA	1000003
1	C92	OP 330PF 100V 5% DIFFER. MICA	1000003
1	C93	OP 330PF 100V 5% DIFFER. MICA	1000003
1	C94	OP 330PF 100V 5% DIFFER. MICA	1000003
1	C95	OP 330PF 100V 5% DIFFER. MICA	1000003
1	C96	OP 330PF 100V 5% DIFFER. MICA	1000003
1	C97	OP 330PF 100V 5% DIFFER. MICA	1000003
1	C98	OP 330PF 100V 5% DIFFER. MICA	1000003
1	C99	OP 330PF 100V 5% DIFFER. MICA	1000003
1	C100	OP 330PF 100V 5% DIFFER. MICA	1000003

*SEE ALLOWABLE SUBSTITUTION LIST & NOTE 4.

DEC 74161	8	16	—
DEC UART	3	1	2
DEC 74173	8	16	—
DEC 8271	8	16	—
DEC 74172	8	16	—
DEC 314	1	8	—
DEC 7493	10	5	—
DEC 7492	10	5	—
DEC 74173	8	16	—
DEC 380	1	8	—
DEC 7490	10	5	—
DEC 74173	8	16	—
IC TYPE	CND	+5V	+12V

QND AND 7V ARE USUALLY PIN 7 AND 14 RESPECTIVELY. EXCEPTIONS ARE STATED ABOVE.

IC PIN LOCATIONS

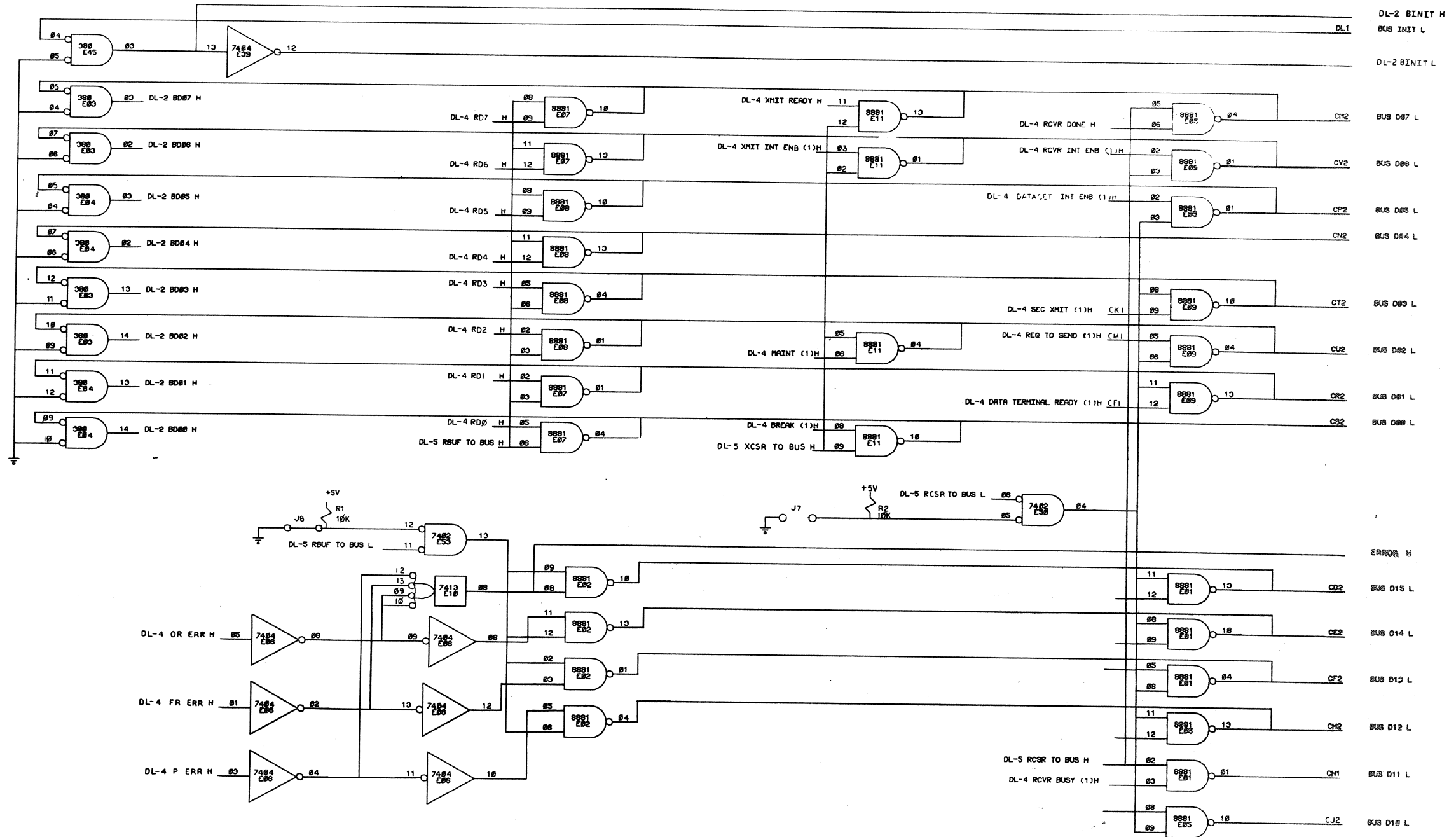


DEC NO.	EIA NO.	SEMICONDUCTOR CONVERSION CHART
74161	161	74161
74173	173	74173
8271	8271	8271
74172	172	74172
314	314	314
7493	7493	7493
7492	7492	7492
74173	173	74173
380	380	380
7490	7490	7490
74173	173	74173

QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.
1	E28	IC DEC 380	1909485	23
1	R3	RES 750 OHM 1/4W 5%	1301401	47
1	R38	RES 390 OHM 1/4W 5%	1300107	44
1	D6	DIODE 1N24GA	1104860	45
2	Q1, Q2	TRANSISTOR GE 34C	1503401-00	64
1	C1	CAP 100PF 100V 5% TANT	1000005	63
1	C2	CAP 500PF 100V 5% TANT	1000005	62
2	C50, C51	CAP .047MF CERAMIC	1004678	61
1	E27	IC DEC 74161	1906550	60
1	C35	OP 330PF 100V 5% DIFFER. MICA	1000003	59
1	C36	OP 330PF 100V 5% DIFFER. MICA	1000003	58
1	C37	OP 330PF 100V 5% DIFFER. MICA	1000003	57
1	C38	OP 330PF 100V 5% DIFFER. MICA	1000003	56
1	C39	OP 330PF 100V 5% DIFFER. MICA	1000003	55
1	C40	OP 330PF 100V 5% DIFFER. MICA	1000003	54
1	C41	OP 330PF 100V 5% DIFFER. MICA	1000003	53
1	C42	OP 330PF 100V 5% DIFFER. MICA	1000003	52
1	C43	OP 330PF 100V 5% DIFFER. MICA	1000003	51
1	C44	OP 330PF 100V 5% DIFFER. MICA	1000003	50
1	C45	OP 330PF 100V 5% DIFFER. MICA	1000003	49
1	C46	OP 330PF 100V 5% DIFFER. MICA	1000003	48
1	C47	OP 330PF 100V 5% DIFFER. MICA	1000003	47
1	C48	OP 330PF 100V 5% DIFFER. MICA	1000003	46
1	C49	OP 330PF 100V 5% DIFFER. MICA	1000003	45
1	C50	OP 330PF 100V 5% DIFFER. MICA	1000003	44
1	C51	OP 330PF 100V 5% DIFFER. MICA	1000003	43
1	C52	OP 330PF 100V 5% DIFFER. MICA	1000003	42
1	C53	OP 330PF 100V 5% DIFFER. MICA	1000003	41
1	C54	OP 330PF 100V 5% DIFFER. MICA	1000003	40
1	C55	OP 330PF 100V 5% DIFFER. MICA	1000003	39
1	C56	OP 330PF 100V 5% DIFFER. MICA	1000003	38
1	C57	OP 330PF 100V 5% DIFFER. MICA	1000003	37
1	C58	OP 330PF 100V 5% DIFFER. MICA	1000003	36
1	C59	OP 330PF 100V 5% DIFFER. MICA	1000003	35
1	C60	OP 330PF 100V 5% DIFFER. MICA	1000003	34
1	C61	OP 330PF 100V 5% DIFFER. MICA	1000003	33
1	C62	OP 330PF 100V 5% DIFFER. MICA	1000003	32
1	C63	OP 330PF 100V 5% DIFFER. MICA	1000003	31
1	C64	OP 330PF 100V 5% DIFFER. MICA	1000003	30
1	C65	OP 330PF 100V 5% DIFFER. MICA	1000003	29
1	C66	OP 330PF 100V 5% DIFFER. MICA	1000003	28
1	C67	OP 330PF 100V 5% DIFFER. MICA	1000003	27
1	C68	OP 330PF 100V 5% DIFFER. MICA	1000003	26
1	C69	OP 330PF 100V 5% DIFFER. MICA	1000003	25
1	C70	OP 330PF 100V 5% DIFFER. MICA	1000003	24
1	C71	OP 330PF 100V 5% DIFFER. MICA	1000003	23
1	C72	OP 330PF 100V 5% DIFFER. MICA	1000003	22
1	C73	OP 330PF 100V 5% DIFFER. MICA	1000003	21
1	C74	OP 330PF 100V 5% DIFFER. MICA	1000003	20
1	C75	OP 330PF 100V 5% DIFFER. MICA	1000003	19
1	C76	OP 330PF 100V 5% DIFFER. MICA	1000003	18
1	C77	OP 330PF 100V 5% DIFFER. MICA	1000003	17
1	C78	OP 330PF 100V 5% DIFFER. MICA	1000003	16
1	C79	OP 330PF 100V 5% DIFFER. MICA	1000003	15
1	C80	OP 330PF 100V 5% DIFFER. MICA	1000003	14
1	C81	OP 330PF 100V 5% DIFFER. MICA	1000003	13
1	C82	OP 330PF 100V 5% DIFFER. MICA	1000003	12
1	C83	OP 330PF 100V 5% DIFFER. MICA	1000003	11
1	C84	OP 330PF 100V 5% DIFFER. MICA	1000003	10
1	C85	OP 330PF 100V 5% DIFFER. MICA	1000003	9
1	C86	OP 330PF 100V 5% DIFFER. MICA	1000003	8
1	C87	OP 330PF 100V 5% DIFFER. MICA	1000003	7
1	C88	OP 330PF 100V 5% DIFFER. MICA	1000003	6
1	C89	OP 330PF 100V 5% DIFFER. MICA	1000003	5
1	C90	OP 330PF 100V 5% DIFFER. MICA	1000003	4
1	C91	OP 330PF 100V 5% DIFFER. MICA	1000003	3
1	C92	OP 330PF 100V 5% DIFFER. MICA	1000003	2
1	C93	OP 330PF 100V 5% DIFFER. MICA	1000003	1

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REVISIONS		
CHK.	CHANGE NO.	REV.

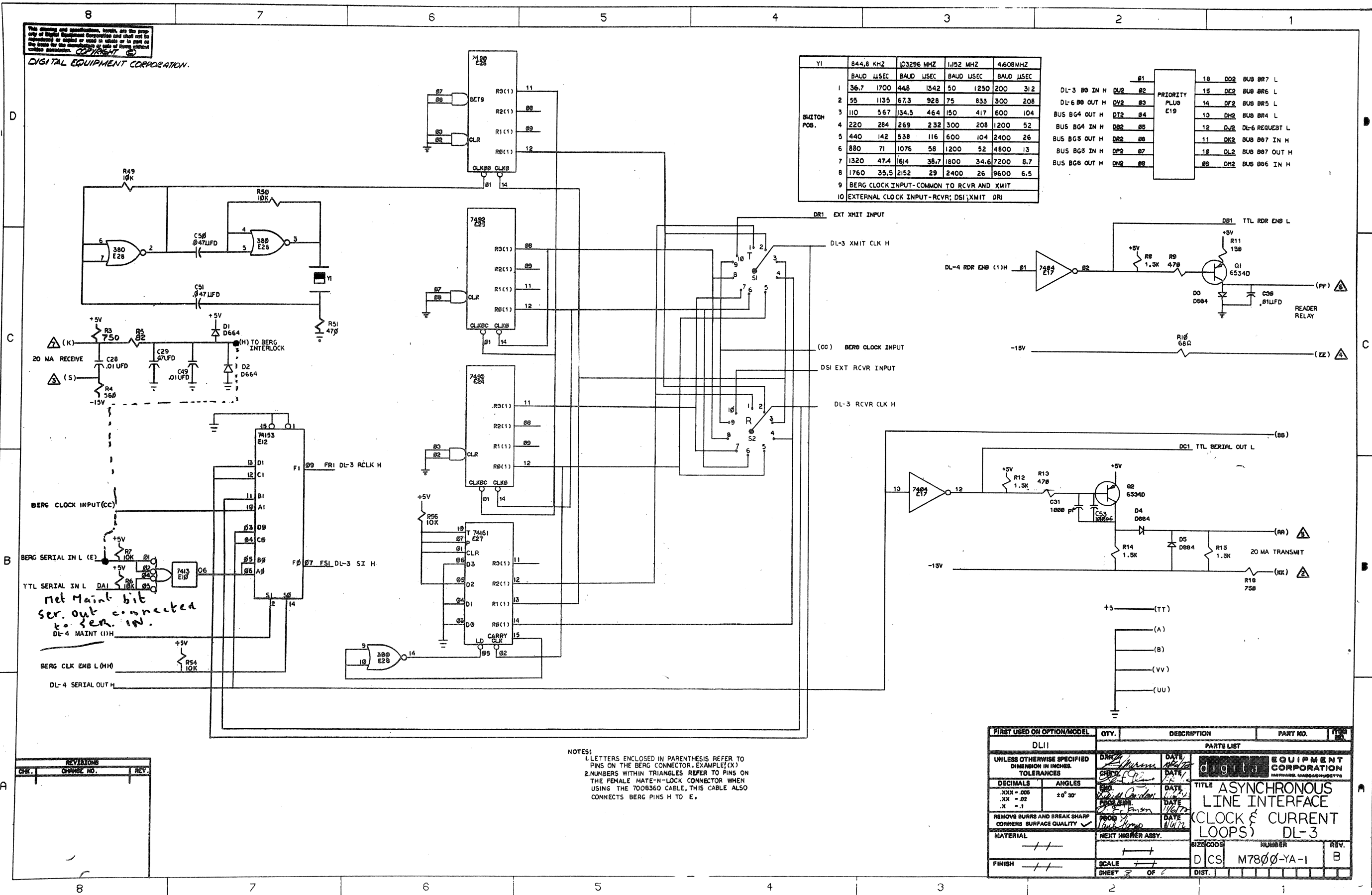
FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
DL11				
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES TOLERANCES	DATE 1/16/72	DATE 1/16/72	DATE 1/16/72	DATE 1/16/72
DECIMALS	ANGLES			
.XXX - .008	±0° 30'			
.XX - .02				
.X - .1				
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY	DATE 1/16/72	DATE 1/16/72	DATE 1/16/72	DATE 1/16/72
MATERIAL	NEXT HIGHER ASSY.	SIZE CODE	NUMBER	REV.
FINISH	SCALE	D/C	M7800-YA-1	B
	SHEET 2 OF 6	DIST.		

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DIGITAL EQUIPMENT CORPORATION.

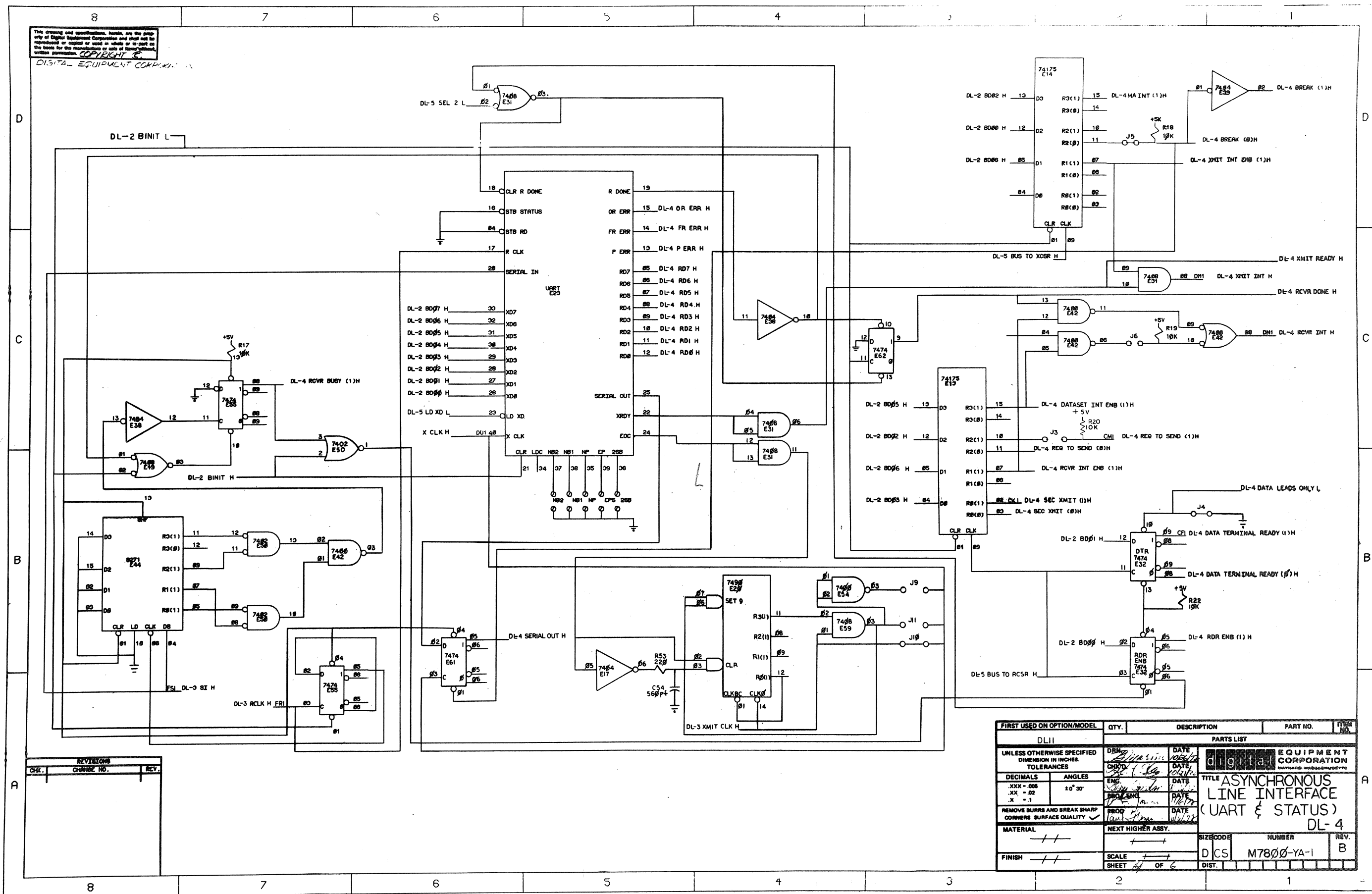
Y1	844.8 KHZ	103296 MHZ	1.152 MHZ	4.608MHZ
BAUD USEC	BAUD USEC	BAUD USEC	BAUD USEC	
1	36.7 1700	448 1342	50 1250	200 312
2	55 1135	673 928	75 833	300 208
3	110 567	1345 464	150 417	600 104
4	220 284	269 232	300 208	1200 52
5	440 142	538 116	600 104	2400 26
6	880 71	1076 58	1200 52	4800 13
7	1320 47.4	1614 38.7	1800 34.6	7200 8.7
8	1760 35.5	2152 29	2400 26	9600 6.5
9	BERG CLOCK INPUT-COMMON TO RCVR AND XMIT			
10	EXTERNAL CLOCK INPUT-RCVR; DSI; XMIT DRI			

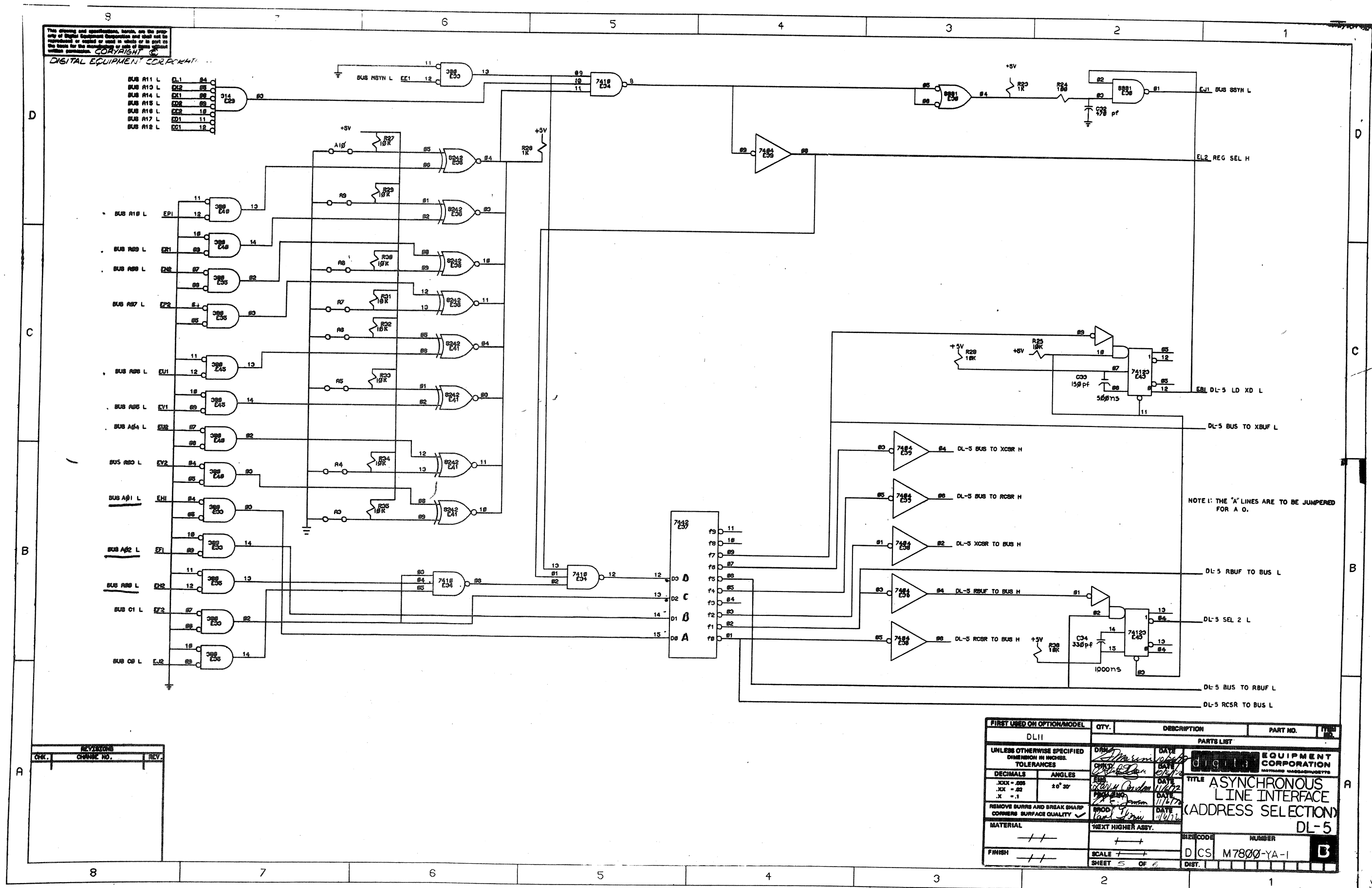
DL-3 IN H	DL-3 OUT H	DL-3 IN H	DL-3 OUT H
DL-3 IN H	DL-3 OUT H	DL-3 IN H	DL-3 OUT H
DL-3 IN H	DL-3 OUT H	DL-3 IN H	DL-3 OUT H
DL-3 IN H	DL-3 OUT H	DL-3 IN H	DL-3 OUT H
DL-3 IN H	DL-3 OUT H	DL-3 IN H	DL-3 OUT H
DL-3 IN H	DL-3 OUT H	DL-3 IN H	DL-3 OUT H
DL-3 IN H	DL-3 OUT H	DL-3 IN H	DL-3 OUT H
DL-3 IN H	DL-3 OUT H	DL-3 IN H	DL-3 OUT H
DL-3 IN H	DL-3 OUT H	DL-3 IN H	DL-3 OUT H
DL-3 IN H	DL-3 OUT H	DL-3 IN H	DL-3 OUT H



NOTES:
1. LETTERS ENCLOSED IN PARENTHESIS REFER TO PINS ON THE BERG CONNECTOR. EXAMPLE: (X)
2. NUMBERS WITHIN TRIANGLES REFER TO PINS ON THE FEMALE MATE-N-LOCK CONNECTOR WHEN USING THE 7008360 CABLE. THIS CABLE ALSO CONNECTS BERG PINS H TO E.

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	REV.
DL11				
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES				
DECIMALS	ANGLES			
.XXX - .005	±0° 30'			
.XX - .02				
.X - .1				
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY				
MATERIAL				
FINISH				
DATE	DATE	DATE	DATE	DATE
BY	BY	BY	BY	BY
CHKD	CHKD	CHKD	CHKD	CHKD
APPROVED	APPROVED	APPROVED	APPROVED	APPROVED
TITLE	ASYNCHRONOUS LINE INTERFACE (CLOCK & CURRENT LOOPS) DL-3			
SIZE/CODE	NUMBER	REV.		
D CS	M7800-YA-1	B		
SHEET	OF	DIST.		





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DIGITAL EQUIPMENT CORPORATION

D

C

B

A

8

7

6

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8

7

6

5

4

3

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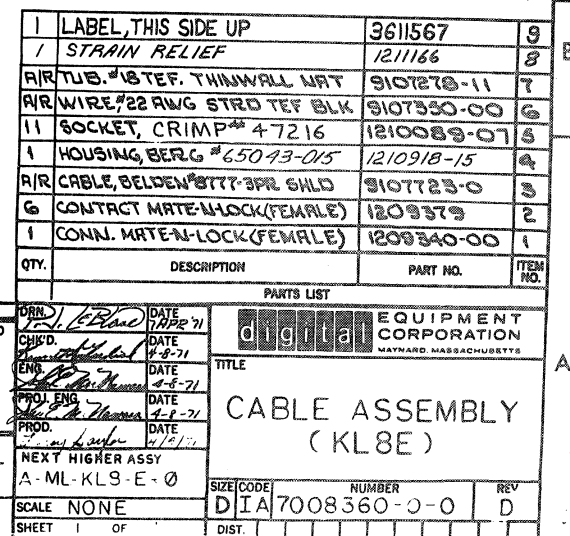
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NOTES:

1. * **ASTERISKS INDICATE** CAVITIES NOT USED OR DESIGNATED BY LETTERS.
2. DRAIN WIRES TO BE CUT BACK TO OUTER INSULATION ON P1 END OF CABLE ONLY. SHIELDS TO BE CUT BACK TO OUTER INSULATION ON BOTH ENDS OF CABLES.
3. DRAIN WIRES ON P2 END OF CABLE TO BE EACH ENCLOSED WITH ITEM*7 (TUBING) FROM END OF CABLE JACKET TO POINT WHERE THEY ENTER P2 CONNECTOR.
4. ITEM*6(WIRE) TO BE APPROXIMATELY ONE(1) INCH LONG.
5. PLACE ITEM*8("THIS SIDE UP" STICKER) ON LETTERED SIDE OF ITEM*4 (BERG HOUSING) AS SHOWN.



[illegible]

DIGITAL EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS				LEGEND		QUANTITY/VARIATION											
ACCESSORY LIST																	
MADE BY E. Pellegrini		CHECKED <i>P. Janson</i>		SECTION		PA PAPER TAPE ASCII											
DATE June 26, 1972		DATE 8-8-72				PB PAPER TAPE BINARY											
ENG Paul Janson		PROD <i>J. Janson</i>		ISSUED SECT.		PM PAPER TAPE											
DATE June 26, 1972		DATE 8-8-72				READ-IN-MODE											
ITEM NO.	DWG NO. / PART NO.	DESCRIPTION				DL11-A	DL11-B	DL11-C	DL11-D	DL11-E		KIT CHECK	BY	DATE	INSTALLATION CHECK	BY	DATE
1	M7800	ASYNCHRONOUS LINE INTERFACE (EIA)				1	1	1	1	1							
2	G8000	FILTER NETWORK				0	A/R	0	A/R	0							
3	M7800-YA	ASYNCHRONOUS LINE INTERFACE (CURRENT LOOP)				1	0	1	0	0							
4	5408776	PRIORITY JUMPER LEVEL #4				1	1	1	1	1							
5	BC05-C-25	MODEM CABLE				0	1	0	1	1							
6	7008360	TTY CABLE				1	0	1	0	0							
7	-	CRYSTAL				1	1	1	1	1							
8	-	DL11 ENGINEERING DRAWINGS				1	1	1	1	1							
9	DEC-11-HDLAA-A-D	DL11 ASYNCHRONOUS LINE INTERFACE MANUAL				1	1	1	1	1							
10	LIBKIT-11-KL11-04	KL11 MAINDEC				1	1	0	0	0							
11	LIBKIT-11-DL11C-A-K	DL11 MAINDEC				0	0	1	1	0							
12	LIBKIT-11-DL11E-A-K	DL11 MAINDEC				0	0	0	0	1							
13	H315	MODEM TEST CONNECTOR				0	0	0	0	A/R							
NOTES: 1. G8000 IS REQUIRED ONLY IN PDP-11 SYSTEMS																	
WHERE +15V IS NOT AVAILABLE. ONE PER DD11-A.																	
2. CRYSTAL FREQUENCY DEFINED BY CUSTOMER SPECIFIED BAUD RATE.																	
3. ONE H315 PER PDPII SYSTEM																	
4. INSURE THAT TRANSPARENT VINYL TAPE HAS BEEN APPLIED TO THE																	
TOP SURFACE OF THE CRYSTAL AND MOUNTING BRACKET.																	
TITLE DL11 CHECK LIST				ASSY. NO.		SIZE CODE A AL		NUMBER DL11-0-5				REV. C		ECO NO DL11-00005			
				SHEET 1 OF 1		DIST.											

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DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

DATE 6-21-72

TITLE DL11 INSTALLATION PROCEDURE

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
C	CHANGE PER ECO	DL11-4	JANSON	3/73	P. Janson	4-6-73
D	CHANGE PER ECO	DL11-5	CONDON	7/73	L. Condon	8/73

ENG	APPD	SIZE	CODE	NUMBER	REV
Paul F. Janson	<i>Paul F. Janson</i>	A	SP	DL11 0-2	D

DEC FORM NO.
DRA 107A

SHEET 1 OF 8

ENGINEERING SPECIFICATION

000000

CONTINUATION SHEET

TITLE DL11 INSTALLATION PROCEDURE

DL11 INSTALLATION PROCEDURE:

Installation of the M7800 module or its variation as a DL11-A through DL11-E option consists of the following preparations:

1. Jumper insertion/deletion for selection of operation mode (A, B, C, D, or E).
2. Register address assignment.
3. Vector address assignment.
4. Priority assignment.
5. Special NPR jumper insertion/deletion.
6. Selection of data format (data bits, stop bits, parity).
7. Selection of crystal for baud rate.
8. Installation of G8000 in systems where +15v is not available.
9. Filter capacitor selection for high baud rate current-loop.

A. OPERATION MODE:

The following describes the jumpers associated with controlling the mode of operation (A,B,C,D, or E):

- J1. Ties EIA driver to REQUEST-TO-SEND lead (pin 4) of dataset cable. IN for DL11-B,D, and E; does not affect DL11-A and C. Drawing DL-7.
- J2. Ties EIA driver, normally used for the REQUEST-TO-SEND lead, to FORCE BUSY lead (pin 25) for use with Bell 103E. This is a customer option. If not specified, jumper is OUT for all DL11's. Drawing DL-7.
- J3. When inserted, allows REQUEST-TO-SEND lead (pin 4) to be controlled by bit 2 of the receiver status register. OUT for DL11-B and D; IN for DL11-E; does not affect DL11-A and C. Drawing DL-4.
- J4. When inserted, forces "DATA LEADS ONLY" mode of EIA operation. Turns DATA TERMINAL READY (pin 20) and REQUEST-TO-SEND (pin 4) on. IN for DL11-B and D; OUT for DL11-E; does not affect DL11-A and C. Drawing DL-4.
- J5. When inserted, allows the BREAK bit to function. OUT for DL11-A and B; IN for DL11-C,D, and E. Drawing DL-4.
- J6. When inserted, allows DSET INT to cause interrupts. OUT for DL11-A,B,C and D; IN for DL11-E. Drawing DL-4.
- J7. When inserted, allows dataset control bits to be read as part of the receiver status register.

SIZE	CODE	NUMBER	REV
A	SP	DL11-0-2	D

DEC FORM NO. DEC 16-(381)-1022-N370
DRA 108

SHEET 2 OF 8

ENGINEERING SPECIFICATION

CONTINUATION SHEET

TITLE DL11 INSTALLATION PROCEDURE

J7. (con't)

OUT for DL11-A,B,C and D; IN for DL11-E.
Drawing DL-2.

J8. When inserted, allows error bits to be read
as part of the receiver data register. OUT
for DL11-A and B; IN for DL11-C,D and E.
Drawing DL-2.

Summary of mode control jumpers:

JUMPER	A	B	C	D	E	DRAWING
J1	*	IN	*	IN	IN	DL-7
J2	OUT	OUT	OUT	OUT	OUT	DL-7
J3	*	OUT	*	OUT	IN	DL-4
J4	*	IN	*	IN	OUT	DL-4
J5	OUT	OUT	IN	IN	IN	DL-4
J6	OUT	OUT	OUT	OUT	IN	DL-4
J7	OUT	OUT	OUT	OUT	IN	DL-2
J8	OUT	OUT	IN	IN	IN	DL-2

*= don't care

B. REGISTER ADDRESS ASSIGNMENTS:

The DL11 can respond to addresses with the following format:

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	1	1	1	JUMPERS										

Selects 1 of 4
Registers

Byte Control

Bits 10 through 3 are controlled by jumpers A10 to A3. A
jumper inserted indicates a zero.

For the DL11-A and B used as the console device, address
777560 is assigned. For additional units, assign 776XX0,
where XX=50 for the first additional unit and XX=67 for
the 16th unit.

For the DL11-C,D and E assign address 77XXX0, where XXX=561
for the first line, and XXX=617 for the 31st line. Assign
all C's first, then D's, and then E's.

SIZE	CODE	NUMBER	REV
A	SP	DL11-0-2	D

ENGINEERING SPECIFICATION

CONTINUATION SHEET

TITLE DL11 INSTALLATION PROCEDURE

C. VECTOR ADDRESS ASSIGNMENT:

Jumpers V8 through V3 control the interrupt vector. A
jumper inserted provides a vector bit of one. Vectors can
be produced in the form XX0 and XX4, where XX ranges from
00 to 77.

For the DL11-A and B used as a console device the vector
address is 060/064. For additional units, vectors are
floating.

For the DL11-C,D, and E vector addresses are floating.
Assign all C's first, then D's, then E's.

D. PRIORITY ASSIGNMENT:

Interrupt priority is established by inserting a "priority
plug" in the socket at IC location F19. For DL11-A,B,C,D
and E use level 4.

SUMMARY OF REGISTER, VECTOR AND PRIORITY ASSIGNMENTS:

	ADDRESS	VECTOR	PRIORITY
DL11-A,B CONSOLE	777560 777562 777564 777566	60/64	BR4
DL11-A,B ADDITIONAL UNITS	776XX0 776XX2 776XX4 776XX6	Floating	BR4

Where XX= 50 for line #1
and XX= 67 for line #16

	ADDRESS	VECTOR	PRIORITY
DL11-C,D,E	77XXX0 77XXX2 77XXX4 77XXX6	Floating	4

Where XXX= 561 for line #1
and XXX= 617 for line #31

SIZE	CODE	NUMBER	REV
A	SP	DL11-0-2	D

ENGINEERING SPECIFICATION

CONTINUATION SHEET

TITLE DL11 INSTALLATION PROCEDURE

E. SPECIAL NPR JUMPER:

Jumper N1, shown on drawing DL-6, controls the response of the interrupt circuit to an NPR request. The jumper should normally be IN, except for 11/20 and 11/15 systems without the KH11 option.

F. SELECTION OF DATA FORMAT:

1. Data Bits

Split lug pairs NB2 and NB1 control the number of data bits in the serial character as follows:

NB2	NB1	# OF DATA BITS
OUT	OUT	8
OUT	IN	7
IN	OUT	6
IN	IN	5

2. Parity

Parity is controlled by split lug pairs NP and EPS as follows:

NP	EPS	PARITY
OUT	OUT	OFF
OUT	IN	OFF
IN	OUT	EVEN
IN	IN	ODD

3. Stop Bits

Split lug pair 2SB and jumpers J9, J10 and J11 control the number of stop bits in the serial character as follows:

2SB	J9	J10	J11	# OF STOP BITS
OUT	OUT	IN	OUT	2
IN	OUT	IN	OUT	1
IN	OUT	OUT	IN	1.5 for TI, GI, and SCM UARTS
IN	IN	OUT	OUT	1.5 for WD UARTS

G. CRYSTAL SELECTION:

The clocking scheme of the DL11 consists of a single crystal oscillator feeding a divider network, with two 10-position switches tapping various points to feed into the UART's

SIZE	CODE	NUMBER	REV
A	SP	DL11-0-2	D

ENGINEERING SPECIFICATION

CONTINUATION SHEET

TITLE DL11 INSTALLATION PROCEDURE

G. Con't

transmitter and receiver sections. Thus, for a given crystal frequency, 8 baud rates are independently selectable for transmit and receive. The two addition switch positions select external clocks.

SPEED GROUP		1	2	3	4
		CRYSTAL (HZ)			
POSITION	FACTOR	844.8K	1.03296M	1.152M	4.608M
1*	23040	36.7	44.8	50	200
2	15360	55	67.3	75	300
3	7680	110	134.5	150	600
4	3840	220	269	300	1200
5	1920	440	538	600	2400
6	960	880	1076	1200	4800
7	640	1320	1614	1800	7200
8	480	1760	2152	2400	9600

*Most counter-clock wise position.

To determine a crystal frequency for a non-standard baud rate, pick the position of the closest baud rate in the 1.152MHz column, and then multiply the non-standard baud rate by the factor for that position. For example, if the customer specifies 1050 baud, this is closest to 1200 baud, position 6.

$$1050 \times 960 = 10080000 = 1.008\text{MHz.}$$

The crystal frequency should not fall outside the range of the standard crystals.

DEC part numbers for the standard crystals are as follows:

844.8 KHz	18-10245-1*
1.03296 MHz	18-05501-6
1.152 MHz	18-05501-5
4.608 MHz	18-05501-7

*Use A or C cut crystals only. Do not use crystals marked NE-6D.

When ordering a special crystal, refer to purchase specification 18-05501 for crystal specification.

Insure that transparent vinyl tape (9008269) is applied to the top surfaces of the crystal and mounting brackets to insulate from adjacent modules.

SIZE	CODE	NUMBER	REV
A	SP	DL11-0-2	D

ENGINEERING SPECIFICATION

CONTINUATION SHEET

TITLE DL11 INSTALLATION PROCEDURE

H. G8000 INSTALLATION:

For DL11-B, D, and E a positive voltage is required between 9 and 15 volts to operate the EIA drivers. For PDP-11/20 and PDP-11/15 systems with the H720 power supply, a G8000 module must be installed to provide this voltage. Using a filter network, this module converts the full-wave rectified "+8V" signal to a positive DC voltage.

1. Install G8000 into slot A02 of DD11-A.
2. Wire A03V2 to A02V2.
3. Wire A02N2 to CXXU1 where XX is the slot location of the M7800.

Refer to diagram 1.

I. FILTER CAPACITOR SELECTION:

For DL11-A's and DL11-C's, which operate with 20ma current loops, capacitors are used to filter the receive line and slow the switching time of the transmit line. To avoid excessive distortion above 150 baud, the capacitance in each of these two circuits must be reduced. This is accomplished by clipping C29 (.47 mfd) and C31 (1000 pf), both shown on drawing DL-3.

- J. DL11-B,D,E in Systems with +15V available using DD11-A
There is a special situation of using a DD11-A to mount a DL11-B, D, or E in systems with +15V available. These systems have +15V available and it appears at pin A03V2 of the DD11-A when using power harness such as 7009177, 7008855, or 7008909. In this situation, no G8000 is necessary, and +15V can be wired directly from A03V2 to CXXU1, where XX is the slot number of the DL11.
NOTE: this does not apply to DL11-A or C or DD11-B.

- K. When using the DL11-B,D,E in an 11/05 processor pin CXXU1 has +15V available on it so no G8000 or no jumpers are required.

SIZE	CODE	NUMBER	REV
A	SP	DL11-0-2	D

ENGINEERING SPECIFICATION

CONTINUATION SHEET

TITLE DL11 INSTALLATION PROCEDURE

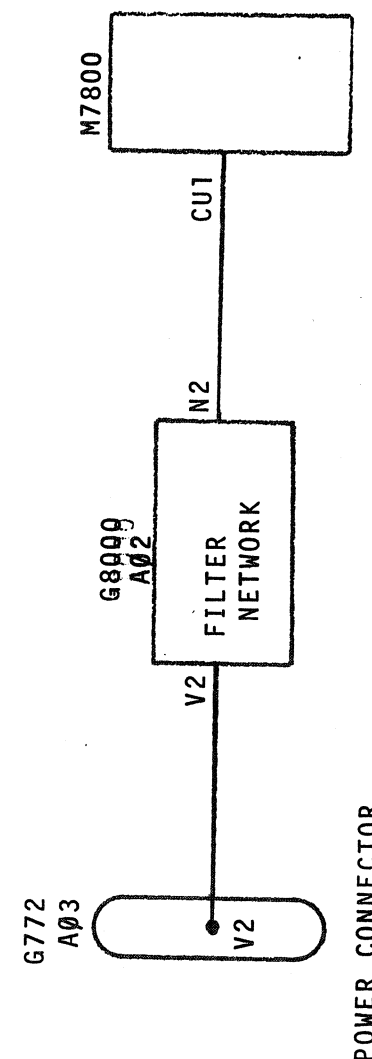


DIAGRAM 1. G8000 INSTALLATION

SIZE	CODE	NUMBER	REV
A	SP	DL11-0-2	D