

FIELD MAINTENANCE PRINT SET

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M9312
M9312-YA

Digital Equipment Corporation

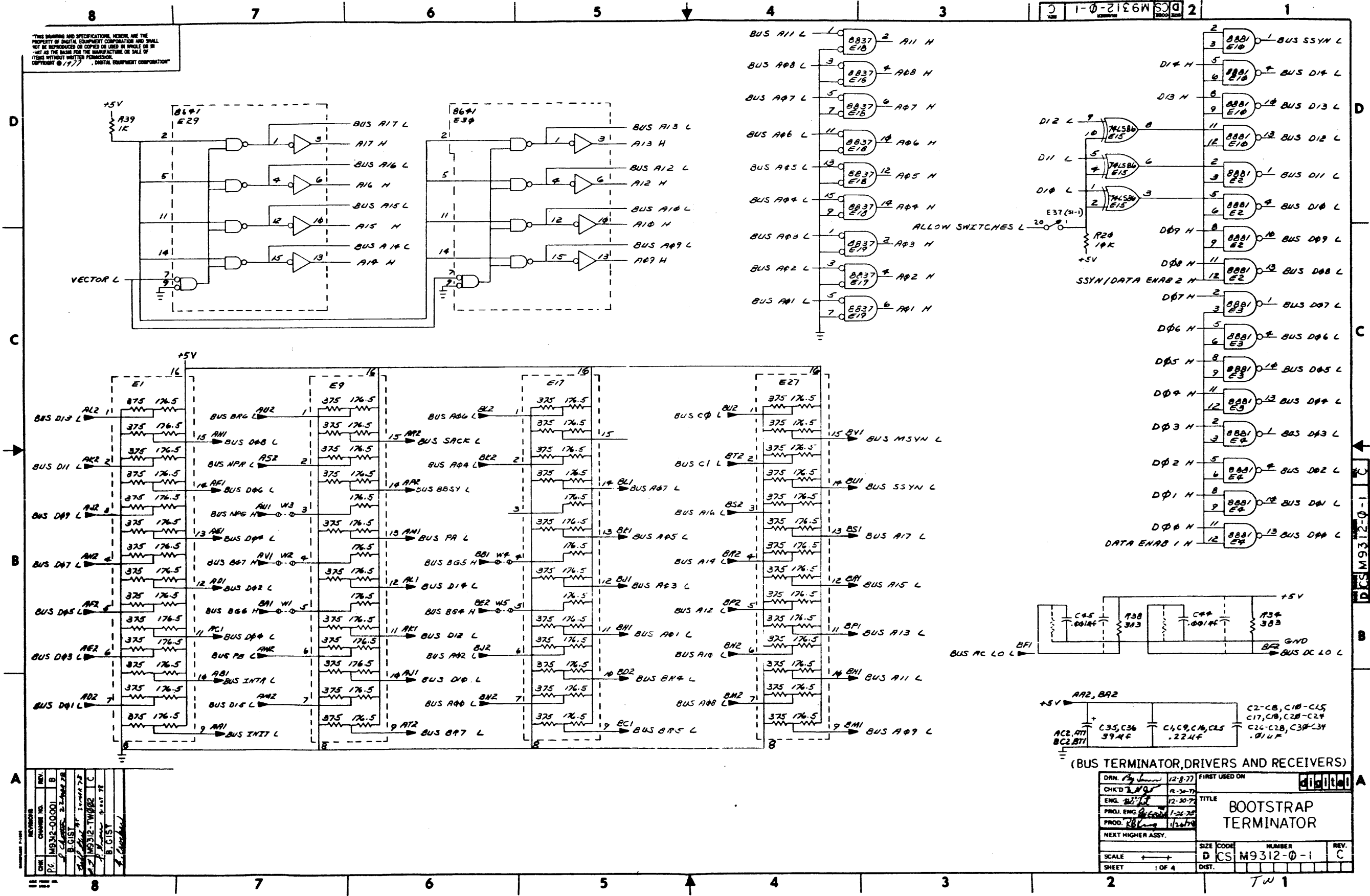
digital

SIZE B	CODE TC	NUMBER M9312-Ø-2					REV. A
DIST.							

REVISIONS

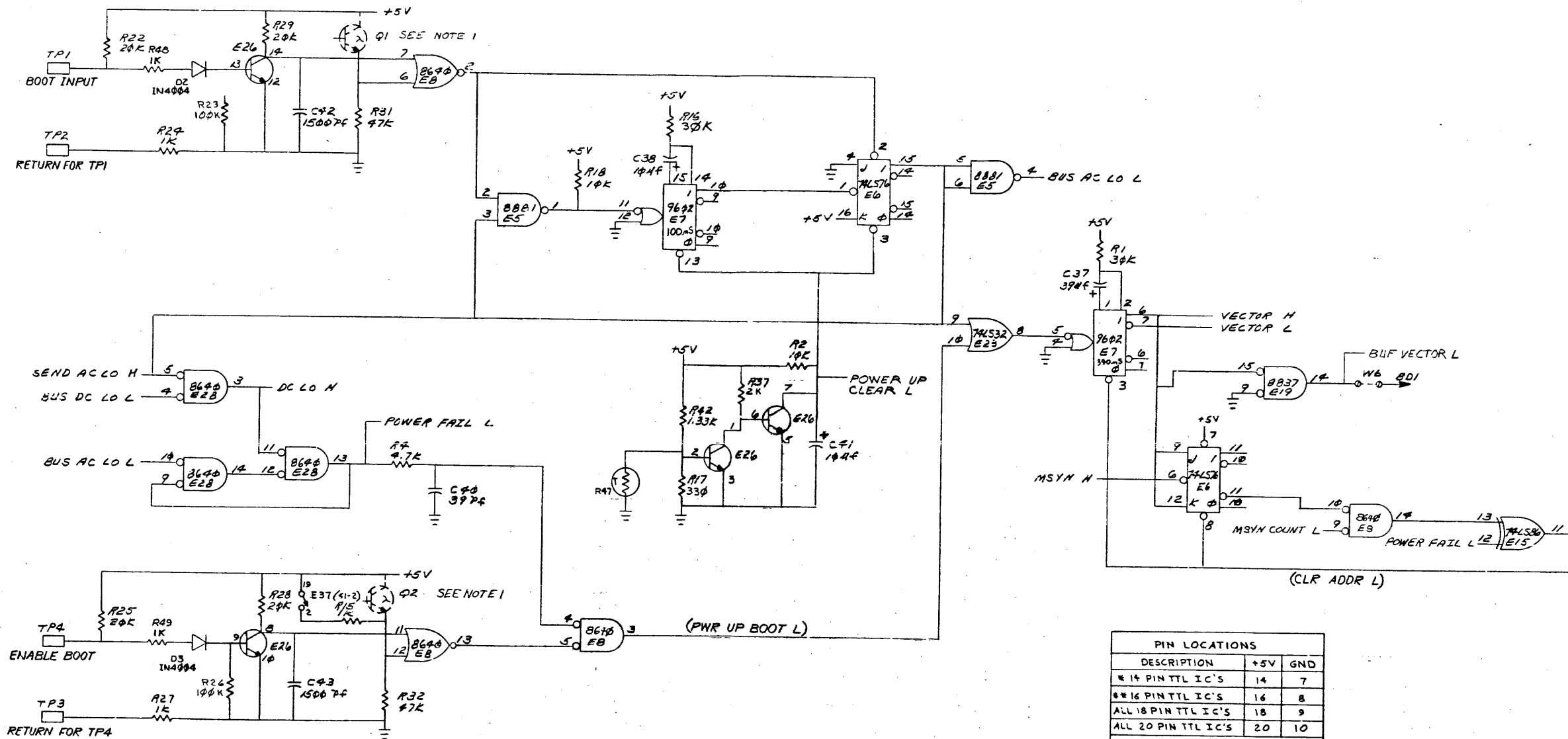
DRB 124

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DRA. <i>[Signature]</i> 12-8-77		FIRST USED ON	
CHK'D <i>[Signature]</i> 12-30-77	TITLE		
ENG. <i>[Signature]</i> 12-30-77	BOOTSTRAP TERMINATOR		
PROJ. ENG. <i>[Signature]</i> 1-26-78	REV. C		
PROD. <i>[Signature]</i> 1-26-78	NEXT HIGHER ASSY.		
SCALE	SIZE	CODE	NUMBER
SHEET 1 OF 4	D	CS	M9312-0-1
DIST.		REV. C	

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NOTES: 1. PHOTO TRANSISTORS Q1 AND Q2
DO NOT APPEAR ON THE PARTS LIST.
THEY ARE INTENDED FOR FUTURE
APPLICATIONS.

PIN LOCATIONS		
DESCRIPTION	+5V	GND
* 14 PIN TTL IC'S	14	7
* 16 PIN TTL IC'S	16	8
ALL 18 PIN TTL IC'S	18	9
ALL 20 PIN TTL IC'S	20	10
EXCEPTIONS		
* E8, E28 (DEC 8640)	8	1
* E6 (74LS76)	5	13

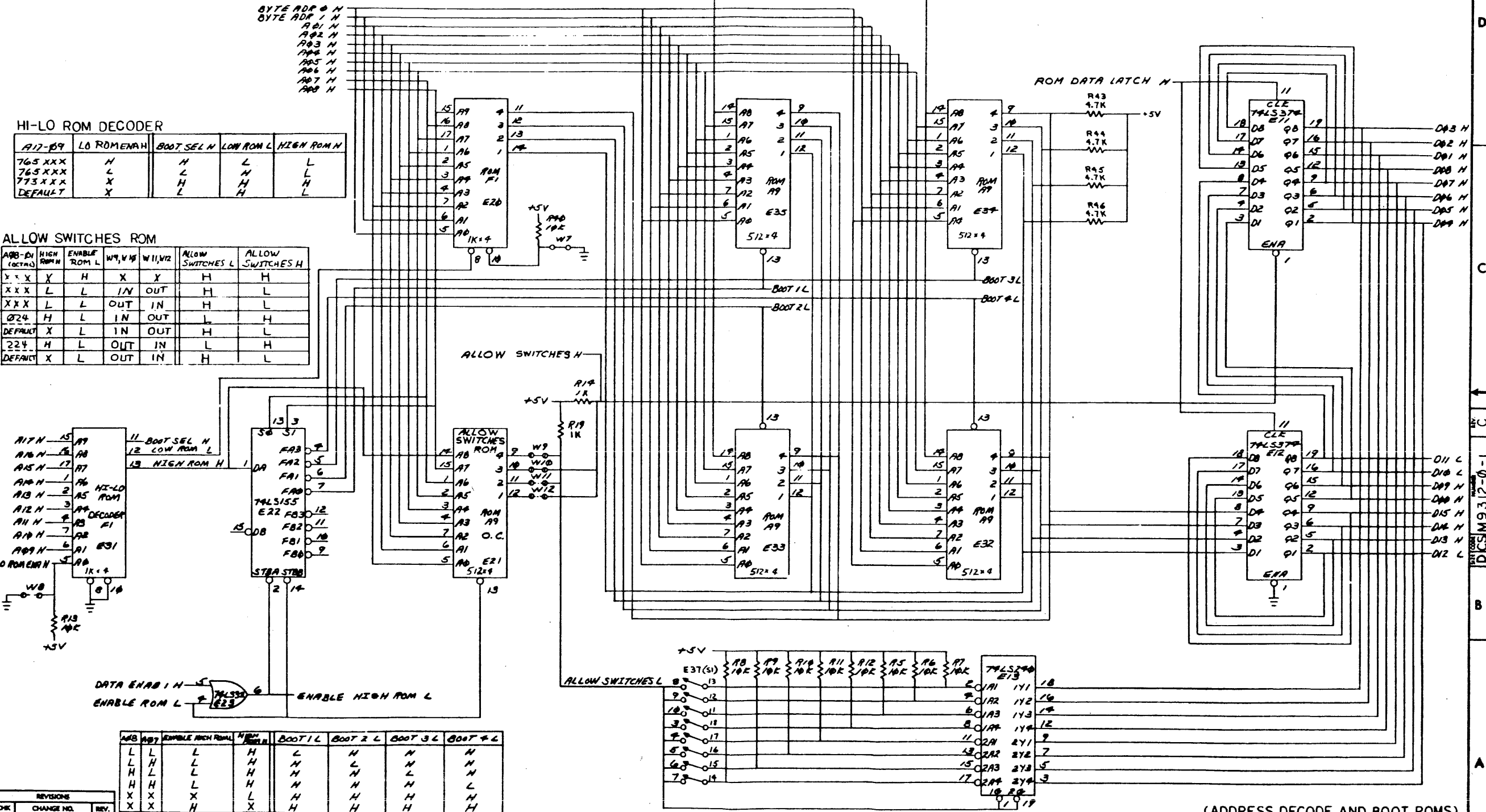
REVISIONS		
CHK	CHANGE NO.	REV.

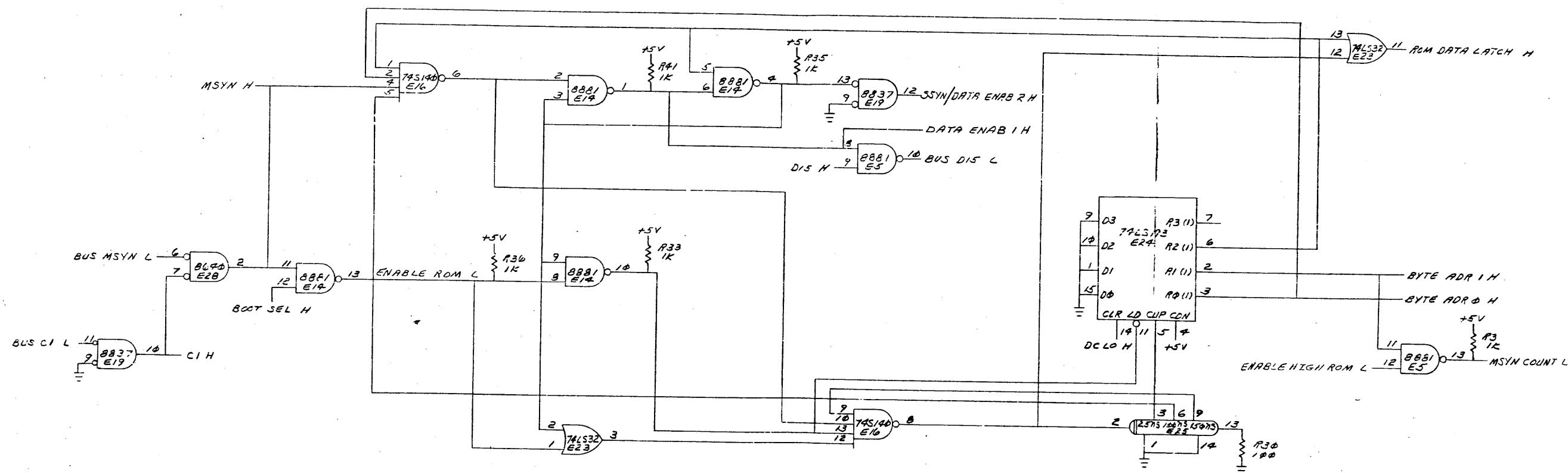
(SWITCH FILTERS AND AC LO GENERATION)

TITLE	SIZE CODE	NUMBER	REV.
BOOTSTRAP TERMINATOR	D CS	M9312-0-1	C
SCALE	SHEET	DIST.	
	2 OF 4		

TW 1

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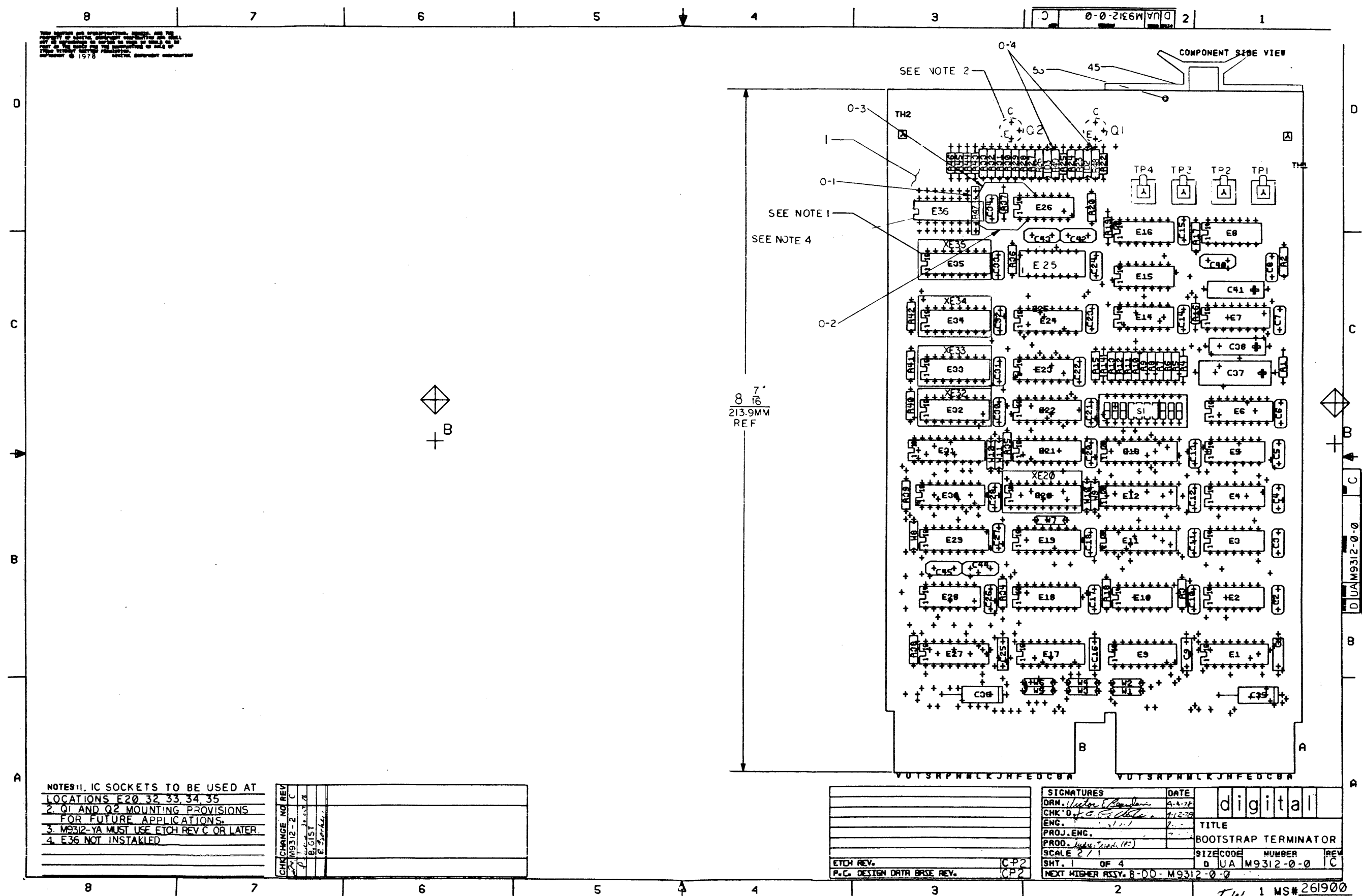




REVISIONS		
CHK	CHANGE NO.	REV.

(TIMING AND CONTROL)

TITLE		SIZE	CODE	NUMBER	REV.
BOOTSTRAP TERMINATOR		D	CS	M9312-0-1	C
SCALE	SHEET	4 OF 4			
	DIST.				

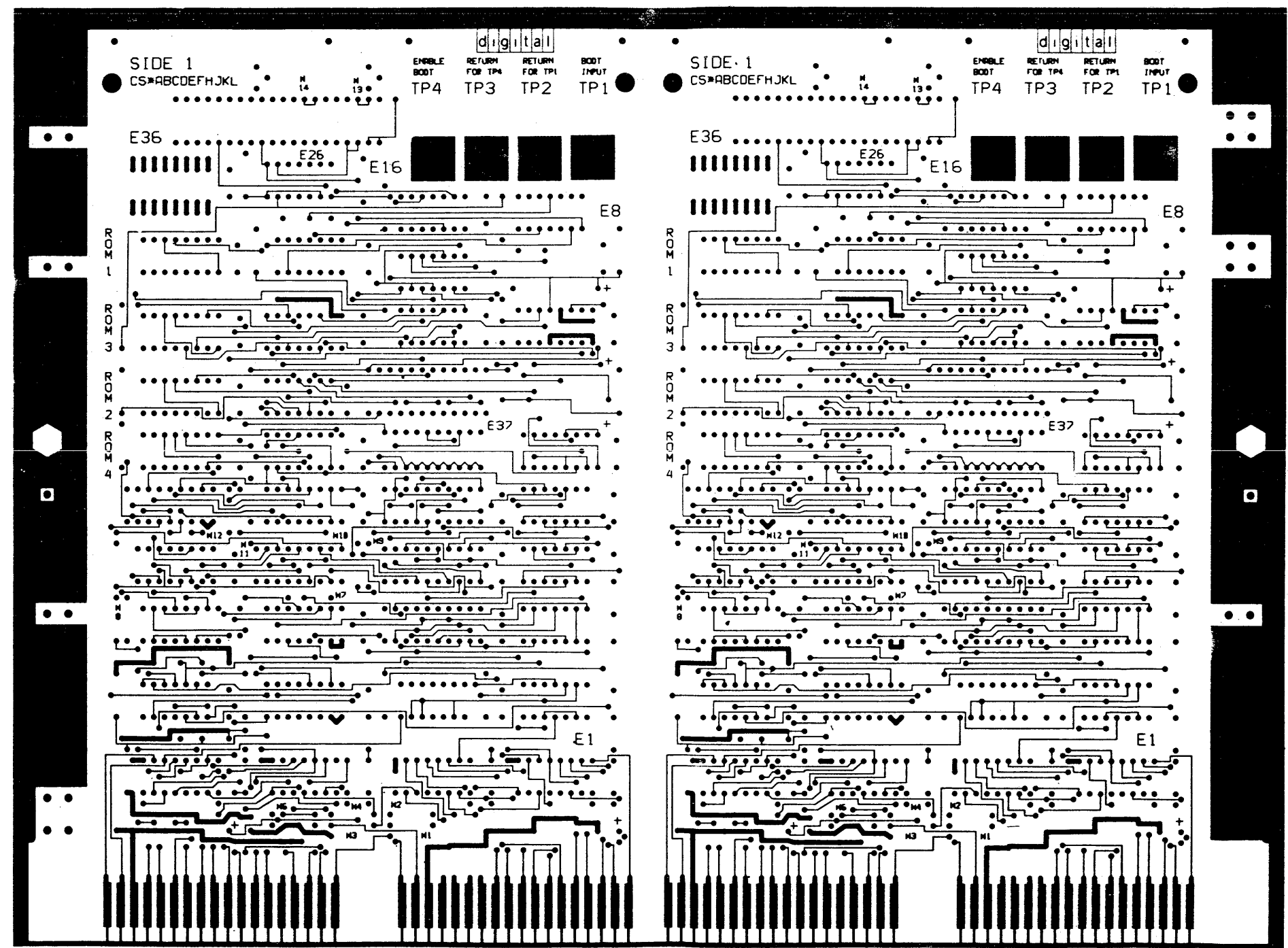


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M9312 5013263 C-P2 L1

M9312 5013263 C-P2 L1

LAYER 1



REVISIONS		
CHK	CHANGE NO.	REV.

TITLE		SIZE CODE	NUMBER	REV.
BOOTSTRAP TERMINATOR		D UA	M9312-0-0	C
SCALE	++	SHEET	2 OF 4	DIST.

REV. C
NUMBER M9312-0-0
DATE CODE D UA

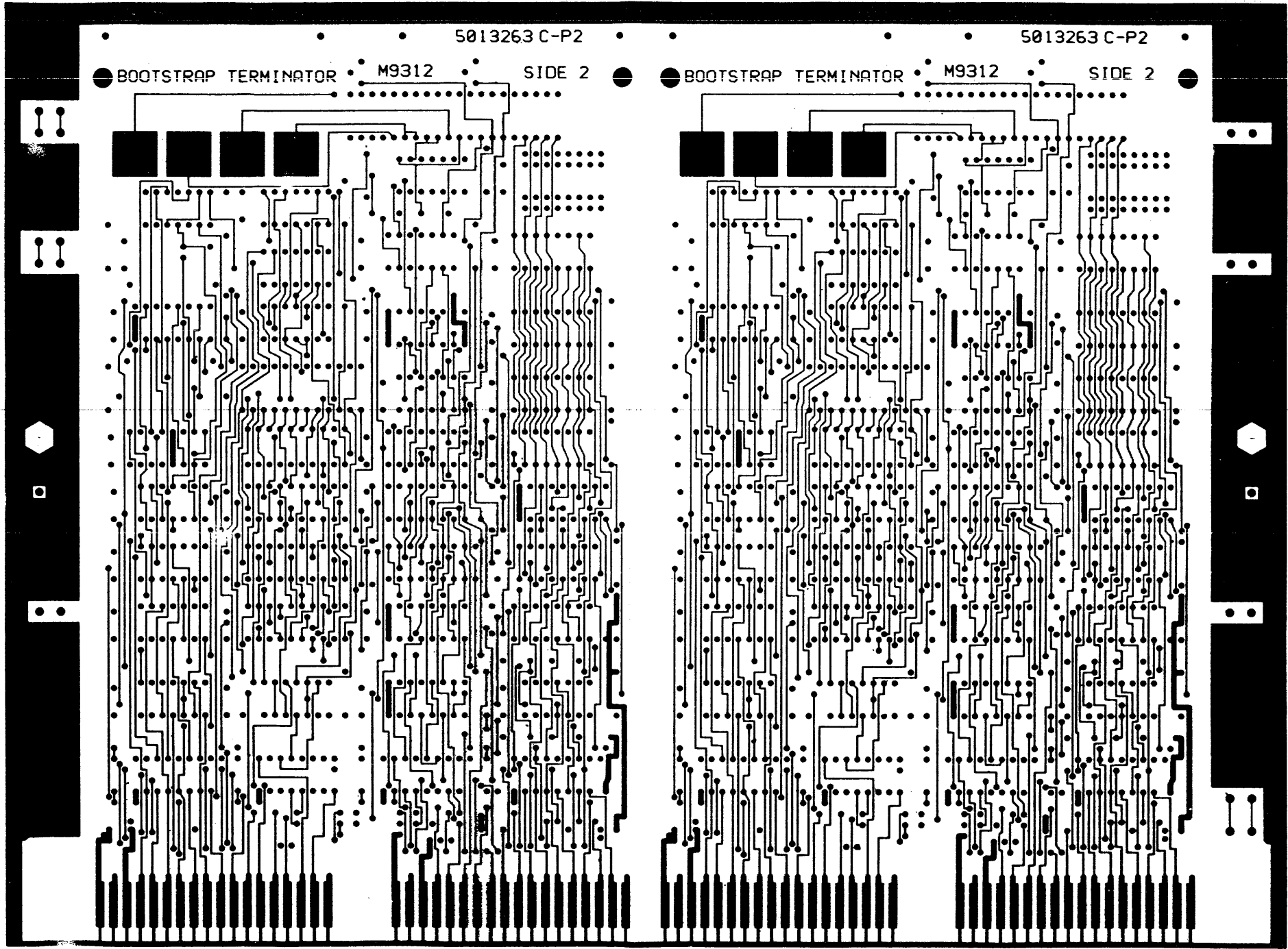
8 7 6 5 4 3 2 1

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L4

83411J

L4



REVISIONS		
CHK	CHANGE NO.	REV.

TITLE		SIZE CODE	NUMBER	REV.
BOOTSTRAP TERMINATOR		D UA	M9312-0-0	C
SCALE		SHEET	3 OF 4	DIST.

8 7 6 5 4 3 2 1 TW1

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REWORK INSTRUCTIONS
ECO #2
COMPONENT ADDS SIDE 1:
0-1 THERMISTOR R47 PIN (1316312) BETWEEN
PINS E36-R & E36-S
WIRE ADDS SIDE 1:
0-2 FROM E36-R TO E26-2
0-3 FROM E36-S TO E26-12
OTHER DELETES SIDE 1:
0-4 REMOVE FROM THE P.C. BOARD
THE WORDS W13 & W14

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE BOOTSTRAP TERMINATOR		SIZE CODE D UA	NUMBER M9312-0-0	REV. C
SCALE	SHEET 4 OF 4	DIST.	TW 1	

LINE	ITEM	DOCUMENT NO.	PART NO.	DESCRIPTION	QTY	REFERENCE DESIGNATORS
1	1		1000010-00	39.0 MMF 100V 5%200PPM DM15S	(10-00 1	C40
2	2		1000043-00	1000.0 MMF 250V 20% Y5F DISC	2	C44,C45
3	3		1000054-00	1500.0 MMF 250V 10% Z5P DISC	2	C42,C43
4	4		1000076-00	39 MFD 10V 10% 150D S.TA	(10-00 2	C35,C36
5	5		1001610-01	.01 MFD 100V OR 50V Z5U DISC/800PF MIN	28	C2-C8,C10-C15,C17,C18,C20-C24,
					CONT	C26-C28,C30-C34
6	6		1004813-00	10 MFD 20V 10% 150D S.TA	(10-00 2	C38,C41
7	7		1005335-00	39 MFD 20V 10% 150D S.TA	(10-00 1	C37
8	8		1010274-01	.22 MFD 50V X% 3C023 CER.	4	C1,C9,C16,C25
9	9		1100113-00	D 662 OS 600PCB(STABISTOR)	2	D2,D3
10	10		1211164-06	SW,DIP 1P 1A 10POS	1	S1
11	11		1215006-02	SOCKET 16PIN IC LOW PROFILE	4	E32-E35
12	12		1215006-03	SOCKET 18PIN IC LOW PROFILE	1	E20
13	13		1300229-00	100 1/4W 5% CC	(13-00 1	R30
14	14		1300365-00	1 K 1/4W 5% CC	(13-00 11	R3,R15,R23,R24,R26,R27,R33,
					CONT	R35,R36,R39,R41
15	15		1300447-00	4.7 K 1/4W 5% CC	(13-00 1	R4
16	16		1300479-00	10 K 1/4W 5% CC	(13-00 15	R5-R14,R18-R20,R40,R2
17	17		1302177-00	47 K 1/4W 5% CC	(13-00 2	R31,R32
18	18		1302391-00	20 K 1/4W 5% CC	(13-00 5	R22,R25,R28,R29,R37
19	19		1302394-00	30 K 1/4W 5% CC	(13-00 2	R1,R16
20	20		1302873-00	261 1/4W 1% RN55D-F 100PPM	(13-00 1	R17
21	21		1305125-00	383 1/4W 1% RN55D-F 100PPM	(13-00 2	R34,R38
22	22		1310630-00	1.33 K 1/4W 1% RN55D-F 100PPM	(13-00 1	R42
23	23		1312628-00	R NETWORK 14-176.5 14-375	2	E1,E27
24	24		1312628-01	R NETWORK 14-176.5 11-375	2	E9,E17
25	25		1513265-00	3725 QUAD CORE DRIVER	1	E26
26	26		1611243-00	DELAY=25-250NS,10TAPS RCL#L-183 E PE#9829	1	E25
27	27		1909705-00	DEC 8881-INAND GATE-QUAD 2IN,OPN COLL.	6	E2,E3,E4,E5,E10,E14
28	28		1910546-00	74S140 NAND GATE-DUAL 4INPUT,BUFFER	1	E16

REVISION HISTORY			VARIATIONS FOR THIS ASSY.		DIGITAL EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS	
CHK	ECO NO	REV		FIRST USED ON: M9312-00		
---	INIT	A	00	MADE BY: D SIREEN	DATE: 02-DEC-77	TITLE
PG	00001	B		CHECKED: F SMART	DATE: 02-DEC-77	PARTS LIST
				DSN.ENG.: BILL GIST	DATE: 29-DEC-77	BOOTSTRAP TERMINATOR
				PROD.: BOB KING	DATE: 30-DEC-77	SIZE CODE: DOCUMENT NUMBER
				RESP.ENG.: RAY GRUDA	DATE: 29-DEC-77	K PL M9312-0-0
						REV
						EDIT#
						8

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LINE	ITEM	DOCUMENT NO.	PART NO.	DESCRIPTION	QTY	REFERENCE DESIGNATORS
29	29		1910951-00	9602 ONE SHOT-DUAL	1	E7
30	30		1911116-00	DEC 8837 RECEIVER,BUS,HEX,UNIBUS	2	E18,E19
31	31		1911469-00	DEC 8640 RECEIVER,BUS,QUAD,UNIBUS,Q-BU	2	E8,E28
32	32		1911579-00	8641 TRANSCEIVER,BUS,QUAD,UNIBUS	2	E29,E30
33	33		1912816-00	LS32 OR GATE-QUAD 2IN,POSITIVE	1	E23
34	34		1912825-00	LS76 FF-JK DUAL W/PRESET & CLEAR	1	E6
35	35		1912829-00	LS86 X-OR GATE-QUAD 2IN	1	E15
36	36		1912846-00	LS155 DECODER,2 OF 4(DUAL) & DEMUX	1	E22
37	37		1912854-00	LS193 COUNTER,SYNCHR,4BIT,UP/DN,BINA	1	E24
38	38		1913777-00	LS240 DRIVER,LINE,OCTAL,TRI-ST	1	E13
39	39		1914214-00	LS374 FF-D OCTAL EDGE TRIGGER	2	E11,E12
40	40		23217F1-00	F1-01	1	E31
41	41		23690A9-00	A9-04	1	E21
42	42	D-MD-5013263-0-0	5013263-00	ETCH BOARD FOR M9312	1	
43	43		9006732-00	EYELET, ROLLED FLANGE, .121 OD X .219 LG	2	
44	44		9007112-00	TERM QUICK 1POS ADAPTER	4	TP1,TP2,TP3,TP4
45	45		9008337-06	HANDLE, FLIP CHIP, MAGENTA	1	
46	46		9009000-00	EYELET, ROLLED FLANGE, .121 OD X .156 LG	4	
47	47		9009157-00	ADHESIVE, PERMABOND #101	A/R	
48	48		9009185-00	JUMPER, WIRE, INSULATED, BLACK BAND	3	W7,W9,W10
49	49		9105740-55	WIRE(WRAP)30AWG UL1423 (91-00 A/R		

50 NOTE: I C SPARE LOCATIONS INCLUDE E36

DIGITAL EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS	TITLE PARTS LIST BOOTSTRAP TERMINATOR	SIZE K	CODE PL	DOCUMENT NUMBER M9312-0-0	REV B
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REVISION HISTORY			VARIATIONS FOR THIS ASSY.		FIRST USED ON: M9312		DIGITAL EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS		
CHK	ECO NO	REV					TITLE		
				MADE BY: B CRAMM	DATE: 1 AUG 78		SETUP AND INSTALLATION PROCEDURE		
				CHECKED: N POLLITT	DATE: 17 AUG 78				
				DSN.ENG.: B GIST	DATE: 1 AUG 78				
				PROD.: D PETERSON	DATE: 17 AUG 78		SIZE: K	CODE: SP	DOCUMENT NUMBER: M9312-0-4
				RESP.ENG.: E CROCKER	DATE: 1 AUG 78		ASSY. #:		REV: D
									EDIT NO: 8

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SCOPE

THIS DOCUMENT OUTLINES THE FOLLOWING:

SECTION 1. JUMPER W1-W12 CONFIGURATION-----	PAGE 4
SECTION 2. ROM INSTALLATION (BOOT ROMS, AND DIAGNOSTIC ROMS)---	PAGE 7
SECTION 3. CONNECTING FAST-ON TABS TP1-TP4,-----	PAGE 9
SECTION 4. ROM CROSS-REFERENCE TABLE-----	PAGE 11
SECTION 5. ROM IDENTIFICATION TABLE-----	PAGE 15
SECTION 6. S1 SWITCH SETTING FOR CPU DIAGNOSTIC ROM-----	PAGE 17
SECTION 7. S1 SWITCH SETTING FOR PERIPHERAL BOOT ROMS-----	PAGE 21
SECTION 8. S1 SWITCH SETTING FOR COMMUNICATION BOOT ROMS-----	PAGE 35

TW

USEAGE

THE M9312 IS CURRENTLY USED 4 WAYS

1. MUD MACHINE BEGINNING OF BUS TERMINATOR 11/04/24/34/34A
2. 11/70 BEGINNING OF BUS TERMINATOR
3. 11/60 BEGINNING OF BUS TERMINATOR
4. OTHER UNIBUS PDP 11'S BEGINNING OR END OF BUS TERMINATOR
(IF A UNIBUS REPEATER IS USED IN THE SYSTEM, THE M9312
MUST BE ON THE PROCESSOR SIDE OF THE REPEATER.)

TW

SECTION 1.

JUMPER W1-W12 CONFIGURATION

TW

THE NORMAL JUMPER SETUP IS SHOWN BELOW

USEAGE	W1	W2	W3	W4	W5	W6	W7	W8	W9	W10	W11	W12
11/04/34/34A (MUD MACHINE) M9312 IN SLOT AB2,3,4 OF PROCESSOR BACKPLANE	OUT	OUT	OUT	OUT	OUT	OUT	IN	OUT	IN	IN	OUT	OUT
11/70 WITH M9312 IN SLOT EF1 OF PROCESSOR BACKPLANE (SEE NOTES 1,2,3)	IN	IN	IN	IN	IN	IN	IN	OUT	IN	IN	OUT	OUT
11/60 WITH M9312 IN THE LAST AB SLOT OF THE LAST MEMORY BACKPLANE(SEE NOTE 2,3)	OUT	OUT	OUT	OUT	OUT	OUT	IN	OUT	OUT	OUT	IN	IN
OTHER UNIBUS CPU'S WITH M9312 IN PLACE OF M930 (OR EQUIVALENT)	IN	IN	IN	IN	IN	OUT	IN	IN	IN	IN	OUT	OUT
11/24 (MUD MACHINE) M9312 IN SLOT AB 9 OF PROCESSOR BACKPLANE	IN	IN	IN	IN	IN	OUT	IN	OUT	IN	IN	OUT	OUT

NOTES :

1 FOR BOOT ON POWER UP THE 11/70 REQUIRES THE FOLLOWING.

1.1. 7010329 BACKPLANE ECO 8 (WIRE LIST REV J OR LATER)

1.2. M8130 ECO'S 1,2 AND 3 (CS REV C OR LATER)

M8130 JUMPERS SET AS FOLLOWS: W1-IN,W2-OUT,W3-IN,W4-OUT,W5-OUT,W6-OUT,W7-OUT,W8-IN,W9-OUT

1.3. M8136 ECO 5 (CS REVS C1 OR E OR LATER)

1.4. M9312 ECO 1 (CS REV B OR LATER)

2. TO BOOT ON POWER UP FROM THE MK11 MEMORY THE CABLE SHOULD BE CONNECTED TO TABS 3 AND 4 ALSO THE SWITCH S1-2 HAS TO BE OFF

3. IF A REMOTE INITIALIZER PANEL IS USED THE CABLES FROM THE PANEL TO THE M9312 CAN NOT HAVE ANY RESISTORS OR CAPS ON IT

TW

EXPLANATION OF JUMPER FUNCTIONS

JUMPER	FUNCTION PERFORMED
W1	PULL UP FOR BUS BG6 H (WHEN IN)
W2	PULL UP FOR BUS BG7 H (WHEN IN)
W3	PULL UP FOR BUS NPG H (WHEN IN)
W4	PULL UP FOR BUS BG5 H (WHEN IN)
W5	PULL UP FOR BUS BG4 H (WHEN IN)
W6	BUF VECTOR L (IN FOR 11/70)
W7	RESERVED (ALWAYS IN)
W8	LO ROM ENABLE (WHEN OUT)
W9,W10	POWER UP BOOT TO 773024 (IN FOR ALL CPU'S EXCEPT 11/60)
W11,W12	POWER UP BOOT TO 773224 (IN FOR 11/60 ONLY)

TW

SECTION 2.

ROM INSTALLATION (BOOT ROM, AND DIAGNOSTIC ROMS)

TW

ROM INSTALLATION

THERE ARE 5 SOCKETED LOCATIONS ON THE M9312. THESE ARE E20, E32, E33, E34, AND E35 (M9312 ETCH REV B AND C). THESE LOCATIONS EACH ACCEPT A ROM. ROMS USED WITH THE M9312 ARE SEPARATED INTO TWO CLASSIFICATIONS.

1. DIAGNOSTIC ROM (CPU SPECIFIC)

THIS ROM ALWAYS PLUGS INTO LOCATION "E20".
IT IS ONLY POSSIBLE TO INSTALL ONE OF THESE PER M9312.
THIS ROM CAN BE IDENTIFIED BY THE LAST 2 CHARACTERS OF THE PATTERN NUMBER THAT IS STAMPED ON THE ROM. THEY WILL ALWAYS BE "F1".

2. BOOTSTRAP ROMS

THESE ROMS ARE USED TO BOOT VARIOUS MEDIAS.
FOR M9312 ETCH REV B AND C, THEY ARE PLUGGED IN TO LOCATIONS E32, E33, E34, AND E35.
FROM THIS POINT ON IN THIS DOCUMENT E32, E33, E34, AND E35 WILL BE REFERRED TO AS ROM 4, ROM 2, ROM 3 AND ROM 1 RESPECTIVELY.
IT IS NOT REQUIRED THAT A PARTICULAR DEVICE BOOT GO INTO A PARTICULAR SOCKET BUT THE ORDER IN WHICH THE BOOT ROM SOCKETS ARE FILLED IS EXTREMELY IMPORTANT, AND FOR CONFIGURATION CONSISTENCY ROMS WILL BE INSTALLED IN ALPHABETIC ORDER BY THEIR FIRST TWO LETTER MNEMONIC. (SEE PAGE 12 AND 14) A TABLE IS PROVIDED BELOW WHICH OUTLINES THE ORDER IN WHICH THE ROMS SHOULD BE INSERTED.
NOTE THAT BOOT ROMS CAN BE DISTINGUISHED FROM DIAGNOSTIC ROMS BY THE LAST 2 CHARACTERS OF THE PATTERN NUMBER PRINTED ON THE ROM. THE BOOT ROMS ALWAYS END WITH "A9".

TABLE FOR ROM INSTALLATION ORDER		
ORDER OF		
INSTALLATION	LOC.	(IC NUMBER)
FIRST *	ROM 1	(E35)
SECOND	ROM 2	(E33)
THIRD	ROM 3	(E34)
FOURTH	ROM 4	(E32)

* ON 11/60, IF THERE IS ONLY ONE ROM, IT MUST BE INSTALLED IN ROM 2 SOCKET TO DO A POWER-UP BOOT.

TW

SECTION 3

FAST-ON TAB CONNECTION

TW

THE FAST-ON TABS ARE DEFINED IN THE TABLE BELOW.

FAST-ON	FUNCTION PERFORMED
TP1	BOOT INPUT
TP2	RETURN FOR BOOT INPUT
TP3	RETURN FOR ENABLE BOOT ON POWER UP
TP4	ENABLE BOOT ON POWER UP

IT WOULD BE IMPOSSIBLE TO LIST ALL THE DIFFERENT WAYS TO CONNECT THESE POINTS. FOR A SPECIFIC APPLICATION OF THE MODULE, SYSTEM DOCUMENTATION MUST BE CONSULTED.

ONE OF THE FREQUENT APPLICATIONS OF THE M9312 IS TO REPLACE THE M9301. A TABLE IS PROVIDED BELOW THAT OUTLINING HOW THIS SUBSTITUTION CAN BE MADE WITH RESPECT TO THE FAST-ON CONNECTIONS.

WIRE CONNECTION				
FROM		TO		
MODULE	FAST-ON	MODULE	FAST-ON	COLOR
M9301	TP1	M9312	TP4	BLK
M9301	TP2	M9312	TP1	RED
M9301	TP3	M9312	TP3	CLEAR

NOTES:

1. IF A REMOTE INITIALIZER PANEL IS USED THE CABLE FROM THE PANEL TO THE M9312 CAN NOT HAVE ANY RESISTORS OR CAPS ON IT
2. TO BOOT ON POWER UP FROM THE MK11 MEMORY THE CABLE SHOULD BE CONNECTED TO TABS 3 AND 4 ALSO THE SWITCH S1-2 HAS TO BE OFF

TW

SECTION 4

ROM CROSS-REFERENCE TABLES

TW

ROM CROSS-REFERENCE TABLES

CROSS REFERENCE ROM P/N TO ROM TABLE NUMBER			
PART NUMBER	FUNCTION PERFORMED BY CPU ROM	ROM ID	SEE TABLE
23-			
616F1	DIAGNOSTIC FOR 11/60/70	ROM ID=B0	1-1
248F1	ASCII CONSOLE AND DIAGNOSTIC FOR 11/04/05/34/35/40/45/50/55	ROM ID=A0	1-2
446F1	DIAGNOSTIC FOR 11/44	ROM ID=C0	N/A
774F1	DIAGNOSTIC FOR 11/24	ROM ID=D0	1-3

NOTE::REFER TO 11/44 DOCUMENTATION

TW

ROM CROSS-REFERENCE TABLES

CROSS REFERENCE ROM P/N TO ROM TABLE NUMBER					
PART NUMBER	THE FOLLOWING ROMS ARE BOOTSTRAP ROMS				SEE TABLE
23-	BOOTABLE DEVICES				
	MNEMON-IC	FIRST DEVICE IN ROM	MNEMON-IC	SECOND DEVICE IN ROM	
751A9	DL	RL01	NA	NA	2-1
752A9	DM	RK06/07	NA	NA	2-2
753A9	DX	RX01	NA	NA	2-3
811A9	DY	RX02	NA	NA	2-11
755A9	DP	RP02/03	DS	RP04/5/6 RM02/3	2-4
756A9	DK	RK03/05	DT	TU55/56	2-5
757A9	MM	TU16/45/77/E16	NA	NA	2-6
758A9	MT	TU10/E10,TS03	NA	NA	2-7
759A9	DS	RS03/04	NA	NA	2-8
760A9	PR	PC05	TT	LO SPD RDR	2-9
761A9	CT	TU60	NA	NA	2-10
764A9	MS	TS04	NA	NA	2-12
765A9	DD	TU58	NA	NA	2-13
862A9	XM	DMC-11	NA	NA	3-1
863A9					
864A9					

CROSS REFERENCE DEVICE TO CONTROLER	
DEVICE	CONTROLER
RL01	RL11
RK06/07	RK611
RX01	RX11
RX02	RX211
RK06/07	RK611
RK06/07	RK611
RX02	RX211
RP02/03	RP11C/E
RP04/05/06 RM02/03	RH11/70
RK03/05	RK11C/D
TU55/56	TC11
TU16/U45/U77/E16	RH11/70
TU10/E10,TS03	TM11/A11/B11
RS03/04	RH11/70
PC05 (HI SPD RDR)	PC11/R11
LO SPD RDR (ASR33)	DL11A/W
TU60	TA11
TS04	TS11
TU58	DL11-W
COMM	DMC-11
COMM	DU11
COMM	DUP-11
COMM	DL11

TW

ROM CROSS-REFERENCE TABLES

[illegible][illegible]

TW

SECTION 5

ROM IDENTIFICATION TABLE

TW

ROM IDENTIFICATION TABLE

SOMETIMES, WHEN THE ROM CONFIGURATION OF AN M9312 IN A SYSTEM IS NOT KNOWN, IT IS DESIRABLE TO OBTAIN THE CONFIGURATION WITHOUT PULLING OUT THE MODULE. THIS CAN BE ACCOMPLISHED BY RUNNING DIAGNOSTIC C2M9B, OR EXAMINATING DATA IN 5 LOCATIONS AND REFERRING TO THE LIST BELOW.

THE LOCATIONS ARE AS FOLLOWS:

- 1. 765774 DIAGNOSTIC ROM
- 2. 773000 ROM 1
- 3. 773200 ROM 2
- 4. 773400 ROM 3
- 5. 773600 ROM 4

BY COMPARING THE DATA OBSERVED AT THE ABOVE LOCATIONS TO THE TABLE BELOW, YOU CAN IDENTIFY THE TYPE AND LOCATION OF EACH ROM.

OCTAL DATA	MNE- MONIC	P/N 23-	SEE TABLE
040460	A0	248F1	1-2
041060	B0	616F1	1-1
041524	CT	761A9	2-10
042113	DK	756A9	2-5
042114	DL	751A9	2-1
042115	DM	752A9	2-2
042120	DP	755A9	2-4
042123	DS	759A9	2-8
042130	DX	753A9	2-3
042131	DY	811A9	2-11
046515	MM	757A9	2-6
046524	MT	758A9	2-7
050122	PR	760A9	2-9
046523	MS	764A9	2-12
042104	DD	765A9	2-13
17776	*****	*****	*****
XXX77	*****	*****	*****

OCTAL DATA	MNE- MONIC	P/N 23-	SEE TABLE
074115	XM	862A9	3-1
17776		863A9	
17776		864A9	
074167	XW	865A9	3-3
17776		866A9	
17776		867A9	
074167	XU	868A9	3-2
17776		869A9	
17776		870A9	
054114	XL	926A9	3-4
17776		927A9	
17776		928A9	
041524	CT	766A9	2-10
041460	CM	446F1	N/A

OCTAL DATA	MNE- MONIC	P/N 23-	SEE TABLE
042060	D0	774F1	1-3

NOTE::REFER TO 11/44 DOCUMENTATION.

THIS IS A CONTINUATION ROM OF A MULTIPLE-ROM BOOT

BAD ROM OR NO ROM PRESENT

TW

SECTION 6

S1 SWITCH SETTING FOR CPU DIAGNOSTIC ROM

TW

TABLE 1-1
ROM P/N 23-616F1

11/60/70 DIAGNOSTIC ROM

THERE ARE NO SPECIAL M9312 SWITCH SETTINGS THAT PERTAIN TO THIS ROM.
THE ONLY WAY THESE DIAGNOSTICS CAN BE EXECUTED IS BY ENTERING A BOOTSTRAP
AT AN ENTRY POINT THAT CALLS FOR DIAGNOSTICS TO BE RUN.

THIS ROM ALLOWS BOOTING VIA CONSOLE SWITCH REGISTER.
THIS CAN BE DONE AS FOLLOWS:

- 1. LOAD ADDRESS 765744
- 2. SET SWITCH REGISTER AS SHOWN BELOW

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
NA	NA	NA	NA												
				OCTAL UNIT		SWR CODE FROM BOOT ROM TABLES									
				NUMBER											

- 3. NOW START

TW

TABLE 1-2
ROM P/N 23-248F1

ASCII CONSOLE AND DIAGNOSTIC ROM FOR USE WITH 11/04/05/34/35/40/45/50/55

THIS ROM CONTAINS CPU DIAGNOSTICS AND AN ASCII CONSOLE. TO ENTER THE ASCII CONSOLE VIA POWER-UP BOOT OR PUSH-BUTTON BOOT, THE M9312 SWITCH SETTINGS MUST BE AS SHOWN BELOW.

FUNCTION TO BE BOOTED	ROM LOC.	DIAG- NOSTIC	MANUAL STARTING ADDR.	S1 SWITCH SETTINGS FOR PUSH-BUTTON OR POWER FAIL BOOT									
				1	2	3	4	5	6	7	8	9	10
CONSOLE EMULATOR!	E20	NO	165144	ON	*	OFF	OFF	ON	ON	OFF	OFF	ON	OFF
CONSOLE EMULATOR!	E20	YES	165020	ON	*	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF

* S1-2: WHEN ON, POWER-UP BOOT IS ENABLED; WHEN OFF, POWER-UP BOOT IS DISABLED, NOTE:: MUST ALWAYS BE OFF IN 11/24 MACHINES.

THE CONSOLE EMULATOR CAN PERFORM THE FOLLOWING FUNCTIONS:

1. LOAD ADDRESS
2. EXAMINE
3. DEPOSIT
4. START
5. BOOT A DEVICE

A FULL DESCRIPTION OF THE FIRST FOUR FUNCTIONS IS GIVEN IN THE M9312 BOOTSTRAP/TERMINATOR MODULE TECHNICAL MANUAL, EK-M9312-TM-001.

TO BOOT A DEVICE VIA THE CONSOLE EMULATOR, DO THE FOLLOWING:

1. START THE CONSOLE EMULATOR
THIS CAN BE DONE BY SETTING UP THE M9312 SWITCHES AS OUTLINED IN THE TABLE ABOVE, THEN POWER FAILING THE CPU (S1-2 MUST BE ON TO DO THIS), OR PRESSING THE BOOT SWITCH (IF ONE IS AVAILABLE). ANOTHER WAY OF STARTING THE CONSOLE EMULATOR IS BY MANUALLY LOADING AND STARTING VIA CONSOLE SWITCH REGISTER (IF ONE IS AVAILABLE), USING THE MANUAL STARTING ADDR. SUPPLIED IN THE TABLE ABOVE.
2. TYPE IN THE APPROPRIATE BOOT COMMAND.
ONCE THE CONSOLE EMULATOR IS RUNNING, TYPE IN THE TWO LETTER MNEMONIC OF THE DEVICE TO BE BOOTED, FOLLOWED BY A CARRIAGE RETURN; OR TYPE IN THE TWO LETTER DEVICE MNEMONIC FOLLOWED BY AN OCTAL UNIT NUMBER, THEN A CARRIAGE RETURN. (TWO LETTER DEVICE MNEMONICS CAN BE FOUND IN THE FOLLOWING BOOT ROM TABLES.)

TW

TABLE 1-3
ROM P/N 23-774F1

ASCII CONSOLE AND DIAGNOSTIC ROM FOR USE WITH 11/24

THIS ROM CONTAINS CPU DIAGNOSTICS AND AN ASCII CONSOLE. TO ENTER THE ASCII CONSOLE VIA POWER-UP BOOT OR PUSH-BUTTON BOOT, THE M9312 SWITCH SETTINGS MUST BE AS SHOWN BELOW.

FUNCTION TO BE BOOTED	ROM LOC.	DIAG- NOSTIC	MANUAL STARTING ADDR.	S1 SWITCH SETTINGS FOR PUSH-BUTTON OR POWER FAIL BOOT									
				1	2	3	4	5	6	7	8	9	10
CONSOLE EMULATOR	E20	NO	165004	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF
CONSOLE EMULATOR	E20	YES	165006	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON

THE CONSOLE EMULATOR CAN PERFORM THE FOLLOWING FUNCTIONS:

1. LOAD ADDRESS
2. EXAMINE
3. DEPOSIT
4. START
5. BOOT A DEVICE

A FULL DESCRIPTION OF THE FIRST FOUR FUNCTIONS IS GIVEN IN THE M9312 BOOTSTRAP/TERMINATOR MODULE TECHNICAL MANUAL, EK-M9312-TM-001.

TO BOOT A DEVICE VIA THE CONSOLE EMULATOR, DO THE FOLLOWING:

1. START THE CONSOLE EMULATOR

THIS CAN BE DONE BY SETTING UP THE M9312 SWITCHES AS OUTLINED IN THE TABLE ABOVE, THEN POWER FAILING THE CPU (REFER TO 11/24 MANUAL FOR PWR UP BOOT), OR PRESSING THE BOOT SWITCH (IF ONE IS AVAILABLE). ANOTHER WAY OF STARTING THE CONSOLE EMULATOR IS BY MANUALLY LOADING AND STARTING VIA CONSOLE SWITCH REGISTER (IF ONE IS AVAILABLE), USING THE MANUAL STARTING ADDR. SUPPLIED IN THE TABLE ABOVE.

2. TYPE IN THE APPROPRIATE BOOT COMMAND.

ONCE THE CONSOLE EMULATOR IS RUNNING, TYPE IN THE TWO LETTER MNEMONIC OF THE DEVICE TO BE BOOTED, FOLLOWED BY A CARRIAGE RETURN; OR TYPE IN THE TWO LETTER DEVICE MNEMONIC FOLLOWED BY AN OCTAL UNIT NUMBER, THEN A CARRIAGE RETURN. (TWO LETTER DEVICE MNEMONICS CAN BE FOUND IN THE FOLLOWING BOOT ROM TABLES.)

TW

SECTION 7

S1 SWITCH SETTING FOR PERIPHERAL BOOT ROMS
TABLE 2-1
ROM P/N 23-751A9

THE TABLE BELOW CONTAINS THE FOLLOWING:
1. M9312 SWITCH SETTINGS FOR POWER-UP BOOT OR PUSH-BUTTON BOOT OF DEVICE.
2. THE START ADDRESS FOR THE CONSOLE LOAD AND START SEQUENCE.
NOTES IF DIAGNOSTIC ARE TO BE RUN, A CPU DIAGNOSTIC ROM MUST BE IN LOCATION E20, AND JUMPER W8 MUST BE OUT.

DEVICE TO BE BOOTED	ROM LOC.	DIAG- NOSTIC	UNIT	START ADDR.	SWITCH SETTINGS S1-										SWR CODE
					1	2	3	4	5	6	7	8	9	10	
RL01	ROM 1	NO	0	173004	OFF	*	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	NA
RL01	ROM 1	YES	0	173006	OFF	*	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	012
RL01	ROM 2	NO	0	173204	OFF	*	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	NA
RL01	ROM 2	YES	0	173206	OFF	*	OFF	ON	OFF	OFF	OFF	OFF	ON	ON	212
RL01	ROM 3	NO	0	173404	OFF	*	ON	OFF	OFF	OFF	OFF	OFF	ON	OFF	NA
RL01	ROM 3	YES	0	173406	OFF	*	ON	OFF	OFF	OFF	OFF	OFF	ON	ON	412
RL01	ROM 4	NO	0	173604	OFF	*	ON	ON	OFF	OFF	OFF	OFF	ON	OFF	NA
RL01	ROM 4	YES	0	173606	OFF	*	ON	ON	OFF	OFF	OFF	OFF	ON	ON	612

* S1-2: WHEN ON, POWER-UP BOOT IS ENABLED; WHEN OFF, POWER-UP BOOT DISABLED. (MUST BE OFF FOR 11/24,/60. SEE 11/24,/60 DOCUMENTATION FOR POWER-UP BOOT)

WHEN BOOTING FROM THE CONSOLE EMULATOR, A DEVICE MNEMONIC AND UNIT NUMBER ARE REQUIRED. IF UNIT NUMBER IS NOT ENTERED, IT IS ASSUMED TO BE ZERO. LISTED BELOW ARE THE DEVICE MNEMONIC AND UNIT NUMBERS SUPPORTED BY THIS ROM, AND THE DEVICE CSR ADDRESS ASSUMED BY THE BOOT CODE.

DEVICE	MNEMONIC	UNIT	CSR
RL01	DL	0-3	774400

TW

TABLE 2-2
ROM P/N 23-752A9

THE TABLE BELOW CONTAINS THE FOLLOWING:
1. M9312 SWITCH SETTINGS FOR POWER-UP BOOT OR PUSH-BUTTON BOOT OF DEVICE.
2. THE START ADDRESS FOR THE CONSOLE LOAD AND START SEQUENCE.
NOTES IF DIAGNOSTIC ARE TO BE RUN, A CPU DIAGNOSTIC ROM MUST BE IN LOCATION E20, AND JUMPER W8 MUST BE OUT.

DEVICE TO BE BOOTED	ROM LOC.	DIAG- NOSTIC	UNIT	START ADDR.	SWITCH SETTINGS S1-										SWR CODE
					1	2	3	4	5	6	7	8	9	10	
RK06/07	ROM 1	NO	0	173004	OFF	*	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	NA
RK06/07	ROM 1	YES	0	173006	OFF	*	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	012
RK06/07	ROM 2	NO	0	173204	OFF	*	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	NA
RK06/07	ROM 2	YES	0	173206	OFF	*	OFF	ON	OFF	OFF	OFF	OFF	ON	ON	212
RK06/07	ROM 3	NO	0	173404	OFF	*	ON	OFF	OFF	OFF	OFF	OFF	ON	OFF	NA
RK06/07	ROM 3	YES	0	173406	OFF	*	ON	OFF	OFF	OFF	OFF	OFF	ON	ON	412
RK06/07	ROM 4	NO	0	173604	OFF	*	ON	ON	OFF	OFF	OFF	OFF	ON	OFF	NA
RK06/07	ROM 4	YES	0	173606	OFF	*	ON	ON	OFF	OFF	OFF	OFF	ON	ON	612

* S1-2: WHEN ON, POWER-UP BOOT IS ENABLED; WHEN OFF, POWER-UP BOOT DISABLED. (MUST BE OFF FOR 11/24,/60. SEE 11/24,/60 DOCUMENTATION FOR POWER-UP BOOT)

WHEN BOOTING FROM THE CONSOLE EMULATOR, A DEVICE MNEMONIC AND UNIT NUMBER ARE REQUIRED. IF UNIT NUMBER IS NOT ENTERED, IT IS ASSUMED TO BE ZERO. LISTED BELOW ARE THE DEVICE MNEMONIC AND UNIT NUMBERS SUPPORTED BY THIS ROM, AND THE DEVICE CSR ADDRESS ASSUMED BY THE BOOT CODE.

DEVICE	MNEMONIC	UNIT	CSR
RK06/07	DM	0-7	777440

TW

TABLE 2-3
ROM P/N 23-753A9

THE TABLE BELOW CONTAINS THE FOLLOWING:

1. M9312 SWITCH SETTINGS FOR POWER-UP BOOT OR PUSH-BUTTON BOOT OF DEVICE.

2. THE START ADDRESS FOR THE CONSOLE LOAD AND START SEQUENCE.

NOTES IF DIAGNOSTIC ARE TO BE RUN, A CPU DIAGNOSTIC ROM MUST BE IN LOCATION F20, AND JUMPER W8 MUST BE OUT.

DEVICE TO BE BOOTED	ROM LOC.	DIAG- NOSTIC	UNIT	START ADDR.	SWITCH SETTINGS S1-										SWR CODE
					1	2	3	4	5	6	7	8	9	10	
RXM1	ROM 1	NO	0	173004	OFF	*	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	NA
RX01	ROM 1	YES	0	173006	OFF	*	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	012
RXM1	ROM 2	NO	0	173204	OFF	*	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	NA
RX01	ROM 2	YES	0	173206	OFF	*	OFF	ON	OFF	OFF	OFF	OFF	ON	ON	212
RXM1	ROM 3	NO	0	173404	OFF	*	ON	OFF	OFF	OFF	OFF	OFF	ON	OFF	NA
PXM1	ROM 3	YES	0	173406	OFF	*	ON	OFF	OFF	OFF	OFF	OFF	ON	ON	412
RXM1	ROM 4	NO	0	173604	OFF	*	ON	ON	OFF	OFF	OFF	OFF	ON	OFF	NA
RX01	ROM 4	YES	0	173606	OFF	*	ON	ON	OFF	OFF	OFF	OFF	ON	ON	612

* S1-2: WHEN ON, POWER-UP BOOT IS ENABLED; WHEN OFF, POWER-UP BOOT DISABLED. (MUST BE OFF FOR 11/24, /60. SEE 11/24, /60 DOCUMENTATION FOR POWER-UP BOOT)

WHEN BOOTING FROM THE CONSOLE EMULATOR, A DEVICE MNEMONIC AND UNIT NUMBER ARE REQUIRED. IF UNIT NUMBER IS NOT ENTERED, IT IS ASSUMED TO BE ZERO. LISTED BELOW ARE THE DEVICE MNEMONIC AND UNIT NUMBERS SUPPORTED BY THIS ROM, AND THE DEVICE CSR ADDRESS ASSUMED BY THE BOOT CODE.

DEVICE	MNEMONIC	UNIT	CSR
RXM1	DX	0-1	777170

TW

TABLE 2-4
ROM P/N 23-755A9

THE TABLE BELOW CONTAINS THE FOLLOWING:

1. M9312 SWITCH SETTINGS FOR DEFAULT BOOT OF DEVICES SUPPORTED BY THIS ROM.
2. THE STARTING ADDRESS FOR MANUALLY BOOTING DEVICES SUPPORTED BY THIS ROM

NOTES:

1. IF DIAGNOSTIC IS TO BE RUN, A CPU DIAGNOSTIC ROM MUST BE IN LOCATION E20 AND JUMPER W8 MUST BE OUT
2. * = CAN BE ON OR OFF. FOR S1-2 ON=BOOT ON POWER UP OFF=DO NORMAL POWER UP

DEVICE TO BE BOOTED	ROM LOC.	DIAG-NOSTIC	UNIT	START ADDR.	SWITCH SETTINGS S1-										SWR CODE	
					1	2	3	4	5	6	7	8	9	10		
RP02/03	ROM 1	NO	0	173004	OFF	*	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	NA
RP02/03	ROM 1	YES	0	173006	OFF	*	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	012
RP02/03	ROM 2	NO	0	173204	OFF	*	OFF	ON	OFF	OFF	OFF	OFF	OFF	ON	OFF	NA
RP02/03	ROM 2	YES	0	173206	OFF	*	OFF	ON	OFF	OFF	OFF	OFF	OFF	ON	ON	212
RP02/03	ROM 3	NO	0	173404	OFF	*	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	NA
RP02/03	ROM 3	YES	0	173406	OFF	*	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	412
RP02/03	ROM 4	NO	0	173604	OFF	*	ON	ON	OFF	OFF	OFF	OFF	OFF	ON	OFF	NA
RP02/03	ROM 4	YES	0	173606	OFF	*	ON	ON	OFF	OFF	OFF	OFF	OFF	ON	ON	612
RP04/5/6 RP02/3	ROM 1	NO	0	173050	OFF	*	OFF	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	NA
RP04/5/6 RP02/3	ROM 1	YES	0	173052	OFF	*	OFF	OFF	OFF	OFF	ON	OFF	ON	OFF	ON	056
RP04/5/6 RP02/3	ROM 2	NO	0	173250	OFF	*	OFF	ON	OFF	OFF	ON	OFF	ON	OFF	OFF	NA
RP04/5/6 RP02/3	ROM 2	YES	0	173252	OFF	*	OFF	ON	OFF	OFF	ON	OFF	ON	OFF	ON	256
RP04/5/6 RP02/3	ROM 3	NO	0	173450	OFF	*	ON	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	NA
RP04/5/6 RP02/3	ROM 3	YES	0	173452	OFF	*	ON	OFF	OFF	OFF	ON	OFF	ON	OFF	ON	456
RP04/5/6 RP02/3	ROM 4	NO	0	173650	OFF	*	ON	ON	OFF	OFF	ON	OFF	ON	OFF	OFF	NA
RP04/5/6 RP02/3	ROM 4	YES	0	173652	OFF	*	ON	ON	OFF	OFF	ON	OFF	ON	OFF	ON	656

* S1-2: WHEN ON, POWER-UP BOOT IS ENABLED; WHEN OFF, POWER-UP BOOT DISABLED. (MUST BE OFF FOR 11/24,/60. SEE 11/24,/60 DOCUMENTATION FOR POWER-UP BOOT)

WHEN BOOTING FROM THE CONSOLE EMULATOR, A DEVICE MNEMONIC AND UNIT NUMBER ARE REQUIRED. IF UNIT NUMBER IS NOT ENTERED, IT IS ASSUMED TO BE ZERO. LISTED BELOW ARE THE DEVICE MNEMONIC AND UNIT NUMBERS SUPPORTED BY THIS ROM, AND THE DEVICE CSR ADDRESS ASSUMED BY THE BOOT CODE.

DEVICE	MNEMONIC	UNIT	CSR
RP02/03	DP	0-7	776714
RP04/5/6 RP02/3	DB	0-7	776700

TW

TABLE 2-5
ROM P/N 23-756A9

THE TABLE BELOW CONTAINS THE FOLLOWING:

- 1. M9312 SWITCH SETTINGS FOR POWER-UP BOOT OR PUSH-BUTTON BOOT OF DEVICE.
- 2. THE START ADDRESS FOR THE CONSOLE LOAD AND START SEQUENCE.

NOTES IF DIAGNOSTIC ARE TO BE RUN, A CPU DIAGNOSTIC ROM MUST BE IN LOCATION E20, AND JUMPER W8 MUST BE OUT.

DEVICE TO BE BOOTED	ROM LOC.	DIAG- NOSTIC	UNIT	START ADDR.	SWITCH SETTINGS S1-										SWR CODE
					1	2	3	4	5	6	7	8	9	10	
RK03/05	ROM 1	NO	0	173004	OFF	*	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	NA
RK03/05	ROM 1	NO	2	173164	OFF	*	OFF	OFF	ON	ON	ON	OFF	ON	OFF	NA
RK03/05	ROM 1	YES	0	173006	OFF	*	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	012
RK03/05	ROM 2	NO	0	173204	OFF	*	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	NA
RK03/05	ROM 2	NO	2	173364	OFF	*	OFF	ON	ON	ON	ON	OFF	ON	OFF	NA
RK03/05	ROM 2	YES	0	173206	OFF	*	OFF	ON	OFF	OFF	OFF	OFF	ON	ON	212
RK03/05	ROM 3	NO	0	173404	OFF	*	ON	OFF	OFF	OFF	OFF	OFF	ON	OFF	NA
RK03/05	ROM 3	NO	2	173564	OFF	*	ON	OFF	ON	ON	ON	OFF	ON	OFF	NA
RK03/05	ROM 3	YES	0	173406	OFF	*	ON	OFF	OFF	OFF	OFF	OFF	ON	ON	412
RK03/05	ROM 4	NO	0	173604	OFF	*	ON	ON	OFF	OFF	OFF	OFF	ON	OFF	NA
RK03/05	ROM 4	NO	2	173764	OFF	*	ON	ON	ON	ON	ON	OFF	ON	OFF	NA
RK03/05	ROM 4	YES	0	173606	OFF	*	ON	ON	OFF	OFF	OFF	OFF	ON	ON	612
TU55/56	ROM 1	NO	0	173034	OFF	*	OFF	OFF	OFF	OFF	ON	ON	ON	OFF	NA
TU55/56	ROM 1	YES	0	173036	OFF	*	OFF	OFF	OFF	OFF	ON	ON	ON	ON	042
TU55/56	ROM 2	NO	0	173234	OFF	*	OFF	ON	OFF	OFF	ON	ON	ON	OFF	NA
TU55/56	ROM 2	YES	0	173236	OFF	*	OFF	ON	OFF	OFF	ON	ON	ON	ON	242
TU55/56	ROM 3	NO	0	173434	OFF	*	ON	OFF	OFF	OFF	ON	ON	ON	OFF	NA
TU55/56	ROM 3	YES	0	173436	OFF	*	ON	OFF	OFF	OFF	ON	ON	ON	ON	442
TU55/56	ROM 4	NO	0	173634	OFF	*	ON	ON	OFF	OFF	ON	ON	ON	OFF	NA
TU55/56	ROM 4	YES	0	173636	OFF	*	ON	ON	OFF	OFF	ON	ON	ON	ON	642

* S1-2: WHEN ON, POWER-UP BOOT IS ENABLED; WHEN OFF, POWER-UP BOOT DISABLED. (MUST BE OFF FOR 11/24, /60. SEE 11/24, /60 DOCUMENTATION FOR POWER-UP BOOT)

WHEN BOOTING FROM THE CONSOLE EMULATOR, A DEVICE MNEMONIC AND UNIT NUMBER ARE REQUIRED. IF UNIT NUMBER IS NOT ENTERED, IT IS ASSUMED TO BE ZERO. LISTED BELOW ARE THE DEVICE MNEMONIC AND UNIT NUMBERS SUPPORTED BY THIS ROM, AND THE DEVICE CSR ADDRESS ASSUMED BY THE BOOT CODE.

DEVICE	MNEMONIC	UNIT	CSR
RK03/05	DK	0-7	777404
TU55/56	DT	0-7	777342

TW

TABLE 2-6
ROM P/N 23-757A9

THE TABLE BELOW CONTAINS THE FOLLOWING:
1. M9312 SWITCH SETTINGS FOR POWER-UP BOOT OR PUSH-BUTTON BOOT OF DEVICE.
2. THE START ADDRESS FOR THE CONSOLE LOAD AND START SEQUENCE.
NOTES IF DIAGNOSTIC ARE TO BE RUN, A CPU DIAGNOSTIC ROM MUST BE IN LOCATION E20, AND JUMPER W8 MUST BE OUT.

DEVICE TO BE BOOTED	ROM LOC.	DIAG- NOSTIC	UNIT	START ADDR.	SWITCH SETTINGS S1-										SWR CODE
					1	2	3	4	5	6	7	8	9	10	
TU16/45/77/E16	ROM 1	NO	0	173004	OFF	*	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	NA
TU16/45/77/E16	ROM 1	YES	0	173006	OFF	*	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	012
TU16/45/77/E16	ROM 2	NO	0	173204	OFF	*	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	NA
TU16/45/77/E16	ROM 2	YES	0	173206	OFF	*	OFF	ON	OFF	OFF	OFF	OFF	ON	ON	212
TU16/45/77/E16	ROM 3	NO	0	173404	OFF	*	ON	OFF	OFF	OFF	OFF	OFF	ON	OFF	NA
TU16/45/77/E16	ROM 3	YES	0	173406	OFF	*	ON	OFF	OFF	OFF	OFF	OFF	ON	ON	412
TU16/45/77/E16	ROM 4	NO	0	173604	OFF	*	ON	ON	OFF	OFF	OFF	OFF	ON	OFF	NA
TU16/45/77/E16	ROM 4	YES	0	173606	OFF	*	ON	ON	OFF	OFF	OFF	OFF	ON	ON	612

* S1-2: WHEN ON, POWER-UP BOOT IS ENABLED; WHEN OFF, POWER-UP BOOT DISABLED. (MUST BE OFF FOR 11/24,/60. SEE 11/24,/60 DOCUMENTATION FOR POWER-UP BOOT)

WHEN BOOTING FROM THE CONSOLE EMULATOR, A DEVICE MNEMONIC AND UNIT NUMBER ARE REQUIRED. IF UNIT NUMBER IS NOT ENTERED, IT IS ASSUMED TO BE ZERO. LISTED BELOW ARE THE DEVICE MNEMONIC AND UNIT NUMBERS SUPPORTED BY THIS ROM, AND THE DEVICE CSR ADDRESS ASSUMED BY THE BOOT CODE.

DEVICE	MNEMONIC	UNIT	CSR
TU16/45/77/E16	MM	0-7	772440

TW

TABLE 2-7
ROM P/N 23-758A9

THE TABLE BELOW CONTAINS THE FOLLOWING:

- 1.M9312 SWITCH SETTINGS FOR POWER-UP BOOT OR PUSH-BUTTON BOOT OF DEVICE.
- 2.THE START ADDRESS FOR THE CONSOLE LOAD AND START SEQUENCE.

NOTES IF DIAGNOSTIC APE TO BE RUN,A CPU DIAGNOSTIC ROM MUST BE IN LOCATION E20, AND JUMPER W8 MUST BE OUT.

DEVICE TO BE BOOTED	ROM LOC.	DIAG- NOSTIC	UNIT	START ADDR.	SWITCH SETTINGS S1-										SWR CODE
					1	2	3	4	5	6	7	8	9	10	
TU10/E10,TS03	ROM 1	NO	0	173004	OFF	*	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	NA
TU10/E10,TS03	ROM 1	YES	0	173006	OFF	*	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	012
TU10/E10,TS03	ROM 2	NO	0	173204	OFF	*	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	NA
TU10/E10,TS03	ROM 2	YES	0	173206	OFF	*	OFF	ON	OFF	OFF	OFF	OFF	ON	ON	212
TU10/E10,TS03	ROM 3	NO	0	173404	OFF	*	ON	OFF	OFF	OFF	OFF	OFF	ON	OFF	NA
TU10/E10,TS03	ROM 3	YES	0	173406	OFF	*	ON	OFF	OFF	OFF	OFF	OFF	ON	ON	412
TU10/E10,TS03	ROM 4	NO	0	173604	OFF	*	ON	ON	OFF	OFF	OFF	OFF	ON	OFF	NA
TU10/E10,TS03	ROM 4	YES	0	173606	OFF	*	ON	ON	OFF	OFF	OFF	OFF	ON	ON	612

* S1-2: WHEN ON,POWER-UP BOOT IS ENABLED;WHEN OFF,POWER-UP BOOT DISABLED.(MUST BE OFF FOR 11/24,/60,SEE 11/24,/60 DOCUMENTATION FOR POWER-UP BOOT)

WHEN BOOTING FROM THE CONSOLE EMULATOR,A DEVICE MNEMONIC AND UNIT NUMBER ARE REQUIRED. IF UNIT NUMBER IS NOT ENTERED, IT IS ASSUMED TO BE ZERO,LISTED BELOW ARE THE DEVICE MNEMONIC AND UNIT NUMBERS SUPPORTED BY THIS ROM,AND THE DEVICE CSR ADDRESS ASSUMED BY THE ROOT CODE.

DEVICE	MNEMONIC	UNIT	CSR
TU10/E10,TS03	MT	0-7	772522

TW

TABLE 2-8
ROM P/N 23-759A9

THE TABLE BELOW CONTAINS THE FOLLOWING:
1.M9312 SWITCH SETTINGS FOR POWER-UP BOOT OR PUSH-BUTTON BOOT OF DEVICE.
2.THE START ADDRESS FOR THE CONSOLE LOAD AND START SEQUENCE.
NOTES IF DIAGNOSTIC ARE TO BE RUN,A CPU DIAGNOSTIC ROM MUST BE IN LOCATION E20, AND JUMPER W8 MUST BE OUT.

DEVICE TO BE BOOTED	ROM LOC.	DIAG- NOSTIC	UNIT	START ADDR.	SWITCH SETTINGS S1-										SWR CODE
					1	2	3	4	5	6	7	8	9	10	
RS03/04	ROM 1	NO	0	173004	OFF	*	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	NA
RS03/04	ROM 1	YES	0	173006	OFF	*	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	012
RS03/04	ROM 2	NO	0	173204	OFF	*	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	NA
RS03/04	ROM 2	YES	0	173206	OFF	*	OFF	ON	OFF	OFF	OFF	OFF	ON	ON	212
RS03/04	ROM 3	NO	0	173404	OFF	*	ON	OFF	OFF	OFF	OFF	OFF	ON	OFF	NA
RS03/04	ROM 3	YES	0	173406	OFF	*	ON	OFF	OFF	OFF	OFF	OFF	ON	ON	412
RS03/04	ROM 4	NO	0	173604	OFF	*	ON	ON	OFF	OFF	OFF	OFF	ON	OFF	NA
RS03/04	ROM 4	YES	0	173606	OFF	*	ON	ON	OFF	OFF	OFF	OFF	ON	ON	612

* S1-2: WHEN ON,POWER-UP BOOT IS ENABLED;WHEN OFF,POWER-UP BOOT DISABLED.(MUST BE OFF FOR 11/24,/60.SEE 11/24,/60 DOCUMENTATION FOR POWER-UP BOOT)

WHEN BOOTING FROM THE CONSOLE EMULATOR,A DEVICE MNEMONIC AND UNIT NUMBER ARE REQUIRED. IF UNIT NUMBER IS NOT ENTERED, IT IS ASSUMED TO BE ZERO.LISTED BELOW ARE THE DEVICE MNEMONIC AND UNIT NUMBERS SUPPORTED BY THIS ROM,AND THE DEVICE CSR ADDRESS ASSUMED BY THE BOOT CODE.

DEVICE	MNEMONIC	UNIT	CSR
RS03/04	DS	0-7	772040

TW

TABLE 2-9
ROM P/N 23-760A9

THE TABLE BELOW CONTAINS THE FOLLOWING:

- 1. M9312 SWITCH SETTINGS FOR POWER-UP BOOT OR PUSH-BUTTON BOOT OF DEVICE.
- 2. THE START ADDRESS-FOR THE CONSOLE LOAD AND START SEQUENCE.

NOTES IF DIAGNOSTIC ARE TO BE RUN, A CPU DIAGNOSTIC ROM MUST BE IN LOCATION E20, AND JUMPER W8 MUST BE OUT.

DEVICE TO BE BOOTED	ROM LOC.	DIAG- NOSTIC	UNIT	START ADDR.	SWITCH SETTINGS S1=										SWR CODE
					1	2	3	4	5	6	7	8	9	10	
PC05	ROM 1	NO	0	173004	OFF	*	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	NA
PC05	ROM 1	YES	0	173006	OFF	*	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	012
PC05	ROM 2	NO	0	173204	OFF	*	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	NA
PC05	ROM 2	YES	0	173206	OFF	*	OFF	ON	OFF	OFF	OFF	OFF	ON	ON	212
PC05	ROM 3	NO	0	173404	OFF	*	ON	OFF	OFF	OFF	OFF	OFF	ON	OFF	NA
PC05	ROM 3	YES	0	173406	OFF	*	ON	OFF	OFF	OFF	OFF	OFF	ON	ON	412
PC05	ROM 4	NO	0	173604	OFF	*	ON	ON	OFF	OFF	OFF	OFF	ON	OFF	NA
PC05	ROM 4	YES	0	173606	OFF	*	ON	ON	OFF	OFF	OFF	OFF	ON	ON	612
LO SPD RDR	ROM 1	NO	0	173034	OFF	*	OFF	OFF	OFF	OFF	ON	ON	ON	OFF	NA
LO SPD RDR	ROM 1	YES	0	173036	OFF	*	OFF	OFF	OFF	OFF	ON	ON	ON	ON	042
LO SPD RDR	ROM 2	NO	0	173234	OFF	*	OFF	ON	OFF	OFF	ON	ON	ON	OFF	NA
LO SPD RDR	ROM 2	YES	0	173236	OFF	*	OFF	ON	OFF	OFF	ON	ON	ON	ON	242
LO SPD RDR	ROM 3	NO	0	173434	OFF	*	ON	OFF	OFF	OFF	ON	ON	ON	OFF	NA
LO SPD RDR	ROM 3	YES	0	173436	OFF	*	ON	OFF	OFF	OFF	ON	ON	ON	ON	442
LO SPD RDR	ROM 4	NO	0	173634	OFF	*	ON	ON	OFF	OFF	ON	ON	ON	OFF	NA
LO SPD RDR	ROM 4	YES	0	173636	OFF	*	ON	ON	OFF	OFF	ON	ON	ON	ON	642

* S1-2: WHEN ON, POWER-UP BOOT IS ENABLED; WHEN OFF, POWER-UP BOOT DISABLED. (MUST BE OFF FOR 11/24, /60. SEE 11/24, /60 DOCUMENTATION FOR POWER-UP BOOT)

WHEN BOOTING FROM THE CONSOLE EMULATOR, A DEVICE MNEMONIC AND UNIT NUMBER ARE REQUIRED. IF UNIT NUMBER IS NOT ENTERED, IT IS ASSUMED TO BE ZERO. LISTED BELOW ARE THE DEVICE MNEMONIC AND UNIT NUMBERS SUPPORTED BY THIS ROM, AND THE DEVICE CSR ADDRESS ASSUMED BY THE BOOT CODE.

DEVICE	MNEMONIC	UNIT	CSR
PC05	PR	N/A	777550
LO SPD RDR	TT	N/A	777560

TW

TABLE 2-10
ROM P/N 23-761A9,766A9

THE TABLE BELOW CONTAINS THE FOLLOWING:
1.M9312 SWITCH SETTINGS FOR POWER-UP BOOT OR PUSH-BUTTON BOOT OF DEVICE.
2.THE START ADDRESS FOR THE CONSOLE LOAD AND START SEQUENCE.

NOTES IF DIAGNOSTIC ARE TO BE RUN,A CPU DIAGNOSTIC ROM MUST BE IN LOCATION E20, AND JUMPER W8 MUST BE OUT.

DEVICE TO BE BOOTED	ROM LOC.	DIAG- NOSTIC	UNIT	START ADDR.	SWITCH SETTINGS S1-										SWR CODE
					1	2	3	4	5	6	7	8	9	10	
TU60	ROM 1	NO	0	173004	OFF	*	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	NA
TU60	ROM 1	YES	0	173006	OFF	*	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	012
TU60	ROM 2	NO	0	173204	OFF	*	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	NA
TU60	ROM 2	YES	0	173206	OFF	*	OFF	ON	OFF	OFF	OFF	OFF	ON	ON	212
TU60	ROM 3	NO	0	173404	OFF	*	ON	OFF	OFF	OFF	OFF	OFF	ON	OFF	NA
TU60	ROM 3	YES	0	173406	OFF	*	ON	OFF	OFF	OFF	OFF	OFF	ON	ON	412
TU60	ROM 4	NO	0	173604	OFF	*	ON	ON	OFF	OFF	OFF	OFF	ON	OFF	NA
TU60	ROM 4	YES	0	173606	OFF	*	ON	ON	OFF	OFF	OFF	OFF	ON	ON	612

* S1-2: WHEN ON,POWER-UP BOOT IS ENABLED;WHEN OFF,POWER-UP BOOT DISABLED.(MUST BE OFF FOR 11/24,/60.SEE 11/24,/60 DOCUMENTATION FOR POWER-UP BOOT)

WHEN BOOTING FROM THE CONSOLE EMULATOR,A DEVICE MNEMONIC AND UNIT NUMBER ARE REQUIRED. IF UNIT NUMBER IS NOT ENTERED, IT IS ASSUMED TO BE ZERO.LISTED BELOW ARE THE DEVICE MNEMONIC AND UNIT NUMBERS SUPPORTED BY THIS ROM,AND THE DEVICE CSR ADDRESS ASSUMED BY THE BOOT CODE.

DEVICE	MNEMONIC	UNIT	CSR
TU60	CT	0-1	777500

TW

TABLE 2-11
ROM P/M 23-811A9

THE TABLE BELOW CONTAINS THE FOLLOWING:

- 1. M9312 SWITCH SETTINGS FOR POWER-UP BOOT OR PUSH-BUTTON BOOT OF DEVICE.
- 2. THE START ADDRESS FOR THE CONSOLE LOAD AND START SEQUENCE.

NOTES IF DIAGNOSTIC ARE TO BE RUN, A CPU DIAGNOSTIC ROM MUST BE IN LOCATION E20, AND JUMPER W8 MUST BE OUT.

DEVICE TO BE BOOTED	ROM LOC.	DIAG- NOSTIC	UNIT	START ADDR.	SWITCH SETTINGS S1-										SWR CODE
					1	2	3	4	5	6	7	8	9	10	
RX02	ROM 1	NO	0	173004	OFF	*	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	NA
RX02	ROM 1	YES	0	173006	OFF	*	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	012
RX02	ROM 2	NO	0	173204	OFF	*	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	NA
RX02	ROM 2	YES	0	173206	OFF	*	OFF	ON	OFF	OFF	OFF	OFF	ON	ON	212
RX02	ROM 3	NO	0	173404	OFF	*	ON	OFF	OFF	OFF	OFF	OFF	ON	OFF	NA
RX02	ROM 3	YES	0	173406	OFF	*	ON	OFF	OFF	OFF	OFF	OFF	ON	ON	412
RX02	ROM 4	NO	0	173604	OFF	*	ON	ON	OFF	OFF	OFF	OFF	ON	OFF	NA
RX02	ROM 4	YES	0	173606	OFF	*	ON	ON	OFF	OFF	OFF	OFF	ON	ON	612

* S1-2: WHEN ON, POWER-UP BOOT IS ENABLED; WHEN OFF, POWER-UP BOOT DISABLED. (MUST BE OFF FOR 11/24,/60. SEE 11/24,/60 DOCUMENTATION FOR POWER-UP BOOT)

WHEN BOOTING FROM THE CONSOLE EMULATOR, A DEVICE MNEMONIC AND UNIT NUMBER ARE REQUIRED. IF UNIT NUMBER IS NOT ENTERED, IT IS ASSUMED TO BE ZERO. LISTED BELOW ARE THE DEVICE MNEMONIC AND UNIT NUMBERS SUPPORTED BY THIS ROM, AND THE DEVICE CSR ADDRESS ASSUMED BY THE BOOT CODE.

DEVICE	MNEMONIC	UNIT	CSR
RX02	DY	0-1	777170

TW

TABLE 2-12
ROM P/N 23-764A9

THE TABLE BELOW CONTAINS THE FOLLOWING:

1. M9312 SWITCH SETTINGS FOR POWER-UP BOOT OR PUSH-BUTTON BOOT OF DEVICE.

2. THE START ADDRESS FOR THE CONSOLE LOAD AND START SEQUENCE.

NOTES IF DIAGNOSTIC ARE TO BE RUN, A CPU DIAGNOSTIC ROM MUST BE IN LOCATION E20, AND JUMPER W8 MUST BE OUT.

DEVICE TO BE BOOTED	ROM LOC.	DIAG- NOSTIC	UNIT	START ADDR.	SWITCH SETTINGS S1-										SNR CODE
					1	2	3	4	5	6	7	8	9	10	
TS04	ROM 1	NO	0	173004	OFF	*	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	NA
TS04	ROM 1	YES	0	173006	OFF	*	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	012
TS04	ROM 2	NO	0	173204	OFF	*	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	NA
TS04	ROM 2	YES	0	173206	OFF	*	OFF	ON	OFF	OFF	OFF	OFF	ON	ON	212
TS04	ROM 3	NO	0	173404	OFF	*	ON	OFF	OFF	OFF	OFF	OFF	ON	OFF	NA
TS04	ROM 3	YES	0	173406	OFF	*	ON	OFF	OFF	OFF	OFF	OFF	ON	ON	412
TS04	ROM 4	NO	0	173604	OFF	*	ON	ON	OFF	OFF	OFF	OFF	ON	OFF	NA
TS04	ROM 4	YES	0	173606	OFF	*	ON	ON	OFF	OFF	OFF	OFF	ON	ON	612

* S1-2: WHEN ON, POWER-UP BOOT IS ENABLED; WHEN OFF, POWER-UP BOOT DISABLED. (MUST BE OFF FOR 11/24, /60. SEE 11/24, /60 DOCUMENTATION FOR POWER-UP BOOT)

WHEN BOOTING FROM THE CONSOLE EMULATOR, A DEVICE MNEMONIC AND UNIT NUMBER ARE REQUIRED. IF UNIT NUMBER IS NOT ENTERED, IT IS ASSUMED TO BE ZERO. LISTED BELOW ARE THE DEVICE MNEMONIC AND UNIT NUMBERS SUPPORTED BY THIS ROM, AND THE DEVICE CSR ADDRESS ASSUMED BY THE BOOT CODE.

DEVICE	MNEMONIC	UNIT	CSR
TS04	MS	0-3	772520

TW

TABLE 2-13
ROM P/N 23-765A9

THE TABLE BELOW CONTAINS THE FOLLOWING:
1.M9312 SWITCH SETTINGS FOR POWER-UP BOOT OR PUSH-BUTTON BOOT OF DEVICE.
2.THE START ADDRESS FOR THE CONSOLE LOAD AND START SEQUENCE.

NOTES IF DIAGNOSTIC ARE TO BE RUN,A CPU DIAGNOSTIC ROM MUST BE IN LOCATION E20, AND JUMPER W8 MUST BE OUT.

DEVICE TO BE BOOTED	ROM LOC.	DIAG- NOSTIC	UNIT	START ADDR.	SWITCH SETTINGS S1-										SWR CODE
					1	2	3	4	5	6	7	8	9	10	
TU58	ROM 1	NO	0	173004	OFF	*	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	NA
TU58	ROM 1	YES	0	173006	OFF	*	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	012
TU58	ROM 2	NO	0	173204	OFF	*	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	NA
TU58	ROM 2	YES	0	173206	OFF	*	OFF	ON	OFF	OFF	OFF	OFF	ON	ON	212
TU58	ROM 3	NO	0	173404	OFF	*	ON	OFF	OFF	OFF	OFF	OFF	ON	OFF	NA
TU58	ROM 3	YES	0	173406	OFF	*	ON	OFF	OFF	OFF	OFF	OFF	ON	ON	412
TU58	ROM 4	NO	0	173604	OFF	*	ON	ON	OFF	OFF	OFF	OFF	ON	OFF	NA
TU58	ROM 4	YES	0	173606	OFF	*	ON	ON	OFF	OFF	OFF	OFF	ON	ON	612

* S1-2: WHEN ON,POWER-UP BOOT IS ENABLED;WHEN OFF,POWER-UP BOOT DISABLED.(MUST BE OFF FOR 11/24,/60.SEE 11/24,/60 DOCUMENTATION FOR POWER-UP BOOT)

WHEN BOOTING FROM THE CONSOLE EMULATOR,A DEVICE MNEMONIC AND UNIT NUMBER ARE REQUIRED. IF UNIT NUMBER IS NOT ENTERED, IT IS ASSUMED TO BE ZERO.LISTED BELOW ARE THE DEVICE MNEMONIC AND UNIT NUMBERS SUPPORTED BY THIS ROM,AND THE DEVICE CSR ADDRESS ASSUMED BY THE BOOT CODE.

DEVICE	MNEMONIC	UNIT	CSR
TU58	DD	0-1	776500

TW

SECTION 8

S1 SWITCH SETTING FOR COMMUNICATION BOOT ROMS

TW

TABLE 3-1
ROM P/N 23-862A9,863A9,864A9

THE TABLE BELOW CONTAINS THE FOLLOWING:
1.M9312 SWITCH SETTINGS FOR POWER-UP BOOT OR PUSH-BUTTON BOOT OF DEVICE.
2.THE START ADDRESS FOR THE CONSOLE LOAD AND START SEQUENCE.

DEVICE TO BE BOOTED	ROM LOC.	DIAG-NOSTIC	UNIT	START ADDR.	SWITCH SETTINGS S1-										SWR CODE
					1	2	3	4	5	6	7	8	9	10	
DMC-11	ROM 1	NO	0	173004	OFF	*	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	NA
DMC-11	ROM 1	YES	0	173006	OFF	*	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	012
DMC-11	ROM 1	NO	1	173030	OFF	*	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	NA
DMC-11	ROM 1	YES	1	173032	OFF	*	OFF	ON	OFF	OFF	OFF	OFF	ON	ON	012
DMC-11	ROM 2	NO	0	173204	OFF	*	ON	OFF	OFF	OFF	OFF	OFF	ON	OFF	NA
DMC-11	ROM 2	YES	0	173206	OFF	*	ON	OFF	OFF	OFF	OFF	OFF	ON	ON	212
DMC-11	ROM 2	NO	1	173230	OFF	*	ON	ON	OFF	OFF	OFF	OFF	ON	OFF	NA
DMC-11	ROM 2	YES	1	173232	OFF	*	ON	ON	OFF	OFF	OFF	OFF	ON	ON	212

* S1-2: WHEN ON,POWER-UP BOOT IS ENABLED;WHEN OFF,POWER-UP BOOT DISABLED.(MUST BE OFF FOR 11/24,/60,SEE 11/24,/60 DOCUMENTATION FOR POWER-UP BOOT)

NOTES

WHEN BOOTING FROM THE CONSOLE EMULATOR,A DEVICE MNEMONIC AND UNIT NUMBER ARE REQUIRED. IF UNIT NUMBER IS NOT ENTERED, IT IS ASSUMED TO BE ZERO.LISTED BELOW ARE THE DEVICE MNEMONIC AND UNIT NUMBERS SUPPORTED BY THIS ROM,AND THE DEVICE CSR ADDRESS ASSUMED BY THE BOOT CODE.

THE BOOT ROMS *** MUST ABSOLUTELY AND WITHOUT EXCEPTION *** BE INSTALLED IN SEQUENCE. THAT IS ,23-862A9 THRU 23-864A9 IN BOOT ROM POSITIONS 1 THRU 3,OR IN BOOT ROM POSITIONS 2 THRU 4!!!

IF DIAGNOSTICS ARE TO BE RUN ,A CPU DIAGNOATIC ROM MUST BE IN LOCATION E20 ,AND JUMPER W8 MUST BE OUT.

DEVICE	MNEMONIC	UNIT	CSR
DMC-11	XM	0-16	ADDRESS AND VECTOR SET TO FLOATING ADDRESS AND VECTOR CONVECTIONS

TW

TABLE 3-2
ROM P/N 23-868A9,869A9,870A9

THE TABLE BELOW CONTAINS THE FOLLOWING:

- 1.M9312 SWITCH SETTINGS FOR POWER-UP BOOT OR PUSH-BUTTON BOOT OF DEVICE.
- 2.THE START ADDRESS FOR THE CONSOLE LOAD AND START SEQUENCE.

DEVICE TO BE BOOTED	ROM LOC.	DIAG- NOSTIC	UNIT	START ADDR.	SWITCH SETTINGS S1-										SWR CODE
					1	2	3	4	5	6	7	8	9	10	
DU11	ROM 1	NO	0	173004	OFF	*	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	NA
DU11	ROM 1	YES	0	173006	OFF	*	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	012
DU11	ROM 1	NO	1	173030	OFF	*	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	NA
DU11	ROM 1	YES	1	173032	OFF	*	OFF	ON	OFF	OFF	OFF	OFF	ON	ON	012
DU11	ROM 2	NO	0	173204	OFF	*	ON	OFF	OFF	OFF	OFF	OFF	ON	OFF	NA
DU11	ROM 2	YES	0	173206	OFF	*	ON	OFF	OFF	OFF	OFF	OFF	ON	ON	212
DU11	ROM 2	NO	1	173230	OFF	*	ON	ON	OFF	OFF	OFF	OFF	ON	OFF	NA
DU11	ROM 2	YES	1	173232	OFF	*	ON	ON	OFF	OFF	OFF	OFF	ON	ON	212

* S1-2: WHEN ON,POWER-UP BOOT IS ENABLED;WHEN OFF,POWER-UP BOOT DISABLED.(MUST BE OFF FOR 11/24,/60,SEE 11/24,/60 DOCUMENTATION FOR POWER-UP BOOT)

NOTES

WHEN BOOTING FROM THE CONSOLE EMULATOR,A DEVICE MNEMONIC AND UNIT NUMBER ARE REQUIRED. IF UNIT NUMBER IS NOT ENTERED, IT IS ASSUMED TO BE ZERO,LISTED BELOW ARE THE DEVICE MNEMONIC AND UNIT NUMBERS SUPPORTED BY THIS ROM,AND THE DEVICE CSR ADDRESS ASSUMED BY THE BOOT CODE.

THE BOOT ROMS *** MUST ABSOLUTELY AND WITHOUT EXCEPTION *** BE INSTALLED IN SEQUENCE.
THAT IS ,23-868A9 THRU 23-870A9 IN BOOT ROM POSITIONS 1 THRU 3,OR IN BOOT ROM POSITIONS 2 THRU 4!!!

IF DIAGNOSTICS ARE TO BE RUN ,A CPU DIAGNOATIC ROM MUST BE IN LOCATION E20 ,AND JUMPER W8 MUST BE OUT.

DEVICE	MNEMONIC	UNIT	CSR
DU11	XU	0-16	ADDRESS AND VECTOR SET TO FLOATING ADDRESS AND VECTOR CONVENTION

TW

TABLE 3-3
ROM P/N 23-865A9,866A9,867A9

THE TABLE BELOW CONTAINS THE FOLLOWING:
1.M9312 SWITCH SETTINGS FOR POWER-UP BOOT OR PUSH-BUTTON BOOT OF DEVICE.
2.THE START ADDRESS FOR THE CONSOLE LOAD AND START SEQUENCE.

DEVICE TO BE BOOTED	ROM LOC.	DIAG- INOSTIC	UNIT	START ADDR.	SWITCH SETTINGS S1-										SWR CODE
					1	2	3	4	5	6	7	8	9	10	
DUP-11	ROM 1	NO	0	173004	OFF	*	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	NA
DUP-11	ROM 1	YES	0	173006	OFF	*	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	012
DUP-11	ROM 1	NO	1	173030	OFF	*	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	NA
DUP-11	ROM 1	YES	1	173032	OFF	*	OFF	ON	OFF	OFF	OFF	OFF	ON	ON	012
DUP-11	ROM 2	NO	0	173204	OFF	*	ON	OFF	OFF	OFF	OFF	OFF	ON	OFF	NA
DUP-11	ROM 2	YES	0	173206	OFF	*	ON	OFF	OFF	OFF	OFF	OFF	ON	ON	212
DUP-11	ROM 2	NO	1	173230	OFF	*	ON	ON	OFF	OFF	OFF	OFF	ON	OFF	NA
DUP-11	ROM 2	YES	1	173232	OFF	*	ON	ON	OFF	OFF	OFF	OFF	ON	ON	212

* S1-2: WHEN ON,POWER-UP BOOT IS ENABLED;WHEN OFF,POWER-UP BOOT DISABLED.(MUST BE OFF FOR 11/24,/60.SEE 11/24,/60 DOCUMENTATION FOR POWER-UP BOOT)

NOTES

WHEN BOOTING FROM THE CONSOLE EMULATOR,A DEVICE MNEMONIC AND UNIT NUMBER ARE REQUIRED. IF UNIT NUMBER IS NOT ENTERED, IT IS ASSUMED TO BE ZERO,LISTED BELOW ARE THE DEVICE MNEMONIC AND UNIT NUMBERS SUPPORTED BY THIS ROM,AND THE DEVICE CSR ADDRESS ASSUMED BY THE BOOT CODE.

THE BOOT ROMS *** MUST ABSOLUTELY AND WITHOUT EXCEPTION *** BE INSTALLED IN SEQUENCE.
THAT IS ,23-865A9 THRU 23-867A9 IN BOOT ROM POSITIONS 1 THRU 3,OR IN BOOT ROM POSITIONS 2 THRU 4!!!

IF DIAGNOSTICS ARE TO BE RUN ,A CPU DIAGNOATIC ROM MUST BE IN LOCATION E20 ,AND JUMPER W8 MUST BE OUT.

DEVICE	MNEMONIC	UNIT	CSR
DUP-11	XW	0-16	ADDRESS AND VECTOR SET TO FLOATING ADDRESS AND VECTOR CONVENTION

TW

TABLE 3-4
ROM P/N 23-926A9,927A9,928A9

THE TABLE BELOW CONTAINS THE FOLLOWING:
1.M9312 SWITCH SETTINGS FOR POWER-UP BOOT OR PUSH-BUTTON BOOT OF DEVICE.
2.THE START ADDRESS FOR THE CONSOLE LOAD AND START SEQUENCE.

DEVICE TO BE BOOTED	ROM LOC.	DIAG- NOSTIC	UNIT	START ADDR.	SWITCH SETTINGS S1-										SWR CODE
					1	2	3	4	5	6	7	8	9	10	
DL11	ROM 1	NO	0	173004	OFF	*	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	NA
DL11	ROM 1	YES	0	173006	OFF	*	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	012
DL11	ROM 1	NO	1	173030	OFF	*	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	NA
DL11	ROM 1	YES	1	173032	OFF	*	OFF	ON	OFF	OFF	OFF	OFF	ON	ON	012
DL11	ROM 2	NO	0	173204	OFF	*	ON	OFF	OFF	OFF	OFF	OFF	ON	OFF	NA
DL11	ROM 2	YES	0	173206	OFF	*	ON	OFF	OFF	OFF	OFF	OFF	ON	ON	212
DL11	ROM 2	NO	1	173230	OFF	*	ON	ON	OFF	OFF	OFF	OFF	ON	OFF	NA
DL11	ROM 2	YES	1	173232	OFF	*	ON	ON	OFF	OFF	OFF	OFF	ON	ON	212

* S1-2: WHEN ON,POWER-UP BOOT IS ENABLED;WHEN OFF,POWER-UP BOOT DISABLED.(MUST BE OFF FOR 11/24,/60.SEE 11/24,/60 DOCUMENTATION FOR POWER-UP BOOT)

NOTES

WHEN BOOTING FROM THE CONSOLE EMULATOR,A DEVICE MNEMONIC AND UNIT NUMBER ARE REQUIRED. IF UNIT NUMBER IS NOT ENTERED, IT IS ASSUMED TO BE ZERO.LISTED BELOW ARE THE DEVICE MNEMONIC AND UNIT NUMBERS SUPPORTED BY THIS ROM,AND THE DEVICE CSR ADDRESS ASSUMED BY THE BOOT CODE.

THE BOOT ROMS *** MUST ABSOLUTELY AND WITHOUT EXCEPTION *** BE INSTALLED IN SEQUENCE.
THAT IS ,23-926A9 THRU 23-928A9 IN BOOT ROM POSITIONS 1 THRU 3,OR IN BOOT ROM POSITIONS 2 THRU 4!!!

IF DIAGNOSTICS ARE TO BE RUN ,A CPU DIAGNOATIC ROM MUST BE IN LOCATION E20 ,AND JUMPER W8 MUST BE OUT.

DEVICE	MNEMONIC	UNIT	CSR
DL11	XL	0-16	ADDRESS AND VECTOR SET TO FLOATING ADDRESS AND VECTOR CONVENTION

TW

REVISION HISTORY			VARIATIONS FOR THIS ASSY.		FIRST USED ON: M9312		DIGITAL EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS			
CHK	ECO NO	REV			MADE BY: B CRAMM	DATE: 1 AUG 78	TITLE			
					CHECKED: N POLLITT	DATE: 16 AUG 78	ROM LISTING DIAGNOSTIC			
					DSN,ENG.: B GIST	DATE: 1 AUG 78	SIZE	CODE	DOCUMENT NUMBER	REV
					PROD.: D PETERSON	DATE: 3 AUG 78	K	SP	M9312-0-5	D
					RESP,ENG.: E CROCKER	DATE: 1 AUG 78	ASS. #:		EDIT NO: 8	
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TW

IDENTIFICATION

PRODUCT NAME ROM LISTING DIAGNOSTIC (K-SP-M9312-0-5)

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SECTION 1

ROM 23-248F1

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1.0 OPERATIONAL NOTES

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TW

1.0 OPERATIONAL NOTES

1.1. OVERVIEW

THE M9312 IS DESIGNED TO PROVIDE BOOTSTRAPPING CAPABILITIES FOR ALL PDP-11 SYSTEMS WITH OR WITHOUT THE CONSOLE SWITCH REGISTER. IN ADDITION TO PROVIDING BOOTSTRAPPING FUNCTIONS FOR ALL MAJOR PDP-11 DEVICES, THE M9312 INCLUDES ROUTINES FOR CONSOLE EMULATION AND ALSO PROVIDES SOME BASIC CPU AND MEMORY GO-NOGO DIAGNOSTIC TESTS.

THIS BOOTSTRAP HAS BEEN DESIGNED FOR MAXIMUM FLEXIBILITY OF OPERATION. ITS FUNCTIONS MAY BE INITIATED AUTOMATICALLY AT A POWER UP, OR BY DEPRESSING THE CONSOLE BOOT SWITCH, OR BY A LOAD ADDRESS AND START SEQUENCE, OR EVEN BY USING THE CONSOLE TTY WHILE RUNNING THE CONSOLE EMULATOR.

1.2. INTERNAL SWITCH SETTING

A SET OF EIGHT MICRO SWITCHES ARE LOCATED ON THE M9312 MODULE. THESE ARE USED BY THE ROUTINES TO DETERMINE WHAT ACTION IS TO BE TAKEN. THEY GIVE THE USER AUTOMATIC ACCESS TO ANY FUNCTION.

A. POWER UP AND CONSOLE BOOT SWITCHES

THE PRIMARY ACTIVATING PROCESSES FOR THE M9312 PROGRAMS ARE EITHER A POWER UP SEQUENCE OR THE ENABLING OF THE CONSOLE BOOT SWITCH.

TO ACTIVATE THE M9312 ON A POWER UP, SWITCH 2 IN THE M9312 MICRO SWITCH REGISTER MUST BE IN THE ON POSITION. IF THIS SWITCH IS OFF THEN A NORMAL TRAP TO LOCATION 24 TO EXECUTE THE USER POWER UP ROUTINE WILL OCCUR. WHEN THIS SWITCH IS ON THE OTHER SWITCHES, 3 THROUGH 10, WILL DETERMINE WHAT ACTION THE M9312 WILL TAKE WHEN THE POWER UP OCCURS (SEE MICRO SWITCH SETTING BELOW).

IF THE SYSTEM INCLUDES A CONSOLE BOOT SWITCH THEN ANY TIME THAT SWITCH IS PRESSED THE M9312 WILL BE ACTIVATED (SOME PROCESSORS MAY HAVE TO BE HALTED FOR THIS SWITCH TO HAVE ANY EFFECT). THE PROCESS USED TO ENTER THE ROM IS A "FAKE" POWER DOWN FOLLOWED BY A POWER UP CAUSED BY PRESSING THE BOOT SWITCH (NOTE THAT THE POSITION OF MICRO SWITCH 2 DESCRIBED ABOVE IS IRRELEVANT TO THE OPERATION OF THIS BOOT SWITCH). THIS RESULTS IN A NORMAL POWER UP SEQUENCE IN THE CPU. PRIOR TO THE POWER UP SEQUENCE, THE M9312 ASSERTS 773000 ON THE UNIBUS ADDRESS LINES. THIS CAUSES THE NEW PC TO BE TAKEN FROM ROM LOCATION 773024 INSTEAD OF FROM LOCATION 000024. THE NEW PC WILL BE THE LOGICAL 'OR' OF THE CONTENTS OF ROM LOCATION 773024 AND THE EIGHT MICRO SWITCHES ON THE M9312 MODULE (A SWITCH IN THE ON POSITION IS SEEN AS A ONE; LIKEWISE A SWITCH IN THE OFF POSITION IS A ZERO).

TW

IN THIS WAY ALL THE M9312 OPTIONS ARE ACCESSABLE BY MERELY GIVING EACH OPTION A DIFFERENT STARTING ADDRESS. NOTE HERE THAT MICRO SWITCH NUMBER 10 IS OR'ED WITH BIT 1 OF THE DATA IN ROM LOCATION 773024, MICRO SWITCH NUMBER NINE IS OR'ED WITH BIT 2 ETC., AND THAT IT IS UNNECESSARY TO PROVIDE A SWITCH WHICH IS OR'ED WITH DATA BIT 0 AS THIS COULD RESULT IN AN ODD ADDRESS WHEN GOING THROUGH THE TRAP TO LOCATION = 773024 SEQUENCE.

B. THE MICRO SWITCH SETTINGS.

THE SETTING OF THE MICRO SWITCHS DEPENDS ON THE VARIOUS ROMS USED AND THE POSITION THEY ARE USED IN ON THE M9312.

1.3. CONSOLE EMULATOR

THESE ROUTINES ARE ESSENTIAL TO ANY PROCESSOR WITHOUT A CONSOLE. THEY PROVIDE THE USER THE CONSOLE FUNCTIONS OF LOAD ADDRESS, EXAMINE, DEPOSIT, AND START. ALSO THE ABILITY TO EXECUTE A BOOTSTRAP FUNCTION WITH ANY OF THE ABOVE DEVICES IS GIVEN.

THE FIRST THING THAT WILL EXECUTED (IF 020 IS THE CONTENTS OF THE MICRO SWITCHES) ARE THE PRIMARY CPU DIAGNOSTICS.

THEN THE DISPLAY ROUTINE IS ENTERED. THIS ROUTINE TYPE THE CONTENTS OF R0, R4, SP AND R5 (NOTE THE SEQUENCE!) ON THE TELETYPE AS FOUR 16 BIT OCTAL NUMBERS. PRESSING THE CONSOLE BOOT SWITCH CAUSES PDP-11 SYSTEMS (E.G. PDP-11/04'S) WITHOUT CONSOLE SWITCH REGISTERS TO COPY THE PC INTO R5 BEFORE THE POWER UP SEQUENCE STARTS.

A KEYBOARD DISPATCH ROUTINE IS THEN ENTERED TO INTERPRETE THE USERS COMMANDS. THIS ROUTINE TYPES A CARRIAGE RETURN AND A LINE FFED, THEN GIVES THE PROMPT '@'. ALL COMMANDS ARE TWO CHARACTERS. IF THE USER TYPES AN ILLEGAL COMMAND IT WILL BE IGNORED AND THE KEYBOARD DISPATCH IS RESTARTED. LEGAL COMMANDS ARE:

L<SPC>NUMBER

LOAD ADDRESS::LOAD THE INTERNAL ADDRESS POINTER WITH 'NUMBER', A 16 BIT OCTAL NUMBER.

E<SPC>

EXAMINE::EXAMINE AND DISPLAY ON THE TELETYPE THE ADDRESS AND THE CONTENTS OF THAT ADDRESS IN THE INTERNAL ADDRESS POINTER (SEE LOAD ADDRESS). NOTE THAT IF THE PREVIOUS COMMAND WAS ALSO AN EXAMINE COMMAND THEN THE INTERNAL ADDRESS POINTER IS INCREMENTED BY 2.

D<SPC>

DEPOSIT::DEPOSIT THE VALUE NUMBER INTO THE LOCATION POINTED TO BY THE INTERNAL ADDRESS POINTER (SEE LOAD ADDRESS). IF THE PREVIOUS COMMAND WAS ALSO DEPOSIT THEN THE POINTER IS INCREMENTED BY 2.

S<CR>

START::CAUSES A RESET INSTRUCTION TO BE EXECUTED AND A JMP TO THE LOCATION SPECIFIED IN THE INTERNAL ADDRESS POINTER.

TW

DP#
BOOT RP02 OR RP03::LOAD AND EXECUTE
THE MONITOR FROM THE DEVICE USING
THE DRIVE NUMBER OPTIONALLY
SPECIFIED BY # (DEFAULT 0) WITH OR
WITHOUT FIRST RUNNING SECONDARY CPU
AND MEMORY DIAGNOSTICS.

DB#
BOOT RP04/5/6 OR RM02/3::LOAD AND
EXECUTE THE MONITOR FROM THE DEVICE
USING THE DRIVE NUMBER OPTIONALLY
SPECIFIED BY # (DEFAULT 0) WITH OR
WITHOUT FIRST RUNNING SECONDARY CPU
AND MEMORY DIAGNOSTICS.

DS#
BOOT RS03 OR RS04::LOAD AND EXECUTE
THE MONITOR FROM THE DEVICE USING
THE DRIVE NUMBER OPTIONALLY
SPECIFIED BY # (DEFAULT 0) WITH OR
WITHOUT FIRST RUNNING SECONDARY CPU
AND MEMORY DIAGNOSTICS.

DK#
BOOT RK05 RK03/RK05J::LOAD AND
EXECUTE THE MONITOR FROM THE DEVICE
USING THE DRIVE NUMBER OPTIONALLY
SPECIFIED BY # (DEFAULT 0) WITH OR
WITHOUT FIRST RUNNING SECONDARY
CPU AND MEMORY DIAGNOSTICS.

DM#
BOOT RK06/RK07::LOAD AND EXECUTE THE
MONITOR FROM THE DEVICE USING THE
DRIVE NUMBER OPTIONALLY SPECIFIED BY
(DEFAULT 0) WITH OR WITHOUT FIRST
RUNNING SECONDARY CPU AND MEMORY
DIAGNOSTICS.

DX#
BOOT RX01::LOAD AND EXECUTE THE
MONITOR FROM THE DEVICE USING THE
DRIVE NUMBER OPTIONALLY SPECIFIED BY
WHICH MUST BE 0 OR 1 (DEFAULT 0)
WITH OR WITHOUT FIRST RUNNING
SECONDARY CPU AND MEMORY
DIAGNOSTICS.

DT#
BOOT TU56/TU55
LOAD AND EXECUTE THE
MONITOR FROM THE DEVICE USING THE
DRIVE NUMBER OPTIONALLY SPECIFIED BY
(DEFAULT 0) WITH OR WITHOUT FIRST
RUNNING SECONDARY CPU AND MEMORY
DIAGNOSTICS.

DY#
BOOT RX02::LOAD AND START THE
MONITOR FROM THE DEVICE USING THE
DRIVE NUMBER OPTIONALLY SPECIFIED BY
(DEFAULT 0) WITH OR WITHOUT FIRST
RUNNING SECONDARY CPU AND MEMORY
DIAGNOSTICS.

MT#
BOOT TU10 TE10,TS03
LOAD AND EXECUTE THE
MONITOR FROM THE DEVICE USING THE
DRIVE NUMBER OPTIONALLY SPECIFIED BY
(DEFAULT 0) WITH OR WITHOUT FIRST
RUNNING SECONDARY CPU AND MEMORY
DIAGNOSTICS.

MM#
BOOT TU16,TE16,TM02/3::
LOAD AND EXECUTE THE
MONITOR FROM THE DEVICE USING THE
DRIVE NUMBER OPTIONALLY SPECIFIED BY
(DEFAULT 0) WITH OR WITHOUT FIRST
SECONDARY CPU AND MEMORY
DIAGNOSTICS.

TT
BOOT DL11::READ THE ABSOLUTE PAPER
TAPE LOADER FROM THE TELETYPE PAPER
TAPE READER WITH OR WITHOUT FIRST
RUNNING THE SECONDARY CPU AND MEMORY
DIAGNOSTICS.

PR
BOOT PC11::READ THE ABSOLUTE PAPER
TAPE LOADER FROM THE HIGH SPEED
PAPER TAPE READER WITH OR WITHOUT
FIRST EXECUTING SECONDARY CPU AND
MEMORY DIAGNOSTICS.

DL#

BOOT RL11/RL01
LOAD AND EXECUTE THE
MONITOR FROM THE DEVICE USING THE
DRIVE NUMBER OPTIONALLY SPECIFIED BY
(DEFAULT 0) WITH OR WITHOUT FIRST
RUNNING SECONDARY CPU AND MEMORY
DIAGNOSTICS.

CT#

BOOT TU60:: LOAD AND EXECUTE THE
MONITOR FROM THE DEVICE USEING
THE DRIVE NUMBER OPTIONALLY
SPECIFIED BY # (DEFAULT 0) WITH OR
WITHOUT CPU AND MEMORY DIAGNOSTICS.

NOTE:: MORE DEVICES MAY BE ADDED AFTER THIS
DOCUMENT IS RELEASED. THE INSTALATION
DOCUMENT(K-SP-M9312-0-4)WILL BE UPDATED
AFTER EACH NEW ROM FOR A DEVICE WRITTEN
YOU MAY REFERENCE THAT DOCUMENT.

ALSO THE DIAGNOSTIC FOR THE M9312 WILL
TYPE OUT ALL NUMONICS WITHIN THE M9312.

TW

1.4. BOOTSTRAPPING

THESE ROUTINES TO BOOTSTRAP A DEVICE TYPICALLY READ IN THE FIRST SECTOR, BLOCK OR 512 (DEC) WORDS, OFF THE DEVICE INTO LOCATION 0 THROUGH 512 (DEC) OF MEMORY. THE EXCEPTIONS TO THIS RULE ARE THE PAPER TAPE BOOT, THE FLEXIBLE DISK BOOT AND THE MAGNETIC TAPE BOOTS. THE PAPER TAPE BOOT IS UNIQUE IN THAT IT CAN DO NO ERROR CHECKING AND THAT THE SECONDARY BOOTSTRAP (THE ABSOLUTE LOADER, FOR EXAMPLE) IS READ INTO THE UPPER PART OF MEMORY. THE ACTUAL LOCATION LOADED BY THE PAPER TAPE BOOT ARE PARTIALLY DETERMINED BY THE SECONDARY BOOTSTRAP ITSELF AND BY THE 'SIZE' ROUTINE WHICH DETERMINES THE HIGHEST AVAILABLE MEMORY ADDRESS WITHIN THE FIRST 28K. THE FLEXIBLE DISK (OR FLOPPY) READS SECTOR 1 ON TRACK 1 INTO LOCATIONS STARTING AT ZERO. THE MAGNETIC TAPE BOOTS READ THE SECOND BLOCK INTO LOCATIONS STARTING AT 0. IF NO ERRORS ARE DETECTED IN THE DEVICE, THE BOOTSTRAPS NORMALLY TRANSFER CONTROL TO LOCATION 0 IN ORDER TO EXECUTE THE SECONDARY BOOTSTRAP JUST LOADED. THE ONLY EXCEPTION TO THIS STARTING ADDRESS IS WITH THE PAPER TAPE BOOTS. THEY TRANSFER CONTROL TO LOCATION XXX374, WHERE XXX WAS DETERMINED INITIALLY BY THE SIZE ROUTINE TO BE AT THE TOP OF MEMORY; THIS IS WHERE THE ABSOLUTE LOADER WAS JUST LOADED.

IF A DEVICE ERROR IS DETECTED A RESET WILL BE EXECUTED AND THE BOOTSTRAP WILL TRY AGAIN. THE BOOTSTRAP WILL BE RETRIED INDEFINITELY UNTIL IT SUCCEEDS WITHOUT ERROR UNLESS THE USERS (OPERATOR) INTERVENES. THE ADVANTAGE OF RETRYING THE BOOT IS THAT IF A PARTICULAR DEVICE BEING BOOTED IS NOT ONLINE OR LOADED, SAY BECAUSE OF A POWER FAILURE RESTART, THE BOOT WILL GIVE THE DEVICE A CHANCE TO POWER UP (FOR DISKS THIS IS ESSENTIAL). A MAGNETIC TAPE TRANSPORT WILL NOT AUTOMATICALLY RELOAD ITSELF AFTER A POWER FAILURE AND RESTART. THIS SITUATION REQUIRES USER INTERVENTION. THE USER MUST RELOAD THE MAGTAPE AND BRING IT BACK ONLINE AT WHICH TIME THE MAGTAPE BOOTSTRAP, WHICH WAS CONTINUALLY ATTEMPTING TO BOOT THE TAPE, WILL SUCCEED.

NOTE:: AN EXCEPTION TO THIS RULE ARE DEVICE BOOTS FOR THE RK06/RK07 AND RX02.
 IN THE CASE OF THE RK06, IF A DRIVE TYPE ERROR IS ENCOUNTERED, THE DRIVE IS SET TO AN RK07.
 IN THE CASE OF AN RX02, FIRST DOUBLE DENSITY IS TRYED, SOULD WE GET A DENSITY ERROR ON READ TRY, WE CHANGE THE DENSITY TO SINGLE DENSITY. IN EITHER CASE, WE READ TWO (2) SECTORS OF DATA.
 SOME BOOTS ALLOW POWER-UP OR BOOT SWITCH BOOTING FOR DRIVES OTHER THAN DRIVE 0. REFER TO INDIVIDUAL BOOTS FOR THIS INFORMATION.

1.5. DIAGNOSTIC TESTS

THERE ARE THREE DIFFERENT TYPES OF TESTS INCLUDED IN THE M9312 :

- 1 PRIMARY CPU TESTS
- 2 SECONDARY CPU TESTS
- 3 MEMORY TEST

THE PRIMARY CPU TESTS ARE TESTS OF ALL UNARY AND DOUBLE OPERAND INSTRUCTIONS WITH ALL SOURCE MODES. THESE TESTS DO NOT MODIFY MEMORY. IF A FAILURE IS DETECTED A BRANCH DOT WILL BE EXECUTED.

THE SECONDARY CPU TESTS MODIFY MEMORY AND INVOLVE THE USE OF THE STACK POINTER. THESE TESTS INCLUDE TESTING OF THE JMP AND JSR INSTRUCTIONS AS WELL AS TESTS OF ALL DESTINATION MODES. IF A FAILURE IS DETECTED THESE TESTS, UNLIKE THE PRIMARY TESTS, WILL EXECUTE A HALT. THE USER MAY THEN CONSULT THIS LISTING TO DETERMINE THE FAULT CLASS FOR THE PARTICULAR LOCATION THE TEST HALTED.

FINALLY THE MEMORY TEST PERFORMS BOTH A DUAL ADDRESSING AND DATA CHECK OF ALL THE AVAILABLE MEMORY ON THE SYSTEM LESS THAN 28K. THIS TEST WILL LEAVE ALL OF MEMORY CLEAR. LIKE THE SECONDARY TESTS THE MEMORY TEST WILL HALT WHEN AN ERROR IS DETECTED. AT THE TIME THE MEMORY ERROR HALT IS EXECUTED R0 WILL CONTAIN THE ADDRESS AT WHICH THE FAILURE WAS DETECTED PLUS TWO! R4 WILL CONTAIN THE FAILING DATA PATTERN AND R6 WILL CONTAIN THE EXPECTED DATA PATTERN. THUS AFTER A MEMORY FAILURE HAS OCCURRED THE USER CAN ENTER THE CONSOLE EMULATOR AND HAVE THIS INFORMATION PRINTED OUT TO HIM IMMEDIATELY BY THE DISPLY ROUTINE (SEE ABOVE SECTION ON CONSOLE EMULATOR).

NOTE: HERE THAT DIAGNOSTICS ARE RUN OR NOT RUN (OPTIONALLY) DEPENDING ON WHETHER BIT 1 IS CLEAR OR SET (RESPECTIVELY) IN EITHER:

- 1 THE INTERNAL MICRO SWITCHES DESCRIBED ABOVE (IF THE POWER UP OR CONSOLE BOOT SWITCH METHOD IS USED); OR
- 2 THE CONSOLE SWITCH REGISTER (IF THE LOAD ADDRESS AND START WITH OPTION CODE IN SWITCHES METHOD DESCRIBED BELOW IS USED).

1.6. RESTARTING AT THE USER POWER FAIL ROUTINE

IF THE USER WISHES TO RESTART HIS OWN SOFTWARE ON A POWER UP HE MAY DO SO BY MERELY DISABLING THE POWER FAIL RESTART SWITCH IN THE MICRO SWITCHES (TURN SWITCH 2 OFF).

BUT THE USER CAN USE THE M9312 TO RUN DIAGNOSTICS (JUST THE PRIMARY CPU TESTS DESCRIBED ABOVE) BEFORE RUNNING HIS POWER UP ROUTINE. THIS WILL IN NO WAY DISTURB THE CONTENTS OF MEMORY AND WILL IN FACT VERIFY THE MACHINE'S BASIC INTEGRITY AFTER THE POWER DOWN AND UP SEQUENCE.

TO USE THIS OPTION PUT THE CODE 644 INTO THE MICRO SWITCHES AS DESCRIBED ABOVE. ALSO SWITCH 2 MUST BE OFF. THIS WILL RESULT IN THE RUNNING OF THE PRIMARY CPU DIAGNOSTICS AND THEN A SIMULATED TRAP THROUGH 24 WHICH WILL START THE USER'S SPECIFIED POWER UP ROUTINE.

IF THE CODE 646 IS PLACED IN THE INTERNAL SWITCHES THEN THE SIMULATED TRAP THROUGH 24 IS EXECUTED WITHOUT RUNNING ANY DIAGNOSTICS.

1.7. LOAD ADDRESS AND START PROCEDURE

ASCII CONSOLE AND DIAGNOSTIC ROM FOR USE WITH 11/04/05/10/20/34/35/40/45/50/55

FUNCTION TO BE BOOTED	ROM LOC.	DIAG- NOSTIC	MANUAL STARTING ADDR.
CONSOLE EMULATOR	E20	NO	165144
CONSOLE EMULATOR	E20	YES	165020

THE CONSOLE EMULATOR CAN PERFORM THE FOLLOWING FUNCTIONS:

- 1. LOAD ADDRESS
- 2. EXAMINE
- 3. DEPOSIT
- 4. START
- 5. BOOT A DEVICE

THE EXAMPLE BELOW CONTAINS THE START ADDRESS FOR EACH OF THE 4 ROM LOCATIONS REFERENCE THE INSTALLATION AND SET UP PROCEDURE (K-SP-M9312-0-4)FOR A COMPLETE LISTING

DEVICE TO BE BOOTED	ROM LOC.	DIAG- NOSTIC	UNIT	START ADDR.
RL01	ROM 1	NO	0	173004
RL01	ROM 1	YES	0	173006
RL01	ROM 2	NO	0	173204
RL01	ROM 2	YES	0	173206
RL01	ROM 3	NO	0	173404
RL01	ROM 3	YES	0	173406
RL01	ROM 4	NO	0	173604
RL01	ROM 4	YES	0	173606

2.0 PRIMARY CPU DIAGNOSTICS

2.1 COMMON DATA TABLE

2.2 TEST 1 SINGLE OPERAND INSTRUCTIONS

2.3 TEST 2 DOUBLEOPERAND INSTRUCTIONS, ALL SOURCE MODES, DEST MODE 0

2.4 TEST 3 JMP TEST MODES 1,2AND 3

2.5 TEST 4 SINGLE OPERAND, NON-MODIFYING INSTRUCTION, BYTE REFERENCING TEST

TW

2.1 THIS IS A TABLE OF DATA USED IN BOTH THE PRIMARY AND THE SECONDARY CPU DIAGNOSTICS.

165000	165000	POOL:	.WORD	POOL
165002	165000		.WORD	POOL
165004	100000	T4DATA:	.WORD	100000
165006	177777	T6DATA:	.WORD	177777
165010	165006		.WORD	T6DATA
165012	165006		.WORD	T6DATA
165014	000500	T6DAT1:	.WORD	500
165015	000501		.WORD	501

2.2 ***** TEST 1 SINGLE OPERAND INSTRUCTIONS *****

165020	005003	TEST1:	CLR	R3		000000	0100
165022	005203		INC	R3		000001	0000
165024	005103		COM	R3		177776	1001
165026	006203		ASR	R3		177777	1010
165030	006303		ASL	R3		177776	1001
165032	006003		ROR	R3		177777	1010
165034	005703		TST	R3		177777	1000
165036	005403		NEG	R3		000001	0001
165040	005303		DEC	R3		000000	0101
165042	005603		SBC	R3		177777	1001
165044	006103		ROL	R3		177777	1001
165046	005503		ADC	R3		000000	0101
165050	000303		SWAB	R3		000000	0100
165052	001377		BNE	.			

;ERROR IF NOT ZERO.

2.3 ***** TEST 2 DOUBLE OPERAND INSTRUCTIONS, ALL SOURCE MODES, DEST MODE 0. *****

165054	012702	165000	TEST2:	MOV	#POOL,R2	;SET UP ADDRESS.
165060	011203			MOV	(R2),R3	;MOVE FROM TABLE DEFERRED.
165062	022203			CMP	(R2)+,R3	;CHECK FOR CORRECT DATA.
165064	001377			BNE	.	;LOOP HERE IF NOT EQUAL.
165066	063203			ADD	@(R2)+,R3	;ADD TO REGISTER.
165070	165203			SUB	@-(R2),R3	;SUBTRACT SAME DATA FROM REGISTER.
165072	044203			BIC	-(R2),R3	;SHOULD CLEAR REGISTER.
165074	056203	000012		BIS	12(R2),R3	;SHOULD SET ALL REGISTER'S BITS.
165100	037203	000012		BIT	@12(R2),R3	;SHOULD TEST NOT ZERO (Z=0).
165104	001777			BEQ	.	;LOOP HERE ON ERROR.

2.4 ***** TEST 3 JMP TEST MODES 1, 2 AND 3. *****

165106	010703		TEST3:	MOV	PC,R3	;SET UP ADDRESS FOR MODE 1 JMP.
165110	000123		JMP1:	JMP	(R3)+	;EXECUTE JMP MODE 2.
165112	012703	165122		MOV	#JMP2A,R3	;SET UP ADDRESS OF ADDRESS FOR MODE 3 JMP.
165116	000133			JMP	@(R3)+	;EXECUTE JMP MODE 3.
165120	000113		JMP2:	JMP	(R3)	;EXECUTE MODE 1 JMP TO NEXT TEST.
165122	165120		JMP2A:	.WORD	JMP2	

2.5 ***** TEST 4 SINGLE OPERAND, NON-MODIFYING INSTRUCTION, BYTE REFERENCING TEST. *****

165124	105767	177654	TEST4:	TSTB	T4DATA	;TEST EVEN BYTE.
165130	001377			BNE	.	;LOOP ON ERROR, NOT ZERO.
165132	022222			CMP	(R2)+,(R2)+	;GET ADDRESS OF T4DATA IN R2.
165134	105722			TSTB	(R2)+	;EXAMINE DATA USING MODE 2.
165136	001377			BNE	.	;LOOP IF NOT ZERO.
165140	105712			TSTB	(R2)	;TST ODD BYTE MODE 1.
165142	100377			BPL	.	;LOOP IF POSITIVE.

ROM LISTING DIAGNOSTIC (K-SP-M9312-0-5)

3.0 CONSOLE FUNCTIONS

3.1 DISPLAY

3.2 START

3.3 DEPOSIT

3.4 LOAD ADDRESS

3.5 EXAINE

TW

3.0 CONSOLE FUNCTIONS

3.1 ***** DISPLAY *****

165144	010701	DSPLY:	MOV	PC,R1	
165146	000554		BR	PUTCR	;PRINT CR, LF AND FILLER CHARACTERS.
165150	010701		MOV	PC,R1	
165152	000526		BR	PUTNUM	;PRINT R0.
165154	010400		MOV	R4,R0	
165156	000524		BR	PUTNUM	;PRINT R4.
165160	010600	OUT:	MOV	SP,R0	
165162	010701		MOV	PC,R1	
165164	000521		BR	PUTNUM	;PRINT R6.
165166	010500		MOV	R5,R0	
165170	000517		BR	PUTNUM	;PRINT R5.
165172	010605		MOV	SP,R5	
165174	010701	CONSEM:	MOV	PC,R1	
165176	000540		BR	PUTCR	;PRINT CR, LF AND FILLER CHARACTERS.
165200	112702		MOVB	#100,R2	;44 (OCTAL) IS THE ASCII FOR '\$', THE
165204	010703		MOV	PC,R3	;COMMAND PROMPT CHARACTER.
165206	000554		BR	PUTCHR	
165210	010706	READ:	MOV	PC,SP	
165212	000544		BR	GETCHR	;GET THE FIRST CHARACTER OF A COMMAND.
165214	000302		SWAB	R2	
165216	000542		BR	GETCHR	;GET THE SECOND CHARACTER OF THE COMMAND.
165220	020227		CMP	R2,(PC)+	;LOAD ADDR. INSTRUCTION?
165222	046040		.ASCII	"L"	
165224	001450		BEQ	LA	
165226	020402		CMP	R4,R2	;EQUALS LAST COMMAND?
165230	001001		BNE	IS	;NO SKIP.
165232	005725		TST	(5)+	;YES-UPDATE ADDR. POINTER.
165234	010204	IS:	MOV	R2,R4	;RECORD THIS COMMAND.
165236	020227		CMP	R2,(PC)+	;IS CMMD A EXAM?
165240	042440		.ASCII	"E"	
165242	001446		BEQ	EX	;IF SO DO EXAM FUNCTION.
165244	020227		CMP	R2,(PC)+	;IS CMMD A DEPOSITE?
165246	042040		.ASCII	"D"	
165250	001432		BEQ	DE	;IF SO DO DEPOSITE FUNCTION.
165252	020227		CMP	R2,(PC)+	;IS IT A START COMMAND?
165254	051415		.ASCII	<CR>'S'	

3.0 CONSOLE FUNCTIONS

3.2 ***** START *****

165256	001002		BNE	2\$	
165260	000005		RESET		
165262	000115		JMP	(R5)	
165264	012704	173000	2\$: MOV	173000,R4	
165270	031427	000200	3\$: BIT	(R4),#200	;NO ROM?
165274	001323		BNE	DSPLY	;YEA,GO BACK,ABORT SEARCH.
165276	022402		CMP	(R4)+,R2	;MATCH ON BOOT HEADER VERSES CMMD?
165300	001405		BEQ	4\$;YES!--GO AHEAD.
165302	061404		ADD	(R4),R4	;NO-ADD INDEX TO GET TO NEW BOOT HEADER.
165304	020427	174000	CMP	R4, 174000	;HAVE WE EXCEEDED ROM RANGE?
165310	001731		BEQ	CONSEM	
165312	000766		BR	3\$;LOOP UNTILL MATCH OR TRAPS OUT.
165314	010701		4\$: MOV	PC,R1	
165316	000423		BR	GETNUM	
165320	000005		RESET		;INIT SYSTEM
165322	113705	173024	MOVB	#*INITSW,R5	;GET MICRO SWITCHES.
165326	106105		ROLB	R5	;ASSUMES HERE THAT THAE STARTING
165330	106105		ROLB	R5	;ADDR. OF DISPLY IS 165144
					;SO C BIT GETS SET.
165332	000164	000010	5\$: JMP	10(R4)	;GO DO BOOT.

3.3 ***** DEPOSIT *****

165336	010701		DE: MOV	PC,R1	
165340	000412		BR	GETNUM	;GET INPUT DATA.
165342	010015		MOV	R0,(R5)	;PUT INPUT DATA IN MEMORY.
165344	000713		BR	CONSEM	;RETURN FOR NEXT COMMAND.

3.4 ***** LOAD ADDRESS *****

165346	010701		LA: MOV	PC,R1	
165350	000406		BR	GETNUM	;GET INPUT DATA.
165352	010005		MOV	R0,R5	;LEAVE IT AS THE CURRENT ADDRESS
					;POINTER IN R5.
165354	005004		KBDCLR: CLR	R4	;CLEAR THE PREVIOUS COMMAND FLAG.
165356	000706		BR	CONSEM	;RETURN FOR NEXT COMMAND.

3.5 ***** EXAMINE *****

165360	010506		EX: MOV	R5,SP	;USE THE DISPLAY ROUTINE TO PRINT
165362	011505		MOV	(R5),R5	;OUT THE ADDRESS, R5, AND THE DATA IN THAT
165364	000675		BR	OUT	;ADDRESS, (R5).

TW

4.0 TTY HANDLERS

4.1 OCTAL NUMBER INPUT ROUTINE

4.2 OCTAL NUMBER OUTPUT ROUTINE

4.3 CR,LF, AND FILLER CHARACTER OUTPUT ROUTINE

4.4 CHARACTER INPUT ROUTINE

4.5 CHARACTER OUTPUT ROUTINE

4.6 REGISTER DISPLAY ROUTINE

TW

4.0 TTY HANDLERS

4.1 ***** OCTAL NUMBER INPUT ROUTINE *****

;THIS ROUTINE IS CALLED BY PLACING THE RETURN ADDRESS MINUS TWO
 ;IN R1 AND THEN BRANCHING TO GETNUM. THE ROUTINE WILL ATTEMPT TO
 ;INPUT A STRING OF CHARACTERS FROM THE TELETYPE, TERMINATED BY CR,
 ;AND ASSEMBLE THEM AS A 16 BIT OCTAL NUMBER IN R0. IF AN ILLEGAL
 ;CHARACTER IS TYPED IN THE STRING, NOT AN
 ;OCTAL DIGIT, THE CONSOLE EMULATOR WILL BE RESTARTED. THE PREVIOUS
 ;CONTENTS OF R2 AND R3 ARE LOST. THE ROUTINE WILL RETURN WITH THE
 ;OCTAL NUMBER IN R0, TO THE ADDRESS SPECIFIED IN R1 PLUS TWO.
 ;BUT NOTE THAT R1 WILL HAVE BEEN INCREMENTED BY FOUR UPON RETURN.

```

165366 005000
165370 005002
165372 010703
165374 000453
165376 120227 000015
165402 001433
165404 162702 000070
165410 062702 000010
165414 103357
165416 006300
165420 006300
165422 006300
165424 050200
165426 000700

```

```

GETNUM: CLR      R0
28:      CLR      R2
          MOV      PC,R3
          BR       GETCHR
          CMPB     R2,#CR
          BEQ      X1RTN
          SUB      #'0,R2
          ADD      #'0-'0,R2
          BCC      KBDCLR
          ASL      R0
          ASL      R0
          ASL      R0
          BIS      R2,R0
          BR       28

;INITIALIZE R0.
;INITIALIZE R2.
;GO GET A CHARACTER.

;IS IT CR?
;IF YES RETURN WITH THE NUMBER IN R0.
;IS THE CHARACTER A LEGAL OCTAL DIGIT?

;IF NOT GO RESTART THE CONSOLE EMULATOR.
;OTHERWISE ASSEMBLE THE NUMBER.

;LOOP BACK FOR NEXT CHARACTER.

```


4.0 TTY HANDLERS

4.2 ***** OCTAL NUMBER OUTPUT ROUTINE *****

;THIS ROUTINE, PUTNUM, IS CALLED BY PLACING THE RETURN ADDRESS
 ;MINUS TWO IN R1 AND THE 16 BIT OCTAL NUMBER TO BE TYPED
 ;IN R0. PUTNUM WILL TYPE 6 CHARCTERS COMPRISING THE OCTAL DIGITS
 ;OF THE NUMBER IN R0 FOLLOWED BY ONE SPACE CHARACTER. THE PREVIOUS
 ;CONTENTS OF R2 AND R3 ARE LOST. RETURN IS MADE TO THE ADDRESS
 ;IN R1 PLUS TWO, BUT R1 IS INCREMENTED BY FOUR.

165430 012702
 165432 000030
 165434 000261
 165436 006100
 165440 106102
 165442 010703
 165444 000435
 165446 012702
 165450 206
 165451 040
 165452 006300
 165454 001403
 165456 106102
 165460 103774
 165462 000765
 165464 000302
 165466 010703
 165470 000423
 165472 022121
 165474 000151 177776

PUTNUM: MOV (PC)+,R2 ;COMPUTE FIRST DIGIT.
 .WORD <'0>/2
 SEC
 2S: ROL R0 ;SHIFT NUMBER INTO R2 TO COMPUTE NEXT CHARACTER.
 ROLB R2
 MOV PC,R3 ;PRINT CHARACTER.
 BR PUTCHR
 MOV (PC)+,R2 ;GET READY TO COMPUTE NEXT CHARACTER.
 .BYTE 200!<'0/10>
 .BYTE <'>
 4S: ASL R0 ;SHIFT NUMBER AND SEE IF DONE.
 BEQ 6S ;BRANCH IF DONE.
 ROLB R2
 BCS 4S
 BR 2S
 6S: SWAB R2 ;WHEN DONE COME HERE TO PRINT SPACE.
 MOV PC,R3
 BR PUTCHR
 X1RTN: CMP (R1)+,(R1)+ ;AND RETURN.
 JMP -2(R1)

4.3 ***** CR, LF AND FILLER CHARACTER OUTPUT ROUTINE *****

;THIS ROUTINE IS CALLED TO TYPE A CARRIAGE RETURN, LINE FEED FOLLOWED
 ;BY 12 FILLER CHARACTERS. THE CALL IS MADE BY FIRST PLACING THE RETURN
 ;ADDRESS MINUS TWO IN R1 AND EXECUTING BR PUTCR.
 ;THE PREVIOUS CONTENTS OF BOTH REGISTERS R2 AND R3 ARE LOST.
 ;WHEN FINISHED THIS SUBROUTINE WILL RETURN TO THE ADDRESS SPECIFIED
 ;IN R1 PLUS TWO, BUT R1 WILL BE INCREMENTED BY FOUR.

165500 012702
 165502 014012
 165504 010703
 165506 000414
 165510 061702
 165512 003767
 165514 105002
 165516 152702 000015
 165522 000770

PUTCR: MOV (PC)+,R2
 .WORD 14012
 1S: MOV PC,R3
 BR PUTCHR
 ADD (PC),R2
 BLE X1RTN
 CLRB R2
 BISB *CR,R2
 BR 1S

4.0 TTY HANDLERS

4.4 ***** CHARACTER INPUT ROUTINE *****

;THIS ROUTINE IS CALLED TO BOTH INPUT AND ECHO A CHARACTER FROM
 ;THE TTY. THE CHARACTER IS SAVED IN THE LOW BYTE OF R2. THE
 ;HIGH BYTE OF R2 IS NOT MODIFIED. A CALL TO THIS
 ;SUBROUTINE IS MADE BY FIRST PLACING THE RETURN ADDRESS MINUS 2 IN R3
 ;AND THEN EXECUTING A BRANCH TO GETCHR. WHEN FINISHED
 ;A RETURN WILL BE MADE TO THE ADDRESS SPECIFIED IN R3 PLUS TWO, BUT
 ;R3 WILL HAVE BEEN INCREMENTED BY FOUR.

165524	105737	177560	GETCHR: TSTB	@TKS	;WAIT FOR KEYBOARD INPUT, READY.
165530	100375		BPL	GETCHR	
165532	105002		CLRB	R2	;CLEAR THE LOW BYTE OF R2.
165534	153702	177562	BISB	@TKB,R2	;PLACE THE CHARACTER IN THE LOW BYTE OF R2.
					;PROCEED ON TO PUTCHR IN ORDER TO
					;ECHO THE CHARACTER IN THE LOW BYTE
					;OF R2.

4.5 ***** CHARACTER OUTPUT ROUTINE *****

;THIS SUBROUTINE IS CALLED TO PRINT A CHARACTER. THE CHARACTER
 ;MUST BE PLACED IN THE LOW ORDER BYTE OF R2. TO CALL THIS ROUTINE
 ;PLACE THE RETURN ADDRESS MINUS TWO IN R3 AND BRANCH TO
 ;PUTCHR. THE CONTENTS OF R2 ARE NOT MODIFIED. RETURN IS MADE
 ;TO THE ADDRESS SPECIFIED IN R3 PLUS TWO, BUT R3 IS LEFT INCREMENTED
 ;BY FOUR.

165540	105737	177564	PUTCHR: TSTB	@TPS	;WAIT FOR PRINTER READY.
165544	100375		BPL	PUTCHR	
165546	110237	177566	MOVB	R2,@TPB	;WHEN READY PRINT THE CHARACTER.
165552	142702	100200	BICB	*100200,R2	;CLEAR ANY PARITY BITS THAT MAY BE SET.
					;THIS ROUTINE IS USED TO MAKE RETURNS FROM SUBROUTINES WHICH USE
					;R3 AS AN ADDRESS LINK. THOSE SUBROUTINES ARE CALLED
					;BY PLACING THE RETURN ADDRESS MINUS 2 IN R3. WHEN THE SUBROUTINE
					;IS FINISHED PROCESSING IT WILL BRANCH TO X3RTN. X3RTN
					;WILL INCREMENT R3 BY FOUR BUT RETURN TO THE ADDRESS SPECIFIED IN R3
					;PLUS TWO.
165556	022323		X3RTN: CMP	(R3)+,(R3)+	;INCREMENT R3 BY 4.
165560	000163	177776	JMP	-2(R3)	;RETURN TO THE ADDRESS WHICH WAS
					;ORIGINALLY IN R3 PLUS TWO.

4.6 ***** REGISTER DISPLAY ROUTINE *****

;DSPLY IS THE FIRST PART OF THE CONSOLE EMULATOR THAT IS EXECUTED.
 ;IT WILL PRINT THE CONTENTS OF R0, R4, R6 AND R5 (IN THAT ORDER) AS
 ;FOUR SIXTEEN BIT OCTAL NUMBERS ON THE TTY. NOTE THAT ON SOME ELEVEN
 ;SYSTEMS (E.G. THE 11/04) WHEN THE BOOT SWITCH IS DEPRESSED AND
 ;THE PROCESS OF BOOTING INITIATED THE PC WILL BE PLACED INTO R5.

TW

5.0 SECONDARY CPU DIAGNOSTICS

5.1 DOUBLE OPERAND, MODIFYING INSTRUCTIONS, BYTE REFERENCE TEST

5.2 JSR TEST WITH MODES 1 AND 6

TW

5.0 SECONDARY CPU DIAGNOSTICS

;THESE ARE THE MEMORY MODIFYING TESTS. THEY ARE RUN AS SUBROUTINE
 ;WHICH IS CALLED BY PLACING THE RETURN ADDRESS IN THE CALLING
 ;ROUTINE MINUS TWO IN R1. THE PREVIOUS CONTENTS OF R2,
 ;R3, R5 AND R6 ARE LOST. IF ANY OF THESE TESTS DETECTS AN ERROR
 ;A HALT WILL BE EXECUTED. THE USER CAN THEN CONSULT THIS LISTING
 ;FOR FURTHER INFORMATION ABOUT THE FAULT. ISSUING A
 ;CONTINUE FUNCTION WILL NOT BE MEANINGFUL AFTER
 ;ANY OF THESE TESTS DETECTS AN ERROR AND HALTS. NOTE THAT
 ;WHEN THE MEMORY TEST DETECTS A FAILURE AND HALTS CERTAIN
 ;IMPORTANT PARAMETERS USED IN THAT TEST WILL BE SAVED IN THE
 ;REGISTERS. THESE REGISTERS ARE INCLUDED IN THOSE WHICH ARE
 ;DISPLAYED WHEN THE CONSOLE EMULATOR PORTION OF THIS ROM
 ;IS INITIATED. SO THAT IF A MEMORY ERROR IS DETECTED THE USER
 ;CAN START THE CONSOLE EMULATOR TO EASILY ACCESS THIS MEMORY
 ;ERROR DATA. CAUTION SHOULD BE OBSERVED WHEN SELECTING THESE
 ;TESTS TO BE RUN. THEY WILL DESTROY THE PREVIOUS CONTENTS
 ;OF ANY MAIN MEMORY AVAILABLE UP TO 28K WORDS.

5.1 ***** DOUBLE OPERAND, MODIFYING INSTRUCTIONS, BYTE REFERENCE TEST. *****

165564	012705	165006	TEST6:	MOV	#T6DATA,R5	;SET UP TEST DATA ADDRESS.
165570	012702	000500		MOV	#500,R2	;SET UP DEST ADDRESS.
165574	011503			MOV	(R5),R3	;SET UP CMP OPERAND FOR TEST.
165576	005012			CLR	(R2)	;CLR 500.
165600	112512			MOVB	(R5)+,(R2)	;500=000377.
165602	005202			INC	R2	;POINTER TO UPPER BYTE, 501.
165604	112512			MOVB	(R5)+,(R2)	;500=177777.
165606	005302			DEC	R2	;MOVE POINTER BACK TO LOW BYTE.
165610	023512			CMP	@(R5)+,(R2)	;CHECK FOR ALL ONES.
165612	001015			BNE	T6ERR	
165614	005202			INC	R2	;MOVE POINTER UP TO ODD BYTE.
165616	143522			BICB	@(R5)+,(R2)+	;CLEAR HIGH BYTE OF LOCATION 500.
165620	024542			CMP	-(R5),-(R2)	;MOVE POINTERS BACK.
165622	143522			BICB	@(R5)+,(R2)+	;CLEAR LOW BYTE OF LOCATION 500.
165624	001010			BNE	T6ERR	;BRANCH IF NOT ZERO.
165626	010502			MOV	R5,R2	;GET DEFERRED ADDRESS OF 500 INTO R2.
165630	016505	177772		MOV	-6(R5),R5	;GET TEST DATA.
165634	110532			MOVB	R5,@(R2)+	;500 SHOULD BE 000377.
165636	150572	000000		BISB	R5,@(R2)	;SET UPPER BITS.
165642	020352			CMP	R3,@-(R2)	;CHECK FOR ALL ONES, 177777.
165644	001407			BEQ	TEST7	;IF NO ERROR GO TO NEXT TEST.
165646	000000		T6ERR:	HALT		

5.0 SECONDARY CPU DIAGNOSTICS

5.2 ***** JSR TEST WITH MODES 1 AND 6. *****

165650	005723		TSTJSR: TST	(R3)+	;R3 SHOULD POINT TO ZERO WORD AT T7ERR.
165652	001011			BNE T7ERR	;IF NOT THEN HALT ON ERROR.
165654	021605			CMP (SP),R5	;SP SHOULD POINT TO 177777.
165656	001007			BNE T7ERR	;IF NOT THEN HALT ON ERROR.
165660	000203			RTS R3	
165662	000000			HALT	
165664	011206		TEST7: MOV	(R2),SP	;SET UP STACK TO START AT 502.
165666	012702	165650		MOV #TSTJSR,R2	;SET UP ADDRESS FOR JSR.
165672	005726			TST (SP)+	;MOVE SP UP ONE WORD.
165674	004312			JSR R3,(R2)	;EXECUTE JSR TO TSTJSR.
165676	000000		T7ERR: HALT		
165700	004362	000004		JSR R3,4(R2)	;EXECUTE JSR TO TSTJSR+4.

6.0 MEMORY DIAGNOSTIC AND SIZE ROUTINES

TW

6.0 MEMORY DIAGNOSTIC AND SIZE ROUTINES

;THIS ROUTINE PERFORMS BOTH A DUAL ADDRESSING TEST AND A RUDIMENTARY
;DATA INTEGRITY TEST OF ANY MEMORY AVAILABLE UP TO 28K WORDS.
;FIRST EVERY LOCATION IS WRITTEN WITH ITS OWN ADDRESS, STARTING
;FROM LOCATION 0 AND WORKING UP. THEN AFTER EVERY LOCATION HAS
;BEEN WRITTEN WITH ITS OWN ADDRESS, THE ROUTINE RETURNS TO LOCATION
;0 AND NEGATES ITS CONTENTS. THEN THE
;ADDRESS OF THE LOCATION WHICH WAS JUST NEGATED IS ADDED TO
;THAT LOCATION. THE RESULT SHOULD BE ZERO. THE PROCESS IS CONTINUED
;FROM 0 TO THE TOP OF MEMORY. IF NO ERRORS ARE DETECTED MEMORY
;WILL BE LEFT FILLED WITH ZEROES. IF AN ERROR IS DETECTED THEN:
; 1 THE ADDRESS BEING TESTED IS LEFT IN R4
; 2 THE EXPECTED DATA FROM THAT LOCATION IS IN R6
; 3 THE FAILING DATA IS IN R0
; 4 FINALLY THE HALT AT LOCATION 165776 IN THIS
; ROM IS EXECUTED.

165704				MENTST:		
165704	012705	160000		SIZE:	MOV	#160000,R5 ;SET UP R5.
165710	005037	000006			CLR	#6 ;SET UP TRAP VECTOR 4.
165714	012737	165722	000004		MOV	#18,0#4
165722	012706	000502		18:	MOV	#522,SP ;SET UP THE STACK POINTER.
165726	005745				TST	-(R5) ;MAKE THE REFERENCE AND DECREMENT R5.
165730	005003				CLR	R3 ;R3 IS A POINTER USED TO READ AND WRITE MEMORY.
165732	010313			26:	MOV	R3,(R3) ;WRITE THE CONTENTS OF R3 INTO THE LOCATION
						;ADDRESSED BY R3.
165734	005723				TST	(R3)+ ;INCREMENT R3 BY 2.
165736	020305				CMP	R3,R5 ;R5 CONTAINS THE LAST AVAILABLE MEMORY
						;ADDRESS UNDER 28K WORDS. SEE IF
						;THE END OF MEMORY HAS BEEN REACHED.
165740	101774				BLOS	28 ;LOOP UNTIL DONE.
165742	005003				CLR	R3 ;RETURN R3 TO LOCATION 0.
165744	005413			48:	NEG	(R3) ;NEGATE THE LOCATION REFERENCED BY R3.
165746	060313				ADD	R3,(R3) ;ADD THE CONTENTS OF R3.
165750	005723				TST	(R3)+ ;INCRMENT THE POINTER, R3, BY 2; AND SEE IF THE
						;RESULT OF THE ADDITION WAS 0.
165752	001004				BNE	MEMERR ;IF NOT 0, THEN AN ERROR HAS OCCURRED.
165754	020305				CMP	R3,R5 ;OTHERWISE CONTINUE UP UNTIL THE TOP
						;OF MEMORY IS REACHED.
165756	101772				BLOS	48
165760	000164	000002		ENDIST:	JMP	2(R4)

;RESULT IN A TRAP THEN RETURN
;WITH THE HIGHEST MEMORY ADDRESS
;AVAILABLE IN R5.

;IF A MEMORY ERROR IS DETECTED COME HERE TO SAVE IMPORTANT
;PARAMETERS IN THE REGISTERS AND HALT.

165764	014304			MEMERR:	MOV	-(R3),R4	
165766	010300				MOV	R3,R0	
165770	005006				CLR	SP	
165772	000000				HALT		
165774	040460				.ASCII	"0A"	;IDENTIFIES ROM AS "A0" OR A VERSION 0 ECB 12-12-77
1012	165776	123162			.WORD	123162	;CRC WORD FOR LAST 255. WORDS.
1013		000001			.END		

TW

248F1.P11 SYMBOL TABLE

BIT8 = 000400	BIT9 = 001000	CONSEM 165174	CR = 000015
CRCWD = 200000	DE 165336	DIAG = 165564	DL11CR= 177560
DSPLY 165144	ENDTST 165760	EX 165360	GETCHR 165524
GETNUM 165366	HBOOT 165000	HSRCR = 177550	INITSW= 173024
JMP1 165110	JMP2 165120	JMP2A 165122	KBDCLR 165354
LA 165346	LF = 000012	MEMERR 165764	MEMTST 165704
MPRESER= 173000	OUT 165160	PC =%000007	PC11CR= 177550
PDIAG 165564	POOL 165000	PSW = 177776	PUICHR 165540
PUICR 165500	PUTNUM 165430	READ 165210	RESERV= 000340
RK05CR= 177404	RK06CR= 177440	RL01CR= 174400	RP03CR= 176714
RP04CR= 176700	RS03CR= 172040	RS04CR= 172040	RX01CR= 177170
RX02CR= 177170	R0 =%000000	R1 =%000001	R2 =%000002
R3 =%000003	R4 =%000004	R5 =%000005	R6 =%000006
R7 =%000007	SIZE 165704	SP =%000006	SNR = 177570
TEST1 165020	TEST2 165054	TEST3 165106	TEST4 165124
TEST6 165564	TEST7 165664	TKB = 177562	TKS = 177560
TPB = 177566	TPS = 177564	TSTJSR 165650	TTCR = 177560
TU10CR= 172522	TU16CR= 172440	TU56CR= 177342	T4DATA 165004
T6DATA 165006	T6DAT1 165014	T6ERR 165646	T7ERR 165676
X1PTN 165472	X3RTN 165556	. = 166000	

SECTION 2

ROM 23-616F1

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TEST4 TEST "ROR", MODE "0", AND "BVC", "BHS", "BNE"
TEST5 TEST REGISTER DATA PATH
TEST6 TEST "ROL", "BCC", "BLT"
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TW

OPERATIONAL NOTES

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 - A. POWER UP AND CONSOLE BOOT SWITCHES
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OPERATIONAL NOTES

1. OVERVIEW

THE M9312 IS DESIGNED TO PROVIDE BOOTSTRAPPING CAPABILITIES FOR ALL PDP-11 SYSTEMS WITH OR WITHOUT THE CONSOLE SWITCH REGISTER. IN ADDITION TO PROVIDING BOOTSTRAPPING FUNCTIONS FOR ALL MAJOR PDP-11 DEVICES, THE M9312 INCLUDES ROUTINES FOR SOME BASIC CPU AND MEMORY GO-NOGO DIAGNOSTIC TESTS.

THIS BOOTSTRAP HAS BEEN DESIGNED FOR MAXIMUM FLEXIBILITY OF OPERATION. ITS FUNCTIONS MAY BE INITIATED AUTOMATICALLY AT A POWER UP, OR BY DEPRESSING THE CONSOLE BOOT SWITCH, OR BY A LOAD ADDRESS AND START SEQUENCE.

2. INTERNAL SWITCH SETTING

A SET OF EIGHT MICRO SWITCHES ARE LOCATED ON THE M9312 MODULE. THESE ARE USED BY THE ROUTINES TO DETERMINE WHAT ACTION IS TO BE TAKEN. THEY GIVE THE USER AUTOMATIC ACCESS TO ANY FUNCTION.

A. POWER UP AND CONSOLE BOOT SWITCHES

THE PRIMARY ACTIVATING PROCESSES FOR THE M9312 PROGRAMS ARE EITHER A POWER UP SEQUENCE OR THE ENABLING OF THE CONSOLE BOOT SWITCH.

TO ACTIVATE THE M9312 ON A POWER UP, SWITCH 2 IN THE M9312 MICRO SWITCH REGISTER MUST BE IN THE ON POSITION. IF THIS SWITCH IS OFF THEN A NORMAL TRAP TO LOCATION 24 TO EXECUTE THE USER POWER UP ROUTINE WILL OCCUR. WHEN THIS SWITCH IS ON THE OTHER SWITCHES, 3 THROUGH 10, WILL DETERMINE WHAT ACTION THE M9312 WILL TAKE WHEN THE POWER UP OCCURS (SEE MICRO SWITCH SETTING BELOW).

IF THE SYSTEM INCLUDES A CONSOLE BOOT SWITCH THEN ANY TIME THAT SWITCH IS PRESSED THE M9312 WILL BE ACTIVATED (SOME PROCESSORS MAY HAVE TO BE HALTED FOR THIS SWITCH TO HAVE ANY EFFECT). THE PROCESS USED TO ENTER THE ROM IS A "FAKE" POWER DOWN FOLLOWED BY A POWER UP CAUSED BY PRESSING THE BOOT SWITCH (NOTE THAT THE POSITION OF MICRO SWITCH 2 DESCRIBED ABOVE IS IRRELEVANT TO THE OPERATION OF THIS BOOT SWITCH). THIS RESULTS IN A NORMAL POWER UP SEQUENCE IN THE CPU. PRIOR TO THE POWER UP SEQUENCE, THE M9312 ASSERTS 773000 ON THE UNIBUS ADDRESS LINES. IN THE CASE OF THE 11/60, THE PROCESSOR ASSERTS 000224 ON THE BUS, WHICH IS ORED WITH THE 773000 ASSERTED BY THE M9312. THE 11/70 ASSERTS THE ENTIRE ADDRESS ON THE UNIBUS AS A FUNCTION OF JUMPER SETTINGS (SEE OR M9312 USER MANUAL.) THE NEW PC IS DETERMINED BY ROM LOCATION 773024 OR 773224 (WITH THE 11/60) INSTEAD OF FROM LOCATION 000024. THE NEW PC WILL BE THE LOGICAL "OR" OF THE CONTENTS OF ROM LOCATION 773024 AND THE EIGHT MICRO SWITCHES ON THE M9312 MODULE (A SWITCH IN THE ON POSITION IS SEEN AS A ONE; LIKEWISE A SWITCH IN THE OFF POSITION IS A ZERO).

IN THIS WAY ALL THE M9312 OPTIONS ARE ACCESSABLE BY MERELY GIVING EACH OPTION A DIFFERENT STARTING ADDRESS. NOTE HERE THAT MICRO SWITCH NUMBER 10 IS OR'ED WITH BIT 1 OF THE DATA IN ROM LOCATION 773024, MICRO SWITCH NUMBER NINE IS OR'ED WITH BIT 2 ETC., AND THAT IT IS UNNECESSARY TO PROVIDE A SWITCH WHICH IS OR'ED WITH DATA BIT 0 AS THIS COULD RESULT IN AN ODD ADDRESS WHEN GOING THROUGH THE TRAP TO LOCATION 773024 SEQUENCE.

B.OPTIONS AND THE MICRO SWITCH SETTINGS.

THE SETTING OF THE MICRO SWITCHS DEPENDS ON THE VARIOUS ROMS ON THE M9312 AND THE DEVICE BOOTS POSTION ON THE M9312.

3. BOOTSTRAPPING

THESE ROUTINES TO BOOTSTRAP A DEVICE TYPICALLY READ IN THE FIRST SECTOR, BLOCK OR 512 (DEC) WORDS, OFF THE DEVICE INTO LOCATION 0 THROUGH 512 (DEC) OF MEMORY. THE EXCEPTIONS TO THIS RULE ARE THE PAPER TAPE BOOT, THE FLEXIBLE DISK BOOT AND THE MAGNETIC TAPE BOOTS. THE PAPER TAPE BOOT IS UNIQUE IN THAT IT CAN DO NO ERROR CHECKING AND THAT THE SECONDARY BOOTSTRAP (THE ABSOLUTE LOADER, FOR EXAMPLE) IS READ INTO THE UPPER PART OF MEMORY. THE ACTUAL LOCATIONS LOADED BY THE PAPER TAPE BOOT ARE PARTIALLY DETERMINED BY THE SECONDARY BOOTSTRAP ITSELF AND BY THE 'SIZE' ROUTINE WHICH DETERMINES THE HIGHEST AVAILABLE MEMORY ADDRESS WITHIN THE FIRST 28K. THE FLEXIBLE DISK (OR FLOPPY) READS SECTOR 1 ON TRACK 1 INTO LOCATIONS STARTING AT ZERO. THE MAGNETIC TAPE BOOTS READ THE SECOND BLOCK INTO LOCATIONS STARTING AT 0. IF NO ERRORS ARE DETECTED IN THE DEVICE, THE BOOTSTRAPS NORMALLY TRANSFER CONTROL TO LOCATION 0 IN ORDER TO EXECUTE THE SECONDARY BOOTSTRAP JUST LOADED. THE ONLY EXCEPTION TO THIS STARTING ADDRESS IS WITH THE PAPER TAPE BOOTS. THEY TRANSFER CONTROL TO LOCATION XXX374, WHERE XXX WAS DETERMINED INITIALLY BY THE SIZE ROUTINE TO BE AT THE TOP OF MEMORY; THIS IS WHERE THE ABSOLUTE LOADER WAS JUST LOADED.

IF A DEVICE ERROR IS DETECTED A RESET WILL BE EXECUTED AND THE BOOTSTRAP WILL TRY AGAIN. THE BOOTSTRAP WILL BE RETRIED INDEFINITELY UNTIL IT SUCCEEDS WITHOUT ERROR UNLESS THE USER (OPERATOR) INTERVENES. THE ADVANTAGE OF RETRYING THE BOOT IS THAT IF A PARTICULAR DEVICE BEING BOOTED IS NOT ONLINE OR LOADED, SAY BECAUSE OF A POWER FAILURE RESTART, THE BOOT WILL GIVE THE DEVICE A CHANCE TO POWER UP (FOR DISKS THIS IS ESSENTIAL). A MAGNETIC TAPE TRANSPORT WILL NOT AUTOMATICALLY RELOAD ITSELF AFTER A POWER FAILURE AND RESTART. THIS SITUATION REQUIRES USER INTERVENTION. THE USER MUST RELOAD THE MAGTAPE AND BRING IT BACK ONLINE AT WHICH TIME THE MAGTAPE BOOTSTRAP, WHICH WAS CONTINUALLY ATTEMPTING TO BOOT THE TAPE, WILL SUCCEED.

TW

NOTE: AN EXCEPTION TO THIS RULE ARE DEVICE BOOTS FOR THE RK06/RK07 AND RX02.
 IN THE CASE OF THE RK06, IF A DRIVE TYPE ERROR IS ENCOUNTERED, THE DRIVE IS SET TO AN RK07.
 IN THE CASE OF AN RX02, FIRST DOUBLE DENSITY IS TRYED, SOULD WE GET A DENSITY ERROR ON READ TRY, WE CHANGE THE DENSITY TO SINGLE DENSITY. IN EITHER CASE, WE READ TWO (2) SECTORS OF DATA.

SOME BOOTS ALLOW POWER-UP OR BOOT SWITCH BOOTING FOR DRIVES OTHER THAN DRIVE 0. REFER TO INDIVIDUAL BOOTS FOR THIS INFORMATION.

4. DIAGNOSTIC TESTS

THERE ARE THREE DIFFERENT TYPES OF TESTS INCLUDED IN THE M9312 :

- 1 PRIMARY CPU TESTS
- 2 SECONDARY CPU TESTS
- 3 MEMORY TEST
- 4 CACHE TESTS

THE PRIMARY CPU TESTS ARE TESTS OF MOST UNARY AND DOUBLE OPERAND INSTRUCTIONS WITH MOST SOURCE MODES. THESE TESTS DO NOT MODIFY MEMORY. IF A FAILURE IS DETECTED A HALT WILL OCCUR.

THE SECONDARY CPU TESTS MODIFY MEMORY AND INVOLVE THE USE OF THE STACK POINTER. THESE TESTS INCLUDE TESTING OF THE JMP AND JSR INSTRUCTIONS AS WELL AS TESTS OF ALL DESTINATION MODES. IF A FAILURE IS DETECTED THESE TESTS WILL ALSO EXECUTE A HALT. THE USER MAY THEN CONSULT THIS LISTING TO DETERMINE THE FAULT CLASS FOR THE PARTICULAR LOCATION THE TEST HALTED.

THE MEMORY TEST PERFORMS BOTH A DUAL ADDRESSING AND DATA CHECK OF ALL THE AVAILABLE MEMORY ON THE SYSTEM LESS THAN 20K. THIS TEST WILL CHANGE ALL OF MEMORY TESTED. LIKE THE SECONDARY TESTS THE MEMORY TEST WILL HALT WHEN AN ERROR IS DETECTED. AT THE TIME THE MEMORY ERROR HALT IS EXECUTED R0 WILL CONTAIN THE ADDRESS AT WHICH THE FAILURE WAS DETECTED. R1 WILL CONTAIN THE FAILING DATA PATTERN AND R0 WILL CONTAIN THE EXPECTED DATA PATTERN.

FINALLY THERE ARE TWO CACHE TESTS WHICH DETERMINE CPU TYPE (11/60 OR 11/70) AND TEST CACHE CONTROLS, DATA INTEGRITY AND MEMORY VIA CACHE. FOR DETAILS, SEE TESTS 16 AND 17 OF THE PROGRAM LISTING.

TW

NOTE: HERE THAT DIAGNOSTICS ARE RUN OR NOT RUN (OPTIONALLY) DEPENDING ON WHETHER BIT 1 IS CLEAR OR SET (RESPECTIVELY) IN EITHER:

- 1 THE INTERNAL MICRO SWITCHES DESCRIBED ABOVE (IF THE POWER UP OR CONSOLE BOOT SWITCH METHOD IS USED); OR
- 2 THE CONSOLE SWITCH REGISTER (IF THE LOAD ADDRESS AND START WITH OPTION CODE IN SWITCHES METHOD DESCRIBED BELOW IS USED).

5. RESTARTING AT THE USER POWER FAIL ROUTINE

IF THE USER WISHES TO RESTART HIS OWN SOFTWARE ON A POWER UP HE MAY DO SO BY MERELY DISABLING THE POWER FAIL RESTART SWITCH IN THE MICRO SWITCHES (TURN SWITCH 2 OFF).

6. LOAD AND START PROCEDURE

11/60/70 DIAGNOSTIC ROM

THERE ARE NO SPECIAL M9312 SWITCH SETTINGS THAT PERTAIN TO THIS ROM. THE ONLY WAY THESE DIAGNOSTICS CAN BE EXECUTED IS BY ENTERING A BOOTSTRAP AT AN ENTRY POINT THAT CALLS FOR DIAGNOSTICS TO BE RUN.

THIS ROM ALLOWS BOOTING VIA CONSOLE SWITCH REGISTER. THIS CAN BE DONE AS FOLLOWS:

- 1. LOAD ADDRESS 765744
- 2. SET SWITCH REGISTER AS SHOWN BELOW

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
NA	NA	NA	NA												
OCTAL UNIT								SWR CODE FROM BOOT ROM TABLES							
NUMBER															

3. HOW START

NOTE: THE SWR CODES ARE CONTAINED IN THE BOOT ROM TABLES OF K-SP-M9312-W-4 (SET-UP AND INSTALLATION PROCEDURE).

TW

```

000014      .ABS
000030      MISS=14
000044      GRP0=30
165000      GRP1=44
              .=165000
165000 010037 000700      START:  MOV    R0,R#700
165004 010137 000702      MOV    R1,R#702
165010 010437 000704      MOV    R4,R#704
165014 005037 000706      CLR     R#706
165020 052737 100000 177776      BIS     #100000,R#177776      ;SET FOR 11/70 IF ZERO.
165026 032737 040000 177776      BIT     #40000,R#177776      ;SET BIT 15 IF 11/60,BIT 14 WILL SET
165034 001402                      ;SEE IF 11/60
165036 005237 000706      BEQ     18                      ;IF NOT SET,11/70
165042 005037 177776      INC     R#706      ;SET ,WAS AN 11/60
              CLR     R#177776      ;CLR PSW WORD.
              18:
              ;*****
TEST1  THIS TEST VERIFIES THE UNCONDITIONAL BRANCH
              ;*
              ;*   THE REGISTERS AND CONDITION CODES ARE ALL UNDEFINED WHEN
              ;*   THIS TEST IS ENTERED AND THEY SHOULD REMAIN THAT WAY UPON
              ;*   THE COMPLETION OF THIS TEST.
              ;*****
165046      TST1:
165046 000401      BR     YST2      ; * BRANCH ALWAYS
165050 000000      HALT
              ;*****
TEST2  TEST "CLR", MODE "0", AND "BMI","BVS","BHI","BLT","BLOS
              ;*
              ;*   THE REGISTERS AND CONDITION CODES ARE ALL UNDEFINED WHEN
              ;*   THIS TEST IS ENTERED. UPON COMPLETION OF THIS TEST THE "SP"
              ;*   (R6) SHOULD BE ZERO AND ONLY THE "Z" FLIP-FLOP WILL BE SET.
              ;*****
165052      TST2:
165052 005006      CLR     SP      ;N=0,Z=1,V=0,C=0,SP=000000
165054 100404      BMI     18      ; V BRANCH IF N=1
165056 102403      BVS     18      ; V BRANCH IF V=1
165060 101002      BHI     18      ; V BRANCH IF Z AND C ARE BOTH 0
165062 002401      BLT     18      ; V BRANCH IF (N XOR V)=1
165064 101401      BLOS    TST3    ; * BRANCH IF (Z XOR C)=0
165066 000000      18:  HALT
              ;*****
TEST3  TEST "DEC", MODE "0", AND "BPL","BEQ","BGE","BLE"
              ;*
              ;*   UPON ENTERING THIS TEST THE CONDITION CODES ARE:
              ;*   N = 0, Z = 1, V = 0, AND C = 0.
              ;*   THE REGISTERS ARE: R0 = ?, R1 = ?, R2 = ?
              ;*   R3 = ?, R4 = ?, R5 = ?, SP = 000000
              ;*   UPON COMPLETION OF THIS TEST THE CONDITION CODES WILL BE:
              ;*   N = 1, Z = 0, V = 0, AND C = 0
              ;*   THE REGISTERS AFFECTED BY THE TEST ARE:
              ;*   SP = 177777
              ;*
              ;*****

```

```

165070 005306      TST3:      DEC      SP      ;N=1,Z=0,V=0,C=0,SP=177777
165072 100003      BPL      18      ; V BRANCH IF N=0
165074 001402      BEQ      18      ; V BRANCH IF Z=1
165076 002001      BGE      18      ; V BRANCH IF (N XOR V)=0
165100 003401      BLE      TST4     ; * BRANCH IF (Z OR (N XOR V))=1
165102 000000      18:      HALT
;*****
TEST4  TEST "ROR, MODE "0", AND "BVC","BHS","BNE"
;*****
; *
; * UPON ENTERING THIS TEST THE CONDITION CODES ARE:
; * N = 1, Z = 0, V = 0, AND C = 0.
; * THE REGISTERS ARE: R0=?, R1=?, R2 = ?
; * R3 = ?, R4 = ?, R5 = ?, SP = 177777
; * UPON COMPLETION OF THIS TEST THE CONDITION CODES WILL BE:
; * N = 0, Z = 0, V = 1, AND C = 1
; * THE REGISTERS AFFECTED BY THE TEST ARE:
; * SP = 077777
; *
;*****
165104 006006      TST4:      ROR      SP      ;N=0,Z=0,V=1,C=1,SP=077777
165106 102002      BVC      18      ; V BRANCH IF V=0
165110 103001      BHS      18      ; V BRANCH IF C=0
165112 001001      BNE      TST5     ; * BRANCH IF Z=0
165114 000000      18:      HALT
;*****
TEST5  TEST REGISTER DATA PATH
;*****
; *
; * WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:
; * N = 0, Z = 0, V = 1, AND C = 1.
; * THE REGISTERS ARE: R0 = ?, R1 = ?, R2 = ?
; * R3 = ?, R4 = ?, R5 = ?, SP = 077777.
; * UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
; * N = 0, Z = 1, V = 0, AND C = 0.
; * THE REGISTERS ARE LEFT AS FOLLOWS:
; * R0 = 125252, R1 = 000000, R2 = 125252, R3 = 125252
; * R4 = 125252, R5 = 125252, AND SP = 125252
; *
;*****
165116 012706 125252 TST5:      MOV      #125252,SP ;N=0,Z=0,V=0,C=1,SP=125252
165122 010600      MOV      SP,R0      ;N=0,Z=0,V=0,C=1,R0=125252
165124 010001      MOV      R0,R1      ;N=0,Z=0,V=0,C=1,R1=125252
165126 010102      MOV      R1,R2      ;N=0,Z=0,V=0,C=1,R2=125252
165130 010203      MOV      R2,R3      ;N=0,Z=0,V=0,C=1,R3=125252
165132 010304      MOV      R3,R4      ;N=0,Z=0,V=0,C=1,R4=125252
165134 010405      MOV      R4,R5      ;N=0,Z=0,V=0,C=1,R5=125252
165136 160501      SUB      R5,R1      ;N=0,Z=1,V=0,C=0, AND R1=000000
165140 002401      BLT      18      ; V BRANCH IF (N XOR V)=1
165142 001401      BEQ      TST6     ; * BRANCH IF Z=1
165144 000000      18:      HALT

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TEST6  TEST "ROL", "BCC", "BLT"
;*****
;*
;*  WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:
;*  N = 0, Z = 1, V = 0, AND C = 0.
;*  THE REGISTERS ARE: R0 = 125252, R1 = 000000, R2 = 125252
;*  R3 = 125252, R4 = 125252, R5 = 125252, SP = 125252.
;*  UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
;*  N = 0, Z = 0, V = 1, AND C = 1.
;*  THE REGISTERS ARE LEFT UNCHANGED EXCEPT FOR
;*  R2 WHICH SHOULD NOW EQUAL 052524.
;*
;*****
165146 006102          TST6:
165150 103001          ROL    R2          ;N=0,Z=0,V=1,C=1, AND R2 = 052524
165152 002401          BCC    18          ; V BRANCH IF C=0
165154 000000          BLT    TST7        ; * BRANCH IF (N XOR V)=1
18:      HALT
;*****
TEST7  TEST "ADD", "INC", "COM", AND "BCS", "BLE"
;*
;*  WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:
;*  N = 0, Z = 0, V = 1, AND C = 1.
;*  THE REGISTERS ARE: R0 = 125252, R1 = 000000, R2 = 052524
;*  R3 = 125252, R4 = 125252, R5 = 125252, SP = 125252
;*  UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
;*  N = 0, Z = 1, V = 0, AND C = 0.
;*  THE REGISTERS ARE LEFT UNCHANGED EXCEPT FOR
;*  R3 WHICH NOW EQUALS 000000, AND R1 WHICH IS ALSO 000000
;*
;*****
165156 060203          TST7:
165160 005203          ADD    R2,R3      ;(R2 = 052524) + (R3 = 125252)
165162 005103          INC    R3         ;N=1,Z=0,V=0,C=0, AND R3=177776
165164 060301          COM    R3         ;N=1,Z=0,V=0,C=0, AND R3=177777
165166 103401          ADD    R3,R1      ;N=0,Z=1,V=0,C=1, AND R3=000000
165170 003401          BCS    18         ;N=0,Z=1,V=0,C=0, AND R1 = 000000
165172 000000          BLE    TST10     ; V BRANCH IF C=1
18:      HALT                          ; * BRANCH IF (Z OR (N XOR V))=1
;*****
TEST10 TEST "ROR", "DEC", "RIS", "ADD", AND "BLO"
;*
;*  WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:
;*  N = 0, Z = 1, V = 0, AND C = 0.
;*  THE REGISTERS ARE: R0 = 125252, R1 = 000000, R2 = 052524
;*  R3 = 000000, R4 = 125252, R5 = 125252, SP = 125252.
;*  UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
;*  N = 1, Z = 0, V = 0, AND C = 0.
;*  THE REGISTERS ARE LEFT UNCHANGED EXCEPT FOR
;*  R4 WHICH SHOULD NOW EQUAL 052525, AND
;*  R1 WHICH SHOULD NOW EQUAL 177777
;*
;*****

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165174
165174 006004
165176 050403
165200 260503
165202 005203
165204 103402
165206 005301
165210 002401
165212 000000

TST10:
ROR    R4                ;N=0,Z=0,V=1,C=0, AND R4 = 052525
RIS    R4,R3            ;N=0,Z=0,V=0,C=0, AND R3 = 052525
ADD    R5,R3            ;N=1,Z=0,V=0,C=0, AND R3 = 177777
INC    R3                ;N=0,Z=1,V=0,C=0, AND R3 = 000000
BLO    1$                ; V BRANCH IF C=1
DEC    R1                ;N=1,Z=0,V=0,C=0, AND R1 = 177777
BLT    TST11            ; * BRANCH IF (N XOR V)=1
1$:    HALT
;*
;*****
TEST11  TEST "COM", "BIC", AND "BGT", "BLE"
;*
;*   WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:
;*   N = 1, Z = 0, V = 0, AND C = 0.
;*   THE REGISTERS ARE: R0 = 125252, R1 = 177777, R2 = 052524
;*   R3 = 000000, R4 = 052525, R5 = 125252, SP = 125252.
;*   UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
;*   N = 0, Z = 0, V = 1, AND C = 1.
;*   THE REGISTERS ARE LEFT UNCHANGED EXCEPT FOR
;*   R0 WHICH SHOULD NOW EQUAL 052525, AND
;*   R1 WHICH SHOULD NOW EQUAL 052524
;*
;*****
165214
165214 005100
165216 101401
165220 000000
165222 040001
165224 060101
165226 003001
165230 003401
165232 000000

TST11:
COM     R0                ;N=0,Z=0,V=0,C=1, AND R0 = 052525
BLOS    2$                ; * BRANCH IF (Z OR C)=1
HALT    ;STOP HERE IF BRANCH FAILED
2$:     BIC     R0,R1      ;N=1,Z=0,V=0,C=1, AND R1 = 125252
ADD     R1,R1            ;N=0,Z=0,V=1,C=1, AND R1 = 052524
BGT     1$                ; V BRANCH IF Z AND (N XOR V) ARE BOTH 0
BLE     TST12            ; * BRANCH IF (Z OR (N XOR V))=1
1$:     HALT
;*****
TEST12  TEST "SWAB", "CMP", "BIT", AND "BNE", "BGT"
;*
;*   WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:
;*   N = 0, Z = 0, V = 1, AND C = 1.
;*   THE REGISTERS ARE: R0 = 052525, R1 = 052524, R2 = 052524
;*   R3 = 000000, R4 = 052525, R5 = 125252, SP = 125252.
;*   UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
;*   N = 0, Z = 0, V = 0, AND C = 1.
;*   THE REGISTERS ARE NOW:
;*   R0 = 052525, R1 = 052125, R2 = 052524, R3 = 000000
;*   R4 = 052525, R5 = 052525, SP = 125252.
;*
;*****
165234
165234 000301
165236 020127 052125
165242 001004

TST12:
SWAB    R1                ;N=0,Z=0,V=0,C=0, AND R1 = 052125
CMP     R1,#052125        ;N=0,Z=1,V=0,C=0
BNE     1$                ; V BRANCH IF Z=0
;R4 = 052525 R5 = 125252
;N=0,Z=1,V=0,C=0
; V BRANCH IF Z OR (N XOR V) ARE 0
;N=0,Z=0,V=0,C=1, AND R5 = 052525
BIT     R4,R5
BGT     1$
COM     R5

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165252 001001
165254 000000
TEST13 TEST "MOVR", "SOB", "CLR", "TST" AND "BPL", "BNE"
;*****
; *
; * WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:
; * N = 0, Z = 0, V = 0, AND C = 1.
; * THE REGISTERS ARE: R0 = 052525, R1 = 052125, R2 = 052524
; * R3 = 000000, R4 = 052525, R5 = 052525, SP = 125252.
; * UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
; * N = 0, Z = 1, V = 0, AND C = 0.
; * R0 IS DECREMENTED BY A SOB INSTRUCTION TO 000000
; * R1 IS CLEARED AND THEN INCREMENTED AROUND TO 000000
; *
;*****
TST13:
165256 112700 177401
165262 100001
165264 000000
165266 077002
165270 005001
165272 005201
165274 077002
165276 005700
165300 001002
165302 005701
165304 001401
165306 000000
165310
165312 012706 000776
165314 004767 000002
165320 000000
165322 022716 165320
165326 001401
165330 000000
165332 012716 105342
165336 000207
165340 000000
165342 005046
165344 012746 165354
165350 000002
165352 000000
165354 000137 165362
165360 000000

165254 BNE TST13 ; * BRANCH IF Z=1
165254 HALT
;*****
; *
; * WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:
; * N = 0, Z = 0, V = 0, AND C = 1.
; * THE REGISTERS ARE: R0 = 052525, R1 = 052125, R2 = 052524
; * R3 = 000000, R4 = 052525, R5 = 052525, SP = 125252.
; * UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
; * N = 0, Z = 1, V = 0, AND C = 0.
; * R0 IS DECREMENTED BY A SOB INSTRUCTION TO 000000
; * R1 IS CLEARED AND THEN INCREMENTED AROUND TO 000000
; *
;*****
TST13:
MOV B #177401, R0 ;N=0,Z=0,V=0,C=1, AND R0 = 000001
BPL 2$ ; * BRANCH IF N=0
;STOP IF "BPL" FAILED
165254 HALT ;DO NOT LOOP SINCE (R0 -1) = 0
26: SOB R0, 1$ ;N=0, Z=1, V=0, C=0, AND R1 = 000000
CLR R1 ;INCREMENT 64K TIMES (2 ** 16)
36: SOB R0, 3$ ;LOOP BACK TO "INC" 64K TIMES
TST R0 ;N=0,Z=1,V=0,C=0, AND R0 = 000000
BNE 4$ ; V BRANCH IF Z=0
TST R1 ;N=0,Z=1,V=0,C=0, AND R1 = 000000
BEQ TST14
46: HALT
;*****
TEST14 TEST "JSR", "RTS", "RTI", "JMP"
;*****
; *
; * THIS TEST FIRST SETS THE STACK POINTER TO 776,
; * AND THEN VERIFIES THAT "JSR", "RTS", "RTI", AND "JMP"
; * ALL WORK PROPERLY.
; *
; * ON ENTRY TO THIS TEST THE STACK POINTER "SP" IS INITIALIZED
; * TO 00776 AND IS LEFT THAT WAY ON EXIT.
; *
;*****
TST14:
118: MOV #776, SP ;SET UP THE STACK POINTER
JSR PC, 1$ ;TRY TO JSR TO 1$
108: HALT ;THE "JSR" MUST HAVE FAILED
16: CMP #10$, (SP) ;WAS THE CORRECT ADDRESS PUSHED?
BEQ 2$ ;BRANCH IF YES
;WRONG THING PUSHED ON STACK
26: MOV #3$, (SP) ;CHANGE THE ADDRESS ON THE STACK
RTS PC ;TRY TO RETURN TO 3$
36: HALT ;DID NOT RETURN PROPERLY
CLR -(SP) ;PUSH A ZERO ON THE STACK
MOV #4$, -(SP) ;PUSH THE RETURN ADDRESS ON STACK
RTI ;SEE IF AN "RTI" WORKS
46: HALT ;THE "RTI" FAILED
JMP #5$ ;TRY TO "JMP"
HALT ;THE "JMP" FAILED

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165362          5S:          ;ADDRESS TO "JMP" TO
;*****
TEST15  TEST MAIN MEMORY FROM VIRTUAL 001000 TO LAST ADDR.
;*****
;*
;*  THIS TEST WILL TEST MAIN MEMORY WITH THE CACHE DISABLED, FROM
;*  VIRTUAL ADDRESS 001000 TO LAST ADDR. IF THE DATA DOES NOT COMPARE
;*  PROPERLY THE TEST WILL HALT AT EITHER 165516 OR 165536. IF A
;*  PARITY ERROR OCCURS THE TEST WILL HALT AT ADDRESS 165750, WITH
;*  THE PC + 2 ON THE STACK WHICH IS IN THE KERNEL D-SPACE.
;*
;*  IN THIS TEST THE REGISTERS ARE INITIALIZED AS FOLLOWS:
;*  R0 = 001000, R1 = DATA READ, R2 = 001000, R3 = 177746 (CACHE CONTROL REG.)
;*  R4 = COUNT VALUE, R5 = LAST MEMORY ADDRESS, SP = 000776
;*
;*****
165362          TST15:
165362  012705  160000      MOV    #160000,R5      ;FIRST GET SIZE OF MEMORY.
165366  005037  000006      CLR    #6
165372  012737  165400  000004  MOV    #18,R#4
165400  012706  000776      1S:  MOV    #776,SP
165404  005745              TST    -(R5)
;IN END,R5 CONTAINS LAST MEM ADDR.
165406          FIX:
;THE LAST MEMORY ADDRESS
165406  012737  165714  000114  10S:  MOV    #CONT,R#114  ;SET UP PARITY VECTOR
165414  005037  000116      CLR    #116      ;SET PROCESSOR STATUS WORD TO ZERO
165420  012703  177746      MOV    #177746,R3    ;CACHE CONTROL REGISTER ADDRESS
165424  012713  000014      MOV    #MYSS,(R3)    ;FORCE MISS BOTH GROUPS
165430  012702  001000      MOV    #1000,R2     ;FIRST ADDRESS STORAGE
165434  010200      MOV    R2,R0      ;SETUP FIRST ADDRESS
165436  010010      1S:  MOV    R0,(R0)      ;LOAD EACH ADDRESS WITH ITS
;OWN ADDRESS
165440  005720      TST    (R0)+
165442  020005      CMP    R0,R5
165444  101774      BLOS   1S
165446  010200      MOV    R2,R0      ;SET STARTING ADDRESS IN R0
165450  011001      2S:  MOV    (R0),R1      ;GET THE DATA
165452  020001      CMP    R0,R1      ;IS IT CORRECT?
165454  001401      BEQ    3S          ;BRANCH IF YES
165456  000000      HALT              ;DATA ERROR ON READING MEMORY LOCATION
;R0 = ADDRESS, R1 = DATA RECEIVED, R2 = DATA EXPECTED
;COMPLEMENT DATA AND INCREMENT ADDRESS
165460  005120      3S:  COM    (R0)+
165462  020005      CMP    R0,R5
165464  101771      BLOS   2S
165466  014001      4S:  MOV    -(R0),R1      ;READ THE DATA (IT SHOULD NOW BE THE
;COMPLEMENT OF THE ADDRESS)
165470  005101      COM    R1          ;COMPLEMENT BEFORE CHECKING
165472  020001      CMP    R0,R1      ;IS THE DATA CORRECT?
165474  001401      BEQ    5S          ;BRANCH IF YES
165476  000000      HALT              ;DATA ERROR ON READING MEMORY LOCATION
;R0=ADDRESS, R1=DATA RECEIVED, R2=DATA EXPECTED
165500  020002      5S:  CMP    R0,R2
165502  001371      BNE    4S

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TW


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165560 001362      BNE      3$
165562 000402      BR       6$
165564 000167 177210 JMP      START      ;ENTRY POINT FROM ROM WITH DIAGNOSTIC SELECTED
165570 005720      6$:    TST      (R0)+      ;MOVE TO NEXT ADDRESS
165572 077223      SOB      P2,3$      ;BRANCH IF NOT DONE
165574 012713 000044 MOV      #GRP1,(R3)    ;FORCE MISS LOWER 1/2K OF CACHE ON 11/60
165600 012700 006000 MOV      #6000,R0
165604 105166 000001 COMB     1(SP)      ;COMPLEMENT THE CYCLE FLAG
165610 001344      BNE      1$      ;LOOP IF NOT DONE
;*****
TEST17 TEST MEMORY WITH THE DATA CACHE ON
;*
;* THIS TEST CHECKS VIRTUAL MEMORY FROM 001000 THRU LAST ADDRESS
;* TO INSURE THAT YOU CAN GET HITS ALL THE WAY UP THROUGH MAIN
;* MEMORY. ON THE PDP11/70, IT STARTS WITH GROUP 1 ENABLED, THEN TESTS
;* GROUP 0, AND FINALLY CHECKS MEMORY WITH BOTH GROUPS ENABLED.
;* ON THE PDP11/60, THE TEST IS DONE WITH THE
;* WHOLE CACHE ENABLED.
;*
;* UPON ENTRY THE REGISTERS WILL BE SET UP AS FOLLOWS:
;*
;* R0 = 001000 (ADDRESS), R1 = 3 (PASS COUNT), R2 = (FIRST ADDRESS),
;* R3 = 177746 (CONTROL REG.),
;* R5 = (LAST MEMORY ADDRESS, SP = 776
;*
;* UPON COMPLETION OF THIS TEST MAIN MEMORY FROM VIRTUAL ADDRESS
;* 001000 THRU LAST ADDRESS WILL CONTAIN ITS OWN VIRTUAL ADDRESS.
;*****
TST17:
165612      MOV      #1000,R2      ;SETUP FIRST ADDRESS
165616 012702 001000 MOV      R2,R0      ;FIRST ADDRESS IS 1000 OCTAL
165620 010010      1$:    MOV      R0,(R0)      ;FILL MEMORY WITH ADDRESSES
165622 005720      TST      (R0)+
165624 020005      CMP      R0,R5
165626 101774      BLOS     1$
165630 012701 000003 MOV      #3,R1      ;SET PASS COUNT TO THREE
165634 005016      CLR      (SP)
165636 005737 000706 TST      0#706      ;IF 11/60 THIS LOC=1,11/70=00
165642 001020      BNE      6$      ;IT IS PDP11/60
165644 012716 000030 MOV      #GRP0,(SP)    ;LOAD CODE TO FORCE GROUP 0 ONTO STACK
165650 010200      2$:    MOV      R2,R0      ;FIRST ADDRESS
165652 005110      3$:    COM      (R0)      ;DOUBLE COMPLEMENT DATA AND
165654 005110      COM      (R0)      ;MAKE SURE IT IS IN THE CACHE.
165656      51$:    CMP      P0,(R0)      ;COMPARE DATA, AND SET BIT 0 IN HIT/MISS REG.
165660      BEQ      5$      ;ALSO POINT TO NEXT ADDRESS
165662 000000      HALT     ;BRANCH IF DATA MATCHES
165664 005720      5$:    TST      (R0)+      ;DATA DIDN'T MATCH R0 = ADDRESS + 2
165666 006037 177752 ROR      0#177752    ;WAS THE LAST MEMORY REFERENCE A HIT?
165672 103402      BCS      4$      ;BRANCH IF YES
165674 000000      HALT     ;HIT FAILED TO OCCUR R0 = ADDRESS + 2
165676 000410      BR      ROOTMISS    ;ABORT REST OF TEST IF "CONTINUE" PRESSED
165700 020005      4$:    CMP      P0,R5
165702 101763      BLOS     3$

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TW

	165704	011613	68:	MOV	(SP),(R3)	;FORCE MISS GRP1 ON PASS 2, FULLY
						;ENABLE CACHE ON PASS THREE. (11/70)
						;ON 11/60, RUN EACH PASS WITH THE SHOLE
						;CACHE ENABLED.
	165706	005016		CLR	(SP)	;GET READY TO FULLY ENABLE CACHE ON PASS 3
	165710	077121		S0B	R1,2\$;RUN THREE PASSES THRU THIS TEST
	165712	000404	JUMP0:	BR	JUMP	;GO TO BOOT STRAP CODE
	165714	000000	CONT:	HALT		;STOP HERE IF THERE IS A CACHE PARITY ERROR
						;OR A MAIN MEMORY PARITY ERROR
						;CHECK CCR, MEMORY REGISTER AND CPU REGISTER
						;TO FIND WHICH ONE
	165716	000402		BR	JUMP	
	165720		BOOTMISS:			
	165720	012713		MOV	#MISS,(R3)	;FORCE MISSES IN BOTH GROUPS OF CACHE
	165724	013700	JUMP:	MOV	#700,R0	;NOW RESTORE ALL NEEDED REGISTERS.
	165730	013701		MOV	#702,R1	;AND RETURN TO BOOTSTRAP.
	165734	013704		MOV	#704,R4	
	165740	000164		JMP	2(R4)	
TEST17	TEST MEMORY WITH THE DATA CACHE ON					
	165744	013704		MOV	#177570,R4	;SWITCH REGISTER TO R4
						;OFFSET ADDR.IN BITS 0-8 OF R4
	165750	042704		BIC	#177000,R4	
	165754	052704		BIS	#173000,R4	;BITS 0-8 OF SWP CONTAINS STARTING CODE.
						;OF DESIRED ROM.
	165760	113700		MOVB	#177571,R0	;BITS 9-11 OF SWR = OCTAL UNIT NUMBER.
	165764	006200		ASR	R0	;UNIT # RIGHT JUSTIFIED IN R0
	165766	000241		CLC		;MAKE SURE C BIT CLEAR
	165770	000114		JMP	(R4)	;EXIT TO BOOT ROM
	165772	000000		HALT		;EXTRA WORD
	165774	041060		.ASCII	"0B"	;IDENTIFIES ROM AS "80" OR B VERSION REV 0. ECB
12-12						
	165776	025055		.WORD	025055	;CONTAINS CRC-16 WORD FOR LAST 255 WORDS.
		000001		.END		

616F1.M11 SYMBOL TABLE

BIT8 = 000400
CRCWD = 000000
GRP1 = 000044
JUMP0 165712
RC11CR= 177446
RK06CR= 177440
RS03CR= 172040
R0 = %000000
P4 = %000004
SP = %000006
TST11 165214
TST15 165362
TST3 165070
TST7 165156
TU56CR= 177342

BIT9 = 001000
DIAG = 165564
HSRCR = 177550
MISS = 000014
RESERV= 000340
RL01CR= 174400
RS04CR= 172040
R1 = %000001
R5 = %000005
START 165000
TST12 165234
TST16 165504
TST4 165104
TTCR = 177560
.
= 165000

ROOTMI 165720
FIX 165406
INITSW= 173024
MRESER= 173000
RF11CR= 177460
RP03CR= 176714
RX01CR= 177170
R2 = %000002
R6 = %000006
TST1 165046
TST13 165256
TST17 165612
TST5 165116
TU10CR= 172522

CONT 165714
GRP0 = 000030
JUMP 165724
PC = %000007
RK05CR= 177404
RP04CR= 176700
RX02CR= 177170
R3 = %000003
R7 = %000007
TST10 165174
TST14 165310
TST2 165052
TST6 165146
TU16CR= 172440

TW

SECTION 3

ROM 23-774F1

CIM9AA MACY11 30A(1052) 25-MAR-80 16:43
CIM9AA.P11 25-MAR-80 16:20

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.REM 8

IDENTIFICATION

PRODUCT CODE: AC-F554A-AC

PRODUCT NAME: CIM9AA0 11/24 ROM M9312

PRODUCT DATE: JUNE, 1979

MAINTAINER: DIAGNOSTIC ENGINEERING

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DIGITAL	PDP	UNIBUS	MASSBUS
DEC	DECUS	DECTAPE	DECX/11

HISTORY

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1.0	GENERAL PROGRAM INFORMATION
1.1	ABSTRACT
	THIS DIAGNOSTIC IS GO/NOGO VERIFICATION OF AN 11/24 SYSTEM WHICH TESTS:
1.	ALL SINGLE AND DOUBLE OPERAND INSTRUCTIONS, INCLUDING EIS, UTILIZING ALL SOURCE AND DESTINATION ADDRESSING MODES.
2.	ALL OF MEMORY, IN 4K PAGES, VIA MEMORY MANAGEMENT AND PRINT THE MEMORY SIZE (LAST MEMORY ADDRESS +2).
3.	SLU1 VIA MAINTENANCE MODE (ALSO CHECKS CONSOLE PRINTER AND INTERFACE WHEN PRINTING MEMORY SIZE).
4.	THE DIAGNOSTIC IS COMPATIBLE WITH M9312 DIAGNOSTIC ROM FORMAT REQUIREMENTS.

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1.2 SYSTEM REQUIREMENTS

A. HARDWARE REQUIREMENTS

THIS DIAGNOSTIC IS DESIGNED TO RUN ON AN 11/24 WITH CONSOLE
TERMINAL AND 4K OF MEMORY (MINIMUM). FURTHER, IT ASSUMES THE
PRESENCE OF THE MEMORY MANAGEMENT UNIT (MMU) CHIP.

B. SOFTWARE REQUIREMENTS

NONE

1.3 RELATED DOCUMENTS AND STANDARDS

THE FOLLOWING DOCUMENTS WERE USED OR REFERENCED DURING THE
CREATION OF THIS DIAGNOSTIC:

1. DIAGNOSTIC ENGINEERING STANDARDS AND CONVENTIONS PROGRAMMING
PRACTICES (DOC. NO. 175-03-009-02).
2. PDP-11 SYSMAC PACKAGE (MAINDEC-11-DZQAC-C3).
3. REQUIRMENTS FOR NEW BOOT ROMS AND CPU ROMS USED IN THE M9312
(K-SP-M9312-0-2).

1.4 DIAGNOSTIC HIERARL PREREQUISITES

NONE

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1.5 ASSUMPTIONS

THE DIAGNOSTIC ASSUMES PROPER STEPUP OF THE DIP SWITCHPAK ON THE M9312 BOOTSTRAP MODULE (SEE M9312 USER'S MANUAL AND TABLE BELOW FOR THIS INFORMATION) AND PRESENCE OF A BOOT ROM IN THE M9312.

S1 (1-10)				
BOOTSTRAP:	DIAGNOSTICS:	FIRST DEVICE (ALL ROMS)	VIRTUAL ADDRESS	SWITCHPACK S1 SWITCHES ON
ODT	NO	2004	165004	1,9
	YES	2006	165006	1,9,10
DEVICE ROM #1	NO	0004	173004	9
	YES	0006	173006	10
DEVICE ROM #2	NO	0204	173204	4,9
	YES	0206	173206	4,9,10
DEVICE ROM #3	NO	0404	173404	3,9
	YES	0406	173406	3,9,10
DEVICE ROM #4	NO	0604	173604	3,4,9
	YES	0606	173606	3,4,9,10

2.0 OPERATING INSTRUCTIONS

2.1 LOADING AND STARTING PROCEDURE

IF DIAGNOSTIC IS SELECTED BY M9312 SWITCHPAK, IT WILL BE RUN ON POWER UP, BUT CAN ALSO BE SELECTED FROM MICRO-ODT BY COMMAND:

165000G

TO BOOT A DEVICE ROM DIRECTLY, USE THE VIRTUAL ADDRESS COLUMN OF THE ABOVE TABLE. FOR EXAMPLE, TO BOOT DEVICE ROM #3 WITH DIAGNOSTICS, USE 173406G (FROM MICRO-ODT).

2.2 PROGRAM OPTIONS

NONE

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2.3 EXECUTION TIMES

A. FIRST PASS (QV)

A PASS OF THIS CODE TAKES APPROXIMATELY 6 SECONDS TO COMPLETE INCLUDING THE PRINTING OF THE MEMORY SIZE. THIS TIMING IS BASED ON A 11/24 CPU WITH 128K WORD OF MOS MEMORY.

B. LONGEST TEST

THE LONGEST SINGLE TEST IS THE MEMORY TEST WHICH TAKES APPROXIMATELY 5 SECONDS PER 128K WORDS OF MEMORY.

C. ADDITIONAL TIME FOR UNITS

APPROXIMATELY 5 SECONDS IS ADDED TO THE TEST TIME FOR EVERY ADDITIONAL 128K WORDS OF MEMORY. THIS TIMING IS BASED ON AN 11/24 WITH MOS MEMORY.

SAMPLE TEST TIMES BASED ON ABOVE FIGURES:

128KW=	6 SECONDS
256KW=	11 SECONDS
512KW=	21 SECONDS
1024KW=	41 SECONDS
1536KW=	61 SECONDS
1920KW=	76 SECONDS

D. FULL PASS TIME (ITERATIONS)

THIS PROGRAM DOES NOT DO ANY ITERATIONS ON ANY OF THE TESTS AND IN FACT ONLY MAKES ONE PASS THRU THE CODE FOR EACH START.

3.0 ERROR INFORMATION

3.1 ERROR REPORTING PROCEDURES

SINCE THIS DIAGNOSTIC IS A GO/NOGO, LOW-LEVEL TEST, NO ERROR REPORTING, AS SUCH, IS IMPLEMENTED; HOWEVER, IF THE MICRO-ODT AND CONSOLE TERMINAL ARE OPERATIONAL THE ERROR HALT ADDRESS+2 WILL BE TYPED FOR THE OPERATOR.

3.2 ERROR HALTS

BADADD = 165142 THIS ERROR IS CAUSED BY TRAPPING TO LOCATION 4 AT ANY TIME PRIOR TO EXECUTING THE MEMORY TEST ON THE FIRST 4K OF MEMORY. THE PROGRAM DOES ACCESSES TO SOME OF THE MEMORY MANAGEMENT REGISTERS DURING THIS TIME. IT MAY BE HELPFUL TO EXAMINE THE STACK BUT SINCE THE PROGRAM HAS NOT SET IT UP THE INFORMATION RECIEVED MAY NOT BE VALID.

CPUERR = 165144 THIS ERROR INDICATES A FAILURE WITH EITHER THE BASE INSTRUCTION SET OR THE EIS INSTRUCTION SET. FIRST SUSPECT THE DCF11-A HYBRID OR THE CPU BOARD.

MEMERR = 165542 THIS ERROR INDICATES A MEMORY SYSTEM FAILURE. FIRST SUSPECT THE MEMORY THEN THE KTF11-A. TO LOCATE THE FAILING BANK DIVIDE THE CONTENTS OF PAR0 (1772342) BY 200(8) THEN MULTIPLY BY 4.

SLUERR = 165702 THIS HALT INDICATES A DATA ERROR IN THE CONSOLE SLU. THE GOOD DATA IS IN R2.

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4.0 PERFORMANCE AND PROGRESS REPORTS

4.1 PERFORMANCE REPORTS

NONE

4.2 PROGRESS REPORTS

THE PROGRAM REPORTS ITS PROGRESS USING TWO LEDS LOCATED ON THE 11/24 CPU BOARD. THEY ARE LOCATED ON THE HANDLE EDGE OF THE BOARD ALONG WITH THE RUN LIGHT. THEY ARE DRIVEN THROUGH BITS 0 AND 1 OF THE DISPLAY REGISTER WITH BIT 0 DRIVING THE LED FURTHEST FROM THE FRONT OF THE BOX AND BIT 1 DRIVING THE LED IN THE CENTER OF THE THREE LIGHTS. THE LIGHT CLOSEST TO THE FRONT OF THE BOX IS THE RUN LIGHT. THE PROGRAM FIRST WRITES AN OCTAL 3 TO THE REGISTER (TURNING BOTH LEDS ON) TO SIGNAL THE START OF THE CPU TEST. THE COUNT IS DECREMENTED BY ONE AT THE START OF EACH OF THE NEXT THREE TEST SECTIONS.

LIGHT COUNT

3
2
1
0

LAST TEST COMPLETED

NONE-SUCCESSFUL ENTRY TO PROGRAM
CPU TEST
MEMORY TEST
SLU TEST

5.0 DEVICE INFORMATION TABLES

POOL (LOC 165102) CONTAINS DATA USED BY DOUBLE OPERAND SECTION.

6.0 PROGRAM DESCRIPTION

6.1 PROGRAM EXECUTION CHARACTERISTICS

PROPER EXECUTION OF THE DIAGNOSTIC RESULTS IN PRINTOUT OF THE MEMORY SIZE AND BOOTING A PERIPHERAL OR ENTERRING MICRO-ODT (DEPENDING ON M9312 SWITCH SETTINGS).

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6.2 SUBTEST SUMMARIES

A. CPUTST - THIS SUBTEST VERIFIES THE PDP-11 INSTRUCTION SET, INCLUDING EIS, FOR BOTH WORD AND BYTE FORMATS. IT CONSISTS OF FIVE SECTIONS - SINGLE OPERAND (DESTINATION MODE 0), DOUBLE OPERAND (ALL SOURCE MODES, DESTINATION MODE 0), CONDITIONAL BRANCHES, BYTE INSTRUCTIONS (ALL DESTINATION MODES), AND JSR/RTS WITH EIS.

B. MEMTST - THIS SUBTEST CHECKS ALL OF MEMORY IN 4K PAGES USING THE MMU, DETERMINES MEMORY SIZE, AND CONSTRUCTS A PHYSICAL ADDRESS FROM THE VIRTUAL ADDRESS WHICH CAUSED A TIMEOUT TRAP. LOOPING THROUGH EACH 4K PAGE IS CONTROLLED BY THE 1s LOOP, AND; WITHIN THIS LOOP, THE 2s LOOP LOADS EACH LOCATION WITH ITS ADDRESS, THE 3s LOOP CHECKS THE DATA AND COMPLEMENTS IT, THE 4s LOOP ADDS THE CONTENTS OF EACH LOCATION TO ITS COMPLEMENT AND INCREMENTS THE RESULT TO PRODUCE ZERO. SECTION TIMEOUT TURNS OFF MEMORY MANAGEMENT AND BUILDS A PHYSICAL ADDRESS IN R0 AND R1.

NOTE: BECAUSE OF SPACE LIMITATIONS THERE IS A KNOWN FLAW IN THE MEMORY SIZING ROUTINE. IF MAXIMUM MEMORY IS CONFIGURED ON THE SYSTEM(1920KW) THE SIZING ROUTINE WILL REPORT A MEMORY SYSTEM SIZE OF 2044KW. THIS IS BECAUSE OF THE UNIBUS MAP WILL MAP THE LAST 124K OF VIRTUAL ADDRESS SPACE TO THE LOWER 124K OF MAIN MEMORY.

C. SLUTST - THIS SUBTEST PLACES SLU1 IN MAINTENANCE MODE (SERIAL OUT OF UART TIED TO SERIAL IN OF UART) AND TESTS THAT ALL 8-BIT PATTERNS CAN BE TRANSMITTED AND RECEIVED. SECTION PRINT PRINTS THE MEMORY SIZE CALCULATED BY MEMTST, AND TRANSFERS CONTROL BACK TO ODT OR THE APPLICABLE BOOT ROM.

6.3 SPECIAL SUBROUTINE DESCRIPTION

THE PRINT ROUTINE TYPES THE LAST 22-BIT MEMORY ADDRESS+2 FOUND BY THE MEMORY SIZE ROUTINE. THE 16 HIGH ORDER BITS ARE SAVED IN R0 AND THE 6 LOW ORDER BITS ARE SAVED IN R1.


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7.0 LISTING
*
.TITLE CIM9AA
.SBTTL ROM AREA 165000-165776
.SBTTL GO/NOGO MINIMUM DIAGNOSTIC
.TITLE F11 DIAGNOSTIC ROM FOR M9312
;*COPYRIGHT (C) JUNE,1979
;*DIGITAL EQUIPMENT CORP.
;*MAYNARD, MASS. 01754
;*
;*PROGRAM BY D. SOBIK
;*
;*THIS PROGRAM WAS ASSEMBLED USING THE PDP-11 MAINDEC SYSMAC
;*PACKAGE (MAINDEC-11-D7QAC-C3), JAN 19, 1977.
;*
$TN=1
$SWR=160000 ;;HALT ON ERROR, LOOP ON TEST, INHIBIT ERROR TYP0UT

.SBTTL REGISTER DEFINITIONS
$WR= 177570 ;SWITCH REGISTER (DIAGNOSTIC LIGHTS)
$PS= 177776 ;PROCESSOR STATUS WORD
;SLU1 REGISTERS
$RCSR= 177560 ;RECEIVER CSR
$RBUF= 177562 ;RECEIVER BUFFER
$XCSR= 177564 ;TRANSMITTER CSR
$XBUF= 177566 ;TRANSMITTER BUFFER

;MMU REGISTERS
$PAR0= 172340 ;KERNAL PAGE ADDRESS REGISTERS
$PAR1= 172342
$PAR7= 172356
$PDR0= 172300 ;KERNAL PAGE DESCRIPTOR REGISTERS
$PDR1= 172302
$PDR7= 172316
$UPAR0= 177640 ;USER PAGE ADDRESS REGISTERS
$UPAR1= 177642
$SR0= 177572 ;STATUS REGISTER 0
$SR3= 172516 ;STATUS REGISTER 3 (22-BIT)
.=165000
START: JMP 0173024 ;TRANSFER TO SELECTED BOOT ROM OR ODT
HALT ;ENTRY POINT FOR ODT, NO DIAGNOSTICS
;ENTRY POINT FOR ODT WITH DIAGNOSTICS
MOV #165002,R4 ;SET UP RETURN ADDRESS-2 IN R4

.SBTTL CPU TEST
;*****
; BASIC CPU TEST
;*****
CPU1ST: MOV #3, 0$SWR ;LIGHTS = 3, INDICATING CPU1ST
MOV #BADADD,0$4 ;SET UP TIME OUT VECTOR INCASE OF TRAP

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399 165026 005037 000006 CLR R0, #6 ;CLEAR PRIORITY OF TRAP ROUTINE
400 165032 010037 177640 MOV R0, #UPAR0 ;WE ARE USING THE UPAR'S HERE SIMPLY BECAUSE
401 165036 010137 177642 MOV R1, #UPAR1 ;THEY ARE AVAILABLE UNUSED INTERNAL REGS.
402                                     ;WE ARE STORING PARAMETERS FROM THE BOOT ROM
403
404                                     ;R1 CONTENTS      N Z V C
405 165042 005001 CLR R1 ;000000 0 1 0 0
406 165044 005201 INC R1 ; 1 0 0 0 0
407 165046 005101 COM R1 ;177776 1 0 0 1
408 165050 006201 ASR R1 ;177777 1 0 1 0
409 165052 006301 ASL R1 ;177776 1 0 0 1
410 165054 006001 ROR R1 ;177777 1 0 1 0
411 165056 005701 TST R1 ;177777 1 0 0 0
412 165060 005401 NEG R1 ; 1 0 0 0 1
413 165062 005301 DEC R1 ; 0 0 1 0 1
414 165064 005601 SBC R1 ;177777 1 0 0 1
415 165066 005501 ADC R1 ; 0 0 1 0 1
416 165070 001026 BNE CPUERR ;ERROR IF NOT ZERO
417
418 ; SECTION FOR DOUBLE OPERAND, ALL SOURCE MODES, DEST MODE 0
419
420 165072 012702 165126 MOV #POOL, R2 ;SET UP ADDRESS OF DATA TABLE
421 165076 011201 MOV (R2), R1 ;R1/POOL, SMODE 1
422 165100 022201 CMP (R2)+, R1 ;DATA CORRECT? SMODE 2
423 165102 001021 BNE CPUERR
424 165104 063201 ADD 0(R2)+, R1 ;R1/POOL + 1, SMODE 3
425 165106 165201 SUB 0-(R2), R1 ;R1/POOL , SMODE 5
426 165110 044201 BIC -(R2), R1 ;R1/0 ,SMODE 4
427 165112 056201 000004 BIS 4(R2), R1 ;R1/177777, SMODE 6
428 165116 037201 000006 BIT 06(R2), R1 ;RESULT IS 177777, SMODE 7
429 165122 001411 BEQ CPUERR
430 165124 000411 BR CONT ;BRANCH AROUND DATA TABLE
431
432 165126 165126 POOL: .WORD POOL
433 165130 165136 .WORD DATA1
434 165132 177777 DATA2: .WORD 177777
435 165134 165132 .WORD DATA2
436 165136 000001 DATA1: .WORD 1
437 165140 000500 DOUBLES: .WORD 500
438 165142 000500 .WORD 500
439 165144 000000 BADADD: HALT
440 165146 000000 CPUERR: HALT
441
442 ; CHECK CONDITIONAL BRANCHES
443
444 165150 000277 CONT: SCC ;SET ALL CONDITION CODES
445 165152 001375 RNE CPUERR ;BR IF Z=0
446 165154 100374 BPL CPUERR ;" " N=0
447 165156 102373 BVC CPUERR ;" " V=0
448 165160 103372 BCC CPUERR ;" " C=0
449 165162 002771 BLT CPUERR ;" " N XOR V=1
450 165164 003370 BGT CPUERR ;" " Z OR (N XOR V)=0
451 165166 101367 BHI CPUERR ;" " C OR Z=0
452 165170 000257 CCC ;CLR ALL CONDITION CODES
453 165172 001765 BEQ CPUERR ;BR Z=1

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454      165174  100764
455      165176  102763
456      165200  103762
457      165202  003761
458      165204  101760
459      165206  000270
460      165210  002356
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466      165212  105001
467      165214  105201
468      165216  105101
469      165220  106201
470      165222  106301
471      165224  106001
472      165226  105401
473      165230  105301
474      165232  105601
475      165234  106101
476      165236  105501
477      165240  000301
478      165242  012703  000500
479      165246  105063  000001
480      165252  110113
481      165254  120123
482      165256  001333
483      165260  105143
484      165262  012703  165140
485      165266  153733  165136
486      165272  143753  165132
487      165276  130173  000002
488      165302  001321
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490
491
492      165304  012706  000500
493      165310  004767  000006
494      165314  000714
495      165316  000167  000042
496      165322  012701  000040
497      165326  070127  000010
498      165332  006700
499      165334  072127  000006
500      165340  073127  000071
501      165344  071027  000200
502      165350  005201
503      165352  074001
504      165354  001274
505      165356  062716  000002
506      165362  000207
507
508

      BMI      CPUERR      ;BR N=1
      BVS      CPUERR      ;BR V=1
      BCS      CPUERR      ;BR C=1
      BLE      CPUERR      ;BR Z OR (N XOR V)=1
      BLOS     CPUERR      ;BR C OR Z=1
      SEN      ;N=1
      BGE      CPUERR      ;BR N XOR V=0

;      CHECK BYTE INSTRUCTIONS, ALL DEST MODES

;R1 CONTENTS      N Z V C
CLRB      R1      ;177400      0 1 0 0
INCB      R1      ;177401      0 0 0 0
COMB      R1      ;177776      1 0 0 1
ASRB      R1      ;177777      1 0 1 0
ASLB      R1      ;177776      1 0 0 1
RORB      R1      ;177777      1 0 1 0
NEGR      R1      ;177401      0 0 0 1
DECB      R1      ;177400      0 1 0 1
SBCB      R1      ;177777      1 0 0 1
ROLB      R1      ;177777      1 0 0 1
ADCB      R1      ;177400      0 1 0 1
SWAB      R1      ;000377      1 0 0 0
MOV      #500, R3      ;SETUP FOR DMODE TESTING
CLRB      1(R3)      ;CLR LOC 501, DMODE 6
MOVB      R1, (R3)      ;500/000 377, DMODE 1
CMPB      R1, (R3)+      ;SHOULD COMPARE, DMODE 2
BNE      CPUERR
COMB      =(R3)      ;500/000 000, DMODE 4
MOV      #DOUBLE,R3      ;SETUP DEFERRED DMODES
BISB      @DATA1,@(R3)+      ;500/1, DMODE 3
BICB      @DATA2,@=(R3)      ;500/0, DMODE 5
BITB      R1, @2(R3)      ;Z=1, DMODE 7
BNE      CPUERR

;      CHECK JSR/RTS AND EIS

MOV      #500, SP      ;SET UP STACK
JSR      PC, EISTST
BR      CPUERR
JMP      MEMTST      ;EXIT CPU TEST
EISTST: MOV      #40, R1      ;R1/ 40
MUL      #10, R1      ;R1/ 400
SXT      R0      ;R0/ 0
ASH      #6, R1      ;R1/ 40000
ASHC     #71, R1      ;R1/ 200
DIV      #200, R0      ;R0/1 R1/0
INC      R1      ;R1/1
XOR      R0, R1      ;R1/0
BNE      CPUERR
ADD      #2, (SP)      ;FIX RETURN ADDRESS TO BYPASS ERROR BR
RTS      PC      ;EXIT TO MEMORY TEST
;*****

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509      .SBTTL MEMTST
510
511      ;*****
512
513      ;+
514      ;      THIS TEST SIZES MEMORY AND CHECKS MEMORY FROM LOC 1000 TO END OF
515      ;      MEMORY BY WRITING IN EACH LOCATION THE ADDRESS OF THE LOCATION
516      ;      AND COMPARING THE LOCATION AND ITS CONTENTS. THE PROCEDURE IS
517      ;      REPEATED USING THE COMPLEMENTS OF THE ADDRESS IN EACH LOCATION.
518      ;      MEMORY IS CLEARED ON EXIT FROM THIS TEST IN 4K BLOCKS; THAT IS,
519      ;      IF 122K IS PRESENT, 120K GETS CLEARED, THE REST HAS THE ADDRESS
520      ;      WRITTEN IN IT.
521      ; -
522
523
524      ;*****
525
526      165364 012737 000002 177570 MEMTST: MOV      #2,      @#SWR ;LIGHTS = 2, INDICATING MEMTST
527      165372 005037 172340          CLR      @#PAR0 ;MAP VECTOR SPACE TO PAR0
528      165376 012737 077406 172300          MOV      #77406,    @#PDR0 ;4K PAGE R/W
529      165404 005037 172342          CLR      @#PAR1 ;PAR1 IS MOVABLE WINDOW INTO MEMORY
530      165410 012737 077406 172302          MOV      #77406,    @#PDR1
531      165416 012737 177600 172356          MOV      #177600,@#PAR7 ;MAP PAR7 TO I/O PAGE
532      165424 012737 077406 172316          MOV      #77406,    @#PDR7
533      165432 005037 177776          CLR      @#PS      ;ENSURE KERNEL MODE
534      165436 005237 177572          INC      @#SR0      ;TURN ON KT
535      165442 012737 000020 172516          MOV      #20,      @#SR3 ;SET UP FOR 22-BIT RELOCATION
536      165450 012702 000002          MOV      #2,      R2      ;WORD INCREMENT
537      165454 012737 165552 000004 1s:      MOV      #TIMOUT,@#4 ;SETUP TIMEOUT VECTOR FOR MEMORY SIZE
538      165462 012703 020000          MOV      #20000,    R3      ;START AT VIRTUAL ZERO
539      165466 012705 010000          MOV      #10000,    R5      ;PAGE LENGTH = 4K
540      165472 010301          MOV      R3,      R1      ;WORKING COPY OF FIRST ADDRESS
541      165474 010500          MOV      R5,      R0      ;COPY PAGE LENGTH
542      165476 010111          2s:      MOV      R1,      (R1) ;WRITE ADDRESS INTO LOCATION
543      165500 060201          ADD      R2,      R1      ;INCREMENT ADDRESS
544      165502 077003          SOB      R0,      2s      ;LOOP TILL PAGE DONE
545      165504 010301          MOV      R3,      R1      ;RESTORE INITIAL CONDITIONS FOR
546      165506 010500          MOV      R5,      R0      ; DATA CHECK AND COMPLEMENTING
547      165510 020111          3s:      CMP      R1,      (R1) ;GOOD DATA?
548      165512 001014          BNE      MEMERR ;NO, HALT
549      165514 005121          COM      (R1)+      ;COM DATA AND INC ADDRESS
550      165516 077004          SOB      R0,      3s      ;LOOP TILL PAGE DONE
551      165520 010301          MOV      R3,      R1      ;START AGAIN TO TEST COM DATA
552      165522 010500          MOV      R5,      R0
553      165524 060111          4s:      ADD      R1,      (R1) ;RESULT SHOULD BE -1
554      165526 005221          INC      (R1)+      ;RESULT=0 AND SETUP NEXT ADDRESS
555      165530 001005          BNE      MEMERR
556      165532 077004          SOB      R0,      4s      ;FINISH THE PAGE
557      165534 062737 000200 172342          ADD      #200,    @#PAR1 ;RELOC TO A NEW PAGE
558      165542 000744          BR      1s          ;CHECK OUT A NEW PAGE
559      165544 005037 177572          MEMERR: CLR      @#SR0 ;TURN OFF KT
560      165550 000000          HALT          ;BAD MEMORY
561      165552 005037 177572          TIMEOUT: CLR      @#SR0 ;TURN OFF KT
562      165556 005037 172516          CLR      @#SR3 ;RESTORE 18-BIT RELOCATION
563      165562 000240          NOP          ;SPACE FILLER FOR ROM ENTRY POINT

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564 165564 000402 BR 15 ;BRANCH AROUND ENTRY POINT
565 165566 000167 177220 JMP CPUTST ;BOOT ROM ENTRY POINT
566 165572 012737 000006 000304 1s: MOV #6, R4 ;TIMEOUT TRAPCATCHER
567 165600 160301 SUB R3, R1 ;GET RID OF VIRTUAL OFFSET
568 165602 005000 CLR R0 ;CLR HIGH HALF OF DOUBLEWORD
569 165604 073027 200012 ASHC #12, R0 ;LSH 10. TO BUILD PHYSICAL ADDRESS
570 165610 063700 172342 ADD 0#PAR1, R0 ;ADD PAGE BASE ADDRESS
571 165614 073027 177776 ASHC #-2, R0 ;ACCOUNT FOR 1-BIT MSD
572 ;SMTTL SLUI TEST
573
574 ;*****
575 ;
576 ; CHECK SLUI VIA MAINTENANCE MODE
577 ;*****
578
579
580 165620 012737 000001 177570 SLUTST: MOV #1, R5 ;LIGHTS = 1, INDICATING SLUTST
581 165626 005002 CLR R2 ;FIRST ASCII CODE TO BE CHECKED
582 165630 012737 000004 177564 MOV #4, R4 ;ENABLE MAINTENANCE MODE
583 165636 105737 177564 2s: TSTB 0#XCSR ;TRANSMITTER READY?
584 165642 100375 BPL 2s ;NO, WAIT FOR READY
585 165644 110237 177566 MOV R2, R4 ;TRANSMIT CHAR
586 165650 105737 177560 3s: TSTB 0#RCSR ;DATA RECEIVED?
587 165654 100375 BPL 3s ;NO
588 165656 120237 177562 CMPB R2, R4 ;DID DATA LOOP AROUND CORRECTLY?
589 165662 001006 BNE SLUERR ;NO
590 165664 005202 INC R2 ;SET UP NEXT PATTERN
591 165666 105702 TSTB R2 ;DONE ALL PATTERNS?
592 165670 001362 BNE 2s ;NO, CONTINUE
593 165672 005037 177564 CLR 0#XCSR ;EXIT MAINTENANCE MODE
594 165676 000403 BR PRINT ;PRINT LAST ADDRESS
595 165700 005037 177564 SLUERR: CLR 0#XCSR ;EXIT MAINT MODE
596 165704 000000 HALT
597
598 ;*****
599 ;
600 ; PRINT MEMORY SIZE (LAST ADDRESS + 2) AND EXIT
601 ;*****
602
603
604 165706 005037 177570 PRINT: CLR 0#SWR ;LIGHTS = 0, ALL TESTS PASSED
605 165712 012705 000010 MOV #10, R5 ;PRINT 8. DIGITS
606 165716 012703 000003 1s: MOV #3, R3 ;SHIFT COUNT FOR DIGIT ASSEMBLY
607 165722 005002 CLR R2 ;CLR DIGIT ASSEMBLY AREA
608 165724 073027 000001 2s: ASHC #1, R0 ;PUT BIT IN C-BIT
609 165730 006102 ROL R2 ;MOVE C-BIT TO R2
610 165732 077304 SOB R3, 2s ;BUILD A DIGIT IN R2
611 165734 062702 000060 ADD #0, R2 ;CNVRT TO ASCII
612 165740 105737 177564 3s: TSTB 0#XCSR ;PRINTER READY?
613 165744 100375 BPL 3s
614 165746 110237 177566 MOV R2, R4 ;PRINT IT
615 165752 077517 SOB R5, 1s ;PRINT 8. DIGITS

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616
617 ;////////////////////////////////////
618
619 ;      EXIT TO ODT OR TO BOOT ROM
620
621 ;////////////////////////////////////
622
623 165754 013700 177640      MOV      @#UPAR0, R0      ;RESTORE BOOT ROM PARAMETERS
624 165760 013701 177642      MOV      @#UPAR1, R1
625 165764 000164 000002      JMP      2(R4)          ;RETURN TO BOOT ROM OR ODT
626 165770      015          CRLF: .BYTE 15
627 165771      012          .BYTE 12
628
629
630      165774              .=165774
631 165774 042060              .ASCII "0D"          ;#4 CPU ROM FOR M9312
632
633      165000              .END  START

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BADADD	165144	398	439*											
CONT	165150	430	444											
CPUERR	165146	416	423	429	440	445	446	447	448	449	450	451	453	454
		455	456	457	458	460	482	488	494	504				
CPUTST	165012	397	565											
CRLF	165770	626												
DATA1	165136	433	436	485										
DATA2	165132	434	435	486										
DOUBLE	165140	437	484											
EISTST	165322	493	496											
MENERR	165544	548	555	559										
MEMTST	165364	495	526											
PAR0 =	172340	374	527*											
PAR1 =	172342	375	529*	557*	570									
PAR7 =	172356	376	531*											
PDR0 =	172300	377	528*											
PDR1 =	172302	378	530*											
PDR7 =	172316	379	532*											
POOL	165126	420	432											
PRINT	165706	594	604											
PS =	177776	366	533*											
RBUF =	177562	369	588											
RCSR =	177560	368	586											
SLUERR	165700	589	595											
SLUTST	165620	580												
SR0 =	177572	382	534*	559*	561*									
SR3 =	172516	383	535*	562*										
START	165000	395	633											
SWR =	177570	365	397*	526*	580*	604*								
TIMOUT	165552	537	561											
UPAR0 =	177640	380	400*	623										
UPAR1 =	177642	381	401*	624										
XBUF =	177566	371	585*	614*										
XCSR =	177564	370	582*	583	593*	595*	612							
\$HD =	000003	361	362											
\$SWR =	160000	361	362											
\$TN =	000001	361												
.	= 165776	384	630											
SLASH	351	617	621											
STARS	351	391	395	507	511	524	574	578	598	602				
.HEADE	351													
.ABS.	165776	000												
ERRORS DETECTED: 0														
CIM9AA,CIM9AA/SOL/CRF=CIM9AA.P11														
RUN-TIME: 4 3 .2 SECONDS														
RUN-TIME RATIO: 28/8=3.2														
CORE USED: 5K (9 PAGES)														

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