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DDT	LAB-8	TYPESET-11
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CHAPTER 1

INTRODUCTION

1.1 GENERAL

Minicomputers are changing our world. In banks, hospitals, supermarkets, and factories, people are realizing that computers don't have to be large and expensive to get a job done. A computer is no longer a multimillion dollar giant that can only survive in spotlessly clean, air-conditioned rooms. Minicomputers are going where the job is because they are rugged, dependable, and inexpensive. Industries such as oil refineries and automobile manufacturers are using the power and speed of computers to produce better products. Minicomputers are not just for big business: hospitals, schools, laboratories, and factories are using minis just as effectively. New and old companies are exploring minicomputers.

More than 50,000 DIGITAL minicomputers serve in almost every field of endeavor known to man. The PDP-8/A is DIGITAL's newest model of the PDP-8 family. Existing PDP-8 software can be used with the PDP-8/A. Users may take advantage of the large number of applications programs available from DIGITAL's Computer Users' Society (DECUS) and the full line of real time and operating systems from the DIGITAL Program Library. Existing PDP-8 options and peripherals can be interfaced to the PDP-8/A via the Omnibus connector. We invite you to explore the advantages of owning this small machine with big ideas.

1.2 PDP-8/A FAMILY

The PDP-8/A minicomputer is completely compatible with other PDP-8 computers already at work in locations around the world. The various members of the PDP-8/A family are summarized below:

KIT 8/A—a set of modules consisting of a CPU module and 1K to 16K core, Read Only Memory (ROM), Reprogrammable Read Only Memory (PROM), or Random Access Memory (RAM). The KIT 8/A does not include a cabinet or power supply.

PDP-8/A MINICOMPUTERS. PDP-8/A minicomputers include CPU, memory, etc., in an enclosure containing a power supply and backplane.

8A100. The 8A100 minicomputer incorporates ROM/RAM (see chapter 4) memory combinations which offer complete program integrity for dedicated applications. A new hardware technique enables the user to program ROM/RAM combinations like core memory. The 8A100 system is mounted on a 10-slot backplane and incorporates 1K, 2K, or 4K of RAM and/or 1K, 2K or 4K of ROM up to a total of 32K semiconductor memory.

8A400. The 8A400 minicomputer provides the OEM user with all the capabilities of core memory plus a wide range of peripherals. It utilizes both 8K and 16K stacks and has a 12-slot backplane.

8A420. The 8A420 minicomputer is the same as the 8A400 but incorporates a 20-slot backplane instead of the 12-slot backplane. The enclosure contains the additional power capability required to support the extra module capacity.

8A600. The 8A600 minicomputer incorporates a PDP-8/E processor in a PDP-8/A enclosure and utilizes all PDP-8/A options and memory configurations. The 8A600 offers 1.2 μseconds cycle time as opposed to the 8A400 which offers 1.5 μseconds cycle time. This system optionally offers the Extended Arithmetic Element (EAE) and expansion capability beyond the CPU enclosure.

NOTE

The EAE cannot be used in those systems utilizing a PDP-8/A processor.

8A620. The 8A620 system is the same as the 8A600 system but incorporates a 20-slot backplane instead of the 12-slot backplane. The enclosure contains additional power capability required to support the extra module capacity.

8A800. The 8A800 system (referred to as Super 8), is the newest member of the PDP-8/A family. It provides the user with high-speed, fixed and floating point hardware (FPP8/A) in a dual processor configuration with the PDP-8/A CPU. This new minicomputer performs fixed and floating point computations with up to 17 digit accuracy (60 bit mantissa, 12 bit exponent). The floating point processor performs fixed and floating point arithmetic while the PDP-8/A processor handles other functions such as input/output operations and systems management.

The FPP8/A Floating Point Processor operates in three modes: 24-bit fixed point, 24-bit floating point with 12-bit exponent (36 bits), and 60-bit floating point with 12-bit exponent (72 bits) for extended precision arithmetic. The floating point processor uses a 15-bit address path to allow direct addressing of 32K words of memory.

8A820—The 8A820 (also called Super 8) is similar to the 8A800 but incorporates a 20-slot backplane instead of the 12-slot backplane. The enclosure contains additional power capability and provides for system expansion beyond the 8A800.

DESK BASED SYSTEMS

In addition to the KIT8/A and PDP-8/A minicomputer, DIGITAL offers the following System 800 desk based models with dual floppy disks.

MS800A—contains 8K of core memory

MS800B—contains 16K of core memory

MS880A—contains 8K core in a Super 8 configuration.

MS880B—contains 16K core in a Super 8 configuration

Each of the above desk based systems contains a PDP-8/A, a dual floppy disk drive, two option boards, automatic ROM based diagnostics and the OS/8 operating system. The Super 8 series (8A800, 8A820,

and MS880 desk based system) incorporates a FPP8/A Floating Point Processor.

The FPP8/A operates in parallel with the PDP-8/A CPU. On application of power, the FPP remains stopped until started by the PDP-8/A using IOTs. Once started, the FP uses the data break system to obtain instructions from the PDP-8/A's memory, as needed. The FPP continues to run until the PDP-8 is halted, the 8/A issues a command to halt, or the FPP encounters an exit or pause instruction.

PDP-8/A SPECIFICATION SUMMARY

Word Length:
12 bits

Processor Cycle Time:
1.5 microseconds—KK8-A; 1.2 microseconds—KK8-E

Hardware Registers:
2

Auto-Index Registers:
8 per 4K memory field

Memory:
CORE, 8K, 16K

Memory Expansion:
Up to 32K

Battery Back-up:
Standard on 8A100

Option Boards:
2 option configurations available on single boards.

DKC8-AA

Front panel control	Real-time clock
Serial line unit	Parallel I/O

KM8-AA

Power fail/auto-restart	Timeshare control
Memory extension	Bootstrap loader

Physical Size:
26.52 cm. high by 48.3 cm. wide by 26.04 cm. deep (10.44" by 19.00" by 10.50")

FPP8/A SPECIFICATION SUMMARY

Mechanical:
2 hex modules. Plug into the 8/A OMNIBUS

Calculating Modes:
Double Precision Mode—Fixed point with 24-bit signed 2's complement arithmetic.

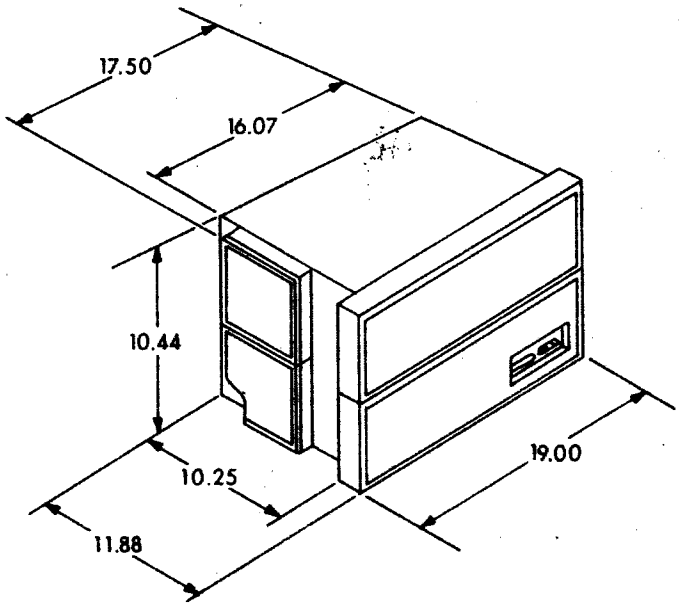
Floating Point Mode—Floating point with 12-bit signed 2's complement exponent, plus 24-bit signed 2's complement fraction. Fraction calcula-

tions are made on a 36-bit word and the result rounded to 24 bits at the end of each arithmetic operation. The FPP is initialized to this mode upon application of power.

Extended Precision Mode—Floating point with 12-bit signed 2's complement exponent, plus 60-bit signed 2's complement fraction. Calculations are carried to 60 bits with no roundoff.

15-Bit Address:
Allows up to 32K of direct addressing.

Omnibus Power:
+5V, 8 Amp. (40w)



H9300 ENCLOSURE

CHAPTER 2

SYSTEM DESCRIPTION

2.1 PDP-8/A BASIC SYSTEM

The PDP-8/A is a general purpose computer. (See figure 2-1). Its development is the successful culmination of many years of computer design research directed toward providing better computers at the lowest possible price. This computer is designed to meet the needs of the average user, yet it is capable of modular expansion to accommodate almost any requirements for a user's specific application.

The PDP-8/A basic processor is a single-address, fixed word length, parallel transfer computer using 12-bit, two's complement arithmetic. Standard features include indirect addressing and facilities for instruction skipping, program interrupts as a function of input/output device conditions, and auto-restart.

Five 12-bit registers are used to control computer operations, address memory, perform arithmetic or logical operations and store data. The registers that are of use to the programmer are the accumulator, multiplier-quotient, status, and program counter. A programmer's console provides switches and indicators that permit convenient monitoring and modification of machine states and major register contents. The PDP-8/A may be programmed locally, using the optional programmer's console, or by means of a console terminal.

2.1.1 Arithmetic Computations

The cycle time (see Table 2-1) of the PDP-8/A yields a computation rate of 333,333 additions per second. Each addition requires 3.0 microseconds, and subtraction requires 6.0 microseconds. Multiplication is performed in 209 microseconds or less, by a subroutine that operates on two signed, 12-bit numbers to produce a 24-bit product, leaving the 12 most significant bits in the accumulator. Division of two signed, 12-bit numbers is performed in 483 microseconds or less by a subroutine that produces a 12-bit quotient in the accumulator and a 12-bit remainder in memory.

2.1.2 Input/Output

The flexible, high throughput and input/output capabilities of the PDP-8/A allow it to operate a great variety of peripheral devices. More than 60 input/output device options including high-speed paper-tape equipment, card readers, line printers, disk and magnetic tape bulk storage devices, and a wide range of data acquisition, transmission, and display peripherals are available from DIGITAL for the PDP-8/A.

2.1.3 Power

Each PDP-8/A system is completely self-contained. A single source of 115 or 230 Vac power is required; internal power supplies produce all the necessary operating voltages for the system. The basic PDP-8/A computer consists of a rack mountable chassis with a power supply, and an Omnibus (backplane) into which the central processor, memory system, and optional programmer's console and console terminal control mount.

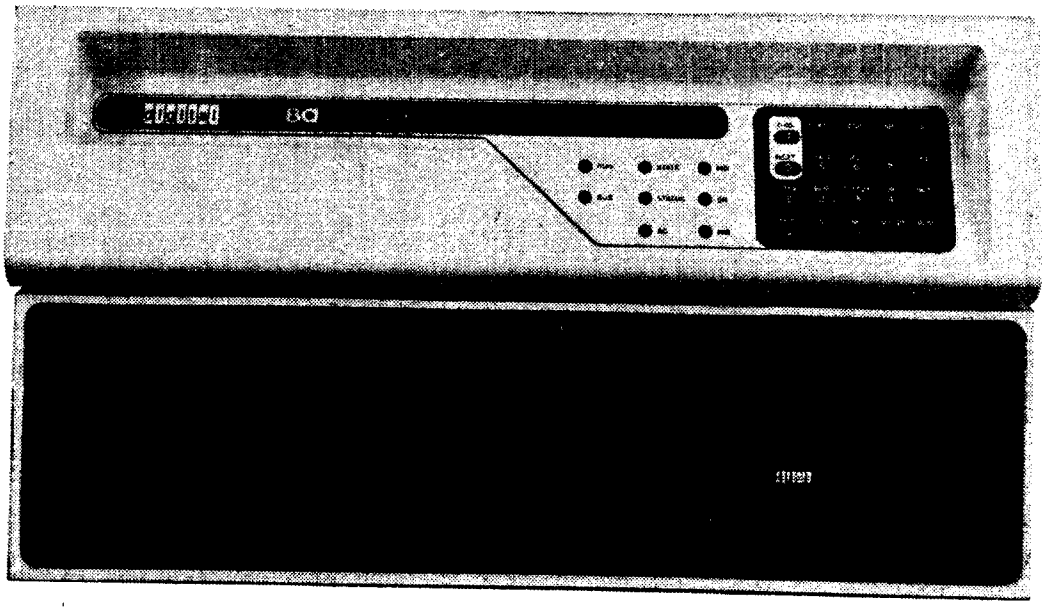


Figure 2-1 PDP-8/A Minicomputer

2.1.4 Omnibus

In the PDP-8/A, a bus is defined as a group of signal lines carrying related information such as the 12 bits of an instruction or data word. The Omnibus is a wide bus containing several smaller buses. Each PDP-8/A Omnibus has one slot for the central processor unit, two slots reserved for the two multi-option boards, and several identical non-dedicated module slots. Each slot will accept a 144-pin quad or hex-sized module. The Omnibus provides two-way signal paths between corresponding pins of the modules that are plugged into it (Figure 2-2).

2.2 CENTRAL PROCESSING UNIT

The central processor unit (CPU) is contained on one 8-1/2 x 15-3/4 in. (21.6 x 40 cm) hex board (Figures 2-3 and 2-4). It contains the major registers and control, instruction decoder, timing generator, auto start logic, and all of the timing and gating circuitry necessary to manipulate data and generate control signals. The major parts of the CPU are described in the following paragraphs.

2.2.1 Accumulator (AC)

The accumulator is a 12-bit register in which arithmetic and logical operations are performed. The accumulator may be cleared, complemented, or incremented under program control, and its contents may be rotated right or left. The contents of the AC may be transferred to memory or the contents of memory may be transferred to the AC. The AC may also serve as an input/output register. All programmed data transfers between memory and I/O devices pass through the AC to data lines located on the Omnibus. I/O transfers performed via data breaks (direct memory access), however, do *not* pass through the AC.

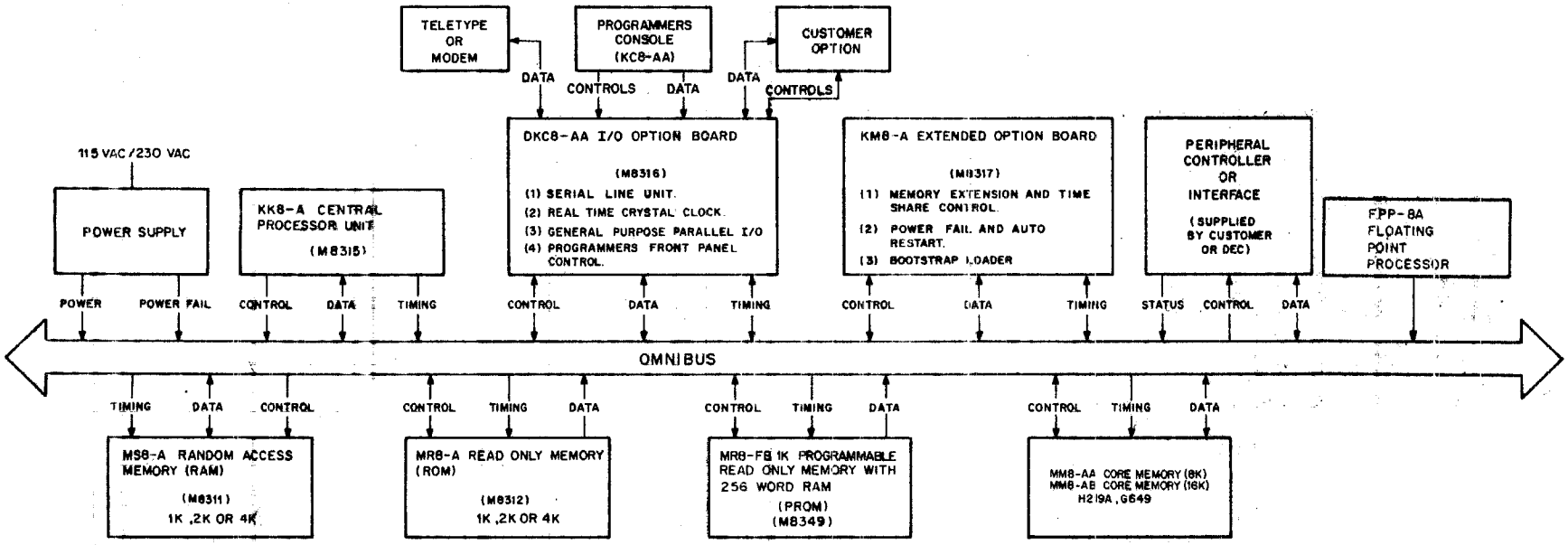


Figure 2-2 PDP-8/A System Block Diagram

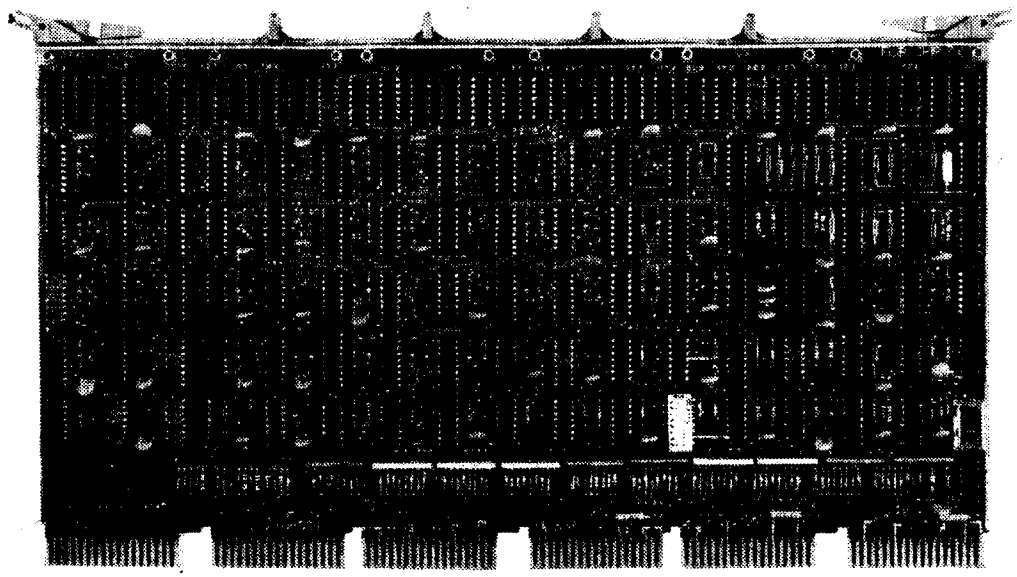


Figure 2-3 PDP-8/A CPU Module (M8315)

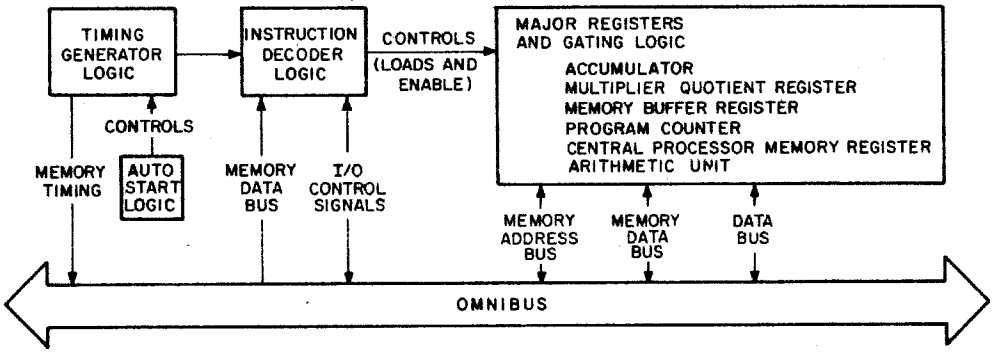


Figure 2-4 Central Processing Unit Block Diagram

2.2.2 Multiplier Quotient Register (MQ)

The multiplier quotient register is a 12-bit register that acts as a temporary storage register for the accumulator.

2.2.3 Link (L)

The link is a 1-bit register that serves as a high-order extension of the AC. It is used as a carry register for two's complement arithmetic. The link may be set, cleared, or complemented under program control. It may also be rotated left or right as part of the accumulator.

2.2.4 Program Counter (PC)

The program counter is a 12-bit register that contains the address of the memory location from which the next instruction will be taken. The PC is automatically incremented by 1 after each instruction is read from memory. It may be incremented, under program control, to conditionally skip the next sequential instruction, or may be loaded from the memory buffer register to cause a programmed jump to a prescribed memory location.

2.2.5 Central Processor Memory Address Register (CPMA)

The CPMA is a 12-bit register that contains the 12 low order bits of the memory address currently selected for reading or writing. The CPMA may be loaded from the memory buffer register, the program counter, or the programmer's console switch register.

2.2.6 Memory Buffer Register (MB)

The MB is a 12-bit register through which all information is transferred between the central processor registers and memory. Data may be read into the MB from any memory location in 0.75 microsecond and re-written at the same location in another 0.75 microsecond. The MB may be loaded from either the AC, the PC, or memory.

2.2.7 Data Gates and Adders

The CPU also contains the gating circuitry necessary to move data from one register to another. At the heart of the data gating circuitry is a 12-bit parallel adder. Information from a register is gated to the adder inputs. The output of the adder serves as data input to the MA, MB, and PC; it is also applied to a set of shift gates, the output of which serves as data input to the AC.

2.2.8 Major Register Control Circuits

The major register control circuits gate timing, data, and control signals to enable the adder input, shift gates, and major register inputs. They also gate timing pulses that regulate data transfers to and from the major registers.

2.2.9 Major State Generator

The major state generator produces the three major processor states (FETCH, DEFER, or EXECUTE) used by the central processor. Each major state corresponds to a signal that is asserted to enable the appropriate register control circuitry. A fourth major state (DIRECT MEMORY ACCESS) is entered when none of the signals produced by the major state generator are asserted. The major state determines which data gating circuits will be enabled during a given memory cycle.

2.2.10 Instruction Decoder

The Instruction Register (IR) decoder decodes the instruction that is currently being executed. The three most significant bits of each instruction are loaded into the IR after the instruction is read from memory. This data is decoded and used to determine which major states will be entered during instruction execution.

2.2.11 Interrupt Control Circuits

The interrupt control circuits comprise the major portion of the interrupt system. This circuitry responds whenever an interrupt request signal is received from an interface controller module. Processor input/output transfer instructions are used to initialize and operate the interrupt system under program control.

2.2.12 Timing Generator Logic

The timing generator logic contains the time pulse generator and other miscellaneous control circuits. The time pulse generator provides four time states, designated TS1 through TS4, four time pulses, designated TP1 through TP4, and five memory timing signals. Each time pulse over-

laps the end of one time state and the beginning of the following time state. The time states are used to initiate sequential, time-synchronized gating operations. The time pulses are used as gating pulses throughout the system. In addition, the power clear pulse generator produces a pulse that resets registers and control circuits during power turn-on and turn-off. This pulse is available to control peripheral devices.

2.2.13 Auto-Start Logic

In many control applications, it is desirable to have the computer start operating upon application of power. Logic and switches on the CPU allow automatic startup at address 0, 200, 400, 1000, 2000, or 4000 in memory field 0 or memory field 7. This logic must be disabled (a disable switch is provided) if the Power Fail/Auto Restart option is activated, or if the user wishes to start the computer manually. The physical setting of the switches from which the starting address is selected is provided in the User's Manual and the Operator's Handbook. Each unit has an Operator's Handbook shipped with it.

2.3 KC8-AA PROGRAMMER'S CONSOLE

The I/O option board contains the circuitry required to connect the PDP-8/A programmer's console to the Omnibus. This console consists of an array of controls and indicators that facilitate computer operation and maintenance. Octal key pad switches provide convenient control of the system by allowing the operator to start and stop program execution, examine and modify the content of memory, select various modes of operation, and load and execute short machine language programs.

2.4 OPERATOR'S PANEL

The operator's panel which is often used without the programmer's console in dedicated applications provides the necessary controls to apply power to the computer and start the bootstrap. A PANEL LOCK switch allows the operator to disable all programmer's console switches that would affect the operation of the program, protecting this program from accidental switch operations.

2.5 MEMORY

The PDP-8/A memory can be configured from read only memory (ROM), random access memory (RAM), or programmable read only memory (PROM), or core memory to meet the user's particular requirements and gain the lowest cost solution to his problem. Memory sizes below 4K, (such as 1K RAM, 1K ROM, and 1K PROM) are allowed, and the memory system can be expanded to 32K provided there is adequate current available from the power supply. Each of the various memory options available is discussed in the following paragraphs.

2.5.1 MM8-A Core Memory

The MM8-AA (8K) and the MM8-AB (16K) are 12-bit random access core memory systems for the PDP-8/A computer.

2.5.2 MS8-A Read/Write Semiconductor Memory (RAM)

The MS8-A is a random access semiconductor memory (RAM) on a single quad board with a capacity of 1K, 2K, or 4K 12-bit words.

2.5.3 MR8-A Read Only Memory (ROM)

The MR8-A is a semiconductor read only memory on a single quad board with a capacity of 1K, 2K, or 4K 12-bit words.

2.5.4 MR8-FB Reprogrammable Read Only Memory (PROM)

The MR8-FB is an ultraviolet-erasable semiconductor memory on a single quad board with a capacity of 1024 12-bit words of PROM and 256 words of read/write memory. Each PROM memory word also has a 13th bit which can be set to one, to address one of the 256 RAM locations. When the 13th bit is one, the eight least significant bits read from a PROM location are used as an address to select one of the RAM locations. This allows the programmer to use instructions that require read/write operations.

2.6 POWER ASSEMBLIES

Three different power assemblies are available in PDP-8/A systems. The assembly is selected based on the type of memory desired and the number of Omnibus slots required. (See Table 2-1.)

2.6.1 G8016 Power Supply

The G8016 power supply module provides +5 Vdc and ±15 Vdc for the semiconductor version of the PDP-8/A Miniprocessor. The supply consists of a quad size board containing all the power generation, and regulation circuitry necessary to provide these voltages. The power available is:

+5 Vdc	20 A	
+15 Vdc	0.75 A	sum ⩽ 1 A
−15 Vdc	0.75 A	

The +5 V supply is derived from a series regulator; ±15 V is obtained from an inverter circuit supplied from the +5 V line. The quad module supply plugs into a dedicated backplane. This backplane contains a circuit which controls the 861 Power Control, and a MASTER/SLAVE switch. In MASTER position, the PDP-8/A controls the 861 to allow the application or absence of ac power to peripherals connected to the 861. In SLAVE position, the PDP-8/A can be controlled from a remote location.

All three dc voltages have automatic battery backup. This backup can sustain *full* CPU operation; not just memory protection. The backup battery consists of four 2V sealed lead-acid cells that are trickle charged by the supply charger. A LED indicator on the operator's panel indicates when the battery is being charged. The batteries are protected from overcharging. As soon as the ac input voltage falls below a predetermined level, battery backup is automatically initiated. The batteries will sustain the CPU and memory for 45 seconds at full load (20 A). This is long enough to guard against noise spikes, power fluctuations, cycle dropouts, brown outs, etc., but not against total power failure. Battery recovery after power outage takes 24 hours after a complete discharge. Battery recovery is linear with respect to time:

Charge Time (hr)	Supported Line Outage (sec)
2	3.75
6	11.25
12	22.5
24	45.0

The 45 second time will cover 95% of all power failures. Tab connections are available on the power supply module for connections of an

extended external battery backup if required. If external batteries are used to extend the period of operation, the user must ensure that an adequate method of cooling the CPU, memory, etc. and the power supply regulator board is provided (since there is no ac present, the fans are not running). Two signals (ac low and battery empty) are sent to the power fail/auto restart section of the extended option board. For more details on the use of those two signals, refer to Chapter 9.

To change the semiconductor machine from 110 Vac to 220 Vac, the line cord set (ac cord) must be changed and a Mate-N-Lok connection must be changed on the power supply backplane. However, the same power supply module is used for both voltages. To change from 50 Hz to 60 Hz, the power transformer jumpers must be changed; but, as in the voltage conversion, the same power supply module is utilized.

2.6.2 G8018 Power Supply Module

The G8018 module supplies power for core memory systems for the PDP-8/A. It differs from the semiconductor power supply module in that more power is available.

+5 V	25 A
+15 V	2 A
−15 V	2 A
+20 V	3.5 A
−5 V	2 A

Moreover, there is no battery backup needed for core memory; therefore, none is provided on this supply. Both the semiconductor and the core power supplies use the same type backplane as described in the previous paragraph; however, their power transformers are different. The same rules apply to changing from 110 Vac to 220 Vac or from 50 Hz to 60 Hz as apply to the semiconductor power supply. However, to change a core power supply from 60 Hz to 50 Hz, the power transformer must be changed.

NOTE

The G8016 and G8018 power supply modules are not interchangeable. The semiconductor supply will operate only in the semiconductor chassis and Omnibus.

Table 2-1 PDP-8/A Family Primary Power Assemblies

COMPUTER TYPE	BASE POWER ASSEMBLY	POWER ASSEMBLY INCLUDES
PDP-8/A	H763 Power Supply Assembly	H9192 Omnibus (10 module slots) G8016 Power Supply Module (Semiconductor Memory) Power Board Transformer Assembly Line Set Operator's Panel

Table 2-1 PDP-8/A Family Primary Power Assemblies (Cont.)

COMPUTER TYPE	BASE POWER ASSEMBLY	POWER ASSEMBLY INCLUDES
8A100 8A400, 8A600, 8A800	H9300 Chassis Assembly	H9194 Omnibus (12 slots) G8016 Power Supply Module (Semiconductor Memory) G8018 Power Supply Module (Core Memory) Transformer Assembly Line Set Operator's Panel
8A420, 8A620, 8A820	BA8-C Expander Chassis Assembly	H9195 Omnibus (20 slots) 2 G8018 Power Supply Modules (Core Memory) Transformer Assembly Line Set Operator's Panel Power Distribution Assembly

2.7 INTERFACING

The PDP-8/A Omnibus is an internal input/output bus designed to provide convenient access to data and control signals.

The KA8-E positive I/O bus interface provides an extension to the bus system that facilitates interfacing PDP 8 family positive bus equipment with the PDP-8/A. The positive I/O bus was designed for use with PDP-8/I and PDP-8/L compatible peripherals, but it may be employed with almost any positive bus equipment.

PDP-8/A systems provide three types of data transfer: programmed data transfers, program interrupt transfers, and direct memory access transfers. Programmed data transfer is the easiest to implement and is the most direct method of handling data I/O. Program interrupt transfers provide an extension of programmed I/O capabilities by allowing the user to more easily structure his programmed I/O to handle multiple devices. The data break system uses direct memory access for applications involving extremely fast data transfer rates.

The Omnibus provides access to 96 data and control signals. Interfacing is accomplished by inserting modules into the non-dedicated slots. Chapter 7 contains a complete description of the Omnibus and Chapters 8 and 9 contain the information required to select an interface for the PDP-8/A. The PDP-8/A User's Manual contains a detailed description of the Omnibus and its signals.

2.8 MODULE OPTIONS

The PDP-8/A has two multi-option hex modules available, the DKC8-AA and the KM8-A. Each of these modules and the options provided by them are discussed in the following paragraphs and more fully described in Chapter 9.

2.8.1 DKC8-AA I/O Option Board (M8316)
The M8316 Module is an I/O option which contains a serial line unit (SLU), a real-time crystal clock, a general purpose 12-bit parallel I/O, and interface logic for the programmer's front panel control.

2.8.2 KM8-A Extended Option Board (M8317)
The KM8-A module contains the memory extension and timeshare control, the power fail and auto restart, and the bootstrap loader options.

2.9 PERIPHERAL OPTIONS
Digital Equipment Corporation designs and manufactures many of the PDP-8A peripheral devices and consequently can offer reliable equipment, low prices, and quantity discounts. All peripheral options purchased from DIGITAL include the necessary cables, controllers, interfaces, etc., required for system operation. Most options can be added to the system by simply inserting the modules into the Omnibus and connecting cables between the modules and the peripherals.

A wide variety of input/output and mass storage devices are available for the PDP-8/A and are described in Chapter 9.

2.10 SUMMARY OF PDP-8/A SPECIFICATIONS
Table 2-2 lists the specifications for the PDP-8/A family of computers.

Table 2-2 PDP-8/A Functional Characteristics

Type: Single address, fixed word length, parallel transfer programmed data processor.

Word Length: 12 bits.

Cycle Time:

MEMORY TYPE	CYCLE TIME (μsec) FETCH MAJOR STATE	ALL OTHER STATES
ROM only	1.5	1.5
ROM/RAM (ROM cycle)	1.6	1.6
ROM/RAM (RAM cycle)	2.7	3.1
RAM only	2.4	2.8
Core memory (with KK8-A CPU)	1.5	1.5
Core memory (with KK8-E CPU)	1.2	1.4

Memory Types:

RAM	1K, 2K, 4K
ROM	1K, 2K, 4K
PROM	1K
Core	8K or 16K words

Memory Expansion: Up to 32K
Hardware Registers: 2 (AC and MQ)

Auto Index: 8 auto index registers per 4K memory field.

Addressing Capability: One instruction may address 256 locations directly or 4096 locations indirectly.

Instruction Set: 5 memory reference instructions, jump instruction, one microprogrammable operate instruction, one microprogrammable input/output transfer (IOT) instruction for the CPU and up to 60 I/O devices.

Instruction Execution Time:

Operate microinstruction	1.5 μsec*
Directly addressed MRI	3.0 μsec*
Indirectly addressed MRI	4.5 μsec*

Input/Output Capability: Programmed data transfer, program interrupt system transfer, and 12 channels of direct memory access (data break).

Auto Start Feature: The CPU contains circuitry to start the CPU at one of six switch selectable addresses upon application of power.

Options: Two new option boards.

1. DKC8-AA
   Front Panel Control
   Serial Line Unit
   Parallel I/O
   Real Time Clock
2. KM8-AA
   Power Fail Auto Restart
   Memory Extension
   Timeshare Control
   Bootstrap Loader

Size:

Small Enclosure (H9300-B)
19 x 10.5 x 10.5 inches
(48 x 27 x 27 cm.)

Large Enclosure (BA8-C)
19 x 10.5 x 23.75 inches
(48 x 27 x 60.3 cm.)

Weight:

Small Enclosure (H9300-B)
55 lb. (25 kg.) with full complement of modules.

Large Enclosure (BA8-C)
115 lb. (52.21 kg.) with full complement of modules.

Operating Environment:

Ambient Temperature	41° to 122° F 5° to 50° C
Relative Humidity	10% to 95% maximum, non-condensing wet bulb 32° C (90° F)

Power Requirement: Small Enclosure (H9300-B)
Approximately 450 w. maximum
Large Enclosure (BA8-C)
Approximately 1200 w. maximum
(Voltage and frequency specified at time of order).

* Times reflect 1.5 μsec memory cycle.

CHAPTER 3

FPP8/A FLOATING POINT PROCESSOR

3.1 GENERAL

The FPP8/A is a floating point processor (FPP) that is designed to be used with Omnibus-equipped PDP-8 computers. It provides the PDP-8 Central Processor Unit (CPU) with a hardware option that implements floating point arithmetic and avoids the necessity of writing complex software routines.

The FPP8/A consists of two hex-size printed-circuit modules that plug directly into the Omnibus, as illustrated in Figure 3-1. The modules are inter-connected by a signal cable, with no external connections necessary. Power requirements for the FPP8/A are 8.5A. at +5 Vdc. The FPP8/A uses the data break system of the PDP-8 to obtain instruction words and to obtain and store operands; thus, both processors run simultaneously, sharing common memory.

In addition to its physical and electrical compatibility with the Omnibus, the FPP8/A features instruction-set compatibility with the FPP12/A and will support OS/8 FORTRAN IV.

3.2 FLOATING POINT NUMBERS

The FPP8/A performs calculations on fixed point and floating point numbers. The utility of the floating point numbering system lies in its ability to express extremely large or small numbers in a relatively small number of bits by using scientific notation. In one form of scientific notation, a number is represented by a mantissa (number greater than or equal to 1 and less than 10) multiplied by an exponent (10 raised to a power).

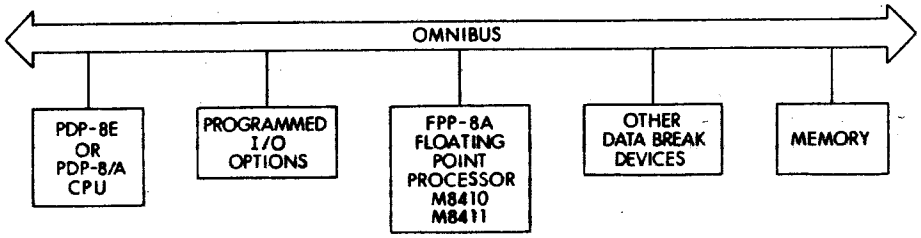


Figure 3-1. PDP-8/A Block Diagram

For example, the speed of light is 186,000 miles per second. Thus, this number could be expressed as 1.86×10^5 miles per second.

When numbers are expressed in scientific notation, two parameters are involved. The first of these parameters is the range of the number. which is represented by an exponent. If the exponent is limited to two decimal digits, the largest number that can be expressed using scientific notation is $9.999 \ldots\ldots \times 10^{99}$. Similarly, the smallest number expressable is $1.000 \ldots\ldots 10^{-99}$. Hence, the range is determined by the maximum and minimum values of the exponent; the number of digits

following the decimal point in the mantissa is of little consequence in determining the range. The second parameter that must be considered is the **precision** of the mantissa which can be increased by using a greater number of digits (for example, representing pi as 3.14159 instead of 3.14).

Binary floating point numbers are expressed in a manner similar to the scientific decimal notation described above. A number is expressed as a signed binary fraction multiplied by the base 2 which is raised to a signed exponent. Figure 3-2 shows a binary floating point number as it would appear in the FPP8/A with both the fraction and the exponent comprising 12 bit positions.

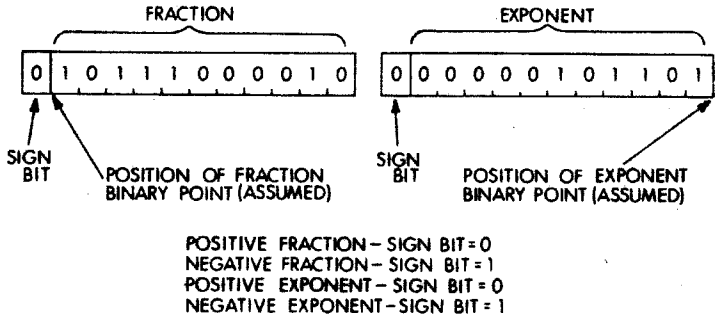


Figure 3-2. Floating Point Representation

The binary fraction is normalized when the absolute value of the binary fraction is greater than or equal to ½ (decimal) and less than 1. Consequently, in the above example the bit position immediately to the right of the binary point must be a 1.

NOTE

The decimal fractional value of each binary fraction bit position is indicated below.

Decimal fraction	½	¼	⅛	1/16	. . . etc . . .
Binary fraction	.1	1	1	1	. . . etc . . .

An unnormalized fraction can be normalized by left shifting it until the bit immediately to the right of the binary point is a 1. Each left shift is accompanied by a subtraction of one from the exponent in order to preserve the original magnitude of the number. For example, consider the unnormalized floating-point number shown below.

FRACTION	EXPONENT
0.00 100 000 111	000 000 001 001

To normalize the fraction, it must be left shifted two places. This is done as follows with each left shift accompanied by a subtraction of 1 from the exponent.

	FRACTION	EXPONENT
First Shift	0.01 000 001 110	000 000 001 000
Second Shift	0.10 000 011 100	000 000 000 111

In the PDP-8/A, positive normalized fractions are represented as 0.1 . . . while negative normalized fractions are represented as 1.0 . . . . Note that in both cases, the two most significant digits are different. There are two exceptions to this. One is the fraction of 0.00 000 000 000 which is considered to be normalized and the other is the negative fraction equal to $\frac{1}{2}$. This number is represented as 1.10 000 000 000 and is also considered normalized.

3.3 ARITHMETIC OPERATIONS

The rules of exponent operations in algebra also apply to binary floating point arithmetic. Addition and subtraction require that the exponents of the two numbers be made equal. When the exponents are made equal, the two operands are added or subtracted. The common exponent is affixed to the result and the result is then normalized. The process of making exponents equal is called alignment. In the FPP8/A, aligning is accomplished by right-shifting the fraction having the smaller exponent. The number of right shifts needed is equal to the difference between the original exponents. The example below is a subtraction operation with the operands having different exponents.

$$(2.0300 \times 10^3) - (1.02 \times 10^1)$$

Since the exponents are different they must be aligned by right shifting the fraction having the smaller exponent.

$$1.02 \times 10^1 = .102 \times 10^2 = .0102 \times 10^3$$

Now the exponents are equal and one fraction can be subtracted from the other.

$$(2.0300 \times 10^3) - (.0102 \times 10^3) = 2.0198 \times 10^3$$

Normalization is not needed in this particular example since the result is already in standard format. Generally, the more alignment required, the less normalization needed. The FPP8/A automatically aligns, adds or subtracts, and normalizes whenever a floating point add or subtract is executed.

In floating point multiplication, the multiplier and multiplicand are multiplied and the exponents are added. In floating point division, the dividend is divided by the divisor (being careful to avoid division by zero) and the exponent of the divisor is subtracted from the exponent of the dividend to obtain the exponent of the quotient. In both cases, the result is placed in standard format (result is normalized). The FPP8/A performs this entire operation upon receipt of a multiplication or division command.

3.4 FPP8/A NUMBERS AND CALCULATING MODES

A floating point number in the FPP8/A consists of a 12-bit, 2's-complement exponent, plus a 24-bit or 60-bit, 2's-complement fraction. The 12-bit exponent allows direct representation of decimal exponents to $10^{\pm 620}$ (corresponding to binary exponents in the range 2^{+2047} to 2^{-2048}). For most applications, a 24-bit fraction (allowing 6 to 7 decimal digits of precision) is adequate. For those applications requiring greater precision, the 60-bit fraction allows 17 decimal digits of precision.

The FPP8/A employs three calculating modes (see figure 3-3).

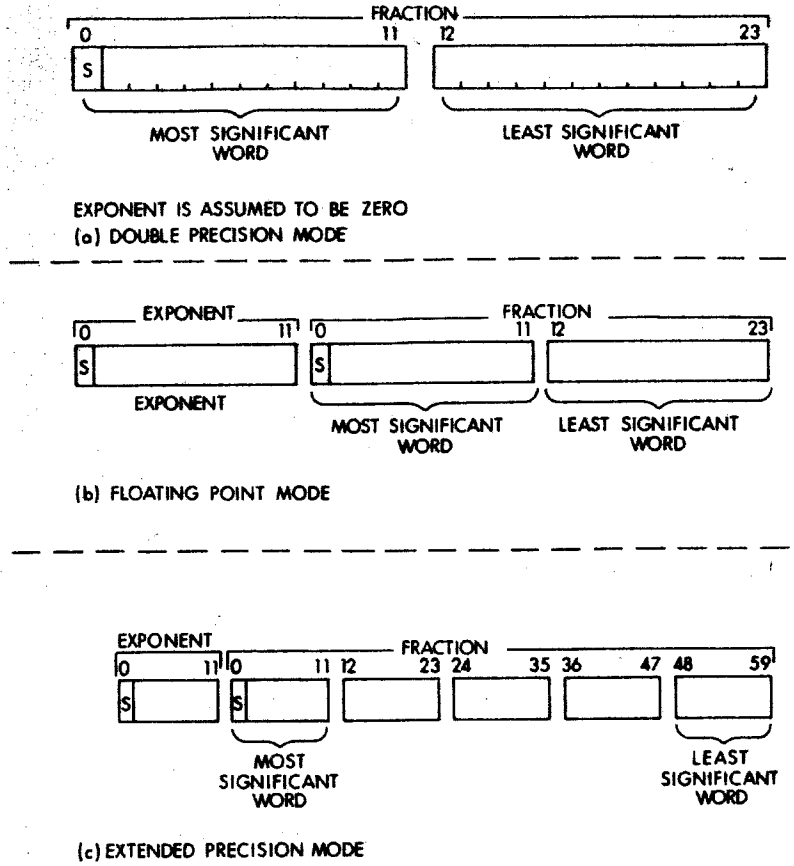


Figure 3-3. FPP8/A Floating Point Formats

a. The Floating Point (FP) mode performs floating point arithmetic with a 12-bit, signed, 2's-complement exponent plus a 24-bit, signed, 2's-complement fraction. Fraction calculations are made on a 36-bit word, and the result is rounded off to 24 bits at the end of each arithmetic operation. The FPP is initialized to this mode of application of power.

b. The Extended Precision (EP) mode performs floating point arithmetic with a 12-bit, signed, 2's-complement exponent plus a 60-bit, signed, 2's-complement fraction. Calculations are carried to 60 bits with no roundoff.

c. The Double Precision (DP) mode performs fixed point arithmetic with a 24-bit, signed, 2's-complement fraction. This mode is the same as the FP mode, except that the exponent is ignored and treated as if it were always zero.

In the DP mode (for multiply and divide operations only) or the FP mode (for all arithmetic operations), calculations are carried to 36 bits, although only 24 bits are retained as the answer. If the result is positive, 4000_8 is added to the 12 least-significant bits. If the result is negative, 3777_8 is added to the 12 least-significant bits. In either case, any resulting carry is propagated to the 24 most-significant bits to cause roundoff.

In the DP mode, any calculation which results in 4000 0000_8 as an an-

swer or which causes an overflow, sets the DP OVERFLOW bit in the Status Register. At the conclusion of the current calculation, this bit causes the FPP to exit. In the FP or EP mode, a result of 4000 0000_8 is converted to 6000 0000_8 with a corresponding increase of exponent. 4000_8 is, however, considered to be a legal value for the exponent. Calculations which result in an exponent overflow set the EXPONENT OVERFLOW bit in the status word and cause an exit at the end of the current instruction. Calculations which result in exponent underflow will either cause an exit or be stored as a zero result, depending upon the state of bit 1 (the ZTRAP bit) of the Command Register. Except for underflow which is stored as zero, the FPP completes the calculation and stores the erroneous result.

3.5 FPP8/A INITIALIZATION

The FPP8/A operates in parallel with the PDP-8/A CPU. When power is applied to the system, the FPP remains stopped until started by IOT instructions issued by the CPU. After the FPP has been started, it obtains instructions and operands, as necessary, from the PDP-8 memory by data break transfers. Two operating modes are available: interleaved and lockout. Interleaved operation permits the FPP to use every other memory cycle for data break transfers allowing the PDP-8 CPU to run at half speed (providing no higher priority data break device assumes control). Lockout operation permits the FPP to use every memory cycle, providing a request for interrupt servicing is not made by another system device. In both modes, higher priority DMA transfers take precedent over FPP cycles.

Two IOT instructions must be issued to start the FPP after the system is turned on. The joint action of the FPCOM instruction and the FPST instruction causes a 15-bit address to be loaded into the FPP hardware from the PDP-8 AC Register. This address represents the starting location in the PDP-8 memory of the FPP's Active Parameter Table (APT, Table 3-1), which consists of a number of consecutive memory locations that contain initializing information for several FPP registers. The information in the APT is loaded into these registers, one of which is the Floating Program Counter (FPC). Then, the FPP starts executing floating point instructions at the PDP-8 memory address specified by the contents of the FPC. When floating point calculations are finished, the APT is updated by the FPP during the exit operation and the FPP flag is set.

The APT can occupy as many as 11 consecutive locations in the PDP-8 memory. These 11 locations contain the information listed in Table 3-1. If the FPCOM instruction has directed a fast start (refer to the FPCOM instruction description), only the information in locations 1 and 2 is loaded into the FPP hardware; if a normal start is programmed, the information in either the first 8 locations (DP or FP mode selected) or all 11 locations (EP mode selected) is obtained by the FPP.

3.6 IOT INSTRUCTIONS

The PDP-8 IOT instructions relating to the FPP8/A are listed and described in Table 3-2. All IOT instructions require one memory cycle. The FPP8/A has device codes of 55 and 56.

Table 3-1. FPP8/A APT Contents

SEQUENCE OF MEMORY LOCATIONS	CONTENTS OF LOCATION
1	FIELD BITS Bits 0-2 = operand address field Bits 3-5 = base register field Bits 6-8 = index register address field Bits 9-11 = FPC field
2	FPC (Floating Program Counter) 12 low-order bits
3	Index register address—12 low-order bits
4	Base register—12 low-order bits
5	Operand address—12 low-order bits (this word is ignored upon FPP start-up, but is filled upon FPP exit).
6	FAC exponent
7	FAC bits 0-11
8	FAC bits 12-23
9	FAC bits 24-35*
10	FAC bits 36-47*
11	FAC bits 48-59*

* EP mode only

Table 3-2. FPP8/A IOT Instructions

OCTAL CODE	MNEMONIC	DESCRIPTION
6551	FPINT	Skip if the FPP-8A flag is set
6552	FPICL	Produces same results as issuing initialize on the Omnibus. Initialize the FPP—clear flag, enable interleaved operation, stop the FPP, enable FP mode, clear all status register flags. The APT pointer is not changed.
6553	FPCOM	If the FPP is not in a run state and the FPP flag is not set, the FPP command register is loaded with the contents of the PDP-8 AC. The AC is not changed

Table 3-2. FPP8/A IOT Instructions (Cont.)

OCTAL CODE	MNEMONIC	DESCRIPTION
		by this IOT. If the FPP is in a run state or if the FPP flag is set, the FPCOM instruction is ignored. AC0 = 0—Select FP mode AC0 = 1—Select DP mode AC1 = 0—If exponent underflow occurs, make result of calculation = 0 and continue. AC1 = 1—If exponent underflow occurs, exit. AC2 = 0—Normal addressing AC2 = 1—Forbid access to 4K memory fields other than the one occupied by the last location of the APT. AC3 = 0—Disable FPP interrupt. AC3 = 1—Enable FPP interrupt. AC < 4:7 > = 17—Obtain and restore only the FPC on entry and exit. All other FPP registers retain their previous values. The most-significant field bits of the APT are ignored on entry and cleared upon exit. This mode of operation provides an extremely fast (2 cycle) start and exit, but sacrifices generality. AC < 4:7 > not 17—Obtain entire APT upon startup except for operand address. Restore entire APT upon exit, including operand address. AC8 = 0—Interleaved operation AC8 = 1—Lockout operation AC < 9:11 >—Most-significant 3 bits of APT pointer.
		NOTE Upon application of power, the APT pointer is undefined.
6554	FPHLT	Force the FPP to exit, dump its status in the APT, set the forced exit bit in the status word, and set the FPP flag at the end of the current instruction. The following special features apply: 1. If FPHLT is issued prior to FPST,

Table 3-2. FPP8/A IOT Instructions (Cont.)

OCTAL CODE	MNEMONIC	DESCRIPTION
		the FPP will single-step. FPHLT must be issued after FPIST (or FPICL) and before FPST for each instruction the FPP is to single-step. 2. If the FPP is currently in pause (result of FPAUSE instruction), the FPC will be decremented at exit. 3. If FPHLT and FEXIT occur at virtually the same time (causing a common exit), the status bit indicating forced exit (bit 2) will be cleared.
6555	FPST	If the FPP is not running and the FPP. flag is not set, the contents of the AC are loaded into the 12 least-significant bits of the APT pointer and the FPP is started. If the FPP is in the run state but paused, the FPST instruction will cause the FPP to continue. If the FPST instruction causes the FPP to start or continue, the next PDP-8 instruction is skipped. Unless the above conditions are met, the FPST instruction has no effect on the FPP and the PDP-8 skip does not occur.
6556	FPRST	Read (jam transfer) the FPP status register into the PDP-8 AC. The FPRST IOT may be issued at any time. Status Word: AC0 = 0—FP or EP mode AC0 = 1—DP mode AC1 = 1—Trapped instruction caused exit. AC2 = 1—FPHLT instruction caused exit. AC3 = 1—Attempted divide by 0 caused exit. The FAC was not altered. AC4 = 1—Fraction overflow in DP mode caused exit. AC5 = 1—Exponent overflow caused exit. AC6 = 1—Exponent underflow has occurred. Exit on underflow is optional.

Table 3-2. FPP8/A IOT Instructions (Cont.)

OCTAL CODE	MNEMONIC	DESCRIPTION
		AC7 = 1—FADDM or FMULM instruction AC8 = 0—Interleaved operation AC8 = 1—Lockout operation AC9 = 1—EP mode AC10 = 1—FPP is currently paused. AC11 = 1—FPP is currently in a run state.
6557	FPIST	Skip if the FPP flag is set. If the skip occurs, read the FPP status register (defined above) into the PDP-8 AC, clear the status bits and the FPP flag.
6567	FPEP	Select EP mode if AC0 = 1 and the FPP is not in the run state. Then clear the AC. This command must be issued after the FPCOM (6553) IOT if EP mode is desired.

3.7 FPP INSTRUCTIONS

There are two basic classes of floating point instructions: data reference instructions and special instructions. Data reference instructions perform arithmetic operations on specified data and transfer data between memory and the Floating Accumulator (FAC). Special instructions cause jumps, branches, Index Register modifications, pointer moves, manipulations of the FAC, and various housekeeping movements (e.g., alignment and normalization).

The 10 data reference instructions are listed in Table 3-3, along with a description of each. The operation carried out by each instruction is noted in the OPERATION column. For example, the FLDA instruction causes the operand (i.e., the contents, "C," of the effective address, "Y") to be loaded into the FAC. Each of the instructions, except LEA and LEAI, can use any one of 3 modes to specify the effective address. The format of these modes is illustrated in Figure 3-4. Bits 0, 1, and 2 (which represent the op code) identify the instruction, while bits 3 and 4 identify the mode of addressing. The remaining bits of each instruction determine the operand address, as described by the equations below each format. For example, the operand address for the single-word, direct reference format is derived by multiplying bits 5 through 11 by 3 and adding the result to the 7 (or 8, since the product might overflow) least-significant bits of the base address.

3.8 ADDRESSING FORMATS

The three addressing formats (single word direct reference, double word

direct reference, and single word indirect reference) formats are described below.

3.8.1. Single Word Direct Reference Format

The single word, direct reference format is employed when the operand is stored on the base page, which consists of a block of 384 12-bit locations. The origin of the base page is determined by the base address, which can be changed at any time; thus, the base page can encompass a block of locations anywhere in memory. The base address is contained in the Base Register, which is initially set from the APT and which can be changed with the SETB (Set Base Register) instruction. Data on the base page is stored in the FP format; thus, the operand consists of 3 12-bit words; the 12-bit exponent followed by the 24-bit fraction. Consequently, 128 operands are available on the base page. The relative address of any operand exponent can be specified by multiplying the 7 offset bits by 3. When this quantity is added to the base address, the location of the operand exponent is completely identified.

3.8.2. Double Word Direct Reference Format

The double word, direct reference format allows one to specify the 15-bit absolute address of an operand. In addition, this format permits address indexing, which simplifies programming techniques like loop counting and manipulation of push-down stacks.

Address indexing is accomplished by using the contents of an index register to modify the 15-bit absolute address specified by the data reference instruction. There are 8 consecutive 12-bit locations in the PDP-8 memory that are designated as FPP Index Registers. The address, X0, of the first of these registers is provided initially by the APT, but can be changed by the special SETX instruction whenever necessary.

Bits 6. 7, and 8 (XR bits) ofg the double word, direct reference instruction identify Index Registers 0 through 7 in octal notation. If Index register 0 is designated, no indexing is to be performed. Instead, the operand absolute address is given by bits 9-23 of the instruction, and the contents of Index Register 0 may or may not be incremented. However, if an index register other than 0 is specified, the 15-bit absolute address is modified by the contents of the selected index register; note that the contents of the register may or may not be incremented before the operand address is calculated.

3.8.3. Single Word Indirect Reference Format

Indexing is also permitted by the single word, indirect reference instruction. Once again, bits 6, 7 and 8 identify the index register that will be used in an address modification. However, in this case, the address is specified indirectly, using the base address as the point of reference. As before, bit 5 of the instruction determines if the contents of the index register are incremented.

3.9 SPECIAL INSTRUCTIONS

The FPP special instructions are listed in Table 3-4. The op code for each instruction is included and a description of the function is provided.

Table 3-3. Data Reference Instructions

MNEMONIC	OP CODE	OPERATION	DESCRIPTION
FLDA	0	C(Y) → FAC	The contents of the effective address are loaded into the FAC.
LEA LEAI	6 7	Y → FAC	The effective address (not its contents) is loaded into the FAC (available only in FP and EP modes). LEA and LEAI are available only in EP and DP modes. LEA and LEAI have only one addressing mode available to each—the double word, direct reference for the LEA instruction, and the single word, indirect reference for the LEAI instruction. Each operation is begun similarly, i.e., the address calculation is performed in whichever mode has been programmed; however, when the address calculation for LEA and LEAI is complete, the FPP loads the operand address into the FAC and then switches to DP mode. In DP mode, the LEA and LEAI instructions are replaced by IMUL and IMULI respectively.
IMUL IMULI	6 7	C(FAC)*C(Y) → FAC	Integer multiply. An address calculation is accomplished, and then an integer multiply is performed between the contents of the effective address and the FAC. The 24-bit result is loaded into the FAC. The old FAC is the multiplier; the contents of the effective address is the multiplicand. The operation is similar to FMUL, except that the binary point is assumed to be to the right of bit 23. Any propagation of bits out of bit 0 are lost. A continuous check of overflow is maintained. Available only in DP mode.

Table 3-3. Data Reference Instructions (Cont.)

MNEMONIC	OP CODE	OPERATION	DESCRIPTION
FADD FSUB	1 2	C(Y) + C(FAC) → FAC C(FAC) — C(Y) → FAC	The contents of the effective address are added to or subtracted from, the contents of the FAC. In DP mode, no alignment or post-normalization occurs. The 24 bits from memory are combined with the 24 MSB of the FAC, and bits 24 through 35 of the FAC are unchanged. In FP or EP mode, the two words are aligned by right-shifting the word with the lesser exponent until the two exponents are the same (providing this can be done in 24 or 60 bits). Bits shifted out of the least-significant end of the word are lost. The two fractions are then added or subtracted, using either the 36 MSB (FP) or all 60 bits (EP) of the FAC. The result is normalized by shifting the result left until its first two bits are different, and decrementing the exponent for each shift. 0 is shifted into the least-significant bit. The result is then rounded. If either argument is 0, or if the exponent is of such a value that alignment will shift the word completely out of the register, no shifting occurs. Under these circumstances, the FAC is either cleared, or loaded with the contents of the effective address.
FDIV FMUL	3 4	C(FAC)/C(Y) → FAC C(FAC)*C(Y) → FAC	The old contents of the FAC are the multiplier or dividend; the contents of the effective address are the multiplicand or divisor. In FP or EP mode, the exponent is calculated, and the 36 (FP or DP) or 60 (EP) MSB of the fraction of product or quotient are placed in the FAC. Lesser bits or product, or the division remainder are lost. In DP or FP mode, the result is rounded to 24 bits.

Table 3-3. Data Reference Instructions (Cont.)

MNEMONIC	OP CODE	OPERATION	DESCRIPTION
			In EP mode, the operation takes place in such a way that a true truncated result occurs. (i.e., No significant bits are lost by post-normalization, but no roundoff takes place.) For floating point division, the hardware normalizes the divisor (if it is not already normalized) before division starts, thus guaranteeing that divide overflow will not occur.
FADDM FMULM	5 7	C(Y) + C(FAC) → Y C(FAC)*C(Y) → Y	The descriptions of FADD and FMUL apply equally to FADDM and FMULM, with these exceptions: the FAC contents are not changed by FADDM or FMULM; the computation result is stored at the effective address.
FSTA	6	C(FAC) → Y	The contents of the FAC are stored at the effective address, the FAC remaining unchanged.

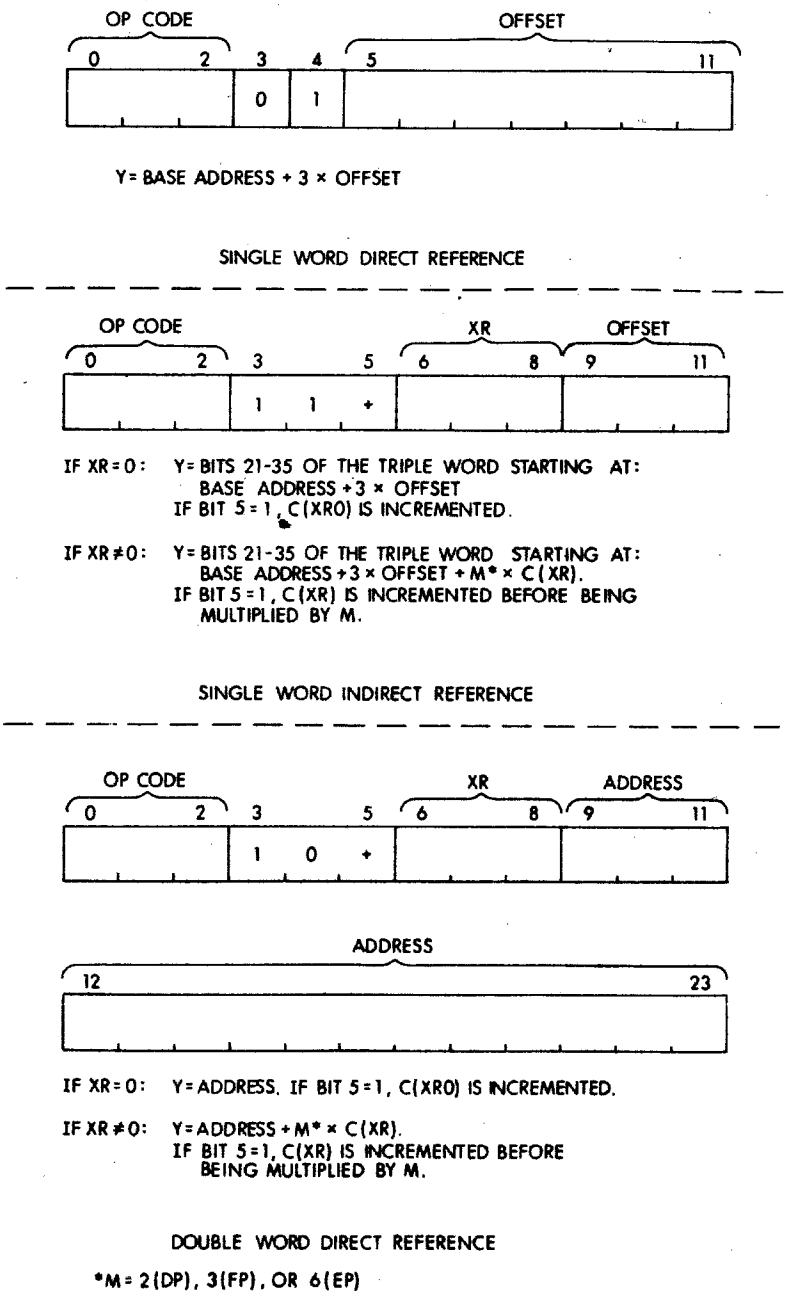


Figure 3-4. Data Reference Instruction, Addressing Mode Formats

Table 3-4. FPP Special Instructions

Mnemonic	OP Code										
	0	1	2	3	4	5	6 — 8	9	10	11
LTR	1	0	1	0	0	0	COND	X	X	X

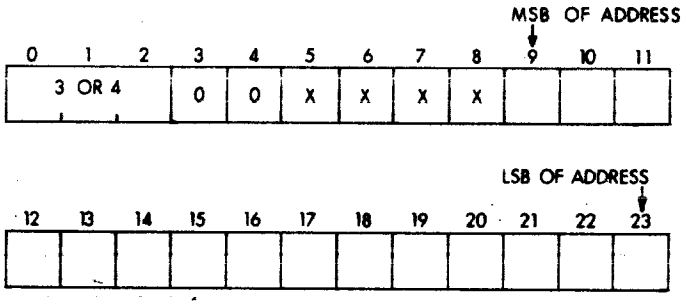
X = DON'T CARE

Function
Load Truth—If the condition is met, +1 (2000 0000 in DP mode) is loaded into the FAC. If the condition is not met, the FAC is cleared.

Conditions:	Octal	Meaning
	0	FAC = 0
	1	FAC greater than or equal 0
	2	FAC less than or equal 0
	3	Always
	4	FAC not equal 0
	5	FAC less than 0
	6	FAC greater than 0
	7	FAC Exponent greater than 27 (octal)

Mnemonic **OP Code**

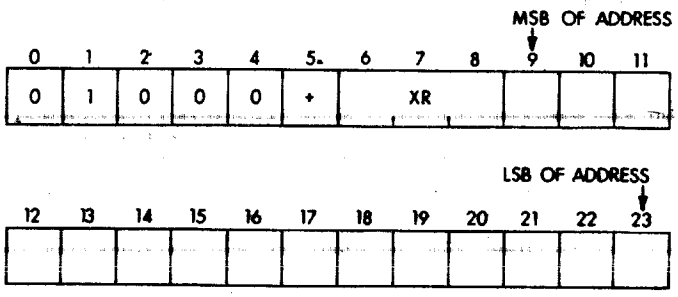
TRAP 3, TRAP 4



Function
Trapped Instructions—The instruction trap status bit is set, and the FPP exits. The 15-bit address is placed in the APT.

Mnemonic **OP Code**

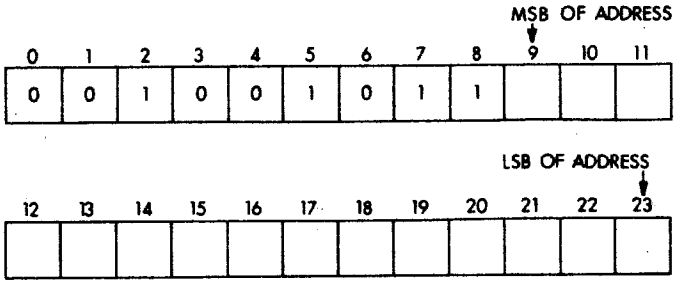
JNX



Function
Jump if Index Register is Non-Zero—The specified index register is incremented if bit 5 = 1. If the (incremented) address register is not 0, bits 9-23 are loaded into the FPC, causing a jump.

Mnemonic **OP Code**

JSR

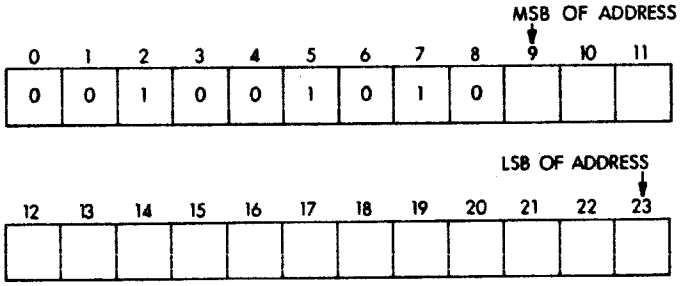


Function

Jump and Save Return—The current FPC is stored in bits 21-35 of the triple word starting at the base address. Bits 0-11 of this triple word are not modified; bits 12-20 are loaded with "103" (JA instruction). Bits 9-23 of the instruction are then loaded into the FPC.

Mnemonic **OP Code**

JSA

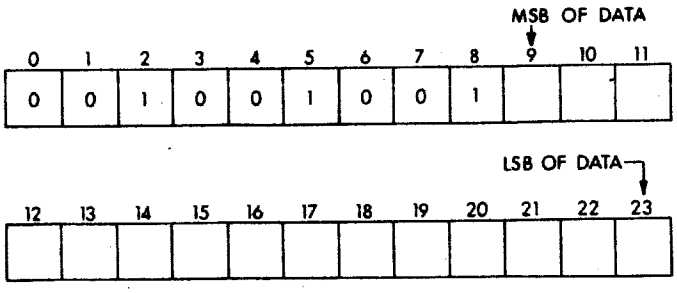


Function

Jump and Save at Address—An unconditional jump to the address presently in the FPC (JA = 103X XXXX) is deposited at the double-word starting at the address specified by bits 9-23 of the instruction. The FPC is then changed to equal 2 + bits 9-23 of the instruction.

Mnemonic **OP Code**

SETB

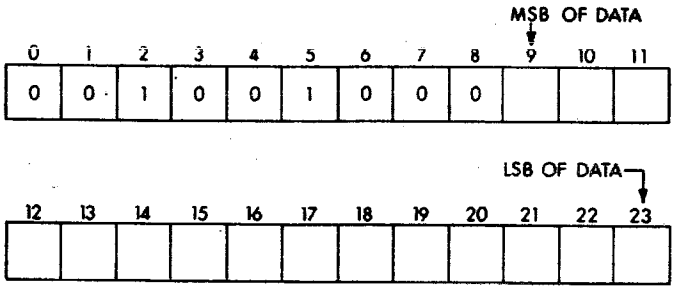


Function

Set Base Register—Bits 9-23 are loaded into the BR.

Mnemonic **OP Code**

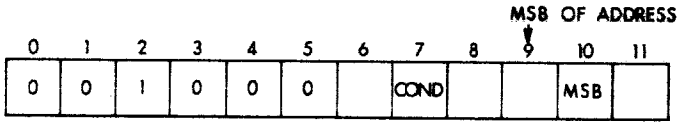
SETX



Function
Set Index Register Pointer—Bits 9-23 are loaded into X0.

Mnemonic **OP Code**

See below



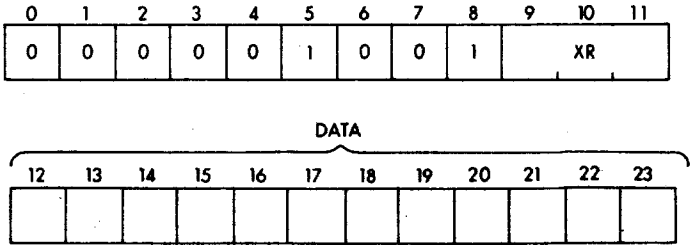
Function
Branch Instructions—If condition is met, bits 9-23 are loaded into the FPC, causing a jump to that address.

Conditions:

	Octal	Meaning
JEQ	0	If FAC = 0, bits 9-23 are loaded into the PC causing a jump to that address
JGE	1	If FAC greater than or equal 0
JLE	2	If FAC less than or equal 0
JA	3	Always
JNE	4	If FAC not equal 0
JLT	5	If FAC less than 0
JGT	6	If FAC greater than 0
JAL	7	If FAC exponent greater than 27 (octal). This condition signifies that the FAC contains a number too large to be fixed in 24 bits.

Mnemonic **OP Code**

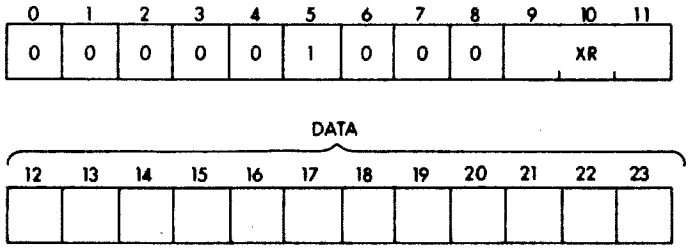
ADDX



Function
Add to Index Register—Bits 12-23 are added to the contents of the index register specified by bits 9-11.

Mnemonic **OP Code**

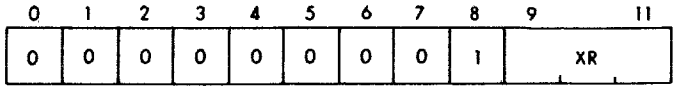
LDX



Function
Load Index Register—Bits 12-23 are loaded into the index register specified by bits 9-11.

Mnemonic **OP Code**

ALN



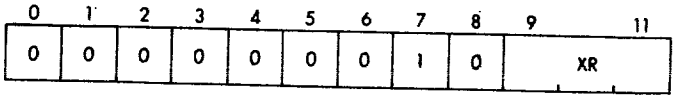
Function
In FP and EP mode, the fraction of the FAC is shifted until the FAC exponent equals the contents of the index register specified by bits 9-11. If bits 9-11 of the instruction are zero, the fraction of the FAC is shifted until the FAC exponent equals 23 (decimal).

In DP mode, an arithmetic shift is performed on the FAC. The number of shifts is equal to the value of the contents of the index register specified by bits 9-11. The sign of the index register indicates the direction of

shift; a positive sign causes a shift toward the least significant bit. If the shift is toward the least significant bit, vacated bits are filled with FACO. If the shift is toward the most significant bit, vacated bits are filled with zeros. If bits 9-11 of the instruction are zero, a 23-bit right shift of the FAC is performed.

Mnemonic **OP Code**

ATX

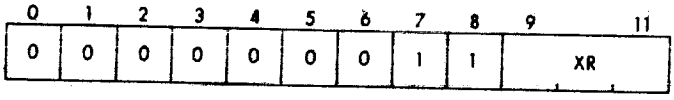


Function

FAC to Index Register—If the mode is FP or EP, the contents of the FAC are fixed (i.e., shifted until the exponent = 23 decimal). ATX does not test to see if fixing is possible. If the mode is DP, the contents of the FAC are already fixed, so this portion is omitted. Bits 12-23 of the result are then loaded into the index register specified by bits 9-11. The FAC is not changed by the ATX instruction.

Mnemonic **OP Code**

XTA



Function

Index Register to FAC—The contents of the index register specified by bits 9-11 are loaded into FAC 12-23. FAC 0-11 is loaded with the contents of FAC 12.

FAC 24-59 are cleared. 23 (decimal) is then loaded into the FAC exponent. If the mode is FP or EP, the FAC is then normalized. (The normalizing operation is omitted in DP mode.)

Mnemonic	OP Code	Function
NOP	004X	No Operation—None, other than a 1-cycle delay in the program. This is the only instruction which will always remain a NOP despite future expansion.
STARTE	005X	Start Extended-Precision Mode—The FPP enters EP mode. If the FPP was previously in a mode other than EP, FAC 24-59 are cleared.
FEXIT	0000	Exit Floating-Point—The contents of the FPP registers are dumped onto the active parameter

Mnemonic	OP Code	Function
		table, the FPP run flip-flop is cleared, and the FPP flag is set. The FPP interrupts the PDP-8 if interrupts are enabled.
FPAUSE	0001	Pause—Suspend FPP operations without updating the APT. IOT FPST will cause the FPP to continue.
FCLA	0002	Clear the FPP Accumulator—Make the FAC exponent and fraction zero.
FNEG	0003	Complement the FPP Accumulator—The FAC fraction is replaced by its 2's complement.
FNORM	0004	Normalize—If the FAC fraction is non-zero, and if the FPP mode is FP or EP, the FAC fraction is shifted toward the most significant bit until the two most-significant bits are different from each other or until the FAC fraction equals 6000 0000. The FAC exponent is decremented by one for each position shifted. If the FAC fraction is 0, or if the mode is DP, no operation is performed.
STARTF	0005	Enter 24-Bit Floating Point Mode—The FPP enters FP mode. If issued in EP mode, the FAC is rounded to 24 bits.
STARTD	.0006	Enter Double-Precision Mode—The FPP enters DP mode. If issued in EP mode, the FAC is chopped to 24 bits. The FAC exponent is ignored, but not modified.
JAC	0007	Jump Per FAC—FAC bits 9-23 are loaded into the FPC.

CHAPTER 4

MEMORY

4.1 MEMORY ORGANIZATION

PDP-8/A memory can be viewed as a series of storage locations with an octal number assigned to each location. This number is an address providing a means of specifying any memory location. For example, a 4K word (K=1024) memory could be shown as in Figure 4-1, with the octal addresses shown on the left and the corresponding decimal equivalents on the right.

Four octal digits (12 binary bits) are required to address 4K of memory directly. The PDP-8/A can accommodate 32K of memory through the addition of three extended memory address bits. These bits are located on the KM8-A Extended Option Board which is required when the system is expanded above 4K of memory.

Each 4K memory block is called a memory field. There can be a maximum of eight memory fields, numbered sequentially from 0 through 7 (see Figure 4-2). Each memory field is divided into 32 pages and each page contains 128 words.

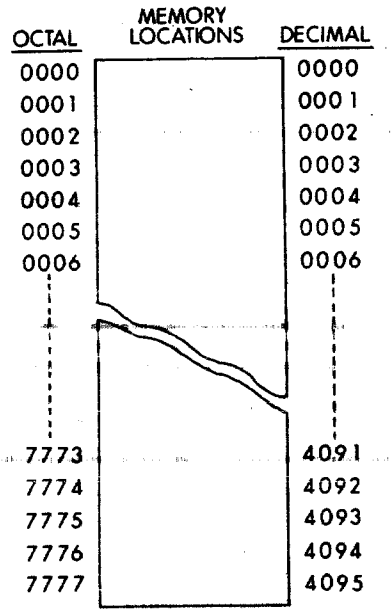


Figure 4-1 Memory Addresses

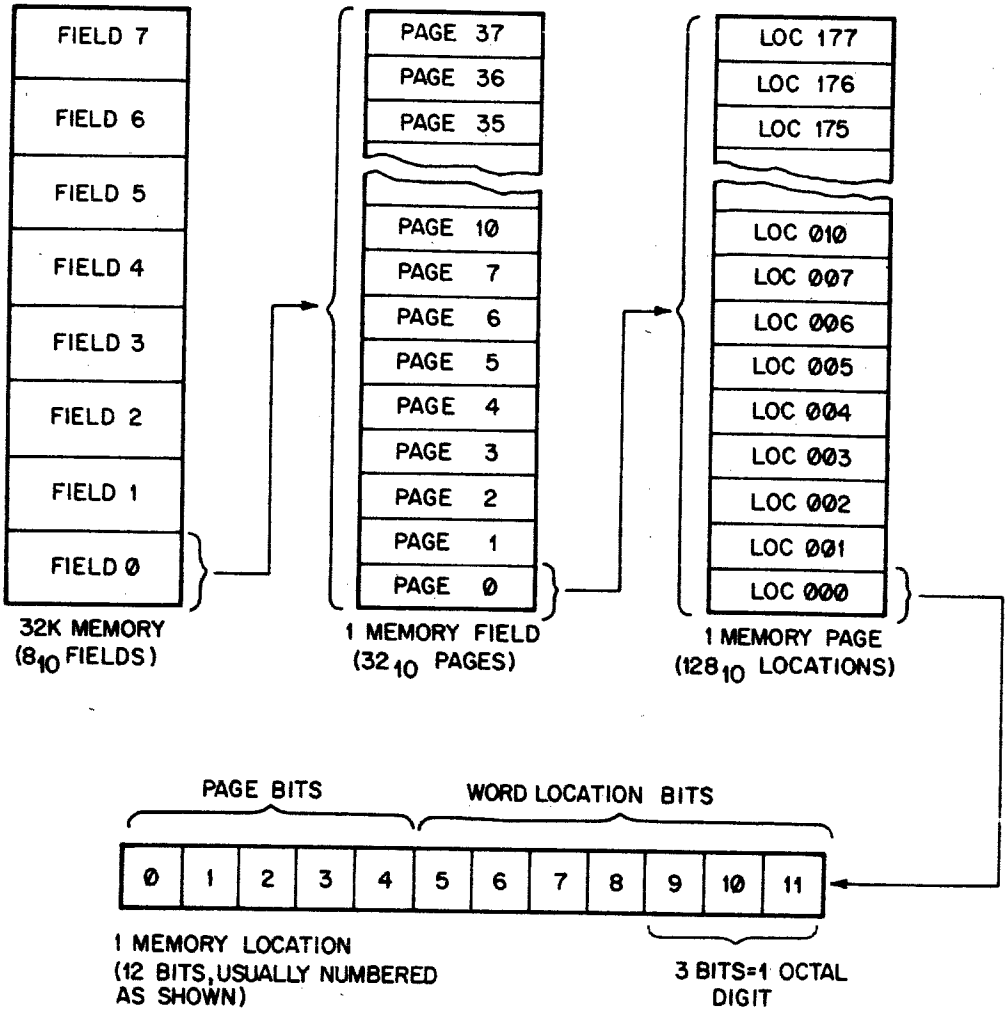


Figure 4-2 PDP-8/A Memory Organization

Memory pages are numbered sequentially, in octal, from page 0 (which contains addresses 0000 to 0177) to page 37 (addresses 7600 to 7777). Within each memory page, the 128 locations on the page are numbered sequentially, in octal, from 0 to 177. This number is called the page address of the memory location. Page addresses are not redundant; the page address of a memory location is simply the low order 7 bits of the 12-bit address.

The high order five bits of a 12-bit memory address are called the page bits and specify one of the 32 pages in a memory field. The octal value of the page bits for any memory address is identical to the number of the memory page on which the address is located. The low order seven bits of the 12-bit address are called the word location bits and specify one of 128 locations on the page specified by the page bits. The octal value of the word location bits for any memory address is identical to the memory location. Thus, location 4716 is at word location 116 on page 23, while location 2257 is at word location 057 on page 11.

Unlike memory fields, which may be physically separated by being located on different modules plugged into the Omnibus, memory pages do not correspond to any physical separation within memory. The computer has no way of recognizing which page of memory it is executing in, and it is not cognizant of executing across a page boundary. Memory pages represent an artificial subdivision of memory that facilitates understanding the PDP-8/A memory reference instruction decoding process.

The individual bits of a PDP-8/A memory word are numbered, for reference purposes, as shown in Figure 4-2. The bits of major registers are numbered in the same manner, but the abbreviated register name is prefixed to the number for identification purposes. Thus, bit 0 is always the high order bit of a memory word, while AC0 is the high order bit of the accumulator and PC11 is the low order bit of the program counter.

4.2 MEMORY TYPES

A variety of memory types and configurations are available for PDP-8/A systems. This section describes these configurations and defines some of the commonly used terms. Table 4-1 summarizes the memory cycle times for the various configurations.

Memory Space	The number of memory locations which may be accessed by a central processor.
Random Access Memory (RAM)	A memory in which the time required to access a particular location is not a function of the last location accessed.
Read-Only Memory (ROM)	A memory, usually random access, whose contents cannot be altered by the central processor or peripheral devices. Most read-only memories are of the semiconductor type, although diode arrays and braided wire arrays are occasionally found.
Masked ROM	A read-only memory whose data content is fixed during one or more of the masking steps in the manufacturing process.
Programmable ROM	A read-only memory whose content can be set once or more than once, usually by a specialized device called a "loader" or "blaster."
UV-Eraseable ROM (UV-PROM)	A read-only memory whose content may be erased by exposure to a high-intensity source of ultra-violet (UV) wavelength radiation; the new content is then loaded electrically by a specialized loading device.
Blastable ROM	A read-only memory whose content, once loaded, cannot be erased. Sometimes called B-ROM or P-ROM, the blastable ROM is called a "ROM" in the PDP-8/A literature.

Read-Write Memory	A memory whose content can be altered by the central processor or peripheral devices.
Core Memory	A memory type, usually read-write, in which the individual bit storage elements are small ferrite toroids.
Semiconductor Memory	A memory type whose storage elements are diodes or transistors. Most modern semiconductor memories are large-scale integrated (LSI) devices, having from 1024 to 4096 storage elements on a single substrate. Semiconductor memories can be either read-only or read-write.
Read-Write Semiconductor Memory	In the PDP-8/A, a 1024-bit chip is the basic storage element. Arrays of these devices are used to configure modules having 1024, 2048, or 4096 12-bit words. These modules are called "RAM" memories in the PDP-8/A literature.
Dynamic RAM	A type of read-write semiconductor memory whose contents must be periodically "refreshed" to prevent information loss. (The PDP-8/A does **not** use dynamic RAM.)
Static RAM	A type of semiconductor memory which requires no "refreshing." The penalty paid for this advantage is slightly more power dissipation. (The PDP-8/A uses static RAM.)
Volatile Memory	One whose contents are lost when power is removed. This includes virtually all read-write semiconductor RAMS. (In PDP-8/A systems, battery backup is included to prevent such loss of memory content.)

TABLE 4-1 Summary of Memory Cycle Times

MEMORY CONFIGURATION	FETCH MAJOR STATE (usec)	ALL OTHER STATES (usec)
ROM only (KK8-A CPU)	1.5	1.5
ROM only (KK8-E CPU)	1.2	1.2
ROM/RAM (ROM cycle)	1.6	1.6
ROM/RAM (RAM cycle)	2.7	3.1
RAM only	2.4	2.8
MR8-FB PROM (KK8-A, KK8-E, CPU's)	3.4	3.7
Core Memory (KK8-A CPU)	1.5	1.5
Core Memory (KK8-E CPU)	1.2	1.4

4.3 CORE MEMORY

The MM8-AA (8K) and MM8-AB (16K) are 12-bit random access core memory systems for the PDP-8/A computer. The memory consists of ferrite cores wired in a 3-D, 3-wire planar configuration and is expandable from 8K to 32K in 8K or 16K increments. The memory system performs three basic functions for the PDP-8/A processor:

1. Decodes and selects the desired core location in which a 12-bit word is stored or will be stored.
2. Reads a 12-bit word from the selected location.
3. Writes a 12-bit word into the same selected location.

Core memory (either the MM8-AA or the MM8-AB) is contained on a one-inch thick module assembly consisting of a hex module of electronic components are a planar stack assembly. The MM8-AA memory system consists of a G649 module assembly and an H219-A 8K stack assembly while the MM8-AB memory system consists of a G650 module assembly and an H219-B 16K stack assembly. The memory is inserted into one slot on the OMNIBUS but requires two slot spaces because of the extra thickness of the module.

4.3.1 Core Memory Block Diagram Description

Figure 4-3 is a functional block diagram of the core memory system. At the beginning of a memory cycle, the MA register in the CPU is loaded. The address decoders in the core memory system receive the MA bits and turn on the corresponding driver and sink current switches. XY current flows when the read or write current source is pulsed by the internal memory timing.

The outputs from the 12 selected cores are fed to their respective sense amplifiers. A strobe signal is used to gate the sense amplifier into the sense register. During the first or read portion of the memory cycle, MD DIR is low (active) and the output of the sense register is placed on the MD lines. During the latter, or write portion, of the memory cycle, the memory selection system uses the same address inputs and control signals. If MD DIR is low during the write portion of the memory cycle, the contents of the sense register is written back into core. If MD DIR is high, the contents of the sense register is inhibited from being placed on the MD lines, and instead, a word from the processor is written back into core, via the MD lines and the inhibit drivers.

4.3.2 Module Assembly

The module contains circuitry which decode the memory address bits from the Omnibus to select the X-Y lines of the core array. The circuits include X and Y selection switches, X-Y current sources, selection diodes for address decoding, inhibit drivers, sense amplifiers and timing logic. This logic is used to transfer data to the MD lines and restore data in the addressed location following a read operation. During a read/write modify operation, the contents of the addressed location is modified to correspond to data from the MD lines.

The memory power fail circuitry cuts off the X and Y current sources after sufficient delay. This delay allows the processor to complete a

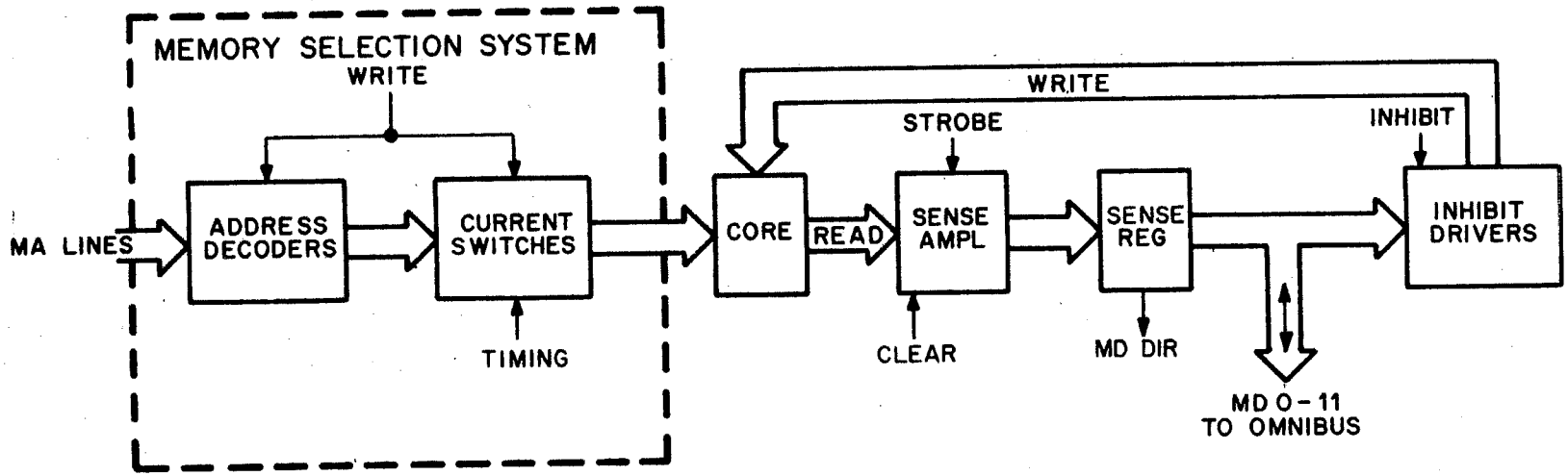


Figure 4.3 Core Memory System Functional Block Diagram

cycle before memory locks off. When the machine is turned on, POWER OK H goes high and the current source is reactivated after sufficient delay. A thermistor circuit causes X and Y currents to track the change in temperature measured on the baseboard. Temperature changes of 0° to 50° are tracked so that the proper current and temperature relationships are maintained.

4.3.3 Core Stack Assembly

The core stack on the stack board assembly contains the storage elements for the MM8-AA and MM8-AB core memory. The stack consists of 8192 or 16,384 12-bit words arranged in 12 core mats. Each core mat consists of two 64 × 128 core matrices.

4.3.4 Addressing

The MM8-AA has an 8192 (8K) 12-bit word address space and the MM8-AB has a 16,384 (16K) word address space. Jumpers on the memory module allow the MM8-AA to be installed in fields 0 and 1, 2 and 3, 4 and 5, or 6 and 7. The 16K memory can be installed to start (first address) in field 0 or field 4.

4.3.5 Core Memory Specifications

The specifications for the PDP-8/A core memory systems are shown below:

WARNING

The G8018 regulator board is required for core memory. Semiconductor machines cannot be changed to core machines unless the power supply and power transformer are both changed. Call your local DIGITAL Sales Office for complete information.

SPECIFICATIONS

Memory Cycle Time:	1.5 μs. (KK8-A CPU); 1.2 μs. (KK8-E CPU)
Physical Size:	15¾ in. wide x 8½ in. deep x 1 in. thick.

Operating Environment:

Temperature:	0° to 50° C (32° to 122° F)
Humidity:	0 to 90% relative humidity (noncondensing)
Air Flow:	Sufficient to maintain ≤3° C temperature gradient across the stack.

4.4 SEMICONDUCTOR MEMORY

A variety of semiconductor memories are available for the PDP 8/A user. The reliability and non-volatile characteristics of read only memory (ROM) protect the user against program loss caused by electrical noise, AC cycle dropouts, power brownouts, operator error, or power failures. The semiconductor read/write memory (RAM) provides the user with an attractive alternative to core memory in systems that require small amounts of writable memory. Moreover, ROM and RAM memories on the PDP-8/A can be combined. In these configurations, the main program can be stored in non-volatile ROM memory while the RAM can be

addressed by the ROM to store or retrieve data. With the special PDP-8/A ROM hardware construction, instructions that require write capabilities (DCA, JMS, ISZ), special operations such as auto-index and interrupt, and direct memory access (DMA) can utilize some RAM memory as scratch-pad memory or buffer memory. Programming ROM/RAM combinations is no different from programming core as far as machine and assembly language programming and the PDP-8 instruction set are concerned. This means that core programs will run without alteration in semiconductor machines. However, there are a few special rules for assembly of ROM programs and the blasting of ROM programs. These rules, along with programming and hardware information on ROM/RAM configurations, will be covered in detail in this chapter.

PDP-8/A semiconductor memory is available in the following configurations:

- MR8-A read only memory (ROM), available in 1K, 2K, 3K, or 4K configurations.
- MS8-A read/write random access memory (RAM), available in 1K, 2K, or 4K configurations.
- MR8-A/MS8-A ROM/RAM configuration, consisting of MR8-A and MS8-A modules connected together. Any combination of the MR8-A and the MS8-A may be used.
- MR8-FB reprogrammable read only memory (PROM), available in 1K PROM with 256 words of RAM. PROM may be erased and reprogrammed up to 100 times.

Each of these memory configurations is listed in Table 4-2 and is discussed in the following paragraphs.

TABLE 4-2 PDP-8/A Semiconductor Memories

OPTION	DESCRIPTION	CYCLE TIME	MEMORY TYPE
MS8-AA	1K Semiconductor Read/Write Random Access Memory (RAM)	2.4 μs Read 2.8 μs Write	Read/Write
MS8-AB	2K Semiconductor Read/Write Random Access Memory (RAM)	2.4 μs Read 2.8 μs Write	Read/Write
MS8-AD	4K Semiconductor Read/Write Random Access Memory (RAM)	2.4 μs Read 2.8 μs Write	Read/Write
MR8-AA	1K Semiconductor Blastable Read Only Memory (ROM)	1.5 μs	Read-Only
MR8-AB	2K Semiconductor Blastable Read Only Memory (ROM)	1.5 μs	Read-Only

TABLE 4-2 PDP-8/A Semiconductor Memories (Cont.)

OPTION	DESCRIPTION	CYCLE TIME	MEMORY TYPE
MR8-AD	4K Semiconductor Blastable Read Only Memory (ROM)	1.5 μs	Read-Only
MR8-FB	1K UV Erasable Blastable Read Only Memory (PROM) with 256 words of RAM	3.7 μs	Read only with limited amount of RAM, and with the ability to erase with ultraviolet light and reprogram.

4.4.1 MR8-A Read Only Memory (ROM)

The MR8-A is capable of running core type programs. Existing PDP-8 programs written for core machines may be converted to ROM, or new programs may be written without changing program styles or methods. The MR8-A is a 1K to 4K word, 13-bit memory. When the MR8-A is used in ROM only modes, twelve bits provide data and the thirteenth bit is not used. When used in conjunction with a read/write memory (MS8-A), the 13th bit is used to designate the addressed location as writable. The content of the ROM location is used to address a location in RAM for instructions that require read/write operations (i.e., DCA, ISZ, or JMS).

MR8-A FUNCTIONAL BLOCK DIAGRAM DESCRIPTION

Figure 4-4 is a block diagram of the MR8-A read-only memory. The memory address is decoded by the address logic and the switches which select one of eight 4K fields. The select signal from the address logic asserts the ROM ENABLE signal which specifies a 1K segment consisting of 13 chips.

The NTS STALL L signal is grounded by the ROM logic early in the memory cycle to allow for the long propagation delay of the RAM cycle if a ROM/RAM cycle is designated. The ROM logic holds the STALL signal grounded for 200 ns which halts the processor for this period. If a ROM/RAM cycle is executed, the RAM logic will keep the STALL signal grounded during the RAM cycle. If a ROM only cycle is designated, the STALL signal is ungrounded after 200 ns and the CPU resumes normal operation.

After the memory data has been accessed, it is clocked into the memory data buffers by the Memory Data Clock. The MD DIR L signal enables the memory data onto the Omnibus.

Storage Device

The ROM storage device is a 256 $\times$ 4 bit TTL P-ROM chip. A high current or voltage pulse is used to permanently alter the internal structure of the chip, providing a new current path or opening an existing one. This process of altering or programming the chip is called "blasting" the memory.

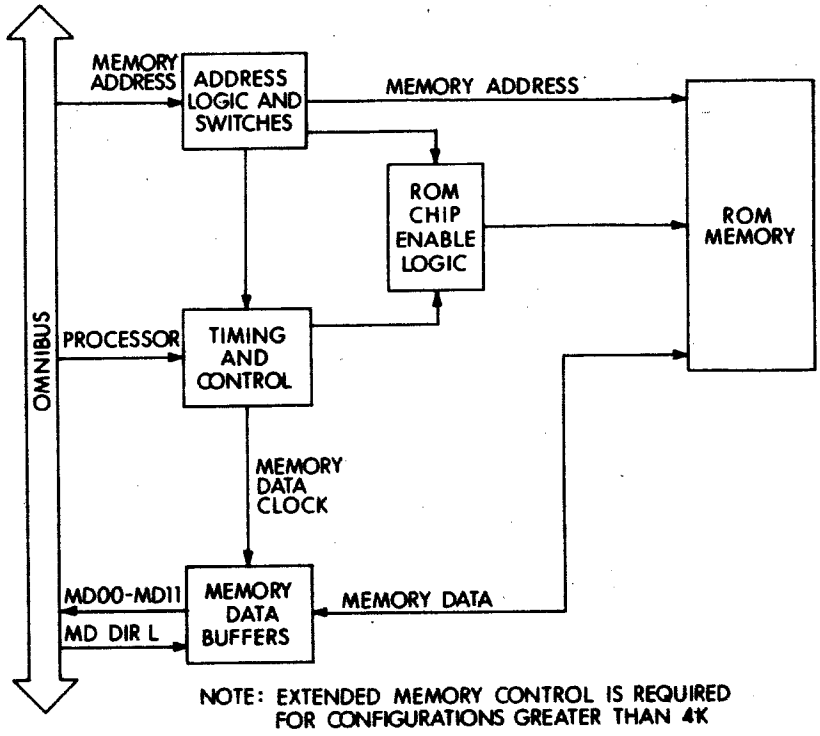


Figure 4-4 MR8-A Read Only Memory Block Diagram

Addressing
The MR8-A must start at location 0000 in the selected field, and may be 1K, 2K, 3K, or 4K in size.

Cycle Time
The MR8-A cycle time is 1.5 μs if no read/write memory is used.

Power Requirements
The MR8-A requires +5.0 V $\pm$ 5% @ 7.4 A (max) for 4K and 2.7 A for 1K. Typical measured values are 5.0 A for 4K and 2.0 A for 1K.

Programming
The MR8-SA computer-controlled ROM loader is available from DIGITAL for users who wish to program their own MR8-A memories.

The ROM chips are mounted in sockets to facilitate replacement in the event of programming errors or failures. The computer-controlled loader also checks the MR8-A ROM memory for errors after the module is blasted and will isolate any failure to the chip level and print out the number of the defective chip on the console device. Additional information on the programming of ROM memories can be obtained through the local DIGITAL sales office or by referring to The ROM/RAM Programming Users' Guide.

4.4.2 MS8-A Random Access Memory (RAM)

The MS8-A is a semiconductor read/write memory. The MS8-A is static (does not need a refresh cycle) and volatile (the contents of memory

are lost when power is removed). However the PDP-8/A has a battery supply for short power failures.

MS8-A FUNCTIONAL BLOCK DIAGRAM DESCRIPTION

Figure 4-5 is a block diagram of the MS8-A Semiconductor RAM. The memory address is decoded by the address logic and switches to select one of eight 4K fields. The switches also can be used to specify a RAM starting address of 0000, 2000, 4000 or 6000_8.

The NTS STALL L signal is initially held at ground by the ROM logic. If a ROM/RAM cycle is executed, the RAM will continue to keep the NTS STALL L signal grounded for the remainder of the cycle. This places the CPU in a halt mode and necessitates a restart to resume normal operation.

After memory has been addressed, the data is clocked into the memory data buffers and onto the Omnibus if MD DIR L is asserted. If MD DIR L is negated, the data is loaded into memory from the Omnibus via the memory data buffers.

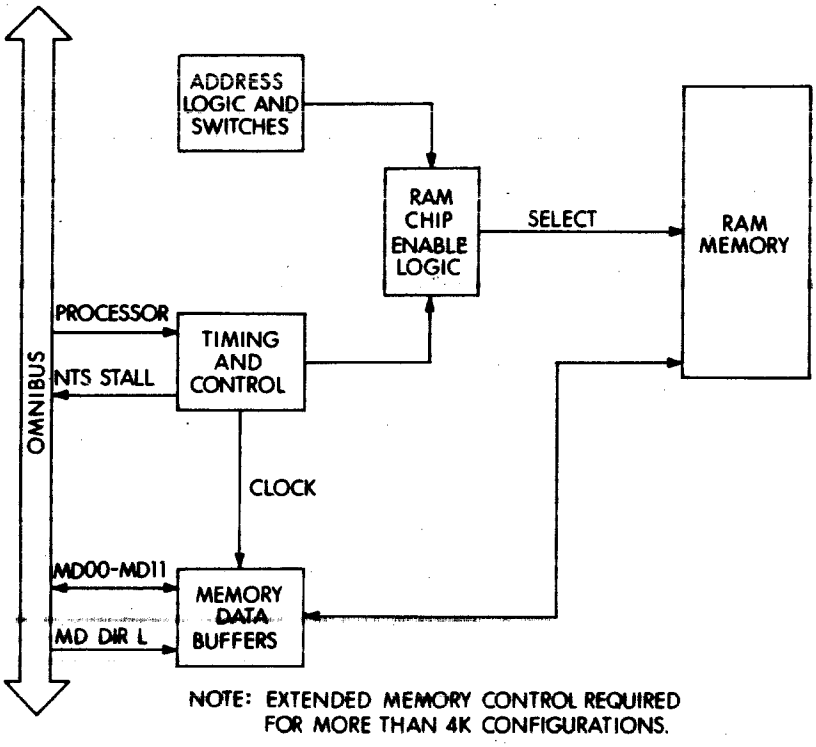


Figure 4-5 MS8-A Read/Write Memory

The MS8-A may also be used as a read/write scratch-pad memory for the MR8-A (MR8-A/MS8-A configurations).

Storage Device

The storage device is a 1024 $\times$1, static MOS RAM in a 16 pin package.

Addressing
The MS8-A may be used in any memory field. The 1K word memory may start at any 1K boundary within the 4K field. For example, if the user has 2K of ROM, the RAM could start at location 4000 in the field that contains the ROM.

Cycle Time
The cycle time is 2.4 μs for a read operation, and 2.8 μs for a write operation.

Power Requirements
The MS8-A uses +5 V ±5% @ 4.6 A for 4K and 2.4 A for 1K. Typical measured values are 3.0 A for 4K and 1.6 A for 1K.

4.4.3 RAM/ROM Combination

Overview
The trade-offs between ROM, RAM, and core require that care be taken when considering the type of memory to be used in a particular application. The fact that ROM memories are "blasted" with data ensures the stability of the program but, on the other hand, inhibits the use of any instructions or operations that alter memory (i.e., write instructions and DMA). These and other trade-offs prohibit the optimization of semiconductor memories in conventional mini/micro computers. DIGITAL's ROM/RAM memory configurations provide real advantages over configurations using ROM or RAM alone. The interconnection of read only memory with RAM memory gives the system the capability to execute writable instructions in ROM as a result of a 13th bit technique.

Thirteenth Bit Technique
RAM can be used as scratch-pad memory using an indirect addressing scheme associated with ROM (not to be confused with software indirect address). The indirect addressing is specified by a 13th bit. Each location in ROM has 13 bits instead of the usual 12 bits, and the extra bit acts as a flag to the ROM hardware. Each time the 13th bit is a "0," data is accessed from ROM in the usual manner. However, when the 13th bit of the operand is a "1," the ROM hardware treats the 12 bit contents of the operand as an address that is sent to RAM rather than as data. This 12 bit address is sent to RAM and represents an address in which data will be accessed or stored .

For example:

Assume that at location 200, a deposit accumulator instruction (DCA) is stored and the operand value is 250. (Note: DCA is a write instruction).

In ROM	200/ DCA 250	Tells hardware to go to location 250.
	250/ (1) *7000	At location 250, the address 7000 is stored. Since the 13th bit is set, the other 12 bits are sent to RAM.
In RAM	7000/ AC	The address 7000 would reach RAM via top connectors and the accumulator would be written into location 7000 of RAM.

*Note: The assignment of the value 7000 was arbitrary.

The 13th bit is inaccessible to the programmer. The ROM blaster/loader performs the necessary hardware function of setting the 13th bit as required.

With combined ROM/RAM configurations as shown in Figure 4-6, the advantages of both memory types are available. The main program can be stored in nondestructive ROM, while the RAM can be used as scratch-pad for write operands and data storage. The RAM is also available for DMA transfers, and may be directly addressed by the CPU.

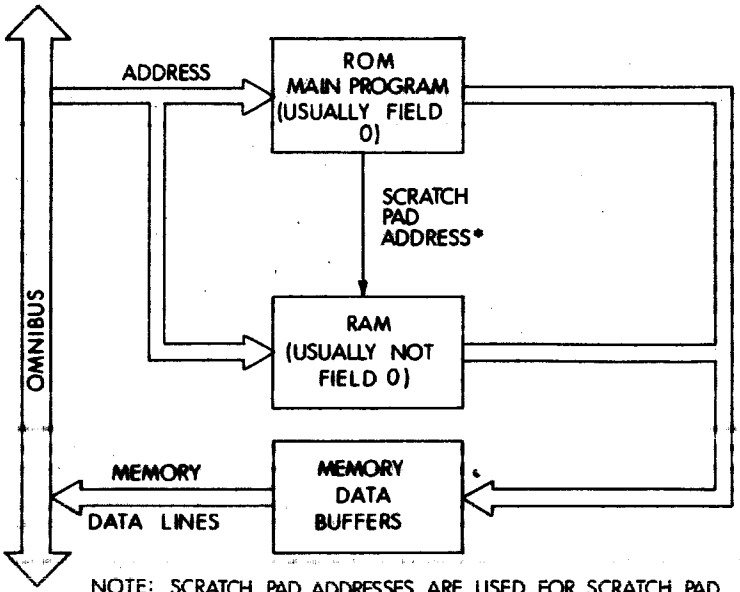


Figure 4-6 ROM/RAM Configuration Block Diagram

4.4.4 MR8-FB Reprogrammable Read Only Memory (PROM)

The MR8-FB is a 1K word (12-bit words) reprogrammable read only memory (PROM) with 256 words of RAM. The MR8-FB is addressed the

same way as core memory although it is a 13-bit memory, as is the MR8-A. The 13th bit of PROM may be set to a logical 1 when the MR8-FB is programmed to address a word in read/write memory.

> **NOTE**
> The 13th bit is inaccessible to the programmer and is set, as required, by the ROM blaster/loader.

When the 13th bit of PROM is a one, the 8 least significant bits of the PROM output are used to address one of the 256 RAM locations. During a read access the 8 least significant bits are treated as an address to point to a read/write location in RAM. This allows the programmer to use instructions that require a write operation. The 256 words of RAM may be spread throughout the 1K of PROM memory where they are needed. All or none of the RAM locations may be used as scratch-pad read/write memory, but none of RAM locations can be addressed directly.

The MR8-FB memory cycle is 3.7 μs for both read and read/write operations.

ADDRESSING

The MR8-FB first address may be 0000, 2000, 4000, or 6000 in any field. The field and first address are selected by jumpers on the module.

The MR8-FB may be started at location 0000_8 or 0200_8, relative to the start of the 1K segment it occupies, when BOOT on the programmer's console or operator's panel is depressed. This feature is enabled by the installation of a jumper.

PROM ERASING PROCEDURE

The PROM chips may be erased by exposure to high intensity, ultraviolet light at a wave length of 2537Å. The ultraviolet lamps should be used without short wave filters and the PROM should be placed about one inch away from the lamp tube for 20 minutes. This operation has the effect of writing all 0s into the PROM. A UV Lamp (model S-52) and UV contrast safety goggles (model UVC-303) can be purchased from Ultra-Violet Products, Inc. San Gabriel, California 91778.

POWER REQUIREMENTS

The MR8-FB requires +5 V @ 3.8 A and −15 V @ 350 mA.

PROGRAMMING OF ROM MEMORIES

Programmers code ROM programs as they would core with one exception. As noted earlier, to have the ability to write data, ROM must be connected to some RAM memory. Therefore, since the amount of RAM to be used as a scratch-pad area for ROM is finite, the number of writeable locations must not exceed the size of the RAM. Likewise, any data buffers set aside for DMA type transfers must be included in consideration for the size of RAM needed.

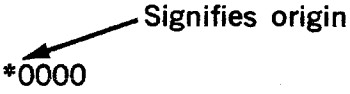
The MR8-SL is a PDP-8 option for loading programs into the MR8-FB 1702A PROM memory chips on the MR8-FB 1K module. Additional information can be obtained through the local DIGITAL sales office or by referring to the ROM/RAM Programming Users Guide.

4.5 SPECIAL PROGRAMMING EXAMPLES

Since both auto-indexing and interrupt functions require read/write capability, the DWRITE command must be assigned to those locations involved with interrupt and auto-indexing (locations 10 through 17). The DWRITE command is a pseudo op which is used to label all the locations in ROM which specify a write operation. An example of the procedure for tagging those locations is presented below.

4.5.1 Interrupts and Auto-Index

By nature, both auto-indexing and interrupt functions require read/write capabilities. Therefore, the DWRITE command must be assigned to those locations that are involved with auto-index and interrupt. These locations include locations for the interrupt system and locations 10–17 for auto-indexing. An example of the procedure for tagging those locations is presented below:




```
*0000

INT, DWRITE 2000        Denotes Loc 0 to be writable into RAM
                        Loc 2000.

*10

AUTO 10, DWRITE 2001    Assigns RAM Loc 2001 to be writable
                        for auto-index Loc 10.

AUTO 11, DWRITE 2002
```

NOTE

The values 2000, 2001 and 2002 are arbitrary depending on the address range of the RAM memory attached to the ROM.

4.5.2. Data Retrieval from RAM

Often, data that has been deposited into RAM must be retrieved for manipulation. By using the TAD instruction, and assigning the same symbolic address code that was used to deposit the data, data can be retrieved. For example:

```
DCA STORE               Instruction used to deposit data.
•
•
•
•
•
TAD STORE               Instruction used to retrieve that data.
STORE, DWRITE 600
•
```

NOTE

Both DCA STORE and TAD STORE instructions access LOC 6000 in RAM memory.

With the 13th bit hardware, at first glance, it would seem that for every word in RAM, a location in ROM must be assigned as a pointer to the RAM location. For example:

```
TAD Buffer 1
TAD Buffer 2
TAD Buffer 3
•
•
•
•
Buffer 1, DWRITE 2201
Buffer 2, DWRITE 2202      Pointers to RAM
Buffer 3, DWRITE 2203
```

Obviously, this approach to handling large buffers in RAM is both cumbersome and inefficient. However, there are programming techniques that resolve this inefficiency. For example:

Assembly Language

```
TAD I Buffer
ISZ Buffer
JMP. –2

Buffer, DWRITE 7000
```

Machine Language

```
200/1650
201/2250
250/7000 (plus 13th bit)

RAM 7000/Address of data in RAM
```

The ISZ instruction is utilized to update the absolute address in the pointer location 7000 by adding +1 to that value in 7000. By using the TAD indirect instruction, one more level of indirection allows data to be stored into the address specified by the contents of LOC 7000 instead of into LOC 7000 itself.

4.6. ROM/RAM CONFIGURATION OPTIMIZATION

When initially configuring ROM/RAM combinations, a few basic rules should be followed. The lower boundary of ROM memory is always location 0000. Therefore, ROM will always range from location 0000 to 1777, 3777, 5777 or 7777 depending on the size of the ROM chosen. RAM, on the other hand, can begin at either location 0000, 2000, 4000 or 6000 of any field or address space not occupied by ROM. For switch settings of address assignment, see the *PDP-8/A Operator's Handbook.*

CHAPTER 5

INSTRUCTION SET

5.1. INTRODUCTION

A PDP-8/A instruction is a single 12-bit word, stored in memory, that tells the computer to perform a specific operation or sequence of operations. The 12-bit word can be represented as four octal digits and is referred to as the octal code of the instruction. Each instruction has an assigned mnemonic which is a 3- or 4-character name that may be supplied to an assembler program to generate the corresponding octal code.

Like most stored program computers, the PDP-8/A makes no distinction between instructions and data; it will manipulate instructions as though they are stored variables or attempt to execute data as instructions if it is programmed to do so.

5.2. CLASSES OF INSTRUCTIONS

There are three classes of PDP-8/A instructions: memory reference instructions, augmented instructions and the jump instruction.

Memory reference instructions, or MRIs cause the computer to operate on the content of a memory location, or to use the content of a memory location to operate on the accumulator. Every MRI specifies an operation, which is coded in bits 0 through 2 of the instruction, and the address of an operand (the data to be operated on), which is coded in bits 3–11. There are five PDP-8/A memory reference instructions.

Augmented instructions cause the computer to perform a logical (non-arithmetic) operation on the content of one of the major registers. Augmented instructions include: rotate the AC right or left, test the content of the AC or link, load an I/O device buffer from the AC and operate the I/O device, or initialize the interrupt system. Since augmented instructions do not reference a memory address, all 12-bits of the instruction are available for coding the precise operation or sequence of operations to be performed.

The jump instruction causes a specified 12-bit address to be loaded in the Program Counter (PC) so that the instruction at this address will be the next instruction to be executed.

5.2.1. Memory Reference Instructions

Every memory reference instruction contains an operation code, or OP code, that occupies bits 0–2 of the instruction and an address code that occupies bits 3–11. This format is illustrated in Figure 5-1. The OP code of an MRI is one of the digits 0 to 4, corresponding to one of five possible operations. The address code specifies the address of an operand if the instruction is directly addressed, or the address of a pointer to the operand if the instruction is indirectly addressed.

Bit 3 of an MRI is the indirect address bit. If this bit is set (contains a 1), the MRI is indirectly addressed. This means that bits 5 through 11 of the address code of the MRI specify the address of a memory location in which the 12-bit address of the operand is stored. If the indirect

address bit is not set, the instruction is directly addressed. In this case bits 5 through 11 of the address code specify the address at which the operand itself is stored.

Bit 4 of an MRI is the page bit, and bits 5 through 11 are the word location bits. If the page bit is set, the word location bits reference the memory page on which the MRI itself is stored (called the current page). If the page bit is not set, the word location bits reference page 0. In either case, the address specified by the page bit and the word location bits will be the address of the operand if the MRI is directly addressed, or the address of a memory location that contains the 12-bit address of the operand if the instruction is indirectly addressed.

In this manner, an MRI may address any one of 256_{10} (400_8) locations directly, unless this instruction is stored on page zero. If the MRI is stored in one of the locations 0000–0177, the current page is page zero and the MRI may only address 128_{10} (200_8) locations directly. An MRI may address any of 4096_{10} (10000_8) locations indirectly.

Table 5-1 lists the mnemonics for the five memory reference instructions, their octal codes, and the operations they perform. Only bits 0–2 of the octal codes are listed explicitly; bits 3–11 make up the address code, which depends upon where in memory the operand for the MRI is stored.

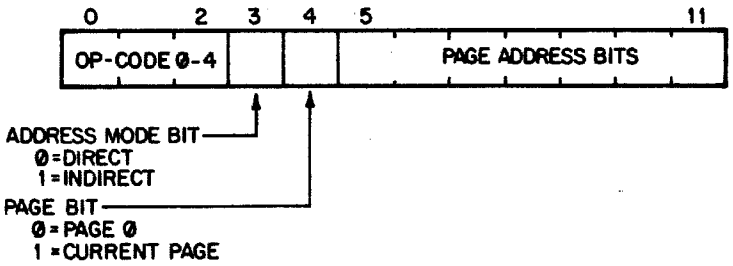


Figure 5-1 Memory Reference Instruction Format

5.2.2. Augmented Instructions

The two augmented instructions are the input/output transfer (IOT) instruction and the operate instruction.

- THE INPUT/OUTPUT TRANSFER INSTRUCTION
  Input/Output transfer (IOT) instructions are used to initiate the operation of peripheral devices and to transfer data between peripherals and the central processor. Figure 5-2 shows the format of an IOT instruction. Bits 0 through 2 contain the OP code, which must be 6 to specify an IOT instruction. Bits 3 through 8 contain a device selection code that is transmitted to every peripheral device whenever the IOT instruction is executed. Device selectors within the peripheral devices monitor these device codes. When a peripheral device recognizes a device code as that peripheral's assigned code, the device accepts the last three bits of the IOT instruction (bits 9 through 11), which contain the operation specification code. These bits may be set to specify one of up to eight operations. If a peripheral device is capable of performing more than eight different operations, it is necessary to assign more than one device code to the peripheral device.

Table 5-1
Memory Reference Instructions

MNEMONIC	OCTAL	OPERATION
AND	0XXX	Logical AND. The content of the memory location specified by XXX is combined with the contents of the AC by a bitwise logical AND operation. The result is left in the AC; the content of memory and the original content of the AC is lost. This instruction, often called "extract" or "mask," may also be considered as a bit-by-bit binary multiplication.
TAD	1XXX	Two's Complement Add. The contents of the memory location specified by XXX is combined with the content of the AC by two's complement addition. The result is left in the AC, the content of memory is unchanged, and the original content of the AC is lost. If there is a high-order carry from AC0, the link is complemented.
ISZ	2XXX	Increment and Skip if Zero. The contents of the memory location specified by XXX is incremented by 1 and restored to memory. If the content of the referenced location becomes zero, the PC is incremented by 1 to skip the next sequential instruction. If the content of the referenced location does not become zero, the next instruction is executed. AC is not affected.
DCA	3XXX	Deposit and Clear the Accumulator. The contents of the AC is stored in the memory location specified by XXX and then the AC is set to zero. The original content of the referenced memory location is lost.
JMS	4XXX	Jump to Subroutine. The content of the PC is stored in the memory location specified by XXX. Then the PC is loaded with (XXX + 1), so that the instruction stored in the memory location following the referenced location is the next instruction to be executed. The content of the AC is not affected.

- THE OPERATE INSTRUCTION
  The operate instruction consists of three groups of microinstructions. Bits 0-2 contain the OP code, which must be 7 to specify an operate

instruction. Group 1 microinstructions, which are identified by the presence of a 0 in bit 3, are used to perform logical operations on the content of the accumulator and link. Group 2 microinstructions, which are identified by the presence of a 1 in bit 3 and a 0 in bit 11, are used primarily to test the content of the accumulator and link, then conditionally skip the next sequential instruction. Group 3 microinstructions have a 1 in bit 3 and a 1 in bit 11; they are used to perform logical operations on the content of the accumulator and multiplier quotient registers.

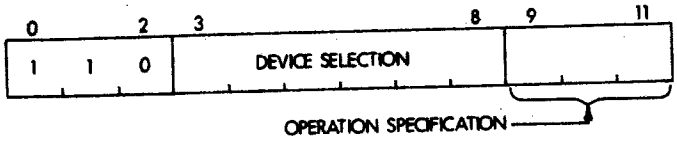


Figure 5-2 IOT Instruction Format

Operate microinstructions from any group may be microprogrammed with most other operate microinstructions of the same group. The octal code for a microprogrammed combination of two (or more) microinstructions is the bitwise logical OR of the octal codes for the individual microinstructions. When more than one operation is microprogrammed into a single instruction, the operations are performed in a prescribed sequence, with logical sequence 1 microinstructions performed first, then logical sequence 2 microinstructions, and so on. Thus, programmed operations with the same logical sequence number are performed simultaneously.

Group 1 Microinstructions—Figure 5-3 shows the format of a group 1 microinstruction. The OP code must be 7 to indicate an operate instruction, and bit 3 must contain a 0 to indicate a group 1 microinstruction. Any of bits 4 to 11 may be set (loaded with a binary 1) to indicate a specific group 1 microinstruction. If more than one of these bits is set, the instruction is a microprogrammed combination of group 1 microinstructions, which will be executed according to the logical sequence shown in Figure 5-3.

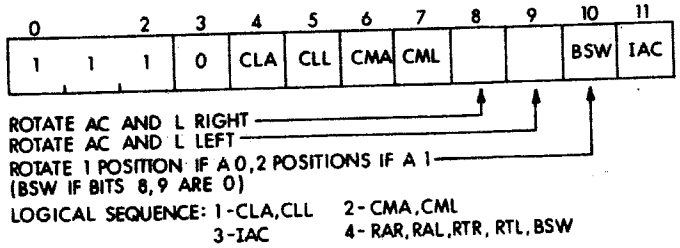


Figure 5-3 Group 1 Operate Microinstructions

Table 5-2 lists the group 1 microinstructions, their assigned mnemonics, and the operations they perform. Two or more of these microinstruc-

tions may be microprogrammed into a single 12-bit instruction as long as the instruction does not contain more than 1 of the logical sequence 4 microinstructions (RAR, RAL, RTR, RTL and BSW). This restriction should not impose any constraint on the user since the five logical sequence 4 microinstructions perform mutually incompatible operations.

The undefined codes in the Rotate group (bits 8, 9, and 10 = 110 or 111) must not be used as instructions. Failure to observe this constraint will likely result in code which will not work on any other machines in the PDP-8 series.

Table 5-3 lists four microprogrammed combinations of group 1 microinstructions which are used so frequently that they have been assigned their own mnemonics. Note that the octal codes for a microprogrammed combination of operate microinstructions is the bitwise logical OR of the octal codes of the individual microinstructions. Other frequently used combinations of operate microinstructions are listed in Appendix A of this handbook.

Group 2 Microinstructions—Figure 5-4 shows the format of a group 2 microinstruction. The operation code must be 7 to indicate an operate instruction; bit 3 must contain a 1, and bit 11 a 0 to indicate a group 2 microinstruction. Bits 4 through 10 may be set to indicate a specific group 2 microinstruction. If more than one of bits 4–7 or 9–10 is set, the instruction is a microprogrammed combination of group 2 microinstructions, which will be executed according to the logical sequence shown in Figure 5-4. Table 5-4 lists the group 2 microinstructions, their mnemonics, and the operations they perform.

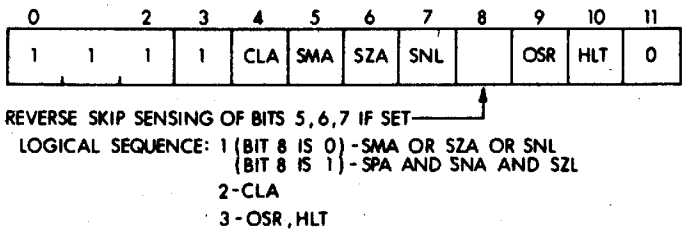


Figure 5-4 Group 2 Operate Microinstructions

Skip microinstructions may be microprogrammed with CLA, OSR, or HLT microinstructions, and also with other skip microinstructions that have the same value in bit 8. Skip microinstructions that have a 0 in bit 8 may not be microprogrammed with skip microinstructions that have a 1 in bit 8, however. When two or more skip microinstructions are microprogrammed into a single instruction, the resulting condition on which the decision will be based is the logical OR of the individual conditions when bit 8 is 0, or the logical AND of the individual conditions when bit 8 is 1 (Figure 5-4).

Table 5-2
Group 1 Operate Microinstructions

MNEMONIC	OCTAL	OPERATION
NOP	7000	No Operation. This instruction causes a 1-cycle delay in program execution without affecting the state of the computer. It may be used for timing synchronization or as a convenient means of deleting another instruction from a program.
IAC	7001	Increment Accumulator. The content of the accumulator is incremented by 1. The link is complemented if there is a carry from the most significant bit of the AC.
BSW	7002	Byte Swap. The content of the six low-order bits of the AC is exchanged with the content of the six high-order bits. That is, AC0 is exchanged with AC6, AC1 is exchanged with AC7, etc. The content of the link is not affected.
RAL	7004	Rotate Accumulator Left. The content of AC1–11 is shifted into AC0–10. The content of AC0 is shifted into the link, and the content of the link is shifted into AC11.
RTL	7006	Rotate Two Left. Equivalent to two consecutive RAL operations.
RAR	7010	Rotate Accumulator Right. The content of AC0–10 is shifted into AC1–11. The content of the link is shifted into AC0, and the content of AC11 is shifted into the link.
RTR	7012	Rotate Two Right. Equivalent to two consecutive RAR operations.
CML	7020	Complement Link, The content of the link is complemented.
CMA	7040	Complement Accumulator. The content of each bit of the AC is complemented. This has the effect of replacing the content of the AC with its one's complement.
CLL	7100	Clear Link. The link is loaded with a binary 0.
CLA	7200	Clear Accumulator. Each bit of the AC is loaded with a binary 0.

Table 5-3
Microprogrammed Combinations of Group 1 Microinstructions

MNEMONIC	OCTAL	OPERATION
CIA	7041	Complement and Increment Accumulator. The content of the AC is replaced with its two's complement. This is a microprogrammed combination of CMA and IAC.
STL	7120	Set the Link. The link is loaded with a binary 1. This is a microprogrammed combination of CLL and CML.
STA	7240	Set the Accumulator. Each bit of the AC is loaded with a binary 1. This is a microprogrammed combination of CLA and CMA.
GLK	7204	Get the Link. The AC is cleared and the content of the link is shifted into AC11 while a 0 is shifted into the link. This is a microprogrammed combination of CLA and RAL.

Table 5-4
Group 2 Microinstructions

MNEMONIC	OCTAL	OPERATION
HLT	7402	Halt. Clears the run flip-flop so that program execution stops at the end of TP4 of the current machine cycle.
OSR	7404	Logical OR with Switch Register. The content of the programmer's console switch register (SR) is combined with the content on the AC by a bitwise logical OR operation. The result is left in the AC and the original content of the AC is lost. The content of the SR is not affected.
SKP	7410	Skip. The content of the PC is incremented by 1 to skip the next sequential instruction.
SNL	7420	Skip on Non-Zero Link. The content of the link is sampled. If the link contains a 1, the content of the PC is incremented to skip the next sequential instruction. If the link contains a 0, the PC is not incremented.

Table 5-4 (Cont.)
Group 2 Microinstructions

MNEMONIC	OCTAL	OPERATION
SZL	7430	Skip on Zero Link. The content of the link is sampled. If the link contains a 0, the content of the PC is incremented to skip the next sequential instruction. If the link contains a 1, the PC is not incremented.
SZA	7440	Skip on Zero Accumulator. The content of each bit of the AC is sampled. If every bit contains a 0, the content of the PC is incremented to skip the next sequential instruction. If any bit contains a 1, the PC is not incremented.
SNA	7450	Skip on Non-Zero Accumulator. The content of each bit of the AC is sampled. If any bit contains a 1, the content of the PC is incremented by 1 to skip the next sequential instruction. If every bit contains a 0, the PC is not incremented.
SMA	7500	Skip on Minus Accumulator. The content of AC0 is sampled. If AC0 contains a 1, indicating that the AC contains a negative two's complement number, the content of the PC is incremented to skip the next sequential instruction. If AC0 contains a 0, the PC is not incremented.
SPA	7510	Skip on Positive Accumulator. The content of AC0 is sampled. If AC0 contains a 0, indicating that the AC contains a positive two's complement number (or zero), the content of the PC is incremented to skip the next sequential instruction. If AC0 contains a 1, the PC is not incremented.
CLA	7600	Clear Accumulator. Each bit of the AC is loaded with a binary 0.

Table 5-5 lists every legal combination of skip microinstructions, with the conditions on which the decision to skip or execute the next sequential instruction is based. This table does **not** include microprogrammed combinations of skip microinstructions and the CLA, OSR, or HLT microinstructions.

Group 3 Microinstructions—Group 3 microinstructions are used to transfer data between the AC and multiplier quotient (MQ) registers. Figure 5-5 shows the format of a group 3 microinstruction. The operation code must be 7 to indicate an operate instruction, while bits 3 and 11 must

Table 5-5
Microprogrammed Combinations of Group 2 Microinstructions

MNEMONIC			OCTAL	OPERATION
SZA	SNL		7460	Skip if AC = 0 or L = 1 or both.
SNA	SZL		7470	Skip if AC = 0 and L = 0.
SMA	SNL		7520	Skip if AC < 0 or L = 1 or both.
SPA	SZL		7530	Skip if AC ≥ 0 and L = 0.
SMA	SZA		7540	Skip if AC ≤ 0.
SPA	SNA		7550	Skip if AC > 0.
SMA	SZA	SNL	7560	Skip if AC ≤ 0 or L = 1 or both.
SPA	SNA	SZL	7570	Skip if AC > 0 and L = 0.

both contain a 1 to indicate a group 3 microinstruction. Any one of bits 4, 5, or 7 may be set to indicate a specific group 3 microinstruction. If more than one of these bits is set, the instruction is a microprogrammed combination of group 3 microinstructions. Bits 6, 8, 9, and 10 are ignored by the PDP-8/A, but should always be made 0 to guarantee compatibility with other machines in the PDP-8 series which have Extended Arithmetic Element (EAE) capability.

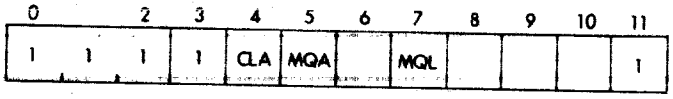


Figure 5-5 Group 3 Operate Microinstructions

Table 5-6 lists the group 3 microinstructions, their assigned mnemonics, and the operations they perform. This table also lists two useful microprogrammed combinations of group 3 microinstructions.

5.2.3. Jump Instruction (JMP)

The Jump Instruction references a memory location and loads the address of the memory location into the Program Counter (PC). This address is then the address of the next instruction to be executed. Figure 5-6 shows the format of the instruction and Table 5-7 shows the mnemonic, the opcode and the operation of the instruction.

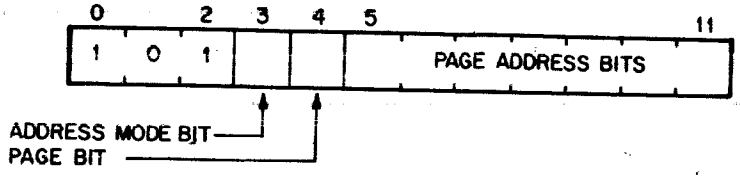


Figure 5-6 Jump Instruction Format

5.3. MAJOR STATES OF AN INSTRUCTION

To process an instruction, the PDP-8/A must:

1. Obtain the instruction from memory. This operation is commonly called "fetching" the instruction. If no additional information is

Table 5-6
Group 3 Microinstructions

MNEMONIC	OCTAL	OPERATION
CLA	7601	Clear Accumulator. Each bit of the AC is loaded with a binary 0.
MQL	7421	Multiplier Quotient Load. The content of the AC is loaded into the MQ. The AC is cleared, and the original content of the MQ is lost.
MQA	7501	Multiplier Quotient into Accumulator. The content of the MQ is combined with the content of the AC by a bitwise logical OR operation, and the result is loaded into the AC. The original content of the AC is lost, but the original content of the MQ is not affected. Note that this instruction provides the programmer with a direct inclusive OR operation.
SWP	7521	Swap Accumulator and Multiplier Quotient. The content of the AC and the content of the MQ are exchanged. This is a microprogrammed combination of MQA and MQL.
CAM	7621	Clear Accumulator and Multiplier Quotient. Each bit of both the AC and the MQ are loaded with a binary 0. This is a microprogrammed combination of CLA and MQL.

Table 5-7
Jump Instruction

MNEMONIC	OCTAL	OPERATION
JMP	5XXX	Jump. The 12-bit address of the memory location specified by XXX is loaded into the PC so that the instruction stored at this address will be the next instruction to be executed. The original content of the PC is lost. The content of the AC is not affected.

needed to execute the instruction, the instruction is executed during the FETCH cycle. The PDP-8/A then fetches the next instruction. OPR,

IOT, and direct JMP are the only instructions that are executed in the FETCH cycle. All other instructions load the page address into the memory address register (MA) and then enter a DEFER or EXECUTE cycle.

2. If the instruction is an indirect AND, TAD, ISZ, DCA, JMS or JMP, the PDP-8/A enters a DEFER cycle to obtain the indirect address from memory. This indirect word (which is first incremented if it is located in address 10–17) is either loaded into the PC (if the instruction is JMP) or loaded into the MA. If the instruction is a JMP, the PDP-8/A then fetches the next instruction; otherwise, it proceeds to the EXECUTE cycle.

3. The EXECUTE cycle is the cycle during which MRI instructions are actually carried out. The PDP-8/A fetches the next instruction after every EXECUTE cycle.

5.3.1. Instruction Execution Time

A summary of the time required and major states used to execute the various PDP-8/A instructions is contained in Table 5.8. The table assumes a 1.5 μs memory.

Table 5-8 Major State and Execution Time Summary

INSTRUCTION	MAJOR STATES USED (IN ORDER OF USAGE)	EXECUTION TIME* (μs)
Direct, AND, TAD, ISZ, DCA, JMS (Bit 3 = 0)	FETCH, EXECUTE	3.0
Indirect, AND, TAD, ISZ, DCA, JMS (Bit 3 = 1)	FETCH, DEFER, EXECUTE	4.5
Direct, JMP (Bit 3 = 0)	FETCH	1.5
Indirect, JMP (Bit 3 = 1)	FETCH, DEFER	3.0
IOT, Operate	FETCH	1.5

* Assumes 1.5 μs memory.

CHAPTER 6

CONSOLE OPERATION

6.1 INTRODUCTION

There are two types of consoles for the PDP-8/A—the operator's panel and the programmer's console. The operator's panel is supplied with each PDP-8/A. The programmer's console is optional.

6.2 OPERATOR'S PANEL

The operator's panel (Figure 6-1) contains the necessary switches to apply power and bootstrap the computer, and also contains the necessary indicators—POWER ON, RUN, and BATTERY CHARGING—to determine whether or not the computer is operating. Table 6-1 describes the function of the various switches on the panel. A PANEL LOCK switch is provided to prevent the accidental modification of memory contents or system operation by inappropriate use of switches on the programmer's console.

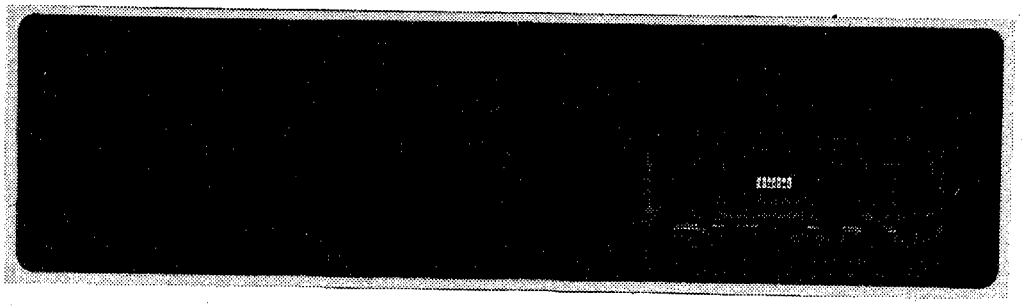


Figure 6-1 PDP-8/A Operator's Panel

6.3 PROGRAMMER'S CONSOLE

The key pad switches and indicators on the PDP-8/A programmers' console (Figure 6-2) augment the operator's panel by allowing manual control of computer operation and presenting a convenient indication of system conditions. PDP-8/A program execution can be started, stopped, monitored, or switched between various modes of operation by use of the keys. The key pad switches also provide a means of selecting a memory location or major register for examination and allow selective modification of read/write memory. Table 6-2 describes the indicators and functions relating to the programmer's console.

Table 6-1 PDP-8/A Operator's Console Controls and Indicators

CONTROL OR INDICATOR	FUNCTION
POWER ON/OFF	In the up position, this switch applies power to the computer and all controls and indicators. Power is removed by moving the switch down.
PANEL LOCK	In the up position, this switch prevents the removal of power from the computer and disables all key pad switches except switch register (SR) and the read functions.
BOOT	When this switch is down, the Omnibus SW line is disabled (voltage level high). When it is up, the SW line is asserted (low). This switch is used to start programmable read only memory (PROM) and bootstrap loader programs. The key pad BOOT switch on the programmer's console has the same function.
POWER	This indicator is lit when ac power is applied to the computer.
BATTERY CHARGING	This indicator is lit when the battery backup supply is charging.
RUN	This indicator is lit when the RUN flip-flop is set.

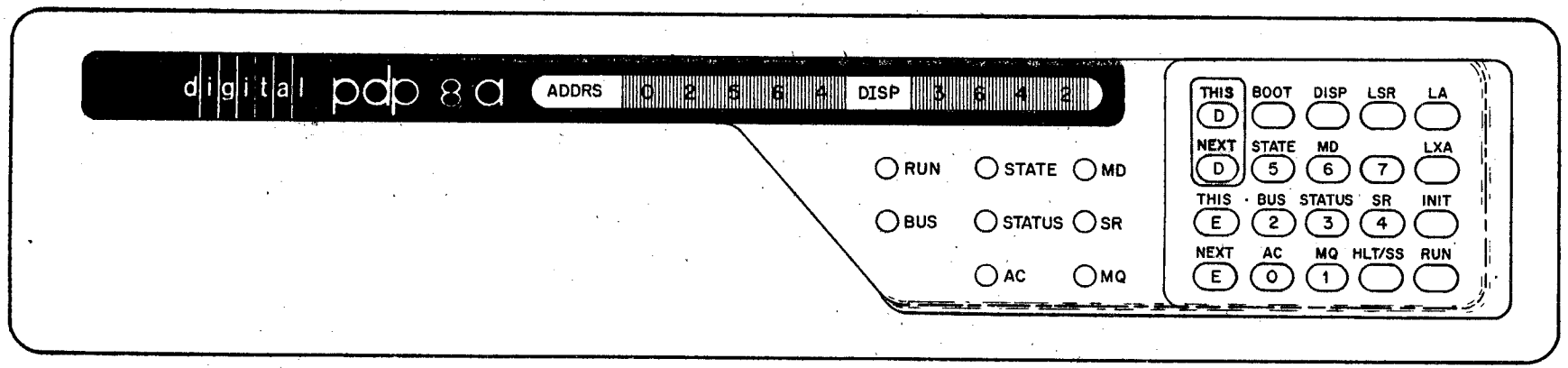


Figure 6-2 PDP-8/A Programmer's Console

Table 6-2 PDP-8/A Programmer's Console Controls and Indicators

CONTROL OR INDICATOR	FUNCTION
ADDRS (Octal Readout)	ADDRS is a 5 character octal readout that displays the content of the 3-bit extended memory address (EMA) register and the 12-bit memory address (MA) register. The five characters (digits) show the address of the memory to be accessed next.
DISP (Octal Readout)	DISP is a 4 character octal readout that displays the content of the register that has been selected for display. The accumulator (AC), multiplier quotient (MQ), STATUS register, switch register (SR), STATE, memory data (MD), or data bus (BUS), contents may be read. To select one of these for display, first depress the appropriate key pad switch (i.e., AC) and then press DISP. One of the LED indicators to the left of the key pad will be lit indicating which data is displayed in the readout. If none of the indicators are lit, the content of the entry register is displayed.
RUN	This indicator is lit when the RUN flip-flop is set.
Key Pad Switches AC (0)	When key pad AC and then DISP are depressed, the content of the AC is displayed in the 4 character octal readout. The AC indicator to the left of the key pad will also light.
MQ (1)	When key pad MQ and then DISP are depressed, the content of the MQ register is displayed in the 4 character octal readout. The MQ indicator to the left of the key pad will also light.
BUS (2)	When key pad BUS and then DISP are depressed, the content of the DATA BUS (DATA 0–11) is displayed in the 4 character octal readout. The BUS indicator to the left of the key pad will also light.
STATUS (3)	When key pad STATUS and then DISP are depressed, the contents of the STATUS register is displayed in the 4-bit octal readout (Figure 6-3). The STATUS indicator to the left of the key pad will also light. The six most significant bits of the status register (bits 0–5) indicate either a set or cleared condition (logical one or logical zero). Thus, the octal readout for

Table 6-2 (Cont.)
PDP-8/A Programmer's Console Controls and Indicators

CONTROL OR INDICATOR	FUNCTION
	these digits must be decoded to determine whether the bit is set or cleared.

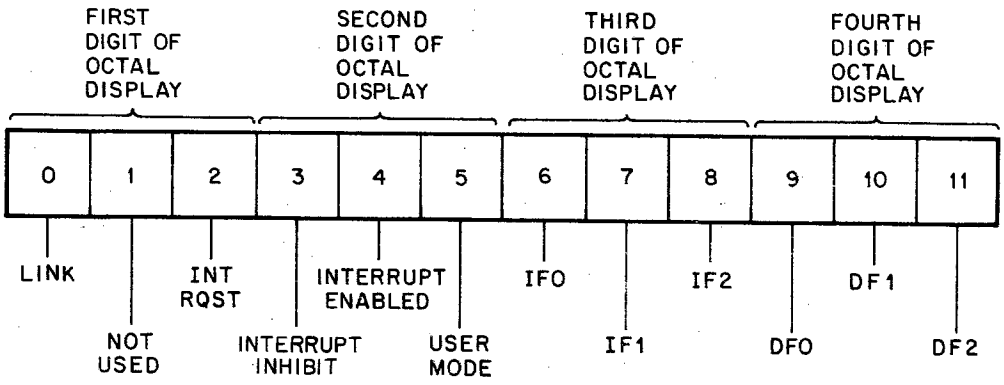


Figure 6-3 Status Register

First Digit Position	An octal 4 or 5 indicates that the link is set. An octal 1 or 5 indicates that the Omnibus interrupt request line is asserted.
Second Digit	An octal 4, 5, 6, or 7 indicates that the interrupt inhibit flip-flop is set. The interrupt inhibit flip-flop is located in the memory extension and timeshare option.
	An octal 2, 3, 6, or 7 indicates that the interrupt system is enabled.
	An octal 1, 3, 5, or 7 indicates that the USER MODE line is asserted. Signal USER MODE originates in the memory extension and timeshare option on the KM8-A option board to disable execution of all OSR, LAS, HLT and IOT instructions when the computer is operating in timeshare mode.
Third Digit	Displays the content of the 3-bit instruction field register (IF0–2) contained in the memory extension and timeshare option on the KM8-A option board.
Fourth Digit	Displays the content of the 3-bit data field register (DF0–2) contained in the memory extension and timeshare option on the KM8-A option board.
SR (4)	When key pad switch SR and then DISP are depressed, the content of the SR (switch register) will be displayed in the 4 character octal readout. The SR indi-

Table 6-2 (Cont.)
PDP-8/A Programmer's Console Controls and Indicators

CONTROL OR INDICATOR	FUNCTION
	cator to the left of the key pad will also light.
STATE (5)	When key pad switch STATE and then DISP are depressed, the condition of the major states, 3 bits of the instruction register (IR0–2), and 6 major Omnibus signals are displayed in the 4 character octal readout (Figure 6-4). The STATE indicator to the left of the key pad will also light. The octal readout must be decoded to determine if the individual bits are in a set or cleared condition (a logical one or a logical zero).

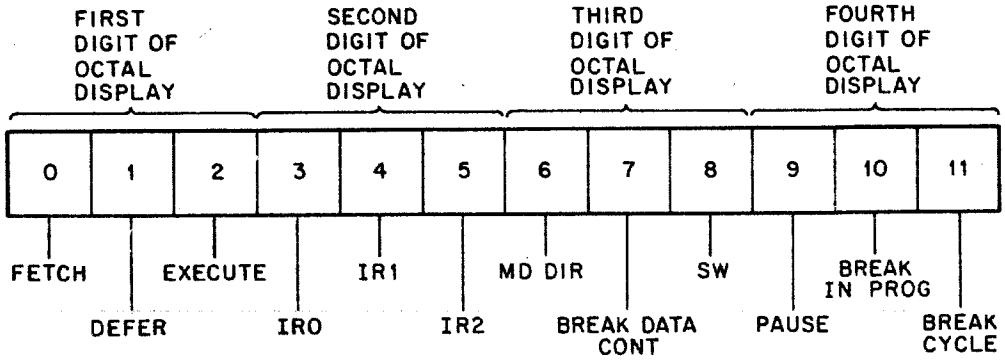


Figure 6-4 Major States Register

First Digit	A zero indicates that the processor is in the DMA state. An octal 1 indicates that the processor is in the EXECUTE major state. An octal 2 indicates that the processor is in the DEFER major state. An octal 4 indicates that the processor is in the FETCH major state.
Second Digit	Displays the content of the 3-bit instruction register (IR0–2).
Third Digit	An octal 4, 5, 6, or 7 indicates that the MD DIR line on the Omnibus is asserted (low). Signal MD DIR is low and bit 6 is a logical one during operations that read data from memory. MD DIR is high and bit 6 is a logical 0 during operations that write data into memory.

Table 6-2 (Cont.)
PDP-8/A Programmer's Console Controls and Indicators

CONTROL OR INDICATOR	FUNCTION
	An octal 2, 3, 6, or 7 indicates that BREAK DATA CONT line on the Omnibus is asserted. BREAK DATA CONT is low and bit 7 is a logical one during some direct memory access (DMA) operation.
	An octal 1, 3, 5, or 7 indicates that the SW line on the Omnibus is asserted. This occurs only when BOOT on the programmer's console or the operator's panel is depressed.
Fourth Digit	An octal 4, 5, 6, or 7 indicates that the I/O PAUSE line on the Omnibus is asserted. Signal I/O PAUSE L is generated during execution of an IOT instruction.
	An octal 2, 3, 6, or 7 indicates that the BREAK IN PROG line on the Omnibus is asserted (one or more devices are requesting a data break). The highest priority device will begin a DMA operation at the beginning of the next cycle.
	An octal 1, 3, 5, or 7 indicates that the BREAK CYCLE line on the Omnibus is asserted, (a DMA operation is taking place).
MD (6)	When MD and then DISP are depressed, the data on the 12-bit MEMORY DATA bus (MD0–11) on the Omnibus are displayed in the four character octal readout. The bus normally carries the content of the last memory location addressed by the 15-bit memory address register.
LA	Depressing LA (load address) loads the contents of the entry into the central processor memory address (CPMA) register and enables the FETCH major state for the next processor cycle.
LXA	Depressing LXA (load extended address) loads the right most digit of the entry into the data field (DF) register and the next digit of the entry into the instruction field (IF) register.
INIT	Depressing INIT (Initialize) generates an INIT pulse that clears the AC, the LINK, all I/O device flags and registers, and all interrupt system flip-flops. This is equivalent to a programmed CAF instruction.

Table 6-2 (Cont.)
PDP-8/A Programmer's Console Controls and Indicators

CONTROL OR INDICATOR	FUNCTION
RUN	Depressing RUN generates a MEM START L signal, which sets the RUN flip-flop. The program starts executing at the address that is in the CPMA register.
LSR	Depressing LSR switch loads the entry into the switch register. The switch register serves as a 12-bit temporary storage register for data entries. The contents of the switch register can be read under program control by the OSR and LAS instruction.
BOOT	Depressing BOOT twice causes the SW flip-flop to assert and then negate the SW line on the Omnibus. The transition from assertion to negation of the SW line causes a bootstrap operation to be performed. The signal from this BOOT switch is ORed with the signal generated by BOOT on the operator's panel so that either switch can assert the SW signal on the Omnibus.
E THIS	Depressing E THIS (examine this) loads the contents of the memory location addressed by the CPMA register into the memory buffer (MB) register. The CPMA and PC are not incremented after this operation. To observe the contents of the MB, depress MD, then DISP.
E NEXT	Depressing E NEXT (examine next) loads the content of the memory location addressed by the CPMA into the memory buffer (MB) register and increments the CPMA and PC registers. This feature allows the operator to step through a program and observe the operation of one of the major registers, buses, etc., in the octal readout.
D THIS	Depressing D THIS (deposit this) loads the content of the entry into the MB register and into memory at the address specified by the CPMA register. The CPMA and PC are not incremented by this operation.
D NEXT	Depressing D NEXT (deposit next) loads the content of the entry into the MB register and into memory at the address

Table 6-2 (Cont.)
PDP-8/A Programmer's Console Controls and Indicators

CONTROL OR INDICATOR	FUNCTION
	specified by the CPMA register. At the end of the operation, the PC and CPMA registers are incremented.
HLT/SS	Depressing HLT/SS (halt/single step) while the machine is running will cause it to stop. If the machine is stopped, depressing HLT/SS causes the machine to execute one machine cycle.

6.3.1 Entering Data From the Programmer's Console

Data is entered into registers from the programmer's panel by depressing the numbered key pad switches corresponding to the octal number to be entered, followed by depressing the key pad switch corresponding to the register into which the data is to be entered. For example, to load an octal number 7000 into the switch register, depress 7, then depress 0 three times, and then depress LSR. The data entered will be transferred to the switch register. To read the data that was entered in the switch register, press SR and then DISP (Table 6-2) and the data is displayed in the 4 character octal readout.

6.3.2 Examining Memory Locations

To determine the content of a location in memory, enter the memory field and depress LXA, then enter the memory address and depress LA. Depress MD and then DISP. Now depress E THIS and the contents of this memory location will be displayed in the 4 character octal readout. If two or more consecutive memory locations are to be examined, depress E NEXT. The content and the next memory location will be displayed each time E NEXT is depressed.

6.3.3 Entering Data in Memory

To enter (deposit) data in a memory location, first enter the field into which data is to be deposited and depress LXA. Then, enter the address and depress LA. Now enter the data and depress D THIS. If data is to be entered into two or more consecutive memory locations, depress D NEXT after each entry is made.

CHAPTER 7

OMNIBUS

7.1 GENERAL

Commands and signals, are transferred between modules on the PDP-8 computer via the Omnibus. The Omnibus is a circuit board with rows of connectors soldered to it. Because all connectors on the Omnibus carry the same signals, a module can be placed anywhere on the bus at the convenience of the user. All random backplane wiring is eliminated. Considerable space is conserved, providing a unique packaging capability that allows a high density of electronic circuitry in a small area.

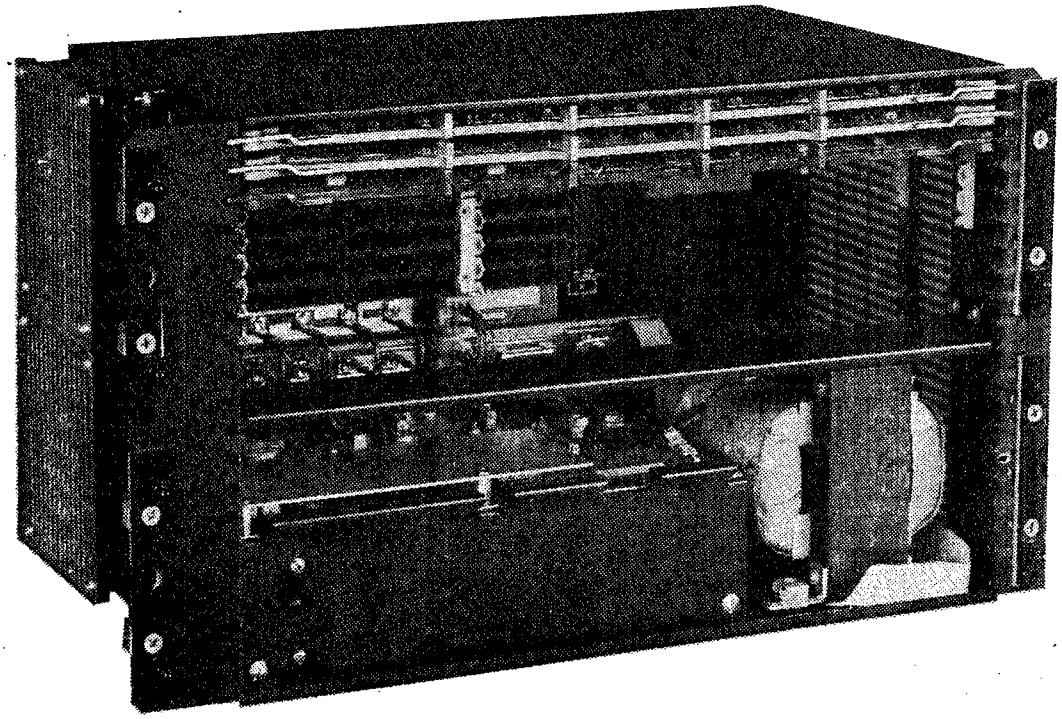


Figure 7-1 Omnibus Mounted in PDP-8/A Cabinet

7.2 BUS STRUCTURE

The Omnibus is a printed circuit board with connectors to it. It is attached to the PDP-8/A mounting box and is the means by which all modules are connected. There are slots for hex modules (quad modules plug into hex module slots). Slot number 1 (top slot) is reserved for the CPU, and the option boards are installed in slots 2 or 3. MOS memory cannot be installed in slots 2 or 3.

If a functional unit on the bus requires more than one module, H851 edge type connectors on the top of the board connect multiple boards together. For cables to the "outside world," connectors on the side of the module connect to a shielded coaxial or flat ribbon cable.

7.3 BUS SIGNAL SPECIFICATIONS

Logic Levels

Logic 1,	Max Voltage:	0.4 V
	Min Voltage:	−0.5 V
Logic 0,	Max Voltage:	4.5 V
	Min Voltage:	2.7 V

7.4 OMNIBUS SIGNAL SUMMARY

The Omnibus consists of 96 signals which can be divided into 9 major classes depending on their use within the computer.

7.4.1 Memory Address (15 Lines)

The 15 signals EMA (0-2) L, MA (0-11) L form a bus which defines the currently active memory address. The source of MA (0-11) L is the CPU during instruction processing, and the currently active data break device during DMA operations. The source of EMA (0-2) L is the memory extension control during instruction processing, and the currently active data break device during DMA operations. Load resistors within the CPU define EMA (0-2) L as zeros (highs) if there is no memory extension control in the system.

7.4.2 Memory Data and Direction Control (13 Lines)

The 12 signals MD (0-11) L form a bidirectional data path between memory and CPU. In addition, these lines are monitored by programmed I/O devices to determine device code and sub-device operation, and by data break devices to obtain output (memory-to-DMA device) words.

The source of information on MD (0-11) L is controlled by MD DIR L. If MD DIR L is low, the data on the currently active memory is gated onto MD (0-11) L. If MD DIR L is high, the contents of the CPU's memory buffer register is gated onto MD (0-11) L.

7.4.3 Data Bus (12 Lines)

The 12 signals DATA (0-11) L form a multipurpose 12-bit bus. This bus is used for data exchange between peripheral and CPU, for data input from DMA devices, for front panel monitoring of selected registers, and for the determination of data break priority.

7.4.4 I/O Control Signals (10 Lines)

This group of signals controls the I/O dialogue between CPU and programmed peripherals. This group also includes INITIALIZE H, which is used for clearing peripheral flags.

7.4.5 DMA Control Signals (8 Lines)

This group of signals controls the operation of data break (DMA). Several of these signals are also activated for certain front panel operations. Also included in this group is RUN L, which is used for clearing data break requests when the computer is halted.

7.4.6 Timing Signals (9 Lines)

Five time pulses serve as system clocks. Similarly, four time state levels serve as system enabling levels. All of these signals originate within the main timing generator of the CPU.

7.4.7 CPU State (6 Lines)
The major state of the CPU appears on the major state lines (F L, D L, E L). The operation code of the instruction currently being processed appears on IR (0-2) L.

7.4.8 Memory Timing Signals (5 Lines)
Five signals orginate in the main timing generator of the CPU and are bused to all memories. These signals (SOURCE H, RETURN H, WRITE H, INHIBIT H, and STROBE H) control all memory operations.

7.4.9 Miscellaneous Signals (18 Lines)
These signals do not fit into any of the categories just mentioned. A large percentage of them are used by the operator's console (front panel). Two signals (ROM ADDRESS L and NTS STALL L) are driven by some types of memories under special conditions and are monitored by the CPU and other memories. The remainder of these signals are truly miscellaneous. Included in this group is a signal (POWER OK H) that reports the validity of the power supply voltages.

A detailed description of all Omnibus signals and their pin assignments is contained in the *PDP-8/A Users' Manual.*

7.5 SELECTING AN OMNIBUS INTERFACE
This section provides information for users who want to select an interface. It deals primarily with the hardware and it is understood that the user must create his own program for his own functions. If the user lacks sufficient experience to design or program his interface, he can contact his local DIGITAL Sales Office for special design information.

Two basic types of peripherals are used with the PDP-8/A: one that is designed to transmit or receive one character or 12-bit word per service routine by the processor; and one that is designed to transmit or receive a block of characters or 12-bit words per service routine by the processor.

7.5.1 Data Transfer Types
There are three major types of data transfer available on the PDP-8/A: Programmed data transfers, programmed interrupt transfers, and data break (direct memory access).

PROGRAMMED DATA TRANSFER
The simplest method of accomplishing a data transfer is by means of non-interrupt, programmed I/O transfer. This method relies upon the processor to check the status flag, service the flag, and do a data transfer. The state of the flag is tested by an IOT instruction, which causes a skip if the flag is set. Data transfers take place between the PDP-8/A's accumulator and the device. The program is straightforward and consists of few instructions as shown in the following example for a terminal:

```
KSF         /Test keyboard flag.
JMP.–1      /Try again if flag not set.
KRB         /Get input, clear flag.
```

PROGRAMMED INTERRUPT TRANSFERS

Another method of input/output transfers is to employ the interrupt system. The hardware required is the same as the hardware needed for programmed I/O, with additional logic required to assert the INT RQST signal on the Omnibus if the device flag is set (DIGITAL-designed programmed I/O peripherals have this logic which allows them to be used in either programmed I/O or interrupt mode.) The major difference between programmed I/O transfer and interrupt operation is in the software. Proper use of the interrupt allows the PDP-8/A to run in a foreground-background mode, handling many I/O devices whenever they make an interrupt request for service and carrying on useful calculations as a background task. Refer to introduction to Programming, Chapter 6, Volume 1, for a thorough discussion of interrupt programming.

DATA BREAK TRANSFER

Use of the data break system allows data transfers between the device and memory in either direction without disturbing the state of the CPU. More hardware is required in the device controller, since the device must supply a 15-bit memory address to the Omnibus and count the number of data transfers. In most cases, programmed I/O is required as well as the data break hardware; therefore, this method is relatively expensive but it allows the highest transfer rate.

DATA TRANSFER RATES

Programmed I/O or the interrupt system may be used for data transfer rates up to 50K per second. For rates above 50K per second, the data break system should be used.

7.5.2 Hardware Selection

After the user has selected the type of interface, (programmed data I/O, programmed interrupt, or data break) he must choose the hardware to implement this interface. The following possibilities exist for the user:

1. Use the serial line unit and/or the general purpose input/output on DKC8-AA I/O Option Board. This offers a cost effective solution to many programmed I/O and programmed interrupt interfaces required for asynchronous serial devices.

2. Use a DIGITAL-designed and tested interface. DIGITAL has designed many interfaces for various types of peripherals that may be purchased as off-the-shelf items. Besides obtaining an interface that is an off-the-shelf item, the user may also obtain user and diagnostic software that has already been written for his interface.

3. Use a DIGITAL-designed and tested interface and make modifications to adapt it to the user's particular application. DIGITAL has personnel available to assist in the redesign and modification of the interface, or Computer Special Systems can do the necessary work and sell the interface ready for installation in the system with the user's peripheral.

4. Use one of the DIGITAL-designed and tested interface foundation modules with the necessary wirewrap pads for the user to install integrated circuits and design a customized interface for his peripheral device.

5. Design a completely new interface for the user's device.

The simplest and least costly way to interface is to buy an interface that has been designed and tested by DIGITAL; the most complicated and expensive way is to start from scratch and build one's own interface, although that may be necessary for specific applications. Regardless of how the user decides to proceed, the information in Chapter 8 should help him to select or design an interface for the PDP-8/A.

CHAPTER 8

INTERFACE

8.1 INTRODUCTION

This chapter provides an example of each interface type described in Chapter 7 so that the user can start design work for an interface to the PDP-8/A. More detailed information about interfacing to the Omnibus and a detailed description of all Omnibus signals is contained in the *PDP-8/A Users Manual.*

The interface examples contain some special integrated circuits (IC). These ICs, which are listed below, were chosen to minimize loading on the Omnibus. Do not replace them with other devices having the same functions unless you have compared input loading and threshold figures (for input devices) or output driver and leakage (for the output device).

Input Devices (Device Number)	Manufacturer Type	DEC Part Number
314	Signetics SP314A	19-09704
380	Signetics SP380A	19-09485
384	Signetics SP384A	19-09486
8640		19-11469
Output Devices (Device Number)	**Manufacturer Type**	**DEC Part Number**
8881	Several 7438*	19-09705

*The 7438 has a different pin assignment from that of the 8881, but has the necessary electrical parameters.

8.2 PROGRAMMED DATA TRANSFER

Programmed data transfer is the easiest and most common means of performing I/O. Each input/output transfer (IOT) instruction initiates one programmed transfer which may transmit data or status information either to or from a peripheral device. The amount of information that will be transferred by an IOT instruction depends upon the particular operation that is coded into the instruction and the design of the I/O device interface. In general, programmed data transfers are limited to a maximum of 12 bits of information per IOT instruction.

8.2.1 Peripheral Device Status

Many I/O devices maintain only one bit of status information. This is usually the state of a busy/done flip-flop which indicates whether the device is in the process of performing a data transfer or free to commence a new I/O operation. Thus, IOT instructions that set or modify device status often require no data transfer.

8.2.2 Peripheral Data Transfer

If an information transfer is required, the I/O device must decode the operation specification bits to determine the exact nature of the transfer,

gate the content of its device buffer onto the Omnibus if necessary, then generate up to three control signals which enable the adder circuits and shift gates of the central processor to perform one of six possible operations:

1. Data may be received from a device, ORed with the content of the AC, and the result loaded into the AC.
2. Data may be received from a device and added to the content of the PC.
3. Data may be received from a device and loaded into the PC.
4. The content of the AC may be sent to a device and the AC may then be cleared.
5. Data may be received from a device and loaded into the AC.
6. The content of the AC may be sent to a device.

The six operations listed are the data transfer operations that may be performed during a programmed data transfer by any I/O device, but not all of these operations are performed by every device. These operations are performed by circuitry in the central processor controlled by signals generated at the I/O device interface. The maximum of three control signals an I/O device may generate for this purpose provides a total of eight data transfer operations, two of which are redundant.

Unless a peripheral is rather complicated, the entire I/O transfer can be completed within the time available in a normal memory cycle. If a peripheral device requires additional time to complete a data transfer, it may transmit a control signal that disables processor timing during some or all of the operations the device is capable of performing. The positive I/O interface (KA8-E) is an example. Refer to the *PDP-8/A User's Manual* for information on expansion of the I/O cycle.

8.2.3 Programmed I/O Interface Example

The basic interface (Figure 8-1) that illustrates the most commonly used transfer consists of: 1. a device selection circuit, 2. a device operations decoder, 3. I/O control logic, and 4. input/output buffers.

DEVICE SELECTION CIRCUIT

Bits MD3–8 are used to carry the device select information. The example given in Figure 8-1 shows the DEC380 and DEC314 being used as a simple decoder. When octal 52 is received and signal I/O PAUSE L is asserted by the processor, gate 314 is qualified. The output is used to assert signals INTERNAL I/O L and MY DEVICE L. No operation can occur unless signal MY DEVICE L is asserted by the device selection decoder.

OPERATIONS DECODER

Bits MD9–11 determine the type of operation to be performed. Three DEC 380's are shown (Figure 8-1) receiving these bits. The outputs of these gates are in turn presented to a binary-to-octal decoder type 8251 and the decoded results control the interface. The IOT's in Table 8-1 illustrate the various types of transfers available.

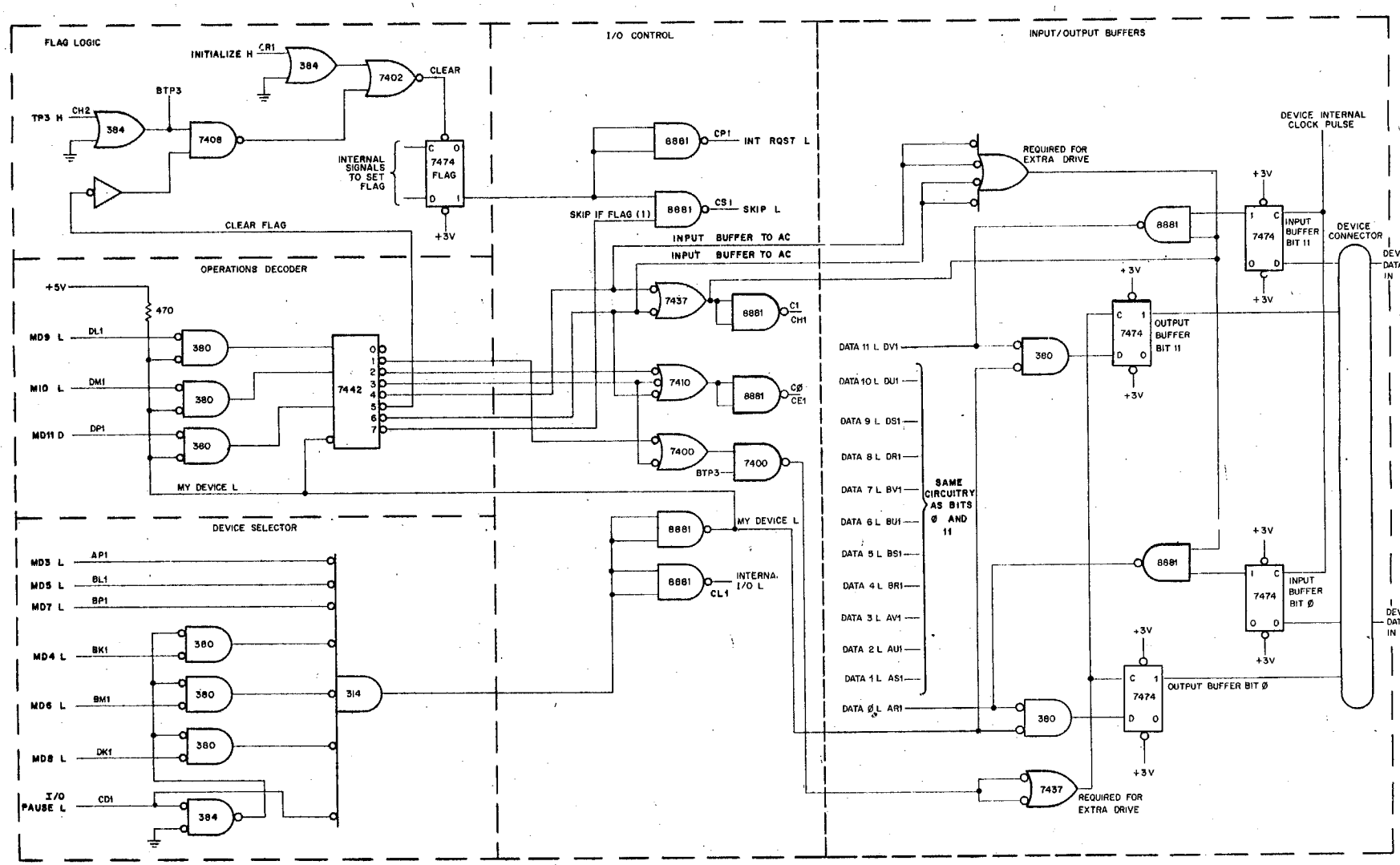


Figure 8-1 Sample Programmed I/O Interface

Table 8-1 IOTs For Sample Interface

IOT	FUNCTION
6520	Not used.
6521	Transfer contents of the AC to the output buffer.
6522	Clear the AC.
6523	Transfer the contents of the AC to the output buffer and clear the AC.
6524	Transfer the contents of the input buffer to the AC (OR transfer).
6525	Clear the flag.
6526	Transfer the contents of the input buffer to the AC (jam transfer).
6527	Skip if flag is set (1).

FLAG LOGIC

The flag is represented as a 7474 D-type flip-flop. The C and D inputs are used by the peripheral device to set the flag. If the flag is an input flag it is set when data is loaded into the input holding register. If the flag is an output flag, it is set when the data in the output holding register has been processed by the peripheral, (i.e., when new data may be loaded into the output register without disturbing the output devices operation). For both input and output transfers, two flags are required.

INTERRUPT REQUEST

The basic I/O interface may also be used to perform interrupt transfers by adding a gate to assert the interrupt request line when a flag is set by an external signal (Figure 8-1). The processor responds to the INT RQST line by completing the current instruction and then executing a JMS to location 0. Simultaneously, the interrupt system is turned off. The execution of the JMS instruction saves the current program count in location 0. It is up to the program to identify the interrupting device by polling (testing) device flags sequentially. After the device has been serviced, the interrupt service routine returns to the main program with a JMP indirect instruction. It is a good idea to have an interrupt gate in the logic even if the interrupt system is not going to be used. There is no penalty for adding this gate because the CPU will not respond to the state of INT RQST unless the interrupt system is enabled or an SRQ instruction is executed. Including this gate allows the user to recode the program for interrupt without changing the hardware.

OUTPUT BUFFER

The output buffer receives processor data during IOT instructions and outputs data to a device under control of device timing. This buffer must be a D-type (edge-triggered) register. The command signal that loads the output buffer also initiates action within the peripheral. The output flag should be cleared at or before the time this buffer is loaded and should not be set again until the device has completely processed the data word.

INPUT BUFFER

The input buffer receives device data at the device timing and applies the data to the data bus during an IOT instruction. The same signal that loads the input buffer is often used to set the input flag.

I/O CONTROL

The I/O control includes INT RQST, which immediately responds when the flag is set; SKIP, which is asserted when IOT 6527 is decoded and the flag is set; C0 and C1, which may be asserted by the operations decoder during various conditions of data transfer; and input/output enabling logic, which responds to the operations decoder and controls the I/O buffers (Table 8-2).

INPUT/OUTPUT TIMING FOR PROGRAMMED I/O INTERFACES

A timing diagram corresponding to the programmed I/O interface example is illustrated in Figure 8-2. An explanation of the time periods from A to J are as follows:

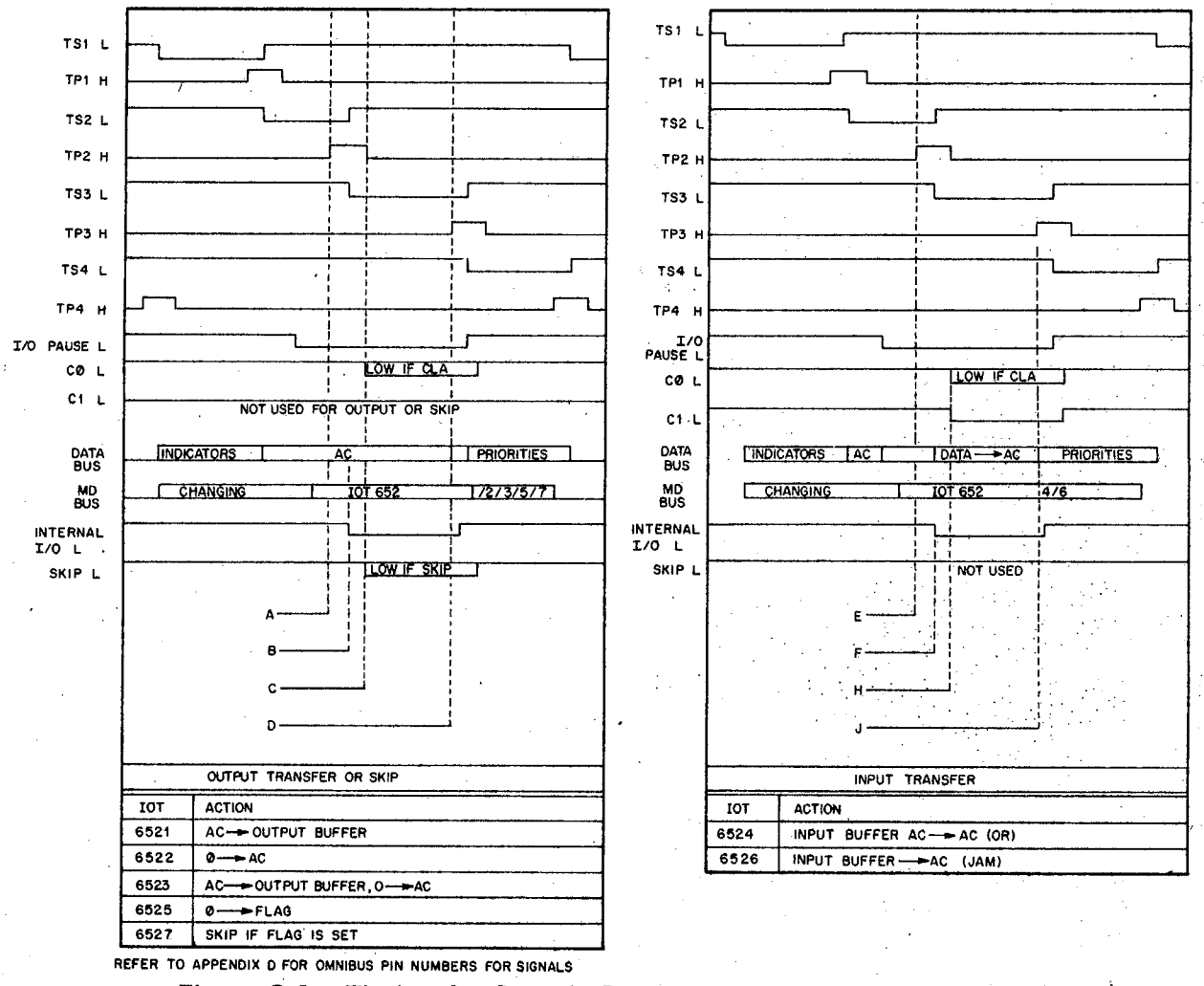
PERIOD	TIME	FUNCTION
A–D & E–J	350 ns	Time required to perform the transfer (PAUSE).
A–B & E–F	70 ns	Time required to decode the device selection and assert INTERNAL I/O.
A–C & E–H	100 ns	Time required to decode the IOT and assert the necessary "C" lines or SKIP and supply data if needed.
D & J		The time when the transfer takes place. Note that the data bus will change at this time. This is the reason that edge triggering must be used.

Note that the C lines control the direction of data transfer.

Table 8-2 Transfer Control Signals

TYPE OF TRANSFER	TRANSFER CONTROL LINES *C0	*C1	INFORMATION GATED ONTO THE DATA BUS	BUS SET-UP TIME WITH RESPECT TO BUS STROBE	ACTION REQUIRED BY PERIPHERAL AT INTERFACE	ACTION BY PROCESSOR	CONTENTS OF DATA BUS DURING TRANSFER
Output AC → Data Bus. AC unchanged.	H	H	AC Register	280 ns	Load data bus into buffer.	Transfers AC to Data Bus. AC remains unchanged.	AC register only. User modification of this type of transfer may bring undesirable results.
Output AC → DATA Bus AC Cleared	L	H	AC Register	280 ns	Ground C0. Load data bus into buffer.	Transfers AC to Data Bus and clears AC.	AC Register.
Input AC Peripheral Data	H	L	Peripheral Data & contents of AC Register.	280 ns	Gate peripheral data to data bus. Ground C1.	Transfers contents of AC to the Data Bus. The ORed result loaded into the AC.	AC ORed with Peripheral Data.
Input Jam. Data Bus → AC.	L	L	Peripheral Data	280 ns	Gate peripheral data to data bus. Ground C0 & C1.	Transfer data bus to AC register.	Peripheral Data.

*C0 is connected to pin CE1. C1 is connected to pin CH1 on the Omnibus.



REFER TO APPENDIX D FOR OMNIBUS PIN NUMBERS FOR SIGNALS

Figure 8-2 Timing for Sample Programmed I/O Interface Control

8.3 PROGRAM INTERRUPT TRANSFERS

The main difference between programmed interrupt transfers and programmed I/O transfers is the software required. Chapter 6, Introduction to Programming, contains a thorough discussion of software for the interrupt system. That discussion will not be repeated here.

The hardware required for interrupt transfers is the same as already described under programmed I/O transfers, except that the gate driving INT RQST L is required.

8.3.1 Interrupt Timing

Within each IOT, timing is the same as that already described for programmed I/O transfers. Since several devices may be simultaneously active using the interrupt system, the speed of response of the interrupt system is of interest.

The state of the interrupt system is sampled 350 nanoseconds before the end of every machine cycle. If a device requests an interrupt, the CPU will start executing the JMS to location 0, a maximum of 3 machine cycles plus 450 nanoseconds after receipt of the request. The JMS to location 0 takes one machine cycle, and the interrupt system is disabled in that same machine cycle. From this point on, the response time of the interrupt system depends on the instruction sequence of the interrupt handler. A typical interrupt handler program requires about 40 machine cycles to completely handle an interrupt. In critical cases, the user should count up the maximum number of machine cycles that can occur with the interrupt system disabled.

8.4 DATA BREAK TRANSFERS

Data break, sometimes called direct memory access or DMA (Figure 8-3), is the preferred form of data transfer for use with high-speed mass storage devices such as magnetic disk or DECtape units. Data break has two advantages over programmed I/O and the interrupt system: it takes precedence over instruction processing, and transfers take place directly between device and memory.

Unlike program interrupts, which are recognized only during the cycle in which execution of an instruction was completed, a data break always occurs at the conclusion of the machine cycle in which it was requested. If two devices request a data break simultaneously, the higher priority device begins its data break during the next cycle, and the lower priority request is honored as soon as the higher priority device relinquishes control. Once all break requests have been honored, instruction execution resumes at the point where it was discontinued. The processor major registers are never modified during a data break transfer so no restoration of machine status is necessary.

Data break devices usually have their own self-contained word count (WC) and current address (CA) registers. Once a device has been initialized to transfer a block of data, it forces the processor into a DMA state for one machine cycle whenever it is ready to transfer a 12-bit data word. The WC and CA registers are incremented before this cycle. As long as WC overflow does not occur, the device circuits remain enabled so that the device relinquishes control of the processor and begins to assemble the next word of data that will be transferred.

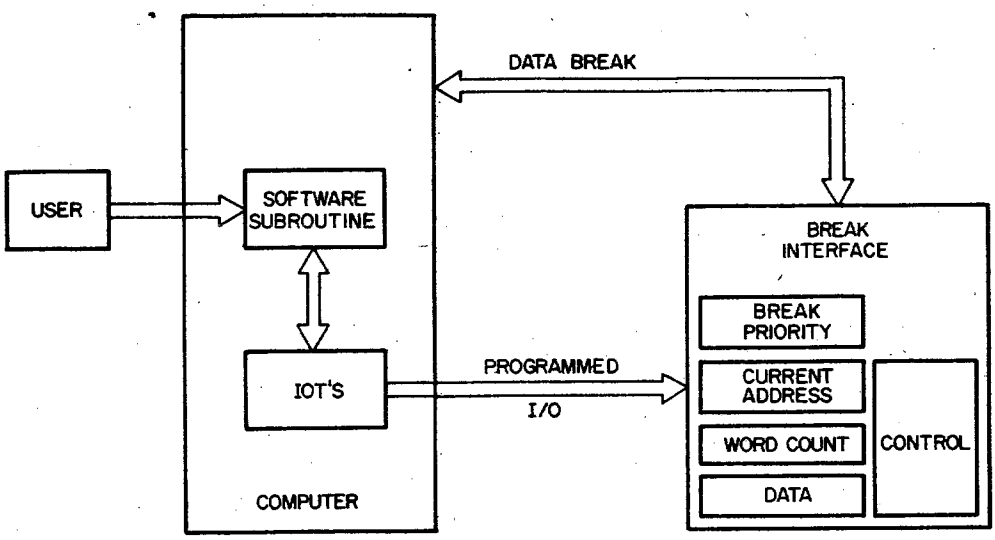


Figure 8-3 General Block Diagram of Basic Data Break Interface

When an internal data break peripheral is ready to perform a data transfer, it gates its priority bit onto the data bus during TS4 and determines whether a higher priority device is also requesting a data break. If there is no higher priority request, the device asserts signals which disable the processor major state generator, instruction register, and CPMA register. At the same time, the data bus is gated to the processor adder inputs to provide a bidirectional data path between the peripheral and the memory system. At this point, the procsesor enters a DMA cycle and the peripheral assumes control over the processor logic circuits by asserting various signal lines on the Omnibus.

During a data break, the peripheral device may generate signals that gate the content of a specified memory location out to the I/O device register, or it may gate the content of the device data register onto the data bus to a specified memory location overwriting the previous content of that location. The device may also gate the content of its data register and the content of a memory location to the processor adder inputs, add these values, and restore the two's complement sum to the designated memory location. This process, called "add data to memory," or ADM, is commonly used to increment the content of a memory location.

8.4.1 Word Count (WC) Register

A 12-bit word count register is also associated with every data break device. At the beginning of a data break transfer, the WC register contains the negative (two's complement) of the number of 12-bit words that remain to be transferred. The content of the WC register is incremented by 1 for every data break transfer. If this value becomes zero, word count overflow has occurred indicating that the word currently being transferred is the last word in the data block. Word count overflow generates a control signal which clears the I/O device enabling circuits and inhibiting further data transfers.

8.4.2 Current Address (CA) Register

A 12-bit current address register is associated with each data break device. At the beginning of a data break transfer, the CA register contains the 12-bit address of the memory location in which the last data break transfer was performed. The content of the CA register is incremented by 1 before a data break transfer, and the incremented value is used as the address of the memory location with which the current transfer will be performed. In this manner, a single I/O operation may transfer up to 4096 words of data between a peripheral device and a series of sequential memory locations.

8.4.3 Data Break Priority

Up to 12 data break peripherals may be interfaced with a PDP-8/A. One of the 12 data lines on the Omnibus is assigned to each data break device to determine break priority. The highest priority line, DATA0, is assigned to the fastest data break device, while the lowest priority line, DATA11, is assigned to the slowest device if the full complement of 12 data break devices is installed. When two or more devices request a data break simultaneously, the higher priority device makes the first DMA transfer.

8.4.4 Transfer Direction and Loading Logic

A method of controlling the type of transfer (input, output, or add to memory) must be provided on the data break control interface. To transfer data into memory via the data bus, the device data must be loaded into the CPU's MB register. This is accomplished by leaving Omnibus signals BREAK DATA CONT and MD DIR high so that the device data can be applied to memory. When it is necessary to add the device data to memory data, MD DIR is left high and the BREAK DATA CONT line is grounded. The MB register is automatically loaded every TP2.

8.4.5 Data Break Example

Figure 8-4 is a simplified diagram that illustrates the interaction between the processor and a single-cycle data break device. During initial set-up, the program executes IOT instructions which load the device WC register with the two's complement of the number of words in the block to be transferred. The CA register is then loaded with one less than the 12-bit address of the first memory location with which a transfer will be performed. Additional IOT instructions may specify the direction of the transfer, the memory field of the processor data buffer, or similar information depending upon the precise nature of the peripheral device. The initial set-up routine usually concludes by executing an IOT instruction that enables the device control circuitry.

As soon as the peripheral is ready to transfer a data word, it places a data break request on the Omnibus. The processor enters the DMA state during the following cycle and one word of data is transferred between the peripheral and memory. The processor then resumes program execution until the device is ready to transfer another word of data.

The device increments its WC and CA registers before each word of data transferred. If WC overflow occurs, the device completes the current transfer and begins the exit phase of the data break operation. In

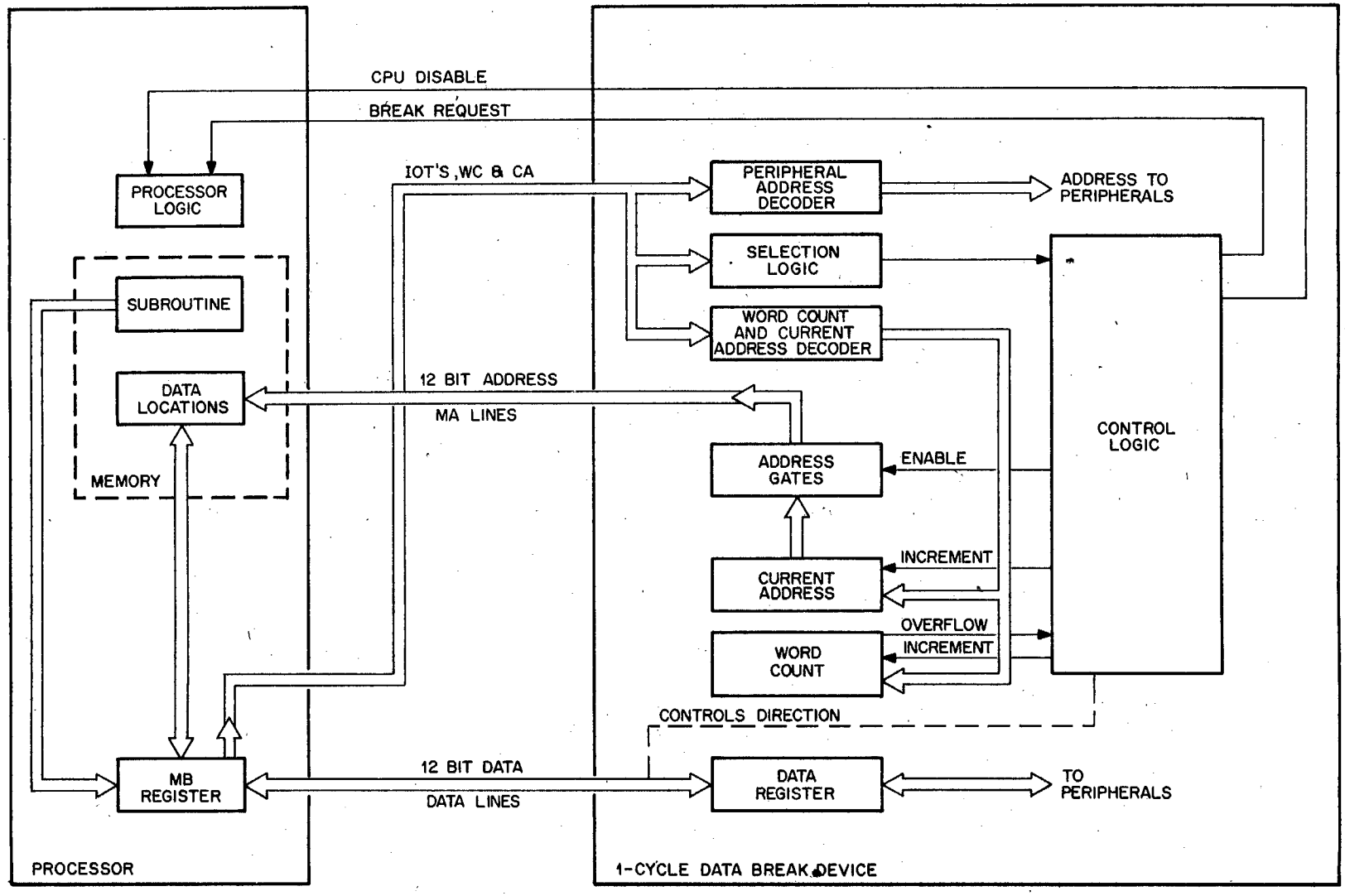


Figure 8-4 Single-Cycle Data Break Simplified Block Diagram

most cases, this simply involves clearing the enable circuitry and setting the device flag which will cause a program interrupt, provided the interrupt system is enabled. The processor normally responds by executing IOT instructions to determine whether error conditions were flagged during the transfer, for example, or to turn off any device components that were not disabled automatically by WC overflow.

8.4.6 Data Break Interface Example

The basic break interface required to transfer data consists of a break memory address register (BKMA) to address memory independently of the processor; a break priority network to assure the activation of the device with the highest priority; input/output buffers and break control logic. A sample data break interface is illustrated in Figure 8-5. The data break sequence of events is described in terms of the primary data break control signals and the processor timing given in Table 8-3.

8.4.7 Data Break Timing

The important timing consideration in data break (Figure 8-6), as in program interrupt, is whether sufficient time is availble from the time the flag (in this case, the break request) is set to the time the data is moved in or out of memory. The PDP-8/A honors break requests between major states of an instruction. The break system is synchronized 350 nanoseconds before the end of every memory cycle. At the same time the processor tests for the possibility of interrupt, it tests for the possibility of break. The break system takes precedence over interrupts. Assuming no extended I/O, the processor requires no more than 1 memory cycle +400 nanoseconds to recognize a break request.

As a rule, the user should assign highest priority to the device that has data available for the shortest amount of time. The user should assume that all devices request data breaks simultaneously and calculate the response time of the break system as seen by each device to ensure that response time is less than the maximum allowable for that device.

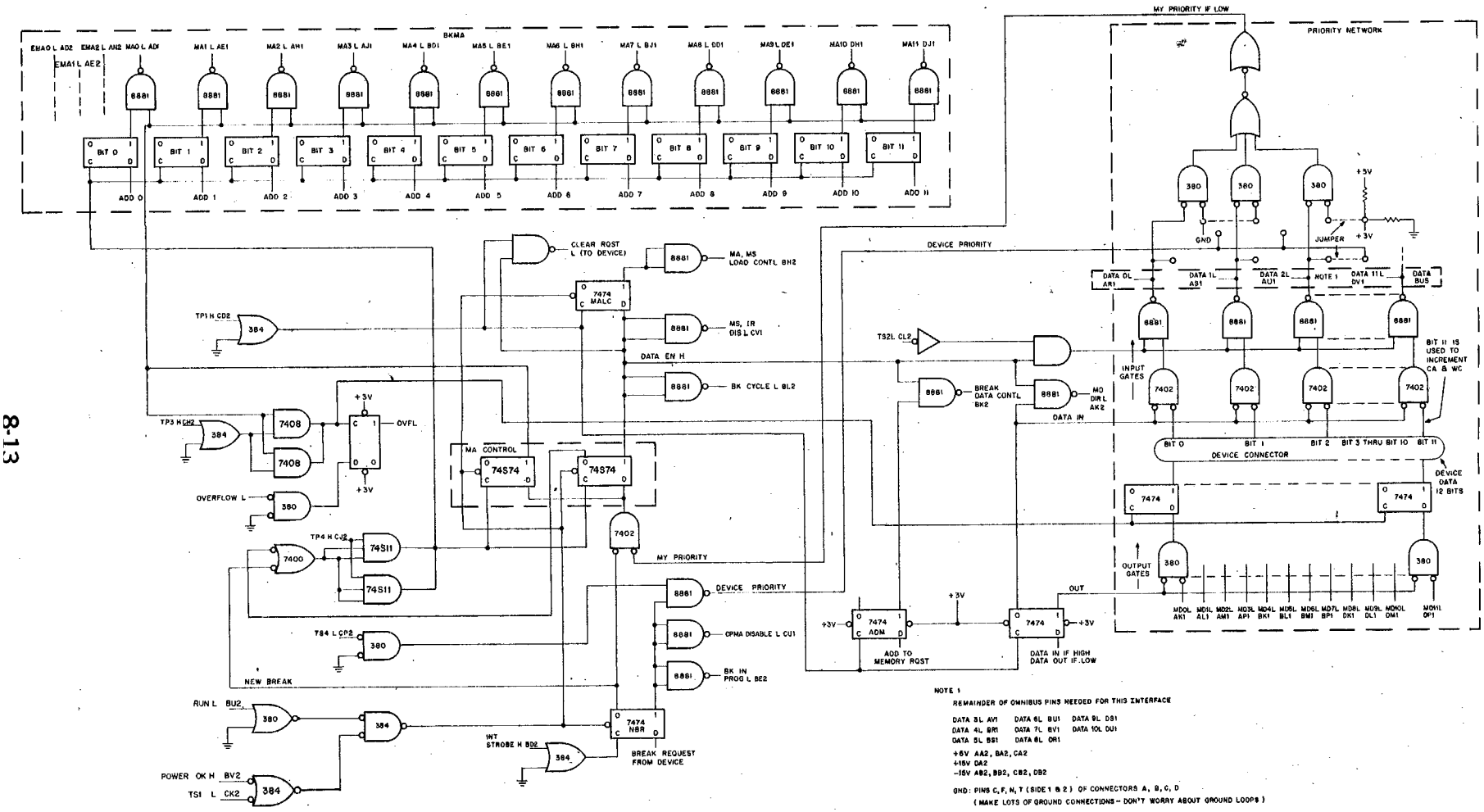


Figure 8-5 Sample One-Cycle Data Break Interface

Table 8-3 One-Cycle Data Break Sequence of Events

DATA BREAK EVENT	PROCESSOR TIMING	DESCRIPTION
BREAK REQUEST	Any time. Sampled by the leading edge of INT STROBE.	Signal BREAK REQUEST is developed by the device any time an input or output transfer is to be made. It is loaded into a new break (NBR) flip-flop by INTERRUPT STROBE, and causes the start of a series of events leading to data break transfers.
ADD TO MEMORY	Must be asserted not later than 100 ns prior to TP1.	Signal ADD TO MEMORY is generated at the same time as BREAK REQUEST whenever data is to be transferred into memory. It is loaded into the ADM flip-flop by TP1.
DATA IN	Must be asserted not later than 100 ns prior to TP1.	Signal DATA IN is enabled only when the data transfer is to memory and at the same time as BREAK REQUEST. It is loaded into a flip-flop by TP1.
INT STROBE L		The following signals are generated as the result of INT STROBE loading the NBR: a. BK IN PROG L (If break requested) b. CPMA DIS L (If break requested) c. DEVICE PRIORITY L (If break requested)
BREAK PRIORITY	TS4	Since each device priority was applied to the data bus at TP3, all priorities are tested during TS4. With the sample data break interface being a priority level 3, signal MY PRIORITY is developed if DATA 0 and DATA 1 are high. The condition of MY PRIORITY L and NBR (0) L will cause the MA CONTROL flip-flop to set at TP4.

Table 8-3 One-Cycle Data Break Sequence of Events (cont.)

DATA BREAK EVENT	PROCESSOR TIMING	DESCRIPTION
BREAK ADDRESS	TP4	The break address is supplied by the data break device. The contents of the address lines are loaded into the BKMA by TP4, and the 1 output of the MA CONT is used to gate the Break Address onto the MA lines.
PROCESSOR DMA STATE	TP4	The designer should watch the propagation delays of circuits so that not more than 50 ns elapses between the start of TP4 and the arrival of MAC(1) at the BKMA output gates. When the MA CONT flip-flop is set, signal MS, IR DIS L is asserted. This disconnects the outputs of the processor's major state and instruction registers and thereby causes the processor to enter into the DMA state. Signal BK CYCLE L is also asserted. If the transfer direction is from memory to the device, MD DIR L is asserted at TP1. If the transfer direction is from the device to memory, BREAK DATA CONT L is asserted at TP1.
INHIBIT MS and MA register loading	TP1	When MA CONT is set, the MALC flip-flop is loaded at TP1. This asserts the MA, MS LOAD CONT L line which prevents the MS and the MA registers from being loaded. The processor is now conditioned so that data break transfers will in no way affect the previous or the next processor instruction. At TP1 the ADM and/or OUT flip-flops are loaded to control the type of data transfer. The break request may be cleared by TP1.

Table 8-3 One-Cycle Data Break Sequence of Events (cont.)

DATA BREAK EVENT	PROCESSOR TIMING	DESCRIPTION
INPUT TRANSFER	TS2	Device data is gated in by DATA IN (0) L and applied to the DATA BUS by DATA EN H and TS2 L.
OUTPUT TRANSFER	TP3	Memory data is gated into the data break interface when a DATA IN L signal is present and loaded into the input buffer by TP3.
NEXT WORD	TP3	At TP3 of the data break cycle, signal INT STROBE L is again generated in the processor. If BREAK REQUEST is asserted at this time indicating that another data word is to be transferred, the break priorities will again be tested during TS4 and a new break address will be applied to the MA lines at TP4. Otherwise, those signals that disabled the processor during the last break cycle will be negated and the processor continues with the current instruction.

8.4.8 Three-Cycle Data Break

It is possible to use memory locations as WC and CA registers by using a more complex DMA control. Figure 8-7 is a simplified diagram illustrating the interaction between the processor and a three-cycle data break device. The initial set-up and exit phases include operations similar to those required for a single-cycle data break; however, the data transfer phase of a three-cycle break is divided into a WC cycle, a CA cycle, and a data transfer cycle.

During initial set-up, the running program uses instructions to load the memory locations designated as the device WC and CA registers, then executes IOT instructions that initialize the device and specify any necessary transfer parameters. Once the device control circuitry has been enabled, the processor is free to perform other tasks while the peripheral accesses storage locations and executes the data break transfers.

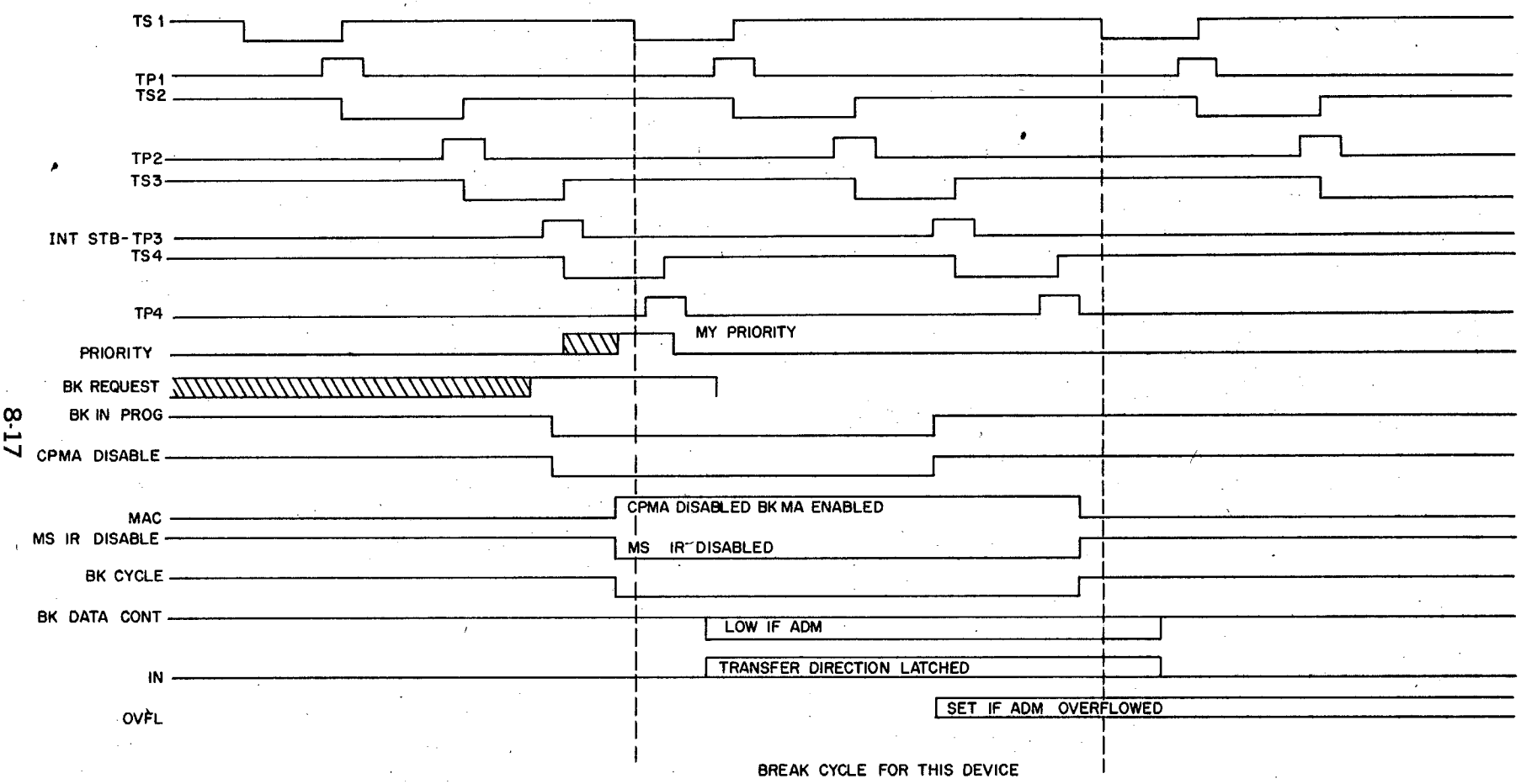


Figure 8-6 Data Break Control Timing Diagram

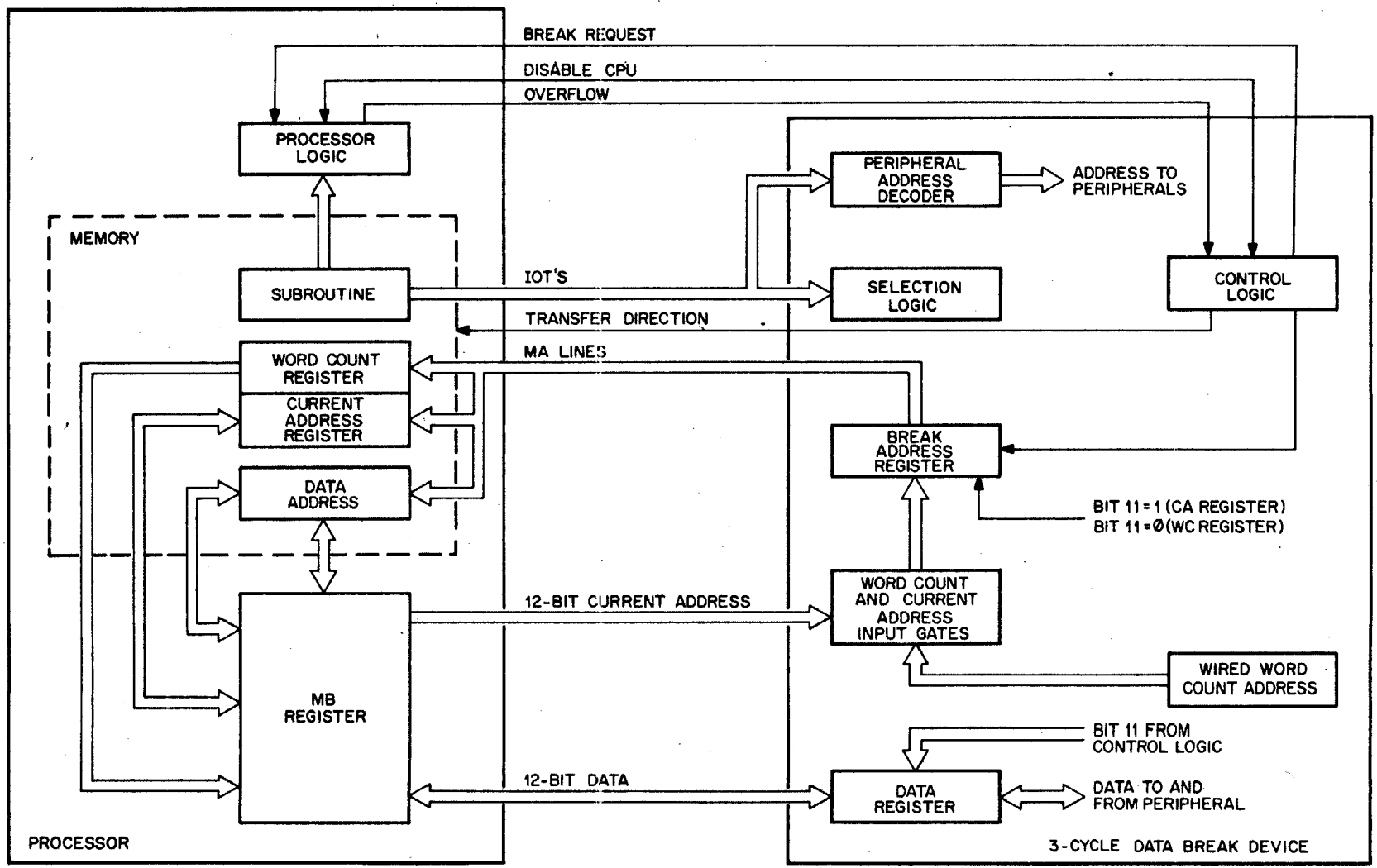


Figure 8-7 Three-Cycle Data Break Simplified Block Diagram

Each three-cycle data break begins with a WC cycle during which the device gates the address of its WC register onto the Omnibus. The address is fixed (hardwired), and is usually an even number (bit 11 = 0) address. During the word count cycle, the contents of the word count location is returned from memory and applied to one leg of the processor's adder register. The device gates a 1 into the other adder inputs via the data bus, thereby incrementing the word count. The resulting addition is tested for overflow while the incremented word count is restored to memory. If overflow occurs, the peripheral clears its enabling circuits and sets its device flag as soon as the current transfer has been completed. In any event, the device concludes each WC cycle by testing the data bus to determine whether any higher priority device has entered a break request.

If there is no higher priority request on the data bus, the device immediately begins its CA cycle. The CA memory address is usually one greater than the WC address. The CA memory location is incremented in the manner just described, and the incremented value is restored to memory and also transferred to the device break address register. Break priority is tested again at the end of the CA cycle.

During the data transfer cycle, the peripheral generates a signal to specify the direction of the transfer, gates the contents of its break address register onto the Omnibus, and either accepts or transmits one word of data. If WC overflow did not occur during the WC cycle, the device relinquishes control of the processor and begins to prepare for the next data transfer. When WC overflow does occur, the device flag is set and the running program executes IOT instructions to perform any operations that may be required to terminate the block I/O process.

CHAPTER 9

PDP-8/A PERIPHERALS AND OPTIONS

9.1 INTRODUCTION

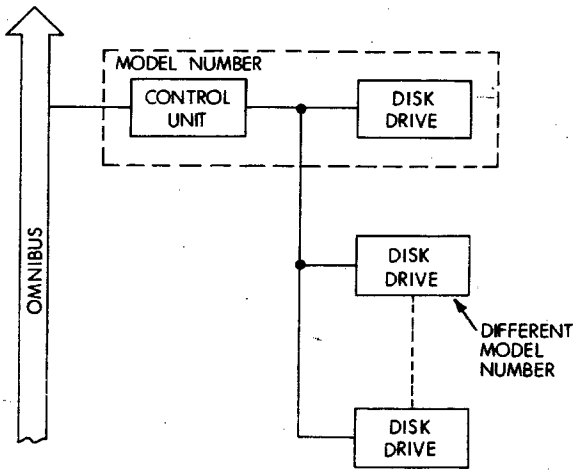
This chapter contains descriptions, specifications, programming, and operating information for the PDP-8 family of options and peripherals. For ease of reference, the peripherals have been arranged alphanumerically by model number, with the model number appearing on the top right corner of each page.

Since some peripherals have similar descriptions and specifications, related peripherals will be described within the same section.

All the peripherals mentioned in this chapter must eventually interface to the Omnibus. Some of the equipment, such as Line Printers, include a control unit as well as the printer itself. The control unit, sometimes referred to as a controller or interface unit, is the actual logic equipment between the Omnibus and the peripheral device. With terminals, the control unit and the terminal itself are separate products. In this case, any one of several different control units could be used, depending on the application. In other cases, such as disk drives, a single model number includes a control unit and the first disk drive of the system. Other disk drives, up to the limit of the controller, are specified by another model number.

9.2 LIST OF PERIPHERALS

A list of PDP-8 options and peripherals are provided in the following table.



Disk Storage System

PDP-8 PERIPHERALS AND OPTIONS

MODEL NUMBER	DESCRIPTION
AD8-E	Analog to Digital Converter
DB8-E	Interprocessor Buffer
DK8-EP	Real Time Programmable Clock
DKC8-AA	I/O Option Module
DP8-EA/DP8-EB	Synchronous MODEM Interface
DR8-EA	12 Channel Buffered Digital I/O
ICS8	Industrial Control System
KE8-E	Extended Arithmetic Element
KG8-EA	Redundancy Check Option
KL8-A	Asynchronous Serial Line Interface
KL8-JA	Asynchronous Data Interface
KL8-M	Automatic Answering Device
KM8-A	Extended Option Module
LA8	Line Printer
LA35	DECwriter II Printer
LA36	DECwriter II Printer Terminal
LE8/LP05	Line Printer
PC8-E	Reader Punch
PR8-E	Paper Tape Reader
RK8-J/RK05J	Cartridge Disk System
RX8/RX01	Floppy Disk System
TA8-E/TU60	DECassette Tape System
TD8-E/TU56	DECtape and Controller
TM8-MA/TS03	Magnetic Tape System
TU56	DECtape Drive
VC8-E/VR17	Point Plot Display System
VT50	Video Terminal
VT52	DECscope Video Terminal
VT55	Graphics Terminal
VT61	Video Terminal

Additional Options

Options not listed previously but available are described here. For more information about these options, contact your local DIGITAL Sales Office and ask for an Option Bulletin for that option.

The following options will operate on the PDP-8/A System in any memory configurations:

DC08H Automatic Calling Unit Controller controls up to 10 Bell System 801A or 801C Automatic Calling Units.

DK8-EC Real Time Clock is a crystal-controlled clock option that causes an interrupt every 50, 500, or 5000 times per second (jumper selectable).

The following options require 4K or more of read/write memory:

VT8-E Alphanumeric and Graphic Display Terminal consisting of a keyboard, video circuits, CRT, power supply, and control logic.

XY8-EB Incremental Plotter Control consisting of the XY8-E interface and the Calcomp Model 563 Incremental Plotter.

CR8-F Card Reader and Control reads standard EIA data cards at a rate of 200 cards per minute.

CM8-F Optical Mark Reader and Control accepts information from marked or punched cards, with timing marks, at a rate of 200 cards per minute.

RF08 256K Word Fixed Head Disk and RS08 Controller provides 262,144 words of mass storage for the PDP-8/A.

RT01 DEClink Data Entry Terminal and RT02 Alphanumeric Terminal feature Teletype and EIA serial line compatibility. DEClink is a self-contained data entry device which is remotely locatable.

LS8-F Line Printer features 132 character column width and 64 characters, with a print rate of 165 characters per second. Printing is done in a 7 $\times$ 9 dot matrix.

DF01-A Acoustic Coupler.

ANALOG TO DIGITAL CONVERTER, AD8-A

DESCRIPTION

The AD8-A is a 5 V full-scale range, 10-bit A/D converter providing 16 channels of input multiplexing with sample-and-hold for use on any PDP-8 Omnibus. The device code is selected by PC switches on the module allowing the use of more than one AD8-A in a system.

FEATURES

Device code selection

Self-contained analog power supply operating from +5 Vdc logic power

Double buffered data output for maximum throughput rate

Programmed unipolar/bipolar operation giving straight 10 bits right justified binary (unipolar) or sign extended 2's complement binary (bipolar)

Program enabled auto increment of the multiplexer register

Conversions may be initiated by program command or from an external source.

REGISTERS

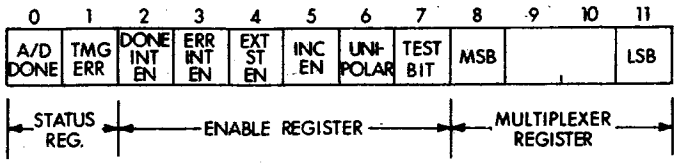
Status Register (AC bits 0 and 1)
A/D DONE is set (1) when an A/D conversion is completed. The buffer is updated 1 μs later. Timing Error is set (1) when a start conversion is attempted, while a conversion is in progress, or when the buffer is updated while a read buffer command (ADRD) is in progress.

Enable Register (AC bits 2 through 7)
Done Interrupt is set (1) from the AC to enable the INT RQST line. Error Interrupt EN is set (1) from the AC to enable the INT RQST line. External Start Enable is set (1) from the AC to enable the external A/D start conversion circuit to initiate conversions from the VC8-E, or from an external source. Increment Enable is set (1) from the AC to automatically increment the MUX Register to the next sequential channel at the end of each conversion. The MUX Register overflows to 00 from 17. Mode select is cleared (0) from the AC to select the bipolar mode or set (1) to select unipolar mode.

Multiplexer Register (AC bits 8 through 11)
The multiplexer register is loaded from the AC to select one of 16 multiplexer channels. It can also be read into the AC to determine the channel being monitored by the AD8-A.

NOTE

All AD8-A registers are cleared by a processor generated INITIALIZE.



AD8-A Registers

PROGRAMMING

Eight instructions are used to program the AD8-A. The device code (XY) is preset by the user using switches provided on the AD8-A.

MNEMONIC	OCTAL CODE	FUNCTION
ADCL	6XY0	Clear Status, Enable, and MUX registers.
ADLM	6XY1	Load MUX Register from the AC, then clear the AC.
ADST	6XY2	Clear the A/D DONE and Error flags (STATUS Register) and start a conversion on the current channel.
ADRB	6XY3	Transfer the contents of the A/D Buffer into the AC and clear the A/D DONE flag.
ADSK	6XY4	Skip the next instruction if the A/D DONE flag is set.
ADSE	6XY5	Skip the next instruction if the Timing Error flag is set.
ADLE	6XY6	Load the ENABLE Register from the AC, then clear the AC.
ADRS	6XY7	Transfer the STATUS, ENABLE, and MUX registers into the AC.

53 is the standard value for XY.

SPECIFICATIONS @ 25° C (77° F) unless otherwise specified

Inputs

Analog Input Impedence ($-5\ V \leqslant V_{in} \leqslant +5\ V$)
Unselected Channel: 1000 MΩ min.
Selected Channel: 10 MΩ min.

ANALOG INPUT BIAS CURRENT ($-5\ V \leqslant V_{in} \leqslant +5\ V$)
Unselected Channel: ±100 nA max
Selected Channel: −2 μA max

ANALOG INPUT VOLTAGE (FSR)
Unipolar: 0 V to +5 V
Bipolar: −2.5 V to +2.5 V

EXTERNAL START INPUT CURRENT

Low:	−3.2 mA max @ 0 V input
High:	+1.1 mA max @ +5 V input

EXTERNAL START LOGIC LEVELS

Low:	0 V to +0.7 V
High:	+2 V to +5 V

A/D Specifications

Resolution:	10 bits (1 part in 1024)

DIFFERENTIAL LINEARITY

Guaranteed:	No skipped states; 95% of states within ±1/2 LSB.
Typical:	99% of states within ±1/2 LSB. 85% of states within ±1/4 LSB.
Unipolar:	10 bits right justified.
Bipolar:	2's complement binary sign extended.

Sample and Hold Specifications

TRACKING

Small signal bandwidth:	700 kHz typical
Slew rate:	1 V/μs typical

APERTURE

Delay:	200 ns max
Jitter:	1 ns max

Multiplexer Specifications

Switching:	break-before-make
Channels:	16 non-expandable single-ended inputs
Crosstalk:	−80 db @ 1 kHz −20 db/decade roll-off

Data Coding

Unipolar

Input (V)	Octal Code
+5 − 1 LSB	0777**
+2.5	0000
0	7000**

Bipolar

Input (V)	Octal Code
+2.5 − 1 LSB	0777
0	0000
−2.5	7000**

** The three MSB's of the output data are tied together.

Performance

Accuracy:	0.1% of FSR (1 LSB)
Linearity:	0.05% of FSR (1/2 LSB)

TEMPERATURE COEFFICIENTS

Gain:	50 ppm/° C max
Linearity:	25 ppm/° C max
Noise:	1/4 LSB rms max
	1/15 LSB rms typical
Warmup Time:	5 minutes max

Power Requirements

+5 Vdc ± 5% @ 3.25 A max

OPERATING ENVIRONMENT

Temperature Range:	5° to 50° C system ambient
	5° to 70° C module ambient
Humidity:	10% to 90%

STORAGE ENVIRONMENT

Temperature Range:	−40° to +76° C (−40 to +169° F)
Humidity:	95% max (noncondensing)

INTERPROCESSOR BUFFER, DB8-E

DESCRIPTION

The DB8-E Interprocessor Buffer (see figure 9-4) plugs directly into the PDP-8 Omnibus and allows for the transfer of data between two PDP-8 processors one 12-bit word at a time. A transfer rate of 50,000 words per second is the practical limit using programmed interrupt transfer.

The DB8-E can also be used to transfer data to user-designed logic on single-ended data lines. Device codes on the module are jumper-selected between 50 and 57, allowing a maximum of eight interprocessor buffers to be used in one PDP-8.

OPERATION

To transfer data from PDP-8 No. 1 to PDP-8 No. 2, data is loaded into the AC of PDP-8 No. 1 and transferred to the output buffer of its DB8-E using the 65X4 IOT. In addition to loading the output buffer, IOT 65X4 also sets the FLAG flip-flop in the DB8-E of PDP-8 No. 2. When the program in PDP-8 No. 2 has sensed its FLAG flip-flop, data is gated into the AC of PDP-8 No. 2 using IOT 65X2. IOT 65X2 then sets the DONE flip-flop of the DB8-E of PDP-8 No. 1, indicating the transfer was completed, and clears the FLAG flip-flop of the DB8-E of PDP-8 No. 2. PDP-8 No. 1 then clears its DB8-E DONE flip-flop using IOT 65X7.

PROGRAMMING

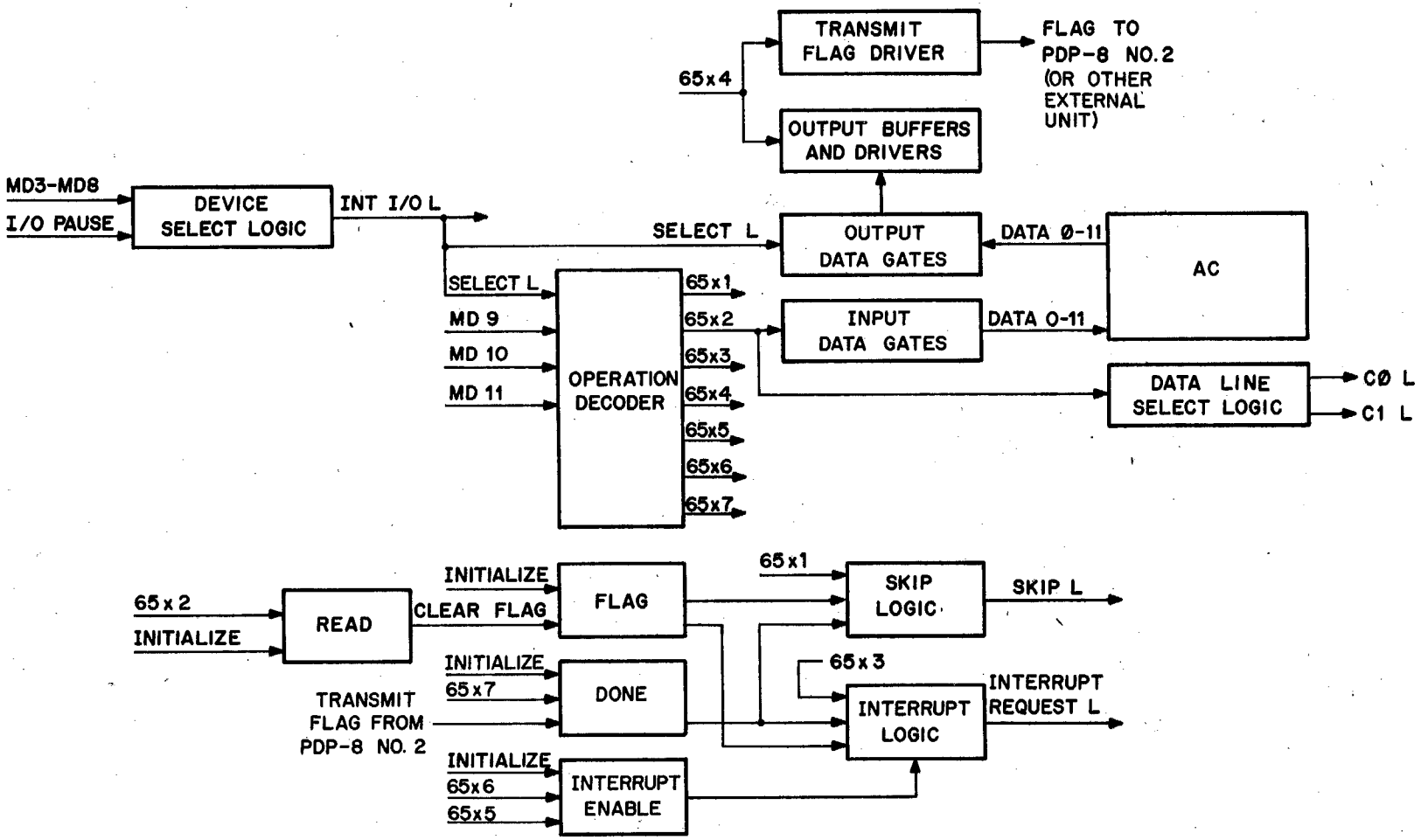
MNEMONIC	OCTAL CODE	FUNCTION
DBRF	65X1	Skip if the RECEIVE Flag equals one.
DBRD	65X2	Read the incoming data into the AC, clear the RECEIVE Flag, and set DONE flip-flop.
DBTF	65X3	Skip if the DONE Flag equals one.
DBTD	65X4	Transfer the contents of the AC register to the transmit buffer. Transmit data and set the Flag.
DBEI	65X5	Enable the interrupt request line.
DBDI	65X6	Disable the interrupt line.
DBCD	65X7	Clear the DONE Flag.

NOTE

Initialize disables interrupts from occurring.

SPECIFICATIONS

Control:	One quad module
Device Codes:	Jumper selectable device codes between 50 and 57.
Temperature:	41° to 122° F (5° to 50° C).
Interconnecting Cable Supplied:	DB8-EA — one 25 ft. interconnecting cable with H856 connector on each end of cable.
Drive Capabilities:	Up to 100 feet.
Speed:	12 bit words at 50 words/second. Data format is 12 bits parallel in and out.



DB8-E Interprocessor Buffer

I/O OPTION MODULE, DKC8-AA

The DKC8-AA I/O option board (M8316) contains four separate PDP-8/A options on one hex size module:

1. Serial line unit (SLU) for interfacing to 20 mA or EIA serial devices.
2. General purpose 12 bit parallel I/O control.
3. Real time crystal clock.
4. Programmers console control which interfaces the programmer's console to the Omnibus.

There are no variations at either the option or module level. Each of the options is described in the following paragraphs.

NOTE

The DKC8-AA module must be inserted in slot 2 or 3 of the Omnibus (slots are numbered from top of enclosure).

Operating Conditions

Operating environmental conditions must be no worse than the following:

Temperature:	5° to 50° C (41° to 122° F)
Humidity:	10 to 90% relative humidity (noncondensing)

Power Requirements

2.1 A @ +5.0 Vdc
150 mA @ +15.0 Vdc
150 mA @ −15.0 Vdc

Serial Line Unit (SLU)

The serial line unit (SLU) is contained on the DKC8-AA I/O option board. The SLU provides an interface for use between the PDP-8/A Omnibus and any asynchronous external device which has electrically compatible data leads and which operates with one of the serial data formats available with this interface.

Operation of the SLU is via the programmed I/O.

FEATURES

The SLU has the following features.

Drive Capability:	20 mA serial	(Drivers/receivers will function properly at 110 baud with up to 5000 feet of 18 gauge or larger twisted pair cable.)
	EIA serial	(Drivers/receivers will function properly with up to 50 feet of cable.)
Baud Rates:	The following baud rates are switch selectable on the M8316 module:	

SLU BAUD RATE SELECT CHART

S1-4	S1-3	S1-2	S1-1	BAUD RATE
ON	ON	ON	ON	50
ON	ON	ON	OFF	75
ON	ON	OFF	ON	110
ON	ON	OFF	OFF	134.5
ON	OFF	ON	ON	150
ON	OFF	ON	OFF	300
ON	OFF	OFF	ON	600
ON	OFF	OFF	OFF	1200
OFF	ON	ON	ON	1800
OFF	ON	ON	OFF	2000
OFF	ON	OFF	ON	2400
OFF	ON	OFF	OFF	3600
OFF	OFF	ON	ON	4800
OFF	OFF	ON	OFF	7200
OFF	OFF	OFF	ON	9600
*OFF	OFF	OFF	OFF	19.2K

* Serial line unit will **not** run at this baud rate. This setting is **not** to be used.

S1-7 ON = 1 stop bit in SLU character
OFF = 2 stop bits in SLU character

S1-8 ON = ASR/KSR 33 DR35 filter in (across SLU 20 mA rec'v leads. ON if baud rate is 110 or below.)
OFF = Filter out

Transmit and receive baud rates must be the same.

Stop Bits: One or two (switch selectable).

Parity: Parity is enabled by installing a jumper. Even or odd parity is selectable using a second jumper.

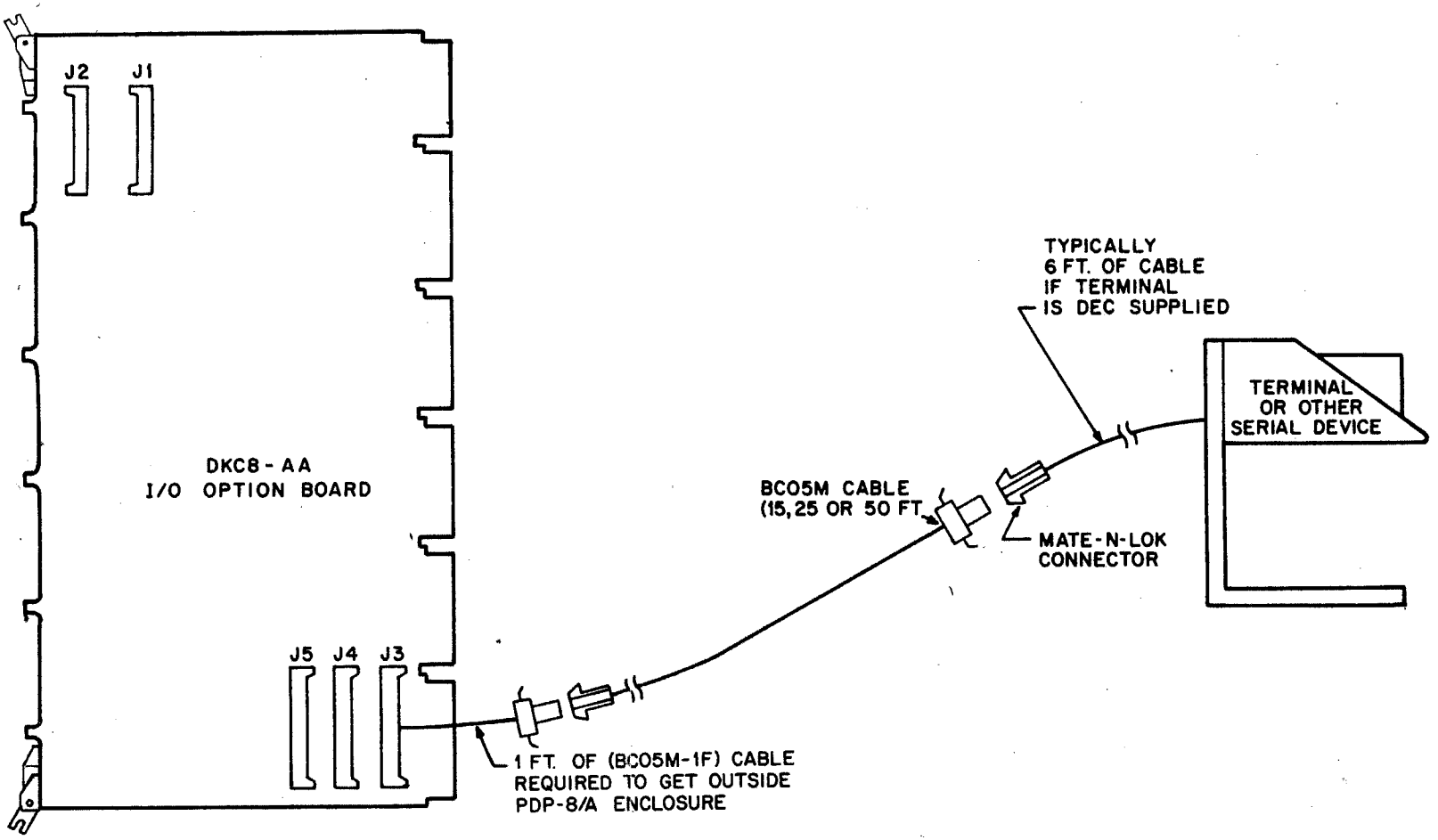
Device Codes: 03 (receive) and 04 (transmit); no other device codes are provided for.

Number of Bits per Character: The number of bits per character is jumper selectable between 5 and 8. Jumpers NB1 and NB2 are used to select the number of bits per character as follows:

Number of Bits	NB1	NB2
5	IN	IN
6	OUT	IN
7	IN	OUT
8	OUT	OUT

The normal configuration is 8 bits per character.

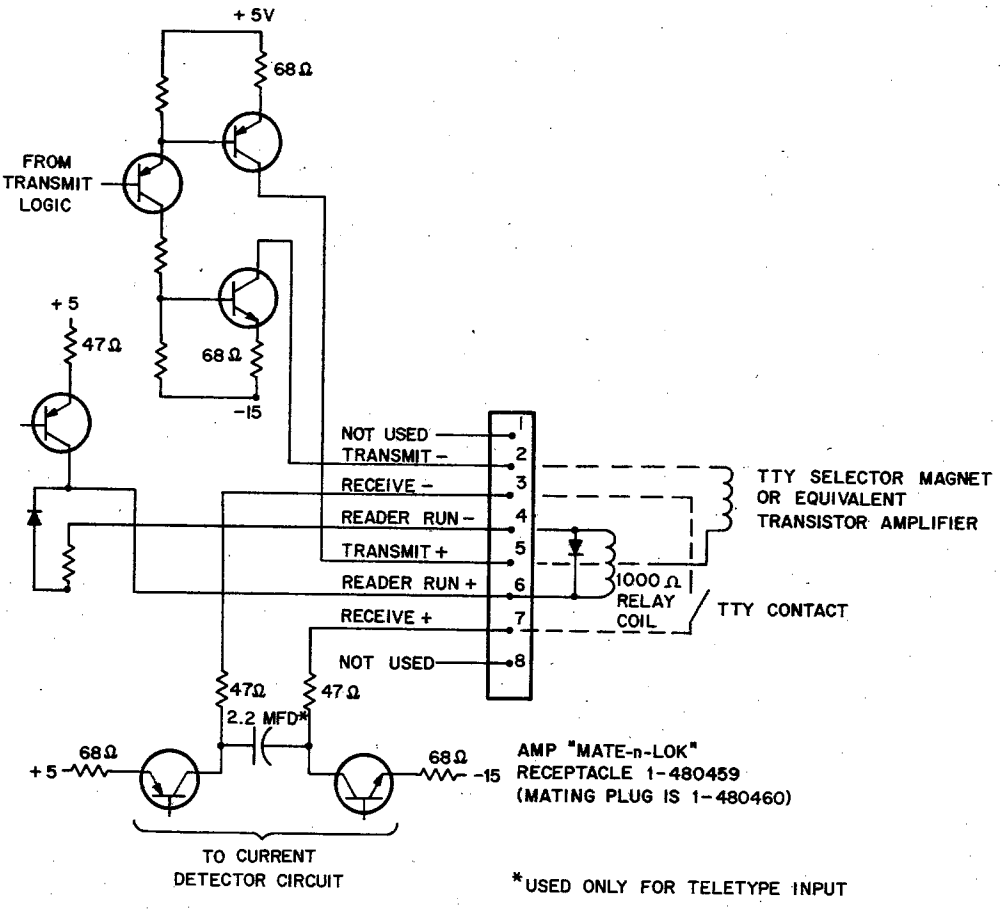
Cables: DIGITAL has a BC05M cable that connects to J3 on the M8316 module in lengths of 15, 25, or 50 feet.



Serial Line Unit Connected to a Serial Device

DIGITAL will build a customized cable for users who require more than 50 feet of cable.

The end of the cable that connects to J3 on the M8316 modules is a 6504-15 male Berg connector and the other end is a Mate-N-Lok female connector.



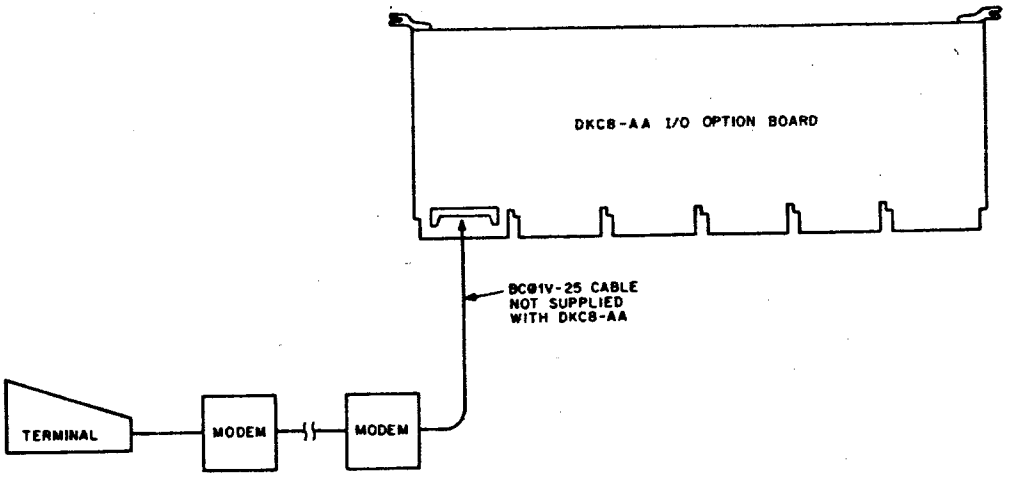
BC05M Cable Connections

MODEMS

The SLU will accommodate Bell 103A/E/F/G/H, 202/D, and 113B or equivalent type modems. A BC01V-25 cable must be purchased separately to make connection to the modem. Only the transmit and receive data leads are activated by this cable. The modem system must be a full-duplex dedicated line type modem. Furthermore, the READER RUN feature, normally present on local terminals, cannot be used.

FUNCTIONAL DESCRIPTION

The SLU uses a universal asynchronous receiver/transmitter (UART) that connects through drivers and a cable to the external device. The UART performs serial to parallel (receive) and parallel to serial (trans-



Modem Interface to SLU on the DKC8-AA

mit) conversion of data that is received from or sent to the serial device. Timing for the UART is derived from a 5.0688 MHz crystal oscillator and a switch selectable baud rate generator.

The SLU receives instructions and data from the processor via the Omnibus. The instructions are decoded by two instruction decoders within the SLU when I/O PAUSE L is received. One instruction decoder is enabled when device code 03 is received to decode receive instructions and the other instruction decoder is enabled when device code 04 is received to decode transmit instructions. The device codes 03 and 04 are fixed for this unit and no other device can use these device codes when the SLU is used. A list of IOT instructions is included under programming in the next section.

The receive flag is set when the UART has assembled a complete character and transferred it to its receive buffer. When the receive flag sets, INT RQST L is asserted if interrupt is enabled. SKIP L is asserted if the program then tests the receive flag (KSF IOT). The program then transfers the character to the AC via IOT instructions. The receive flag is cleared and the receive buffer waits for another character from the input shift register.

During a transmit operation the transmit flag sets each time a parallel character from the AC has been transferred to the output shift register. When the transmit flag sets, the INT RQST L line is asserted. The flag may also be checked by a skip instruction. The program may then transfer another character from the AC, clearing the transmit flag and causing the new character to be transferred to the output shift register and shifted out to the device as serial data.

PROGRAMMING

The IOT instructions for the SLU are as follows:

Receive Instructions (Device Code 03)

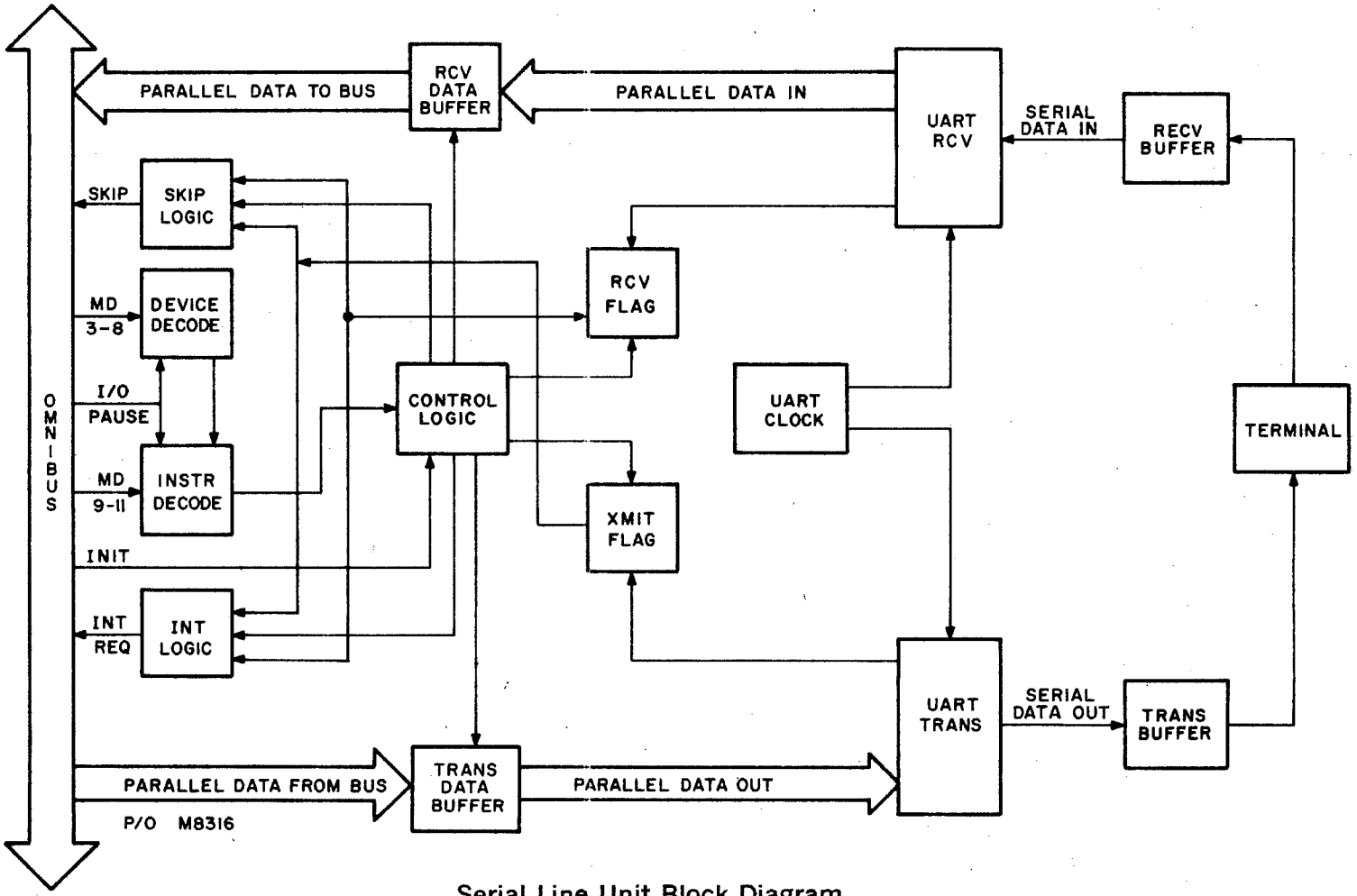
MNEMONIC	OCTAL CODE	FUNCTION
KCF	6030	Clear receive flag, do not set reader run, do not request a new character from the reader if it is in operation, do not clear the AC. READER RUN is automatically cleared by the new incoming character.
KSF	6031	Skip if the receive flag is set.
KCC	6032	Clear receive flag and AC, set reader run.
KRS	6034	Inclusive OR receive buffer into the AC.
KIE	6035	Load AC11 into interrupt enable for both receive and transmit. AC11 = 1. Enable interrupt AC11 = 0. Disable interrupt
KRB	6036	Combined KCC and KRS. Clear flag, load AC with contents of receive buffer, and set reader run.

Transmit Instructions (Device 04)

MNEMONIC	OCTAL CODE	FUNCTION
TFL	6040	Set transmit flag.
TSF	6041	Skip if the transmit flag is set.
TCF	6042	Clear transmit flag.
TPC	6044	Load AC4-11 into transmit buffer and transmit.
SPI	6045	Skip on transmit or receive flag if interrupt enable is set to a 1.
TLS	6046	Combined TCF and TPC commands.

ADDITIONAL SERIAL DEVICE INTERFACES

For those users who require an interface for more than one serial device, DIGITAL has designed and manufactures the KL8-JA Asynchronous Data Interface and the KL8A serial line unit. The KL8-JA is compatible with and operates on the PDP-8/A Omnibus. The KL8-JA electrical specifications and operation are similar to the SLU on the I/O option module and use the same cables for connection to serial devices and modems (see KL8-JA description). One additional feature provided by the KL8-JA is the ability to select different device codes using switches located on the M8655 module. This allows the user to assign device codes that are different from the SLU allowing the operation of more than one serial device on the PDP-8/A Omnibus.



Serial Line Unit Block Diagram

DKC8

The KL8A is a four-channel Serial Line Unit with three channels having partial modem control capabilities and one having full modem control capabilities.

General Purpose Parallel I/O

This option allows the PDP-8/A to transmit or receive one 12-bit word at a time between user designed logic on single ended data lines or two PDP-8/A processors to transfer data to each other, provided each processor has a DKC8-AA I/O option board and the proper cables.

Maximum practical data transfer rate is approximately 50,000 words/second when using programmed interrupt transfers.

FEATURES

Input/Output: 12 bits of parallel data input and output.

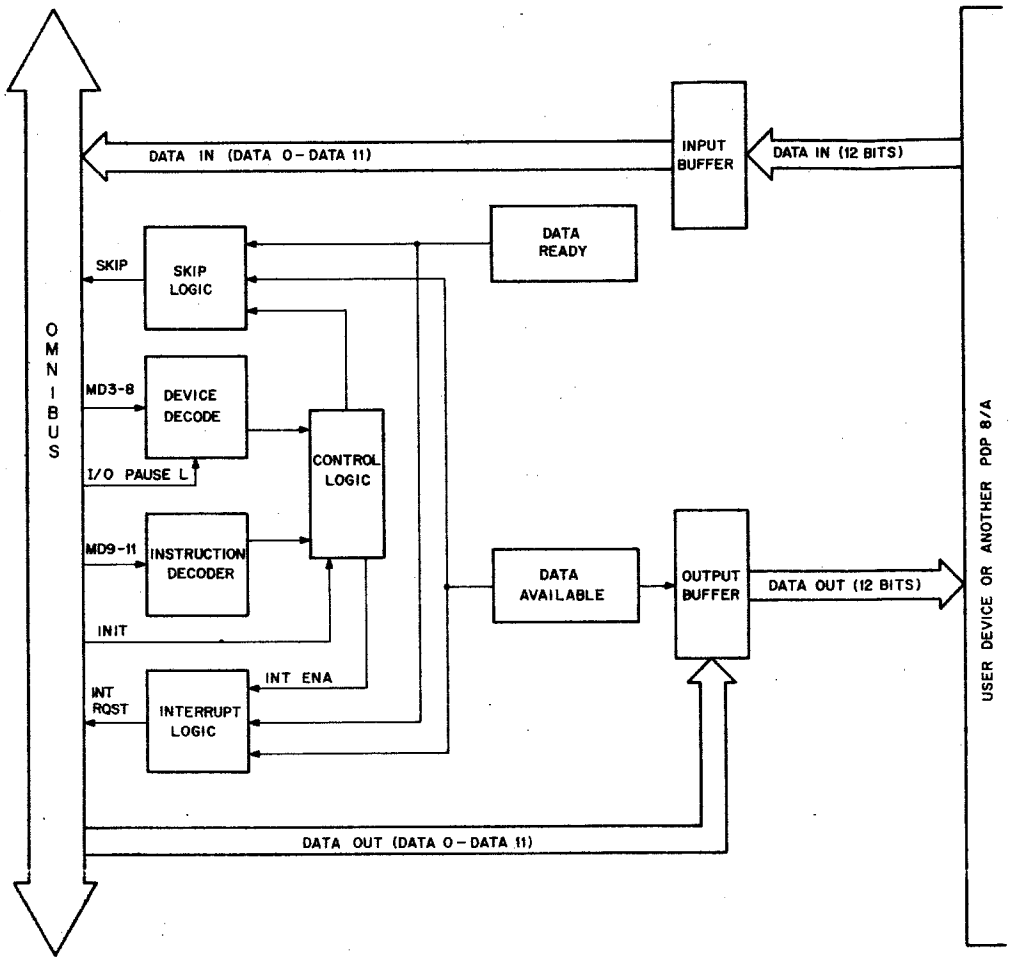
Drive Capability: Each output drives up to 25 TTL unit loads. Data In presents 4 TTL unit loads to the driver circuit.

Signal Levels: Logic High is 4.0 V to 2.6 V
Logic Low is 0.0 V to 0.6 V
All signals are TTL compatible.

Cables: All cables must be ordered separately. The BC08R cable should be used; the standard length is 10 feet, but other lengths up to 25 feet are available on special order. Two cables are needed if both transmit and receive functions are used.

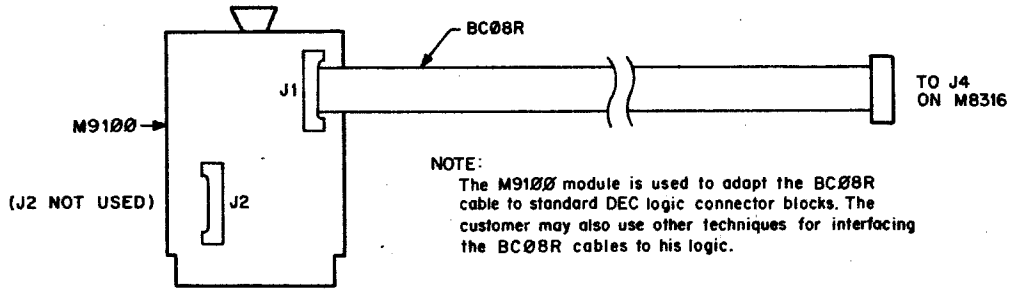
To transmit data between two PDP-8/A computers, use two BC08R cables. Each cable connects J5 of one DKC8-AA to J4 of the other. The cable must be turned over (connected backwards: pin A is plugged into the pin VV end of the connectors) at one end of each cable. (See accompanying Tables.)

Switch: SI-9 ON—TS1 clears DATA AVAIL flip-flop in parallel I/O section.
SI-9 OFF—DATA AVAIL not cleared by TS1



General Purpose Parallel I/O Block Diagram

J4 Input Signal Pin Assignments

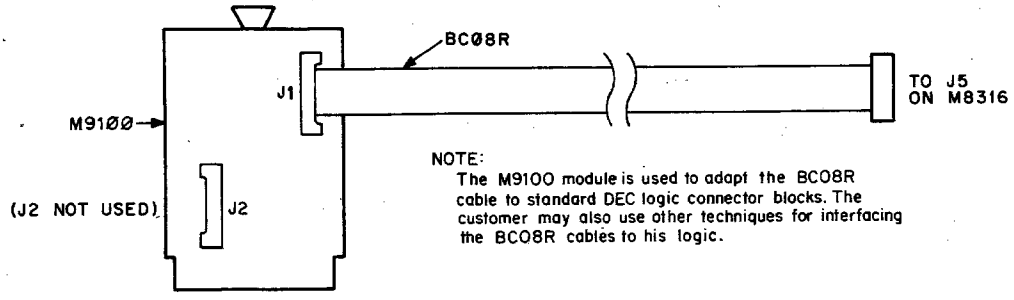


NOTE:
The M91ØØ module is used to adapt the BCØ8R cable to standard DEC logic connector blocks. The customer may also use other techniques for interfacing the BCØ8R cables to his logic.

FINGERS	J1	DKC8-AA J4 PIN NO.	SIGNAL NAME	COMMENTS
D1	SS	D	STROBE L	450 ns control pulse, drives 10 unit loads.*
F1	PP	F	Not used	
J1	MM	J	Not used	
L1	KK	L	DATA IN 0 L	Most significant bit.
N1	HH	N	DATA IN 1 L	Input data low is true.**
R1	EE	R	DATA IN 2 L	
S1	CC	T	DATA IN 3 L	
V1	AA	V	Not used	
U1	Y	X	SET DATA READY L	Low when input data is valid.
U2	W	Z	DATA ACCEPTED OUT L	Low when input data is accepted. Drives 25 unit loads.*
C1	U	BB	Not used	
D2	S	DD	DATA IN 4 L	
F2	P	FF	DATA IN 5 L	
J2	M	JJ	DATA IN 6 L	
L2	K	LL	DATA IN 7 L	Input data, low is true.**
N2	H	NN	DATA IN 8 L	
R2	E	RR	DATA IN 9 L	
T2	C	TT	DATA IN 10 L	
V2	A	VV	DATA IN 11 L	Least significant bit.

All unspecified pins are ground.
* 1 unit load = 1.6 mA @ a logic low and 0.04 mA @ a logic high.
** Presents 4 unit loads to the drive circuit.

J5 Output Signal Pin Assignments



FINGERS	J1	DKC8-AA J5 PIN NO.	SIGNAL NAME	COMMENTS
D1	SS	D	Not used	
F1	PP	F	Not used	
J1	MM	J	Not used	
L1	KK	L	DATA OUT 0 L	Most significant bit.
N1	HH	N	DATA OUT 1 L	
R1	EE	R	DATA OUT 2 L	Output data, low is true.**
S1	CC	T	DATA OUT 3 L	
V1	AA	V	Not used	
U1	Y	X	DATA AVAILABLE L	Low when output data is valid.
U2	W	Z	DATA ACCEPTED IN L	Low when output data is accepted. Presents 4 unit loads to the driver circuit.*
C1	U	BB	Not used	
D2	S	DD	DATA OUT 4 L	
F2	P	FF	DATA OUT 5 L	
J2	M	JJ	DATA OUT 6 L	
L2	K	LL	DATA OUT 7 L	Output data, low when true.**
N2	H	NN	DATA OUT 8 L	
R2	E	RR	DATA OUT 9 L	
T2	C	TT	DATA OUT 10 L	
V2	A	VV	DATA OUT 11 L	Least significant bit.

Pins A, B, C, E, H, K, M, P, S, U, W, Y, AA, CC, EE, HH, KK, MM, PP, and SS are grounded.

* 1 unit load.

** Each output can drive 25 unit loads.

IOT Instructions

MNEMONIC	OCTAL CODE	FUNCTION
DBST	6570	Skip on Data Accepted, clear Data Accepted and Data Available, if Data Accepted flag is set.

MNEMONIC	OCTAL CODE	FUNCTION
DBSK	6571	Skip on Data Ready flag.
DBRD	6572	Read data into AC0—AC11.
DBCF	6573	Clear Data Ready flag, issue Data Accepted out pulse.
DBTD	6574	Load AC0—AC11 into buffer and transmit data out.
DBSE	6575	Set interrupt enable to a 1.
DBCE	6576	Reset interrupt enable to a 0.
DBSS	6577	Issue a strobe pulse.

FUNCTIONAL DESCRIPTION

Transmit Operation

To transmit a 12-bit data word, perform the following:

1. Load the output buffer with IOT 6574. Data will be transferred from the data lines on the bus into the buffer at TP3 time.
2. At the trailing edge of TP3, Data Available becomes true (low) on the output cable. If desired, there is a switch on the M8316 that will cause Data Available to be negated (go high) on the leading edge of the next TS1 pulse. This yields a pulse of about 450 ns in duration on the Data Available signal line. The trailing edge of the pulse, on Data Available, could be used to strobe the output data of the M8316 into the user's register. If TS1 is not used to negate Data Available, IOT 6570 (DBST) should be used to negate Data Available.
3. The receiving device should then ground Data Accepted to signal the CPU that the transmitted data has been received.
4. Assuming interrupt enable is true, the Data Accepted flip-flop will assert INT RQST L on the bus.
5. The CPU then issues the 6570 IOT to test the Data Accepted flip-flop and to clear both Data Available and Data Accepted flip-flops. At TP3 of the 6570 IOT, Data Available will go high on the output cable. This signals the end of the transmit sequence.

Receive Operation

The receive sequence is as follows:

1. The external device grounds the Set Data Ready line on the input cable which raises the Data Ready flag.
2. Assuming Interrupt Enable is true, INT RQST L will be asserted on the bus.
3. The CPU then issues the 6571 IOT to test the Data Ready flip-flop; then IOT 6572 should be issued to read the input data into AC0—11.

4. The CPU should then issue IOT 6573 to clear Data Ready. This also sends a pulse out on the Data Accepted out line on the input cable. This signal should be used by the external device to negate the Set Data Ready signal.

Strobe
IOT 6577 (DBTS) creates a pulse on the "strobe" line that goes from the high to low state at TP3 of IOT 6577 and returns to the high state at the next TS1. This pulse may be used to start an event external to the CPU or it may signal the end of an event.

Additional Parallel I/O Interface
The DB8-E interprocessor buffer is available for those customers who need more than one parallel I/O interface (see DB8-E description).

The DB8-E interprocessor buffer is used to transfer data between two PDP-8/As or PDP-8/Es, a PDP-8/A and PDP-8/E, or it may be used single-ended as a data path between a PDP-8/A and user designed logic.

NOTE

The DB8-E and DKC8-AA parallel interface cables are not compatible with each other.

Device codes are jumper selectable between 50 and 57 allowing up to 8 DB8-Es to be connected to one PDP-8/A. The PDP-8/As may be interconnected at distances up to 100 feet apart by means of two BC08-R type cables.

All logic is mounted on a single quad size board which plugs directly into the Omnibus. Two 40 pin connectors type H854 mounted on the module receive cable type BC08-R or BC08-J. On the terminal end of the cable, connector type H856 is provided.

LA180 Printer Capability
J5 of the parallel I/O can be used to interface with DIGITAL's LA180. A BC80A cable is necessary to connect the DKC8-AA (M8316) to the LA180.

NOTE

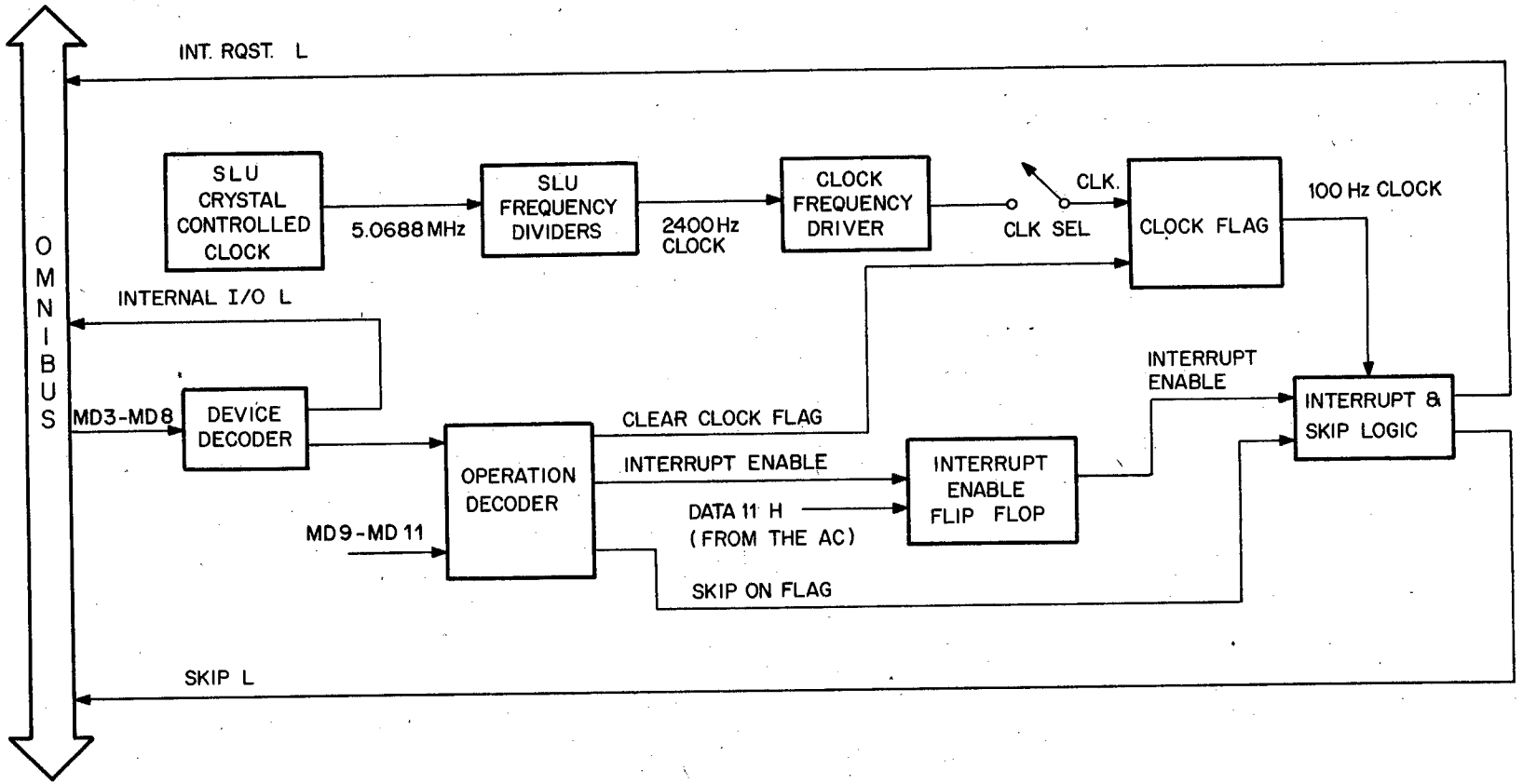
Data must be presented in its 1's complemented form to the LA180 if interfacing with M8316. Also the IOTs differ from those used with the usual LA180 Interface (M8365).

Real Time Crystal Clock
The real time crystal clock on the DKC8-AA module interrupts the processor every 10 ms if interrupt enable is set (100 Hz $\pm$ 0.01%).

FEATURES
A skip instruction, CLSK, causes the program to skip an instruction if the clock flap is set.

Switches:
S1-5 ON —enable real time clock
OFF—disable real time clock

S1-6 ON—Test switch (normally on; for production use only).



Real Time Crystal Clock Block Diagram

Programming

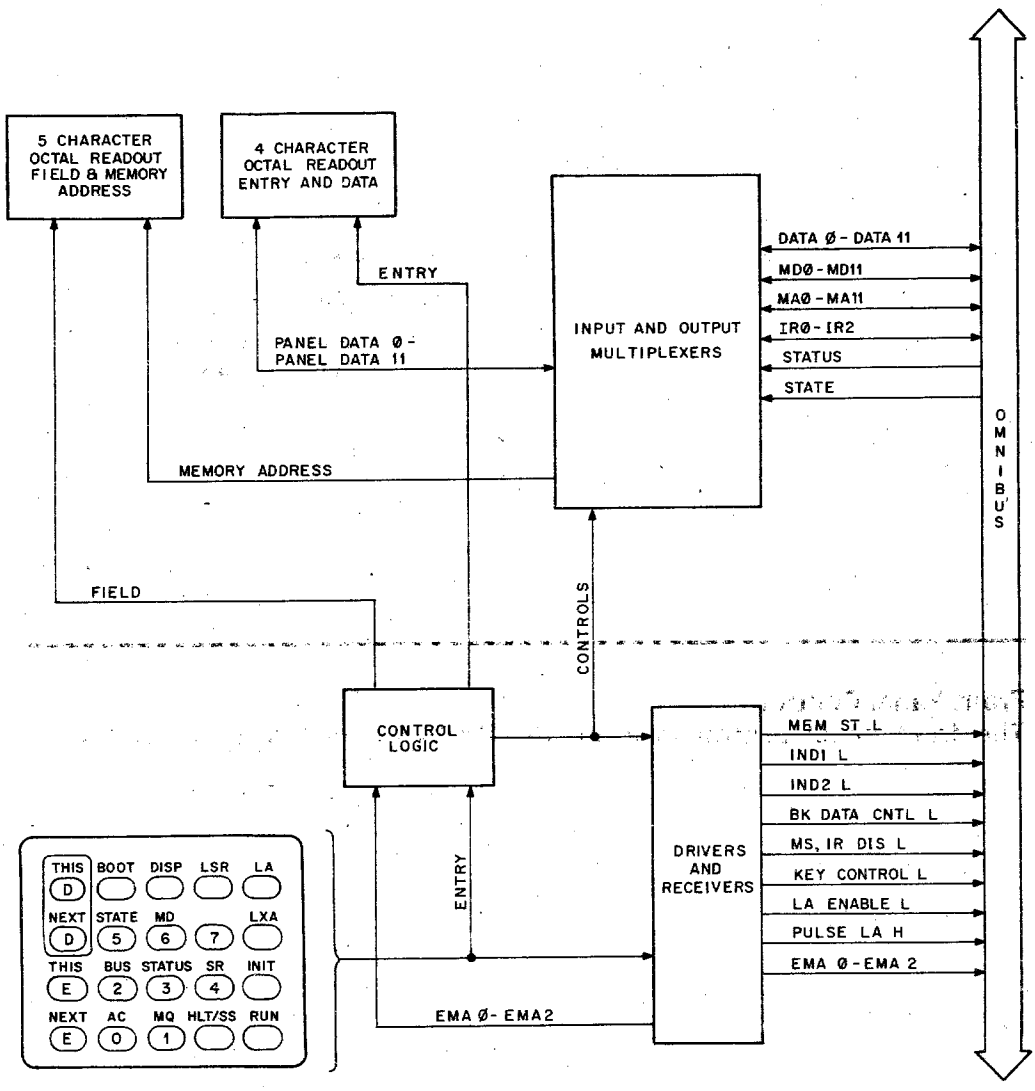
The instructions used to program the real time crystal clock are as follows:

MNEMONIC	OCTAL CODE	FUNCTION
CLLE	6135	Load the interrupt enable from AC11 AC11 = 1, set interrupt enable AC11 = 0, clear interrupt enable Interrupt enable is turned off when power is turned on and when the system is initialized by INIT on the programmer's console, or if the CAF instruction is executed.
CLCL	6136	Clear clock flag.
CLSK	6137	Skip on clock flag.

Front Panel Control

The front panel control logic on the DKC8-AA module provides the interface between the programmer's console (KC8-AA, AB) and the Omnibus. The front panel is connected to the DKC8-AA by two BC08S cables. Standard length is 1 foot (30.5 cm) but cables up to 15 feet (457 cm) are allowed when the panel is operated remotely.

The DKC8-AA contains the necessary control logic, multiplexers, drivers, and receivers to load extended memory and memory address registers, deposit instructions and data, examine memory locations, and manual control computer operation. The controls on the operator's panel and the programmer's console are explained in Chapter 5. The DKC8-AA and the programmer's console are not required to operate the PDP-8/A. Normal operation only requires the operator's panel.



Programmer's Console and Interface Block Diagram

REAL TIME PROGRAMMABLE CLOCK, DK8-EP

DESCRIPTION

The DK8-EP provides a programmable time base that allows the user to control and/or record the occurrence of events both internal and external to the PDP-8/E. The clock can be used to count the number of events in a given amount of time, to measure the amount of time between two given events, or to initiate repetitive operations at specified intervals of time.

The control register that performs the above described functions is called the Clock Enable Register. This register is loaded under program control (see accompanying table). Different bits are used to control different functional sections of the DK8-EP. For example: bit 7 of the register enables internally-generated clock pulses to be applied to the Clock Counter Register; bit 9, by enabling one of the Schmitt trigger circuits, allows an external source to control some aspects of the clock operation. The Clock Enable Register (see accompanying table) can be set or cleared under program control and its contents can be transferred to the CPU AC Register at any time by an IOT instruction.

The DK8-EP Real-Time Programmable Clock consists of two quad modules (M860 and M518) that plug into the Omnibus and are interconnected by an H851 Edge Connector. The M860 module, Real-Time Clock Control, contains a 12-bit binary counter, a 12-bit buffer register, and logic. The logic controls the counter/register operation and operation of the M518 module. The M518 includes a 12-bit storage register, logic that derives five different clock frequencies from a crystal-controlled oscillator, and three Schmitt trigger circuits that enable the user to control certain clock operations from external sources.

The Clock Counter Register counts clock pulses in a way that is predetermined by the state of Clock Enable Register bits 1 and 2. For example, the Clock Counter Register can count from 0 to 4095 repetitively, generating a signal (OVERFLOW L) each time it overflows from 4095 to 0. In other circumstances, the programmer might wish the OVERFLOW L signal to be generated every 2000 clock pulses. The Clock Counter Register can be preset, to a count of 2096 in this example, in order to produce the desired result. The contents of the Clock Counter Register can be transferred to the AC Register at any time by a program instruction; however, to accomplish this transfer, the logic makes use of a 12-bit Clock Buffer Register.

The Clock Buffer Register is essential to the DK8-EP operation. Data is transferred between the AC Register and the Clock Counter Register via the Clock Buffer Register. To preset the Clock Counter Register, as in the example given, the program causes the Clock Buffer Register to be loaded from the AC Register with the preset count. Bits 1 and 2 of the Clock Enable Register can then be set so that the preset count, 2096, is loaded into the Clock Counter Register each time the OVERFLOW L

signal is generated. Thus, the Clock Counter Register counts repetitively from 2096 to 4096. The Clock Buffer Register can be controlled by the program, and to a certain extent, by an external source. For example, Clock Enable Register bits 9-11 allow an external source to cause the Clock Buffer Register to be loaded; however, transfers between the AC and Clock Buffer Registers are limited to program control.

Clock Enable Register

REGISTER BIT	ENABLE SIGNAL NAME	FUNCTION
0	CLOCK ENABLE 0	Enables a status check of the OVERFLOW flip-flop (CLSA), an instruction Skip on an overflow condition (CLSK), and a possible Interrupt request on an overflow condition.
1-2	MODE ENABLE 1 MODE ENABLE 2	Determine the Clock Counter Register mode of counting. The four possible modes are: 00 Register counts at the selected rate with overflow occurring every 4096 counts. 01 Register counts at the selected rate. At each overflow a preset count is loaded into the register from the Clock Buffer Register. 10 Register counts at the selected rate. An external event can sample the register at any time, causing the sample count to be transferred to the Clock Buffer Register. The Clock Counter Register continues counting. 11 Register counts at the selected rate. An external event can sample the register at any time. The sample count is transferred to the Clock Buffer Register and the Clock Counter Register is cleared before it resumes counting.
3-5	RATE ENABLE 3 RATE ENABLE 4 RATE ENABLE 5	Select the frequency of the internally-generated clock pulses.
6	CLOCK ENABLE 6	Enables each Clock Counter Register overflow to generate the EXT PULSE L pulse that can be used by other Omnibus-connected devices (A/D START).

Clock Enable Register

REGISTER BIT	ENABLE SIGNAL NAME	FUNCTION
7	COUNT ENABLE 7	Inhibits clock pulses from being applied to the Clock Counter Register. (This bit can be cleared by firing an enabled Schmitt trigger.)
8	CLOCK ENABLE 8	Connects the Clock Interrupt logic to the computer interrupt system, enabling the Clock Interrupt conditions to assert the Omnibus INT RQST L signal.
9-11	EVENT ENABLE 9 EVENT ENABLE 10 EVENT ENABLE 11	Enable Schmitt trigger firings to turn on the clock, to cause a program interrupt, and to sample the Clock Counter Register (as set by bits 1, 2, 7, and 8).

Frequencies Selected by Rate Enable Bits 3-5

CONTENTS OF BITS 3-5	SELECTED MULTIPLEXER OUTPUT
000	No output
001	External frequency
010	100 Hz
011	1 kHz
100	10 kHz
101	100 kHz
110	1 MHz
111	No output

SPECIFICATIONS

Control: 20 MHz crystal controlled

Schmitt Triggers: Three threshold detectors that accept pulse or varying analog inputs (±5 V variations)

Input: +50 V maximum differential input, 50 kΩ input impedance, common mode rejection 35 db

Input Pulse Width: Minimum input pulse width 2 μs

Schmitt Trigger Propagation Time: 60 ns (input to output)

Time Base: Programmable time base rate set in Clock Enable Register, 1 MHz to 100 Hz (selectable)

Slope: ± switch selectable

Data Format: 12 bits parallel

INSTRUCTION SET

DK8-EP Instructions

MNEMONIC	OCTAL CODE	FUNCTION
CLZE	6130	Clear clock Enable Register per AC Register. Each bit in the clock Enable Register is cleared if the corresponding bit in the AC Register is set. The AC Register is unchanged.
CLSK	6131	Skip on a CLOCK flag. The next program instruction is skipped if either of the following skip conditions exists: a. An enabled Schmitt trigger has fired. b. The Clock Counter Register has overflowed.
CLOE	6132	Set Clock Enable Register per AC Register. Each bit in the Clock Enable Register is set if the corresponding bit in the AC Register is set. The AC Register is unchanged.
CLAB	6133	AC Register to Clock Counter Register. The contents of the AC Register are transferred to the clock and loaded into both the Clock Buffer and the Clock Counter Registers. The AC Register is unchanged.
CLEN	6134	Clock Enable Register to AC Register. The contents of the Clock Enable Register are transferred to the computer and into the AC Register. The Clock Enable Register is unchanged.
CLSA	6135	Status to AC Register. The state of the OVERFLOW flip-flop and of the three Schmitt input circuits is transferred to the computer and into the AC Register. Only the following AC bits are affected: AC Bit — Status Condition 0 — Enabled OVERFLOW flip-flop 9 — Enabled Schmitt input 3 10 — Enabled Schmitt input 2 11 — Enabled Schmitt input 1

CLBA	6136	Clock Buffer Register to AC Register. The contents of the Clock Buffer Register are transferred to the computer and into the AC Register. The Clock Buffer Register is unchanged.
CLCA	6137	Clock Counter Register to AC Register. The contents of the Clock Counter Register are transferred, via the Clock Buffer Register, to the computer and into the AC Register. The Clock Counter Register is unchanged.

SYNCHRONOUS MODEM INTERFACE, DP8-EA/DP8-EB

DESCRIPTION

The DP8-E is a synchronous modem interface that provides a high speed data break facility for modem control, parallel to serial and serial to parallel data conversion. The DP8 modem interface is contained on two quad modules which plug directly into the PDP-8/A Omnibus. Also included with the modem interface is a 25 foot cable terminated by a modem connector.

The DP8-E modem interface is designed to accommodate the Bell 201, 301, and 303 series modems or equivalent in either a full or half duplex mode of operation.

Data Transfers

Each character transfer requires three single cycle data breaks for both transmit and receive. An additional cycle is required for each special character to be tested (receive circuits only). Transfers to and from memory are accomplished in any memory field. The word count, current address, and characters for test (character recognition) are located in specified locations within field zero.

Control Transfers

Control transfers are maintained via the data bus. The types of control available are: idle, terminal ready, enable, transmit request, and transfer field.

Clocks

The clocks are normally provided for by the modem. The exception is anticipated by providing split lugs for insertion of a local clock at the M866 level converter module.

FEATURES

Jumper selectable device codes

Programmable character detection

Jumper selectable access address

Jumper selectable character length

Jumper selectable break priority

Jumper selectable sync code detection

SPECIFICATIONS

Device Codes

The M839 is programmable for one of four sets of IOT codes.

All IOTs are fully decoded and two device codes are required for each DP8-E. DP8-E IOTs are paired as follows:

640X/641X or 642X/643X or
644X/645X or 646X/647X

Cycle Time
Single cycle data break—1.5 microseconds.

Break Priority
The DP8-E databreak priority is jumper selectable. One of seven priorities (1 through 7).

Character Recognition
The hardware will detect four program selected characters to generate an interrupt when one of these characters is detected. A flag bit, stored with the character, determines if the hardware will flag the program or strip the character upon detection.

Synchronizing Character
Transmit: Non-hardware function—must be part of data for transmission.

Receive: The receive synchronizing character (SYNC) is jumper selected. Two or more consecutive SYNC characters must be received before the hardware will be activated.

Carrier Detect
Jumper selection of detect carrier (AGC ON and/or OFF transitions).

Bit Assignment and Description Status
The AC assignments are as follows:

A "one" in the bit location indicates assertion of the function.

Status 1 (SRS1)

AC00	R-RQST	Indicates a received character is ready for transfer to core.
AC01	T-RQST	Indicates a transmit request for data.
AC02	SYNC 2	The hardware synchronized on two incoming SYNC characters.
AC03	SYNC 1	The hardware synchronized on the first SYNC character. This bit will be maintained if two consecutive SYNC characters are detected.
AC04		Receive Field EMA0
AC05		Receive Field EMA1
AC06		Receive Field EMA2
AC07	MODEM READY	Indicates that either interlock or data set ready is ON.

Status 2 (SRS2)

AC00	Carrier/AGC	Indicates that either the carrier or the AGC is ON.

AC02	Terminal Ready
AC03	Clear to Send
AC04	Transmit Field EMA0
AC05	Transmit Field EMA1
AC06	Transmit Field EMA2
AC07	Transmit Data

Access Address

The access address is assigned (by jumpers) in even groups of 16 addresses. The hardware utilizes a four bit counter to select eight of the sixteen addresses for word count, current address and character recognition.

The following list, in binary, is the four low order bits, as they apply to the access addresses namely 7600, 7620, 7640, 7660, 7700, and 7720.

0000	Test character
0001	Test character
0010	Test character
0011	Test character
0100	Receive word count (2's complement)
0101	Receive current address
0111	Transmit word count (2's complement)
1000	Transmit current address
0110	*
1001	*
1010	*
1011	*
1100	Not used
1101	Not used
1110	*
1111	*

* Access address counter increments to these locations prior to character transfer with the PDP-8/A. When the counter is set at 0110, a receive character has been transferred to a location specified by the receive current address. When the counter is set at 1001, a character for transmit has been transferred to the DP8-E from the location specified by the transmit current address.

PROGRAMMING

MNEMONIC	OCTAL CODE	FUNCTION
SRTA	6407/6427 6447/6467	Transfers the content of the transfer address register into the AC. In use, the transfer address register latches the cur-

MNEMONIC	OCTAL CODE	FUNCTION
		rent address prior to incrementing and returning it to core. During data transfers, this register then becomes the memory address.
SLCC	6412/6432 6452/6472	Transfers the contents of AC00–AC05 for selecting terminal ready, idle mode, transmit request, and selectable functions, respectively. (AC00) Terminal Ready permits the modem to enter into the data mode. (AC01) Idle Mode allows a continuous transmission from the same location in core without program intervention. The hardware will enter the idle mode when the word count goes to ZERO. Further, the transmit current address and word count will no longer be incremented and access to the last address will continue until the SGTT instruction is issued or the idle bit is negated. (AC02) Interface Enable allows program interrupts and data break cycles. (AC03) Transmit Request activates the request to send line. (AC04, AC05) are for use by end users. When modem timing signals are used, one EIA (or current mode) transmitter is available to be used with AC04 or AC05.
SSRG	6410/6430 6450/6470	Skips the next instruction and clears the ring flag if the ring flag is a ONE.
SSCA	6411/6431 6451/6471	Skips the next instruction and clear the carrier/AGC flag if the carrier/AGC flag is in the ONE state. The flag is in the ONE state if the carrier/AGC line has made an ON and/or OFF transition. The detected transitions are jumper selectable.
SRS2	6414/6434 6454/6474	Transfers status to AC00–AC07. This instruction is primarily for diagnostic and/or program debug. The AC vs. status is as follows: AC00 Carrier/AGC AC01 Request to send AC02 Terminal ready

MNEMONIC	OCTAL CODE	FUNCTION
		AC03 Clear to send AC04 TEMA 0 field AC05 TEMA 1 select AC06 TEMA 2 register AC07 Receive data
SRS1	6415/6435 6455 6475	Transfers status to AC00–AC07. This instruction is primarily for diagnostic and/or program debug. The AC vs. status is as follows: AC00 R-RQST Receive & transmit AC01 T-RQST Break requests AC02 Sync 2 Received "sync" AC03 Sync 1 characters AC04 REMA 0 field AC05 REMA 1 select AC06 REMA 2 register AC07 modem ready

Transmit and Receive Data
The 6, 7, or 8-bit character is right justified. When 6 or 7 bit characters are used, the remaining bits up to 8 are zeros.

AC00 Terminal RDY
AC01 IDLE (1)
AC02 Enable (2)
AC03 Send RQST
AC04 For customer use (write only TTL output)
AC05 For customer use (write only TTL output)

1. If word count goes to zero while in IDLE mode, the transmit current address and word count will no longer be incremented and access to the last address will continue until the instruction SGTT (transmit GO) is assigned or the idle bit is negated.
2. If enable is negated, interrupt request, break in progress and break priority gates are inhibited and the break request flip-flop is latched in the ZERO state.

Character Recognition
Character Recognition (detection) is accomplished for 6, 7, or 8 bit characters. The characters must be stored right justified. When 6 bit characters are used, bits 7 and 8 should be negated. When 7 bit characters are used, bit 8 should be negated.

The stripping or flag generation upon character detection is dependent upon bit 0 of the compare character word. If bit 0 of the compare char-

acter word is set to a ONE and the stored character is found to compare with the received character, further memory cycles will be terminated (i.e., the word count and current address will not be incremented and there will be no stored character.) If bit 0 is a ZERO and there is a character comparison, the character detected flag will be raised, the number of the recognized character will be stored for one character time in a two bit register, and the received character will be transferred to the current address + 1.

Field Selection
The selected field (increments of 4K of memory up to 32K) address combined with the current word address forms a 15 bit address for transfers to and from memory.

The field for character transfer is specified by program instruction (SLFL) and the contents of the AC. The field vs. AC assignments are as follows:

AC00, AC01, AC02	Transmit field (octal 0–7)
AC03, AC04, AC05	Receive field (octal 0–7)

Character Detected (Reading of)
When the instruction "read character detected (SRCD)" is used to determine what character was detected, two bits, corresponding to the low order bits of the access address are transferred to AC10 and AC11 as follows:

AC10	AC11	Access Address (Binary)
0	0	0000
0	1	0001
1	0	0010
1	1	0011

MNEMONIC	OCTAL CODE	FUNCTION
SGTT	6405/6425 6445/6465	SGTT sets the transmit go flip-flop. This instruction implies that the program is ready to transmit data (i.e., the current address (CA) and word count (WC), have been updated). Upon receipt of this instruction, provided clear to send (CS) has been received in response to request to send (RS), memory references begin immediately. Memory references will cease only when word count (WC) decrements to zero (WC → 0). In this event, if SGTT is not issued in one character time, the transmit

MNEMONIC	OCTAL CODE	FUNCTION
		line will be maintained at mark hold. Transmit request should be asserted (SGTT instruction) and should not be cleared until two bit times after the last bit has been transmitted.
SGRR	6404/6424 6444/6464	SGRR sets the receive go flip-flop. This instruction implies that the program is ready to achieve data from the communications line, (i.e., the current address (CA) and word count (WC) have been updated). The hardware, upon receipt of this instruction, will begin memory references if two consecutive synchronizing characters have been recognized by the hardware on the incoming serial data line. Memory references will cease only when WC decrements to zero (WC → 0) and SGRR is not issued in less than one character time.
SSCD	6400/6420 6440/6460	The SSCD instruction causes the program to skip the next instruction if the character detect flag is a ONE. The character detect flag is a ONE if an assembled character is found to be identical with one of the stored characters in the first four locations of the access address. Additionally, the SSCD instruction clears the character detected flag. If the program is required to identify which of the four stored characters compared to the contents of the receive buffer, then a read character detected (SRCD instruction) should be utilized. See the SRCD instruction for details.
SCSD	6406/6426 6446/6466	Clears the "sync character detection" flip-flops. This instruction enables the programmer to initialize the sync detection circuits and clear the receive registers without initializing the modem interface.
SSRO	6402/6424 6444/6464	Skips the next instruction and clears the flag if the receive overflow flag is a ONE. The receive overflow flag is a ONE if, during the receive data break sequence, the word count (in memory) overflowed.
SCSI	6401/6421 6441/6461	Initializes all active functions in the synchronous interface.

MNEMONIC	OCTAL CODE	FUNCTION
SLFL	6413/6433 6453/6473	Transfers the contents of AC00–AC05 to the field select registers. AC00–AC02 selects the transmit field while AC03–AC05 selects the receive field. The selected field (increments of 4K of core—up to 32K) combined with the current address forms a 15 bit address for data transfers to and from memory.
SSTO	6403/6423 6443/6463	Skips the next instruction and clears the flag if the transmit overflow flag is a ONE. The transmit overflow flag is a ONE if, during the transmit data break sequence, the word count (in memory) overflowed.
SSBE	6416/6436 6456/6476	Skips the next instruction and clears the bus error flag if the flag was in the ONE state. The bus error flag will be in the ONE state if a transmit or receive break request has not been serviced in less than 1/baud time. This flag implies that the break bus is either overloaded or is inoperative.
SRCD	6417/6437 6457/6477	The contents of a two bit register, which contains the address of the detected character, is transferred to AC10 and AC11. The two bits correspond to the two low order bits of the access address where the characters for detection are stored.

MAINTENANCE INSTRUCTION

The SRCD instruction issued when AC00 is set to a ONE causes a single clock pulse on the maintenance clock line to the modem. In the test configuration this line is returned as the transmit and receive clocks enabling single step testing of the transmit and receive circuits.

DP8-E DESIGNATIONS

The DP8-EA synchronous modem interface and modem cable is used on Bell 201, or equivalent, modems.

The DP8-EB synchronous modem interface and modem cable is used on Bell 300 series, or equivalent, modems.

MNEMONIC	OCTAL CODE	FUNCTION
SSCD	6400/6420 6440/6460	Skip if character detected

MNEMONIC	OCTAL CODE	FUNCTION
SCSI	6401/6421 6441/6461	Clear synchronous interface
SSRO	6402/6422 6442/6462	Skip if receive word count overflow
SSTO	6403/6423 6443/6463	Skip if transmit word count overflow
SGRR	6404/6424 6444/6464	Receive go
SGTT	6405/6425 6445/6465	Transmit go
SCSD	6406/6426 6446/6466	Clear sync detect
SRTA	6407/6427 6447/6467	Read transfer address register
SSRG	6410/6430 6450/6470	Skip if ring flag
SSCA	6411/6431 6451/6471	Skip if carrier/AGC flag
SLCC	6412/6432 6452/6472	Load control
SLFL	6413/6433 6453/6473	Load field
SRS2	6414/6434 6454/6474	Read status 2 AC00 carrier/AGC AC01 request to send AC02 terminal ready AC03 clear to send AC04 TEMA 0 AC05 TEMA 1 AC06 TEMA 2 AC07 receive data (inv.)
SRS1	6415/6435 6455/6475	Read status 1 AC11 R-RQST AC01 T-RQST AC02 SYNC 2 AC03 SYNC 1 AC04 REMA 0 AC05 REMA 1 AC06 REMA 2 AC07 modem ready
SSBE	6416/6436 6456/6476	Skip on bus error

MNEMONIC	OCTAL CODE	FUNCTION
SRCD	6417/6437 6457/6477	Read character detected Lower order bits (access address) AC10 and AC11
—	6417/6437 6457/6477 with AC00-ONE	Maintenance clock

12-CHANNEL BUFFERED DIGITAL I/O, DR8-EA

DESCRIPTION

The DR8-EA digital I/O can be used to control 12 discrete digital switching circuits located externally and can be used to accept 12 discrete digital inputs from external sources. The unit consists of IOT control logic, a 12-bit input buffer, a 12-bit output buffer, and 3 multiplexer ICs that control the flow of data for input and output operations. All DR8-EA circuits are TTL logic and are mounted on a single quad module which plugs into the Omnibus. The standard TTL outputs are connected to the external load via two H854 connectors on the module. Inputs from external sources are also connected to the DR8-EA, using H854 connectors.

OUTPUT BUFFER

Data outputs are updated under program control. Standard output drivers have a TTL 30-unit load capability. For an output function, the computer issues a DBSO, DBCO, or DBRO instruction. For DBSO instructions, only logical 1s in the AC are loaded into the output register; AC bits containing logical 0s do not affect output register bits. For DBCO instructions, logical 1s in the AC result in logical 0s in corresponding bits of the output register. For DBRO instructions, the content of the output register is transferred into the AC register.

INPUT BUFFER

Data inputs must be TTL compatible, have negative transition to 0.8 V or less for a logical 1, and have a pulse duration of greater than 50 ns. Pulse rise time and fall time should be less than 150 ns for maximum noise immunity. In one mode of operation, the input register bits, after being set by the data inputs, remain set until read by a DBRI instruction. In the second mode of operation, the inputs can be placed directly on the bus and are not cleared by the DBRI instruction. The DBRI instruction is also used to read the input data. When this IOT is issued, the contents of the input register is gated to the AC via the Omnibus. A DBCI instruction, used with a DBRI instruction, enables inputs that occurred too late to be read by the next DBRI instruction. Correct usage of this feature results in *zero dead time* for events. Any of the input lines can cause a skip and an interrupt. If the proper jumpers are removed, individual input lines can be disconnected from the skip and interrupt gating. The interrupt facility can be enabled by instruction DBEI and disabled by instruction DBDI.

EXPANSION

A maximum of eight DR8-EA options can be used. The user determines each device selector code by means of jumpers. Device codes 50 to 57 are legal; however, the DR8-EA normally comes with device code 50 installed.

SPECIFICATIONS

Input Format: Parallel, 12 bits

Input Levels:	TTL-compatible levels. Input lines clamped at +0.6 V to −15 V for negative input protection.
Input Connections and Pulse Width:	Inputs to inverter buffers are normally held high by resistors. A negative transition of 0.8 V or less causes the input to become a logical 1. Optional inputs bypass the flip-flop for direct interrogation of input line status.
Output Format:	Parallel, 12 bits
Output Levels:	TTL-compatible levels capable of driving 30 unit loads. Output lines are protected against damage from short circuits to ground.
Environmental:	5° to 50° C (41° to 122° F) 10% to 90% relative humidity (noncondensing)
Power Requirements:	+5.0 V, 2.25 A (worst case)

PROGRAMMING THE DR8-EA

The following instructions are used for DR8-EA operation. The X refers to a jumper selectable code. However, the DR8-EA normally comes with code 50 installed.

MNEMONIC	OCTAL CODE	FUNCTION
DBDI	65X0	Disables all interrupts that are caused by a logical 1 on the input.
DBEI	65X1	Sets interrupt enable flip-flop. This tests the IN FLAG and causes an interrupt request if IN FLAG equals 1.
DBSK	65X2	Tests the IN FLAG. If the flag is a 1, the next sequential memory location is skipped.
DBCI	65X3	1s in the AC clear respective bits in the input register.
DBRI	65X4	Transfers the complete 12-bit input register to the AC.
DBCO	65X5	1s in the AC clear the respective bits in the output register.
DBSO	65X6	1s in the AC set the respective bits in the output register.
DBRO	65X7	Transfers the complete 12-bit output register to the AC.

INTERFACE

Interface to the "outside world" is by two edge connectors on the M863 module. Signals leaving the board (12 bits parallel) are high

(+3 V) for a logical false and ground (0 V) for a logical true. Each output line has approximately 20 mA of drive (high level) and 20 mA of sink (low level). Output levels remain fixed except when changed by the processor.

Signals entering from the "outside world" must be TTL compatible. The input represents approximately two unit loads. When jumpered for *edge detection,* a negative-going edge (3 V to 0 V) is sensed. The signal must remain low (0 V) for at least 50 ns. When sensing for an external level, ground (0 V) represents a logical true and a high (+3 V) represents a logical false. With all bits jumpered this way, the option represents a 12-bit parallel input register, rather than an event detector. The DR8-EA is shipped with edge detection jumpers installed.

OPTIONAL INTERFACE METHOD

An optional means of interfacing to the DR8-EA is available by using two BC08J-X cables. Each cable (ribbon type) is terminated by a Berg-type connector on one end (for interfacing to the DR8EA module) and a standard DIGITAL FLIP-CHIP module on the other end. One cable is used for the input, and the other is used for output.

CABLE DESCRIPTIONS

The 7008418 cable is used to jumper the input to the output for diagnostic purposes. This cable is part of the DR8-EA option. If the user wants interface cables, a BC08-J cable consisting of the 1210073-0 Berg connector, cable, and the M953 module, can be purchased.

PIN CONNECTIONS

The output and input pins on the Berg-type connector that correspond to the particular AC bits enabled in the DR8-EA are as follows:

J2 — Input		J1 — Output	
D	— Bit 0	D	— Bit 0
F	— Bit 1	F	— Bit 1
J	— Bit 2	J	— Bit 2
L	— Bit 3	L	— Bit 3
N	— Bit 4	N	— Bit 4
R	— Bit 5	R	— Bit 5
T	— Bit 6	T	— Bit 6
V	— Bit 7	V	— Bit 7
X	— Bit 8	X	— Bit 8
Z	— Bit 9	Z	— Bit 9
BB	— Bit 10	BB	— Bit 9
DD	— Bit 11	DD	— Bit 11

M953 Connections (BC08-J Cable)

Bit	Pin	Gnds
0	B1	A1
1	D2	C1
2	D1	F1
3	E2	K1

DR8

Bit	Pin	Gnds
4	E1	N1
5	H2	R1
6	H1	T1
7	K2	C2
8	J1	F2
9	M2	J2
10	L1	L2
11	P2	N2
		R2

INDUSTRIAL CONTROL SYSTEM, ICS8

DESCRIPTION

The ISC8 is a cabinet-mounted subsystem used to monitor and/or control industrial operations and equipment. The device interfaces with PDP-8/A computers, and provides real-time monitoring and control capability with minimal computer overhead. Applications range from simple monitoring functions to control of complex closed-loop systems. Environmental monitoring and control, batch mixing, material handling, quality control, and testing are but a few of the many applications for which the ICS8 is suited.

The flexibility of the ICS8 in adapting to many different applications is possible because of the modularity of the device and the many different types of I/O modules offered. A system may contain from 1 to 16 subsystems, or files, with each file containing up to 16 I/O modules. I/O modules are available to perform the following functions:

a. Outputs: Solid state and relay

b. Inputs: Solid state isolated and direct voltage sense and interrupt

c. I/O Counter

d. Analog-to-digital (A/D) converters.

e. Digital-to-analog (D/A) converters.

File dimensions:	width 19 in. (48.3 cm.) height 21 in. (53.3 cm.) depth 12 in. (30.5 cm.)
Weight:	82 lbs (37 kg) less I/O modules but includes H772 Power Supply and M8091 Master Control Module or M8092 File Control Module.

FUNCTIONAL DESCRIPTION

The ICS8 consists of one Master File and up to 15 additional Expander Files. The Master File contains a Master Control module (M8091). This module consists of the ICS8 System Control and one File Interface. The System Control coordinates all activities within the ICS8 in response to programmed IOT instructions and interrupts.

The function of the File Interface is to decode and encode the I/O module addresses and route data to and from the addressed I/O modules. Each Expander File contains a File Control module (M8092). This module consists of one File Interface which is functionally identical to the file interface on the M8091. Since each file can contain up to 16 I/O modules, and 16 files are allowed, the total system capacity is 256 I/O modules. Communication between the PDP-8, the Master Control, the File Control, and the I/O modules is accomplished via the following three buses:

Positive I/O Bus
The Positive I/O bus is utilized by the PDP-8 to communicate with many peripherals, including the ICS8. It routes 12-bit words and control signals between the PDP-8A and the ICS8 Master Control. For more information about the Positive I/O Bus, see Volume 1 of the PDP-8/E/F/M Maintenance Manual.

Expander Bus
The master control communicates with up to 16 I/O modules, utilizing the ICS I/O Bus. There is a separate ICS I/O Bus for each file. Note that this bus is etched on the backplane of the ICS File.

Each I/O module in the ICS can be accessed by a unique 8-bit address. Once accessed, data can be loaded into the selected module or data can be read from the module. For data output operations, the interface and control modules route a 12-bit data word from the Buffered Accumulator (BAC) lines of the PDP-8 Positive I/O Bus to the I/O module specified by the content of an Address Register. For data input operations, the interface and control modules select a 12-bit data word from the I/O module specified by the content of the Address Register, and gate this data to the Accumulator (AC) lines of the PDP-8 Positive I/O Bus. An interrupt request scheme is also provided to allow certain I/O modules to request service by the PDP-8.

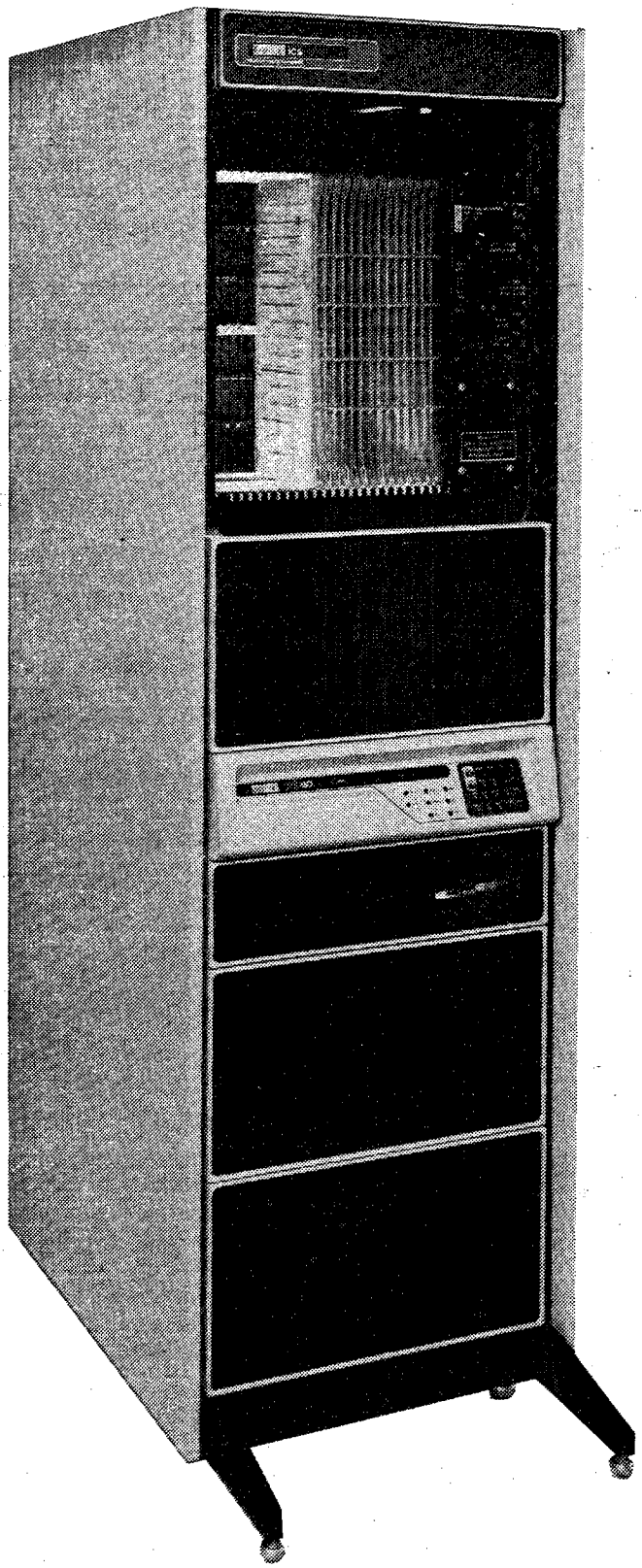
EQUIPMENT DESCRIPTION
The ICS8 is available in four configurations:

ICS8-MA	115/230 Vac, 60 Hz, Master File
ICS8-MB	115/230 Vac, 50 Hz, Master File
ICS8-XA	115/230 Vac, 60 Hz, Expander File
ICS8-XB	115/230 Vac, 50 Hz, Expander File

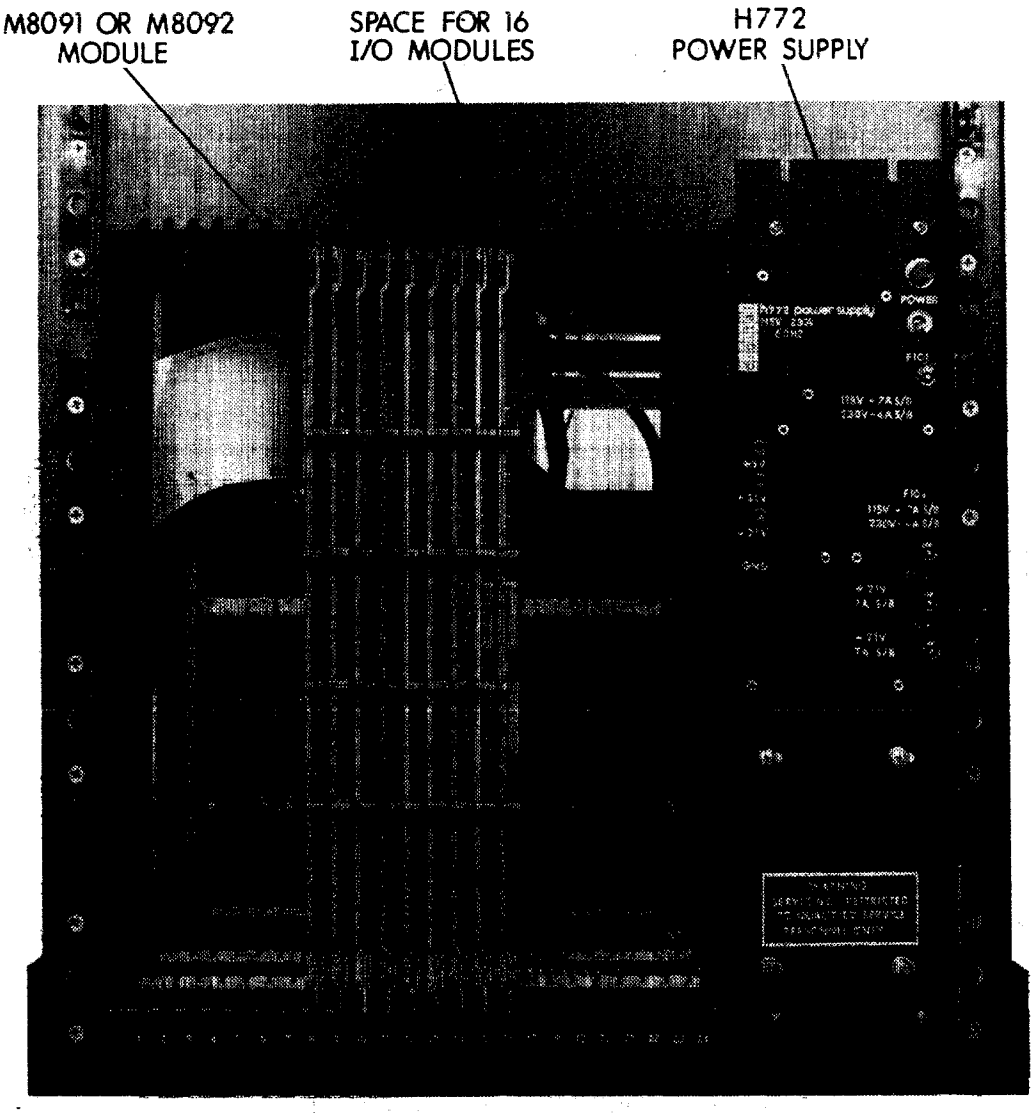
The ICS8 subsystem is housed in cabinet-mounted files with self-contained dc power supplies. The subsystem can comprise the following:

a. Printed circuit backplane
b. Master Control module (M8091)
c. File Control module (M8092)
d. H772 Power Supply
e. Cooling fan assembly
f. H009 screw terminal mounting hardware
g. Electromagnetic shield
h. Space for mounting 16 I/O modules (optionally selected by type).

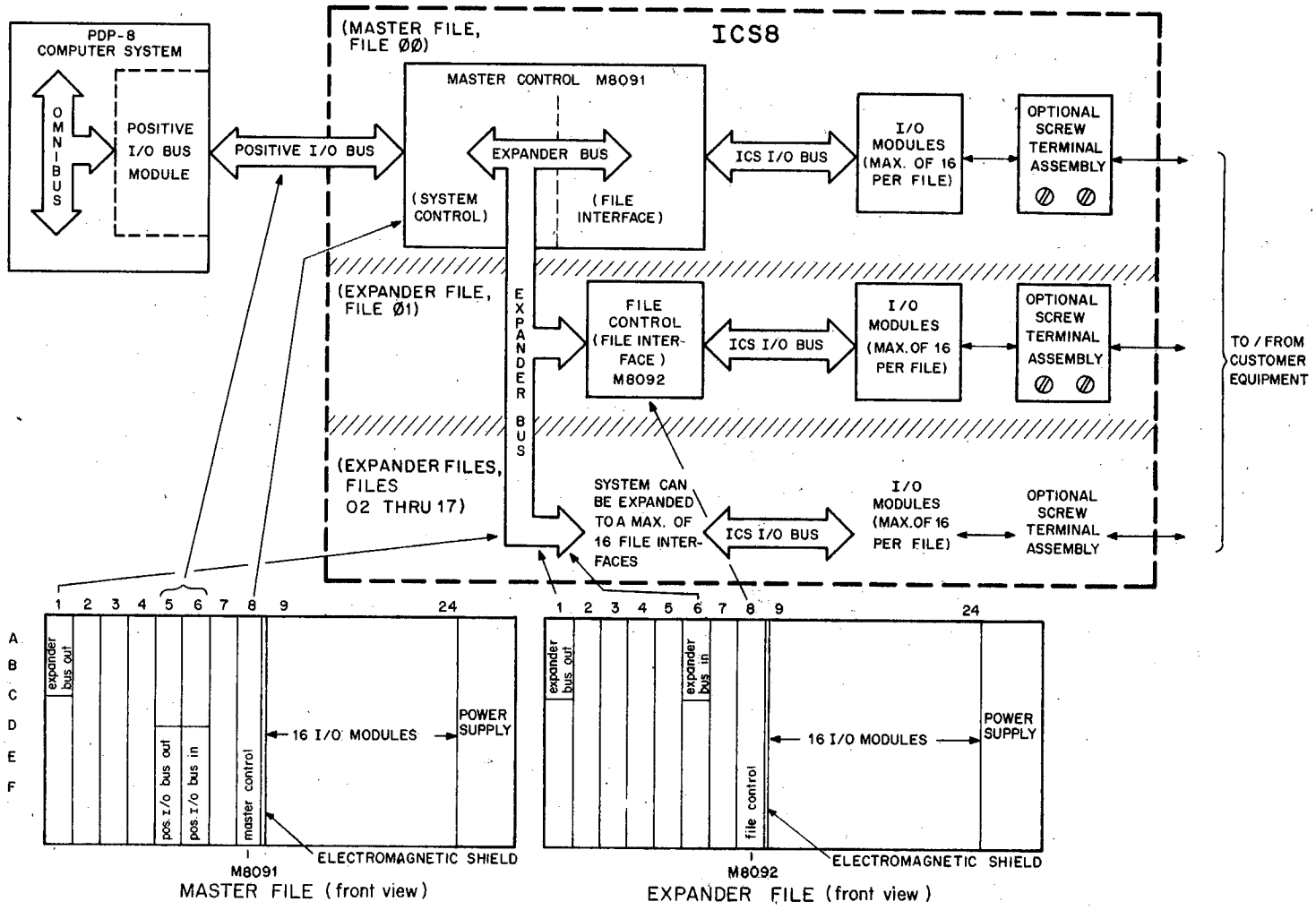
M8091 Master Control Module—The M8091 is a hex module that mounts in slot 8 of the Master File. It contains circuits to control addresing, data transfer and interrupt servicing between the Positive I/O Bus and the Expander Bus. It also interfaces the Expander Bus to the functional I/O modules in the Master File.



ICS8 System



Typical File Arrangement (Front View)



ICS8 Functional Block Diagram

M8092 File Control Module—The M8092 is a hex module that mounts in slot 8 of an Expander File. This module contains circuits for controlling addressing, data transfer, and interrupt servicing between the Expander Bus and the ICS I/O bus for the Expander File.

I/O Modules—The I/O modules are hex modules which mount in file slots 9-24. The modules contain logic and signal conditioning circuitry and, except where noted below, handle 12 bits of parallel data. The accompanying table provides a brief description of each I/O module available. These modules are optionally selected by the customer in accordance with particular needs and applications.

H772 Power Supply—The H772 power supply generates all dc operating power required by the ICS8, including the interface and control module and the I/O modules. The unit outputs regulated +5V and unregulated +21V and −21V.

Optional Equipment

The following options may be purchased with the ICS8 subsystem:

a. H964 DEC Cabinet
b. Digital/Analog Screw Terminal Assembly
c. H8030 Connector Block
d. H964P Top Entry Kit

H964 DEC Cabinet—This DEC-built 19-inch cabinet is recommended for mounting the ICS8 (see accompanying figure). The cabinet will mount two ICS8 files, and is equipped with an 861 Power Controller, air baffle, and cooling fans. If ordering the cabinets separately, the H964-FA version should be ordered for 115 Vac, 50/60 Hz; the H964-FB version for 230 Vac, 50/60 Hz.

I/O Module Descriptions

OPTION	MODULE NO.	DESCRIPTION
IDC-IA	W7410	Solid-state isolated voltage sense input module, containing optically-coupled differential inputs. Voltage ranges of 6, 24, and 48 V are jumper-selectable.
IDC-IB	W7430	Solid-state isolated voltage interrupt input module containing optically-coupled differential inputs. Voltage ranges of 6, 24, and 48 V are jumper-selectable.
IDC-IC	W7440	16-bit asynchronous binary counter.
IDC-ID	W7411	Solid-state non-isolated voltage input module compatible with TTL logic levels. Input voltage ranges from −30 to +55 V maximum.
IDC-IE	W7431	Solid-state non-isolated voltage interrupt module compatible with TTL logic levels. In-

OPTION	MODULE NO.	DESCRIPTION
		put voltage ranges from —30 to +55 V maximum.
IDC-OA	M6850	Solid-state dc output used to drive solid-state logic, or as a current sink. Output circuit includes diode protection against transients due to inductive loads. Open-collector outputs can take externally supplied voltages up to +55 volts dc maximum, and can sink up to 250 mA maximum.
IDC-OB	M6870	Solid-state single-shot dc output to drive solid-state logic or as a current sink. Output circuit includes diode protection against transients due to inductive loads. Open-collector outputs can take externally supplied voltages up to +55 volts dc maximum, and can sink up to 250 mA maximum.
IRL-OA	M8030	Latching relay output with electrically isolated mercury wetted relays. Form A (normally open) or B (normally closed) contacts with a rating of 55 volts dc or peak ac, 2A, 100 VA maximum.
IRL-OB	M8050	Flip-flop relay output with electrically isolated mercury wetted relays. Form A (normally open) or B (normally closed) contacts with a rating of 55 volts dc or peak ac, 2A, 100 VA maximum.
IDA-OA	A6330	4-channel, 10-bit digital-to-analog converters. Output ranges of 0 to +10 volts (15 mA maximum) or 0 to 20 milliamps (+10 volts maximum).
IAD-IA	A005	8-channel wide-range differential analog-to-digital converter. Uses flying capacitor mercury wetted relay multiplexer. Resolution is 12 bits bipolar with a scan rate of 200 samples per second and a sample rate of 20 samples per second, same channel. Input ranges of ±10 millivolts to ±10 volts or ±1 milliamp to ±50 milliamps full scale.
IMX-IA	A007	16-channel flying capacitor relay multiplexer module for use in expanding IAD-IA. Up to 7 IMX-IA modules may be added to each IAD-IA.
ISH-IA	A907	Analog shield used to electromagnetically shield the IAD-IA and IMX-IA. Required when an IRL-OA or IRL-OB is placed within four module slots of an IAD-IA or IMX-IA. ISH-IA takes one module slot in the ICS8.

I/O Module Descriptions (Cont.)

OPTION	MODULE NO.	DESCRIPTION
ICJ-IA	M908 (modified)	Empty slot jumper module. Used when I/O module slots are left empty between interrupt-generating modules. One ICJ-IA is required for each empty slot in the interrupting module file.
IAC-OA	M6850, H912, and BC40J-06	12-bit solid-state isolated 120 Vac output. Used to convert logic levels to 120 Vac to drive field devices. Continuous current rating, 2A. (Uses H1601 I/O converters.)
IAC-OB	M6870, H912, and BC40J-06	12-bit solid-state isolated 120 Vac single-shot output. Used to convert logic levels to 120 Vac to drive field devices. Continuous current rating, 2A. (Uses H1601 I/O converters.)
IAC-IA	W7411, H912, and BC40J-06	12-bit solid-state isolated 120 Vac sense. Used to convert 120 V inputs from limit switches, photocells, pushbutton switches, etc., into logic level signals that are compatible with ICS8. (Uses H1501 converters.)
IAC-IB	W7431, H912, and BC40J-06	12-bit solid-state isolated 120 Vac interrupt. Same as IAC-IA with the addition of interrupt capability. (Uses H1501 converters.)
IAC-OC	M6850, H912, and BC40J-15	Same as IAC-OA except longer cable.
IAC-OD	M6870, H912, and BC40J-15	Same as IAC-AB except longer cable.
IAC-IC	W7411, H912, and BC40J-15	Same as IAC-IC except longer cable.
IAC-ID	W7431, H912, and BC40J-15	Same as IAC-ID except longer cable.

SPECIFICATIONS

Physical

	Width	Height	Depth
File Dimensions:	19 in. (48.3 cm)	21 in. (53.3 cm)	12 in. (30.5 cm)

File Weight: 82 lb (37 kg) (Less I/O modules, but including the H772 Power Supply and the M8091 Master Control module or the M8092 File Control module)

Environmental

The ICS8 meets the requirements of DEC Standard 102 for a Class C environment:

a.	Temperature:	Operating (in DEC cabinet):	+5° C (41° F) to +50° C (122° F) ambient
		Nonoperating:	−40° C (−40° F) to +66° C (150.8° F) ambient
b.	Humidity:	Operating: 10% to 95% R.H. Maximum wet bulb: +32° C (89.6° F) Minimum dew point: +2° C (35.6° F)	
		Nonoperating: 10% to 95% R.H.	

Power Requirements

ICS8-MA, ICS8-XA	104–127/208–254 Vac 6.4/3.2 amps max. 60 Hz ± 1% 600 Watts maximum
ICS8-MB, ICS8-XB	104–127/208–254 Vac 6.4/3.2 amps max. 50 Hz ± 1% 600 Watts maximum

Performance

a.	Operational Modes	Programmed I/O (digital and analog) Interrupt-controlled I/O (digital and analog)
b.	Number of Digital Inputs and outputs	Sixteen 12-bit words (192 points) maximum per file
c.	Number of Analog Inputs	240 differential channels maximum per file (two groups of an 8-channel, 12-bit A/D converter with expansion in 16-channel groups to 120 channels each).
d.	Number of Analog Outputs	Twelve 4-channel, 10-bit D/A converters maximum per file
e.	Digital Input Types	
	solid-state isolated	Voltage sense and interrupt (6 V, 24 V, 48 V jumper-selectable)
	solid-state nonisolated	Voltage sense and interrupt (High-impedance input, TTL-compatible)
f.	Digital Output Types	
	Solid-state nonisolated	DC output (open-collector 250 mA maximum, up to +55 Vdc) DC single-shot output (open-collector 250 mA maximum, up to +55 Vdc)

	Solid-state isolated	AC flip-flop driver (120 Vac); AC single-shot driver (120 Vac)
	Relay—Mercury wetted	2A maximum, 0–55 Vdc or peak ac; 100 VA maximum
g.	I/O Word Selection	Addressable by means of Address Register
h.	Interrupting Module Identification	A 4-bit generic code and 8-bit address code are available when the interrupt is serviced. Generic code associated with module selected by the Address Register is always available.
i.	System Hardware I/O Data Rate	
	Load Data	7.4×10^4 words/sec maximum (based on PDP-8/E with core memory)
	Read Data	8.0×10^4 words/sec maximum (based on PDP-8/E with core memory)
j.	Computer Interface	
	Master File	Interfaces to PDP-8 Positive I/O Bus
	Expander File	Interfaces with Master File via ICS8 Expander Bus
k.	Power Supply Outputs	
	+5 Vdc regulated @ 25 A maximum	
	+21 Vdc unregulated @ 5.5 A maximum	
	−21 Vdc unregulated @ 2.5 A maximum	
	LTC (Line Time Clock)	AC line frequency square wave, 30% to 70% duty cycle worst case, −1 V to +5 V amplitude
l.	Heat Dissipation	2050 Btu/hr maximum, exclusive of heat dissipation due to field input circuits

NOTE

Heat dissipation is a function of the type and quantity of I/O modules used.

APPLICABLE DOCUMENTS

The following table lists other documents applicable to the ICS8 subsystem.

Table 1-2 Applicable Documents

TITLE	NUMBER	COVERAGE
PDP-8 Maintenance Manuals		A series of maintenance and theory manuals that provide a detailed description of the basic PDP-8 system.

Table 1-2 (Cont.) Applicable Documents

TITLE	NUMBER	COVERAGE
PDP-8/E, PDP-8/M and PDP-8/F Small Computer Handbook or PDP-8/A Minicomputer Handbook	N/A N/A	A general handbook that discusses system architecture, addressing modes, the instruction set, programming techniques, and software.
Introduction to Programming	DEC-08-XINPA-A-D	A handbook which provides an explanation of computer mathematics, and an introduction to machine language and assembly language programming. It also describes the basics of program loading and error correction. The programs in this handbook are designed to be run on the PDP-8/E, F, M, or A.
861-A, B, C Power Controller Maintenance Manual	DEC-00-H861A-A-D	A maintenance manual covering operation and maintenance of the 861 Power Controller. Detailed descriptions included.
Industrial Control Subsystem AC Option Descriptions	EK-ICSAC-OD-001	A manual describing the eight AC options available for use in the ICS8 Industrial Control subsystem.

* Applicable manuals are furnished with the system at time of installation. The document number depends upon the specific PDP-8 family processor.

EXTENDED ARITHMETIC ELEMENT (EAE), KE8-E

DESCRIPTION

The KE8-E Extended Arithmetic Element (EAE) enables the central processor to perform arithmetic operations at high speeds. By incorporating the EAE option with the existing central processor logic, the two equipments operate asynchronously. The option consists of two quad modules containing circuits that perform parallel arithmetic operations on positive binary numbers. It includes the registers and control logic circuits described in the following paragraphs.

NOTE

The EAE is available for use with 8E, 8M, and 8A 600/620 series machines.

Step Counter

The 5-bit step counter register is used to record the number of shifts performed during a logical or arithmetic shift operation and to stop the operation once the correct number of shifts has been executed. The step counter is incremented as each shift is performed, and step counter overflow terminates the shift operation. When an ASR, LSR, SCL, or SHL instruction is executed, the step counter is loaded with the complement of the step count contained in bits 7–11 of the memory location following the instruction. Bits 7–11 of the AC are loaded directly into the step counter during execution of an ACS instruction. The step counter is cleared for MUY, DVI and NMI instructions.

EAE Instruction Register (IR)

The EAE IR is a 12-bit register that is loaded during the FETCH cycle of EAE instruction execution. Bits 6 and 8–10 of the IR are of particular interest, since these bits identify the particular EAE operation to be executed.

EAE Timing and Control Logic

The EAE control logic is contained on modules which plug into the PDP-8/A Omnibus. These circuits are used in conjunction with the accumulator, link, multiplier quotient and memory buffer registers of the basic PDP-8/A to perform asynchronous arithmetic operations. The EAE control logic adds a larger class of arithmetic instructions to the group 3 operate instruction list.

EAE Mode Flip-Flop

The state of the EAE mode flip-flop determines which of two subsets of EAE instructions is currently implemented. The mode flip-flop is set to mode A when power is applied to the machine, when the INIT key on the programmer's console or operator's panel is operated, and when a CAF instruction is executed. It may be set to mode B or reset to mode A by EAE instructions.

Greater Than Flag

The greater than flag (GTF, not to be confused with the GTF instruction)

is a 1-bit register that is activated during execution of mode B EAE instructions. The GTF remains cleared during execution of all mode A instructions. When the GTF is activated, it receives the content of MQ11 during right shift operations. This facilitates subsequent round-off by indicating whether the content of the MQ should be rounded up (GTF set) or left alone (GTF cleared). The GTF is also set during execution of a SAM instruction, whenever the signed number in the MQ at the end of the operation is greater than or equal to the signed number that was in the AC at the beginning of the operation.

PROGRAMMING THE EXTENDED ARITHMETIC ELEMENT

Extended Arithmetic Element instructions are an extension of the group 3 microinstructions. Like the other group 3 microinstructions, they have an OP-code of 7, while bits 3 and 11 are both set to contain binary ones. Mode A instructions are wholly compatible with PDP-8/I extended arithmetic element instructions, so that programs written for the PDP-8/I extended arithmetic element may run on the KE8-E Extended Arithmetic Element without modification. Mode B provides a greatly extended set of instructions that is available for new programming on the PDP-8/A. Several EAE operations may be executed in either mode. The common features of these operations are described below.

Multiplication

During a multiplication operation, the content of the 12-bit MQ register is multiplied by a 12-bit multiplier (whose location depends upon the instruction mode). At the conclusion of the multiplication, the 12 most significant bits of the product are in the accumulator while the 12 least significant bits are in the MQ register. The multiplication is an unsigned integer multiply. That is, multiplier and multiplicand are treated as 12-bit, positive binary numbers with the binary point positioned after the least significant bit of each. The binary point of the product is positioned after the least significant bit of the MQ register. If the accumulator is non-zero at the start of the multiplication, its content is added to the low-order half of the product (conained in the MQ register). The link is always cleared.

Division

During a division operation, the content of the AC and MQ registers is treated as a 24-bit dividend with the 12 high-order bits in the AC. This number is divided by a 12-bit divisor (whose location depends upon the instruction mode) and the quotient and remainder are left in the MQ and AC registers, respectively. The division is an unsigned integer divide. The link is cleared if the first subtraction produces a negative result, indicating that divide overflow has not taken place. If the first subtraction produces a positive result, the link is set to indicate that divided overflow has occurred, and the division operation is terminated immediately. The content of the AC and MQ registers is modified by divide overflow, even though the operation is terminated prematurely. Thus, the divide instruction is ordinarily followed by a test of the link to check for overflow before further computation occurs.

Left Shift
During a left shift operation the link, AC and MQ are treated as one long register, with a high-order bit in the link and low-order bits in the MQ. The previous content of the link is lost during each shift, while AC0 is shifted into the link, MQ0 is shifted into AC11, and a zero is shifted into MQ11. The number of shifts to be executed is determined by a shift count contained in bits 7–11 of the location following the left shift instruction. Program execution resumes at the location following the shift count.

Logical Right Shift
During the logical right shift operation, the link, AC and MQ are treated as one long register. MQ11 is either lost or shifted into the GTF, depending upon the mode of the instruction. AC11 is shifted into MQ0, while a zero is shifted into the link and into AC0. As in a left shift, the number of shifts to be executed is determined by a shift count contained in bits 7–11 of the location following the logical right shift instruction. Program execution resumes at the location following the shift count.

Arithmetic Right Shift
The arithmetic right shift operation is identical to the logical right shift except that AC0 is shifted into itself and into the link.

Normalization
Normalization is the process of adjusting a number such that the most significant bit is equal to 1. The exponent is adjusted accordingly to maintain the equality of the number. The step counter is initially cleared. The contents of the link, AC and MQ are then shifted left, as described above, until AC0 and AC1 are different. The step counter is incremented once for each shift. (If AC2 through MQ11 are all zero, the number is already normalized and no shift occurs.) At the conclusion of a normalize operation, the step counter contains the binary number by which the AC and MQ were multiplied to accomplish normalization. Normalize instructions must not be microprogrammed with other instructions because the resulting octal codes are reserved to switch instruction modes.

EAE Mode Changing Instructions

MNEMONIC	OCTAL CODE	FUNCTION
SWAB	7431	Switch from A to B. If the mode flip-flop was set to A, it is set to B. If the mode flip-flop was already set to B, it remains in mode B. In either case, an MQL instruction is also executed.
SWBA	7447	Switch from B to A. If the mode flip-flop was set to B, it is set to A. If the mode flip-flop was already set to A, no operation occurs.

The following instruction sequence is used to test the EAE mode flip-flop and determine which mode is currently implemented:

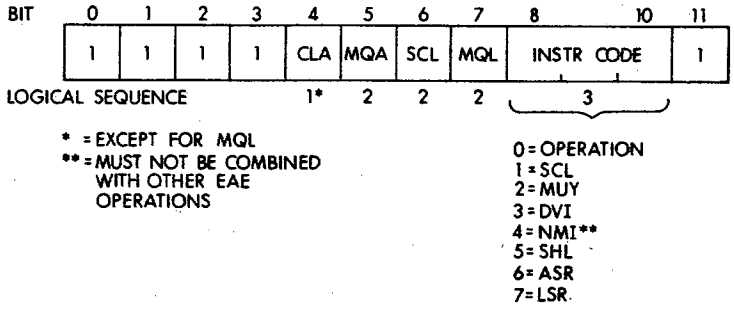
MNEMONIC	OCTAL CODE
CAM	7621
DPSZ	7451

A skip will occur if the EAE is in mode B. If the EAE is in mode A, the skip will not occur and the SC will be loaded into the AC and normalized (a meaningless operation that modifies the content of the AC).

MODE A INSTRUCTIONS

The OP-code in a mode A instructor must be 7, while bits 3 and 11 are both 1. Bits 4, 5 and 7 are used by the group 3 operate microinstructions introduced in Chapter 5. Bit 6 is set to indicate an SCA instruction. Bits 8–10 are set to indicate one of the mode A instructions listed in the accompanying figure. These instructions may be microprogrammed with SCA and the group 3 microinstructions to form non-conflicting combined operations. The microprogrammed combination of two (or more) extended arithmetic element instructions is the bitwise logical OR or the octal codes for the individual instructions.

Most of the mode A EAE instructions require an operand, which is assumed to occupy the next word in memory, following the instruction. After execution of an EAE instruction that requires an operand, program execution resumes at the memory location following the operand. The greater than flag (GTF) is always zero for mode A instructions.



EAE Mode "A" Bit Assignments

KE8-E Mode A instructions

MNEMONIC	OCTAL CODE	FUNCTION
SCA	7441	Step Counter OR with AC. The content of the step counter is combined with the content of the low-order 5 bits of the AC (AC7–11) by a bitwise logical OR operation, and the result is loaded into AC7–11. AC0–6 remain unchanged.

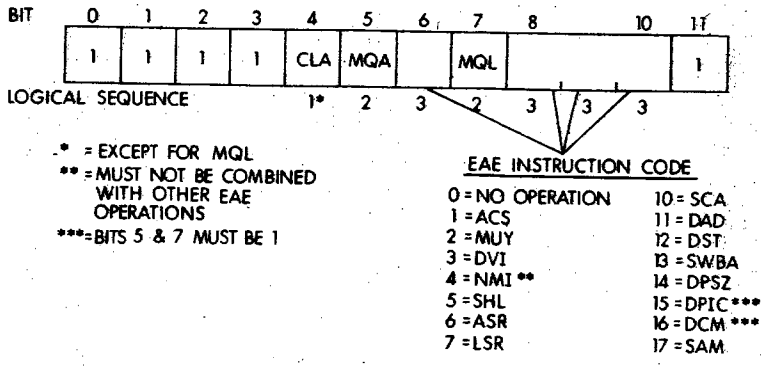
MNEMONIC	OCTAL CODE	FUNCTION
SCA CLA	7641	Step Counter to AC. The content of the step counter is loaded directly into AC7–11. AC0–6 is cleared. This instruction is a microprogrammed combination of SCA and CLA.
SCL	7403	Step Counter Load from Memory. The next word in memory is treated as an operand. The one's complement of the low-order 5 bits of this operand (bits 7–11) is loaded into the step counter, and program execution resumes at the location following the operand. The SCL instruction is most commonly used during interrupt servicing to restore the content of the step counter.
MUY	7405	Multiply. The next word in memory is taken as a multiplier. Multiplication occurs as described above, and program execution resumes at the location following the multiplier.
DVI	7407	Divide. The next word in memory is taken as a divisor. Division occurs as described above, and program execution resumes at the location following the divisor. If divide overflow occurs, the link is set. If the division was legal, the link is cleared.
NMI	7411	Normalize. The content of the AC and MQ are normalized as described above. This instruction must not be microprogrammed with any other instruction.
SHL	7413	Shift left. The content of the AC and MQ is shifted left as described above. The number of shifts performed is equal to one more than the content of the 5 low-order bits (bits 7-11) of the next location in memory. Program execution resumes at the location following the shift count.
ASR	7415	Arithmetic Shift Right. The content of the link, AC, and MQ are shifted right as described above. The number of shifts performed is equal to 1 more than the content of the 5 low-order bits (bits 7-11) of the next location in memory. The previous content of MQ11 is lost as each shift is executed. Program execution resumes at the location following the shift count.

MNEMONIC	OCTAL CODE	FUNCTION
LSR	7417	Logical Shift Right. The content of the link, AC and MQ are shifted right as described above. The number of shifts performed is equal to 1 more than the content of the 5 low-order bits (bits 7-11) of the next location in memory. The previous content of MQ11 is lost as each shift is executed. Program execution resumes at the location following the shift count.

MODE B INSTRUCTIONS

Mode B instructions differ from mode A instructions in the use of bit 6 of the instruction word, the location of operands, and in greatly increased double-precision arithmetic capability. The accompanying figure shows the format of a mode B instruction. As with mode A instructions, mode B instructions may be microprogrammed to combine non-conflicting logical operations.

Some mode B instructions require a double precision operand, which is simply two consecutive memory locations that are assumed to contain a 24-bit number with the 12 most significant bits in the location having the lower memory address. A double precision operand is addressed by specifying the 12-bit address of the high-order half of the operand.



EAE Mode "B" Bit Asignments

The Greater Than Flag (GTF) is activated during execution of mode B instructions. The GTF may be manipulated by means of processor IOT instructions. It is conditionally loaded by the SAM instruction, and it receives the content of MQ11 during right shift operations.

KE8-E Mode B Instructions

MNEMONIC	OCTAL CODE	FUNCTION
ASC	7403	Accumulator to Step Count. The low-order 5 bits of the AC (AC7-11) are loaded into the step counter, and the AC is then cleared.
MUY	7405	Multiply. The next word in memory is taken as the address of a multiplier. If extended memory is installed, the multiplier is obtained from the current data field. Multiplication occurs as described above, and program execution resumes at the location following the address of the multiplier.
DVI	7407	Divide. The next word in memory is taken as the address of a divisor. If extended memory is installed, the divisor is obtained from the current data field. Division occurs as described above, and program execution resumes at the location following the address of the divisor. If divide overflow occurs, the link is set. If divide overflow does not occur, the link is cleared.
NMI	7411	Normalize. The content of the AC and MQ is normalized as described above. This command must not be microprogrammed with any other instruction.
SHL	7413	Shift Left. The content of the AC and MQ is shifted left as described above. The number of shifts performed is equal to the content of the 5 low-order bits (bits 7-11) of the next location in memory. A shift count of zero is legal, and leaves the link, AC, and MQ registers unchanged. Program execution resumes at the location following the shift count.
ASR	7415	Arithmetic Shift Right. The link is loaded from AC0 and remains unaltered for the remainder of the operation. The content of the AC and MQ is then shifted right as described above. The number of shifts performed is equal to the content of the 5 low-order bits (bits 7-11) of the next location in memory. A shift count of zero is legal, and loads the link from AC0 but leaves the AC and MQ registers unchanged. Bits shifted out of MQ11 are shifted into the GTF, to facilitate round-off operations. Pro-

KE8-E Mode B Instructions (Cont.)

MNEMONIC	OCTAL CODE	FUNCTION
		gram execution resumes at the location following the shift count.
LSR	7417	Logical Shift Right. The link is cleared and remains unaltered for the remainder of the operation. The content of the AC and MQ is shifted right as described above. The number of shifts performed is equal to the content of the 5 low-order bits (bits 7-11) of the next instruction in memory. A shift count of zero is legal, and clears the link without changing the AC or MQ registers. Bits shifted out of MQ11 are shifted into the GTF to facilitate round-off operations. Program execution resumes at the location following the shift count.
SCA	7441	Step Counter OR with AC. The content of the step counter is combined with the content of the low-order 5 bits of the AC (AC7-11) by a bitwise logical OR operation, and the result is loaded into AC7-11. AC0-6 remain unchanged.
SCA CLA	7641	Step Counter to AC. The content of the step counter is loaded into AC7-11. AC0-6 are cleared. This instruction is a microprogrammed combination of SCA and CLA.
SAM	7457	Subtract AC from MQ. The content of the AC is subtracted from the content of the MQ in two's complement arithmetic. The result is loaded into the AC. The MQ remains unchanged. If a borrow is propagated from the most significant bit, the link is set. Otherwise, the link is cleared. Hence, the link is set if, and only if, the original content of the AC was less than or equal to the content of the MQ. The GTF is helpful when comparing signed numbers. It is set if the signed number in the MQ is greater than or equal to the original signed number in the AC, and cleared otherwise.
DAD	7443	Double Precision Add. The double precision word addressed by the next memory location is added to the previous content of the AC and MQ registers. If extended memory is installed, the double-precision word is obtained from the

KE8-E Mode B Instructions (Cont.)

MNEMONIC	OCTAL CODE	FUNCTION
		current data field. If there is a carry from the most significant bit, the link is set. If there is no carry, the link is cleared. Program execution resumes at the memory location following the operand address. This instruction may be microprogrammed with the CAM instruction to produce a double precision load (DLD) instruction.
DST	7445	Double Precision Store. The content of the MQ and AC is stored at the double precision location addressed by the next memory location. If extended memory is installed, the storage location will be in the current data field. The AC, MQ and link remain unchanged. Program execution resumes at the location following the operand address. This instruction may be microprogrammed with the CAM instruction to produce a Double Precision Deposit Zero (DDZ) instruction.
DPIC	7573	Double Precision Increment. The double precision constant "one" is added to the double precision number in the AC and MQ by two's complement arithmetic. The high-order carry (or lack thereof) is propagated into the link. This instruction requires that the MQL and MQA bits be set to function as defined.
DCM	7575	Double Precision Complement. The content of the AC and MQ, considered as a 24-bit number, is complemented and incremented. This has the effect of replacing the content of the AC and MQ with its two's complement. The high-order carry (or lack thereof) is propagated into the link. This instruction requires that the MQL and MQA bits be set in order to function as defined.
DPSZ	7451	Double Precision Skip if Zero. The double precision number contained in the AC and MQ is tested. If all bits are zero, the PC is incremented to skip the next sequential instruction. If any bit is 1, the next instruction is executed.

The chart below lists the differences between Mode A and Mode B Instructions.

INSTRUCTION	MODE A	MODE B
MUY	The next location holds the multiplexer.	The next location holds the address of the multiplier.
DVI	The next location holds the divisor.	The next location holds the address of the divisor.
SHL, LSR, ASR	The next location holds one less than the number of shifts.	The next location holds the number of shifts. (A shift of zero places is legal.)
	On Right Shifts, MQ11 is lost.	On Right Shifts, MQ11 is shifted into the greater than flag.

REDUNDANCY CHECK OPTION, KG8-EA

DESCRIPTION

The KG8-EA redundancy check option is designed to complement the DP8-EA synchronous interface by providing parity generation and checking facilities. Vertical redundancy checks (VRC), longitudinal redundancy checks (LRC), and cyclic redundancy checks (CRC) can be performed by this option. The cyclic redundancy check is industry compatible CRC-12 and CRC-16.

The KG8-EA operates directly with the PDP-8/A from program-controlled instructions. Thus, when not used with the communications equipment, it can be used with other devices. The KG8-EA consists of MSI logic packaged on a single quad module which plugs into the Omnibus. All control functions and character options are programmable. The primary purpose of the KG8-EA parity option is to reduce processor overhead for data communications applications where character parity (VRC) and/or block check character (BCC) accumulation (LRC or CRC) are required for error detection. The types of parity generation or checks that the KG8-EA can perform are defined below:

Vertical Redundancy—Parity is on a character basis where one bit position of each character is reserved for the parity bit. Odd parity (odd number of binary ones) is generated by this option; however, capabilities are provided for checking odd or even parity.

Longitudinal Redundancy—This type is a BCC accumulation over a block of message characters; that is, the LRC is an accumulated EXCLUSIVE OR of all character bits (including parity bits) in a message. This method is more reliable than the VRC in detecting errors. A system may use both the LRC and VRC to increase the probability of detecting errors. Both the transmitting and receiving stations must compute the BCC; at the end of the message block, the BCC accumulations and the transmitted BCC are compared at the receiving station. If they are equal, the message is assumed to be without error.

Cyclic Redundancy—As implemented in this option, cyclic redundancy is industry compatible for CRC BCC accumulation (CRC 16/12).

The CRC checksum is the remainder derived from dividing the numerical value of the message by a constant. The division is performed serially, the quotient is discarded, and the remainder is stored. Both the transmitting and receiving stations must compute the BCC accumulation. At the end of each message block, the BCC accumulation is sent to the receiving station for comparison with the receive station's accumulation. If the two are equal, the message is assumed to be without error. CRC and VRC operations can be combined to increase the probability of error detection.

SPECIFICATIONS

Vertical Redundancy Check (VRC):	Tests and generates odd parity for up to eight-bit characters. Parity bit is either right-justified (AC11) or left-justified (AC04).
Longitudinal Redundancy:	Computes or compares BCC accumulation for 6, 7, 8, 12 or 16-bit characters. Two bytes required for LRC 16.
Cyclic Redundancy Check (CRC):	Industry compatible for CRC-12 and CRC-16. Division constants used are: $X^{12} + X^{11} + X^3 + X^2 + X^1$ for CRC 12, and $X^{16} + X^{15} + X^2 + 1$ for CRC-16 where X is modulus 2.
Fetch Cycle Time:	1.5 μs

PROGRAMMING

The instructions associated with the KG8-EA option are as follows:

MNEMONIC	OCTAL CODE	FUNCTION
RCCV	6XX3	Transfers character in AC4—11 to KG8-EA parity register. Clears AC and generates odd vertical parity. Result is then jam-transferred to AC with parity bit in AC04 or AC11 as defined by the program.
RCTV	6XX0	Checks parity of character in AC4—11. For odd parity, the next instruction is skipped if parity of character is odd.
RCGB	6XX4	Generates an LRC or CRC block check character (BCC). The LRC can be generated from 6, 7, 8, 12, or 16 (two six-bit bytes) bit characters, while CRC 12/16 can be computed from 6 to 8-bit characters, respectively. BCC verification: The transmitted BCC is compared to the Receive BCC by treating the BCC as part of the overall accumulation. In doing so, the receive BCC generator will go to zero if there were no errors in transmission. This instruction also provides the functions defined for RCCV and RCTV if the appropriate control bits are included (see RCLC instruction).
RLRL	6XX2	Jam-transfers the 6, 7, 8, or 12 LSBs of BCC accumulation to the AC (right-justified). The quantity of bits transferred to the AC is de-

MNEMONIC	OCTAL CODE	FUNCTION
		pendent on the BCC length selected with the RCLC instruction. The LSB of each byte is also right-justified.
RCRH	6XX1	Jam-transfers the 8 MSBs of BCC accumulation to AC (right-justified). The instruction is used for the 16-bit BCC. The LSB of each byte is also right-justified.
RCCB	6XX6	Clears the 16-bit BCC register.
RCLC	6XX5	Jam-transfers content of AC to redundancy control register to define the operation as follows: AC05 = 1: CRC BCC 0: LRC BCC AC 6 7 8 0 0 0 = 16-bit BCC 0 0 1 = 12-bit BCC 0 1 0 = 8-bit BCC 0 1 1 = 7-bit BCC 1 0 0 = 6-bit BCC AC 9 = 0: Generated parity to AC4 = 1: Generated parity to AC11 AC10 = 1: An RCGB instruction also causes a RCCV instruction sequence. The BCC accumulation will be computed with the corrected character parity. AC11 = 1: An RCGB instruction also causes a RCTV instruction sequence.
RCTC	6XX7	This instruction can only be implemented by grounding test point DA1 on the module. RCTC causes a single clock pulse to the registers, permitting single step testing of LRC and CRC operations.

XX = device code

ASYNCHRONOUS SERIAL LINE INTERFACE KL8-A

DESCRIPTION

The KL8-A Asynchronous Serial Line Interface, used with the PDP-8/A minicomputer, contains four separate channels that may be interfaced to either 20 mA current loop or EIA RS-232-C type devices. Three lines have partial modem control and one line provides full modem control. Each line may operate at any one of 15 different baud rates.

Asynchronous Serial Transmission

All four channels on the KL8-A have either 20 mA or EIA input/output capability.

The EIA level converters meet or exceed the electrical specifications of EIA specification RS-232-C. The EIA circuits will perform to the RS-232-C and CCITT specification when connected to a maximum of 50 feet of cable, not including the cable between the KL8-A and the H326 Patch Panel, if used.

For 20mA lines, the maximum cable length is dependent on dc resistance, cable type and baud rate. The 20mA lines will support cable lengths up to 500 feet using standard DIGITAL cables at the baud rates offered on the KL8-A.

The Silo

Included in the KL8-A is a 32-character buffer called a silo. Serial data received by the KL8-A is transferred to the top of the silo. Words previously loaded into the silo propagate down the silo to empty locations. The program may either empty the silo with a series of MSRD (read) instructions, storing the data for future interpretation by a service routine, or unload and service each word one at a time.

Maintenance Features

The control board and UARTs (universal asynchronous receiver/transmitter) are self-tested each time bit 0 in a control word is set. Also, jumpers are available on the H326 Patch Panel to test the complete EIA/20mA circuit.

Modem Control Capability

Lines 0, 1, 2 provide for partial modem control. Features are skip on ring; data terminal ready; request to send (permanently enabled); read the status of ring and read the status of carrier.

Line 3 provides for full modem control. Features include all partial modem features plus change of phase detection on carrier; clear to send; secondary receive; programmable secondary transmit; request to send; data terminal ready; speed select.

The H326 Patch Panel contains jumpers for line 3 to assert the busy signal; assert the data ready signal; connect secondary receive to normal ready signal; connect secondary receive to normal or to Bell 202

secondary receive; connect secondary receive to restraint on Bell 811B modems; connect secondary transmit to normal or to Bell 202 secondary transmit.

Modems Supported
The following Bell-series modems and their equivalents are supported by the KL8-A:

Bell series 103A and F
113
202C and D
103E, G and H*
811B*

* Fully supported with optional H326 Patch Panel.

Interfacing Accessories
To facilitate interfacing of the many different devices that can be used with the KL8-A, a full range of cables and a connecting panel are available. These enable the user to purchase the arrangement best suiting individual needs.

BC08W—A 25-foot cable that connects to the KL8-A on one end (via a 50-pin connector) and terminates with four EIA plugs (25-pin). Each EIA connection is labeled for the particular KL8-A channel (0, 1, 2, 3).

BC08X—A six-foot cable that connects to the KL8-A on one end (via a 50-pin connector) and terminates with four 20mA plugs (8-pin). This cable will not interface with Teletypes.

BC08Z—Connects to the KL8-A on one end (via a 50-pin connector) and terminates with one 25-foot EIA connection and three six-foot non-Teletype 20mA connections.

The EIA line uses channel 3 of the KL8-A. The three non-Teletype 20mA lines use channels 0, 1 and 2 of the KL8-A.

BC08Y—A ten-foot cable that connects the KL8-A to the H326 Patch Panel.

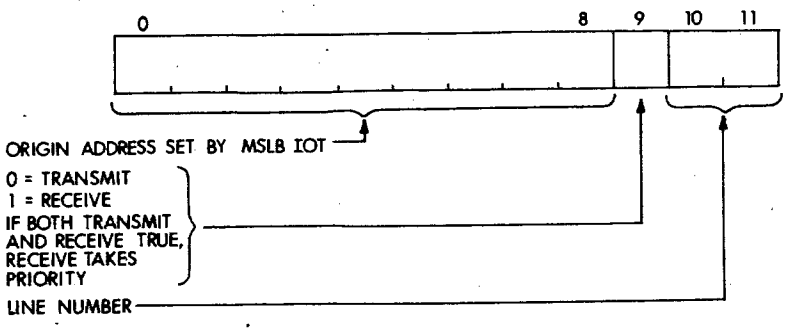
H326 Patch Panel—The H326 Patch Panel can serve as a central distribution point for up to eight lines.

It occupies a rack-mountable space of 5.25-inches high by 19-inches wide by 4.5-inches deep. The H326 contains eight EIA connectors and eight 20mA connectors. In order to interface ASR/KSR Model 33 or 35 Teletypes to the KL8-A, the H326 must be used. Neither the KL8-A or the H326 support the low-speed Teletype papertape reader. The H326, in conjunction with the KL8-A, must be used to support Bell 811B modem.

PROGRAMMING

INSTRUCTION MNEMONIC	OCTAL CODE	OPERATION
MSIE	6XX0	Load interrupt enable from AC11; 1 = set, 0 = clear.
MSAB	6XX1	If device flag (transmit or receive) is true, branch to service routine and load AC 10 and 11 with line number. Then clear transmit flag if set.
MSRA	6XX2	Read status A into AC 0-11.
MSSR	6XX3	Skip on "ring," then clear if set (for lines 0, 1 and 2).
MSXD	6XX4	Transmit data.
MSRD	6XX5	Receive data; clear receiver flag if silo empty.
MSCT	6XX6	Unconditionally clear transmit flag.
—	6XX7	Spare.
MSCD	6XY0	Clear device, flags, silos, control and status words.
MSLC	6XY1	Load control word from AC 0-4.
MSLB	6XY2	Load branch address from AC 0-8.
MSSB	6XY3	Skip on "ring," clear "ring" if set (line 3 only).
MSSS	6XY4	Skip on "clear to send," clear "clear to send" if set (line 3 only).
MSSC	6XY5	Skip on "carrier," clear "carrier" if set. (Line 3 only).
MSSV	6XY6	Skip on "secondary receive," clear "secondary receive" if set. (Line 3.)
MSRB	6XY7	Read status B into AC 0-11.

Branch Address Register



SPECIFICATIONS

Number of start bits: 1

Number of data bits: 5, 6, 7 or 8 (jumper-selectable per channel).

Number of stop bits: 1, 1½ (when 5 bits/character selected), or 2 (jumper-selectable per channel).

Parity/No Parity: Jumper-selectable per channel.

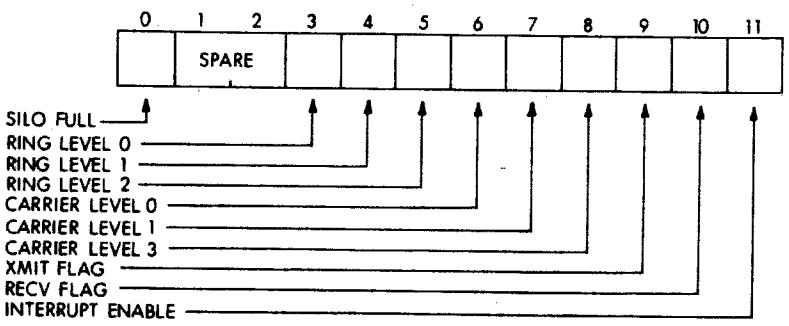
Even/Odd Parity: Jumper-selectable per channel.

Device codes: 00-77 jumper selectable. The option uses two device codes, the first being even; the second is always the next sequential number.

Module is shipped with following settings:

IOT code—40
Stop bits—2
Character length—8
Parity—disabled
Branch addresses—8

Status A Register



Status A Register Bits

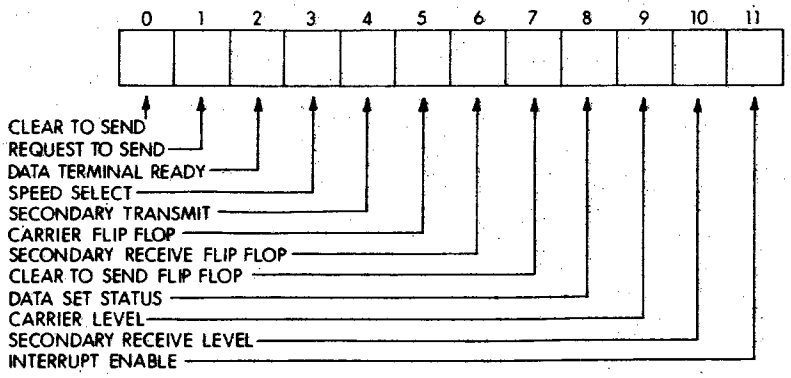
Status A Register Bit Description

AC BIT	DESCRIPTION	FUNCTIONS
0	SILO FULL	SILO FULL is a one when there are 32 words in the FIFO register.
1 and 2		Not used.
3	RING LEVEL 0	RING LEVEL 0 is a one when a ring is received on line 0.
4	RING LEVEL 1	RING LEVEL 1 is a one when a ring is received on line 1.
5	RING LEVEL 2	RING LEVEL 2 is a one when a ring is received on line 2.

Status A Register Bit Description (Cont.)

AC BIT	DESCRIPTION	FUNCTION
6	CARRIER LEVEL 0	CARRIER LEVEL 0 is a one when an incoming carrier is present on line 0.
7	CARRIER LEVEL 1	CARRIER LEVEL 1 is a one when an incoming carrier is present on line 1.
8	CARRIER LEVEL 3	CARRIER LEVEL 3 is a one when an incoming carrier is present on line 3.
9	XMIT FLAG	The XMIT FLAG is set (1) when one or more of the UART's are ready for a new transmit word.
10	RECV FLAG	The RECV FLAG is set (1) when the CHARACTER flag is set. The CHARACTER flag sets when there is one or more words in the FIFO register.
11	INTERRUPT ENABLED	INTERRUPT ENABLED is a one when the interrupt flip-flop has been set by the MSIE instruction.

Status B Register



Status B Bit Assignments For Line 3

Status B Register Bit Description

AC BIT	DESCRIPTION	FUNCTION
0	CLEAR TO SEND	CLEAR TO SEND is asserted to a one when the data set is ready to transmit data.

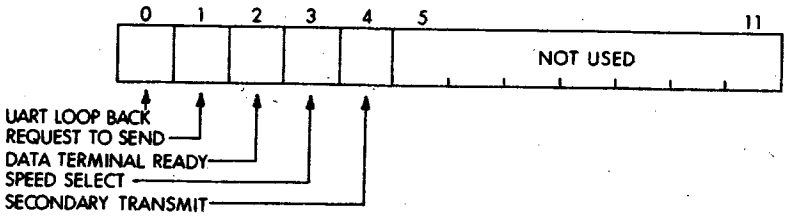
Status B Register Bit Description (Cont.)

AC BIT	DESCRIPTION	FUNCTION
1	REQUEST TO SEND	REQUEST TO SEND is asserted to a one to condition the data communications device for a transmit operation.
2	DATA TERMINAL READY	DATA TERMINAL READY is asserted to a one to indicate that the local data communication equipment is connected to a communication channel (not in test or talk modes), the equipment has completed (where applicable) any timing functions required to complete the call, and the transmission of any answer tone is complete.
3	SPEED SELECT	SPEED SELECT is asserted to a one when the highest signaling rate has been selected in the data communication equipment. The equipment must contain the circuitry to select between two signaling rates if this feature is used.
4	SECONDARY TRANSMIT	SECONDARY TRANSMIT is asserted to a one if the secondary transmit channel (if there is one) has been selected for transmit operations.
5	CARRIER	The CARRIER flip-flop is set (1) when the data communications equipment is receiving a suitable signal from the communications line.
6	SECONDARY RECEIVE	The SECONDARY RECEIVE flip-flop is set (1) if the secondary receive channel has been selected for receiving data.
7	CLEAR TO SEND	The CLEAR TO SEND flip-flop is set (1) if the communication equipment is ready to transmit data.
8	DATA SET STATUS	The DATA SET STATUS flip-flop is set (1) if the following are true: 1. The data communications equipment is connected to a communications channel.

Status B Register Bit Description (Cont.)

AC BIT	DESCRIPTION	FUNCTION
		2. The data communications equipment is not in test or talk mode. 3. The data communications equipment has completed where applicable a. Any timing functions required to complete a call b. The transmission of any answer tone of which the duration is determined by the equipment.
9	CARRIER LEVEL	CARRIER LEVEL is asserted (1) when the data communication equipment is receiving a signal which meets its stability criteria.
10	SECONDARY RECEIVE LEVEL	The SECONDARY RECEIVE LEVEL line is asserted (1) for circuit assurance or to interrupt the flow of data in the primary channel.
11	INTERRUPT ENABLE	INTERRUPT ENABLE is set (1) when the program executes the MSIE instructions and loads a one from AC11 to enable an interrupt request.

Control Word



Control Word For Line 3

Control Word For Line 3 Bits

AC BIT	DESCRIPTION	FUNCTION
0	UART LOOP BACK	UART LOOP BACK is used during maintenance operations to enable

Control Word For Line 3 Bits

AC BIT	DESCRIPTION	FUNCTION
		serial data out of the UART to be fed back as serial data into the UART for all four lines. This allows the transmit and receive logic to be checked while the KL8-A is not connected to a device.
1	REQUEST TO SEND	REQUEST TO SEND is set to one to assert the RQST TO SEND signal to the modem or data set on line 3. This signal is permanently enabled on all lines except line 3.
2	DATA TERMINAL READY	DATA TERMINAL READY on line 3 is asserted low to indicate that the line data communication equipment is connected to a channel (not in a talk mode, or test mode), the equipment has completed (where applicable) any timing functions required to complete the call, and the transmission of any answer tone is complete.
3	SPEED SELECT	SPEED SELECT on line 3 is set to one to activate the signal rate selection circuitry in the modem and select the highest signaling rate if the modem is equipped with this circuitry.
4	SECONDARY TRANSMIT	SECONDARY TRANSMIT on line 3 is set to a one to activate a secondary channel in the modem for transmission of data.

Baud Rates

Switch-selectable for each channel, both send and receive, 50, 75, 110, 134.5, 150, 300, 600, 1200, 1800, 2000, 2400, 3600, 4800, 7200 and 9600.

Power Requirements

+5V	−15V	+15V
2.5A	425mA	90mA

(All four channels being used.)

For each 20mA channel not connected, the +5 and −15 voltages decrease by 40mA each. Maximum of four KL8-As per system.

Temperature Requirements
5°C(41°F) to 50°C(122°F).

Relative Humidity
10% to 90%.

Physical Size
One hex-size module fits into one Omnibus slot.

Example of KL8-A Interrupt Handler Programming

```
/SET UP KL8-A IOT SYMBOLS
/1ST KL8-A USES DEVICE CODES 40 & 41
/
MSLB=6412          /LOAD BRANCH ADDR (AC 0-8)
MSAB=6401          /ASSERT BRANCH ADDR
/
/
*0
        0
        JMP12      /JUMP TO SKIP
        SERV       /CHAIN SERVICE ROUTINE
/
/INTERRUPT SERVICE ROUTINE
/
SERV,   SPF        /TEST POWER FAIL
        SKP
        JMP PFAIL  /GO TO PF ROUTINE
        MSAB       /ASSERT BRANCH ADDRESS
        IOTX       /NEXT DEVICE FLAG TEST
        SKP
        JMP NEXTX  /SERVICE THIS DEVICE
        ....       /REMAINDER OF SKIP
        ....       /CHAIN FOLLOWS
/
*200
/
/INITIALIZE ROUTINE—APART FROM
/OTHER HOUSEKEEPING, THE BRANCH
/ADDRESS FOR THE KL8-A MSAB
/IOT SHOULD BE SET UP NOW
/
        CLA CLL
        TAD (3600  /SET UP START OF
        MSLB       /BRANCH ADDRESS
        ....
        ....
```

```
/
*3600
/
/TABLE OF JUMPS TO KL8-A SERVICE ROUTINES
/
        JMP SRVTR0  /SERV TRANSMIT LINE #0
        JMP SRVTR1  /SERV TRANSMIT LINE #1
        JMP SRVTR2  /SERV TRANMIST LINE #2
        JMP SRVTR3  /SERV TRANSMIT LINE #3
        JMP SRVRV0  /SERV RECEIVE LINE #0
        JMP SRVRV1  /SERV RECEIVE LINE #1
        JMP SRVRV2  /SERV RECEIVE LINE #2
        JMP SRVRV3  /SERV RECEIVE LINE #3
/
/REMAINDER OF PROGRAM
```

ASYNCHRONOUS SERIAL LINE INTERFACE, KL8-JA

DESCRIPTION

The KL8-JA asynchronous serial line interface is used with the PDP-8/A family of minicomputers. It provides full duplex, double-buffered data operations to devices with 20mA current loop or EIA RS-232-C compatibility.

FEATURES

- Low price
- EIA or 20mA current loop compatible
- Switch-selectable device codes
- Switch-selectable baud rates
- Double buffered
- Hardware-generated null characters

SPECIFICATIONS

Number of start bits:	1
Number of data bits:	5, 6, 7, or 8 (jumper selectable)
Number of stop bits:	1 or 2 (jumper selectable)
Parity/no parity:	jumper selectable
Odd/even parity:	jumper selectable
Device codes:	00—77 (switch selectable).
Error status word:	jumper selectable
Reader control:	for LT33 teletypewriter operation

Baud Rates (Switch-selectable)

Common transmit-receive baud rates available

110	1200
150	2400
300	4800
600	9600

Split speed: Receive rate of 150 baud.

Transmit rate of 300, 600, 1200, 2400, 4800 or 9600 baud.

Error Status Word

Installation of the SWD jumper causes the following error checks to be made upon received data:

Parity Error

Framing Error—illegal length character received

Overrun Error—a character previously received by the interface was not transferred to the CPU and another character was received on top of it.

Hardware-Generated Filler Characters
Four null characters (jumper selectable) are provided. They are generated upon transmision of a line feed character. This feature permits the use of certain terminals without special programming.

Data Leads
Data leads are provided for either EIA level or 20mA current loop operation.

Power Requirements (DC)

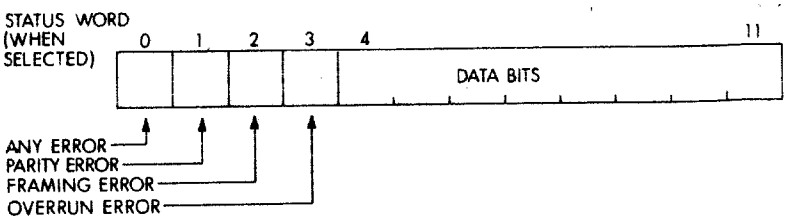
+5V	−15V	+15V
1.1A	0.1A	0.05A

Quad Slots
One quad slot is required per KL8-JA.

Cable (not included)
BC05M-2C—2-foot cables for 20mA current loop operation.

BC01V-25—25-foot cable for EIA operation.

NOTE
Whenever a KL8-M option is used with the KL8-JA, no additional cables are required. One BC05C-25 cable is included with the KL8-M.



KL8-JA Data and Status Word

PROGRAMMING

MNEMONIC	OCTAL CODE	FUNCTION
KCF	6XX0	Clear keyboard flag.
KSF	6XX1	Skip if keyboard flag = 1.
KCC	6XX2	Clear keyboard flag and set reader run. Clear the receiver flag, the AC, and enable the reader.
KRS	6XX4	Read keyboard statically.

MNEMONIC	OCTAL CODE	FUNCTION
		Performs inclusive OR of the receiver register and the AC, leaving the result in the AC.
KIE	6XX5-AC11	Set/clear interrupt enable.
		Load AC bit 11 into the interrupt enable flip-flop. (1) = enable, (0) = disable.
KSE	6XX5-AC10	Set/clear status enable.
		Load AC bit 10 into status enable flip-flop. (1) = enable, (0) = disable. With SWD jumper installed, the status enable flip-flop set causes the status word to be loaded into AC bits 0 through 3, along with the received character when KRS or KRB instructions are executed.
KRB	6XX6	Read keyboard buffer dynamically.
		Performs the combined operations of KCC and KRS.
TFL	6YY0	Set teleprinter flag.
		Set transmit flag.
TSF	6YY1	Skip if teleprinted flag = 1.
TCF	6YY2	Clear teleprinter flag.
		Clear transmit flag.
TPC	6YY4	Load teleprinter and print.
		The least significant bits of the AC are transferred to a data-holding register and then transmitted. The transmit flag is not cleared by this instruction.
SPI	6YY5	Skip on teleprinter interrupt. The next sequential instruction is skipped if the transmit or receive flag is set and the interrupt enable flip-flop is set.
TLS	6YY6	Print character.
		Combination of TCF and TPC performed.

AUTOMATIC ANSWERING DEVICE, KL8-M

DESCRIPTION

The KL8-M, Automatic Answering Device, working under program control through the KL8-JA, provides "auto answer," "carrier detect," "clear to send," and "ring detect" functions as well as a secondary transmit and receive channel on a bit basis. The KL8-M provides control for "data terminal ready," and "request to send" functions. All of the previous functions conform to EIA RS-232-C and CCITT specifications. The KL8-M will accommodate Bell 103A/E/F/G/H, 202 C/D and 113B or equivalent type modems.

SPECIFICATIONS

Quad Slots

One quad slot is required per KL8-M.

Interrupt Functions

Interrupt is generated under the following conditions:

Carrier phase shift
Ring indicator
Clear-to-send phase shift
Secondary-receive phase shift

Power Requirements (DC)

+5 V	−15 V	+15 V
0.4 A	0.037 A	0.04 A

Cables

All necessary jumper and modem cables are supplied with the KL8-M.

PROGRAMMING

MNEMONIC	OCTAL CODE	FUNCTION
MCCI	6XX0	Initializes the interface. It sets all modem control signals to the EIA/CCITT control OFF state (mark hold).
MCLC	6XX1	Transfers the contents of AC00–AC03 to the control register.
MCST	6XX2	Transfers the contents of AC04 to the secondary transmit circuit of the modem.
MCRF	6XX3	Causes a skip if the ring flag is set. Also clears the ring flip-flop. The ring flag is set on the leading edge of the ring signal.
MCSS	6XX4	Causes a skip if the clear-to-send flag is set. It also clears the flag.

MNEMONIC	OCTAL CODE	FUNCTION
MCSC	6XX5	Causes a skip if the carrier flag is set. It also clears the flag.
MCSR	6XX6	Causes a skip if the secondary-receive flag is set. It also clears the flag.
MCRS	6XX7	Clears the AC and transfers the contents of the modem control status register to the AC.

Status and Control Word

*AC00	ENABLE—Interrupt circuitry enabled.
*AC01	REQUEST TO SEND—Request to send is being generated (CA).
*AC02	DATA TERMINAL READY—Machine is ready to receive data (circuit CD).
*AC03	SPEED SELECT—Indicates the state of CH/CI circuit.

* Indicates control word as well as status word.

AC04	SECONDARY TRANSMIT STATE—Indicates the state of the secondary-transmit circuit (SBA).
AC05	CARRIER STATE—Indicates the state of the carrier interrupt circuit.
AC06	SECONDARY RECEIVE STATE—Indicates the state of the secondary-receive data interrupt circuit.
AC07	CLEAR-TO-SEND STATE—Indicates the state of the clear-to-send interrupt circuit.
AC08	DATA SET STATUS—Indicates condition of the data set status circuit (CC).
AC09	CARRIER STATE—Indicates state of carrier line.
AC10	SECONDARY-RECEIVE STATE—Indicates state of secondary-receive line.
AC11	CLEAR-TO-SEND STATE—Indicates the state of the clear-to-send line.

EXTENDED OPTION MODULE, KM8-AA

DESCRIPTION

The KM8-AA extended option module (M8317) is a hex size (15 x 8½ in.) (38.10 x 21.59 cm) module which comprises four PDP-8/A options:

- Memory extension
- Timeshare control
- Power fail and auto restart
- 128 location bootstrap loader

MEMORY EXTENSION AND TIMESHARE OPTION

The memory extension and timeshare option provides the user with two capabilities. The memory extension portion extends the addressing capabilities of the machine from 4096 words up to 32,768 words; the timeshare portion enables the computer to operate in either the normal manner (executive mode) or User Mode. User Mode enables the machine to function in a timesharing environment in which a user program is prevented from disturbing or interfering with another user program. These options are packaged on the M8317 module that plugs into the Omnibus.

MEMORY EXTENSION

The functional circuit elements that make up the memory extension control perform the following:

Instruction Field Register (IF)—The IF is a three-bit register that serves as an extension of the PC. The contents of the IF determine the field from which all instructions are taken and the field from which operands are taken in directly-addressed Memory Reference Instructions. Depressing the console LXA switch transfers Entry Register bits 6 through 8 into the IF register. During a JMP or JMS instruction, the IF is set by a transfer of information from the Instruction Buffer register. If the intion is a JMP, the IF is updated at the conclusion of the instruction. If the instruction is a JMS, the IF is updated just before the execute portion of the instruction saving the return address in the new field. When a program interrupt occurs, the contents of the IF is automatically stored in bits 0 through 2 of the Save Field register for restoration to the IF from the instruction buffer register at the conclusion of the program interrupt subroutine.

Data Field Register (DF)—This three-bit register determines the memory field from which operands are taken in directly-addressed Memory Reference Instructions. Depressing the console LXA switch transfers the ENTRY register bits 9 through 11 into the DF register. During a CDF instruction, the DF register is loaded from MD6–8 to establish a new data field. When a program interrupt occurs, the contents of the DF are automatically stored in bits 3–5 of the Save Field register. The DF is set by a transfer of information from Save Field register bits 3 through

5 by the RMF instruction. This action is required to restore the Data Field at the conclusion of the program interrupt subroutine.

Instruction Buffer Register (IB)—The IB serves as a three-bit input buffer for the Instruction Field register. All field number transfers into the Instruction Field register, except transfers from the operator's console switches, are made through the Instruction Buffer. The IB is set by depressing the console LXA switch in the same manner as the instruction field register. A CIF microinstruction loads the IB with the programmed field. An RMF microinstruction transfers Save Field register bits 0 through 2 into the IB to restore the instruction field that existed before a program interrupt.

Save Field Register (SF)—When a program interrupt occurs, this seven-bit register is loaded from the User Field flip-flop, and the IF and DF registers. The SF register is loaded during the cycle in which the program count is stored at address 0000 of the JMS instruction forced by a program interrupt request; then the Instruction Field, Instruction Buffer, and Data Field registers are cleared. An RMF instruction can be given immediately before exit from the program interrupt subroutine to restore the Instruction Field and Data Field by transferring the SF into the IB and the DF registers. (Also, see GTF and RTF instructions.)

PROGRAMMING

Instructions associated with the extended memory portion of the KM8-A option are as follows:

MNEMONIC	OCTAL CODE	FUNCTION
GTF	6004	Loads the contents of the SF register into AC5–11. Other AC bits are loaded with information from the CPU, i.e., link, interrupt bus, interrupt on.
RTF	6005	Loads the User Buffer flip-flop, the Instruction Buffer register, and the Data Field register with the contents of AC bits 5, 6–8, and 9–11, and inhibits processor interrupts until the next JMP or JMS instruction. At the conclusion of the JMP or JMS instruction, the contents of the User Buffer flip-flop and the Instruction Buffer register are transferred into the User Field flip-flop and the Instruction Field register, respectively. AC0 is loaded into the Link. The Interrupt On flip-flop in the CPU is unconditionally set by this instruction.
CDF	62N1	Loads the Data Field register with the program-selected field number (N = 0 to 7). All subsequent memory requests for indirect operands are automatically switchd to that Data Field.

MNEMONIC	OCTAL CODE	FUNCTION
CIF	62N2	Loads the Instruction Buffer register with the program-selected field number (N = 0 to 7) and inhibits processor interrupts until the next JMP or JMS instruction. At the conclusion of a JMP instruction or at the beginning of the executive portion of a JMS instruction, the contents of the Instruction Buffer register is transferred into the Instruction Field register.
CDF, CIF	62N3	Performs the combination of CDF and CIF operations.
RDF	6214	ORs the contents of the Data Field register into bits 6–8 of the AC. All other bits of the AC are unaffected.
RIF	6224	ORs the contents of the Instruction Field register into bits 6–8 of the AC. All other bits of the AC are unaffected.
RIB	6234	ORs the contents of the Save Field register (which is loaded from the instruction and Data Field during a program interrupt) into bits 6–8 and 9–11 of the AC, respectively. Thus, AC 6–11 contains the Instruction and Data Fields that were in use before the last program interrupt. AC 5 is loaded by the timeshare bit of the Save Field register. All other bits of the AC are unaffected.
RMF	6244	Restores the contents of the Save Field register (which is loaded from the instruction and Data Field during a program interrupt) into the Instruction Buffer, the Data Field register, and the User Buffer (if timeshare option is enabled). This command is used upon exit from the program interrupt subroutine.

Instructions and data are accessed from the currently assigned instruction and data fields, which may be in the same or different memory fields. When indirect memory references are executed, the operand address refers first to the instruction field to obtain an effective address, which, in turn, refers to a location in the currently assigned data field. All instructions and operands are obtained from the field designated by the contents of the instruction field register, except indirectly addressed operands, which are specified by the contents of the data field register. In other words, the DF is effective only in the EXECUTE cycle that directly follows the DEFER cycle of a memory reference instruction.

INDIRECT (BIT 3)	PAGE BIT (BIT 4)	FIELD IN IF	FIELD IN DF	EFFECTIVE ADDRESS
0	0	m	n	The operand is in page 0 of field m at the address specified by bits 5 through 11.
0	1	m	n	The operand is in the current page of field m at the page address specified by bits 5 through 11 of the instruction.
1	0	m	n	The absolute address of the operand in field n is taken from the contents of field m. Page 0 at the page address is specified by bits 5 through 11 of the instruction.
1	1	m	n	The absolute address of the operand in field n is taken from the contents of field m current page, at the page address specified by bits 5 through 11 of the instruction .

Each field of extended memory contains eight auto-index registers in addresses 10_8 through 17_8. For example, assume that a program in field 2 is running (IF = 2) and using operands in field 1 (DF = 1) when the instruction TAD I 10 is fetched. The Defer cycle is entered (bit 3 = 1), and the contents of location 10 in field 2 are read, incremented, and rewritten. If address 10 in field 2 originally contained 4321, it now contains 4322. In the execute cycle, the operand is fetched from location 4322 of field 1. Program control is transferred between memory fields by the CIF instruction. The instruction does not change the instruction field directly, because this would make it impossible to execute the next sequential instruction; instead, it loads the new instruction field in the IB for automatic transfer into the IF when either a JMP or JMS instruction is executed. The DF is unaffected by the JMP and JMS instructions.

The 12-bit program counter is set in the normal manner and, because the IF is an extension on the most significant end of the PC, the program sequence resumes in the new memory field following a JMP or JMS. Interrupts are inhibited after the CIF instruction until a JMP or JMS is executed.

NOTE

The IF is not incremented if the PC goes from 7777 to 0000. This feature protects the user from accidentally entering a nonexistent field.

To call a subroutine that is out of the current field, the data field register is set to indicate the field of the calling JMS, which establishes the location of the operands as well as the identity of the return field. The instruction field is set to the field of the starting address of the subroutine.

When a program interrupt occurs, the current instruction and data field numbers are automatically stored in the 7-bit save field register; then the IF, IB, and DF are cleared. The PC content is stored in location 0000 of field 0 and program control advances to location 0001 of field 0. At the end of the program interrupt subroutine, the RMF instruction restores the IF, IB, and DF from the contents of the SF. Alternatively, the GTF and RTF instructions may be used to handle the save field and link information.

Timeshare Control

The Timeshare portion of the KM8-A module operates in two modes defined by the user flag (UF) flip-flop. When the UF flip-flop is in the logic 1 state, operation is in the user mode and a user program is running. When the UF flip-flop is in the logic 0 state, operation is in the executive mode and the timesharing system's monitor is in control of the central processor. Four instructions (CINT, SINT, CUF, and SUF) are used by the timesharing system's monitor in the executive mode and are never used by a user program. If a user program attempted to use one of these instructions, execution of the instruction would be blocked (see next paragraph). The timeshare option adds the necessary hardware to the PDP-8/A to implement these instructions.

In executive mode, the computer operates normally. When the computer is operated in user mode, operation is normal except for IOT, HLT, LAS, and OSR instructions. When one of these instructions is encountered, the hardware inhibits the normal instruction sequence (other than rewriting the instruction in memory), and generates an interrupt at the end of the current memory cycle. Any interrupt returns timeshare control to executive mode. The timesharing system's monitor program then analyzes the source of interrupt and takes appropriate action.

The timeshare option requires at least 8K of memory; thus, it is packaged with the memory extension option. A switch on the KM8-A module is used to enable the timeshare function.

PROGRAMMING

Instructions associated with the timeshare portion of the KM8-A are as follows:

MNEMONIC	OCTAL CODE	FUNCTION
CINT	6204	Clears the user interrupt flip-flop.
SINT	6254	When the user interrupt flip-flop is set the next sequential instruction is skipped.
CUF	6264	Clears the user buffer flip-flop.
SUF	6274	Sets user buffer flip-flop and inhibits processor interrupts until the next JMP or JMS instruction. At the conclusion of either of these instructions, the content of the user buffer flip-flop is transferred into the user flag flip-flop.

NOTE

If the machine is stopped while in user mode, the user flag (UF) is cleared by operating the extended address load key (LXA).

Power Fail/Auto Restart

The power supply monitors the AC line voltage and detects when the AC line voltage has fallen below a certain level, (93 V $\pm$ 3% for 117 Vac operation), and generates a logic signal AC LOW. This signal causes logic in the Power Fail/Auto Restart portion of the extended option board to interrupt the program, which takes the necessary action as the AC power is going away. In MOS memory systems the automatic switch-over to a battery supply, that allows the system to continue operation for an additional 45 seconds, will occur. If power is restored during this time the system will automatically switch back to the regular power supply. In core memory systems, the program should store all active registers (AC, MQ, etc.) and stop the system when a low AC voltage is detected. The computer will restart and the program can restore the active registers when AC power goes above 105 Vac (117 Vac operation).

FEATURES

Restart Addresses: One of four restart addresses may be selected, as shown below.

Auto-Restart Select Switch Settings

RESTART ADDRESS	S2-2	S2-3	S2-4
0	OFF	OFF	OFF
200	OFF	ON	OFF
2000	ON	OFF	OFF
4200	ON	ON	OFF

Auto Restart
If auto restart is enabled, the PDP-8/A starts automatically when power is applied. This allows the user to apply power remotely and start the system without going to the PDP-8/A. (Auto-start on the CPU must be disabled.)

PROGRAMMING
The IOT instructions used with the power fail and auto restart option are as follows:

MNEMONIC	OCTAL CODE	FUNCTION
SPL	6102	Skip if the AC low flag is set. After detecting an AC LOW condition, the flag will remain set for testing by the SPL instruction until AC goes above 105 V. The CAL instruction (see next instruction) merely removes the AC LOW interrupt from the Omnibus.
CAL	6103	Clear the AC LOW interrupt.
SBE	6101	Skip if the battery empty flag is set.

The device code for this option is 10.

Bootstrap Loader
The bootstrap loader on the M8317 module provides the logic to deposit into read/write memory one of several programs that is contained in two ROMs on the M8317 module. These programs provide the necessary instructions to load programs from paper tape, disk, magnetic tape, etc., and to start the program at the specified location. The user may purchase ROM chips from DIGITAL and load his own programs in the ROM chips.

There are 128 locations available.

The bootstrap loader may be activated by depressing the BOOT switch on the operator's panel or the optional programmers console or from the transition of AC Low from low to high. Three switches (S1-6, S1-7, and S1-8) on the KM8 module (M8317) select the appropriate signal (AC Low, SW Low) to active the desired bootstrap procedure (see accompanying table).

The bootstrap can also be started when the computer is turned on. This feature is enabled by switch S1-4 (see accompanying Table) on the KM8 module and allows the computer to be started remotely when the PDP-8/A is used as a peripheral.

The following tables show the bootstrap select switch settings and the bootstrap/auto restart switch settings.

Bootstrap Select Switch Settings

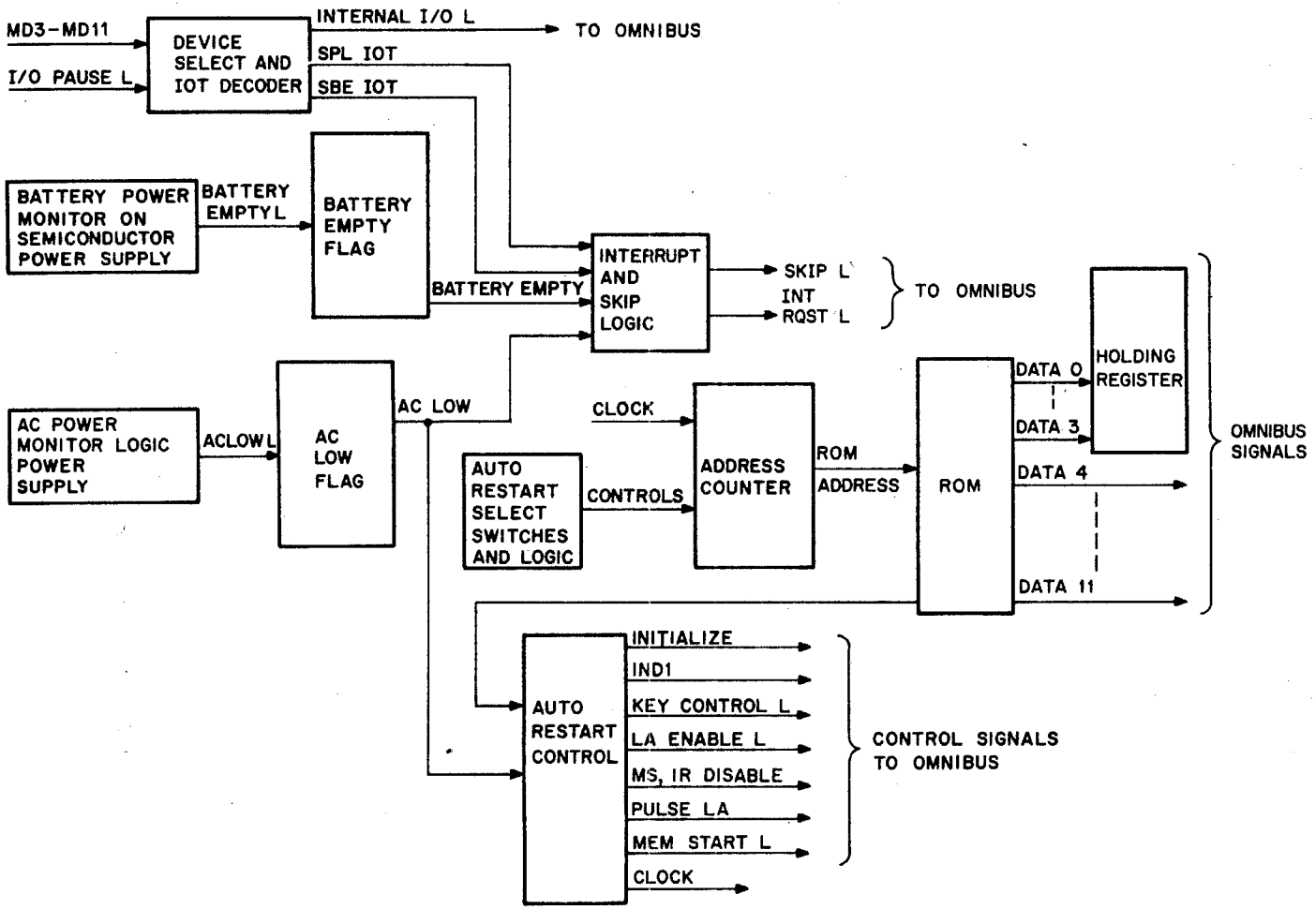
PROGRAM	S2-5	S2-6	S2-7	S2-8	S1-1	S1-2	S1-3	MEMORY ADDRESS
*HI-LO RIM	ON	ON	ON	OFF	ON	ON	ON	7737
*RK8-E	ON	OFF	ON	OFF	ON	OFF	ON	0024
*TC08	ON	OFF	OFF	ON	OFF	ON	ON	7613
*RF08/DF32D	OFF	ON	ON	ON	ON	OFF	OFF	7750
*TA8-E	OFF	ON	ON	OFF	ON	OFF	OFF	4000

* May only be used with 4K of Read/Write Memory in field 0.

Bootstrap/Auto Restart Switch Settings

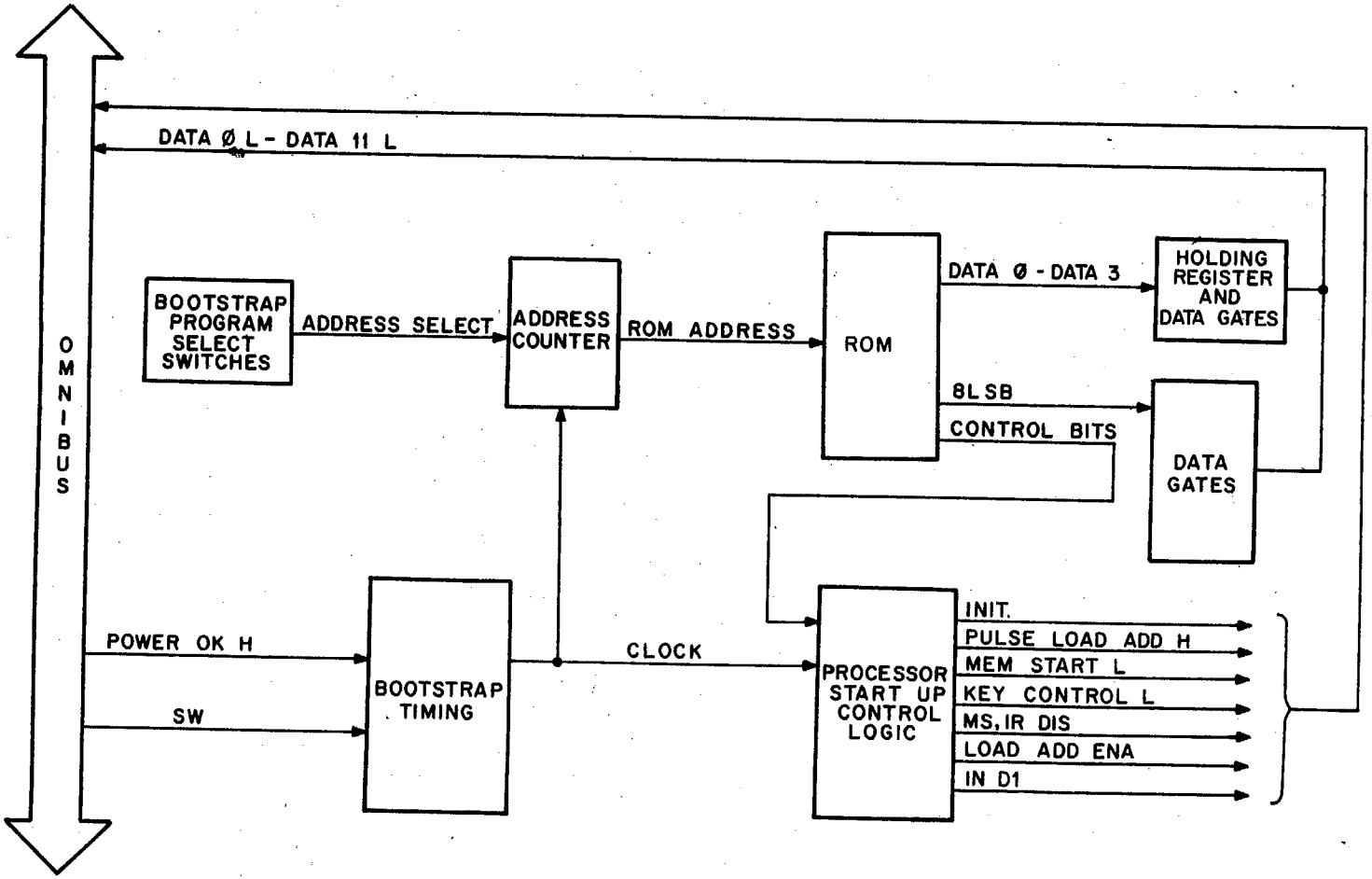
FEATURE	START SWITCH OR ACTIVATING SIGNAL	SWITCHES S1-6	S1-7	S1-8
Bootstrap Enabled And Auto Restart Disabled	BOOT Key	OFF	OFF	ON
Bootstrap Enabled And Auto Restart Enabled	BOOT Key or AC OK *	ON	ON	ON
Bootstrap Disabled And Auto Restart Enabled	AC OK *	ON	ON	OFF
Bootstrap Enabled And Auto Restart Disabled	AC OK *	ON	OFF	OFF
Bootstrap Enabled And Auto Restart Disabled	AC OK * or BOOT Key	ON	OFF	ON
Bootstrap And Auto Restart Disabled		OFF	OFF	OFF
		S2-1		
Time Share Enabled		OFF		
Time Share Disabled		ON		
		S1-4		
Bootstrap Activated In Run Or Stopped State		OFF		
Bootstrap Activated in Stopped State Only		ON		
Not used		S1-5		

* Starts if power voltage becomes adequate.



Power Fail and Auto Restart Block Diagram

KM8



Bootstrap Loader Block Diagram

DECPRINTER I MEDIUM SPEED PRINTER, LA8

DESCRIPTION

The LA8 DECprinter I is a medium-speed printer with an extensive array of standard features which makes it the most cost competitive in the industry. DECprinter I extends the field-proven technology of the LA36 DECwriter into applications demanding higher speed capabilities.

DECprinter I has many operator features which enhance its ease of use. Included are a forms-length switch (which sets the top-of-form to any of 11 common lengths) and paper-out switch and alarm. Also featured are quiet operation, variable forms adjustment, variable forms width, and multipart forms capability.

Operation

Seven solenoid-driven wires form the characters by scanning the page from left to right. The machine prints a line at a time and automatically performs a carriage return upon receipt of a CR, LF, or FF command.

Power-Up

Upon power-up, the DECprinter I is initialized to execute incoming data. The head moves to the left and stops at column 1.

Carriage System

The carriage system transports the head along the horizontal axis of the machine, provides accurate character positioning and character placement and provides printhead adjustment for clean impressions on a variety of forms.

The carriage is controlled by a servo system which assures accurate dot placement. The servo operates in the forward direction at 18 inches per second and has a carriage return time of less than 275 ms.

Ribbon Feed System

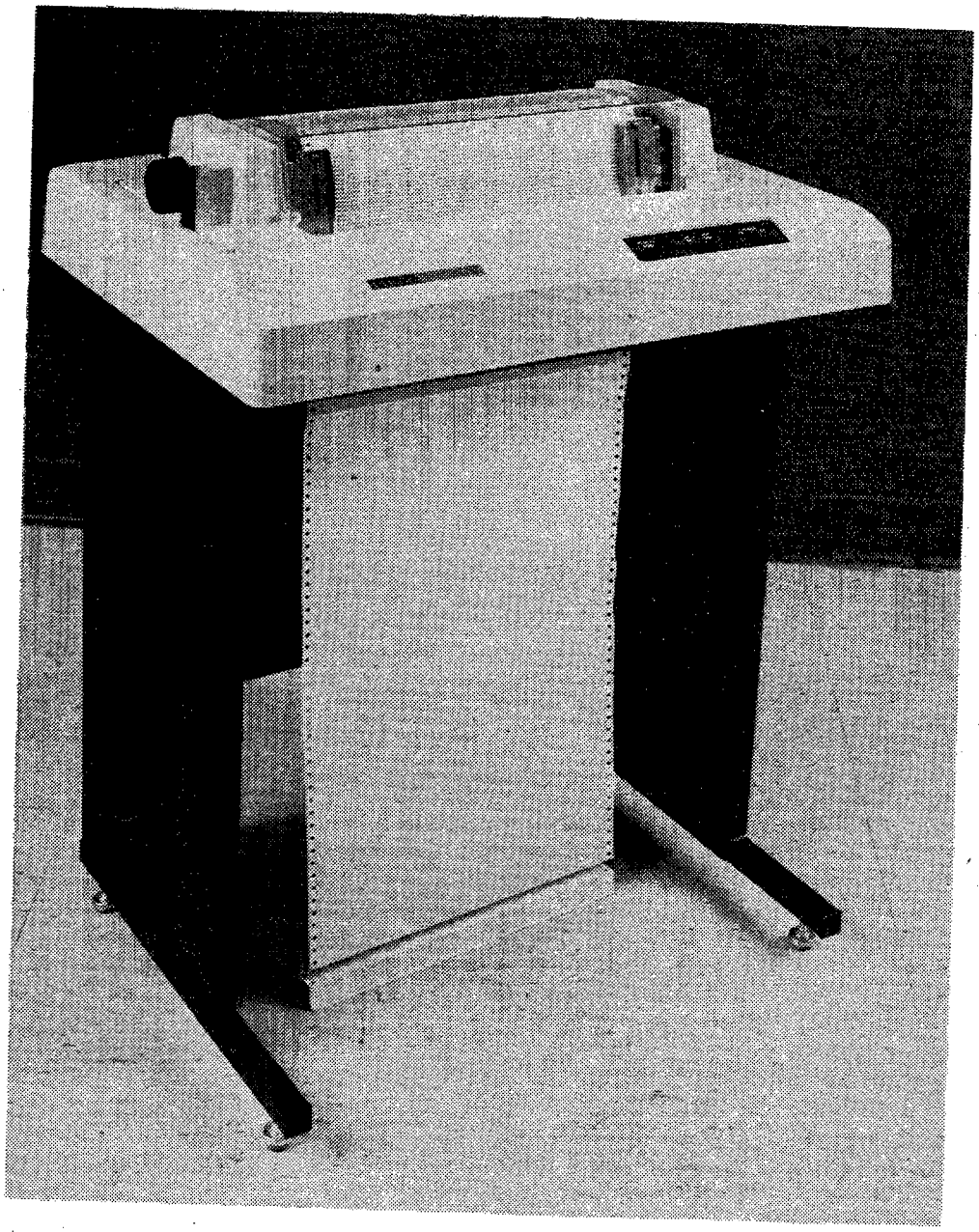
The ribbon feed system is driven by the carriage motion only when the carriage is moving from left to right. This prevents ribbon smudging when the DECprinter is not printing.

Paper Feed System

The paper feed system is a stepping-motor-driven tractor feed. The tractor design provides 3-to-4-pin engagement of the form and a flat bed for control and positive feeding of multipart forms. Paper may be fine-positioned vertically by pushing the line feed knob inward and rotating it in the direction desired.

Operator Controls

POWER ON-OFF	Applies and removes AC power to entire machine.
LINE/OFF LINE	Enables or disables communications.
HEAD OF FORM	Form feeds to the next top-of-form or single line feeds, if LENGTH OF FORM switch is set in single-line position.



LA8 DECprinter I Medium Speed Printer

LENGTH OF FORM	Selects any of 11 forms lengths.
SET VFU	Used in conjunction with Length-of-Form switch to reset forms length.
SELF TEST	Will run test pattern locally if set in this position.
Forms Thickness Adjustment	Located on right side of printhead carriage. Selects proper gap for 1-through-6-part form. Approximately 1 detent for each part.

Right and Left Tractor Adjustment	Thumb screw may be loosened to allow movement of both tractors for various forms widths.
Fine Vertical Tractor Release	Line-feed knob may be depressed inward and rotated in the appropriate direction for precise location of printing with respect to vertical zones.

DKC8-AA/LA180 Line Printer Interface

The General Purpose Parallel I/O on the DCK8-AA I/O option module may be used as an interface for the LA180 line printer with cable BC80A.

PROGRAMMING

The instruction set for the General Purpose Parallel I/O when used with the LA180 is as follows:

OCTAL CODE	MNEMONIC	OPERATION
6570	DBST	Skip on demand Clear if set
6574	DBTD	Load contents of AC0-11 into Xmit buffer
6575	DBSE	Set Interrupt Enable to a one
6576	DBCE	Set Interrupt Enable to a zero

The data is loaded in bits 5-11 of the central processor AC. The data is then complemented to produce the appropriate character and is then transferred to the Xmit buffer in the general purpose parallel I/O. For example, normally 101 octal will produce the letter "A" on the printer. However, to print the letter "A", 076 (complement of 101) must be loaded into the DCK8-AA Xmit buffer, by IOT 6574 from AC bits 5 thru 11. The AC is not cleared by this IOT.

If the DKC8-AA, is used as the LA180 line printer interface, there will be no interrupts for "BUSY", "FAULT", "ONLINE" as the absence of DEMAND from the LA180 will indicate that the printer is "off-line". The DKC8-AA assumes that the LA180 is on line with power.

FEATURES

180 characters per second
Parallel interface
Accommodates 6-part form (.120 inches maximum thickness)
Handles variable-width forms, 3 through 14-7/8 inches wide 132-column print.
128-character ASCII upper/lower case set
7 × 7 dot matrix
Backspace capability
Quiet operation
Excellent character readability
Fine vertical adjustment for accurate forms placement

Paper-out switch
Paper-out override
Switch-selectable forms length (11 lengths)
Drives 100-foot cable

OPTIONS

Paper stacking tray
Casters for rear of cabinet
RS-232-C serial interface
Special character sets
Auto line feed

SPECIFICATIONS

Printing Speed:	180 characters/second
Number of Columns:	132
Printing Characters:	96 characters (ASCII set)
Printing Type:	Impact 7 × 7 dot matrix
Vertical Spacing:	6 lines/inch
Horizontal Spacing:	10 characters/inch
Paper Type:	3 through 14-7/8 inches wide, continuous business form, original and 5 copies; .020 inch (.5 mm) maximum pack thickness
Single-line skip:	32ms
Slew speed:	7.5 inches/second; 45 lines/second
Mechanical Mounting:	1 free-standing unit
Size:	33.2 inches (84.3 cm) high × 27.5 inches (69.9 cm) wide × 20 inches (50.8 cm) deep.
Weight:	102 lbs (46.3 kg)
Power Input Current:	3.0A at 115 Vac 1.5A at 230 Vac
Heat Dissipation:	400 W printing 200 W non printing
Environment Operating Temperature:	10°C to 40°C (50° to 104°F)
Relative humidity:	19% to 90% noncondensing, maximum wet bulb 29°C

Ribbon	DIGITAL-specified nylon fabric, spool assembly, (.5 inches wide × 60 yards long) Order #3612153

LA8 Interface Module:

Size	Quad Module
Input current	1.5A at +5V.

LA8 CONFIGURATIONS

DESIG-NATION	EQUIPMENT	OPERATING VOLTAGE	OPERATING FREQUENCY	CABLE LENGTH
LA8-PA	LA180 and controller for PDP-8,	115V	60Hz	25 ft
LA8-PB	LA180 and controller for PDP-8,	230V	60Hz	25 ft
LA8-PC	LA180 and controller for PDP-8,	115V	50Hz	25 ft
LA8-PD	LA180 and controller for PDP-8,	230V	50Hz	25 ft

If the DKC8-AA module is used as the LA180 interface, an LA180 and a BC80A cable is required. The cable comes in lengths of 25 feet and 100 feet.

PROGRAMMING

The normal LA8 device code is 66, but can be changed to 65.
The instruction set is as follows:

MNEMONIC	OCTAL CODE	FUNCTION
PSSF	6660	Set printer flag
PSKF	6661	Skip printer flag
PCLF	6662	Clear printer flag*
PSTB	6664	Load printer buffer
PCIE	6665	Set/Clear interrupt enable**
PCLF, PSTB	6666	Load printer buffer sequence

* cleared by initialize or CAF
** set by initialize or CAF

MECHANICAL

Size:	1 Quad module slot
Input Current:	1.5A at +5V

DECWRITER II PRINTER, LA35

DESCRIPTION

The LA35 DECwriter is a medium-sized, low-cost printer for use as a local or remote printer only. It is capable of handling multipart and multiform line printer paper from 3 to 14-7/8 in. wide and is especially suited for preprinted forms due to its horizontal and vertical positioning capabilities. The LA35 is a receive only version of the LA36 and does not have a keyboard.

SPECIFICATIONS

Printing

Switch selectable: 10, 15, or 30 characters/second throughput
BAUD rates (selectable): 110, 150, and 300 BAUD.

Line Length

132 characters maximum

Spacing

10 characters/in. (horizontal)
6 lines/in. (vertical)

Characters

96 upper/lower case ASCII
7 × 7 dot matrix (0.07 × 0.10 in.)

Paper

Variable width: 3 to 14-7/8 in.
Single-Part:

15 lb paper minimum
Card stock thickness of 0.010 in. maximum

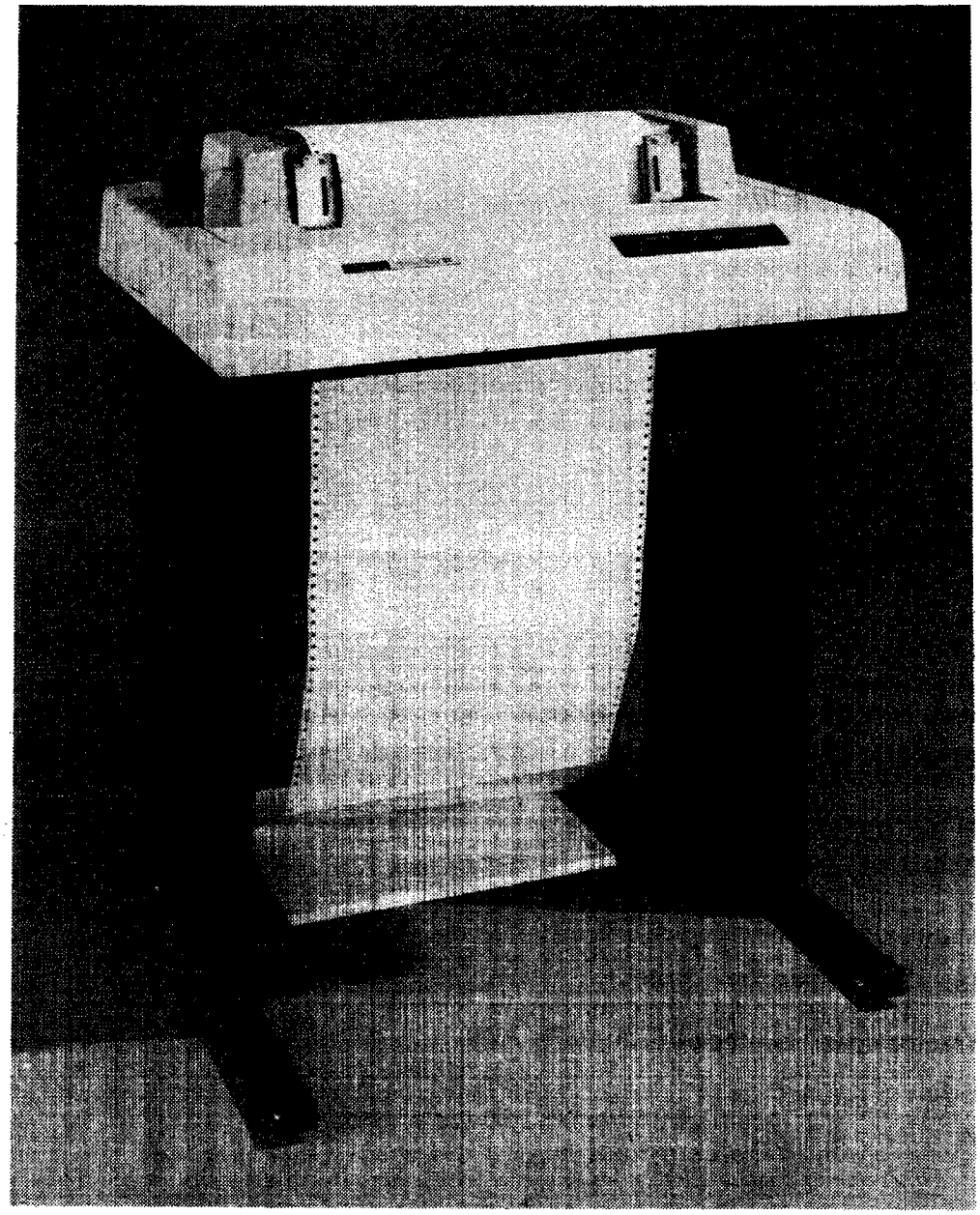
Multipart:

2- to 6-part (see Notes)
Thickness of 0.020 in. maximum

Tractor-drive, pin-feed

NOTES

1. Multipart forms may have only one card part. The card must be the last part.
2. NCR or 3M paper, up to 6-part, must use ribbon on top copy. First surface impact paper is not recommended.
3. Continuous-feed, fan-fold business forms with 3 or 4-prong margin crimps on both margins (multi-part) are recommended. Stapled forms are not recommended and may damage tractors and other areas of the machine. Dot or line glue margins are acceptable (if line is on one margin only). Do not line glue both margins as air will not be able to escape and poor impressions will result.



LA35 DECwriter II Printer

Interface
20 mA current loop (standard) or EIA/CCITT (optional).

Ribbon
DIGITAL-specified nylon fabric (Part No. 36-10558)
Spool assembly: 0.5 in. wide × 40 yd long

Power
90-132 Vac or 180-264 Vac
50 or 60 Hz ± 1 Hz
300 W maximum (printing)
160 W maximum (idle)

Temperature
Operating
10° to 40°C (50° to 104°F), noncondensing

Nonoperating
—40° to 66°C (—40° to 151°F) noncondensing

Relative Humidity
Operating

10 to 90% with a maximum wet bulb temperature of 28°C (82°F) and a minimum dew point of 2°C (36°F), noncondensing

Nonoperating
5 to 95%

Dimensions
27.5 in. wide (69.9 cm.)
33.5 in. high (85.1 cm.)
21.7 in. deep (55.1 cm.)

Weight
97 lb (44 kg.)

Interface
DKC8-AA General Purpose Parallel I/O, KL8A Serial Line Unit, and KL8-JA asynchronous Data Interface

OPTIONS
The basic LA35 DECwriter can be expanded to provide the user with a number of functional options for receiving and handling data. These functional options are described in the following table.

LA35 Options

OPTION	NAME	DESCRIPTION
LAXX-LB	Expander Option Mount	The Expander Option Mounting Kit includes the logic, cables, and mounting hardware required to expand the LA35 to include options LAXX-LA, LAXX-KV, LAXX-KW, LAXX-KX, LAXX-KY, and LAXX-PK.
LAXX-PK	APL/ASCII Dual Character Set	This option provides an APL alternate character set for use with the standard character set in the LA35.

LA35 Options (Cont)

OPTION	NAME	DESCRIPTION
LAXX-LA	Auto LF After CR	The LAXX-LA option causes the printer to execute a line feed after each received carriage return code.
LAXX-KV	Top of Forms Control	Controls mounted under the top cover provide the operator with a method of selecting the length of the paper to be used. After the desired setting is selected and the paper is lined up for proper vertical alignment, the operator presses the SET TOP OF FORM switch so that the internal logic will be preset to this paper length as defined by the operator.
LAXX-KW	Selective Addressing	The Selective Addressing option allows the LA35 to operate with other terminals on a single data communications channel.
LAXX-KX	Auto Answer Back and Auto LF Options	The Automatic Answer Back option allows the terminal to transmit a preprogramed message of 20 characters (maximum). The message is initiated upon receipt of the ENQ control code from another device. The LAXX-KX may be configured to incorporate the features of the Automatic Line Feed option (LAXX-LA).
LAXX-KY	Forms Control, Vertical and Horizontal Tabs	The Forms and Tabbing option enables the printer to set horizontal and vertical tab positions via the system software. This option also incorporates features of the Top of Forms option (LAXX-KV) and operates in the same manner.
LAXX-LG	EIA/CCITT Interface	The LAXX-LG EIA/CCITT interface provides the user with an RS-232-C interface which includes a 9-ft cable terminated with a standard EIA connector. This option replaces the previously offered interface, LAXX-KG.
LAXX-KJ	Compressed Print Option	The compressed print option is a mechanical option that provides the LA35 with the ability to print 132 columns on a form 8½ in. wide.

LA35 Options (Cont)

OPTION	NAME	DESCRIPTION
LAXX-LC	TTL to CCITT (V28) Converter and Modem Protector	The TTL to CCITT (V28) Converter and Modem Protector is a BPO DATEL services interface that meets the requirements of CCITT (V28), with BPO-required modem protection circuitry.
LAXX-LH	Current Loop Cable	20 mA current loop with Mate-N-Lok.
LAXX-LK	Current Loop Cable	20 mA current loop with 4-pin plug for DEC-10.

LA35 DECwriter MODEL VARIATIONS

The LA35 variations and associated model numbers are listed below.

LA35-CE	90-132 V, 60 Hz
LA35-CF	180-264 V, 60 Hz
LA35-CH	90-132 V, 50 Hz
LA35-CJ	180-264 V, 50 Hz

LA35 Jumper Configurations

LA35 OPTIONAL CURRENT LOOP CONFIGURATION

The LA35 is normally configured for passive operation. To modify this configuration for active operation, jumpers on the logic board must be changed.

LA35 PARITY

The LA35 is configured with no parity and no parity error printout. To modify this configuration for odd or even parity with or without error printout, jumpers on the logic board must be changed.

LA35 SPEAKER (BELL) VOLUME

The LA35 can be configured for a lower speaker volume by removing a jumper.

DECPRINTER II PRINTER TERMINAL, LA36

DESCRIPTION

The LA36 DECwriter II is a second generation printer terminal which offers quiet, fast, reliable operation and is extremely easy to interface as a remote terminal or local computer I/O device.

The typewriter-style keyboard ensures easy operator adaptation. The 7-wire print head is designed for long life and produces extremely clear character definition.

OPERATION

A printer head containing seven solenoid driven wires forms the characters by scanning the page from left to right.

The carriage system transports the head along the horizontal axis of the machine and provides accurate horizontal positioning for character placement and precise print gap and adjustment for clean impressions on a variety of forms. The carriage is controlled by a servo system for accurate dot placement. The servo operates in the forward direction at 3 and 6 inches per second. The 3 ips speed is the normal mode while the 6 ips speed is used for catch up following a carriage return.

The paper feed system is driven by a stepping motor. The tractor design provides 3 to 4 pins engagement of the form and a flat bed for control and positive feeding of multipart paper. Paper may be fine positioned vertically by pushing the line feed knob inward and rotating it in the direction desired.

OPERATOR CONTROLS

Power On-Off:	Applies and removes ac power to the entire machine
Line/Local:	Selects on-line or local operation.
Baud Rate:	3-position switch selects the baud rate; 110, 150, or 300 baud
Forms thickness adjustment:	Located on right side of print head carriage. Selects proper gap for 1- through 6-part form. Approximately 1 detent for each part.
Right tractor adjustment:	Thumb screw may be loosened to allow movement of right tractor for various forms widths.
Fine vertical tractor release:	Line feed knob may be depressed inward and rotated in the appropriate direction for precise location of printing with respect to vertical zones.

FEATURES

STANDARD

True 30-character per second throughput

Accommodates 6-part form (.020 maximum thickness)

Handles variable width forms; 3 through 14⅞ in. wide

132-column printing; 10 characters per inch horizontal

6 lines per inch vertical spacing

128-character ASCII upper/lower case set

7 x 7 dot matrix

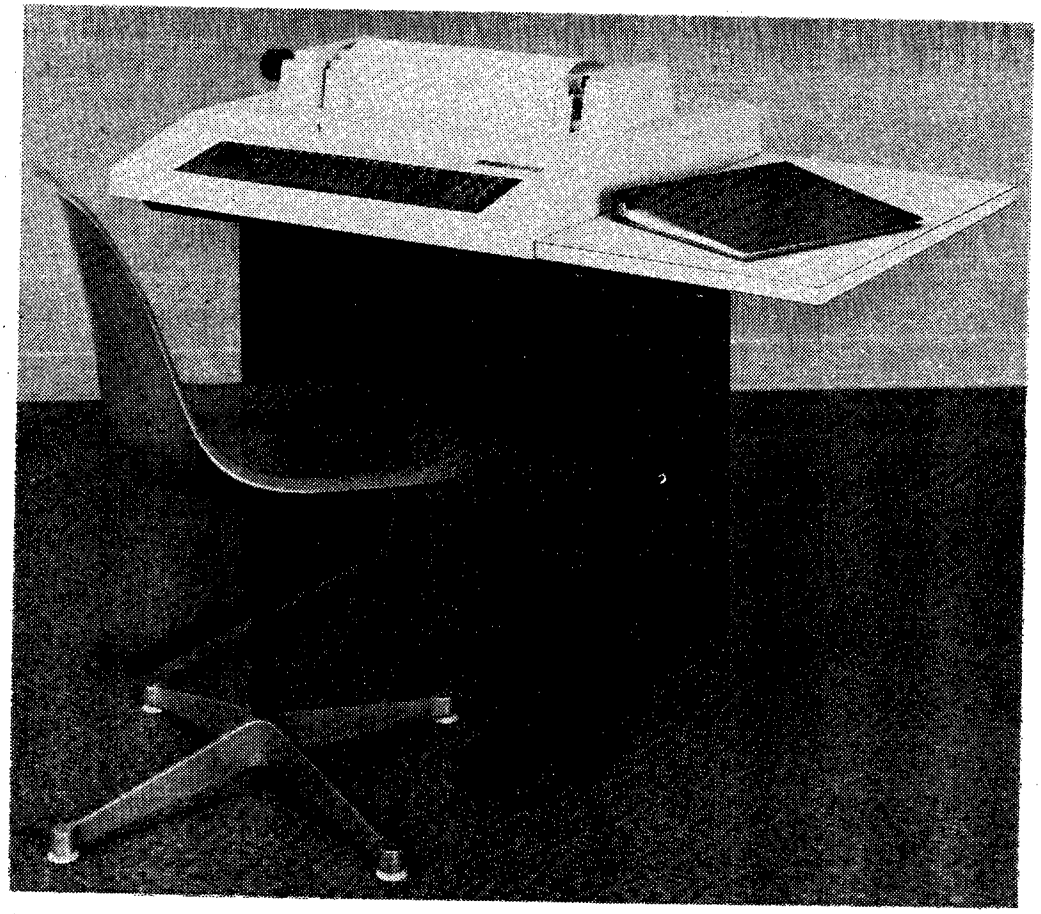
ANSI-standard typewriter-like keyboard

Quiet operation

Excellent character readability

Integrated 20mA current loop interface with jumpers for active and passive modes

Fine vertical adjustment for accurate forms placement



LA-36 DECwriter Printer Terminal

FEATURES

Paper stacking tray

Casters for rear of cabinet

Right and/or left work surface

OPTIONS

(Uses same options as LA35)

SPECIFICATIONS

Printing speed:	30 char/sec, asynchronous
Number of columns:	132
Keyboard characters:	96 or 128 (selectable with internal switch)

PRINTING

Type:	Impact, 7 x 7 dot matrix
Vertical spacing:	6 lines/inch
Horizontal spacing:	10 char/inch

PAPER

Type:	3 to 14⅞ in. wide, continuous form tractor driven, original plus 5 copies (20 mils maximum pack thickness)
Slew speed:	30 lines/sec.

MECHANICAL

Mounting:	1 free-standing unit
Size:	33.2 in. H x 27.5 in. W x 24 in. D (84.3 cm x 69.8 cm x 61 cm)
Weight:	102 lb (46.3 kg.)

POWER

90–132 Vac or 180–264 Vac

Heat dissipation:	300 W Printing 160 W Nonprinting

ENVIRONMENT

Operating temperature:	10° to 40° C (50° to 104° F)
Relative humidity:	10% to 90%

RIBBON

DIGITAL specified nylon fabric, spool assembly 0.5 in. wide x 40 yards. Order #36-10558

CABLE

BC05F-15 cable standard (20 mA current loop operation). Can be extended to 1500 ft.

INTERFACE

KL8-JA Asynchronous Data Interface or SLU on DKC8-AA.

LINE PRINTER, LE8

DESCRIPTION

The LE8 line printer offers the user a low-cost, high-speed, flexible method of printing computer output at a rate dependent upon the option selected. It accepts ASCII characters from the AC, and has adjustable column width to 132 characters. Each character is selected from the set of 64 (or 96) available by means of six-bit or seven-bit binary code. Each code is loaded separately from the computer into the line printer buffer from AC6–11 (or AC5–11), with the least significant bit appearing in AC11. After each code is transferred into the line printer buffer, the line printer DONE flag appears, indicating that the printer is ready to receive the next character. When the line printer buffer is filled, or a control character has been received, the print cycle is initiated. The line feed command and carriage return command are similar to the corresponding commands in the Teletype. The form feed command advances the paper to the top of the page. The printer DONE Flag is set after each of these operations.

OPERATION

There are no operator controls in the control module. The following controls are on the printer:

TOP OF FORM—Advances paper to top-of-form position; disabled in on-line mode

PAPER STEP—Advances paper one line; disabled in on-line mode

ON LINE/OFF LINE—Selects mode of operation for the printer

SPECIFICATIONS

LP05 WA	96 character scientific drum	
LP05 WE	96 character EDP drum	
LP05 VA	64 character scientific drum	
LP05 VE	64 character EDP drum	
Print rate	64 character	300 lines per minute (minimum)
	96 character	230 lines per minute (minimum)

Format	Top-of-form control, single line advance and perforation step over.
Paper feed	One pair of pin-feed tractors for ½-inch hole center, edge-punched paper. Adjustable for any paper width from 4 inches to a maximum width of 14⅞ inches for the 132 columns.
Paper slew speed	20 inches per second (minimum)
Print area	Up to 13.2 inches wide, left justified
Character Spacing	10 characters per inch
Line spacing	6 or 8 lines per inch, operator selectable
Line advance time	40 milliseconds (maximum)

Character synchronization	Variable reluctance pick-offs sense drum position
Printer Power Requirements	90–132 Vac 47–63 Hz. 180–264 Vac 47–63 Hz. 700 watts (max).
Signal cable	25 foot interconnecting signal cable is supplied with system
Paper	
Type	Standard fan-fold, edge punched
Dimensions	4 inches (10.16 cm.) to 14⅞ inches wide (37.78 cm.) (132 column) with 11 inches between folds
Weight	printer 330 lbs. ((150 kg.) shipping 355 lbs. (161 kg.)
(single copy)	15 pound bond (minimum)
(multi copy)	12 bound bond with single-shot carbon for up to six parts
Ribbon	
type	inked roll
width	9 inches (80 column); 15 inches x 25 yards. 0.004 inch thick nylon

PROGRAMMING

The IOT instructions for the line printer are:

MNEMONIC	OCTAL CODE	FUNCTION
PSKF	6661	Senses the content of the line printer DONE flag; if it contains a binary 1, the contents of the PC are incremented by one so that the next sequential instruction is skipped.
PCLF	6662	Clears the Line Printer DONE Flag.
PSKE	6663	Senses the content of the Line Printer Error Flag; if it contains a binary 1, indicating that an error (drum gate open, out of paper, excessive temperature) has been detected, the contents of the PC are incremented by one so that the next sequential instruction is skipped.
PSTB	6664	Loads the character into the print buffer, and prints if the buffer is full, or if the character was a control instruction. This instruction does not clear the AC.

MNEMONIC	OCTAL CODE	FUNCTION
PSIE	6665	Sets the interrupt enable (IE) flip-flop to a one, permitting the Printer DONE Flag to request a program interrupt.
(PCLF, PSTB)	6666	This is a microprogram combination of PCLF and PSTB.
PCIE	6667	Clears the interrupt enable flip-flop.

READER/PUNCH, PC8-E

DESCRIPTION

The PC8-E is available in two versions: the rack mountable version (PC8-EA) and the table top version (PC8-EB).

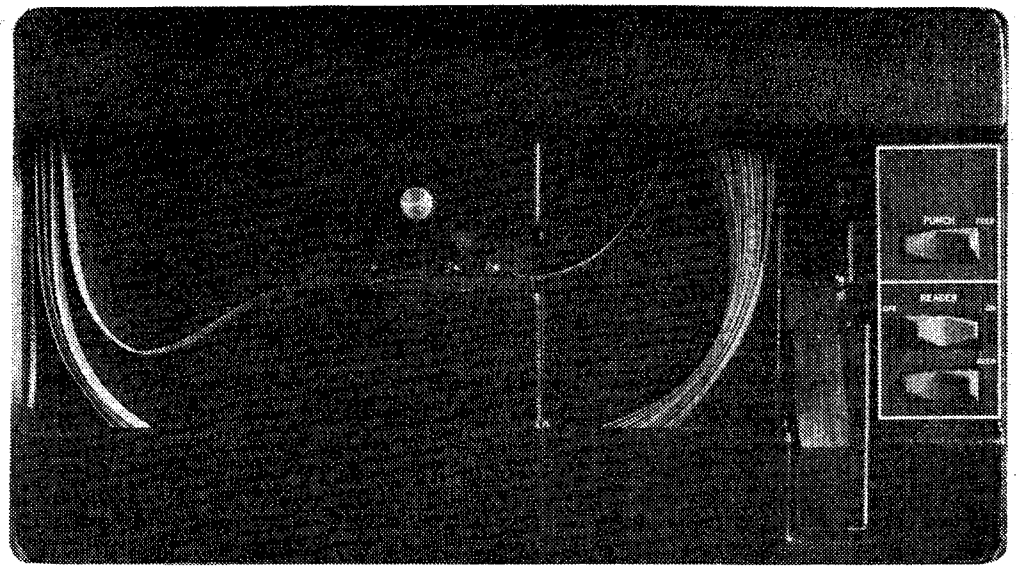
The PC8-E consists of a reader and punch mounted on the same chassis and a control unit which plugs into the Omnibus and controls the action of the reader/punch from program instructions. All connections between the control unit and reader/punch are made using two BC08-K cables.

The reader portion of the PC8-E operates in the same manner as the PR8-E. The punch portion responds to the following additional instructions:

MNEMONIC	OCTAL CODE	FUNCTION
RPE	6010	Sets the reader/punch interrupt enable flip-flop so that an interrupt request can be generated when punch or reader flag is set.
PCE	6020	Clear the reader/punch enable flip-flop so that interrupt requests cannot be generated.
PSF	6021	Senses the punch flag; if it contains a binary one, increments the PC by one so that the next sequential instruction is skipped.
PCF	6022	Clears the punch flag in preparation for receiving a new character from the computer.
PDC	6024	Transfers the eight-bit character in AC4–11 into the PB, then punches that character. The instruction does not clear the punch flag or the PB.
PLS	6026	Clears the punch flag, transfers the contents of AC4–11 into the punch buffer, punches the character in the PB on tape, and sets the punch flag when the operation is completed.

A program sequence loop to punch a character when the punch buffer is free can be written as follows:

```
FREE, PSF          /SKIP IF PUNCH FLAG = 1
      JMP FREE     /JUMP BACK & TEST FLAG AGAIN
      PLS          /CLEAR PUNCH FLAG & PB, LOAD PB
                   /FROM AC, PUNCH CHARACTER, SET
                   /PUNCH FLAG WHEN DONE
```



PC04 Paper-Tape Reader/Punch

SPECIFICATIONS

Channels	8 data channels plus feedhole
Read Rate (Continuous)	300 characters/second
Read Rate (Start-Stop Mode)	25 characters/second
Punch Rate	50 characters/second
Physical dimensions	Height: 10.5 in. (26.7 cm) Width: 19 in. (48.3 cm) Depth: 15 in. (38.1 cm)
Tape characteristics	Reader: Gray, unoiled, fan-folded* Punch: Oiled or unoiled, fan-folded
Tape tension (in punch)	6 oz, maximum
Voltage requirements	115 Vac ± 10%, 50 or 60 Hz
Power supplies (internal)	Regulated, −15V ± 1V Regulated, +5V ± 0.25V Unregulated, −36V ± 4V
Logic levels	Logic 1 (H): +2.0V, input +2.4V, output Logic 0 (L): +0.8V, input +0.4V, output
Temperature (Operating)	Reader: 55° to 110°F Punch: 55° to 110°F

Temperature (Nonoperating)	Reader: 10° to 150°F Punch: 10° to 150°F
Humidity** (Operating)	Reader: 20 to 95% (w/o condensation) Punch: 20 to 95% (w/o condensation)
Humidity (Nonoperating)	Reader: 5 to 95% (w/o condensation) Punch: 5 to 95% (w/o condensation)

* Tape of up to 12% transmittance may be used. Consult DIGITAL for operation of reader with more transparent tape.

** The humidity specifications are for the reader/punch mechanism. Paper-tape manufacturers' recommendations for operating environment should be followed. Suppliers of paper tape include Digital Equipment Corporation and Carter, Rice, Storrs and Bement.

PAPER TAPE READER, PR8-E

DESCRIPTION

The PR8-E is available in two versions: the rack mounted version (PR8-EA) and the table top version (PR8-EB).

The PR8-E reader senses eight-hole unoiled grey perforated paper tape photo-electrically at a maximum rate of 300 characters per second. The control unit of the PR8-E plugs into the Omnibus and controls the action of the reader from program instructions. All connections between the control unit and the reader are made using a BC08-K cable.

A read operation is initiated by an RFC instruction from the computer. The control unit, in turn, initiates tape movement and sensing of a character, transfers the character to its reader buffer (RB), and sets its device flag to indicate that a character is available for transfer to the computer. The computer senses the reader flag by issuing an RSF instruction, and transfers the character from the RB to AC04 through 11 by issuing an RRB instruction. The RRB instruction also clears the reader flag to ready the unit for another read operation.

The control unit also contains an interrupt enable flip-flop. This flip-flop, controlled by program instructions, determines whether the reader can generate an interrupt request to the program interrupt facility. When set by an RPE instruction or initialize input, this flip-flop enables generation of an interrupt request from the reader flag being set. When cleared by a PCE instruction, this flip-flop inhibits interrupt requests.

PROGRAMMING

Instructions for operating the reader are as follows:

MNEMONIC	OCTAL CODE	FUNCTION
RPE	6010	Sets the reader/punch interrupt enable flip-flop so that an interrupt request can be generated when reader or punch flag is set.
RSF	6011	Senses the reader flag if it is set and increments the PC by one so that the next sequential instruction is skipped.
RRB	6012	ORs the content of the reader buffer into AC4–11 and clears the reader flag. This command does not clear the AC.
RFC	6014	Clears the reader flag, loads one character into the RB from the tape, and sets the reader flag when the RB is full.
RRB, RFC	6016	Combines RRB and RFC. The contents of the reader buffer is ORed into the AC. The flag is

MNEMONIC	OCTAL CODE	FUNCTION
		immediately cleared, and a new character is read from tape into the reader buffer. The flag is then set.
PCE	6020	Clears the reader/punch interrupt enable flip-flop so that interrupt requests cannot be generated.

A program sequence loop to read a character from perforated tape can be written as follows:

```
        RFC          /FETCH CHARACTER FROM TAPE
LOOK,   RSF          /SKIP IF READER FLAG IS SET
        JMP LOOK     /JUMP BACK & TEST FLAG AGAIN
        CLA          /CLEAR AC
        RRB          /LOAD AC FROM RB, CLEAR READER FLAG
```

SPECIFICATIONS

Weight:	32 lbs. (14.5 kg.)
Dimensions: Height	10.5 inches (26.7 cm)
Width	19 inches (48.3 cm)
Depth	10.5 inches (26.7 cm)
Heat Dissipation:	510 BTU/hr.
Current:	1 A nominal
Power Consumption:	0.15 kw.

CARTRIDGE DISK SYSTEM, RK8J-E

DESCRIPTION

The RK8J-E cartridge disk system is another in a series of products which enhances the power, flexibility and economy of DIGITAL's PDP-8 family of minicomputers.

The RK8J-E consists of an RK8-E single-cycle data break control and one RK05-J DECpack drive. The control is made up of three quad modules which plug directly into the PDP-8 Omnibus. The modular design permits computing power to be easily expanded since one RK8-E control can support four RK05-J DECdrives. Additional expansion is available by utilizing a second RK8-E Control on a single computer system. Thus, a total of eight RK05-J DECdrives is permitted. Each RK05-J contains its own head position control and power supply.

The RK05J and RK05F Disk Drives, which comprise the RK05 family of disk drives, are self-contained, random-access data storage devices that are especially well-suited for small or medium-sized computer systems, data acquisition systems, terminals and other storage applications. Operational power for all of these devices is provided by power supplies located within the drive cabinets. Drives in the RK05 family are available in four models ,each of which operates on a different power line.

These compact, lightweight drives use high-density, single-disk, 12-sector or 16-sector cartridges as the storage medium. The cartridge used in the RK05J Disk Drive is removable; the cartridge used in the RK05J is fixed. Two movable heads, one flying above the rotating disk surface and one below, can read or record up to 406 data tracks in the RK05J models, and up to 812 data tracks in the RK05F. In all drives, the disks revolve at 1500 rpm. The double-frequency, nonreturn-to-zero (NRZ) recording method used in these drives can store up to 25 million bits of on-line data in the RK05J, and up to 50 million bits in the RK05F. Data formatting is governed by the controller.

With the address select logic contained in each drive, up to four RK05J Disk Drives can be "daisy-chained" and operated from a single controller bus. Combinations of RK05J and RK05F Disk Drives are possible, as long as the RK05F drives are addressed as "Drives 0/1," "Drives 2/3," Drives 4/5," or "Drives 6/7." No other addressing number pairs may be used to address an RK05F Disk Drive.

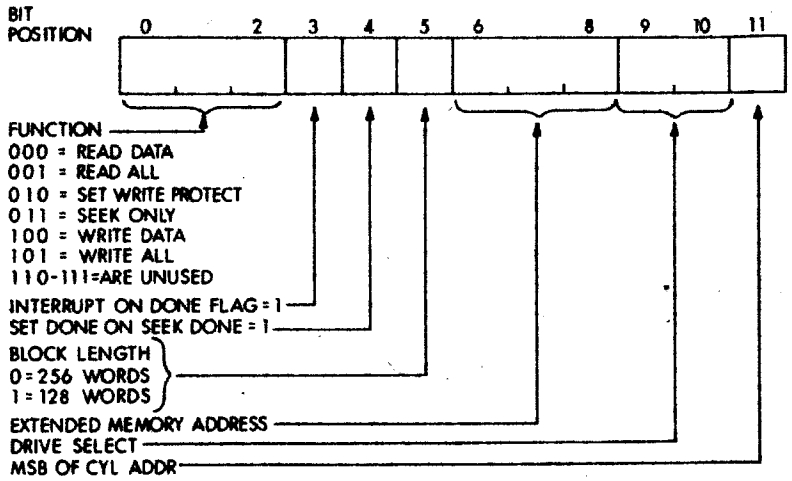
The RK8J-E storage capacity opens a broad range of applications formerly restricted by the high cost of fast access bulk storage. In such applications as inventory control, an RK8J-E cartridge disk system provides an inexpensive storage device for information on thousands of items, with the option of expansion as the need arises.

PROGRAMMING

MNEMONIC	OCTAL CODE	FUNCTION
DSKP	6741	Skip if the TRANSFER DONE flag or ERROR flag is set.
DCLR	6742	Function regulated by AC bits 10 and 11. AC cleared.
DLAG	6743	Load the disk cylinder surface and sector bits from the AC, clear the AC and do the function in the command register.
DLCA	6744	Load current address register from the AC. Clear the AC.
DRST	6745	Clear the AC and read the contents of the status register into the AC.
DLDC	6746	Load the command register from the AC, clear the AC and clear the status register.
DMAN	6747	Maintenance instruction

Command Register (6746)
The command register is loaded by IOT 67x6 from AC bits 0–11. This IOT also clears the accumulator and the status register.

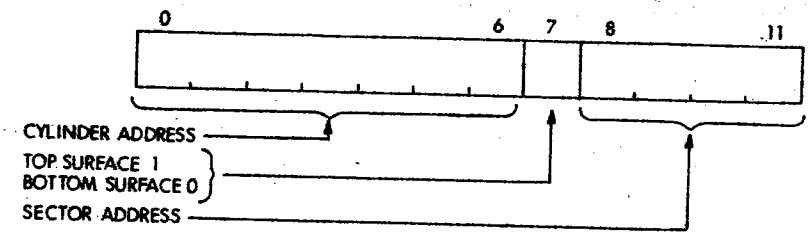
The command register bit functions are:



RK8-E Command Register

Address Register (6743)
The address register is loaded by IOT 6743 from AC bits 0–11.

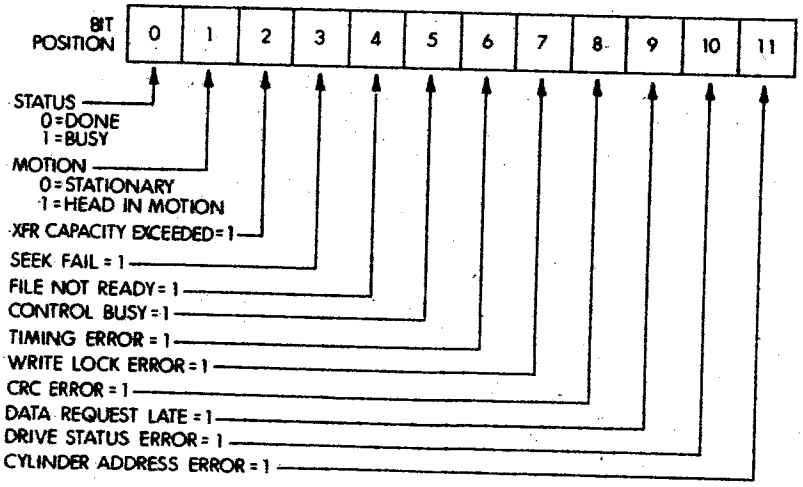
The address register bit functions are:



RK8-E Address Register

Status Register

The status register contains all the information a program requires to determine if the command to the RK8-E is complete and whether or not it was successful:



RK8-E Status Register

RK05 DECpack Operating Features

Complete Status Indication

Indicator lights on each drive show the following conditions: power on, system ready, cylinder on, fault, write protect, load, write, and read.

Smooth, Quiet Operation

The disk is driven by an induction motor and rotates smoothly and quietly with little electrical or mechanical noise. The drive comes on-line less than ten seconds after power is applied.

Transfer Verification, Accurate Positioning

To assure accurate storage and transfer, DECpack systems employ a write-check function, maintenance features, and hardware features that verify the correct track selection and provide a checksum.

Voice coil positioning and an optical position transducer provide fast access times and accuracy to within 100 millionths of an inch. The unique head carriage design requires no lubrication and supports the head at its center of gravity for accurate, repeatable tracking. By eliminating mechanical braking, the design eliminates a major source of wear and critical adjustment. To protect the disk from damage, an emergency retract power supply automatically forces the heads to their home position if line power fails.

Easy Cartridge Handling
Cartridges are easy to load and unload since each disk is permanently mounted inside a protective case that automatically opens when inserted in the disk drive. As the cartridge is pushed into place, the access door is tightly sealed, protecting the disk from dust and dirt.

The cartridge handling system of the RK05J contains two cartridge clamps to provide a positive cartridge location force. As the drive front door is opened, the lifting cams rotate to elevate the cartridge receiver as well as to lift the cartridge clamps away from the cartridge; thus freeing the cartridge for removal. Upon closing the door, the receiver is lowered and the cartridge clamps are simultaneously brought down on the upper cartridge surface to ensure proper cartridge seating on the cartridge support posts. The RK05F (having a fixed cartridge) has a vastly simplified cartridge locating system consisting of a duckbill, door opening wedge, two cartridge support posts, two cartridge retaining springs, and a cartridge guide bracket. As the drive is prepared for initial operation at the customer's site the retaining springs are attached to the cartridge and the cartridge door opening wedge is inserted. The cartridge is then manually guided by the cartridge guide bracket into position onto the duckbill and support posts and finally secured with the cartridge retaining springs.

Reliable, Air-Cooled Operation
For high reliability, the electronics of the DECpack system are cooled with forced air whenever power is on, even when the disk is stopped. Clean cabinet air is introduced into the rear of the drive through a foam prefilter. The air passes over the electronics module through the blower to a high-efficiency filter which removes 99.97 percent of the ambient particles greater than 0.3 micron in size. The resulting ultra-clean air is fed at a rate of more than 30 cubic feet per minute to the power supply, positioner and disk cartridge.

Self-Contained Power Supply
The DECpack power supply is self-contained in each drive to simplify system installation and ensure compatibility. Due to drive efficiency, only 160 watts per drive are required during operation.

SPECIFICATIONS

Capacities
Disks/drive: 1

Surfaces/disk:	2
Heads/drive:	2
Disk capacity (words-formatted):	1,662,976 (RK05J); 3,325,952 (RK05F)
Disk capacity (bits-unformatted):	24,400,000 (RK05J); 48,800,000 (RK05F)
Drives/controller:	1 to 4
Density	2200 bpi max
Tracks (RK05J)	406 (200 plus 3 spare on each side of disk)
Tracks (RK05F)	812 (400 plus 6 spare on each side of disk)
Cylinders (RK05J)	203 (two tracks each)
Cylinders (RK05F)	406 (two tracks each)
Sectors (records) (RK05J)	6,496 (16 per track)
Sectors (records) (RK05F)	12,992 (16 per track)

Transfers

Minimum transfer:	128 words
Data transfer rate:	120,192 words/second
Bit transfer rate:	1.44 million bits per second
Recording scheme:	Double frequency, non-return-to-zero

Access Times

Disk rotational speed:	1500 rpm
Average latency:	20 ms (half revolution)
Typical access times (including head settling):	10 ms (track-to-track), 50 ms (average random move), 85 ms (200 track movement)

Physical Control

3 quad modules plug into Omnibus (3.1 A @ +5 V). Two cables connect the control to first drive.

AC Drive Power

Operating Power:	160 W at 2.1 A (117 V)/1.1 A (230 V)
Idle Power:	85 W at 0.74 A (117 V)/0.37 A (230 V)
Starting Current (power only):	1.8 A (117 V)/0.9 A (230 V)
Starting Current (to start spindle):	10 A for 2 sec. (117 V) 5 A for 2 sec. (230 V)

Environment

Ambient temperature:	60° to 110° F (15° to 43° C)
Relative humidity:	8 to 80 percent (no condensation)

Dimensions

Drive dimensions:	19 in. wide (48.3 cm), 26½ in. deep (67.3 cm), 10½ in. high (26.7 cm) (rack mounted, slides included)
Weight of drive:	110 lb (50 kg)

Ordering Information

Controller/Drive Model No.:	RK8J-EA includes control plus one drive (60 Hz); RK8J-EB includes control plus one drive (50 Hz)

Additional drives

RK05J-AA, RK05F-AA, 95–130 Vac, 60 Hz.
RK05J-BB, RK05F-AD, 190–260 Vac, 50 Hz.

Cartridge Model No.

RK03-KB

FLOPPY DISK, RX8

DESCRIPTION

The RX8 Floppy Disk System is a highly reliable, low-cost mass storage subsystem. It is capable of storing either 256,256 8-bit bytes or 128,128 12-bit words per drive in an industry-compatible format. The RX8 provides a compact data interchange and software distribution medium for I/O applications. In addition, the RX8's random-access capability allows configuring very low-cost, disk-based systems with PDP-8 processors. Such systems can satisfy the needs of applications that could never before afford random-access storage.

The RX8 Floppy Disk System includes an RX01 Floppy Disk drive unit and a quad interface module which plugs into an Omnibus slot. The RX01 includes either one or two drives, a microprogrammed controller module, and a read/write electronics and power supply module, all housed in a 10½ inch, rack-mountable chassis. Up to two drives can be supported by each controller for a total storage capacity of 512,512 8-bit bytes or 256,256 12-bit words. Up to eight controllers can be supported by a processor.

The RX01 Floppy Disk uses a standard oxide coated Mylar® medium which responds to temperature and humidity. The environmental limits for satisfactory operation are 50°–125°F (10°–52°C) and 20% to 80% RH, 86°F (30°C) wet bulb maximum . Operation outside of these limits may cause excessive error rates or premature failure of the floppy diskette.

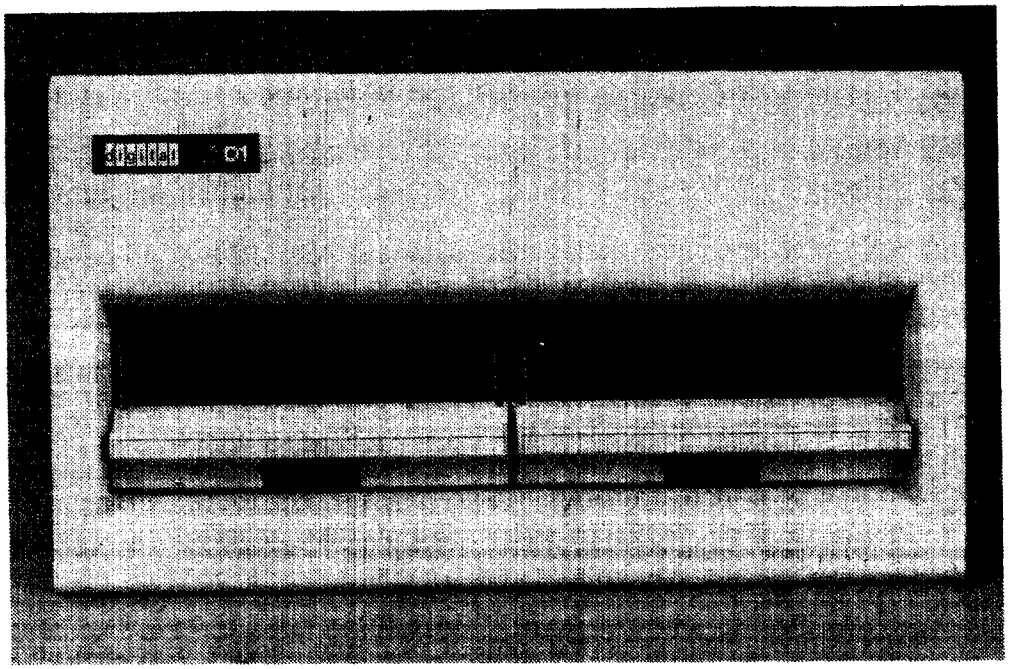
Those configuring and installing RX01 Floppy Disk systems must provide cabinet air flow sufficient to keep air temperature, measured at the disk surface, below 125°F (52°C). Local environmental controls, such as dehumidifiers or air conditioning, may be required to keep relative humidity below 80%.

Given an absolute sector address, the RX01 locates the desired sector and performs the indicated function. Head position is automatically verified, and the cyclic redundancy check (CRC) character is generated and verified.

Track-to-track moves require ten milliseconds for the move plus twenty milliseconds for settling time if the head is loaded for a read or write. The rotational speed of the diskette is 360 rpm resulting in an average latency time of 83 milliseconds. The track-to-track moves, head settling, and latency time produce an average access time of 483 milliseconds. During a sequential access, the whole diskette can be read in about thirty seconds.

THE MEDIA

The RX01 Floppy Disk uses the industry-standard "diskette" or "floppy" media—thin, flexible, oxide-coated disks similar in size to 45-rpm phonograph records. The disk is recorded on one side only and is permanently contained in an 8-inch square, flexible envelope.



RX01 Floppy Disk

The envelope has a large center hole for the drive spindle, a small hole for track index sensing, and a large slit for the read/write head. The inside of the envelope is covered with a soft material designed to wipe the disk surface clean just before reading.

The diskette contains 77 tracks with 26 sectors per track. Each sector can store 128 8-bit bytes or 64 12-bit words for a total formatted capacity of 256,256 bytes or 128,128 words.

The diskette is an ideal storage, interchange, and software distribution medium. It is very inexpensive compared to disk cartridges or disk packs. Being flat and thin, the diskette is compact, enabling large amounts of data to be conveniently stored in a small space. Diskettes can also be easily transported in a briefcase or in a manila envelope.

Because the diskette is preformatted in the industry-standard format, it ensures industry compatibility and drive-to-drive interchangeability. The RX01 can read diskettes written on other industry-standard, floppy disk equipment and vice versa. Preformatted diskettes reduce hardware costs by eliminating the circuitry required to generate the correct format.

RELIABILITY

The RX01 provides exceptional reliability as well as low cost. The simple mechanical construction of the drive and the use of a microprogrammed controller that reduces hardware complexity contribute to the

design goal of 5000 hours MTBF (Mean Time Between Failures). To enhance diskette life, the head contacts the diskette only during reading or writing. With the head loaded on a given track, the diskette can withstand one million revolutions.

Each sector has a CRC character as part of the header field and another CRC character as part of the data field. The RX01 generates and verifies the CRC characters and provides error indications.

OPERATION

The RX01 Floppy Disk drive unit is simple to operate. When the door is opened, the diskette, properly oriented, can be inserted. When the door is closed, the diskette is engaged on the registration hub. When the diskette drive is at operating speed, the software takes over. To remove the diskette, the reverse of the insertion procedure is followed. Elimination of any other operator controls greatly simplifies operation.

FEATURES

High Reliability
Industry compatibility
Ease of maintenance
Simple operation
Use as an I/O device or a random-access file device
Low-cost, compact, removable diskettes
256,256 8-bit bytes or 128,128 12-bit words of data storage capacity per diskette
Average access time of 483 milliseconds
Head loaded only when reading or writing
Extensive operating system and diagnostic software support

SPECIFICATIONS

Storage medium:	preformatted diskette (industry-compatible)
Capacity per diskette:	256,256 8-bit bytes or 128,128 12-bit words
Approximate Data transfer speed:	10K bytes/second in byte mode 5K words/second in 12-bit mode (assume software interleaves every other sector and the whole diskette is read or written)
Time for half revolution:	83 msec
Diskette rotation speed:	360 rpm
Drives per control:	2 (maximum)

Track Positioning Time

One track move:	10 msec
Average track seek:	380 msec
Maximum track seek:	760 msec
Head settling:	26 msec
Average access time:	483 msec

Data Organization

Surfaces per diskette:	1
Tracks:	77
Sectors:	26
Capacity per sector:	128 8-bit bytes or 64 12-bit words
Recording method:	double frequency
Recording density:	3200 bits per inch maximum

Device Codes

70 to 77

Mechanical Specifications

Mounting:	RX01 fits in standard 19-inch cabinet, which is *not* supplied with the system. The unit requires 10½ inches of cabinet space. Interface requires one Omnibus slot.
Size:	10 inches x 19 inches x 17 inches (26.67 cm. x 48.26 cm. x 43.18 cm.)
Weight:	60 lbs. (dual drive); 27kg.
Interface cable:	BC05L-15, 15-foot length (4.57m.)

Power

Running current:	5A maximum at 115V, 60Hz (dual drive) 2.5A maximum at 230V, 50Hz (dual drive)
Current for interface:	1.5A maximum at 5Vdc
Heat dissipation:	500 watts maximum (dual drive)

Environment Specs

Temperature:	15°C (59°F) to 32°C (90°F) with a maximum temperature gradient of 20°F per hour or 11°C per hour
Relative humidity:	20% to 80% with a maximum wet bulb of 25°C (77°F) and a minimum dew point of 2°C (36°F)

Models*

RX8-AA:	PDP-8 single-drive system, 115V, 60Hz
RX8-AC:	PDP-8 single-drive system, 115V, 50Hz
RX8-AD:	PDP-8 single-drive system, 230V, 50Hz
RX8-BA:	PDP-8 dual-drive system, 115V, 60Hz
RX8-BC:	PDP-8 dual-drive system, 115V, 50Hz
RX8-BD:	PDP-8 dual-drive system, 230V, 50Hz

* System includes drive, cable and interface.

DECassette TAPE SYSTEM, TA8

DESCRIPTION

The TA8 DECassette small magtape system designed and manufactured by DIGITAL as an alternate to paper tape.

Two major components comprise the TA8 DECassette system—the TU60 dual cassette drive and the TA8-E quad board interface card.

The TU60 consists of several elements. The first are two separate cassette drives, each having a single solenoid and a pair of dc motors to provide direct reel-to-reel motion without a capstan. The second element consists of two large printed-circuit modules securely mounted on a movable frame so that the boards swing up for servicing.

These modules perform the data formatting, error checking (CRC generation and testing), and bit-to-byte conversion. The third element is the self-contained dc power supply. All these elements are housed in a compact, completely enclosed chassis that mounts in a standard 19 in. DIGITAL cabinet, or can be used in a table-top configuration.

The TA8 interface is contained on a single quad board that uses one Omnibus slot. It is connected to the TU60 via two flat ribbon cables in the rack mounted version, and via one round cable in the table-top configuration. In both cases, the cables are standard lengths, up to a maximum of 25 feet.

Cassette and Tape

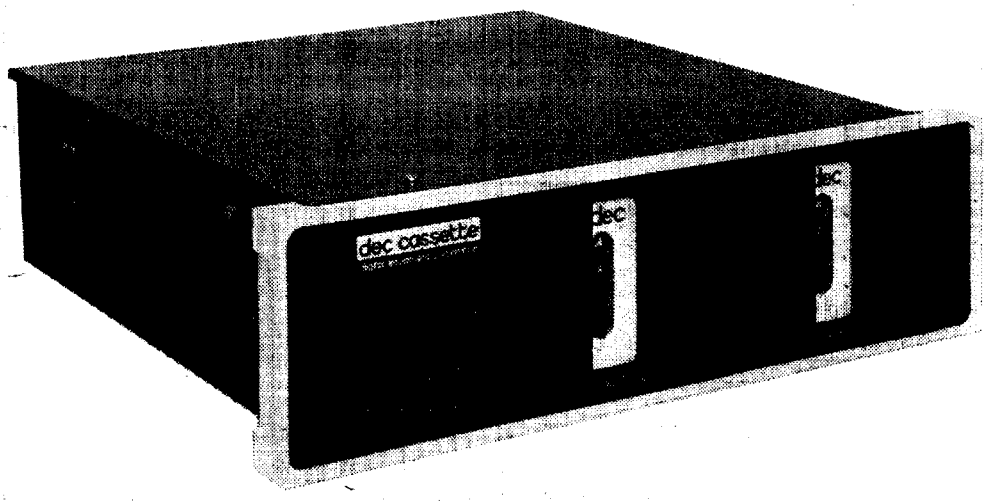
The physical cassette is a DIGITAL-grade "Philips" type, with the hub modified to optimize data capacity.

The tape is a heavy "sandwich" type having a 1 mil base, hard oxide, and the same proprietary coating used on DECtape. The length is 150 feet. By using this stronger, heavier tape, the useful life of the cassette is vastly extended. In actual "real world" life tests, performed under normal operating conditions, the cassette tape has withstood thousands of full passes with error rates well within those specified.

FEATURES

Rugged Tape:	Heavy mylar backing significantly reduces tape failure.
Reel-to-reel Drive:	Increases tape life. Only two driving elements. No pinch rollers, capstans, brakes, clutches, pulleys, or belts.
Single Track Recording:	Differentially balanced head eliminates external noise sensitivity. Low density and wide track recording ensure reliability.
DC Motors:	Linear servos provide precise, gentle tape acceleration and deceleration, eliminate stretching and guarantee gap spacing.

Solid-casting Drive:	All elements needed to control tape position, skew, and motion are mounted on a precision solid casting.
Modified Hub:	Optimizes data capacity, simplifies loading.
Leader Detection:	Optical, foolproof, failsafe.
Interchangeable Cassettes:	Assured by precision construction and frequency-independent read electronics.
Error Checking Circuits:	16-bit cyclic redundancy check.
Phase-encoded Recording:	Read by sensitive, noise-immune peak detection circuits and phase lock loop.
Serviceable:	Electronics, drives, and power supply are easily accessible plug-in subassemblies.



TA8-E DECassette Tape System

PROGRAMMING

The IOT instructions for the TA8-E are as follows:

MNEMONIC	OCTAL CODE	FUNCTION
KCLR	67X0	Clear A and B status registers.
KSDR	67X1	Skip on data flag.
KSEN	67X2	Skip on any one or any combination of: EOT/BOT, EOF, drive empty, timing error, block error, combination of (write lock and "write" true).

MNEMONIC	OCTAL CODE	FUNCTION
KSBF	67X3	Skip on ready flag.
KLSA	67X4	Load status A from AC4–11, clear AC, and load complement of status A into the AC. AC0–3 remain zero. The function specified is not performed until a KGOA command is issued.
KSAF	67X5	Skip on any flag or error condition.
KGOA	67X6	Execute the command given by the contents of the status A register.
KRSB	67X7	Read status B into AC4–11 (jam transfer).

X is the device code, jumper selectable 0 through 7.

Status A register definition:

AC Bit	Function
11	Enable Interrupts
10	Not used
09	Not used
08, 07, 06	Function Select Bits
05	Drive A/B (0 = A, 1 = B)
04	Select Enable

Functions

000 Read. Each time a KGOA command is issued, read data from the TU60's RD/WR buffer into AC4–11, clear data flag, and set the data flag when a new character is available in the RD/WR buffer. Failure to issue a KGOA command before a second word is loaded into the RD/WR buffer results in loss of data and the setting of the timing error bit of status B register. The tape will continue to move until a block or file gap is encountered, and will then stop.

001 Rewind; set ready flag and EOT/BOT bit when done.

010 Write. Each time a KGOA command is issued, load RD/WR buffer from AC4–11, clear data flag and write data on tape. Set data flag when RD/WR buffer can accept a new character.

011 Backspace to file gap, set ready flag when done.

100 Write file gap, set ready flag when done.

101 Backspace one block gap, set ready flag when done.

110 Read/write CRC character. The CRC character is 16 bits, so the KGOA command must be performed twice. The hardware retains the last read or write command issued, and uses this information to determine whether to read or write the checksum. Performing a write checksum also appends a block gap to the block being written. During a read checksum operation, the checksum characters also appear in the AC—they may be used or ignored. If the resulting CRC is erroneous (non-zero), the CRC/block error bit in Status B is set.

111 Space forward to next file gap, set ready flag when done.

Typical tape format:

BOT							EOT
Clear Leader	File Gap	#1 Blk	#2 Blk	File Gap	#1 Blk	File Gap	Clear Leader

This diagram illustrates a 2 block file and a one block file written on tape.

Block Format:

Gap	Preamble Invisible to Programmer	Word Count	"N" 8-bit Bytes	CRC	Gap

SPECIFICATIONS

Medium:	0.150 in. wide computer-grade, 100% certified, 150 ft., 1 mil mylar substrate, proprietary DEC "Philips-Type" cassette.
Type of Recording:	Phase encoded, blocked.
Number of Tracks:	One (full width)
Cassette Capacity:	Full tape 93,000 bytes minimum; with 256 byte blocks, 87,000 bytes minimum.
Transfer Rate:	560 bytes/sec. (peak); with 256 byte block, 497 bytes/sec. (average).
Number of Drives:	Two per control electronics
Functions:	Read forward, write forward, back up one block, space forward to file gap, space back to file gap, write gap, rewind, manual rewind.
Data Format:	Variable block length, hardware formatted, with length software controlled.
Block Length:	1 byte minimum, no maximum
Error Control:	16-bit cyclic redundancy check (CRC), hardware generated and appended to data at time of writing. Tested during read by hardware via program command.
Error Rate:	1 in 10^8 write errors 1 in 10^8 unrecoverable errors 1 in 10^7 recoverable read (3 retry)

Drive:	Reel-to-reel. Average speed, read/write 9 in./sec. Average speed, search 21 in./sec.
Start/Stop Time:	< 20 ms, linear ramp controlled
Density of Recording:	350–700 bits/in.
Rewind Time:	< 30 sec., typical 20 sec. Speed, servo controlled
Data Interface:	8-bit parallel, synchronous program transfers via processor interface.
Read Electronics:	Peak detection/phase lock loop (low threshold read).
Power Requirements:	90 V to 132 V, 180 V to 265 V, 48 to 63 Hz (self-contained dc supply). 120 W maximum.
Block Format:	Pre-Gap .25" | Preamble 32 bit | "N" Data Bytes | CRC Character $(X^{16}+X^{15}+X^{2}+1)$ | Post-Gap .25"
Beginning/End Tape Detector:	Clear leader
Environmental:	Operating temperature range: 50° F to 105°F, (10° to 40° C) storage temperature range (cassette): 40° F to 122° F, operating humidity range: 20% to 80% noncondensing. Maximum wet bulb 85° F. Altitude 0 to 10,000 feet.
Indicators and Controls:	Power on (each drive), manual rewind, write protect (on cassette).
Size:	5¼ × 19 × 18½ in. (13.3 cm × 48.3 cm × 47 cm)
Weight:	32 lb (14.5 kg)
TA8 Variations:	TA8-AA Rack Mount—115 Vac TA8-AB Rack Mount—230 Vac

DECTAPE AND CONTROLLER, TD8-E

DESCRIPTION

The TU56 DECtape drive and TD8-E controller comprise a bi-directional magnetic tape storage system designed for the PDP-8/E, 8/F, 8/M, and 8/A series of minicomputers.

This fixed address tape system provides random access for high speed reading or writing of files on 260 feet of 3/4-in. wide magnetic tape, contained on a reel less than 4 in. in diameter.

Redundant recording (each bit of data is recorded on two separate tracks) ensures high reliability.

TD8-E Control Unit

The TD8-E control unit interfaces a TU56 type DECtape drive to the PDP-8 series of minicomputers. When reading, writing, or searching, the computer acts as a controller for the DECtape unit. Data transfers to and from the computer are through the accumulator, in a non-interrupt mode.

The TD8-E controller occupies a single quad Flip Chip module which plugs directly into the Omnibus. This unique packaging arrangement allows the end user to expand his system in small increments from 1 to 8 drives.

The TD8-E is available in four versions:

TD8-EH is a single DECtape drive and control. (Rack Mountable.)

TD8-EM is a dual drive DECtape and control. (Rack Mountable.)

TD8-EJ is a single DECtape drive and control. (Table Top Model.)

TD8-ER is a duel DECtape drive and control. (Table Top Model.)

Tape Compatibility

Tapes may be certified, programmed, read, modified, and rewritten interchangeably on either the larger automatic DECtape units (TC08/TC01) or on the TD8-E. All the necessary subroutines and MAINDECs for the TD8-E are available; for example:

Read/Write Subroutines

Tape Certification Routine

MAINDEC Maintenance Programs

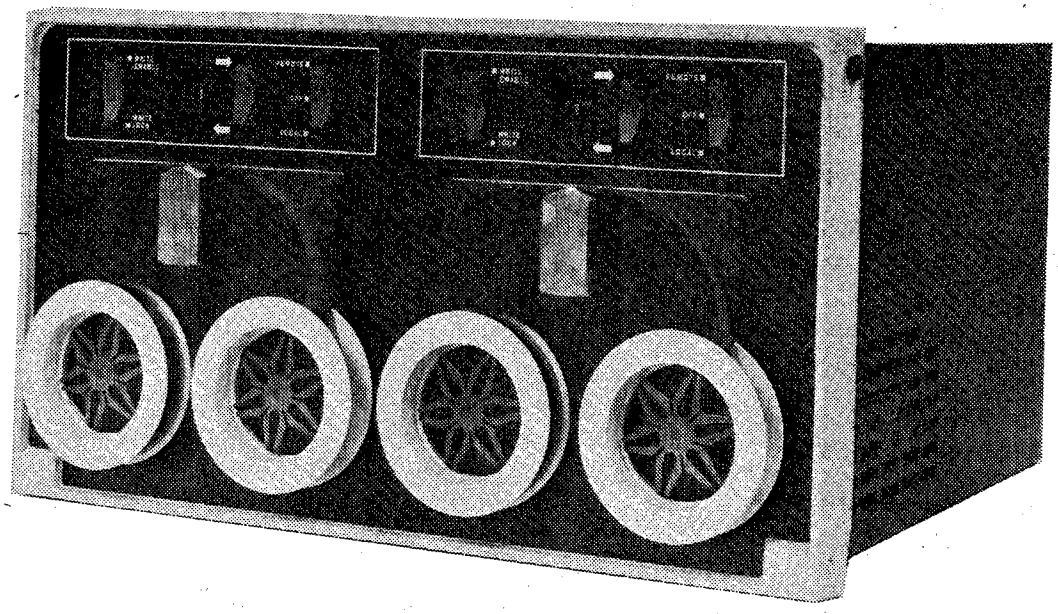
OS/8 Programing System which operates with an 8K (plus 256 word ROM) or larger core memory configuration.

A DECtape Copy Program

DECtape is unique—convenient pocketsized reels are handy to carry and easy to mount and dismount. The reels permit convenient, separate filing, and mailing of tape files. Each reel holds up to 196,672 12-bit words.

FEATURES

- Low price
- Pocket-sized reels
- High reliability



TU56 DECtape Drive

Insensitive to line voltage or frequency variation

One or two tape drives in a single unit

Low maintenance

Control plugs into Omnibus

SPECIFICATIONS

Tape Characteristics

Size:	260 feet of 3/4 in., 1 mil Mylar sandwich tape, coated both sides.
Reel diameter:	3.9 in. (9.9 cm)
Tape Handling:	Direct drive hubs and specially designed guides float the tape over the head. No capstans or pinch rollers are used.
Speed:	97 ± 14 ips
Density:	350 ± 55 bpi
Information capacity:	2702_8 Blocks with 201_8 12-bit words per block (196, 146 12-bit words)
Tape motion:	Bi-directional

Word Transfer Rate

8325 12-bit words per second.

Addressing
Mark and timing tracks allow searching for a particular block by number in a forward or backward direction.

Tape Motion Timing

Start Time:	150 msec ± 15 msec
Stop Time:	100 msec ± 10 msec
Turn around time:	200 msec ± 50 msec

Mounting
TU56 drive mounts in a standard 19 in. equipment rack.

Size—TU56 Drive
10-1/2 in. high (26.7 cm)
19 in. wide (48.3 cm)
15-1/4 in. deep (38.7 cm)
1 quad module TD8/E Control

Cooling
Internally mounted fan provided for TU56.

Environmental Conditions
Temperature: 40° to 90° F (4.4° to 32° C)

NOTE

The magnetic tape manufacturer recommends 40–60% relative humidity and 60° to 80° F as an acceptable operating environment for DECtape.

Controls for TU56

UNIT SELECT:	8 position rotary switch.
WRITE ENABLE-WRITE LOCK:	2 position rocker switch.
FORWARD-REVERSE:	2 position spring-loaded rocker switch to enable manual winding of tape when transport is in local control.
REMOTE-OFF-LOCAL:	3 position rocker switch. REMOTE enables computer control of transport. OFF disables transport.

PROGRAMMING

TD8-E instructions

MNEMONIC	OCTAL CODE	FUNCTION
SDSS	67X1	Skip if single line flag is set. Single line flag is set each time a line of data is read.
SDST	67X2	Skip if time error flag is set.

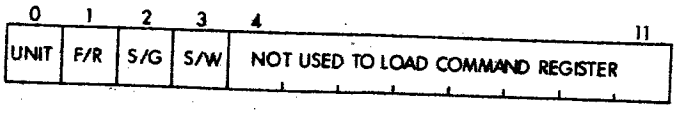
TD8-E instructions

MNEMONIC	OCTAL CODE	FUNCTION
SDSQ	67X3	Skip if quad line flag is set. Quad line flag is set after 4 lines of data are read.
SDLC	67X4	Load command register from the AC, clear time error, and start UTS delay if UNIT, DIRECTION or STOP/GO flip-flops are changed.
SDLD	67X5	Load data register from the AC, do not clear the AC, and clear single line and quad line flags.
SDRC	67X6	Load contents of command register, mark track register, and status bits into the AC. Clear single line and quad line flags.
SDRD	67X7	Load contents of data register into the AC, and clear single line and quad line flags.

X is the device code.

Command Register Format

The accompanying figure shows the format of data loaded into the Command Register when the SDLC instruction is executed.



Format of Data Loaded into the Command Register

The Command Register is made up of four flip-flops which are loaded from the DATA BUS by the SDLC instruction. 1s set the flip-flops and 0s clear it.

UNIT — Selects which drive on the TU56 is to be used. If UNIT is cleared, Unit 0 is selected.

F/R — Determines which direction the tape is to move. If F/R is cleared, direction is Forward (CW).

S/G — Tells the selected unit to move tape or stop. If S/G is cleared, the selected tape will stop. The GO signal is delayed 200 ns after an SDLC instruction to ensure that the unit select line has had time to switch in the Tape Drive Unit before the tape starts to move.

R/W — Instructs the selected unit to read or write data. If R/W is cleared, a read operation will take place; if it is set, a write operation is executed.

MAGNETIC TAPE SYSTEM, TM8-MA/TS03

DESCRIPTION

The TM8-MA/TS03 is a low-cost, 9-track magnetic tape system that uses industry-standard 800-bpi NRZI recording format. The basic system consists of a TS03 master tape drive, TM8-E controller and power supply. A second tape drive can be added at the cost of the tape drive only, because the second (slave) drive uses the master drive's controller and power supply.

The major features of the TM8-MA are high reliability, low cost, small size, and low power consumption. The major benefit is that, despite its low cost, the TS03 magnetic tape drive does not sacrifice reliability. It uses the same technique to record data in the same manner as larger, more expensive transports, but it does this with a slower, extremely simple mechanism.

TS03 Magnetic Tape Drive

The TS03 is a 9-track, 800 bpi magnetic tape drive. Each tape drive is a self-contained unit including read and write electronics, low inertia friction capstan and two linear-drive reel servos. The reel servos use mechanical servo arms for controlling the tape storage loops. Magnetic arm transducers are employed to sense the arm position and control tape tension. The linear servos provide gentle tape handling to prolong tape life.

The recording head assembly includes an open-loop tape path with single edge guiding, tape cleaner, EOT/BOT station and a 9-track read-after-write head. The recorder has a transparent plastic door enclosing the tape path and recording area to allow viewing while still excluding airborne dust.

The 7-inch diameter tape reel is mounted on a quick-release tape hub. A fixed take-up hub is provided and does not require a separate tape reel.

The master drive is mounted on slides and occupies 10½-inches of panel height in a standard DIGITAL cabinet. The controller for interfacing to a PDP-8 plugs directly into the Omnibus.

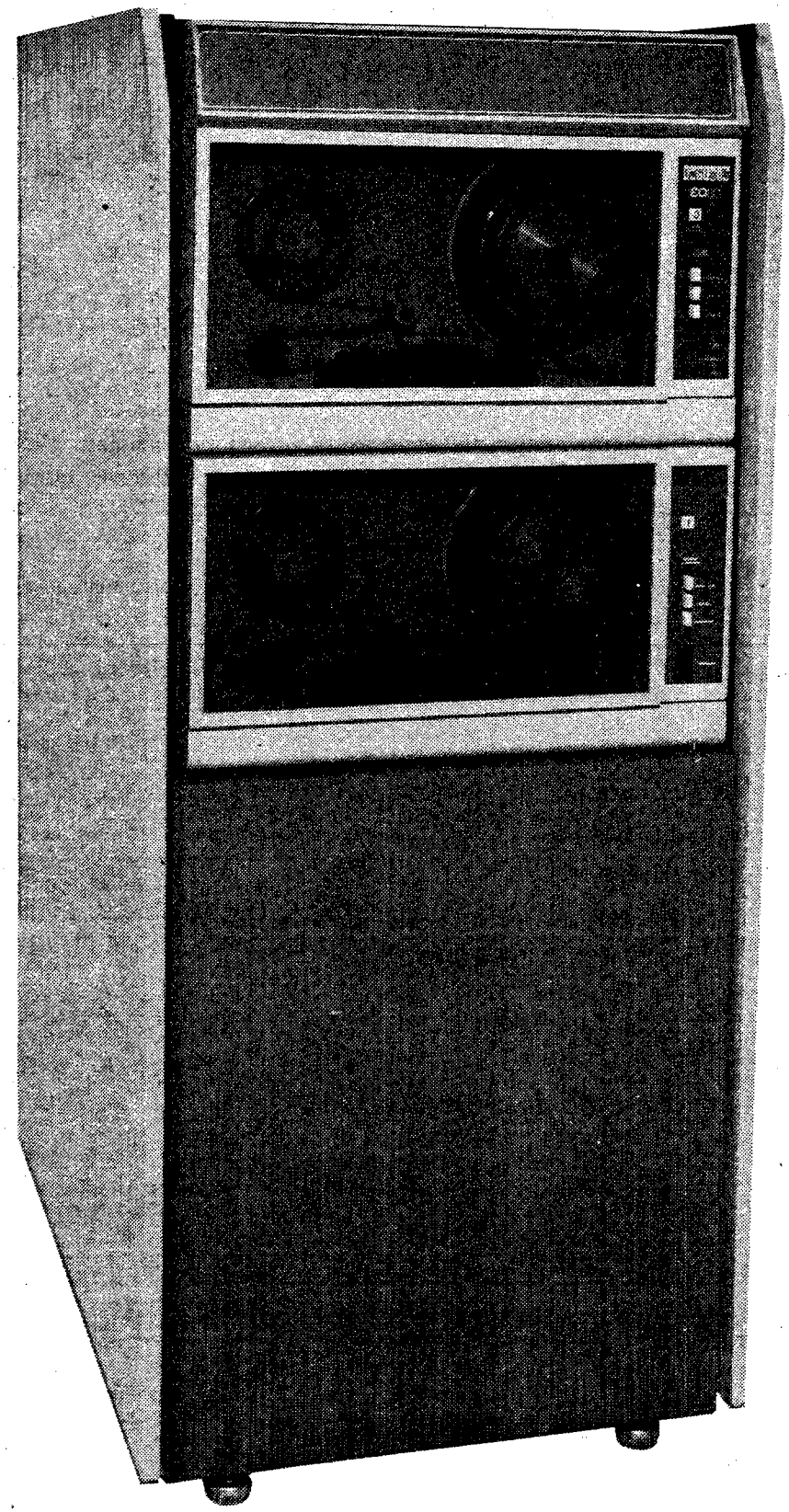
The master drive includes portions of controller circuitry (adapted on a printed circuit board) mounted beneath the drive mechanism enclosure. The board is hinged to facilitate access for servicing and maintenance.

MASTER CONTROLLER FUNCTIONS

The TS03 Master Controller performs the following tasks:

TAPE FORMAT

A Cyclic Redundancy Check character is generated on write data passing to the TS03 and is strobed onto tape. This CRC character is generated in accordance with ANSI standard for 800-bpi NRZI recording. Data is also checked for errors while reading the tape.



TS03 Magnetic Tape Drive

A Longitudinal Redundancy Check character is also written onto the tape.

An industry-compatible tape mark is generated when a Write Tape Mark instruction (also known as Write EOF or Write File Mark) command is in progress.

RECORD DETECTION
Once tape motion has been initiated on a tape transport, motion will not be halted until either a valid record is detected or the INITIALIZE signal is given.

DATA CHECKING
A verical parity bit is attached to each data character written. Whenever the TS03 is moving tape at read/write speed, it checks data for correct vertical parity and a correct Longitudinal Redundancy Check character for each record read.

The TS03 also contains logic for detecting industry-compatible tape marks (END-OF-FILE mark).

Cost savings result from small size because the TS03 frequently fits into existing cabinets. The TS03, with controller, can fit into a processor cabinet with spare room left over for another subsystem.

Small size also means lower power consumption because:

1. There is no vacuum motor.
2. The TS03 uses very low standby power—approximately 60 watts.
3. It takes less power to drive the TS03's seven-inch diameter reels.
4. Lower power consumption means a smaller load if back-up generator or batteries are used.
5. Heat dissipation is so low that no cooling fans are needed.

The absence of cooling fans also means that the TS03 is quiet—so quiet it cannot be heard running.

RELIABILITY
The TS03 is designed to read and write data to industry standards with high reliability. The calculated MTBF (Mean Time Between Failures) is 5,080 hours for the tape drive.

A unique feature of the TS03 eliminates the writing of hard errors on tape. If an error is detected in the read-after-write check, programming can cause the entire record to be rewritten. Hardware within the TS03 automatically senses that this is a retry and the read-checking margins are tightened up to ensure distinguishing between a transient error and a bad tape area. If the data passes on a second (or subsequent) pass, the written data is guaranteed to exceed the read thresholds. If there was a bad section of tape, the faulty record can be erased, then recorded correctly further down the tape.

TM8-MA Tape Control

The TM8-E control provides the interface between the PDP-8/A and the TS03 magnetic tape transport. The data transfers are via single cycle data break with a transfer rate of 36KHz.

The TM8-MA contains six registers which are used to control the transport and report status of the transports to the computer. The registers are loaded and read using IOT instructions which require no data break.

TM8-E Instructions

MNEMONIC	OCTAL CODE	OPERATION
LWCR	6701	Load Word Count Register
CWCR	6702	Clear Word Count Register
LCAR	6703	Load Current Address Register
CCAR	6704	Clear Current Address Register
LCMR	6705	Load Command Register
LFGR	6706	Load Function Register
LDBR	6707	Load Data Buffer Register
RWCR	6711	Read Word Count Register
CLT	6712	Clear Transport
RCAR	6713	Read Current Address Register
RMSR	6714	Read Main Status Register
RCMR	6715	Read Command Register
RFSR	6716	Read Function Register & Status
RDBR	6717	Read Data Buffer
SKEF	6721	Skip if Error Flag
SKCB	6722	Skip if Not Busy
SKJK	6723	Skip if Job Done
SKTR	6724	Skip if Tape Ready
CLF	6725	Clear Controller and Master

OPERATION

All operation is controlled and monitored through four switches and associated indicators on the front panel:

POWER
ON-LINE
LOAD
REWIND

An additional indicator, WRITE ENABLE, shows the operator whether the tape is write-protected or not. Each of the indicators uses solid-state illuminators (as opposed to light bulbs). The advantage of the solid-state indicators is that they will last considerably longer than an incandescent light bulb.

There is extensive software available for operating the TS03. The software is compatible with the TU10 Tape Drive.

SPECIFICATIONS

Main Specifications

Storage medium:	½-inch wide magnetic tape (industry compatible)
Capacity/tape reel:	5 million characters
Data transfer speed:	10,000 char/sec
Drives/control, max:	2

Data Organization

Number of tracks:	9
Recording density:	800 bits/inch
Inter-record gap:	0.5 inches, min.
Recording method:	NRZI

Tape Motion

Read/write speed:	12½-inches/sec
Rewind time:	1 minute, max.
Tape drive:	single capstan
Reel braking:	dynamic servo control
Speed variation:	3% instantaneous; 1% long term
Start/stop distance:	0.19 inch
Start/stop time:	30 msec

Tape Characteristics

Length:	600 ft
Type:	Mylar base, iron-oxide coated
Reel diameter:	7 inches

Mechanical

Tape drive, mounting:	mounts on slides in a standard 19-inch cabinet
Tape drive, size:	10½-inch (26.7 cm) panel height, 17-inches (43.2 cm) deep
Tape drive, weight:	37 lbs (16.8 kg.)

Power

Input current:	1A at 90 to 132 Vac, or 0.5 A at 180 to 240 Vac
Power consumption:	100 W

Operating Environment

Temperature:	15°C to 32°C (59° to 90°F)
Relative humidity:	20% to 80%, with maximum wet bulb 25°C and minimum dew point 2°C
Altitude:	10,000 feet

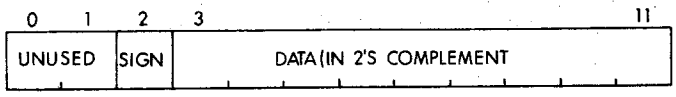
Miscellaneous

BOT, EOT detection:	photoelectric sensing of reflective strip, industry compatible
Magnetic head:	dual gap, read after write, 0.15-inch gap

POINT PLOT DISPLAY CONTROL, VC8-E/VR17

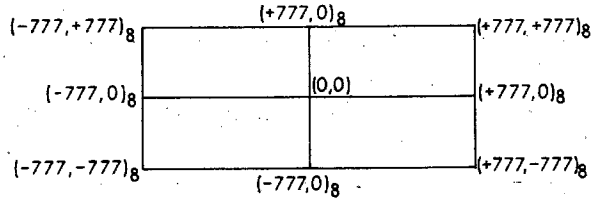
DESCRIPTION

The VC8-E is a two-axis (X and Y) digital-to-analog converter plus intensifying circuitry (Z axis) that provides deflection and intensity information to the display oscilloscope. Coordinate data is transferred to the X and Y axis from bits 2–11 of the accumulator. The VC8-E Interfaces with Tektronix 602, 611, and 613 oscilloscopes or with the VR17. It provides programmable two color displays and storage mode on the 611 and 613.



X and Y Buffer Register

The position of the oscilloscope beam will be determined by the contents of X and Y buffer registers. Coordinate (0,0) is located in the center of the screen.



CRT Coordinate System

The user is reminded of the relationship between the signed octal numbers used above and their corresponding 2's complement form.

Signed Values (used in example)	2's Complement (10 bit)	Position
+777	0777	Top or right
+1	0001	
0	0000	Center
−1	1777	
−777	1001	Bottom or left

VC8-E/VR17 Point Plot Display System

The VC8-E, when combined with a VR17 Oscilloscope, or a user supplied scope, displays data in the form of a 1024_{10} by 1024_{10} dot array. Under programmed control, a bright spot may be momentarily produced at any selected point in this array. Thus, a series of these intensified dots may be programmed to produce graphical output on a CRT.

Interfacing to any PDP-8 Processor is accomplished with the VC8-E control which plugs directly into the Omnibus. Information is transferred from the AC to the display by means of programmed IOT instructions. The displayed information can therefore be on-line sampling or memory data or data from a mass storage device.

VR17 Oscilloscope Display

The VR17 is a compact solid-state CRT display with self-contained power supplies and a viewing area of 9¼ inches x 9¼ inches. The VR17 can plot 1500 random points with no flicker. X/Y deflection speed is 900 ns intensified, 700 ns non-intensified, and less than 20 μs is required for a maximum deflection step in any direction. Interface with the VC8-E is by means of connector assembly BCO1K-10 (10 feet—standard length, included with VC8-E/VR17), BCO1K-25 (25 feet), or BCO1K-50 (50 feet).

SPECIFICATIONS

The VC8-E consists of a two-axis digital-to-analog converter and intensifying circuit that provides deflection and intensity signals, which are then applied to the input amplifier circuitry of such display units as the VR17 oscilloscope. The control circuit for the VC8-E is located on a PDP-8 module (M869), which plugs into the Omnibus.

The basic VC8-E system consists of the following circuitry:

a. Omnibus interface, IOT decoding, skip, clear AC, and interrupt control.

b. X-axis buffer, D/A converter, filter and summing amplifier, and bipolar line driver.

c. Y-axis buffer, D/A converter, filter and summing amplifier, and bipolar line driver.

d. Z-axis control, which consists of provision for intensity signal necessary for most oscilloscopes, and intensity and channel select signals necessary for the VR17 oscilloscope.

NOTE

The display times of those instructions that include intensification depend upon the type of oscilloscope used, for example:

VR17	21 μs
Tektronix 602	6 μs

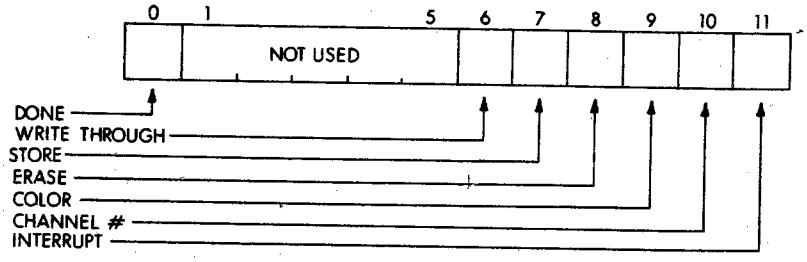
A switch is provided to select the proper settling interval.

PROGRAMMING

Instructions for outputting data to the oscilloscope display are:

MNEMONIC	OCTAL CODE	FUNCTION
DILC	6050	Clears enable, flag, and delay flip-flops.
DICD	6051	Clear Done Flag

MNEMONIC	OCTAL CODE	FUNCTION
DISD	6052	Skip if Done Flag (1). Do not Clear Done Flag.
DILX	6053	Clear Done Flag; load X register, wait for settle. Set Done Flag. Do not clear AC.
DILY	6054	Clear Done Flag; load Y register, wait for settle. Set Done Flag. Do not clear AC.
DIXY	6055	Clear Done Flag; intensify; Set Done Flag.
DILE	6056	Transfer contents of AC to Enable Register as defined below. Clears AC.
DIRE	6057	Transfer the contents of the Display Enable/ Status Register to the AC as defined below:



Display Enable/Status Register

Display Enable/Status Register Bit Descriptions

BIT	TITLE	DESCRIPTION
0	Done Flag	May be read using a DIRE (transfer enable to AC) command. It may not be set under program control using the DILE (load enable, clear AC) command.
6	Write Through	When set to a 1 and a 6055 intensity command is given, this will generate a small ellipse on 611, 613 storage scope. Its purpose is to locate the writing beam on the screen in a store mode without storing the ellipse.
7	Store	When set to a 1, this will cause the 611, 613 to go to a store mode. When set to a 0 the 611, 613 will go to a non-store mode.
8	Erase	When set to 1, this will generate an erase cycle in the 611, 613 storage scope. When doing an erase nothing can be displayed until the Done flag is set. The erase cycle lasts 450 Ms ±50 Ms. The erase bit is a write bit only and can not be read back using the DIRE command.

BIT	TITLE	DESCRIPTION
9	Color	N/A
10	Channel Number	Channel number selects the VR17 display channel. When set to a 0, information is displayed on channel 1. When set to a 1 information is displayed on channel 2.
11	Interrupt Enable	When set to a 1, causes the processor to interrupt (JMS 0) on done = 1.

The Done flag (bit 0) may be read using a DIRE (transfer enable to AC) command. It may not be set under program control using the DILE (load enable, clear AC) command.

Channel number selects the VR17 display channel. Bit 10 = 0, channel 0; Bit 10 = 1, channel 1.

Interrupt set to a one will cause the processor to interrupt (JMS) on done = 1.

Both channel number and interrupt may be loaded from the read into the AC using the DILE and DIRE commands respectively.

Programming Example

The VC8-E is a very fast display control. So fast, in fact, that most display oscilloscopes cannot position their beam before an intensify command is performed. For this reason a Done flag has been incorporated into the control and should be used whenever random points are plotted sequentially.

```
    •
    •
    •
CLA
TAD   X          /GET X-COORDINATE
DILX             /LOAD X REGISTER
CLA
TAD   Y          /GET Y-COORDINATE
DILY             /LOAD Y REGISTER
DISD             /SKIP ON DISPLAY DONE FLAG
JMP .—1
DIXY             /INTENSIFY POINT
```

VIDEO TERMINAL, VT50

DESCRIPTION

The VT50 is a low cost, high speed, alphanumeric CRT display with a keyboard for data entry. The VT50 is quiet because it needs no cooling fans. The screen is designed for optimum character definition; it is recessed and tilted to avoid glare from overhead lighting. Since no filter covers the screen, it can be cleaned very easily.

SPECIFICATIONS

Dimensions

Height:	14.1 in. (35.8 cm)
Width:	20.9 in. (53.1 cm)
Depth:	27.2 in. (69.1 cm)

Weight

43 lb (19.4 kg)

Environmental

Temperature:	50° to 104° F (10° to 40° C)
Relative humidity:	10% to 90% with maximum wet bulb 28° C (82° F) and minimum dew point 2° C (36° F)

Input Voltage

115 V:	100 to 126 V @ 60 Hz ± 1 Hz
230 V:	195 to 255 V @ 50 Hz ± 1 Hz
Power consumption:	110 watts

Display

Format:	12 lines x 80 characters
Character matrix:	5 x 7
Character size:	.11 in. x .20 in. (2.8 mm x 5.1 mm)
Screen size:	8.7 in. x 4.3 in. (22.1 cm x 10.9 cm)
Capabilities:	Control data transmission at high baud rates; will contain FORTRAN or COBOL full-card images; operator-adjustable character intensity

Keyboard

Character set:	64 ASCII upper case, alpha, numeric, and punctuation characters. Typewriter format keyboard. Audio/tactile response mechanism for fast operator feedback. 3-key roll-over feature to minimize typing errors. BREAK key included for half duplex software

Terminal Modes

Off-line:	
On-line:	Full Duplex

Page Overflow

Upward scroll

Parity
Even or mark (no parity) selectable

Cursor
Control: Up or down one line, right or left one position, home, erase from cursor to end of line, erase from cursor to end of screen
Type: Non-destructive, underscore

Communications
20 mA current loop standard; EIA interface optional

Interface
SLU on DKC8-AA I/O Option Module, KL8-JA Asynchronous Data Interface, or KL8A Serial Line Unit

Transmission Code
USASCII extended through Escape Sequences

Operator Controls
Power on/off, intensity control, baud rate switches, Full Duplex or Full Duplex with Local Copy switch

Overload Protection
Thermal switch in line transformer

Transmission Rates
Switch-selectable
Full Duplex: 75, 110, 150, 300, 600, 1200, 2400, 4800, and 9600 baud

DECscope VIDEO DISPLAY TERMINAL, VT52

DESCRIPTION

The VT52 DECscope is an upper-and-lower-case ASCII video terminal whose display holds 24 lines of 80 characters.

The VT52 is upward-compatible with the VT50, but an identification feature allows software to distinguish between the two models. Software which uses Hold-Screen Mode to produce operator-controlled, screenful-by-screenful output to the VT50 will work perfectly on the VT52 without modification, despite the different screen capacities.

The VT50's human-engineering features carry over to the VT52: A clicking sound provides feedback to the operator when keys are typed; a rollover feature lets the terminal get the message straight even if two or three keys are pressed at once; the keyboard follows the standard typewriter layout.

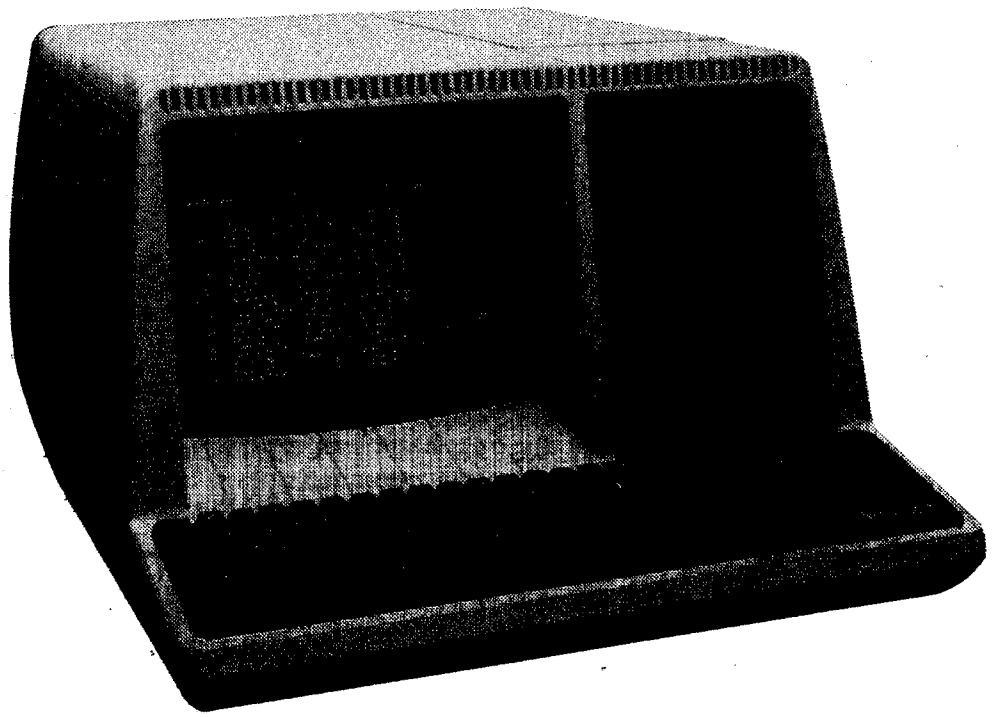
The VT52 goes beyond the VT50, however, to provide a "two-way" auxiliary keypad. In one mode, the keypad is used to generate program-compatible numeric codes.

Applications which require much numeric input can use the VT52 without modifying hardware or software, while the operator uses the convenient "numeric pad." Or, software may place the VT52 in the alternate mode, in which each key on the keypad transmits a unique Escape Sequence. This allows the host computer to distinguish between keys typed on the auxiliary keypad and similar keys on the main keyboard. In this mode, each key on the keypad can be used to invoke a user-defined function.

The VT52 has a wide range of cursor-positioning functions. As well as moving the cursor one position in any direction, software can move the cursor to any position on the screen with a Direct Cursor Addressing command which specifies the destination for the cursor. The VT52 also offers fixed horizontal tabs, a "Cursor-to-Home" command, and two screen-erasure functions. Data on the screen scrolls up when a Line Feed function is performed with the cursor on the bottom line; it scrolls down when a Reverse Line Feed function is performed with the cursor on the top line.

SPECIFICATIONS

Parity	Even or mark (no parity) switch-selectable. Odd or space possible with rewiring.
Cursor	Type: Blinking underline. Control: Up or down one line; right or left one character; home; tab (fixed tab stops every 8 spaces); direct cursor addressing (allows cursor to be moved to any character position on the screen).



VT52 DECscope Video Display Terminal

Functions	Erase display from cursor position to end of line; erase to end of screen; scroll up; scroll down.
Hold-Screen Mode	Allows operator to halt transmission from host, preserving data on display. Operator can request new data, line- or screenful-at-a-time. Enabled/disabled by Escape sequences sent by system software.
Terminal Self-Identification	Terminal transmits on command a sequence unique to its model; software can then look up features available on the terminal with which it is in contact.
Communications	20mA current loop or EIA interface; specify at time of order. Code: USASCII extended through Escape Sequences. Speed: Switch-selectable. Transmission rates, full duplex (switch selectable) 75, 110, 150, 300, 600, 1200, 2400, 4800, and 9600 Baud. Switch-selectable local copy.
Synchronization	Automatically transmits control codes to host, requesting suspension and resumption of transmission, when unable to process data.

Operator Controls	Power On/Off, Intensity Control, Baud Rate Switch, Terminal Mode Switch, Key-Click On/Off, Even/No Parity.
Overload Protection	Thermal cutout.
Case Material	Injection molded Noryl thermoplastic.
Screen Phosphor	P4
Dimensions	Height: 14.1 in. (35.8 cm.) Width: 20.9 in. (53.1 cm.) Depth: 27.2 in. (69.1 cm.) Minimum Table Depth: 450mm (17.7 in.)
Weight	20 kg (44 lbs)
Operating Environment	DEC STD 102—Class B environment 10°C to 40°C (50°F to 104°F) Relative Humidity 10% to 90% Maximum wet bulb 28°C (82°F) Minimum dew point 2°C (36°F)
Line Voltage	(US model) 100–126 volts (European model) 191–238 volts or 209–260 volts
Line Frequency	(US model) 60 ± 1 Hz (European model) 60 ± 1 Hz or 50 ± 1 Hz
Power Consumption	110 Watts
Power Line Hash Filter	Low Leakage Balun type
Display	Format: 24 lines x 80 characters Character Matrix: 7 x 7 Character Size: 2.0mm x 4.0mm (0.08 in. x 0.16 in.) Screen Size: 210mm x 105mm (8.3 in. x 4.1 in.) Character Set: 96-character displayable ASCII subset (upper and lower-case, numeric, and punctuation).
Keyboard	Character Set: Complete 7-bit ASCII set (128 codes) Key layout: Typewriter—rather than keypunch—format, 63 keys. Auxiliary keypad: 19-keys: numerals, cursor-movement, 3 user-definable function keys. CAPS LOCK key: Locks alphabetic keys to upper-case state, but does not affect non-alphabetic keys.
Audible Signals	Key-click: Switch-controlled Bell: Sounds (a) upon receipt of control characters BEL; (b) when Keyboard input approaches right margin (output from host approaching right margin does not cause bell to ring).
Page Overflow	LF causes upward scroll; Reverse Line Feed causes downward scroll.

GRAPHICS TERMINAL, VT55

DESCRIPTION

The VT55 is an on-line, interactive CRT terminal that offers waveform graphics capability—a new and significant extension to meet the needs of a variety of applications. Two graphs of 512 (maximum) data points each can be displayed with a screen resolution of 512 horizontal by 236 vertical points. Cursors (20-point vertical lines) are available (one per data point) to facilitate data editing and graph generation. In addition, the VT55 allows simultaneous display of any combination of text and graphics. By simply pressing a specified key, the VT55 supplies a hard copy reproduction of the display screen for both characters and graphs.

Waveform graphics capability is an important addition to applications involved with such activities as plotting histograms, waveforms and peak analyses, data acquisition, monitoring, trending, simulation, laboratory charts and forms . . . wherever results can be improved through graphics with extended capability.

The VT55 can hold up to 1,920 characters in 24 lines of an 80 characters-per-line matrix. The 24th line of text is positioned below any graphs to facilitate labelling the x axis.

VT55 Screen

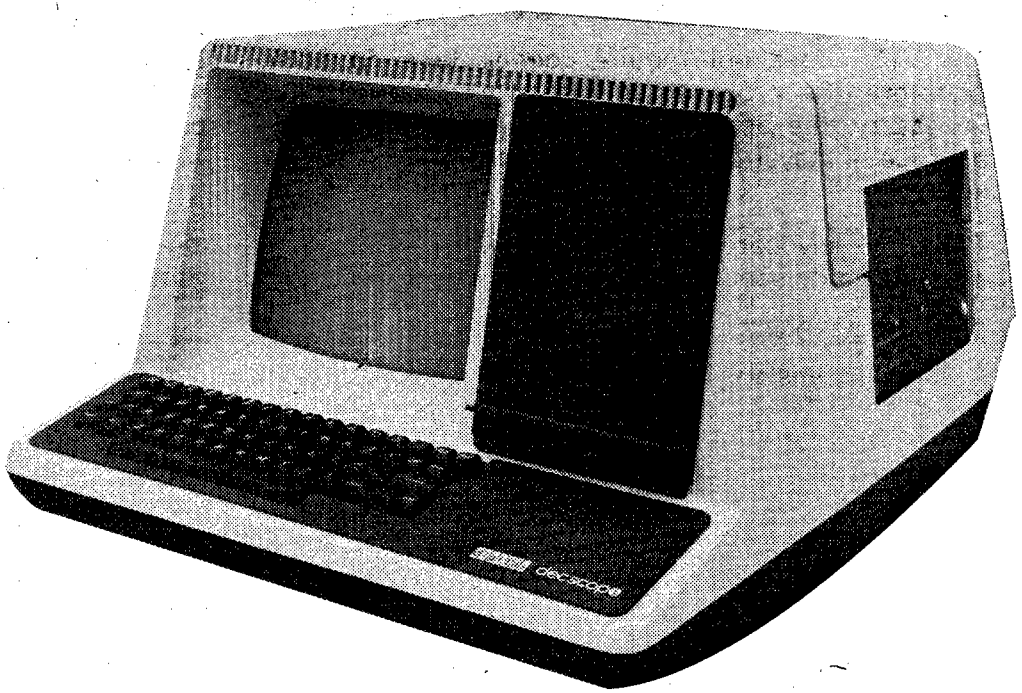
A control at the rear of the terminal allows the operator to adjust screen brightness for the best possible vision under varying light conditions. The standard model has no filter covering, so it can be easily cleaned. For users with special applications, the VT55 will accept colored filters.

Operator response to the VT55 is based on the cursor—a flashing underline that indicates where the next character will appear. Because it is a fast position indicator, the cursor encourages quick operator response. (Programs can also direct the computer to display a form on the screen and move the cursor to its proper location so the operator can fill in responses.)

The cursor provides a full range of user control flexibility, including both conventional and extended-movement commands utilizing escape sequences. Up, down, right, and left movements, plus 8-space tabbing are allowed.

The full screen, as well as individual characters and lines, can be erased by using simple "ESCape" commands (an escape character followed by another character). Line speeds of up to 9600 baud allow high-speed display of, and interaction with, the terminal's character and graphic displays.

At high baud rates, the operator can freeze data transmission with the SCROLL key. When the bottom line of text on the screen is displayed, and the cursor is directed to move to the next line, the top line of text automatically "scrolls" off the screen to allow space for the new line.



VT55 Graphics Terminals

When receiving data at high baud rates, this scrolling can occur so rapidly that a visual inspection of screen information is impossible. The VT55 allows scrolling to be controlled at the terminal. When the screen is full, transmission stops until the SCROLL key is pressed, signaling that the operator is ready to proceed.

Two control dials let the operator select transmission rates from 75 to 9600 baud (75, 110, 150, 300, 600, 1200, 2400, 4800, and 9600). These controls can be set separately so that some reception and transmission speeds can be mixed.

VT55 Copier

The new electrolytic copier, located on the side of the terminal, prints line-for-line images of the text and graphics that are displayed on the screen.

To copy all lines currently on the screen, the operator simply presses the COPY key. The terminal tells the host computer to wait (sends XOFF code) and normal operations will resume after the copying is done (terminal sends XON code). This operation can also be initiated by the computer program.

VT55 Keyboard

The VT55 keyboard is built to a universally accepted standard—the office typewriter. Its layout, stroke and touch are familiar to any typist, thereby maintaining the training and familiarization period to an absolute minimum, without sacrificing accuracy and speed.

The VT55 does not require cooling fans. In noise-sensitive locations, therefore, the VT55 can operate in absolute silence. When silence is not necessary, the operator simply turns on an audible response switch to produce a keystroke click that encourages rhythmic, high-throughput keying.

The VT55 keyboard features three-key rollover construction that encourages operator speed by eliminating errors due to striking multiple keys.

SPECIFICATIONS

Cabinet dimensions	—Height	14.1 in (36 cm.)
	—Width	20.9 in (53 cm.)
	—Depth	27.2 in (69 cm.)
	—Minimum Table depth	17.7 in (45 cm.)
System weight	—With copier	57 lbs (25.8 Kg.)
	—Without copier	49 lbs (22.2 Kg.)
Operating environment		
(models without copier)		
	—Temperature	50°F (10°C) 104°F (40°C)
	—Humidity	10%—90% (non-condensing)
(models with copier)		
	—Temperature	59°F (15°C) 90°F (32°C)
	—Humidity	20%—80% (non-condensing)
Non-operating environment	—Temperature	—40°F (—40°C) 151°F (66°C)
	—Humidity	0%—95% (non-condensing
	115 Vac @ 1.5A 230 Vac @ 0.7A	
Fault Protection	Circuit breaker	
Power Cord Length	9 feet (2.74 meters)	
Video Display		
	Size	12 in. (30.5cm) diagonal
	Active	8.0 in. x 5.0 in. (20.3cm x
	Screen Size	12.7cm)
	Method	Raster scan, roll-free
	Phosphor	±½ point
	Linearity	P4

Alphanumerics	Character lines	24
	Character columns	80
	Control	Blinking alpha—cursor,
	Character set	64 character upper case ASCII subset plus 32 control characters.
	Special features	Upward scroll, bell, erase, tabulate, cursor control, buzzer on 73rd typed character on a line.
	Character matrix	5 x 7
Graphics resolution		512 horizontal x 236 vertical points
	Graphs or histograms	Two single valued functions of x, each individually controlled.
	Grid	512 vertical lines and 236 horizontal lines each line individually controlled.
	Graphical cursor	512 per graph, total of 1024. Each graphical cursor is individually controllable.
	Special features	Individual blanking and unblanking of all graphics features, clear all graphics.
	Hold screen mode	Allows interruption of data transmission for extended display viewing.
	Terminal identifier	Terminal will respond with ESC/C when receiving ESC Z.
Keyboard	Format	ANSI x 4.14-1971 standard typewriter keyboard.
	Keyclick	Audible feedback on each keystroke.
	Error correction	Three key- rollover to reduce errors caused by fast typing.
	Special keys	Extra control keys for special and commonly used control functions includes ESC, TAB, PAGE CONT, BACK SPACE, BREAK, LINE FEED, RETURN, AUTO PRINT.
User Controls	Intensity	Variable to adjust character and graphics brightness.

	PARITY	Even or no parity, switch selectable.
	EIA	EIA/20mA. switch selectable (with EIA option).
	KEY CLICK disable	Switch disables keyclick for quiet environments.
	Power/Logic Reset	Line voltage on and off, and resets unit to alphanumeric mode.
	Baud rate/interface mode	Allows choice of baud rate, full duplex, full duplex with local copy, and local mode with rotary switches.
Copier	Image copied	Display on screen less the alphanumeric cursor.
	Time per print	Approximately 25 seconds per copy.
	Copy size	Approximately 3 in. (7.62cm).
	Paper roll size	120 feet (36.5 meters) long by 3½ in. (8.89cm.) wide.
	Character format	5 x 7 dot matrix.
	Graph field	512 point horizontal x 236 point vertical.

Interface Specifications

Type		20mA. current loop standard, EIA interface optional.
Speed	—Full Duplex	75, 110, 150, 300, 600, 1200, 2400, 4800 and 9600 Baud.
	—Full duplex with local copy	110, 600, 1200, 2400, 4800 and 9600 Baud.
	—Full duplex split speeds	Transmission at 75, 150, or 300 Baud with reception at any of 600, 1200, 2400, 4800 or 9600 Baud.
Transmission	—10 bit length	75, 15, 300, 600, 1200, 2400, 4800, and 9600 Baud.
	—11 bit length	110 Baud only.
	—parity	Generated on transmission as even parity or a mark (no parity—switch selectable). Parity is not checked on reception.

Supplied cable length	—20mA.	13.1 feet (4 meters).
	—EIA option	25 feet (7.6 meters).
Maximum cable length	—20mA.	1000 feet (304.8 meters).
	—EIA option	50 feet (15.2 meters).

The DCK8-AA SLU, KL8-A, or KL8J-A may be used to provide the interface between the VT55 and the PDP-8/A.

VIDEO TERMINAL, VT61

DESCRIPTION

The VT61 is a microprocessor-driven ASCII video terminal suitable for interactive, block, form-filling, and text-editing applications. Its over 80 commands include text-editing and justification, reverse-video and protected forms, and output to "sub-peripheral" hardcopy devices controlled by the VT61. The VT61 can be operated in Conversational Mode, in which each character typed is sent to the host computer, or in Block Mode, where the operator enters and edits text without interacting with the host computer, and then transmits it a block at a time to the host.

Modes: Software-Controlled Terminal Settings

An example of the exceptional versatility of the VT61 is its 18 "Modes". A Mode is a special setting of the terminal which takes effect on command and remains in effect until canceled. Modes can be enabled and disabled by software, and provisions exist to allow the operator to set the terminal in the most common Modes. Some Modes will typically be set once at power-up by software to adjust the terminal to the computing environment. For example, the VT61 can be set to treat the octal code 012 as either "Line Feed" or "New Line", depending on its implementation in the computer system. Some Modes can be set by application software to adapt the terminal's use to that application. A program could place the VT61 in a Mode in which each key on the 19-key numeric pad transmits a unique Escape Sequence, allowing redefinition by applications programs. Some Modes are set and reset as necessary by the operator—such as Insert Mode, which determines whether new text entered into the screen will destroy old text already on the screen, or move the old text over to make room.

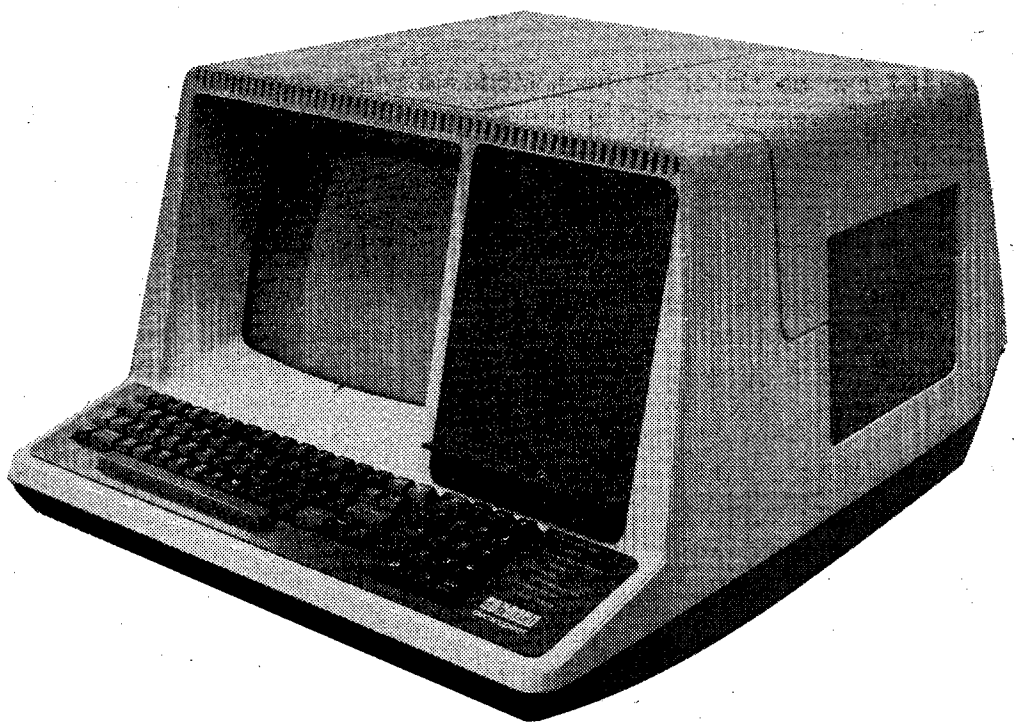
To adjust such settings, or to invoke other terminal commands, the operator types a special "Function" key followed by a regular alphabetic key. Labels on the alphabetic keys give the operator a "menu" of functions he can invoke, while limiting the number of special command keys that he must cope with.

Synchronization Prevents Data Loss

Like the VT50-series terminals, the VT61 uses the XOFF and XON control codes to request that the host suspend and resume its transmission. These signals, and a small input buffer called the Silo, make filler characters or other programmed delays obsolete, prevent data loss, and allow the VT61 to pass data to slower hardcopy devices and execute time-consuming editing functions. (When transmitting a block of data to the CPU, the VT61 will respond to the same XOFF and XON signals, so that the computer can take the data from the VT61 at its own rate.)

Printer or Copier Controlled by the VT61

The user can select from two hardcopy devices which can be controlled by the VT61. The integral electrolytic copier is useful for quick con-



VT61 Video Terminal

firmations, recalling instructions, and listing programs. It is a low-cost alternative to buying a separate teleprinter, and allows users who need occasional hardcopy to enjoy the speed and efficiency of a video terminal. The copier is an extra-cost option of the VT61. When use of paper is heavy or a higher-quality output is required, the VT61 provides a parallel interface to an LA180 printer. Data from the screen may be printed a line or a page at a time. In addition, software may place the VT61 in a Mode in which it becomes a remote printer-controller, passing all characters received through to the printer without disturbing the display. This allows programmers to use all 132 columns of the printer, despite the 80-character width limitation of the screen. The printer interface is standard on all models of the VT61; the printer is ordered separately.

THE VT61 AS A COMMUNICATIONS TERMINAL

The VT61 ordinarily operates in a Full Duplex environment. Data entered from the keyboard is sent to the host; data received from the host is displayed on the screen. Any character on the screen may be displayed in normal video (light on dark) or reverse video (dark on light). The computer typically puts reverse-video information on the screen by

placing the terminal in the Reverse-Video Mode, in which all characters received are deposited in the screen in reverse video. The operator typically invokes the Change Emphasis function to convert text on the screen to reverse-video.

Block Mode
The VT61 can be placed in Block Mode, in which the operator uses the keyboard to create and edit information on the screen in a simulated "Off-Line" environment. When the operator has prepared the data on the screen, one of the TRANSMIT keys is used to send the information to the computer. The computer is thus relieved of error-correcting and pre-processing duties.

Transmissions to the Host
The various TRANSMIT functions allow the computer to request the contents of any selected area on the screen, the data at the cursor position or on the cursor line, the data past the cursor to the end of the screen, the entire contents of the screen, and the following additional information about the terminal:

Where the cursor is;
What the character shifted off the screen is;
Whether a hard output error occurred at the terminal's sub-peripherals, the printer or the copier;
Whether the terminal is a VT61, as opposed to a VT50 or VT52;
Whether a printer or copier is attached to the terminal.

Checksums
In addition, the VT61 computes checksums based on every significant character received from or transmitted to the computer, and the host can request the contents of either the Transmitter Checksum Register or the Receiver Checksum Register. The computer may also command the terminal to clear either register.

Null Data Included or Suppressed
The VT61 provides several different formats to allow the computer to determine the location of the transmitted information on the screen. In Character Format, the terminal transmits the contents of each position on the screen, allowing the computer to distinguish between Spaces which were explicitly entered into the screen, and NUL characters, which occupy the screen by default. In Line Format, NULs are omitted in the transmission, so that only characters which the terminal regards as significant as text are transmitted. To mark the end of a screen-line of text, the terminal sends a line-delimiter. Software may select either CR or LF (NL) to be this marker.

Requesting Spontaneous Notification
The computer places the terminal in Transmit-Request Mode to specify that the terminal should notify the computer on an unsolicited basis whenever a situation occurs in which the computer may want to take special action. Such situations are: a hard error at a sub-peripheral, powering-up of the terminal, or, in Block Mode, action by the operator

which caused a character to be shifted off the end of the screen, or action which would have caused a scroll of the display.

Host Can Regulate Output from Terminal
In Transmit-Request Mode and Block Mode, whenever the operator invokes a COPY, PRINT, or TRANSMIT command, the terminal transmits a "Request" to the computer instead of performing the specified output. The computer can initiate the transmission when it is ready. This allows the CPU to postpone a transmission from the terminal until resources for handling that transmission become available, and increases the CPU's efficiency in handling multiple terminals.

Two-Way Transmission Control
Once a transmission from the terminal is under way, the computer may use the Full Duplex synchronization signals XOFF and XON to moderate the data flow from the terminal. The terminal will promptly suspend all transmissions when it receives XOFF from the host, and resume them from where they were suspended when it receives XON. The terminal will send the same XOFF and XON signals to the host under a variety of conditions in which processing of input to the terminal must be temporarily suspended, as the VT50-series terminals do; and to prevent data loss during any latency period in the computer's responses to XOFF, it buffers incoming characters in a small input buffer called the Silo.

Locking the Keyboard
The computer can lock and unlock the terminal's keyboard at any time. In addition, the computer can set the VT61 to implicitly lock at the end of every transmission, allowing the computer to take additional action before allowing data entry to continue. The computer might typically verify the checksum of the transmission, or display new data on the screen, before unlocking the keyboard.

Half Duplex Control
If the appropriate interface option is selected, the VT61 will operate in a true Half Duplex environment, using the control signals CTS, SRD, STD, DTR, RTS, and CD to communicate with a type 103 or 202 modem with a secondary channel.

Local Loop
To work compatibly with software written for a Half Duplex environment but running in Full Duplex, in which the computer does not "echo" typed characters back to the screen, the terminal may be set via an easily-accessible switch to Local Loop, in which this function is done in hardware. (This setting poses some programming and operating constraints.)

THE VT61 AS A BUSINESS TERMINAL

Auxiliary Keypad—Numeric or User-Defined
The VT61 provides a 19-key auxiliary keypad to the right of the main keyboard. In its normal state, 10 of the keypad keys transmit codes for

the numerals which are indistinguishable from the codes the numeric keys on the main keyboard transmit. A decimal point and ENTER (CR) key are also available. Therefore, the operator can use the convenient "calculator-keyboard" format to speed entry of numeric data, but software need not be rewritten to support the keypad.

At other times, it is advantageous for the computer to be able to differentiate between the typing of keys on the auxiliary keypad and typing of similar keys on the main keyboard. Software may place the terminal in Editing-Keypad Mode, in which each of the numeric keys transmits a unique, three-character Escape Sequence to the computer. (When the terminal is also in Block Mode, the keypad may be used to perform common editing functions with a single keystroke.)

The other seven keys on the keyboard generate Escape Sequences at all times. In a Full Duplex setting, these seven keys can likewise be relabeled and user-defined; however, if the codes generated by these keys are returned to the terminal, the terminal will take special action. Four of these keys are labeled with an arrow, and will cause the cursor to move one position in the specified direction.

Protected Forms
When the VT61 is placed in Forms Mode, all the reverse-video characters then on the screen become "protected". The terminal will ring its bell if the operator tries to type data into a protected field, although the terminal will allow the cursor to be moved through a protected field. The Forms Mode commands (Forward Field, Backward Field, Erase to End-of-Field, and Transmit Field) are provided, with the TAB key invoking the Forward Field command. The terminal has TRANSMIT functions which will send to the host the entire contents of the screen (protected "form" as well as unprotected "responses"), the data in a specific field, or all unprotected data only, with TAB characters used to separate unprotected fields.

Automatic Tabbing to Next Field
The host may set the VT61 to automatically move the cursor to the start of the next field when data is entered into the last character in a field.

32 Special Graphic Characters
The VT61 has the capability to store 32 characters in its screen in addition to the ASCII character set. The VT61 can be placed in a Mode in which codes for the lower-case letters will instead call out one of the special symbols. Ten of these symbols are displayed as the subscripts zero through nine. Four others are displayed as "1/", "3/", "5/", and "7/". By preceding one of the subscripts with one of these four characters, fractions from 1/8 to 7/8 can be displayed on the screen. Eight other control codes in the screen are displayed as horizontal bars at various heights within the character position. This feature allows a graph to be plotted on the screen. The magnitude being graphed can be represented not only by which text line a bar occurs on, but by how

far up within that text line the bar is located. A slight vertical distortion is produced by the fact that bars can be displayed on only eight of the ten video scans which comprise one text line.

THE VT61 AS A TEXT EDITING TERMINAL

Character- and Line-Insertion and Deletion

The VT61 provides insertion and deletion on a line-at-a-time or character-at-a-time basis. Inserting characters is done by placing the terminal in Insert Mode. All text received when the terminal is in Insert Mode move the previous text to the right rather than replacing it with the new text. This Mode can be entered and exited from the keyboard. Also available at the keyboard are the Delete Character function, and the functions Insert Line and Delete Line. These functions cause line-rippling to occur below the cursor: Insert Line shifts text below the cursor down one line, and Delete Line shifts it up one line. Two additional line-movement functions can be invoked by the computer which affect the text above the cursor: an Insert Line function which ripples that text upward, and a Delete Line function which moves it downward. Using these four line-movement commands in Full Duplex, the computer can maintain a "split-screen" display, arbitrarily dividing the screen horizontally into an upper and a lower half and scrolling each half separately without causing the other half to flicker even momentarily. For instance, one half of the screen might be used by software to display instructions or a list of the functions currently available, while the other half is the "conversational" portion where the operator can see the result of the most recent interactions with the computer.

Host Can Set or Read Cursor Position

The computer can further subdivide the screen into small pieces, using each to display the status of a single event. The computer uses the Direct Cursor Addressing command to move the cursor to any position on the screen regardless of its previous position. Thus, to update any piece of the screen, it is necessary to rewrite only that much of the screen.

In addition, the terminal will transmit to the host on command the coordinates of the cursor, so that the host can alter various parts of the display and return the cursor to its original position.

Text Justification

When the VT61 is used as a text-editing terminal, the operator will enter text into the screen without regard to the position of the cursor. When the cursor reaches the end of a line, it will wrap around to the beginning of the next line down. Some words will be split between lines on the screen. The Text Justify function rectifies this situation, by causing all such words to wrap completely around to the next line down. After the Text Justify function is completed, the screen is left in an aesthetic, left-justified format with ragged right margins.

Justification Markers

The only time during text entry that the operator will type the RETURN key is to signify that subsequent text must always be forced to the next

line—in other words, to mark the beginning of a new paragraph. Typing the RETURN key places a Paragraph Marker in the screen, which the Text Justify operation responds to by in fact pushing all subsequent text forward to the next line. The TAB key stores a Tab Marker in the screen, and pushes subsequent text forward to the next TAB stop. Columnar data formed using TAB is restored to its columnar appearance by the Text Justify function, even if character insertions or deletions had disturbed the formatting.

The REPEAT Key and Auto-Repeating Keys

Any key may be made to repeat by holding down the REPEAT key on the keyboard along with the desired key. In addition, certain keys on the keyboard are "auto-repeating": After a 1/2-second delay, these keys will begin to repeat, just as if the REPEAT key were down. Auto-repeating keys include the Space bar and the BACK SPACE key, as well as the text-editing keys on the auxiliary keypad.

VT61 COMMANDS

1. Control Codes

OCTAL CODE	NAME	USE
000 177	NUL DEL	NUL and DEL are ignored by the terminal to support software written for slower electromechanical devices which use these codes as fillers.
002	STX	Begins messages
004	EOT	Ends messages
007	BEL	Sounds the audible alarm
010	BS	Backspace—same as the Cursor Left command
011	TAB	TAB command: Normally, a cursor movement command. In Block Mode, a formatting command.
012	LF	Line feed
012	NL	New line (Carriage return + line feed) (If VT61 has been set to New Line Mode by software)
015	CR	Carriage Return
023	XOFF	Sent by either device to request that other device suspend its transmission
021	XON	Sent by either device to request that other device resume its transmission
033	ESC	Escape introduces multiple-character commands from following list

2. Two-Character Escape Sequences

SEQUENCE	MEANING
ESC =	ENTERs Alternate-Keypad Mode. Each of the 19 keys on the auxiliary keypad will transmit a unique Escape Se-

2. Two-Character Escape Sequences

SEQUENCE	MEANING
	quence, which can be defined by software. In Block Mode, the 19 keys invoke predefined editing functions.
ESC >	EXITs Alternate-Keypad Mode. The numerical keys and decimal point key on the auxiliary keypad will be indistinguishable to software from corresponding keys on the main keyboard.
ESC ?	An introducer; see Group 6.
ESC A	Moves the cursor up one line unless it was at the top of the screen.
ESC B	Moves the cursor down one line unless it was at the bottom of the screen.
ESC C	Moves the cursor right one column (nondestructively) unless it was at the right end of a line.
ESC D	Moves the cursor left one column unless it was at the start of a line.
ESC F	ENTERs Graphics Mode. Lower-case letters received by a VT61 in Graphics Mode will be converted to one of 32 Special Graphic Characters before being placed in the screen. These Special Characters are seen on the screen as subscripts, horizontal bars at various heights, fractions, and assorted mathematical symbols.
ESC G	EXITs Graphics Mode. Lower-case codes cause lower-case letters to be seen on the screen; Special Graphic Characters already entered in the screen do not change their appearance.
ESC H	Moves the cursor HOME—to the upper left corner of the screen.
ESC I	Moves the cursor up one line, performing a downward scroll if the cursor was on the top line (Reverse Line Feed).
ESC J	Erases from the cursor position to the end of the screen.
ESC K	Erases from the cursor position to the end of the same line.
ESC O	An introducer; see Group 3.
ESC P	An introducer; see Group 4.
ESC Q	In Forms Mode, moves the cursor to the start of the previous field.
ESC R	In Forms Mode, moves the cursor to the start of the following field.
ESC V	Outputs the line containing the cursor to hardcopy.
ESC W	ENTERs Printer-Controller Mode. All characters received from the host are passed through to the parallel printer interface.
ESC X	EXITs Printer-Controller Mode.
ESC Y	Direct Cursor Addressing command; see Group 5.

2. Two-Character Escape Sequences

SEQUENCE	MEANING
ESC Z	Causes the VT61 to transmit a three-character Escape Sequence (see Group 7) to the host to uniquely identify its model and configuration.
ESC [	ENTERs Hold-Screen Mode. No scrolls will be performed until the operator types the SCROLL key. (The terminal will buffer incoming data and send XOFF to the host to request it to suspend transmission.)
ESC \	EXITs Hold-Screen Mode. Scrolls can occur freely without special action by the terminal.
ESC]	Outputs the entire screen to hardcopy.
ESC —	ENTERs Auto-Copy Mode. A line will be automatically output to hardcopy whenever the cursor moves downward off that line. Used for copying variable-length files.
ESC _	EXITs Auto-Copy Mode.

3. The ESC O Group

SEQUENCE	MEANING
ESC O A	ENTERs Maintenance Mode. Each key on either keyboard will transmit its octal key-address instead of an ASCII code; Maintenance Mode will be implemented identically on customized versions of the VT61.
ESC O a	EXITs Maintenance Mode.
ESC O B	ENTERs Block Mode. The keyboard can be used to enter and edit text on the screen in a simulated "off-line" environment, requiring no processing time from the host computer. When satisfactory text has been generated, it can be transmitted to the host by invoking one of the TRANSMIT commands.
ESC O b	EXITs Block Mode. The keyboard functions only to transmit codes to the host, character-at-a-time as keys are typed; functions are executed by the terminal only when codes are received from the host (or by enabling the Local Loop from keyboard to receiver).
ESC O C	ENTERs Linear-Addressing Mode. The cursor will automatically wrap around to the next line when it reaches the end of a line.
ESC O c	EXITs Linear-Addressing Mode. The cursor will remain at the end of a line until explicitly repositioned.
ESC O D	ENTERs New-Line Mode. The terminal will use octal 012 as its line delimiter, in block-transmissions and when the RETURN key is typed. 012 on receipt by the terminal

3. The ESC O Group

SEQUENCE	MEANING
	will be sufficient to move the cursor to the start of the next line.
ESC O d	EXITs New-Line Mode. The terminal will use octal 015 as its line delimiter, in block-transmissions and when the RETURN key is typed. Carriage Return and Line Feed must both be sent to move the cursor to the start of the next line.
ESC O E	Locks the keyboard. In true Half-Duplex environments, the BREAK key will remain operative. The operator is alerted that this action has been taken by illumination of an LED on the console, and by absence of the key-click sound. The VT61 can be set to lock the keyboard automatically after each transmission to the host.
ESC O e	Unlocks the keyboard.
ESC O F	ENTERs Forms Mode. Characters which appear on the screen in reverse-video become "protected," and cannot be modified, deleted, or moved.
ESC O f	EXITs Forms Mode. Reverse-video characters may be placed in the screen, moved, and deleted without restriction by the terminal.
ESC O G	ENTERs Alarm Mode. The entire screen oscillates between normal and reverse-video. This allows the operator to be alerted in environments where the audible alarm might be ineffective.
ESC O g	EXITs Alarm Mode.
ESC O H	ENTERs Transmit-Request Mode. All automatic messages from terminal to host are bracketed by STX and EDT. In Block Mode, the VT61 sends a "request" Escape Sequence to the host whenever the operator invokes a TRANSMIT function from the keyboard, and requires confirmation from the host before the transmission will commence.
ESC O h	EXITs Transmit-Request Mode.
ESC O I	ENTERs Auto-Tab Mode. In Forms Mode, the cursor will automatically advance to the start of the next field when the last position in a field is filled.
ESC O i	EXITS Auto-Tab Mode. In Forms Mode, after the last position in a field is filled, the cursor will enter the protected field and will sound the audible alarm if additional characters are typed until the cursor is explicitly moved.
ESC O J	ENTERs Reverse-Video Mode. All subsequently received characters will be displayed in reverse-video.
ESC O j	EXITs Reverse-Video Mode. All subsequently received characters will be displayed in normal (light-on-dark) video.

3. The ESC O Group

SEQUENCE	MEANING
ESC O N	Deletes the line containing the cursor. All text above that line is moved down one line.
ESC O O	Creates a new line at the cursor. All text above that line is moved up one line in order to make room.
ESC O P	Defines the current cursor location as the start of the Selected Area.
ESC O Q	Defines the current cursor location as the end of the Selected Area.
ESC O R	Resets the terminal to its initial state. All modes are EXITed, the screen is erased, and the cursor is moved HOME.
ESC O S	The Selected Area is transmitted to the host.
ESC O T	The VT61 invokes a routine which verifies the integrity of the entire microprogram, verifies the operation of the Random-Access Memory, and exercises a large portion of the terminal.
ESC O V	The entire screen is transmitted to the host.
ESC O W	The character at the cursor position is transmitted to the host.
ESC O X	The contents of the Overflow Buffer are transmitted to the host.
ESC O Y	The current position of the cursor is transmitted to the host.
ESC O Z	In Half-Duplex environments, the terminal attempts to gain control of the transmission line.
ESC O [	The Receiver Checksum is set to zero.
ESC O \	The Transmitter Checksum is set to zero.
ESC O]	The Receiver Checksum is transmitted to the host.
ESC O ‾	The Transmitter Checksum is transmitted to the host.
ESC O _	The Output Abort Flag is initialized.
ESC O '	The status of the Output Abort Flag is transmitted to the host. This allows the host to determine which sub-peripheral was the location of the most recent hard error.
ESC O x	Transmitted to the host by the terminal on command to report that no outputs have been aborted since the flag was last initialized.
ESC O y	Transmitted to the host by the terminal to report a hard error at the electrolytic copier.
ESC O z	Transmitted to the host by the terminal to report a hard error at the printer.
ESC O (	On VT61s set to power-up to Block Mode, transmitted to the host by the terminal to indicate that it has been switched on or that a power failure has occurred.
ESC O |	In Block Mode and Transmit-Request Mode, sent to the

3. The ESC O Group

SEQUENCE	MEANING
	host by the terminal to indicate that the operator has tried to scroll the display and special action by the host may be necessary.
ESC O)	In Block Mode and Transmit-Request Mode, sent to the host by the terminal to indicate that text has shifted off the screen and can be recovered if the host takes proper action.

4. The ESC P Group

NOTE: THE FCN key on the auxiliary keypad is used by the operator to generate ESC P. The Escape Sequences in this group will typically originate from the operator as well as from software. The operator types FCN followed by an alphabetic key. The key may be either shifted or unshifted, except for Mode commands. In Mode commands, the alphabetic key must be shifted in order to ENTER a Mode, and unshifted in order to EXIT a Mode.

SEQUENCE	MEANING
ESC P <numeral>	Reserved for definition by software. In Block Mode, whenever the operator types FCN followed by a numeral key, a message of this form is sent to the host.
ESC P A or a	Inserts a Paragraph Delimiter in the screen. The Paragraph Delimiter is a formatting marker used by the Text Justify operation.
ESC P B or b	The line containing the cursor is transmitted to the host.
ESC P C or c	The "ruler" is written over the cursor line. The ruler is a line of numbers. The numbers 1 through 0 are repeated, alternating between normal and reverse-video, making it easy for the operator to determine which column the cursor is in.
ESC P D or d	Deletes the line containing the cursor. All text below that line is moved up one line.
ESC P E or e	The emphasis (normal or reverse-video) of the character at the cursor position is changed or complemented. Then the cursor is moved rightward.
ESC P F or f	Creates a new line at the cursor. All text below that line is moved down one line in order to make room.
ESC P G or g	The line containing the cursor is output to hardcopy.
ESC P H or h	The entire screen is output to the parallel printer interface.
ESC P I	ENTERs Insert Mode. Text entered into the screen will

SEQUENCE	MEANING
	shift to the right the text that was already in the screen.
ESC P i	EXITs Insert Mode. Text entered into the screen will destroy the text formerly located at the same positions.
ESC P J or j	The line containing the cursor is output to the parallel printer.
ESC P K	ENTERs Alternate-Keypad Mode (Same as ESC =)
ESC P k	EXITs Alternate-Keypad Mode (Same as ESC >)
ESC P M or m	A "message" is transmitted to the host. The area of the message will be defined so that it does not include any data previously transmitted as a message. A message delimiter will be placed in the screen.
ESC P N or n	All data from the cursor position to the end of the screen is transmitted to the host. In Forms Mode, this command will transmit only the operator's responses to the protected form, and not the form itself.
ESC P Q or q	The cursor moves HOME.
ESC P R or r	Text preceding the cursor in the screen is erased, then a Text Justify operation (ESC P V) is performed.
ESC P S or s	The character at the cursor position is deleted. Text to the right moves leftward to take up the space.
ESC P T or t	A Command Delimiter is inserted in the screen. The operator will typically type after the Command Delimiter a string of characters which is meaningful to the software, and then invoke the Transmit Message command. The "message" will then be this string, and the VT61, in transmitting it, will identify it to software as a "command."
ESC P U	ENTERs Hold-Screen Mode.
ESC P u	EXITs Hold-Screen Mode.
ESC P V or v	Performs a Text Justify function. Any words which, due to automatic line wraparound, were split between lines are moved completely to the lower line; text following a TAB marker is shifted rightward to the next TAB stop; text following a Paragraph Delimiter is shifted rightward to the beginning of the next line.
ESC P W or w	Positions the cursor past the last data character in the screen. Also invoked upon the completion of a Justify function.
ESC P X or x	Erases characters from the cursor to the end of the same line.
ESC P Y	ENTERs Auto-Print Mode.
ESC P y	EXITs Auto-Print Mode.
ESC P Z or z	Erases characters from the cursor to the end of the screen.

SEQUENCE	MEANING
ESC P \	Not to be assigned.
ESC P |	Not to be assigned. (The operator types the \ key, labeled "Cancel," to cancel a partially-entered FCN-sequence.)

5. ESC Y

The Direct Cursor Addressing command is immediately followed by two parameters, the first of which selects a line on the screen, the second of which selects a column. The effect is that the cursor is positioned at the selected row and column of the screen. The legal range for the first parameter is 040–067; the second parameter may range from 040 to 157.

ESC Y 040 040 selects column 1 of line 1; its effect is the same as that of the HOME command, ESC H

6. The ESC ? Group

When the terminal is in Alternate-Keypad Mode but not in Block Mode,

the key labeled . . .	transmits the Escape Sequence . . .
0/Delete Char	ESC ? p
1/TxJus	ESC ? q
2/XmMsg	ESC ? r
3/Cmd	ESC ? s
4/F3	ESC ? t
5/F4	ESC ? u
6/I/R	ESC ? v
7/F1	ESC ? w
8/F2	ESC ? x
9/Home	ESC ? y
./CEmph	ESC ? n
ENTER/XmDat	ESC ? M

ESC ? s is also used by the Transmit Message function to identify a message as a "command" to software (having detected a Command Delimiter in the screen).

7. RESPONSES TO ESC Z

ESC / ' I am a VT61 without copier or printer.
ESC / a I am a VT61 with copier but no printer.
ESC / b I am a VT61 with printer but no copier.
ESC / c I am a VT61 with printer and copier.

All VT50-series terminals respond to ESC Z with different Escape Sequences of the same format.

SPECIFICATIONS

Display	Cathode Ray Tube—12" diagonal measure
Display Format	24 lines of 80 characters (1920 characters)
Character Set	96-character displayable ASCII set: Includes upper-, lower-case, numerals, symbols, 32 special graphic characters including 8 scaled horizontal bars
Character Format	7x8 dot matrix in 10x10 area; one-scan descenders
Alternate Video Setting	Reduced-intensity reverse-video characters intermixable with regular characters
Keyboard	DEC Standard Keyboard
Transmittable Characters	ANY pattern of 7 bits—Upper-, lower-case, numerals, symbols, control codes
Auxiliary keypad	19-keys; Two modes make it suitable for Numeric Data Entry or Text Editing
Interface Settings	Standard; switch-selectable
Half-Duplex	103 Dataset, 202 Dataset and Current Loop
Parity	Even/odd/none
Variable Speeds	Transmission and reception at 75 to 9600 Baud
Split Speeds	Transmission at 75/110/150/300/600 Baud with reception at 1200/1800/2400/4800/9600 Baud
Interface Hardware	Choice of: 20mA Current Loop—Mate 'N Lok (R) connector 20mA Current Loop—4-pin telephone plug EIA Connector for Full Duplex Operation EIA Connector with Half Duplex Control Signals Slot for DF11BA or DF11BB Integral Modem Cards
Copier (Optional)	Electrolytic type
Character Set and Format	Same as display
Width	80 columns
Page Size	Variable (continuous paper roll)
Printer (Optional)	LA180 or equivalent (adapter to drive a serial printer will be available)
Character Set and Format	Device-dependent; lower-case supported by VT61
Width	At least 80 columns required
Modes	Software-controlled options
Block Mode	Simulated off-line editing environment

CHAPTER 10

OPERATING SYSTEMS AND SOFTWARE

10.1 PDP-8/A OPERATING SYSTEMS AND SOFTWARE

One of the most common problems encountered during design and implementation of computer systems is that program development and software support often cost more in terms of both time and money, than the hardware. To alleviate this problem for users, Digital Equipment Corporation maintains a library of more than 2000 user written and maintained programs, ranging from sophisticated applications routines for limited markets, to complete operating systems. No matter how exotic or innovative a particular application may appear, chances are that a significant portion of the requisite supporting software is already available, along with full documentation which generally includes binary and source language tapes, listings, instruction manuals, execution timing summaries and a frank appraisal of worst-case interactions.

PDP-8/A software is designed to provide maximum adaptability and reduce early obsolescence. Most programs and packages will run on a wide variety of hardware configurations, including non-standard peripheral devices and, often, without reassembly or recompilation. The OS/8 operating system, for example, may be used with virtually any peripheral device by simply coding a 1- or 2-page device handler and adding it to the library of standard device handlers supplied with the system.

Many widely-accepted programming languages are supported on the PDP-8/A including FORTRAN IV and full standard Dartmouth College BASIC (two versions). Timesharing, full I/O device independence, and real-time support are among the capabilities available to every PDP-8/A user. The remainder of this chapter contains brief descriptions of a selection of PDP-8/A programs and software packages. This is not, by any means, an exhaustive summary of available software. It is intended to illustrate the powerful features of standard PDP-8/A programs and systems with an emphasis on newly-released software products.

10.2 RTS-8

RTS-8 (Real-Time System for PDP-8/A) allows up to 63 non-resident or memory resident tasks to run concurrently, sharing resources on a fixed priority basis. The RTS-8 monitor supports intertask communication, task synchronization, and task scheduling. RTS-8 also includes system tasks that control most standard DIGITAL peripheral devices, an interactive monitor console routine, and a task that allows a module of OS/8 to run in the background, creating a foreground/background real-time development system.

The RTS-8 Monitor Console Routine (MCR) allows the operator at the system console to request the execution of any task in the system or

suspend the execution of any task that has been started. Tasks may be scheduled for execution at a specified time of day or at specified time intervals. Each task installed in the system is identified by a four character name. The MCR allows the operator to examine the contents of one or more consecutive memory locations or to deposit data in one or more consecutive memory locations.

The date and time of day can be entered into the system or read from the system once it has been entered. All tasks that have been scheduled use this time for real-time task scheduling. At any time the user may request to return to the OS-8 system and perform development under OS/8.

I/O Tasks—A full complement of peripherals will be supported including the RK8-E, TC08, TA8-E, DK8-EC, DK8-EP, ICS8, LA8, LA36, RX8-E, VT50, and VT52. (See Chapter 9 for a list of peripherals.)

OS/8 Background Module—Users with 12K or more of read/write memory, and timeshare hardware (on the KM8-A or KM8-E extended option-board) are able to develop new tasks in the background in parallel with foreground execution. All the standard OS/8 programs may be run with the exception of BUILD, Industrial Basic, and the run-time options for FORTRAN IV. If no foreground task performs I/O to the teletype, a second teletype is unnecessary. With 16K of core, OS/8 batch may be run in the background. The foreground tasks are protected from background jobs, but background jobs are not protected. OS/8 is treated as a task under RTS-8.

Minimum System Requirements For RTS-8

1. PDP-8/A central processor.
2. 4K of read/write memory (foreground only).
3. OS/8 for development (see OS/8 for requirements).

10.3 DECnet/8

A software package (DECnet/8) is being provided which runs under RTS-8 enabling the PDP-8/A to communicate with other PDP-8's, PDP-11's, PDP-15's and DECsystem 10 computers.

The basic function of DECnet is to provide a set of software tools making it easy for programs running in one computer to communicate with programs running in another. For example, the program controlling a machine tool, running in a dedicated mini, needs to be able to tell the parts flow program, running in the supervisory computer, that the tool has failed and hence cannot accept new work. The supervisory computer, once it has adjusted its parts flow, may in turn have to notify a master plant computer. DECnet makes this intercommunication easy by providing a simple, easy-to-use set of network commands.

The software, which is provided with DECnet/8, is controlled by simple commands that let the system or user application programs establish contact with remote DIGITAL computors and request data and/or commands.

DIGITAL users should contact their local sales office for specific information or availability and implementation.

10.4 OS/8 Operating System

OS/8 is a comprehensive library of system programs operating under the supervision of an integrated executive. This operating system is easily learned can run in a minimum of 8K read/write memory, and optimizes program development.

Programmers can use OS/8 to store data files or executable programs in a system library, where they may be accessed for loading, modification, or execution by means of console terminal keyboard commands. OS/8 provides for convenient program chaining so that a program may be divided into a set of smaller programs, each written in the language best suited to it. In the same manner, very large programs may be coded in small segments that can be overlaid during execution to conserve memory storage.

Programs written under OS/8 may be coded in a manner that allows complete I/O device independence. Program I/O is performed by standardized calls to system device handlers and by a comprehensive I/O supervisor called the User Service Routine. This feature permits programs to be written without regard for the characteristics of a particular I/O device. When a device independent program is executed, the user enters a run-time I/O specification command selecting the I/O devices to be employed during program execution, tailoring the I/O to a specific application or system configuration. When a system is expanded, programs use the new I/O capabilities to full advantage immediately—no rewriting or reassembly.

Logical names may be assigned to devices within the OS/8 system. This permits symbolic referencing of peripheral devices and makes certain classes of devices fully interchangeable from a programming standpoint. User programs retain full control over the length of I/O buffers to ensure optimum use of available storage and fast, efficient block data transfers.

OS/8 consists of an executive and a library of system programs. The executive, which supervises the execution of system programs, is composed of four major elements: the Keyboard Monitor, Command Decoder, User Service Routine, and I/O device handlers. The Keyboard Monitor accepts commands from the console terminal to Assign logical device names, to Load, Run, and Save system or user programs, and to Execute the "invisible" debugging routine, (so designated because it appears to the user as though it does not occupy any memory). These features of the keyboard monitor provide full communication between the user and the OS/8 executive by means of only seven monitor level commands.

The Command Decoder is called during execution of a system program or a device independent user program. It accepts a command line from the console terminal and decodes the command to determine what combination of input files, output files, and run-time options will be used during the current execution of the program. In this manner, I/O specification commands are standardized for most system programs greatly reducing the time required to become familiar with the system command structure.

The User Service Routine (USR) controls file directory operations under OS/8. Any system or user program may access the USR by executing a standard calling sequence. Functions performed by the USR include loading device handlers, searching file directories, creating, opening, and closing files, calling the command decoder, and program chaining.

The resident portion of OS/8 is only 256 locations, allowing maximum utilization of available storage for user programs or data. Nonresident portions of the system are swapped into memory from the system device automatically, as required.

The minimum configuration required for OS/8:

- 8K of read/write memory
- Terminal (ex: LA36)
- 64K of mass storage
- OS/8 batch (requires an additional 4K of read/write memory).

The library of OS/8 and OS/8 extension kit programs includes:

- EDIT, a line-oriented text editor.
- TECO, a powerful character-oriented text editor.
- PAL8, a symbolic assembler producing absolute code.
- SABR, a symbolic assembler producing relocatable code.
- BASIC, a compiler and run-time system that is especially fast and core efficient.
- BATCH, low priority background task.
- FORTRAN II, a complete programming system using the FORTRAN II compiler and the SABR symbolic assembler.
- FORTRAN IV, programming language with compiler which translates source programs into relocatable assembly language versions of the source program (available at extra cost).

In addition, the library includes a series of utility programs for copying, debugging, and loading programs. For more information about the OS/8 operating system, refer to the OS/8 Handbook (DEC-08-OSHBA-A-D), which can be obtained from Digital Equipment Corporation, Communications Services, 146 Main Street, Maynard, Massachusetts 01754.

10.5 CAPS-8

The cassette keyboard monitor system combines the convenience of a mass storage resident operating system with the economy and basic adaptability of a paper-tape system. Versatile, low-cost bulk storage is provided by the dual magnetic tape cassette drive and controller.

The cassette keyboard monitor accepts typed commands to load and run library programs, list tape directories, and perform various functions associated with cassette file management. System command structure is similar to that of OS/8, providing the same concise format and ease of use. The tape cassette serves as an unformatted, file-structured, bulk-storage device which contains the system executive along

with a library of system and user programs. Monitor level control is maintained by refreshing the memory-resident portion of the system executive from the cassette whenever necessary.

The library of programs for the CAPS-8 system includes:

- SYMBOLIC EDIT, a line and character oriented text editor.
- PALC ASSEMBLER, an assembler which accepts machine language files and produces absolute code.
- BASIC, a compiler and run-time system.
- SYSCOP allows the user to transfer and copy cassette files.

The minimum configuration for CAPS-8 consists of a PDP-8/A processor, 8K of read/write memory, a terminal, and a dual drive magnetic cassette (TA8-A).

10.6 PAPER-TAPE SYSTEMS

Paper-tape systems allow the input and output of data and programs to be performed using a paper-tape reader/punch and terminal. DIGITAL can supply the user with several software systems that may be used in this type of configuration.

The paper-tape system library includes:

- Symbolic Tape Editor, allows the user to prepare and edit symbolic tapes on-line in ASCII code with a terminal and/or paper-tape reader/punch.
- FOCAL, an interactive programming language used for problem solving, offering a full range of mathematical functions, input/output, and self-editing functions. FOCAL can also be used in a calculator mode approach to solve one-time-only problems without writing a conventional program.
- PAL III, a two-pass assembler with optional third pass that uses either high or low speed paper tape with console terminal I/O (ex: LA36). The optional third pass is used to produce a full symbolic program on the console terminal and/or paper tape.
- BASIC, a programming language which allows the user to solve problems without writing machine language programs, or to write programs and store them in memory or punch them on paper tape. The programs and solutions are printed out using the console printer.

  The minimum configuration for a paper-tape system is a PDP-8/A computer, 4K of read/write memory, a terminal, and paper-tape reader. To generate programs on paper tape a paper-tape punch is required.

More information about the software available for the PDP-8/A may be obtained from your nearest DIGITAL Sales Office.

PRODUCT	COMPILER/ ASSEMBLER SIZE	RUNTIME PACKAGE SIZE	MINIMUM STORAGE REQUIREMENTS	MAXIMUM STORAGE UTILIZED	COMPILATION/ ASSEMBLY SPEED
FOCAL DEC-08-AJAE	Not applicable	2.5K	4K	8K	Not applicable. (FOCAL is fully interpretive.)
8K BASIC (PDP-8 BASIC)	Not applicable	4K	8K	8K	Not applicable. (PDP-8 BASIC is fully interpretive.)
8K FORTRAN DEC-08-A2B1	5K	3.5K	8K	Compiler, 8K, Runtime, 32K.	From high speed paper tape 15–25 min.
PAL III Assembler DEC-08-ASC1	2K	—	4K	Assembler, 4K, Runtime, 32K.	From high speed paper tape, 3–15min. From low speed paper tape, 6–90 min.
PAL-D Assembler DEC-08-ASAC	3K	—	4K	Assembler, 4K, Runtime, 32K.	From DECdisk 10 sec–30 min.
MACRO-8 Assembler DEC-08-CMAB	3K	—	4K	4K	From high speed paper tape, 3–20 min. From low speed paper tape, 10 min.–2 hr.

8K SABR Assembler DEC-08-A2D2	5K	—	8K	Assembler, 8K. Run-time, 32K.	4 min. From DECdisk, 5 sec–2 min. From DECtape 30 sec–
Symbolic Editor DEC-08-ESAC-PB	—	—	4K	4K	—
ODT-8 Octal Debugging Program DEC-08-COC2-PB	—	—	3 pages (Loc. 7000–7577)	4K	—
23-Bit Floating Point Package DEC-08-NFPPA-PB	—	3K	—	Not applicable	—
Utility Programs	—	—	—	—	—

Summary

EXECUTION SPEED (RELATIVE)	PERIPHERALS/ OPTIONS REQUIRED	ADDITIONAL PERIPHERALS/ OPTIONS UTILIZED	FEATURES
Slow	LA36/ PC8-E or LT33D	PC8-E	• Easy to learn, easy to use. • Run large programs in 4K machine. • Immediate mode commands for fast problem solving and debugging. • Program may be stopped at any time–variables examined, etc., and then program execution resumed.
Medium	LA36/ PC8-E or LT33D	PC8-E, LE8	• Simple to learn, easy to use.

Medium	PC8-E/ LA36 or LT33D	None	• Well known programming language. • Does not require mass storage. • E, F, I, A, X, H, format specs.
Machine speed	LA36/ PC8-E or LT33D	PC8-E	• Largest possible symbol table on basic 4K machine. • Easy to use. • Includes all basic PDP-8 family symbol definitions.
Machine speed	Disk monitor system	PC8-E	• Literals. • Automatic link generations to off-page symbols.
Machine speed	LA36/ PC8-E or LT33D	PC8-E	• Macro generation. • Literals. • Double precision and floating point constants.
Approx. 65% slower than machine speed	PC8-E, LA36 or LT33D	DF32-D. RF08/ RS08, TC08/ TU56	• Page independent relocatable code. • Automatic linkage to off page symbols. • Local, external, and common assignment. • Conditional assembly.
I/O Bound	LA36/ PC8-E or LT33D	LE8	• Generate or edit ASCII files on paper tape.
—	LA36	—	• Allows examination and modification of program. • Break-point allows execution of program at machine speed up to specified instruction. Control then returns to terminal.
Medium	Not applicable	Not applicable	• Allows floating point calculations via software only.
—	—	—	• A group of small machine language programs including RIM punch Binary punch Octal memory dump Master tape duplicator

10.7 DIAGNOSTICS

In addition to the software systems and programs described in this chapter, diagnostic program kits are available for all of DIGITAL's computers, interfaces, and devices. These programs may be run at the time the sys-

tem is installed and periodically thereafter to ensure that the equipment is operating correctly. The diagnostics are also used for troubleshooting the equipment when problems develop. While the diagnostics are running, numbers can be entered into the switch register, causing the program to loop on one particular portion of the test, checking out one section of logic. This allows the troubleshooter to monitor signals on a part of the logic without waiting for the program to check the rest of the logic and return to the test for the logic being checked. Memory diagnostics are written in 1K segments so that they can be run on systems with 1K, 2K, or 4K memory configurations. The PDP-8/A Operator's Handbook, shipped with each system, has detailed instructions on loading and running diagnostic programs. The diagnostics available for the PDP-8/A are:

Diagnostic	Equipment Tested
For small (less than 4K computers)	
MAINDEC-08-D-DJKKA-PM1	Central Processor Unit
MAINDEC-08-DJMSA-PM	MS8-A, 1 or 2K RAM Memory
MAINDEC-08-DJDKA-PM1 through 4	DKC8-AA I/O Option Board (4 separate paper tapes)
For computers with 4K or more of memory	
MAINDEC-08-LBAA-PM	BINARY Loader (required to load tapes in BINARY format)
MAINDEC-08-DJKKA-BN	Central Processor Unit
MAINDEC-08-DJMMA-BN	4 to 32K RAM Memory
MAINDEC-08-DJKMA-BN	KM8-A Extended Option Board
MAINDEC-08-DJDKA-BN	DKC8-AA I/O Option Board
MAINDEC-08-DJKLA-BN	KL8-A Four Channel Asynchronous Interface
MAINDEC-08-DJFPA-BN	FPP8/A Maintenance Diagnostic
MAINDEC-08-DJFPB-BN	FPP8/A Instructor Test and Data Exerciser

Documentation is available for each diagnostic providing the information necessary to run the diagnostics and interpret the test results.

10.8 DECUS

Additional programs and applications packages may be obtained from DECUS, the Digital Equipment Computer Users' Society. DECUS is a non-profit users' group (the second largest such group, worldwide) that sponsors technical symposia, publishes a periodic newsletter, and maintains a library of more than 2000 programs for the PDP-8. Every customer who has purchased or ordered a computer manufactured by DIGITAL is eligible for an installation membership in DECUS. Two classes of individual membership are also available. Membership in DECUS is strictly voluntary, and does not require payment of dues. Programs from the DECUS library are available to all members on a request basis. In some instances, a nominal charge may be associated with a particular program. A complete catalog of available programs may be obtained from the Society.

CHAPTER 11

INSTALLATION PLANNING AND DELIVERY

11.1 INTRODUCTION

Digital Equipment Corporation has more than 18 years of experience installing and maintaining over 50,000 computers in a wide variety of operating environments all over the world. Highly qualified, DIGITAL's engineers are available to either perform or assist in the performance of every phase of computer delivery and unpacking, equipment installation, and final acceptance testing. Adequate planning and initial site preparation are particularly important because they can simplify the installation process and result in an efficient, more reliable data processing system. The suggestions contained in this chapter are intended to simplify and enumerate some of the factors that should be considered during planning and preparation for delivery of a computer system.

The *Computer Site Preparation Handbook*, published by Digital Equipment Corporation, provides an invaluable reference that covers almost every aspect of pre-delivery planning and system installation. This handbook contains suggestions that will help to optimize the performance of any data processing installation, and it is particularly pertinent to installations that include magnetic disk or magnetic tape I/O equipment. A companion document, the *PDP-8 Site Preparation Worksheet*, contains additional data and a convenient checklist for evaluating system requirements. Additional information can be obtained by referring to the PDP-8 Configuring Guide.

11.2 PRE-DELIVERY PLANNING AND SITE PREPARATION

The size of the system to be installed is the prime consideration in determining the degree of planning and site preparation required. A small system may have requirements similar to those of household appliances, needing only desk space and a connection to existing primary power. A medium-size system often requires the more controlled environment of a typical modern office. Larger systems, and especially systems containing magnetic disk and tape equipment, may require a well controlled environment that maintains acceptable levels of temperature, humidity, cleanliness, etc. Regardless of the size of the proposed system, primary planning considerations include provision for adequate space, safety and fire precautions, adequate electrical power, and any environmental conditioning that may be required.

Space and layout requirements will differ at various installations, depending upon the intended application. The floor area required for a particular system may be determined by considering the size of the specific components to be installed, length-to-width ratio of the room, location of columns or obstructions, and provision for future expansion. Adequate space must be provided to allow unrestricted access to all equipment doors and panels for maintenance. Space must also be allocated

for printer forms stands, storage cabinets, card and paper tape files, work tables, communications equipment, and related items. Personnel should have easy access to peripheral devices that require manual operation or adjustment, and control panels should not be located directly on main aisles or traffic centers. Best results are achieved by preparing scale layouts of proposed system configurations in the room under consideration.

11.2.1 Processor Space Requirements

The processor is supplied with a power supply and a 6 foot (1.83 meter) power cord. The non-dedicated Omnibus slots provide room within the chassis for controllers for many optional devices which may be included with the system or ordered at a later date. The Omnibus slots may also be used for user designed interfaces. At least two of the Omnibus slots are occupied by the processor module and memory. The other slots may be used for additional memory or options.

The 8A420, 8A620, and 8A820 dimensions are shown in Figure 11-1. These systems use the BA8-C expander box which requires more space for the larger Omnibus and power assembly. The BA8-C is supplied with a power supply and 6 foot (1.83 meter) power cord. Allocation of slots is the same as for the regular 8A enclosure.

11.3 CABINET OPTIONS AND SPACE REQUIREMENTS

Standard Digital Equipment Corporation cabinets allow the PDP-8/A to share floor space with an assortment of peripheral devices. This provides easy access to peripherals that require operator initialization or adjustment, such as high-speed paper tape units, along with minimal system space requirements. Use of standard cabinets can also simplify electrical wiring and eliminate most external cabling, contributing to a safer and more convenient data processing area.

The PDP-8/A may be installed in an H960-BC standard basic cabinet illustrated in Figure 11-2 or an H967-BA short basic cabinet illustrated in Figure 11-3. Either cabinet provides space for a selection of peripheral device options, which may be included with the basic system or ordered separately at a later date. Additional peripherals may be mounted in one or more H961-A standard option cabinets, which are similar to the H960-BC standard basic cabinet, or H967-AA short option cabinets, which are similar to the H967-BA short basic cabinet. Both types of option cabinet are designed to be positioned adjacent to the H960-BC or H967-BA basic cabinet that houses the PDP-8/A computer.

Figure 11-4 is a top view of a standard cabinet or short cabinet that shows the floor space required for either type of installation. It is very important to allow enough space around the cabinet so that unimpeded access to the equipment is maintained, even with the doors fully open. Cabinets housing the PDP-8/A and certain peripherals will not have front swinging doors; in these cases, the floor space indicated in Figure 11-4 is required so that the equipment may slide freely out of the cabinet for maintenance. Additional space should be provided in front of cabinets housing equipment that requires frequent adjustment by operating personnel.

11.3.1 I/O Cabling Requirements

Cabling is routed from the upper rear side, through the opening in the rear of the processor. Cables must be left loose with enough length to allow modules to be removed from the front of the chassis.

All Digital Equipment Corporation interconnecting cables are standard lengths and factory installed. If the cabinets must be shipped separately because of shipping or receiving restrictions, the cabinet interconnecting cables are reconnected at the installation site. Cable lengths should be as short as possible, and under no circumstances should any of the maximum lengths be exceeded. External interconnecting cables may be protected from damage by installing a protective cover over the cables in a manner that will not present a safety hazard to operating personnel.

11.4 TEMPERATURE AND HUMIDITY

Recommended operating conditions for a typical computer system provide an ambient temperature of 21° ± 1° C (70° ± 2° F) with a noncondensating relative humidity of 45% ± 5%. As indicated in Table 11-1, however, PDP-8/A systems are designed to permit operation, storage, and shipment under highly adverse conditions, when necessary.

PDP-8/A computer systems are air cooled, with cooling air circulated internally by fans in each cabinet. The air flow pattern varies slightly from one unit to the next; however, in general, air enters standard cabinets through the top filter and exists at the bottom. On short cabinets, air enters through a filter at the bottom of the unit and exits at the top rear. A minimum clearance of 30 inches (75 centimeters) above each cabinet is recommended to permit free circulation of cooling air. If this requirement cannot be met, some other means of allowing free air flow above and around the equipment should be devised.

11.5 FACTORS AFFECTING SYSTEM RELIABILITY

Although Digital Equipment Corporation computer systems are designed to be substantially more reliable in adverse environments than other systems of similar size, system environment has an unavoidable effect on system reliability. Reasonable control of the system environment will usually minimize maintenance requirements and provide more reliable system operation. Undesirable factors which may affect system reliability in some cases include the following.

11.5.1 Extreme of Temperature and Humidity

High temperature increases the rate of deterioration of virtually every material. In addition, thermal gradients induce temporary or permanent changes in most materials. High temperature and high humidity can combine to cause moisture absorption, resulting in dimensional and handling changes in paper and plastic media. Low humidity permits the build-up of static electricity, which can be annoying to personnel and may affect the system in extreme cases.

11.6 PDP-8/A ENVIRONMENTAL LIMITS

The following limits apply to a basic PDP-8/A (freestanding or cabinet mounted). All parameters are measured at the fan air intake of the chassis.

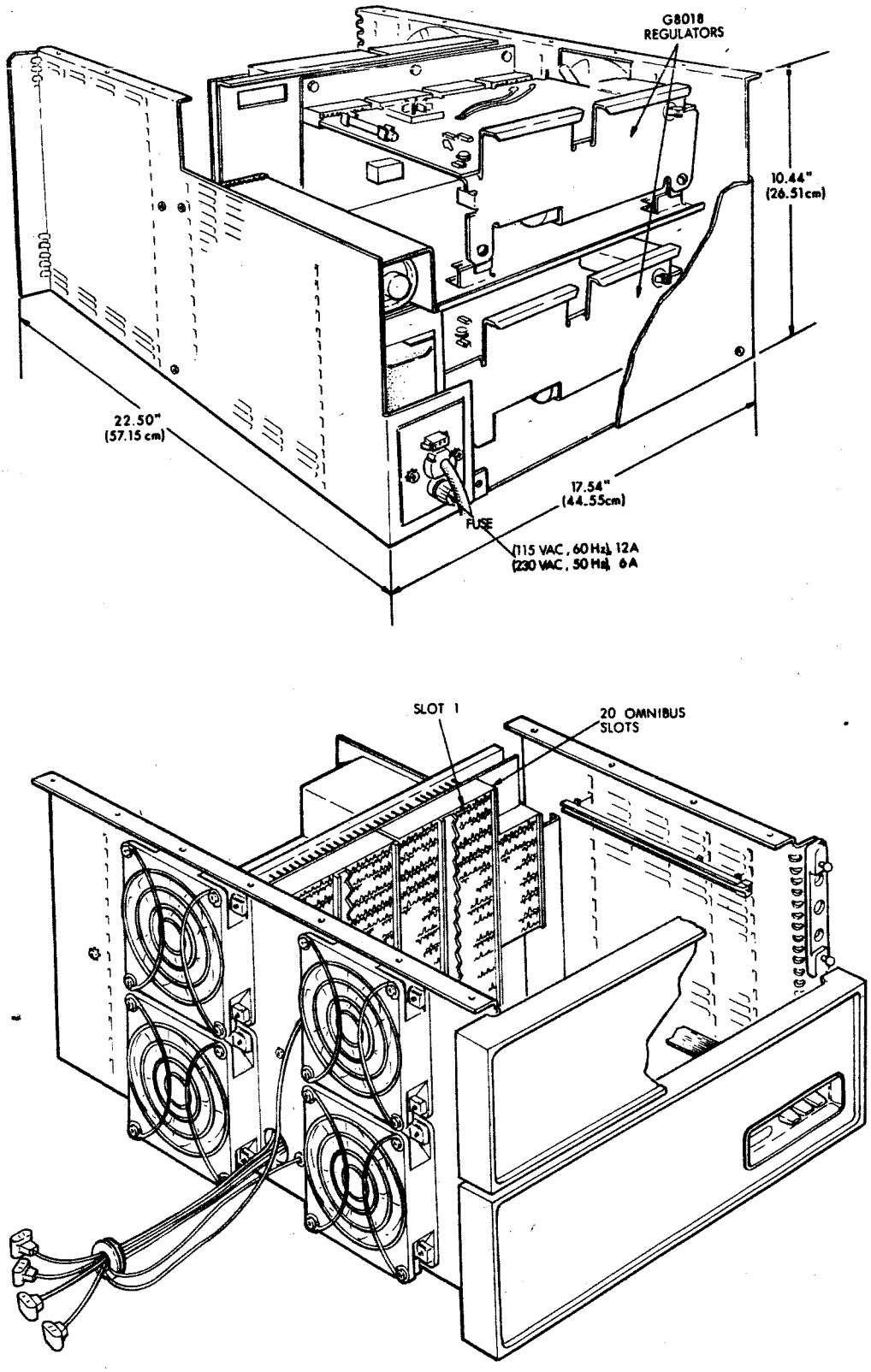


Figure 11-1 BA8-C Expander Box

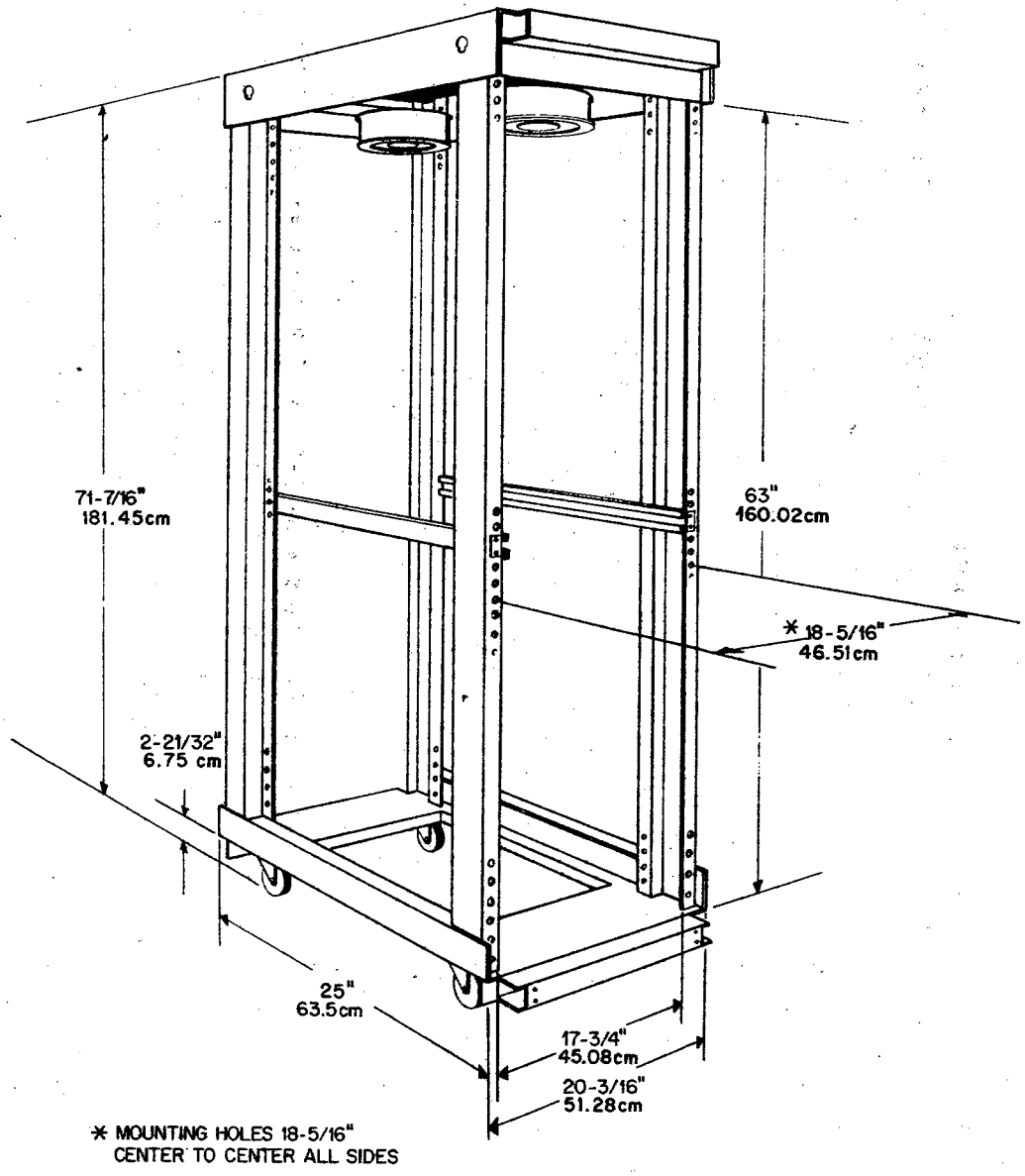


Figure 11-2 Standard Basic Cabinet

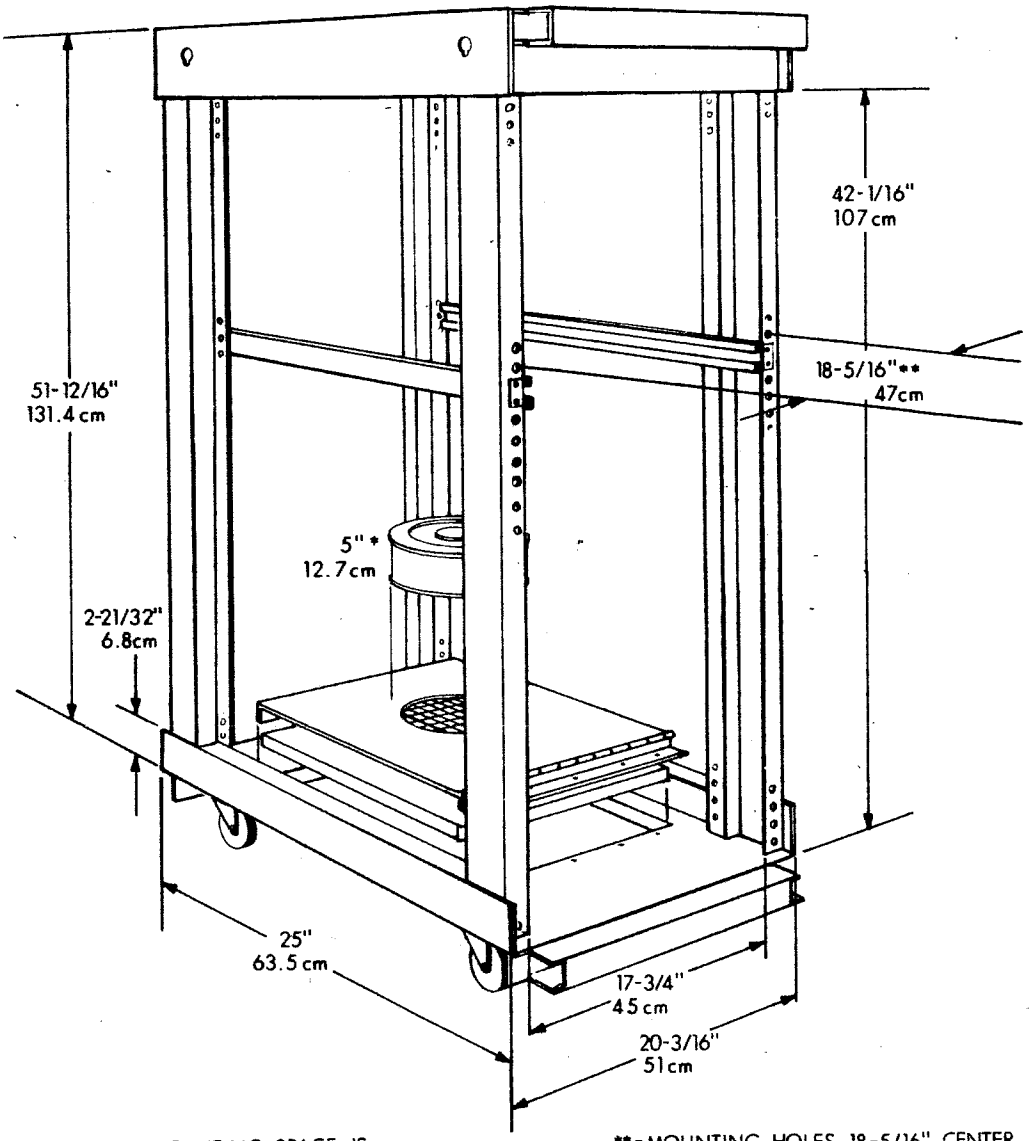


Figure 11-3 Short Basic Cabinet

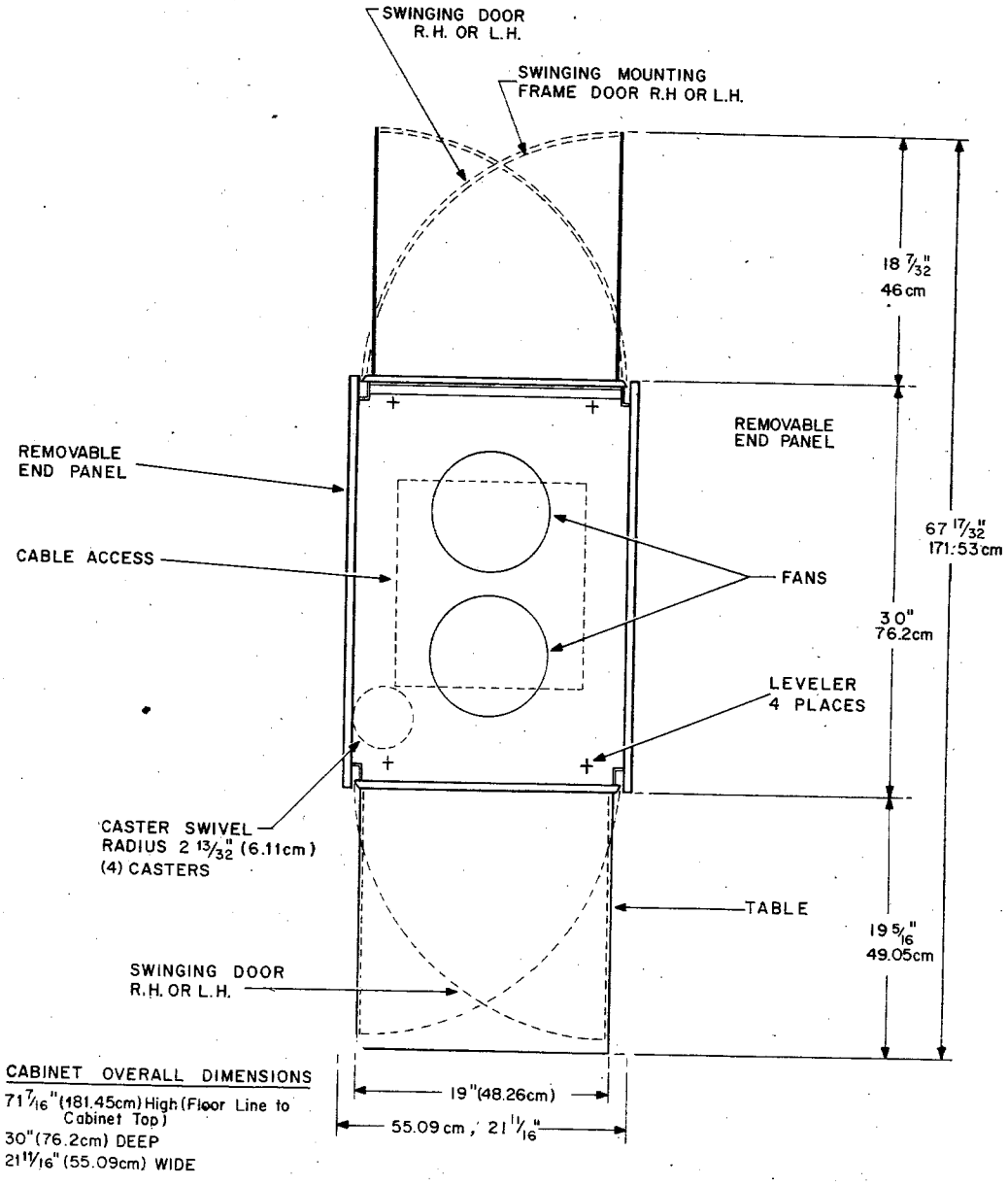
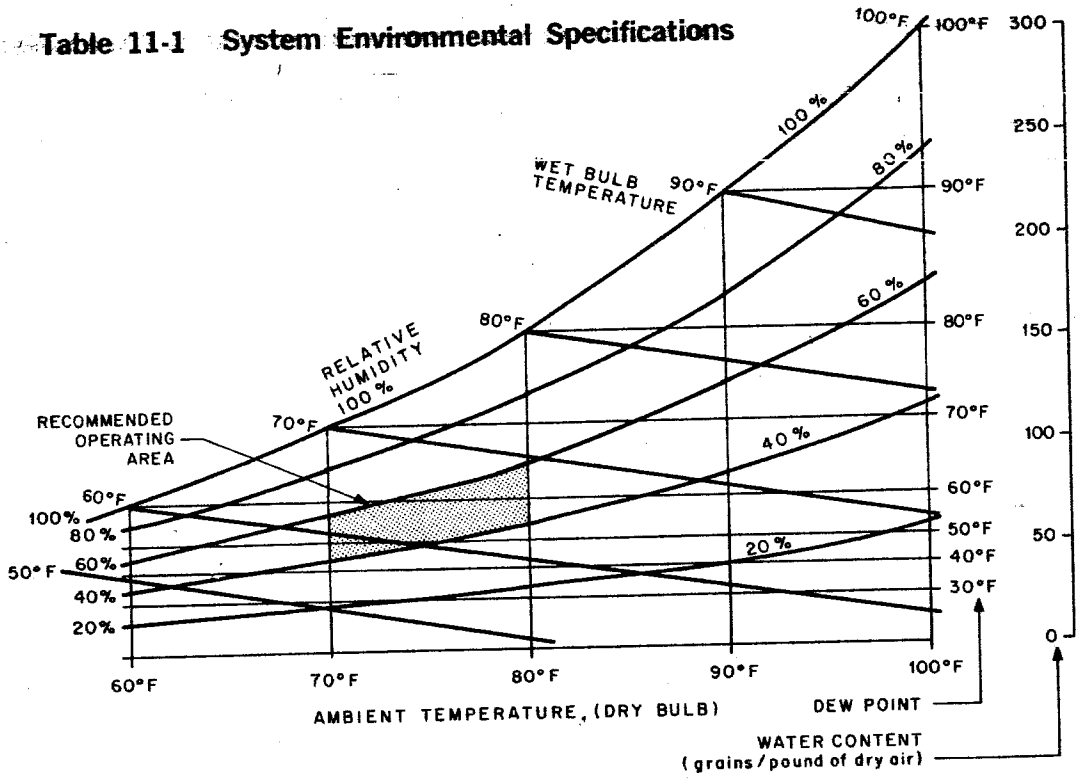
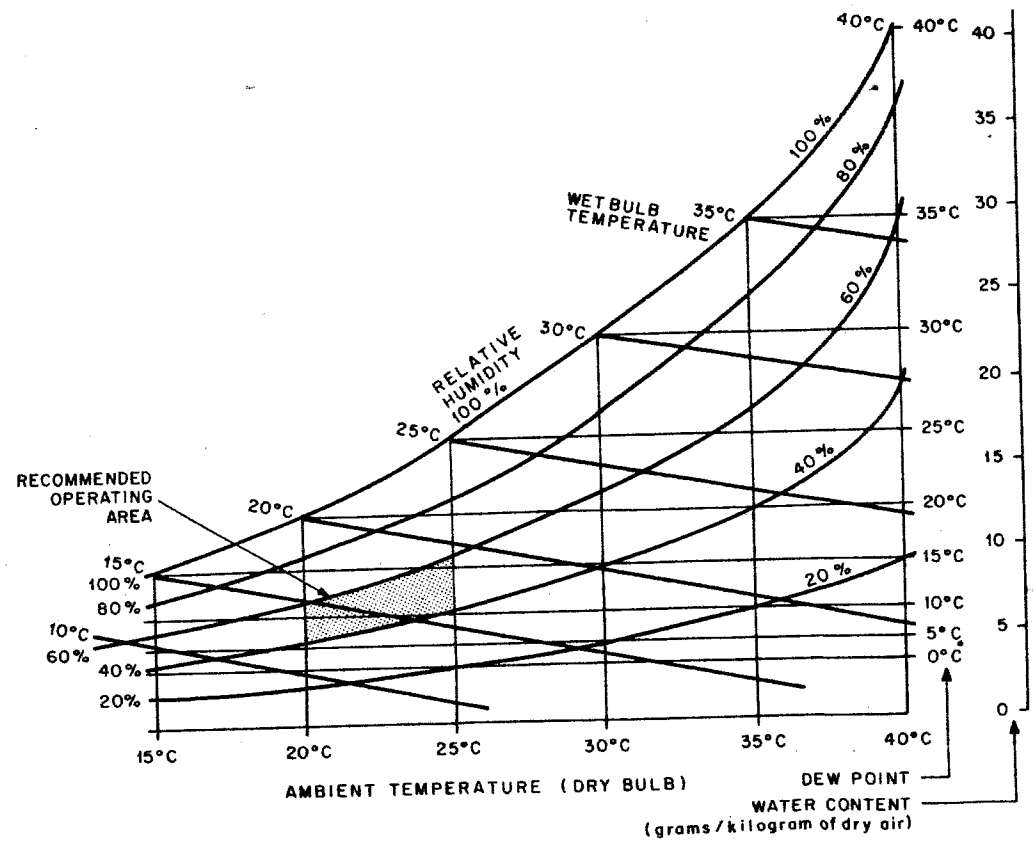


Figure 11-4 Cabinet Floor Space Requirements

Table 11-1 System Environmental Specifications





Operating Limits

Temperature:	5° C (41° F) to 50° C (122° F)
Humidity:	10—95% RH non-condensing, maximum wet bulb 32° C (90° F), minimum dew point 2° C (36° F).
Altitude:	2400 m (8000 ft)
Shock:	10 g (peak) of 10 ms ± 3 ms duration, half sine wave for each of three orthogonal directions.
Vibration:	Sine wave with the following components: 5—50 Hz 0.004 in. D.A. 50—500 Hz 0.5 g (peak) 500—50 Hz 0.5 g (peak) 50—5 Hz 0.004 in. D.A. Sweep rate 1 octave/minute for each of three orthogonal directions.

Non-Operating Limits (when packaged for shipping in a DIGITAL supplied container)

Temperature:	—40° C (—40° F) to +66° C (151° F) See Note below.
Humidity:	0—95% RH non-condensing.
Altitude:	9100 m (30,000 ft)
Shock:	40 g (peak) of 30 ms ± 10 ms duration, half sine wave (the shock pulses to be applied perpendicular to each of the six package surfaces).
Vibration:	Vertical axis — 1.4 g (r.m.s.), 10—300 Hz. Power spectral density 0.029 g^2/Hz from 10—50 Hz with 8 db/octave rolloff from 50—300 Hz. Horizontal axis — 0.68 g (r.m.s.), 10—200 Hz. Power spectral density 0.007 g^2/Hz from 10—50 Hz with 8 db/octave rolloff from 50—200 Hz.

NOTE

Batteries used in PDP-8/A (8A100) semiconductor memory machines have a self discharge rate which varies directly with the storage temperature. At room temperature the discharge rate is ~6–8% per month; at 66° C the rate rate is ~6—8% per month, at 66° C the rate becomes 50% per month. Batteries must not be allowed to become completely discharged; thus, periodic recharging is required as a function of storage temperature.

11.6.1 High Altitude

Airborne systems, or systems operated at altitudes above 7000 feet (2000 meters) occasionally require additional blowers for adequate cooling. Disk subsystems have a maximum altitude specification of 12,000 feet (3500 meters).

The *Computer Site Preparation Handbook* contains suggestions for isolating and eliminating all of the conditions listed above, as well as

other factors whch may affect the operation of a computer system in extreme cases. Digital Equipment Corporation should be notified if any of these factors may be present at the proposed installation site.

11.7 ELECTRICAL CONSIDERATIONS

Computers and related equipment require a reliable power source with minimum voltage and frequency fluctuations. The exact power requirements for a given installation will depend upon the intended application. In general, line voltage disturbances with a magnitude greater than ±10% of nominal voltage and a duration greater than 5 milliseconds are undesirable.

Local disturbances in the power supply may be caused by overloading transformers and feeders or switching large loads such as elevators, air conditioners, and lighting. Other local disturbances result from devices such as arc welding and Xray equipment injecting rf components into the power line. In some areas, power source disturbances can result from voltage fluctuations or power factor corrections at the public utility. The effects of these conditions may be minimized if they are identified prior to equipment installation by monitoring the electrical service for a period of time consistent with expected system operating time throughout a typical week. Test equipment used to monitor the service should have sufficient response to detect objectionable disturbances of short duration.

11.7.1 General Power Requirements

The total current required for a computer system may be determined from the data in Table 11-2 by adding the requirements for every cabinet and every free-standing peripheral device. Even though an installation may not use all of the options in a particular cabinet, it is advisable to provide adequate power for the entire cabinet. Once the total current drawn by the installation is known, the type and quantity of ac connectors may be determined. Connectors must conform to statutory requirements of the locality in which the equipment is installed. In the U.S., power lines must terminate in NEMA receptacles to be compatible with the NEMA plugs supplied with the equipment.

11.7.2 Power Failure

In case of a power failure, the system will shut down automatically with no loss of internal data or damage to system hardware (if core memory and the Power Fail/Auto Restart option are used). Source power supply failures are of two types: power outages and line voltage irregularities. Power outages may include short duration dips in voltages as well as prolonged failures. If the frequency of power outages is unacceptably high, they may be prevented by the installation of static inverters, motor generator sets, or a combination of both types of line buffering equipment.

Voltage irregularities may result from transient electrical noise or inductive spikes superimposed on the line voltage. This problem can be caused by a wide variety of industrial, medical, and communications equipment operated in the vicinity of the power distribution system. The effects of line disturbances that persist even when transient-producing devices are disconnected from the riser and power distribution panel

may be minimized by installing an isolation transformer or rf filter. Installing power service and distribution in accordance with Digital Equipment Corporation specifications, as outlined in the *Computer Site Preparation Handbook*, will reduce the extent to which such measures are necessary.

11.7.3 Ground Requirements

A system involving a digital/analog interface usually requires that the digital system ground be tied to the analog system ground at a single point, usually at the analog/digital interface. A low-resistance ground connection is required in these cases. In systems where no analog interface is involved, the grounding provided by a large electrical conduit is usually adequate.

The 3-wire plug supplied with the PDP-8/A provides the only ground connection required by this processor; however, rack-mounted systems and, especially systems that include a variety of peripherals, require additional grounding. The grounding schemes described in the *Computer Site Preparation Handbook* are recommended as effective means of keeping electrical noise and differential potentials under control in large systems. Whatever grounding system is used, it should provide less than 10 ohms impedance to moist earth from dc to 10 MHz. It should also be insulated from sources of electrical noise, to prevent noise from entering the system via ground.

11.8 AC POWER FACILITY INSTALLATION AND TESTING

The ac power connection requirements of the PDP-8/A computer are consistent with good electrical practice. The importance of correct electrical connections cannot be overstressed. Significant operational difficulties are likely in the event of either a poor neutral or a poor ground circuit. Voltage readings must be made at the power receptacle before the computer is plugged in. It is an extremely wise precaution to take a voltage reading from the frame of the computer to an established ground point before touching the cabinet.

Figure 11-5 illustrates the recommended wiring for the wall receptacle servicing a small computer system. It is advisable to provide a separate central load breaker panel for the computer system, with a circuit breaker for the computer and one for each cabinet or free-standing peripheral receptacle; however, this is not an operational requirement. Following installation of the power facilities, voltage readings should be taken at each receptacle in the system. A checkout procedure for testing the electrical system is provided by Digital Equipment Corporation on request. In any event, the tests described in the following section should be run as soon as all equipment has been uncrated and installed.

Table 11-2 Installation Data

Unit	Weight (lbs)	Dimensions (in.) Height	Width	Depth	Heat Dissipation Btu/hr.	AC Current (Amps) @ 115 V Nom.	Surge	Power Consumption (KW)	Mounting Panels	Remarks
PDP-8/A	55	10.5	19	10.5	510	4.0	6.0	0.3	2	
BA8-C	120	10.5	19	23	1000	10.5		0.88	—	
Teletype ASR-33	70	45	23	19	375	2.0	8.0	0.11	—	
Paper Tape Reader PR8-E	32	10.5	19	16	510	1.0	—	0.15	2	
Card Readers CR8-F or CM8-F	70	13	20	15	1200	3.2	—	0.40	—	Table space required
Magtape Drive Industry Compatible TU10	143	26.25	19	26	3750	11	—	1.10	Separate Cabinet	TU10C = 9 track TU10D = 7 track
DECtape Control TC08	30	10.5	19	—	1000	3.0	—	0.30	4	Controls up to 4 TU56 transports
Dual DECtape Transport TU56	80	10.375	19	15.25	1740	115 V = 2.85 A +10 V = 800 mA ± 10% −15 V = 550 mA ± 10%		0.51	2	Optional + 5V or +10 V supply may be used
DECassette Tape System TA8-E	32	5	19	19	300	1.0	—	0.12	1	
KL8-A	—	Hex Module			2100	5.04	—	0.62	1	
Oscilloscope Display: VR14	68	10.5	19	17	680	1.75	—	0.20	2	
TS03	35	10.5	19	17	341	1.0		0.1	—	
Disk File and Control RF08/RS08	depending on size of system	71.44	21.69	30	510/620 (Plus RS08 Motors)	1.3/2.6 (Plus 4.0 A per RS08 motor)	—	0.15/0.30 (Plus RS08 Motors)	Separate Cabinet	Dimensions are for subsystem mounted in 2 standard cabinets
RX8-E Floppy Disk	—	10.5	19	17	1680	5.5		0.50	—	—

Table 11-2 (Cont.) Installation Data

Disk Cartridge System RK8-E	110	10.5	19	27	800 (Logic) 2400 (Per Drive)	2.0.(motor & blowers)	10.0	0.20	—	
LA35 DECprinter	97	27.5	33.5	21.7	1000	1.3	2.6	0.30		—
Line Printer and Control LE8 (80 col., 64 ch.)	280	46	24	22.25	1125	3.0	—	0.33	—	Paper; standard fanfold Edge punched 4" to 9⅞" wide
LA180 DECprinter	102	33.2	27.5	20	1708	3.0		0.40 printing 0.20 non-printing	—	Paper guide: 5" paper catcher 11½"
Line Printer and Control LE8/JA (132 col., 64 ch.)	300	46	48	25	1700	5.0	—	0.50	—	Paper: 14" to 14⅞" wide
30" Incremental Plotter & Control XY8/EA	31	10	39.5	14.75	600	1.5	—	0.175	—	Paper guide: 5" Table space required for Plotter
12" Incremental Plotter & Control XY8-EB	18	9.75	18	14.75	600	1.5	—	0.175	—	Table space required for Plotter
LA36 DECwriter and Control	102	33.2	27.5	24.2	1000	3.0	—	0.3 (printing) 0.175 (non-printing)	—	
VT50 Video Terminal	43	14.1	20.9	27.2	—	6.95	—	0.3	—	Table space required
VT52	44	14.1	20.4	27.2	375	1.0	—	0.11	—	Table space required
VT55	57	14.1	20.4	27.2	580	1.5	—	0.17	—	Table space required
VT61	20	14.3	20.4	27.6	380	1.0	—	0.11	—	Table space required

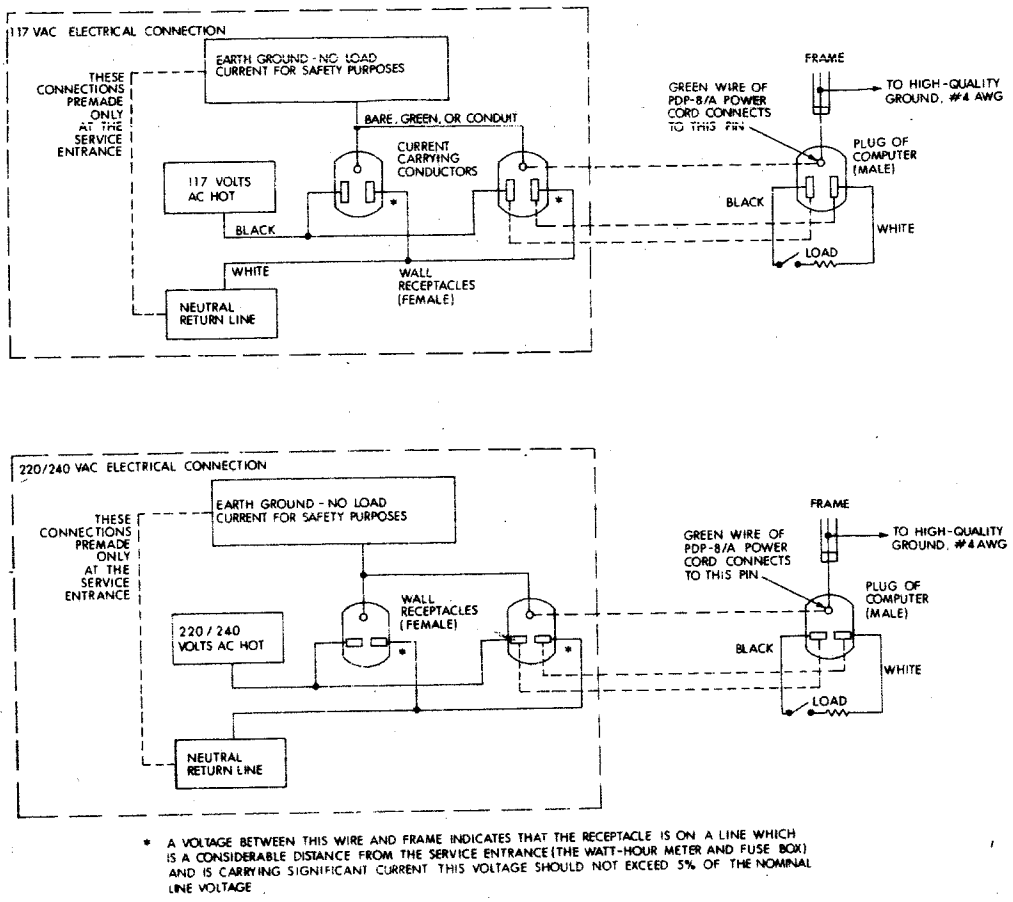


Figure 11-5 Recommended Receptacle Wiring

Digital Equipment Corporation engineers are available for assistance and consultation during installation and testing. Further technical assistance in the field is provided by home office engineers, branch office applications engineers, and field service engineers.

11.9 GROUNDING AND FACILITY POWER TESTS

CAUTION

This procedure involves measurement of dangerous voltages.

If these tests indicate that faulty wiring exists, a qualified, licensed electrician should be consulted.

These tests should be performed in sequence; do not proceed beyond an abnormal indication until the fault has been corrected.

These tests are to be made at the computer receptacle with no peripheral equipment connected to ac power.

The voltage readings below assume a nominal 117 Vac, phase neutral supply. They should be modified accordingly for other distribution systems.

TEST STEP	AC VOLTMETER FROM	TO	MAXIMUM VOLTAGE IF MISWIRED	EXPECTED METER READING	INDICATES
1.	Hot	Neutral	240 Vac	117 Vac	Ok
2.	Hot	Ground	240 Vac	117 Vac	Ok
3.	Neutral	Ground	240 Vac	0 Vac	Ok, Unloaded Circuit
	Neutral	Ground	240 Vac	Up to 5 Vac	Note*
4.	Ground	Conduit or Box	240 Vac	0 Vac	Ok
5.	Neutral	Conduit or Box	240 Vac	Up to 5 Vac	Note*

6. If 0 Vac was found in test 3, tests 4 and 5 should be made with the computer, or some other significant load, on the line. Test 4 should again be 0 Vac and test 5 should show some voltage up to 5 Vac. A reversal of these readings indicates a reversal of the ground and neutral lines.

7. Test steps 1 through 6 should next be made at each appliance receptacle which is to be used to supply power to a peripheral device. Test steps 9 through 11 must be made before any peripheral device is plugged in to ac power.

8. The previous tests have ensured a properly wired ac supply for the computer. The following tests should now be made with the computer in operation. They are to be made between each appliance receptacle and the plug prongs of the peripheral device which is about to be plugged in. An open circuit in the ac wiring of the device will negate the validity of these tests; power switches must be on and all cables to the computer must be plugged into their correct slots.

TEST STEP	FROM RECEPTACLE	TO PLUG	MAXIMUM VOLTAGE IF MISWIRED	EXPECTED METER READING	INDICATES
9.	Neutral	Neutral	Up to 5 Vac**	0 Vac	Ok
10.	Ground	Ground	Up to 5 Vac**	0 Vac	Ok

* A voltage between the white wire and frame indicates that the receptacle is on a line which is a considerable distance from the service entrance and is carrying a significant current. This voltage should not exceed 5% of the nominal line voltage.

** In addition to a reversal of neutral and ground in the peripheral device, a reading here may also indicate that the computer and the receptacle being tested are not on the same circuit.

*** There is an ac path through the line filter to ground. This assumes that a proper ground connection exists between the peripheral device and the PDP-8/A.

CHAPTER 12

CUSTOMER SERVICES

12.1 GENERAL

DIGITAL offers a wide variety of services to its customers. These services can be categorized as follows:

- Maintenance Services
- Software Services
- Educational Services
- Design Services
- Documentation

Each is briefly described in the following paragraphs.

12.2 MAINTENANCE SERVICES

12.2.1 The DIGITAL Service Agreement

For most products, DIGITAL service contracts are available on a single or multi-shift basis, depending on system requirements. DIGITAL service contracts not only handle emergency repairs but also fully cover both preventive maintenance and engineering changes at no extra cost. DIGITAL also provides complete equipment rebuilding as part of the standard agreement. With a DIGITAL service agreement, maintenance expenditures are preplanned—there can be no unwelcome surprises. And since the agreement includes all parts and labor, budgeting is easier and more accurate.

12.2.2 Field Service Outage System

Under a Field Service "outage" system, support personnel monitor all systems that are under service agreement and out of service. These systems are flagged by the local office and reported daily to the regional and district managers as well as to Maynard, Massachusetts headquarters. This information is the basis for directing the product support activities and getting help where it is needed.

12.2.3 Per Call Service

Per call coverage permits DIGITAL's customers to obtain maintenance service on a time and materials basis. Under this service alternative, DIGITAL dispatches a field service engineer to repair the computer system, charging for labor, parts, and travel expenses.

12.2.4 ECO Log

An ECO Log, for a nominal charge, is offered to whomever uses DIGITAL field service on a per call basis. This document is a monthly publication that outlines the engineering change orders (ECOs) for all of DIGITAL's equipment. Each issue includes all relevant ECO information, such as the purpose of the change and the estimated time required for installation and testing. The user must then identify the changes pertinent to

his equipment and, if he wishes to make the change, purchase a kit from DIGITAL. The user is also responsible for installing the change but may elect to have DIGITAL's Field Service do it.

12.2.5 Depot Service

For PDP-8s, PDP-11s and Teletypes®, DIGITAL provides depot repair stations that are located strategically throughout the world. Users can ship or "drop off" equipment for depot repair, permitting quality service at significantly reduced rates. Charges, exclusive of shipping and insurance costs, are computed on a time and materials basis.

Depot Repair facilities are currently open in Maynard, Massachusetts; Princeton, New Jersey; Chicago, Illinois; Houston, Texas; San Francisco and Los Angeles, California; Kanata, Canada; The Hague, Netherlands; Munich, West Germany; Reading, Berkshire, England; Paris, France; Tokyo, Japan; and Sydney, Australia.

12.2.6 Module Mailer

DIGITAL's Module Mailer Program is geared specifically to the needs of OEM customers who provide on-site remedial service to their customers through module swapping.

12.2.7 Module Subscription

For those OEMs who have the expertise and manpower to perform their own remedial maintenance, the Module Subscription Agreement furnishes the same quick turnaround that our Field Service offices obtain on many of DIGITAL's modules. In short, the program enables you to tap the same corporate resources that supply our own Field Service offices. This rapid turnaround means a reduction in both your inventories and associated costs.

12.2.8 Spare Parts Network

DIGITAL Field Service maintains an extensive logistics network as well as an administrative group to ensure the availability of spare parts. The first level of spares is usually maintained at the computer site but inventory is also maintained in a hierarchy of storage locations from the branch and district levels to the regional and main factory locations.

For depot or per call service users, DIGITAL provides "spares planning" and inventory procurement assistance which consists of recommended spares listings for specific configurations. Spare parts are available on either a routine or an emergency basis. Under emergency service DIGITAL will supply the required spare part within 48 hours (for a nominal handling charge).

12.3 SOFTWARE SERVICES—ANOTHER RESOURCE

Through DIGITAL's Software Consulting Service, users have been able to reduce development costs and still obtain quality customized software. Areas of expertise include process control, data communications, data analysis, information retrieval, numerical control, direct digital control, typesetting, simulation, commercial data processing, and special purpose timesharing.

12.3.1 Scheduled Consulting

Many users have found that periodic visits by software consultants are

beneficial. Through DIGITAL's scheduled Consulting Service, consulting periods can be established at a frequency that best meets the needs of the user.

®Teletype is a registered trademark of Teletype Corporation.

12.3.2 On-Call Service

An on-call service is provided for users who want software consulting services on an unscheduled basis. A guaranteed response time is provided for on-site service requests. This is especially useful to users who have critical applications.

12.4 EDUCATIONAL SERVICES

To meet the educational needs of its customers, DIGITAL has established Education Centers completely equipped and staffed with full-time instructors. These centers are located at DIGITAL's headquarters in Maynard, Massachusetts, and at Sunnyvale, California; Blue Bell, Pennsylvania; Chicago, Illinois; Lanham, Maryland; Reading, England; Munich, Germany; Hague, Netherlands; Stockholm, Sweden; Paris, France; Milan, Italy; Sydney, Australia; and Tokyo, Japan.

Course curriculums include introductory material that provides the necessary educational foundation for individuals without computer background. Software familiarization courses are designed to give those without computer experience the required preliminary training to write programs in machine language or higher level language. Hardware familiarization courses are designed to give the student an understanding of hardware operation and interfacing techniques. Advanced software courses teach the student to make efficient use of the language being studied, the features, programming techniques, and applications. Maintenance courses are designed to provide the student with skills and techniques necessary to perform preventive and corrective maintenance on DIGITAL's computers, peripherals, and terminals.

12.4.1 Seminars

DIGITAL offers specialized customer seminars conducted in a number of locations throughout the world and arranged through DIGITAL's local offices. These are designed to compulement and expand the current curriculum, and involve highly technical detail on new and existing software and/or hardware systems. Seminars are given by local specialists, educators, and guest speakers, as well as instructors and specialists from the home office and field installations. These local seminars assist the customer by making detailed knowledge and operational information more easily obtainable.

Examples of seminars that have been given are:

- DECsystem-10 Operator Training
- DECsystem-10 Monitor Conversion
- Real-Time Programming Systems for FORTRAN IV
- Writing FNEW Functions for FOCAL
- Device Handlers—RSX-15, DOS-15, DOS-11 and OS/8
- DOS-11 Graduate School

For more information on the courses offered and enrollment procedures, obtain DIGITAL's *Educational Courses Catalog* from your nearest DIGITAL Education Center.

12.4.2 On-Site Standard Courses

When a large group requires training, it may be more economical to have the course conducted at the customer's facility. Price per student for these courses is based on on-site rates plus instructor expenses. Prices include all standard course materials.

12.4.3 Special Courses

DIGITAL will design special courses of unique lesson material tailored to a customer's needs and time schedule. If the course is conducted at one of DIGITAL's Education Centers, the price per student is determined by the duration of the course, the material to be covered, the instructor preparation time required, and the number of students in attendance. The price for conducting a special course at a customer's facility is the same as the Education Center pricing, plus any additional instructor expense.

Audio Visual Courses

Audio visual courses are available to aid in training users of DIGITAL computers and peripherals.

Education Consultants

DIGITAL can also help a user set up his own training program, providing services that range from advice on course objectives to fully developed courses.

12.5 DESIGN SERVICES

12.5.1 Computer Special Systems

In addition to a wide range of standard products, DIGITAL offers the user an expert product design capability. The sole function of the Computer Special Systems (CSS) Group is to provide custom-tailored products to meet the user's specific requirements. Whether the requirement is for a custom peripheral, an interface to a unique device, a multi-processor system, a custom software routine, or a complete turn-key package, this group will provide the solution.

CSS is prepared to serve the needs of the single custom purchase as well as to meet the requirements of volume purchases. The following items are of particular value to the user:

- CSS can provide custom products on a production schedule to meet the user's particular needs. If necessary, special production facilities will be established to ensure that requirements are met on time.
- CSS can deliver a complete package consisting of the user's standard and custom items completely integrated and tested as a system.
- CSS can provide competitive prices commensurate with the user's volume.

All CSS custom products share the following features:

COMPONENTS—All devices are constructed from standard catalog items

and parts. This means a small spare parts inventory and easy maintenance.

WARRANTY—All custom products are fully warranted for at least ninety days.

DOCUMENTATION—Complete documentation packages are supplied containing schematic diagrams, technical manuals, diagnostic descriptions, and parts listings.

DIAGNOSTICS—Special diagnostics are prepared for each custom interface. CSS also provides complete system exerciser routines for the more complex configurations.

MAINTENANCE—All CSS products are eligible for maintenance services provided by DIGITAL's extensive Field Service Organization.

CSS has teams functioning efficiently in eight locations: Maynard, Massachusetts; Chicago, Illinois; Santa Ana, California; Kanata, Ontario; Reading, England; Munich, Germany; Paris, France; and Sydney, Australia.

12.5.2 Custom Designed Logic Modules

As the world's largest manufacturer of logic modules, DIGITAL offers a broad line of logic devices designed for system interfacing. If interfacing requirements cannot be met by standard modules, DIGITAL's Custom Modules Group can design and fabricate custom modules. DIGITAL's engineers can provide full design and development services or they can work with user-supplied drawings and parts lists, depending upon the user's requirements.

Custom-designed modules offer the same production advantages as standard modules:

- Computer-controlled component testing.
- Computerized PC board drilling.
- Precision gauged contact plating.
- Pantograph-controlled module assembly.
- High-quality, low-cost.

After assembly, modules are tested according to the user's specifications. These tests can range from a simple I/O check to a full diagnostic test procedure using automatic test equipment. With automated test stations, trouble-shooting and fault detection can be performed in an average of three minutes. Without this equipment, the test procedure could take hours.

DIGITAL offers all users a special wire-wrap service called "smooth flow" which uses the latest automatic wire-wrapping equipment. The user supplies the wire connection list, and DIGITAL prepares a punched card deck or paper tape for the wiring programs. Wiring is performed under the control of a PDP-8 computer. After panels are prepared, they are fully tested by another PDP-8 system—the same hardware and equipment used to check the quality of the wire-wrap assemblies for DIGITAL's computers.

APPENDIX A

FUNCTIONAL CHARACTERISTICS AND INSTRUCTION SUMMARY

PDP-8/A FUNCTIONAL CHARACTERISTICS

Type: Single address, fixed word length, parallel transfer programmed data processor.

Word Length: 12 bits.

Cycle Time: 1.5 μsec minimum (See memory speeds).

Memory Type	Cycle Time (μsec) Fetch Major State	All Other States
ROM Only	1.5	1.5
ROM/RAM (ROM Cycle)	1.6	1.6
ROM/RAM (RAM Cycle)	2.7	3.1
RAM Only	2.4	2.8
Core Memory	1.5	1.5

Memory Types:

RAM	1K, 2K, 4K
ROM	1K, 2K, 4K
PROM	1K
Core	8K or 16K words

Memory Expansion: Up to 32K.

Hardware Registers: 2 (AC and MQ).

Auto Index: 8 auto index registers per 4K memory field.

Addressing Capability: Typically one instruction may address 256 locations directly or 4096 locations indirectly.

Instruction Set: 6 memory reference instructions, 20 microprogrammable operate microinstructions, and 8 input/output transfer instructions for the CPU and each of up to 60 I/O devices.

Instruction Execution Time:

Operate microinstruction:	1.5 μsec*
Directly addressed MRI:	3.0 μsec*
Indirectly addressed MRI:	4.5 μsec*

Input/Output Capability: Programmed data transfer, program interrupt system transfer, and 12 channels of internal and/or external direct memory access (data break).

Auto Start Feature: The CPU contains an Auto Start which can start the CPU at one of six switch selectable addresses upon application of power.

Options: Two new option boards (DKC8-AA and KM8-AA) which may be used separately or together.

	DKC8-AA Front Panel Control Serial Line Unit Parallel I/O Real Time Clock	
	KM8-AA Power Fail/Auto Restart Memory Extension Timeshare Control Bootstrap Loader	
Size:	19 × 10.5 × 10.5 in. (48 × 27 × 27 cm)	
Weight:	55 lb (25 Kg)	
Operating Environment:	Ambient temperature	41° to 122° F 5° to 50° C
	Relative humidity	10% to 95% maximum, wet bulb 32° C (90° F)
Power Requirement:	Approximately 150 W at 115 Vac, 50 or 60 Hz or 230 Vac, 50 or 60 Hz. (Voltage and frequency specified at time of order.)	

* Cycle times reflect 1.5 μsec memory.

CPU INSTRUCTION SUMMARY

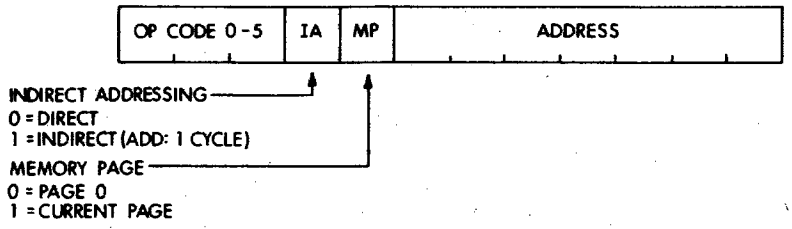
BASIC INSTRUCTIONS

			Cycles
AND	0000	logical AND	2
TAD	1000	2's complement add	2
ISZ	2000	increment, and skip if zero	2
DCA	3000	deposit and clear AC	2
JMS	4000	jump to subroutine	2
JMP	5000	jump	1
IOT	6000	in/out transfer	—
OPR	7000	operate	1

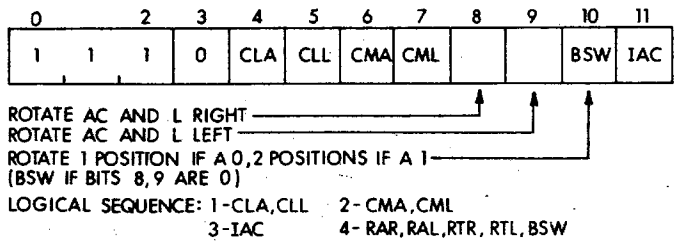
GROUP 1 OPERATE MICROINSTRUCTIONS (1 CYCLE)

			Sequence
NOP	7000	no operation	—
CLA	7200	clear AC	1
CLL	7100	clear link	1
CMA	7040	complement AC	2
CML	7020	complement link	2
RAR	7010	rotate AC and link right one	4
RAL	7004	rotate AC and link left one	4
RTR	7012	rotate AC and link right two	4
RTL	7006	rotate AC and link left two	4

IAC	7001	increment AC	3
BSW	7002	swap bytes in AC	4



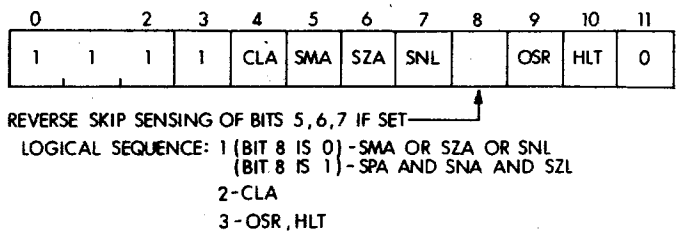
Memory Reference Instruction Bit Assignments



Group 1 Operate Instruction Bit Assignments

GROUP 2 OPERATE MICROINSTRUCTIONS (1 CYCLE)

			Sequence
SMA	7500	skip on minus AC	1
SZA	7440	skip on zero AC	1
SPA	7510	skip on plus AC	1
SNA	7450	skip on non-zero AC	1
SNL	7420	skip on non-zero link	1
SZL	7430	skip on zero link	1
SKP	7410	skip unconditionally	1
OSR	7404	inclusve OR switch register with AC	3
HLT	7402	halts the program	3
CLA	7600	clear AC	2



Group 2 Operate Instruction Bit Assignments

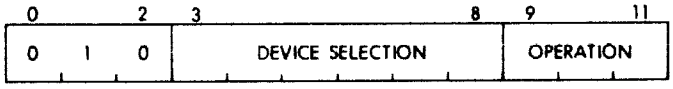
COMBINED OPERATE MICROINSTRUCTIONS (1 CYCLE)

CIA	7041	complement and increment AC
LAS	7604	load AC with switch register
STL	7120	set link (to 1)

GLK		7204	get link (put link in AC bit 11)
CLA	CLL	7300	clear AC and link
CLL	RAR	7110	shift positive number one right
CLL	RAL	7104	shift positive number one left
CLL	RTL	7106	clear link, rotate 2 left
CLL	RTR	7112	clear link, rotate 2 right
SZA	CLA	7640	skip if AC = 0, then clear AC
SZA	SNL	7460	skip if AC = 0 or link is 1, or both
SNA	CLA	7650	skip if AC ≠ 0, then clear AC
SMA	CLA	7700	skip if AC < 0, then clear AC
SMA	SZA	7540	skip if AC ≤ 0
SMA	SNL	7520	skip if AC < 0 or link is 1, or both
SPA	SNA	7550	skip if AC > 0
SPA	SZL	7530	skip if AC ≥ 0 and the link is 0
SPA	CLA	7710	skip if AC ≥ 0, then clear AC
SNA	SZL	7470	skip if AC ≠ 0 and link = 0

INTERNAL IOT MICROINSTRUCTIONS
PROGRAM INTERRUPT AND FLAG (1 CYCLE)

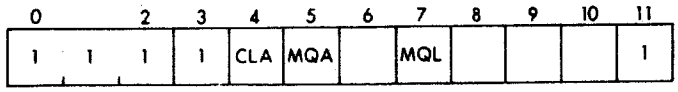
SKON	6000	skip if interrupt ON, and turn OFF
ION	6001	turn interrupt ON
IOF	6002	turn interrupt OFF
SRQ	6003	skip on interrupt request
GTF	6004	get interrupt flags
RTF	6005	restore interrupt flags
CAF	6007	clear all flags



IOT Instruction Bit Assignments

MQ MICROINSTRUCTIONS (1 CYCLE)

NOP	7401	no operation
CLA	7601	clear AC
MQL	7421	load MQ from AC then clear AC
MQA	7501	inclusive OR the MQ with the AC
CAM	7621	clear AC and MQ
SWP	7521	swap AC and MQ
ACL	7701	load MQ into AC
CLA SWP	7721	load AC from MQ then clear MQ



LOGICAL SEQUENCE:

1- CLA
2- MQA, MQL
3- ALL OTHERS

MQ Microinstruction Bit Assignments

DKC8-AA I/O OPTION BOARD INSTRUCTIONS

Serial Line Unit IOT Instructions (1 Cycle)

MNEMONIC	OCTAL CODE	OPERATION
KCF	6030	Clear Receive flag, do not set Reader Run.
KSF	6031	Skip if Receive flag is set.
KCC	6032	Clear Receive flag and AC, set Reader Run.
KRS	6034	Read Receive Buffer.
KIE	6035	Load AC11 into Interrupt Enable. AC11 = 1. Set interrupt Enable. AC11 = 0. Clear Interrupt Enable.
KRB	6036	Combined KCC & KRS.
		Transmit
TFL	6040	Set Transmit Flag.
TSF	6041	Skip if Transmit flag is set.
TCF	6042	Clear Transmit flag.
TPC	6044	Load AC4-AC11 into transmit buffer and transmit.
SPI	6045	Skip if transmit or receive flag is set and if interrupt enable is set.
TLS	6046	Combined TCF and TPC commands.

General Purpose Parallel I/O Instruction (1 Cycle)

MNEMONIC	OCTAL CODE	OPERATION
DBST	6570	Skip on Data Accepted, clear Data Accepted and Data Available, if Data Accepted flag is set. (See DCK8-AA description—Chapter 9.)
DBSK	6571	Skip on Data Ready flag.
DBRD	6572	Read Data into AC0-AC11.
DBCF	6573	Clear Data Ready flag, issue Data Accepted Out pulse.
DBTD	6574	Load AC0–AC11 into buffer and transmit Data Out.
DBSE	6575	Set Interrupt Enable to a 1.
DBCE	6576	Reset Interrupt Enable to a 0.
DBSS	6577	Issue a Strobe pulse.

Real Time Crystal Clock Instructions (1 Cycle)

MNEMONIC	OCTAL CODE	OPERATION
CLLE	6135	Load Interrupt Enable from AC11 AC11 = 1, set Interrupt Enable AC11 = 0, clear Interrupt Enable
CLCL	6136	Clear Clock flag.
CLSK	6137	Skip if Clock flag = 1.

KM8-A EXTENDED OPTION BOARD INSTRUCTIONS

Memory Extension/Time Share Control Instructions (1 Cycle)

MNEMONIC	OCTAL CODE	OPERATION
GTF	6004	Jam Transfer the status of the flags and link into AC0, AC2, and AC4–AC11. (O = cleared, 1 = set) AC0 = Link AC2 = Interrupt Request AC4 = Interrupt Enable AC5-11 = User Mode and Save Field
RTF	6005	Transfer the contents of AC5, AC6-AC11 to the user buffer flip-flop, the instruction buffer and data field, and inhibit processor interrupts until the next JMP or JMS instruction. User Field flip-flop and the Instruction Field are loaded at the conclusion of the next JMP or JMS instruction. The CPU loads the contents of AC0 into the Link and enables the interrupt system in response to this IOT.
CDF	62N1	Load the Data Field register with the program selected number N (N = 0–7).
CIF	62N2	Load the Instruction Buffer with the program selected number N (N = 0–7) and inhibit program interrupts until the next JMP or JMS instruction.
CDF CIF	62N3	Load the Data Field and Instruction Buffer with program selected number N (N = 0–7). Combines CDF and CIF.
RDF	6214	OR's the content of the Data Field register with AC6–AC8.
RIF	6244	OR's the contents of the Instruction Field register with AC6–AC8.
RIB	6234	OR's the contents of the Save Field with AC6–AC8 and AC9–AC11. The time share bit of the Save Field is ORed into AC5.
RMF	6224	Restores the contents of the Save Field register into the Instruction Buffer, Data Field, and (if time share is enabled) user buffer.
CINT	6204	Clear User Interrupt flip-flop.

Memory Extension/Time Share Control Instructions (1 Cycle) (Cont)

MNEMONIC	OCTAL CODE	OPERATION
SINT	6254	Skip if User Interrupt flip-flop is set.
CUF	6264	Clear User Buffer flip-flop (exit time share mode).
SUF	6274	Set User Buffer flip-flop (enter time share mode) following next JMP or JMS instruction.

Power Fail/Auto Restart

MNEMONIC	OCTAL CODE	OPERATION
SPL	6102	Skip if AC Low flip-flop is set.
CAL	6103	Clear AC Low flip-flop.
SBE	6101	Skip if Battery Empty flip-flop is set.

PERIPHERAL AND OPTION INSTRUCTION SUMMARY

AD8-A Analog to Digital Converter

MNEMONIC	OCTAL CODE	OPERATION
ADCL	6XY0	Clear Status, Enable, and MUX registers.
ADLM	6XY1	Load MUX register from the AC, then clear the AC.
ADST	6XY2	Clear the A/D DONE and Error flags (Status Register) and start a conversion on the current channel.
ADRB	6XY3	Transfer the contents of the A/D Buffer into the AC and clear the A/D DONE flag.
ADSK	6XY4	Skip the next instruction if the A/D DONE flag is set.
ADSE	6XY5	Skip the next instruction if the Timing Error flag is set.
ADLE	6XY6	Load the ENABLE Register from the AC, then clear the AC.
ADRS	6XY7	Transfer the STATUS, ENABLE, and MUX Registers into the AC.

53 is standard value for XY.

LE-8 Line Printer

MNEMONIC	OCTAL CODE	OPERATION
PSKF	6661	Skip on Character Flag
PCLF	6662	Clear the Character Flag
PSKE	6663	Skip on Error
PSTB	6664	Load Printer Buffer, Print on Full Buffer or Control Character
PSIE	6665	Set Program Interrupt Flag
PCLF, PSTB	6666	Clear Line Printer Flag. Load Character, and Print
PCIE	6667	Clear Program Interrupt Flag

CR8-E Card Reader and Control or CM8-E

Optical Mark Card Reader and Control

MNEMONIC	OCTAL CODE	OPERATION
RCSF	6631	Skip on Data Ready
RCRA	6632	Read Alphanumeric
RCRB	6634	Read Binary
RCNO	6635	Read Conditions Out to Card Reader
RCRC	6636	Read Compressed
RCNI	6637	Read Condition In From Card Reader
RCSD	6671	Skip on Card Done Flag

RCSE	6672	Select Card Reader and Skip if Ready
RCRD	6674	Clear Card Done Flag
RCSI	6675	Skip If Interrupt Being Generated
RCTF	6677	Clear Transition Flags

XY8-E Incremental Plotter Control

MNEMONIC	OCTAL CODE	OPERATION
PLCE	6500	Clear Interrupt Enable
PLSF	6501	Skip on Plotter Flag
PLCF	6502	Clear Plotter Flag
PLPU	6503	Pen Up
PLLR	6504	Load Direction Register, Set Flag
PLPD	6505	Pen Down
PLCF, PLLR	6506	Clear Flag, Load Direction Register, Set Flag
PLSE	6507	Set Interrupt Enable

VC8-E CRT Display Control

MNEMONIC	OCTAL CODE	OPERATION
DILC	6050	Clears Enables, Flags, and Delays
DICD	6051	Clears Done Flag
DISD	6052	Skip on Done Flag
DILX	6053	Load X Register
DILY	6054	Load Y Register
DIXY	6055	Clear Done Flag; Intensify; Set Done Flag
DILE	6056	Transfer AC to Enable Register
DIRE	6057	Transfers Display Enable/Status Register to AC

DR8-EA 12-Bit Buffered Digital I/O

MNEMONIC	OCTAL CODE	OPERATION
DBDI	65x0	Disable Interrupt
DBEI	65x1	Enable Interrupt
DBSK	65x2	Skip on Done Flag
DBCI	65x3	Clear Selective Input Register
DBRI	[illegible]	Transfer Input to AC
DBCO	65x5	Clear Selective Output Register
DBSO	65x6	Set Selective Output Register
DBRO	65x7	Transfer Output to AC

DP8-EA/EB Synchronous Modem Interface

MNEMONIC	OCTAL CODE	OPERATION
SGTT	6405	Set TRANSMIT GO Flip Flop
SGRR	6404	Set RECEIVE GO Flip Flop
SSCD	6400	Skip if Character Detected
SCSD	6406	Clear Sync Detect
SSRO	6402	Skip if Receive Word Count Overflow
SCSI	6401	Clear Synchronous Interface
SRTA	6407	Read Transfer Address Register
SLCC	6412	Load Control
SSRG	6410	Skip if Ring Flag

SSCA	6411	Skip if Carrier/AGC Flag
SRS2	6414	Read Status 2
SRS1	6415	Read Status 1
SLFL	6413	Load Field
SSBE	6416	Skip on Bus Error
SRCD	6417	Read Character Detected (if AC0 = 0) Maintenance Instruction (if AC0 = 1)
SSTO	6403	Skip if Transmit Word Count Overflows

DK8-EP Programmable Real Time Clock

MNEMONIC	OCTAL CODE	OPERATION
CLZE	6130	Clear Clock Enable Register per AC
CLSK	6131	Skip on Clock Interrupt
CLOE	6132	Set Clock Enable Register per AC
CLAB	6133	AC to Clock Buffer
CLEN	6134	Load Clock Enable Register
CLSA	6135	Clock Status to AC
CLBA	6136	Clock Buffer to AC
CLCA	6137	Clock Counter to AC

DK8-EC Crystal Clock

MNEMONIC	OCTAL CODE	OPERATION
CLEI	6131	Enable Interrupt
CLDI	6132	Disable Interrupt
CLSK	6133	Skip on Clock Flag and Clear Flag

KG8-EA Redundancy Check Option

MNEMONIC	OCTAL CODE	OPERATION
RCTV	6110	Test VRC and Skip
RCRL	6112	Read BCC Low
RCRH	6111	Read BCC High
RCCV	6113	Compute VRC
RCGB	6114	Generate BCC
RCLC	6115	Load Control
RCCB	6116	Clear BCC Accumulation

KE8-E Extended Arithmetic Element

MNEMONIC	OCTAL CODE	OPERATION

Mode Changing Instructions

SWAB	7431	Switch from Mode A to B
SWBA	7447	Switch from Mode B to A
SKB	7471	Skip if Mode B

Standard Instructions

CAM	7621	0→ AC, 0→ MQ
MQA	7501	MQ "OR"ed with AC→ AC
ACL	7701	MQ→ AC (MQA CLA)
MQL	7421	AC→ MQ, 0→ AC
SWP	7521	AC→ MQ, MQ→ AC

Mode A Instructions

SCA	7441	Step Counter "OR" with AC
SCA CLA	7641	Step Counter to AC
SCL	7403	Step Counter Load from Memory
MUY	7405	Multiply
DVI	7407	Divide
NMI	7411	Normalize
SHL	7413	Shift Left
ASR	7415	Arithmetic Shift Right
LSR	7417	Logical Shift Right

Mode B Instructions

ACS	7403	AC to Step Count
MUY	7405	Multiply
DVI	7407	Divide
NMI	7411	Normalize
SHL	7413	Shift Left
ASR	7415	Arithmetic Shift Right
LSR	7417	Logical Shift Right

Double Precision Instructions

DAD	7443	Double Precision Add
DST	7445	Double Precision Store
DPIC	7573	Double Precision Increment
DCM	7575	Double Precision Complement
DPSZ	7451	Double Precision Skip if Zero

DB8-E Interprocessor Buffer

MNEMONIC	OCTAL CODE	OPERATION
DBRF	65x1	Skip if the receive flag set to a 1
DBRD	65x2	Read incoming data into the AC, clear receive flag
DBTF	65x3	Skip if the transmit flag is set to a 1
DBTD	65x4	Load the AC into the transmit buffer, transmit and set the transmit flag
DBEI	65x5	Enable the Interrupt Request line
DBDI	65x6	Disable the Interrupt Request Line
DBCD	65x7	Clear done flag

KL8-JA Terminal Control/Asynchronous Data Interface

MNEMONIC	OCTAL CODE	OPERATION
KCF	6030	Clear Receive Flag
KSF	6031	Skip on Keyboard Flag
KCC	6032	Clear Keyboard Flag and set Reader Run Flag
KRS	6033	Read Keyboard Status
KIE	6035 (AC11)	Set or clear Interrupt Enable AC11 = 1 set AC11 = 0 clear

KSE	6035 (AC10)	Set/Clear Status Enable AC10 = 1 Enable Status AC10 = 0 Disable Status
KRB	6036	Read Keyboard Buffer Combined KCC and KRS
TFL	6040	Set Transmit Flag
TSF	6041	Skip on Transmit Flag
TCV	6042	Clear Transmit Flag
TPC	6043	Load Print Buffer and Print
SPI	6045	Skip if Interrupt Enabled and Transmit or Receive Flag is set
TLS	6046	Print character. Combined TCF and TPC.

KL8-A Four-Channel Asynchronous Serial Line Unit

MNEMONIC	OCTAL CODE	OPERATION
MSIE	6XX0	Load interrupt enable from AC11; 1 = set, 0 = clear.
MSAB	6XX1	If device flag (transmit or receive) is true, branch to service routine and load AC10 and 11 with line number. Then clear transmit flag if set.
MSRA	6XX2	Read status A into AC0-11.
MSSR	6XX3	Skip on "ring," then clear if set (for lines 0, 1 and 2).
MSXD	6XX4	Transmit data.
MSRD	6XX5	Receive data; clear rec'r flag if silo empty.
MSCT	6XX6	Unconditionally clear transmit flag.
—	6XX7	Spare.
MSCD	6XY0	Clear device, flags, silos, control and status words.
MSLC	6XY1	Load control word from AC0-4.
MSLB	6XY2	Load branch address from AC0-8.

LA8 DECprinter

MNEMONIC	OCTAL CODE	OPERATION
PSSF	6660	Set printer flag
PSKF	6661	Skip printer if flag set.
PCLF	6662	Clear printer flag*
PSTB	6664	Load printer buffer
PCIE	6665	Set/clear interrupt enable**
PCLF, PSTB	6666	Load printer buffer sequence

* cleared by initialize or CAF
** set by initialize or CAF

PC8-E Reader/Punch

MNEMONIC	OCTAL CODE	OPERATION
RPE	6010	Set Reader/Punch Interrupt Enable
RSF	6011	Skip on Reader Flag
RRB	6012	Read Reader Buffer
RFC	6014	Reader Fetch Character

RFC, RRB	6016	Read Buffer and Fetch New Character
PCE	6020	Clear Reader/Punch Interrupt Enable
PSF	6021	Skip on Punch Flag
PCF	6022	Clear Punch Flag
PPC	6024	Load Punch Buffer and Punch Character
PLS	6026	Load Punch Buffer Sequence

RK8-E CONTROL AND RK05J DECPACK DRIVE

MNEMONIC	OCTAL CODE	OPERATION
DSKP	67X1	Disk skip on Flag
DCLR	67X2	Disk Clear
DLAG	67X3	Load Address and Go
DLCA	67X4	Load Current Address
DRST	67X5	Read Status Register
DLDC	67X6	Load Command Register
DMAN	67X7	Maintenance Instructions

X is the Device Code

RX8 Floppy Disk System

MNEMONIC	OCTAL CODE	OPERATION
MSIE	6XX0	Load interrupt enable from AC11; 1 = set, 0 = clear.
MSAB	6XX1	If device flag (transmit or receive) is true, branch to service routine and load AC 10 and 11 with line number. Then clear transmit flag, if set.
MSRA	6XX2	Read status A into AC0-11.
MSSR	6XX3	Skip on "ring," then clear if set (for lines 0, 1 and 2).
MSXD	6XX4	Transmit data.
MSRD	6XX5	Receive data; clear rec'r flag if silo empty.
MSCT	6XX6	Unconditionally clear transmit flag.
—	6XX7	Spare.
MSCD	6XY0	Clear device, flags, silos, control and status words.
MSLC	6XY1	Load control word from AC0-4.
MSLB	6XY2	Load branch address from AC0-8.

TM8-E Control

MNEMONIC	OCTAL CODE	OPERATION
LWCR	6701	Load Word Count Register
CWCR	6702	Clear Word Count Register
LCAR	6703	Load Current Address Register
CCAR	6704	Clear Current Address Register
LCMR	6705	Load Command Register
LFGR	6706	Load Function Register
LDBR	6707	Load Data Buffer Register
RWCR	6711	Read Word Count Register
CLT	6712	Clear Transport
RCAR	6713	Read Current Address Register
RMSR	6714	Read Main Status Register

RCMR	6715	Read Command Register
RFSR	6716	Read Function Register & Status
RDBR	6717	Read Data Buffer
SKEF	6721	Skip if Error Flag
SKCB	6722	Skip if Not Busy
SKJD	6723	Skip if Job Done
SKTR	6724	Skip if Tape Ready
CLR	6725	Clear Controller and Master

TA8-E DECassette

MNEMONIC	OCTAL CODE	OPERATION
KCLR	67X0	Clear Status Register A and B
KSDR	67X1	Skip on Data Flag
KSEN	67X2	Skip on EOT/BOT, EOF, or Drive Empty
KSBF	67X3	Skip on Ready Flag
• KLSA	67X4	Load Status A from the AC
KSAF	67X5	Skip on any flag or error
KGOA	67X6	Read Status A
KRSB	67X7	Read Status B

X is the Device Code.

APPENDIX B

ASCII[1] CHARACTER CODES

CHARACTER	8-BIT OCTAL	6-BIT OCTAL	DECIMAL EQUIVALENT (A1 FORMAT) [2]	CHARACTER	8-BIT OCTAL	6-BIT OCTAL	DECIMAL EQUIVALENT (A1 FORMAT) [2]
A	301	01	96	!	241	41	−1952
B	302	02	160	"	242	42	−1888
C	303	03	224	#	243	43	−1824
D	304	04	288	$	244	44	−1760
E	305	05	352	%	245	45	−1696
F	306	06	416	&	246	46	−1632
G	307	07	480	'	247	47	−1568
H	310	10	544	(	250	50	−1504
I	311	11	608	)	251	51	−1440
J	312	12	672	*	252	52	−1376
K	313	13	736	+	253	53	−1312
L	314	14	800	,	254	54	−1248
M	315	15	864	-	255	55	−1184
N	316	16	928	.	256	56	−1120
O	317	17	992	/	257	57	−1056
P	320	20	1056	:	272	72	−352
Q	321	21	1120	;	273	73	−288
R	322	22	1184	<	274	74	−224
S	323	23	1248	=	275	75	−160
T	324	24	1312	>	276	76	−96
U	325	25	1376	?	277	77	−32
V	326	26	1440	@	300		32
W	327	27	1504	[	333	33	1760
X	330	30	1568	\	334	34	1824
Y	331	31	1632	]	335	35	1888
Z	332	32	1696	↑(^) [3]	336	36	1952
0	260	60	−992	←(_) [3]	337	37	2016
1	261	61	−928	Leader/ Trailer	200		
2	262	62	−864	LINE FEED	212		
3	263	63	−800	Carriage RETURN	215		
4	264	64	−736	SPACE	240	40	−2016
5	265	65	−672	RUBOUT	377		
6	266	66	−608	Blank	000		
7	267	67	−544	BELL	207		
8	270	70	−480	TAB	211		
9	271	71	−416	FORM	214		

[1] An abbreviation for American Standard Code for Information Interchange.
[2] For use by 8K papertape and OS/8 FORTRAN only.
[3] The character in parentheses is printed on some Teletypes.

APPENDIX C

PROGRAM LOADING PROCEDURES FOR PAPER TAPE SYSTEMS

INTRODUCTION

This appendix provides the user with procedures to accomplish the following:

- Turn the system on.
- Load the Read IN Mode (RIM) program. RIM must be in memory to load tapes from the high or low speed paper-tape readers.
- Load the BINARY (BIN) loader—The BINARY loader is a program that is used to load the programs punched in BIN format on paper into memory.
- Load BIN paper tapes using the BINARY loader.

NOTE

RIM and BIN paper-tape formats are discussed in Chapter 4 of the *Introduction to Programming Handbook.*

TURNING ON THE SYSTEM

Before using the computer system, it is good practice to initialize all units. Ensure that all switches and controls are as specified below:

1. Main power cord is properly plugged in.
2. Teletype is turned to ON-LINE.
3. Low-speed punch is OFF.
4. Low-speed reader is set to FREE.
5. Computer POWER ON.
6. Console LOCK OFF (set to down).
7. Ensure any peripherals supplied with the system are turned on. Refer to the maintenance manual supplied with the equipment for the startup procedures.

The system is now initialized and ready for use.

READ-IN MODE (RIM) LOADER

The RIM loader is the very first program loaded into the computer, and it is loaded by the programmer console switches or the BOOT switch. Operating the BOOT switch causes a RIM program, contained in a ROM ON on the extended option module to be deposited in memory. The RIM loader instructs the computer to receive and store, in memory, data punched on paper tape in RIM coded format. (The RIM Loader is used to load the BIN loader described in the next paragraph.)

There are two RIM loader programs: one is used when the input is to be from the low-speed Teletype reader, and the other is used when input is to be from the high-speed paper-tape reader. The locations and corresponding instructions for both loaders are listed in Table C-1.

Table C-1
RIM Loader Programs

LOCATION	INSTRUCTION	
	LOW-SPEED READER	HIGH-SPEED READER
7756	6032	6014
7757	6031	6011
7760	5357	5357
7761	6036	6016
7762	7106	7106
7763	7006	7006
7764	7510	7510
7765	5357	5357
7766	7006	7006
7767	6031	6011
7770	5367	5374
7771	6034	6016
7772	7420	7420
7773	3776	3776
7774	3376	3376
7775	5356	5357
7776	0000	0000
7777	0000	0000

The procedure for loading (keypadding) the RIM loader into memory is as follows:

NOTE

On systems with an extended option module selected for paper tape bootstrap the user can press BOOT on the programmer's console twice and the RIM program is loaded automatically. Then go on to the procedure to load the BINARY loader.

1. Depress MD and then DISP to display the contents of the MD in the 4 character octal readout.
2. Enter the field that RIM is to be loaded into twice (i.e., if field 7 is being used, enter 77). Depress LXA (load extended address).
3. Enter 7756 and then depress LOAD ADDRESS (LA) to load the starting address.
4. Enter the first instruction in Table C-1 for the low-speed reader or high-speed reader and depress D NEXT.
5. Enter the remaining instructions in Table C-1; depress D NEXT after each entry.
6. After all of the instructions have been entered, enter the starting address 7756 and depress LA.

7. At this time it is a good idea to check the entries you have made in the first 5 steps. To examine the first location, enter 7756 and then depress E NEXT. The numbers displayed in the 4 character octal readout should correspond to the first number entered from Table C-1.
8. Depress E NEXT and the second number from Table C-1 will be displayed. Check each instruction by observing the number. If any errors are found, enter the address and depress LA and the correct number using the keypad switches and depress D NEXT.
9. After RIM has been loaded and checked, follow the instructions for loading the binary loader.

BINARY (BIN) LOADER

The BIN loader is a short utility program which instructs the computer to read binary-coded data punched on paper tape and store it in memory. BIN is used primarily to load the programs furnished in the software package (excluding the loaders and certain subroutines) and the programmer's binary tapes.

BIN is furnished to the programmer on punched paper tape in RIM-coded format. Therefore, RIM must be in memory before BIN can be loaded. The procedure for loading the binary loader is as follows:

1. Depress MD and then DISP to display the MD bits in the 4 character octal readout.
2. Enter the memory field into which RIM was loaded followed by the field into which BIN is to be loaded and then depress LXA.
3. Enter 7756 and depress LA. 7756 is the starting address of the RIM loader program.

NOTE

Systems with high-speed readers perform steps 4 and 5 and systems with low-speed readers perform steps 6 and 7.

4. Turn high-speed reader on.
5. Put the BINARY loader tape in the right hand side of the high speed reader with the printed arrows up and pointing to the left (proceed to step 8).
6. Set the TTY to LINE.
7. Put the BINARY loader tape in the low-speed reader with the printed arrows up and pointing toward you. Set the low-speed reader lever to START.
8. Depress INIT and RUN. The tape should read in. If the tape does not read in, go back to step 1 to be certain an operator error was not the reason the tape did not read in.
9. If the tape reals in, depress HLT/SS, when trailer (single row of holes, passes under the read head.
10. Enter the field the BINARY loader was loaded into and depress LXA.
11. Enter 7777 and depress LA.

12. The MD should read 5301. If it doesn't, go back to step 1 and do the procedure again.

When stored in memory, BIN resides on the last page of core occupying absolute locations 7625 through 7752, and location 7777.

BIN was purposely placed on the last page of core so that it would always be available for use; most of the programs in DIGITAL's software package do not use the last page of memory. The programmer must be aware that if he or she writes a program that uses the last page of memory, BIN will be overwritten when the program runs on the computer. When this happens, the programmer must load RIM and then BIN before loading binary tape.

LOADING BINARY TAPES

The procedure for loading binary tapes is as follows:

1. Verify that the BINARY loader has been loaded.
2. Depress AC and then DISP.
3. Enter the field into which the BINARY loader was loaded, and then enter the field into which binary tape is to be loaded. Depress LXA.
4. Enter 7777 and depress LA.

NOTE

Perform steps 5 and 6 for low-speed readers and steps 8, 9, and 10 for high-speed readers.

5. Turn TTY to line and put the tape in the low-speed reader, ensuring that the leader (code 200) is in the reader. The tape moves from back to front; the printed arrows on the tape should be up and pointing toward you.
6. Enter 7777 and depress LSR.
7. Set low-speed reader to START. Proceed to step 11.
8. Turn high-speed reader on.
9. Enter 3777 and press LSR.
10. Put the tape in the high-speed reader, ensuring the leader (code 200) is in the reader. The tape moves from right to left; the printed arrows on the tape should be up and pointing left.
11. Depress AC and then DISP.
12. Depress INIT and then RUN.
13. The tape should read in and stop at the first trailer code (not the physical end of tape), with the AC equal to 0000. In case of difficulty go back to step 1. Problems with reader motion are usually caused by the BIN loader not being correctly loaded. Checksum errors (AC not equal to 0) are often the result of worn tapes.

APPENDIX D

OMNIBUS SIGNAL LOCATOR

SIGNAL	OMNIBUS	SIGNAL	OMNIBUS
+5 V	AA2	GROUND	AN1
	BA2		AT1
	CA2		AC2
+15 V	DA2		AF2
−15 V	AB2		AN2
	BB2		AT2
	CB2		BC1
	DB2		BF1
BREAK CYCLE L	BL2		BN1
BREAK DATA CONT L	BK2		BT1
BRK IN PROG L	BE2		BC2
BUS STROBE L	CK1		BF2
C0 L	CE1		BN2
C1 L	CH1		BT2
C2 L	CJ1		CC1
CPMA DISABLE L	CU1		CF1
D L	DK2		CN1
DATA0 L	AR1		CT1
DATA1 L	AS1		CC2
DATA2 L	AU1		CF2
DATA3 L	AV1		CN2
DATA4 L	BR1		CT2
DATA5 L	BS1		DC1
DATA6 L	BU1		DF1
DATA7 L	BV1		DN1
DATA8 L	DR1		DT1
DATA9 L	DS1		DC2
DATA10 L	DU1		DF2
DATA11 L	DV1		DN2
E L	DL2	GROUND	DT2
EMA0 L	AD2	IND1 L	CU2
EMA1 L	AE2	IND2 L	CV2
EMA2 L	AH2	INHIBIT H	AP2
F L	DJ2	INITIALIZE H	CR1
FSET L	DP2	INT IN PROG H	BP2
GROUND	AC1	INT RQST L	CP1
GROUND	AF1	INT STROBE H	BD2

SIGNAL	OMNIBUS	SIGNAL	OMNIBUS
INTERNAL I/O L	CL1	SOURCE H	AL2
I/O PAUSE L	CD1	STOP L	DS2
IR0 L	DD2	STROBE H	AM2
IR1 L	DE2	SW	DV2
IR2 L	DH2	TEST POINT	AA1
KEY CONTROL L	DU2	↓	AB1
LA ENABLE L	BM2	↓	BA1
LINK DATA L	CR2	↓	BB1
LINK L	AV2	↓	CA1
LINK LOAD L	CS2	↓	CB1
MA0 L	AD1	↓	DA1
MA1 L	AE1	TEST POINT	DB1
MA2 L	AH1	TP1 H	CD2
MA3 L	AJ1	TP2 H	CE2
MA4 L	BD1	TP3 H	CH2
MA5 L	BE1	TP4 H	CJ2
MA6 L	BH1	TS1 L	CK2
MA7 L	BJ1	TS2 L	CL2
MA8 L	DD1	TS3 L	CM2
MA9 L	DE1	TS4 L	CP2
MA10 L	DH1	USER MODE L	DM2
MA11 L	DJ1	WRITE H	AS2
MA, MS LOAD CONT L	BH2		
MD0 L	AK1		
MD1 L	AL1		
MD2 L	AM1	In slots listed, the following non-Omnibus signals appear.	
MD3 L	AP1		
MD4 L	BK1		
MD5 L	BL1		
MD6 L	BM1	BOZA1 } Battery Empty	
MD7 L	BP1	BO3A1 }	
MD8 L	DK1		
MD9 L	DL1		
MD10 L	DL1	AO1A1 } +5	
MD11 L	DP1	AO1C1 }	
MD DIR L	AK2		
MEM START L	AJ2		
MS, IR DISABLE L	CV1	DOZA1 } Panel Lock	
NOT LAST XFER L	CM1	DO3A1 }	
NTS STALL L	BR2		
OVERFLOW L	BJ2		
POWER OK H	BV2	BOZB1 } AC Low	
PULSE LA H	DR2	BO3B1 }	
RES	BS2		
RETURN H	AR2		
ROM ADDRESS L	AU2		
RUN L	BU2		
SKIP L	CS1		

APPENDIX E

PAL8 PATCH FOR ROM PROGRAMMING

Following is the dialogue required with DS-8 to create PAL8R from PAL8:

PAL8 ROM Patch

```
/PATCH TO CONVERT PAL8 TO PAL8R ON OS8 SYSTEM USING ODT
/FORMAT PSEUDO-OP: DWRITE
.GET SYS:PAL8 CR
.ODT CR
0363/XXXX1367CR
0364/XXXX3125CR
0365/XXXX5766CR
0366/XXXX4400CR
0367/XXXX1143CR
1532/XXXX0322CR
1533/XXXX0262CR
4552/XXXX4756CR
4556/XXXX1143CR
5400/XXXX1371LF
5401/XXXX3125LF
5402/XXXX4564LF
5403/XXXX5604LF
5404/XXXX3026CR
5416/XXXX0000LF
5417/XXXX3370LF
5420/XXXX1370LF
5421/XXXX4566LF
5422/XXXX7004LF
5423/XXXX0175LF
5424/XXXX4447LF
5425/XXXX1370LF
5426/XXXX0175LF
5427/XXXX1115LF
5430/XXXX4447LF
5431/XXXX1234LF
5432/XXXX3125LF
5433/XXXX5616LF
5434/XXXX1143CR
5571/XXXX5416CR
6710/XXXX4253LF
6711/XXXX1243LF
6712/XXXX5351CR
7215/XXXX0363CR
```

```
↑C
.SAVE SYS:PAL8R CR

—
```

CR = Carriage Return
LF = Line Feed
Underlined items are Computer responses.
↑C = CTRL/C

APPENDIX F

POWER REQUIREMENTS AND MODULE ASSIGNMENT

Tables F-1 and F-2 list the PDP-8/A configurations and options, their size, preferred slot, and power requirements. The slot assignments should be rigidly adhered to since some options will not work in slots two and three. To determine the feasibility of a particular configuration, it is necessary to determine the available power for the system, compute and compare the power consumed, and total the slots used. Please contact your local DIGITAL Sales Office if any doubt exists. When configuring systems, bear in mind that DMA type devices, such as disk and magtapes, require at least 4K of read/write memory. A maximum of three core memory modules can be accommodated—either the 8K or 16K stack, each of which requires two slots.

Power Available

PROCESSOR	+5V	−15V	+15V
8A100	20A	.75A*	.75A*
8A400, 8A600 8A800, MS800	25A	2.0A	2.0A
8A420, 8A620 8A820	50A**	4.0A**	4.0A**

* The sum of +15V and −15V must not exceed 1A total.

** Total current. These processors have dual power supplies. One supply provides 25A @ +5V, 2A @ +15V and 2A @ −15V to the top 10 slots, and the other supply provides the same voltages to the bottom 10 slots. Therefore, the power consumption must be balanced between the top 10 slots and the bottom 10 slots.

Table F-1 Basic PDP-8/A Configurations and Power Requirements

OPTION	+5V	−15V	+15V	NUMBER OF OMNIBUS SLOTS USED
8A100-AC (115 Vac) 8A100-AD (230 Vac)	6.40A	0.04A	NA	2
8A100-AE (115 Vac) 8A100-AF (230 Vac)	7.10A	0.04A	NA	2
8A100-AK (115 Vac) 8A100-AL (230 Vac)	8.50A	0.04A	NA	2
8A100-FA (115 Vac) 8A100-FB (230 Vac)	8.80A	0.39A	NA	2
8A400-EM (115 Vac) 8A400-EN (230 Vac)	8.50A	0.04A	NA	4
8A400-EP (115 Vac) 8A400-ER (230 Vac)	8.50A	0.04A	NA	4
8A400-BM (115 Vac) 8A400-BN (230 Vac)	9.50A	0.04A	NA	4
8A400-BP (115 Vac) 8A400-BR (230 Vac)	9.50A	0.04A	NA	4
8A420-BM (115 Vac) 8A420-BN (230 Vac)	9.50A	0.04A	NA	4
8A420-BP (115 Vac) 8A420-BR (230 Vac)	9.50A	0.04A	NA	4
8A600-BM (115 Vac) 8A600-BN (230 Vac)	9.00A	1.0A	.53A	7
8A600-BP (115 Vac) 8A600-BR (230 Vac)	9.00A	1.0A	.53A	7
8A620-BM (115 Vac) 8A620-BN (230 Vac)	9.00A	1.0A	.53A	7
8A620-BP (115 Vac) 8A620-BR (230 Vac)	9.00A	1.0A	.53A	7
8A800-PM (115 Vac) 8A800-PN (230 Vac)	18.30A	NA	NA	6
8A800-PP (115 Vac) 8A800-PR (230 Vac)	18.30A	NA	NA	6
8A820-PM (115 Vac) 8A820-PN (230 Vac)	18.30A	NA	NA	6
8A820-PP (115 Vac) 8A820-PR (230 Vac)	18.30A	NA	NA	6
MS800-AA (115 Vac) MS800-AD (230 Vac)	13.00A	.14A	.06A	6
MS800-BA (115 Vac) MS800-BD (230 Vac)	13.00A	.14A	.06A	6
MS880-CA (115 Vac) MS880-CD (230 Vac)	21.8A	.14A	.06A	8
MS880-DA (115 Vac) MS880-DD (230 Vac)	21.8A	.14A	.06A	8

Figure F-1 illustrates the Omnibus slot assignments for semiconductor memory machines. There are 10 slots available.

CPU	1
DKC8-AA OR KM8-A	2
DKC8-AA OR KM8-A	3
OPTIONS & CONTROLLERS (QUAD OR HEX)	4 THRU 10

Figure F-1 Omnibus Assignments for Semiconductor Machines

Some options can be plugged into slots 2 and 3 (see Table F-2). Core memory will not run in semiconductor machines.

Figure F-2 illustrates the Omnibus slot assignments for core memory machines. There are 12 slots available.

CPU	1
DKC8-AA OR KM8-AA	2
DKC8-AA OR KM8-AA	3
MM8-AA (CORE) OR OPTIONS	4 5 6 7 8
OPTIONS OR ROM, RAM, PROM	9 10 11 12

Figure F-2 Omnibus Slot Assignments for Core Machines

MM8-AA core requires 2 slots per memory and may only be mounted in slots 4–8. Some options can be plugged into slots 2 and 3 (see Table F-2).

Table F-2 Omnibus Slot Assignment and Power Requirements

OPTION OPTION	BOARD SIZE BOARD SIZE	+5V +5V	−15V −15V	+15V +15V	ASSIGNED SLOT NO.	NUMBER OF OMNIBUS SLOTS USED
AD8-A, B	QUAD	3.25A	NA	NA	4-Last	1
CM8-F (control)	QUAD	0.55A	NA	NA	4-Last	1
CR8-F (control)	QUAD	0.55A	NA	NA	4-Last	1
DB8-EA	QUAD	0.80A	0.03A	NA	2-Last	1
DKC8-AA	HEX	2.00A	0.10A	0.06A	2-3	1
DK8-EC	QUAD	0.34A	NA	NA	2-Last	1
DK8-EP	QUAD	1.43A	0.07A	NA	2-Last	2
DP8-EA, EB	QUAD	1.80A	0.11A	0.05A	2-Last	2
DR8-EA	QUAD	2.25A	NA	NA	2-Last	1
DR8-ED	QUAD	1.50A	NA	NA	4-Last	1
FPP8-A	DOUBLE HEX	8.80A	NA	NA		2
KA8-E	QUAD	1.40A	NA	NA	2-Last	1
KC8-AA, AB	FRONT PANEL	2.50A	NA	NA	NA	0
KD8-E	QUAD	1.20A	NA	NA	2-Last	1
KE8-E	QUAD	1.59A	NA	NA	4-Last	2
KG8-EA	QUAD	0.94A	NA	NA	4-Last	1
KL8-A	HEX	2.50A	0.42A	0.09A	4-Last	1
KL8-E	QUAD	0.80A	0.07A	0.07A	4-Last	1
KL8-JA	QUAD	1.10A	0.10A	0.05A	2-Last	1
KL8-M	QUAD	0.40A	0.04A	0.04A	2-Last	1
KM8-AA	HEX	2.00A	NA	NA	2-3	1
KM8-E	QUAD	1.00A	NA	NA	4-Last	1
LA8 (Control)	QUAD	0.65A	NA	NA	4-Last	1
LE8 (Control)	QUAD	0.35A	NA	NA	2-Last	1
M1703	QUAD	0.55A	NA	NA	4-Last	1
M1705	QUAD	1.15A	NA	NA	4-Last	1
MI8-E	QUAD	0.71A	0.27A	NA	4-Last	1
MM8-AA operating or Steady State	DOUBLE HEX	2.50A	NA	NA	4-8* or 4-11	2 2
MM8-AB operating or Steady State	DOUBLE HEX	2.50A	NA	NA	4-8* or 4-11	2 2
MR8-AA	QUAD	2.00A	NA	NA	2-Last	1
MR8-AB	QUAD	3.00A	NA	NA	2-Last	1
* Core memory slots on 12-slot versions (8A400, 8A600, 8A800, MS800 & MS880) are 4-8. Core memory slots on 20-slot versions (8A420, 8A620 & 8A820) are 4-11.						
MR8-AC	QUAD	4.00A	NA	NA	2-Last	1
MR8-AD	QUAD	5.00A	NA	NA	2-Last	1
MR8-FB	QUAD	3.80A	0.35	NA	2-Last	1
MR8-SA (Control)	QUAD	0.80A	0.03A	NA	2-Last	1
MR8-SL (Control)	QUAD	1.15A	NA	NA	4-Last	1
MS8-AA	QUAD	1.40A	NA	NA	4-Last	1
MS8-AB	QUAD	2.10A	NA	NA	4-Last	1
MS8-AD	QUAD	3.50A	NA	NA	4-Last	1
PC8-E, PR8-E (Control)	QUAD	0.84A	0.05A	NA	4-Last	1
RK8J-E (Control)	QUAD	3.10A	NA	NA	4-Last	3
RX8 (Control)	QUAD	1.50A	NA	NA	4-Last	1
TA8 (Control)	QUAD	2.80A	NA	NA	2-Last	1
TD8-E (Control)	QUAD	1.25A	0.08A	NA	2-Last	1
TM8 (Control)	QUAD	4.18A	NA	NA	4-Last	4
VC8-E	QUAD	0.31A	NA	NA	2-Last	2
XY8-E	QUAD	0.42A	0.03A	0.01A	4-Last	1

APPENDIX G

CONFIGURATIONS AND OPTIONS

8A100 SERIES

OPTION	DESCRIPTION	OPTION	DESCRIPTION
8A100-AC* 115 V/60 Hz, 8A100-AD* 230 V/50 Hz	Computer, 1K RAM Memory, rack mountable. Unit consists of: 1 KK8-A Central Processor 1 MS8-AA 1K RAM Memory 1 Operator's Panel 1 Combination Power Supply, Chassis and Omnibus with 10 slots.	8A100-AK* 115 V/60 Hz, 8A100-AL* 230 V/50 Hz	Computer, 4K RAM Memory, rack mountable. Unit consists of: 1 KK8-A Central Processor 1 MS8-AD 4K RAM Memory 1 Operator's Panel 1 Combination Power Supply, Chassis and Omnibus with 10 slots.
8A100-AE* 115 V/60 Hz, 8A100-AF* 230 V/50 Hz	Computer, 2K RAM Memory, rack mountable. Unit consists of: 1 KK8-A Central Processor 1 MS8-AB 2K RAM Memory 1 Operator's Panel 1 Combination Power Supply, Chassis and Omnibus with 10 slots.	8A100-FA* 115 V/60 Hz, 8A100-FB* 230 V/50 Hz	Computer, 1K PROM Memory, rack mountable. Unit consists of: 1 KK8-A Central Processor 1 MR8-FB 1K PROM Memory 1 Operator's Panel 1 Combination Power Supply, Chassis and Omnibus with 10 slots.

* These designations will replace the configuration designation in Table F-1.

8A100 MEMORY OPTIONS

OPTION	DESCRIPTION	OPTION	DESCRIPTION
MS8-AA	1K Semiconductor Random Access Memory (RAM)	MR8-AB	2K Semiconductor Blastable Read-Only Memory (ROM)
MS8-AB	2K Semiconductor Random Access Memory (RAM)	MR8-AD	4K Semiconductor Blastable Read-Only Memory (ROM)

8A100 MEMORY OPTIONS

OPTION	DESCRIPTION	OPTION	DESCRIPTION
MS8-AD	4K Semiconductor Random Access Memory (RAM)	MR8-FB	1K UV Erasable Reprogrammable Read-Only Memory (PROM)
MR8-AA	1K Semiconductor Blastable Read-Only Memory (ROM)		

8A400 SERIES

OPTION	DESCRIPTION	OPTION	DESCRIPTION
8A400-EM 115 V/60 Hz, 8A400-EN 230 V/60 Hz	Computer, 8K Core Memory, rack mountable. Unit consists of: 1 KK8-A Central Processor 1 MM8-AA 8K Core Memory 1 Operator's Panel 1 KM8-E Memory Extension Control 1 Combination Power Supply, Chassis and Omnibus with 12 slots.	8A400-BM 115 V/60 Hz, 8A400-BN 230 V/50 Hz	Computer, 8K Core Memory, rack mountable. Unit consists of: 1 KK8-A Central Processor 1 MM8-AA 8K Core Memory 1 Operator's Panel 1 KM8-AA Extended Option Board 1 Combination Power Supply, Chassis and Omnibus with 12 slots.
8A400-EP 115 V/60 Hz, 8A400-ER 230 V/60 Hz	Computer, 16K Core Memory, rack mountable. Unit consists of: 1 KK8-A Central Processor 1 MM8-AB 16K Core Memory 1 Operator's Panel 1 KM8-E Memory Extension Control 1 Combination Power Supply, Chassis and Omnibus with 12 slots.	8A400-BP 115 V/60 Hz, 8A400-BR 230 V/50 Hz	Computer, 16K Core Memory rack mountable. Unit consists of: 1 KK8-A Central Processor 1 MM8-AB 16K Core Memory 1 Operator's Panel 1 KM8-AA Extended Option Board 1 Combination Power Supply, Chassis and Omnibus with 12 slots.

8A400 MEMORY OPTIONS

MM8-AA	8K Core Memory	MR8-AD	4K Semiconductor Blastable Read-Only Memory (ROM)
MM8-AB	16K Core Memory		

8A400 MEMORY OPTIONS (Cont.)

MR8-AA	1K Semiconductor Blastable Read-Only Memory (ROM)	MR8-FB	1K UV Erasable Reprogrammable Read-Only Memory (PROM)
MR8-AB	2K Semiconductor Blastable Read-Only Memory (ROM)		

MULTIPLE OPTION BOARDS

OPTION	DESCRIPTION	OPTION	DESCRIPTION
DKC8-AA	Input/Output Option Board. Includes: Real-Time Clock—100 Hz fixed-frequency, Programmer's Console Control, Input/Output, Interface, 12-bit Parallel I/O, Asynchronous Serial Line Unit, Switch Selectable Baud Rates of 110, 150, 300, 600, 1200, 2400, 4800, 9600.	KM8-AA	Extended Option Board. Includes: Memory Extension and Timeshare Control, Power Fail and Auto Restart, Bootstrap Loader, Switch Selectable for DECtape (TC08, TD8-E), Disk (RK8-E, DF32, RF08) Cassette and Paper-tape Reader.