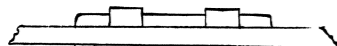


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MODULE VARIATIONS AA&CA

- 1.
2. W2 THRU W5 SHOULD BE INSTALLED WITH ASSEMBLY SPACERS SO THAT THEY LOOK LIKE THE FOLLOWING:



3. R. PACKS SHOULD BE INSTALLED SO THAT LEADS DO NOT INTERFERE WITH OTHER COMPONENTS
4. ⊗ WIRE WRAP PIN.

MEMORY TYPE	JUMPER CONFIG	VARIATION
NON-PARITY	5-7	AA, CA

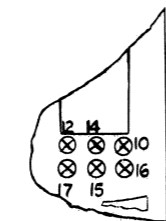
MEMORY SIZE	JUMPER CONFIG	VARIATION
4K	17-15	AA
16K	16-15	CA

7. OPTIONAL JUMPER I-2 WILL ALLOW USER TO EXTEND USABLE MEMORY SPACE FROM 28K TO 30K. NORMAL JUMPER IS I-3.

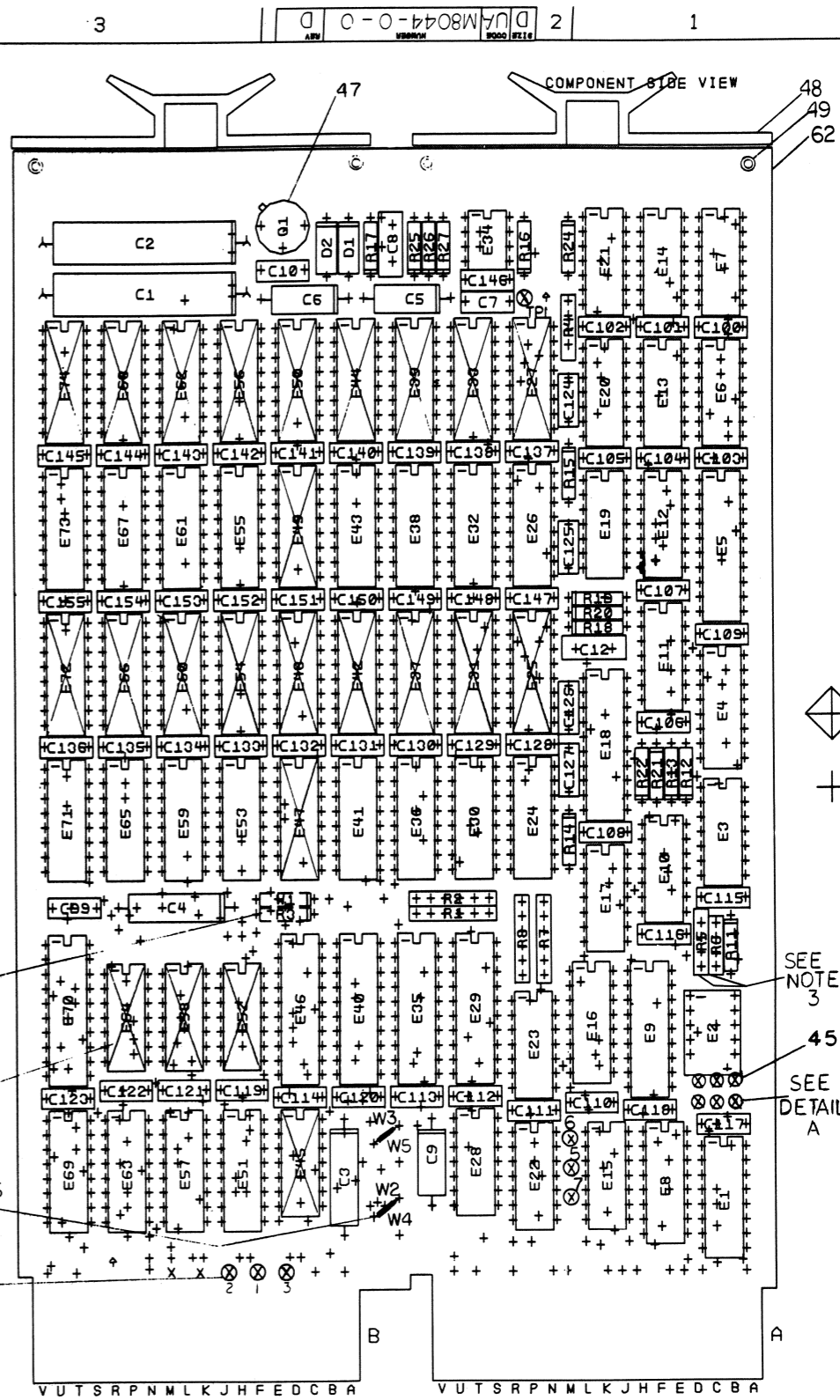
JUMPER	BATTERY BACK-UP	NON BATTERY BACK-UP
W2	OUT	IN
W3	OUT	IN
W4	IN	OUT
W5	IN	OUT

MEMORY SIZE	W1	R3	VARIATION
4K	IN	OUT	AA
16K	OUT	IN	CA

10. THE FOLLOWING IC'S ARE NOT INSTALLED IN AA & CA VARIATIONS:
 E25, 27, 31, 33, 37, 39, 42, 44, 45, 47, 48, 49, 50, 52, 54, 56, 58, 60, 62, 64, 66, 68, 72 & 74.



DETAIL A



SEE NOTE 9
 SEE NOTE 10
 SEE NOTES 2 & 8
 SEE NOTE 7

SEE NOTE 3
 SEE DETAIL A

NOTES:

CHK	CHANGE NO	REV	DATE	BY
✓	1	0001	C	
✓	2	0002	D	
✓	3	0003	E	
✓	4	0004	F	
✓	5	0005	G	
✓	6	0006	H	
✓	7	0007	I	
✓	8	0008	J	
✓	9	0009	K	
✓	10	0010	L	
✓	11	0011	M	
✓	12	0012	N	
✓	13	0013	O	
✓	14	0014	P	
✓	15	0015	Q	
✓	16	0016	R	
✓	17	0017	S	
✓	18	0018	T	
✓	19	0019	U	
✓	20	0020	V	
✓	21	0021	W	
✓	22	0022	X	
✓	23	0023	Y	
✓	24	0024	Z	

ETCH REV. D-P
P.C. DESIGN DATA BASE REV. DL & DM

SIGNATURES	DATE
DRN. ✓ [Signature]	2-2-78
CHK'D. [Signature]	2-20-78
ENC.	
PROJ. ENG.	
PROD.	
SCALE 2/1	
SHT. OF 8	
NEXT HIGHER ASSY. B-DD-M8045-0	

digital	
TITLE 32K 16BIT MOS MEMORY	
SIZE CODE	NUMBER
0 UA	M8044-0-0
REV	D

8

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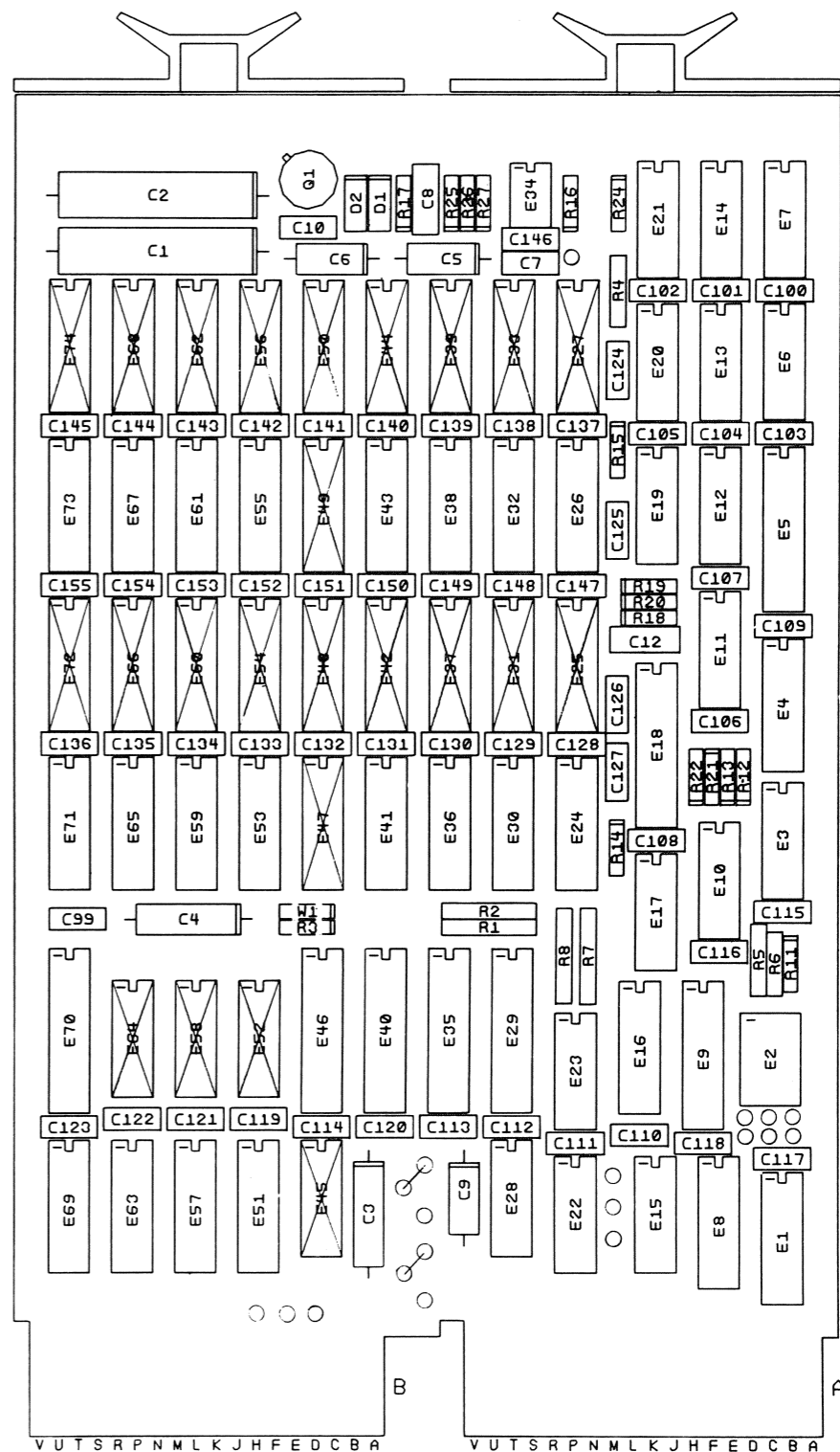
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2

1

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MODULE VARIATIONS AA CA



NOTES:

CHG	NO	REV

SIGNATURES		DATE
DRN.		
CHK'D.		3-20-77
ENG.		
PROJ. ENG.		
PROD.		
SCALE 2/1		
SHT. 2 OF 8		
NEXT HIGHER ASSY. E-DD-M8044-0-0		
TITLE		digital
32K 16 BIT MOS MEMORY		
SIZE CODE	NUMBER	REV
0 UA M8044-0-0		D

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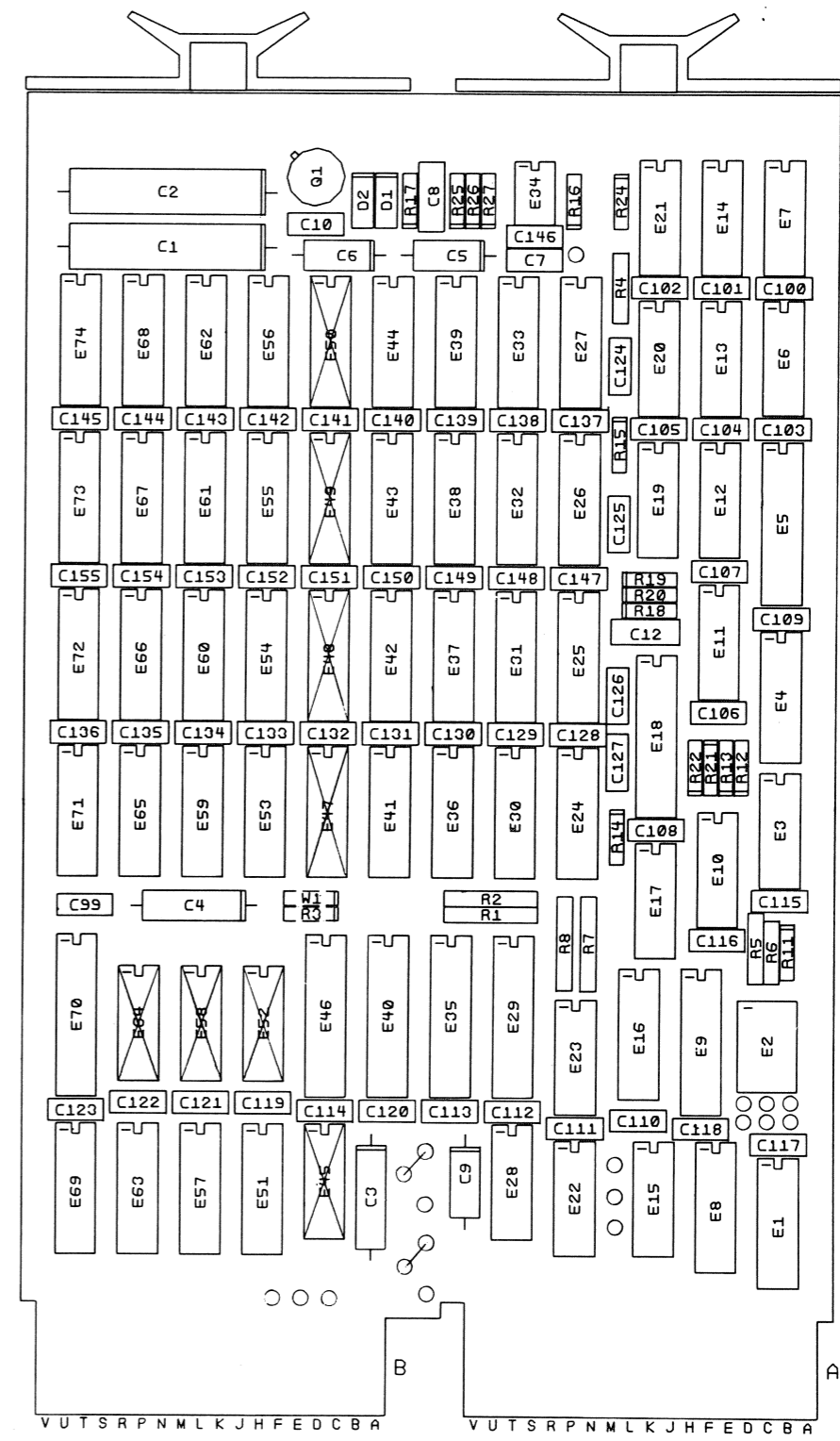
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ml 1 MS#261966

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MODULE VARIATIONS BA & DA



NOTES:

CHK	CHANGE	NO	REV

SIGNATURES		DATE	digital
DRN.		3-20-77	
CHK'D.	Richard V. DeMaris	3-20-77	
ENC.			
PROJ. ENG.			TITLE
PROD.			32K 16BIT MOS MEMORY
SCALE	2/1		SIZE CODE
SHT.	4 OF 8		NUMBER
NEXT HIGHER ASSY.	B-DD-M8044-0-0		REV
			D

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1-0-7708W 2

NOTES:

1. Ⓢ = WIRE WRAP PIN

2.

TYPE MEMORY	JUMPER CONFIGURATION
NON PARITY	5 TO 7
PARITY	5 TO 6

3.

TYPE	JUMPER CONFIGURATION
4K	17 TO 15 & 17 TO 14
8K	17 TO 15 & 12 TO 14
16K	16 TO 15 & 16 TO 14
32K	16 TO 15 & 10 TO 14

4.

DEC (K)	OCTAL	SWITCH SETTING (X = OFF)				
		SI-1	SI-2	SI-3	SI-4	SI-5
0	000000					
4	020000					X
8	040000				X	
12	060000				X	X
16	100000			X		
20	120000			X		X
24	140000			X	X	
28	160000			X	X	X
32	200000		X			
36	220000		X			X
40	240000		X		X	
44	260000		X		X	X
48	300000		X	X		
52	320000		X	X		X
56	340000		X	X	X	
60	360000		X	X	X	X
64	400000	X				
68	420000	X				X
72	440000	X			X	
76	460000	X			X	X
80	500000	X		X		
84	520000	X		X		X
88	540000	X		X	X	
92	560000	X		X	X	X
96	600000	X	X			
100	620000	X	X			X
104	640000	X	X		X	
108	660000	X	X		X	X
112	700000	X	X	X		
116	720000	X	X	X		X
120	740000	X	X	X	X	
124	760000	X	X	X	X	X

5. NORMAL JUMPER 1 TO 3. OPTIONAL JUMPER 1 TO 2 WILL ALLOW USER TO EXTEND USABLE MEMORY SPACE FROM 28K TO 30K.

6.

JUMPER	BATTERY BACK-UP	NON BATTERY BACK-UP
W2	OUT	IN
W3	OUT	IN
W4	IN	OUT
W5	IN	OUT

7.

MEMORY SIZE	W1	R3
4K	IN	OUT
8K	IN	OUT
16K	OUT	IN
32K	OUT	IN

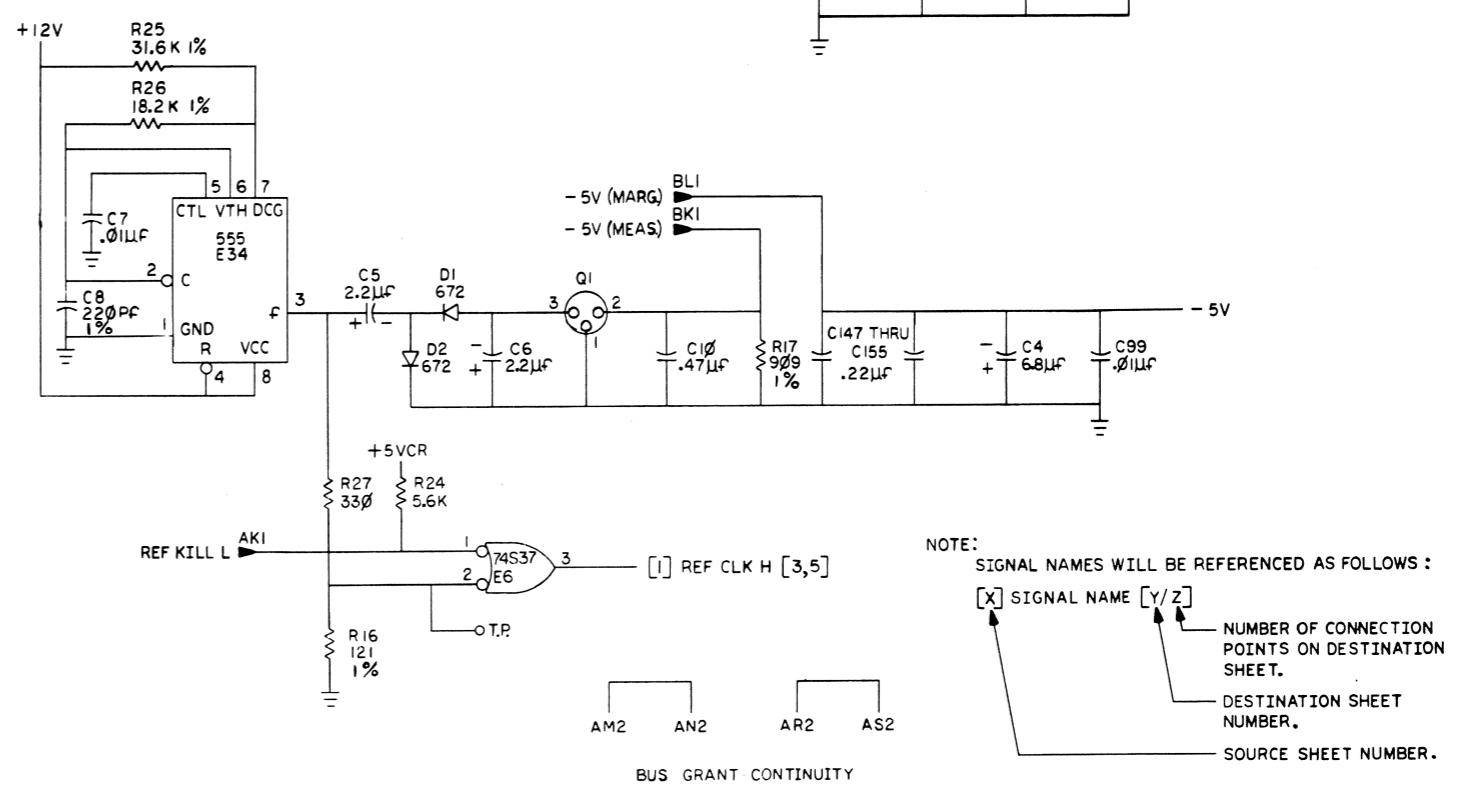
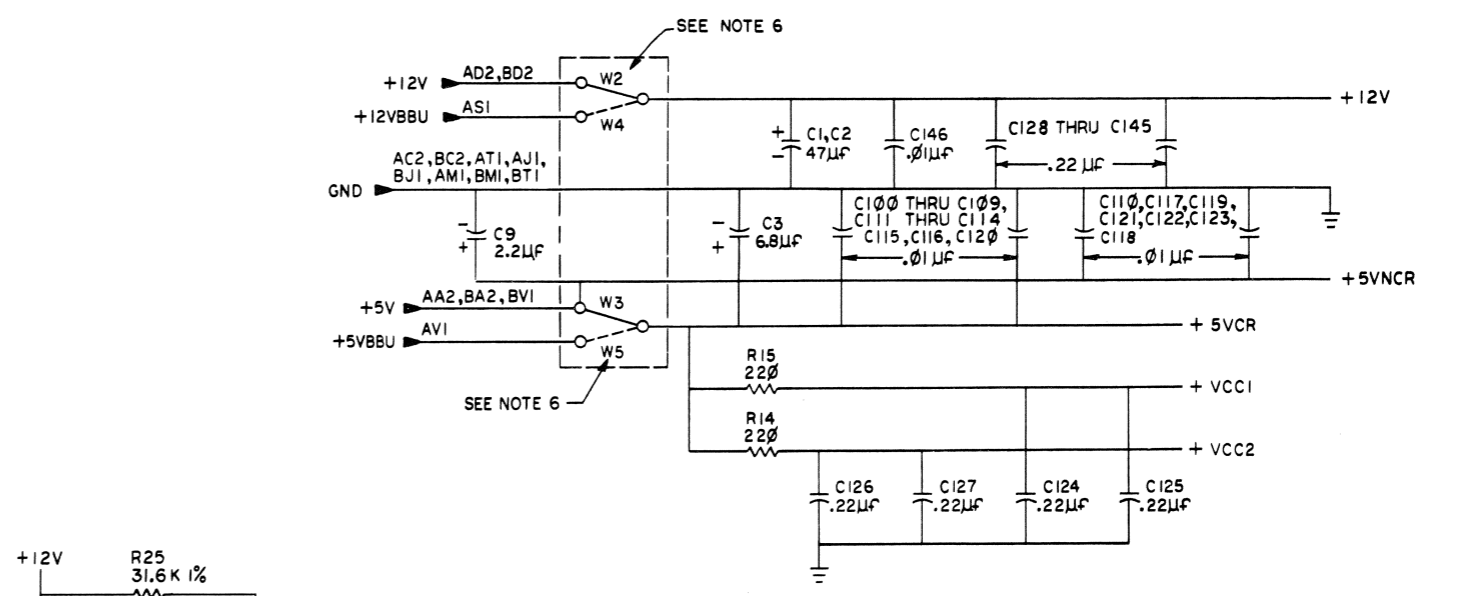
8.

OPTION DESIGNATION	PRIMARY VARIATION	SYSTEM DESCRIPTION
MSVII-DA	M8044-AA	4K X 16 BITS
MSVII-DB	M8044-BA	8K X 16 BITS
MSVII-DC	M8044-CA	16K X 16 BITS
MSVII-DD	M8044-DA	32K X 16 BITS

9.

IC TYPE	+5V	GND	+12V	-5V
555		1	8	
MOS	9	16	8	1
74S373	20	10		
74LS393	14	7		
74S280	14	7		
74S74	14	7		
74S10	14	7		
74S11	14	7		
8641	16	8		
8640	8	1		
74S240	20	10		
74S37	14	7		
74S22	14	7		
1Kx4 PROM	18	9		
74S02	14	7		
74LS75	5	12		
74S32	14	7		
74LS10	14	7		
74LS240	20	10		

10. THESE I.C.'S USED ONLY IN 8K & 32K CONFIG'S.



NOTE: SIGNAL NAMES WILL BE REFERENCED AS FOLLOWS:
 [X] SIGNAL NAME [Y/Z]
 NUMBER OF CONNECTION POINTS ON DESTINATION SHEET.
 DESTINATION SHEET NUMBER.
 SOURCE SHEET NUMBER.

REVISIONS

CHK	CHANGE NO.	REV.
R	1	B
R	2	C
R	3	D

DRN Steve Garity	0-25-77	FIRST USED ON	MSVII-D	digital
CHK'D R GIVEN	2-21-78	TITLE	32K 16BIT MOS MEM	
ENG. R GIVEN	2-21-78	SCALE	1	
PROJ. ENG. R. SUM	2-21-78	SIZE CODE	D CS	
PROD. R. M. L.	2-21-78	NUMBER	M8044-0-1	
NEXT HIGHER ASSY.		REV.	C	
B-DD-M8044-0		SHEET	1 OF 7	
SCALE		DIST.		

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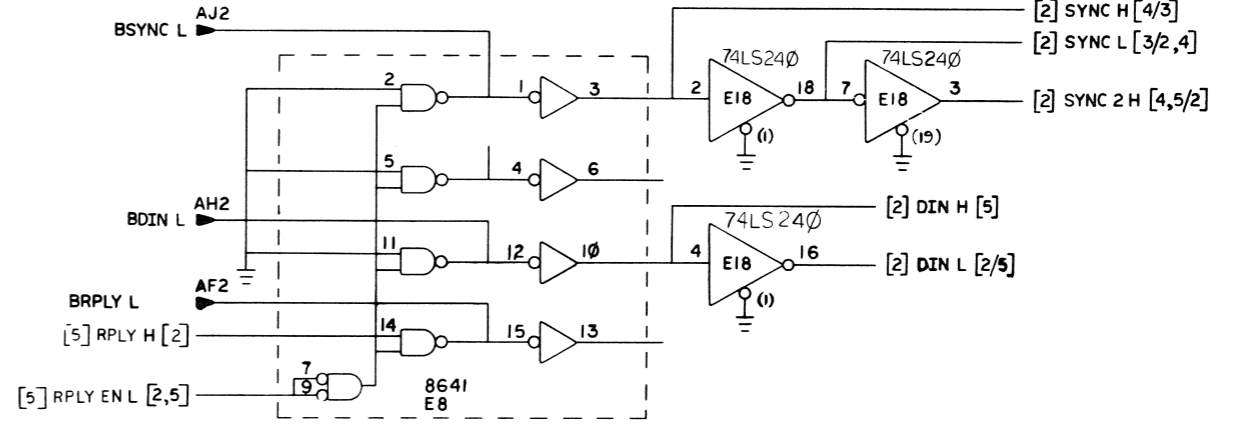
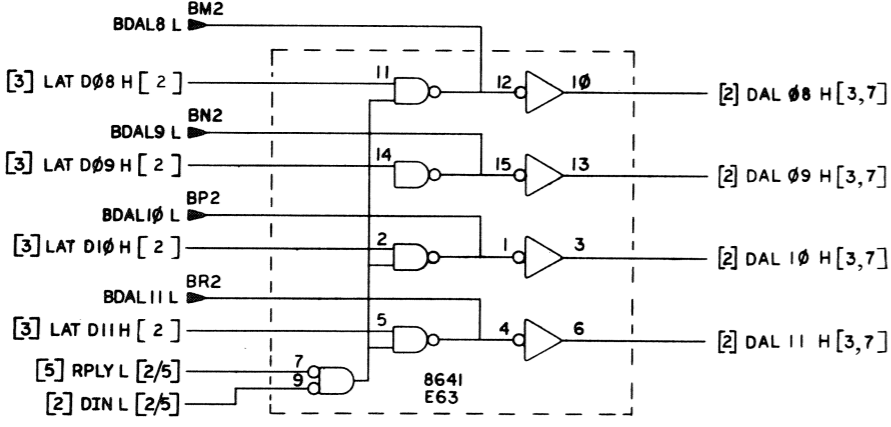
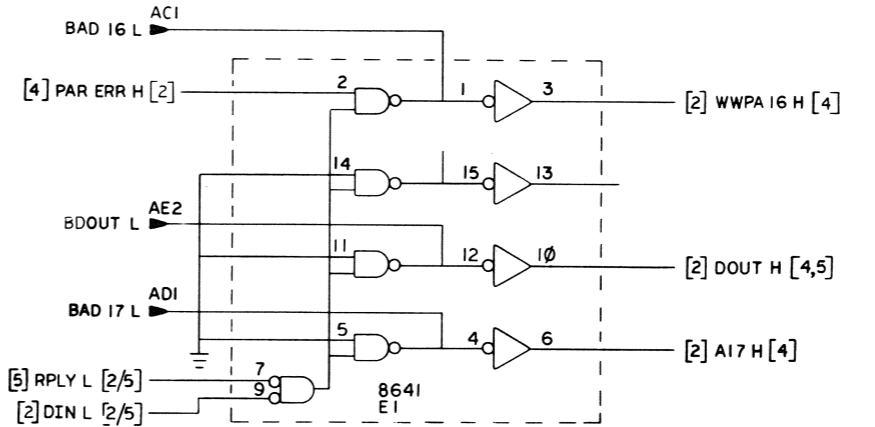
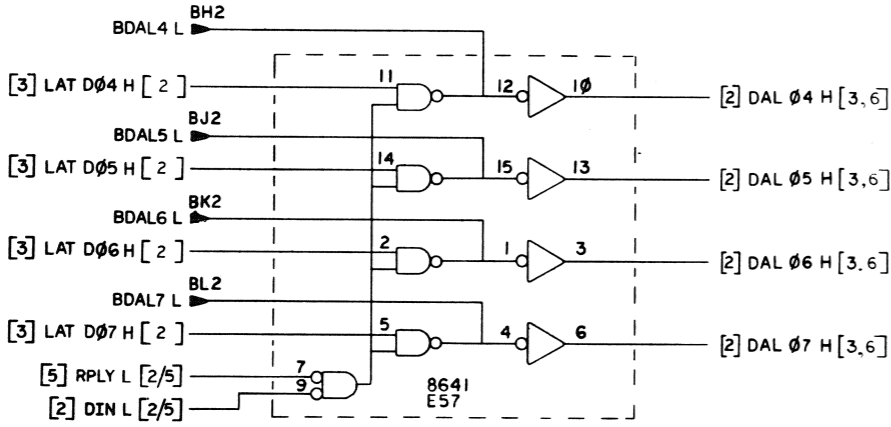
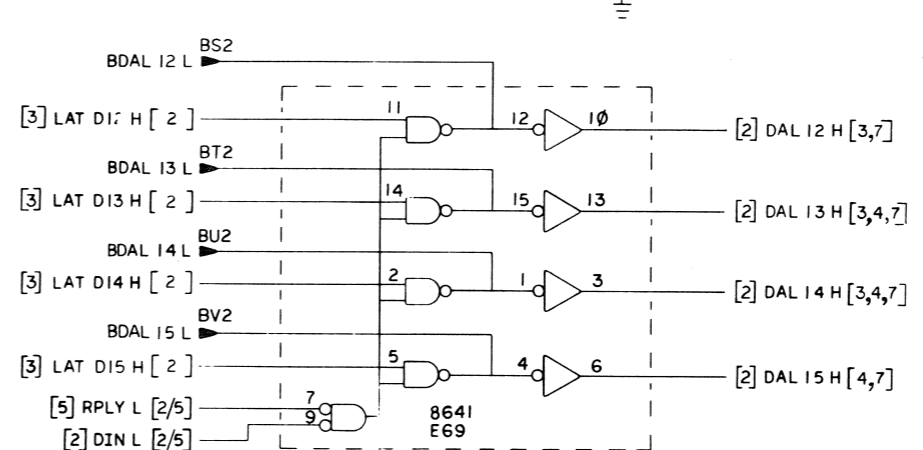
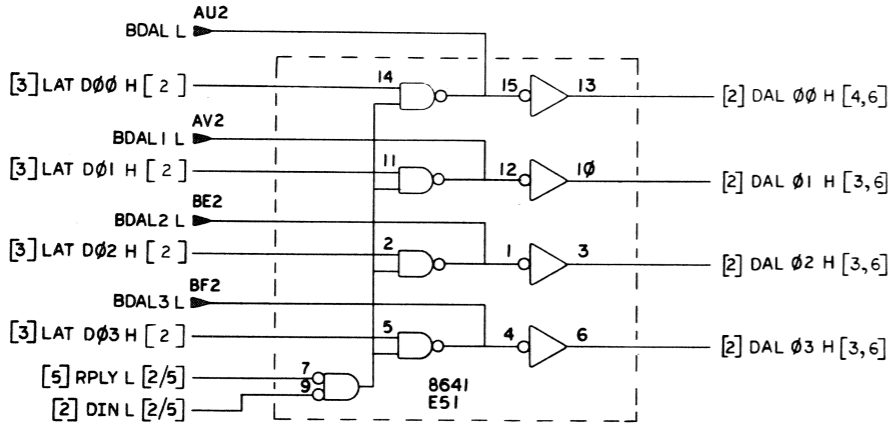
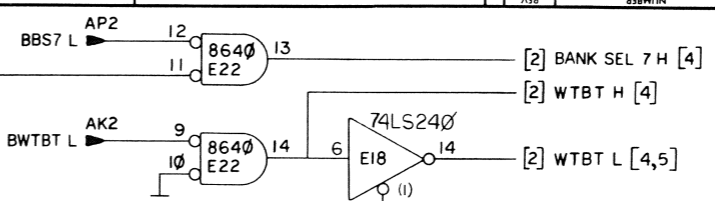
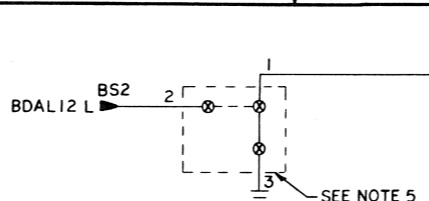
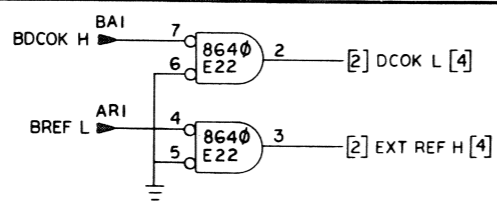
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1

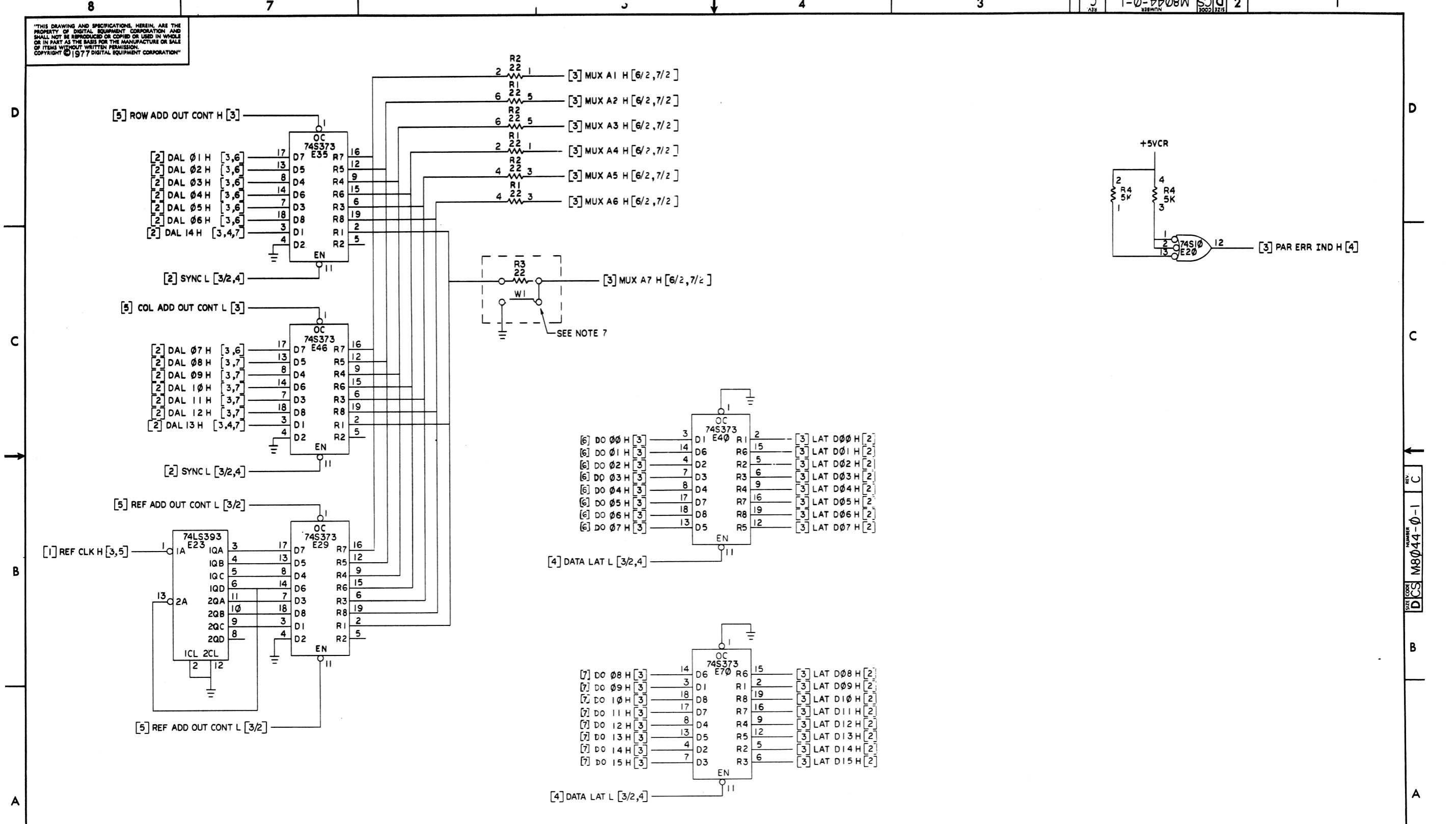
D CS M8044-0-1 2

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REVISIONS		
CHK	CHANGE NO.	REV.

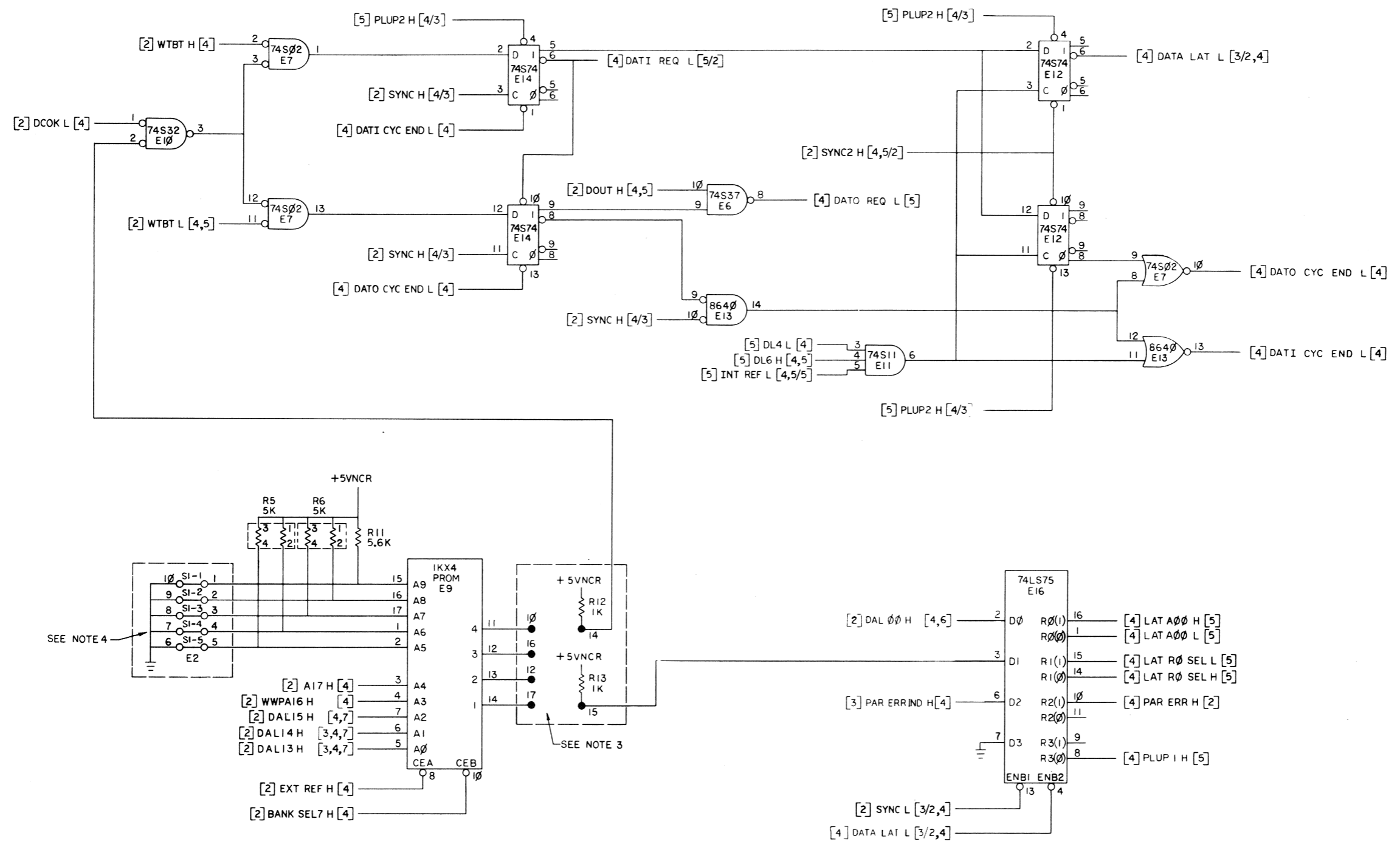
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REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE CODE	NUMBER	REV.
32K 16BIT MOS MEM	DCS	M8044-0-1	C
SCALE	SHEET	DIST.	
	3 OF 7		

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SEE NOTE 4

SEE NOTE 3

REVISIONS		
CHK	CHANGE NO.	REV.

REV. C
M8044-0-1
DCS

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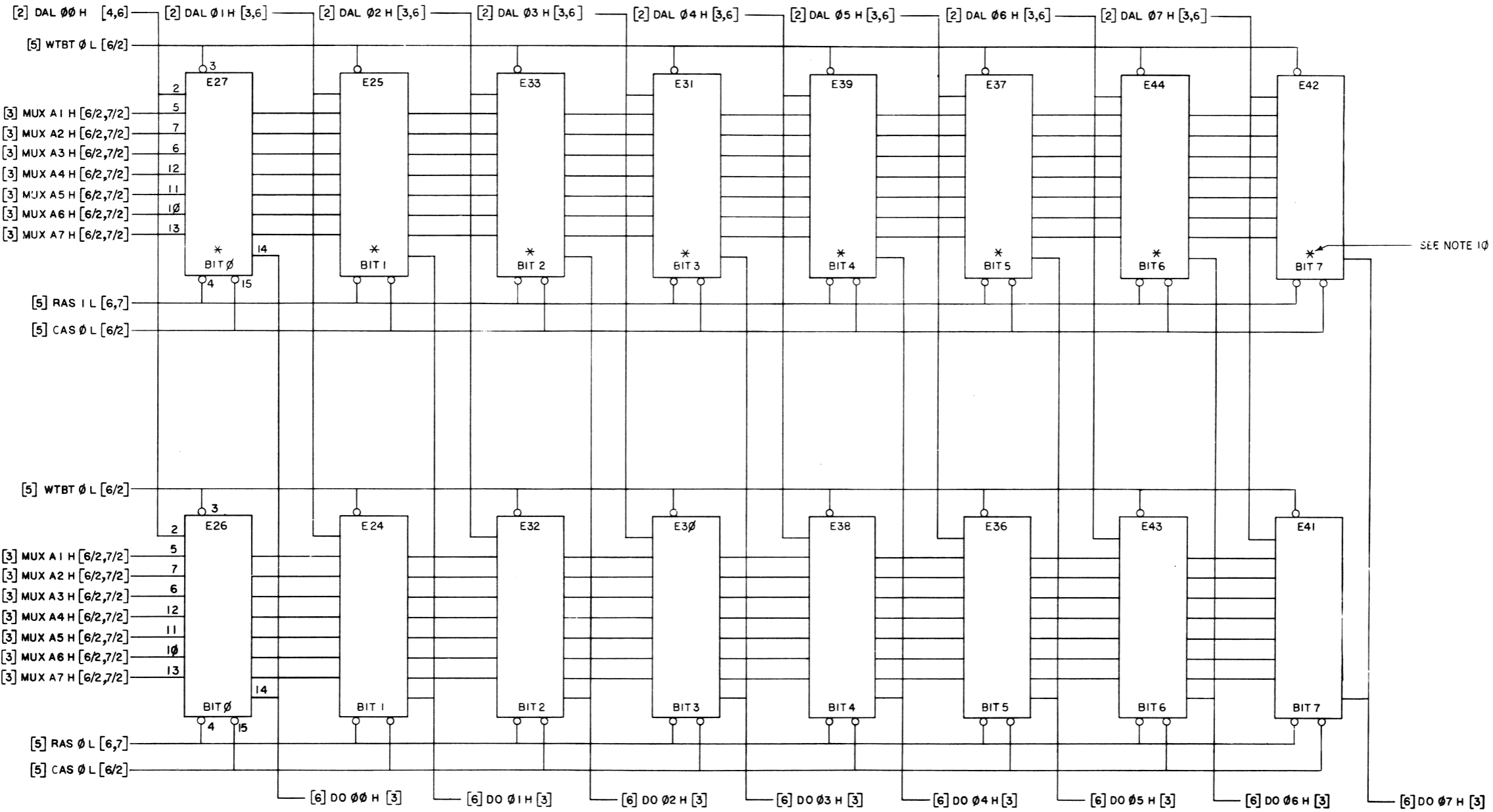
DCS M8044-0-1

1

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D
C
B
A

D
C
B
A



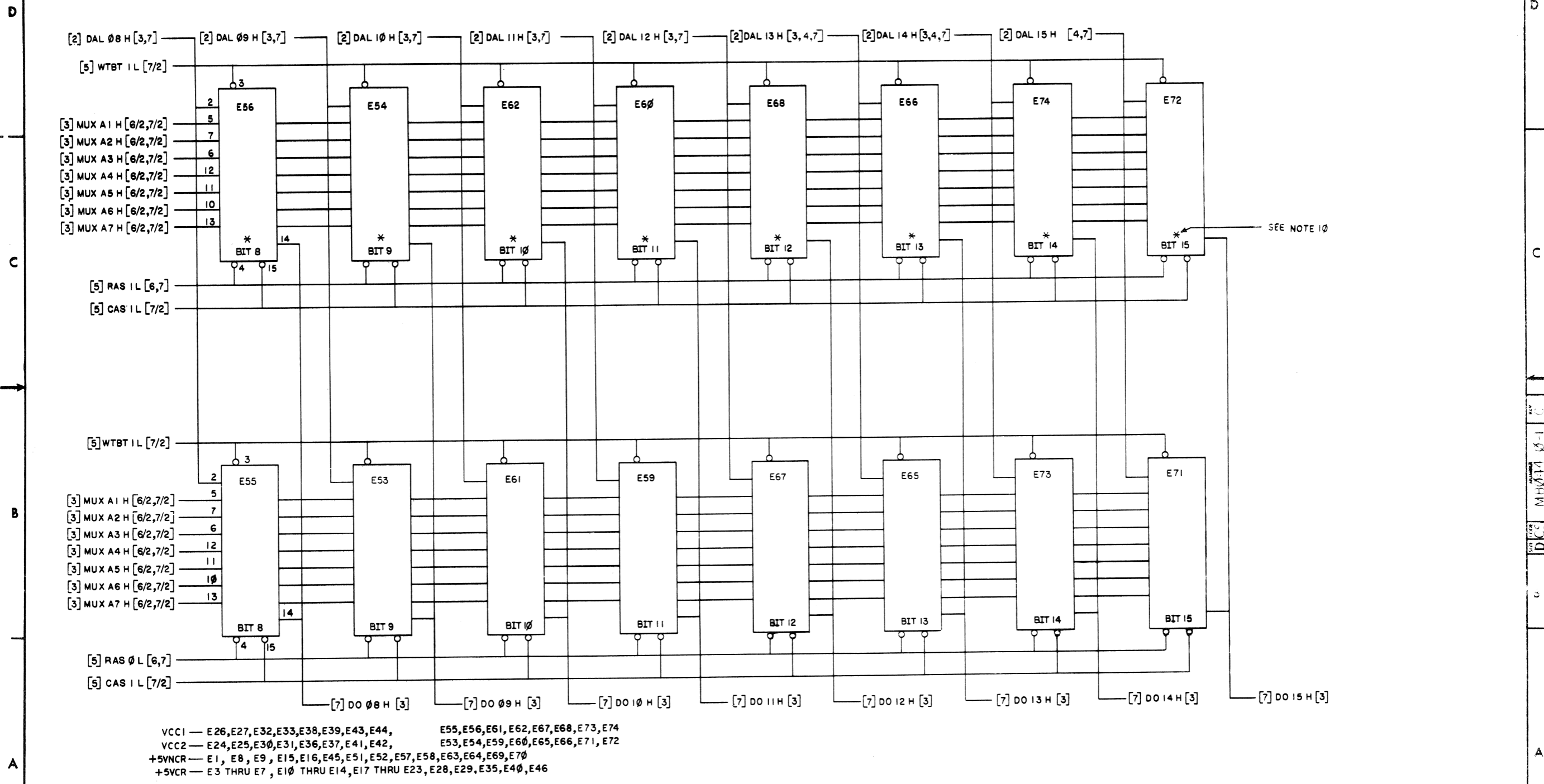
VCC1 — E26, E27, E32, E33, E38, E39, E43, E44, E55, E56, E61, E62, E67, E68, E73, E74
 VCC2 — E24, E25, E30, E31, E36, E37, E41, E42, E53, E54, E59, E60, E65, E66, E71, E72
 +5VNCR — E1, E8, E9, E15, E16, E45, E51, E52, E57, E58, E63, E64, E69, E70
 +5VCR — E3 THRU E7, E10 THRU E14, E17 THRU E23, E28, E29, E35, E40, E46

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	32 K 16 BIT MOS MEM	SIZE CODE	DCS	NUMBER	M8044-0-1	REV.	C
SCALE	1/1	SHEET	6 OF 7	DIST.			

8 7 6 5 4 3 2 1 MLC

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VCC1 — E26, E27, E32, E33, E38, E39, E43, E44, E55, E56, E61, E62, E67, E68, E73, E74
 VCC2 — E24, E25, E30, E31, E36, E37, E41, E42, E53, E54, E59, E60, E65, E66, E71, E72
 +5VNCR — E1, E8, E9, E15, E16, E45, E51, E52, E57, E58, E63, E64, E69, E70
 +5VCR — E3 THRU E7, E10 THRU E14, E17 THRU E23, E28, E29, E35, E40, E46

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	32K 16 BIT MOS MEM	SIZE CODE	D CS	NUMBER	M8044-0-1	REV.	C
SCALE	/ /	SHEET	7 OF 7	DIST.			