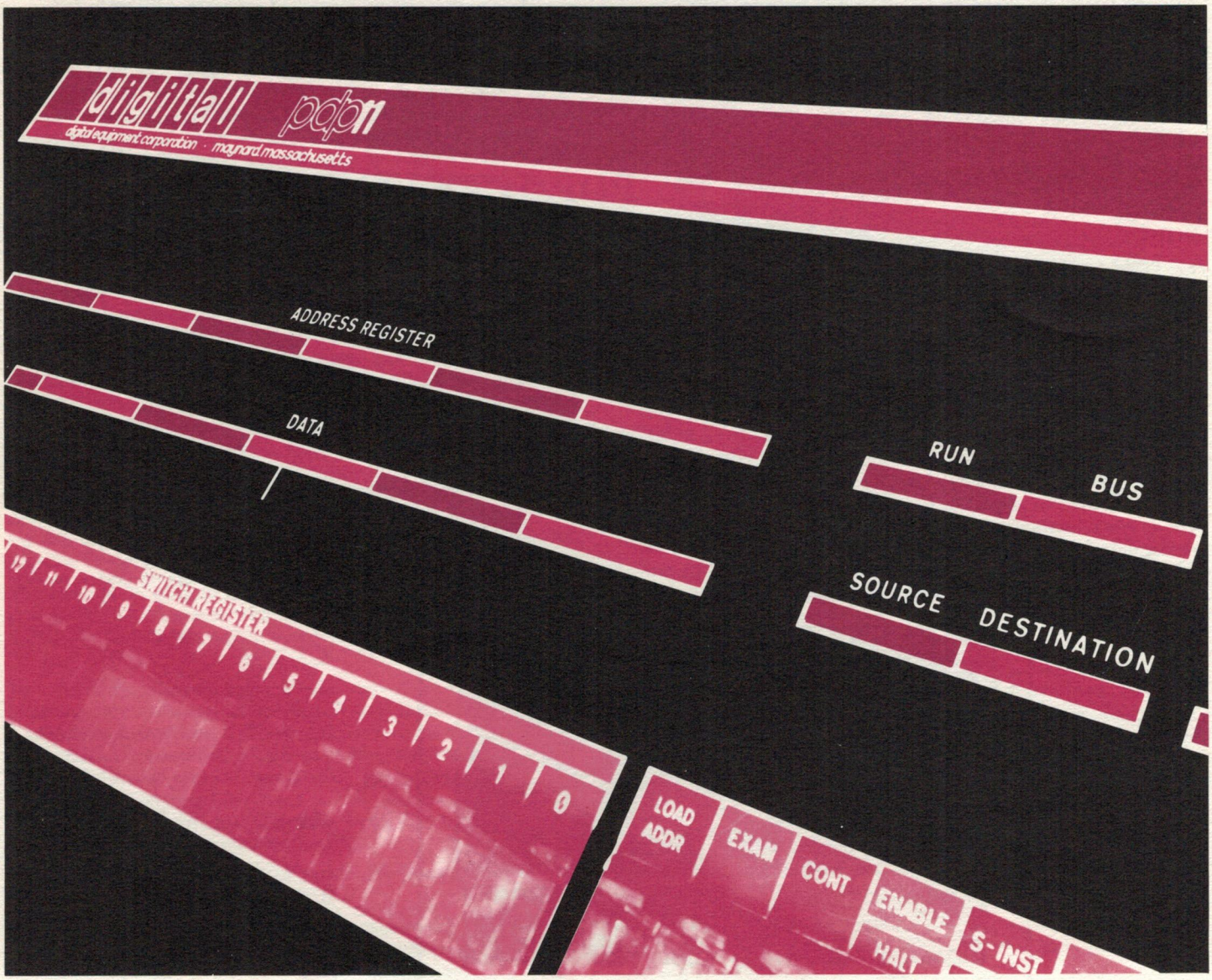
digital equipment corporation

pdp11



The PDP-11 is Digital Equipment Corporation's response to industry demands for a radically new concept in computer design. The first two models in the series incorporate 16-bit processors so that DEC computer users can now choose the most suitable system solution from the widest possible range of computers (12-bit, 16-bit, 18-bit, and 36-bit) and related equipment available today.

The newest DEC system draws on the company's experience with large, medium, and small scale computers—with more than 7,000 installations of DEC computers worldwide!! Expertise gained in systems such as the PDP-8, PDP-9, PDP-10, PDP-12, PDP-14, and PDP-15 computer lines was applied to the design of a new "minicomputer" architecture with its vastly improved processor logic and register configuration.

In refining the architecture for the PDP-11's advanced design, DEC provided for such typical demands imposed on the central processor as:

* Addressing capability, which has been markedly improved
* Multiple general registers; accumulators, index registers, and pointers
* Hardware stack facilities
* Priority structures and rapid context switching in priority interrupt situations
* Byte string handling
* Read-Only memory facilities
* I/O Processing

Using the latest developments in integrated circuit technology and packaging to dissolve many of the logic design constraints previously imposed by circuit costs, the new PDP-11 has been given considerably more freedom and latitude in the structure of its central processor. The computer architecture will thus be able to lower overall programming costs as well as maintain the low hardware cost expected of "minicomputers."

In addition to this unique architecture, the PDP-11 combines speed, a powerful order code, and many real-time hardware features into a compact, modular, low-cost computer which offers the user unique flexibility in program applications. It is a total system concept which incorporates features found in DEC's highly successful large computer system, the PDP-10.

Much of the power of the PDP-11 is derived from its wide range of addressing capabilities. Addressing modes include list sequential addressing, full address indexing, full 16-bit word addressing, 8-bit byte addressing, stack addressing, and direct addressing to 32K words. Variable length instruction formatting allows a minimum number of bits to be used for each addressing mode – resulting in the efficient use of program storage space!

The Unibus™, a unique feature of the system, provides the framework for a family of computers which is easily maintainable and expandable. The PDP-11 has adapted this modular approach to allow custom configuring of systems, easy expansion, and easy servicing. Systems are built from basic building blocks called System Units, which are completely independent subsystems, connected only the the pluggable Unibus and necessary power connections. Additional units can be mounted easily in many combinations within the PDP-11 hardware and connected to the system in the field.

As with previous DEC systems, the PDP-11 comes with a complete package of user-oriented software. This includes:

* Absolute assembler providing object and source listings
* String-oriented editor
* Debugging routines capable of operating in a priority interrupt environment
* Input/Output handlers for standard peripherals
* Relocatable integer and floating point math library

SUMMARY OF PDP-11 FEATURES

UNIBUS

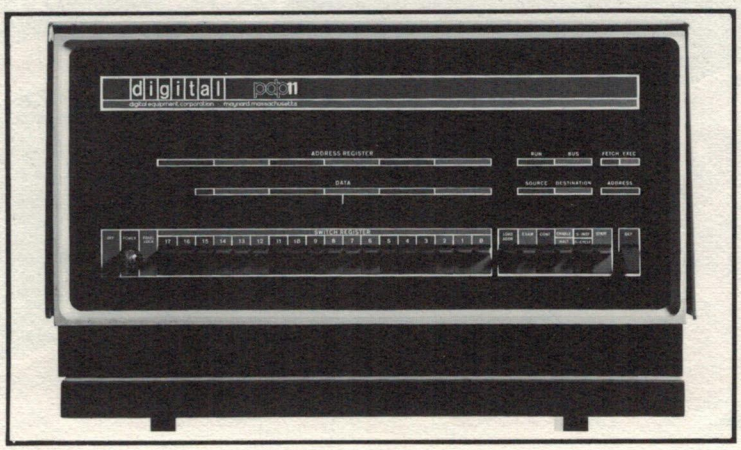
The PDP-11 relies on a highly efficient, single, high-speed Unibus™ for data transfer between the central processor, memory and other devices such as Teletype, disk, line printer, DECtape or analog-to-digital converter.

With the Unibus concept, devices are modular subsystems physically and electrically attached to the Unibus in parallel. In this configuration, instructions may operate directly upon information in device registers, and data transfers from input to output devices can bypass the processor completely. Because of device-memory identity on the Unibus, I/O instructions are not required. I/O is accomplished by word or byte moving instructions in a manner exactly analogous to moving data from one core cell to another. A new dimension is added to I/O operation by allowing *all* instructions to be used with I/O activity (Compare, Bit Set, Bit Test, Add, etc.).

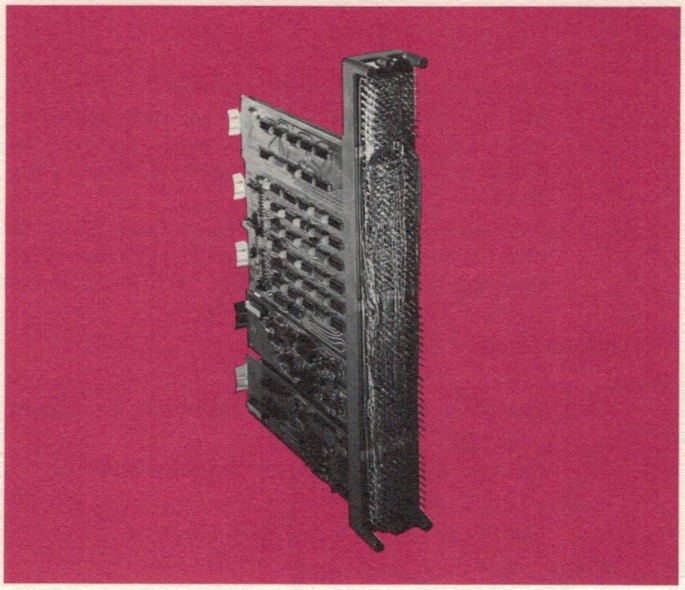
MODULAR CONSTRUCTION OF THE PDP-11

Physically, each Unibus functional subsystem is composed of printed circuit modules plugged into connector blocks on frames called System Units. System Unit subassemblies, such as 4K of core, easily fit side by side into a compact mounting box. A mounting box can contain a power supply, CP, 12K core and two small peripheral controllers. The Unibus, a single cable carrying 56 signals, plugs from one System Unit to another as does the power from the power supply. There is no fixed wiring between System Units. Unibus construction allows:

* True physical and electrical modularity
* Extreme flexibility in original system configuration and field expansion
* Ease of repair and minimum down time
* Low-cost construction without sacrificing device modularity



The PDP-11 is a 16-bit computer with a universal bus called a Unibus allowing networks of memories and peripherals to be used in virtually any combination.



All PDP-11 processors, memories and peripherals are electrically and mechanically modular subsystems supported in System Units which are simply plugged together to form a computer tailored to user needs.

THE KA11 CENTRAL PROCESSOR

The KA11 central processor, connected to the Unibus as a subsystem, controls Unibus allocation between devices and performs arithmetic operations and instruction decoding. It contains eight high-speed general-purpose registers which are used as arithmetic accumulators, index registers, autoincrement and autodecrement registers. The instruction complement of the PDP-11 utilizes the flexibility provided by these general-purpose registers to provide over 400 powerful hard-wired instructions. These instructions, recognizing that most data in a program is structured in some way, exist in a table, in a stack, a table of addresses or perhaps a small set of frequently used variables local to a limited region of program. The PDP-11 handles these common data structures with addressing modes specifically designed for each kind of access. In addition, addressing for unstructured data is general enough to permit direct random access to all of core as well as the writing of relocatable code. The PDP-11 addressing modes include direct register addressing, sequential addressing, full address indexing, and two levels of deferred addressing. The resultant code is highly bit-efficient and each instruction is capable of accomplishing significantly more operations than is possible in any other computer of this size and cost.

The basic order code of the PDP-11 utilizes both single address and double address instructions applicable to either words or bytes. The order code features such instructions as:

MOV A, B

This instruction incorporates, in one statement, the operation of moving the contents of location A to location B. Locations A and B each may be a high-speed register or memory location or a device register on the Unibus. Addresses A and B may be full 16-bit addresses allowing the programmer complete freedom of movement within the full address range of the machine which is 32K words or 65K bytes. Memory, although it is 16 bits parallel, is byte addressable.

Another example of the PDP-11's code efficiency is:

ADD A, B

Any two addressable locations may be added together and the result placed in one of the argument locations using the above command without "Load" and "Store" instructions.

HARDWARE INTERRUPTS

The central processor recognizes four levels of hardware interrupt. Within each major level there are sublevels. Many devices may thus be attached on each level with the device closest to the central processor given priority over the other devices on the same level. The hardware interrupt priority levels are interleaved by programmable central processor priority levels, thus allowing the running program to select the priority of allowable interrupts. Additional speed and power are added to the interrupt structure through the use of the PDP-11 fully vectored interrupt scheme. With the vectored interrupts, the device identifies itself and a unique interrupt service routine is automatically selected by the central processor without device polling. The device's interrupt priority and the service routine priority are independent. This allows dynamic adjustment of system behavior in response to real-time conditions.

The plug-in console board with modular construction is supplied in the basic 11/20 configuration. In addition to aiding programming, console contributes to ease of maintenance on the PDP-11.

STACKS

The PDP-11 central processor has special last-in, first-out "Stack" handling capability. Words may be "pushed" onto a stack or "popped" off a stack with simple instructions.

DIRECT MEMORY ACCESS

Any number of DMA devices may be attached to the Unibus with the priority level among them determined by their placement along the bus. No expensive multiplexers are required. Maximum priority over all is given to DMA devices allowing memory data storage or retrieval at memory cycle speed. Latency is minimized by the organization and logic of the Unibus which allows direct memory access during the execution of instructions.

POWER FAIL AND RESTART

Power fail and restart are standard features of the PDP-11. With these functions, the system senses power failing and traps the processor to a location at which the user has placed a vector to a power fail routine.

SPECIFICATIONS

PHYSICAL

Table Top Model:

Dimensions: 11 inches high, 20 inches wide, 24 inches deep

Weight: 100 lbs. (approximate)

Rack-Mounted Model:

Dimensions: 10½ inches high, 19 inches wide, 23 inches deep with tilt and lock chassis slides for standard 19" rack

Weight: 90 lbs. (approximate)

DEC cabinet: (available with or without programmer's table)

Dimensions: 71½ inches high, 22 inches wide, 39 inches deep including stabilizer feet

Weight: 150 lbs. (approximate)

Table size: 20 inches deep, 19 inches wide, 27 inches above floor

ELECTRICAL

Processor power requirements:

115 volts ±10%, single phase, 47-63 Hz, 7 amperes (230 volt available)

Unibus Logic levels:

Ground and +3 volts

Internal circuit potentials:

+5 volts, -15 volts

FUNCTIONAL

Read/Write Memory:

Cycle time:	1.2 microseconds
Access time:	500 nanoseconds
Word length:	16 bits
Core memory size:	4,096 words, expandable to 28,672

Read Only Memory Available:

Access time:	500 nanoseconds
Word length:	16 bits

Increments of 1,024 words available

256 words of Read/Write 2.0 microsecond cycle time, 1.0 microsecond access time core may be added with each 1,024 words of Read Only Memory

(Increments of 1,024-word Read Only Memory, with or without 256 words of Read/Write Memory, are interchangeable with 4,096-word increments of Read/Write Memory)

Direct Memory Access:

Rate: 83,000 words/second

Maximum latency: 3.5 microseconds for highest priority device

Multiple device capability without multiplexer

Unibus Data Rate:

1,300,000 words/second

Automatic Priority Interrupts:

Four main hardware levels with any number of sublevels

Response time: 7.2 microseconds including storage of the current program counter and status word and establishment of the new program counter

Restore time: 4.5 microseconds including restoring of program counter and status word

Power Fail and Restart:

Included in standard product

General Registers:

Eight high-speed flip-flop registers within central processor. Used as accumulators, 16-bit index registers and autoincrement or autodecrement registers. All registers may serve as stack pointers. Register 6 is used as the processor stack pointer. Register 7 is the program counter.

Instructions:

Over 400 hard-wired instructions through use of general register address modes

Two levels of deferral

Machine directly byte and word addressable to 65,576 bytes or 32,768 words

Environmental: (Processor)

Temperature: 10^{o} - 50^{o} C

Humidity: 20 - 95%

* * CONFIGURATIONS * *

Two main configurations of systems are offered:

PDP-11/20 COMPLETE SYSTEM . . $10,800

KA11 – Central Processor

MM11-E – 4K words, 1.2 microseconds, Read/Write memory

Mounting Box, rack-mountable w/tilt slides. (Also available in tabletop version.)

Power Supply (fits in Mounting Box)

KY11-A – Console (Full operator console)

ASR-33 – Teletype

PDP-11/10 DEDICATED CONTROLLER $7,700

KA11 – Central Processor

MR11-A – 1K words, 500 microsecond access time, Read-Only memory

MW11-A – 256 words, 2.0 microseconds, Read/Write memory

Mounting Box, rack-mountable w/tilt slides. (Also available in tabletop version.)

Power Supply (fits in Mounting Box)

KY11-B – Turn Key Console

Both systems include:

* Power Fail and Restart
* Full priority interrupt structure and multidevice DMA
* Both may use MR11-A Read Only and MM11-E Read/Write Memory