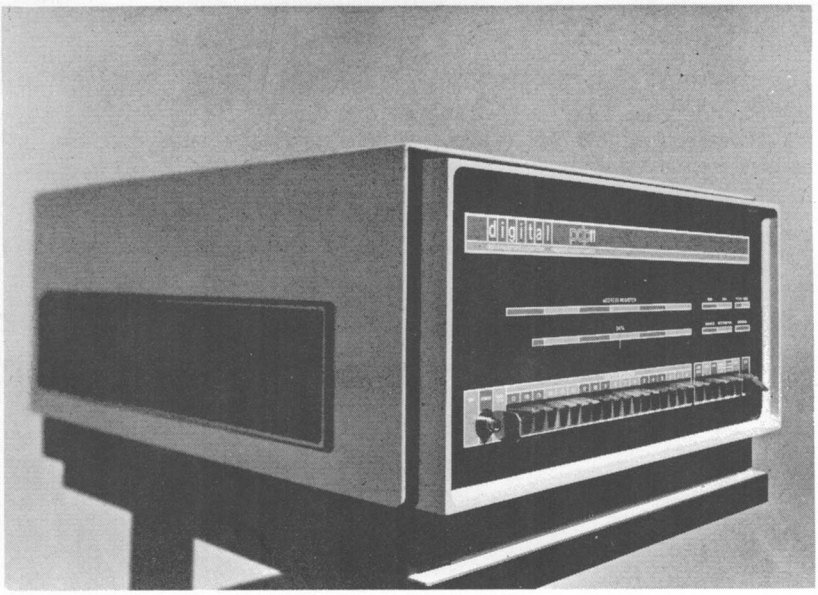


the pdp-8's big brother

The box above may one day be the most common of minicomputers. It is a 16-bit big brother to the Digital Equip. Corp. PDP-8 12-bit computer, a device which undoubtedly now holds the world's record for "number installed" with a figure above 6200 units. The vendor is estimated to have 70%-80% of the minicomputer market, and that fact alone would sell the new machine.

The device now offered has an I/O architecture centered around a single bus called, appropriately, the Unibus. The central processor, the memory, and all peripherals attach to the 56 bi-directional lines of the bus to send address, data, and control information.

DEC worked on the idea of producing a 16-bit machine for over two years, and determined long ago that the machine would have to be more than another fast box. Using the bus, system modules and peripherals can communicate with each other without the intervention of the central processor, at an aggregate data rate of 1.3 million words/sec.

The cpu has a 70 nsec clock time, and performs some instructions in 1.2 usec (an add takes 2.3 usec). It does two's-complement airthmetic and uses an instruction repertoire of 60-70 functional types implemented in 400 hardwired specifics, including double-operand instructions. There are six 16-bit general purpose registers which may be used as index registers, accumulators or stack pointers, another which is reserved as a program counter and one used as a processor stack pointer.

The memory can be addressed as up to 32K 16-bit words or as 64K bytes, and byte addressing does not imply using right and left word halves. Read/write core is provided in 4K increments, has a cycle time of 1.2 usec and an access time of 500 nsec. Read-only memory (modified U-core with a wire braid) is available in 1K word segments and has a 1.0 usec cycle time. Read/-write memory is also available in 128 word segments with a 2.0 usec cycle. The vendor claims, however, that because of the large number of hardwired instructions, the double-operanding, and the I/O and interrupt schemes, the system will run 50%-100% faster than other mini's using the same speed memory.

The 11 recognizes four primary levels of interrupt, but each peripheral is assigned its own interrupt level within that scheme, and interrupts can be infinitely nested.

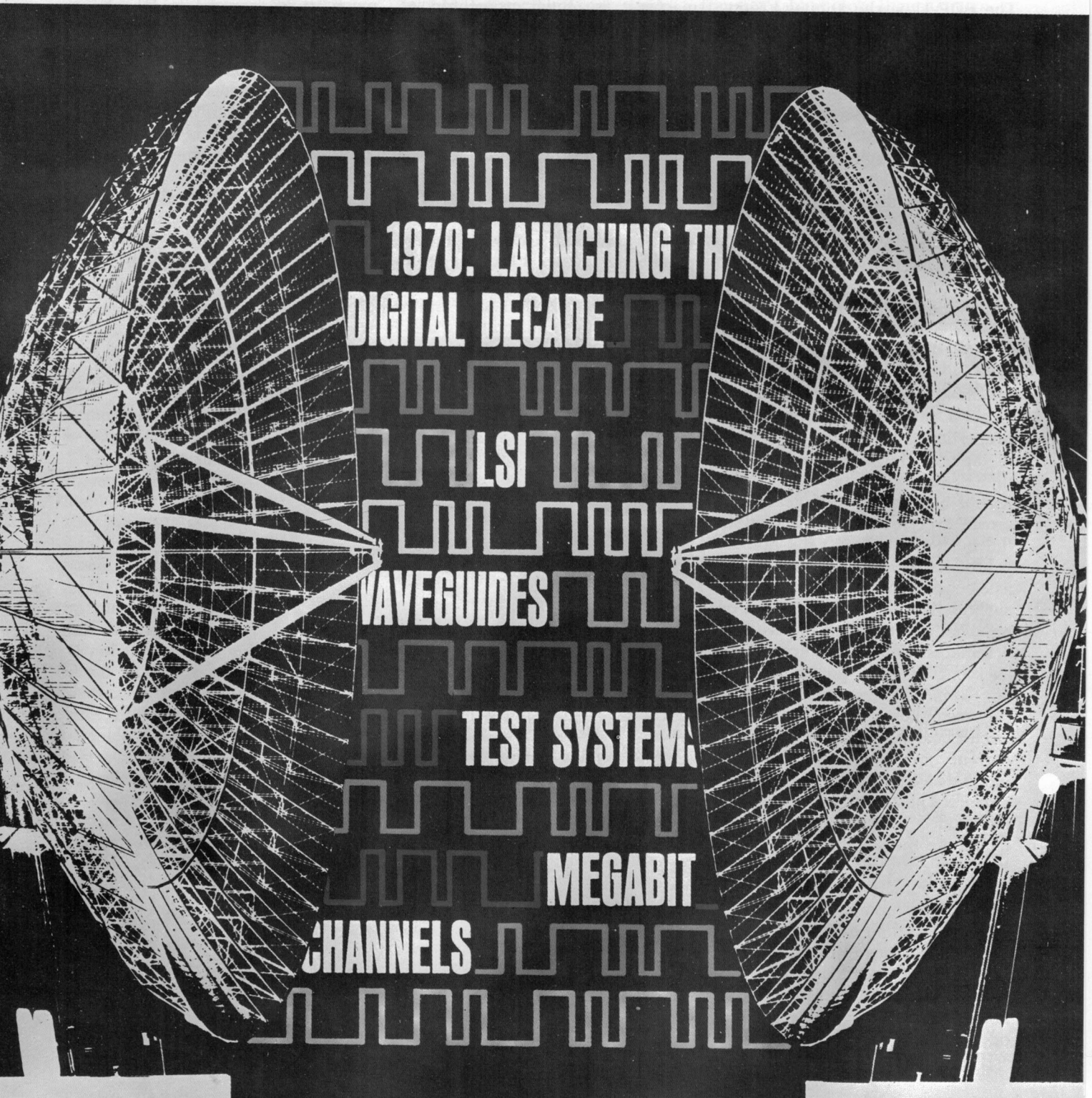
The computer is available in two basic configurations. The PDP-11/10 comes with 1K of read-only memory, 128 words of the slower read/write core, a turnkey console and a direct memory access channel for $7700. Apparently this will be the process control configuration. The PDP-11/20 has the same processor, a 4K core, an operator's console, and a Teletype and sells for $10,800. First deliveries are scheduled for early summer.

Software will at first be minimal, with an assembler, an I/O editor, online debug facilities, and utilities; but editors, compilers, interpreters, and monitors are all promised. DIGITAL EQUIP. CORP., Maynard, Mass. For information:

Reprinted from DATAMATION JANUARY 1970

January 5, 1970

Electronics®



PDP-11 rides on a unibus

Modular 16-bit computer has subsystems strung in parallel on a single data-transfer trunk; this architecture seen as central design theme for family of DEC machines planned for 1970's

The PDP-11 is the Digital Equipment Corp.'s answer to the growing demand for 16-bit midi-computers. It also may be a hint of things to come from DEC in the 1970's.

The new machine is a modular computer with its parts strung in parallel on a single bus. With this sort of wide-open architecture, system parts as diverse as the arithmetic unit and teleprinter console are attached to the bus through buffers. Except for core memory, every part of the PDP-11 can directly address any other, using a scheme based on real and imaginary core locations. From the point of view of the central processor, for example, the teletypewriter is a location in memory with special properties, and the same is true of tape, drum, or disk stores, and digital/analog interfacing electronics for other peripheral gear. In a sense, everything is peripheral to the bus, which DEC calls unibus.

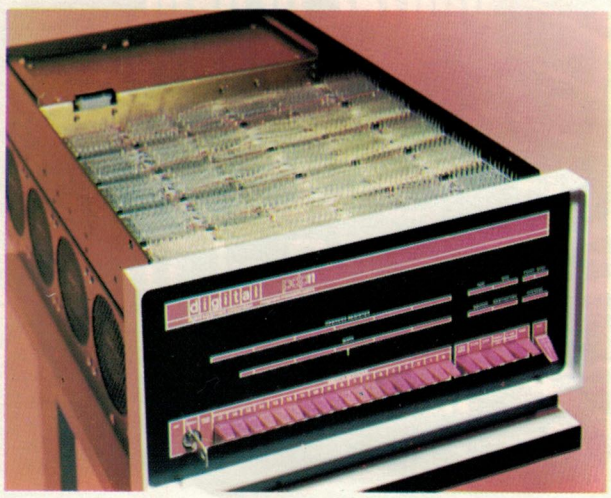
Modularity is physical as well as electronic. Major subassemblies, such as the arithmetic unit, can be removed and replaced in less than 3 minutes, and the computer put back on line when power and unibus connections are made. Minor subassemblies are on individual circuit boards—small ones for high-current circuitry, larger ones for integrated circuits and low-current circuits. Thus the machine is easily maintained as the parts most apt to fail are the smallest and easiest to remove.

Such modularity means the machine can be updated almost infinitely. According to a DEC spokesman, "DEC plans to use the modularity of the machine to take advantage of the most advanced technology as quickly as this technology becomes practical."

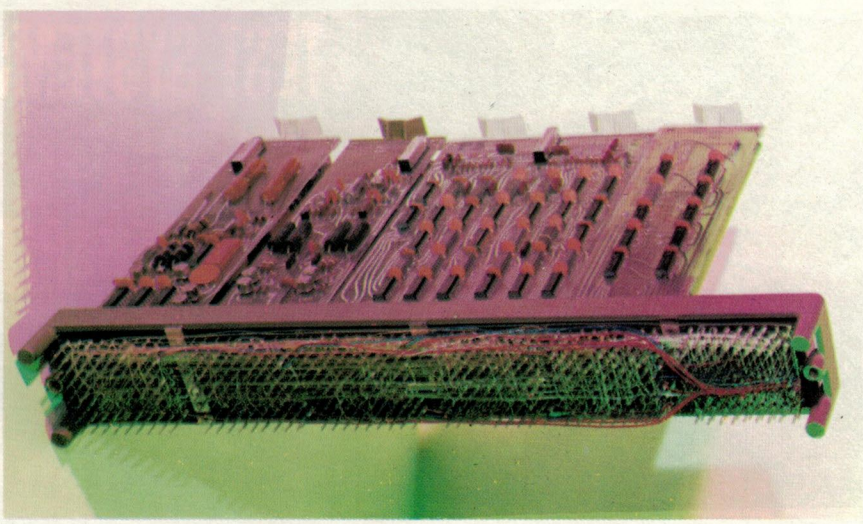
The fact that the unibus-based machine is fully asynchronous helps. Because there need be no common clocks rate throughout the PDP-11 system, faster memories or processors can be added whenever necessary without upsetting operation. Also, slower subassemblies can replace faster ones to achieve a favorable cost tradeoff.

The Flexprint bus used in the PDP-11 could already carry 18-bit words, and there's little to prevent paralleling these Flexprint conductors to create machines of almost arbitrary word length. Nor is there any rule against applying this architecture to 8- or 12-bit machines. For the next few years DEC can be expected to introduce products with a family resemblance to the PDP-11's unibus form.

While the unified busing concept isn't new, only the PDP-11 seems to be using it specifically in the general-purpose commercial computer market. Variations of the concept are used for the Apollo guidance and navigation computer built



Expandable. The PDP-11, shown with top removed is modular in both physical and electronic design. Major subsystems such as the core memory, below, are easily removed and replaced.



for the National Aeronautics and Space Administration by Raytheon Co. [*Electronics*, Jan. 9, 1967, p. 112], and the six-month-old GRI-909 aimed at the systems control market by its builder, GR Industries Inc. [*Electronics*, July 7, 1969, p. 14].

By contrast, the PDP-11 has a powerful central processor and arithmetic unit (the GRI-909 has no arithmetic unit in its standard model). The PDP-11's processor has the almost unheard-of total of eight general-purpose flip-flop registers, any one of which can be an accumulator, stack pointer, auto index register, or true 16-bit address register. In addition, the processor has two temporary storage registers.

Put to work. Not only does it have about twice the typical number of general-purpose registers of other 16-bit machines, but it appears to make better use of them, by allowing almost any system component on the unibus to have direct-memory access. Under the constraints of more common architectures, memory access is via the central processor, with data stopping over in the CPU's registers on the way into, or out of, memory. The PDP-11's almost unlimited memory access thus allows the CPU to operate with fewer interrupts.

The interrupts that do occur are adjustable through software; priorities can be controlled by the running program, and some interrupts disallowed. Some other situations which normally would cause interrupts don't arise. This is because instructions can operate directly on data in the registers at input and output devices—data can be transferred from one buffer register to another on the bus, bypassing the central processor (and its registers) completely. And since each subassembly attached to the bus is addressed in the same code used to spot core locations, no special I/O instructions are needed.

There are only slightly more than 60 software instructions in the PDP-11's instruction set, but DEC spokesmen like Andrew C. Knowles, product-line manager for the PDP-11, believe that the flexibility provided by the machine's general-purpose registers makes these 60 instructions equivalent to more than 400 hardwired instructions.

The rationale behind this is DEC's statement that most data in a program are structured in tables, lists, tables of addresses, etc. Addressing modes have been engineered into the PDP-11 to deal with these common data structures. Thus the PDP-11 addressing modes include direct register addressing, sequential addressing, full address indexing, and others.

Another case in point is DEC's use of double operand instructions in the PDP-11, something which may be unique to a computer system this small.

In addition to the usual single-address instructions, the PDP-11 includes a repertoire of seven double-address instructions. Such double operand instructions can be very flexible; MOV (move) for example, can at various times replace any one or a combination of the following individual instructions: load, store, load from table, store in table, push down, pull up, load index register, and output to peripheral.

Thus, for at least part of its repertoire, the PDP-11's instruction set is a machine language as simple as many higher-level languages.

Catching the bus. With a large number of devices sharing a common data-transfer bus, how does the PDP-11 keep order? The umpire is a control and priority arbitrator included in—but electronically distinct from—the central processor unit. There's no polling of the system; a unit requests use of the unibus whenever it needs it.

When the request is made, the controller checks the central processor's status register, and if the processor is between bus cycles of an instruction execution, the requester at least has a chance of getting at the bus.

Nonprocessor requests—those from a disk memory, say—always have first crack at the bus. However, the software in use and the contents of the processor-status register interleave eight levels of processor priority between those of devices on various bus request lines. So the processor has the second-highest priority (and the lowest) plus six levels between the other priority levels of PDP-11 devices, such as peripheral equipment.

In response to a bus request, the controller sends out a "bus grant" pulse, and the device that made the request prevents the grant signal from passing down the line to devices more distant from the controller. Thus, devices hardwired closer to the processor automatically have higher priorities than those further away.

Once a device has the bus, it holds it until its job is done, and meanwhile sends out a "bus busy" signal.

After a nonprocessor request is made, it takes a maximum 3.5 microseconds to catch the bus. And after the device has control, it can transfer data at more than 20 megabits per second if it has the capability.

Big fleas, small fleas. Some devices using the bus will require the aid of the processor in what are called device servicing programs. When such a bus request is made, the task under way in the processor is interrupted and the return address for the interrupted routine and the processor status word are held in a pushdown list, a combination of hardware and software also known as a last-in, first-out stack. In the PDP-11, the list is automatically maintained for interrupt processing, making it possible for higher priority interrupts to break into the processing of lower priority interrupt routines.

It takes 7.2 μsec for the processor to get the interrupt command and fetch the first instruction in the new routine (assuming there are no nonprocessor bus requests). When the interrupt routine is done, the last instruction is "return from interrupt," and this returns the processor to the job next downward in priority—at the top of the pushdown list. That is, it restores former processor status and the contents of the registers. The return to a preinterrupt state takes about 4.5 μsec to accomplish.

Even second and third level (and beyond) interrupts can in turn be interrupted by bus requests with high enough priorities. This nesting of priority interrupts, as DEC calls it, can go on until all available core memory is used up holding prior processor conditions.

Judging it. Since the PDP-11 is asynchronous, and has characteristics like multidevice direct-memory access, it's hard to compare it with other machines. Even standby

specifications like cycle time don't mean much in the Unibus format. DEC claims, however, that in benchmark tests against other machines, the PDP-11 is faster on the average. "Some competing machines do some operations faster," says a spokesman, "but when all task times are added and averaged out, we come out ahead."

For engineers who want numbers, the PDP-11's standard 4K memory module (the MM11-E) cycles in 1.2 μsec and has a 500-nanosecond access time. The MR 11-A read-only memory module also has a 500-nsec access time, and with it comes the MW11-A, a 128-word, 2-μsec-cycling read-write memory.

Direct-memory access can occur at the full speed possible with the main core memory since the Unibus scheme makes multiplexing unnecessary; the rate is 833,000 words per second. Maximum latency time is 3.5 μsec for highest-priority bus users.

The amount of time saved by direct-memory access, and by direct data transfer between parts of the PDP-11 system without involving the general registers, is not specified, and probably varies with the individual system and application. But it exists, and may be the factor that allows the PDP-11 to come out ahead in DEC's benchmark tests.

The PDP-11 initially is going to be available in two models; the PDP-11/20, which uses the 4K core memory and comes equipped with an ASR-33 teletypewriter, at $10,800, and the PDP-11/10 "dedicated controller," equipped with read-only memory and a small amount of read-write core. The 11/10 substitutes a turnkey console for the full operator's console of the 11/20. Its $7,700 price doesn't include a teletypewriter.

Knowles says both machines already are back-ordered. Initial deliveries of 11/20's to customers already on the books should be in the second quarter of 1970 with mass deliveries early in the third quarter. The PDP-11/10 should be ready for deliveries late in 1970.

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