DEC-11-HADB-D

AD01-D analog-to-digital conversion subsystem manual

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CHAPTER 1
GENERAL INFORMATION

1.1 INTRODUCTION

The AD01-D Analog-to-Digital Conversion Subsystem is a peripheral device used with the PDP-11 Computer Systems in data acquisition and control applications. Refer to the *PDP-11 Unibus Interface Manual* for information relevant to the architecture of the computer and peripheral devices.

1.2 PURPOSE

The AD01-D operates under computer or external clock control as a highly flexible analog input device to digitize analog inputs connected to directly addressable, multiplex switch modules. As many as eight multiplex switch modules can be implemented. Each module can service four individual analog inputs.

The basic AD01-D provides 10-bit digitization of unipolar, high-level analog signals with a nominal full-scale range of 0V to +1.25V, +2.5V, +5.0V or +10V. These four ranges are program-selectable and are achieved by a selectable gain amplifier. Options are available for digitization of bipolar analog signals and for sample and hold applications.

1.3 FUNCTIONAL DESCRIPTION

The AD01-D comprises

a. An expandable solid-state input multiplexer

b. A programmable input range selector

c. A high-speed A/D converter

d. The computer interface logic.

The interface logic includes two registers to store control and status information and data. The AD01-D is accessed and controlled by a control and status word with a Move (MOV) instruction. A single control and status word from the computer selects the input range and multiplexer channel and starts the conversion. Other novel features of the interface logic are the ability to place the AD01-D in an interrupting or noninterrupting mode and to select an external clock. In the interrupting mode, the AD01-D can issue an interrupt when conversion is done or when an error condition is produced by starting a new conversion before the previous conversion is complete. The noninterrupting mode enables the converter to approach its maximum throughput rate under program control. After the conversion is complete, the data is easily transferred from the AD01-D to the computer by programming another MOV instruction.

1.4 PHYSICAL DESCRIPTION

The AD01-D Analog-to-Digital Converter Subsystem can be configured and modified according to application needs. All logic, options, and a Type H727 A/B Analog Power Supply are housed in a single, 5-1/4 in., rack-mountable assembly. Insertion slots for the multiplex switch modules, bipolar option, and sample and hold option are prewired to simplify field installation and modification. Only simple jumper wire changes are required. The module complement and optional modules for the AD01-D are listed in Table 1-1; the location of each module is shown in Figure 1-1. Logic power for the AD01-D is supplied by a separate H716 Logic Power Supply, which can be rack mounted. Operation with an input voltage of 115V requires an H727-A power supply and the system is designated AD01-DA; an input voltage of 230V requires an H727-B and the system is designated AD01-DB. If rack mounting of the subsystem is desired, DEC offers a 19-in. industrial Type H950 Cabinet with a blower fan and front and rear doors.

Table 1-1
AD01-D Module Complement

Type/Part No.	Name	Quantity	Location
A124	Four Input Multiplex Switch	1	B16
A124*	Four Input Multiplex Switch	8 (max)	A17-A20 B17-B20
A220	Selectable Gain Buffer Amplifier	1	A16
A862 (AH05)*	Bipolar A/D Converter	1	AB13 (AB12)
A405 (AH04)*	Sample and Hold	1	AB15
A708	Dual Voltage Regulator	1	A24
A812	10-Bit A/D Converter	1	AB12
G736	Request Jumper	1	A10
M105	Address Selector	1	A3
M111	Inverter	1	A9
M112	NOR Gate	1	B7
M113	10 2-Input NAND Gates	1	A7
M161	Binary to Octal/Decimal Decoder	1	B10
M206	Six Flip-Flops	2	AB6
M302	Dual Delay Multivibrator	3	AB11, B8
M501	Schmitt Trigger	1	AB22
M617	6 4-Input NOR Buffers	1	B9
M782	Interrupt Control	1	B3
M783	Unibus ™ Drivers	2	AB5
M784	Unibus Receivers	1	A4
M785	Unibus Transceivers	1	B4
M908	Connector	2	AB21

*Denotes optional modules.

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1.5 SPECIFICATIONS

1.5.1 Environmental

Temperature:	0°C to +55°C, operating -25°C to +85°C, storage
Humidity:	to 90 % without condensation

1.5.2 Power Requirements

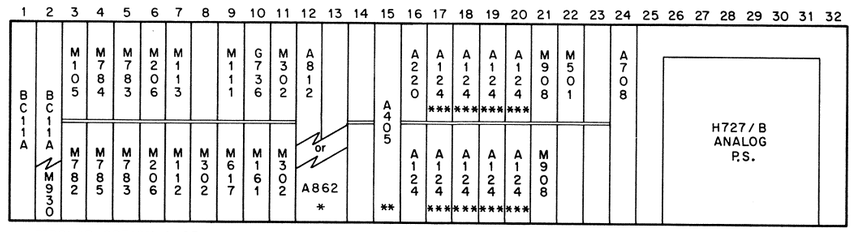
Input voltage (ac):	115V/230V ± 10%
Input frequency (ac):	47 Hz to 63 Hz, single phase
Power dissipation:	<75W

1.5.3 Packaging

Size:	Height: 5-1/4 in. Width: 19 in. Depth: 12 in. (plus separate power supply)
Weight:	15 lb

1.5.4 Performance Parameters

Conversion time:	22 μs, including channel and gain selection with or without sample and hold option. Bipolar option adds 7 μs.
Conversion aperture:	17.5 μs, 24 μs with Bipolar Option AH05, or 0.1 μs with Sample and Hold Option AH04
Sample and Hold	
Acquisition:	5 μs to 0.01% of full-scale step change
Aperture:	100 ns
Number of analog input channels:	4 minimum (expandable to 32 in groups of 4)
Input voltage range (program-selectable)	
Unipolar:	0V to 1.25V, +2.5V, +5.0V or +10.0V, full-scale
Bipolar:	0V to ± 1.25V, ± 2.5V, ± 5.0V or ± 10.0V, full-scale
System accuracy:	± 0.1% of full-scale ± 0.125% of full-scale with Sample and Hold Option AH04



* BIPOLAR OPTION AH05

** SAMPLE AND HOLD AMPL OPTION AH04

*** MULTIPLEX SWITCH MODULES

11-0331

Figure 1-1 AD01-D Configuration

Input impedance:	1000 MΩ in parallel with 20 pF
Input isolation:	Enhancement mode MOS FET switches, off when unselected or power off
Analog input connections:	Plug-in cable modules
Channel selection: (program-selectable)	6-bit address
Overload capability:	±20V on all ranges without damage
Cross-Channel attenuation:	78 dB, dc to 80 Hz for 20V p-p signals, 100-Ω source impedance
Input gain: (program-selectable)	2-bit code

1.6 REFERENCE DOCUMENTS

The following documents are essential to understand the PDP-11 Computer System:

PDP-11 Handbook
PDP-11 Unibus Interface Manual
PDP-11 Maintenance Manuals

The following diagnostic program is required to test the performance of the AD01-D:

AD01-D MainDEC-11-D6AB
A-SP-AD01-D-12 Acceptance Procedure

CHAPTER 2
INSTALLATION AND ADJUSTMENTS

2.1 INSTALLATION PLANNING

The AD01-D is a Type 1943 rack-mountable assembly, which can be installed in the Type H950 Equipment Cabinet. The Type 1943 Assembly has the following dimensions:

Width:	19 in.
Depth:	12 in.
Height:	5-1/4 in.

The associated H716 Logic Power Supply mounts on the rear door of the cabinet.

2.2 ENVIRONMENTAL REQUIREMENTS

The AD01-D and PDP-11 operate in identical environments; the environmental limitations are listed in Chapter 1.

2.3 CONFIGURATIONS

The basic AD01-D Subsystem consists of a 5-1/4 in. rack-mountable logic assembly and a H716 Logic Power Supply. A physical description of the AD01-D and associated options is presented in Chapter 1. The following paragraphs summarize the requirements for installing and configuring the AD01-D.

2.3.1 Channel Expansion

Eight prewired insertion slots are provided in the logic shelf for the multiplex switch modules. The slots are A17 through A20 and B17 through B20 (see Figure 1-1). When expanding the channel capacity, modules must be added in the A level before the B level, progressing from slot 17 toward slot 20.

2.3.2 Bipolar Option AH05

To accommodate A/D conversion of bipolar analog voltages, Bipolar Option AH05 must be installed in the AD01-D logic assembly. The option consists of a replacement Bipolar A/D Converter Module, A862.

The replacement A/D converter occupies two insertion slots while the A812 10-Bit A/D Converter occupies only one. The insertion slot is prewired to accept either A/D converter without wiring changes (see Figure 1-1).

2.3.3 Sample and Hold Amplifier Option AH04

If skewless sampling of analog signals is desired, Sample and Hold Amplifier Option AH04 must be installed in the AD01-D logic assembly. The option consists of a single module designated the A405 Sample and Hold Module. A prewired insertion slot located at AB15 (see Figure 1-1) on the logic assembly is reserved for the module.

2.3.4 Unibus Connections

Only one BC11-A Cable is required to connect the Unibus from the computer to the AD01-D. This cable must be inserted into slot AB01 on the logic assembly. If the AD01-D is the last peripheral device on the Unibus, Terminator Module M930 is inserted in slot AB02; otherwise, this slot is used to connect the Unibus to another peripheral device using another BC11-A Cable.

2.3.5 Multiplexer Channel Connections

The input connections to the multiplexer switch modules are wired to two M908 Connector Modules located in slots AB21 of the logic assembly. The analog signals to be converted should be carried on user-supplied twisted pairs of wires (shielded if necessary). These twisted pairs should be soldered to the appropriate split lugs on the M908 Modules. The assigned channel numbers and the associated pin numbers on the M908 Modules are identified in Table 2-1.

2.3.6 External Clock Connection

As with the multiplexer channel connections, external clock input connections to the timing circuits of the AD01-D are also wired to the M908 Connector Module located in slot A21. If an external clock is to be used in an AD01-D installation, the clock signal should be carried on user-supplied twisted pairs of wires (shielded if necessary). The twisted pair should be soldered to split lugs A1 and B1 or A2 and B1 on the M908 Connector Module in slot A21.

2.4 INSTALLATION PROCEDURE

The installation procedure for the AD01-D Analog Subsystem is as follows:

Step	Procedure
1	Unpack the equipment from the shipping container(s) and inspect the unit(s) for damage. Damage claims should be made to the DEC district supervisor. **NOTE** **DEC Field Service personnel should be available for consultation on potential problems.**
2	Remove the tape that secures the modules and cables in the AD01-D Assembly and varify that the modules and connectors are seated in the proper connector slots (refer to drawing D-MU-AD01-D-02).
3	Mount the AD01-D Assembly in the assigned location (H950 Equipment Cabinet), using the appropriate hardware.

(continued on page 2-2)

Table 2-1
Channel, Module, and Pin Number Cross-Reference List

Channel No.	A124 Multiplex Switch Module Slot	M908 Connector Module		
		Slot	Hot Pin	Gnd Pin
0	A17	A21	B2	C2
1			C1	D1
2			D2	E2
3			E1	F1
4	A18		F2	H2
5			H1	J1
6			J2	K2
7			K1	L1
8	A19		L2	M2
9			M1	N1
10			N2	P2
11			P1	R1
12	A20		R2	S2
13			S1	T1
14			T2	U2
15			U1	V1
16	B17	B21	B2	C2
17			C1	D1
18			D2	E2
19			E1	F1
20	B18		F2	H2
21			H1	J1
22			J2	K2
23			K1	L1
24	B19		L2	M2
25			M1	N1
26			N2	P2
27			P1	R1
28	B20		R2	S2
29			S1	T1
30			T2	U2
31			U1	V1
EXT IN EXT IN A		A21	A1 A2	B1 B1

Step	Procedure
4	Install the logic power supply and chassis subassembly in the assigned location (refer to drawing D-UA-H716-B-0 for AD01-DA or drawing D-UA-H716-D-0 for AD01-DB).
5	Connect the H716 Logic Power Supply Cable from the power supply to the left end panel of the AD01-D Subsystem where noted.
6	Determine where Unibus is terminated and connect BC11-A Cable to last device. If the AD01-D is the last device on the bus, install the Terminator Modules M930 in slot AB02 of the AD01-D.
7	Perform the acceptance checkout of the AD01-D logic and analog circuits using the MainDEC-11-D6AB Diagnostic Program and A-SP-AD01-D-12 Acceptance Procedure. Adjustment should not be necessary because all potentiometers are sealed at the factory after adjustment.
8	If, at any time, the AD01-D is not within its stated specifications (accuracy), perform the adjustment procedure in Paragraph 2.6. When this adjustment is complete, perform the acceptance tests again.

2.5 OPTION INSTALLATION

The AD01-D options necessitate some changes in the back panel wiring. All information regarding the wiring for each option configuration is given in Figure 2-1. Add and/or delete wires according to this diagram when installing options.

2.6 ADJUSTMENT PROCEDURE

The adjustment procedure for the AD01-D depends on the particular option configuration. If a given option is not included in the AD01-D, disregard the corresponding adjustment procedure. To achieve accurate calibrations, perform the adjustments in the following sequence.

1. Power Supplies
2. Timing
3. A/D Converter (A812 or A862)
4. Sample and Hold A405
5. Switched-Gain Amplifier A220
6. Multiplexer Setup
7. External Sync

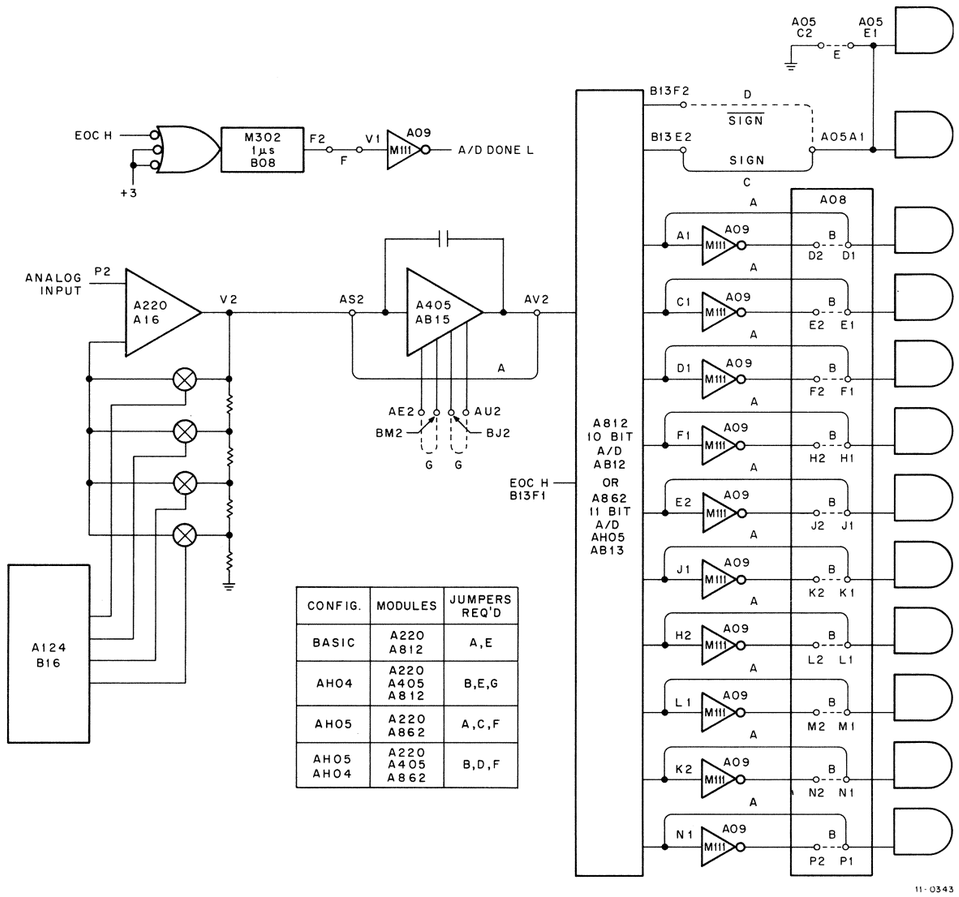
2.6.1 Power Supply Adjustments

Table 2-2 summarizes the necessary information for adjusting the power supplies in the AD01-D.

Table 2-2
Power Supply Adjustments

Supply	Voltage*	Pin	Adjustment Location
H716	+5V ± 0.25V	A03A2 A03C2 (GND)	
H727	+15V ± 0.1V	A24V2	POWER MATE – Top Right (Blue Case)
		A24T2 (GND)	DELTRON – Bottom Right (Black Case)
	-20V ± 0.1V	A24N2	POWER MATE – Top Left (Blue Case)
		A24T2 (GND)	DELTRON – Bottom Left (Black Case)

*Voltage measurement can be made with EDC null meter and DEC 10:1 Divider (refer to Table 5-1).



CONFIG.	MODULES	JUMPERS REQ'D
BASIC	A220 A812	A,E
AH04	A220 A405 A812	B,E,G
AH05	A220 A862	A,C,F
AH05 AH04	A220 A405 A862	B,D,F

Jumper	From	To
A	A09A1 A09C1 A09D1 A09F1 A09E2 A09J1 A09H2 A09L1 A09K2 A09N1 A15S2	A08D1 A08E1 A08F1 A08H1 A08J1 A08K1 A08L1 A08M1 A08N1 A08P1 A15V2
B	A08D2 A08E2 A08F2 A08H2 A08J2 A08K2 A08L2 A08M2 A08N2 A08P2	A08D1 A08E1 A08F1 A08H1 A08J1 A08K1 A08L1 A08M1 A08N1 A08P1
C	B13E2	A05A1
D	B13F2	A05A1
E	A05C2	A05E1
F	B08F2	A09V1
G	A15E2 B15J2	B15M2 A15U2

Figure 2-1 Option Configuration Diagram

Table 2-2 (Cont)
Power Supply Adjustments

Supply	Voltage*	Pin	Adjustment Location
A708	-15V ± 0.1V	A24S2 A24T2 (GND)	No Adjustment
*Voltage measurement can be made with EDC null meter and DEC 10:1 Divider (refer to Table 5-1).			

2.6.2 **Timing Adjustment**

The timing of the AD01-D can be adjusted while running the WAS-IS TEST (SA 270_8) of the diagnostics with inhibit printout option. The required timing adjustments are summarized in Table 2-3.

2.6.3 **A/D Converter**

2.6.3.1 **A812** – The following adjustment should be performed while running the Display Conversion Loop (SA 220_8) of the diagnostic program.

Table 2-3
Timing Adjustments

Module	Slot	Pin	Time
M302	A11	F2	5 μs
M302	A11	T2	0.5 μs
M302	B11	F2	0.5 μs
M302	B11	T2	0.1 μs
M302	B08	F2	1 μs/AH05 only
M302*	B08	T2	2.5 μs 0.1 μs with AH05

*External sync signal is required to set this single-shot, because it derives output signal from Ext Sync input.

NOTE

The procedure should be performed with the A220 and A405 Modules removed from their insertion slots.

Step	Procedure
1	Extend A812 Module using two W982 Extender Modules.
2	Set EDC to 5 mV and connect to B12V2.
3	Adjust comparator sensitivity potentiometer (see Figure 2-2) for 000 000_8 to 000 001_8 on console DATA indicators. (Adjust for 001 777_8 to 001 776_8 if AH04 is installed.)
4	Set EDC to +9.9853V.
5	Adjust reference potentiometer for 001 777_8 to 001 776_8 on console DATA indicators. (Adjust for 000 000_8 to 000 001_8 if AH04 is installed.)

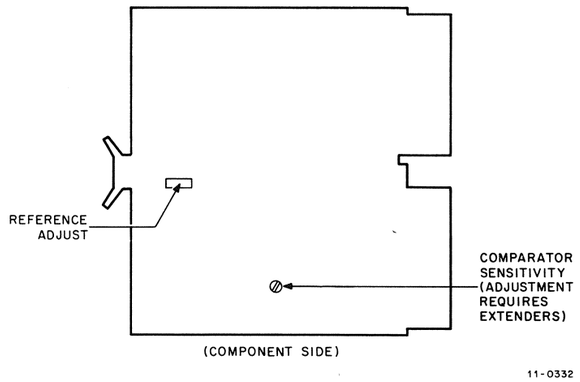


Figure 2-2 A812 A/D Converter

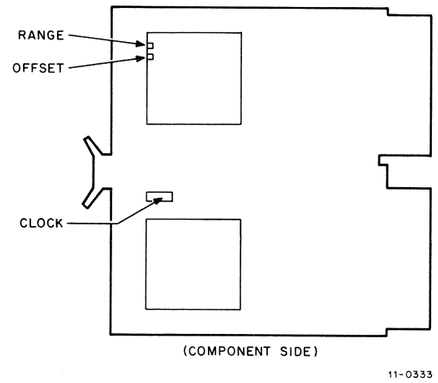


Figure 2-3 A862 A/D Converter

2.6.3.2 **A862 (AH05 Option)** – The following adjustment procedure uses the WAS-IS TEST and the Display Conversion Loop of the diagnostic program. Adjust the A862 A/D Converter as follows:

NOTE

The procedure should be performed with the A220 and A405 Modules removed from their insertion slots.

Step	Procedure
1	Start the WAS-IS TEST (SA 270_8) with inhibit printout bit 13 = 1.
2	Connect scope to B13F1 and adjust clock potentiometer (conversion time) to obtain a 24-μs positive pulse (see Figure 2-3).
3	Stop program and restart at Display Conversion Loop (SA 220_8).
4	Connect EDC to A13J2 and A13F2 (GND). Set EDC to +5 mV ± 2 mV.
5	Adjust offset potentiometer for 000 000_8 to 000 001_8 on console DATA indicators. (Adjust for 001 777_8 to 001 776_8 if AH04 is installed.)

2.6.4 **Sample and Hold A405 (AH04 Option)**

The adjustment procedure of the A405 Module depends on the AD01-D option configuration. Two procedures are outlined below. One procedure applies to systems that have only the AH04 Option (Sample and Hold); the other procedure applies to systems that have both the AH04 and AH05 (Bipolar) Options.

2.6.4.1 **AH04 Option Only** – Adjust the A405 Module as follows:

NOTE

The procedure should be performed with the A220 Module removed from its insertion slot.

Step	Procedure
1	Ensure that all proper jumpers (except those marked G) are installed (see Figure 2-1).
2	Ensure that split lugs A and B on the A405 Module are connected (see Figure 2-4).
3	Start Display Conversion Loop (SA 220_8) of the diagnostic program.
4	Connect EDC to A15S2 and A15F2 (GND). Set EDC to -5 mV.

(continued on Page 2-5)

Step	Procedure
5	Adjust bias potentiometer (see Figure 2-4) on A405 Module for 001 776_8 to 001 777_8 on console DATA indicators.
6	Stop program and turn off computer power.
7	Add jumper wire G to back panel wiring.
8	Turn on computer power and set EDC to 9.9853V.
9	Restart Display Conversion Loop (SA 220_8).
10	Adjust offset coarse potentiometer on A405 for 001 776_8 to 001 777_8 (or as close as possible) on console DATA indicators.
11	Adjust offset fine potentiometer on A405 for 001 776_8 to 001 777_8 on console DATA indicators.

2.6.4.2 **AH04 with AH05 Option Only** – Adjust the A405 Module as follows:

Step	Procedure
1	Ensure that all proper jumpers are installed (see Figure 2-1).
2	Ensure that split lugs A and B on the A405 Module are connected (see Figure 2-4).
3	Connect EDC to A15S2 and A15F2 (GND). Set EDC to +5 mV.
4	Start the Display Conversion Loop (SA 220_8) of the diagnostic program.
5	Adjust bias potentiometer (see Figure 2-4) on A405 Module for 000 001_8 to 000 000_8 on console DATA indicators.

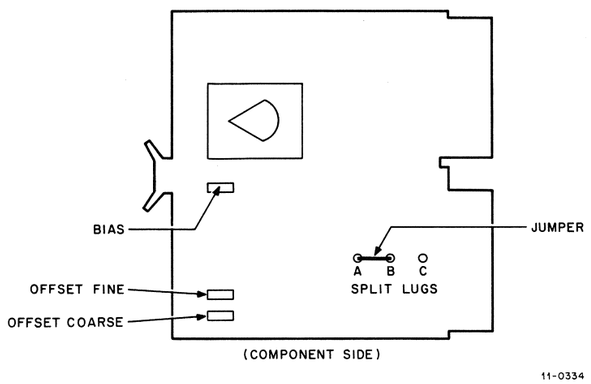


Figure 2-4 A405 Sample and Hold

2.6.5 **Switched-Gain Amplifier A220**

Adjust the A220 Switched-Gain Amplifier as follows:

Step	Procedure
1	Ensure that Module A220 is installed in slot A16 and that Module A124 is installed in slot B16.
2	Connect EDC to A16P2 and A16F2 (GND). Set EDC to +600 μV.
3	Start the Display Conversion Loop (SA 220_8) of the diagnostic program with a gain of 8 (SW6 and SW7 = 1).
4	Adjust input offset potentiometer (Figure 2-5) on A220 Module for 000 001_8 to 000 000_8 on the console DATA indicators.
5	Set EDC to 0.625V and verify that DATA indicators display the following readouts with specified gain settings:

Data (±1 bit)	SW6	SW7	Gain
000100_8	0	0	1
000200_8	1	0	2
000400_8	0	1	4
001000_8	1	1	8

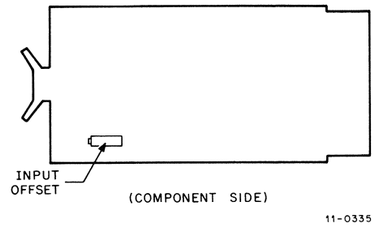


Figure 2-5 A220 Switched-Gain Amplifier

2.6.6 **Multiplexer Setup**

Set up multiplexer as follows:

a. Verify that A124 Multiplexer Switch Modules are installed in the following slots:

CH00	CH03	Slot A17
CH04	CH07	Slot A18
CH08	CH11	Slot A19
CH12	CH15	Slot A20
CH16	CH19	Slot B17
CH20	CH23	Slot B18
CH24	CH27	Slot B19
CH28	CH31	Slot B20

b. If the G735 Test Card Module is available, perform the following procedure:

NOTE

The G735 Module produces eight distinct voltage levels when fed from the EDC. The first level, fed to channels 0, 10_8, 20_8, 30_8 is equal to the input level from the EDC. Each successive level is half the previous one and appears on the next channel, except that the last level is ground. Jumper X should be connected on the module for testing the AD01-D.

Step	Procedure
1	Insert the G735 Module in slot AB21.
2	Connect EDC to the tabs at the handle end, and set EDC to +10V.
3	Set the SR on the console to 270_8 and press start.
4	Load the initial channel of the multiplexer to be tested in DATA bits 00_8 through 04_8, then press CONT. The program will halt.
5	Load the number of channels to be tested in DATA bits 00_8 through 04_8, then press CONT. The program will again halt.
6	Set the SR to all 0s and press CONT. The program should run. After one complete pass, the Teletype bell will sound.
7	Set bit 06 of the SR to 1. The following table is printed:

Channel	Initial Value	Final Value
CH00	1777	1777
CH01	1000	1000
CH02	0400	0400
CH03	0200	0200
CH04	0100	0100
CH05	0040	0040
CH06	0020	0020
CH07	0000	0000
↓		↓
CH37	0000	0000

NOTE

If differences between initial values and final values of more than one count occur, check the multiplexer channel in question. It may be noisy and should be replaced.

c. If the G735 Module is unavailable, perform the following procedure:

Step	Procedure
1	With the program running the Display Conversion Loop (SA 220_8) check each multiplexer channel by moving the EDC to the proper input pins in slot AB21.
2	Verify the correct results on the DATA indicators of the computer.

2.6.7 External Sync

NOTE

Before connecting the external sync to the AD01-D, associated jumpers must be removed. These jumpers are:

EXT IN – A22R2 to A22C2
EXT IN A – B08B2 to B08N2

After connecting the external sync (refer to Table 2-1), the EXTEST and EXFAST Diagnostic Subroutines can be run to verify proper operation of the AD01-D under control of external sync.

CHAPTER 3
OPERATION AND PROGRAMMING

3.1 INTRODUCTION

Operation of the AD01-D is controlled entirely by the PDP-11 Computer program. All I/O and control programming is done by issuing the normal memory reference instructions. The nature of the program depends on the system application and the familiarity of the programmer with the particular application and the PDP-11 instruction set.

3.2 ADDRESS FORMAT

The AD01-D is assigned two bus addresses:

a. 776770_8 for the control and status register (CSR)

b. 776772_8 for the data buffer register (DBR).

All information flows between the processor and the AD01-D through these registers. The address format is shown in Figure 3-1.

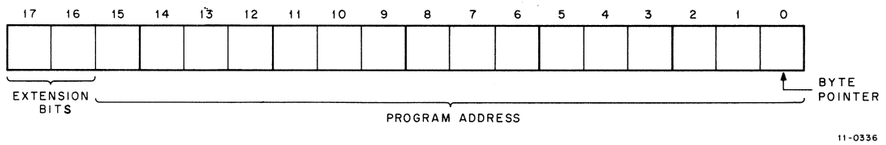


Figure 3-1 Address Format

3.3 CSR FORMAT

The operating condition of the AD01-D is established by transferring a 16-bit control word or an 8-bit control byte from the processor to the CSR. The status of the AD01-D can be determined by transferring the contents of the CSR to the processor and testing the status bits. The CSR format and bit assignments are illustrated in Figure 3-2. The purpose and description of each bit in the CSR is presented in Table 3-1.

3.4 DBR FORMAT

On command, the AD01-D digitizes the unipolar analog voltage of the selected channel into a 10-bit binary code, using the successive-approximation technique. The bipolar option permits conversion of bipolar analog voltage

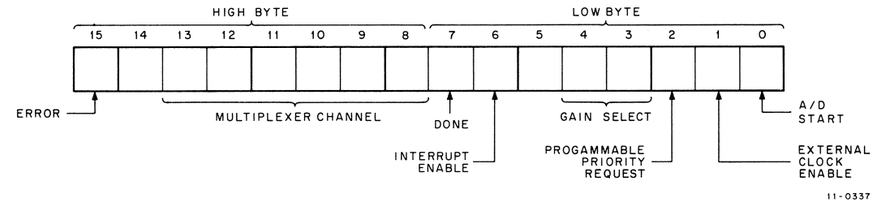


Figure 3-2 CSR Format

Table 3-1
CSR Bits

Bit	Description
15	ERROR(ER) – indicates device has been issued a START command during the time between Start Conversion and Read ADDB. Cleared by INIT. Set by CONVERT command if error condition is present. Cleared under program control when new Gain and MUX Channel data is loaded. **NOTE** **The main purpose of the Error Bit is to indicate timing problems that could occur if an external clock is starting conversions at certain intervals and conversions are being made under program control between the external clock pulses.**
14	Unused.
13-08	MULTIPLEXER CHANNEL (MC) – Selects 1 of 64 multiplexer channels. Loaded under program control. Cleared by INIT.
07	DONE (DN) – Indicates state of converter. Reset by INIT. Set by A/D Done. Reset by reading ADDB. Read only.

(Continued on page 3-2)

Table 3-1 (Cont)
CSR Bits

Bits	Description
06	INTERRUPT ENABLE (IE) – Allows interrupts on A/D Done or Error. Set under program control. Cleared by INIT.
05-03	Unused.
4-3	GAIN SELECT (GS) – Selects gain for programmable gain amplifier. Loaded under program control. Cleared by INIT.
02	PROGRAMMABLE PRIORITY REQUEST SELECT (PS) – Allows selection of bus request line under program control. When bit 02 = 0, bus requests are made at level 7. When bit 02 = 1, bus requests are made at a level determined by bus grant jumper socket on G736 Module. Set under program control. Cleared by INIT.
01	EXTERNAL CLOCK ENABLE (EE) – Allows converter to be controlled by external input. Loaded under program control. Cleared by INIT.
00	A/D START – Start conversion. Loaded under program control. Cleared by INIT. Cleared by A/D Done (Write Only).

into an 11-bit two's complement code with an extended sign format. The digitized analog voltage is stored in the DBR when the conversion is done. A single move instruction can then be programmed to gate the contents of the DBR onto the Unibus. The data format for unipolar and bipolar operation is illustrated in Figure 3-3. Table 3-2 relates the octal representation of the data word to the input analog voltage to highlight differences between unipolar and bipolar operation.

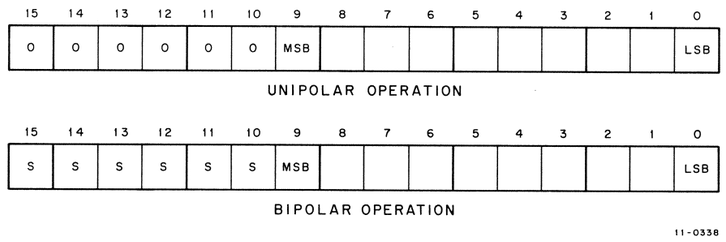


Figure 3-3 DBR Format

3.5 INTERRUPT STRUCTURE

The AD01-D utilizes the interrupt structure of the PDP-11 System to inform the processor that the A/D conversion is done or to indicate that an error condition exists. The interrupt logic in the AD01-D can be enabled or disabled under program control. Bit 06 of the CSR is assigned to enable the interrupt logic. If the interrupt logic is enabled, one of two priority levels can be selected by the program. Bit 02 is assigned to select the priority level. Priority level 7 is enabled when bit 02 is reset, and the priority level established by the bus grant jumper socket on the G736 Module is selected when bit 02 is set. Bus grant jumpers are available for priority levels 4, 5, and 6. When the AD01-D is shipped from the factory, jumper plug S408778 for priority level 5 is installed in the G736 Module.

Table 3-2
Output Notations

Analog Input Voltage*	Unipolar	Bipolar
-10.0	---	176000_8
- 5.0	---	177000_8
0.0	000000_8	000000_8
+ 5.0	001000_8	001000_8
+ 9.9902	001777_8	001777_8

*For 10V full-scale input range. Divide by appropriate gain factor for the input ranges.

3.6 EXTERNAL CLOCK CONTROL

The AD01-D contains two inputs for external control of the conversion process: EXT IN and EXT IN A.

3.6.1 EXT IN

The EXT IN signal is brought into the converter on the M908 Analog Input Module in slot A21, pins A1 and B1 (B1 is EXT common). Input signal conditioning is provided by the M501 Schmitt Trigger circuit. The upper and lower thresholds are set at 1.7V and 1.1V. Input signal swing is limited to ±20V. Input standards are as follows:

Signal swing: ±20V
Loading: 2.7 KΩ to +5V or 1.8 mA at GND

NOTE
Before connecting EXT IN to the AD01-D, the jumper wire from A22R2 to A22C2 should be removed.

3.6.2 EXT IN A

The EXT IN A signal is brought into the converter on the M908 Analog Input Module in slot A21, pins A2 and B1 (B1 is EXT common). This input is T^2L compatible. Triggering is accomplished by a level change from high to low or a pulse to low, the duration of which is $\geq$ 50 ns. The fall time of the input trigger should be $<$ 400 ns.

Input standards are as follows:

Signal swing: T^2L logic levels
Timing: Level – high to low fall time $<$ 400 ns
Pulse – high to low, duration $\geq$ 50 ns
Loading: 2-1/2 unit loads

NOTE
Before connecting EXT IN A to the AD01-D, the jumper wire from B08B2 to B08N2 should be removed.

3.6.3 External Clock Timing Considerations

Figure 3-4 is a timing diagram that shows the operation of the AD01-D under external clock control. In the external mode, time is not allowed for the switched gain amplifier to settle, thereby initiating a conversion at the time the external signal is applied. Thus, the user must allow at least 5 μs for settling of the input amplifier, if necessary.

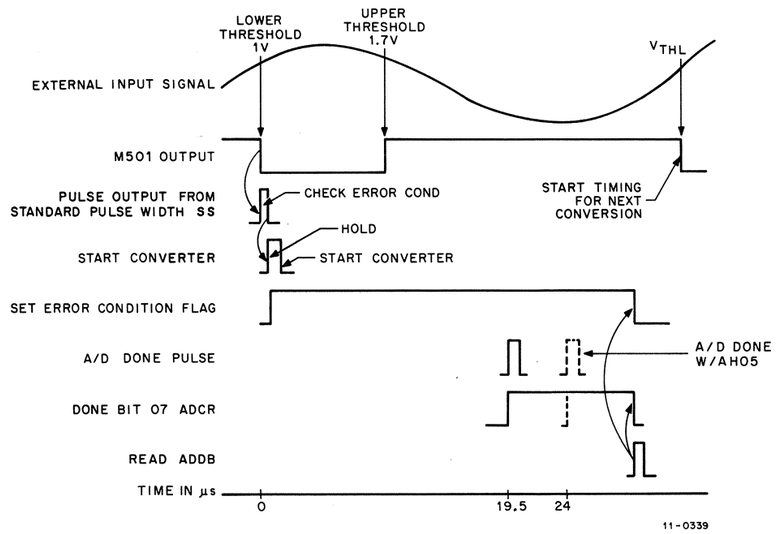


Figure 3-4 External Clock Timing