DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

ACCESSORY LIST

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- D DOCUMENT
- DN DOCUMENT CHANGE NOTICE
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ITEM NO.	DWG NO./PART NO.	DESCRIPTION	QUANTITY/VARIATION							KIT CHECK BY ___ DATE ___	INSTALLATION CHECK BY ___ DATE ___
1	DEC11-HADA-D	AD01-D Maintenance Manual	1								
2	C-13531	Schematic Deltron	1								
		(DEC # 12-3185-2 H727-A)									
		(DEC # 12-3185-4 H727-B)									

TITLE	ASSY. NO.	SIZE	CODE	NUMBER	REV.	ECO NO
Accessory List	SHEET 1 OF 1	A	AL	AD01-D-08		

DIST.

DEC FORM NO.
DRA 121

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

DATE 1-21-71

TITLE AD01-D Specifications

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE

ENG	APPD	SIZE	CODE	NUMBER	REV
		A	SP	AD01-D-10	

DEC FORM NO. DRA 107A

ENGINEERING SPECIFICATION — CONTINUATION SHEET

TITLE AD01-D 10 Bit A/D Converter Subsystem - Specifications

0.0 AD01-D GENERAL DESCRIPTION

The AD01-D is an analog input subsystem for use with the PDP-11 computer. It features a 10 bit analog to digital converter with extended dynamic range. This range is achieved by means of an amplifier with gains of 1, 2, 4 and 8 selectable under program control.

0.1 A single-ended multiplexer is provided for. Channels can be implemented in groups of four up to a maximum of 32. A one word output from the computer to the Gain-MUX control register selects both amplifier gain and multiplexer channel address.

0.2 The computer interface includes two registers: a control and status register, ADCS and data register, ADDB. Novel features of the interface include the ability to set the converter into the interrupting or non-interrupting mode. In the interrupting mode the AD01-D is capable of interrupting on A/D done or on the error condition of starting a new conversion before the previous conversion is complete. The non-interrupting mode enables the converter to approach its maximum throughput rate under program control.

	SIZE	CODE	NUMBER	REV
	A	SP	AD01-D-10	

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0.3 Conversion results are entered on the data lines of the unibus of the computer at the right most end. When bipolar operation is implemented, the sign bit is extended to the left to fill the remaining bits.

0.4 The AD01-D subsystem is contained in a single 5¼" high rack mounting panel. This includes an analog power supply sufficient for the basic unit and all prewired options. Also required is an externally mounted 5 volt power supply.

1.0 GENERAL SPECIFICATIONS

1.1 The AD01-D consists of several functional parts as enumerated in the following paragraphs:

1.1.1 A812 Analog to Digital Converter - (10 Bit Unipolar)

When provided with an input voltage and start pulse the converter module produces ten output bits which correspond to the value of the input voltage. The successive (serial) approximation technique is used. When the ten output bits have been determined the converter module produces a done pulse. The input voltage range of the converter is 0 to +10 volts. The input resistance is 1250 ohms ±0.1%.

1.1.2 Multiplexer Control

The six bit MUX channel address is received by the ADCS. An M161 octal decoder converts the three most significant of these bits to an enabling level for one of eight A124 multiplexer modules. The eight prewired slots provided for these modules are A17 through A20 and B17 through B20. When expanding the channel capacity modules must be added in the A level before the B level progressing from slot 17 toward slot 20. The last two bits of the channel address are decoded on the enabled A124 module. The sixth bit is included for future expansion to 64 channels.

1.1.3 Power Supplies

Analog power for the circuitry is furnished by an H727 power supply in conjunction with an A708 voltage regulator module. The H727 supplies +15VDC at 400ma and -20VDC at 400ma. The -20VDC power is used only by the A124 multiplexer modules (30ma each). All other A series modules use -15 volts derived from the negative regulator section of the A708. The maximum current drain on this -15 volt regulator is 200ma. The A708, when fully loaded, takes 200ma from the -20 volt output of the H727. The +15 volt output of the H727 provides

350ma to the analog modules.

1.1.4 Remote Gain Control Amplifier

The gain control bits are received from the accumulator through the gain and mux register. These bits are decoded and converted to gain switching action by an A124 multiplexer module. The operational amplifier used is an A220. The configuration is non-inverting with gains of 1, 2, 4 and 8. A truth table is given in the programming section of this document. The input impedance of the amplifier is greater than 1000 megohms in parallel with 20pF. Settling time to either a gain change or a 10 volt input change is less than 3 microseconds to within one count of the ADC.

1.2 Options

1.2.1 Multiplexer Modules

The A124 multiplexer switch selects one of four input channels on the basis of two input bits and an enabled input. These logic inputs are TTL compatible, and all represent less than one unit load. The analog switches are enhancement-mode mosfets, and all channels

are off when power is removed. The ON resistance is less than 2000 ohms. OFF resistance and capacitance are 200 megohms and 1 picofarad respecitively. Normal operation requires that the input voltage be in the range of ±10 volts. Input voltages up to 20 volts and input currents up to 3ma will cause no damage. Response time (including delay) is less than 1.2 microsecond in both the ON and OFF directions.

1.2.2 Sample and Hold Amplifier - AH04

The A405 Sample and Hold Module Specifications are enumerated here:

Acquisition Time	
Within 5mv, 10v step input, max:	5usec
Aperture Time, max:	0.1usec
Gain	-1.000 (±.02%)
Input	
Voltage range	±10v
Impedance	2K ohms ±1%
Output	
Voltage range, max:	±10v
Current, mas:	10ma
Impedance, Max:	0.1 ohm

Offset (between sample & hold modes):	Less than or equal to 15mv
Temperature coefficient of offset, mx:	50uV per ^{o}C
Droop (max at 25^{o}C, Note 1):	10mV/msec
Track-Hold Control	
Level Control - Pin BF2 (jmper - W1)	T^2L compatible 1 unit load Logic Ø or Low - Hold Logic 1 or High - Track
Pulse Control - Pin BF2 (jmper - W2) - Pin BH2	Track - 1 unit load Hold - 1 unit load

NOTE 1: Droop doubles for each 10^{o}C increase in temperature.

1.2.3 AH05 Sign Option

Implementation of the AH05 option is accomplished by substituting the A812 module in slots AB12 with the A862 bipolar A-D converter module in slots AB13. Conversion time for this module is 24usec. giving 10 bits + sign in two's complement notation. Total system conversion time is 29usec with AH05.

1.3 Mechanical Configuration

The entire AD01-D is contained in an H911 logic rack with six H803 connector blocks. The right hand end (as viewed from the front of the rack) is occupied by the analog power supply. The 5 volt logic supply is also rack mount.

1.4 General Specifications

1.4.1 Power Requirements

1.4.1.1 AD01-DA:	110v, 60Hz
Analog Power Supply:	H727A
AC current:	less than ½ amperes
Power Dissipation:	less than 25 watts
Digital Logic Supply:	H716B
AC current:	less than 3 amperes

1.4.1.2	AD01-DB:	230V, 50Hz
	Analog Power Supply:	H727B
	AC Current:	less than ¼ amperes
	Power Dissipation:	less than 25 watts
	Digital Logic Supply:	H716D
	AC Current:	less than 1.5 amperes
	Power Dissipation:	less than 25 watts

1.4.2 Environmental Specification

Temperature Range (operating):	$0^{o}C$ to $55^{o}C$
Temperature Range (storage):	$-25^{o}C$ to $+85^{o}C$
Temperature Coefficient of Zero:	less than 30 microvolts per ^{o}C referred to input +100 microvolts per ^{o}C referred to output.
Temperature Coefficient of Gain:	less than 0.005% per ^{o}C.

1.5 General Performance Specifications

1.5.1 Number of Channels

Any number of channels up to 32 can be accommodated by the AD01-D. Expansion to 64 channels is possible with the addition of another 1943 rack.

1.5.2 System Speed

The AD01-D conversion time is 22usec ±1usec including response to new channel and gain selection. This time is measured from the initiation of new gain and channel address information or the setting of the A/D start bit in the control & status register. The conversion period is terminated by the done pulse, which sets the done bit. Conversion time with AH05 is 29usec ±1usec.

1.5.3 Input Specifications

1.5.3.1 Configuration: Single-Ended

1.5.3.2 Input Impedance

Greater than 1,000 megohms in parallel with less than 20pF.

1.5.3.3 System Accuracy

0.1% of full scale ±½LSB

1.5.3.4 Gain

Gains of 1, 2, 4 and 8 are selectable by program control.

1.5.3.5 Gain Accuracy

±0.05%

1.5.3.6 Input Voltage

0 to 10 volts, 5 volts, 2.5 volts, and 1.25 volts. These ranges are unipolar and positive on the basic

AD01-D and are bipolar two's complement on the AD01-D

with sign and magnitude option.

1.5.4 Noise

The peak-to-peak noise including both line frequency and random components is less than 0.2 LSB on the 10 volt and 5 volt ranges, less than 0.4 LSB on the 2.5 volt range, and less than 0.8 LSB on the 1.25 volt range. These figures are to 99.7% confidence. When sample and hold is included, increase these figures by 20%.

1.5.5 Zero Offset

Adjustable to zero. Calibrated for first switching point at

+½ LSB.

1.5.6 Resolution

One part in 1.024 of full scale (9.8mv).

2.0 SPECIFICATIONS OF VENDOR-SUPPLIED EQUIPMENT

2.1 Regulated DC analog power supply H727A. See DEC Purchase Specification 12-03185-2. Use H727B when 230VAC input is desired. See Purchase Specification 12-03185-4. Regulated DC 5v logic supply H716B. See DEC Purchase Specification 30-9282.

3.0 PROGRAMMING SPECIFICATIONS

3.1 Starting the Converter

In the AD01-D a conversion can be initiated in three different ways:

1) Set A/D start, Bit ØØ ADSC.

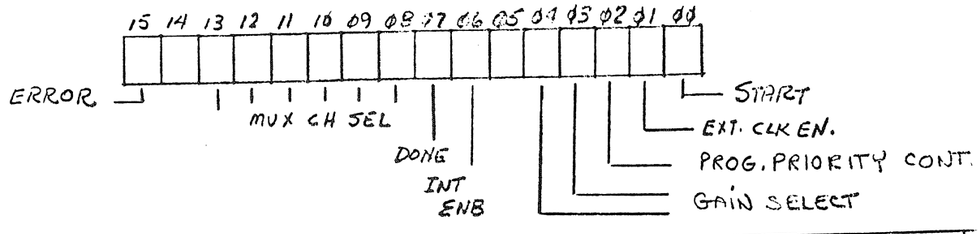
2) Loading MUX channel address. [illegible] However, if the External Clock is enabled the programmer must set A/D start to initiate a conversion under program control. This feature makes it possible to change gain and MUX address between External Clock pulses. It is noted here that if the error Bit(15) is set and causes an interrupt, it should not be reset until a new conversion is to be initiated as clocking any data into the upper byte of the ADCS will initiate a conversion.

3) External Clock, when enabled.

3.2 Device Registers

All software control of the AD01-D is done via two (2) register. The following presents the bit assignment within each register. All bits are read/write unless stated otherwise.

3.2.1 Control and Status Register (ADCS=77677Ø)



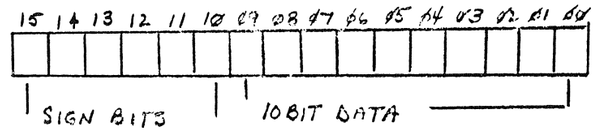
Bit	Meaning and Operation
15	ERROR - indicates device has been issued a start command during the time between start conversion and read ADDB. Cleared by INIT. Set by Convert Command. Cleared under program control upon loading new Gain and MUX Channel data.

NOTE: The main purpose of the ERROR bit is to indicate timing problems that could occur if an external clock is starting conversions at certain intervals and conversions are being made underprogram control between the external clock pulses.

13-Ø8	MUX CH - Six bits to select 1 of 64 multiplexer channels. Cleared by INIT, loaded under program control.
Ø7	DONE - indicates state of converter. Reset by init. Set by A/D Done. Reset by reading ADDB. Read Only.
Ø6	INT ENB - Will allow interrupts on A/D Done or Error. Cleared by INIT, set under program control.

Ø5	UNUSED
Ø4-Ø3	GAIN SELECT - Gain select for programmable gain amplifier. Loaded under program control. Cleared by INIT.
Ø2	PROG-PRIORITY REQUEST - Will allow selection of bus request line under program control. Bits Ø2=Ø BR7 Bit Ø2=1 priority determined by bus grant jumper socket on G736 module. Cleared by INIT, set under program control.
Ø1	EXT CLK ENB - Will allow converter to be controlled by external input. Cleared by A/D Done (Write Only).

3.2 Data Buffer (ADDB=776772)



BIT	MEANING AND OPERATION
15-1Ø	SIGN - When AH05 Sign Bit option is installed bits will take on sign in two's complement. Read Only.
Ø9-ØØ	DATA - 10 bit data word. Read Only.

3.3 Interrupt

The converter interrupts when INT ENB=1, and DONE=1 or ERROR=1. Both become true. Vector Address=130

3.4 Timing

Figure 3.3 shows the timing operations within the AD01-D

3.5 Control

No operator controls are included in this device. Any trouble shooting or calibration procedures are carried out by the use of the computer console.

3.6 External Clock Control

The AD01-D contains two inputs for external control of the conversion process.

3.6.1 Ext In

The EXT IN signal is brought into the converter on the M908 analog input module in slot A21 pins A1 and B1 (B1 is EXT common). Input signal conditioning is provided by the M501 Schmitt Trigger circuit. The upper and lower threshholds are set at 1.7 volts and 1.1 volts. Input signal swing is limited to ±20 volts.

INPUT STANDARDS

Signal Swing = ±20V
Loading = 2.7K ohms to +5V or 1.8ma @GND

3.6.2 Ext In A

The EXT IN A signal is brought into the converter on the M908 analog input module in slot A21 pins A2 and B1 (B1 is EXT common). This input is T^2L compatable. Triggering is accomplished by a level change from high to low or a pulse to low whose duration is equal to or greater than 50 nanoseconds. The fall time of the input trigger should be less than 400 nanoseconds.

INPUT STANDARDS

Signal Swing = T^2L logic levels
Timing = Level - high to low fall time $<$400nsec
Pulse - high to low, duration $>$50nsec

Loading = 2½ unit loads

3.6.3 External Clock Timing Considerations

A timing diagram is given in Figure 3.6 to show the operation of the AD01-D under external clock control. In the external mode time is not allowed for the switch gain amplifier to settle. This is done in this manner so that a conversion is initiated at the time the external signal is applied. Thus it is the responsibility of the user to allow at least 5usec for settling of the input amplifier if necessary. A logic diagram of the external clock input circuitry is provided in Figure 3.6a

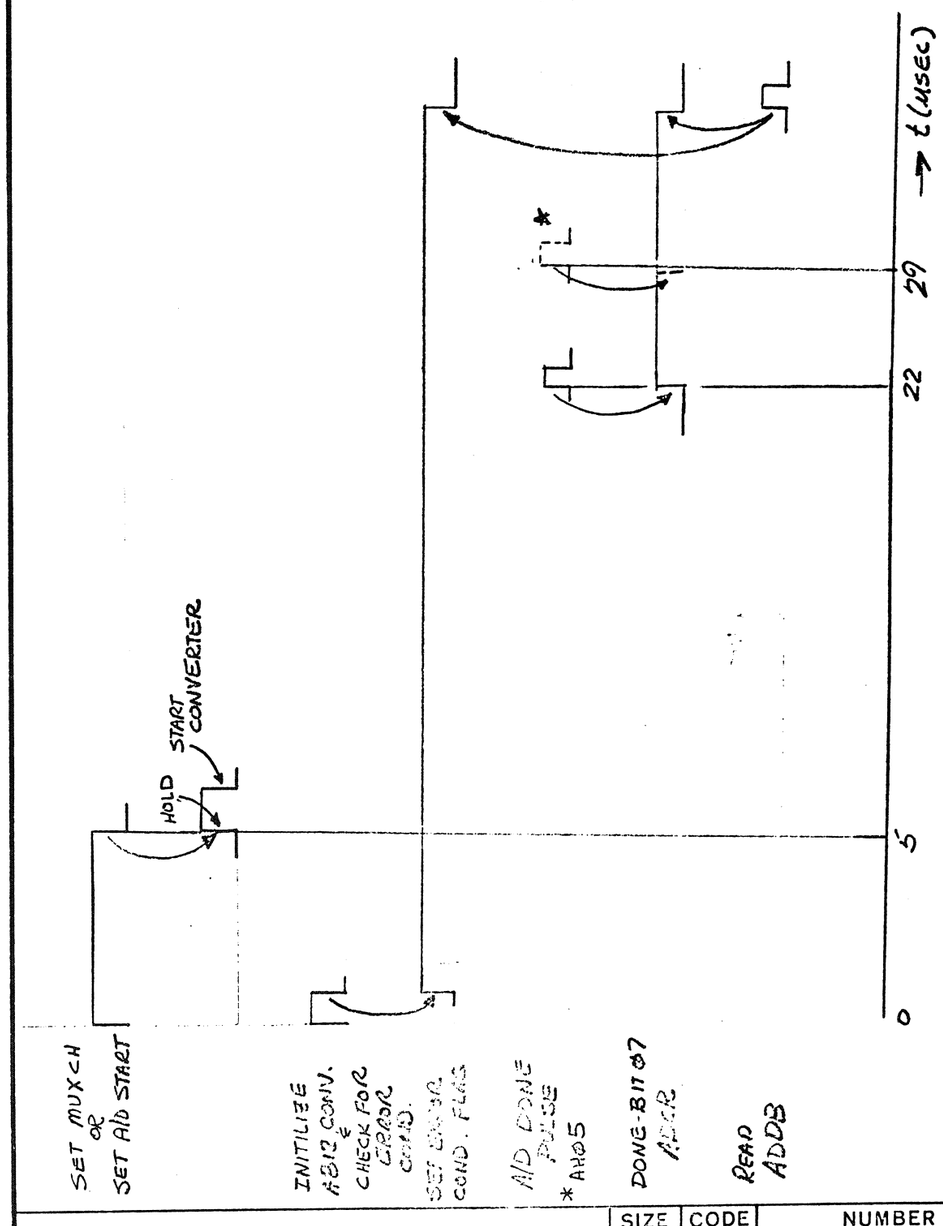


FIG 3.3 AD01-D SYSTEM TIMING

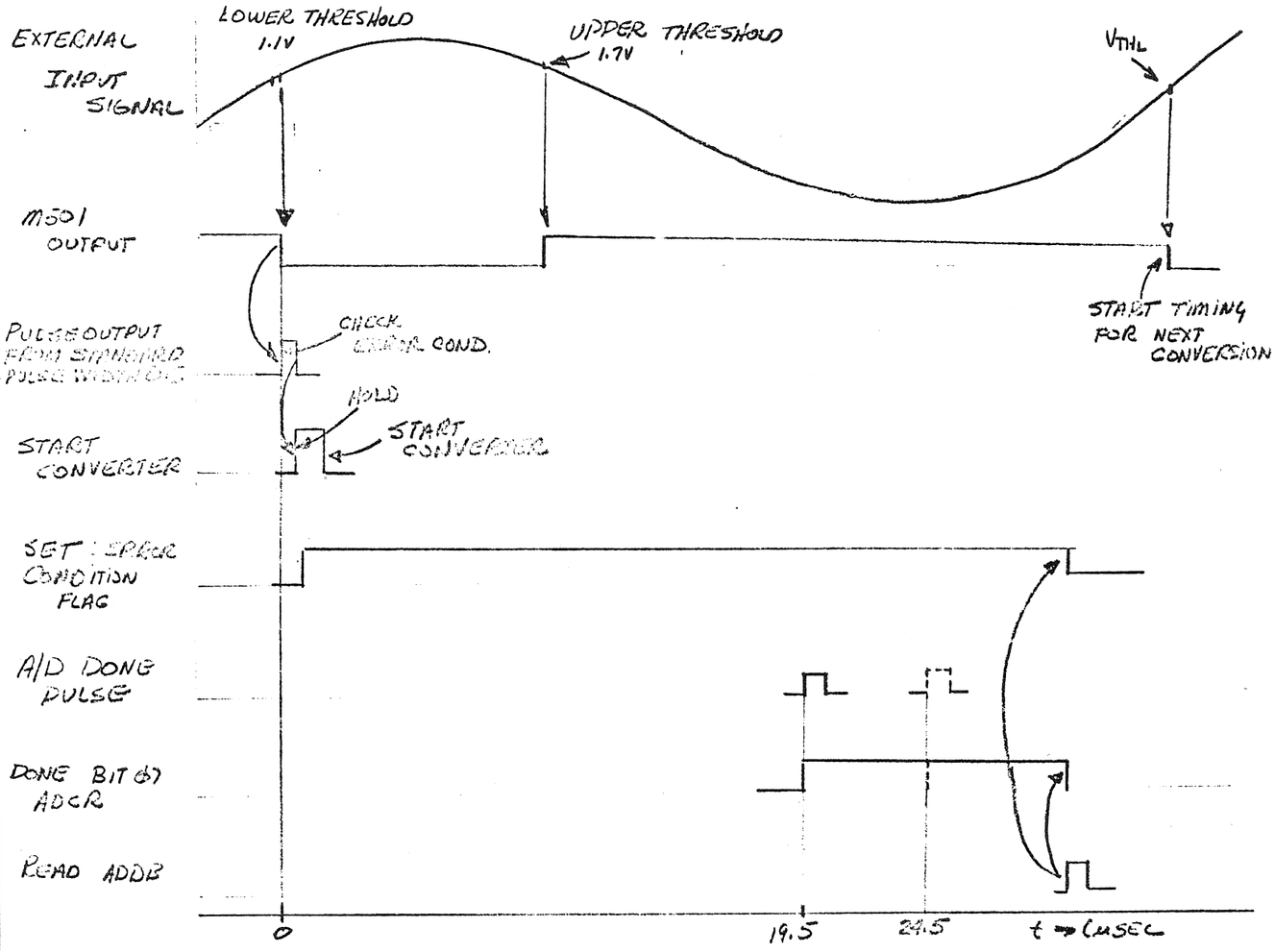


FIGURE 3.6 AD01-D EXTERNAL CLOCK TIMING.

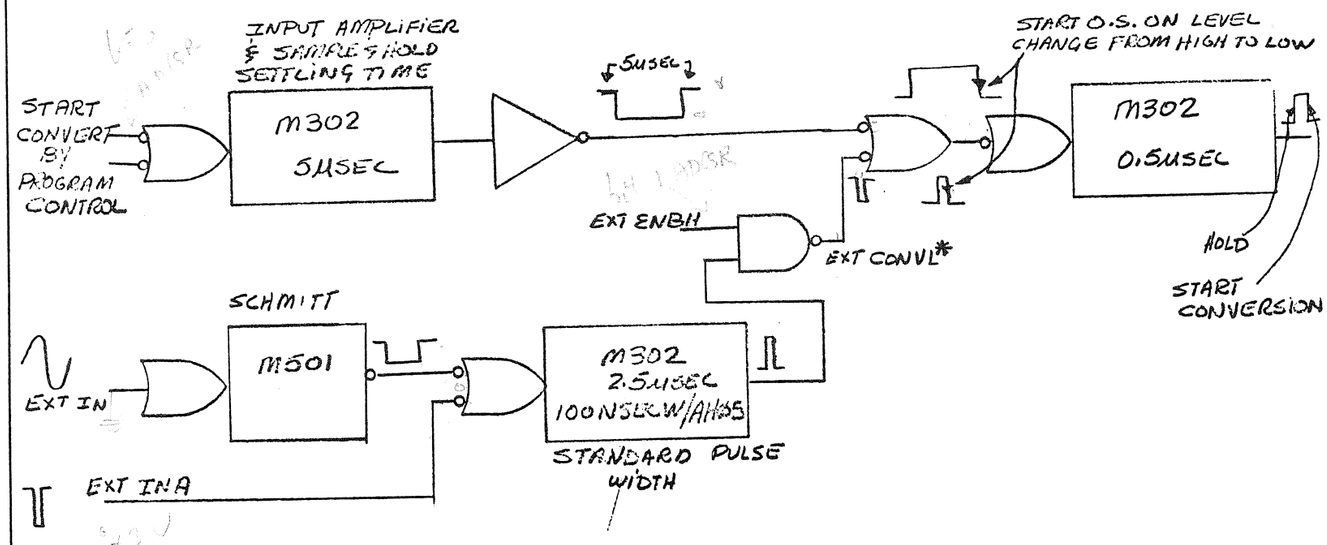


FIGURE 3.6a

EXTERNAL CLOCK INPUT SIGNAL CONDITIONING

* EXT CONVL SIGNAL BYPASSES 5USEC DELAY FOR INPUT SETTLING

BIT 14	BIT 13	GAIN	FULL SCALE VOLTS
Ø	Ø	1	10
Ø	1	2	5
1	Ø	4	2.5
1	1	8	1.25

FIG 3.1.2 GAIN SELECT TABLE

Analog-Channel Input
Pin Assignment

Channel Number		Input Pin	
Decimal	Octal	Connection	Gnd
00	00	A21B2	A21C2
01	01	A21C1	A21D1
02	02	A21D2	A21E2
03	03	A21E1	A21F1
04	04	A21F2	A21H2
05	05	A21H1	A21J1
06	06	A21J2	A21K2
07	07	A21K1	A21L1
08	10	A21L2	A21M2
09	11	A21M1	A21N1
10	12	A21N2	A21P2
11	13	A21P1	A21R1
12	14	A21R2	A21S2
13	15	A21S1	A21T1
14	16	A21T2	A21U2
15	17	A21U1	A21V1
16	20	B21B2	B21C2
17	21	B21C1	B21D1
18	22	B21D2	B21E2
19	23	B21E1	B21F1
20	24	B21F2	B21H2
21	25	B21H1	B21J1
22	26	B21U2	B21K2
23	27	B21K1	B21L1
24	30	B21L2	B21M2
25	31	B21M1	B21N1
26	32	B21N2	B21P2
27	33	B21P1	B21R1
28	34	B21R2	B21S2
29	35	B21S1	B21T1
30	36	B21T2	B21U2
31	37	B21U1	B21V1