

KWV11

KWV11A DIAGNOSTIC
CVKWACO

AH-8224C-MC

COPYRIGHT '76-80

FICHE 1 OF 1

JAN 1980

digital

MADE IN USA

IDENTIFICATION

B 1

SEQ 0001

Product Code: AC-8222C-MC
Product Name: CVKWACO KVV11A Diagnostic
Date Created: October 1976
Date Revised: July 1979
Maintainer: Diagnostic Engineering

Copyright (C) 1976,1979
Digital Equipment Corporation

This software is furnished under a license for use only on a single computer system and may be copied only with the inclusion of the above copyright notice. This software, or any other copies thereof, may not be provided or otherwise made available to any other person except for use on such system and to one who agrees to these license terms. Title to and ownership of the software shall at all times remain in DEC.

The information in this document is subject to change without notice and should not be construed as a commitment by Digital Equipment Corporation.

DEC assumes no responsibility for the use or reliability of its software on equipment which is not supplied by DEC.

Table of Contents

1.0	ABSTRACT
2.0	REQUIREMENTS
2.1	Equipment
2.2	Storage
3.0	LOADING PROCEDURE
3.1	Method
3.2	Non-Standard Address, Vector, or Use of Software Switch Register
4.0	STARTING PROCEDURE
4.1	Control Switch Settings
4.2	Starting Address
4.3	Program and/or Operator Action
5.0	OPERATING PROCEDURE
5.1	Switch Register Function
5.2	Scope Loops
5.3	Program and/or Operator Action
5.3.1	Logic Test
5.4	Inhibiting Auto-Size Feature
6.0	ERRORS
6.1	Error Printout
6.1.1	Example
6.2	Non-Standard Error Halts
7.0	RESTRICTIONS
7.1	External Inputs
7.2	Starting Restriction
7.3	Possible Program 'BOMBS'
8.0	MISCELLANEOUS
8.1	Power Fail
8.2	XXDP, ACT, APT
8.3	Execution Time
8.4	LSI-11 'ODT' Commands
8.5	Entering LSI-11 'ODT'
8.6	Use of Program Software SWR
8.7	Special I/O Signal Tests
8.8	Production Starting Address
8.9	Testor Starting Address
8.10	Trap Catcher

1.0 ABSTRACT

This program allows the user check-out or debug the KWV11A, Programmable Real-Time Clock. The logic test is self contained and needs no external maintenance hardware or operator intervention with only one exception: If the customer hardware connected to the KWV11 could inject signals on ST2, ST1, or SLAVE IN inputs, it must be disconnected.

Even though the KWV11 is a Q BUS option, this program was designed to run on any PDP-11 Family computer. If the user is unfamiliar with an LSI-11 he should review sections 8.4 and 8.5. A software switch register is included with this program.

Every effort was made to make this program conform to LSI-11 programming restrictions, however; the user should read sections 7.2 and 7.3.

2.0 REQUIREMENTS

2.1 Equipment

1. PDP-11 Family computer with 8K of memory (or more) and I/O facilities (i.e., TTY).
2. KWV11 under test.

2.2 Storage

This program occupies and uses 8K of memory.

3.0 LOADING PROCEDURE

3.1 Method

Standards procedure for normal binary tapes should be followed.

1. Absolute loader must be in memory.
2. Place binary tape in reader.
3. Type Address *7500 (5* determine by location of loader).
4. Type 'G' (program will be loaded into memory).

The program can also be loaded by XXDP, ACT, or APT.

3.2 Non-Standard Address, Vector, or Use of Software Switch Register

This program is set to test a KW11 with a standard address and vector. If any of these are different on the KW11K you are testing, change the corresponding location in memory before starting this test.

<u>LOCATION</u>	<u>TAG</u>	<u>CURRENT CONTENTS</u>	<u>COMMENTS</u>
1250	\$BASE:	170420	::BASE ADDRESS OF EQUIPMENT :: UNDER TEST
1244	\$VECT1:	000440	::INTERRUPT VECTOR #1
176	\$SWREG:	000000	::MANUAL SWR.
1157	\$TPFLG:	.BYTE 0	::'TERMINAL AVAILABLE' :: FLAG (BIT<0:7>=0=YES)

4.0 STARTING PROCEDURE

4.1 Control Switch Setting

Before starting the diagnostic, set all switch register bits as desired, see section 5.1.

4.2 Starting Addresses

200 Start of Logic Tests
204 Restart Address for Logic Test
210 I/O Signal Test #1
214 I/O Signal Test #2
220 I/O Signal Test #3
230 Production Starting Address
240 Testor Starting Address

4.3 Program and/or Operator Action

All switches in switch pack 2 should be in the 'OFF' position except when instructed.

1. Load program into memory.
2. Enter keyboard 'ODT'.
3. Alter location '\$SWREG' (Address 176) to reflect desired options of a switch register - see section 5.1.
4. Type starting address, followed by 'G' to start program.

5.0 OPERATING PROCEDURE

5.1 Switch Register Function

SWR BIT	OCTAL	FUNCTION WHEN SET
15	100000	HALT ON ERROR
14	040000	LOOP ON TEST
13	020000	INHIBIT ERROR TYPEOUT
12	010000	ENABLE LINE FREQ. RATE TESTING
11	004000	INHIBIT ITERATIONS (SHORT PASS)
10	002000	BELL ON ERROR
09	001000	LOOP ON ERROR
08	000400	LOOP ON TEST IN SWR <7:0>

5.2 Scope Loops

If an error occurs and the user wishes to scope the error, '\$SWREG' should be altered to '100000' at the start of the test to halt on error, then when the program halts on error and the CPU enters 'ODT', '\$SWREG' should be altered to '060000' to loop on current test and inhibit error typeout, then type 'P' to continue program execution.

5.3 Program and/or Operator Action

All switches in switch pack 2 should be in the 'OFF' position except when instructed.

5.3.1 Logic Test

The first pass through the program will be made with iterations inhibited. Successive passes will enable iterations if SWR11=0.

If not inhibited by APT, the program will look for more KVV11's to exercise, one pass will exercise all KVV11's.

If four units are detected, the following will be typed:

```
UNIT #000001 COMPLETED TESTING UNIT #000002  
UNIT #000002 COMPLETED TESTING UNIT #000003  
UNIT #000003 COMPLETED TESTING UNIT #000004  
UNIT #000004 COMPLETED
```

At End of Pass when all units have been tested, the following typeout will occur:

```
'ENDPASS 12 - TOTAL ERRORS 4 THERE ARE 4 (OCTAL) UNITS -  
GOOD UNITS (L TO R) 000000000001011''.
```

This indicates that the program has completed 12 octal (10 decimal) passes. During that time 4(octal) errors were detected. Also we tested 4 units and the third unit was the only unit to fail.

5.4 Inhibiting Auto-Size Feature

This program will automatically auto-size and test each KVV11 it detects on the system. To inhibit this feature, set bit 15 of location '\$ENVM'. Also, to test an individual KVV11 in a group, set this bit and refer to section 3.2 for changing the base address of the KVV11 under test.

6.0 ERRORS

6.1 Error Printout

Printout varies with the error detected. The error PC typed out is the actual location of the error call.

A HALT at location '\$TYPE'+10 when running with no terminal indicates an error has occurred. To find out the number of the error, examine location '\$STNM'. This is the item number of the error. To find out what the error typeout would have been goto to the error pointer table beginning at location 'ERRTB'.

6.1.1 Example

If we examined location '\$STNM' and found a 5(101) we go to location '\$ERRTB' and look through the error pointer table until we found item 5. The information would look like:

;ITEM 5

```
EM5      ;CLOCK SR DATA ERROR
DH5      ;ERRPC ASR WAS S/B
DT5      ;$ERRPC,ASR,$BDDAT,$GDDAT
DF0      ;ALL NUMBERS ARE IN OCTAL FORM
```

To find out the information specified by DT5 (\$ERRPC,BSR,\$BDADR,\$BDADR) follow these steps:

1. Look up the address of the label (i.e., \$ERRPC) in the symbol table which follows the listing.
 2. * Put this address in the switch register and depress the LOAD ADDRESS switch on the processor's console.
 3. * Now depress the EXAMINE switch.
 4. * The data displayed in the data lights is the information that would have been printed for his label if you had a input/output terminal.
- * See section 8.4 for LSI-11 ODT commands.

6.2 Non-Standard Error Halts

Bus errors will cause a Halt to the routine "IOTRD". The address that caused this trap will be in address "TRTC".

7.0 RESTRICTIONS

All switches in switch pack 2 should be in the "OFF" position except when instructed.

7.1 External Inputs

External inputs such as "SLAVE IN", "ST1" and "ST2" must not be connected to any customer hardware that might generate these signal while the diagnostic is running.

7.2 Starting Restriction

If a free-running clock, such as 60Hz from the power supply, is attached to the "BEVNT" bus line on both Rev level C/D and E systems, an interrupt to location 100 will occur when using the "G" and "L" commands prior to executing the first instruction. Therefore this program can not disable the BEVNT bus line by inhibiting interrupts.

User systems requiring a free-running clock attached to the BEVNT bus line can temporarily avoid this situation by setting the PSW(RS) to 200, loading the PC with the starting address instead of using the "G" command, and then using the "P" command. Before using the "L" command, the PSW(RS) can be set to 200, thereby inhibiting interrupts, to avoid receiving the event interrupt after loading the ABS loader.

7.3 Possible Program 'BOMBS'

The first two tests of this program check to see if the KVV11 responds to the address the program thinks its at. If the KVV11 does not respond, a bus error occurs. Also bus errors can occur during the time the program sizes to see how many KVV11 are on you system.

For more information on the next subject, see JAN. 1976 LSI-11 ENGINEERING BULLETIN issued by The Digital Components Group.

Bus errors may alter the preset contents of location 4 before the trap is executed, thereby transferring program control to area in the program that was not set up to handle the trap. If this happens, the program will 'BOMB' and possibly rewrite parts of itself.

8.0 MISCELLANEOUS

8.1 Power Fail

After a power failure occurs, the program execution will continue at the point where the power occurred. The program will type 'POWER'.

8.2 XXDP, ACT, APT

The program is chainable under XXDP, ACT, or APT. Although 'APT Hooks' have been installed, they have not been tested.

8.3 Execution Time

0.5 minutes (30 sec) iteration inhibited - no errors
2.5 minutes (150 sec) with iterations - no errors

8.4 LSI-11 'ODT' Commands

<u>FORMAT</u>	<u>DESCRIPTION</u>
<CR> return	Close opened location and accept next command.
<LF> line feed	Close current location; open next sequential location.
^(uparrow)	Open previous location.
_(left arrow)	Take contents of opened location, indexed by contents of PC, and open that location.
@	Take contents of opened location as absolute address and open that location.
R/	Open the word at location R.
/	Reopen the last location.
\$N/ or RN/	Open general register N(0-7) or S(PS register).
R;G or RG	GOTO location R and start program.
NL	Execute bootstrap loader using N as device CSR. Console device is 177560.
;P or P	Proceed with program execution.
RUBOUT	Erases previous numeric character. Response is a backslash ().

8.5 Entering LSI-11 'ODT'

The HALT or ODT microcode state of the KD11F (LSI-11 module) can be entered in five different ways (others are a subset of these) from the run state:

1. Execution of a LSI-11 HALT instruction.
2. A double BUS error.
3. As a POWER UP option.
4. ASCII break with DLV11 framing error asserting the B HALT line (enabled by jumper of DLV11).

Upon entering the HALT state, the KD11F responds through the set of command listed in section 8.4.

8.6 Use of Program Software SWR

The program software switch register is enabled if

1. No hardware SWR exists;
2. If you start with all ones (SWR=177777) in the switch register.

The software switch register may be changed by typing ^G (Control and letter G keys typed simultaneously). When ^G is typed, the program responds by typing 'SWR=XXXXXX' where XXXXXX equals the former contents of the switch register.

If you wish to keep the current value, type <CR>. If you wish to change the value, type the new value followed by a <CR>.

It is important to note that the diagnostic is not running after the ^G until a <CR> is typed.

8.7 Special I/O Signal Tests

Three tests were included to enable checkout of I/O signals: ST1, ST2, and Clock Overflow. These tests have a special starting address. Since end-passes are immediate, no 'END of Pass' message is reported. Errors are reported by typing out the PC where the error was detected. When started, the program remains in a loop generating and detecting the specified signals. HALT ON ERROR and INHIBIT ERROR timeout options may be used.

Logic test must have already been run on the KVV11.

8.7.1 I/O Signal Test #1 ST1 IN, ST2 OUT

Switch pack S2 must be set up as follows:

SWITCH STATE

1 OFF
2 ON
3 OFF
4 OFF
5 ON
6 ON
7 not used

The following jumper must be installed.

J1-SS (ST2 out) to J1-VV (ST1 in)

Load and start the program at 210.

8.7.2 I/O Signal Test #2 Clock Overflow Test

Switch pack S2 must be set up as follows:

SWITCH STATE

1 OFF
2 OFF
3 OFF
4 ON
5 OFF
6 ON
7 not used

The following jumper must be installed.

J1-RR (clock overflow) to J1-TT (ST2 in)

Load and start at location 214.

8.7.3 I/O Signal Test #3 ST1 out and ST2 in
Switch Pack S2 must be set up as follows:

SWITCH STATE

- 1 OFF
- 2 OFF
- 3 OFF
- 4 ON
- 5 ON
- 6 ON
- 7 not used

The following jumper must be installed:

J1-UU (ST1 out) to J1-TT (ST2 in)

Load and start at location 220.

8.8 Production Starting Address

A special starting address has been provided for In-house production to use to start the logic diagnostic and inform the test that production is using it.

In the field only enough addresses were allotted for 4 sequential KWV11s. When the logic tests are started at location 200, we only auto-size up to 4 KWV11s.

In house testing may wish to exercise up to 16 KWV11s at one time. The logic tests may be started at location 230 and the program will auto size up to 16 KWV11s.

8.9 Testor Starting Address

A special starting address has been provided for manufacturing to use to start the logic diagnostic and inform the program that the clock module is cabled to an in-house testor.

Manual intervention is needed in this sequence of testing. The program will type out all instructions. A cable should connect J1 on the clock module to J10 on the testor. Switches 1 and 3 of S2 (on the clock module) should be on, all other switches on S2 should be off.

8.10 Trap Catcher

The Trap Catcher in this diagnostic employs a new concept. This concept will enable the user of this diagnostic to gain more knowledge of the events that lead the program to this area.

The Trap Catch consists of PC+2 and JSR PC,R0. (i.e., Location 300 would contain 302 and location 302 would contain 4700.)

When a device interrupts unexpectedly to the Trap Catcher, it would pick up the PC+2 of the trap as an address of the interrupt service routine.

The program would then pick up '4700' as the new PSW. Bit 7 of the new PSW having been set, would cause further interrupts from happening. When the CPU attempts to execute '4700' (JSR PC,R0), a Bus-time-out trap will occur to location 4. Location 4 contains a pointer to 'IOTRD', a routine that will report the trap as an error.

To guard against 'Real' Bus errors routing us through location 4 to 'IOTRD', we check to see if the trap that brought us to location 4 really came from the Trap Catcher area. If not we'll halt and leave the Trap Address in 'TRTO'.

More about the interrupt error can be found in the description of the error in the program listing in the routine 'IOTRD'.

56	OPERATIONAL SWITCH SETTINGS
58	TRAP CATCHER
100	BASIC DEFINITIONS
109	ACT11 HOOKS
111	APT PARAMETER BLOCK
112	COMMON TAGS
(2)	APT MAILBOX-ETABLE
(1)	ERROR POINTER TABLE
225	INITIALIZE THE COMMON TAGS
234	TYPE PROGRAM NAME
(2)	GET VALUE FOR SOFTWARE SWITCH REGISTER
294	T1 *TEST THE ADDRESSABILITY OF CLOCK CSR
295	T2 *TEST THE ADDRESSABILITY OF CLOCK BUFFER REG.
342	T3 *TEST THAT CLOCK A STATUS REGISTER BIT 14 CAN BE SET AND CLEARED
343	T4 *TEST THAT CLOCK A STATUS REGISTER BIT 13 CAN BE SET AND CLEARED
344	T5 *TEST THAT CLOCK A STATUS REGISTER BIT 11 CAN BE SET AND CLEARED
345	T6 *TEST THAT CLOCK A STATUS REGISTER BIT 6 CAN BE SET AND CLEARED
346	T7 *TEST THAT CLOCK A STATUS REGISTER BIT 5 CAN BE SET AND CLEARED
347	T10 *TEST THAT CLOCK A STATUS REGISTER BIT 4 CAN BE SET AND CLEARED
348	T11 *TEST THAT CLOCK A STATUS REGISTER BIT 3 CAN BE SET AND CLEARED
349	T12 *TEST THAT CLOCK A STATUS REGISTER BIT 2 CAN BE SET AND CLEARED
350	T13 *TEST THAT CLOCK A STATUS REGISTER BIT 1 CAN BE SET AND CLEARED
351	T14 *TEST THAT CLOCK A STATUS REGISTER BIT 0 CAN BE SET AND CLEARED
385	T15 *TEST THAT PATTERN 125252 WILL SET AND CLEAR IN BUFFER REG.
387	T16 *TEST THAT PATTERN 052525 WILL SET AND CLEAR IN BUFFER REG.
390	*
391	* PHASE 2 ADVANCED BASIC LOGIC TESTS
392	*
404	T17 *TEST THE LOW BYTE OPERATION OF CLOCK'S STATUS REGISTER
430	T20 *TEST THE HIGH BYTE OPERATION OF A'S STATUS REGISTER
460	T21 *TEST CLOCK'S COUNT REGISTER WITH 125252 PATTERN
486	T22 *TEST CLOCKS COUNTER REGISTER WITH 052525 PATTERN
519	T23 *TEST THAT INIT CLEARS STATUS REGISTER
556	T24 *TEST THAT INIT CLEARS BUFFER REGISTER
578	T25 *TEST THE SETTING OF MAINTENANCE ST2 IN CLOCK BIT 15 TO SET
603	T26 *TEST THAT BIT00 IN CLOCK STATUS REG. WILL SET WHEN BIT13 AND MAIN. ST2
618	*
619	*PHASE 3 COUNT TESTS
620	*
623	T27 *TEST TO SEE IF THE COUNTER WILL INCREMENT
647	T30 *SEE IF CLOCK WILL COUNT UP FROM A ZERO BASE, RATE:ST1
683	T31 *TEST THAT OVERFLOW (CSR BIT07) WILL SET ON OVERFLOW
720	T32 *TEST THAT OVERFLOW WILL CLEAR THE GO BIT
741	T33 *TEST THAT GO BIT DOES NOT CLEAR ON OVERFLOW, IF MODE 1
806	T34 *TEST THE ABILITY OF CLOCK TO COUNT AT 1MHZ RATE
808	T35 *TEST THE ABILITY OF CLOCK TO COUNT AT 100KHZ RATE
810	T36 *TEST THE ABILITY OF CLOCK TO COUNT AT 10KHZ RATE
812	T37 *TEST THE ABILITY OF CLOCK TO COUNT AT 1KHZ RATE
814	T40 *TEST THE ABILITY OF CLOCK TO COUNT AT 100HZ RATE
816	T41 *TEST THE ABILITY OF CLOCK TO COUNT AT LINEFREQ RATE
819	T42 *TEST THAT COUNTER DOESN'T COUNT WHEN 'SLAVE IN' RATE IS SELECTED
845	T43 *TEST THAT THE CLOCK WILL COUNT IN MODE 1
864	*
865	*PHASE 4 CLOCK INTERRUPT TEST.
866	*
876	T44 *TEST THAT THE CLOCK WILL INTERRUPT ON OVERFLOW

897	T45	*TEST THAT ST2 WILL CAUSE AN INTERRUPT
916	*	
917	*PHASE 5 ADVANCED TESTING	
918	*	
1000	T46	*TEST THAT THE 'FOR' BIT WILL SET ON 2 ST2'S
1018	T47	*TEST THAT FOR BIT WILL SET ON TWO OVERFLOWS
1038	T50	*TEST THAT FOR BIT WILL CLEAR IF GO BIT IS SET
1060	T51	*TEST THAT WE CAN DISABLE THE INTERNAL OSC
1079	T52	*TEST THAT CLOCK CAN BE COUNTED USING MAINTENANCE OSC
1172	T53	*TEST THE CLOCK'S 1MHZ DIVIDER
1173	T54	*TEST THE CLOCK'S 100KHZ DIVIDER
1174	T55	*TEST THE CLOCK'S 10KHZ DIVIDER
1176	T56	*TEST THE CLOCK'S 1KHZ DIVIDER
1177	T57	*TEST THE CLOCK'S 100HZ DIVIDER
1198	T60	*TEST THE CLOCK'S MODE 2 OPERATION
1238	T61	*TEST THE CLOCK'S MODE 3 OPERATION
1278	T62	*IF ENABLED,CHECK THRESHOLD ST1 FROM TESTOR
1312	T63	*IF ENABLED, CHECK ST1,ST2 IN FROM TESTOR
1410	END OF PASS ROUTINE	
1446		:I/O SIGNAL TEST #1 ST1 IN AND ST2 OUT IN AND OUT
1474		:I/O SIGNAL TEST #2 CLOCK OVFLOW OUT TEST.
1502		:I/O SIGNAL TEST #3 ST1 OUT AND ST2 IN
1542		
1543	*SYSMAC ROUTINES	
1544		
1546	BINARY TO OCTAL (ASCII) AND TYPE	
1547	BINARY TO ASCII AND TYPE ROUTINE	
1560	ERROR HANDLER ROUTINE	
1561	ERROR MESSAGE TYPEOUT ROUTINE	
1562	SCOPE HANDLER ROUTINE	
1563	TTY INPUT ROUTINE	
1564	TYPE ROUTINE	
1565	APT COMMUNICATIONS ROUTINE	
1566	POWER DOWN AND UP ROUTINES	
1635	TRAP DECODER	
(3)	TRAP TABLE	

1
2
3
4
9
10
11
23
27
36
52
53
54
(1)
(1)
(1)
(1)
(1)
(1)
(1)
(1)
(1)
55
56
(1)
(1)
(1)
(1)
(1)
(1)
(1)
(1)
57
58
59
60
61
62
63
64
65
75
76
77
78
79
80
81
82
83
84
85
86
87

167400

000001

000000

000004 017102 000200

000174 000000

000176 000000

000100 000104 000200 000002

000200 000137 001506
 000204 000137 001444

```

.NLIST MC,MD,CND
.LIST ME
.ENABL ABS
.ENABL AMA
$SWR= 167400

.TITLE KWV11A DISAGNOSTIC MAINDEC-11-CVKWA-C
;*COPYRIGHT (C) 1979
;*DIGITAL EQUIPMENT CORP.
;*MAYNARD, MASS. 01754
;*
;*
;*THIS PROGRAM WAS ASSEMBLED USING THE PDP-11 MAINDEC SYSMAC
;*PACKAGE (MAINDEC-11-DZQAC-C3), JAN 19, 1977.
;*
$TN=1

.SBTTL OPERATIONAL SWITCH SETTINGS
;*
;* SWITCH USE
;* -----
;* 15 HALT ON ERROR
;* 14 LOOP ON TEST
;* 13 INHIBIT ERROR TYPEOUTS
;* 11 INHIBIT ITERATIONS
;* 10 BELL ON ERROR
;* 9 LOOP ON ERROR
;* 8 LOOP ON TEST IN SWR<7:0>

.SBTTL TRAP CATCHER
.=0
;*ALL UNUSED LOCATIONS FROM 4-776 CONTAIN A ".+2"
;*AND "JSR PC,R0" SEQUENCE TO CATCH ILLEGAL INTERRUPTS.
;*AND INTERRUPTS TO THE WRONG VECTOR.
;*LOCATION 0 CONTAINS A 0 TO CATCH IMPROPERLY LOADED
;*VECTORS.
.=4
.WORD IOTRD,200 ;HANDLE BUSS ERROR.
.=174
DISPREG: .WORD 0 ;;SOFTWARE DISPLAY REGISTER.
SWREG: .WORD 0 ;;SOFTWARE SWITCH REGISTER.
.=100
.WORD 104,200,2 ;IF 'B EVENT' ON Q-BUS IS
;CONNECTED,WE NEED A WAY OF
;IGNORING ITS INTERRUPTS.

.=200
JMP @#START
JMP @#QSTART

```

```
88 000210 000137 014046      JMP    @#OITST1
89 000214 000137 014136      JMP    @#OITST2
90 000220 000137 014216      JMP    @#OITST3
91
92                000230      .=230
93 000230 000137 001472      JMP    @#WSTART      ;WESTFIELD STARTING ADDRESS
94                000240      .=240
95 000240 000137 001456      JMP    @#TSTSTR      ;ALL TESTER TESTS
96                                     ;IF STARTED HERE.
97                                     ;ALLOWS PRODUCTION TO EXERCISE
98                                     ;UP TO 16 CLOCKS.NORMAL=4.
99
```

```
100 .SBTTL BASIC DEFINITIONS
(1)
(1) ;*INITIAL ADDRESS OF THE STACK POINTER *** 1100 ***
(1) 001100 STACK= 1100
(1) .EQUIV EMT,ERROR      ;;BASIC DEFINITION OF ERROR CALL
(1) .EQUIV IOT,SCOPE     ;;BASIC DEFINITION OF SCOPE CALL
(1)
(1) ;*MISCELLANEOUS DEFINITIONS
(1) 000011 HT= 11      ;;CODE FOR HORIZONTAL TAB
(1) 000012 LF= 12      ;;CODE FOR LINE FEED
(1) 000015 CR= 15      ;;CODE FOR CARRIAGE RETURN
(1) 000200 CRLF= 200   ;;CODE FOR CARRIAGE RETURN-LINE FEED
(1) 177776 PS= 177776  ;;PROCESSOR STATUS WORD
(1) .EQUIV PS,PSW
(1) 177774 STKLMT= 177774 ;;STACK LIMIT REGISTER
(1) 177772 PIRQ= 177772 ;;PROGRAM INTERRUPT REQUEST REGISTER
(1) 177570 DSWR= 177570 ;;HARDWARE SWITCH REGISTER
(1) 177570 DDISP= 177570 ;;HARDWARE DISPLAY REGISTER
(1)
(1) ;*GENERAL PURPOSE REGISTER DEFINITIONS
(1) 000000 R0= %0      ;;GENERAL REGISTER
(1) 000001 R1= %1      ;;GENERAL REGISTER
(1) 000002 R2= %2      ;;GENERAL REGISTER
(1) 000003 R3= %3      ;;GENERAL REGISTER
(1) 000004 R4= %4      ;;GENERAL REGISTER
(1) 000005 R5= %5      ;;GENERAL REGISTER
(1) 000006 R6= %6      ;;GENERAL REGISTER
(1) 000007 R7= %7      ;;GENERAL REGISTER
(1) 000006 SP= %6      ;;STACK POINTER
(1) 000007 PC= %7      ;;PROGRAM COUNTER
(1)
(1) ;*PRIORITY LEVEL DEFINITIONS
(1) 000000 PR0= 0      ;;PRIORITY LEVEL 0
(1) 000040 PR1= 40     ;;PRIORITY LEVEL 1
(1) 000100 PR2= 100    ;;PRIORITY LEVEL 2
(1) 000140 PR3= 140    ;;PRIORITY LEVEL 3
(1) 000200 PR4= 200    ;;PRIORITY LEVEL 4
(1) 000240 PR5= 240    ;;PRIORITY LEVEL 5
(1) 000300 PR6= 300    ;;PRIORITY LEVEL 6
(1) 000340 PR7= 340    ;;PRIORITY LEVEL 7
(1)
(1) ;*'SWITCH REGISTER' SWITCH DEFINITIONS
(1) 100000 SW15= 100000
(1) 040000 SW14= 40000
```

(1)	020000	SW13=	20000
(1)	010000	SW12=	10000
(1)	004000	SW11=	4000
(1)	002000	SW10=	2000
(1)	001000	SW09=	1000
(1)	000400	SW08=	400
(1)	000200	SW07=	200
(1)	000100	SW06=	100
(1)	000040	SW05=	40
(1)	000020	SW04=	20
(1)	000010	SW03=	10
(1)	000004	SW02=	4
(1)	000002	SW01=	2
(1)	000001	SW00=	1
(1)		.EQUIV	SW09,SW9
(1)		.EQUIV	SW08,SW8
(1)		.EQUIV	SW07,SW7
(1)		.EQUIV	SW06,SW6
(1)		.EQUIV	SW05,SW5
(1)		.EQUIV	SW04,SW4
(1)		.EQUIV	SW03,SW3
(1)		.EQUIV	SW02,SW2
(1)		.EQUIV	SW01,SW1
(1)		.EQUIV	SW00,SW0

.*DATA BIT DEFINITIONS (BIT00 TO BIT15)

(1)	100000	BIT15=	100000
(1)	040000	BIT14=	40000
(1)	020000	BIT13=	20000
(1)	010000	BIT12=	10000
(1)	004000	BIT11=	4000
(1)	002000	BIT10=	2000
(1)	001000	BIT09=	1000
(1)	000400	BIT08=	400
(1)	000200	BIT07=	200
(1)	000100	BIT06=	100
(1)	000040	BIT05=	40
(1)	000020	BIT04=	20
(1)	000010	BIT03=	10
(1)	000004	BIT02=	4
(1)	000002	BIT01=	2
(1)	000001	BIT00=	1
(1)		.EQUIV	BIT09,BIT9
(1)		.EQUIV	BIT08,BIT8
(1)		.EQUIV	BIT07,BIT7
(1)		.EQUIV	BIT06,BIT6
(1)		.EQUIV	BIT05,BIT5
(1)		.EQUIV	BIT04,BIT4
(1)		.EQUIV	BIT03,BIT3
(1)		.EQUIV	BIT02,BIT2
(1)		.EQUIV	BIT01,BIT1
(1)		.EQUIV	BIT00,BIT0

.*BASIC "CPU" TRAP VECTOR ADDRESSES

(1)	000004	ERRVEC=	4	::TIME OUT AND OTHER ERRORS
(1)	000010	RESVEC=	10	::RESERVED AND ILLEGAL INSTRUCTIONS

(1)	000014	TBITVEC=14	:: 'T' BIT
(1)	000014	TRTVEC= 14	:: TRACE TRAP
(1)	000014	BPTVEC= 14	:: BREAKPOINT TRAP (BPT)
(1)	000020	IOTVEC= 20	:: INPUT/OUTPUT TRAP (IOT) **SCOPE**
(1)	000024	PWRVEC= 24	:: POWER FAIL
(1)	000030	EMTVEC= 30	:: EMULATOR TRAP (EMT) **ERROR**
(1)	000034	TRAPVEC=34	:: 'TRAP' TRAP
(1)	000060	TKVEC= 60	:: TTY KEYBOARD VECTOR
(1)	000064	TPVEC= 64	:: TTY PRINTER VECTOR
(1)	000240	PIRQVEC=240	:: PROGRAM INTERRUPT REQUEST VECTOR

101			
102	170420	ABASE=	170420
103	000440	AVECT1=	440
104	000200	APRIOR=	200
105			
106	167400	\$SWR=	167400
107	000001	\$TN=	1
108			
109			

.SBTTL ACT11 HOOKS

```
*****
:HOOKS REQUIRED BY ACT11
(1) 000244 $SVPC= ;SAVE PC
(1) 000046 .=46
(1) 000046 013720 $ENDAD ;;1)SET LOC.46 TO ADDRESS OF $ENDAD IN .$EOP
(1) 000052 000052 .=52
(1) 000052 000000 .WORD 0 ;;2)SET LOC.52 TO ZERO
(1) 000244 .=$SVPC ;; RESTORE PC
110 001000 .=1000
```

.SBTTL APT PARAMETER BLOCK

```
*****
:SET LOCATIONS 24 AND 44 AS REQUIRED FOR APT
:*****
(1) 001000 .SX= ;;SAVE CURRENT LOCATION
(1) 000024 .=24 ;;SET POWER FAIL TO POINT TO START OF PROGRAM
(1) 000024 000200 200 ;;FOR APT START UP
(1) 000044 .=44 ;;POINT TO APT INDIRECT ADDRESS PNTR.
(1) 000044 001000 $APTHDR ;;POINT TO APT HEADER BLOCK
(1) 001000 .=$X ;;RESET LOCATION COUNTER
```

```
*****
:SETUP APT PARAMETER BLOCK AS DEFINED IN THE APT-PDP11 DIAGNOSTIC
:INTERFACE SPEC.
```

(1)	001000	\$APTHD:	
(1)	001000	\$HIBTS:	.WORD 0 ;;TWO HIGH BITS OF 18 BIT MAILBOX ADDR.
(1)	001002	\$MBADR:	.WORD \$MAIL ;;ADDRESS OF APT MAILBOX (BITS 0-15)
(1)	001004	\$STMT:	.WORD 2 ;;RUN TIM OF LONGEST TEST
(1)	001006	\$PASTM:	.WORD 120. ;;RUN TIME IN SECS. OF 1ST PASS ON 1 UNIT (QUICK VERIFY)
(1)	001010	\$UNITM:	.WORD 120. ;;ADDITIONAL RUN TIME (SECS) OF A PASS FOR EACH ADDITIONAL UNIT
(1)	001012		.WORD \$ETEND-\$MAIL/2 ;;LENGTH MAILBOX-ETABLE(WORDS)


```
(2) 001212 000000 $MSGLG: .WORD  AMISGLG  ;;MESSAGE LENGTH
(2) 001214          $ETABLE:          ;;APT ENVIRONMENT TABLE
(2) 001214 000      $ENV: .BYTE   AENV      ;;ENVIRONMENT BYTE
(2) 001215 000      $ENVM: .BYTE  AENVM     ;;ENVIRONMENT MODE BITS
(2) 001216 000000  $SWREG: .WORD  ASWREG   ;;APT SWITCH REGISTER
(2) 001220 000000  $USWR: .WORD  AUSWR    ;;USER SWITCHES
(2) 001222 000000  $CPUOP: .WORD  ACPUOP   ;;CPU TYPE,OPTIONS
(2)                :*          BITS 15-11=CPU TYPE
(2)                :*          11/04=01,11/05=02,11/20=03,11/40=04,11/45=05
(2)                :*          11/70=06,PDQ=07,Q=10
(2)                :*          BIT 10=REAL TIME CLOCK
(2)                :*          BIT 9=FLOATING POINT PROCESSOR
(2)                :*          BIT 8=MEMORY MANAGEMENT
(2) 001224 000      $MAMS1: .BYTE  AMAMS1  ;;HIGH ADDRESS,M.S. BYTE
(2) 001225 000      $MTYP1: .BYTE  AMTYP1  ;;MEM. TYPE,BLK#1
(2)                :*          MEM.TYPE BYTE -- (HIGH BYTE)
(2)                :*          900 NSEC CORE=001
(2)                :*          300 NSEC BIPOLAR=002
(2)                :*          500 NSEC MOS=003
(2) 001226 000000  $MADR1: .WORD  AMADR1  ;;HIGH ADDRESS,BLK#1
(2)                :*          MEM.LAST ADDR.=3 BYTES,THIS WORD AND LOW OF 'TYPE' ABOVE
(2) 001230 000      $MAMS2: .BYTE  AMAMS2  ;;HIGH ADDRESS,M.S. BYTE
(2) 001231 000      $MTYP2: .BYTE  AMTYP2  ;;MEM. TYPE,BLK#2
(2) 001232 000000  $MADR2: .WORD  AMADR2  ;;MEM.LAST ADDRESS,BLK#2
(2) 001234 000      $MAMS3: .BYTE  AMAMS3  ;;HIGH ADDRESS,M.S.BYTE
(2) 001235 000      $MTYP3: .BYTE  AMTYP3  ;;MEM. TYPE,BLK#3
(2) 001236 000000  $MADR3: .WORD  AMADR3  ;;MEM.LAST ADDRESS,BLK#3
(2) 001240 000      $MAMS4: .BYTE  AMAMS4  ;;HIGH ADDRESS,M.S.BYTE
(2) 001241 000      $MTYP4: .BYTE  AMTYP4  ;;MEM. TYPE,BLK#4
(2) 001242 000000  $MADR4: .WORD  AMADR4  ;;MEM.LAST ADDRESS,BLK#4
(2) 001244 000440  $VECT1: .WORD  AVECT1  ;;INTERRUPT VECTOR#1,BUS PRIORITY#1
(2) 001246 000000  $VECT2: .WORD  AVECT2  ;;INTERRUPT VECTOR#2BUS PRIORITY#2
(2) 001250 170420  $BASE: .WORD  ABASE   ;;BASE ADDRESS OF EQUIPMENT UNDER TEST
(2) 001252 000000  $DEVM: .WORD  ADEVM   ;;DEVICE MAP
(2) 001254 000000  $CDW1: .WORD  ACDW1   ;;CONTROLLER DESCRIPTION WORD#1
(2) 001256          $ETEND:
(2)                .MEXIT
```

```
(1) .SBTTL ERROR POINTER TABLE
(1)
(1) ;*THIS TABLE CONTAINS THE INFORMATION FOR EACH ERROR THAT CAN OCCUR.
(1) ;*THE INFORMATION IS OBTAINED BY USING THE INDEX NUMBER FOUND IN
(1) ;*LOCATION $ITEMB. THIS NUMBER INDICATES WHICH ITEM IN THE TABLE IS PERTINENT.
(1) ;*NOTE1: IF $ITEMB IS 0 THE ONLY PERTINENT DATA IS ($ERRPC).
(1) ;*NOTE2: EACH ITEM IN THE TABLE CONTAINS 4 POINTERS EXPLAINED AS FOLLOWS:
(1)
(1) ;* EM ;:POINTS TO THE ERROR MESSAGE
(1) ;* DH ;:POINTS TO THE DATA HEADER
(1) ;* DT ;:POINTS TO THE DATA
(1) ;* DF ;:POINTS TO THE DATA FORMAT
```

```
(1) 001256 $ERRTB:
113
118
119 ;ITEM 1
120
121 001256 017232 EM1 ;CLOCK SR FUNCTION ERROR
122 001260 017555 DH1 ;ERRPC ASR WAS S/B
123 001262 017764 DT1 ;$ERRPC,ASR,$BDDAT,$GDDAT
124 001264 020062 DF0 ;ALL NUMBERS ARE IN OCTAL FORM
```

```
125
126 ;ITEM 2
127
128 001266 017264 EM2 ;CLOCK SR DATA ERROR
129 001270 017555 DH1 ;ERRPC ASR WAS S/B
130 001272 017764 DT1 ;$ERRPC,ASR,$BDDAT,$GDDAT
131 001274 020062 DF0 ;ALL NUMBERS ARE IN OCTAL FORM
```

```
132
133 ;ITEM 3
134
135 001276 017312 EM3 ;CLOCK BR DATA ERROR
136 001300 017601 DH3 ;ERRPC ABR WAS
137 001302 017776 DT3 ;$ERRPC,ABR,$BDDAT,$GDDAT
138 001304 020062 DF0 ;ALL NUMBERS ARE IN OCTAL FORM
```

```
139
140 ;ITEM 4
141
142 001306 017340 EM4 ;INTERRUPT ERROR.
143 001310 017625 DH4A ;ERRPC TO ROM ADDR.
144 001312 020010 DT4 ;$ERRPC, TRTO,TRFRO
145 001314 020062 DF0 ;ALL NUMBERS ARE IN OCTAL FORM
```

```
146
147 ;ITEM 5
148
149 001316 017361 EM5 ;CLOCK COUNT REG ERROR
150 001320 017555 DH1 ;ERRPC ASR WAS S/B
151 001322 017764 DT1 ;$ERRPC,ACR,$BDDAT,$GDDAT
152 001324 020062 DF0 ;ALL NUMBERS ARE IN OCTAL FORM
(1)
```

153					
154			:ITEM	6	
155					
156	001326	017423		EM12	:CLOCK COUNT FUNCTION ERROR
157	001330	017661		DH12	:ERRPC ASR
158	001332	020020		DT12	:ERRPC, ASR
159	001334	020062		DF0	:ALL NUMBERS ARE IN OCTAL FORM
(1)					
160					
161			:ITEM	7	
162					
163	001336	017452		EM16	:CLOCK INTERRUPT ERROR
164	001340	017661		DH12	:ERRPC ASR
165	001342	020020		DT12	:SERRPC, ASR
166	001344	020062		DF0	:ALL NUMBERS ARE IN OCTAL FORM
(1)					
167					
168			:ITEM	10	
169					
170	001346	017503		EM20	:CLOCK REPEATABILITY ERROR
171	001350	017676		DH20	:ERROR ASR 2ND CNT 1ST CNT 3RD CNT
172	001352	020026		DT20	:SERRPC, ASR, \$BDDAT, \$GDDAT, \$TMP0
173	001354	020062		DF0	:ALL NUMBERS ARE IN OCTAL FORM
(1)					
174					
175			:ITEM	11	
176					
177	001356	017404		EM11	:CLOCK COUNT ERROR
178	001360	017555		DH1	:ERRPC ASR WAS S/B
179	001362	020042		DT22	:SERRPC, ASR, \$BDDAT, \$TMP0
180	001364	020062		DF0	:ALL NUMBERS ARE IN OCTAL FORM
(1)					
181					
182			:ITEM	12	
183					
184	001366	017532		EM26	:CLOCK ADDRESSING ERROR
185	001370	017737		DH26	:ERRPC CLOCK ADDR.
186	001372	020054		DT26	:SERRPC, \$TMP0
187	001374	020062		DF0	:ALL NUMBERS ARE IN OCTAL FORM
(1)					
188					
189	001376	170420	ASR:	.WORD	ABASE
190	001400	170422	ABR:	.WORD	ABASE+2
191	001402	000440	VECT1:	.WORD	AVECT1
192	001404	000442	VECTP:	.WORD	AVECT1+2
193	001406	000444	VECT2:	.WORD	AVECT1+4
194	001410	000446	VECT2P:	.WORD	AVECT1+6
195	001412	000200	PRIOR:	.WORD	APRIOR
196	001414	167774	DR:	.WORD	167774
197	001416	167772	DR2:	.WORD	167772
198	001420	000000	\$TMP0:	.WORD	0
199	001422	000000	\$TMP1:	.WORD	0
200	001424	000000	\$TMP3:	.WORD	0
201	001426	000000	ROTATE:	.WORD	0
202	001430	000000	UTEST:	.WORD	0
203	001432	000000	ERCNT:	.WORD	0

:VECTOR ADDR. OF ST2 INTRS.

:TEMP STORAGE.
 :TMP STORAGE.

:POINT TO DEVICE UNDER TEST.
 :KEEPS TRACK OF GOOD UNITS.
 :COUNTS ERRORS.

204	001434	000000			MDEVCT: .WORD	0		:COUNTS DEVICES TESTED.
205	001436	000000			TSTCNT: .WORD	0		:MAX DEVICES TO BE TESTED.
206	001440	000000			EXS: .WORD	0		: =0, NORMAL: =1 SPECIAL TESTOR START, BY L+S @ 2
207	001442	000000			LCNT: .WORD	0		:TOTAL UNITS TESTED.
208								
209								
211	001444	012737	002144	001420	QSTART: MOV	#RSTART,\$TMP0		:LOAD SETUP RETURN ADDRESS
212	001452	000137	001526		JMP	INIT		:INIT THE PROGRAM VECTOR SPACE
213								
214	001456	005237	001440		TSTSTR: INC	EXS		:SET FOR TESTOR.
215	001462	012737	000020	001436	MOV	#16.,TSTCNT		:ALLOW 16 UNITS
216	001470	000413			BR	1\$		
217		001472			WSTART=.			
218	001472	012737	000020	001436	MOV	#16.,TSTCNT		:TEST UP TO 16 UNITS.
219	001500	005037	001440		CLR	EXS		
220	001504	000405			BR	1\$		
221		001506			START=.			
222	001506	012737	000004	001436	MOV	#4,TSTCNT		:TEST UP TO FOUR UNITS.
223	001514	005037	001440		CLR	EXS		
224	001520	012737	001774	001420	1\$: MOV	#ZSTART,\$TMP0		:LOAD SETUP RETURN
225	001526				INIT:			
(1)					.SBTTL	INITIALIZE THE COMMON TAGS		
(1)					::CLEAR	THE COMMON TAGS (\$CMTAG) AREA		
(1)	001526	012706	001100		MOV	#SCMTAG,R6		::FIRST LOCATION TO BE CLEARED
(1)	001532	005026			CLR	(R6)+		::CLEAR MEMORY LOCATION
(1)	001534	022706	001140		CMP	#SWR,R6		::DONE?
(1)	001540	001374			BNE	.-6		::LOOP BACK IF NO
(1)	001542	012706	001100		MOV	#STACK,SP		::SETUP THE STACK POINTER
(1)					::INITIALIZE	A FEW VECTORS		
(1)	001546	012737	015136	000020	MOV	#\$SCOPE,@#IOTVEC		::IOT VECTOR FOR SCOPE ROUTINE
(1)	001554	012737	000340	000022	MOV	#340,@#IOTVEC+2		::LEVEL 7
(1)	001562	012737	014574	000030	MOV	#\$ERROR,@#EMTVEC		::EMT VECTOR FOR ERROR ROUTINE
(1)	001570	012737	000340	000032	MOV	#340,@#EMTVEC+2		::LEVEL 7
(1)	001576	012737	017152	000034	MOV	#\$TRAP,@#TRAPVEC		::TRAP VECTOR FOR TRAP CALLS
(1)	001604	012737	000340	000036	MOV	#340,@#TRAPVEC+2		::LEVEL 7
(1)	001612	012737	016724	000024	MOV	#\$PWRDN,@#PWRVEC		::POWER FAILURE VECTOR
(1)	001620	012737	000340	000026	MOV	#340,@#PWRVEC+2		::LEVEL 7
(1)	001626	005037	001160		CLR	\$TIMES		::INITIALIZE NUMBER OF ITERATIONS
(1)	001632	005037	001162		CLR	\$ESCAPE		::CLEAR THE ESCAPE ON ERROR ADDRESS
(1)	001636	112737	000001	001115	MOVB	#1,\$ERMAX		::ALLOW ONE ERROR PER TEST
(1)	001644	012737	001644	001106	MOV	#.,\$LPADR		::INITIALIZE THE LOOP ADDRESS FOR SCOPE
(1)	001652	012737	001652	001110	MOV	#.,\$LPERR		::SETUP THE ERROR LOOP ADDRESS
(2)					::SIZE	FOR A HARDWARE SWITCH REGISTER. IF NOT FOUND OR IT IS		
(2)					::EQUAL	TO A "-1", SETUP FOR A SOFTWARE SWITCH REGISTER.		
(2)	001660	013746	000004		MOV	@#ERRVEC,-(SP)		::SAVE ERROR VECTOR
(2)	001664	012737	001720	000004	MOV	#64,@#ERRVEC		::SET UP ERROR VECTOR
(2)	001672	012737	177570	001140	MOV	#DSWR,SWR		::SETUP FOR A HARDWARE SWICH REGISTER
(2)	001700	012737	177570	001142	MOV	#DDISP,DISPLAY		::AND A HARDWARE DISPLAY REGISTER
(2)	001706	022777	177777	177224	CMP	#-1,@SWR		::TRY TO REFERENCE HARDWARE SWR
(2)	001714	001012			BNE	66\$::BRANCH IF NO TIMEOUT TRAP OCCURRED
(2)								::AND THE HARDWARE SWR IS NOT = -1
(2)	001716	000403			BR	65\$::BRANCH IF NO TIMEOUT
(2)	001720	012716	001726		64\$: MOV	#65\$,(SP)		::SET UP FOR TRAP RETURN
(2)	001724	000002			RTI			
(2)	001726	012737	000176	001140	65\$: MOV	#SWREG,SWR		::POINT TO SOFTWARE SWR
(2)	001734	012737	000174	001142	MOV	#DISPREG,DISPLAY		

```

(2) 001742 012637 000004      66$:  MOV      (SP)+,@#ERRVEC  ;;RESTORE ERROR VECTOR
(1)
(2) 001746 005037 001202      CLR      $PASS                ;;CLEAR PASS COUNT
(2) 001752 132737 000200 001215  BITB     #APTSIZE,$ENVM       ;;TEST USER SIZE UNDER APT
(2) 001760 001403                BEQ      67$                  ;;YES,USE NON-APT SWITCH
(2) 001762 012737 001216 001140  MOV      #$$SWREG,$SWR       ;;NO,USE APT SWITCH REGISTER
(2) 001770
226 001770 000177 177424      67$:  JMP      @ $TMP0              ;EXIT PROGRAM VECTOR SETUP SPACE
227
228 001774
(1)
(1) 001774 012746 000340      MOV      #340,-(SP)           ;SET CPU PRIORITY ON RETERN.
(1) 002000 012746 002006      MOV      #64$,-(SP)          ;SHOW RETURN ADDRESS.
(1) 002004 000002                RTI                          ;CAUSE A RETURN(PUTS STATUS IN STATUS REG.).
(1) 002006      64$:
229 002006 005037 001204      CLR      $DEVCT              ;ZERO DEVICE COUNT.
230 002012 012737 017102 000004  MOV      #IOTRD,@#ERRVEC     ;FIX TRAP CATCHER.
231 002020 013737 001244 001402  MOV      $VECT1,VECT1        ;NOW FIX VECTOR ADDR.
232 002026 013737 001250 001376  MOV      $BASE,ASR           ;FIX ADDRESS OF CSR.
233
234      .SBTTL  TYPE PROGRAM NAME
(1)      ;;TYPE THE NAME OF THE PROGRAM IF FIRST PASS
(1) 002034 005227 177777      INC      #-1                  ;;FIRST TIME?
(1) 002040 001041                BNE     65$                   ;;BRANCH IF NO
(1) 002042 104401 002110      TYPE     ,66$                 ;;TYPE ASCIZ STRING
(2)      .SBTTL  GET VALUE FOR SOFTWARE SWITCH REGISTER
(2) 002046 005737 000042      TST     @#42                  ;;ARE WE RUNNING UNDER XXDP/ACT?
(2) 002052 001012                BNE     67$                   ;;BRANCH IF YES
(2) 002054 123727 001214 000001  CMPB    $ENV,#1              ;;ARE WE RUNNING UNDER APT?
(2) 002062 001406                BEQ     67$                   ;;BRANCH IF YES
(2) 002064 023727 001140 000176  CMP     $SWR,#$SWREG         ;;SOFTWARE SWITCH REG SELECTED?
(2) 002072 001005                BNE     68$                   ;;BRANCH IF NO
(2) 002074 104406                GTSWR                          ;;GET SOFT-SWR SETTINGS
(2) 002076 000403                BR      68$
(2) 002100 112737 000001 001134 67$:  MOVB    #1,$AUTOB            ;;SET AUTO-MODE INDICATOR
(2) 002106      68$:
(1) 002106 000416                BR      65$                   ;;GET OVER THE ASCIZ
(1)      ;;66$: .ASCIZ <CRLF>#CVKWAC KWV11 DIAGNOSTIC#<CRLF>
(1) 002144      65$:
235 002144      RSTART:
236 002144 005737 001440      TST     EXS                   ;TESTOR MODE ENABLED??
237 002150 001441                BEQ     1$                    ;NO DON'T TYPE NEXT MESSAGE.
238 002152 104401 002160      TYPE     ,65$                 ;;TYPE ASCIZ STRING
(1) 002156 000436                BR      64$                   ;;GET OVER THE ASCIZ
(1)      ;;65$: .ASCIZ <15><12>#TESTOR MODE ENABLED--SEE DOCUMENTATION FOR INSTRUCTIONS.#
(1) 002254      64$:
239 002254      1$:
(1) 002254 104401 002262      TYPE     ,67$                 ;;TYPE ASCIZ STRING
(1) 002260 000411                BR      66$                   ;;GET OVER THE ASCIZ
(1)      ;;67$: .ASCIZ <15><12>#TEST RUNNING...#
(1) 002304      66$:
240 002304 005037 001434      CLR     MDEVCT                ;TESTING FIRST UNIT.
241 002310 005037 001432      CLR     FRCNT                 ;NO ERRORS.
242 002314 005037 001202      CLR     $PASS                 ;NO PASSES.
243 002320 012737 000001 001426  MOV     #1,ROTATE             ;POINT TO FIRST UNIT.
  
```



```

(1)                               :/ #
(5)                               :*****
(4)                               :*TEST 3          *TEST THAT CLOCK A STATUS REGISTER BIT 14 CAN BE SET AND CLEARED
(5)                               :*
(5)                               :*CLOCK STATUS REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(5)                               :*F/FS OR GATES
(5)                               :*

```

```

(4)                               :*****
(3) 002556 000004 TST3: SCOPE
(2) 002560 012737 000100 001160 MOV #100,$TIMES ;;DO 100 ITERATIONS
(1)                               CLR @ASR ;/CLEAR THE STATUS REGISTER.
(1) 002566 005077 176604 BIS #BIT14,@ASR ;/SET BIT 14.
(1) 002572 052777 040000 176576 MOV #BIT14,$GDDAT ;/SET FOR ERROR TYPEOUT S/B.
(1) 002600 012737 040000 001124 MOV @ASR,$BDDAT ;/READ THE STATUS REGISTER.
(1) 002606 017737 176564 001126 CMP $GDDAT,$BDDAT ;/DID BIT 14 AND ONLY BIT 14 SET?
(1) 002614 023737 001124 001126 BEQ 1$ ;/IF SO-LETS TRY CLEARING IT.
(1) 002622 001402

```

::: \$>>> ERROR <<< \$

```

(1) 002624 104002 ERROR 2 ;/ERROR CLOCK AS STATUS REGISTER
(1)                               ;/BIT 14 FAILED TO BIT SET.
(2)

```

::: \$>>> ERROR <<< \$

```

(1) 002626 000412 BR 2$ ;/BR TO END SUBTEST.
(1)                               1$: BIC #BIT14,@ASR ;/TRY CLEARING BIT 14.
(1) 002630 042777 040000 176540 CLR $GDDAT ;/CLEAR S/B FOR TYPEOUT IF ANY.
(1) 002636 005037 001124 001126 MOV @ASR,$BDDAT ;/NOW READ IT BACK.
(1) 002642 017737 176530 001126 BEQ 2$ ;/IF ZERO - NO ERROR!
(1) 002650 001401

```

::: \$>>> ERROR <<< \$

```

(1) 002652 104002 ERROR 2 ;/ERROR - CLOCK A STATUS REGISTER.
(1)                               ;/BIT 14 FAILED TO CLEAR.
(1)
(2)

```

::: \$>>> ERROR <<< \$

```

(1) 002654 2$:
(1)

```


(1) ;/ #
(5) :*****
(4) *TEST 5 *TEST THAT CLOCK A STATUS REGISTER BIT 11 CAN BE SET AND CLEARED
(5) *
(5) *CLOCK STATUS REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(5) *F/FS OR GATES
(5) *
(5)

(4) :*****
(3) 002752 000004 TST5: SCOPE
(2) 002754 012737 000100 001160 MOV #100,\$TIMES ;:DO 100 ITERATIONS
(1) CLR @ASR ;:/CLEAR THE STATUS REGISTER.
(1) 002762 005077 176410 BIS #BIT11,@ASR ;:/SET BIT 11.
(1) 002766 052777 004000 176402 MOV #BIT11,\$GDDAT ;:/SET FOR ERROR TYPEOUT S/B.
(1) 002774 012737 004000 001124 MOV @ASR,\$BDDAT ;:/READ THE STATUS REGISTER.
(1) 003002 017737 176370 001126 CMP \$GDDAT,\$BDDAT ;:/DID BIT 11 AND ONLY BIT 11 SET?
(1) 003010 023737 001124 001126 BEQ 1\$;:/IF SO-LETS TRY CLEARING IT.
(1) 003016 001402

;: \$>>> ERROR <<< \$

(1) 003020 104002 ERROR 2 ;:/ERROR CLOCK AS STATUS REGISTER
(1) ;:/BIT 11 FAILED TO BIT SET.
(2)

;: \$>>> ERROR <<< \$

(1) 003022 000412 BR 2\$;:/BR TO END SUBTEST.
(1) 003024 0427.7 004000 176344 1\$: BIC #BIT11,@ASR ;:/TRY CLEARING BIT 11.
(1) 003032 005037 001124 CLR \$GDDAT ;:/CLEAR S/B FOR TYPEOUT IF ANY.
(1) 003036 017737 176334 001126 MOV @ASR,\$BDDAT ;:/NOW READ IT BACK.
(1) 003044 001401 BEQ 2\$;:/IF ZERO - NO ERROR!

;: \$>>> ERROR <<< \$

(1) 003046 104002 ERROR 2 ;:/ERROR - CLOCK A STATUS REGISTER.
(1) ;:/BIT 11 FAILED TO CLEAR.
(1)
(2)

;: \$>>> ERROR <<< \$

(1) 003050 2\$:

```
(1)
(5)      :/
(4)      :*****
(5)      :*TEST 6      *TEST THAT CLOCK A STATUS REGISTER BIT 6 CAN BE SET AND CLEARED
(5)      :
(5)      :*CLOCK STATUS REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(5)      :*F/FS OR GATES
(5)      :
(4)      :*****
(3) 003050 000004  IST6:  SCOPE
(2) 003052 012737  000100 001160    MOV      #100,$TIMES      ;;DO 100 ITERATIONS
(1)
(1) 003060 005077  176312      CLR      @ASR           ;/CLEAR THE STATUS REGISTER.
(1) 003064 052777  000100 176304      BIS      #BIT6,@ASR     ;/SET BIT 6.
(1) 003072 012737  000100 001124      MOV      #BIT6,$GDDAT   ;/SET FOR ERROR TYPEOUT S/B.
(1) 003100 017737  176272 001126      MOV      @ASR,$BDDAT   ;/READ THE STATUS REGISTER.
(1) 003106 023737  001124 001126      CMP      $GDDAT,$BDDAT ;/DID BIT 6 AND ONLY BIT 6 SET?
(1) 003114 001402      BEQ      1$           ;/IF SO-LETS TRY CLEARING IT.
(2)
      :;*****
(1) 003116 104002      ERROR 2           ;/ERROR CLOCK AS STATUS REGISTER
(1)                                     ;/BIT 6 FAILED TO BIT SET.
(2)
      :;*****
(1) 003120 000412      BR      2$           ;/BR TO END SUBTEST.
(1)
(1) 003122 042777  000100 176246 1$:  BIC      #BIT6,@ASR     ;/TRY CLEARING BIT 6.
(1) 003130 005037  001124      CLR      $GDDAT        ;/CLEAR S/B FOR TYPEOUT IF ANY.
(1) 003134 017737  176236 001126      MOV      @ASR,$BDDAT   ;/NOW READ IT BACK.
(1) 003142 001401      BEQ      2$           ;/IF ZERO - NO ERROR!
(1)
(2)
      :;*****
(1) 003144 104002      ERROR 2           ;/ERROR - CLOCK A STATUS REGISTER.
(1)                                     ;/BIT 6 FAILED TO CLEAR.
(1)
(2)
      :;*****
(1) 003146      2$:
(1)
346
```

```
(1) :/##
(5) :*****
(4) :*TEST 7 *TEST THAT CLOCK A STATUS REGISTER BIT 5 CAN BE SET AND CLEARED
(5) :*
(5) :*CLOCK STATUS REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(5) :*F/FS OR GATES
(5) :*
```

```
(4) :*****
(3) 003146 000004 TST7: SCOPE
(2) 003150 012737 000100 001160 MOV #100,$TIMES ;;DO 100 ITERATIONS
(1)
(1) 003156 005077 176214 CLR @ASR ;/CLEAR THE STATUS REGISTER.
(1) 003162 052777 000040 176206 BIS #BIT5,@ASR ;/SET BIT 5.
(1) 003170 012737 000040 001124 MOV #BIT5,$GDDAT ;/SET FOR ERROR TYPEOUT S/B.
(1) 003176 017737 176174 001126 MOV @ASR,$BDDAT ;/READ THE STATUS REGISTER.
(1) 003204 023737 001124 001126 CMP $GDDAT,$BDDAT ;/DID BIT 5 AND ONLY BIT 5 SET?
(1) 003212 001402 BEQ 1$ ;/IF SO-LETS TRY CLEARING IT.
(2)
```

;;\$>>> ERROR <<<\$

```
(1) 003214 104002 ERROR 2 ;/ERROR CLOCK AS STATUS REGISTER
(1) ;/BIT 5 FAILED TO BIT SET.
(2)
```

;;\$>>> ERROR <<<\$

```
(1) 003216 000412 BR 2$ ;/BR TO END SUBTEST.
(1)
(1) 003220 042777 000040 176150 1$: BIC #BIT5,@ASR ;/TRY CLEARING BIT 5.
(1) 003226 005037 001124 CLR $GDDAT ;/CLEAR S/B FOR TYPEOUT IF ANY.
(1) 003232 017737 176140 001126 MOV @ASR,$BDDAT ;/NOW READ IT BACK.
(1) 003240 001401 BEQ 2$ ;/IF ZERO - NO ERROR!
(1)
(2)
```

;;\$>>> ERROR <<<\$

```
(1) 003242 104002 ERROR 2 ;/ERROR - CLOCK A STATUS REGISTER.
(1) ;/BIT 5 FAILED TO CLEAR.
(1)
(2)
```

;;\$>>> ERROR <<<\$

```
(1) 003244 2$:
(1)
347
```

(1)
 (5)
 (4)
 (5)
 (5)
 (5)
 (5)
 (4)
 (3)
 (2)
 (1)
 (1)
 (1)
 (1)
 (1)
 (1)
 (1)
 (2)
 (1)
 (1)
 (2)
 (1)
 (1)
 (1)
 (1)
 (1)
 (1)
 (2)
 (1)
 (1)
 (1)
 (2)
 (1)
 (1)
 (1)
 (2)
 (1)
 (1)
 (1)
 (2)
 (1)
 (1)
 348

```

    ;/##
    *****
    *TEST 10 *TEST THAT CLOCK A STATUS REGISTER BIT 4 CAN BE SET AND CLEARED
    *
    *CLOCK STATUS REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
    *F/FS OR GATES
    *
    *****
    TST10: SCOPE
    MOV #100,$TIMES ;;DO 100 ITERATIONS

    CLR @ASR ;/CLEAR THE STATUS REGISTER.
    BIS #BIT4,@ASR ;/SET BIT 4.
    MOV #BIT4,$GDDAT ;/SET FOR ERROR TYPEOUT S/B.
    MOV @ASR,$BDDAT ;/READ THE STATUS REGISTER.
    CMP $GDDAT,$BDDAT ;/DID BIT 4 AND ONLY BIT 4 SET?
    BEQ 1$ ;/IF SO-LETS TRY CLEARING IT.

    *****
    ERROR 2 ;/ERROR CLOCK AS STATUS REGISTER
    ;/BIT 4 FAILED TO BIT SET.

    *****
    BR 2$ ;/BR TO END SUBTEST.

    1$: BIC #BIT4,@ASR ;/TRY CLEARING BIT 4.
    CLR $GDDAT ;/CLEAR S/B FOR TYPEOUT IF ANY.
    MOV @ASR,$BDDAT ;/NOW READ IT BACK.
    BEQ 2$ ;/IF ZERO - NO ERROR!

    *****
    ERROR 2 ;/ERROR - CLOCK A STATUS REGISTER.
    ;/BIT 4 FAILED TO CLEAR.

    *****
    2$:
  
```

```
(1)                                     :/##
(5)                                     :*****
(4) :*TEST 11          *TEST THAT CLOCK A STATUS REGISTER BIT 3 CAN BE SET AND CLEARED
(5) :*
(5) :*CLOCK STATUS REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(5) :*F/FS OR GATES
(5) :*
(4)                                     :*****
(3) 003342 000004 TST11: SCOPE
(2) 003344 012737 000100 001160 MOV #100,$TIMES ;;DO 100 ITERATIONS
(1)
(1) 003352 005077 176020 CLR @ASR ;/CLEAR THE STATUS REGISTER.
(1) 003356 052777 000010 176012 BIS #BIT3,@ASR ;/SET BIT 3.
(1) 003364 012737 000010 001124 MOV #BIT3,$GDDAT ;/SET FOR ERROR TYPEOUT S/B.
(1) 003372 017737 176000 001126 MOV @ASR,$BDDAT ;/READ THE STATUS REGISTER.
(1) 003400 023737 001124 001126 CMP $GDDAT,$BDDAT ;/DID BIT 3 AND ONLY BIT 3 SET?
(1) 003406 001402 BEQ 1$ ;/IF SO-LETS TRY CLEARING IT.
(2)
:::*****>>> ERROR <<<*****
(1) 003410 104002 ERROR 2 ;/ERROR CLOCK AS STATUS REGISTER
(1) ;/BIT 3 FAILED TO BIT SET.
(2)
:::*****>>> ERROR <<<*****
(1) 003412 000412 BR 2$ ;/BR TO END SUBTEST.
(1)
(1) 003414 042777 000010 175754 1$: BIC #BIT3,@ASR ;/TRY CLEARING BIT 3.
(1) 003422 005037 001124 CLR $GDDAT ;/CLEAR S/B FOR TYPEOUT IF ANY.
(1) 003426 017737 175744 001126 MOV @ASR,$BDDAT ;/NOW READ IT BACK.
(1) 003434 001401 BEQ 2$ ;/IF ZERO - NO ERROR!
(1)
(2)
:::*****>>> ERROR <<<*****
(1) 003436 104002 ERROR 2 ;/ERROR - CLOCK A STATUS REGISTER.
(1) ;/BIT 3 FAILED TO CLEAR.
(1)
(2)
:::*****>>> ERROR <<<*****
(1) 003440 2$:
(1)
349
```

(1) ;/#
(5) :*****
(4) :*TEST 12 *TEST THAT CLOCK A STATUS REGISTER BIT 2 CAN BE SET AND CLEARED
(5) :*
(5) :*CLOCK STATUS REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(5) :*F/FS OR GATES
(5) :*

(4) :*****
(3) 003440 000004 TST12: SCOPE
(2) 003442 012737 000100 001160 MOV #100,\$TIMES ;;DO 100 ITERATIONS
(1) CLR @ASR ;/CLEAR THE STATUS REGISTER.
(1) 003450 005077 175722 BIS #BIT2,@ASR ;/SET BIT 2.
(1) 003454 052777 000004 175714 MOV #BIT2,\$GDDAT ;/SET FOR ERROR TYPEOUT S/B.
(1) 003462 012737 000004 001124 MOV @ASR,\$BDDAT ;/READ THE STATUS REGISTER.
(1) 003470 017737 175702 001126 CMP \$GDDAT,\$BDDAT ;/DID BIT 2 AND ONLY BIT 2 SET?
(1) 003476 023737 001124 001126 BEQ 1\$;/IF SO-LETS TRY CLEARING IT.
(1) 003504 001402

:::*****>>> ERROR <<<*****

(1) 003506 104002 ERROR 2 ;/ERROR CLOCK AS STATUS REGISTER
(1) ;/BIT 2 FAILED TO BIT SET.
(2)

:::*****>>> ERROR <<<*****

(1) 003510 000412 BR 2\$;/BR TO END SUBTEST.
(1) 003512 042777 000004 175656 1\$: BIC #BIT2,@ASR ;/TRY CLEARING BIT 2.
(1) 003520 005037 001124 CLR \$GDDAT ;/CLEAR S/B FOR TYPEOUT IF ANY.
(1) 003524 017737 175646 001126 MOV @ASR,\$BDDAT ;/NOW READ IT BACK.
(1) 003532 001401 BEQ 2\$;/IF ZERO - NO ERROR!

:::*****>>> ERROR <<<*****

(1) 003534 104002 ERROR 2 ;/ERROR - CLOCK A STATUS REGISTER.
(1) ;/BIT 2 FAILED TO CLEAR.
(1)

:::*****>>> ERROR <<<*****

(1) 003536 2\$:
(1)
350

(1) ;/#
(5) :*****
(4) :*TEST 13 *TEST THAT CLOCK A STATUS REGISTER BIT 1 CAN BE SET AND CLEARED
(5) :*
(5) :*CLOCK STATUS REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
(5) :*F/FS OR GATES
(5) :*

(4) :*****
(3) 003536 000004 TST13: SCOPE
(2) 003540 012737 000100 001160 MOV #100,\$TIMES ;;DO 100 ITERATIONS
(1) 003546 005077 175624 CLR @ASR ;/CLEAR THE STATUS REGISTER.
(1) 003552 052777 000002 175616 BIS #BIT1,@ASR ;/SET BIT 1.
(1) 003560 012737 000002 001124 MOV #BIT1,\$GDDAT ;/SET FOR ERROR TYPEOUT S/B.
(1) 003566 017737 175604 001126 MOV @ASR,\$BDDAT ;/READ THE STATUS REGISTER.
(1) 003574 023737 001124 001126 CMP \$GDDAT,\$BDDAT ;/DID BIT 1 AND ONLY BIT 1 SET?
(1) 003602 001402 BEQ 1\$;/IF SO-LETS TRY CLEARING IT.

(2) :;*****>>> ERROR <<<*****
(1) 003604 104002 ERROR 2 ;/ERROR CLOCK AS STATUS REGISTER
(1) ;/BIT 1 FAILED TO BIT SET.

(2) :;*****>>> ERROR <<<*****
(1) 003606 000412 BR 2\$;/BR TO END SUBTEST.
(1) 003610 042777 000002 175560 1\$: BIC #BIT1,@ASR ;/TRY CLEARING BIT 1.
(1) 003616 005037 001124 CLR \$GDDAT ;/CLEAR S/B FOR TYPEOUT IF ANY.
(1) 003622 017737 175550 001126 MOV @ASR,\$BDDAT ;/NOW READ IT BACK.
(1) 003630 001401 BEQ 2\$;/IF ZERO - NO ERROR!

(2) :;*****>>> ERROR <<<*****
(1) 003632 104002 ERROR 2 ;/ERROR - CLOCK A STATUS REGISTER.
(1) ;/BIT 1 FAILED TO CLEAR.

(2) :;*****>>> ERROR <<<*****
(1) 003634 2\$:

385

(5)

(4)

(4)

(3) 003732 000004

(1)

(1) 003734 005077 175440

(1) 003740 012737 125252 001124

(1) 003746 013777 001124 175424

(1) 003754 017737 175420 001126

(1)

(1) 003762 023737 001124 001126

(1) 003770 001402

(1)

(2)

 *TEST 15 *TEST THAT PATERN 125252 WILL SET AND CLEAR IN BUFFER REG.

 TST15: SCOPE

```

CLR @ABR ;/CLEAR THE BUFFER REG.
MOV #125252,$GDDAT ;/RECORD PATTERN: 125252
MOV $GDDAT,@ABR ;/SET PATTERN IN BUFFER REG.
MOV @ABR,$BDDAT ;/READ THE BUFFER REG.

CMP $GDDAT,$BDDAT ;/DID THE PATTERN SET OK?
BEQ 1$ ;/YES-TRY CLEARING IT.
    
```

:::*****>>> ERROR <<<*****

(1) 003772 104003

(1)

(2)

```

ERROR 3 ;/ERROR PATTERN 125252 FAILED TO
           ;/SET PROPERLY IN BUFFER REG.
    
```

:::*****>>> ERROR <<<*****

(1) 003774 000412

(1)

(1)

(1) 003776 042777 125252 175374 1\$:

(1) 004004 005037 001124

(1) 004010 017737 175364 001126

(1)

(2)

```

BR 2$ ;/GOTO SCOPE LOOP.
BIC #125252,@ABR ;/TRY CLEARING PATTERN.
CLR $GDDAT ;/EXPECT ZERO BACK.
MOV @ABR,$BDDAT ;/READ BUFFER REG.,WAS IT ZERO?
BEQ 2$ ;/YES-NEXT TEST.
    
```

:::*****>>> ERROR <<<*****

(1) 004020 104003

(1)

(2)

```

ERROR 3 ;/BUFFER REG. COULD NOT BE LOADED
           ;/TO A ZERO.
    
```

:::*****>>> ERROR <<<*****

(1) 004022

(1)

2\$:

404
(3)
(4)
(4)
(4)
(4)
(4)
(4)
(3)
(2) 004112 000004
(1) 004114 012737 000050 001160
405
406 004122 005077 175250
407 004126 112777 127677 175242
408
409
410
411
412 004134 017777 175236 174764
413
414 004142 013737 001126 001124
415 004150 105037 001125
416
417 004154 105737 001127
418
419 004160 001401
420
421

422 004162 104001
423
424
425
426

427 004164
428

```
*****
*TEST 17 *TEST THE LOW BYTE OPERATION OF CLOCK'S STATUS REGISTER
**
*WE CAN SUCCESSFULLY WRITE EVERY BIT IN STATUS REG A
*NOW LETS CHECK THE BYTE OPERATION OF THIS REGISTER.
*
*****
TST17: SCOPE
MOV #50,$TIMES ;;DO 50 ITERATIONS

CLR @ASR ;MAKE SURE THE STATUS REGISTER IS CLEAR.
MOVB #127677,@ASR ;TRY WRITING ALL BITS IN THE
;STATUS REGISTER. LOGIC SHOULD PREVENT IT
;FROM BEING WRITTEN INTO BECAUSE
;WE ARE USING A DATOB INSTRUCTION.

MOV @ASR,@$BDDAT ;NOW EXAMINE THE
;STATUS REGISTER.
MOV $BDDAT,$GDDAT ;FIX $GDDAT FOR ERROR TYPEOUT IF
CLRB $GDDAT+1 ;ANY RROR HAS OCCURRED, UPPER BYTE CLEARED.

TSTB $BDDAT+1 ;ARE ANY BITS IN THE UPPER BYTE
;OF THE STATUS REGISTER SET?
BEQ 1$ ;BRANCH NEXT TEST IF UPPER BYTE=0.

*****
;;$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$ ERROR <<<$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
ERROR 1 ;ERROR - WROTE INTO UPPER BYTE OF
;CLOCK'S STATUS WHEN
;DOING A DATOB TO THE LOW BYTE.

*****
1$:
*****
```

430
(3)
(4)
(4)
(4)
(4)
(4)
(4)
(3)
(2) 004164 000004
(1) 004166 012737 000050 001160
431
432 004174 005077 175176
433
434 004200 005237 001376
435
436
437
438 004204 112777 177313 175164
439
440
441
442
443
444 004212 005337 001376
445
446 004216 017737 175154 001126
447 004224 013737 001126 001124
448 004232 105037 001124
449 004236 105737 001126
450 004242 001401
451
452

453 004244 104001
454
455
456

457 004246
458

```
::*****  
: *TEST 20 *TEST THE HIGH BYTE OPERATION OF A'S STATUS REGISTER  
:  
: *  
: *WE CAN SUCCESSFULLY WRITE EVERY BIT IN STATUS REG A  
: *NOW LETS CHECK THE BYTE OPERATION OF THIS REGISTER.  
: *  
:  
:*****  
TST20: SCOPE  
MOV #50,$TIMES ;:DO 50 ITERATIONS  
CLR @ASR ;:CLEAR THE STATUS REGISTER.  
INC ASR ;:ADD #1 TO THE STATUS REGISTER'S ADDRESS  
;:SO THAT WE WILL BE WRITING INTO  
;:THE HIGH BYTE.  
MOVB #177313,@ASR ;:TRY WRITING ALL BITS IN THE STATUS  
;:REGISTER. LOGIC SHOULD PREVENT THE LOW  
;:BYTE OF THE STATUS REGISTER FROM  
;:BEING WRITTEN INTO BECAUSE WE ARE USING  
;:A DATOB INSTRUCTION WITH AOO SET.  
DEC ASR ;:FIX ADDRESS OF THE STATUS REGISTER ADDR.  
;:SO WE CAN LOOK AT THE WHOLE WORD.  
MOV @ASR,$BDDAT ;:READ BACK WHAT THE STATUS REG. CONTAINS  
MOV $BDDAT,$GDDAT ;:FIX $GDDAT FOR ERROR TYPEOUT IF AN ERROR  
;:OCCURRED, LOWER BYTE CLEARED.  
CLRB $GDDAT  
TSTB $BDDAT ;:IS LOWER BYTE CLEAR?  
BEQ 1$ ;:BR IF YES TO NEXT SUBTEST.  
  
: ***** ERROR <<<*****  
ERROR 1 ;:ERROR - WROTE INTO LOWER BYTE  
;:OF CLOCKS STATUS REGISTER WHEN  
;:DOING A DATOB TO THE HIGH BYTE.  
: ***** ERROR <<<*****  
1$:
```


:: \$>>> ERROR <<< \$<<<<

675 005264 000410
676
677 005266 005077 174104
678 005272 013777 001124 174100
679 005300 005737 001124
680 005304 001312
681 005306
682
683
(3)
(3)
(2) 005306 000004
684
685 005310 005737 001440
686 005314 001411
687
688 005316 005037 170500
689 005322 005737 170502
690 005326 052737 000040 170500
691 005334 012700 000010
692 005340
693 005340 005077 174032
694 005344 012777 177777 174026
695
696 005352 052777 000061 174016
697
698 005360 052777 000400 174010
699
700 005366 105777 174004
701 005372 100402
702
703

```
BR 3$ :GOTO SCOPE LOOP.
2$: CLR @ASR
MOV $GDDAT,@ABR
TST $GDDAT ;ALL DONE?
BNE 1$ ;NO DO NEXT INCREMENT.
3$:
:*****
:*TEST 31 *TEST THAT OVERFLOW (CSR BIT07) WILL SET ON OVERFLOW
:*****
TST31: SCOPE
TST EXS ;TESTOR MODE ENABLED??
BEQ 2$ ;NO-THEN SKIP NEXT SECTION OF CODE.
CLR @#170500 ;CLEAR TESTOR A/D
TST @#170502 ;DUMB READ OF A/D BUFFER.
BIS #BIT5,@#170500 ;ENABLE EXTRENAL START OF A/D.
MOV #8,R0 ;SET TIME OUT NUMBER.
2$: CLR @ASR ;CLEAR THE CSR
MOV #-1,@ABR ;SET PRESET BUFFER TO ALL ONES.
BIS #BIT5!BIT4!BIT0,@ASR ;START CLOCK, RATE ST1.
BIS #BIT8,@ASR ;COUNT CLOCK ONCE, OVERFLOW
;SHOULD OCCUR.
TSTB @ASR ;DID OVERFLOW SET?
BMI 1$ ;YES - THEN NEXT TEST
```

:: \$>>> ERROR <<< \$<<<<

704 005374 104006
705
706 005376 000411
707 005400 005737 001440
708 005404 001406
709 005406 105737 170500
710
711 005412 100403
712 005414 005300
713 005416 001370
714

```
ERROR 6 ;ERROR - OVERFLOW, CSR BIT0?
;FAILED TO SET ON OVERFLOW
1$: BR TST32
TST EXS ;TEST EXTERNAL SIGNALS?
BEQ TST32
TSTB @#170500 ;IF OVERFLOW GOT OUT,IT GAVE A/D START,
;WE'RE LOOKING FOR A/D DONE-DID IT GET SET?
BMI TST32
DEC R0 ;DID WE ALLOW ENOUGH TIME??
BNE 1$ ;NO-THEN WAIT.
```

:: \$>>> ERROR <<< \$<<<<

715 005420 104006
716
717

```
ERROR 6 ;OVERFLOW OUT NOT DETECTED
;BY TESTOR
```

:: \$>>> ERROR <<< \$<<<<

718
719

720
(3)
(3)
(2) 005422 000004
721
722 005424 005077 173746
723
724 005430 012777 177777 173742
725
726 005436 052777 000061 173732
727
728 005444 052777 000400 173724
729
730
731
732 005452 032777 000001 173716
733 005460 001401
734
735

```
::*****  
:*TEST 32 *TEST THAT OVERFLOW WILL CLEAR THE GO BIT  
:*****  
TST32: SCOPE  
CLR @ASR ;CLEAR THE CSR.  
MOV #-1,@ABR ;PRESET CLOCK TO -1.  
BIS #BIT5!BIT4!BIT0,@ASR ;START CLOCK, RATE:ST1  
BIS #BIT8,@ASR ;COUNT ONCE, OVERFLOW  
;SHOULD OCCUR CLEARING  
;ENABLE (CSR BIT00)  
BIT #BIT0,@ASR ;DID THE ENABLE CLEAR?  
BEQ 1$ ;YES - NEXT TEST.
```

::\$>>> ERROR <<<\$

736 005462 104006
737
738
739 005464
740
741

```
ERROR 6 ;ERROR - OVERFLOW FAILED  
;TO CLEAR ENABLE (CSR BIT00)  
1$:
```

(3)
(3)
(2) 005464 000004
742
743 005466 005077 173704
744 005472 012777 177777 173700
745 005500 052777 000063 173670
746
747 005506 052777 000400 173662
748
749 005514 032777 000001 173654
750 005522 001001
751

```
::*****  
:*TEST 33 *TEST THAT GO BIT DOES NOT CLEAR ON OVERFLOW, IF MODE 1  
:*****  
TST33: SCOPE  
CLR @ASR ;CLEAR THE CSR.  
MOV #-1,@ABR ;PRESET BUFFER=ONE COUNT FROM OVERFLOW.  
BIS #63,@ASR ;MODE 1, RATE:ST1, GO.  
BIS #BIT8,@ASR ;GENERATE MAINTENANCE ST1.  
BIT #BIT0,@ASR ;DID ENABLE (GO BIT) CLEAR?  
BNE 1$ ;NO (GOOD) NEXT TEST.
```

::\$>>> ERROR <<<\$

752 005524 104006
753
754

```
ERROR 6 ;GO BIT CLEARED ON OVERFLOW  
;WHEN MODE 1 WAS SELECTED
```

::\$>>> ERROR <<<\$

755
756 005526 005077 173644
757
803
804

```
1$: CLR @ASR ;CLEAR THE CLOCK.
```

806
 (5)
 (4)
 (5)
 (5)
 (5)
 (5)
 (5)
 (4)
 (3)
 (2)
 (1)
 (1)
 (1)
 (1)
 (1)
 (1)
 (1)
 (1)
 (1)
 (1)
 (1)
 (1)
 (2)
 (2)
 (2)
 (2)
 (2)
 (2)
 (2)
 (1)
 (1)
 (1)
 (1)
 (1)
 (1)
 (2)
 (1)
 (1)
 (1)
 (1)
 (1)

```

: *****
:*TEST 34      *TEST THE ABILITY OF CLOCK TO COUNT AT 1MHZ RATE
:
:*
:*THIS TEST IS DESIGNED TO TEST THE CLOCK'S ABILITY
:*TO COUNT AT 1MHZ RATE.
:*
: *****
TST34: SCOPE
MOV #5,$TIMES      ;;DO 5 ITERATIONS
:
CLR @ASR           ;/CLEAR CLOCK
CLR @ABR           ;/CLEAR PRESET BUFFER
MOV #BIT0!10,@ASR ;/START CLOCK, MODE0, RATE:1MHZ
CLR R0             ;/NOW WE'LL DO A LITTLE DELAY. THIS DELAY
:
1$: INC R0         ;/WILL AMOUNT TO APPROXIMATELY
   BNE 1$         ;/369 MS.
:
MOV @ASR,-(6)     ;/SAVE CSR
MOV (6),$TMP3     ;/GET CSR.
BIC #177707,$TMP3 ;/SAVE RATE BITS.
BIS #BIT11!BIT2!BIT0,$TMP3 ;/SET MODE 2, NO RATE,DISABLE INTERNAL OSC
MOV $TMP3,@ASR   ;/LOAD CSR.
: /THIS MUST BE DONE IN
: /ORDER TO XFERR COUNTER
: /TO BUFFER ON ST2.
: /GENERATE ON ST2 PULSE
: /READ THE PRESET BUFFER,
: /PREVIOUS COUNTER
: /CONTENTS ARE IN $BDDAT.
BIS #BIT9,@ASR   ;/RESTORE CSR
MOV @ABR,$BDDAT  ;/YES - NEXT TEST.
TST $BDDAT
BNE 2$          ;/AT HIGH RATE MAY HAVE HAD OVERFLOW
TSTB -2(6)     ;/NOTE: CSR HAD BEEN PUT ON STACK.
BMI 2$         ;/NEXT TEST IF OVERFLOW.
:
: *****
ERROR 6
: /CLOCK FAILED TO COUNT AT
: /RATE:1MHZ
:
: *****
:
2$: CLR @ASR     ;/CLEAR THE CLOCK.
```

ERROR 6

005654 104006
 005656 005077 173514

812
 (5)
 (4)
 (5)
 (5)
 (5)
 (5)
 (5)
 (4)
 (3)
 (2)
 (1)
 (1)
 (1)
 (1)
 (1)
 (1)
 (1)
 (1)
 (1)
 (1)
 (2)
 (2)
 (2)
 (2)
 (2)
 (2)
 (2)
 (2)
 (2)
 (2)
 (2)
 (1)
 (1)
 (1)
 (1)
 (1)
 (1)
 (1)
 (1)
 (1)
 (2)

 : *TEST 37 *TEST THE ABILITY OF CLOCK TO COUNT AT 1KHZ RATE

* *
 : *THIS TEST IS DESIGNED TO TEST THE CLOCK'S ABILITY
 : *TO COUNT AT 1KHZ RATE.
 : *
 : *
 : *****

```
TST37:  SCOPE
      MOV    #5,$TIMES      ;;DO 5 ITERATIONS

      CLR    @ASR           ;/CLEAR CLOCK
      CLR    @ABR           ;/CLEAR PRESET BUFFER
      MOV    #BIT0!40,@ASR ;/START CLOCK, MODE0, RATE:1KHZ
      CLR    R0             ;/NOW WE'LL DO A LITTLE DELAY. THIS DELAY
                              ;/WILL AMOUNT TO APPROXIMATELY
                              ;/369 MS.

1$:   INC    R0
      BNE   1$

      MOV    @ASR,-(6)      ;/SAVE CSR
      MOV    (6),$TMP3      ;/GET CSR.
      BIC   #177707,$TMP3 ;/SAVE RATE BITS.
      BIS   #BIT11!BIT2!BIT0,$TMP3 ;/SET MODE 2, NO RATE,DISABLE INTERNAL OSC
      MOV    $TMP3,@ASR    ;/LOAD CSR.
                              ;/THIS MUST BE DONE IN
                              ;/ORDER TO XFERR COUNTER
                              ;/TO BUFFER ON ST2.
                              ;/GENERATE ON ST2 PULSE
      BIS   #BIT9,@ASR     ;/READ THE PRESET BUFFER,
      MOV    @ABR,$BDDAT ;/PREVIOUS COUNTER
                              ;/CONTENTS ARE IN $BDDAT.
      MOV    (6)+,@ASR     ;/RESTORE CSR
      TST   $BDDAT         ;/YES - NEXT TEST.
      BNE   2$
      TSTB  -2(6)          ;/AT HIGH RATE MAY HAVE HAD OVERFLOW
                              ;/NOTE: CSR HAD BEEN PUT ON STACK.
                              ;/NEXT TEST IF OVERFLOW.

      BMI   2$
```

;;\$>>> ERROR <<<\$

(1) 006264 104006 ERROR 6 ;/CLOCK FAILED TO COUNT AT
 (1) ;/RATE:1KHZ
 (2)

;;\$>>> ERROR <<<\$

(1) 006266 005077 173104 2\$: CLR @ASR ;/CLEAR THE CLOCK.
 (1)
 (1)

::: \$>>> ERROR <<< \$

893 007072 000402
894 007074
(1) 007074 062706 000004
895 007100 005077 172272
896
897
(3)
(3)
(2) 007104 000004
898
899
(1) 007106 012746 000340
(1) 007112 012746 007120
(1) 007116 000002
(1) 007120
900
901 007120 005077 172252
902 007124 012777 007200 172254
903 007132 012777 040001 172236
904 007140 052777 001000 172230
905
(1) 007146 012746 000000
(1) 007152 012746 007160
(1) 007156 000002
(1) 007160
906
907 007160 000240
908
(1) 007162 012746 000340
(1) 007166 012746 007174
(1) 007172 000002
(1) 007174
909

BR 2\$
1\$:
ADD #4, SP ;/ADD #4 TO STACK POINTER.
2\$: CLR @ASR ;CLEAR THE CLOCK.
:*****
:*TEST 45 *TEST THAT ST2 WILL CAUSE AN INTERRUPT
:*****
TST45: SCOPE
MOV #340,-(SP) ;PUT PRIORITY ON STACK.
MOV #64\$,-(SP) ;PUT RETURN ADDRESS ON STACK
RTI ;DO AN RTI, PUTS PRIORITY IN CPU.
64\$:
CLR @ASR ;CLEAR CLOCKS CSR.
MOV #1\$,@VECT2 ;SET UP INTERRUPT VECTOR.
MOV #BIT14!BIT0,@ASR ;SET 'INT2',AND GO BIT.
BIS #BIT9,@ASR ;GENERATE A MAINTENANCE ST2.
MOV #0,-(SP) ;PUT PRIORITY ON STACK.
MOV #65\$,-(SP) ;PUT RETURN ADDRESS ON STACK
RTI ;DO AN RTI, PUTS PRIORITY IN CPU.
65\$:
NOP ;STALL TIME
MOV #340,-(SP) ;PUT PRIORITY ON STACK.
MOV #66\$,-(SP) ;PUT RETURN ADDRESS ON STACK
RTI ;DO AN RTI, PUTS PRIORITY IN CPU.
66\$:

::: \$>>> ERROR <<< \$

910 007174 104007
911

ERROR 7 ;CLOCK FAILED TO INTERRUPT ON ST2.

::: \$>>> ERROR <<< \$

912 007176 000402
913 007200
(1) 007200 062706 000004
914 007204 005077 172166
915
916
917
918
919

BR 2\$
1\$:
ADD #4, SP ;/ADD #4 TO STACK POINTER.
2\$: CLR @ASR ;CLEAR CLOCK'S CSR.
.SBTTL *
.SBTTL *PHASE 5 ADVANCED TESTING
.SBTTL *

1074 007570 104011
1075
1076

::: \$>>> ERROR <<< \$

ERROR 11 ;CLOCK DISABLE INTERNAL
;OSC. DID NOT WORK.

::: \$>>> ERROR <<< \$

1077 007572 005077 171600
1078
1079

2\$: CLR @ASR ;CLEAR THE CSR.

(3)

::: *****
:*TEST 52 *TEST THAT CLOCK CAN BE COUNTED USING MAINTENANCE OSC
:*****

(2) 007576 000004
1080

TST52: SCOPE

1081 007600 005077 171572
1082 007604 005077 171570
1083 007610 052777 004000 171560
1084 007616 052777 000011 171552
1085 007624 012700 177754
1086

CLR @ASR ;CLEAR THE CSR.
CLR @ABR ;CLEAR THE PRESET BUFFER.
BIS #BIT11,@ASR ;DISABLE THE INTERNAL OSC.
BIS #BIT3!BIT0,@ASR ;START CLOCK, 1MHZ, GO.
MOV #-20.,R0 ;SET TO COUNT 20 TIMES

1087 007630 052777 002000 171540 1\$:
1088
1089

BIS #BIT10,@ASR ;GENERATE 1 MAINTENANCE OSC.
;NOTE: AT 1MHZ, IT TAKES 10
;MAINT. OSC TO EQUAL 1 COUNT
;DO 20 MAINTENANCE OSC.

1090 007636 005200
1091 007640 001373
1092

INC R0
BNE 1\$

1093 007642 017746 171530
(1) 007646 011637 001424
(1) 007652 042737 177707 001424
(1) 007660 052737 004005 001424
(1) 007666 013777 001424 171502
(1)

MOV @ASR,-(6) ;/SAVE CSR
MOV (6),\$TMP3 ;/GET CSR.
BIC #177707,\$TMP3 ;/SAVE RATE BITS.
BIS #BIT11!BIT2!BIT0,\$TMP3 ;/SET MODE 2, NO RATE,DISABLE INTERNAL OSC
MOV \$TMP3,@ASR ;/LOAD CSR.

(1)
(1)
(1) 007674 052777 001000 171474
(1) 007702 017737 171472 001126
(1)

;/THIS MUST BE DONE IN
;/ORDER TO XFERR COUNTER
;/TO BUFFER ON ST2.
BIS #BIT9,@ASR ;/GENERATE ON ST2 PULSE
MOV @ABR,\$BDDAT ;/READ THE PRESET BUFFER,
;/PREVIOUS COUNTER

(1) 007710 012677 171462
(1) 007714 005737 001126
1094 007720 001001
1095
1096

MOV (6)+,@ASR ;/CONTENTS ARE IN \$BDDAT.
TST \$BDDAT ;/RESTORE CSR
BNE 2\$;YES - NEXT TEST.

::: \$>>> ERROR <<< \$

1097 007722 104011
1098
1099

ERROR 11 ;ERROR COULD NOT COUNT USING
;MAINTENANCE OSC.

::: \$>>> ERROR <<< \$

1100 007724 005077 171446
1101

2\$: CLR @ASR ;CLEAR THE CSR.

:: \$>>> ERROR <<< \$

```
(1) 011466 000447      BR      5$  
(1) 011470 012701 000012   66$:  MOV      #10.,R1  
(1) 011474 012700 023417   3$:  MOV      #9999.,R0           ;/GET THE NUMBER OF MORE OSC PULSES  
(1)                                     ;/TO BE GENERATED.  
(1) 011500 052777 002000 167670 4$:  BIS      #BIT10,@ASR       ;/GENERATE ANOTHER OSC PULSE.  
(1) 011506 005300                DEC      R0                ;/WHAT WE WANT TO CHECK  
(1) 011510 001373                BNE     4$                 ;/100HZ PULSE ON 9999 OSC PULSES.  
(1) 011512 005301                DEC      R1  
(1) 011514 001367                BNE     3$  
(1)  
(2) 011516 017746 167654      MOV      @ASR,-(6)         ;/SAVE CSR  
(2) 011522 011637 001424      MOV      (6),$TMP3        ;/GET CSR.  
(2) 011526 042737 177707 001424 BIC     #177707,$TMP3     ;/SAVE RATE BITS.  
(2) 011534 052737 004005 001424 BIS     #BIT11!BIT2!BIT0,$TMP3 ;/SET MODE 2, NO RATE,DISABLE INTERNAL OSC  
(2) 011542 013777 001424 167626 MOV     $TMP3,@ASR        ;/LOAD CSR.  
(2)                                     ;/THIS MUST BE DONE IN  
(2)                                     ;/ORDER TO XFERR COUNTER  
(2)                                     ;/TO BUFFER ON ST2.  
(2) 011550 052777 001000 167620 BIS     #BIT9,@ASR        ;/GENERATE ON ST2 PULSE  
(2) 011556 017737 167616 001126 MOV     @ABR,$BDDAT      ;/READ THE PRESET BUFFER,  
(2)                                     ;/PREVIOUS COUNTER  
(2) 011564 012677 167606      MOV     (6)+,@ASR        ;/CONTENTS ARE IN $BDDAT.  
(2) 011570 005737 001126      TST     $BDDAT          ;/RESTORE CSR  
(1) 011574 023737 001124 .001126 CMP     $GDDAT,$BDDAT     ;/WAS ANOTHER 100HZ PULSE GENERATED?  
(1) 011602 001401                BEQ     5$                ;/NO - NEXT TEST.  
(2)
```

:: \$>>> ERROR <<< \$

```
(1) 011604 104011      ERROR 11           ;/WE SEEM TO HAVE GENERATED  
(1)                                     ;/ANOTHER 100HZ PULSE ON  
(1)                                     ;/ONLY 9999 MAINTENANCE  
(1)                                     ;/OSC PULSES.  
(2)
```

:: \$>>> ERROR <<< \$

```
(1) 011606 005077 167564   5$:  CLR     @ASR           ;/CLEAR THE CSR.  
(1)
```

1178
1196


```
1344 ;
1345 ;
1346 013056 000004 ENDP: SCOPE
1347 ;
1348 ;
1349 013060 105737 001215 TSTB $ENVM ;SEE IF APT WILL LET UP AUTO-SIZE.
1350 013064 100537 BMI 2$ ;NO - EXIT.
1351 ;
1352 ;
1353 013066 023737 001434 001436 CMP MDEVCT,TSTCNT ;TESTED MAX. UNITS?
1354 013074 001507 BEQ 4$ ;YES EXIT.
1355 013076 006337 001426 ASL ROTATE ;POINT NEXT UNIT.
1356 013102 005237 001434 INC MDEVCT
1357 ;
1358 013106 062737 000004 001376 ADD #4,ASR ;YES, ADD TO BASE ADDR.
1359 013114 013746 000004 MOV ERRVEC,-(6) ;SAVE CONTENTS OF LOC 4.
1360 013120 012737 013274 000004 MOV #1$,ERRVEC ;SET UP IN CASE NO MORE CLOCKS.
1361 ;
1362 013126 005777 166244 TST @ASR ;TIME OUT HERE IF NO MORE CLOCKS.
1363 ;
1364 ;
1365 013132 005737 001202 TST $PASS ;IF HERE, ANOTHER CLOCK FOUND.
1366 013136 001003 BNE 3$ ;IS THIS 1ST PASS?
1367 013140 053737 001426 001430 BIS ROTATE,UTEST ;NO-GET OUT.
1368 013146 3$: ;YES-RECORD THIS UNIT.
1369 013146 104401 013154 TYPE 65$ ;;TYPE ASCIZ STRING
(1) 013152 000405 BR 64$ ;;GET OVER THE ASCIZ
(1) 64$: .ASCIZ <15><12>'UNIT #'
(1) 013166 64$:
1370 013166 013746 001204 MOV $DEVCT,-(SP) ;;SAVE $DEVCT FOR TYPEOUT
(1) 013172 104402 TYPOC ;;GO TYPE--OCTAL ASCII(ALL DIGITS)
1371 013174 104401 013202 TYPE 67$ ;;TYPE ASCIZ STRING
(1) 013200 000406 BR 66$ ;;GET OVER THE ASCIZ
(1) 66$: .ASCIZ '' COMPLETED ''
1372 013216 005237 001204 INC $DEVCT
1373 013222 104401 013230 TYPE 69$ ;;TYPE ASCIZ STRING
(1) 013226 000410 BR 68$ ;;GET OVER THE ASCIZ
(1) 68$: .ASCIZ '' TESTING UNIT #'
1374 013250 68$:
1375 013250 013746 001204 MOV $DEVCT,-(SP) ;;SAVE $DEVCT FOR TYPEOUT
(1) 013254 104402 TYPOC ;;GO TYPE--OCTAL ASCII(ALL DIGITS)
1376 013262 012637 000004 MOV (6)+,ERRVEC ;RESTORE LOC 4.
1377 013270 062737 000010 001402 ADD #10,VECT1 ;UPDATE VECTOR ADDR.
1378 000137 002334 JMP LOOP ;TEST NEW UNIT.
1379 1$:
(1) 013274 062706 000004 ADD #4,SP ;/ADD #4 TO STACK POINTER.
1380 013300 012637 000004 MOV (6)+,ERRVEC ;RESTORE LOC 4
1381 013304 022737 000000 001204 CMP #0,$DEVCT ;TESTED ONLY ONE UNIT?
1382 013312 001424 BEQ 2$ ;YES - NO NEED FOR TYPEOUT.
1383 ;
1384 4$:
1385 013314 104401 013322 TYPE 71$ ;;TYPE ASCIZ STRING
(1) 013320 000405 BR 70$ ;;GET OVER THE ASCIZ
(1) 71$: .ASCIZ <15><12>'UNIT #'
```

(1) 013334
1386 013334 013746 001204
(1) 013340 104402
1387 013342 104401 013350
(1) 013346 000406
(1)
(1) 013364
1388
1389 013364 013737 001250 001376
1390 013372 013737 001244 001402
1391 013400 013737 001204 001442
1392 013406 005237 001442
1393 013412 012737 000000 001204
1394
1395 013420 005037 001434
1396 013424 012737 000001 001426
1408
1409
1410
(1)
(2)
(1)
(1)
(1)
(1)
(1)
(1) 013432
(2) 013432 000240
(1) 013434 005037 001102
(1) 013440 005037 001160
(1) 013444 005237 001202
(1) 013450 042737 100000 001202
(1) 013456 005327
(1) 013460 000001
(1) 013462 003122
(1) 013464 012737
(1) 013466 000001
(1) 013470 013460
(3) 013472 104401 013500
(3) 013476 000406
(3)
(3) 013514
(3) 013514 013746 001202
(3) 013520 104402
(3) 013522 104401 013530
(3) 013526 000411
(3)
(3) 013552
(3) 013552 013746 001432
(3) 013556 104402
(3) 013560 104401 013566
(3) 013564 000407
(3)
(3) 013604
(3) 013604 013746 001442
(3) 013610 104402
(3) 013612 104401 013620

```
70$: MOV $DEVCT,-(SP) ;;SAVE $DEVCT FOR TYPEOUT
      TYPOC ;;GO TYPE--OCTAL ASCII(ALL DIGITS)
      TYPE ,73$ ;;TYPE ASCII STRING
      BR ,72$ ;;GET OVER THE ASCII
      ;;73$: .ASCIIZ "" COMPLETED ""
72$:
2$: MOV $BASE,ASR
     MOV $VECT1,VECT1
     MOV $DEVCT,LCNT
     INC LCNT
     MOV #0,$DEVCT
     CLR MDEVCT ;;BEGIN TESTING 1ST UNIT.
     MOV #1,ROTATE ;;POINT TO IT.

.SBTTL END OF PASS ROUTINE

*****
;*INCREMENT THE PASS NUMBER ($PASS)
;*IF THERES A MONITOR GO TO IT
;*IF THERE ISN'T JUMP TO LOOP

$EOP: NOP
      CLR $TSTNM ;;ZERO THE TEST NUMBER
      CLR $TIMES ;;ZERO THE NUMBER OF ITERATIONS
      INC $PASS ;;INCREMENT THE PASS NUMBER
      BIC #100000,$PASS ;;DON'T ALLOW A NEG. NUMBER
      DEC (PC)+ ;;LOOP?
$EOPCT: .WORD 1
        BGT $DOAGN ;;YES
        MOV (PC)+,@(PC)+ ;;RESTORE COUNTER
$ENDCT: .WORD 1
        $EOPCT
        TYPE ,65$ ;;TYPE ASCII STRING
        BR ,64$ ;;GET OVER THE ASCII
      ;;65$: .ASCIIZ <15><12>#ENDPASS #
64$: MOV $PASS,-(SP) ;;SAVE $PASS FOR TYPEOUT
      TYPOC ;;GO TYPE--OCTAL ASCII(ALL DIGITS)
      TYPE ,67$ ;;TYPE ASCII STRING
      BR ,66$ ;;GET OVER THE ASCII
      ;;67$: .ASCIIZ # TOTAL ERRORS #
66$: MOV ERCNT,-(SP) ;;SAVE ERCNT FOR TYPEOUT
      TYPOC ;;GO TYPE--OCTAL ASCII(ALL DIGITS)
      TYPE ,69$ ;;TYPE ASCII STRING
      BR ,68$ ;;GET OVER THE ASCII
      ;;69$: .ASCIIZ #: THERE ARE #
68$: MOV LCNT,-(SP) ;;SAVE LCNT FOR TYPEOUT
      TYPOC ;;GO TYPE--OCTAL ASCII(ALL DIGITS)
      TYPE ,71$ ;;TYPE ASCII STRING
```

```
(3) 013616 000411          BR      70$          ;;GET OVER THE ASCIZ
(3) 013642          ;;71$: .ASCIZ # (OCTAL) UNITS.#
(3) 013642 104401 013650 70$:          TYPE      73$          ;;TYPE ASCIZ STRING
(3) 013646 000415          BR      72$          ;;GET OVER THE ASCIZ
(3) 013702          ;;73$: .ASCIZ <200>#THE GOOD UNITS (L TO R) #
(3) 013702 013746 001430 72$:          MOV      UTEST,-(SP)      ;;SAVE UTEST FOR TYPEOUT
(3) 013706 104405          TYPBN          ;;GO TYPE--BINARY ASCII
(1) 013710 013700 000042 $GET42: MOV      @#42,R0      ;;GET MONITOR ADDRESS
(1) 013714 001405          BEQ      $DOAGN          ;;BRANCH IF NO MONITOR
(1) 013716 000005          RESET          ;;CLEAR THE WORLD
(1) 013720 004710          $ENDAD: JSR     PC,(R0)      ;;GO TO MONITOR
(1) 013722 000240          NOP          ;;SAVE ROOM
(1) 013724 000240          NOP          ;;FOR
(1) 013726 000240          NOP          ;;ACT11
(1) 013730          $DOAGN:          JMP      @(PC)+          ;;RETURN
(1) 013730 000137          $RTNAD: .WORD   LOOP
(1) 013732 002334          $ENULL: .BYTE  -1,-1,0      ;;NULL CHARACTER STRING
(1) 013734 377 377 000 .EVEN

1411          ;
1412          ;
1413          ; THIS ROUTINE TYPES LAST MESSAGE AND WAITS FOR AN OPERATOR
1414          ; RESPONCE.
1415          ;
1416          ;
1417 013740 105777 165202 ANYKEY: TSTB   @$TKB          ;CLEAR TTY READY FLAG.
1418 013744 104401 013752 TYPE      ,65$          ;;TYPE ASCIZ STRING
(1) 013750 000430          BR      64$          ;;GET OVER THE ASCIZ
(1) 014032          ;;65$: .ASCIZ <200><7>#SWITCH ST1 3 TIMES,TYPE ANY KEY WHEN DONE..#<7>
(1) 014032          64$:
1419          ;
1420 014032 105777 165106 1$: TSTB   @$TKS          ;WAIT FOR OPERATOR.
1421 014036 100375          BPL     1$
1422 014040 105777 165102 TSTB   @$TKB          ;CLEAR TTY READY FLAG.
1423 014044 000207          RTS PC
1443
```

1445
1446
1447
1448
(1)
(1)
(1)
(1)
(1)
(1)
(1)
(1)
(1)
(1)
(1)
(1)
(1)
1449
1450
1451
1452
1453
1454
1455
1456
1457
1458
1459
1460
1461
1462
1463
1464
1465
1466
1467
1468
1469
1470
1471

```
.SBTTL          : I/O SIGNAL TEST #1 ST1 IN AND ST2 OUT IN AND OUT
                :
                : SWITCH PACK S2 MUST BE SET UP AS FOLLOWS:
                :
                : SWITCH  1 - OFF
                :           2 - ON
                :           3 - OFF
                :           4 - OFF
                :           5 - ON
                :           6 - ON
                :           7 - NOT USED
                :
                : THIS SELECTS TTL THRESHOLDS AND POSITIVE SLOPE FOR
                : SCHMITT TRIGGER 1.
                :
                : PLEASE REMOVE ANY PREVIOUS JUMPER.
                :
                : JUMPER THE FOLLOWING PINS TOGETHER:
                :
                : J1 - SS (ST2 OUT)      TO J1 - VV (ST1-IN)
                :
                : LOAD AND START AT LOCATION 210
                : END PASSES OCCUR IMMEDIATELY AND ARE NOT REPORTED
                : ERRORS ARE REPORTED AS IN THE REGULAR LOGIC TEST AND
                : THEIR PRINTOUT MAY BE INHIBITED
```

```
1458 014046 012737 014060 001420 OITST1: MOV #IOTST1,$TMP0 ;LOAD RETURN ADDRESS
1459 014054 000137 001526          JMP INIT ;PRIME THE PROGRAM VECTOR SPACE
1460 014060 104407          IOTST1: CKSWR ;CHECK THE SWR
1461 014062 005077 165310 1$: CLR @ASR ;CLEAR THE CSR
1462 014066 005077 165306          CLR @ABR ;CLEAR THE BUFFER REG.
1463 014072 012777 000061 165276          MOV #61,@ASR ;RATE ST1, MODE 0, GO.
1464 014100 052777 001000 165270          BIS #BIT9,@ASR ;GENERATE A MAINTENANCE ST2.
1465 014106 012777 000005 165262          MOV #5,@ASR ;NOW SET TO READ COUNT REG
1466 014114 052777 001000 165254          BIS #BIT9,@ASR ;FORCE COUNT -> BUFFER REG.
1467 014122 027727 165252 000001          CMP @ABR,#1 ;DID COUNT REG ADVANCE ONCE?
1468 014130 001753          BEQ IOTST1 ;YES - LOOP.
1469 014132 104000          ERROR ;ST2 OUT TO ST1 IN FAILED.
1470 014134 000751          BR IOTST1
```

1473
 1474
 1475
 1476
 (1)
 (1)
 (1)
 (1)
 (1)
 (1)
 (1)
 (1)
 (1)
 (1)
 (1)
 (1)
 (1)
 (1)
 1477
 1478
 1479
 1480
 1481
 1482
 1483
 1484
 1485
 1486
 1487
 1488
 1489
 1490
 1491
 1492
 1493
 1494
 1495
 1496
 1497
 1498
 1499

.SBTTL ;I/O SIGNAL TEST #2 CLOCK OVFLOW OUT TEST.

SWITCH PACK S2 MUST BE SET UP AS FOLLOWS:

- SWITCH 1 - OFF
- 2 - OFF
- 3 - OFF
- 4 - ON
- 5 - OFF
- 6 - ON
- 7 - NOT USED

THIS SELECTS TTL THRESHOLDS AND POSITIVE SLOPE FOR SCHMITT TRIGGER 2.

PLEASE REMOVE ANY PREVIOUS JUMPER.

JUMPER THE FOLLOWING PINS TOGETHER:

J1 - RR (CLK OV) TO J1 - TT (ST2-IN)

LOAD AND START AT LOCATION 214.
 END PASSES OCCUR IMMEDIATELY AND ARE NOT REPORTED.
 ERRORS ARE REPORTED AS IN TH REGULAR LOGIC TEST AND
 THEIR PRINTOUT MAY BE INHIBITED.

```

1486 014136 012737 014150 001420 0ITST2: MOV #IOTST2,$TMP0 ;LOAD RETURN ADDRESS
1487 014144 000137 001526          JMP INIT ;PRIME THE PROGRAM VECTOR SPACE
1488 014150 104407          IOTST2: CKSWR ;CHECK THE SWR.
1489 014152 005077 165220          CLR @ASR ;CLEAR THE CSR.
1490 014156 012777 177777 165214          MOV #-1,@ABR ;PRELOAD PRESET BUFFER.
1491 014164 012777 000063 165204          MOV #63,@ASR ;RATE ST1, MODE 1, GO.
1492 014172 052777 000400 165176          BIS #BIT8,@ASR ;GENERATE A MAIN. ST1.
1493 014200 000240          NOP
1494 014202 000240          NOP
1495 014204 005777 165166          TST @ASR ;DID OVERFLOW SET ST2 FLAG?
1496 014210 100757          BMI IOTST2 ;YES - LOOP
1497 014212 104000          ERROR ;CLK OV OUT TO ST2 IN FAILED.
1498 014214 000755          BR IOTST2 ;LOOP
    
```

```

1501
1502          .SBTTL          :I/O SIGNAL TEST #3 ST1 OUT AND ST2 IN
1503
1504
1505
1506          :SWITCH PACK S2 MUST BE SET UP AS FOLLOWS:
1507          SWITCH 1 - OFF
1508          SWITCH 2 - OFF
1509          SWITCH 3 - OFF
1510          SWITCH 4 - ON
1511          SWITCH 5 - ON
1512          SWITCH 6 - ON
1513          SWITCH 7 - NOT USED
1514          :THIS SELECTS TTL THRESHOLD AND POSITIVE SLOPE FOR
1515          :SCHMITT TRIGGER 2.
1516
1517          :PLEASE REMOVE ANY PREVIOUS JUMPERS.
1518
1519          :JUMPER THE FOLLOWING PINS TOGETHER:
1520          :      J1 - UU (ST1 OUT)          TO J1 - TT (ST2-IN)
1521
1522          :LOAD AND START AT LOCATION 220
1523          :END PASSES OCCUR IMMEDIATELY AND ARE NOT REPORTED
1524          :ERRORS ARE REPORTED AS IN THE REGULAR LOGIC TEST AND
1525          :THEIR PRINTOUT MAY BE INHIBITED
1526
1527 014216 012737 014230 001420 0ITST3: MOV #IOTST3,$TMP0 ;LOAD RETURN ADDRESS
1528 014224 000137 001526          JMP INIT ;PRIME THE PROGRAM VECTOR SPACE
1529 014230 104407          IOTST3: CKSWR ;CHECK THE SWR
1530 014232 012777 000001 165136          MOV #1,@ASR ;SET GO BIT.
1531 014240 052777 000400 165130          BIS #BIT8,@ASR ;GENERATE A MAIN. ST1.
1532 014246 005777 165124          TST @ASR ;DID ST2 FLAG SET?
1533 014252 100401          BMI 1$ ;ST1 OUT TO ST2 IN FAILED
1534 014254 104000          ERROR
1535
1536 014256 032777 010000 165112 1$: BIT #BIT12,@ASR ;DID 'FOR' BIT SET?
1537 014264 001761          BEQ IOTST3 ;NO - GOOD!
1538 014266 104000          ERROR ;'FOR' BIT SET ON ONLY 1 ST2.
1539 014270 000757          BR IOTST3 ;LOOP
    
```



```
(1) 014420 100016          BPL      7$          ::BR IF NO
(1) 014422 042703 177770  BIC      #177770,R3  ::GET RID OF JUNK
(1) 014426 001002          BNE      4$          ::TEST FOR 0
(1) 014430 005704          TST      R4          ::SUPPRESS THIS 0?
(1) 014432 001403          BEQ      5$          ::BR IF YES
(1) 014434 005204          4$: INC      R4          ::DON'T SUPPRESS ANYMORE 0'S
(1) 014436 052703 000060  BIS      #'0,R3     ::MAKE THIS DIGIT ASCII
(1) 014442 052703 000040  5$: BIS      #' ,R3     ::MAKE ASCII IF NOT ALREADY
(1) 014446 110337 014512  MOV      R3,8$      ::SAVE FOR TYPING
(1) 014452 104401 014512  TYPE     ,8$      ::GO TYPE THIS DIGIT
(1) 014456 105337 014514  7$: DECB   $OCNT     ::COUNT BY 1
(1) 014462 003347          BGT      2$          ::BR IF MORE TO DO
(1) 014464 002402          BLT      6$          ::BR IF DONE
(1) 014466 005204          INC      R4          ::INSURE LAST DIGIT ISN'T A BLANK
(1) 014470 000744          BR       2$          ::GO DO THE LAST DIGIT
(1) 014472 012605          6$: MOV      (SP)+,R5  ::RESTORE R5
(1) 014474 012604          MOV      (SP)+,R4  ::RESTORE R4
(1) 014476 012603          MOV      (SP)+,R3  ::RESTORE R3
(1) 014500 016666 000002 000004  MOV      2(SP),4(SP) ::SET THE STACK FOR RETURNING
(1) 014506 012616          MOV      (SP)+,(SP)
(1) 014510 000002          RTI          ::RETURN
(1) 014512 000          8$: .BYTE   0          ::STORAGE FOR ASCII DIGIT
(1) 014513 000          .BYTE   0          ::TERMINATOR FOR TYPE ROUTINE
(1) 014514 000          $OCNT: .BYTE   0          ::OCTAL DIGIT COUNTER
(1) 014515 000          $OFILL: .BYTE   0          ::ZERO FILL SWITCH
(1) 014516 000000          $OMODE: .WORD   0          ::NUMBER OF DIGITS TO TYPE
1547 .SBTTL  BINARY TO ASCII AND TYPE ROUTINE
```

```
(1)
(2)
(1) ::*****
(1) ::*THIS ROUTINE IS USED TO CHANGE A 16-BIT BINARY NUMBER TO A 16-BIT
(1) ::*BINARY-ASCII NUMBER AND TYPE IT.
(1) ::*CALL:
(1) ::*   MOV      NUMBER,-(SP)  ::NUMBER TO BE TYPED
(1) ::*   TYPBN          ::TYPE IT
(1)
(1) 014520 010146          $TYPBN: MOV      R1,-(SP)  ::SAVE R1 ON THE STACK
(1) 014522 016601 000006  MOV      6(SP),R1    ::GET THE INPUT NUMBER
(1) 014526 000261          SEC          ::SET 'C' SO CAN KEEP TRACK OF THE NUMBER OF BITS
(1) 014530 112737 000060 014572  1$: MOV      #'0,$BIN   ::SET CHARACTER TO AN ASCII '0'.
(1) 014536 006101          ROL      R1          ::GET THIS BIT
(1) 014540 001406          BEQ      2$          ::DONE?
(1) 014542 105537 014572  ADCB     $BIN        ::NO--SET THE CHARACTER EQUAL TO THIS BIT
(1) 014546 104401 014572  TYPE     , $BIN     ::GO TYPE THIS BIT
(1) 014552 000241          CLC          ::CLEAR 'C' SO CAN KEEP TRACK OF BITS
(1) 014554 000765          BR       1$          ::GO DO THE NEXT BIT
(1) 014556 012601          2$: MOV      (SP)+,R1  ::POP THE STACK INTO R1
(1) 014560 016666 000002 000004  MOV      2(SP),4(SP) ::ADJUST THE STACK
(1) 014566 012616          MOV      (SP)+,(SP)
(1) 014570 000002          RTI          ::RETURN TO USER
(1) 014572 000          000          $BIN: .BYTE   0,0     ::STORAGE FOR ASCII CHAR. AND TERMINATOR
```

```
1548
1559
1560 .SBTTL  ERROR HANDLER ROUTINE
(1)
(2)
(1) ::*****
(1) ::*THIS ROUTINE WILL INCREMENT THE ERROR FLAG AND THE ERROR COUNT.
```

```
(1) ;*SAVE THE ERROR ITEM NUMBER AND THE ADDRESS OF THE ERROR CALL
(1) ;*AND GO TO $ERRTYP ON ERROR
(1) ;*THE SWITCH OPTIONS PROVIDED BY THIS ROUTINE ARE:
(1) ;*SW15=1 HALT ON ERROR
(1) ;*SW13=1 INHIBIT ERROR TYPEOUTS
(1) ;*SW10=1 BELL ON ERROR
(1) ;*SW09=1 LOOP ON ERROR
(1) ;*CALL
(1) ;* ERROR N ;;ERROR=EMT AND N=ERROR ITEM NUMBER
(1) $ERROR:
(1) 014574 104407 CKSWR ;;TEST FOR CHANGE IN SOFT-SWR
(1) 014574 104407 7$: INCB $ERFLG ;;SET THE ERROR FLAG
(1) 014576 105237 001103 BEQ 7$ ;;DON'T LET THE FLAG GO TO ZERO
(1) 014602 001775 MOV $TSTNM,@DISPLAY ;;DISPLAY TEST NUMBER AND ERROR FLAG
(1) 014604 013777 001102 164330 BIT #BIT10,@SWR ;;BELL ON ERROR?
(1) 014612 032777 002000 164320 BEQ 1$ ;;NO - SKIP
(1) 014620 001402 TYPE $BELL ;;RING BELL
(1) 014622 104401 001164 INC $ERTTL ;;COUNT THE NUMBER OF ERRORS
(1) 014626 005237 001112 1$: MOV (SP),$ERRPC ;;GET ADDRESS OF ERROR INSTRUCTION
(1) 014632 011637 001116 SUB #2,$ERRPC
(1) 014636 162737 000002 001116 MOVVB @ $ERRPC,$ITEMB ;;STRIP AND SAVE THE ERROR ITEM CODE
(1) 014644 117737 164246 001114 BIT #BIT13,@SWR ;;SKIP TYPEOUT IF SET
(1) 014652 032777 020000 164260 BNE 20$ ;;SKIP TYPEOUTS
(1) 014660 001004 JSR PC,$ERRTYP ;;GO TO USER ERROR ROUTINE
(1) 014662 004737 015002 TYPE $CRLF
(1) 014666 104401 001171 20$: CMPB #APTENV,$ENV ;;RUNNING IN APT MODE
(1) 014672 122737 000001 001214 BNE 2$ ;;NO,SKIP APT ERROR REPORT
(1) 014700 001007 MOVVB $ITEMB,21$ ;;SET ITEM NUMBER AS ERROR NUMBER
(1) 014702 113737 001114 014714 JSR PC,$ATY4 ;;REPORT FATAL ERROR TO APT
(1) 014710 004737 016474 21$: .BYTE 0
(1) 014714 000 .BYTE 0
(1) 014715 000 BR 22$ ;;APT ERROR LOOP
(1) 014716 000777 22$: TST @SWR ;;HALT ON ERROR
(1) 014720 005777 164214 2$: BPL 3$ ;;SKIP IF CONTINUE
(1) 014724 100002 HALT ;;HALT ON ERROR!
(1) 014726 000000 CKSWR ;;TEST FOR CHANGE IN SOFT-SWR
(1) 014730 104407 3$: BIT #BIT09,@SWR ;;LOOP ON ERROR SWITCH SET?
(1) 014732 032777 001000 164200 BEQ 4$ ;;BR IF NO
(1) 014740 001402 MOV $LPERR,(SP) ;;FUDGE RETURN FOR LOOPING
(1) 014742 013716 001110 4$: TST $ESCAPE ;;CHECK FOR AN ESCAPE ADDRESS
(1) 014746 005737 001162 BEQ 5$ ;;BR IF NONE
(1) 014752 001402 MOV $ESCAPE,(SP) ;;FUDGE RETURN ADDRESS FOR ESCAPE
(1) 014754 013716 001162 5$:
(1) 014760 001432 INC ERCNT ;/UPDATE ERROR COUNT.
(3) 014760 005237 001432 BNE 10$ ;/BUT DON'T LET IT OVERFLOW.
(3) 014764 001002 DEC ERCNT ;/KEEP AT 177777 IF OVERFLOW.
(3) 014766 005337 001432 10$: BIC ROTATE,UTEST ;/REMOVE UNIT FROM LIST OF GOOD ONES.
(3) 014772 043737 001426 001430 RTI ;/EXIT.
(3) 015000 000002
1561 .SBTTL ERROR MESSAGE TYPEOUT ROUTINE
(1) ;:*****
(2)
```

(1)
(1)
(1)
(1)
(1) 015002
(1) 015002 104401 001171
(1) 015006 010046
(1) 015010 005000
(1) 015012 153700 001114
(1) 015016 001004
(1)
(2) 015020 013746 001116
(2)
(2) 015024 104402
(1) 015026 000426
(1) 015030 005300
(1) 015032 006300
(1) 015034 006300
(1) 015036 006300
(1) 015040 062700 001256
(1) 015044 012037 015054
(1) 015050 001404
(1) 015052 104401
(1) 015054 000000
(1) 015056 104401 001171
(1) 015062 012037 015072
(1) 015066 001404
(1) 015070 104401
(1) 015072 000000
(1) 015074 104401 001171
(1) 015100 011000
(1) 015102 001004
(1) 015104 012600
(1) 015106 104401 001171
(1) 015112 000207
(1) 015114
(2) 015114 013046
(2) 015116 104402
(1) 015120 005710
(1) 015122 001770
(1) 015124 104401 015132
(1) 015130 000771
(1) 015132 020040 000
(1)
1562
(1)
(2)
(1)
(1)
(1)
(1)
(1)
(1)
(1)

;
*THIS ROUTINE USES THE 'ITEM CONTROL BYTE' (\$ITEMB) TO DETERMINE WHICH
*ERROR IS TO BE REPORTED. IT THEN OBTAINS, FROM THE 'ERROR TABLE' (\$ERRTB),
*AND REPORTS THE APPROPRIATE INFORMATION CONCERNING THE ERROR.

```
$ERRTYP:
      TYPE      , $CRLF      ;; 'CARRIAGE RETURN' & 'LINE FEED'
      MOV      R0,-(SP)      ;; SAVE R0
      CLR      R0            ;; PICKUP THE ITEM INDEX
      BISB     @#$ITEMB,R0
      BNE     1$            ;; IF ITEM NUMBER IS ZERO, JUST
                        ;; TYPE THE PC OF THE ERROR
      MOV     $ERRPC,-(SP)   ;; SAVE $ERRPC FOR TIMEOUT
                        ;; ERROR ADDRESS
                        ;; GO TYPE--OCTAL ASCII(ALL DIGITS)
      TYPCC
      BR      6$            ;; GET OUT
1$:   DEC     R0            ;; ADJUST THE INDEX SO THAT IT WILL
      ASL     R0            ;; WORK FOR THE ERROR TABLE
      ASL     R0
      ASL     R0
      ADD     #$ERRTB,R0    ;; FORM TABLE POINTER
      MOV     (R0)+,2$      ;; PICKUP 'ERROR MESSAGE' POINTER
      BEQ     3$            ;; SKIP TIMEOUT IF NO POINTER
      TYPE
                        ;; TYPE THE 'ERROR MESSAGE'
                        ;; 'ERROR MESSAGE' POINTER GOES HERE
2$:   .WORD   0            ;; 'CARRIAGE RETURN' & 'LINE FEED'
      TYPE   , $CRLF      ;; PICKUP 'DATA HEADER' POINTER
3$:   MOV     (R0)+,4$      ;; SKIP TIMEOUT IF 0
      BEQ     5$            ;; TYPE THE 'DATA HEADER'
      TYPE
                        ;; 'DATA HEADER' POINTER GOES HERE
4$:   .WORD   0            ;; 'CARRIAGE RETURN' & 'LINE FEED'
      TYPE   , $CRLF      ;; PICKUP 'DATA TABLE' POINTER
5$:   MOV     (R0),R0       ;; GO TYPE THE DATA
      BNE     7$            ;; RESTORE R0
6$:   MOV     (SP)+,R0      ;; 'CARRIAGE RETURN' & 'LINE FEED'
      TYPE   , $CRLF      ;; RETURN
      RTS     PC
7$:   MOV     @(R0)+,-(SP)  ;; SAVE @(R0)+ FOR TIMEOUT
      TYPCC
                        ;; GO TYPE--OCTAL ASCII(ALL DIGITS)
      TST     (R0)         ;; IS THERE ANOTHER NUMBER?
      BEQ     6$            ;; BR IF NO
      TYPE   , 8$         ;; TYPE TWO(2) SPACES
      BR      7$            ;; LOOP
8$:   .ASCIIZ / /         ;; TWO(2) SPACES
      .EVEN
      .SBTTL SCOPE HANDLER ROUTINE
```

```
*****
*THIS ROUTINE CONTROLS THE LOOPING OF SUBTESTS. IT WILL INCREMENT
*AND LOAD THE TEST NUMBER($STNM) INTO THE DISPLAY REG.(DISPLAY<7:0>)
*AND LOAD THE ERROR FLAG ($ERFLG) INTO DISPLAY<15:08>
*THE SWITCH OPTIONS PROVIDED BY THIS ROUTINE ARE:
*SW14=1      LOOP ON TEST
*SW11=1      INHIBIT ITERATIONS
*SW09=1      LOOP ON ERROR
*SW08=1      LOOP ON TEST IN SWR<7:0>
*CALL
```

```
(1)          ;*      SCOPE          ;;SCOPE=10T
(1)          $SCOPE:
(1) 015136   CKSWR          ;;TEST FOR CHANGE IN SOFT-SWR
(1) 015136 104407          CKSWR
(2) 015140 104407          1$: BIT #BIT14,@SWR          ;;LOOP ON PRESENT TEST?
(1) 015142 032777 040000 163770 BNE $OVER          ;;YES IF SW14=1
(1) 015150 001114          ;#####START OF CODE FOR THE XOR TESTER#####
(1) 015152 000416          $XTSTR: BR 6$          ;;IF RUNNING ON THE 'XOR' TESTER CHANGE
(1)          MOV @#ERRVEC,-(SP)          ;;THIS INSTRUCTION TO A 'NOP' (NOP=240)
(1) 015154 013746 000004          MOV #5$,@#ERRVEC          ;;SAVE THE CONTENTS OF THE ERROR VECTOR
(1) 015160 012737 015200 000004          TST @#177060          ;;SET FOR TIMEOUT
(1) 015166 005737 177060          MOV (SP)+,@#ERRVEC          ;;TIME OUT ON XOR?
(1) 015172 012637 000004          BR $SVLAD          ;;RESTORE THE ERROR VECTOR
(1) 015176 000463          5$: CMP (SP)+,(SP)+          ;;GO TO THE NEXT TEST
(1) 015200 022626          MOV (SP)+,@#ERRVEC          ;;CLEAR THE STACK AFTER A TIME OUT
(1) 015202 012637 000004          BR 7$          ;;RESTORE THE ERROR VECTOR
(1) 015206 000423          6$:#####END OF CODE FOR THE XOR TESTER#####
(1) 015210 032777 000400 163722          BIT #BIT08,@SWR          ;;LOOP ON SPEC. TEST?
(1) 015216 001404          BEQ 2$          ;;BR IF NO
(1) 015220 127737 163714 001102          CMPB @SWR,$STNM          ;;ON THE RIGHT TEST? SWR<7:0>
(1) 015226 001465          BEQ $OVER          ;;BR IF YES
(1) 015230 105737 001103          2$: TSTB $ERFLG          ;;HAS AN ERROR OCCURRED?
(1) 015234 001421          BEQ 3$          ;;BR IF NO
(1) 015236 123737 001115 001103          CMPB $ERMAX,$ERFLG          ;;MAX. ERRORS FOR THIS TEST OCCURRED?
(1) 015244 101015          BHI 3$          ;;BR IF NO
(1) 015246 032777 001000 163664          BIT #BIT09,@SWR          ;;LOOP ON ERROR?
(1) 015254 001404          BEQ 4$          ;;BR IF NO
(1) 015256 013737 001110 001106          7$: MOV $LPERR,$LPADR          ;;SET LOOP ADDRESS TO LAST SCOPE
(1) 015264 000446          BR $OVER
(1) 015266 105037 001103          4$: CLRB $ERFLG          ;;ZERO THE ERROR FLAG
(1) 015272 005037 001160          CLR $TIMES          ;;CLEAR THE NUMBER OF ITERATIONS TO MAKE
(1) 015276 000415          BR 1$          ;;ESCAPE TO THE NEXT TEST
(1) 015300 032777 004000 163632          3$: BIT #BIT11,@SWR          ;;INHIBIT ITERATIONS?
(1) 015306 001011          BNE 1$          ;;BR IF YES
(1) 015310 005737 001202          TST $PASS          ;;IF FIRST PASS OF PROGRAM
(1) 015314 001406          BEQ 1$          ;;INHIBIT ITERATIONS
(1) 015316 005237 001104          INC $ICNT          ;;INCREMENT ITERATION COUNT
(1) 015322 023737 001160 001104          CMP $TIMES,$ICNT          ;;CHECK THE NUMBER OF ITERATIONS MADE
(1) 015330 002024          BGE $OVER          ;;BR IF MORE ITERATION REQUIRED
(1) 015332 012737 000001 001104          1$: MOV #1,$ICNT          ;;REINITIALIZE THE ITERATION COUNTER
(1) 015340 013737 015416 001160          MOV $MXCNT,$TIMES          ;;SET NUMBER OF ITERATIONS TO DO
(1) 015346 105237 001102          $SVLAD: INCB $STNM          ;;COUNT TEST NUMBERS
(1) 015352 113737 001102 001200          MOVB $STNM,$STEN          ;;SET TEST NUMBER IN APT MAILBOX
(1) 015360 011637 001106          MOV (SP),$LPADR          ;;SAVE SCOPE LOOP ADDRESS
(1) 015364 011637 001110          MOV (SP),$LPERR          ;;SAVE ERROR LOOP ADDRESS
(1) 015370 005037 001162          CLR $ESCAPE          ;;CLEAR THE ESCAPE FROM ERROR ADDRESS
(1) 015374 112737 000001 001115          MOVB #1,$ERMAX          ;;ONLY ALLOW ONE(!) ERROR ON NEXT TEST
(1) 015402 013777 001102 163532          $OVER: MOV $STNM,@DISPLAY          ;;DISPLAY TEST NUMBER
(1) 015410 013716 001106          MOV $LPADR,(SP)          ;;FUDGE RETURN ADDRESS
(1) 015414 000002          RTI          ;;FIXES PS
(1) 015416 003720          $MXCNT: 2000          ;;MAX. NUMBER OF ITERATIONS
```

1563
(1)
(2)

;;*****

.SBTTL TTY INPUT ROUTINE

```

(1) .ENABL LSB
(1)
(2) ::*****
(1) ::SOFTWARE SWITCH REGISTER CHANGE ROUTINE.
(1) ::ROUTINE IS ENTERED FROM THE TRAP HANDLER, AND WILL
(1) ::SERVICE THE TEST FOR CHANGE IN SOFTWARE SWITCH REGISTER TRAP CALL
(1) ::WHEN OPERATING IN TTY FLAG MODE.
(1) 015420 022737 000176 001140 $CKSWR: CMP #SWREG,SWR ::IS THE SOFT-SWR SELECTED?
(1) 015426 001074 BNE 15$ ::BRANCH IF NO
(1) 015430 105777 163510 TSTB @STKS ::CHAR THERE?
(1) 015434 100071 BPL 15$ ::IF NO, DON'T WAIT AROUND
(1) 015436 117746 163504 MOVB @STKB,-(SP) ::SAVE THE CHAR
(1) 015442 042716 177600 BIC #^C177,(SP) ::STRIP-OFF THE ASCII
(1) 015446 022726 000007 CMP #7,(SP)+ ::IS IT A CONTROL G?
(1) 015452 001062 BNE 15$ ::NO, RETURN TO USER
(1) 015454 123727 001134 000001 CMPB $AUTOB,#1 ::ARE WE RUNNING IN AUTO-MODE?
(1) 015462 001456 BEQ 15$ ::BRANCH IF YES
(1)
(1) 015464 104401 016145 $GTSWR: TYPE ,SCNTLG ::ECHO THE CONTROL-G (^G)
(1) 015470 104401 016152 TYPE ,SMSWR ::TYPE CURRENT CONTENTS
(2) 015474 013746 000176 MOV SWREG,-(SP) ::SAVE SWREG FOR TYPEOUT
(2) 015500 104402 TYPOC ::GO TYPE--OCTAL ASCII(ALL DIGITS)
(1) 015502 104401 016163 TYPE ,SMNEW ::PROMPT FOR NEW SWR
(1) 015506 005046 19$: CLR -(SP) ::CLEAR COUNTER
(1) 015510 005046 CLR -(SP) ::THE NEW SWR
(1) 015512 105777 163426 7$: TSTB @STKS ::CHAR THERE?
(1) 015516 100375 BPL 7$ ::IF NOT TRY AGAIN
(1)
(1) 015520 117746 163422 MOVB @STKB,-(SP) ::PICK UP CHAR
(1) 015524 042716 177600 BIC #^C177,(SP) ::MAKE IT 7-BIT ASCII
(1)
(1)
(1) 015530 021627 000025 9$: CMP (SP),#25 ::IS IT A CONTROL-U?
(1) 015534 001005 BNE 10$ ::BRANCH IF NOT
(1) 015536 104401 016140 TYPE ,SCNTLU ::YES, ECHO CONTROL-U (^U)
(1) 015542 062706 000006 20$: ADD #6,SP ::IGNORE PREVIOUS INPUT
(1) 015546 000757 BR 19$ ::LET'S TRY IT AGAIN
(1)
(1)
(1) 015550 021627 000015 10$: CMP (SP),#15 ::IS IT A <CR>?
(1) 015554 001022 BNE 16$ ::BRANCH IF NO
(1) 015556 005766 000004 TST 4(SP) ::YES, IS IT THE FIRST CHAR?
(1) 015562 001403 BEQ 11$ ::BRANCH IF YES
(1) 015564 016677 000002 163346 MOV 2(SP),@SWR ::SAVE NEW SWR
(1) 015572 062706 000006 11$: ADD #6,SP ::CLEAR UP STACK
(1) 015576 104401 001171 14$: TYPE ,SCRLF ::ECHO <CR> AND <LF>
(1) 015602 123727 001135 000001 CMPB $INTAG,#1 ::RE-ENABLE TTY KBD INTERRUPTS?
(1) 015610 001003 BNE 15$ ::BRANCH IF NOT
(1) 015612 012777 000100 163324 MOV #100,@STKS ::RE-ENABLE TTY KBD INTERRUPTS
(1) 015620 000002 15$: RTI ::RETURN
(1) 015622 004737 016406 16$: JSR PC,$TYPEC ::ECHO CHAR
(1) 015626 021627 000060 CMP (SP),#60 ::CHAR < 0?
(1) 015632 002420 BLT 18$ ::BRANCH IF YES
(1) 015634 021627 000067 CMP (SP),#67 ::CHAR > 7?
(1) 015640 003015 BGT 18$ ::BRANCH IF YES
    
```

```

(1) 015642 042726 000060      BIC    #60,(SP)+    ;;STRIP-OFF ASCII
(1) 015646 005766 000002      TST    2(SP)        ;;IS THIS THE FIRST CHAR
(1) 015652 001403              BEQ    17$          ;;BRANCH IF YES
(1) 015654 006316              ASL    (SP)         ;;NO, SHIFT PRESENT
(1) 015656 006316              ASL    (SP)         ;;  CHAR OVER TO MAKE
(1) 015660 006316              ASL    (SP)         ;;  ROOM FOR NEW ONE.
(1) 015662 005266 000002      17$:  INC    2(SP)        ;;KEEP COUNT OF CHAR
(1) 015666 056616 177776      BIS    -2(SP),(SP) ;;SET IN NEW CHAR
(1) 015672 000707              BR     7$          ;;GET THE NEXT ONE
(1) 015674 104401 001170      18$:  TYPE  $QUES     ;;TYPE ?<CR><LF>
(1) 015700 000720              BR     20$        ;;SIMULATE CONTROL-U
(1)                               .DSABL  LSB
    
```

 ;*THIS ROUTINE WILL INPUT A SINGLE CHARACTER FROM THE TTY
 ;*CALL:
 ;*

```

(1)                               ;* RDCHR          ;;INPUT A SINGLE CHARACTER FROM THE TTY
(1)                               ;* RETURN HERE    ;;CHARACTER IS ON THE STACK
(1)                               ;*                ;;WITH PARITY BIT STRIPPED OFF
(1)                               ;*
    
```

```

(1) 015702 011646              $RDCHR: MOV    (SP),-(SP)    ;;PUSH DOWN THE PC
(1) 015704 016666 000004 000002  MOV    4(SP),2(SP)    ;;SAVE THE PS
(1) 015712 105777 163226      1$:  TSTB   @TKS        ;;WAIT FOR
(1) 015716 100375              BPL    1$          ;;A CHARACTER
(1) 015720 117766 163222 000004  MOVB   @TKB,4(SP)    ;;READ THE TTY
(1) 015726 042766 177600 000004  BIC    #^C<177>,4(SP) ;;GET RID OF JUNK IF ANY
(1) 015734 026627 000004 000023  CMP    4(SP),#23     ;;IS IT A CONTROL-S?
(1) 015742 001013              BNE    3$          ;;BRANCH IF NO
(1) 015744 105777 163174      2$:  TSTB   @TKS        ;;WAIT FOR A CHARACTER
(1) 015750 100375              BPL    2$          ;;LOOP UNTIL ITS THERE
(1) 015752 117746 163170      MOVB   @TKB,-(SP)    ;;GET CHARACTER
(1) 015756 042716 177600      BIC    #^C177,(SP)  ;;MAKE IT 7-BIT ASCII
(1) 015762 022627 000021      CMP    (SP)+,#21    ;;IS IT A CONTROL-Q?
(1) 015766 001366              BNE    2$          ;;IF NOT DISCARD IT
(1) 015770 000750              BR     1$          ;;YES, RESUME
(1) 015772 026627 000004 000140  3$:  CMP    4(SP),#140  ;;IS IT UPPER CASE?
(1) 016000 002407              BLT    4$          ;;BRANCH IF YES
(1) 016002 026627 000004 000175  CMP    4(SP),#175   ;;IS IT A SPECIAL CHAR?
(1) 016010 003003              BGT    4$          ;;BRANCH IF YES
(1) 016012 042766 000040 000004  BIC    #40,4(SP)    ;;MAKE IT UPPER CASE
(1) 016020 000002              4$:  RTI             ;;GO BACK TO USER
    
```

 ;*THIS ROUTINE WILL INPUT A STRING FROM THE TTY
 ;*CALL:
 ;*

```

(1)                               ;* RDLIN          ;;INPUT A STRING FROM THE TTY
(1)                               ;* RETURN HERE    ;;ADDRESS OF FIRST CHARACTER WILL BE ON THE STACK
(1)                               ;*                ;;TERMINATOR WILL BE A BYTE OF ALL 0'S
    
```

```

(1) 016022 010346              $RDLIN: MOV    R3,-(SP)    ;;SAVE R3
(1) 016024 012703 016130      1$:  MOV    #$TTYIN,R3  ;;GET ADDRESS
(1) 016030 022703 016140      2$:  CMP    #$TTYIN+8.,R3 ;;BUFFER FULL?
(1) 016034 101405              BLOS   4$          ;;BR IF YES
(1) 016036 104410              RDCHR  ;;GO READ ONE CHARACTER FROM THE TTY
(1) 016040 112613              MOVB   (SP)+,(R3)   ;;GET CHARACTER
    
```

```
(1) 016042 122713 000177 10$: CMPB #177,(R3) ;;IS IT A RUBOUT
(1) 016046 001003 BNE 3$ ;;SKIP IF NOT
(1) 016050 104401 001170 4$: TYPE ,SQUES ;;TYPE A '?'
(1) 016054 000763 BR 1$ ;;CLEAR THE BUFFER AND LOOP
(1) 016056 111337 016126 3$: MOVB (R3),9$ ;;ECHO THE CHARACTER
(1) 016062 104401 016126 TYPE ,9$
(1) 016066 122723 000015 CMPB #15,(R3)+ ;;CHECK FOR RETURN
(1) 016072 001356 BNE 2$ ;;LOOP IF NOT RETURN
(1) 016074 105063 177777 CLRB -1(R3) ;;CLEAR RETURN (THE 15)
(1) 016100 104401 001172 TYPE ,SLF ;;TYPE A LINE FEED
(1) 016104 012603 MOV (SP)+,R3 ;;RESTORE R3
(1) 016106 011646 MOV (SP),-(SP) ;;ADJUST THE STACK AND PUT ADDRESS OF THE
(1) 016110 016666 000004 000002 MOV 4(SP),2(SP) ;; FIRST ASCII CHARACTER ON IT
(1) 016116 012766 016130 000004 MOV #TTYIN,4(SP)
(1) 016124 000002 RTI ;;RETURN
(1) 016126 000 9$: .BYTE 0 ;;STORAGE FOR ASCII CHAR. TO TYPE
(1) 016127 000 .BYTE 0 ;;TERMINATOR
(1) 016130 000010 $TTYIN: .BLKB 8. ;;RESERVE 8 BYTES FOR TTY INPUT
(1) 016140 052536 005015 000 $CNTLU: .ASCIZ /*U/<15><12> ;;CONTROL 'U'
(1) 016145 136 006507 000012 $CNTLG: .ASCIZ /*G/<15><12> ;;CONTROL 'G'
(1) 016152 005015 053523 020122 $MSWR: .ASCIZ <15><12>/SWR = /
(1) 016160 020075 000 $MNEW: .ASCIZ / NEW = /
(1) 016163 040 047040 053505
(1) 016170 036440 000040
```

```
1564
(1) .SBTTL TYPE ROUTINE
(2) *****
(1) *ROUTINE TO TYPE ASCIZ MESSAGE. MESSAGE MUST TERMINATE WITH A 0 BYTE.
(1) *THE ROUTINE WILL INSERT A NUMBER OF NULL CHARACTERS AFTER A LINE FEED.
(1) *NOTE1: $NULL CONTAINS THE CHARACTER TO BE USED AS THE FILLER CHARACTER.
(1) *NOTE2: $FILLS CONTAINS THE NUMBER OF FILLER CHARACTERS REQUIRED.
(1) *NOTE3: $FILLC CONTAINS THE CHARACTER TO FILL AFTER.
(1) *
(1) *CALL:
(1) *1) USING A TRAP INSTRUCTION
(1) * TYPE ,MESADR ;;MESADR IS FIRST ADDRESS OF AN ASCIZ STRING
(1) *OR
(1) * TYPE
(1) * MESADR
(1) *
```

```
(1) 016174 105737 001157 $TYPE: TSTB $TPFLG ;;IS THERE A TERMINAL?
(1) 016200 100002 BPL 1$ ;;BR IF YES
(1) 016202 000000 HALT ;;HALT HERE IF NO TERMINAL
(1) 016204 000430 BR 3$ ;;LEAVE
(1) 016206 010046 1$: MOV R0,-(SP) ;;SAVE R0
(1) 016210 017600 000002 MOV @2(SP),R0 ;;GET ADDRESS OF ASCIZ STRING
(1) 016214 122737 000001 001214 CMPB #APTENV,$ENV ;;RUNNING IN APT MODE
(1) 016222 001011 BNE 62$ ;;NO,GO CHECK FOR APT CONSOLE
(1) 016224 132737 000100 001215 BITB #APTPOOL,$ENVM ;;SPOOL MESSAGE TO APT
(1) 016232 001405 BEQ 62$ ;;NO,GO CHECK FOR CONSOLE
(1) 016234 010037 016244 MOV R0,61$ ;;SETUP MESSAGE ADDRESS FOR APT
(1) 016240 004737 016464 JSR PC,$ATY3 ;;SPOOL MESSAGE TO APT
(1) 016244 000000 61$: .WORD 0 ;;MESSAGE ADDRESS
(1) 016246 132737 000040 001215 62$: BITB #APTCSUP,$ENVM ;;APT CONSOLE SUPPRESSED
(1) 016254 001003 BNE 60$ ;;YES,SKIP TYPE OUT
```

```

(1) 016256 112046      2$:   MOVB   (R0)+,-(SP)   ;;PUSH CHARACTER TO BE TYPED ONTO STACK
(1) 016260 001005      BNE    4$              ;;BR IF IT ISN'T THE TERMINATOR
(1) 016262 005726      TST    (SP)+          ;;IF TERMINATOR POP IT OFF THE STACK
(1) 016264 012600      60$:  MOV    (SP)+,R0    ;;RESTORE R0
(1) 016266 062716 000002 3$:   ADD    #2,(SP)      ;;ADJUST RETURN PC
(1) 016272 000002      RTI                    ;;RETURN
(1) 016274 122716 000011 4$:   CMPB   #HT,(SP)     ;;BRANCH IF <HT>
(1) 016300 001430      BEQ    8$              ;;BRANCH IF NOT <CRLF>
(1) 016302 122716 000200  CMPB   #CRLF,(SP)
(1) 016306 001006      BNE    5$              ;;POP <CR><LF> EQUIV
(1) 016310 005726      TST    (SP)+          ;;TYPE A CR AND LF
(1) 016312 104401      TYPE
(1) 016314 001171      $CRLF
(1) 016316 105037 016452  CLRB   $CHARCNT      ;;CLEAR CHARACTER COUNT
(1) 016322 000755      BR     2$              ;;GET NEXT CHARACTER
(1) 016324 004737 016406 5$:   JSR    PC,$TYPEPC    ;;GO TYPE THIS CHARACTER
(1) 016330 123726 001156 6$:   CMPB   $FILLC,(SP)+ ;;IS IT TIME FOR FILLER CHARS.?
(1) 016334 001350      BNE    2$              ;;IF NO GO GET NEXT CHAR.
(1) 016336 013746 001154  MOV    $NULL,-(SP)   ;;GET # OF FILLER CHARS. NEEDED
(1)                                ;;AND THE NULL CHAR.
(1) 016342 105366 000001 7$:   DECB   1(SP)        ;;DOES A NULL NEED TO BE TYPED?
(1) 016346 002770      BLT    6$              ;;BR IF NO--GO POP THE NULL OFF OF STACK
(1) 016350 004737 016406  JSR    PC,$TYPEPC    ;;GO TYPE A NULL
(1) 016354 105337 016452  DECB   $CHARCNT      ;;DO NOT COUNT AS A COUNT
(1) 016360 000770      BR     7$              ;;LOOP
(1)
(1)                                ;HORIZONTAL TAB PROCESSOR
(1)
(1) 016362 112716 000040 8$:   MGVB   #' ,(SP)     ;;REPLACE TAB WITH SPACE
(1) 016366 004737 016406 9$:   JSR    PC,$TYPEPC    ;;TYPE A SPACE
(1) 016372 132737 000007 016452 BITB   #7,$CHARCNT   ;;BRANCH IF NOT AT
(1) 016400 001372      BNE    9$              ;;TAB STOP
(1) 016402 005726      TST    (SP)+          ;;POP SPACE OFF STACK
(1) 016404 000724      BR     2$              ;;GET NEXT CHARACTER
(1) 016406 105777 162536 $TYPEPC: TSTB   @STPS     ;;WAIT UNTIL PRINTER IS READY
(1) 016412 100375      BPL    $TYPEPC
(1) 016414 116677 000002 162530 MOVB   2(SP),@STPB    ;;LOAD CHAR TO BE TYPED INTO DATA REG.
(1) 016422 122766 000015 000002 CMPB   #CR,2(SP)     ;;IS CHARACTER A CARRIAGE RETURN?
(1) 016430 001003      BNE    1$              ;;BRANCH IF NO
(1) 016432 105037 016452  CLRB   $CHARCNT      ;;YES--CLEAR CHARACTER COUNT
(1) 016436 000406      BR     $TYPEPC
(1) 016440 122766 000012 000002 1$:   CMPB   #LF,2(SP)    ;;IS CHARACTER A LINE FEED?
(1) 016446 001402      BEQ    $TYPEPC        ;;BRANCH IF YES
(1) 016450 105227      INCB   (PC)+         ;;COUNT THE CHARACTER
(1) 016452 000000      $CHARCNT: .WORD 0    ;;CHARACTER COUNT STORAGE
(1) 016454 000207      $TYPEPC: RTS    PC
(1)
(1)                                .SBTTL  APT COMMUNICATIONS ROUTINE
(1)
(1)                                ;*****
(1) 016456 112737 000001 016722 $ATY1: MOVB   #1,$FFLG  ;;TO REPORT FATAL ERROR
(1) 016464 112737 000001 016720 $ATY3: MOVB   #1,$MFLG  ;;TO TYPE A MESSAGE
(1) 016472 000403      BR     $ATYC
(1) 016474 112737 000001 016722 $ATY4: MOVB   #1,$FFLG  ;;TO ONLY REPORT FATAL ERROR
(1) 016502      $ATYC:
(3) 016502 010046      MOV    R0,-(SP)      ;;PUSH R0 ON STACK

```

```
(3) 016504 010146          MOV      R1,-(SP)          ;;PUSH R1 ON STACK
(1) 016506 105737 016720    TSTB     $MFLG            ;;SHOULD TYPE A MESSAGE?
(1) 016512 001450          BEQ      5$               ;;IF NOT: BR
(1) 016514 122737 000001 001214    CMPB     #APTENV,$ENV     ;;OPERATING UNDER APT?
(1) 016522 001031          BNE      3$               ;;IF NOT: BR
(1) 016524 132737 000100 001215    BITB     #APTSPOOL,$ENVM ;;SHOULD SPOOL MESSAGES?
(1) 016532 001425          BEQ      3$               ;;IF NOT: BR
(1) 016534 017600 000004          MOV      @4(SP),R0        ;;GET MESSAGE ADDR.
(1) 016540 062766 000002 000004    ADD      #2,4(SP)         ;;BUMP RETURN ADDR.
(1) 016546 005737 001174          TST      $MSGTYPE        ;;SEE IF DONE W/ LAST XMISSION?
(1) 016552 001375          BNE      1$               ;;IF NOT: WAIT
(1) 016554 010037 001210          MOV      R0,$MSGAD       ;;PUT ADDR IN MAILBOX
(1) 016560 105720          TSTB     (R0)+            ;;FIND END OF MESSAGE
(1) 016562 001376          BNE      2$
(1) 016564 163700 001210          SUB      $MSGAD,R0        ;;SUB START OF MESSAGE
(1) 016570 006200          ASR      R0               ;;GET MESSAGE LNGTH IN WORDS
(1) 016572 010037 001212          MOV      R0,$MSGGLT      ;;PUT LENGTH IN MAILBOX
(1) 016576 012737 000004 001174    MOV      #4,$MSGTYPE     ;;TELL APT TO TAKE MSG.
(1) 016604 000413          BR       5$
(1) 016606 017637 000004 016632 3$:      MOV      @4(SP),4$        ;;PUT MSG ADDR IN JSR LINKAGE
(1) 016614 062766 000002 000004    ADD      #2,4(SP)         ;;BUMP RETURN ADDRESS
(3) 016622 013746 177776          MOV      177776,-(SP)    ;;PUSH 177776 ON STACK
(1) 016626 004737 016174          JSR      PC,$TYPE        ;;CALL TYPE MACRO
(1) 016632 000000          4$:      .WORD    0
(1) 016634          5$:
(1) 016634 105737 016722 10$:      TSTB     $FFLG            ;;SHOULD REPORT FATAL ERROR?
(1) 016640 001416          BEQ      12$             ;;IF NOT: BR
(1) 016642 005737 001214          TST      $ENV            ;;RUNNING UNDER APT?
(1) 016646 001413          BEQ      12$             ;;IF NOT: BR
(1) 016650 005737 001174 11$:      TST      $MSGTYPE        ;;FINISHED LAST MESSAGE?
(1) 016654 001375          BNE      11$             ;;IF NOT: WAIT
(1) 016656 017637 000004 001176    MOV      @4(SP),$FATAL   ;;GET ERROR #
(1) 016664 062766 000002 000004    ADD      #2,4(SP)         ;;BUMP RETURN ADDR.
(1) 016672 005237 001174          INC      $MSGTYPE        ;;TELL APT TO TAKE ERROR
(1) 016676 105037 016722 12$:      CLRB     $FFLG            ;;CLEAR FATAL FLAG
(1) 016702 105037 016721          CLRB     $LFLG            ;;CLEAR LOG FLAG
(1) 016706 105037 016720          CLRB     $MFLG            ;;CLEAR MESSAGE FLAG
(3) 016712 012601          MOV      (SP)+,R1        ;;POP STACK INTO R1
(3) 016714 012600          MOV      (SP)+,R0        ;;POP STACK INTO R0
(1) 016716 000207          RTS      PC              ;;RETURN
(1) 016720          000          $MFLG:  .BYTE    0        ;;MESSG. FLAG
(1) 016721          000          $LFLG:  .BYTE    0        ;;LOG FLAG
(1) 016722          000          $FFLG:  .BYTE    0        ;;FATAL FLAG
(1)          016724          .EVEN
(1)          000200          APTSIZE=200
(1)          000001          APTENV=001
(1)          000100          APTSPOOL=100
(1)          000040          APTCSUP=040
1566          .SBTTL POWER DOWN AND UP ROUTINES
(1)
(2)
(1)          *****
:POWER DOWN ROUTINE
(1) 016724 012737 017064 000024 $PWRDN: MOV      #SILLUP,@#PWRVEC ;;SET FOR FAST UP
(1) 016732 012737 000340 000026    MOV      #340,@#PWRVEC+2 ;;PRIO:7
(3) 016740 010046          MOV      R0,-(SP)        ;;PUSH R0 ON STACK
(3) 016742 010146          MOV      R1,-(SP)        ;;PUSH R1 ON STACK
```

(3) 016744 010246
(3) 016746 010346
(3) 016750 010446
(3) 016752 010546
(3) 016754 017746 162160
(1) 016760 010637 017070
(1) 016764 012737 016776 000024
(1) 016772 000000
(1) 016774 000776
(1)
(2)
(1)

MOV R2,-(SP) ;;PUSH R2 ON STACK
MOV R3,-(SP) ;;PUSH R3 ON STACK
MOV R4,-(SP) ;;PUSH R4 ON STACK
MOV R5,-(SP) ;;PUSH R5 ON STACK
MOV @SWR,-(SP) ;;PUSH @SWR ON STACK
MOV SP,\$SAVR6 ;;SAVE SP
MOV #SPWRUP,@#PWRVEC ;;SET UP VECTOR
HALT
BR -2 ;;HANG UP

:POWER UP ROUTINE

(1) 016776 012737 017064 000024
(1) 017004 013706 017070
(1) 017010 005037 017070
(1) 017014 005237 017070
(1) 017020 001375
(3) 017022 012677 162112
(3) 017026 012605
(3) 017030 012604
(3) 017032 012603
(3) 017034 012602
(3) 017036 012601
(3) 017040 012600
(1) 017042 012737 016724 000024
(1) 017050 012737 000340 000026
(1) 017056 104401
(1) 017060 017072
(1) 017062 000002
(1) 017064 000000
(1) 017066 000776
(1) 017070 000000
(1) 017072 005015 047520 042527
(1) 017100 000122
1567
1568
1569
1570
1571
1572
1573
1574
1575
1576
1577
1578
1579
1580
1581
1582
1583
1584
1585
1586
1587

\$PWRUP: MOV #SILLUP,@#PWRVEC ;;SET FOR FAST DOWN
MOV \$SAVR6,SP ;;GET SP
CLR \$SAVR6 ;;WAIT LOOP FOR THE TTY
1\$: INC \$SAVR6 ;;WAIT FOR THE INC
BNE 1\$;;OF WORD
MOV (SP)+,@SWR ;;POP STACK INTO @SWR
MOV (SP)+,R5 ;;POP STACK INTO R5
MOV (SP)+,R4 ;;POP STACK INTO R4
MOV (SP)+,R3 ;;POP STACK INTO R3
MOV (SP)+,R2 ;;POP STACK INTO R2
MOV (SP)+,R1 ;;POP STACK INTO R1
MOV (SP)+,R0 ;;POP STACK INTO R0
MOV #SPWRDN,@#PWRVEC ;;SET UP THE POWER DOWN VECTOR
MOV #340,@#PWRVEC+2 ;;PRIO:7
TYPE \$POWER ;;REPORT THE POWER FAILURE
\$PWRMG: .WORD \$POWER ;;POWER FAIL MESSAGE POINTER
RTI
\$SILLUP: HALT ;;THE POWER UP SEQUENCE WAS STARTED
BR -2 ;;BEFORE THE POWER DOWN WAS COMPLETE
\$SAVR6: 0 ;;PUT THE SP HERE
\$POWER: .ASCIZ <15><12>'POWER'

.EVEN
:*
:*THIS ROUTINE WILL PROTECT THE PROGRAM
:*FROM INTERRUPTS (BAD ONES).
:*
:*THE TRAP CATCHER IS SET UP FOR
:* .WORD +2
:* JSR PC,R0
:*
:*ILLEGAL INTERRUPTS OR INTERRUPTS TO THE WRONG VECTOR
:*GOTO THE VECTOR AND PCITK UP THE ".+2" AS AN ADDRESS
:*AND "4700" AS NEW STATUS.
:*THE .+2 AS A PC WILL CAUSE EXECUTION OF THE "JSR PC,R0" (AN ILLEGAL INSTR.).
:*AND TRAP TO LOCATION "4". IN LOCATION 4 WE HAVE A
:*POINTER HERE. IF THIS CONDITION CAUSES A TRAP TO LOC. 4.
:*WE WILL REPORT IT IN THE SAME MANNER THAT WER WOULD
:*REPORT ANY OTHER ERROR.
:*IF A BUSS ERROR TRAP DID OCCUT AND CAUSE A TRAP TO 4.
:*WE WILL HALT.

IOTRD: MOV (6),TRTO ;GET WHERE WE CAME TO.

```

1588 017106 162737 000004 017146       SUB    #4,TRTO       ;FORM READ ADDR.
1589                                     ;
1590 017114 023727 017146 001000       CMP    TRTO,#1000   ;DID TRAP FROM LESS THAN ADDR. 1000?
1591 017122 003402                                 BLE    2$           ;NO-CONTINUE.
1592                                     ;
1593 017124 000000                                1$:   HALT           ;A BUSS ERROR TIME OUT TRAP BROUGHT US HERE.
1594                                     ;ADDRESS CONTAINED IN TRTO.
1595                                     ;
1596 017126 000776                                BR     1$           ;DON'T ALLOW CONTINUE.
1597                                     ;
1598 017130 016637 000004 017150       2$:   MOV    4(6),TRFRO ;GET TRAPPED FROM ADDR.
1599 017136 062706 000004                                     ADD    #4,SP       ;/ADD #4 TO STACK POINTER.
1600

```

;; \$>>> ERROR <<< \$

```

1601 017142 104004                                ERROR 4
1602                                     ;ERROR! ILLEGAL INTERRUPT OR
1603                                     ;INTERRUPT TO WRONG VECTOR.
1604                                     ;IF TEST NO. IS LESS THAN 10, ITS
1605                                     ;LIKELY(BUT NO EXCLUSIVELY) TO BE A
1606                                     ;DEVICE OTHER THAN THE DEVICE UNDER TEST.
1607                                     ;IF THE INTERRUPT OCCURED
1608                                     ;DURING AN INTERRUPT TEST, I'D
1609                                     ;SUSPECT A PROBLEM WITH THE DEVICE UNDER TEST.
1610                                     ;IF THE ADDRESS THE INTERRUPT
1611                                     ;VECTORED TO IS WITHIN THE RANGE OF
1612                                     ;VECTORS ASSIGNED TO THE DEVICE,
1613                                     ;THEN I'D SUSPECT THE DEVICE
1614                                     ;INTERRUPTD ILLEGALLY.
1615                                     ;IF THE ADDRESS THE INTERRUPT
1616                                     ;VECTORED TO IS OUTSIDE OF THE
1617                                     ;RANGE ASSIGNED TO THE DEVICE
1618                                     ;I'D SUSPECT THAT THE
1619                                     ;DEVICE PUT THE WRONG INTERRUPT
1620                                     ;VICTOR ON THE BUS DURING THE INTERRUPT
1621                                     ;PROCESS.
1622                                     ;
1623                                     ;NOTE:
1624                                     ;FOR THIS ERROR - DON'T USE
1625                                     ;'LOOP ON ERROR' OPTION.
1626                                     ;ALSO EXPECT THAT THE INTERRUPT TEST TO
1627                                     ;WILL REPOT THAT THE DEVICE DIDN'T
1628                                     ;INTERRUPT.
1629                                     ;FOLLOW THE RECOMMENDED PROCEEDURE
1630                                     ;IN THE DOCUMENT (ON THIS DIAGNOSTIC).
1631                                     ;FOR LOOPING ON TEST.

```

;; \$>>> ERROR <<< \$

```

1632 017144 000002                                RTI
1633 017146 000000       TRTO: .WORD 0          ;CONTAINS ADDR. WE TRAPPED OR INTERRUPTED TO.
1634 017150 000000       TRFRO: .WORD 0         ;CONTAINS ADDR. WE TRAPPED OR INTR. FROM.
1635                                         .SBTTL TRAP DECODER

```

;; *****
 ;*THIS ROUTINE WILL PICKUP THE LOWER BYTE OF THE "TRAP" INSTRUCTION
 ;*AND USE IT TO INDEX THROUGH THE TRAP TABLE FOR THE STARTING ADDRESS

```

(1)          : *OF THE DESIRED ROUTINE. THEN USING THE ADDRESS OBTAINED IT WILL
(1)          : *GO TO THAT ROUTINE.
(1)          $TRAP: MOV    R0, -(SP)          :: SAVE R0
(1) 017152 010046          MOV    2(SP), R0          :: GET TRAP ADDRESS
(1) 017154 016600 000002  TST    -(R0)          :: BACKUP BY 2
(1) 017160 005740          MOV    (R0), R0          :: GET RIGHT BYTE OF TRAP
(1) 017162 111000          ASL    R0          :: POSITION FOR INDEXING
(1) 017164 006300          MOV    $TRPAD(R0), R0  :: INDEX TO TABLE
(1) 017166 016000 017206  RTS    R0          :: GO TO ROUTINE
(1) 017172 000200

(1)          ;; THIS IS USE TO HANDLE THE 'GETPRI' MACRO
(1)          $TRAP2: MOV   (SP), -(SP)        :: MOVE THE PC DOWN
(1) 017174 011646          MOV   4(SP), 2(SP)      :: MOVE THE PSW DOWN
(1) 017176 016666 000004 000002  RTI          :: RESTORE THE PSW
(1) 017204 000002

(3)          .SBTTL TRAP TABLE
(3)          ; *THIS TABLE CONTAINS THE STARTING ADDRESSES OF THE ROUTINES CALLED
(3)          ; *BY THE 'TRAP' INSTRUCTION.
(3)          ;
(3)          ; ROUTINE
(3)          ; -----
(3) 017206 017174          $TRPAD: .WORD  $TRAP2
(3) 017210 016174          $TYPE  :: CALL=TYPE      TRAP+1(104401)  TTY TYPEOUT ROUTINE
(3) 017212 014316          $TYPOC :: CALL=TYPOC    TRAP+2(104402)  TYPE OCTAL NUMBER (WITH LEADING ZEROS)
(3) 017214 014272          $TYPOS :: CALL=TYPOS    TRAP+3(104403)  TYPE OCTAL NUMBER (NO LEADING ZEROS)
(3) 017216 014332          $TYPON :: CALL=TYPON    TRAP+4(104404)  TYPE OCTAL NUMBER (AS PER LAST CALL)
(3) 017220 014520          $TYPBN :: CALL=TYPBN    TRAP+5(104405)  TYPE BINARY (ASCII) NUMBER
(1)
(3) 017222 015470          $GTSWR :: CALL=GTSWR    TRAP+6(104406)  GET SOFT-SWR SETTING
(1)
(3) 017224 015420          $CKSWR :: CALL=CKSWR    TRAP+7(104407)  TEST FOR CHANGE IN SOFT-SWR
(3) 017226 015702          $RDCHR :: CALL=RDCHR    TRAP+10(104410) TTY TYPEIN CHARACTER ROUTINE
(3) 017230 016022          $RDLIN :: CALL=RDLIN    TRAP+11(104411) TTY TYPEIN STRING ROUTINE
1636 017232 005015 046103 041517 EM1:  .ASCIZ <15><12>/CLOCK SR FUNCTION ERROR/
      017240 020113 051123 043040
      017246 047125 052103 047511
      017254 020116 051105 047522
      017262 000122
1637 017264 005015 046103 041517 EM2:  .ASCIZ <15><12>/CLOCK SR DATA ERROR/
      017272 020113 051123 042040
      017300 052101 020101 051105
      017306 047522 000122
1638 017312 005015 046103 041517 EM3:  .ASCIZ <15><12>/CLOCK BR DATA ERROR/
      017320 020113 051102 042040
      017326 052101 020101 051105
      017334 047522 000122
1639 017340 044600 052116 051105 EM4:  .ASCIZ <200>/INTERRUPT ERROR/
      017346 052522 052120 042440
      017354 051122 051117 000
1640 017361 015 041412 052517 EM5:  .ASCIZ <15><12>/COUNT REG. ERROR/
      017366 052116 051040 043505
      017374 020056 051105 047522

```

1641	017402	000122								
	017404	005015	047503	047125	EM11:	.ASCIZ	<15><12>#COUNT ERROR #			
	017412	020124	051105	047522						
	017420	020122	000							
1642	017423	015	041412	052517	EM12:	.ASCIZ	<15><12>#COUNT FUNCTION ERROR#			
	017430	052116	043040	047125						
	017436	052103	047511	020116						
	017444	051105	047522	000122						
1643	017452	005015	046103	041517	EM16:	.ASCIZ	<15><12>#CLOCK INTERRUPT ERROR #			
	017460	020113	047111	042524						
	017466	051122	050125	020124						
	017474	051105	047522	020122						
	017502	000								
1644	017503	015	051012	050105	EM20:	.ASCIZ	<15><12>#REPEATABILITY ERROR #			
	017510	040505	040524	044502						
	017516	044514	054524	042440						
	017524	051122	051117	000040						
1645	017532	005015	042101	051104	EM26:	.ASCIZ	<15><12>#ADDRESSING ERROR#			
	017540	051505	044523	043516						
	017546	042440	051122	051117						
	017554	000								
1646										
1647	017555	015	042412	051122	DH1:	.ASCIZ	<15><12>#ERRPC ASR WAS S/B#			
	017562	041520	040411	051123						
	017570	053411	051501	051411						
	017576	041057	000							
1648	017601	015	042412	051122	DH3:	.ASCIZ	<15><12>#ERRPC ABR WAS S/B#			
	017606	041520	040411	051102						
	017614	053411	051501	051411						
	017622	041057	000							
1649	017625	200	051105	050122	DH4A:	.ASCIZ	<200>#ERRPC TO FROM ADDR.#			
	017632	020103	020040	047524						
	017640	020040	020040	020040						
	017646	051106	046517	040440						
	017654	042104	027122	000						
1650	017661	015	042412	051122	DH12:	.ASCIZ	<15><12>#ERRPC ASR #			
	017666	041520	040411	051123						
	017674	000011								
1651	017676	005015	051105	050122	DH20:	.ASCIZ	<15><12>#ERRPC ASR 2NDCNT 1STNCT 3RDCNT#			
	017704	004503	051501	004522						
	017712	047062	041504	052116						
	017720	030411	052123	041516						
	017726	004524	051063	041504						
	017734	052116	000							
1652	017737	015	042412	051122	DH26:	.ASCIZ	<15><12>#ERRPC CLOCK ADDR.#			
	017744	041520	041411	047514						
	017752	045503	040440	042104						
	017760	027122	000							
1653										
1654		017764				.EVEN				
1655										
1656	017764	001116	001376	001126	DT1:	.WORD	\$ERRPC,ASR,\$BDDAT,\$GDDAT,0			
	017772	001124	000000							
1657	017776	001116	001400	001126	DT3:	.WORD	\$ERRPC,ABR,\$BDDAT,\$GDDAT,0			
	020004	001124	000000							
1658	020010	001116	017146	017150	DT4:	.WORD	\$ERRPC,TRTO,TRFRO,0			

```
1659 020016 000000
1660 020020 001116 001376 000000 DT12: .WORD $ERRPC,ASR,0
1660 020026 001116 001376 001126 DT20: .WORD $ERRPC,ASR,$BDDAT,$GDDAT,$TMPO,0
1661 020034 001124 001420 000000
1661 020042 001116 001376 001126 DT22: .WORD $ERRPC,ASR,$BDDAT,$TMPO,0
1662 020050 001420 000000
1662 020054 001116 001420 000000 DT26: .WORD $ERRPC,$TMPO,0
1663
1664 020062 000000 000000 DFO: .WORD 0,0
1665
1666 000001 .END
```

ABASE = 170420	102#	112	189	190										
ABR 001400	190#	256*	257*	295	385*	387*	463*	471	489*	497	559*	563	626*	
	630	650*	668	678*	694*	724*	744*	806*	808*	810*	812*	814*	816*	
	822*	832	848*	881*	1021*	1063*	1071	1082*	1093	1172*	1173*	1174*	1176*	
	1177*	1201*	1211	1220	1241*	1251	1261	1287*	1292	1304	1318*	1323	1462*	
	1467	1490*	1657											
ACDW1 = 000000	112													
ACDW2 = 000000	112													
ACPUOP = 000000	112													
ADDW0 = 000000	112													
ADDW1 = 000000	112													
ADDW10 = 000000	112													
ADDW11 = 000000	112													
ADDW12 = 000000	112													
ADDW13 = 000000	112													
ADDW14 = 000000	112													
ADDW15 = 000000	112													
ADDW2 = 000000	112													
ADDW3 = 000000	112													
ADDW4 = 000000	112													
ADDW5 = 000000	112													
ADDW6 = 000000	112													
ADDW7 = 000000	112													
ADDW8 = 000000	112													
ADDW9 = 000000	112													
ADEVCT = 000000	112													
ADEVN = 000000	112													
AENV = 000000	112													
AENVN = 000000	112													
AFATAL = 000000	112													
AMADR1 = 000000	112													
AMADR2 = 000000	112													
AMADR3 = 000000	112													
AMADR4 = 000000	112													
AMAMS1 = 000000	112													
AMAMS2 = 000000	112													
AMAMS3 = 000000	112													
AMAMS4 = 000000	112													
AMSGAD = 000000	112													
AMSGLG = 000000	112													
AMSGTY = 000000	112													
AMTYP1 = 000000	112													
AMTYP2 = 000000	112													
AMTYP3 = 000000	112													
AMTYP4 = 000000	112													
ANYKEY 013740	1290	1303	1321	1417#										
APASS = 000000	112													
APRIOR = 000200	104#	112	195											
APTCSU = 000040	1564	1565#												
APTENV = 000001	1560	1564	1565#											
APTSIZ = 000200	225	1565#												
APTSPO = 000100	1564	1565#												
ASR 001376	189#	232*	256	294	342*	343*	344*	345*	346*	347*	348*	349*	350*	
	351*	406*	407*	412	432*	434*	438*	444*	446	462*	467*	471*	488*	
	493*	497*	522*	526	580*	581*	583	605*	606*	607	616*	625*	627*	
	628*	630*	649*	654*	656*	668*	677*	693*	696*	698*	700	722*	726*	

PR5	=	000240	100#							
PR6	=	000300	100#							
PR7	=	000340	100#							
PS	=	177776	100#							
PSW	=	177776	100#							
PWRVEC	=	000024	100#	225*	1566*					
QSTART		001444	87	211#						
RDCHR	=	104410	1563	1635#						
RDLIN	=	104411	1635#							
RESVEC	=	000010	100#							
ROTATE		001426	201#	243*	244	1355*	1367	1396*	1560	
RSTART		002144	211	235#						
STACK	=	001100	100#	225						
START	=	001506	86	221#						
STKLMT	=	177774	100#							
SWR		001140	112#	225*	234	816	1560	1562	1563*	1566*
SWREG		000176	79#	225	234	1563				
SW0	=	000001	100#							
SW00	=	000001	100#							
SW01	=	000002	100#							
SW02	=	000004	100#							
SW03	=	000010	100#							
SW04	=	000020	100#							
SW05	=	000040	100#							
SW06	=	000100	100#							
SW07	=	000200	100#							
SW08	=	000400	100#							
SW09	=	001000	100#							
SW1	=	000002	100#							
SW10	=	002000	100#							
SW11	=	004000	100#							
SW12	=	010000	100#							
SW13	=	020000	100#							
SW14	=	040000	100#							
SW15	=	100000	100#							
SW2	=	000004	100#							
SW3	=	000010	100#							
SW4	=	000020	100#							
SW5	=	000040	100#							
SW6	=	000100	100#							
SW7	=	000200	100#							
SW8	=	000400	100#							
SW9	=	001000	100#							
TBITVE	=	000014	100#							
TKVEC	=	000060	100#							
TPVEC	=	000064	100#							
TRAPVE	=	000034	100#	225*						
TRFRO		017150	1598*	1634#	1658					
TRTO		017146	1587*	1588*	1590	1633#	1658			
TRTVEC	=	000014	100#							
TSTCNT		001436	205#	215*	218*	222*	1353			
TSTSTR		001456	95	214#						
TST1		002422	294#							
TST10		003244	347#							
TST11		003342	348#							
TST12		003440	349#							

VECT2	001406	193#	250*	251*	252	902*												
VECT2P	001410	194#	252*	253*														
WSTART=	001472	93	217#															
ZSTART	001774	224	228#															
SAPTHD	001000	111#																
SASTAT=	***** U	1565																
SATYC	016502	1565#																
SATY1	016456	1565#																
SATY3	016464	1564	1565#															
SATY4	016474	1560	1565#															
SAUTOB	001134	112#	234*	1563														
\$BASE	001250	112#	232	1389														
\$BDADR	001122	112#																
\$BDDAT	001126	112#	342*	343*	344*	345*	346*	347*	348*	349*	350*	351*	385*	387*				
		412*	414	417	446*	447	449	471*	473	497*	499	526*	563*	630*				
		668*	670	806*	808*	810*	812*	814*	816*	832*	1010*	1031*	1049*	1052				
		1071*	1093*	1172*	1173*	1174*	1176*	1177*	1211*	1212	1220*	1221	1251*	1252				
		1261*	1271*	1292*	1304*	1323*	1656	1657	1660	1661								
		112#	1560															
\$BELL	001164	112#																
\$BIN	014572	1547#*																
\$CDW1	001254	112#																
\$CHARC	016452	1564#*																
\$CKSWR	015420	1563#	1635															
\$CMTAG	001100	112#	225															
\$CM3 =	000000	112#																
\$CNTLG	016145	1563#																
\$CNTLU	016140	1563#																
\$CPUOP	001222	112#																
\$CRLF	001171	112#	1560	1561	1563	1564												
\$DEVCT	001204	112#	229*	1370	1372*	1374	1381	1386	1391	1393*								
\$DEVN	001252	112#																
\$DOAGN	013730	1410#																
\$ENDAD	013720	109	1410#															
\$ENDCT	013466	1410#																
\$ENULL	013734	1410#																
\$ENV	001214	112#	234	1560	1564	1565												
\$ENVN	001215	112#	225	1349	1564	1565												
\$EOP	013432	1410#																
\$EOPCT	013460	1410#																
\$ERFLG	001103	112#	1560*	1562*														
\$ERMAX	001115	112#	225*	1562*														
\$ERROR	014574	225	1560#															
\$ERRPC	001116	112#	1560*	1561	1656	1657	1658	1659	1660	1661	1662							
\$ERRTB	001256	112#	1561															
\$ERRTY	015002	1560	1561#															
\$ERTTL	001112	112#	1560*															
\$ESCAP	001162	112#	225*	1560	1562*													
\$ETABL	001214	112#																
\$ETEND	001256	111	112#															
\$FATAL	001176	112#	1565*															
\$FFLG	016722	1565#*																
\$FILLC	001156	112#	1564															
\$FILLS	001155	112#	1564															
\$GDADR	001120	112#																
\$GDDAT	001124	112#	342*	343*	344*	345*	346*	347*	348*	349*	350*	351*	385*	387*				
		414*	415*	447*	448*	469*	473	495*	499	521*	558*	651*	669*	670				

TYPBIN	100#	1410													
TYPDEC	100#														
TYPNAM	100#	234													
TYPNUM	100#														
TYPOCS	6#	100#													
TYPOCT	100#	1370	1374	1386	1410	1561	1563								
TYPTXT	100#	238	239	1289	1302	1320	1369	1371	1373	1385	1387	1410	1418		
ZIOTM	1424#	1448	1476												
ZP21	394#	404	430												
ZP25	511#	519													
ZP25A	547#	556													
ZZ1	296#	342	343	344	345	346	347	348	349	350	351	638#	647	806#	808#
\$\$\$MRE	810#	812#	814#	816#	1179#	1198	1230#	1238							
\$\$\$MTM	112#														
\$\$\$ESCA	100#														
\$\$\$NEWT	100#	294	295	342	343	344	345	346	347	348	349	350	351	385	387
	404	430	460	486	519	556	578	603	623	647	683	720	741	806	808
	810	812	814	816	819	845	876	897	1000	1018	1038	1060	1079	1172	1173
	1174	1176	1177	1198	1238	1278	1312								
\$\$\$SET	1635#														
\$\$\$SETM	225#														
\$\$\$SKIP	100#	536	539	542	574	591	593	595	666	706	708	711	816	1258	1268
	1272	1299	1305												
.EQUAT	6#	100													
.HEADE	5#	54													
.SETTR	5#														
.SETUP	5#	210													
.SWRHI	6#	56													
.SWRLO	56#														
.TRMTR	5#														
\$.SACT1	8#	109													
\$.SAPT8	112#														
\$.SAPTH	8#	111													
\$.SAPTY	8#	1565													
\$.SCATC	6#														
\$.SCMTA	6#	112													
\$.SEQP	7#	1410													
\$.SERRO	7#	1560													
\$.SERRT	7#	1561													
\$.SPOWE	6#	1566													
\$.SRDOC	5#														
\$.SREAD	7#	1563													
\$.SSCOP	7#	1562													
\$.STRAP	5#	1635													
\$.STYPB	5#	1547													
\$.STYPD	7#														
\$.STYPE	7#	1564													
\$.STYPO	6#	1546													

. ABS. 020066 000 OVR RO REL LCL I

ERRORS DETECTED: 0

CVKWAC, CVKWAC/CRF=CVKWAC
RUN-TIME: 28 17 1 SECONDS
RUN-TIME RATIO: 78/47=1.6
CORE USED: 27K (53 PAGES)