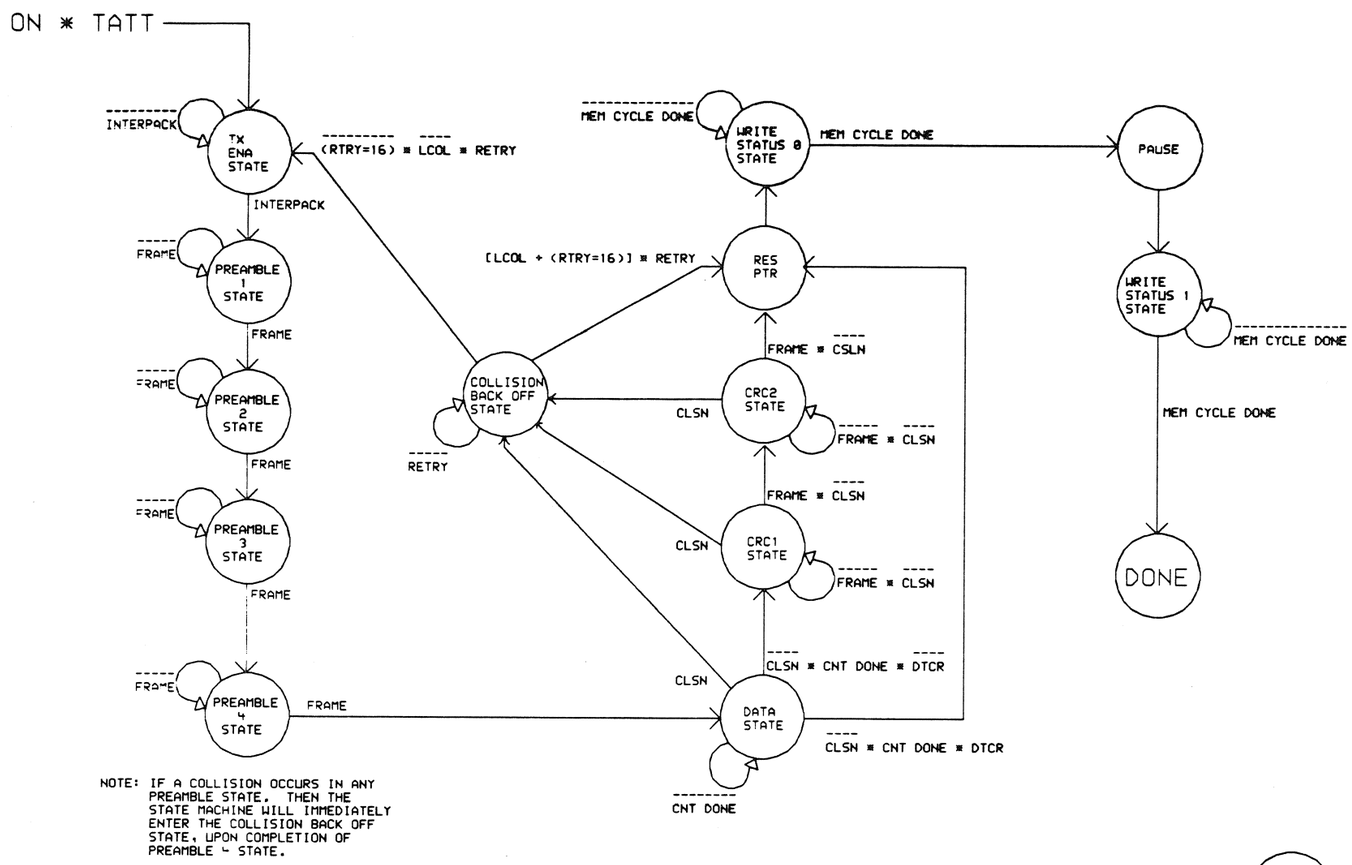


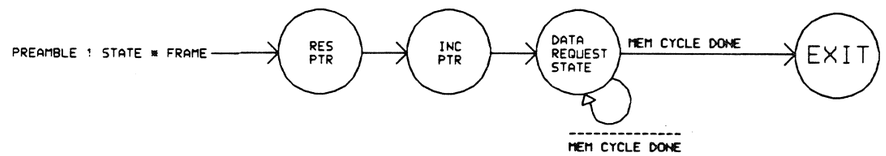
NOTE: IF A COLLISION OCCURS IN ANY PREAMBLE STATE. THEN THE STATE MACHINE WILL IMMEDIATELY ENTER THE COLLISION BACK OFF STATE, UPON COMPLETION OF PREAMBLE 4 STATE.

TRANSMIT STATE MACHINE INPUTS

PROCESS STATE	REFERENCE SIGNAL	REFERENCE PIN
INTERPACK	LNKL INTERPACK L	E92-19
ON	LNKN ON H	E110-2
TATT	LNKH BTATT H	E81-5
FRAME	LNKJ TX FRAME H	E87-8
CSLN	LNKH SYNC CLSN H	E81-12
RETRY	LNKN RETRY H	E61-15
RTRY	LNKK RTRY H	E21-15
CNT DONE	LNKN TX CNT DONE L	E61-12
MEM CYCLE DONE	LNKN TX MEM CYCDN H	E41-2
DTCR	LNKN DTCR H	E93-7

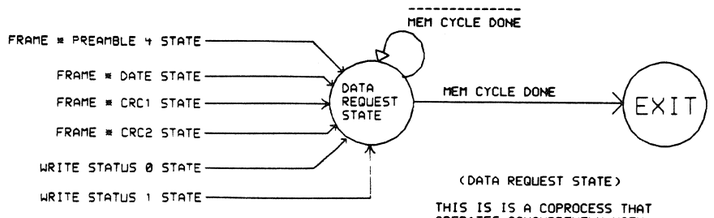
TRANSMIT STATE MACHINE OUTPUTS

PROCESS STATE	REFERENCE SIGNAL	REFERENCE PIN
TX ENA STATE	LNKL TX ENA STATE L	E49-12
TX PREAMBLE 1 STATE	LNKL PREAM 1 STATE L	E49-13
	LNKL TX LEN REQ L	E36-17
TX PREAMBLE 2 STATE	LNKL PREAM 2 STATE L	E49-14
TX PREAMBLE 3 STATE	LNKL PREAM 3 STATE L	E49-15
TX PREAMBLE 4 STATE	LNKL PREAM 4 STATE L	E49-16
DATA STATE	LNKL TX DATA STATE L	E49-18
	LNKL TX ENA CRC L	E36-15
	LNKL SEL TX DATA L	E36-16
CRC 1 STATE	NONE - LOW ASSERTED	E51-12
CRC 2 STATE	NONE - LOW ASSERTED	E51-13
RES PTR STATE	LNKL RES TX PNTR L	E38-8
INC PTR STATE	LNKN INC TX PNTR L	E41-12
WRITE STATUS 0 STATE	LNKL TX WR STAT0 L	E51-15
WRITE STATUS 1 STATE	LNKL TX WR STAT1 L	E51-16
DATA REQUEST STATE	LNKL TX REQUEST H	E62-12
	PP TX ACK L	PORT
	BUS READ H	E100-6
	LNKN TX MEM CYCDN H	E41-2
DONE	LNKL TX DONE L	E51-18



(LOAD BYTE COUNTER STATE)

THIS IS A COPROCESS THAT OPERATES CONCURRENTLY WITH THE TRANSMIT STATE MACHINE.



(DATA REQUEST STATE)

THIS IS IS A COPROCESS THAT OPERATES CONCURRENTLY WITH THE TRANSMIT STATE MACHINE.

TRANSMIT STATE MACHINE-LNKL STATE DIAGRAM-1

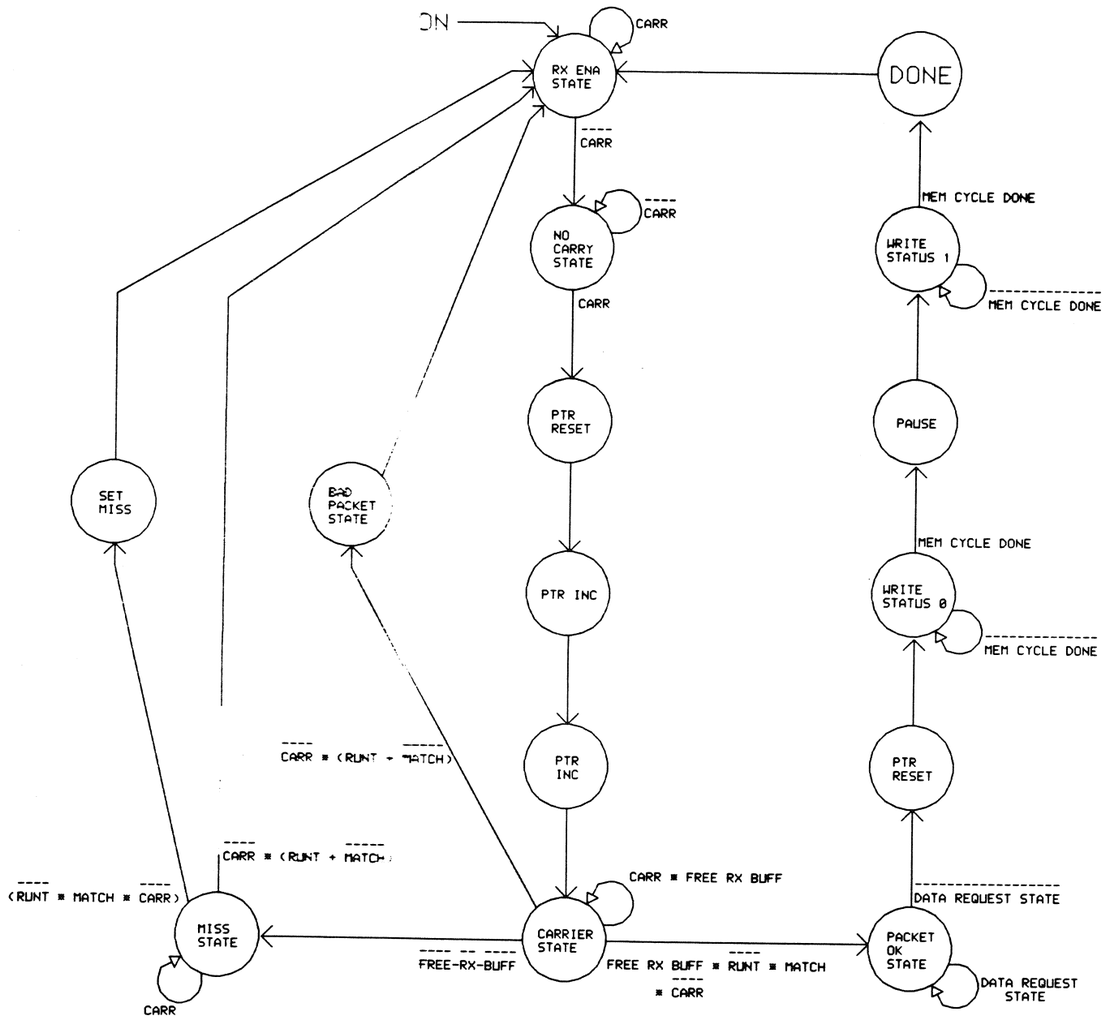
REVISIONS		
CHK	CHANGE NO.	REV

digital

DRN. D.BLANCHARD — DATE 17-NOV-82 — ENG. Neil Bloomberg — DATE 17-NOV-82
CHK'D. — DATE 17-NOV-82 — BOARD LOCATION: — SHEET 1 OF 1
DSKD:<SARGENT>LNKSD1.DRW 05-NOV-82 16:08 — NEXT HIGHER ASSEMBLY: D-UA-M7793-0-0
FIRST USED ON OPTION/MODEL: DELUNA

TITLE: DELUNA LINK MODULE (LNK)

SIZE	CODE	NUMBER	REV.
K	CS	M7793-0-SD1	A

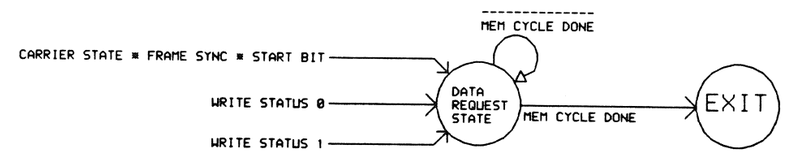


RECEIVE STATE MACHINE INPUTS

PROCESS STATE	REFERENCE SIGNAL	REFERENCE PIN
CARRIER	LNKN DLY CAR DET H	E61-5
ON	LNKN ON H	E110-2
RUNT	NONE - HIGH ASSERTED	E138-6
MATCH	LNKH RX MATCH H	E133-15
FREE RX BUFF	PB RX FREE BUFF H	PORT
MEM CYCLE DONE	LNKN RX MEM CYCDN H	E41-7
FRAME SYNC	LNKH RX FRAME SYNC H	E107-9
START BIT	LNKE RX START BIT H	E73-10

RECEIVE STATE MACHINE OUTPUTS

PROCESS STATE	REFERENCE SIGNAL	REFERENCE PIN
RX ENA STATE	LNKH RX ENA STATE L	E37-12
NO CARRIER STATE	NONE - LOW ASSERTED	E37-15
PTR RESET	LNKH RES RX PNTR L	E38-6
PTR INC	LNKN INC RX PNTR L	E41-15
	LNKH PR INC RX PNTR L	E37-14
CARRIER STATE	LNKH RX ACTIVE H	E99-10
PACK OK STATE	NONE - LOW ASSERTED	E37-18
	LINKH RX ODD BYTE L	E32-19
MISS STATE	NONE - LOW ASSERTED	E37-19
SET MISS	LNKH SET MISS L	E32-12
WRITE STATUS 0	LNKH RX WR STAT0 L	E32-14
	LNKH RX REQUEST H	E62-8
WRITE STATUS 1	LNKH RX WR STAT1 L	E32-16
	LNKH RX REQUEST H	E62-8
PAUSE	NONE - LOW ASSERTED	E32-15
DATA STATE	LNKH RX REQUEST H	E62-8
	PP RX ACK L	PORT
	BUS READ	E100-6
	LNKN RX MEM CYCDN H	E41-7
DONE	LNKH ADV RX PNTR L	E32-17



<DATA REQUEST STATE>

THIS IS A COPROCESS THAT OPERATES CONCURRENTLY WITH THE RECEIVE STATE MACHINE

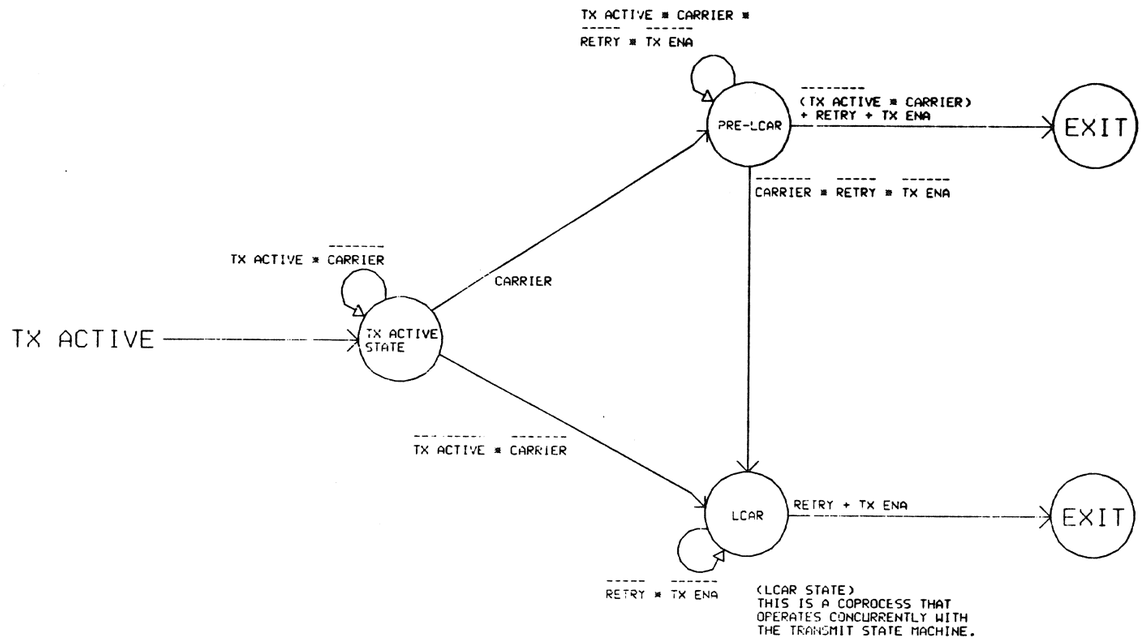
RECEIVE STATE MACHINE-LNKH
STATE DIAGRAM-2

REVISIONS		
CHK	CHANGE NO.	REV

DRN. D. BLANCHARD DATE 17-NOV-82 ENG. Neil Bloomberg DATE 17-NOV-82
CHK: D. Blanchard DATE 17-NOV-82 BOARD LOCATION: SHEET 1 OF 1
DSKD:<SARGENT>LNKSD2.DRW 05-NOV-82 16:08 NEXT HIGHER ASSEMBLY: D-UA-M7793-0-0
FIRST USED ON OPTION/MODEL: DEUNA

TITLE: DEUNA LINK MODULE (LNK)

SIZE	CODE	NUMBER	REV.
K	CS	M7793-0-SD2	A

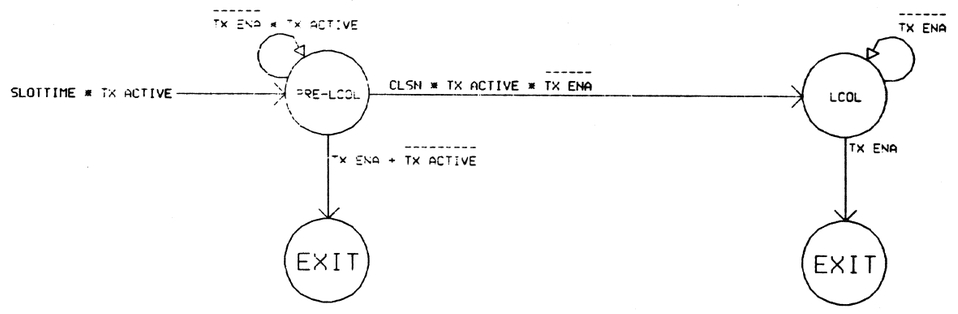


LCAR, LCOL STATE INPUTS

PROCESS STATE	REFERENCE SIGNAL	REFERENCE PIN
TX ENA	LNKL TX ENA STATE H	E35-6
SLOTTIME	LNKK SLOTTIME EN H	E39-13
CLSN	LNKH SYNC CISN H	E81-12
CARRIER	LNKH SYNC CARR H	E81-16
RETRY	LNKK RETRY STATE H	E79-4
TX ACTIVE	LNKL TX ACTIVE H	E109-8

LCAR,LCOL STATE OUTPUTS

PROCESS STATE	REFERENCE SIGNAL	REFERENCE PIN
LCOL	LNKK LCOL H	E35-10
LCAR	LNKK LCAR H	E78-8



(LCOL STATE)
THIS IS A COPROCESS THAT
OPERATES CONCURRENTLY WITH
THE TRANSMIT STATE MACHINE.

LCAR, LCOL-LNKK
STATE DIAGRAM-3

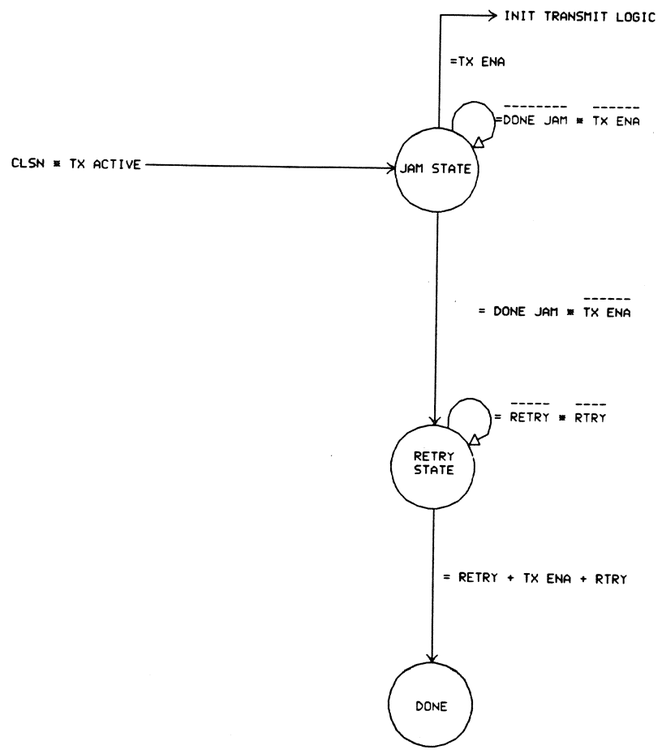
REVISIONS		
CHK	CHANGE NO.	REV

digital

DRN. D. BLANCHARD — DATE 17-NOV-82 — ENG. Neil Bloomberg — DATE 17-NOV-82
CHK'D. — DATE 17-NOV-82 — BOARD LOCATION: — SHEET 1 OF 1
DSKD:<SARGENT>LNKSD3.DRW 05-NOV-82 16:08 — NEXT HIGHER ASSEMBLY: D-UA-M7793-0-0
FIRST USED ON OPTION/MODEL: DEUNA

TITLE: DEUNA LINK MODULE (LNK)

SIZE	CODE	NUMBER	REV.
K	CS	M7793-0-SD3	A



COLLISION BACK OFF STATE INPUTS

PROCESS_STATE	REFERENCE_SIGNAL	REFERENCE_PIN
TX ENA	LNKL TX ENA STATE H	E35-6
CISN	LNKH SYNC CISN H	E81-12
DONE JAM	LNKK COLLISION JAM H	E40-13
RETRY	LNKN RETRY H	E61-15
RTRY	LNKK RTRY H	E21-15

COLLISION BACK OFF STATE OUTPUTS

PROCESS_STATE	REFERENCE_SIGNAL	REFERENCE_PIN
RETRY STATE	LNKK RETRY STATE L	E50-18
JAM STATE	LNKK JAM STATE L	E50-17
	LNKK RETRY INIT L	E50-19

DEFINITIONS

RTRY: FAILURE TO TRANSMIT IN 16 ATTEMPTS DUE TO COLLISION

RETRY: PROPER NUMBER OF SLOTTIMES HAS ELAPSED. TIME TO RETRANSMIT

DONE JAM: TELLS JAM STATE 32 BITS HAVE ELAPSED STOP JAMMING

COLLISION BACK OFF STATE-LNKK

STATE DIAGRAM-4

REVISIONS		
CHK	CHANGE NO.	REV

DRN. C. GIROUARD" DATE 17-NOV-82 ENG. Neil Bloomberg DATE 17-NOV-82

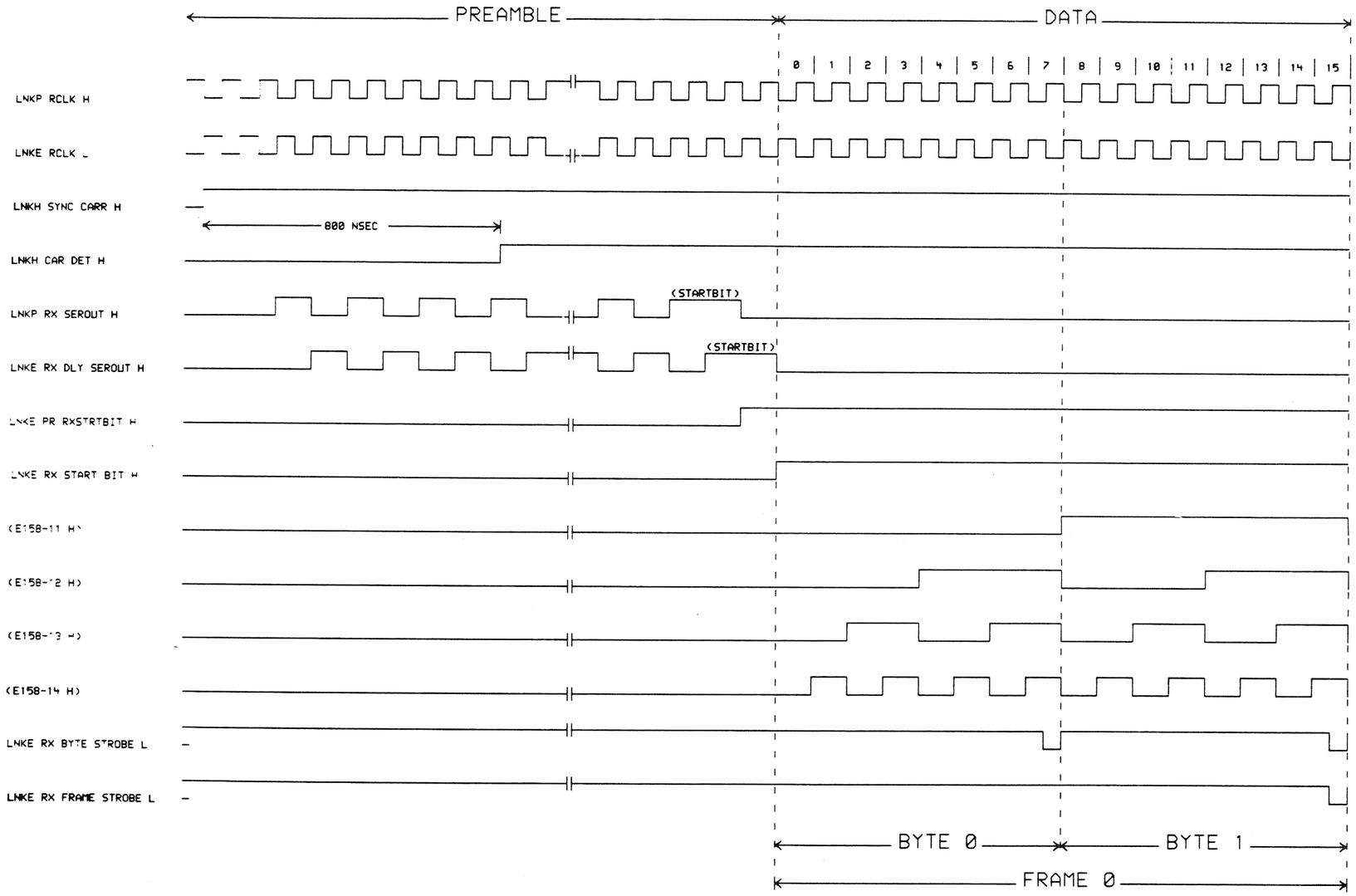
CHK: D. Sargent DATE 17-NOV-82 BOARD LOCATION: SHEET 1 OF 1

DSKD:<SARGENT>LNKSD4.DRW 05-NOV-82 16:08 NEXT HIGHER ASSEMBLY: D-UA-M7793-0-0

FIRST USED ON OPTION/MODEL: DELUNA

TITLE: DELUNA LINK MODULE (LNK)

SIZE	CODE	NUMBER	REV.
K	CS	M7793-0-SD4	A



RECEIVE BYTE TIMING-LNKE

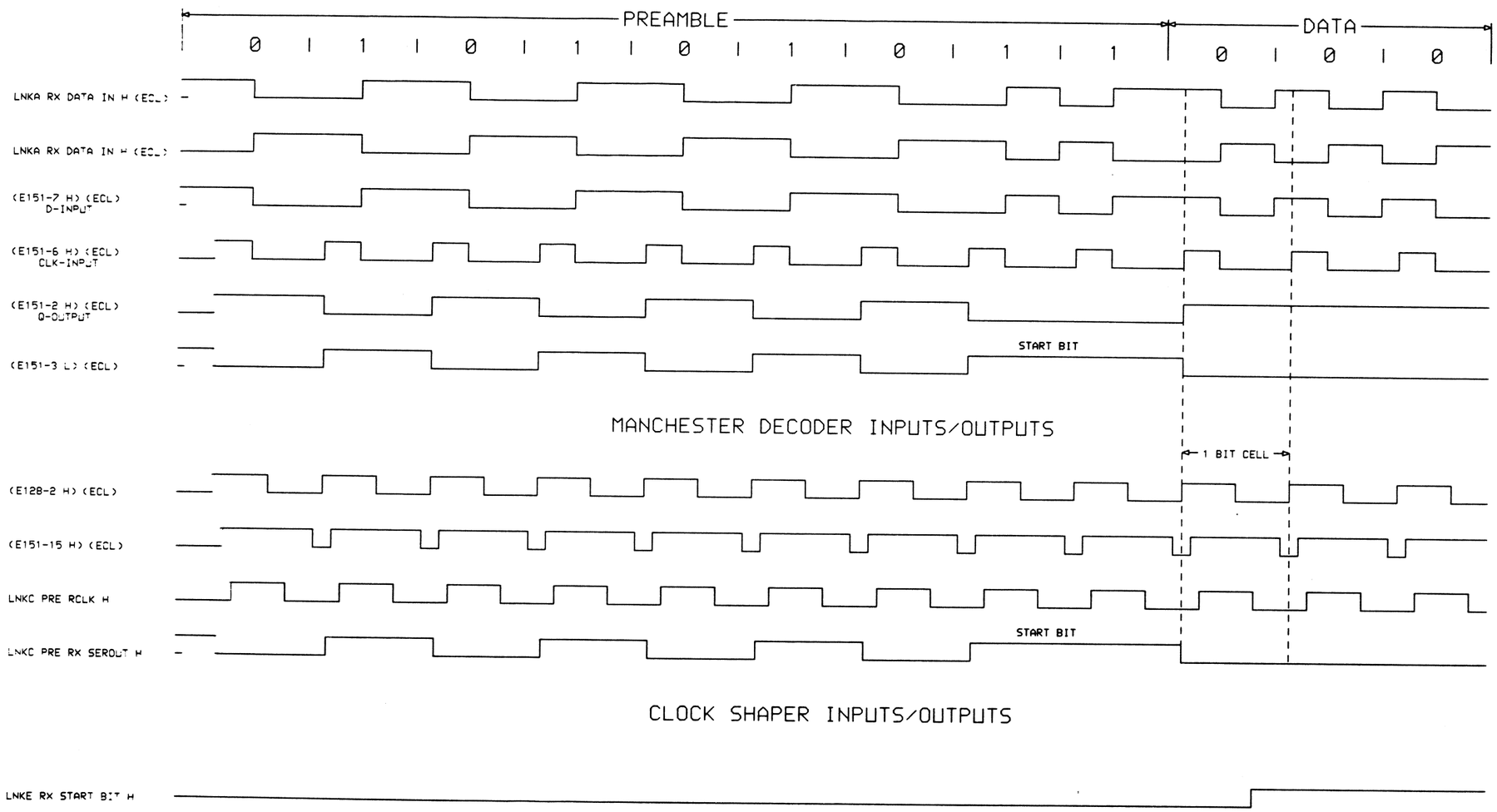
TIMING DIAGRAM-1

REVISIONS		
CHK	CHANGE NO.	REV

digital	DRN. PAUL HEBERT	DATE 17-NOV-82	ENG. Neil Bloomberg	DATE 17-NOV-82
	CHK'D.	DATE 17-NOV-82	BOARD LOCATION: SHEET 1 OF 1	
DSKD:<SARGENT>LNKTDA.DRW 17-NOV-82 11:01			NEXT HIGHER ASSEMBLY: D-UA-M7793-0-0	
FIRST USED ON OPTION/MODEL: DELUNA				

TITLE: DELUNA LINK MODULE (LNK)

SIZE	CODE	NUMBER	REV.
K	CS	M7793-0-TDA	A



RECEIVE DATA DECODE AND CLOCK GENERATOR-LNKC
TIMING DIAGRAM-2

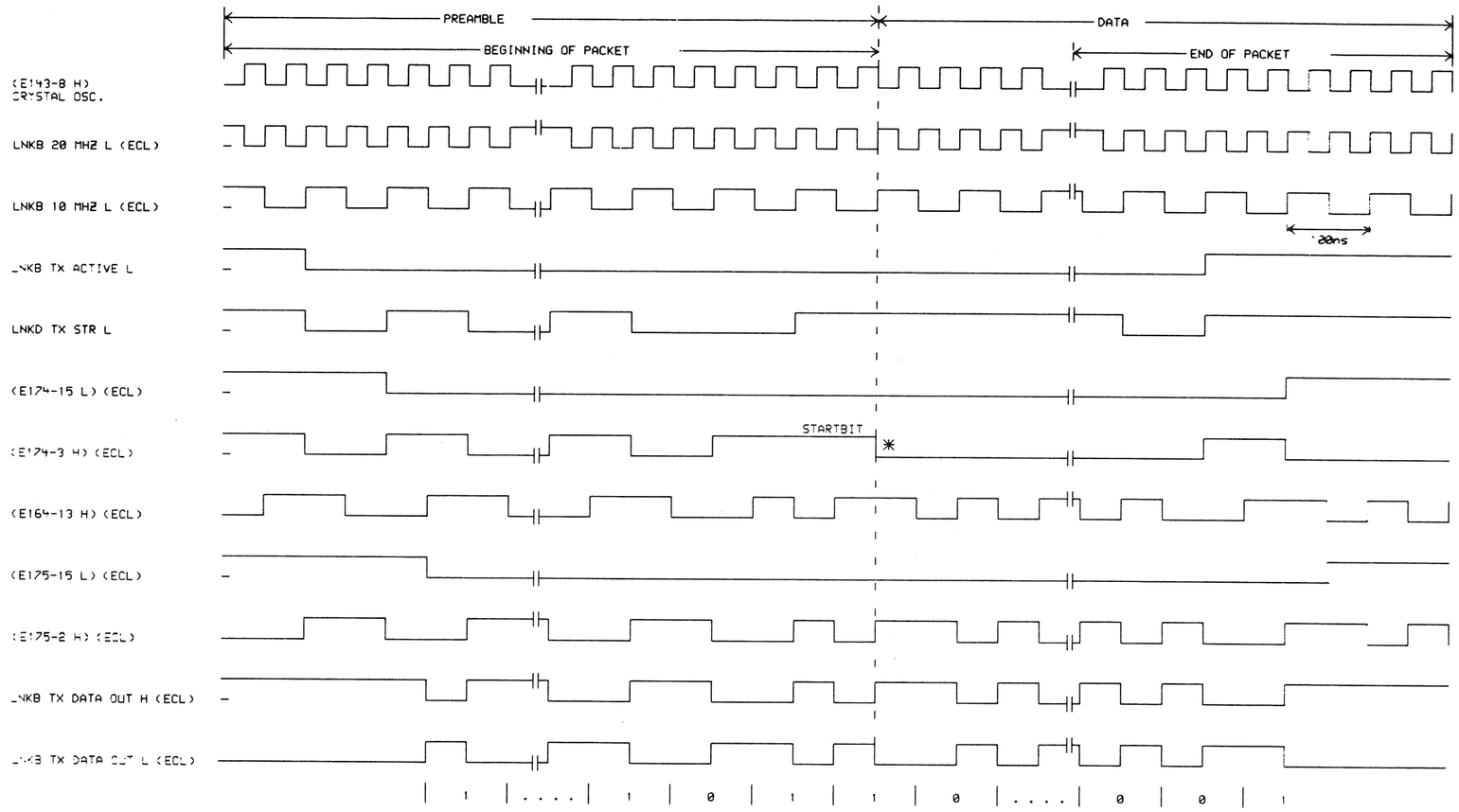
REVISIONS		
CHK	CHANGE NO.	REV

digital

DRN. G.M.HAFNER	DATE 17-NOV-82	ENG. Neil Bloomberg	DATE 17-NOV-82
CHK'D.	DATE 17-NOV-82	BOARD LOCATION: SHEET 1 OF 1	
DSKD:<SARGENT>LNKTDB.DRW;17-NOV-82 11:02		NEXT HIGHER ASSEMBLY: D-UA-M7793-0-0	
FIRST USED ON OPTION/MODEL: DELNA			

TITLE: DELNA LINK MODULE (LNK)

SIZE	CODE	NUMBER	REV.
K	TD	M7793-0-TDB	A



*DATA INDICATED HERE
CAN BE ANY PATTERN

TRANSMIT DATA ENCODE-LNKB
TIMING DIAGRAM-3

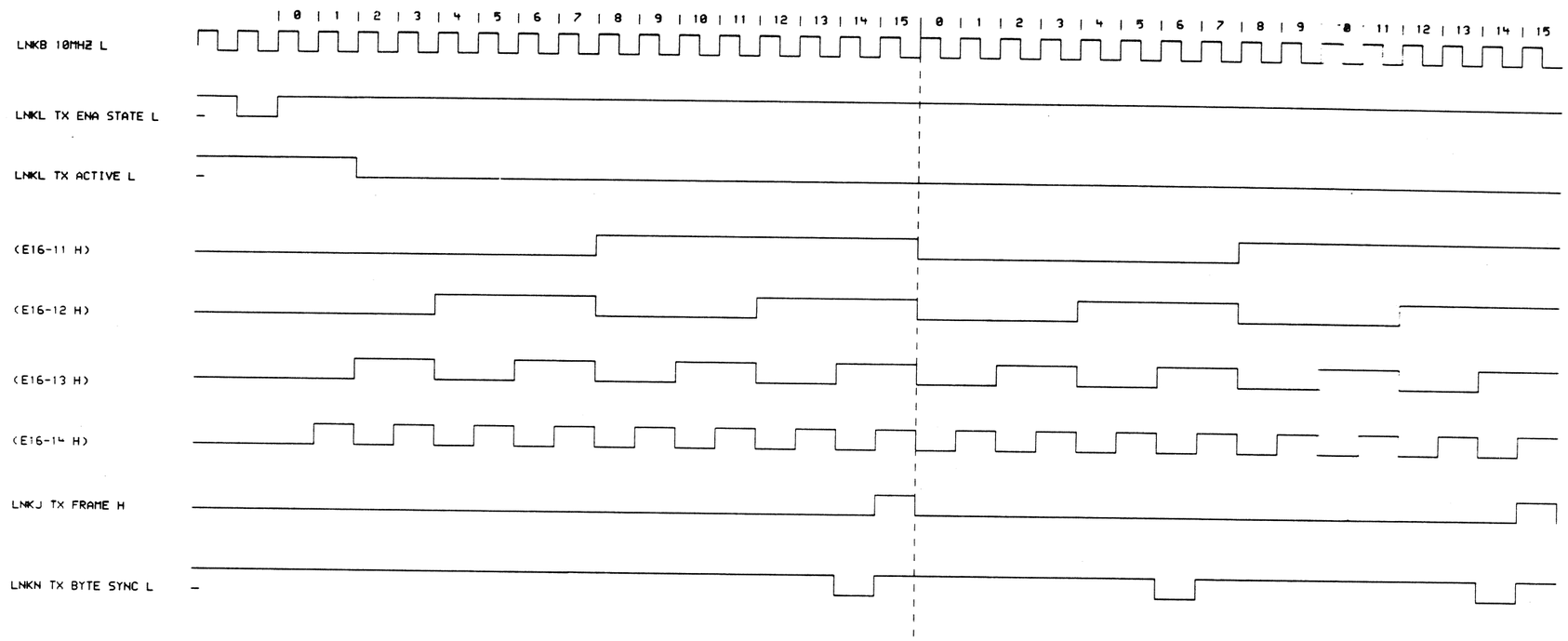
REVISIONS		
CHK	CHANGE NO.	REV

DRN. PAUL HEBERT
CHK'D. K. Sargent
DATE 17-NOV-82 ENG. Mel Bloomberg
DATE 17-NOV-82 EC/ECO LOCATION:
DATE 17-NOV-82 SHEET 1 OF 1
DATE 17-NOV-82

TITLE: DELNA LINK MODULE (LNK)

DSKD:<SARGENT>LNKTDC.DRW 17-NOV-82 11:32 NEXT HIGHER ASSEMBLY:
FIRST USED ON OPTION/MODEL: DELNA

SIZE CODE	NUMBER	REV.
K CS	M7793-0-TDC	A



TRANSMIT BYTE/FRAME TIMING-LNKJ

TIMING DIAGRAM-4

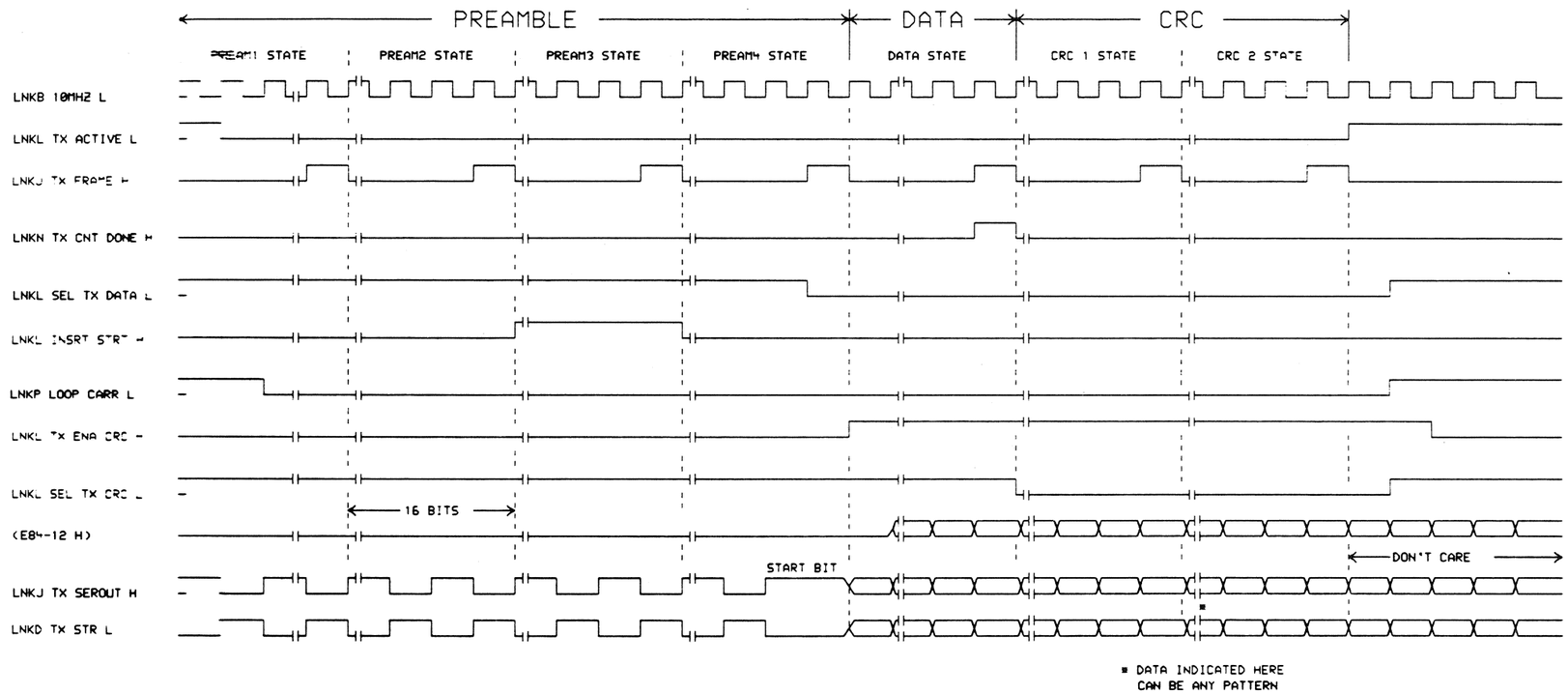
REVISIONS		
CHK	CHANGE NO.	REV

digital

DRN. PAUL HEBERT" DATE 17-NOV-82
ENG. Neil Bloomberg DATE 17-NOV-82
CHK DATE 17-NOV-82
BOARD LOCATION:
SHEET 1 OF 1
DSKD:<SARGENT>LNKTDD.DRW 17-NOV-82 11:02
NEXT HIGHER ASSEMBLY: [illegible]-M7793-0-0
FIRST USED ON OPTION/MODEL: DELUNA

TITLE: DELUNA LINK MODULE (LNK)

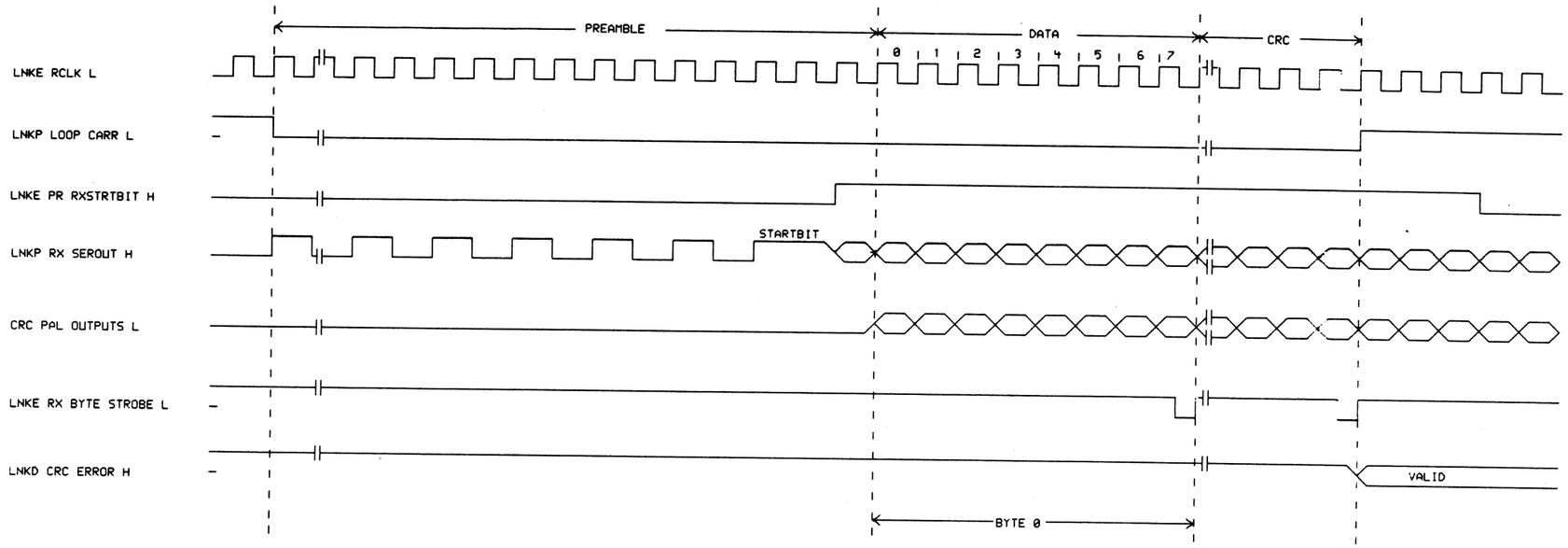
SIZE	CODE	NUMBER	REV.
K	CS	M7793-0-TDD	A



TRANSMIT BIT STREAM-LNKD
TIMING DIAGRAM-5

REVISIONS		
CHK	CHANGE NO.	REV

DRN. CARLSON	DATE 17-NOV-82	ENG. Neil Bloomberg	DATE 17-NOV-82	TITLE: DEUNA LINK MODULE (LNK)
CHK'D.	DATE 17-NOV-82	BOARD LOCATION: SHEET 1 OF 1		
DSKD:<SARGENT>LNKTDE.DRW 17-NOV-82 11:02		NEXT HIGHER ASSEMBLY: D-UA-M7793-0-0		SIZE K / CODE CS / NUMBER M7793-0-TDE / REV. A
FIRST USED ON OPTION/MODEL: DEUNA				



RECEIVE CRC-LNKD

TIMING DIAGRAMS-6

REVISIONS		
CHK	CHANGE NO.	REV

DRN. PAUL HEBERT" DATE 19-NOV-82 ENG. Neil Blomberg DATE 19-NOV-82

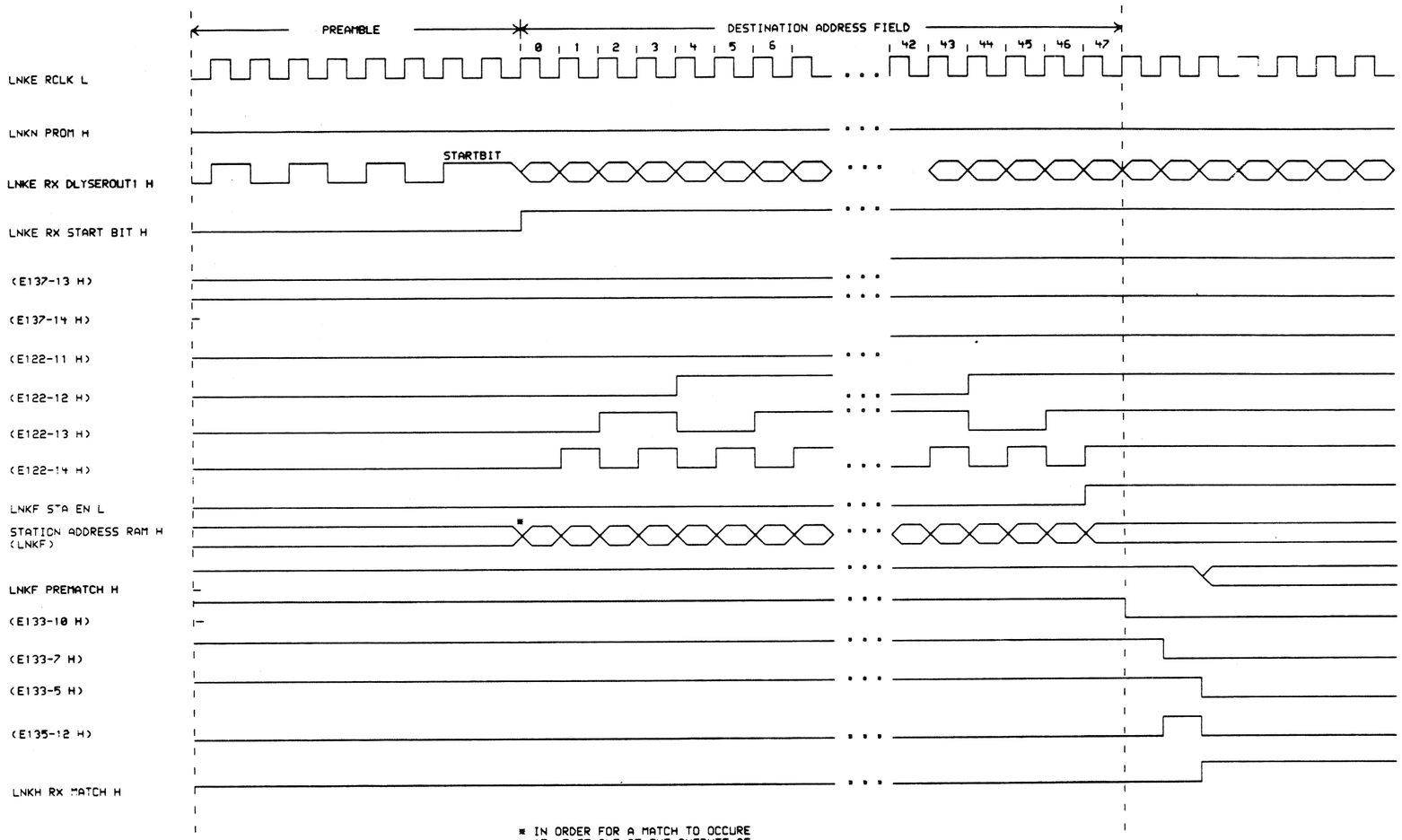
CHK. DATE BOARD LOCATION:

DSKD:<SARGENT>LNKTDF.DRW 19-NOV-82 08:44 NEXT HIGHER ASSEMBLY: SHEET 1 OF 1

FIRST USED ON OPTION/MODEL: DELUNA

TITLE: DELUNA LINK MODULE (LNK)

SIZE	CODE	NUMBER	REV.
K	CS	M7793-0-TDF	A



* IN ORDER FOR A MATCH TO OCCURE
AT LEAST ONE OF THE OUTPUTS OF
THE STATION ADDRESS RAM MUST
MATCH THE SIGNAL LNKE RX DIY SEROUT1 H
FOR ALL 48 BITS OF THE DESTINATION ADDRESS FIELD.

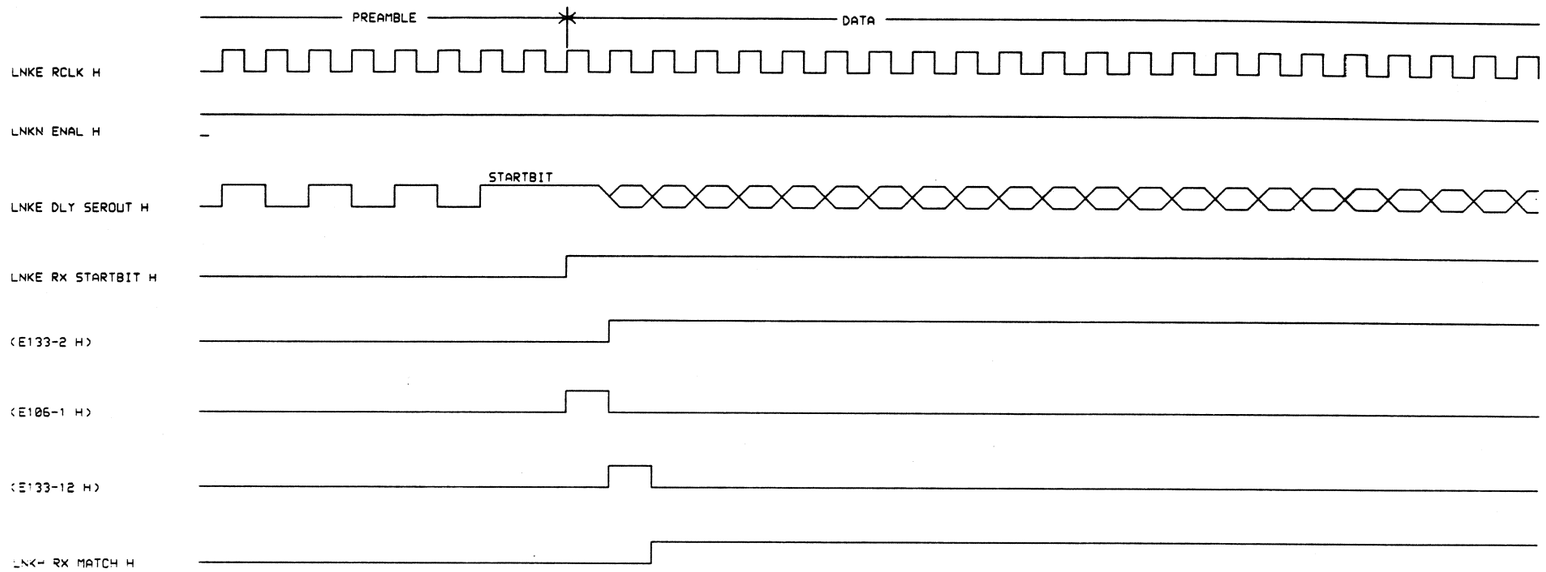
STATION ADDRESS DETECTION-LNKF, LNKH
48 BIT ADDRESS RECOGNITON
TIMING DIAGRAM-7

REVISIONS		
CHK	CHANGE NO.	REV

DRN. C. GIROUARD
CHK'D.
DATE ENG. 17-NOV-82 Neil Bloomberg
DATE BOARD LOCATION: 17-NOV-82
SHEET 1 OF 1
DATE 17-NOV-82
DSKD1:<SARGENT>LNKTDH.DRW;17-NOV-82 11:22
NEXT HIGHER ASSEMBLY: D-UA-M7793-0-0
FIRST USED ON OPTION/MODEL: DELUNA

TITLE: DELUNA LINK MODULE (LNK)

SIZE	CODE	NUMBER	REV.
K	CS	M7793-0-TDH	A



STATION ADDRESS DETECTION-LNKH

ENABLE ALL MULTICAST

TIMING DIAGRAM -8

REVISIONS		
CHK	CHANGE NO.	REV

DRN. "PAUL HEBERT" | DATE 17-NOV-82 | ENG. Neil Bloomberg | DATE 17-NOV-82

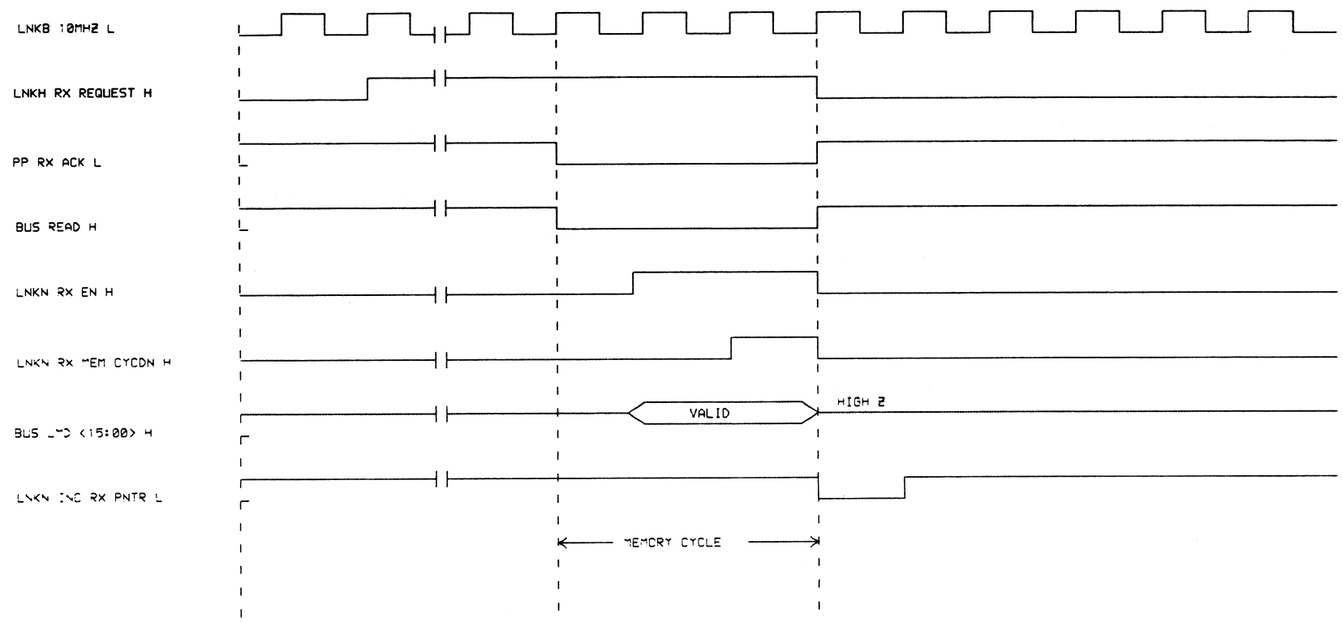
CHKD. | DATE 17-NOV-82 | BOARD LOCATION:

DSKD: <SARGENT>LNKTDJ.DRW 17-NOV-82 11:04 | SHEET 1 OF 1 | NEXT HIGHER ASSEMBLY:

FIRST USED ON OPTION/MODEL: DELNA | D-UA-M7793-0-0

TITLE: DELNA LINK MODULE (LNK)

SIZE	CODE	NUMBER	REV.
K	CS	M7793-0-TDJ	A



RECEIVE LINK MEMORY BUS TRANSFER - LNKE, LNKH, LNKN

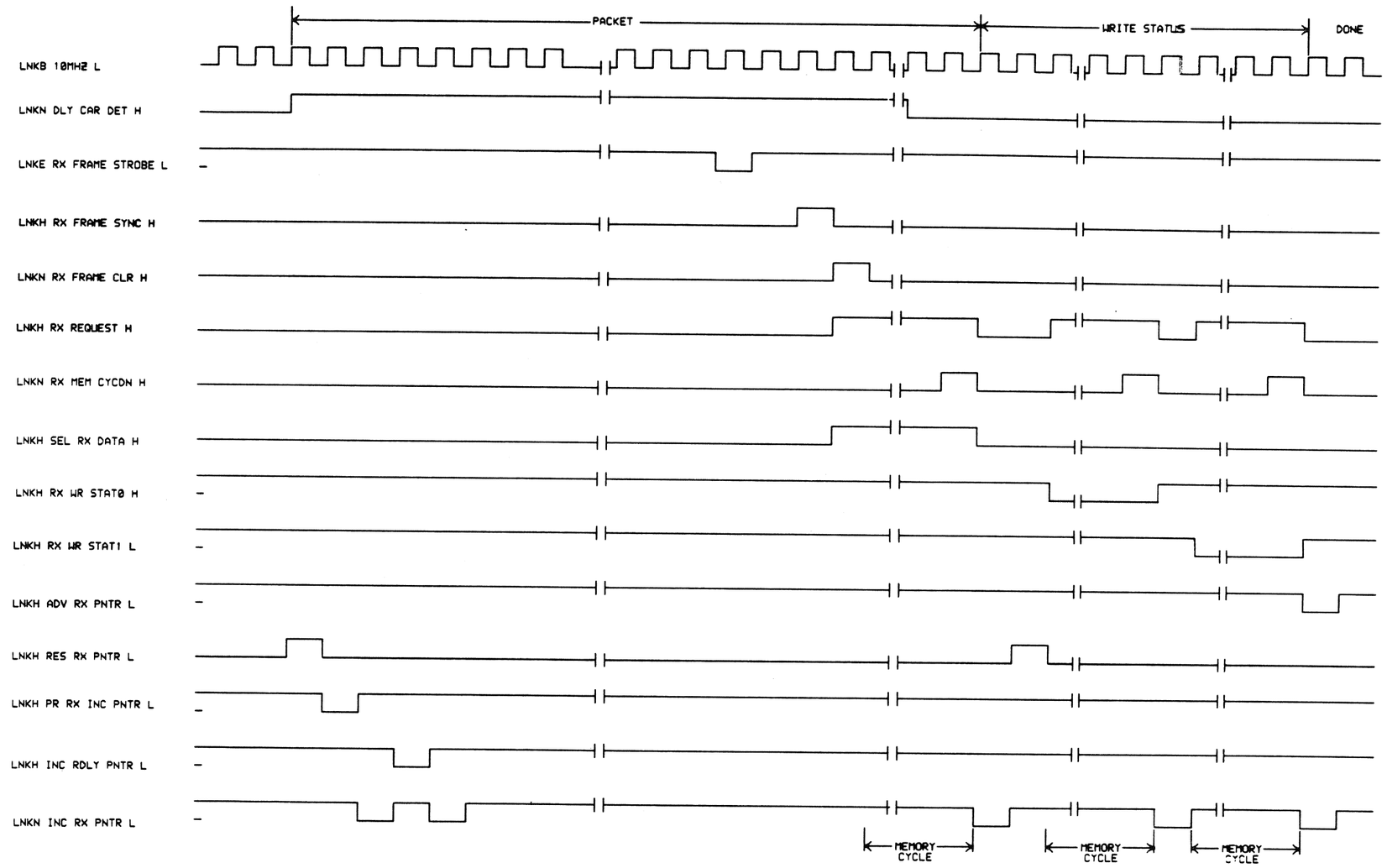
TIMING DIAGRAM-9

REVISIONS		
CHK	CHANGE NO.	REV

DRN. C. GIROUARD" DATE 17-NOV-82
CHK'D. DATE 17-NOV-82
ENG. Neil Bloomberg DATE 17-NOV-82
SCALE NONE SHEET 1 OF 1
DSKD:<SARGENT>LNKTDK.DRW 17-NOV-82 11:02
FIRST USED ON OPTION/MODEL: DELUNA
NEXT HIGHER ASSEMBLY: M7793-0-0

TITLE: DELUNA LINK MODULE (LNK)

SIZE	CODE	NUMBER	REV.
K	CS	M7793-0-TDK	A



LINK RECEIVE MEMORY BUS TRANSFER-LNKE,LNKH,LNKN

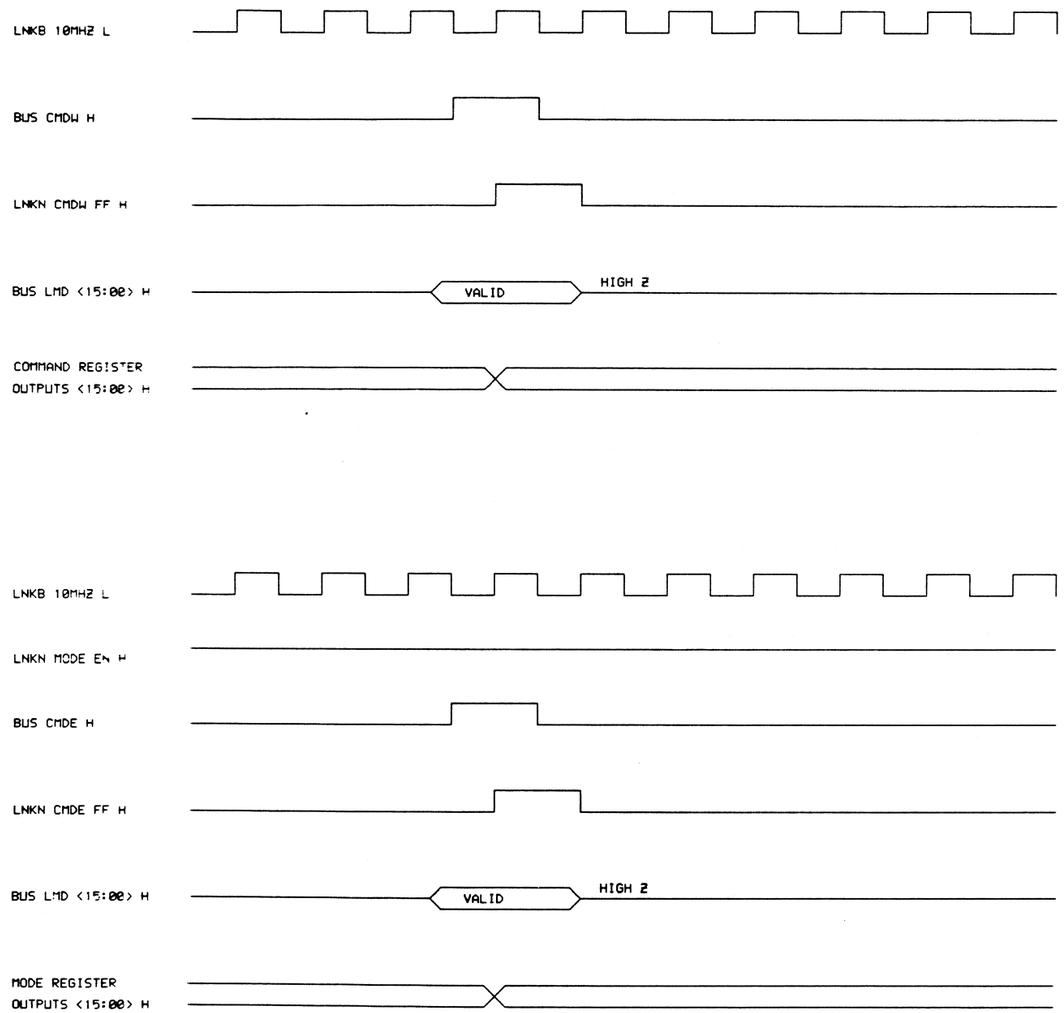
TIMING DIAGRAMS-10

REVISIONS		
CHK	CHANGE NO.	REV

DRN. PAUL HEBERT" DATE 17-NOV-82
CHK: D. DATE 17-NOV-82
ENG. Neil Bloomberg DATE 17-NOV-82
BOARD LOCATION: SHEET 1 OF 1
DSKD:<SARGENT>LNKTDL.DRW 17-NOV-82 11:04
NEXT HIGHER ASSEMBLY: D-UA-M7793-0-0
FIRST USED ON OPTION/MODEL: DELUNA

TITLE: DELUNA LINK MODULE (LNK)

SIZE	CODE	NUMBER	REV.
K	CS	M7793-0-TDL	A



COMMAND REGISTER
WRITE OPERATION

MODE REGISTER
WRITE OPERATION

CONTROL REGISTERS-LNKN

TIMING DIAGRAM-11

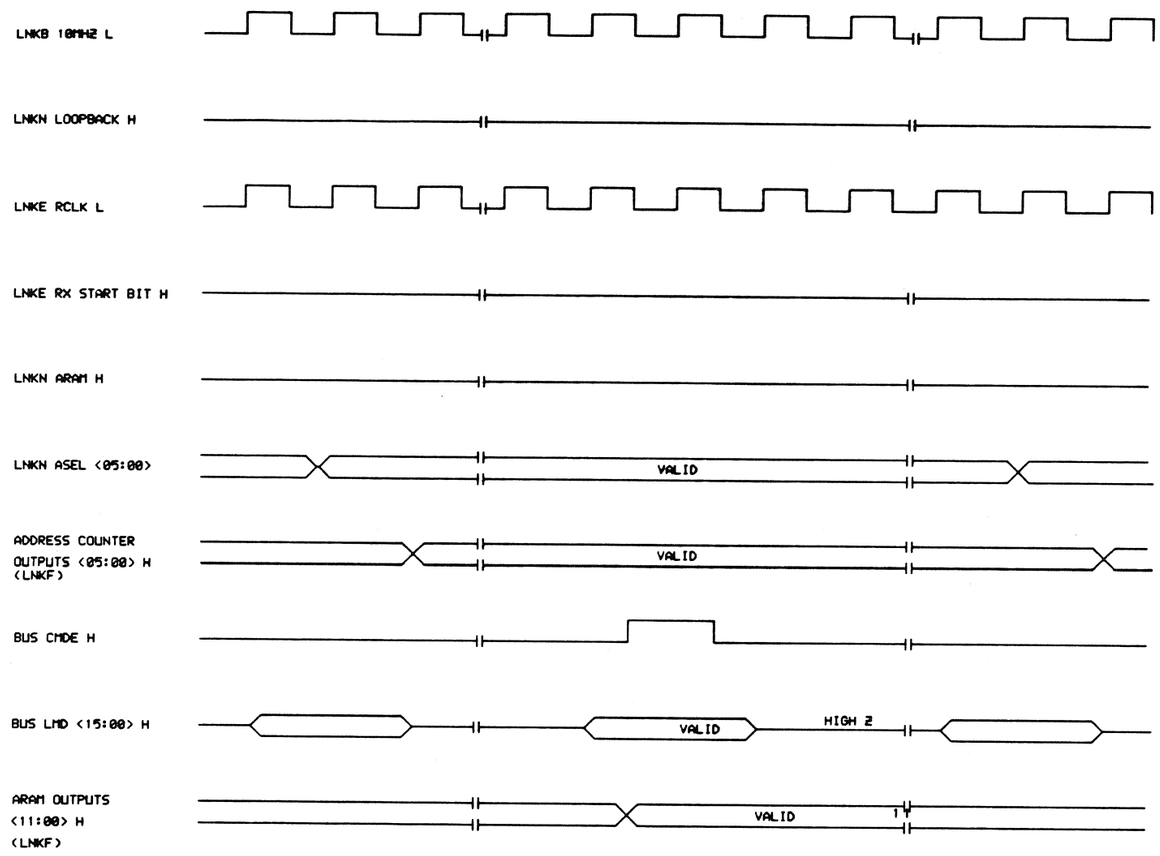
REVISIONS		
CHK	CHANGE NO.	REV

digital

DRN. CARLSON | DATE 17-NOV-82 | ENG. Neil Bloomberg | DATE 17-NOV-82
CHK'D. | DATE 17-NOV-82 | BOARD LOCATION: | SHEET 1 OF 1
DSKD:<SARGENT>LNKTDM.DRW 17-NOV-82 11:02 | NEXT HIGHER ASSEMBLY: D-UA-M7793-0-0
FIRST USED ON OPTION/MODEL: DELNA

TITLE: DELNA LINK MODULE (LNK)

SIZE	CODE	NUMBER	REV.
K	CS	M7793-0-TDM	A



STATION ADDRESS RAM WRITE-LNKF

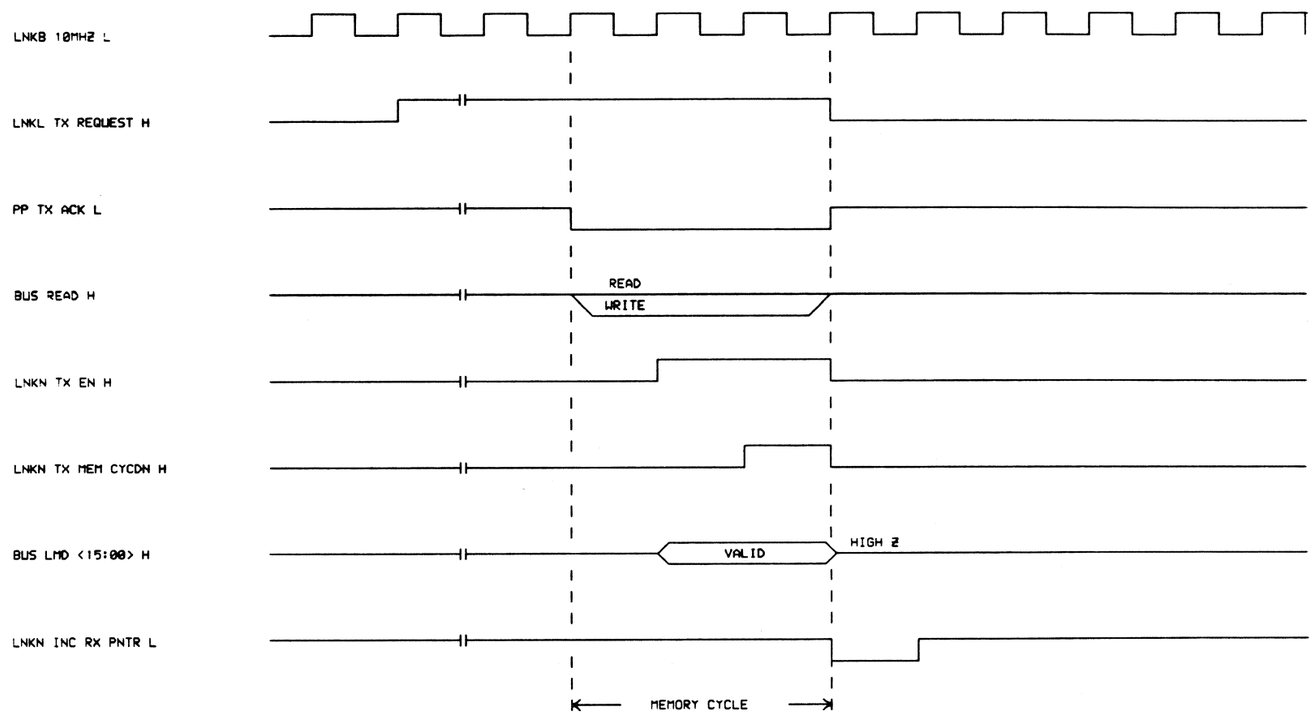
TIMING DIAGRAM-12

REVISIONS		
CHK	CHANGE NO.	REV

DRN. CARLSON
CHKD.
DATE 17-NOV-82
ENG. Neil Bloomberg
DATE 17-NOV-82
DATE 17-NOV-82
SHEET 1 OF 1
DSKD:<SARGENT>LNKTDN.DRW 17-NOV-82 11:02
FIRST USED ON OPTION/MODEL: DELUNA
NEXT HIGER ASSEMBLY: D-JA-M7793-0-0

TITLE: DELUNA LINK MODULE (LNK)

SIZE	CODE	NUMBER	REV.
K	CS	M7793-0-TDN	A



TRANSMIT MEMORY BUS TRANSFER-LNKJ,L,N

TIMING DIAGRAM-13

REVISIONS		
CHK	CHANGE NO.	REV

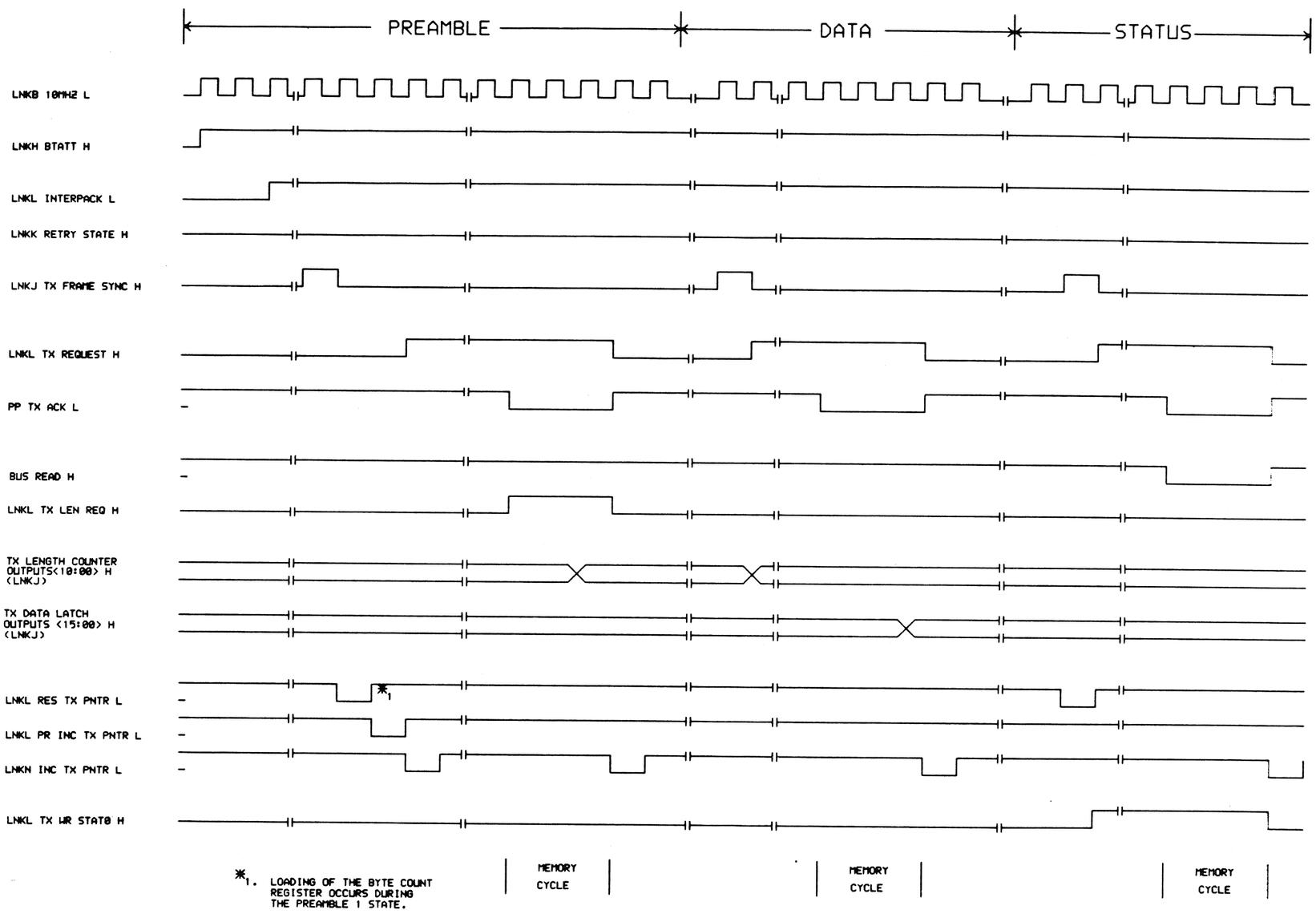
digital

DRN. CARLSON — DATE 17-NOV-82
ENG. Neil Bloomberg — DATE 17-NOV-82
CHK'D. — DATE 17-NOV-82
BOARD LOCATION:
SHEET 1 OF 1

DSKD:<SARGENT>LNKTDP.DRW 17-NOV-82 11:03 NEXT HIGHER ASSEMBLY:
FIRST USED ON OPTION/MODEL: DELNA — D-JS-M7793-0-0

TITLE: DELNA LINK MODULE (LNK)

SIZE	CODE	NUMBER	REV.
K	CS	M7793-0-TDP	A



*1. LOADING OF THE BYTE COUNT REGISTER OCCURS DURING THE PREAMBLE 1 STATE.

TRANSMIT LINK MEMORY TRANSFER-LNKJ,LNKL,LNKN

TIMING DIAGRAM-14

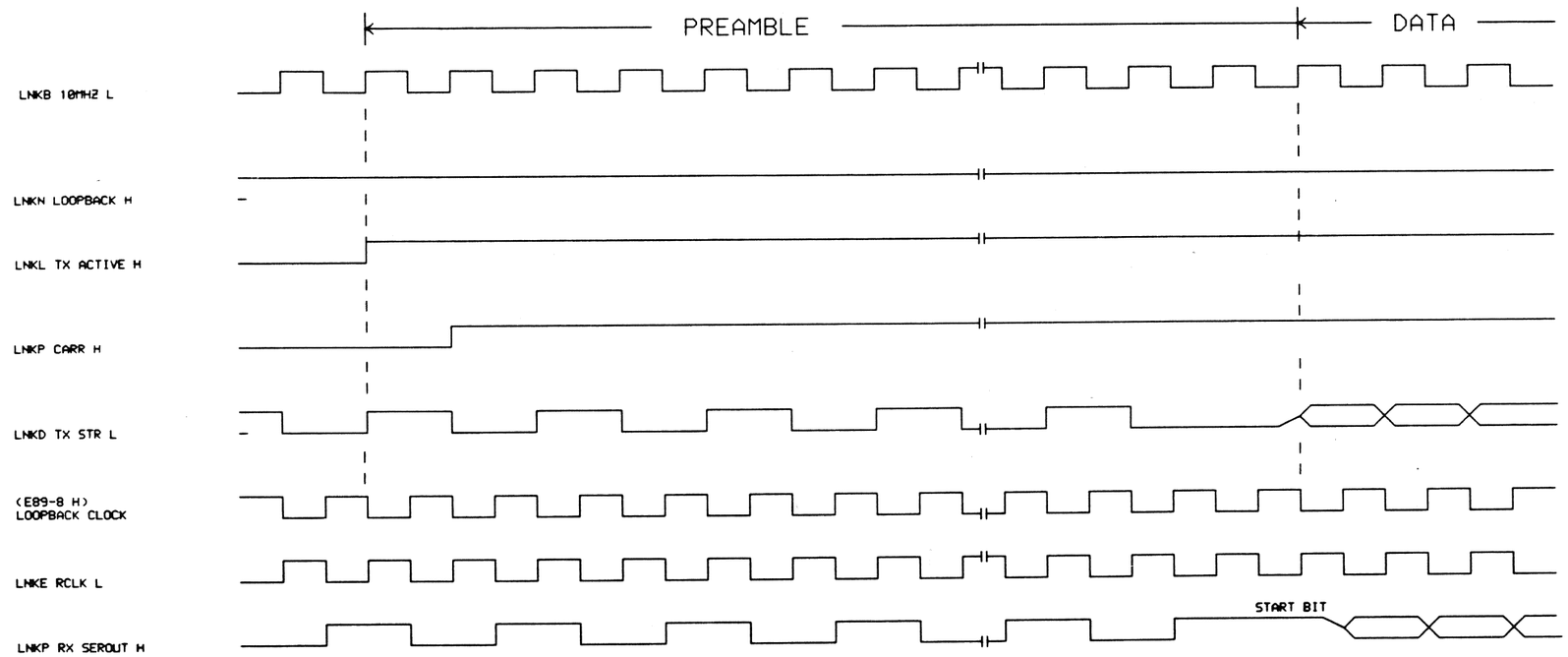
REVISIONS		
CHK	CHANGE NO.	REV

digital

DRN. CARLSON
CHK'D.
DATE ENG. 17-NOV-82 Neil Bloomberg
DATE 17-NOV-82
DATE 17-NOV-82 BOARD LOCATION:
17-NOV-82 SHEET 1 OF 1
DSKD:<SARGENT>LNKTDR.DRW 17-NOV-82 11:05
NEXT HIGHER ASSEMBLY: D-UA-M7793-0-0
FIRST USED ON OPTION/MODEL: DELUNA

TITLE: DELUNA LINK MODULE (LNK)

SIZE	CODE	NUMBER	REV.
K	CS	M7793-0-TDR	A



LOOPBACK LNKP,LNKL

TIMING DIAGRAM-15

REVISIONS		
CHK	CHANGE NO.	REV

digital

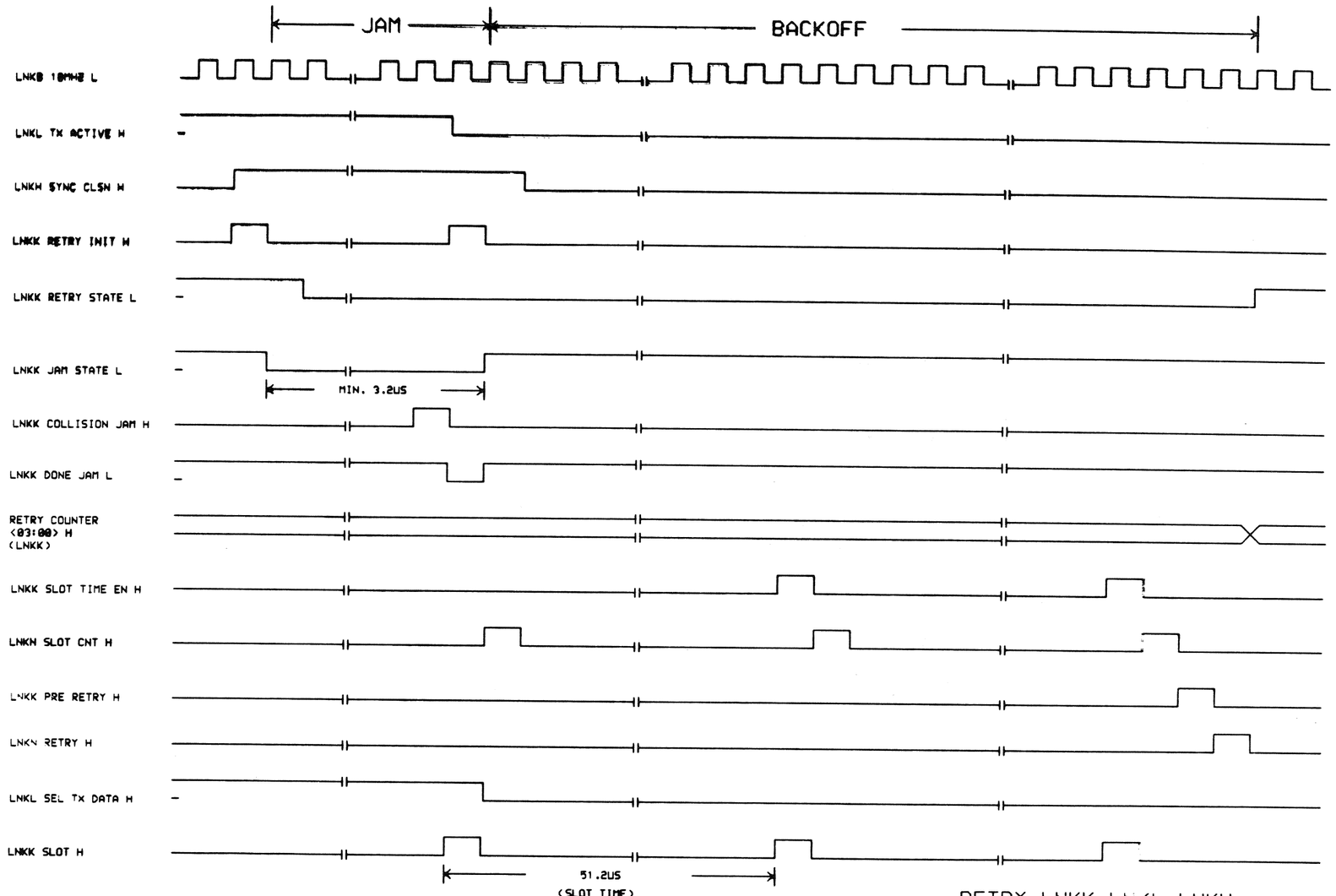
DSKD:<SARGENT>LNKTDS.DRW 17-NOV-82 11:03

FIRST USED ON OPTION/MODEL: DELUNA

DRN. CARLSON	DATE 17-NOV-82	ENG. Neil Bloomberg	DATE 17-NOV-82
CHKD.	DATE 17-NOV-82	BOARD LOCATION: SHEET 1 OF 1	
		NEXT HIGHER ASSEMBLY: D-LA-M7793-0-0	

TITLE: DELUNA LINK MODULE (LNK)

SIZE	CODE	NUMBER	REV.
K	CS	M7793-0-TDS	A



RETRY-LNKK,LNKL,LNKN
JAM AND BACKOFF
TIMING DIAGRAM-16

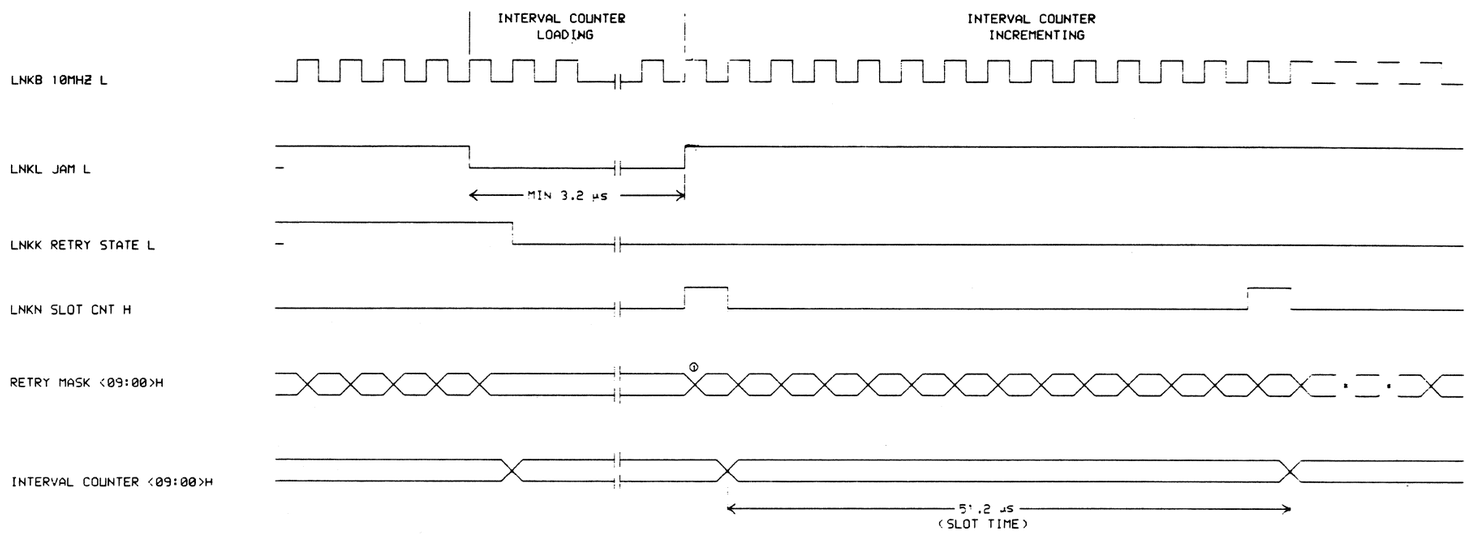
REVISIONS		
CHK	CHANGE NO.	REV

digital

DRN. CARLSON
CHKD. R. Sargent
DATE 17-NOV-82 ENG. Neil Bloomberg DATE 17-NOV-82
DATE 17-NOV-82 BOARD LOCATION:
SHEET 1 OF 1
DSKD:<SARGENT>LNKTDT.DRW 17-NOV-82 11:03 NEXT HIGHER ASSEMBLY:
FIRST USED ON OPTION/MODEL: DELNA D-UA-M7793-0-0

TITLE: DELNA LINK MODULE (LNK)

SIZE	CODE	NUMBER	REV.
K	CS	M7793-0-TDT	A



① RETRY MASK <09:00>H IS CLOCK BY LNKL OSC L AND HENCE IS ASYNCHRONIS TO 10MHZ L.

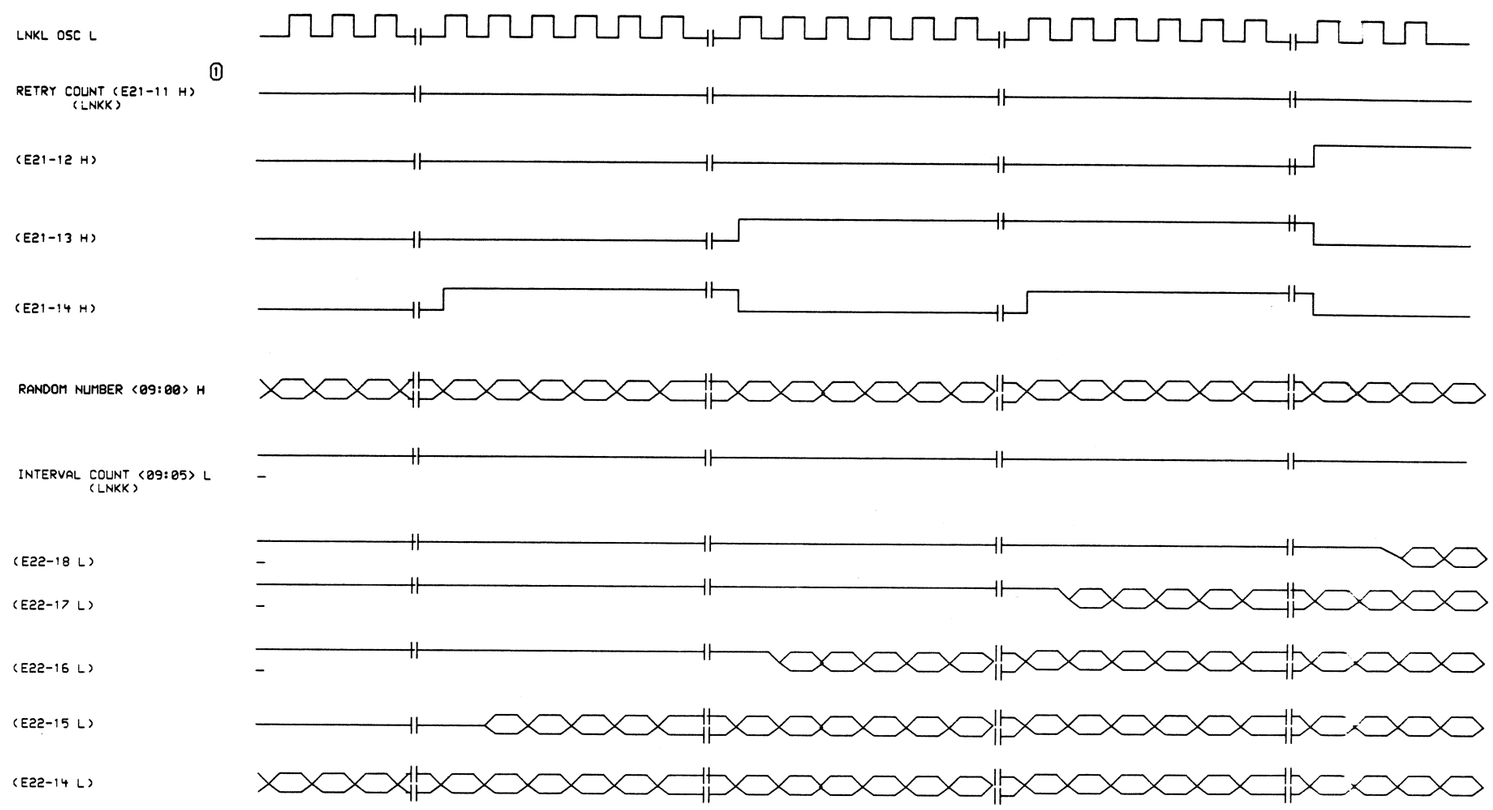
RETRY-LNKK,LNKL
LOADING OF INTERVAL COUNTER
TIMING DIAGRAM-17

REVISIONS		
CHK	CHANGE NO.	REV

DRN. PAUL HEBERT
CHK'D
DATE 17-NOV-82
DATE 17-NOV-82
DATE 17-NOV-82
DSKD:<SARGENT>LNKTDU.DRW 17-NOV-82 11:05
FIRST USED ON OPTION/MODEL: DELNA

TITLE: DELUNA LINK MODULE (LNK)

SIZE	CODE	NUMBER	REV.
K	CS	M7793-0-TDU	A



NOTE 1. THIS COUNT IS INCREMENTED AT THE DEASSERTION OF RNKK RETRY STATE L.

RETRY-LNKK .LNKL

RANDOM NUMBER MASK OPENING

TIMING DIAGRAM-18

REVISIONS		
CHK	CHANGE NO.	REV

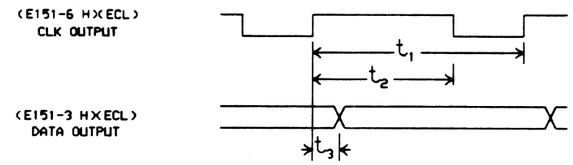
DRN. C. GIROUARD" DATE 17-NOV-82 ENG. Neil Bloomberg DATE 17-NOV-82 CHK. D. Sargent DATE 17-NOV-82 BOARD LOCATION: SHEET 1 OF 1

DSKD:<SARGENT>LNKTDV.DRW 17-NOV-82 11:06 NEXT HIGHER ASSEMBLY:

FIRST USED ON OPTION/MODEL: DEUNA D-A-M7793-0-0

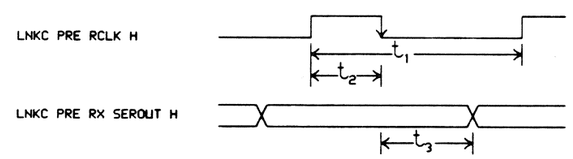
TITLE: DEUNA LINK MODULE (LNK)

SIZE	CODE	NUMBER	REV.
K	CS	M7793-0-TDV	A



PARAMETER	MIN	TYPE	MAX
t_1	80	100	120
t_2	26	50	70
t_3		2	

MANCHESTER DECODER -



PARAMETER	MIN	TYPE	MAX
t_1	80	100	120
t_2		30	
t_3		50	

CLOCK SHAPER -

RECEIVE CLOCK, DATA OUTPUTS-LNKC

TIMING DIAGRAMS-19

REVISIONS		
CHK	CHANGE NO.	REV

DRN. PAUL HEBERT" DATE 17-NOV-82 | ENG. Neil Bloomberg DATE 17-NOV-82 | CHK'D DATE 17-NOV-82 | BOARD LOCATION: | SHEET 1 OF 1

DSKD:<SARGENT>LNKTDW.DRW|17-NOV-82 11:43 | NEXT HIGHER ASSEMBLY:

FIRST USED ON OPTION/MODEL: DELNA | C-LA-M7793-0-0

TITLE: DELNA LINK MODULE (LNK)

SIZE	CODE	NUMBER	REV.
K	CS	M7793-0-TDW	A