VAX 6000-400

VAX 6000–400 Options and Maintenance

Order Number EK–640EB–MG–002

This manual is intended for Digital customer service representatives. It covers the installation of modules and removal and replacement of field-replaceable units (FRUs).

digital equipment corporation
maynard, massachusetts

First Printing, July 1989
Revised, June 1990

Contents

Chapter 3 KA64A Scalar Processor

Chapter 4 FV64A Vector Processor

Chapter 5 MS62A Memory

Chapter 6 DWMBA XMI-to-VAXBI Adapter

Chapter 7 XMI Card Cage

Chapter 8 VAXBI Card Cage

Chapter 9 Control Subsystem Assemblies

Chapter 10 Power Subsystem

Chapter 11 Cabinet and Airflow Subsystem

Appendix A Troubleshooting the System

Appendix B Console Error Messages

Appendix C Cable List

Appendix D XMI Backplane Connectors

Appendix E Parse Trees

Glossary

Index

Examples

Figures

Tables

Preface

Intended Audience

This manual is written for Digital customer service representatives servicing the VAX 6000–400 system. This manual covers the installation of modules and removal and replacement of field-replaceable units (FRUs).

Document Structure

The manuals in the VAX 6000–400 documentation set are designed using structured documentation theory. Each topic has a boldface indented abstract, to help you use the manual as a reference tool. Other typical components of a topic include an illustration or example, a chart or list, and descriptive text.

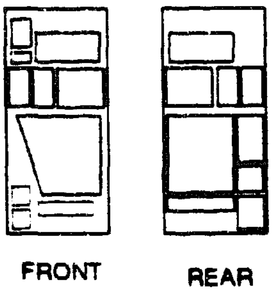
This manual has 11 chapters and six appendixes:

- **Chapter 1, Introduction,** gives an overview of the system, including system specifications, field-replaceable units, system architecture, and location of major assemblies.
- **Chapter 2, Diagnostics,** describes the VAX 6000–400 self-test and the general methods for running ROM-based diagnostics and software diagnostics under the VAX Diagnostic Supervisor.
- **Chapter 3, KA64A Scalar Processor, Chapter 4, FV64A Vector Processor, Chapter 5, MS62A Memory,**, and **Chapter 6, DWMBA Adapter,** give module specifications, configuration rules, main registers, module diagnostics, and self-test information.
- **Chapter 7, XMI Card Cage,** and **Chapter 8, VAXBI Card Cage,** describe the system card cage and the I/O card cage, respectively, and their removal and replacement procedures.
- **Chapter 9, Control Subsystem Assemblies,** presents the four subassemblies housed in the system control assembly area and gives the removal and replacement instructions for each subassembly.

- **Chapter 10, Power Subassemblies,** discusses each field-replaceable unit of the power system, its diagnostics, and the removal and replacement procedure for the unit.
- **Chapter 11, Cabinet and Airflow Subsystem,** presents the field-replaceable units that are specific to the cabinet and their removal and replacement instructions.
- **Appendix A** is a troubleshooting chart. **Appendix B** lists the console error messages. **Appendix C** is the cable list. **Appendix D** shows the pin numbering of XMI backplane connectors. **Appendix E** gives the parse trees for the KA64A and FV64A processor modules. A **Glossary** and **Index** provide additional reference support.

Conventions Used in This Document

The icons shown below are used for designating part placement in VAX 6000–400 systems. A shaded area in the icon shows the location of the component or part being discussed.



VAX 6000–400 Documents

Documents in the VAX 6000–400 documentation set include:

Title	Order Number
VAX 6000–400 Installation Guide	EK–640EA–IN
VAX 6000–400 Owner's Manual	EK–640EA–OM
VAX 6000–400 Mini-Reference	EK–640EA–HR
VAX 6000–400 System Technical User's Guide	EK–640EB–TM
VAX 6000–400 Options and Maintenance	EK–640EB–MG
VAX 6000 Series Upgrade Manual	EK–600EB–UP
VAX 6000 Series Vector Processor Owner's Manual	EK–60VAA–OM
VAX 6000 Series Vector Processor Programmer's Guide	EK–60VAA–PG

Associated Documents

Other documents that you may find useful include:

Title	Order Number
CIBCA User Guide	EK–CIBCA–UG
DEBNI Installation Guide	EK–DEBNI–IN
Guide to Maintaining a VMS System	AA–LA34A–TE
Guide to Setting Up a VMS System	AA–LA25A–TE
HSC Installation Manual	EK–HSCMN–IN
H4000 DIGITAL Ethernet Transceiver Installation Manual	EK–H4000–IN
H7231 Battery Backup Unit User's Guide	EK–H7231–UG
Installing and Using the VT320 Video Terminal	EK–VT320–UG
Introduction to VMS System Management	AA–LA24A–TE
KDB50 Disk Controller User's Guide	EK–KDB50–UG
RA90 Disk Drive User Guide	EK–ORA90–UG
RV20 Optical Disk Owner's Manual	EK–ORV20–OM

Title	Order Number
SC008 Star Coupler User's Guide	EK–SC008–UG
TK70 Streaming Tape Drive Owner's Manual	EK–OTK70–OM
TU81/TA81 and TU81 PLUS Subsystem User's Guide	EK–TUA81–UG
ULTRIX–32 Guide to System Exercisers	AA–KS95B–TE
VAX Architecture Reference Manual	EY–3459E–DP
VAX Systems Hardware Handbook — VAXBI Systems	EB–31692–46
VAX Vector Processing Handbook	EC–H0419–46
VAXBI Expander Cabinet Installation Guide	EK–VBIEA–IN
VAXBI Options Handbook	EB–32255–46
VMS Installation and Operations: VAX 6000 Series	AA–LB36B–TE
VMS Networking Manual	AA–LA48A–TE
VMS System Manager's Manual	AA–LA00A–TE
VMS VAXcluster Manual	AA–LA27A–TE
VMS Version 5.4 New and Changed Features Manual	AA–MG29C–TE

CHAPTER 1

Chapter 1
Introduction

This chapter introduces the VAX 6000–400 system, its architecture and system specifications, the location of components in the cabinet, and the field-replaceable unit list. Sections include:

- System Physical Description
- System Functional Description
- VAX 6000–400 Front View
- VAX 6000–400 Rear View
- Field-Replaceable Units

1.1 System Physical Description

A typical VAX 6000–400 system has a main cabinet with a TK tape drive, a console terminal and printer, storage cabinets, an accessories kit, and a set of documentation.

Figure 1–1: Typical VAX 6000–400 System

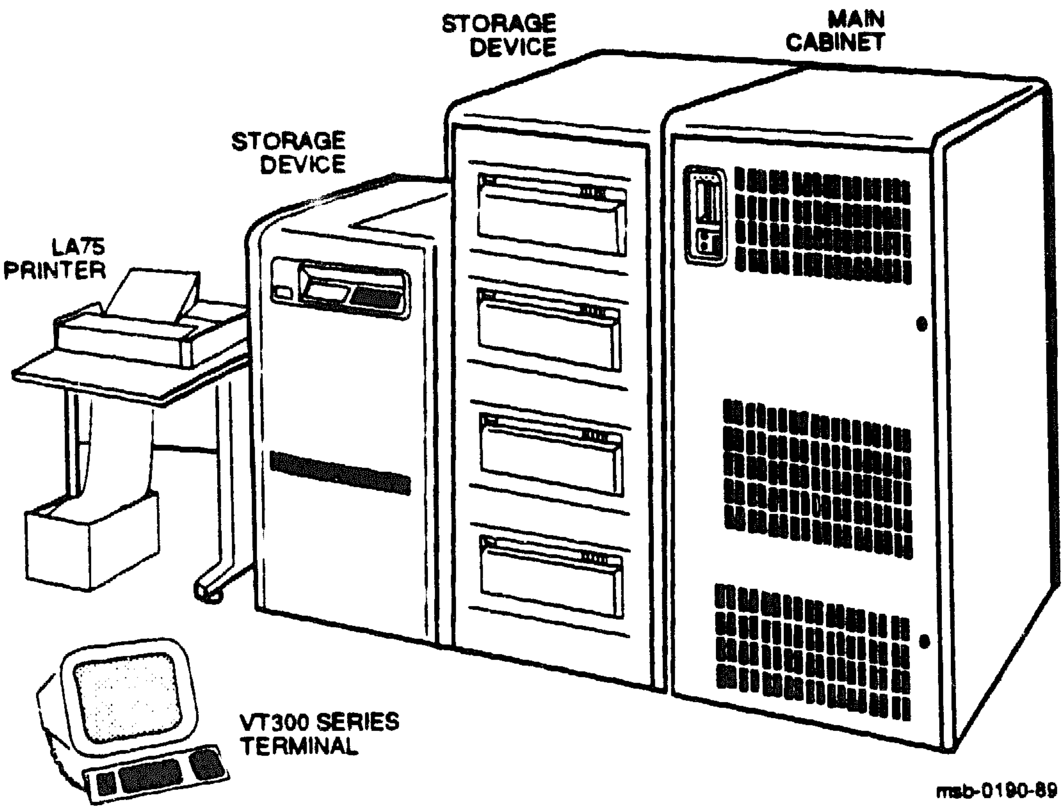


Figure 1–1 shows a typical system.

- **The main cabinet** houses a TK tape drive, the XMI card cage (which contains the processors and memories), two VAXBI card cages, the control panel switches, status indicators, and restart controls.
- **The TK tape drive** in the main cabinet is used for installing operating systems, software, and some diagnostics.
- **The storage cabinets** have local storage and archiving capability.
- **The console terminal** is used for console and system management operations.
- **VAX 6000–400 documentation** that ships with the system includes:
  - *VAX 6000–400 Installation Guide*
  - *VAX 6000–400 Owner's Manual*
  - *VAX 6000–400 Mini-Reference*

  See the Preface for a complete list of system documentation and associated documents.

Table 1-1: VAX 6000-400 System Characteristics

Physical		cm (in)
	Height	154 (60.5)
	Width	78 (30.5)
	Depth	76 (30.0)
	Weight	318 kg (700 lbs)
Environmental		
Heat dissipation (max)		5440 Btu/hr (5712 KJ/hr)
Operating temperature	TK not in use	10° to 40°C (50° to 104°F)
	TK in use	15° to 32°C (59° to 90°F)
Operating humidity	TK not in use	10% to 90% relative humidity
	TK in use	20% to 80% relative humidity
Altitude	Non-operational	2.4 to 9.1 km (8000 to 30,000 ft)
	Operating	0 to 2.4 km (0 to 8000 ft)
Cooling System		
	Type	Pressurized, with air moving device
	Air mover	Dual backward curved blowers
	Air source	Filtered ambient air

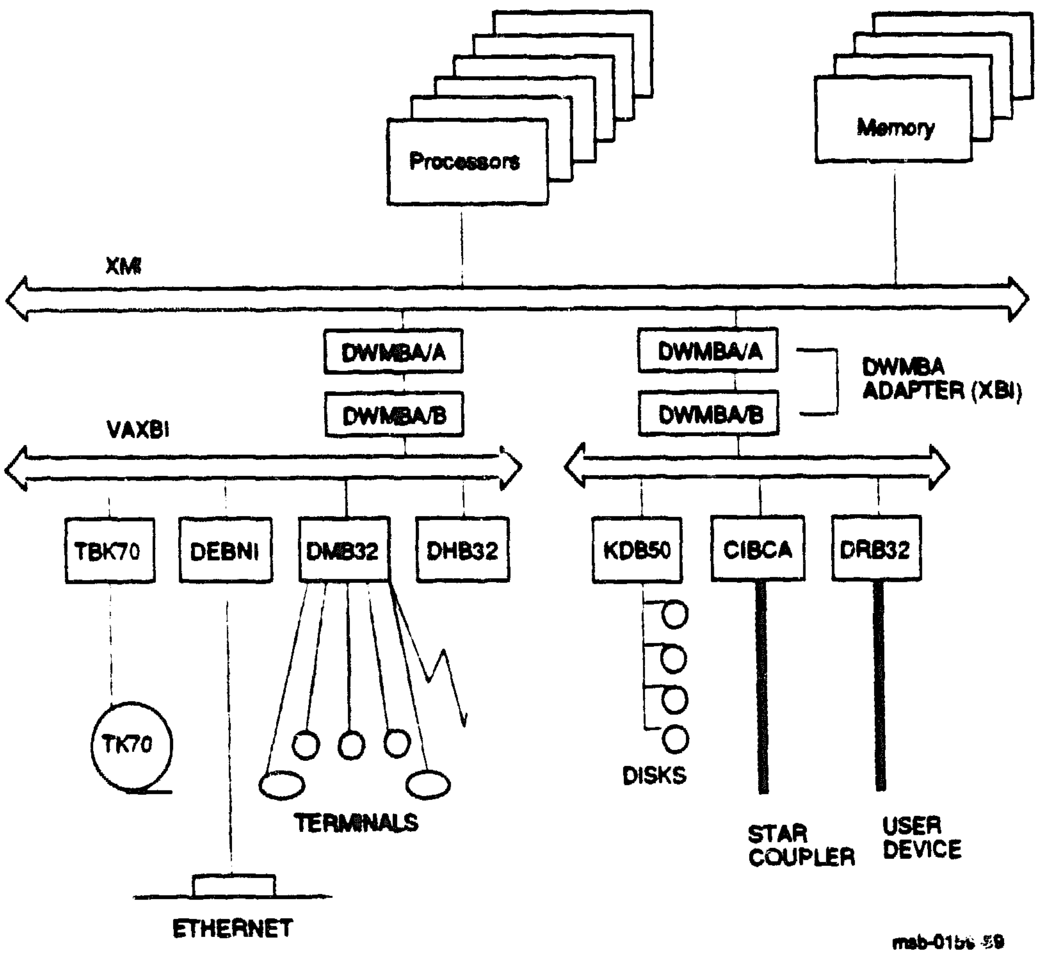
Table 1–1 (Cont.): VAX 6000–400 System Characteristics

Electrical		
AC power consumption (max)		1.6 kW
AC current (max)	60 Hz	8 A (208 V)
	50 Hz	4 A (416 V), 4.5 A (380 V)
Voltage input	60 Hz	3-phase 208 V RMS
	50 Hz	3-phase 380/416 V RMS
Frequency tolerance		47–63 Hz
Surge current		60 A

1.2 System Functional Description

The VAX 6000–400 system supports multiprocessing with up to six KA64A processors. The system uses the XMI bus to interconnect its KA64A processors and its MS62A memory modules. All I/O devices connect to the VAXBI bus.

Figure 1–2: VAX 6000–400 System Architecture



The XMI bus is the VAX 6000–400 system bus; the VAXBI bus supports the I/O subsystem. The XMI bus is a 64-bit system bus[1] that interconnects the central processors, memory modules, and VAXBI I/O adapters.

The VAXBI and XMI buses share similar but incompatible connector and module architecture. Both the VAXBI and XMI buses use the concept of a **node**. A node is a single functional unit that consists of one or more modules.

The XMI bus has three types of nodes: processor nodes (KA64A), memory nodes (MS62A), and the XMI-to-VAXBI I/O adapters (DWMBA).

A **processor node**, called a KA64A, is a single-board VAX processor. It contains a central processor unit (CPU) chip, a floating-point processor, primary and secondary cache, an EEPROM for system parameters, and three custom VLSI components for interfacing to the XMI bus.

Processors communicate with main memory over the XMI bus. The system supports multiprocessing of up to six processors. One processor becomes the boot processor during power-up, and that boot processor handles all system communication. The other processors become secondary processors and are started by the primary processor (see Section 3.4).

A **memory node** is an MS62A. Memory is a global resource equally accessible by all processors on the XMI bus. Each MS62A module has 32 Mbytes of memory, consisting of MOS 1-Mbit dynamic RAMs, ECC logic, and control logic. Memory access is automatically interleaved between modules. An optional battery backup unit protects memory in case of power failure.

An **XMI-to-VAXBI adapter**, called a **DWMBA**, is a two-board adapter that transfers data between these two buses. The DWMBA/A module is installed on the XMI bus; it is cabled to the DWMBA/B module on the VAXBI bus. Every VAXBI bus on this system must have a DWMBA adapter. Therefore, systems with two VAXBI channels have two DWMBA/A modules on the XMI bus, and each VAXBI channel has a DWMBA/B module in its card cage. System error messages and self-test results refer to the pair of DWMBA modules as XBI.

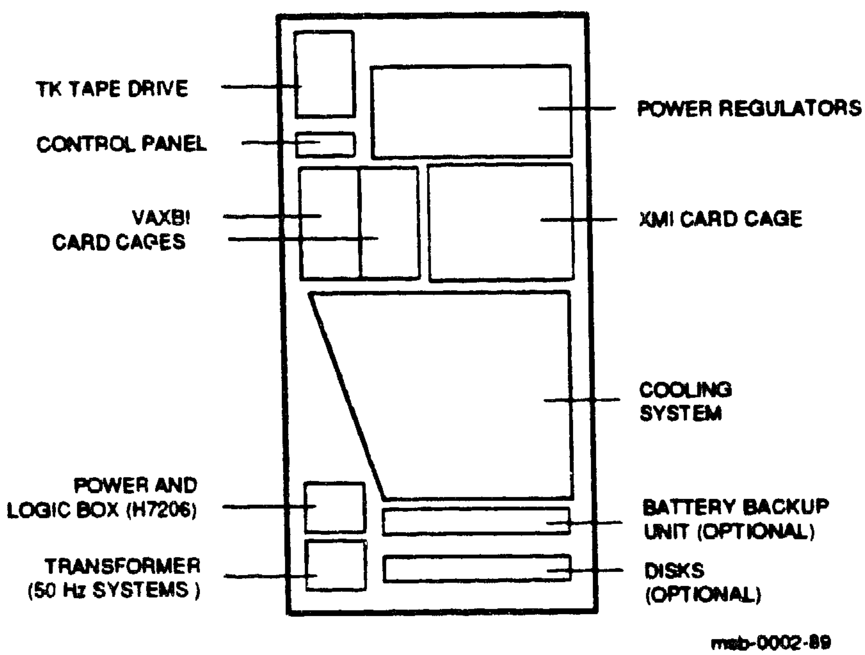
The VAXBI bus, in turn, passes data between the system and the peripheral devices.

[1] The XMI bus has a 64-nanosecond bus cycle, with a maximum throughput of 100 Mbytes per second.

1.3 VAX 6000–400 Front View

The TK tape drive and control panel are on the front of the system cabinet, accessible with the doors closed. With the front door open, field service representatives can access the power regulators, VAXBI and XMI card cages, the cooling system, and, if present, the battery backup unit and disks.

Figure 1–3: VAX 6000–400 System (Front View)



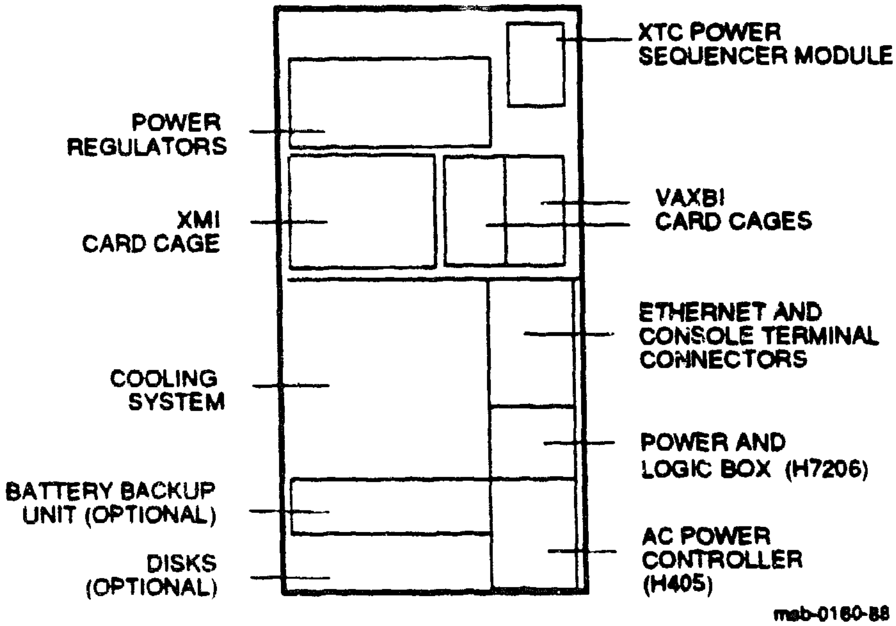
These components are visible from the inside front of the cabinet (see Figure 1–3 for their location):

- TK tape drive
- Control panel
- Power regulators
- Two VAXBI card cages
- XMI card cage
- Cooling system
  One of the two blowers is visible from the front of the cabinet.
- Power and logic box (H7206)
- Battery backup unit and disks (optional)
- Transformer (on 50 Hz systems only)

1.4 VAX 6000–400 Rear View

With the rear door open, field service representatives can access the power sequencer module (XTC); the power regulators; the I/O bulkhead space behind the card cages; Ethernet and console terminal connectors; cooling system; power and logic box; battery backup unit and disks, if present; and the AC power controller.

Figure 1–4: VAX 6000–400 System (Rear View)



These components are visible from the rear of the cabinet (see Figure 1–4):

- Power sequencer module (XTC) located on the back of the TK tape drive and control panel unit
- Five field-replaceable power regulators
- I/O bulkhead space
  The panel covering the XMI and VAXBI areas is the I/O bulkhead panel and provides space for additional I/O connections.
- VAXBI and XMI adapter bulkhead cables
- Ethernet and console terminal connectors
- Cooling system, with open grid over a blower
- Power and logic box (H7206)
- Battery backup unit and disks (optional)
- AC power controller (H405)

1.5 Field-Replaceable Units

Table 1-2 lists the major recommended spares and their part numbers for the VAX 6000-400. SD indicates whether the part is in the field service kit.

Table 1-2: Field-Replaceable Units

	Part Number	SD Kit	Description
Processors:	T2015	Y [1]	CPU module (KA64A)
	T2017	Y	Vector module (FV64A)
Adapters:	T1043	Y	VAXBI adapter (DWMBA/B)
	T2012	Y	VAXBI adapter (DWMBA/A)
Memory:	T2014-B	Y	32 Mbyte memory (MS62A)
VAXBI Card Cage:	H9400-AA	N	VAXBI card cage
XMI Card Cage:	70-24373-01	N	XMI 14-slot card cage
	54-18172-01	Y	XMI daughter card
System Control Assembly:	54-16574-01	Y	Control panel assembly
	54-17243-01 or 20-29176-01	Y	XTC power sequencer
	TK70	Y	Tape drive
	12-19245-02	N	TOY clock battery
Power Supply:	H7214	Y	5 V regulator
	H7215	Y	5 V regulator
	H7206	Y	Power and logic box
	H405E	N	60 Hz AC power controller
	H405F	N	50 Hz AC power controller
Battery Backup:	H7231-N	N	250 W battery backup option

[1]The processor module is in a separate SD kit. The common SD kit contains all indicated parts except the processor module.

Table 1–2 (Cont.): Field-Replaceable Units

	Part Number	SD Kit	Description
Miscellaneous:	12-11255-24	N	Air filter, front
	12-11255-17	N	Air filter, rear
	12-27848-01	N	Blower assembly
	12-24701-06	N	H7206 fan
	17-01844-01	N	Temperature sensor
	12-25024-11	N	Airflow sensor
	16-28393-01	N	Transformer

CHAPTER 2

Chapter 2
Diagnostics

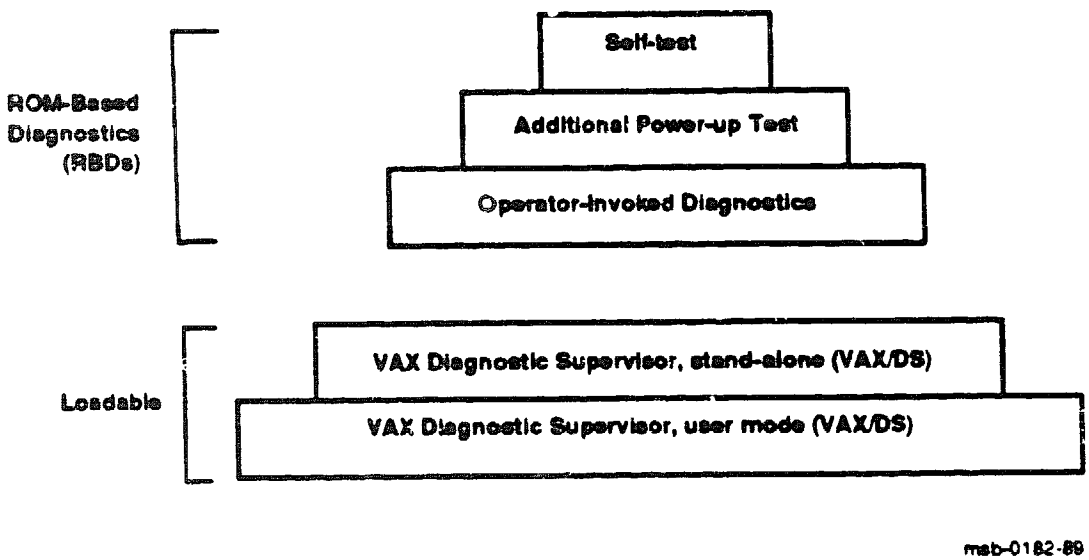
This chapter discusses the design of the VAX 6000–400 diagnostics, the self-test, ROM-based diagnostic monitor program, ROM-based diagnostics for VAXBI devices, and VAX diagnostic supervisor tests. Sections include:

- Diagnostic Overview
- Self-Test
- ROM-Based Diagnostic Monitor Program
    - RBD Monitor Control Characters
    - START Command
    - START Command Qualifiers
    - RBD Test Printout, Passing
    - RBD Test Printout, Failing
    - SUMMARY Command
    - Sample RBD Session
    - Running ROM-Based Diagnostics on VAXBI Devices
- VAX Diagnostic Supervisor Programs
    - Running VAX/DS
    - Sample VAX/DS Session
    - VAX/DS Diagnostics

2.1 Diagnostic Overview

The KA64A system is tested with two types of diagnostics: ROM-based and loadable. The ROM-based diagnostics (RBD) include self-tests, additional power-up tests, and callable diagnostics (from the RBD monitor). The loadable diagnostics run under the VAX Diagnostic Supervisor (VAX/DS) in stand-alone mode or user mode (see Figure 2-1).

Figure 2-1: Diagnostics Design



Self-Tests
Each module on the XMI and VAXBI buses has its own self-test resident in ROM, except for the DWMBA modules. At power-up, initialization, booting, or system reset, each module runs its own self-test. The processor self-test completes within 10 seconds. The memory test completes in less than 60 seconds.

Other Power-Up Tests
Following the modules' self-tests, two additional tests are run and reported in the self-test display: CPU/memory interaction tests and DWMBA tests.

All CPUs that have passed self-test run the CPU/memory interaction test. The CPU/memory interaction test checks that the processors can access memory. Memory also has a self-test that tests actual memory locations. The CPU/memory interaction test is the second test for memory and serves as a check on the memory's XMI interface and on some CPU logic that can be tested only by accessing memory. Results are printed on the ETF line of the self-test display. (See Chapter 6 of the *VAX 6000–400 Owner's Manual* for an explanation of self-test results.)

The DWMBA modules are tested by the boot processor before it queries the VAXBI options for the results of their self-tests. Results from both tests are printed in the XBI lines on the self-test printout (see Example 2–1).

Operator-Invoked ROM-Based Diagnostics
From the console prompt, you can enter RBD mode and run any of four ROM-based diagnostics. These four diagnostics are the KA64A self-tests, CPU/memory interaction tests, DWMBA tests, and memory tests. In RBD mode, you have the capability of running tests other than those in the default suite, running multiple passes of tests, and receiving an error report with information about any failing tests.

VAX Diagnostic Supervisor (VAX/DS)
From the console prompt, you can boot VAX/DS from the TK tape, or other media and run stand-alone VAX/DS level 3 diagnostics (stand-alone mode). From your operating system, run VAX/DS and run level 2R diagnostics (user mode). Level 2 VAX/DS diagnostics may be run either in stand-alone or user mode. See Table 2–8 for a listing of VAX/DS diagnostics.

2.2 Self-Test

The self-test diagnostics reside in ROM on the processors and on-board some other modules. These diagnostics check each module at power-up, when the system is reset, and during booting. Self-test results are written to the console terminal, as shown in Example 2–1.

Example 2–1: Sample Self-Test Results

```
#123456789 0123456789 0123456789 01234567#

F   E   D   C   B   A   9   8   7   6   5   4   3   2   1   0   NODE #

    A   A   .   .   M   M   M   M   P   P   P   P   P   P       TYP
    o   c   .   .   +   +   +   +   +   +   +   +   +   +       STF     ❶
    .   .   .   .   .   .   .   .   E   E   E   E   D   B       BPD
        .   .       .   .   .   .   +   +   +   +   +   +       ETF     ❷
    .   .       .   .   .   .   .   E   E   E   E   D   B       BPD

.   .   .   .   .   .   .   .   .   +   +   .   +   .   +   .   XBI D + ❸
.   .   .   .   .   .       .   .   +   +   .   .   .   +   .   XBI E +

    .   .   .   .   A4  A3  A2  A1  .   .   .   .   .   .       ILV
    .   .   .   .   32  32  32  32  .   .   .   .   .   .       128Mb

ROM0 = V1.00  ROM1 = V1.00  EEPROM = 1.00/1.00   SN = SG01234567

>>>
```

The callouts in Example 2–1 refer to Table 2–1.

Self-test is invoked and results are written to the console under several circumstances:

- At power-up
- When the control panel Restart button is pressed
- During boot procedure
- In console mode, with the systemwide INITIALIZE command

The first line of the self-test printout is the progress trace. This line indicates that the KA64A at node 1 is functioning during self-test.

The remainder of the printout is the self-test display. Table 2–1 describes the tests run during self-test. The callouts in Table 2–1 refer to Example 2–1 .

Table 2–1: Self-Test Components

Test	Description
KA64A	Each processor runs its own self-test resident in its own ROM. A plus sign (+) on line STF ❶ means the processor passed. Each processor also tests interaction with memory. A plus sign on line ETF ❷ means the test passed.
MS62A	Each memory runs its own self-test resident in its sequencer. A plus sign on line STF ❶ means the memory passed.
DWMBA	The XMI-to-VAXBI adapter is tested by the boot processor. A plus sign at the right of the XBI line ❸ means both the DWMBA/A and DWMBA/B passed.
VAXBI	Each VAXBI bus on the system is checked, and each VAXBI node runs its own self-test. A plus sign in column 0 through F of the XBI line ❸ means the VAXBI node passed.

The self-test printout in Example 2–1 reflects a specific configuration. A detailed explanation of self-test results is available by typing HELP SELF at the console prompt. Self-test is also described in Chapter 6 of the *VAX 6000–400 Owner's Manual*.

The tests run during self-test can be individually invoked in RBD mode using the ROM-based diagnostics monitor program. Here you can examine each test more closely and determine which test is failing.

2.3 ROM-Based Diagnostic Monitor Program

The ROM-Based Diagnostic Monitor program is accessed through the console program. Type T/R at the console prompt to enter RBD mode. RBD mode has three commands with qualifiers and a set of control characters that run the RBD tests.

Table 2–2: RBD Monitor Commands

Command	Function
ST[ART]*n*	Starts RBD *n*, where *n* is the number of the RBD program listed in Table 2–3
SU[MMARY]	Prints a summary report of the last RBD program run
QU[IT]	Exits the RBD monitor and returns control to the console program

Table 2–3: ROM-Based Diagnostic Programs

RBD Program	Test Totals	Default (Power-Up)	Default (Callable)	Description
0	37	37	37	Runs CPU tests
	49	49	49	Runs scalar and vector tests
1	13	12	13	Runs CPU/memory interaction tests
	17	16	17	Runs scalar/vector CPU/memory interaction tests
2	26	20	20	Runs DWMBA tests
3	12	0	7	Sizes and runs additional tests on main memory

To enter the RBD monitor, at the console prompt type:

```
>>>  T/R                ! This is the abbreviation for TEST/RBD.
                        !
RBDn>                   ! RBD prompt appears signifying entrance into
                        ! RBD mode, where n is the XMI node number of
                        ! the processor running the RBD monitor program.
```

The RBD commands are explained here and in Sections 2.3.2 and 2.3.6. Table 2–2 gives the commands, their abbreviations, and functions.

Four programs run from the ROM-based diagnostics (RBD) monitor program. The programs are CPU self-test, CPU/memory interaction tests, the DWMBA tests, and memory RBD tests. Each of these programs has several tests, as shown in Table 2–3. The RBDs are designed for use by Digital customer service personnel.

Each RBD has a default number of tests that run at power-up, and another default number of tests that run when the program is called from the RBD monitor (see Table 2–3). The CPU diagnostic (RBD 0) runs all its tests in both modes. The power-up default for the CPU/memory interaction diagnostic (RBD 1) is 12 (scalar only—16 with the vector tests), and the callable default is all tests. The DWMBA diagnostic (RBD 2) runs 20 of the 26 tests available as the default in both modes; tests 2, 3, 4, 10, 11, and 26 must be specifically invoked by qualifier in callable mode. RBD 3, the Memory diagnostic, does not run on power-up. In callable mode, 7 of 12 tests run when invoked; tests 2 through 8 are defaults. To run tests other than the default suite from the RBD monitor, issue a command such as the following, which invokes all DWMBA tests:

```
RBDn> ST2/T=1:26 D
```

It is helpful to use the trace qualifier, /TR, with the RBD START command. (See Section 2.3.3.) This qualifier shows each individual test as it is run. If a test fails, the program displays error messages. By default, the RBDs continue testing after an error is encountered. Adding the halt-on-error qualifier, /HE, causes the program to halt when the first error is encountered. Testing can be aborted at any time by typing CTRL/C.

To exit RBD mode, type QUIT at the RBD prompt. Your next prompt is from console mode.

2.3.1 RBD Monitor Control Characters

Several control characters are supported by the RBD monitor program. These characters manage the program process as shown in Table 2–4.

Table 2–4: RBD Monitor Control Characters

Character	Environment	Function
CTRL/C	Test running	Stops the execution of an RBD test and executes cleanup code.
DELETE	RBD command line	Use for deleting erroneous characters entered on the command line.
CTRL/Q	Test running	Resumes output to terminal that was suspended with CTRL/S.
CTRL/R	At RBD prompt	Refreshes the command line; useful when characters are deleted.
CTRL/S	Test running	Suspends output to the terminal until CTRL/Q is typed.
CTRL/U	At RBD prompt	Disregards previous input.
CTRL/Y	Test running	Stops the execution of an RBD test and does not execute any cleanup code.
CTRL/Z	At RBD prompt	Exits RBD monitor program and enters console program; same effect as the QUIT command.

When CTRL/C is entered from the console terminal that began execution of the RBD test, the diagnostic stops execution, runs cleanup code, and returns control to the RBD monitor program. This happens immediately when running RBD 0, RBD 1, or RBD 2; there may be a wait of up to one minute for a response when RBD 3 is running. If CTRL/C is typed at the RBD monitor prompt, it has the same effect as CTRL/U.

When you use the DELETE key (or rubout key), characters being deleted are preceded by a backslash (\ ) and print as they are rubbed out. When the next valid character is typed, it is preceded by a backslash (\ ) to delineate the deleted characters. You can use CTRL/R to refresh the line.

When the RBD monitor program receives a CTRL/U, the program disregards all previous input typed and returns the RBD prompt. If a test is running when CTRL/U is entered, CTRL/U is ignored.

When a CTRL/Y is received by the RBD monitor program from the console terminal that began execution of the RBD test, the diagnostic stops execution and returns control to the RBD monitor program. No cleanup code is run, and the unit under test is left in an indeterminate state. A CTRL/Y entered at the RBD monitor prompt has the same effect as CTRL/U.

When the RBD monitor program receives a CTRL/Z, the program exits and control is returned to the console program. The next prompt is the console prompt. CTRL/Z has the same effect as the QUIT command. If CTRL/Z is entered while an RBD test is running, CTRL/Z has the same effect as CTRL/C: it halts the test and executes cleanup code.

2.3.2 START Command

The RBD monitor START command invokes a specific RBD program. It takes an argument indicating the RBD program to be run, and can take any of 13 qualifiers.

Example 2-2: START Command

```
>>> T/R                         ! Command to enter RBD monitor program.

RBD3>                           ! RBD monitor prompt, where 3 is the hexa-
                                ! decimal node number of the processor
                                ! that is currently receiving your input.

RBD3> ST2/TR E                  ! Runs the default XBI tests, testing the
                                ! DWMBA at XMI node number E. Test results
                                ! are written to the console terminal.

RBD3> ST1/HE/IE/BE              ! Runs the CPU/memory interaction RBD, halting
                                ! on the first error encountered, inhibiting
                                ! error output, ringing the bell when the
                                ! first error is encountered.
```

The START command syntax is:

`STn[/qualifier] [parameter]`

where:

- *n* is the RBD to be run (see Table 2-3).
- [/qualifier] is one of those listed in Section 2.3.3.
- [parameter] is a program-specific value used in RBD 2 or RBD 3. (For the meaning of this parameter in RBD 2, see Section 6.4, and in RBD 3, see Section 5.10.)

2.3.3 START Command Qualifiers

The START command is the primary RBD program command. Its qualifiers act as switches, allowing you to control the output of the tests—to run portions of a test, to run nondefault tests, and to loop on tests.

Table 2–5: START Command Qualifiers

Qualifier	Default	Function
/BE	Disabled	Bell sounds when an error is encountered
/C	Disabled	Destructive test confirmation
/DS	Disabled	Disable status reports
/HE	Disabled	Halt on the test that incurs a hard error
/HS	Disabled	Halt on the test that incurs a soft error
/IE	Disabled	Inhibit all error output
/IS	Disabled	Inhibit summary reports
/LE	Disabled	Loop on the test that incurs a hard error
/LS	Disabled	Loop on the test that incurs a soft error
/P=*n*	Enabled	Make *n* passes of the test or tests indicated
/QV	Disabled	Quick verify mode
/T=*n[:m]*	Enabled	/T=*n* runs test *n*; /T=*n:m* runs a range of tests from *n* through *m*
/TR	Disabled	Print a trace of test numbers, as they run

NOTE: *A qualifier is valid only for the command with which it is issued. Qualifiers do not remain in effect for the session once they are issued.*

See Example 2–2 for examples and a description of the START command syntax.

With /BE, the RBD monitor program rings the bell on the console terminal whenever an error is encountered. This is useful when error printout is inhibited and a loop is being performed on an intermittent error (/LE).

/C enables execution of destructive tests. See Example 2–7 and Section 5.10 for information on the destructive tests.

/DS disables printout of the diagnostics test results. The summary report is run, unless it is specifically disabled.

/HE halts on hard error and stops execution of tests as soon as the first hard error is encountered. (In this context, a hard error is defined as a recoverable, repeatable error, for example, a ROM checksum error. This differs from a fatal error, which is an unrecoverable fault, for example, an unexpected interrupt or exception. A fatal error is always cause for program abortion, regardless of the state of the /HE or /LE qualifier.) The test number is printed, and a summary indicating failure of the RBD is printed to the console terminal. Also the RBD monitor prompt is returned. Continue on error is the default condition, so if you want a halt on error, you must specifically invoke it in your command line.

/HS halts on soft error and stops execution of tests as soon as the first soft error is encountered. (In this context, a soft error is defined as a recoverable error that goes away after retry, for example, a corrected read data memory error.) The test number is printed, and a summary indicating failure of the RBD is printed to the console terminal. Also the RBD monitor prompt is returned. Continue on soft error is the default condition, so if you want to halt on soft error, you must specifically invoke it in your command line.

/IE inhibits all error output, suppressing printing of RBD results. This qualifier is used primarily for module repair, in conjunction with the /LE or /LS qualifier. Errors are counted even when the printing is disabled.

/IS suppresses printout of RBD summary after the end of the last pass performed by the RBD.

/LE loops on the test where the first hard error is detected. Even if the error is intermittent, looping continues on the test indicated. To terminate /LE, enter CTRL/C, CTRL/Z, or CTRL/Y. After entering one of these control characters, a summary report is printed. A fatal error causes the program to abort, regardless of the state of this qualifier.

/LS loops on the test where the first soft error is detected. Even if the error is intermittent, looping continues on the test indicated. To terminate /LS, enter CTRL/C, CTRL/Z, or CTRL/Y. After entering one of these control characters, a summary report is printed.

/P=*n* runs *n* number of passes of the RBD test invoked, where *n* is a decimal number. If *n* is 0, all selected tests run for an infinite number of passes. If the /P qualifier is not used, the program defaults to one pass of the test invoked. When used with the /T=*n:m* qualifier, you run a range of tests. To terminate /P=*n*, enter CTRL/C, CTRL/Z, or CTRL/Y. After entering one of these control characters, a summary reports prints out and the RBD monitor prompt returns.

/QV selects the quick verify version of any selected test that supports this mode.

/T=*n[:m]* selects individual tests (/T=*n*) or a range of tests (/T=*n:m*) where *n* and *m* are decimal numbers. For example, to run tests T0005 through T0008, use /T=5:8. If no /T qualifier is used, the diagnostic runs its default suite of tests.

/TR prints each test number as it is completed. This qualifier allows you to trace the progress of the diagnostic as it runs. Without the /TR qualifier, just the summary line is printed.

Two **parameter fields** can be appended to the START command string to control aspects of the diagnostic that are not covered by the qualifiers. The parameter(s) must be appended after any qualifiers specified and separated from the qualifiers, and from each other if both are entered, by a space. The format of the parameter field is one to 10 hexadecimal characters. The use of a parameter field is implementation specific and is optional.

2.3.4 RBD Test Printout, Passing

The RBD printout results are different when the RBD tests pass and when they fail. Example 2–3 shows a passing printout, and Example 2–4 is a sample failure printout.

Example 2–3: RBD Test Printout, Passing

```
>>> T/R                          ! Command to enter RBD monitor program at
                                 ! console prompt.
RBD3>                            ! RBD monitor prompt, where 3 is the hexa-
                                 ! decimal node number of the processor
                                 ! that is currently receiving your input.

RBD3> ST2/TR E                   ! Runs the XBI self-test, testing the DWMBA
                                 ! at XMI node number E. Test results
                                 ! written to the console terminal:

, XBI_TEST❶              1.00❷

, T0001  T0005  T0006  T0007  T0008  T0009  T0012  T0013  T0014  T0015
, T0016  T0017  T0018  T0019  T0020  T0021  T0022  T0023  T0024  T0025❸

;         P❹       3❺    8082❻       1❼
; 00000000 00000000 00000000 00000000 00000000 00000000 00000000❽


RBD3> QU❾                        ! RBD prompt returns; test ran successfully.
                                 ! Exit RBD program.
>>>
```

The callouts in Example 2–3 are explained below.

❶ This entry designates which test is being run. Here it is the XBI_TEST, the self-test for the DWMBA.

XRP_ST indicates RBD 0, the CPU tests
CPUMEM indicates RBD 1, the CPU/memory interaction tests
XBI_TEST indicates RBD 2, the DWMBA tests
XMA_RBD indicates RBD 3, the Memory tests

❷ This field lists the revision number of the RBD program.

❸ These T00*nn* fields appear only with the /TR qualifier; each entry corresponds to a test being run and prints out as the test starts running. In a passing RBD, the final T00*nn* number corresponds to the last test run.

Note that T0002 through T0004 and T0010, T0011, and T0026 are not executed. These tests are not part of the default selection and must be individually invoked by qualifier. For a list of the tests for each RBD and the definition of the tests, see the chapter for each module in this manual.

❹ This field indicates whether the RBD passed or failed; P for passed, F for failed.

❺ This field is the XMI node number of the boot processor executing the RBD. It matches the number in your RBD prompt.

❻ This field is always 8082—the device type of the boot processor.

❼ This field displays the total number of passes (in decimal) executed by the RBD. The default number of passes is 1. If you use the START command with the qualifier /P=5, for example, then this field will show 5, indicating 5 passes were completed.

❽ This line contains the summary of the RBD failures. In a successful RBD run, the line will contain all zeros as shown here. Currently only the second and third fields are used. The second field contains the number of hard errors detected during the run. The third field contains the number of soft errors detected during the run.

❾ The console prompt is usually returned in response to the RBD QUIT command, as shown in this example. However, when some tests are run, the response to QUIT is a system reset. Self-test is then run, and the self-test results are printed. The tests that cause a system reset are: Test 1 of RBD 1; Tests 2, 3, 4, 10, and 11 of RBD 2; and Tests 4 and 8 of RBD 3.

2.3.5 RBD Test Printout, Failing

The RBD printout results are different when the RBD passes and when it fails. Example 2–4 is a sample failure printout, and Example 2–3 shows a passing printout.

Example 2–4: RBD Test Printout, Failing

```
>>> T/R                              ! Command to enter RBD monitor program at
                                     ! console prompt.
RBD2>                                ! RBD monitor prompt, where 2 is the hexa-
                                     ! decimal node number of the processor
                                     ! that is currently receiving your input.
RBD2> ST0/TR                         ! Execute RBD 0 (CPU test) and trace results.

; XRP_ST        1.00

; T0001  T0002  T0003  T0004  T0005  T0006  T0007  T0008  T0009  T0010
; T0011  T0012  T0013  T0014  T0015  T0016  T0017  T0018❶

;        F❷        2❸      8082❹        1❺
;       HE❻    REX520❼       XX❽    T0018❾
;       10❿ AAAAAAAA⓫ A8AAAAAA⓬ 00000000⓭ 000004AC⓮ 2006451F⓯ 01⓰
; T0019  T0020  T0021  T0022  T0023  T0024  T0025  T0026  T0027  T0028
; T0029  T0030  T0031  T0032  T0033  T0034  T0035  T0036  T0037⓱

;        F         2       8082         1⓲
; 00000000 00000001⓳ 00000000 00000000 00000000 00000000 00000000

RBD2>                                ! RBD prompt returns; test completed.
RBD2> QUIT                           ! Exit RBD program.
>>>                                  ! Console prompt reappears.
```

The callouts in Example 2–4 are explained below. (See also Example 2–3 for explanation of other fields of the printout.)

❶ These T00*nn* fields appear only with the /TR qualifier; each entry corresponds to a test being run. The entry prints out as the test starts running. This T00*nn* number is the number of the failing test and is followed by a failure report. In this example, test 18 failed. The /HE qualifier was not used, so testing continues.

❷ F indicates failure of the previous test listed, test 18.

❸ This field is the XMI node number of the boot processor executing the RBD. It matches the number in your RBD prompt.

❹ This field is always 8082—the device type of the boot processor.

❺ This field displays the total number of passes (in decimal) executed by the RBD. The default number of passes is 1.

❻ The class of error is displayed here. *HE* indicates that the error was a hard error. *SE* means the error was a soft error, and *FE* indicates a fatal error. (See Section 2.3.3 for a definition of these errors.)

❼ This field describes the failing logic. Here, the processor chip is the failing logic.

❽ This field is the unit number used in memory and DWMBA tests.

❾ This field lists the number of the test that failed; test 18 failed here.

❿ This is a two-digit (decimal) generic error code.

⓫ The expected data is listed here. AAAAAAAA is the data test 18 expected.

⓬ The received data is listed here. A8AAAAAA is the data test 18 received.

⓭ This field shows any unexpected interrupt vectors.

⓮ This is the address in memory where the referenced error is found.

⓯ This is the address of the failing PC at the time of error.

⓰ This is the error number within the failing test. In this example, the failure was detected at the first possible failure point in T0018. This is a decimal field.

⓱ This final T00*nn* number corresponds to the last test run.

⓲ This entire line is the summary line, and a repeat of the failure summary. It lists the pass/fail code (P or F), the node number and device type number of the boot processor executing the RBD, and the number of passes of the RBD.

⓳ This is the number of hard errors detected.

2.3.6 SUMMARY Command

The RBD monitor SUMMARY command displays a summary of the last diagnostic run.

Example 2–5: SUMMARY Command

```
>>> T/R                              ! Command to enter RBD monitor program
RBD1> ST0/IE/IS/P=100                ! Execute RBD 0 (CPU test), inhibiting
                                     ! error outputs and summary report.
; XRP_ST      1.00

RBD1> SU                             ! Request a summary.

; XRP_ST      1.00

;          P❶        1❷     8082❸      100❹
; 00000000 00000000 00000000 00000000 00000000 00000000 00000000❺

RBD1>
```

The callouts in Example 2–5 are explained below.

❶ This field indicates whether the RBD passed or failed; P for passed, F for failed.

❷ This field is the XMI node number of the boot processor executing the RBD. It will match the number in your RBD prompt, which also indicates the node number of your boot processor.

❸ This field is the device type number of the boot processor executing the RBD.

❹ This field displays the total number of passes executed by the RBD.

❺ This line contains the summary of the RBD failures. Presently only the second and third fields are used. The second field contains the number of hard errors detected during the run. The third field contains the number of soft errors detected during the run.

2.3.7 Sample RBD Session

Examples 2-6 and 2-7 show a sample RBD session.

Example 2-6: Sample RBD Session, Part 1 of 2

```
>>>  T/R❶
RBD1> ST0/TR❷

;XRP_ST         1.00

; T0001  T0002  T0003  T0004  T0005  T0006  T0007  T0008  T0009  T0010
; T0011  T0012  T0013  T0014  T0015  T0016  T0017  T0018  T0019  T0020
; T0021  T0022  T0023  T0024  T0025  T0026  T0027  T0028  T0029  T0030
; T0031  T0032  T0033  T0034  T0035  T0036  T0037

;        P         1     8082         1
;00000000 00000000 00000000 00000000 000000000 00000000 00000000

RBD1> ST1/TR/HE❸

;CPUMEM         1.00

; T0001  T0002  T0003  T0004  T0005  T0006  T0007  T0008  T0009  T0010
; T0011  T0012  T0013

;        P         1     8082         1
;00000000 00000000 00000000 00000000 000000000 00000000 00000000

RBD1> ST2 5❹

;XBI_TEST      1.00

;        F         1     8082         1
;       FE  No_Unit        05     T0000
;       00 00000000 00000000 00000000 00000000 200705E7 01

;        F         1     8082         1
;00000000 00000001 00000000 00000000 00000000 00000000 00000000

RBD1>  ST2/TR/T=2:4/P=3 E❺

;XBI_TEST      1.00

; T0002  T0003  T0004  T0002  T0003  T0004  T0002  T0003  T0004

;        P         1     8082         3
;00000000 00000000 00000000 00000000 000000000 00000000 00000000
```

❶ Enter RBD mode from console mode. The RBD prompt appears and indicates you are operating from the boot processor at node 1.

❷ Run RBD 0 and trace the tests. The CPU test runs all 37 tests successfully.

❸ Run RBD 1, trace it and halt on the first error found. All CPU/memory interaction RBD tests run and pass.

❹ Run RBD 2, testing the DWMBA at XMI node 5. The value NO_UNIT on the third line of output indicates that the node value of node 5 is not correct; no DWMBA was found at this node.

❺ Run RBD 2, testing the DWMBA at XMI node E; trace the tests as they run, and run tests 2 through 4 of RBD 2; make 3 passes over these selected tests.

Note that the T00*nn* line lists each of the three tests three times, since the /P=3 called for 3 passes of the tests. And the final parameter in the summary line is a 3, indicating that 3 passes completed.

Example 2-7: Sample RBD Session, Part 2 of 2

```
RBD1> ST3/TR/T=1 ❻

RBD1> ST3/TR/T=1

RBD1> ..3/TR/T=1 /C ❼

;XMA_RBD      1.00

; T0001

;        P        1      8082        1
;00000000 00000000 00000000 00000000 000000000 00000000 00000000

RBD1> QU ❽

         [self-test results may be displayed here]

>>> SET CPU 2 ❾
>>> T/R

RBD2> ST0/TR ❿

;XRP_ST       1.00

; T0001  T0002  T0003  T0004  T0005  T0006  T0007  T0008  T0009  T0010
; T0011  T0012  T0013  T0014  T0015  T0016  T0017  T0018  T0019  T0020
; T0021  T0022  T0023  T0024  T0025  T0026  T0027  T0028  T0029  T0030
; T0031  T0032  T0033  T0034  T0035  T0036  T0037

;        P        2      8082        1
;00000000 00000000 00000000 00000000 000000000 00000000 00000000
```

6. Run RBD 3, trace it, and run only test 1 of this RBD. This test is one of the memory tests that is not part of the default suite of tests. This test corrupts memory. You must add a /C qualifier to the START command, to indicate that you do indeed intend to run this destructive test.

   The /C qualifier was not given in this example. The command line is echoed, waiting for /C to be typed.

   At this point you can press Return to return to the command prompt (RBD1>), or you can type the /C qualifier followed by Return.

7. Run RBD 3, trace the tests as they run, run only test 1, and /C allows the test to run. In this example, the test completed with no errors.

8. Exit from RBD mode. Enter console mode.

9. Make the next processor the primary processor so that RBD 0 can be run on it.

10. Run RBD 0 and trace the tests. The CPU test runs all 37 tests successfully.

2.3.8 Running ROM-Based Diagnostics on VAXBI Devices

Some VAXBI devices can be tested from the console terminal with their on-board ROM-based diagnostics. The Z console command is used to send commands to these VAXBI nodes.

Example 2–8: VAXBI RBD Session

```
>>> SHOW CONFIGURATION (1)
      Type            Rev
  1+  KA64A   (8082)  0007
  A+  MS62A   (4001)  0002
  D+  DWMBA/A (2001)  0002
  E+  DWMBA/A (2001)  0002

  XBI D
  1+  DWMBA/B (2107)  0007
  5+  DMB32   (0109)  210B
  6+  DEBNI   (0118)  0100

  XBI E
  1+  DWMBA/B (2107)  0007
  4+  KDB50   (010E)  0F1C
  5+  TBK70   (410B)  0307
>>> Z/BI:6 D (2)
?33 Z connection successfully started

t/r (3)

RBD6> ST 0/TR (4)

;Debni_ST     1.02

; T01  T02  T03  T04  T05  T06  T07  T08

;       P         6      0118 00000020
;00000000 00000000 00000000 00000000 00000000 00000000 00000000

;    PUDR: FFFFxxxx

RBD6> QUIT (5)
^P
?31 Z connection terminated by ^P

>>> Z/BI:5 E (6)
?33 Z connection successfully started

t/r

RBD5> ST 0/TR

;T1035_St     1.00
```

Example 2–8 Cont'd. on next page

Example 2–8 (Cont.): VAXBI RBD Session

```
; T01   T02   T03   T04   T05   T06   T07   T08   T09   T10   T11   T12   T13   T14
; T15   T16   T17

;       P        6      410B 00000001
;00000000 00000000 00000000 00000000 00000000 00000000 00000000

;    PUDR: 5FF43FDF

RBD5> QUIT
^P
?31 Z connection terminated by ^P

>>>
```

The callouts in Example 2–8 are explained below.

❶ The SHOW CONFIGURATION console command shows that this system includes a DEBNI at node 6 of the VAXBI attached at XMI node D, and a TBK70 at node 5 of the VAXBI attached at XMI node E. (See *VAX 6000–400 Owner's Manual* for more information on the SHOW CONFIGURATION command.)

❷ The Z command is typed at the console prompt. A connection is established to node 6 (/BI:6) of the VAXBI connected at XMI node D (D). The console returns a message confirming that the connection has been made.

❸ After the console message is returned in ❷, no prompt is printed. Typing `t/r` invokes the RBD monitor on the VAXBI adapter being tested and returns the RBD monitor prompt. Note that the "6" in the RBD prompt refers to the VAXBI node.

❹ The START command for VAXBI RBDs requires a space before the 0. When run with the /TR qualifier, test traces are printed. The last line of the summary report indicates the contents of the Power-Up Diagnostic Register. Refer to the technical manual for the device being tested to interpret the contents reported.

❺ The QUIT command exits the RBD monitor. The Z connection remains until CTRL/P is entered.

❻ Steps ❷ through ❺ are repeated to run the RBD of the TBK70 at node 5 of the VAXBI attached at XMI node E.

2.4 VAX Diagnostic Supervisor Programs

The VAX Diagnostic Supervisor (VAX/DS) is a monitor that controls operation of a diagnostic program. You can use VAX/DS in one of two modes: stand-alone mode (exclusive use of the system) or user mode (under the VMS operating system).

Table 2–6: VAX Diagnostic Program Levels

Level	Type of Test	Run-Time Environment
1	System exercisers	Runs under the VMS operating system without VAX/DS
2R	Function tests of peripheral devices	Runs under the VMS operating system with VAX/DS
2	Exercisers and function tests of peripheral devices and processors	Runs under VAX/DS in user mode and stand-alone mode
3	Function tests and logic tests of peripheral devices and processors	Runs under VAX/DS in stand-alone mode

Table 2–7: VAX/DS Documentation

Document	Order Number
VAX Diagnostic Supervisor User's Guide	AA–FK66A–TE
VAX Diagnostic Software Handbook	AA–F152A–TE
VAX Diagnostic Design Guide	AA–FK67A–TE
VAX Systems Hardware Handbook	EB–31692–46

The VAX Diagnostic Supervisor (VAX/DS) can be run in interactive mode. You type commands in response to the VAX/DS program prompt:

```
DS>
```

VAX/DS lets you load diagnostic programs into system memory, select devices to be tested, and run the programs. The VAX/DS command language also lets you control the execution of diagnostic programs; you can specify which tests or sections of a program should run, and how many passes it should run. You can also show the current state of parameters that affect the operation of diagnostic programs. The programs report their results through VAX/DS to the terminal.

VAX/DS supports three types of diagnostic programs:

- Logic tests
  Test a specific section of a device's logic circuitry. Logic tests provide the greatest degree of detail in determining the location of faulty hardware.
- Function tests
  Test the functions of the device. For example, a function test for a disk drive would test the drive's reading and writing capabilities. Function tests can detect the location of faulty hardware, although the results may be less exact than those of a logic test.
- Exercisers
  Test entire systems or subsystems and verify that a system can function properly over a period of time. Exercisers can detect both hardware faults resulting from the simultaneous use of a system's numerous devices and intermittent faults occurring only once or twice over a long period of time.

Table 2–8 lists the VAX/DS programs available for the VAX 6000–400 system. Each program has a HELP file available. To access the help files for any diagnostic, at the VAX/DS prompt, type:

```
DS>   HELP [VAX/DS diagnostic program name]
```

2.4.1 Running VAX/DS

You can use VAX/DS in one of two modes: stand-alone mode (exclusive use of the system) or user mode (under VMS).

Example 2-9: Running Stand-Alone VAX/DS

```
>>> BOOT/R5:10 CSA1              ! Enter BOOT command designating the
                                 ! TK tape drive as input device; /R5:10
                                 ! is the boot flag indicating the
                                 ! VAX/DS program.
                [self-test results print]
Loading system software.
                    VAX DIAGNOSTIC SOFTWARE
                         PROPERTY OF
                 DIGITAL EQUIPMENT CORPORATION
              ***CONFIDENTIAL AND PROPRIETARY***

Use Authorized Only Pursuant to a Valid Right-to-Use License
Copyright, Digital Equipment Corporation, 1989.  All Rights Reserved.

DIAGNOSTIC SUPERVISOR. ZZ-ERSAA-11.XX-NNN  31-DEC-1989 12:01:45
DS>                              ! System boots VAX/DS and displays banner.
                                 ! Run VAX/DS level 3 or 2 programs.
DS> ^P                           ! Enter CTRL/P to exit VAX/DS
?02 External halt (CTRL/P, break, or external halt)
    PC  = 00027056
    PSL = 00000200
    KSP = 0004D210

>>>                              ! Console prompt returns.
```

Example 2-10: Running VAX/DS in User Mode

```
$                                   ! At the operating system prompt, run
$ RUN ERSAA                         ! the VAX/DS program.
          [VAX/DS banner prints, as in example above]
DS>                                 ! VAX/DS prompt appears.
                                    ! Run VAX/DS level 2R or 2 programs.
DS> EXIT                            ! Type EXIT to exit VAX/DS
$                                   ! Operating system prompt returns.
```

Table 2–6 describes the levels of VAX/DS programs. Check Table 2–8 for the programs you wish to run, and determine if you will run VAX/DS in stand-alone or user mode.

To run VAX/DS in stand-alone mode, insert a TK tape containing the VAX 6000–400 VAX/DS program into the TK tape drive on the system.[1] At the console prompt, boot VAX/DS from the TK tape using the /R5:10 qualifier:

```
>>> BOOT /R5:10 CSA1
```

where CSA1 is the device name for the TK tape drive, and /R5:10 is the boot flag designating the VAX/DS program (see Example 2–9). To run VAX/DS in user mode under VMS, you use the RUN command under your operating system (see Example 2–10).

In both stand-alone and user mode, VAX/DS functions the same way. Typically a program running in user mode provides less detailed results than one running in stand-alone mode. For more information on VAX/DS, see the documents listed in Table 2–7.

[1] The VAX 6000–400 Console TK50 tape (part number AQ–FK87A–ME) ships with every system and contains VAX/DS and the autosizer. Digital customer service representatives and licensed self-maintenance customers may use the VAX 6000–400 COMPL DIAG SET TK50 tape (part number AQ–PBPRA–DE) that contains VAX/DS, the autosizer, and a complete set of diagnostics. The nonbootable VAX 6000–400 COMPL DIAG SET 16MT9 tape (part number BB–PBPSA–DE) is also available to customer service and self-maintenance customers for use on a TU81 tape drive.

2.4.2 Sample VAX/DS Session

When you run the VAX/DS programs, run the system autosizer program EVSBA first. This program, which takes several minutes to execute, will save you time as you proceed with other tests. Certain conditions cause the generation of an unexpected trap or interrupt. Use the method shown to avoid these conditions.

Example 2-11: Sample VAX/DS Session, Part 1 of 3

```
>>> SET BOOT DIAG /XMI:E/BI:5/R5:10  DUA0

>>> BOOT DIAG ①

            [self-test results print]

Loading system software.

                    VAX DIAGNOSTIC SOFTWARE
                         PROPERTY OF
                 DIGITAL EQUIPMENT CORPORATION
              ***CONFIDENTIAL AND PROPRIETARY***

Use Authorized Only Pursuant to a Valid Right-to-Use License
Copyright, Digital Equipment Corporation, 1989.  All Rights Reserved.

DIAGNOSTIC SUPERVISOR. ZZ-DS> RUN EVSBA ②

.. Program: EVSBA - AUTOSIZER   level 3   X6.6, revision 6.6, 3 tests,
   at 17:52:20.21.

.. End of run, 0 errors detected, pass count is 1,
   time is 31-DEC-1989 17:55:07.02
```

❶ The SET BOOT command stores a nickname for a set of parameters to the BOOT command. (The lower key switch on the control panel must be set to Update when this command is issued.) This BOOT command loads VAX/DS from disk. Alternatively, you can use the command BOOT/R5:10 CSA1, which loads VAX/DS (/R5:10) as stand-alone from the system TK tape drive (CSA1). For more information on the BOOT and SET BOOT commands, see the *VAX 6000–400 Owner's Manual*.

❷ The off-line autosizer program EVSBA identifies hardware on your system and builds a database for the VAX Diagnostic Supervisor. The autosizer eliminates the need for you to type in the name and characteristics of the hardware you intend to test under VAX/DS with level 3 diagnostic programs.

Example 2-12: Sample VAX/DS Session, Part 2 of 3

```
DS> SHOW DEV❸

_DWMBA1 DWMBA    HUB      61F00000  XMI node # (1,2,3,4,B,C,D,E) =0000000E(X)
BI Node Number  (HEX)=00000001(X)
_DUA     KDB50    _DWMBA1 7C008000  BI Node Number  (HEX)=00000004(X)
_DJA23   RA60     _DUA     7C500000
_KA0     KA64A    HUB      61880000  XMI Node ID=00000001(X)
_KA1     KA64A    HUB      61900000  XMI Node ID=00000002(X)
_DWMBA0 DWMBA    HUB      61E80000  XMI node # (1,2,3,4,B,C,D,E) =0000000D(X)
BI Node Number  (HEX)=00000001(X)
_TXA     DMB32    _DWMBA0 7A00A000  BI Node Number  (HEX)=00000005(X)
_ETA0    DEBNI    _DWMBA0 7A00C000  BI Node Number  (HEX)=00000006(X)
_DUA2    RA82     _DUA     7C500000
_DUA61   RA82     _DUA     7C500000
_MUA     TBK70    _DWMBA1 7C00C000  BI Node Number  (HEX)=00000006(X)
_MUA0    TK70     _MUA     7C580000

DS> SELECT ALL❹
DS> SET TRACE
DS> SET EVENT 2
DS> RUN ERKMP

.. Program: ERKMP - KA64A MP Exerciser, revision 1.0, 10 tests,
   at 18:11:41.25.
Testing:  _KA0 _KA1

                  Booting Secondary Processor #02

Test 1: Memory Interlock Test
Test 2: Interprocessor Interrupt Test
Test 3: Write Error Interrupt Test
Test 4: Cache Invalidate Test
Test 5: XMI Bus Arbitration Test
Test 6: XMI Bus Arbitration Collision Test
Test 7: XMI Lockout Test
Test 8: Cache Coherency Test
Test 9: XMI Suppress Assertion Test
Test 10: Multiprocessor Exerciser
 .. End of run, 0 errors detected, pass count is 1,
    time is 31-DEC-1989 18:16:24.49

DS> ^P❺
?02 External halt (CTRL/P, break, or external halt)
    PC  = 00027056
    PSL = 00000200
    KSP = 0004D210
```

③ You can use the autosizer to print a list of system hardware by running the program EVSBA under VAX/DS and typing the VAX/DS command SHOW DEVICE/BRIEF. The command lists system devices, similar to the SHOW CONFIGURATION command in console mode.

④ Preparing to run a diagnostic, SELECT ALL selects all devices listed in ③. SET TRACE enables printing of test numbers and names when the diagnostic runs. If you run another diagnostic after this one and you want the tests traced, you will need to issue the SET TRACE command again. The SET EVENT 2 command disables some informational messages printed by this diagnostic.

⑤ An external halt causes VAX/DS to print the contents of the program counter, the processor status longword, and the stack pointer. Since VAX/DS was called from console mode, the console prompt is returned.

In a VAX 6000–400 system an external halt can, in some cases, cause an unexpected trap or interrupt through SCB vector 60. The remainder of this example shows how to avoid this condition by using the CLEAR EXCEPTION command and what happens if the condition is not cleared by the console.

Example 2-13: Sample VAX/DS Session, Part 3 of 3

```
>>> CLEAR EXCEPTION 6
XBER   = 00000041
XFADR  = 61880008
RCSR   = 01240001

>>> SHOW CONFIGURATION 7
       Type              Rev
  1+   KA64A    (8082)  0007
  3+   KA64A    (8082)  0007
  A+   MS62A    (4001)  0002
  B+   MS62A    (4001)  0002
  D+   DWMBA/A  (2001)  0002
  E+   DWMBA/A  (2001)  0002

  XBI D
  1+   DWMBA/B  (2107)  0007
  2+   CIBCA    (0108)  41C1
  5+   DMB32    (0109)  210B
  6+   DEBNI    (0118)  0100

  XBI E
  1+   DWMBA/B  (2107)  0007
  4+   KDB50    (010E)  0F1C
  6+   TBK70    (410B)  0307

>>> CLEAR EXCEPTION 8
XBER   = 8001B041
XFADR  = 61900000
RCSR   = 012C0011

>>> CONTINUE
DS> ^P 9
?02 External halt (CTRL/P, break, or external halt)
    PC  = 0002704A
    PSL = 00000204
    KSP = 0004D210

>>> SHOW CONFIGURATION
    .
    .
    .

>>> CONTINUE
?? Unexpected trap or interrupt thru SCB vector 0060
PC at error:            0002704A(X)
PSL at error:           00000004(X)   ; CUR=KERNEL,PRV=KERNEL,IPL=00(X),Z
User return PC:         none found!
DS> CONTINUE
.. Continuing from 0002704A

DS>
```

⑥ The CLEAR EXCEPTION command prints the contents of three registers (XBER, XFADR, and RCSR) and then clears their error bits, if set. No error bits have been set at this point.

⑦ The SHOW CONFIGURATION command attempts to examine unused address space, creating errors.

⑧ Issuing the CLEAR EXCEPTION command again shows the contents of the three registers with error bits set. These error bits are then cleared by the command. When VAX/DS is halted as it was in ⑤ and a command is issued that causes errors, as in ⑦, the CLEAR EXCEPTION command must be issued before issuing the CONTINUE command to resume the VAX/DS session.

⑨ VAX/DS is halted and SHOW CONFIGURATION is issued, again creating errors. (The response to SHOW CONFIGURATION is the same as shown in ⑦.) This time the CONTINUE command is issued without first issuing CLEAR EXCEPTION. Since error bits were not cleared, VAX/DS attempts to perform its error recovery procedures, and an interrupt occurs. This is normal behavior for a VAX 6000–400 system in these circumstances.

2.4.3 VAX/DS Diagnostics

Table 2–8 lists the VAX Diagnostic Supervisor tests available for the VAX 6000–400 system.

Table 2–8: VAX Diagnostic Supervisor Programs

Diagnostic	Level	Diagnostic Title
ERSAA[1]		VAX 6000–400 Diagnostic Supervisor
EVSBA	3	VAX Stand-Alone Autosizer
EVSBB	1	VAX Diagnostic Online Autosizer
		KA64A-Specific Diagnostics
ERKAX[1]	3	Manual Tests (5–6 min[2])
ERKMP[1]	3	Multiprocessor Exerciser (2 min—quick) (4 min—default)
		FV64A-Specific Diagnostics
EVKAG	2	VAX Vector Instruction Exerciser, Part 1 (1 1/2 min—quick) (16 min—default)
EVKAH	2	VAX Vector Instruction Exerciser, Part 2 (1 min—quick) (18 min—default)
		VAX CPU Cluster Exerciser
EVKAQ	2	VAX Basic Instructions Exerciser, Part 1
EVKAR	2	VAX Basic Instructions Exerciser, Part 2
EVKAS	2	VAX Floating-Point Instruction Exerciser, Part 1
EVKAT	2	VAX Floating-Point Instruction Exerciser, Part 2

[1]Diagnostic software with file names beginning with ER are tests created specifically for the VAX 6000–400 system. This software is not transportable.

[2]Operator intervention required.

Table 2–8 (Cont.): VAX Diagnostic Supervisor Programs

Diagnostic	Level	Diagnostic Title
		VAX CPU Cluster Exerciser
EVKAU	3	VAX Privileged Architecture Instruction Test, Part 1
EVKAV	3	VAX Privileged Architecture Instruction Test, Part 2
		KDB50 Diagnostics
EVRLF	3	UDA50/KDB50 Basic Subsystem Diagnostic
EVRLG	3	UDA50/KDB50 Disk Drive Exerciser
EVRLB	3	VAX RAxx Formatter
EVRLJ	3	VAX UDA50-A/KDB50 Subsystem Exerciser
EVRLK	3	VAX Bad Block Replace Utility
EVRLL	3	Disk Drive Internal Error Log Utility
EVRAE	2R	VAX Generic MSCP Disk Exerciser
		DEBNA Diagnostics
EVDYD	2R	DEBNA Online Functional Diagnostic
EVDWC	2R	VAX NI Exerciser
		DEBNI Diagnostics
EVDYE	2R	DEBNI Online Functional Diagnostic
EVDWC	2R	VAX NI Exerciser
		TBK Diagnostic
EVMDA	2R	TK Data Reliability Exerciser
		CIBCA-AA Diagnostics
EVGCA	3	T1015 Repair Level Diagnostic, Part 1
EVGCB	3	T1015 Repair Level Diagnostic, Part 2
EVGCC	3	T1015 Repair Level Diagnostic, Part 3

Table 2–8 (Cont.): VAX Diagnostic Supervisor Programs

Diagnostic	Level	Diagnostic Title
		CIBCA-AA Diagnostics
EVGCD	3	T1015 Repair Level Diagnostic, Part 4
EVGCE	3	T1025 Repair Level Diagnostic
EVGAA	3	CI Functional Diagnostic, Part 1
EVGAB	3	CI Functional Diagnostic, Part 2
EVGDA	3	CIBCA EEPROM Program and Update Utility
EVXCI	1	VAX CI Exerciser
		CIBCA-BA Diagnostics
EVGEE	3	CIBCA-BA Repair Level Diagnostic, Part 1
EVGEF	3	CIBCA-BA Repair Level Diagnostic, Part 2
EVGEG	3	CIBCA-BA Repair Level Diagnostic, Part 3
EVGAA	3	CI Functional Diagnostic, Part 1
EVGAB	3	CI Functional Diagnostic, Part 2
EVGDA	3	CIBCA EEPROM Program and Update Utility
EVXCI	1	VAX CI Exerciser
		KLESI-B/TU81 Diagnostics
EVMBA	2R	VAX TU81 Data Reliability Diagnostic
EVMBB	3	VAX Front-End/Host Functional Diagnostic
		DHB32 Diagnostics
EVDAR	3	DHB32 Diagnostics
EVDAS	2R	DHB32 Macrodiagnostics
		DMB32 Diagnostics
EVAAA	2R	VAX Line Printer Diagnostic
EVDAJ	2R	DMB32 Online Asynchronous Port Test

Table 2–8 (Cont.): VAX Diagnostic Supervisor Programs

Diagnostic	Level	Diagnostic Title
		DMB32 Diagnostics
EVDAK	3	DMB32 Stand-Alone Functional Verification
EVDAL	2R	DMB32 Online Synchronous Port Test
EVDAN	2R	DMB32 Online Data Communications Link
		DRB32 Diagnostics
EVDRH	3	DRB32-M, -E Functional Diagnostic
EVDRI	3	DRB32-W Functional Diagnostic
		UNIBUS Diagnostics
EVCBB	3	VAX DWBUA VAXBI to UNIBUS
EVDRB	2R	VAX DR11W Online Diagnostic
EVDRE	3	VAX DR11W Repair Level Diagnostic
EVDUP	3	DUP11 Repair Level, Part 1
EVDUQ	3	DUP11 Repair Level, Part 2
EVAAA	2R	VAX Line Printer Diagnostic (LP11)
		DSB32 Diagnostics
EVDAP	3	DSB32 Level 3 Diagnostic
EVDAQ	2R	DSB32 Level 2R Diagnostic
		RV20 Diagnostics
EVRVA	3	RV20 Level 3 Functional Diagnostic
EVRVB	2R	RV20 Level 2R Diagnostic
		XMA Online Memory Diagnostic
EVKAM	2R	VAX Memory User Mode Test

CHAPTER 3

Chapter 3
KA64A Scalar Processor

This chapter contains the following sections:

- KA64A Physical Description and Specifications
- KA64A Configuration Rules
- Functional Description
- Boot Processor
- Power-Up Sequence
- KA64A Self-Test Results: Console Display
- KA64A Self-Test Results: Module LEDs
- KA64A Self-Test Results: XGPR Register
- ROM-Based Diagnostics
- KA64A Self-Test—RBD 0
- CPU/Memory Interaction Tests—RBD 1
- VAX/DS Diagnostics
- Machine Checks
- Console Commands
- KA64A Handling Procedures
- How to Replace the Only Processor
- How to Replace the Boot Processor
- How to Add a New Processor or Replace a Secondary Processor
- PATCH EEPROM Command
- PATCH EEPROM Command Error Messages
- KA64A Registers

3.1 KA64A Physical Description and Specifications

The KA64A is a single-module VAX processor. The module designation is T2015. VAX 6000–400 systems include multiple KA64A processors, which use the 100 Mbyte/second XMI system bus to communicate with memory. Features of the module are shown in Figure 3–1.

Figure 3–1: KA64A Module

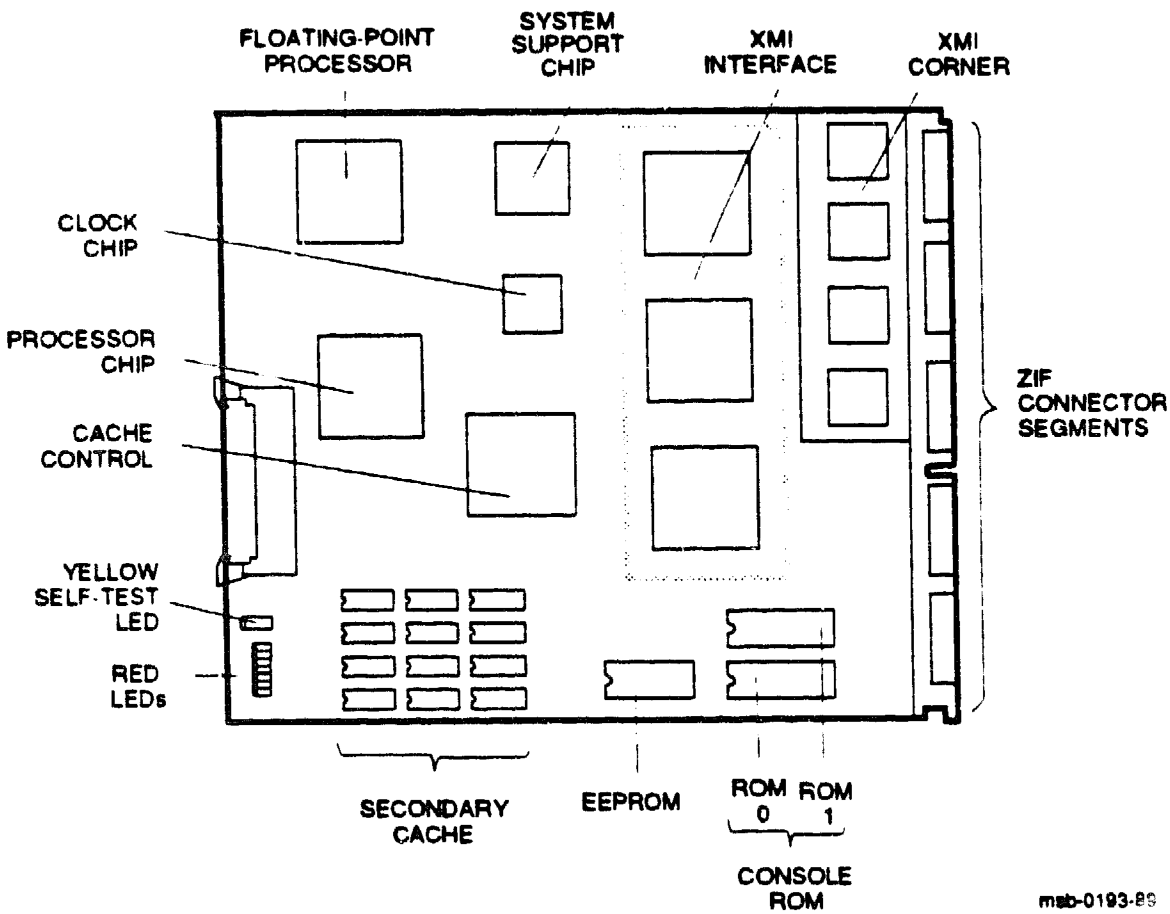


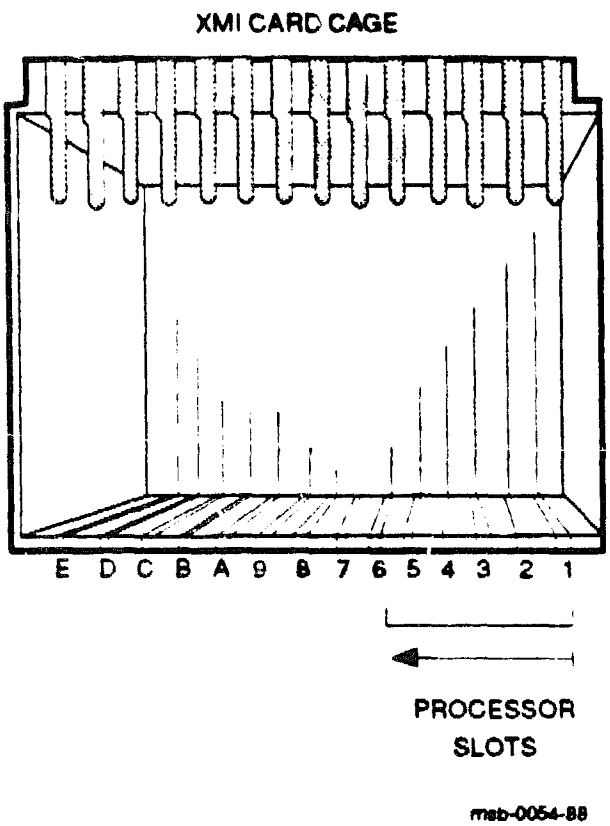
Table 3–1: KA64A Specifications

Parameter	Description
Module Number:	T2015
Dimensions:	23.3 cm (9.2") H x 0.6 cm (0.25") W x 28.0 cm (11.0") D
Temperature:	
Storage Range	-40°C to 66°C (-40°F to 151°F)
Operating Range	5°C to 50°C (41°F to 122°F)
Relative Humidity:	
Storage	10% to 95% noncondensing
Operating	10% to 95% noncondensing
Altitude:	
Storage	Up to 4.8 km (16,000 ft)
Operating	Up to 2.4 km (8000 ft)
Current:	8A at +5V 0.20A at +5VBB
Power:	41W
Cables:	None
Diagnostics:	ROM-based diagnostics (0 and 1) VAX/DS diagnostics, see Section 3.12.

3.2 KA64A Configuration Rules

KA64A modules will operate in any slot of the XMI card cage; however, processors usually go on the right, beginning with slot 1. Special rules apply if the KA64A has an attached vector processor; see Section 4.3.

Figure 3–2: Typical KA64A Configuration



By convention, processors are placed in the right XMI slots, beginning with slot 1 and extending to slot 6. Memories are placed in the middle slots, from slot A to slot 5 and then slots B and C, and VAXBI adapters are installed in the left side of the card cage, beginning with slot E.

An attached vector processor must be in the slot to the left of the KA64A module. The slot to the left of the vector processor can be used *only* for a memory module. Installing another kind of module can damage the vector module.

For performance reasons, the scalar processor of a scalar/vector pair should not be made the primary processor when other scalar processors are in the system.

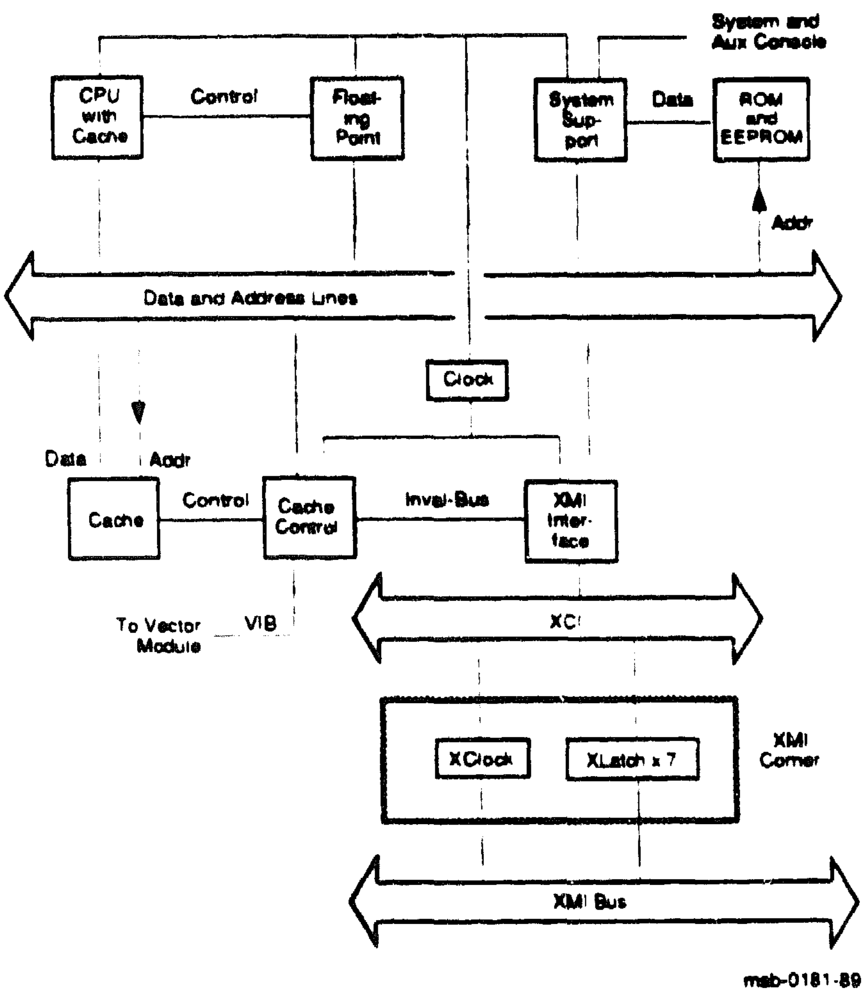
A processor module should be replaced if it consistently fails self-test, or if it causes the operating system to crash. However, you can leave the module in the system temporarily, since the console program prevents the operating system from using that processor. If a processor module fails intermittently, you should prevent the operating system from using it by doing the following:

1. Enter console mode.
2. Use the command SET CPU/NOENABLE to remove the processor from the software configuration.
3. Reboot the operating system.

3.3 Functional Description

The KA64A processor has four functional sections (see Figure 3-3): the CPU section, the backup cache, the XMI interface, and the console and diagnostics sections.

Figure 3-3: KA64A Block Diagram



The CPU section includes:

- The processor chip, which supports the VAX instruction set and data types. It contains a 64-entry, fully associative translation buffer for both process and system-space mappings. The processor chip includes a 2-Kbyte, direct-mapped, write-through instruction and data cache with a quadword block and fill size.
- A floating-point accelerator chip that enhances the computation phase of floating-point and some integer instructions. This chip receives operands from the processor chip, computes the result, and passes the result and status back to the processor chip to complete the instruction.

The backup cache is a 128-Kbyte, direct-mapped, write-through instruction and data cache. It is implemented in 24 16-Kbyte x 4 data RAMs. The backup cache contains 2-Kbyte tags, organized to provide an octaword fill size and a 4-octaword block size.

The XMI interface includes:

- An octaword write buffer that decreases bus and memory controller bandwidth needs by packing writes into larger, more efficient blocks prior to sending them to main memory.
- Cache fill logic that loads the backup cache with four octawords of data on each cache miss.
- XMI write monitoring logic that uses a duplicate tag store to detect when another XMI node writes a memory location that is cached on this processor. Then the XMI interface chips invalidate the corresponding entry in the backup cache.
- Full set of error recovery and logging capabilities.

Example 3–1: ROM and EEPROM Version Numbers

```
#123456789 0123456789 0123456789 012345678#

F   E   D   C   B   A   9   8   7   6   5   4   3   2   1   0   NODE #

    A   A   .   .   M   M   M   M   .   .   P   P   P   P       TYP
    o   o   .   .   +   +   +   +   .   .   +   +   +   +       STF
    .   .   .   .   .   .   .   .   .   .   E   D   E   B       BPD
    .   .   .   .   .   .   .   .   .   .   +   +   +   +       ETF
    .   .   .   .   .   .   .   .   .   .   E   D   E   B       BPD

.   .   .   .   .   .   .   .   .   +   +   .   +   .   +   .   XBI D +
.   .   .   .   .   .   .   .   .   +   .   +   .   +   +   .   XBI E +

    .   .   .   .   A4  A3  A2  A1  .   .   .   .   .   .       ILV
    .   .   .   .   32  32  32  32  .   .   .   .   .   .       128Mb

ROM0 = V1.00(1)  ROM1 = V1.00(2)  EEPROM = 1.00/1.00(3)  SN = SG01234567(4)
```

The console and diagnostics sections include:

- A console read-only memory (ROM), which contains the code for initialization, executing console commands, and bootstrapping the system. The last line of the self-test display shows the ROM version. In this example, callout ❶ indicates that the console ROM, ROM0, is version V1.00.
- A diagnostic ROM, ROM1, which contains the power-up self-test and extended diagnostics. The diagnostic ROM has the same version number as the console ROM. In this example callout ❷ indicates that the diagnostic ROM is version V1.00.
- An electrically-erasable, programmable ROM (EEPROM), which contains system parameters and boot code. You can modify the parameters with the console SET commands. Patching console and diagnostic code in the ROMs is accomplished by reading the patches into a special area of the EEPROM. The console PATCH EEPROM command is described in Section 3.18.

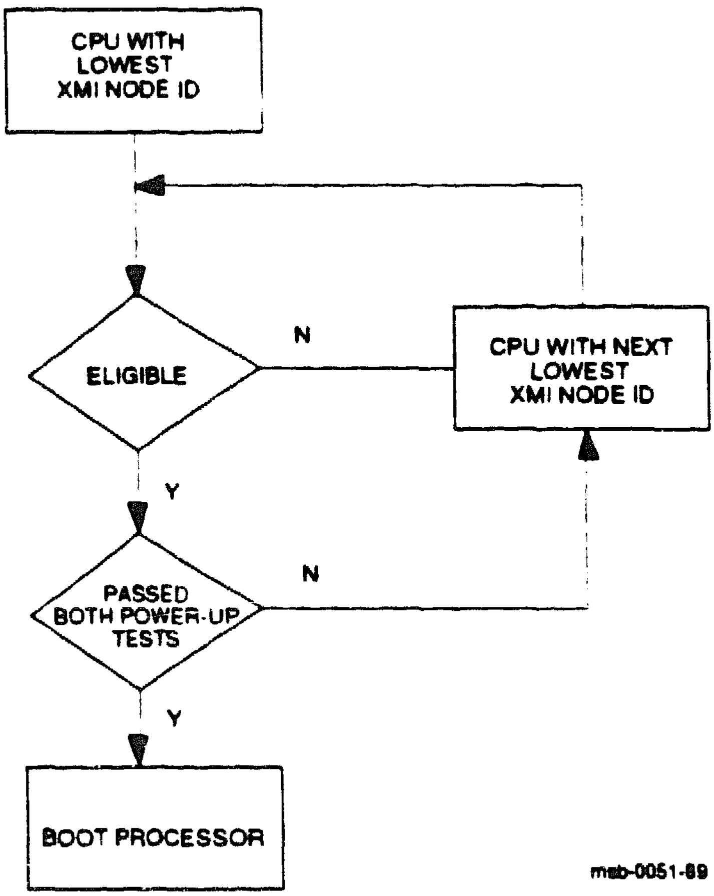
  The last line of the self-test display shows two EEPROM version numbers. The first number ❸ indicates the format version of the EEPROM. This version is changed only when the internal structure of the EEPROM is modified.

  The second number ❹ is the revision of ROM patches that have been applied to the EEPROM. The major number in this revision (before the decimal point) corresponds to the major number of the ROM revision ❶. The minor number indicates the actual patch revision. In this example, the EEPROM has not been patched for console ROM V1.00.
- A system support chip (RSSC) that includes support for external ROM/EEPROM, 1 Kbyte of battery-backed-up RAM, console terminal UARTs, bus reset logic, interval timer, programmable timers, time-of-year (TOY) clock, bus timeout, and halt arbitration logic.

3.4 Boot Processor

In the VAX 6000–400 system all KA64A processors share system resources equally. The processor controlling the console at any given time is designated as the primary or boot processor. The others are called secondary processors. The boot processor is selected during the power-up sequence.

Figure 3–4: Selection of Boot Processor



Using boot code stored in its EEPROM, the boot processor reads the boot block from a specified device. Booting may be triggered by a command issued to the boot processor from the console, or by a system reset with the bottom key switch in the Auto Start position.

The boot processor also communicates with the system console, using the common console lines on the backplane. When you change system parameters in the EEPROM using SET commands, the boot processor automatically copies the new values to the EEPROMs on the secondary processors. If you swap in a new KA64A module, it should be configured as a secondary processor. Then you can use the UPDATE command to copy the boot processor's entire EEPROM to the new secondary. See the *VAX 6000–400 Owner's Manual* for a description of the UPDATE command.

Usually the processor with the lowest XMI node number (which is also the lowest slot number) is selected as the boot processor. However, if this processor does not pass all its power-up tests, the next higher-numbered processor is selected. This is one way the boot processor can change.

The user also has control over boot processor selection with the SET CPU command. This command may declare a processor ineligible for selection. SET CPU can also select a boot processor explicitly.

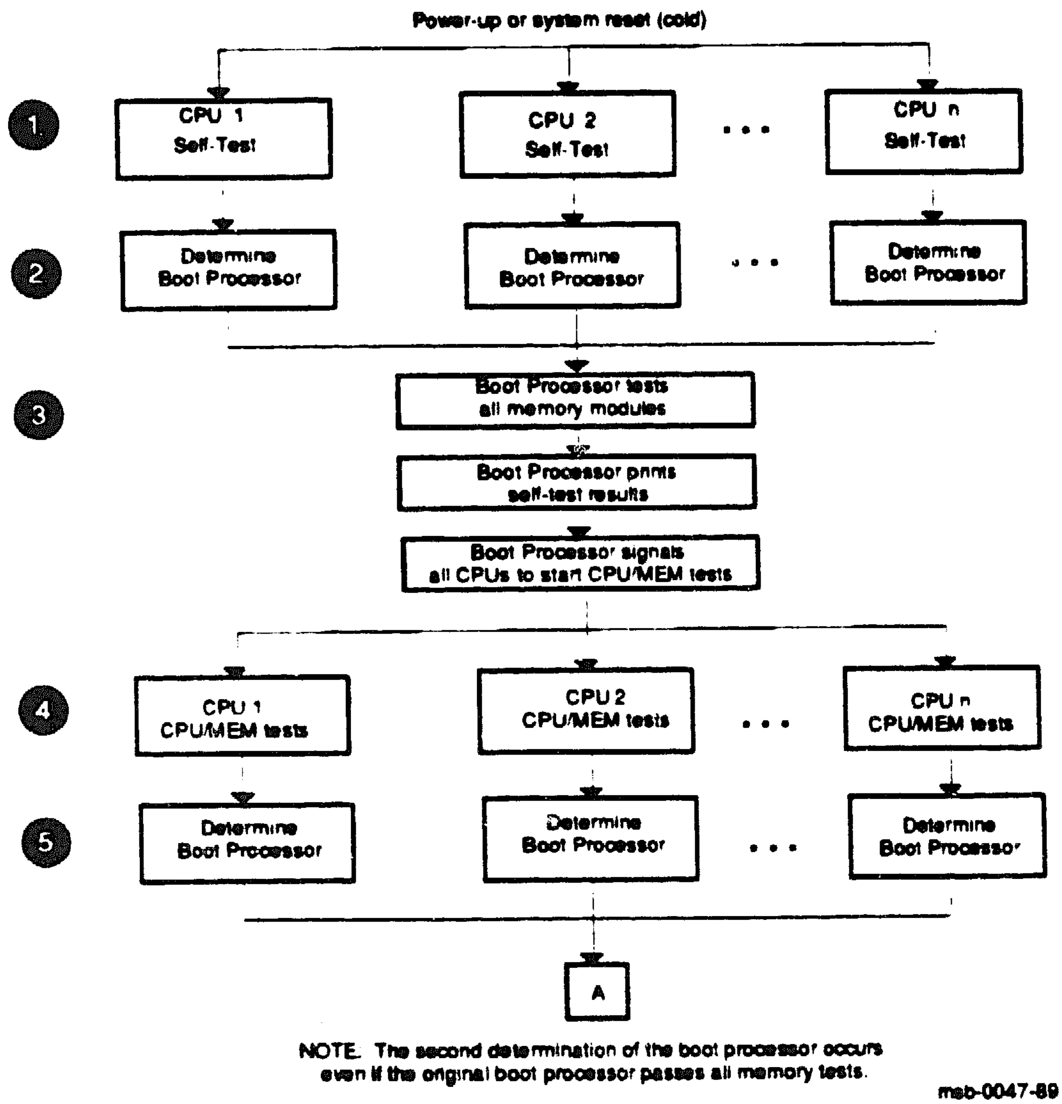
You can see the boot processor selection three ways:

- In the self-test display, the boot processor is indicated by a **B** on the second line labeled **BPD**.
- In console mode, the command SHOW CPU displays the boot processor as "Current primary."
- The bottom red LED is off on the boot processor module. It is lit on secondary processors.

3.5 Power-Up Sequence

Figure 3–5 shows the power-up sequence for KA64A processors. All processors execute two phases of self-test, and a boot processor is selected. The boot processor tests the VAXBI adapters and prints the self-test display.

Figure 3–5: KA64A Power-Up Sequence, Part 1 of 2



❶ All CPUs execute their on-board self-tests at the beginning of the power-up tests. On line **STF** of the self-test display, a plus sign (+) is shown for every module whose self-test passes (see Section 3.6).

❷ The boot processor is determined as described in Section 3.4. On the **first BPD line**, the letter **B** corresponds to the processor selected as boot processor. Because the processors have not yet completed their power-up tests, the designated processor may later be disqualified from being boot processor. For this reason, line BPD appears twice in the self-test display.

❸ The boot processor tests all memory modules, and then prints the results of self-test, lines **NODE, TYP, STF,** and **BPD** on the self-test display. The boot processor then signals all CPUs to start running the extended test.

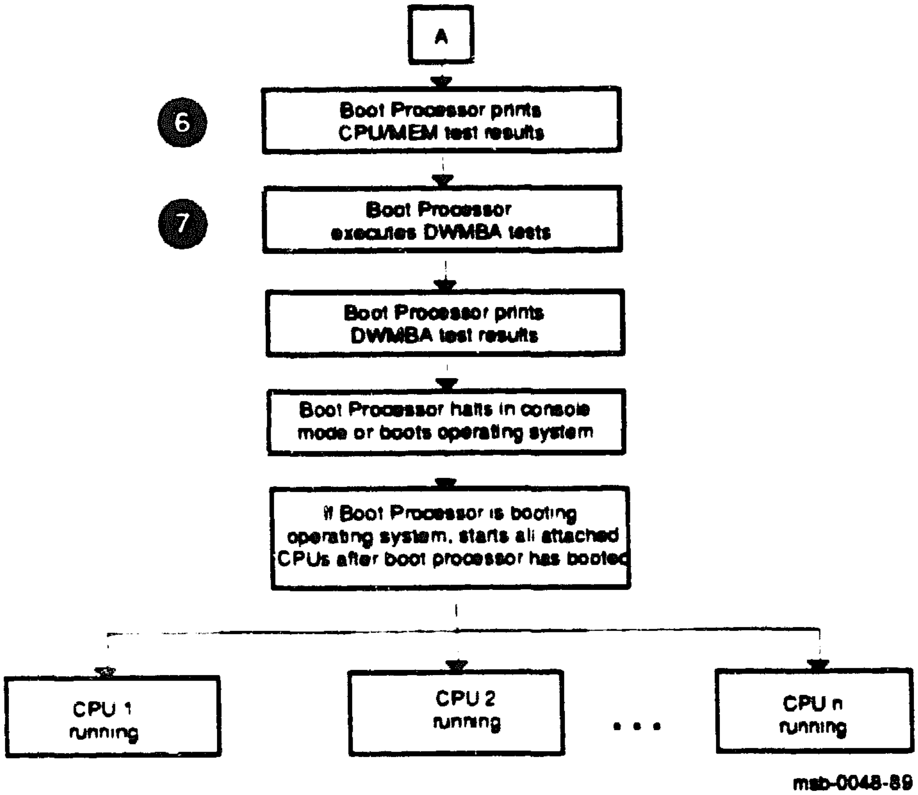
❹ All CPUs execute an extended test using the memories. On line **ETF** of the self-test display, a plus sign (+) is shown for every module that passes extended test.

❺ If all CPUs pass the extended test, the original boot processor selection is still valid. Lines STF and ETF would be identical for all the processors.

The yellow LED and the top red LED are lit on all processor modules that pass both power-up tests. On the secondary processors, the bottom red LED is also lit. On the boot processor, this red LED is off (see Figure 3–7).

If the original boot processor fails the extended test (indicated by a minus sign (–) on line ETF), a new boot processor is selected. On the **second BPD line**, the letter **B** corresponds to the processor finally selected as boot processor.

Figure 3–6: KA64A Power-Up Sequence, Part 2 of 2



❻ The boot processor prints line **ETF** and the second **BPD** line of the self-test display. If none of the processors is successfully selected as the boot processor, no self-test results are displayed and the console hangs You can identify this hung state by examining the LEDs on the processor modules (see Section 3.7). All yellow LEDs will be OFF. The group of seven red LEDS indicate the failing test number in binary-coded decimal.

❼ The boot processor tests the DWMBA. Test results are indicated on the lines labeled **XBI** on the self-test display. A plus sign (+) at the extreme right means that the adapter test passed; a minus sign (–) means that the test failed.

3.6 KA64A Self-Test Results: Console Display

You can check KA64A self-test results in three ways: the self-test display, the lights on the module, and the contents of the XGPR register. Pertinent information in the self-test display is shown in Example 3–2. See Chapter 4 for information on systems with vector modules.

Example 3–2: Self-Test Results

```
#123456789 0123456789 0123456789 01234567#❶

F    E    D    C    B    A    9    8    7    6    5    4    3    2    1    0    NODE #

     A    A    .    .    M    M    M    M    .    .    P    P    P    P         TYP❷
     o    o    .    .    +    +    +    +    .    .    +    +    +    +         STF❸
     .    .    .    .    .    .    .    .    .    .    E    E    D    B         BPD❹
     .    .    .    .    .    .    .    .    .    .    +    +    +    -         ETF❺
     .    .    .    .    .    .    .    .    .    .    E    B    D    E         BPD❻

.    .    .    .    .    .    .    .    .    +    +    .    +    .    +    .    XBI D +
.    .    .    .    .    .    .    .    .    +    .    +    .    +    +    .    XBI E +

     .    .    .    .    A4   A3   A2   A1   .    .    .    .    .    .         ILV
     .    .    .    .    32   32   32   32   .    .    .    .    .    .         128Mb

ROM0 = V1.00   ROM1 = V1.00   EEPROM = 1.00/1.00   SN = SG01234567❼
>>>
```

❶ The first line of the self-test printout is the progress trace. This line prints if a KA64A module is in node 1 and the baud rate is at least 1200. The progress trace has two purposes: to give a visual indication that the system is functioning during self-test, and, if self-test fails, to display the failing test number. The numbers correspond to the 37 tests in the KA64A self-test. When self-test passes, the line prints as in Example 3–2. If a test fails, the failing test number is the last one printed. For example, if test 14 fails, the line is printed as follows:

```
#123456789 01234
```

❷ This line indicates the type (TYP) of module at each XMI node. Processors are type P. In this example, processors are at nodes 1, 2, 3, and 4.

❸ This line shows self-test fail status (STF), which are the results of on-board self-test. Possible values for processors are:

+ (pass)
– (fail)

All processors passed self-test in this example.

❹ The BPD line indicates boot processor designation. When the system completes on-board self-test, the processor with the lowest XMI ID number that passes self-test and is eligible is selected as boot processor — in this example, the processor at node 1.

The results on the BPD line indicate:

- The boot processor (B)
- Processors eligible to become the boot processor (E)
- Processors ineligible to become the boot processor (D)

❺ During extended test (ETF) all processors run additional tests, which include reading and writing memory and using the cache. On line ETF, results are reported for each processor in the same way as on line STF— a plus sign indicates that extended test passed and a minus sign that extended test failed. In this example, the processor at node 1 (originally selected boot processor) failed the CPU/memory interaction tests.

❻ Another BPD line is displayed, because it is possible for a different CPU to be designated boot processor before the system actually boots. This occurs in this example, because the processor at node 1 failed the extended test. The lowest-numbered processor that passed both tests is the processor at node 2. However, a previous SET CPU/NOPRIMARY command has made this processor ineligible to be boot processor (indicated by the designation D on the BPD line). Therefore, the processor at node 3 is designated boot processor.

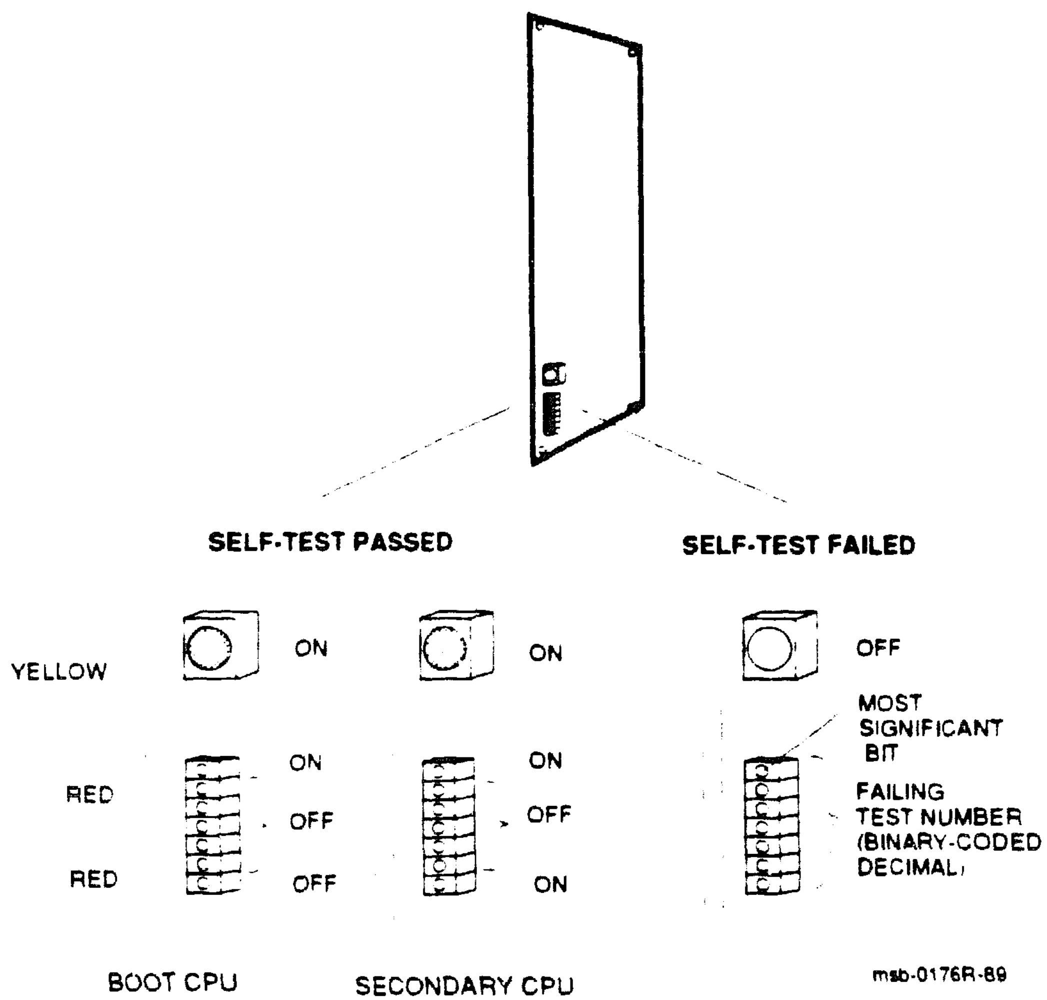
❼ The bottom line of the self-test display shows the ROM and EEPROM version numbers and the system serial number.

A KA64A performs additional tests on an attached FV64A vector module (see Section 4.5).

3.7 KA64A Self-Test Results: Module LEDs

You can check KA64A self-test results in the self-test display, in the lights on the module, or in the XGPR register. If self-test passes, the large yellow LED is on.

Figure 3–7: KA64A LEDs After Power-Up Self-Test



If self-test passes, the large yellow LED at the top of the LEDs is ON. (Here self-test means both the on-board power-up tests, RBD 0, and the CPU/memory interaction tests, RBD 1.) The top red LED (next to the yellow one) is also ON, and the next five red LEDs are OFF. The bottom LED is OFF if the processor is the boot processor, and ON if it is a secondary processor.

If self-test fails, the yellow LED is OFF, and the red LEDs contain an error code that corresponds to the number of the failing test. The test number is represented in binary-coded decimal. In the seven red error LEDs, the most significant bit is at the top, but the lights have a reverse interpretation — a bit is ONE if the light is OFF.

For example, assume a processor fails self-test (yellow LED is OFF) and shows the following pattern in its seven red LEDs:

```
TOP
     (MSB) on       0
           off      1  =  3
           off      1

           on       0
           on       0  =  2
           off      1
           on       0
BOTTOM
```

The failing test number decodes to 011 0010 (binary-coded decimal 32). If you then ran RBD 0 with the /TR and /HE qualifiers, the last test number you would see displayed is T0032.

When any of the red error LEDs is lit, a failure has occurred during the self-test sequence. But system power-up self-test actually comprises three sets of tests: KA64A power-up tests (RBD 0), CPU/memory interaction tests (RBD 1), and VAXBI adapter (DWMBA) tests (RBD 2). Interpretation of the processor board error lights depends on which set of tests was running, as explained below and in Table 3–9.

Processor error LEDs can also indicate failures of memories or VAXBI adapters.

Table 3–9: KA64A Error LEDs

Yellow LED	Red LEDs (Binary-coded decimal)	Diagnostic and Test Number	Device Failing	Self-Test Line
OFF	1–37*	Power-up self-test (RBD 0) T0001–T0037 See Table 3–6.	KA64A	STF
OFF	50–62*	CPU/memory test - Memory 1 (RBD 1) T0001–T0013 See Table 3–7.	KA64A or MS62A 1 (module with lowest XMI node number)	ETF
OFF	67	CPU/memory test - Memory 2 T0003 (equivalent to ST1/T=3)	MS62A 2	ETF
OFF	68	CPU/memory test - Memory 3 T0003 (equivalent to ST1/T=3)	MS62A 3	ETF
OFF	69	CPU/memory test - Memory 4 T0003 (equivalent to ST1/T=3)	MS62A 4	ETF
OFF	70	CPU/memory test - Memory 5 T0003 (equivalent to ST1/T=3)	MS62A 5	ETF
OFF	71	CPU/memory test - Memory 6 T0003 (equivalent to ST1/T=3)	MS62A 6	ETF
OFF	72	CPU/memory test - Memory 7 T0003 (equivalent to ST1/T=3)	MS62A 7	ETF
OFF	73	CPU/memory test - Memory 8 T0003 (equivalent to ST1/T=3)	MS62A 8	ETF
ON	1–26	DWMBA test (RBD 2) T0001–T0026 See Table 6–5.	DWMBA	XBI

*Applies to scalar-only configuration. If scalar CPU running tests has an attached vector module, the power-up tests are 1–49, and the CPU/memory tests are 50–66.

If a processor's yellow LED is OFF and the red LEDs show an error code in the range 1–37, the power-up self-test failed and the processor board is bad. On the self-test console display, the processor shows a minus sign (–) on the STF line.

After the power-up tests, each processor runs the CPU/memory interaction tests. If a test fails, the processor shows a minus sign (–) on the ETF line of the self-test console display. The LED error codes are numbered from 50 to 62, which is the failing test number (1 through 13) plus 49. For example, assume that a processor fails self-test (yellow LED is OFF) and shows the following pattern in the error LEDs:

```
TOP
      (MSB) off     1
            on      0  =  5
            off     1

            on      0
            off     1  =  6
            off     1
            on      0
BOTTOM
```

The failing test number decodes to 101 0110 (binary-coded decimal 56), which corresponds to the seventh CPU/memory interaction test ((56–49 = 7).) If you then run RBD 1 with the /TR and /HE qualifiers, the last test number you see displayed is T0007.

Each processor, after testing with the first memory, runs the CPU/memory interaction tests on every other good memory module. (However, only CPU/memory interaction test T0003 is run.) If a failure occurs, the memory module is probably bad, although the processor's yellow light is OFF and the memory module's yellow light is ON. If several processors fail on the same memory, the memory is certainly bad. Try using SET MEMORY to configure the bad module out of the interleave set. For error codes higher than 66, consult Table 3–9 to determine the failing memory.

The last series is the DWMBA tests. If one fails, the red LEDs contain an error code, although the processor's yellow self-test LED is ON (because the CPU itself has passed). The failing test numbers are listed in Table 6–5. Note that only the boot processor performs the DWMBA tests.

3.8 KA64A Self-Test Results: XGPR Register

You can check KA64A self-test results in the self-test display, in the lights on the module, or in the XGPR register. When a failure occurs during power-up and the failing test number cannot be found in the module LEDs and RBDs cannot be run, you can examine the XGPR register. The failing test number is left in the upper byte of the XGPR register of the failing KA64A processor or of the boot processor if a memory or DWMBA module fails.

Example 3–3: XGPR Register After Power-Up Test Failure

```
>>> E/P/L 2190000C             ! Examine the longword at physical address
                               ! 2190000C, the address of the XGPR
2190000C  30xxxxxx             ! register of the KA64A processor in slot 2.
                               ! The result indicates that test 30 of the
                               ! KA64A self-test failed. See Table 3-4
                               ! to interpret the data returned.

>>> E/P/L 2188000C             ! Examine the XGPR register of the KA64A
                               ! processor in slot 1. Derivation of the
                               ! address is explained below.
2188000C  49xxxxxx             ! CPU/memory interaction test 12 failed.

>>> E/P/L 2188000C             ! Examine the XGPR register of the boot
                               ! processor, which is in slot 1.
2188000C  A0xxxxxx             ! Disregard bit <31> (which indicates a
                               ! DWMBA test failure); the failing test
                               ! number is 20.
```

When a failure occurs in power-up test, you can examine the XGPR register to determine the failing test number. The XGPR register of the KA64A processor that failed self-test or CPU/memory interaction test, or of the boot processor if DWMBA test failed, contains the failing test number. If all power-up tests pass, the XGPR register contains other data and should be ignored.

To examine the XGPR register, first see Table 3–3 to determine the base address (BB) of the KA64A processor's node. Then calculate the address of the XGPR register by adding 0C (hex) to the base address.

The failing test number is derived from the upper byte (bits <31:24>) of the longword returned. For self-test, the upper byte contains the failing test number. If CPU/memory interaction test fails, this byte contains the failing test number plus 49. If DWMBA test fails, bit <31> is set (making the first digit 8 through A), and bits <30:24> contain the failing test number. All numbers are expressed in binary-coded decimal (BCD). See Table 3–4.

Table 3–3: XMI Base Addresses

Slot	Node	Base Address (BB)
1	1	2188 0000
2	2	2190 0000
3	3	2198 0000
4	4	21A0 0000
5	5	21A8 0000
6	6	21B0 0000
7	7	21B8 0000
8	8	21C0 0000
9	9	21C8 0000
10	A	21D0 0000
11	B	21D8 0000
12	C	21E0 0000
13	D	21E8 0000
14	E	21F0 0000

Table 3–4: Interpreting XGPR Failing Test Numbers

Failing Diagnostic	XGPR <31>	XGPR <30:24> (BCD)	Test Numbers
Self-test	Clear	1–49	1–49
CPU/memory interaction test	Clear	50–66	1–17
Additional memory	Clear	67–73	3
DWMBA test	Set	1–26	1–26

3.9 ROM-Based Diagnostics

The KA64A ROMs contain four diagnostics, which you run using the boot processor's RBD monitor program described in Chapter 2. RBD 0 and RBD 1 test the boot processor. RBD 2 tests the DWMBA/A and DWMBA/B adapters, and RBD 3 tests XMI memories.

Table 3–5: ROM-Based Diagnostics

Diagnostic	Test
0	KA64A self-test
1	KA64A CPU/memory interaction tests
2	DWMBA tests
3	XMI memory tests

RBD 0 is the same as the KA64A self-test. It is useful for running several passes when a processor fails self-test intermittently. Section 3.10 shows examples of running RBD 0 on both the boot processor and a secondary processor, and lists the tests in RBD 0.

RBD 1 is the same as the CPU/memory interaction tests. It is useful for running several passes when a processor fails CPU/memory interaction tests intermittently. Section 3.11 shows an example and lists the tests.

RBD 2 is the set of tests that the boot processor runs for each DWMBA VAXBI-to-XMI adapter when the system is powered on. (The DWMBA has no on-board self-test of its own.) Section 6.4 shows an example and lists the tests.

RBD 3 is a set of XMI memory tests that sizes and runs extended tests on all of memory. Sections 5.10 and 5.11 list the tests and show examples.

For a detailed explanation of the diagnostic printout, see Chapter 2.

3.10 KA64A Self-Test—RBD 0

RBD 0 is equivalent to the KA64A self-tests. The first 37 tests test scalar CPU modules; tests 38–49 test vector modules.

Example 3–4: KA64A Self-Test—RBD 0

```
>>> T/R                     ! Command to enter RBD monitor program.
RBD1>                       ! RBD monitor prompt, where 1 is the hexa-
                            ! decimal node number of the boot processor.
RBD1> ST0/TR/HE             ! Runs the KA64A self-test on boot processor
                            ! Trace prints each test number; halt on error
                            ! Test results written to the console terminal:
;XRP_ST          1.00

; T0001  T0002  T0003  T0004  T0005  T0006  T0007  T0008  T0009  T0010
; T0011  T0012  T0013  T0014  T0015  T0016  T0017  T0018 ❶

;       F ❷      1      8082        1 ❸
;       HE   REX520       XX    T0018 ❶
;       10 AAAAAAAA A8AAAAAA 00000000 000004AC 2006451F 01

;       F        1      8082        1
;0000000C 00000001 00000000 00000000 00000000 00000000 00000000

RBD1>
```

In Example 3–4:

❶ Test 18 failed. The /HE switch causes execution to stop when the error is encountered.

❷ F indicates failure.

❸ The diagnostic ran for one pass.

Example 3–5: Running KA64A Self-Test (RBD 0) on a Secondary Processor

```
>>> SET CPU 2❶
>>> T/R
RBD2> ST0/TR❷

;XRP_ST       1.00

; T0001  T0002  T0003  T0004  T0005  T0006  T0007  T0008  T0009  T0010
; T0011  T0012  T0013  T0014  T0015  T0016  T0017  T0018  T0019  T0020
; T0021  T0022  T0023  T0024  T0025  T0026  T0027  T0028  T0029  T0030
; T0031  T0032  T0033  T0034  T0035  T0036  T0037

;      P       2     8082        1
;00000000 00000000 00000000 00000000 000000000 00000000 00000000
```

In Example 3–5:

❶ This command causes the KA64A module at node 2 to become the primary processor.

❷ The prompt indicates that the CPU at node 2 is the primary processor. RBD 0 is run on this processor.

Table 3–6: KA64A Self-Test—RBD 0

Test	Function
T0001	KA64A ROM Checksum Test
T0002	IPL Step-Down Test
T0003	RSSC Configuration Register Test
T0004	RSSC RAM Test
T0005	RSSC Output Port Test
T0006	RSSC Address Decode Register Access Test
T0007	RSSC Console UART External Loopback and Baud Rate Test
T0008	RSSC Console UART Internal Loopback and Interrupt Test
T0009	KA64A EEPROM Test
T0010	RSSC Input Port Test
T0011	RSSC Bus Timeout Test
T0012	RSSC Programmable Timers Test
T0013	RCSR Register Test
T0014	RSSC TOY Clock Test
T0015	RSSC Interval Timer Test
T0016	Interrupts at IPL 14 to 17 Test
T0017	Primary Cache Tag Store Test
T0018	Primary Cache Data RAM March Test
T0019	Backup Tag Store Test
T0020	Flush Cache Test
T0021	Backup Tag Store Parity Error Test
T0022	C-Chip Primary Tag Store Test
T0023	C-Chip Refresh Register Test
T0024	Backup Cache Data Line Test
T0025	Backup Cache Data RAM March Test
T0026	Backup Cache Data Parity RAM March Test
T0027	Cache Mask Write Test

Table 3–6 (Cont.): KA64A Self-Test—RBD 0

Test	Function
T0028	Data Parity Logic Test
T0029	Cache Disable Test
T0030	XGPR Register Test
T0031	CNAK Test
T0032	IVINTR Test
T0033	Multiple Interrupt Test
T0034	DC520 Critical Path Test
T0035	F-Chip Test
T0036	Disable F-Chip Test
T0037	F-Chip Critical Path Test
T0038	VECTL Registers Test
T0039	Verse Registers Test
T0040	Load/Store Registers Test
T0041	VIB Error Logic Test
T0042	Other VECTL Chip Logic Test
T0043	Verse and Favor Test
T0044	Load/Store Translation Buffer and CAM Test
T0045	Load/Store Cache Test
T0046	Load/Store Instruction Test
T0047	Load/Store Tag and Duplicate Tag Test
T0048	Load/Store Error Cases Test
T0049	Module Critical Path Test

3.11 CPU/Memory Interaction Tests — RBD 1

RBD 1 is equivalent to the CPU/memory interaction tests. The first 13 tests test scalar CPU modules; tests 14–17 test vector modules.

Example 3–6: CPU/Memory Interaction Tests—RBD 1

```
>>> T/R                          ! Command to enter RBD monitor program

RBD3>                            ! RBD monitor prompt, where 3 is the hexa-
                                 ! decimal node number of the processor
                                 ! that is currently receiving your input.

RBD3> ST1/TR/HE                  ! Runs the CPU/memory interaction RBD with
                                 ! trace; halt on error.  Test results
                                 ! written to the console terminal:

;CPUMEM        1.00

; T0001  T0002  T0003  T0004  T0005  T0006  T0007  T0008  T0009  T0010
; T0011  T0012  T0013

;           P❶       3     8082          1❷
;00000000 00000000 00000000 00000000 00000000 00000000 00000000

RBD3>
```

In the example above:

❶ P means that the diagnostic ran successfully.

❷ One pass was completed.

Table 3–7: CPU/Memory Interaction Tests—RBD 1

Test	Function
T0001	Parity Error CNAK Read/Write Test
T0002	Miss When Invalid Test
T0003	Cache Read Fill Test
T0004	Interlock Instruction Cache Test
T0005	Octaword Write Buffer Test
T0006	Quadword-Boundary Byte Write Buffer Test
T0007	Two-Byte Write in Different Quadword Write Buffer Test
T0008	Write Buffer Switch and Purge Test
T0009	Statistical Write Buffer Test
T0010	Hit Write Buffer Test
T0011	Write Buffer Address Test
T0012	Invalidate Test
T0013	Hit on Disabled Tag Store Test
T0014	Cache Test
T0015	Write Buffer Test
T0016	Duplicate Tag Test
T0017	Miscellaneous Error Test

3.12 VAX/DS Diagnostics

The KA64A software diagnostics that run under the VAX Diagnostic Supervisor (VAX/DS) are listed in Table 3–8. An example follows. See Section 2.4 for instructions on running the supervisor. See Section 4.8 for vector-specific tests.

Table 3–8: KA64A VAX/DS Diagnostics

Program	Description
EVSBA	VAX Stand-Alone Autosizer
EVSBB	VAX Diagnostic Online Autosizer
EVKAQ	VAX Basic Instructions Exerciser, Part 1
EVKAR	VAX Basic Instructions Exerciser, Part 2
EVKAS	VAX Floating Point Instruction Exerciser, Part 1
EVKAT	VAX Floating Point Instruction Exerciser, Part 2
EVKAU	VAX Privileged Architecture Instruction Test, Part 1
EVKAV	VAX Privileged Architecture Instruction Test, Part 2
ERKAX	Manual Tests
ERKMP	Multiprocessor Exerciser

Example 3–7: VAX/DS Commands for Running Stand-Alone Processor Diagnostics

```
DS> RUN EVSBA ❶
DS> SEL KA0 ❷
DS> RUN ERKAX ❸
DS> EXIT ❹
```

The callouts in Example 3–7 are explained below:

❶ Run the stand-alone autosizer; then you do not need to attach devices to the supervisor explicitly. However, if you want to know how to use the Attach command for a specific diagnostic, enter:

```
DS> HELP diagnostic_name ATTACH
```

❷ The instruction and manual tests run on the boot processor. If the boot processor is the CPU with the lowest XMI node number (which is usually the case), issue the command to select KA0. The Diagnostic Supervisor numbers the processors consecutively. For example, if the KA64A module with the second-lowest XMI node number were boot processor, you would select KA1.

❸ This example runs the manual tests (ERKAX), which include powerfail, machine check, restart, and EEPROM functions. The diagnostic prints messages, and you must manually intervene using console switches.

❹ Exit from VAX/DS.

3.13 Machine Checks

Figure 3–8 and Table 3–9 show parameters for machine checks. The KA64A machine check parse tree appears in Appendix E along with parse trees for hard and soft error interrupts.

Figure 3–8: The Stack in Response to a Machine Check

BYTE COUNT	SP
R | 0 | MACHINE CHECK CODE	SP+4
VIRTUAL ADDRESS	SP+8
VIRTUAL INSTRUCTION BUFFER ADDRESS	SP+C
INTERRUPT STATE	SP+10
INTERNAL STATE	SP+14
INTERNAL REGISTER	SP+18
PROGRAM COUNTER	SP+1C
PROCESSOR STATUS LONGWORD	SP+20

msb-0180R-89

Table 3–9: Machine Check Parameters

Parameter	Value (hex) or Bit	Description
Byte Count (SP)	18	Size of stack frame in bytes, not including PSL, PC, or byte count longword
Machine check code (SP+4)	01	Floating-point operand or result transfer error
	02	Floating-point reserved instruction
	03	Floating-point operand parity error
	04	Floating-point unknown status error

Table 3–9 (Cont.): Machine Check Parameters

Parameter	Value (hex) or Bit	Description
	05	Floating-point returned result parity error
	08	Translation buffer miss in ACV/TNV microflow
	09	Translation buffer hit in ACV/TNV microflow
	0A	Undefined INT.ID value
	0B	Undefined MOVCx state
	0C	Undefined instruction trap code
	0D	Undefined control store address
	10	Cache read tag/data parity error
	11	DAL bus or data parity read error
	12	DAL bus error on write or clear write buffer
	13	Undefined bus error microtrap
	14	Vector module error
Virtual address (SP+8)	<31:0>	Current contents of VAP register
Virtual instruction buffer address (SP+C)	<31:0>	Current virtual instruction buffer address
Interrupt state (SP+10)	<22>	ICCS bit <6>
	<15:1>	SISR bits <15:1>
Internal state (SP+14)	<31:24>	Difference between current PC and opcode PC
	<20:18>	Address of last memory reference
	<17:16>	Data length of last memory reference
	<15:8>	Opcode
	<3:0>	Last GPR referenced by E-box
Internal register (SP+18)	<31:0>	
Program counter (SP+1C)	<31:0>	PC at the start of the current instruction
Processor status longword (SP+20)	<31:0>	Current contents of PSL

3.13 Console Commands

Table 3–10 summarizes the console commands. Commands specific to the VAX 6000 series include CLEAR EXCEPTION, RESTORE EEPROM, SAVE EEPROM, SET BOOT, SET CPU, and Z. The VAX 6000–400 Owner's Manual gives a full description of each command, its qualifiers, and examples.

Table 3–10: Console Commands

Command	Function
BOOT	Initializes the system, causing a self-test, and begins the boot program.
CLEAR EXCEPTION	Cleans up error state in XBER and RCSR registers.
CONTINUE	Begins processing at the address where processing was interrupted by a CTRL/P console command.
DEPOSIT	Stores data in a specified address.
EXAMINE	Displays the contents of a specified address.
FIND	Searches main memory for a page-aligned 256-Kbyte block of good memory or for a restart parameter block.
HALT	Null command, no action is taken since the processor has already halted in order to enter console mode.
HELP	Prints explanation of console commands.
INITIALIZE	Performs a system reset, including self-test.
REPEAT	Executes the command passed as its argument.
RESTORE EEPROM	Copies the TK tape's EEPROM contents to the EEPROM of the processor executing the command.
SAVE EEPROM	Copies to the TK tape the contents of the EEPROM of the processor executing the command.
SET BOOT	Stores a boot command by a nickname.
SET CPU	Specifies eligibility of processors to become the boot processor or whether the vector processor is to be included in the system configuration.

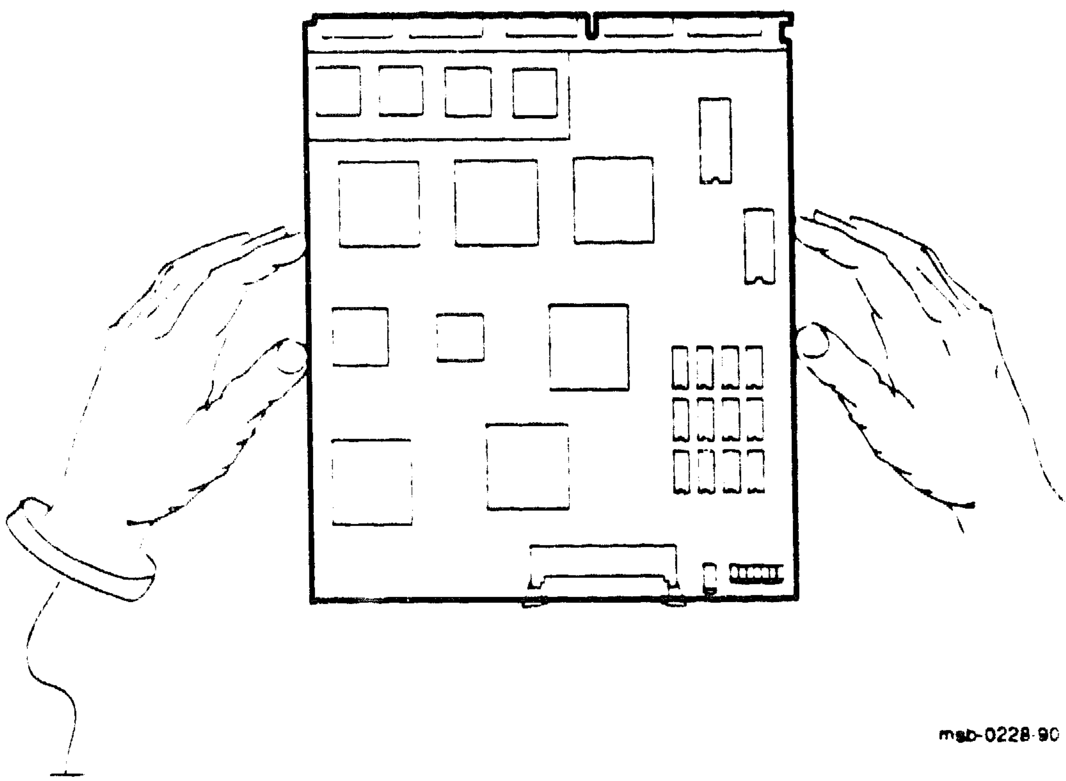
Table 3–10 (Cont.): Console Commands

Command	Function
SET LANGUAGE	Changes the output of the console error messages between numeric code only (international mode) and code plus explanation (English mode).
SET MEMORY	Designates the method of interleaving the memory modules; supersedes the console program's default interleaving.
SET TERMINAL	Sets console terminal characteristics.
SHOW ALL	Displays the current value of parameters set.
SHOW BOOT	Displays all boot commands and nicknames that have been saved using SET BOOT.
SHOW CONFIGURATION	Displays the hardware device type and revision level for each XMI and VAXBI node and indicates self-test status.
SHOW CPU	Identifies the primary processor and the status of other processors.
SHOW ETHERNET	Locates all Ethernet adapters on the system and displays their addresses.
SHOW LANGUAGE	Displays the mode currently set for console error messages, international or English.
SHOW MEMORY	Displays the memory lines from the system self-test, showing interleave and memory size.
SHOW TERMINAL	Displays the baud rate and terminal characteristics functioning on the console terminal.
START	Begins execution of an instruction at the address specified in the command string.
STOP	Halts the specified node.
TEST	Passes control to the self-test diagnostics; /RBD qualifier invokes ROM-based diagnostics.
UPDATE	Copies contents of the EEPROM on the processor executing the command to the EEPROM of another processor.
Z	Logically connects the console terminal to another processor on the XMI bus or to a VAXBI node.
!	Introduces a comment.

3.14 KA64A Handling Procedures

The KA64A module is static sensitive and fragile. The CMOS2 technology used on this module is more vulnerable to static than past technology. The 25 mil leads used to attach chips to the module are very small, close together, and easily bent. Careless handling can easily damage the module. Follow these procedures when handling this module.

Figure 3–8: Holding the KA64A Module



The KA64A module **must** be handled carefully. Figure 3–8 shows the proper way to hold the module. Be sure your hands do not touch any components, leads, or XMI fingers. When inserting it in or removing it from the XMI card cage, grasp the module only at the spot shown in Figure 3–9, avoiding any contact with the 25 mil leads. Do not use any component as a handle.

To avoid damaging the KA64A module, follow these handling procedures:

1. Always wear an antistatic wrist strap.
2. Before removing the module from its ESD box, place the box on a clean, stable surface.

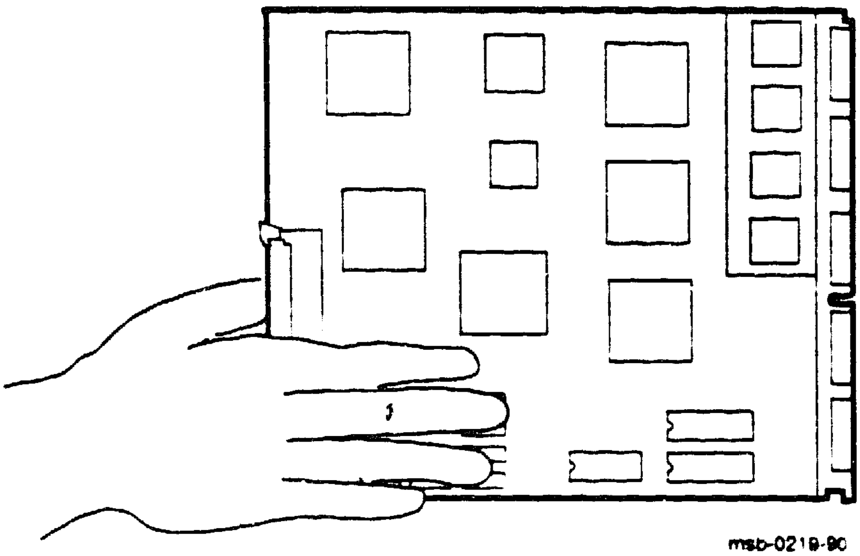
   Be sure the box will not slide or fall. **Never** place the box on the floor. And be sure no tools, papers, manuals, or anything else that might damage the module are near it. Some components on this module can be damaged by a 600-volt static charge; paper, for example, can carry a charge of 1000 volts.
3. Hold the module only by the edges, as shown in Figure 3–8.

   Do not hold the module so that your fingers touch any components or leads. Be sure you do not bend the module as you are holding it.
4. Be sure nothing touches the module surface or any of its components.

   If anything touches the module, components or leads can be damaged. This includes the antistatic wrist strap, clothing, jewelry, cables, components on other modules, and anything in the work area (such as tools, manuals, or loose papers).

   Remove your jacket and roll up your sleeves before handling the module. Also remove any jewelry.

Figure 3–9: Inserting the KA64A Module in an XMI Card Cage



You must take special precautions when inserting the KA64A module in or removing it from the XMI card cage.

1. Be sure, when inserting the module in or removing it from the XMI card cage, that no part of the module comes in contact with another module or a cable.
2. When swapping out a module, place it in an unused XMI slot, if one is available, or set the module on an ESD mat while you install the new module.

   An unused XMI slot is the best place to leave a module that is being swapped out until it can be placed in the ESD box. If there are no extra slots, place the module you removed on an ESD mat on a stable, uncluttered surface, with side 1 (the side with the heat sinks) up. Do not put it on the top of the system cabinet. And never slide the module across any surface. The leads on the components are fragile and can be damaged by contact with fingers or any surface.
3. Hold the XMI card cage handle while removing or inserting the module.

   If it is not held in place, the handle can spring down and damage the module.
4. When inserting the module in the card cage, grasp it as shown in Figure 3–9, and slide it slowly and gently into the slot.
5. **Do not attach the repair tag to the module.**

   Place the repair tag in the plastic bag attached to the bottom of the ESD box. Allowing the repair tag to come in contact with the module can cause damage to a component.

3.15 How to Replace the Only Processor

When replacing the processor module in a single-processor system, you must RESTORE the EEPROM image previously saved on a TK tape. This ensures a correct EEPROM image in the new processor.

CAUTION: *Special care must be taken when handling a KA64A module. Review Section 3.14 before replacing this module.*

Example 3–8: Replacing a Single Processor

```
#123456789 0123456789 0123456789 01234567#

F   E   D   C   B   A   9   8   7   6   5   4   3   2   1   0   NODE #

    A   A           M   M   .   .   .   .   .   .   .   P       TYP 6
    C   C           +   +   .   .   .   .   .   .   .   +       STF 7
    .   .   .   .   .   .   .   .   .   .   .   .   .   B       BPD
    .   .   .   .   .   .   .   .   .   .   .   .   .   +       ETF 7
    .   .   .   .   .   .   .   .   .   .   .   .   .   B       BPD

.   .   .   .   .   .   .   .   .   +   +   .   +   .   +   .   XBI D +
.   .   .   .   .   .   .   .   .   +   .   +   .   +   +   .   XBI E +

    .   .   .   .   A2  A1  .   .   .   .   .   .   .   .       ILV
    .   .   .   .   32  32  .   .   .   .   .   .   .   .       64 Mb

ROM0 = V1.00   ROM1 = V1.00   EEPROM = 1.00/1.01   SN = 0000000000

?4F System serial number has not been initialized
>>> RESTORE EEPROM 10
?6E EEPROM Revision = 1.00/1.01

?7C Tape image Revision = 1.00/1.01

Proceed with EEPROM update (Y or N) >>> Y
?6A EEPROM changed successfully.

!optional - may need latest console/diag patches again 11
>>> PATCH EEPROM

>>> BOOT 14
```

1. Turn the upper key switch straight up to the Off position (0).

   CAUTION: *See Section 3.14 for KA64A module handling procedures.*

2. Remove the defective processor module and temporarily insert it in an unused XMI slot or place it on an ESD mat.
3. Remove the new processor module from the ESD box and insert it in the XMI card cage. Place the old processor module in the ESD box.
4. Turn the lower key switch to Halt.
5. Turn the upper key switch to Enable.
6. Check the self-test display for the processor, indicated by a P on the TYP line (usually in slot 1). See ❻ in Example 3–8.
7. If the processor shows a plus sign (+) on both lines STF and ETF, it passed self-test.
8. Turn the lower key switch to Update.
9. Mount the TK cartridge containing the most recent saved image of the old processor's EEPROM.[1]
10. Issue the console command RESTORE EEPROM. See ❿. The EEPROM revision and tape image revision are displayed, and you are asked if you wish to proceed with the EEPROM update.
11. If any patches had been issued since the last save mount the TK cartridge containing the patches. See ⓫. If the EEPROM has already been patched to the latest revision, go to step 14. For more information about the PATCH command, see Section 3.18.
12. Issue the console command PATCH EEPROM. The patch operation takes approximately 5 minutes.
13. Turn the lower key switch to the Auto Start position.
14. Boot the operating system by issuing the BOOT command. See ⓬.

---

[1] When the system was originally installed, customer service saved the EEPROM on a TK cartridge. (See *VAX 6000–400 Installation Guide*.) The cartridge was left in the care of the customer. Subsequently, the EEPROM might have been changed, then saved, several times. This would normally be the case following a PATCH operation.

If you do not have a tape, set the console terminal to 1200 baud, and then set the system serial number in the new processor as follows:

```
>>> [ESC] (or [CTRL/3]) [DEL] SET SYSTEM SERIAL [RET]
 Enter system serial number? aannnnnnnn [RET]
UPDATE EEPROM? (Y or N) >>> Y [RET]
```

3.17 How to Replace the Boot Processor

The boot processor is indicated by the letter B on the self-test BPD line (slot 1 in Example 3–9). If they have the same version ROMs, you can update the new processor's EEPROM from one of the secondaries.

CAUTION: *Special care must be taken when handling a KA64A module. Review Section 3.15 before replacing this module.*

Example 3–9: Replacing Boot Processor

```
#123456789 0123456789 0123456789 01234567#

F   E   D   C   B   A   9   8   7   6   5   4   3   2   1   0   NODE #

    A   A   .   .   M   M   M   M   .   .   P   P   P   P       TYP ⑥
    o   c   .   .   +   +   +   +   .   .   +   +   +   +       STF ⑦
    .   .   .   .   .   .   .   .   .   .   E   D   E   B       BPD
    .   .   .   .   .   .   .   .   .   .   +   +   +   +       ETF ⑦
    .   .   .   .   .   .   .   .   .   .   E   D   E   B       BPD

.   .   .   .   .   .   .   .   .   +   +   .   +   .   +   .   XBI D +
.   .   .   .   .   .   .   .   .   +   .   +   .   +   +   .   XBI E +

    .   .   .   .   A4  A3  A2  A1  .   .   .   .   .   .       ILV
    .   .   .   .   32  32  32  32  .   .   .   .   .   .       128Mb

ROM0 = V1.00   ROM1 = V1.00   EEPROM = 1.00/1.00   SN = SG01234567

>>> SET CPU/NOPRIMARY 1⑩
>>> SHOW CPU
  Current Primary: 1
  /NOENABLED-
  /NOPRIMARY- 1

>>> SET CPU 2⑪
>>> SHOW CPU
  Current Primary: 2
  /NOENABLED-
  /NOPRIMARY- 1

>>> UPDATE 1⑬
```

1. Turn the upper key switch straight up to the Off position (0).

   CAUTION: *See Section 3.15 for KA64A module handling procedures.*

2. Remove the defective processor module and set it on a static pad.

3. Remove the new processor module from the ESD box and insert it in the XMI card cage. Place the old processor module in the ESD box.

4. Turn the lower key switch to Halt.

5. Turn the upper key switch to Enable.

6. Check the self-test display for the new processor, indicated by a P on the TYP line (usually in slot 1). See ❻ in Example 3–9.

7. If the processor shows a plus sign (+) on both lines STF and ETF, it passed self-test. See ❼.

8. You will see the following message:

```
?50 System serial number not initialized on primary processor
```

9. If you see the error message ?52, the new module will not be able to function as the boot processor. If you don't see this error message, go to step 11.

10. Make the new module ineligible to be boot processor—use the console command SET CPU/NOPRIMARY. See ❿. The new processor will operate as a secondary processor without problems, but you may continue to see error messages ?2D, ?52, and ?54 when the system is powered on or booted.

    CAUTION: *As long as its ROM is out of revision, do not issue the command UPDATE to the new module. Issuing the UPDATE command will disable the EEPROM.*

    Go to step 15.

11. Make one of the secondary processors the boot processor temporarily, because the UPDATE command copies the boot processor's EEPROM. Then you can update the new processor. This command immediately makes the processor at node 2 the boot processor: SET CPU 2. See ⓫.

12. Turn the lower key switch to Update.

13. Now update the EEPROM of the new module from the temporary boot processor, using the UPDATE command. See ⓭.

14. Turn the lower key switch to the Auto Start position.

15. Press the Restart button.

3.18 How to Add a New Processor or Replace a Secondary Processor

Add a new secondary processor in a slot to the left of the boot processor.

CAUTION: *Special care must be taken when handling a KA64A module. Review Section 3.15 before replacing this module.*

Example 3–10: Adding or Replacing Secondary Processor

```
#123456789 0123456789 0123456789 01234567#

F  E  D  C  B  A  9  8  7  6  5  4  3  2  1  0  NODE #

   A  A  .  .  M  M  M  M  .  .  P  P  P  P     TYP❺
   o  o  .  .  +  +  +  +  .  .  +  +  +  +     STF❻
   .  .  .  .  .  .  .  .  .  .  E  D  E  B     BPD
   .  .  .  .  .  .  .  .  .  .  +  +  +  +     ETF❻
   .  .  .  .  .  .  .  .  .  .  E  D  E  B     BPD

.  .  .  .  .  .  .  .  .  +  +  .  +  .  +  .  XBI D +
.  .  .  .  .  .  .  .  .  +  .  +  .  +  +  .  XBI E +

   .  .  .  .  A4 A3 A2 A1 .  .  .  .  .  .     ILV
   .  .  .  .  32 32 32 32 .  .  .  .  .  .     128Mb

ROM0 = V1.00  ROM1 = V1.00  EEPROM = 1.00/1.00❾  SN = SG01234567

>>> SET CPU/NOPRIMARY 3❽
>>> SHOW CPU
  Current Primary: 1
  /NOENABLED-
  /NOPRIMARY- 3

>>> UPDATE 3⓫
```

1. Turn the upper key switch straight up to the Off position (0).

   CAUTION: *You must wear an antistatic wrist strap attached to the cabinet when you handle any modules.*

2. Either remove the defective secondary processor module, or find an empty slot where you can add the new processor. If you are removing a defective module, temporarily insert it in an unused slot.

3. Remove the new processor module from the ESD box and insert it in the XMI card cage. If you are replacing a processor module, place the old module in the ESD box.
4. Turn the lower key switch to Halt and the upper key switch to Enable.
5. Check the self-test display for the new processor, indicated by a P on the TYP line (in this example: slot 3). See ❺ in Example 3–10.)
6. If the processor shows a plus sign (+) on both lines STF and ETF, it passed self-test. See ❻.
7. If you see the error messages ?2D and ?52, the new module will not be able to function as the boot processor. If you don't see these error messages, go to step 9.
8. Make the new module ineligible to be boot processor—use the console command SET CPU/NOPRIMARY. See ❽. The new processor will operate as a secondary processor without problems, but you may continue to see error messages ?2D, ?52, and ?54 when the system is powered on or booted.

   CAUTION: *As long as its ROM is out of revision, do not issue the command UPDATE to the new module. Issuing the UPDATE command will disable the EEPROM. Revision 1.0 and revision 2.0 ROMs are incompatible. Kit #A2-01456-10 has revision 2 ROMs and upgrading procedures that need to be followed.*

   Go to step 13.
9. If you see error messages ?2D and ?54, compare the EEPROM revision numbers of the secondary processor and boot processor (second number in the EEPROM = X/Y field on the bottom line of self-test display). See ❾.

   If the new secondary processor has a *higher* revision number than the boot processor, PATCH the boot processor's EEPROM (see Section 3.18).
10. Turn the lower key switch to Update.
11. Now update the EEPROM of the new module. See ⓫.
12. Turn the lower key switch to the Auto Start position.
13. Press the Restart button.

3.18 PATCH EEPROM Command

The PATCH EEPROM command is a console command used by field service to update console and ROM diagnostics when new revisions are issued.

Example 3–11: PATCH EEPROM Command

```
>>> SAVE EEPROM❶

>>> PATCH EEPROM❺

>>> UPDATE ALL❻

>>> INITIALIZE❼

#123456789 0123456789 0123456789 01234567#

F   E   D   C   B   A   9   8   7   6   5   4   3   2   1   0   NODE #

    A   A   .   .   M   M   M   M   .   .   P   P   P   P       TYP
    O   C   .   .   +   +   +   +   .   .   +   +   +   +       STF
    .   .   .   .   .   .   .   .   .   .   E   D   E   B       BPD
        .   .   .   .   .   .   .   .   .   +   +   +   +       ETF
    .   .   .   .   .   .   .   .   .   .   E   D   E   B       BPD

.   .   .       .   .   .   .   .   +   +   .   +   .   +   .   XBI D +
.   .   .   .   .   .   .   .   .   +   .   +   .   +   +   .   XBI E +

    .   .       .   A4  A3  A2  A1  .   .   .   .   .   .       ILV
    .   .   .   .   32  32  32  32  .   .   .   .   .   .       128Mb

ROM0 = V1.00  ROM1 = V1.00  EEPROM = 1.00/1.01❽  SN = SG01234567

>>> SAVE EEPROM❿
>>>
```

1. Load a tape cartridge into the TK70 drive and queue it to the beginning. Save the current contents of the boot processor's EEPROM to tape using the SAVE EEPROM command. See ❶ in Example 3-11. Mark this tape for use only with this system. See Chapter 5 of the *VAX 6000-400 Owner's Manual* for more information on the SAVE EEPROM command.
2. Halt all processors and enter console mode.
3. Load the new EEPROM patch tape into the TK tape drive.
4. Queue the tape to the beginning by pressing the load/unload pushbutton. (See Appendix A of the *VAX 6000-400 Owner's Manual* for details on using the TK tape drive.)
5. Enter the PATCH EEPROM command. See ❺. Wait approximately 5 minutes for the patch to complete. You receive the console prompt back when the patch is complete.
6. If the system is a multiprocessor system, run UPDATE ALL to copy the new patch information to the secondary processors. See ❻. The time for UPDATE ALL to execute varies with the number of processors; the operation takes approximately 4 minutes for each secondary processor.
7. Reset the system by pushing the Restart button on the control panel or by entering the INITIALIZE command. See ❼.
8. Check the summary line of the self-test. The EEPROM information indicates first the starting revision number of the EEPROM for this system, followed by a slash, and the current revision number of the EEPROM for the processors. See ❽.
9. If the revision numbers on all processors do not match, the system prints out the most current revision number of the EEPROM data and gives an error message indicating that the EEPROM code does not match. (See Section 3.17.)
10. Save the updated contents to tape, using the SAVE EEPROM command. See ❿.

3.19 KA64A Registers

The KA64A registers consist of the processor status longword, internal processor registers, KA64A registers in XMI private space, XMI required registers, and 16 general purpose registers.

Table 3–11: KA64A Internal Processor Registers

Register	Mnemonic	Address	Type	Class
Kernel Stack Pointer	KSP	IPR0	R/W	1
Executive Stack Pointer	ESP	IPR1	R/W	1
Supervisor Stack Pointer	SSP	IPR2	R/W	1
User Stack Pointer	USP	IPR3	R/W	1
Interrupt Stack Pointer	ISP	IPR4	R/W	1
Reserved		IPR5–IPR7		3
P0 Base	P0BR	IPR8	R/W	1
P0 Length	P0LR	IPR9	R/W	1
P1 Base	P1BR	IPR10	R/W	1
P1 Length	P1LR	IPR11	R/W	1

Key to Types:

R–Read
W–Write
R/W–Read/write

Key to Classes:

1–Implemented by the KA64A (as specified in the *VAX Architecture Reference Manual*).
2–Implemented uniquely by the KA64A.
3–Not implemented. Read as zero; NOP on write.
4–Access not allowed; accesses result in a reserved operand fault.
5–Accessible, but not fully implemented; accesses yield UNPREDICTABLE results.
6–Implemented by the FV64A vector module.
I–The register is initialized on KA64A reset (power-up, system reset, and node reset).

Table 3–11 (Cont.): KA64A Internal Processor Registers

Register	Mnemonic	Address	Type	Class
System Base	SBR	IPR12	R/W	1
System Length	SLR	IPR13	R/W	1
Reserved		IPR14–IPR15		3
Process Control Block Base	PCBB	IPR16	R/W	1
System Control Block Base	SCBB	IPR17	R/W	1
Interrupt Priority Level	IPL	IPR18	R/W	1 I
AST Level	ASTLVL	IPR19	R/W	1 I
Software Interrupt Request	SIRR	IPR20	W	1
Software Interrupt Summary	SISR	IPR21	R/W	1 I
Reserved		IPR22–IPR23		3
Interval Counter Control and Status	ICCS	IPR24	R/W	2 I
Reserved		IPR25–IPR26		3
Time-of-Year Clock	TODR	IPR27	R/W	1
Console Storage Receiver Status	CSRS	IPR28	R/W	5 I
Console Storage Receiver Data	CSRD	IPR29	R	5 I
Console Storage Transmitter Status	CSTS	IPR30	R/W	5 I
Console Storage Transmitter Data	CSTD	IPR31	W	5 I
Console Receiver Control/Status	RXCS	IPR32	R/W	2 I
Console Receiver Data Buffer	RXDB	IPR33	R	2 I
Console Transmitter Control/Status	TXCS	IPR34	R/W	2 I
Console Transmitter Data Buffer	TXDB	IPR35	W	2 I
Reserved		IPR36–IPR37		3
Machine Check Error Summary	MCESR	IPR38	W	2
Reserved		IPR39		3
Accelerator Control and Status	ACCS	IPR40	R/W	2 I
Reserved		IPR41		3
Console Saved PC	SAVPC	IPR42	R	2

Table 3–11 (Cont.): KA64A Internal Processor Registers

Register	Mnemonic	Address	Type	Class
Console Saved PSL	SAVPSL	IPR43	R	2
Reserved		IPR44–IPR46		3
Translation Buffer Tag	TBTAG	IPR47	W	2
Reserved		IPR48–IPR54		3
I/O Reset	IORESET	IPR55	W	2
Memory Management Enable	MAPEN	IPR56	R/W	1 I
Translation Buffer Invalidate All	TBIA	IPR57	W	1
Translation Buffer Invalidate Single	TBIS	IPR58	W	1
Translation Buffer Data	TBDATA	IPR59	W	2
Reserved		IPR60–IPR61		3
System Identification	SID	IPR62	R	1
Translation Buffer Check	TBCHK	IPR63	W	1
Reserved		IPR64–IPR111		3
Backup Cache Reserved	BC112	IPR112	R/W	5
Backup Cache Tag Store	BCBTS	IPR113	R/W	2
Backup Cache P1 Tag Store	BCP1TS	IPR114	R/W	2
Backup Cache P2 Tag Store	BCP2TS	IPR115	R/W	2
Backup Cache Refresh	BCRFR	IPR116	R/W	2
Backup Cache Index	BCIDX	IPR117	R/W	2
Backup Cache Status	BCSTS	IPR118	R/W	2 I
Backup Cache Control	BCCTL	IPR119	R/W	2 I
Backup Cache Error	BCERR	IPR120	R	2
Backup Cache Flush Backup Tag Store	BCFBTS	IPR121	W	2
Backup Cache Flush Primary Tag Store	BCFPTS	IPR122	W	2
Reserved		IPR123		2
Vector Interface Error Status	VINTSR	IPR123	R/W	2

Table 3–11 (Cont.): KA64A Internal Processor Registers

Register	Mnemonic	Address	Type	Class
Primary Cache Tag Store	PCTAG	IPR124	R/W	2
Primary Cache Index	PCIDX	IPR125	R/W	2
Primary Cache Error Address	PCERR	IPR126	R/W	2
Primary Cache Status	PCSTS	IPR127	R/W	2 1
Reserved		IPR128–IPR143		3
Vector Processor Status	VPSR	IPR144	R/W	6
Vector Arithmetic Exception	VAER	IPR145	R	6
Vector Memory Activity Check	VMAC	IPR146	R	6
Vector Translation Buffer Invalidate All	VTBIA	IPR147	W	6
Reserved		IPR148–IPR156		5
Vector Indirect Register Address	VIADR	IPR157	R/W	6
Vector Indirect Data Low	VIDLO	IPR158	R/W	6
Vector Indirect Data High	VIDHI	IPR159	R/W	6

The IPRs are explicitly accessible to software only by the Move To Processor Register (MTPR) and Move From Processor Register (MFPR) instructions, which require kernel mode privileges From the console, EXAMINE/I and DEPOSIT/I commands read and write the IPRs.

Table 3–12: XMI Registers for the KA64A

Register	Mnemonic	Address
XMI Device	XDEV	BB + 00
XMI Bus Error	XBER	BB + 04
XMI Failing Address	XFADR	BB + 08
XMI GPR	XGPR	BB + 0C
KA64A Control and Status	RCSR	BB + 10

Note: "BB" = base address of an XMI node, which is the address of the first location in nodespace.

Table 3–13: KA64A Registers in XMI Private Space

Register	Mnemonic	Address
Control Register Write Enable	CREGWE	2000 0000
Console ROM (halt protected)		2004 0000 to 2007 FFFF
Console EEPROM (halt protected)		2008 0000 to 2008 7FFF
Console ROM (not halt protected)		200C 0000 to 200F FFFF
Console EEPROM (not halt protected)		2010 0000 to 2010 7FFF
RSSC Base Address	SSCBAR	2014 0000
RSSC Configuration	SSCCNR	2014 0010
RSSC Bus Timeout Control	SSCBTR	2014 0020
RSSC Output Port	OPORT	2014 0030
RSSC Input Port	IPORT	2014 0040
Control Register Base Address	CRBADR	2014 0130
Control Register Address Decode Mask	CRADMR	2014 0134
EEPROM Base Address	EEBADR	2014 0140
EEPROM Address Decode Mask	EEADMR	2014 0144
Timer 0 Control	TCR0	2014 0160
Timer 0 Interval	TIR0	2014 0164
Timer 0 Next Interval	TNIR0	2014 0168
Timer 0 Interrupt Vector	TIVR0	2014 016C
Timer 1 Control	TCR1	2014 0170
Timer 1 Interval	TIR1	2014 0174
Timer 1 Next Interval	TNIR1	2014 0178
Timer 1 Interrupt Vector	TIVR1	2014 017C
RSSC Interval Counter	SSCICR	2014 01F8
RSSC Internal RAM		2014 0400 to 2014 07FF
IP IVINTR Generation	IPINTR	2101 0000 to 2101 FFFF
WE IVINTR Generation	WEINTR	2102 0000 to 2102 FFFF

CHAPTER 4

Chapter 4

FV64A Vector Processor

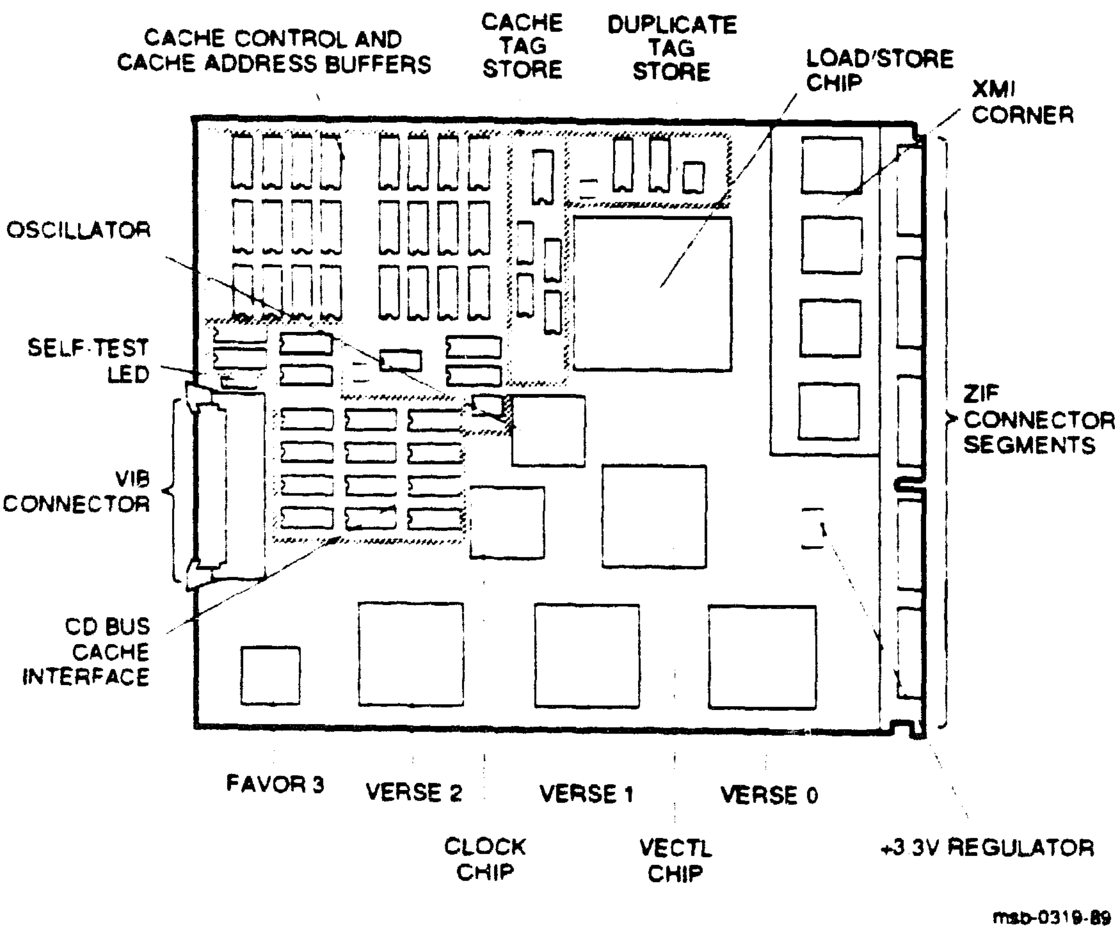
This chapter contains the following sections:

- FV64A Physical Description and Specifications
- KA64A/FV64A Coprocessors
- FV64A Configuration Rules
- Functional Description
- Self-Test Results: Console Display and Self-Test LED
- Self-Test Results: Scalar XGPR Register
- Vector Processor Tests—RBD 0 and RBD 1
- VAX/DS Diagnostics
- Machine Checks
- Vector Console Commands
- FV64A Handling Procedures
- How to Replace a Vector Module
- Vector Processor Registers

4.1 FV64A Physical Description and Specifications

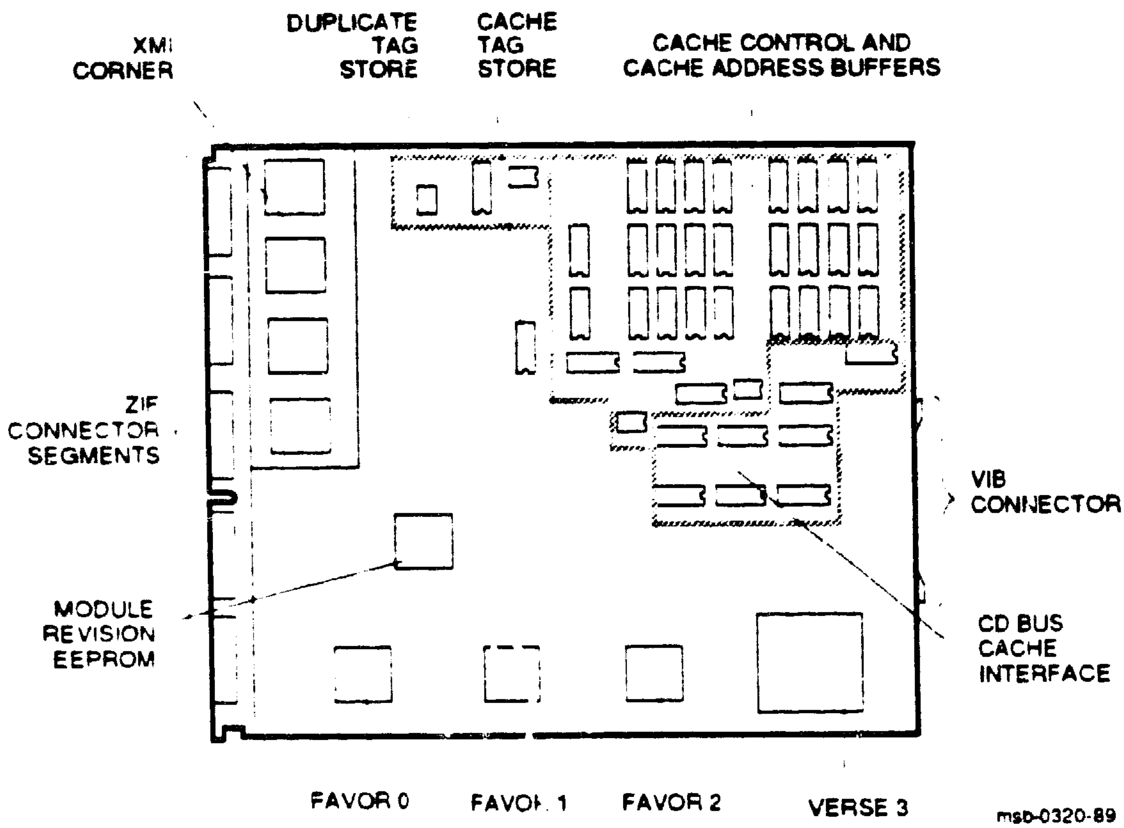
The FV64A is a vector processor used with the KA64A scalar processor. The module designation is T2017. The two processor modules are connected with a VIB cable. Figure 4–1 shows side 1 of the module, and Figure 4–2 shows side 2.

Figure 4–1: FV64A Module (Side 1)



Because the vector module has components on side 2, only memory modules can be installed next to side 2 (see Figure 4–2).

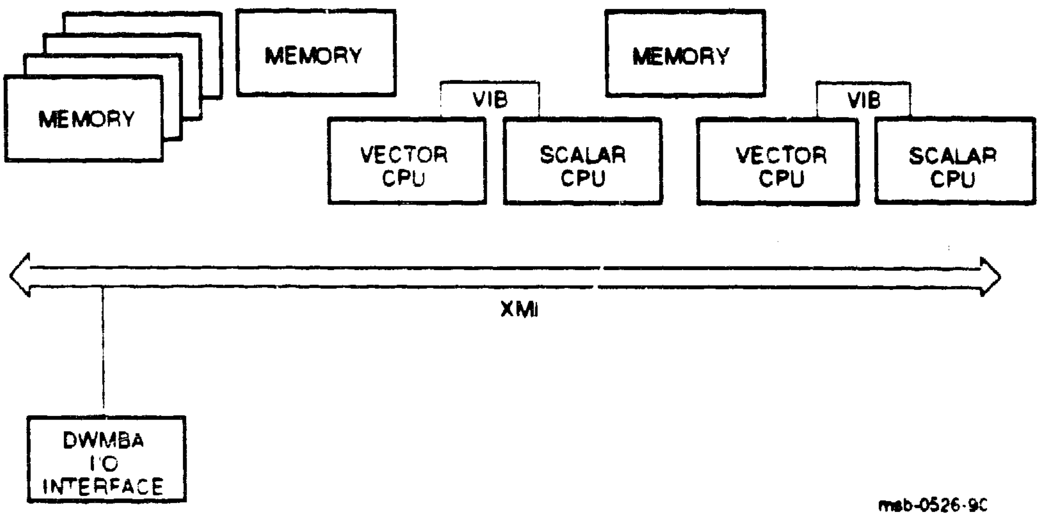
Figure 4–2: FV64A Module (Side 2)



4.2 KA64A/FV64A Coprocessors

The VAX 6000–400 uses a high-speed system bus, called the XMI bus, to interconnect its processors and its memory modules. In Figure 4–3 all I/O devices connect to the VAXBI bus. The VAX 6000–400 supports multiprocessing with up to six scalar processors or one or two scalar/vector pairs.

Figure 4–3: VAX 6000–400 Vector Processing System



NOTE: *Installation of an FV64A vector processor requires that the* ***attached*** *KA64A module (T2015) be at a minimum revision of K. In addition, the ROMs on any additional KA64A modules must be at a minimum revision of V2.0 (ROM 0 and ROM 1).*

Table 4–1: FV64A Specifications

Parameter	Description
Module Number:	T2017
Dimensions:	23.3 cm (9.2") H x 0.6 cm (0.25") W x 28.0 cm (11.0") D
Temperature:	
Storage Range	-40°C to 66°C (-40°F to 151°F)
Operating Range	5°C to 50°C (41°F to 122°F)
Relative Humidity:	
Storage	10% to 95% noncondensing
Operating	10% to 95% noncondensing
Altitude:	
Storage	Up to 4.8 km (16,000 ft)
Operating	Up to 2.4 km (8000 ft)
Current:	14A at +5V 0.20A at +5VBB
Power:	70W
Cables:	VIB cable, 17-02240-03
Diagnostics:	ROM-based diagnostics 0 and 1. VAX/DS diagnostics, see Section 4.8.

The FV64A vector processor is an integrated vector processor; that is, the vector processor module performs as a coprocessor that is tightly coupled with a host scalar processor. The two processors are physically connected by an intermodule cable, the VIB. The scalar processor is specifically designed to support its vector coprocessor, and the vector instruction set is implemented as part of the host native instruction set. Both the scalar and vector processors are on the XMI bus, and they share a common memory.

A VAX 6000 Model 400 system can have one or two scalar/vector pairs. If the system has only one pair, it can also have additional scalar processors. For optimal performance, two memory modules are required for one scalar/vector pair, and four memory modules are required for two scalar/vector pairs.

4.3 FV64A Configuration Rules

A vector processor must be installed to the left of its companion scalar processor. An intermodule cable connects the two modules. A memory module or an empty slot must be to the left of the vector processor. Any other configuration may damage the vector module.

Figure 4–4: Scalar/Vector Configurations

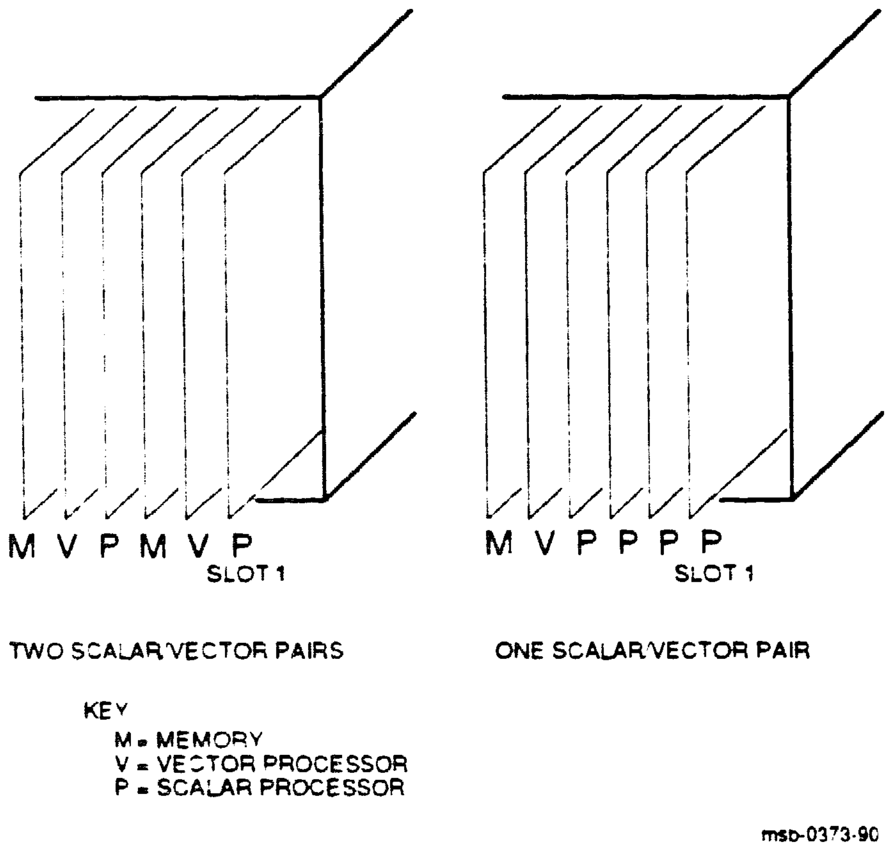


Table 4–2 shows the maximum number of scalar and vector processors supported in a VAX 6000 system.

Table 4–2: Processor Module Combinations

Maximum CPUs	Maximum Vectors	Configuration (Slot 1 at Right)
6	0	P P P P P P
4	1	M V P P P P
2	2	M V P M V P

Figure 4–4 shows system configurations for a VAX 6000 Model 400 system with one or two vector processors. The diagram on the left indicates the configuration for two scalar/vector pairs (V- -P) with a memory module in the slot to the left of the vector processor. The diagram on the right shows a single scalar/vector pair with additional scalar processors.

Typically, processors are placed in the right XMI slots, beginning with slot 1 and extending to slot 6. Memories are placed in the middle slots, from slot A to slot 5 and then slots B and C, and VAXBI adapters are installed in the left side of the card cage, beginning with slot E. However, in a system with a vector processor, the modules should be installed as shown in Figure 4–4. These configurations must be followed to avoid damage to the modules and for performance reasons:

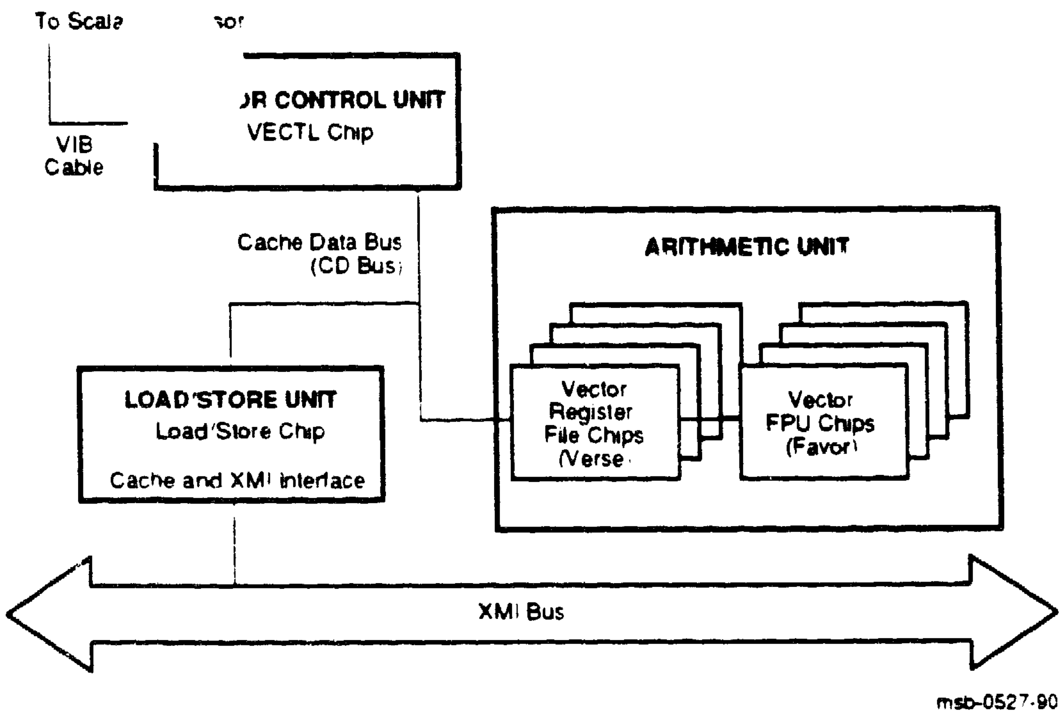
- Because the FV64A module has VLSI components with heat sinks protruding from both sides, only a memory module, with its low components, can be placed next to side 2 of the FV64A.
- In a system with one scalar/vector pair and one or more additional scalar processors, the scalar processor of the pair should be prevented from being the boot processor for performance reasons.

  If the scalar/vector pair is to the left of other scalar processors, then the processor of the scalar/vector pair will not become the boot processor unless other processors fail self-test or have been disabled with the SET CPU console command. Alternatively, you can issue the SET CPU/NOPRIMARY command and give the node number of the attached scalar processor that you do not want to be the boot processor.

4.4 Functional Description

Figure 4–5 shows the three main functional units of the FV64A processor: the vector control unit, the arithmetic unit, and the load/store unit, which includes the XMI interface and cache control.

Figure 4–5: FV64A Block Diagram



The FV64A is an integrated vector processor, tightly coupled to the KA64A scalar processor. The vector instructions are issued from the scalar processor, and the vector processor then dispatches them internally. All communication between the scalar and vector modules takes place across the intermodule VIB cable. All communication with memory is over the XMI bus.

The vector processor has 16 vector data registers, each 64 quadwords long. There is a 1-megabyte direct-mapped cache and a 136-entry translation buffer.

The FV64A is an XMI module with the standard XMI Corner. The module has a cable connector at the rear edge of the module that connects to the rear edge of a KA64A module. The instructions are issued over the VIB bus and pass to the VECTL chip, which then controls the operations on the module. It passes instructions to the load/store unit over the CD bus. The load/store unit then issues XMI memory transactions. The VECTL chip also issues instructions to the four pairs of Verse and Favor chips that make up the arithmetic unit. The vector data registers are in the Verse chips. The Favor chips perform the arithmetic operations on the data held in the Verse chips.

The vector processor module uses the standard XMI Corner interface, but it functions only as an XMI commander. The vector processor does not issue transactions to I/O space, nor does it respond to XMI transactions directed to it. All error reporting is done by the scalar processor.

4.5 Self-Test Results: Console Display and Self-Test LED

You can check the vector processor self-test results in three ways: the self-test display if the vector is attached to the processor in node 1, the yellow self-test LED on the FV64A module, and the contents of the XGPR register of the attached KA64A module. If self-test passes, the large yellow LED on the vector module lights. If the vector module fails self-test, the light remains unlit.

Example 4–1: Self-Test Results

```
#123456789 0123456789 0123456789 0123456789 0123456789 # ❶

F   E   D   C   B   A   9   8   7   6   5   4   3   2   1   0   NODE #

    A   A   .   .   M   M   .   .   M   V-  -P  M   V-  -P      TYP ❷
    o   o   .   .   +   +   .   .   +   +   +   +   +   +       STF ❸
    .   .   .   .   .   .   .   .   .   D   E   .   E   B       BPD ❹
    .   .   .   .   .   .   .   .   .   +   +   +   +   +       ETF ❺
    .   .   .   .   .   .   .   .   .   D   E   .   E   B       BPD ❻

.   .   .   .   .   .   .   .   .   +   +   +   +   .   +   .   XBI D +
.   .   .   .   .   .   .   .   .   +   .   +   .   +   +   .   XBI E +

    .   .   .   .   A4  A3  .   .   A2  .   .   A1  .   .       ILV
    .   .   .   .   32  32  .   .   32  .   .   32  .   .       128Mb

ROM0 = V2.00  ROM1 = V2.00  EEPROM = 2.00/2.00  SN = SG01234567 ❼
>>>
```

Example 4–1 shows the self-test results for a system with two scalar/vector pairs. Each KA64A runs its self-test and then tests any attached vector processor.

❶ The first line of the self-test printout is the progress trace. This line shows the self-test progress of the KA64A in node 1 (the baud rate must be at least 1200). The numbers correspond to tests in the system self-test. If there is an attached vector processor module and self-test passes, the line prints as in Example 4–1 ending with #. If there is no attached vector processor, testing stops after the first 37 tests. If a test fails, the failing test number is the last one printed. For example, if test 14 fails, the line is printed as follows:

```
#123456789 01234
```

❷ This line indicates the type (TYP) of module at each XMI node. Scalar processors are type P, and vector processors are type V. The dashes indicate that the scalar processors are attached to the adjacent vector processors.

❸ This line shows self-test fail status (STF), which are the results of on-board self-test. Possible values for processors are:

+ (pass)
– (fail)

All processors passed self-test in this example. [1]

❹ The BPD line indicates boot processor designation and whether vector processors are enabled or disabled. When the system completes on-board self-test, the scalar processor with the lowest XMI ID number that passes self-test and is eligible is selected as boot processor — in this example, the processor at node 1.

The results on the BPD line indicate:

- The boot processor (B)
- Scalar processors eligible (E) or ineligible (D) to become the boot processor
- Vector processors enabled (E) or disabled (D)

In this example the vector processor attached to the scalar processor at node 4 has been disabled. A vector processor can be disabled by the SET CPU/NOVECTOR_ENABLED command.

❺ During extended test (ETF) all processors run additional tests, which include reading and writing memory and using the cache. On line ETF, results are reported for each processor in the same way as on line STF—a plus sign indicates that extended test passed and a minus sign that extended test failed.

❻ Another BPD line is displayed, because it is possible for a different CPU to be designated boot processor if the processor first designated as the boot processor fails the extended testing.

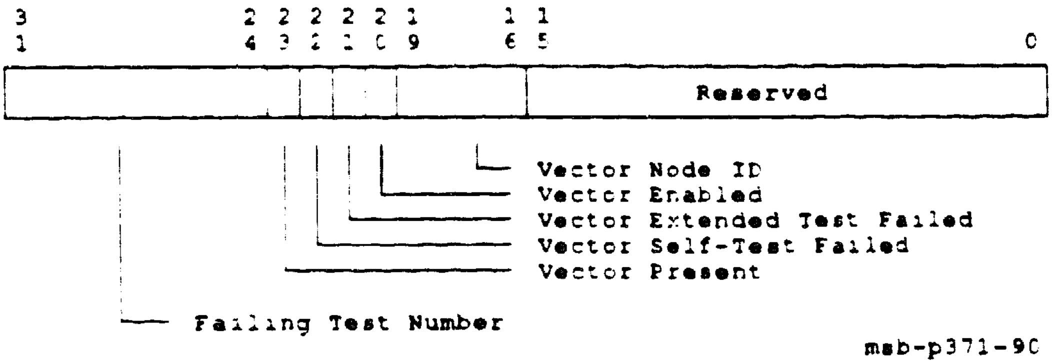
❼ The last line of the self-test display shows the ROM and EEPROM version numbers and the system serial number. Version 2 or greater ROMs and EEPROMs are required to support vector processors.

[1] If a revision J scalar processor has an attached vector module, the vector will be disabled, and this error message is displayed: ?7D Vector module is disabled–check KA64A revision at node *n*. The *attached* scalar module (T2015) must be at a minimum revision of K. In addition, the ROMs on any other KA64A modules must be at a minimum revision of V2.0.

4.6 Self-Test Results: Scalar XGPR Register

You can check self-test results in the self-test display or in the XGPR register. The failing test number is left in the upper byte of the XGPR register of the failing KA64A processor.

Figure 4–6: XGPR Register



Example 4–2: XGPR Register After Power-Up Test Failure

```
>>> E/P L 2188000C              ! Examine the longword at physical address
                                ! 2188000C, the address of the XGPR
2188000C   45F0xxxx             ! register of the processor in slot 1.
                                ! The result indicates that test 45 of
                                ! self-test failed (Load/Store Cache test).
```

Figure 4–6 shows the XGPR register of the scalar processor. Bit <23>, when set, indicates that there is a vector processor attached to this processor. Bits <22:16> give status on an attached vector processor.

The failing test number is derived from the upper byte (bits <31:24>) of the longword returned. For self-test, the upper byte contains the failing test number. If CPU/memory interaction test fails, this byte contains the failing test number plus 49. If DWMBA test fails, bit <31> is set (making the first digit 8 through A), and bits <30:24> contain the failing test number. All numbers are expressed in binary-coded decimal (BCD). See Table 4–3.

As shown in Example 4–2, you can examine the XGPR register of the failing node to determine the failing test number. See Table 3–3 to determine the base address (BB) of the KA64A processor's node. Then calculate the address of the XGPR register by adding 0C (hex) to the base address.

Table 4–3: Interpreting XGPR Failing Test Numbers

Failing Diagnostic	XGPR <31>	XGPR <30:24> (BCD)	Test Numbers
Self-test	Clear	1–49	1–49
CPU/memory interaction test	Clear	50–66	1–17
Additional memory	Clear	67–73	3
DWMBA test	Set	1–26	1–26

4.7 Vector Processor Tests—RBD 0 and RBD 1

T0038 through T0049 of RBD 0 test the vector processor during self-test. Tests 14–17 of RBD 1 test the vector processor during CPU/memory testing.

Example 4–3: Running RBD 0 on a Secondary Processor with an Attached Vector Processor

```
>>> SET CPU 4 ❶
>>> T/R
RBD4> STC/TR ❷

;XPP/V_ST      2.00

; T0001  T0002  T0003  T0004  T0005  T0006  T0007  T0008  T0009  T0010
; T0011  T0012  T0013  T0014  T0015  T0016  T0017  T0018  T0019  T0020
; T0021  T0022  T0023  T0024  T0025  T0026  T0027  T0028  T0029  T0030
; T0031  T0032  T0033  T0034  T0035  T0036  T0037  T0038  T0039  T0040
; T0041  T0042  T0043  T0044  T0045  T0046  T0047  T0048  T0049

;        P         2     8082        1
;0000000C 00000000 0000000C 0000000C 0000000C 00000000 00000000
```

In Example 4–3:

❶ This command causes the KA64A module at node 4 to become the primary processor.

❷ The prompt indicates that the CPU at node 4 is the primary processor. RBD 0 is run on the scalar/vector processor pair at node 4.

Table 4–4: Vector Processor Tests in Self-Test—RBD 0

Test	Function
T0038	VECTL Registers Test
T0039	Verse Registers Test
T0040	Load/Store Registers Test
T0041	VIB Error Logic Test
T0042	Other VECTL Chip Logic Test
T0043	Verse and Favor Test
T0044	Load/Store Translation Buffer and CAM Test
T0045	Load/Store Cache Test
T0046	Load/Store Instruction Test
T0047	Load/Store Tag and Duplicate Tag Test
T0048	Load/Store Error Cases Test
T0049	Module Critical Path Test

Table 4–5: Vector Tests in CPU/Memory Interaction Tests—RBD 1

Test	Function
T0014	Cache Test
T0015	Write Buffer Test
T0016	Duplicate Tag Test
T0017	Miscellaneous Error Test

4.8 VAX/DS Diagnostics

The FV64A software diagnostics that run under the VAX Diagnostic Supervisor (VAX/DS) are listed in Table 4-6. Example 4-4 lists VAX/DS commands used in testing vector processors. See Section 2.4 for instructions on running the supervisor.

Table 4-6: FV64A VAX/DS Diagnostics

Program	Description
ERKMP	Multiprocessor Exerciser (2 min—quick) (4 min—default)
EVKAG	VAX Vector Instruction Exerciser, Part 1 (1 1/2 min—quick) (16 min—default)
EVKAH	VAX Vector Instruction Exerciser, Part 2 (1 min—quick) (18 min—default)

Example 4-4: VAX/DS Commands for Testing Vector Processors

```
DS> RUN ERKMP          ! Multiprocessor Exerciser also tests
                       ! vector processors.
DS> SET QUICK          ! Abbreviated version of the VAX Vector
                       ! Instruction Exerciser will be run.
DS> DESELECT KA1       ! Removes the second scalar/vector pair
                       ! from testing.
DS> RUN EVKAG          ! Part 1 of VAX Vector Instruction Exerciser.
DS> RUN EVKAH          ! Part 2.

DS> BOOT n             ! If more than one vector, make the other
DS> DESELECT KA0       ! scalar of the second scalar/vector pair
DS> SELECT KA1         ! the boot processor.  Run EVKAG and EVKAH
                       ! on the second vector.
DS> BOOT n             ! Restore original boot processor.
DS> EXIT
```

4.9 Machine Checks

A machine check is an exception that indicates a processor-detected internal error. Figure 4–7 and Table 4–7 show these parameters. The FV64A machine check parse tree appears in Appendix E along with parse trees for hard and soft error interrupts and disable faults.

Figure 4–7: The Stack in Response to a Machine Check

BYTE COUNT			SP
R	0	MACHINE CHECK CODE	SP+4
VIRTUAL ADDRESS			SP+8
VIRTUAL INSTRUCTION BUFFER ADDRESS			SP+C
INTERRUPT STATE			SP+10
INTERNAL STATE			SP+14
INTERNAL REGISTER			SP+18
PROGRAM COUNTER			SP+1C
PROCESSOR STATUS LONGWORD			SP+20

msb-0180R-89

Table 4–7: FV64A Machine Check Parameters

Parameter	Value (hex)	Description
Machine check code (SP+4)	14	Vector module error

Machine checks are taken regardless of the current IPL. If the machine check exception vector bits (<1:0>) are not both one, the operation of the processor is undefined. The exception is taken on the interrupt stack and the IPL is raised to 1F (hex). See Table 3–9 for the complete list of machine check codes.

4.10 Vector Console Commands

Table 3–10 gives the console commands specific to the vector processor.

Table 4–8: Vector Console Commands

Command	Function
DEPOSIT	Stores data in a specified address. Additional addresses can be VMR, VCR, and VLR (for Vector Mask Register, Vector Count Register, and Vector Length Register).
/M	Defines the address space as a vector indirect register; accesses addresses 400 and higher.
/Q	Quadword is the default data size for vector registers (except for VCR and VLR).
/VE	Defines the address space as the vector register set.
EXAMINE	Displays the contents of a specified address. Additional addresses can be VMR, VCR, and VLR (for Vector Mask Register, Vector Count Register, and Vector Length Register).
/M	Defines the address space as a vector indirect register; accesses addresses 400 and higher.
/Q	Quadword is the default data size for vector registers (except for VCR and VLR).
/VE	Defines the address space as the vector register set.
SET CPU	Specifies attributes of processors, such as eligibility to become the boot processor or whether a vector processor is enabled.
/NOVECTOR_ENABLED	Prevents a vector module from being recognized in the system configuration.
/VECTOR_ENABLED	Specifies that a vector module will be recognized in the system configuration; the default.

DEPOSIT Examples

1.
```
>>> DEPOSIT/VE V12 0          ! Deposits zero into all 64 elements
                              ! of vector register V12.
```

2.
```
>>> DEPOSIT V6:2C/n:2  0      ! Deposits zero into V6 beginning at
                              ! element 2C (hex) and also in the next
                              ! two elements.
```

3.
```
>>> DEPOSIT VLR 1             ! Deposits one in the Vector Length
                              ! Register.
```

4.
```
>>> DEPOSIT/Q/P 200 FFFFFFFF45370201
                              ! Deposits FFFFFFFF45370201, a quadword
                              ! of data into physical memory at address
                              ! 200.
```

5
```
>>> DEPOSIT/M  440 0          ! Deposits zeros to vector indirect
                              ! register with address 440 (hex).
```

EXAMINE Examples

1.
```
>>> EXAMINE VLR                          ! Examines the Vector Length
                                         ! Register.
    M 00000001 0E
```

2.
```
>>> EXAMINE/Q/P 200                      ! Examines the quadword in
                                         ! physical memory at address 200.
```

3.
```
>>> EXAMINE/VE V12.2E                    ! Examines element 2E (hex)
                                         ! (which is 41 decimal) of vector
                                         ! data register V12.
```

4.
```
>>> EXAMINE/M  440                       ! Examines the vector indirect
                                         ! register at hex address 440.
    M 440 FFFFFFFF 00000000              ! /M is used to access vector
                                         ! indirect registers.
```

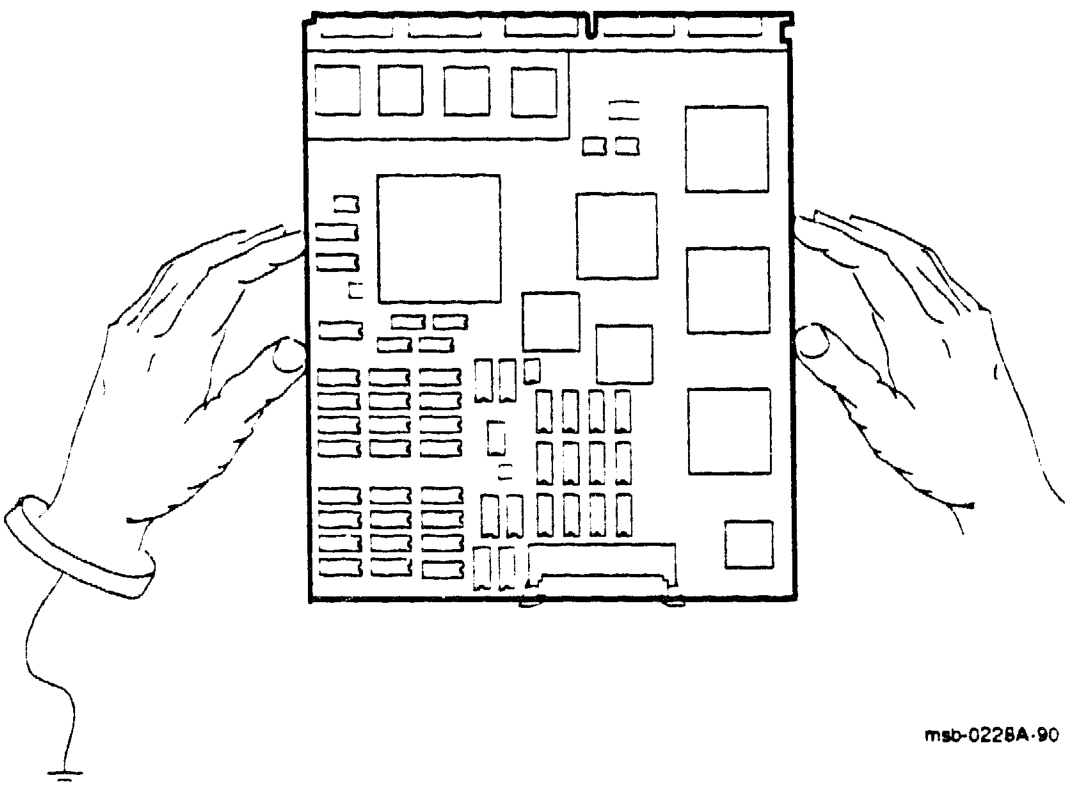
```
5   >>> EXAMINE/VE V0          ! Examines vector register V0; system
                               ! displays all 64 elements of register V0.

    VE V00:00  00000000 00000002      VE V00:01  00000000 00000002
    VE V00:02  00000000 00000002      VE V00:03  00000000 00000002
    VE V00:04  00000000 00000002      VE V00:05  00000000 00000002
    VE V00:06  00000000 00000002      VE V00:07  00000000 00000002
    VE V00:08  00000000 00000002      VE V00:09  00000000 00000002
    VE V00:0A  00000000 00000002      VE V00:0B  00000000 00000002
    VE V00:0C  00000000 00000002      VE V00:0D  00000000 00000002
    VE V00:0E  00000000 00000002      VE V00:0F  00000000 00000002
    VE V00:10  00000000 00000002      VE V00:11  00000000 00000002
    VE V00:12  00000000 00000002      VE V00:13  00000000 00000002
    VE V00:14  00000000 00000002      VE V00:15  00000000 00000002
    VE V00:16  00000000 00000002      VE V00:17  00000000 00000002
    VE V00:18  00000000 00000002      VE V00:19  00000000 00000002
    VE V00:1A  00000000 00000002      VE V00:1B  00000000 00000002
    VE V00:1C  00000000 00000002      VE V00:1D  00000000 00000002
    VE V00:1E  00000000 00000002      VE V00:1F  00000000 00000002
    VE V00:20  00000000 00000002      VE V00:21  00000000 00000002
    VE V00:22  00000000 00000002      VE V00:23  00000000 00000002
    VE V00:24  00000000 00000002      VE V00:25  00000000 00000002
    VE V00:26  00000000 00000002      VE V00:27  00000000 00000002
    VE V00:28  00000000 00000002      VE V00:29  00000000 00000002
    VE V00:2A  00000000 00000002      VE V00:2B  00000000 00000002
    VE V00:2C  00000000 00000002      VE V00:2D  00000000 00000002
    VE V00:2E  00000000 00000002      VE V00:2F  00000000 00000002
    VE V00:30  00000000 00000002      VE V00:31  00000000 00000002
    VE V00:32  00000000 00000002      VE V00:33  00000000 00000002
    VE V00:34  00000000 00000002      VE V00:35  00000000 00000002
    VE V00:36  00000000 00000002      VE V00:37  00000000 00000002
    VE V00:38  00000000 00000002      VE V00:39  00000000 00000002
    VE V00:3A  00000000 00000002      VE V00:3B  00000000 00000002
    VE V00:3C  00000000 00000002      VE V00:3D  00000000 00000002
    VE V00:3E  00000000 00000002      VE V00:3F  00000000 00000002
```

4.11 FV64A Handling Procedures

Handle the processor modules with care. The CMOS2 technology used on the later 6000 series modules is more vulnerable to static than past technology. Also, these modules have 25 mil leads to the chips; these leads are very small, close together, and easily bent.

Figure 4–8: Holding the FV64A Module



The later 6000 series modules require careful handling. Prepare yourself and the work area before handling these modules. Roll up your sleeves and remove any jewelry. Figure 4–8 shows the proper way to hold these modules.

Follow these handling procedures to avoid damaging the processor modules:

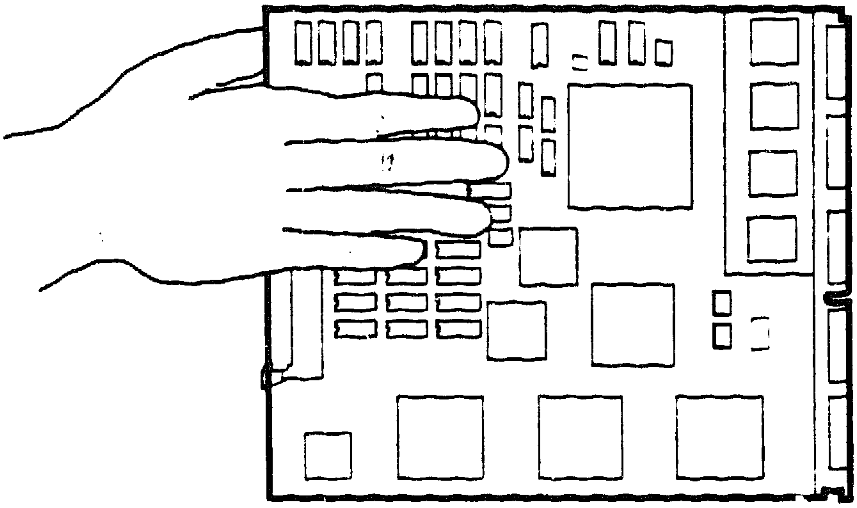
1. Always wear an antistatic wrist strap.
2. Before removing the module from its ESD box, place the box on a clean, stable surface.

   Be sure the box will not slide or fall. **Never** place the box on the floor. And be sure no tools, papers, manuals, or anything else that might damage the module is near it. Some components on this module can be damaged by a 600-volt static charge; paper, for example, can carry a charge of 1000 volts.
3. Hold the module only by the edges, as shown in Figure 4–8.

   Do not hold the module so that your fingers touch any 25 mil devices, leads, or XMI fingers. Be sure you do not bend the module as you are holding it.
4. Be sure nothing touches the module surface or any of its components.

   If anything touches the module, components or leads can be damaged. This includes the antistatic wrist strap, clothing, jewelry, cables, components on other modules, and anything in the work area (such as tools, manuals, or loose papers).

Figure 4-9: Inserting the FV64A Module in an XMI Card Cage



msb-0372-90

You must take special precautions when moving the processor modules in or out of the XMI card cage.

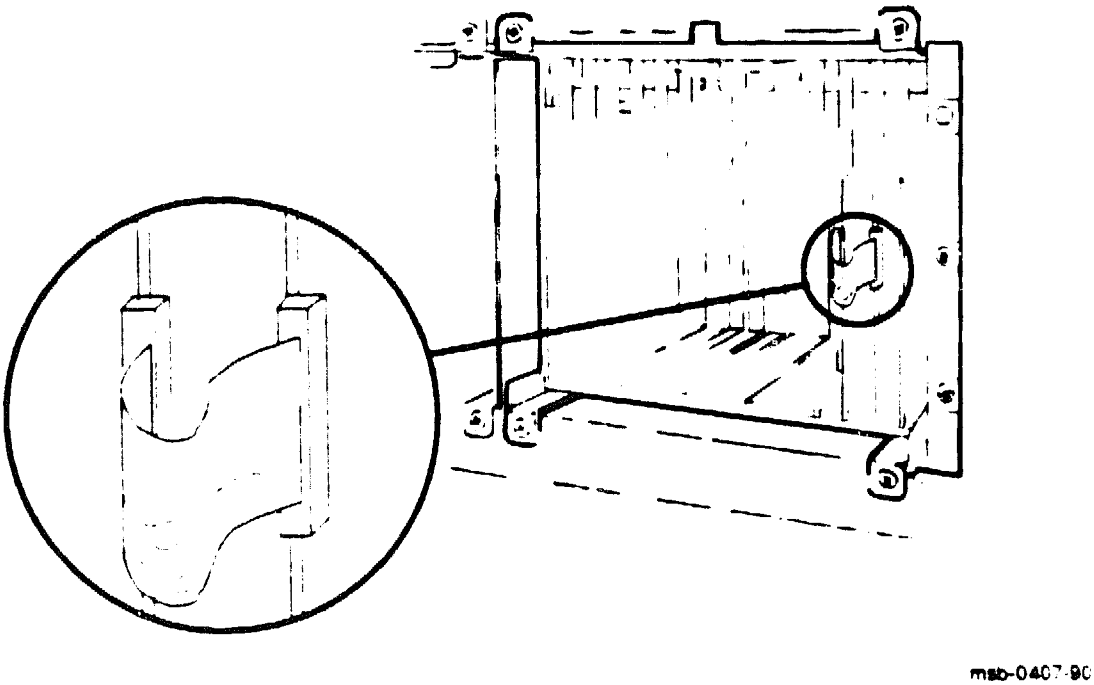
1. Be sure, when inserting the module in or removing it from the XMI card cage, that no part of the module comes in contact with another module or a cable. The leads on the components are fragile and can be damaged by contact with fingers or any surface.
2. When you swap out a module, place it in the correct ESD box before you install the new module.
3. Hold the XMI card cage handle while removing or inserting the module. If it is not held in place, the handle can spring down and damage the module.
4. When inserting the module in the card cage, grasp it as shown in Figure 4–9, being careful not to touch any 25 mil devices, and slide it slowly and gently into the slot.
5. **Do not attach the repair tag to the module.**

   Place the repair tag in the plastic bag attached to the bottom of the ESD box. Allowing the repair tag to come in contact with the module can cause damage to a component.

4.12 How to Replace a Vector Module

If a vector module is defective, you can replace it with a new one. If you install an additional one, see the complete installation instructions in the VAX 6000 Series Upgrade Manual.

Figure 4–10: Replacing a Vector Module in an XMI Card Cage



CAUTION: *Special care must be taken when handling processor modules. See Section 4.11 before replacing this module. Also review the configuration rules in Section 4.3.*

While removing or inserting a module in the XMI card cage, you must hold the XMI card cage lever. Failure to do so may result in damage to the module.

1. Turn the upper key switch straight up to the Off position (0).
2. Open the cabinet door and remove the plastic door in front of the XMI card cage.

   CAUTION: *You must wear an antistatic wrist strap attached to the cabinet when you handle any modules.*
3. Disconnect the VIB cable (17-02240-03) from the vector module.
4. Remove the defective vector processor module.
5. Take the new vector processor module from the ESD box and insert it in the XMI card cage. Place the defective module in the ESD box.
6. Attach the connecting VIB (vector interface bus) cable. The keyed end of the cable attaches to the vector module.
7. Press the lever down to close the connector.
8. Replace the plastic door and shut the cabinet door.
9. Turn the lower key switch to Halt and the upper key switch to Enable.
10. Check the self-test display for the new vector processor, indicated by a V on the TYP line.
11. If the processor shows a plus sign (+) on both lines STF and ETF, it passed self-test.

NOTE: *Installation of an FV64A vector processor requires that the* ***attached*** *KA64A module (T2015) be at a minimum revision of K. In addition, the ROMs on any additional KA64A modules must be at a minimum revision of V2.0 (ROM 0 and ROM 1).*

4.13 Vector Processor Registers

The FV64A internal processor registers are listed in Table 4–9. See Chapter 3 for the complete list of IPR registers. The console program allows you to access the vector registers. Software accesses the vector registers with MTPR/MFPR and MTVP/MFVP instructions.

Table 4–9: FV64A Internal Processor Registers

Register	Mnemonic	Address	Type	Class
Vector Interface Error Status	VINTSR	IPR123	R/W	1
Vector Processor Status	VPSR	IPR144	R/W	2
Vector Arithmetic Exception	VAER	IPR145	R	2
Vector Memory Activity Check	VMAC	IPR146	R	2
Vector Translation Buffer Invalidate All	VTBIA	IPR147	W	2
Vector Indirect Register Address	VIADR	IPR157	R/W	2
Vector Indirect Data Low	VIDLO	IPR158	R/W	2
Vector Indirect Data High	VIDHI	IPR159	R/W	2

Key to Types

R–Read
W–Write
R/W–Read/write

Key to Classes:

1–Implemented by the KA64A CPU module.
2–Implemented by the FV64A vector module.

The IPRs listed in Table 4–9 are explicitly accessible to software only by the Move To Processor Register (MTPR) and Move From Processor Register (MFPR) instructions, which require kernel mode privileges. (The vector indirect registers are also accessed with MTPR and MFPR instructions. These registers are described in the *System Technical User's Guide*.)

From the console, EXAMINE/I and DEPOSIT/I commands read and write the IPRs. EXAMINE/M and DEPOSIT/M commands provide access to the vector indirect registers above hex address 400. EXAMINE/VE and DEPOSIT/VE provide access to the vector data registers.

Other instructions, the Move To/From Vector Processor (MTVP/MFVP) instructions, are used by software to access the Vector Length, Vector Count, and Vector Mask control registers. From the console, these registers are specified as VLR, VCR, and VMR after DEPOSIT and EXAMINE commands, with no qualifiers.

For more information on accessing the vector module registers, see the *VAX 6000 Series Vector Processor Owner's Manual*.

CHAPTER 5

Chapter 5
MS62A Memory

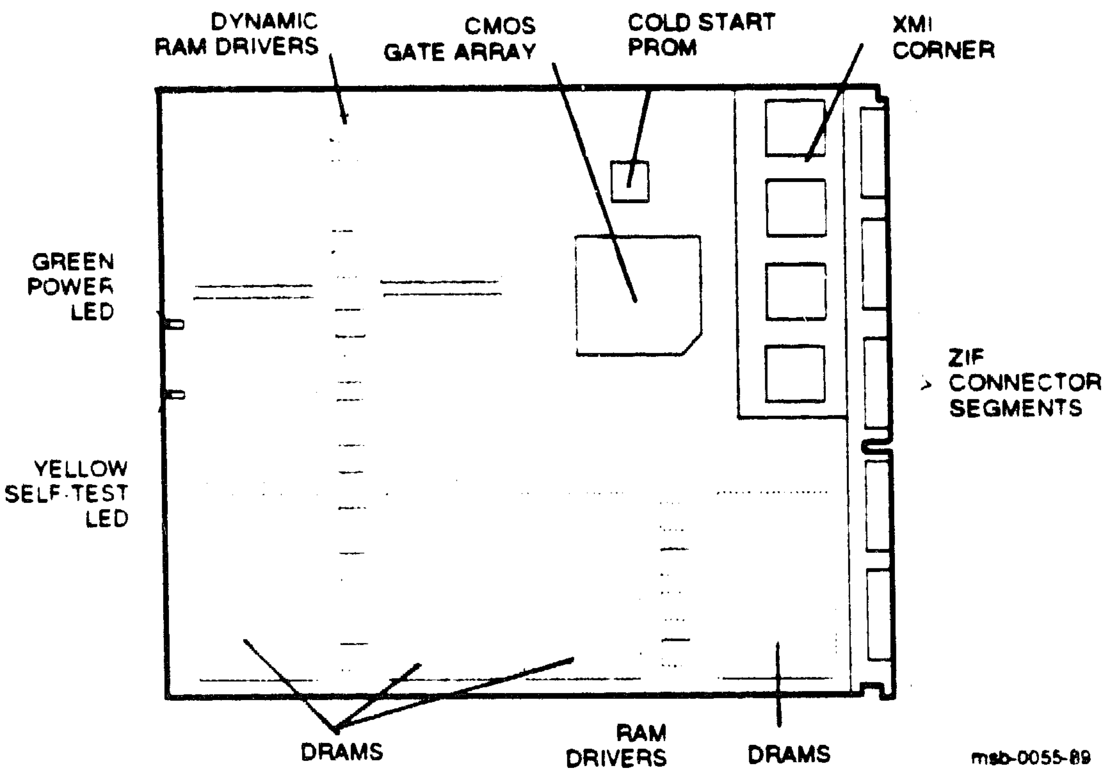
This chapter discusses maintenance of MS62A memory modules. Sections include:

- MS62A Description
- MS62A Configuration Rules
- MS62A Specifications
- MS62A Functional Description
- Interleaving
- Console Commands for Interleaving
- Memory Self-Test
- Memory Self-Test Errors
- MS62A Memory Tests—RBD 3
- Memory Tests (RBD 3) Examples
- MS62A Control and Status Registers
- MS62A Memory Installation

5.1 MS62A Description

The MS62A is a metal-oxide semiconductor (MOS), dynamic random access memory (DRAM), which provides 32 Mbytes of data storage. The memory module is designed for use with the VAX 6000–400 system through the primary interconnect known as the XMI.

Figure 5–1: MS62A Module (Side 1)



The 32-Mbyte memory module has the following features:

- The memory module contains MOS dynamic RAM (DRAM) arrays; a CMOS gate array that contains error correction code (ECC) logic and control logic; and an XMI interface known as the XMI Corner.
- Storage arrays are multiple banks of 72 DRAMs with four banks.
- ECC logic detects single-bit and double-bit errors and corrects single-bit errors on 64-bit quadwords.
- Memory self-test checks all RAMs, the data path, and control logic on power-up.
- Quadwords, octawords, and hexwords are read from memory; quadwords and octawords are written to memory.
- Memory is configured by the console program for 1-, 2-, 4-, 8-way or no interleaving.

5.2 MS62A Configuration Rules

Table 5–1 shows how the XMI card cage should be configured. Memory modules are placed in adjoining XMI slots beginning at slot A.

Table 5–1: Memory Configurations for the XMI Backplane

XMI Slot Number	Contents
A	First memory module
9	Second memory module
8	Third memory module
7	Fourth memory module
6	Fifth memory module[1]
5	Sixth memory module[2]
B	Seventh memory module
C	Eighth memory module

[1] If a processor module is in this slot, install the fifth memory module in slot B.
[2] If a processor module is in this slot, install the sixth memory module in slot C.

NOTE: *Do NOT install memory modules in XMI backplane slots 1 or E.*

Standard configurations include 1, 2, 4, or 8 memory modules. Systems will run with 3, 5, or 7 memory modules, however, system performance may decrease with an odd number of memory modules. Increasing from 1 to 2 or from 2 to 4 memory modules increases performance, but increasing from 4 to 5 memory modules may decrease performance.

5.3 MS62A Specifications

Table 5–2 gives the MS62A specifications.

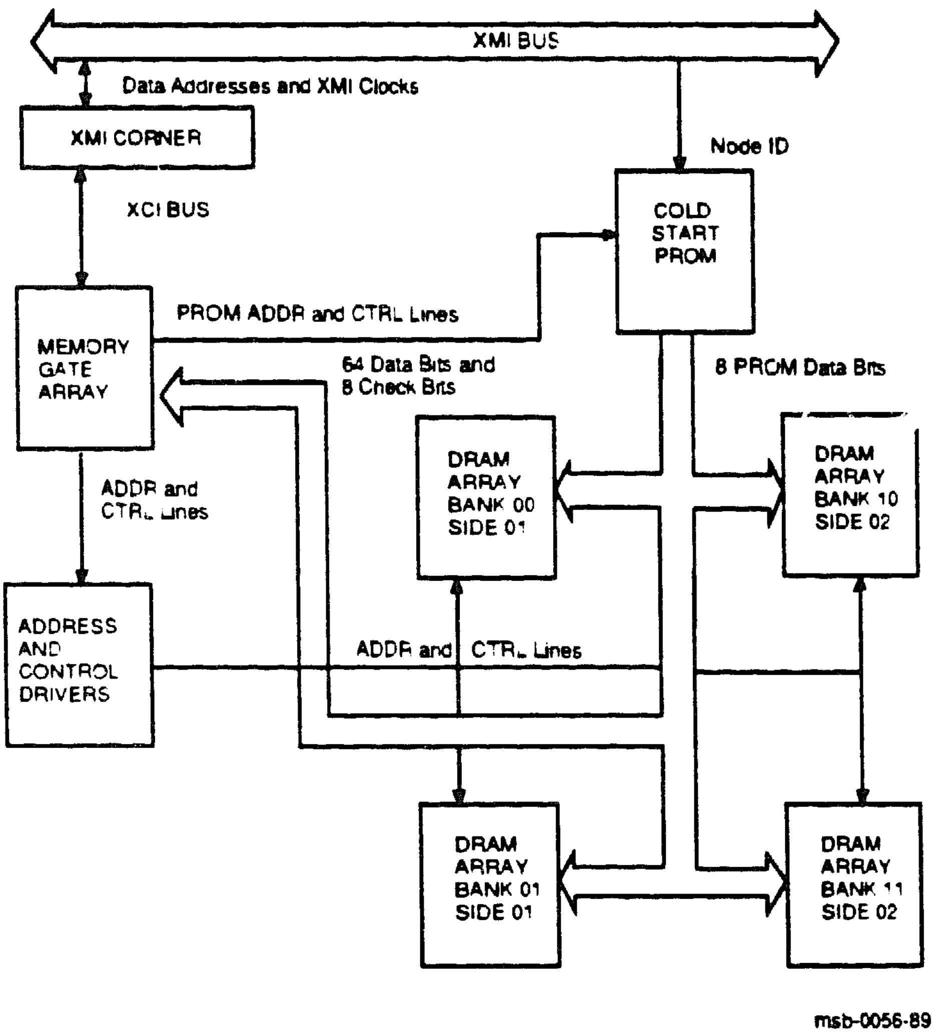
Table 5–2: MS62A Specifications

Parameter	Description
Module Number:	T2014-B
Dimensions:	23.3 cm (9.2") H and 28.0 cm (11.0") D
Addresses:	2-Mbyte boundaries
Starting Address	0 to 510 Mbytes
Ending Address	32 to 512 Mbytes
Technology:	
DRAMS	1 Mbit dynamic RAMs
Gate Arrays	CMOS gate array
Interleave:	1-, 2-, 4-, 8-way or none
Error Correction Code:	Detects single- and double-bit errors and corrects single-bit errors
Temperature:	
Storage Range	-40°C to 66°C (-40°F to 151°F)
Operating Range	5°C to 50°C (41°F to 122°F)
Relative Humidity:	
Storage and Operating	10% to 95% noncondensing
Altitude:	
Storage	Up to 4.8 km (16,000 ft)
Operating	Up to 2.4 km (8000 ft)
Current:	7.5A active, 2.8A standby, max. at +5VBB
Power:	37.5W active, 14.5W standby, max. at +5VBB
Refresh Request Frequency:	9.8 μsec
Refresh Cycle Duration:	6 cycles

5.4 MS62A Functional Description

The MS62A consists of an XMI Corner, a memory gate array, address and control drivers, DRAM arrays, and a cold start PROM.

Figure 5–2: Simplified Block Diagram



The XMI Corner is located on the MS62A and contains interface logic.

The memory gate array transfers data between the XMI Corner and the DRAMs. The gate array also controls address multiplexing, command decoding, arbitration, and CSR logic functions.

Address and control logic modifies address bits received from the XMI Corner. These modified address bits are used to control the selection of the DRAMs during reading and writing.

Memory is arranged in four banks of DRAMs. Each bank contains 72 DRAMs for a total of 288 DRAMs on each memory module.

5.5 MS62A Interleaving

Interleaving optimizes memory access time and increases the effective memory transfer rate by operating memory modules in parallel.

Table 5-3: Interleaving

Interleave	Array	Interleave Address Bits[1]		
		<7>	<6>	<5>
1-Way	A1	-	-	-
2-Way	A1	-	-	0
	A2	-	-	1
4-Way	A1	-	0	0
	A2	-	0	1
	A3	-	1	0
	A4	-	1	1
8-Way	A1	0	0	0
	A2	0	0	1
	A3	0	1	0
	A4	0	1	1
	A5	1	0	0
	A6	1	0	1
	A7	1	1	0
	A8	1	1	1

[1]Bits <7>, <6>, and <5> in the Starting and Ending Address Register (SEADR) define which array is interleaved. Bits <29:8> and <4:0> are not used in interleaving.

The MS62A memory supports 1-, 2-, 4-, 8-way or no interleaving. Up to eight memory modules can be interleaved. Interleaving is done on hexword boundaries. Interleaving addresses are set in the Starting and Ending Address Register by the console program.

NOTE: *Memory modules that fail self-test due to multiple bit errors are not included in the interleave set.*

Unless the system requires a specific, dedicated memory use, you should run the default interleave rather than setting interleaving manually. In default, the console program chooses a configuration for the system.

5.6 Interleaving Examples

Memory can be set up for 3 modes of interleaving.

Figure 5–3: 2-Way Interleaving

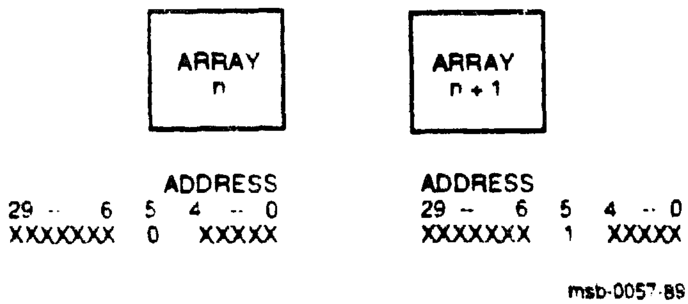


Figure 5–4: 4-Way Interleaving

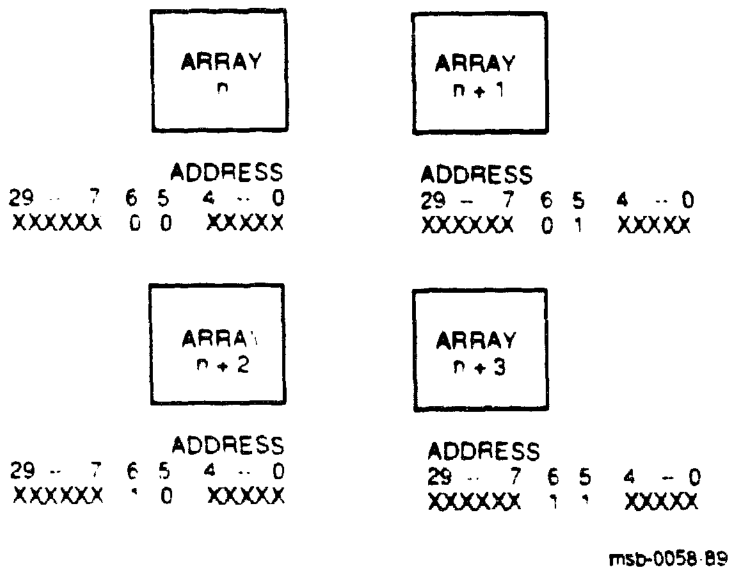
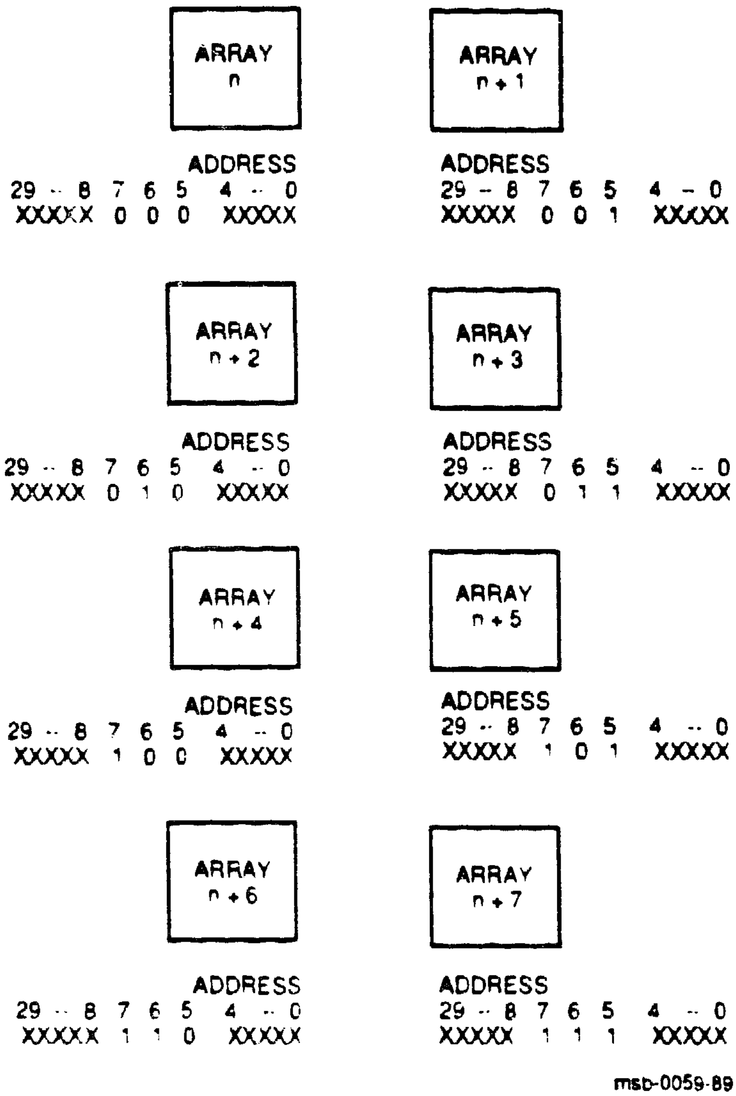


Figure 5–5: 8-Way Interleaving



5.7 Console Commands for Interleaving

The SET MEMORY and SHOW MEMORY commands are useful for setting the interleave to a memory configuration other than the default interleave. This is not usually advisable, but occasional customer use will warrant overriding the original console setting of the interleave.

Example 5-1: SET MEMORY and INITIALIZE Commands

```
>>> SET MEMORY /INTERLEAVE:DEFAULT ❶

>>> SHOW MEMORY ❷

F    E    D    C    B    A    9    8    7    6    5    4    3    2    1    0    NODE #
     .    .    .    .    A4   A3   A2   A1   .    .    .    .    .    .    .    ILV
     .    .    .    .    32   32   32   32   .    .    .    .    .    .    .    128Mb
  /INTERLEAVE:DEFAULT

>>> SET MEMORY /INTERLEAVE:(7+8, 9+A) ❸

>>> INITIALIZE
            [Self-test display prints]

>>> SHOW MEMORY ❹

F    E    D    C    B    A    9    8    7    6    5    4    3    2    1    0    NODE #
     .    .    .    .    B2   B1   A2   A1   .    .    .    .    .    .    .    ILV
     .    .    .    .    32   32   32   32   .    .    .    .    .    .    .    128Mb
  /INTERLEAVE:(7+8, 9+A)

>>> INITIALIZE A ❺
?49 Memory cannot be initialized.
```

The callouts in Example 5–1 are explained below.

❶ Shows the SET MEMORY command that configures interleaving with the console program. This command invokes the default interleaving configuration. If you set a memory configuration and want to revert to the default, use this command.

In this example, the system has four 32-Mbyte memory modules. This command creates a 4-way interleave of the 32-Mbyte modules. Memory modules are located at XMI nodes 7, 8, 9, and A.

❷ The SHOW MEMORY command displays the node number (node #), interleave (ILV), and total usable memory (xxMb) lines from the self-test results.

❸ Shows the SET MEMORY command that creates a 2-way interleave as requested by the user. In this example the user explicitly specified how to interleave the memory modules. Each interleaving set must contain the node number of the memory module. If there is more than one memory module in a set, they are joined by a + sign. Each set of interleaved memory modules must be separated by a comma.

❹ The SHOW MEMORY command displays the memory lines from the self-test printout for the configuration set in ❸.

❺ Memory nodes cannot be initialized. Attempting to do so causes an error message to be returned.

NOTE: *Refer to Chapter 5 of the VAX 6000–400 Owner's Manual for detailed information on the SET MEMORY and SHOW MEMORY commands.*

The SET MEMORY command does not change memory interleaving; it just modifies the memory configuration in the EEPROM. The memory configuration specified by the SET MEMORY command takes place when the system is reset.

5.8 Memory Self-Test

The MS62A performs an initialization and self-test sequence on power-up or when the sequence is requested by a console command. During MS62A self-test the array chip is initialized, all memory locations are tested, and the control and status registers are initialized.

Example 5–2: MS62A Memory Module Results in Self-Test

```
#123456789 0123456789 0123456789 01234567#

F   E   D   C   B   A   9   8   7   6   5   4   3   2   1   0   NODE #
    A   A   .   .   M   M   M   M   .   .   P   P   P   P       TYP     1
    o   o   .   .   -   +   +   +   .   .   +   +   +   +       STF     2
        .   .   .   .   .   .   .   .   .   E   D   E   B       BPD
    .   .   .       .   .   .   .   .   .   +   +   +   +       ETF
    .   .   .   .   .       .   .   .   .   E   D   E   B       BPD

.   .   .   .   .   .   .   .       .   +       +   .   +   .   XBI D +
.   .   .   .   .   .   .   .       +   +   +   .   +   +   .   XBI E +

    .       .       C1  E1  A2  A1  .   .       .   .   .       ILV     3
    .   .   .   .   32  32  32  32  .   .   .   .   .   .       128Mb   4

ROM0 = V1.00  ROM1 = V1.00  EEPROM = 1.00/1.00   SN = SG01234567
```

The callouts in Example 5–2 are explained below.

❶ The **TYP** line shows that memory modules are installed in XMI slots 7 through A as indicated by the M in this row.

❷ The **STF** line shows if memory modules pass self-test, as indicated by the + in this row. If a module fails self-test, a — is indicated, but the console still tests all pages within the module. The failing module is included in the configuration, and the pages that fail self-test are not used by the system.

❸ The **ILV** line indicates that two memory array modules are 2-way interleaved and the other two modules are interleaved by themselves. That is, memory modules in slots 7 and 8 are 2-way interleaved into one interleave set (indicated by all modules beginning with the letter A). Since the memory module in slot A did not pass self-test, it is interleaved by itself (it begins with the letter C). The memory module in slot 9 is interleaved by itself (it begins with the letter B), since it is left alone and cannot be interleaved with A1, A2, or the failing module.

❹ This VAX 6000–400 system contains a total usable memory of 128 Mbytes (four 32-Mbyte memory modules).

If a hard error is detected on a memory node by self-test, that memory module will be used, but it will be interleaved by itself. The page containing the quadword with the hard error will not be used by the operating system. The bit corresponding to that page in the memory bitmap will be clear.

If all MS62A nodes pass self-test, the CPU/memory interaction diagnostic is performed on each MS62A by every CPU. The diagnostic executes a simple read/write test to a small portion of memory. Since there are no errors from the self-test, the memory bitmap is set with all pages as good.

5.9 Memory Self-Test Errors

If an MS62A node fails self-test, an explicit memory test is run on the failing module and console error messages are displayed. The failing module is still included in the memory configuration.

Example 5-3: MS62A Memory Module Node Exclusion

```
>>>  SET MEMORY  /INTERLEAVE:(7+8,9)
>>>  INITIALIZE
            [Self-test display prints]

>>>  SHOW MEMORY

F  E  D  C  B  A  9   8   7   6  5  4  3  2  1  0   NODE #
.              .  -  B1  A2  A1  .  .  .  .  .  .    ILV
.  .  .  .  .  .  32  32  32  .  .  .  .  .  .       96Mb
   /INTERLEAVE (7+8,9)
```

If an MS62A node fails self-test, then the console executes an explicit memory test during the building of the bitmap. Failing memory modules are included in the configuration, although they are interleaved by themselves. The only way to exclude a memory module from interleaving is to use the SET MEMORY command without designating the node you want to exclude. Example 5-3 shows how to exclude the memory module at node A.

During the explicit memory test, any number of the following console messages might be displayed to aid the field service engineer in diagnosing the problem.

```
?37  Explicit interleave list is bad. Configuring
     all arrays uninterleaved.
```

This means that the explicit set of memory arrays for the explicit interleave includes no nodes that are memory arrays. All memory arrays found in the system are unconfigured (the SET MEMORY command may have specified nodes that were not memory modules).

```
?46  Memory interleave set is inconsistent: n n ...
```

This means that the listed nodes (*n n*) do not form a valid memory interleave set. One or more of the nodes might not be a memory array or the set contains an invalid number of memory arrays. Each listed memory array that is valid will be configured uninterleaved; any memory array that is not included in the set will not be interleaved.

```
?47  Insufficent working memory for normal operation.
```

This means that less than 256-Kbytes per processor of working memory were found. There may be insufficient memory for the console to function or for the operating system to boot.

```
?48  Uncorrectable memory errors -- long memory test
     must be performed.
```

This means that a memory array contains an unrecoverable error. The console must perform a slow test to locate all the failing locations.

```
?4A  Memories not interleaved due to uncorrectable errors.
```

This means that the listed arrays would normally have been interleaved (by default or an explicit request). Because one or more arrays contained unrecoverable errors, this interleave set will not be constructed.

NOTE: *Refer to Appendix B, Console Error Messages, and Section 6.7 in the VAX 6000–400 Owner's Manual for more information on these errors.*

When all testing is completed, the yellow LED (located at the center of the module's edge farthest from the XMI backplane) lights, indicating that the module has passed self-test. After self-test, starting and ending addresses are set by the boot processor.

5.10 MS62A Memory Tests—RBD 3

RBD 3 of the ROM-based diagnostics sizes memory, runs extended memory tests, and shows which test (if any) fail.

Table 5–4: Memory Tests — RBD 3

Test	Function
T0001[1]	Memory Self-Test (13 sec[2,3])
T0002[4]	CSR Addressability Test
T0003[4]	CSR Bit Toggling Test
T0004[4]	Parity Error Detection Test
T0005[4]	Error Detection and Correction Logic Test
T0006[4]	Data Path Test
T0007[4]	Quadword and Octaword Masked Write Logic Test
T0008[4]	Interlock Lock Logic Test
T0009[1]	Interleaving and Address Boundary Test (20 sec[2])
T0010[1]	ECC RAM March Test (20 min[2])
T0011[1]	RAM March Test (9 min–RAM; 17 min–ROM[2])
T0012[1]	RAM Moving Inversions Test (2.5 hrs–RAM, 4.5 hrs–ROM[2])

[1]The /C qualifier is required for these tests.
[2]Run times are approximate for one 32-Mbyte module.
[3]If self-test fails, there is a 60 sec timeout.
[4]Tests T0002 through T0008 are run by default.

Tests T0002 through T0008 are run by default. Tests T0001 and T0009 through T0012 have to be selected by the user. Tests are performed on all MS62As unless the user chooses to test a single MS62A. Parameters specified in the command line (refer to Table 5–5) allow one or all memory modules to be tested. These parameters also allow RBD tests to be run from main memory or ROM for RBD tests T0011 and T0012. The /C (confirm destructive memory test) switch is required with RBD tests T0001, T0009, T0010, T0011 and T0012. Parameters are ignored by tests T0001 through T0010.

Table 5–5: RBD 3 Parameters

Parameter[1]	Function
00 (or none)	Run tests T0011 and T0012 from main memory (RAM) and test all memory modules
0n	Run tests T0011 and T0012 from main memory (RAM) and test memory module n only
10	Run tests T0011 and T0012 from ROM and test all memory modules
1n	Run tests T0011 and T0012 from ROM and test memory module n only

[1]The first character indicates if the tests are run from RAM (0) or ROM (1). The second character indicates whether to test all modules (0) or a specific module (n), where n is the memory module backplane slot (must be one of the following: A, 9, 8, 7, 6, 5, B, or C).

NOTE: *If you suspect that all of memory is bad, run tests T0011 and T0012 from ROM.*

The CPU/memory interaction diagnostic also runs tests that exercise memory. See Chapter 3 for information on this CPU/memory interaction diagnostic. See Chapter 2 for more information on running the RBDs.

5.11 Memory Tests (RBD 3) Examples

RBD memory tests are run with a number of user-selectable switches as shown in Example 5–4 through Example 5–6. Refer to Section 2.3 for more details on how to run RBDs.

Example 5–4: RBD 3—All Modules with Halt on Error

```
>>> T/R                          ! Command to enter RBD monitor program

RBD3>                            ! RBD monitor prompt, where 3 is the hexa-
                                 ! decimal node number of the processor
                                 ! that is currently receiving your input

RBD3> ST3/TR/HE                  ! Runs the default MS62A RBD
                                 ! test; test results written to the
                                 ! console terminal; tests will halt on
                                 ! any hard error found (/HE)
,XMA_RBD          1.00

; T0002  T0003  T0004  T0005  T0006  T0007  T0008

;        P          3     8082        1
;00000000 00000000 00000000 00000000 00000000 00000000 00000000

RBD3>
```

Example 5–5: RBD 3—Confirm Switch

```
RBD3> ST3/TR/T=9:10/C            ! Runs the MS62A RBD tests
                                 ! T0009 and T0010 only.  These are
                                 ! destructive tests, so the confirm
                                 ! switch is needed.  Confirm destructive
                                 ! memory test switch (/C) is required
                                 ! on tests T0001 and T0009 through T0012.
,XMA_RBD          1.00

; T0009  T0010

;        P          3     8082        1
;00000000 00000000 00000000 00000000 00000000 00000000 00000000

RBD3>
```

Example 5–6: RBD 3—Parameter

```
RBD3> ST3/TR/T=11:12/C 0A        ! Runs MS62A RBD tests
                                 ! T0011 and T0012 from RAM on the
                                 ! the memory module in slot A. Confirm
                                 ! destructive memory test switch (/C)
                                 ! is required on these tests.
;XMA_RBD         1.00

; T0011  T0012

        [RBD status messages are printed every two minutes;
         use the /DS qualifier in the command string to inhibit
         these messages.]

;       P        3      8082        1
;00000000 00000000 00000000 00000000 00000000 00000000 00000000

RBD3>  QUIT                      ! Exit from RBD monitor program
?06 Halt instruction executed in kernel mode.
PC  = 200601D8
PSL = 041F0604
ISP = 201405B4

>>>                              ! Console prompt returns
```

5.12 MS62A Control and Status Registers

The memory contains 24 control and status registers (CSRs) to control the memory and log errors. All CSRs are 32 bits long and respond only to longword read and write transactions. Only full writes are performed to the CSRs. If a parity error occurs during a write operation, the operation is aborted and the contents of the CSRs are unchanged.

The CSRs start at an address dependent upon the node ID. All CSR addresses are designated as BB + *n*, where *n* is the relative offset of the register.

Table 5–6: MS62A Memory Control and Status Registers

CSR Name	Mnemonic	Address
Device Register	XDEV	BB[1]+ 00
Bus Error Register	XBER	BB + 04
Starting and Ending Address Register	SEADR	BB + 10
Memory Control Register 1	MCTL1	BB + 14
Memory ECC Error Register	MECER	BB + 18
Memory ECC Error Address Register	MECEA	BB + 1C
Memory Control Register 2	MCTL2	BB + 30
TCY Register	TCY	BB + 34
Interlock Flag Status Registers[2]	IFLG*n*	BB + *n*

[1] "BB" refers to the base address of an XMI node (2180 0000 + (node ID x 8000)).

[2] Refer to Table 5–7 for the relative address of the Interlock Flag Status Registers.

Table 5–7: Interlock Flag Registers

Interlock Flag Register	Mnemonic	Address
Interlock Flag 0 Status Register	IFLG 0	BB + 20
Interlock Flag 1 Status Register	IFLG 1	BB + 24
Interlock Flag 2 Status Register	IFLG 2	BB + 28
Interlock Flag 3 Status Register	IFLG 3	BB + 2C
Interlock Flag 4 Status Register	IFLG 4	BB + 40
Interlock Flag 5 Status Register	IFLG 5	BB + 44
Interlock Flag 6 Status Register	IFLG 6	BB + 48
Interlock Flag 7 Status Register	IFLG 7	BB + 4C
Interlock Flag 8 Status Register	IFLG 8	BB + 80
Interlock Flag 9 Status Register	IFLG 9	BB + 84
Interlock Flag 10 Status Register	IFLG10	BB + 88
Interlock Flag 11 Status Register	IFLG11	BB + 8C
Interlock Flag 12 Status Register	IFLG12	BB + 100
Interlock Flag 13 Status Register	IFLG13	BB + 104
Interlock Flag 14 Status Register	IFLG14	BB + 108
Interlock Flag 15 Status Register	IFLG15	BB + 10C

5.13 MS62A Memory Installation

Use the following procedure when removing or installing a memory module.

1. Perform an orderly shutdown of the system.
2. Turn the upper key switch on the front control panel to the Off position.
3. Pull the circuit breaker on the AC power controller to the Off position.
4. Open the front cabinet door.
5. Remove the clear plastic door in front of the XMI cage.

   CAUTION: *You must wear an antistatic wrist strap attached to the cabinet when you handle any modules.*

6. Lift the lever and hold it. Remove the memory module from its slot.
7. Hold the lever while installing the memory module in the appropriate slot, shown in Table 5–1. (Memory modules should be installed adjacent to each other).
8. Close the lever after you have inserted a new memory module.
9. Replace the clear door.
10. Take off the ground strap.
11. Turn on system power and check that all nodes pass self-test.
12. Complete the installation by running appropriate self-test diagnostics (refer to Section 5.8) and RBDs (refer to Section 5.10).

    NOTE: *See the Verification chapter in the VAX 6000–400 Installation Guide for complete acceptance instructions.*

CHAPTER 6

Chapter 6

DWMBA XMI-to-VAXBI Adapter

This chapter discusses the DWMBA modules. Sections include:

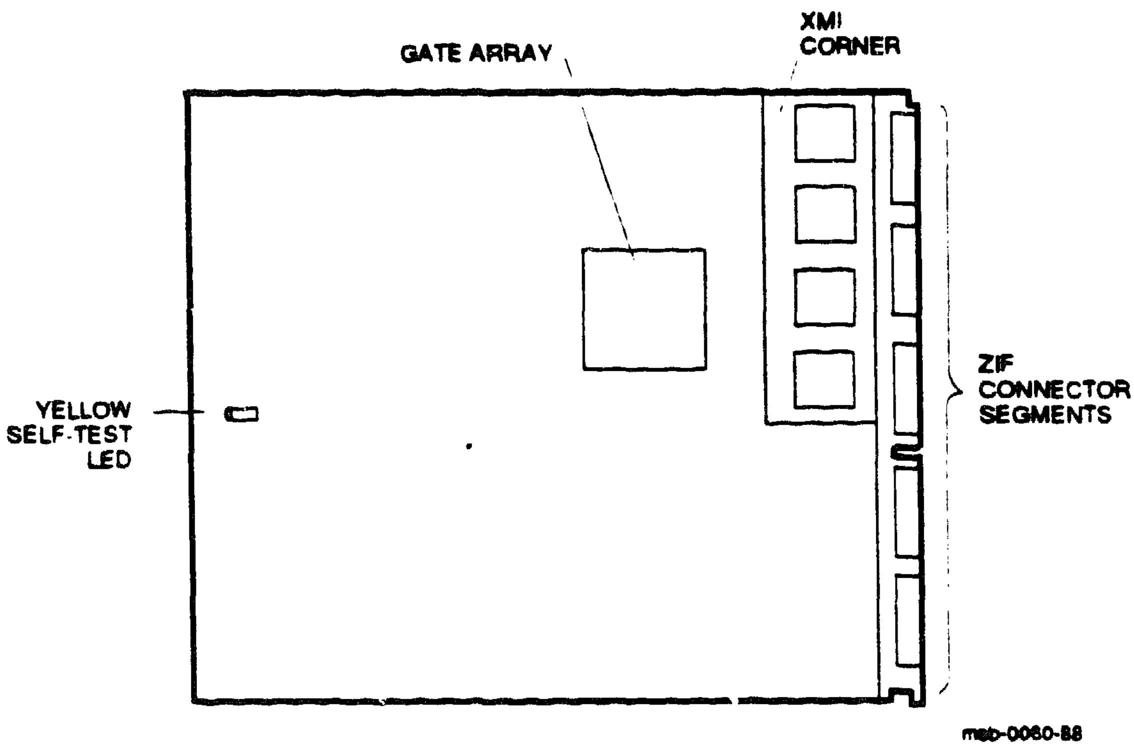
- DWMBA Physical Description
  - Physical Layout
  - DWMBA Specifications
- DWMBA Functional Description
- DWMBA Configuration Rules
- DWMBA Tests—RBD 2
- DWMBA Registers

6.1 DWMBA Physical Description

6.1.1 Physical Layout

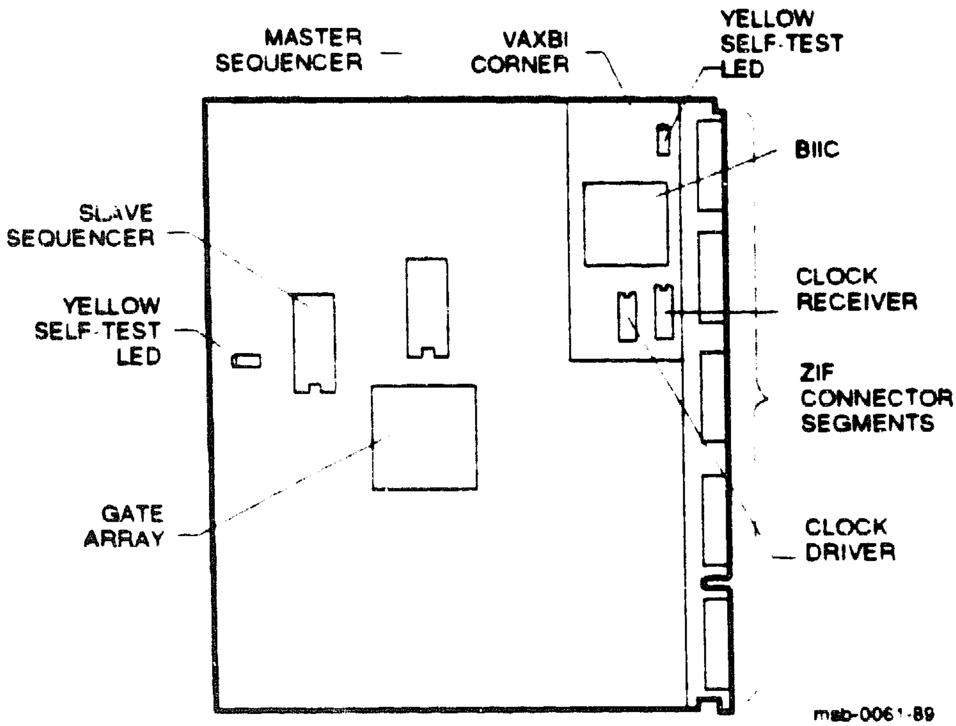
The DWMBA/A is an XMI module with the standard XMI Corner, an XMI self-test OK LED indicator, IBUS drivers/receivers and transceivers, timeout logic, and a gate array that controls the DWMBA/A. Most of the components on the DWMBA/A are surface-mounted.

Figure 6–1: DWMBA/A XMI Module



The DWMBA/B is a standard VAXBI module with a VAXBI Corner, including a BIIC interface chip, the primary interface between the VAXBI bus and the DWMBA/B node logic, a clock driver, and a clock receiver. The DWMBA/B gate array is used mostly for data path logic. The VAXBI self-test OK LED is on the VAXBI Corner, and the module self-test OK LED is at the module edge opposite the connector edge.

Figure 6–2: DWMBA/B VAXBI Module



6.1.2 DWMBA Specifications

The following specifications apply to the DWMBA modules.

Table 6–1: DWMBA/A XMI Module Specifications

Parameter	Description
Module Number:	T2012
Dimensions:	23.3 cm (9.2") H x 28.0 cm (11.0", D x 0.23 cm (0.093") thick
Temperature:	
Sto-age Range	-40°C to 66°C (-40°F to 151°F)
Operating Range	5°C to 50°C (41°F to 122°F)
Relative Humidity:	
Storage and operating	10% to 95% noncondensing
Altitude:	
Storage	Up to 4.8 km (16,000 ft)
Operating	Up to 2.4 km (8000 ft)
Current:	3A at +5V
	200mA at +5VBB
Power:	16W

Table 6–2: DWMBA/B VAXBI Module Specifications

Parameter	Description
Module Number:	T1043
Dimensions:	20.3 cm (8") H x 23.3 cm (9.2") D x 0.23 cm (0.093") thick
Temperature:	
Storage Range	-40°C to 66°C (-40°F to 151°F)
Operating Range	5°C to 50°C (41°F to 122°F)
Relative Humidity:	
Storage and operating	10% to 95% noncondensing
Altitude:	
Storage	Up to 4.8 km (16,000 ft)
Operating	Up to 2.4 km (8000 ft)
Current:	6A at +5V
	10mA at -12V
Power:	30W

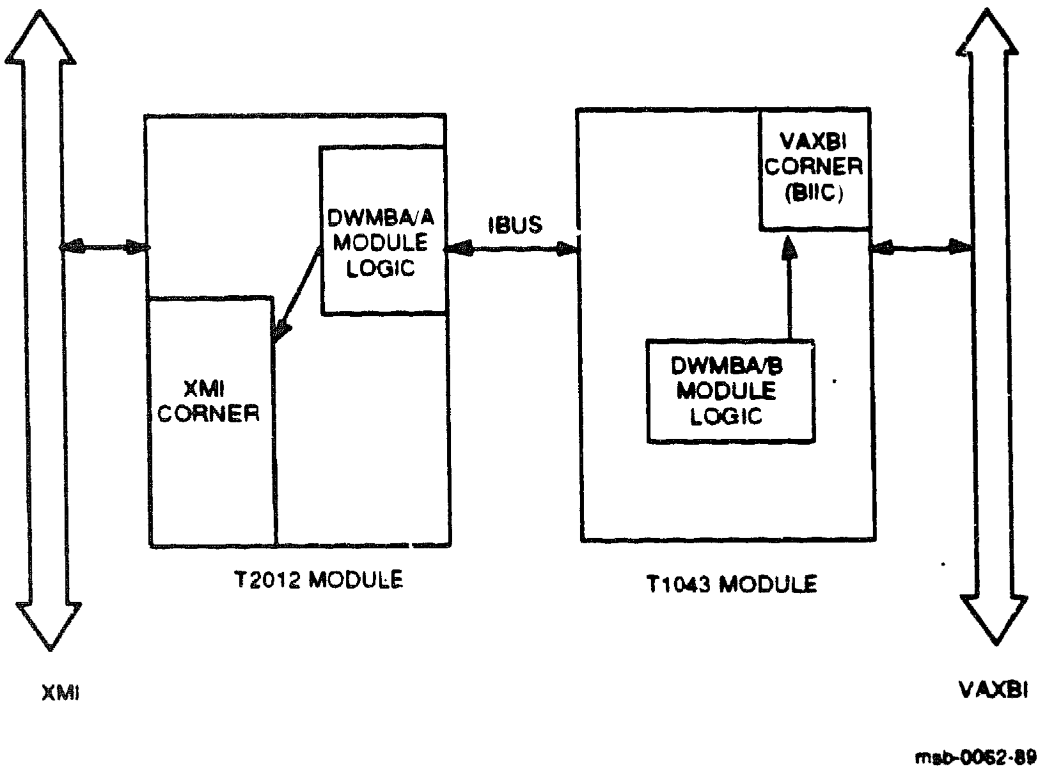
Table 6–3: DWMBA Cables

Part Number	Description
17-00849-08	18" DWMBA/B to DWMBA/B AC/DC OK cable, from VAXBI cage 2 slot 1 (segment C2) to VAXBI cage 1 slot 1 (segment C1).
17-01897-01	15' DWMBA cables for expander cabinet, from XMI slots C, B, 1, and 2 as needed (segments D and E) to VAXBI cages 3, 4, 5, and 6 slot 1 (segments D and E). Two per DWMBA.
17-01897-02	7" DWMBA cables, from XMI slot E (segments D and E) to VAXBI cage 2 slot 1 (segments D and E). Two per DWMBA.
17-01897-03	25" DWMBA cables, from XMI slot D (segments D and E) to VAXBI cage 1 slot 1 (segments D and E). Two per DWMBA.

6.2 DWMBA Functional Description

The DWMBA adapter provides an information path between the XMI bus and I/O devices on the VAXBI bus. The DWMBA consists of two modules: the DWMBA/A and the DWMBA/B. The DWMBA/A resides on the XMI bus, and the DWMBA/B resides on the VAXBI bus. Four 30-pin cables, which make up the IBUS, connect the two modules.

Figure 6–3: DWMBA XMI-to-VAXBI Adapter Block Diagram



The DWMBA/A contains the XMI Corner, the register files, XMI required registers, DWMBA-specific registers, and the control sequencers for the XMI interface.

The DWMBA/B contains the IIC interface chip, interconnect drivers, control sequencers to handle the control of the data transfer, status bits to/from the DWMBA/A's register files and the BIIC, DWMBA/B specific registers, decode logic for direct memory access (DMA) operation, and VAXBI clock-generation circuitry.

The DWMBA/A and DWMBA/B are connected by four cables of 30 wires each. These 120 wires make up the IBUS, which transfers data and control information between the two modules.

The DWMBA uses CPU and DMA transactions to exchange information. CPU transactions originate from the KA64A(s) and are presented to the DWMBA from the XMI bus with the processor as the XMI commander and the DWMBA as the XMI responder.

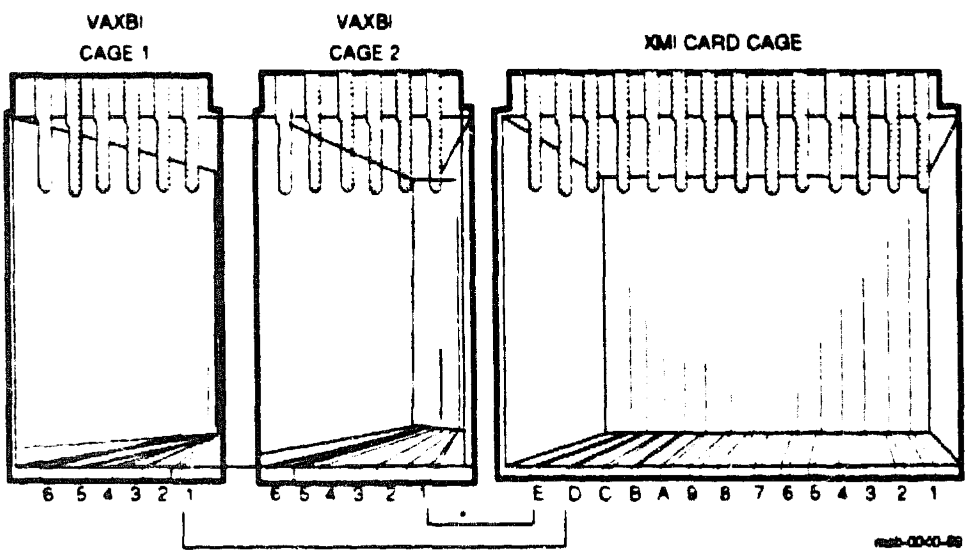
DMA transactions originate from VAXBI nodes that select the DWMBA as the VAXBI slave. These are read or write transactions targeted to XMI memory space or are VAXBI-generated interrupt transactions that target a KA64A. For DMA transactions, the DWMBA is the XMI commander, and the MS62A is the XMI responder.

The VAX 6000–400 system uses a 30-bit physical address. The DWMBA can be both a master and a slave on the VAXBI. As a master, it carries out transactions requested by its XMI devices. As a slave, it responds to VAXBI transactions that select its node.

6.3 DWMBA Configuration Rules

This section describes the configuration rules for the DWMBA/A modules in the XMI card cage and for the DWMBA/B modules in the system's two 6-slot VAXBI card cages.

Figure 6-4: VAX 6000-400 Slot Numbers



DWMBA/As are placed in the order shown in the table below:

Table 6–4: DWMBA Configuration

XMI Node No.	VAXBI Cage No.	Location
D	1	System cabinet
E	2	System cabinet
C	3	Expander cabinet
B	4	Expander cabinet
1	5	Expander cabinet
2	6	Expander cabinet

Configuration rules are as follows:

- The DWMBA/B which corresponds to the DWMBA/A in XMI slot D is placed in VAXBI cage 1, slot 1. The DWMBA/B which corresponds to the DWMBA/A in XMI slot E is placed in VAXBI cage 2, slot 1.
- All additional DWMBA/Bs are placed in slot 1 (rightmost slot) of each card cage in the VAXBI expander cabinet, as shown in Table 6–4.

6.4 DWMBA Tests—RBD 2

The DWMBA ROM-based diagnostic, RBD 2, checks functions of both DWMBA modules. RBD 2 tests the DWMBA modules and can trace the subtests, pinpointing errors.

The DWMBA has no on-board self-test. The boot processor ROM code tests DWMBAs during additional power-up tests. At power-up, the boot processor first sizes all DWMBAs and then serially tests each one.

When invoking RBD 2 from the monitor, the START command requires a parameter. This parameter is the XMI node number (hexadecimal) of the DWMBA/A module of the DWMBA to be tested.

Example 6-1: DWMBA Tests—RBD 2

```
>>> T/R                        ! Command to enter RBD monitor program

RBD1>                          ! RBD monitor prompt, where 1 is the
                               ! hexadecimal node number of the
                               ! processor that is currently receiving
                               ! your input.

RBD1> ST2/TR D                 ! Runs the DWMBA RBD, testing
                               ! the DWMBA at XMI node number D. Test
                               ! results written to the console
                               ! terminal:

;XBI_TEST      1.00

; T0001  T0005  T0006  T0007  T0008  T0009  T0012  T0013  T0014  T0015
; T0016  T0017  T0018  T0019  T0020  T0021  T0022  T0023  T0024  T0025

;        P          1       8082          1
;000000000  00000000  00000000  00000000  00000000  00000000  00000000

RBD1> QUIT

>>>
```

Table 6–5: DWMBA XMI-to-VAXBI Adapter RBD Tests

Test	Function	Default
T0001	DWMBA/A XMI Module CSR test	Yes
T0002	XMI Low Longword Parity Error test	No
T0003	XMI High Longword Parity Error test	No
T0004	XMI Function and ID Parity Error test	No
T0005	DWMBA/B CSR test	Yes
T0006	BIIC VAXBI Loopback Transaction test	Yes
T0007	BIIC VAXBI Transaction test	Yes
T0008	DMA test	Yes
T0009	DMA Buffer test	Yes
T0010	XMI Parity Error Interrupt test	No
T0011	Write Sequence Error Interrupt test	No
T0012	CPU Buffer C/A Fetch Parity Error (Interrupt) test	Yes
T0013	CPU Buffer Data Fetch Parity Error (Interrupt) test	Yes
T0014	DMA Buffer Data Fetch Parity Error (Interrupt) test	Yes
T0015	VAXBI Interlock Read Error (Interrupt) test	Yes
T0016	DMA-A Buffer C/A Load Parity Error (Interrupt) test	Yes
T0017	DMA-A Buffer Data Load Parity Error (IVINTR) test	Yes
T0018	DMA-B Buffer C/A Load Parity Error (Interrupt) test	Yes
T0019	DMA-B Buffer Data Load Parity Error (IVINTR) test	Yes
T0020	CPU Buffer Data Load Parity Error (Interrupt) test	Yes
T0021	BCI Parity Error test	Yes
T0022	Nonexistent Memory (Interrupt) test	Yes
T0023	CRD Error (Interrupt) test	Yes
T0024	VAXBI Interrupt test	Yes
T0025	VAXBI IP Interrupt test	Yes
T0026	No Stall Timeout Test	No

6.5 DWMBA Registers

Two sets of registers are used by the DWMBA adapter: VAXBI registers (residing in the BIIC) and DWMBA registers (residing on both modules of the DWMBA). The DWMBA registers include the XMI required registers and DWMBA-specific registers addressed in DWMBA private space.

Table 6–6: VAXBI Registers

Name	Mnemonic	Address[1]
Device Register	DTYPE	bb+00
VAXBI Control and Status Register	VAXBICSR	bb+04
Bus Error Register	BER	bb+08
Error Interrupt Control Register	EINTRSCR	bb+0C
Interrupt Destination Register	INTRDES	bb+10
IPINTR Mask Register	IPINTRMSK	bb+14
Force-Bit IPINTR/STOP Destination Register	FIPSDES	bb+18
IPINTR Source Register	IPINTRSRC	bb+1C
Ending Address Register	EADR	bb+24
BCI Control and Status Register	BCICSR	bb+28
Write Status Register	WSTAT	bb+2C
Force-Bit IPINTR/STOP Command Register	FIPSCMD	bb+30
User Interface Interrupt Control Register	UINTRCSR	bb+40
General Purpose Register 0	GPR0	bb+F0
General Purpose Register 1	GPR1	bb+F4
General Purpose Register 2	GPR2	bb+F8
General Purpose Register 3	GPR3	bb+FC
Slave-Only Status Register	SOSR	bb+100
Receive Console Data Register	RXCD	bb+200

[1] The abbreviation "bb" refers to the base address of a VAXBI node (the address of the first location of nodespace).

Table 6–6 lists the VAXBI registers. The VAXBI registers are described in Chapter 5 of the *VAXBI Options Handbook*. Table 6–7 lists the DWMBA registers.

Table 6–7: DWMBA XMI Registers

Name	Mnemonic[1]	Address[2]
Device Register	XDEV	BB+00
Bus Error Register	XBER	BB+04
Failing Address Register	XFADR	BB+08
Responder Error Address Register	AREAR	BB+0C
Error Summary Register	AESR	BB+10
Interrupt Mask Register	AIMR	BB+14
Implied Vector Destination/Diagnostic Register	AIVINTR	BB+18
Diag 1 Register	ADG1	BB+1C
Control/Status Register	BCSR	BB+40
Error Summary Register	BESR	BB+44
Interrupt Destination Register	BIDR	BB+48
Timeout Address Register	BTIM	BB+4C
Vector Offset Register	BVOR	BB+50
Vector Register	BVR	BB+54
Diagnostic Control Register 1	BDCR1	BB+58
Reserved Register	—	BB+5C

[1]If the first letter of the mnemonic is "X" or "A," it indicates that the register resides on the DWMBA/A; a first letter of "B" indicates that the register resides on the DWMBA/B.

[2]The abbreviation "BB" refers to the base address of an XMI node (the address of the first location of nodespace).

CHAPTER 7

Chapter 7
XMI Card Cage

This chapter describes the XMI card cage. Removal and replacement procedures are detailed, and configuration restrictions are listed. Sections include:

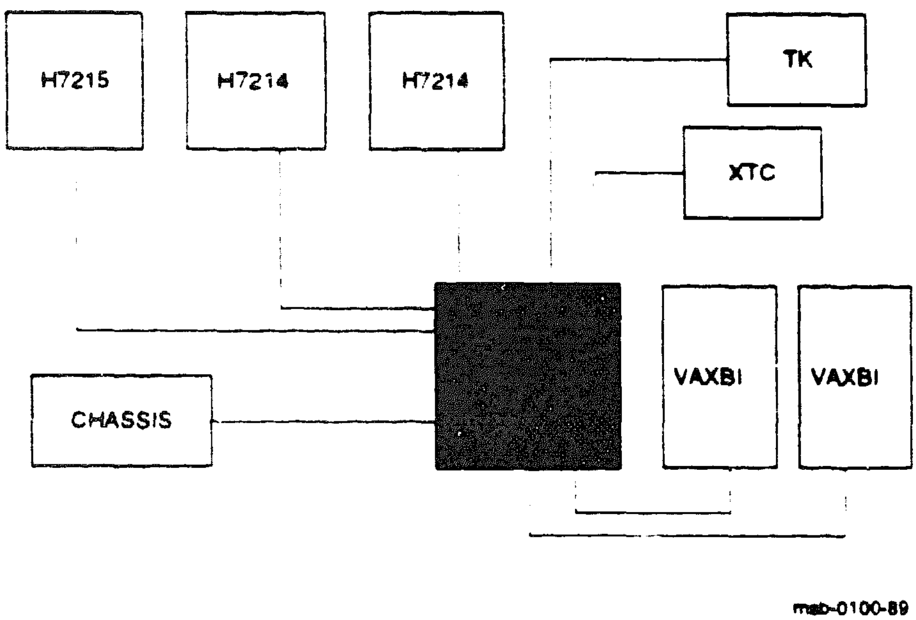
- XMI Card Cage Description
    - System Use
    - Specifications
- XMI Card Cage Removal
- Switching XMI Card Cages
- XMI Card Cage Replacement
- Installing Modules in the XMI Card Cage
- XMI Troubleshooting

7.1 XMI Card Cage Description

7.1.1 System Use

The XMI card cage provides the high-speed system bus. Figure 7-1 is a simplified block diagram showing physical connections between the XMI card cage and other components in the cabinet.

Figure 7-1: XMI Card Cage Connections



The XMI card cage is a 14-slot cage with zero insertion force (ZIF) connectors. The cage is 3 inches deeper than a VAXBI cage, providing for larger XMI modules. The backplane area extends over three of the five connector segments, which leaves two segments for I/O pins. Mounted in the center rear of the XMI backplane is a daughter card that holds the central arbiter chip. Four slots in the center of the cage have no I/O connectors, so only processor or memory modules may be placed in these slots.

For each VAXBI bus, there must be an XMI-to-VAXBI adapter. This adapter (DWMBA) consists of two modules: a DWMBA/A module in the XMI card cage and a DWMBA/B module in the VAXBI card cage. (See Chapter 5.)

7.1.2 XMI Card Cage Specifications

The XMI card cage has 14 slots and is located in the upper part of the cabinet. The field-replaceable unit (70-24373-01) does not include the power bus bar assembly, the two side mounting plates, the daughter card, and three foam air seals.

Figure 7–2: XMI Card Cage

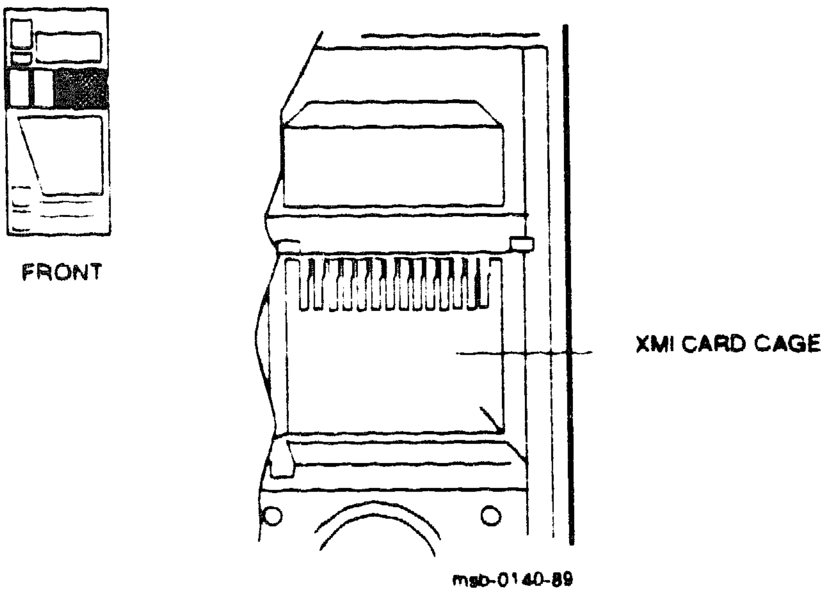


Table 7–1: XMI Card Cage Assembly Specifications

Parameter	Description
Part Number:	70-24373-01, 14-slot cage with no daughter card or bus bars
Location:	Upper right front
Dimensions:	12" H x 10 1/2" W x 12 1/4" L
Weight:	29 lbs
Power:	One H7215 DC regulator and two H7214 DC regulators
Service From:	Front and rear of cabinet

Table 7–2: XMI Card Cage Cables

Item	Part Number	Description
Cables:	17-01525-01	XMI to both H7214s
	17-01566-01	XMI to J3 of H7215
	17-01568-02	XMI to J4 of XTC, 20-pin ribbon
	17-01662-01	XMI ground strap
	17-01812-01	XMI to filter board in system control assembly to power the TK unit
	17-01833-01	Fail safe enable cable, XMI to H7231 battery backup unit and H405
	17-01897-01	15' DWMBA cables for expander cabinet, from XMI slots C, B, 1, and 2 as needed (segments D and E) to VAXBI cages 3, 4, 5, and 6 slot 1 (segments D and E). Two per DWMBA.
	17-01897-02	7' DWMBA cables, from XMI slot E (segments D and E) to VAXBI cage 2 slot 1 (segments D and E). Two per DWMBA.
	17-01897-03	25" DWMBA cables, from XMI slot D (segments D and E) to VAXBI cage 1 slot 1 (segments D and E). Two per DWMBA.
Tools Required:		
VAXBI Tool Kit	A2-M1094-10	Includes: Torque screwdriver Large Phillips and flat screwdrivers Small Phillips screw-holding screwdriver or one with magnetic tip 11/32" nutdriver
Subassemblies:		
Daughter Card	54-18177-01	Small module that mounts on XMI backplane
Bus Bar Assembly	12-27676-01 12-27938-01 12-27939-01	+5V/+5VBB/Ground -5.2V XMI bus bars -2V XMI bus bars
Foam Air Seals	74-34536-01 74-34536-03 74-36670-02	Three pieces of foam used for air seals

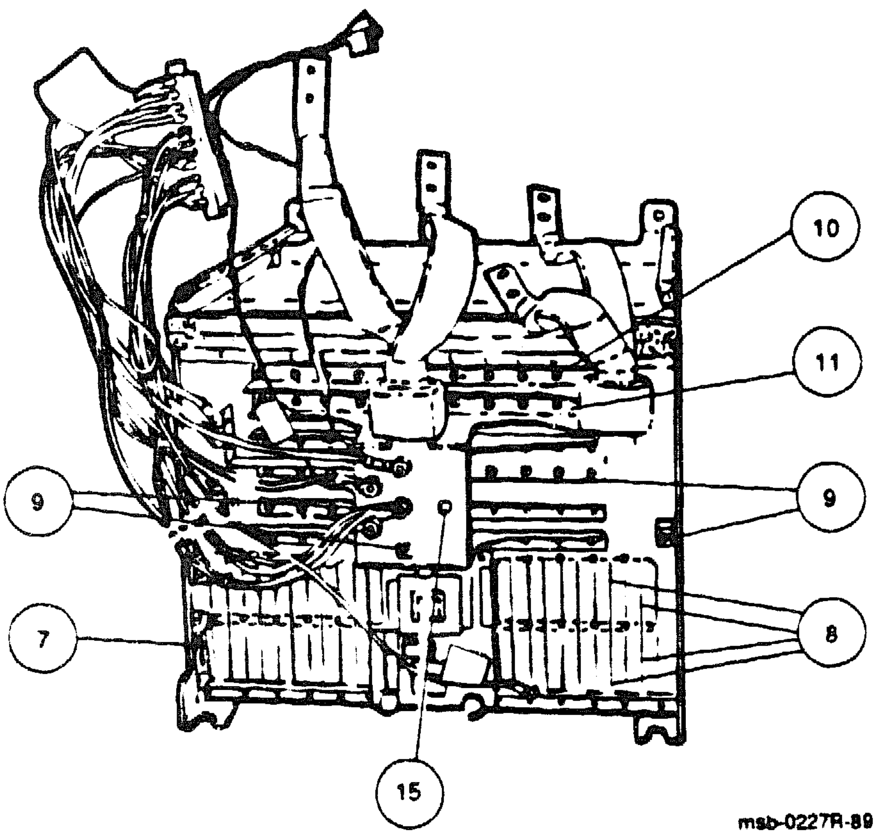
7.2 XMI Card Cage Removal

The XMI card cage is removed from the front of the cabinet after you disconnect connections at the backplane.

7.2.1 Prepare for Removal

Prepare the system for shutdown. Set up a work space nearby where you can store the modules and work on the XMI card cage. Label and disconnect the signal and power connections.

Figure 7-3: XMI Backplane Cables and Power Connections



1. Perform an orderly shutdown of the system.
2. Turn the upper key switch on the front control panel to the Off position.
3. Pull the circuit breaker on the AC power controller to the Off position. The AC power controller is at the bottom rear of the cabinet.
4. Unplug the machine.
5. Open the rear cabinet door.
6. Drop the I/O bulkhead tray to expose the card cages.

CAUTION: *You must wear an antistatic wrist strap attached to the cabinet when you handle any modules.*

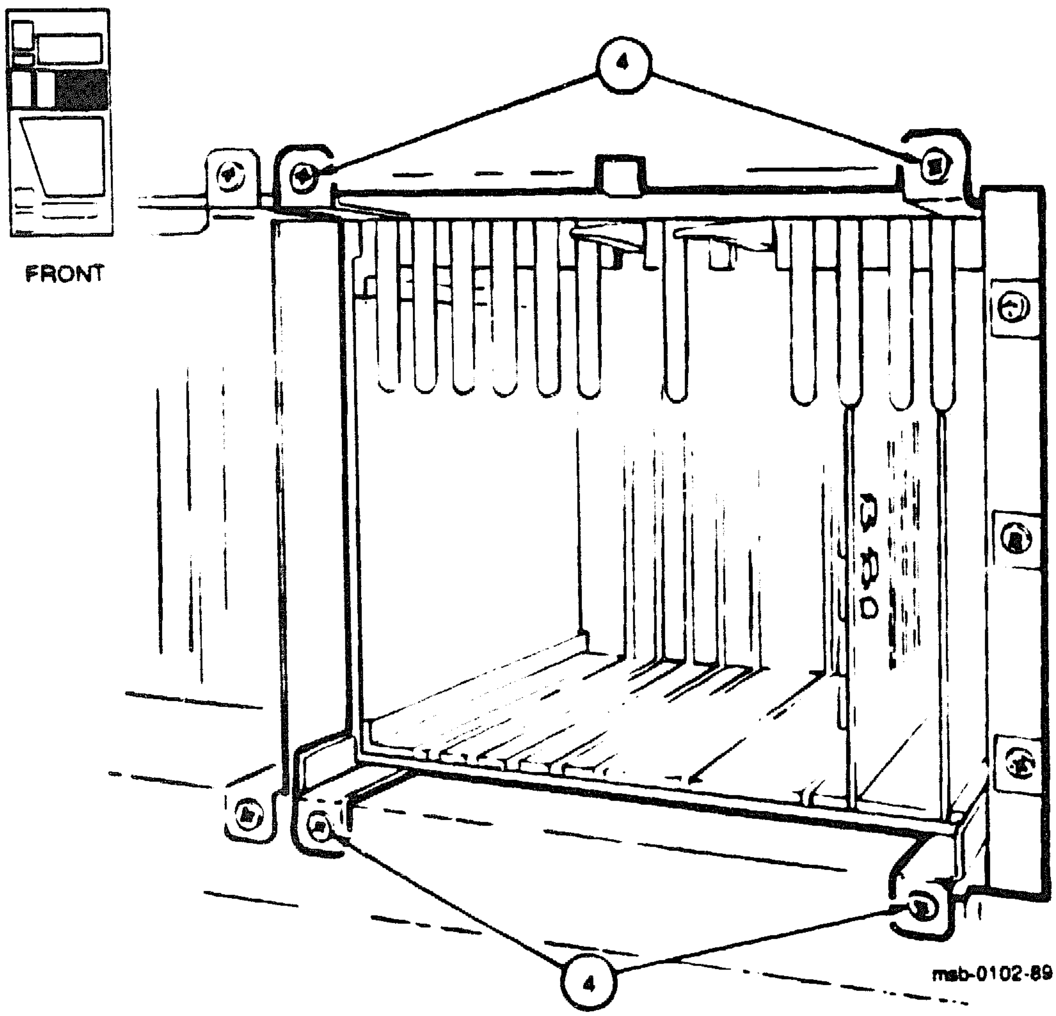
NOTE: *Figure 7–3 shows the end to disconnect for each of the following cables.*

7. Disconnect the cable to the XTC power sequencer (17-01568-02).
8. Disconnect the 8 cables (17-01897-02 and -03) between DWMBA/A modules (in the XMI card cage) and DWMBA/B modules (in the VAXBI card cage).
9. Disconnect four wires on the bus bars that go to the TK unit (17-01812-01): +5V; +12V; and two ground connections (use 11/32 inch nutdriver).
10. Disconnect the fail safe enable cable (17-01833-01) connection to +5VBB.
11. Disconnect the fail safe enable cable (17-01833-01) connection to ground.
12. Disconnect the cable to the H7215 power regulator (17-01566-01). (Remove connector from the regulator.)
13. Disconnect the harnesses to the two H7214 power regulators. (On each regulator, remove the four screws from the leads.)
14. Disconnect the lines to the two H7214 regulators (17-01525-01). (Remove connector from the regulator.)
15. Disconnect the ground strap to the chassis (17-01662-01). Remove the screw from the bus bar with a large Phillips screwdriver, and with your free hand catch the nut in back of the bus bar.

7.2.2 Removal of XMI Card Cage from Cabinet

Before removing the cage from the cabinet, remove all modules and set them aside.

Figure 7–4: XMI Card Cage



1. Open the front cabinet door.
2. Remove the clear plastic door in front of the XMI cage.

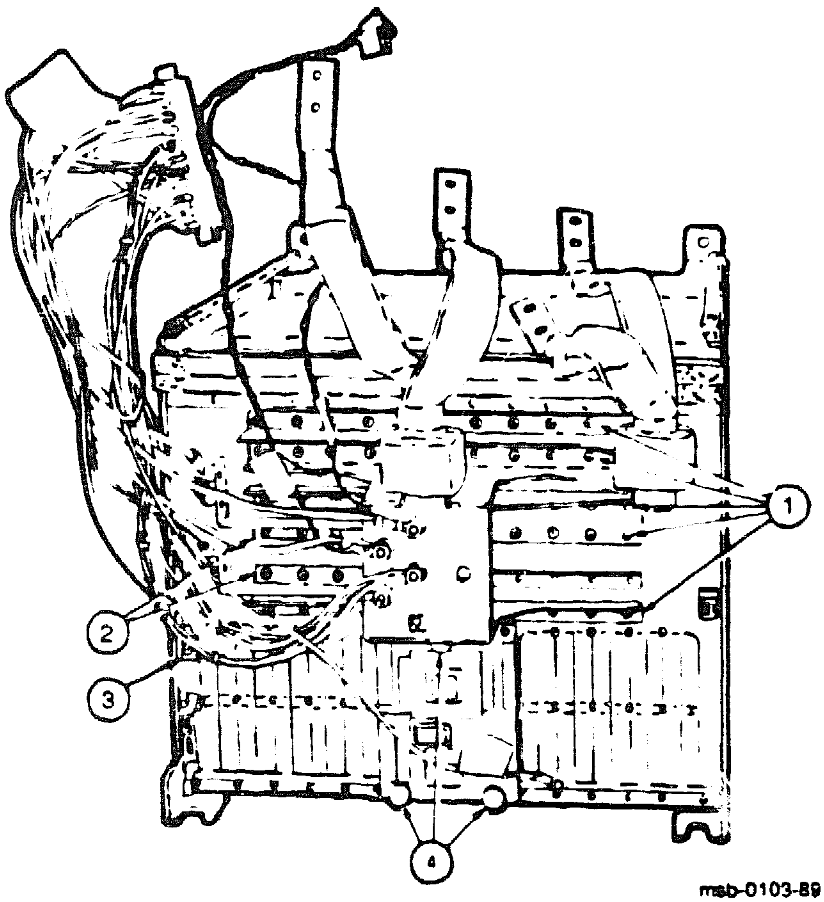
   CAUTION: *You must wear an antistatic wrist strap attached to the cabinet when you handle any modules.*

3. Lift up the levers and hold. Remove modules from the cage. Put them in protective bags or ESD boxes and note which slots they had been in.
4. Remove and save the four mounting screws that fasten the XMI cage assembly to the chassis (see Figure 7–4 for location of these screws).
5. Pull the cage out of the system cabinet carefully so that you do not damage the power harnesses or bus bars. Push from the back to ease the cage out toward the front of the cabinet.

7.3 Switching XMI Card Cages

The entire bus bar assembly, the daughter card (static sensitive), and the two side mounting plates must be removed from the XMI cage taken from the system and installed on the new XMI cage. Three pieces of foam air seal must be installed on the new cage.

Figure 7–5: XMI Bus Bar Assembly and Daughter Card



7.3.1 Removal of Bus Bars and Daughter Card

Remove the bus bars and daughter card as follows:

1. First remove the +5V/+5VBB/Ground bus bar assembly. Keep all screws and note where they came from. See ❶ in Figure 7–5.
2. Then remove the two smaller bus bars for -5.2V and -2V. See ❷.
3. Disconnect the blue cable at the far left that goes to -12V. See ❸.

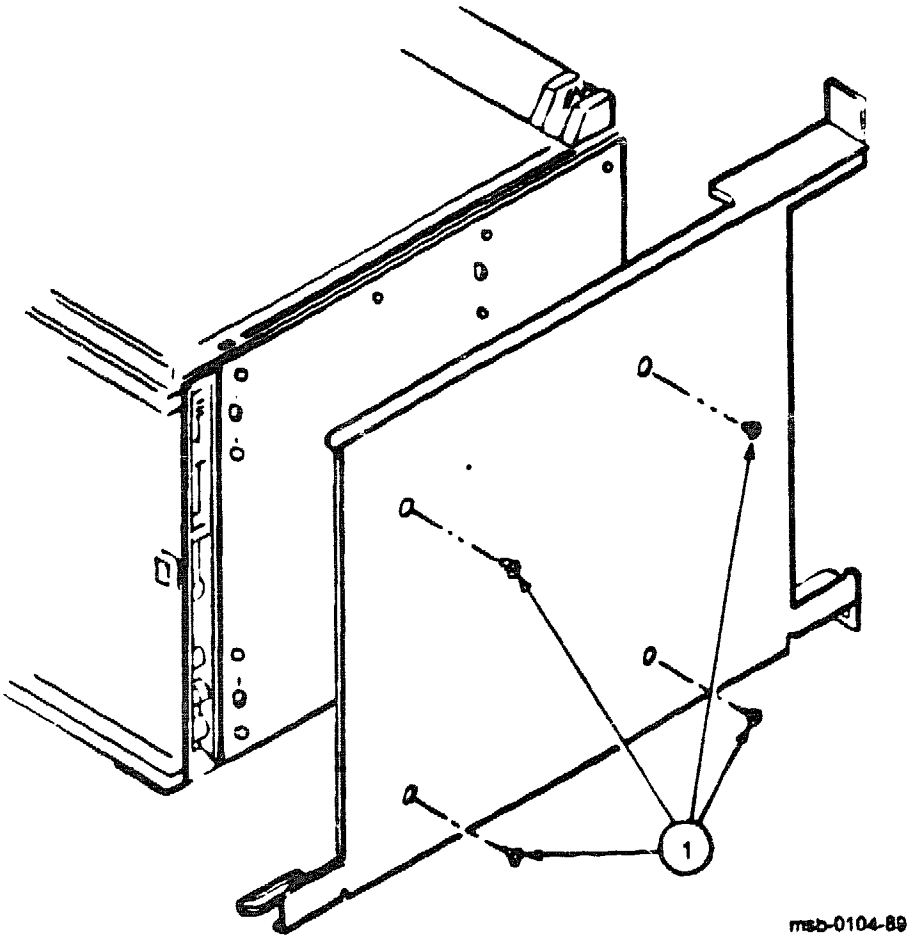
   CAUTION: *The daughter card is static sensitive. You must wear an antistatic wrist strap attached to the cabinet when you handle any modules.*

4. Unscrew the three large thumbscrews that hold the daughter card to the XMI backplane. See ❹.
5. Pull the daughter card away from the backplane.

7.3.2 Moving XMI Side Mounting Plates and Installation of Parts

Remove the two side mounting plates from the defective cage and install on the new cage (see Figure 7–6). Install on the new cage the bus bars and daughter card that you removed from the old cage. Install the new foam air seals.

Figure 7–6: XMI Cage Side Mounting Plates



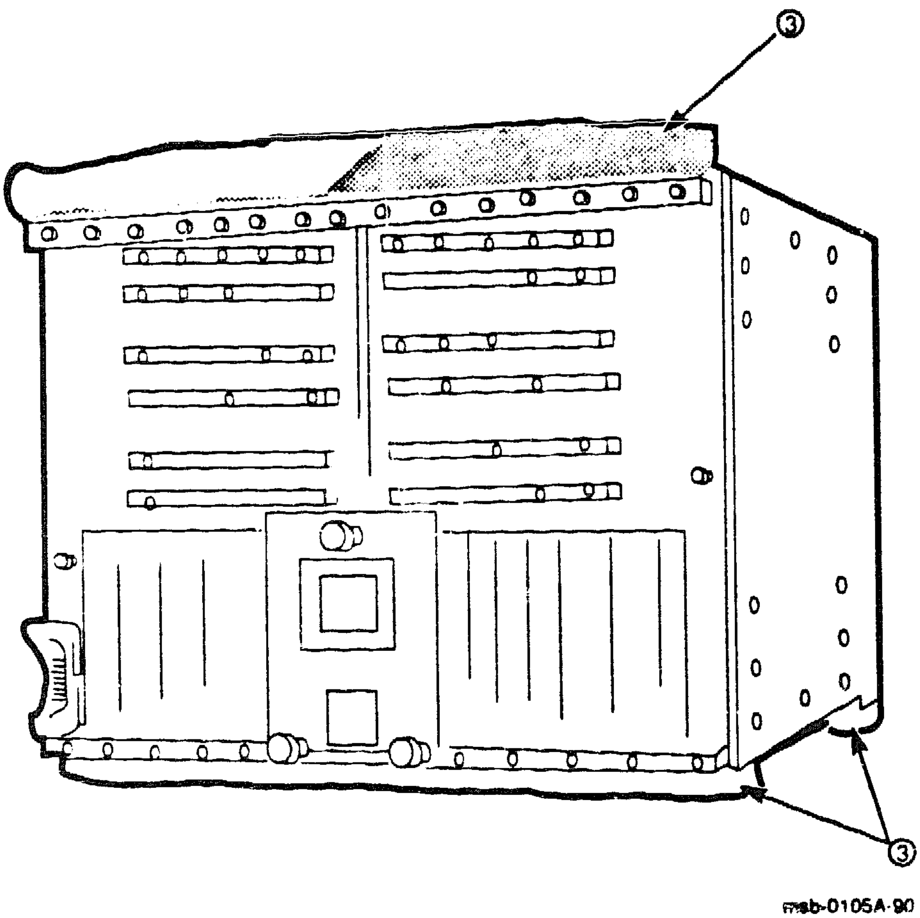
Perform the tasks in the following order:

1. Remove the two side mounting plates by removing four screws. See ❶ in Figure 7–6. Do not install these screws on the new cage yet.
2. On the new cage install the two smaller bus bars and then install the +5V/+5VBB/Ground bus bar assembly. Using the torque screwdriver from the VAXBI tool kit, torque screws to 9 (+/-1) inch-pounds.
3. Install the foam air seals in the locations shown in ❸ in Figure 7–7.
4. Install the side mounting plates.

   CAUTION: *The daughter card is static sensitive. You must wear an antistatic wrist strap attached to the cabinet when you handle it.*

5. Install the daughter card.

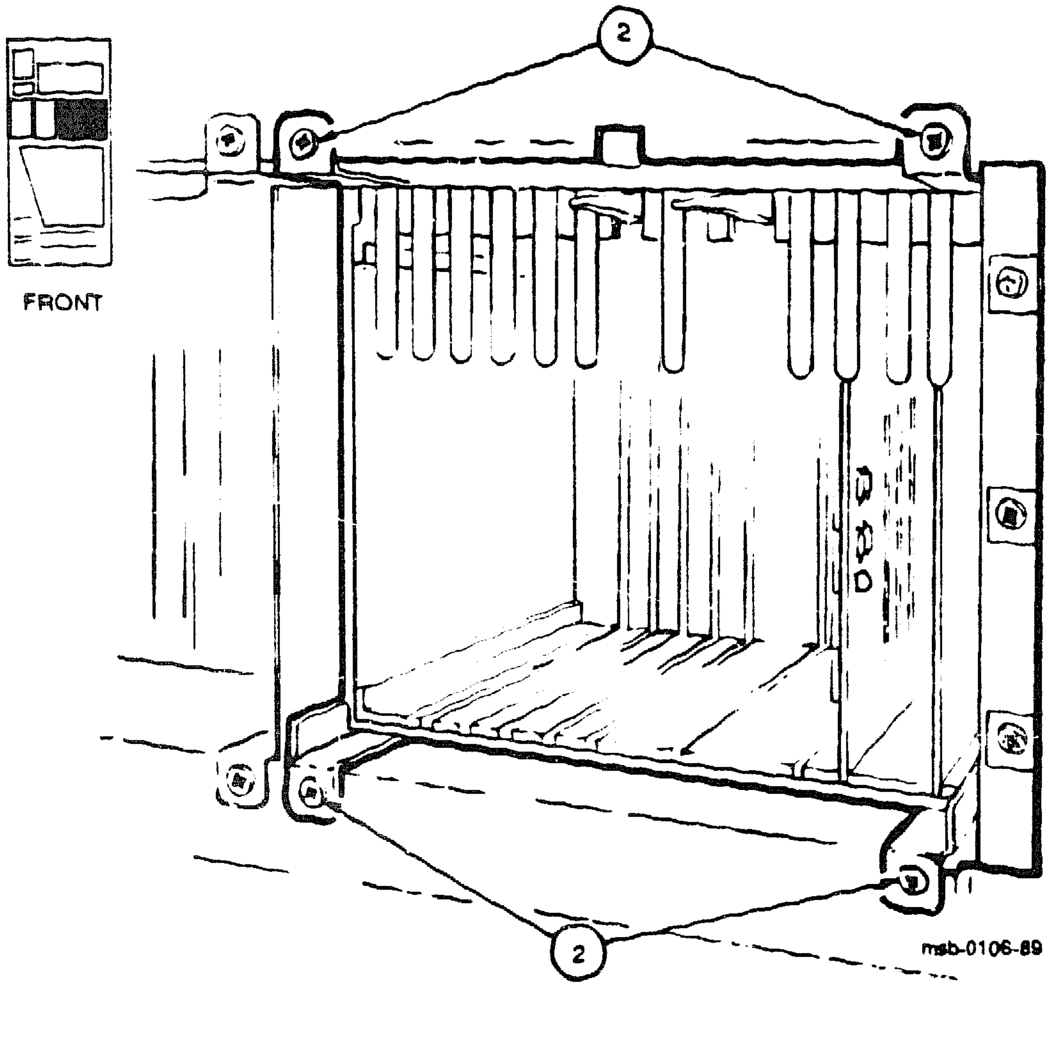
Figure 7–7: Installation of Foam Air Seals



7.4 XMI Card Cage Replacement

Return the new cage to the system cabinet. Reattach all the connections on the backplane, install the screws attaching the cage to the chassis, and then put the modules back into their slots (see Figure 7–8).

Figure 7–8: XMI Card Cage



The new XMI cage should be installed in the cabinet as follows:

1. Slide the XMI card cage into the system cabinet taking care not to damage the power harnesses or bus bars. Push from the front and pull from the rear.
2. Install the four mounting screws that secure the XMI cage assembly to the system cabinet. See ❷ in Figure 7–8.
3. Reattach the power connections.

   On the H7214 regulators, torque the screws to 27 (+/-5) inch-pounds.

   Make sure the two remote sense wires going to the two H7214 regulators go to the correct regulator. If they are switched, the +5V supplies may not turn on.
4. Reattach all signal connections.
5. Put the I/O bulkhead tray back into place at the rear of the cabinet.

   CAUTION: *You must wear an antistatic wrist strap attached to the cabinet when you handle any modules.*
6. Insert the modules into their correct slots.
7. Replace the clear door.
8. Turn on system power and check that all nodes pass self-test.

   NOTE: *See the Verification chapter in the VAX 6000–400 Installation Guide for complete acceptance instructions.*

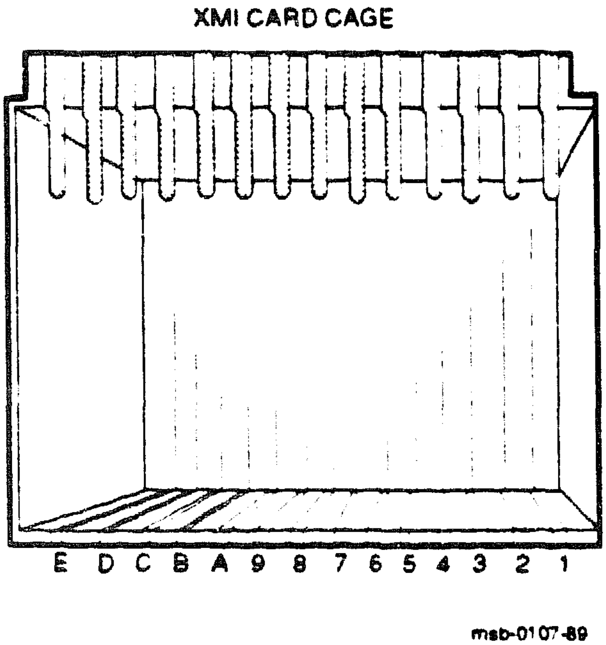
7.5 Installing Modules in the XMI Card Cage

The XMI card cage design and XMI architecture place some restrictions on the use of the slots.

- Slot 1 or slot E must hold a module. This module must be a KA64A or a DWMBA.
- No memory modules in slots 1 and E.
- No I/O modules in slots 5 through A.

Only XMI modules may be placed in the XMI card cage; installing any other modules may destroy the modules.

Figure 7–9: Numbering of XMI Slots



An XMI node takes its node number from the slot in which it resides. This is unlike the VAXBI bus where the node number assignment derives from node ID plugs inserted into the backplane for each slot.

CAUTION: *You must wear an antistatic wrist strap attached to the cabinet when you handle any modules.*

CAUTION: *You must hold the XMI card cage lever while removing or inserting a module in the XMI card cage. Failure to do so may result in damage to the module.*

Figure 7–9 shows the numbering of the slots in the XMI card cage. Slots are numbered in hexadecimal to correspond to the self-test display. Because the daughter card is mounted in the center of the XMI backplane, no I/O cables can be connected to slots 6 through 9. Also, no I/O modules are to go in the two adjoining slots, 5 and A. Another configuration restraint is that either the first or last slot in the cage must house a non-memory module. If no module is in either slot, the XMI shuts down. Memory modules must not be placed in the first and last slots.

Any problems with the XMI cage or modules are indicated in the first three lines of the self-test display (see Section 2.2 for an explanation of these lines).

CAUTION: *Never attempt to insert a VAXBI module into an XMI card cage. The backplane technology for the XMI and VAXBI is similar but incompatible. Inserting a VAXBI module into an XMI card cage can destroy the module. Note that VAXBI modules are shorter than XMI modules.*

7.6 XMI Troubleshooting

When you install modules in the XMI card cage, several items need to be checked. Table 7-3 gives a checklist of items to troubleshoot.

Table 7-3: XMI Troubleshooting Checklist

Symptom	Possible Cause
No power to cages	Clear plastic door not in place or not latched.
Intermittent module response	Poor contact at connector
	Loose cabling at the backplane
Module does not appear on self-test results	Loose cabling at the backplane
	System not configured correctly.

The XMI and VAXBI card cages are in back of clear plastic doors.

NOTE: *If these doors are opened when power is still on, a power interlock switch cuts off power from the regulators to either the VAXBI side or to the XMI side, depending on the door opened.*

Before turning power back on, make sure the clear plastic doors are in place and latched. You can then push the reset switch on the H7206 PAL unit (see Figure 9-9) to return power to the system.

The XMI bus requires a non-memory module in slots 1 or E. If both of these slots are empty, the bus will shut down.

CAUTION: *Inserting a memory module in slot 1 or E will damage the memory module.*

If you receive intermittent module response, or the module does not show up on self-test as being present at all, make sure that the module is seated properly, and check the backplane cabling.

Modules may fail self-test because of poor contact at the connector. A thorough cleaning of the gold pads on the module and of the connector in the card cage corrects this contact failure. If the connections seem to be faulty, clean the contact areas of the connector and module. Table 7–4 lists tools and supplies for connector cleaning.

Table 7–4: XMI Connector Cleaning Supplies

Item	Part Number	Function
VAXBI tool kit	A2-M1094-10	Maintaining card cages
Paddle wipe handle	47-00116-02	Holding paddle wipes
Paddle wipes	12-26321-01	Cleaning contact area inside ZIF connectors
Gold-wipes™	49-01603-00	Cleaning module connector contact area
Protective goggles	29-16141-10	Eye protection
Nitrile gloves	29-26403-00	Hand protection

™Gold-wipes is a trademark of TEXWIPE.

CHAPTER 8

Chapter 8

VAXBI Card Cage

This chapter describes the VAXBI card cage and its use in the VAX 6000–400 system. Removal and replacement procedures are detailed, and configuration restrictions are listed. Sections include:

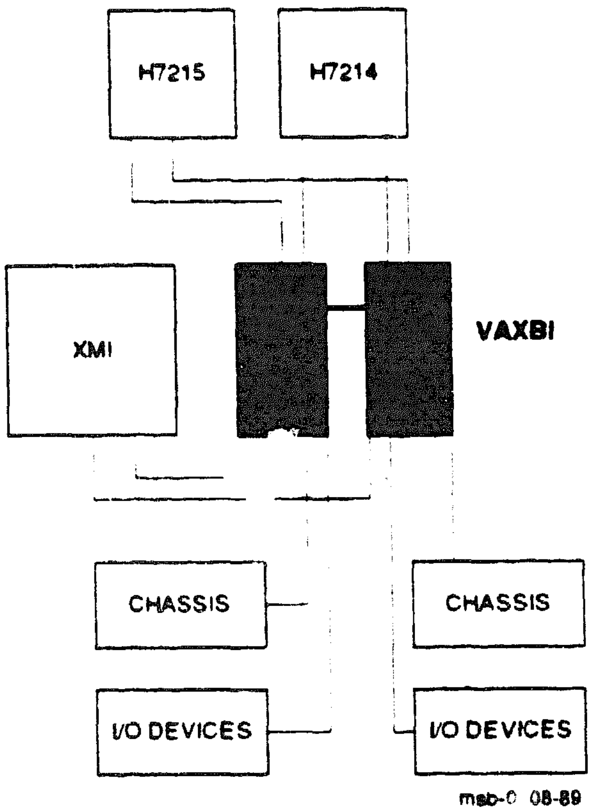
- VAXBI Card Cage Description
  - System Use
  - Specifications
  - Subassemblies
- VAXBI Card Cage Removal
- Switching VAXBI Cages
- VAXBI Card Cage Replacement
- VAXBI Expansion and Configuration Rules
- VAXBI Troubleshooting

8.1 VAXBI Card Cage Description

8.1.1 System Use

The VAXBI card cage serves as the I/O subsystem of the VAX 6000–400 system. Each processor cabinet has two VAXBI card cages, each providing a separate VAXBI channel. The interface between the VAXBI bus and the XMI bus is the DWMBA option. The DWMBA/B module requires one slot in the VAXBI card cage.

Figure 8–1: VAXBI Card Cage Connections



The VAX 6000–400 system uses the VAXBI bus for input/output. Each system has two VAXBI card cages, which provide two VAXBI channels of six slots each. A VAXBI expander cabinet can also be added, which can hold up to four VAXBI cages.

The VAXBI card cage has zero insertion force (ZIF) connectors. The backplane area extends over two of the five connector segments; the remaining three segments are used for I/O connections. Installed on the cage are I/O transition headers.

Each VAXBI bus has its own XMI-to-VAXBI adapter (DWMBA). The DWMBA/B module of this adapter resides in the VAXBI card cage.

8.1.2 VAXBI Card Cage Specifications

The VAXBI card cage (see Figure 8-2) is a 6-slot cage. The VAXBI card cages are located in the upper part of the cabinet, on the left as you view the system from the front. The field-replaceable unit (H9400-AA) does not include the power bus bar assembly, the node ID plugs, and the terminators. Two cages configured as two separate VAXBI channels are in each system cabinet.

Figure 8-2: VAXBI Card Cages

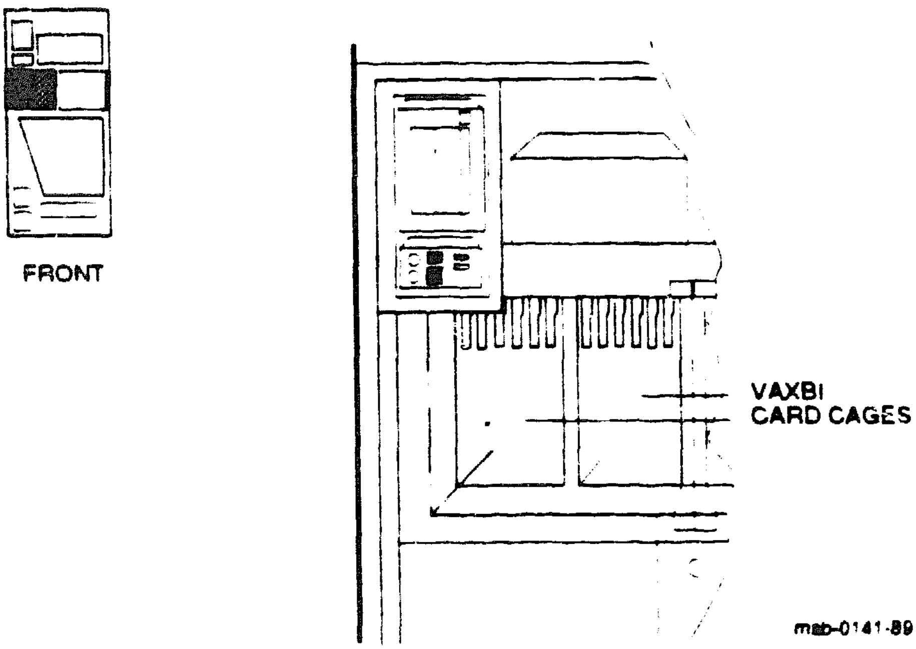


Table 8–1: VAXBI Card Cage Assembly Specifications

Parameter	Description
VAXBI Card Cage	H9400-AA, one 6-slot cage with no terminators or bus bars; includes transition headers
Location:	Upper left front
Dimensions:	12.5" W x 9.5" D x 10" L
Weight:	26 lbs (2-cage assembly)
Power:	One H7215 DC regulator and one H7214 DC regulator supply power to the 2-cage assembly.
Service From:	Front and rear

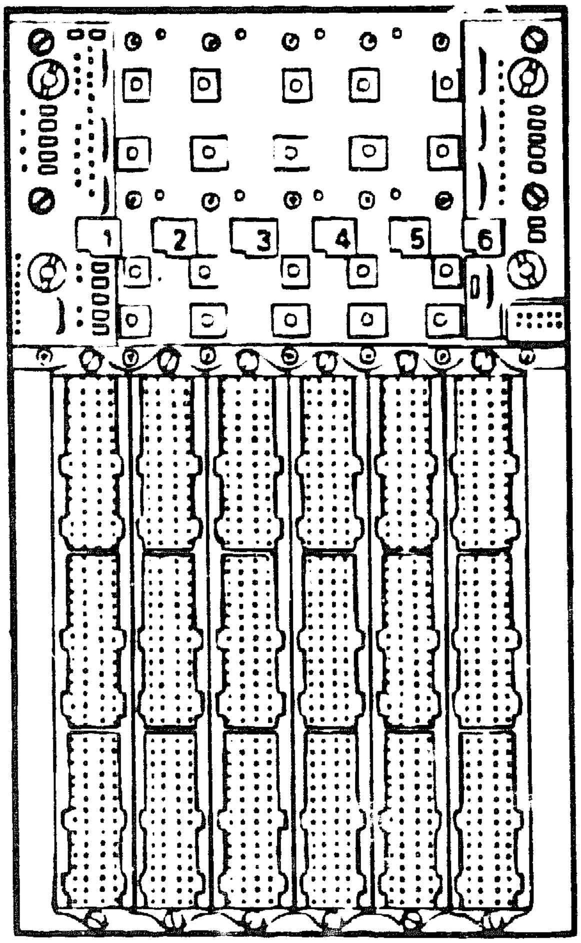
Table 8–2: VAXBI Card Cage Cables

Part Number	Description
17-00849-08	18" DWMBA/B to DWMBA/B AC/DC OK cable, from VAXBI cage 2 slot 1 (segment C2) to VAXBI cage 1 slot 1 (segment C1).
17-01149-01	Firmware console-enable jumper (on Ethernet adapter slot, slot 6, segment E1)
17-01458-02	VAXBI ground strap
17-01496-01	Ethernet (from slot 6, segment E2, to H7214 (+13V) and to Ethernet port)
17-01523-01	VAXBI +/-12V to J3 on H7215
17-01569-01	DWMBA, from slot 1, segment C1, to J11 of H7206
17-01897-01	15' DWMBA cables for expander cabinet, from XMI slots C, B, 1, and 2 as needed (segments D and E) to VAXBI cages 3, 4, 5, and 6 slot 1 (segments D and E). Two per DWMBA.
17-01897-02	7" DWMBA cables, from XMI slot E (segments D and E) to VAXBI cage 2 slot 1 (segments D and E). Two per DWMBA.
17-01897-03	25" DWMBA cables, from XMI slot D (segments D and E) to VAXBI cage 1 slot 1 (segments D and E). Two per DWMBA.
17-01920-01	AC/DC OK cable, from VAXBI slot 1, segment C1. Installed in system to provide for expansion to VAXBI expander cabinet.

8.1.3 VAXBI Card Cage Subassemblies

Table 8–3 lists the part numbers for FRUs of the VAXBI card cage assembly in the VAX 6000–400 system.

Figure 8–3: VAXBI Card Cage Subassemblies



msb-0109-89

Table 8–3: VAXBI Subassemblies and Tools Required

Item	Part Number	Description
Subassemblies:		
Bus Bar Assembly	12-28508-01	+5V/+5VBB/Ground VAXBI bus bars
	12-28342-01	-5.2V VAXBI bus bars
	12-28345-01	-2V VAXBI bus bars
Terminators	20-24486-01	Near end (GIF)
	20-24487-01	Far end (GOM)
VAXBI Node IDs	12-23701-17	Set of 16
Transition Header	12-22246-01	Three-segment I/O header
Foam Air Seals	74-34536-01	Three pieces of foam used for air seals
	74-34536-02	
	74-34536-03	
Tools Required:		
VAXBI Tool Kit	A2-M1094-10	Includes: Torque screwdriver Offset ratchet screwdriver Large and small Phillips screwdrivers Small Phillips screw-holding screwdriver or one with magnetic tip Flat screwdriver

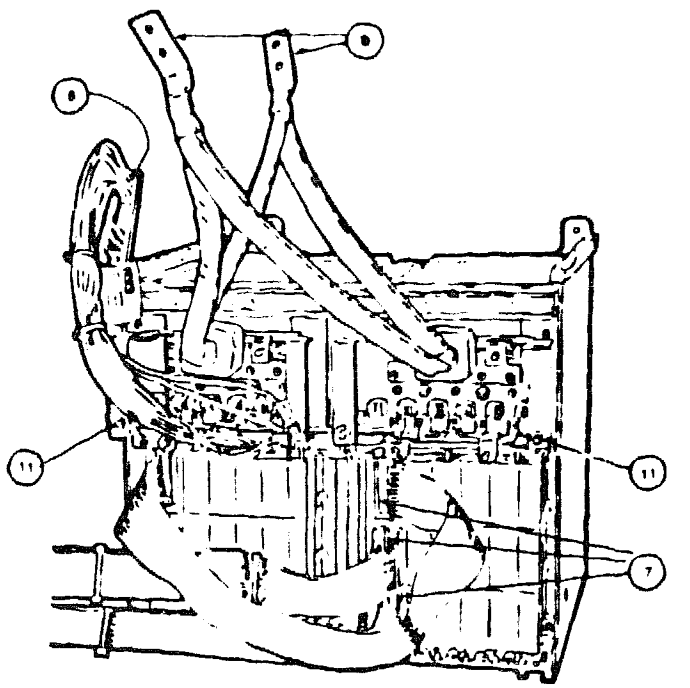
8.2 VAXBI Card Cage Removal

The two VAXBI card cages are bolted together and must be removed as a unit. Remove them from the front of the cabinet after you disconnect connections at the backplane. You must remove the system control assembly before you can remove the VAXBI card cage assembly (see Chapter 8 for instructions).

8.2.1 Prepare for Removal

Prepare the system for shutdown. Set up a work space nearby where you can store the modules and work on the VAXBI card cages. Label and disconnect the signal and power connections.

Figure 8–4: VAXBI Backplane Cables and Power Connections



msb-0192R-89

The VAXBI card cage assembly, which contains both cages, slides out the front of the system cabinet. Before attempting to remove the assembly, detach cables from other system components that go to the backplanes of both cages.

1. Perform an orderly shutdown of the system.
2. Turn the upper key switch on the front control panel to the Off position.
3. Pull the circuit breaker on the AC power controller to the Off position.
4. Unplug the machine.

   NOTE: *You must first remove the system control assembly; see Chapter 8 for the removal procedure.*

5. Open the rear cabinet door.
6. Drop the I/O panel to expose the card cages.

   CAUTION: *You must wear an antistatic wrist strap attached to the cabinet when you handle any modules.*

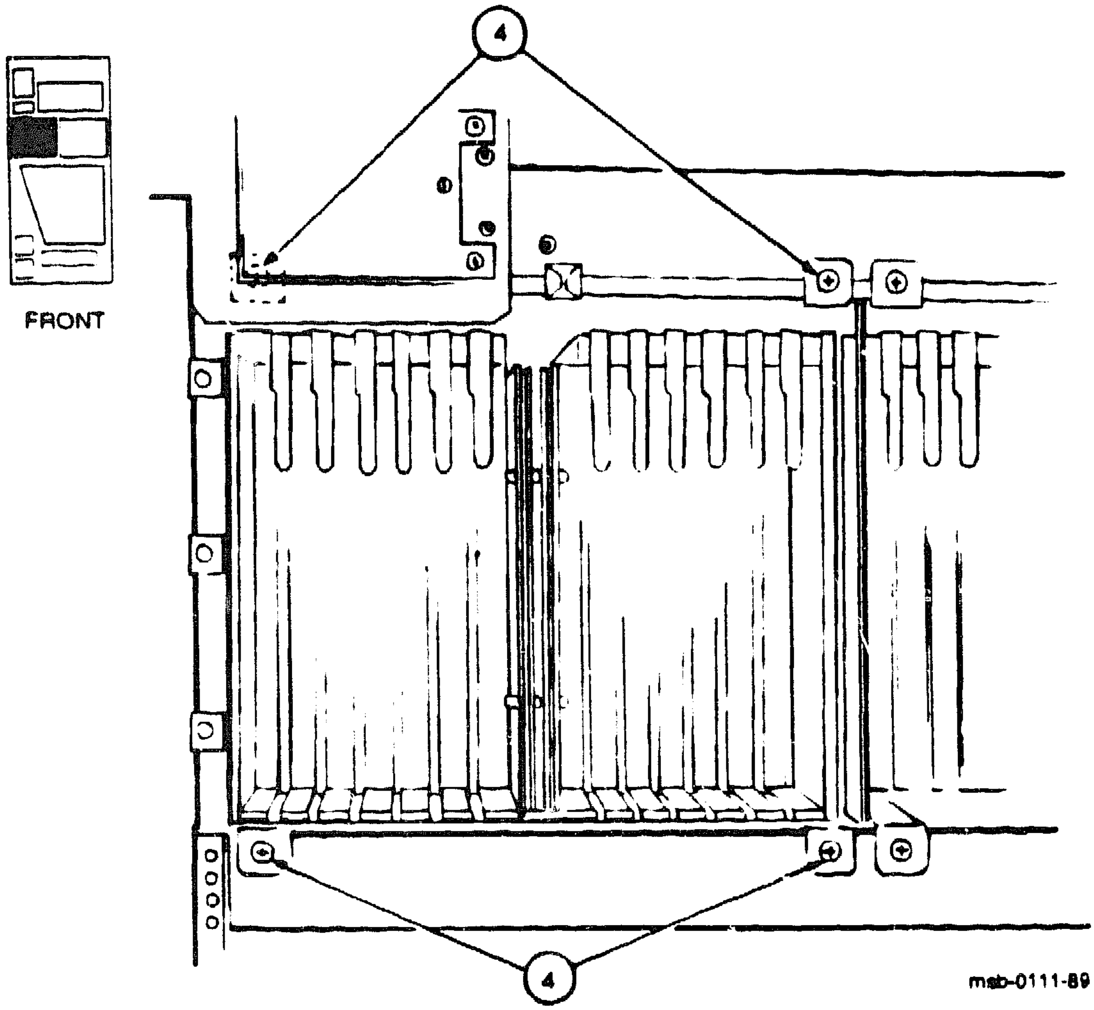
   NOTE: *Figure 8–4 shows the end to disconnect for each of the following cables.*

7. Remove all connectors from segments C, D, and E of the transition headers. For the CIBCA and KDB50, instead of removing cables, remove the transition headers from the card cage, since the I/O segment is a permanent part of the transition header. To do this, remove the top and bottom screws, and then remove the header.
8. Disconnect the cable to the H7215 power regulator (17-01523-01). (Remove connector from the regulator.)
9. Disconnect the harness to the H7214 power regulator. (On the regulator, remove the four screws that fasten the harness to the regulator.)
10. Disconnect the Ethernet line to the H7214 regulator (17-01525-01) from each cage with a DEBNI adapter. (Remove connector from the lower half of J1 on the H7214 regulator. This connection is not shown on Figure 8–4.)
11. Disconnect the ground strap from each cage to the chassis (17-01458-02).

8.2.2 Removal of VAXBI Card Cages from Cabinet

Before removing the cages from the cabinet, remove all modules and set them aside.

Figure 8–5: VAXBI Card Cages



1. Open the front cabinet door and lift it from its hinges to provide more clearance.
2. Remove the clear plastic door in front of the VAXBI cage area.

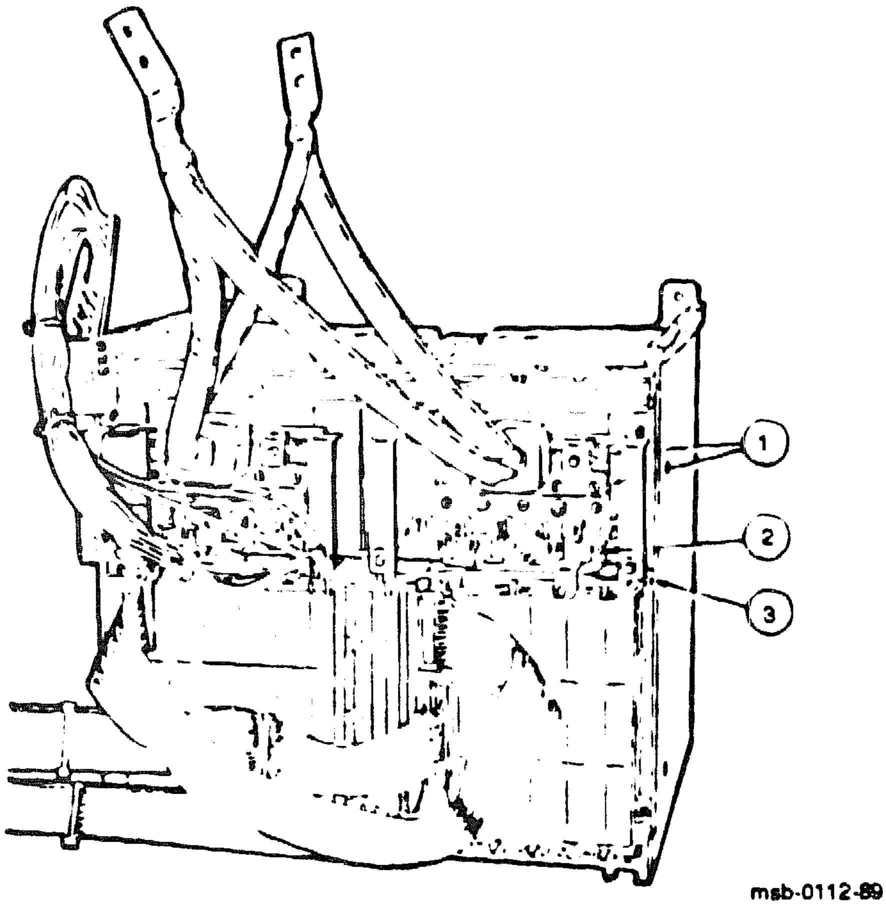
   CAUTION: *You must wear an antistatic wrist strap attached to the cabinet when you handle any modules.*

3. Lift up the levers to remove modules. Put them in protective bags and note which slots they had been in.
4. Remove and save the four mounting screws that fasten the VAXBI assembly to the chassis (see Figure 8–5 for location of these screws).
5. Pull the cages out of the system cabinet carefully so that you do not damage the power harnesses or bus bars.

8.3 Switching VAXBI Cages

The following sections contain directions for switching a cage.

Figure 8–6: VAXBI Bus Bar Assembly



8.3.1 Removal of VAXBI Bus Bars

On ONLY the cage that needs to be swapped out of the two-cage assembly, remove the bus bars in the following order:

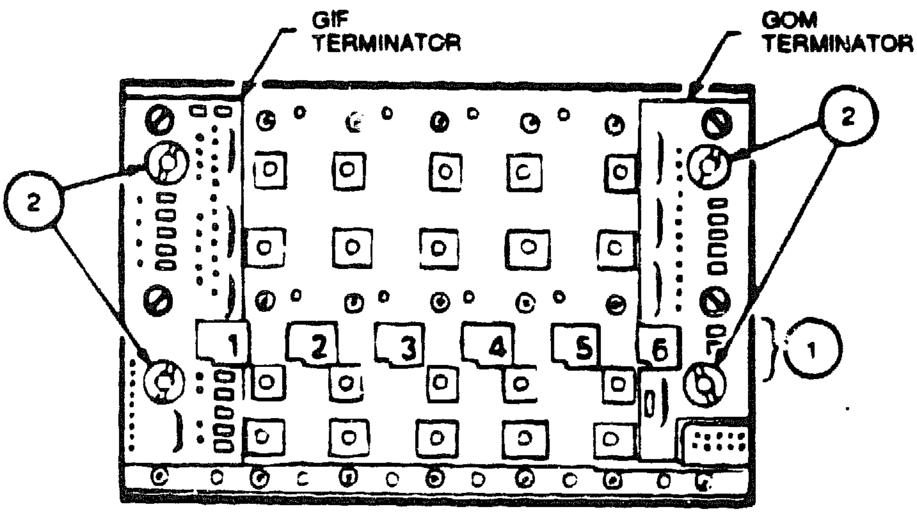
1. First remove the +5V/+5VBB/Ground bus bar assembly (12-28508-01), 14 screws. See ❶ in Figure 8–6.
2. Next remove the -5.2V and -2V bus bars (5 screws into the power cubes). See ❷.
3. Disconnect the +/-12V connection (17-01523-01) to the H7215 regulator. See ❸.

Use a small Phillips screwdriver (#6-32 screws). See Figure 8–6 for a detailed view of the VAXBI bus bar assembly.

8.3.2 Removal of Other VAXBI Parts

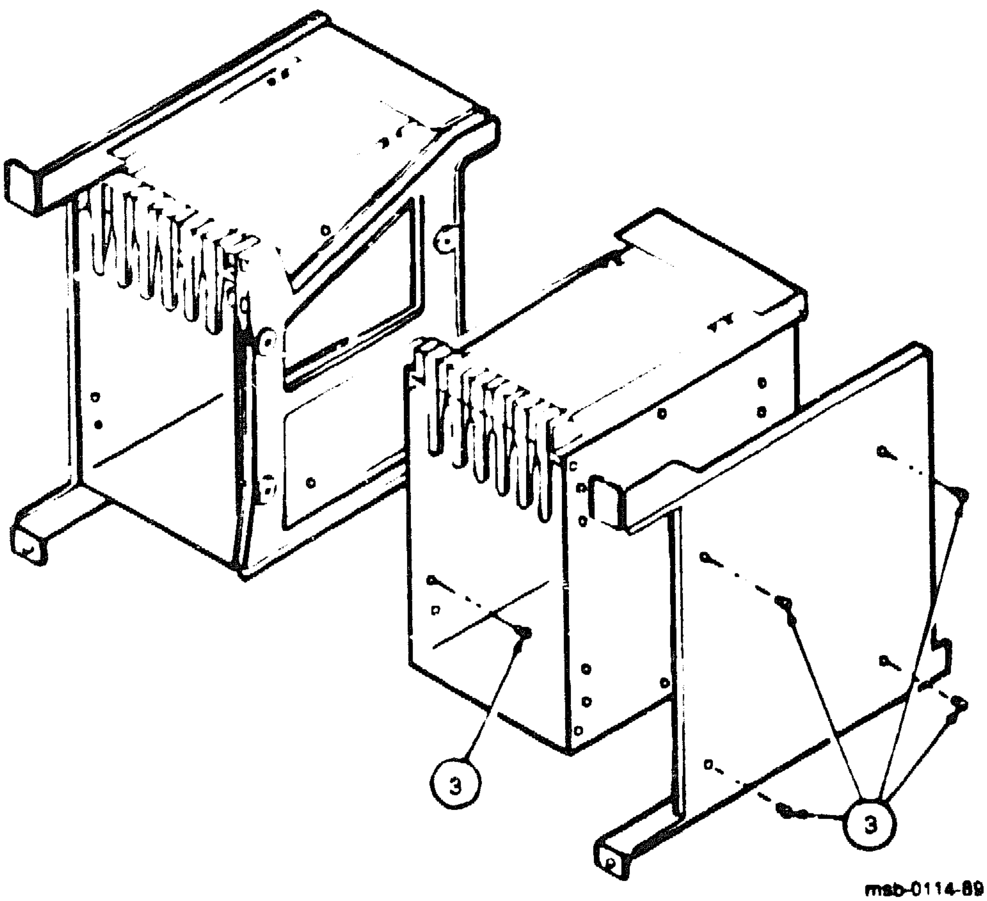
Remove the node ID plugs, the terminators, and the mounting plates from the old cage (see Figure 8-7 for their locations).

Figure 8-7: VAXBI Backplane Components



1. Remove the node ID plugs. See ❶ in Figure 8–7.
2. Remove the terminators by removing the two screws. See ❷.
3. Remove the side and inner mounting plate so that you can slide the defective cage away from the remaining cage. For the inside plate, remove the innermost screws with an offset ratchet screwdriver. See ❸ in Figure 8–8.

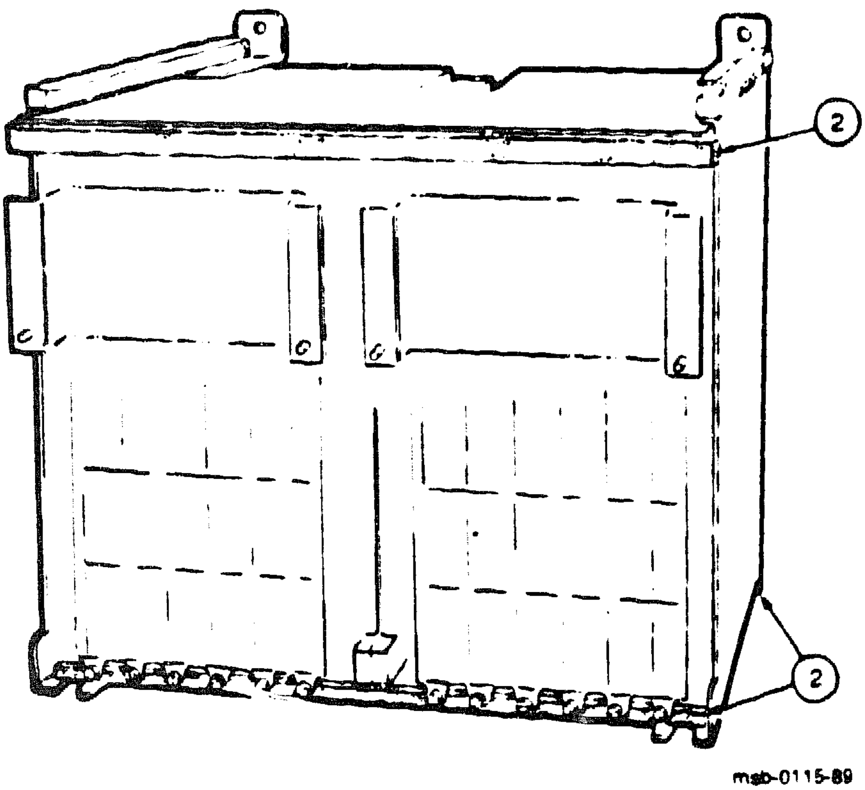
Figure 8–8: VAXBI Cage Mounting Plates



8.3.3 Installation of VAXBI Parts

Install the terminators, node ID plugs, and bus bar assembly taken from the old cage. Attach the side and inner mounting plates. Finally, install new foam air seals.

Figure 8-9: Installation of Foam Air Seals

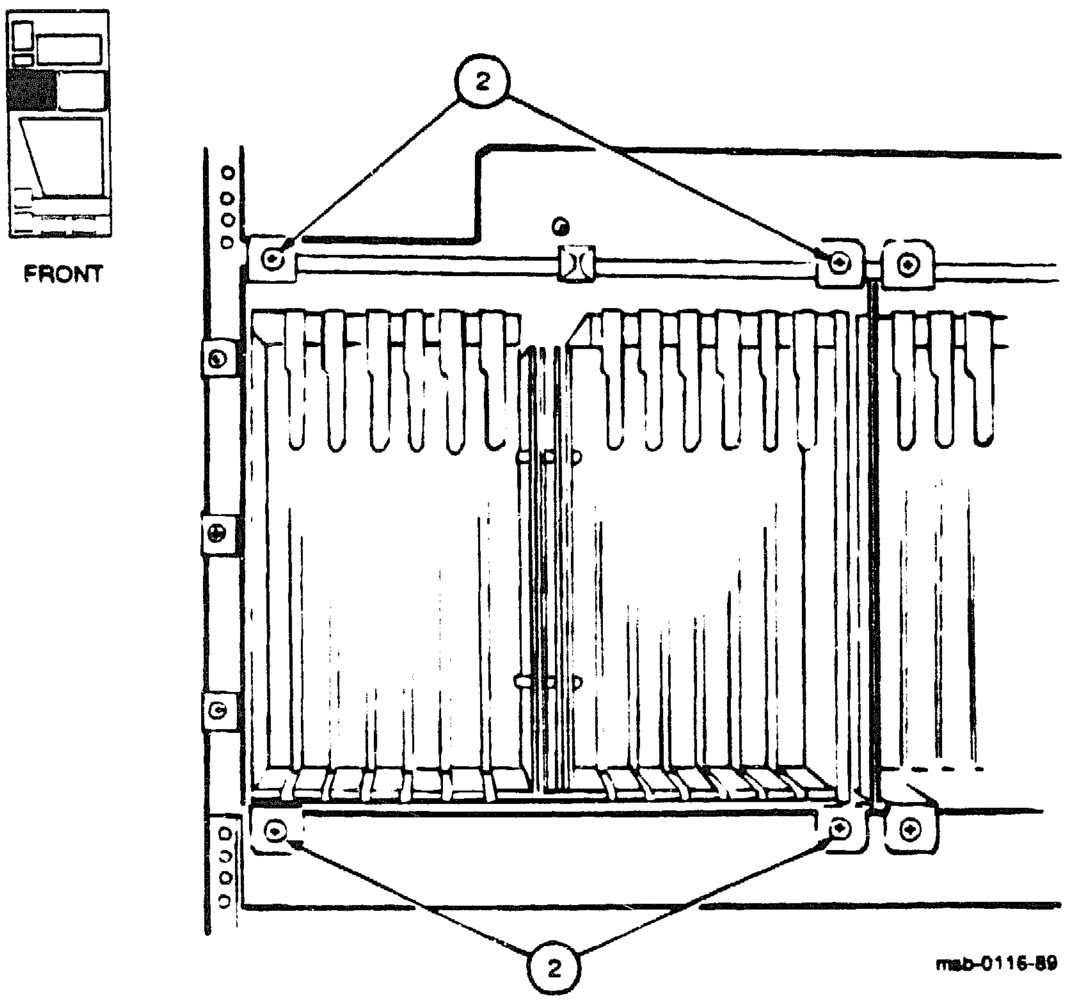


1. On the replacement cage, install the parts that you removed from the defective VAXBI card cage:
   - Terminators
   - Node ID plugs
   - Bus bar assembly, in the reverse order of the removal. Torque screws to 9 (+/-1) inch-pounds.
   - Side and inner mounting plates
2. Three foam air seals need replacement: the top front of the backplane and the bottom surfaces of the cages, back and front. See ❷ in Figure 8–9.
3. The new cage, the H9400-AA, is shipped with six transition headers installed. For the slots that are to hold the CIBCA and KDB50 options, remove the transition headers.

8.4 VAXBI Card Cage Replacement

Return the two-cage assembly to the system. Reattach all the connections on the backplane, install the screws attaching the cage to the chassis, and then put the modules back into their slots (see Figure 8–10).

Figure 8–10: VAXBI Card Cages



The VAXBI cage assembly should be installed in the cabinet as follows:

1. Slide the VAXBI card cages into the system cabinet taking care not to damage the power harnesses or bus bars. You will also need to pull the cages from the back.
2. Install the four mounting screws that secure the VAXBI cage assembly to the system cabinet. See ❷ in Figure 8–10.
3. Reinstall the system control assembly (see Chapter 8 for instructions).
4. Screw on the transition headers containing the CIBCA and KDB50 cables. Tighten the screws in stages: do not tighten one completely before tightening the other. Torque both screws to 6 (+/-1) inch-pounds, using the torque screwdriver.
5. Attach the other signal connections in the I/O area.
6. Reattach the power connections.

   At the H7214 regulator, torque screws to 27 (+/-5) inch-pounds.

   On the bus bars torque screws to 9 (+/-1) inch-pounds.
7. Put the I/O bulkhead tray back into place at the rear of the cabinet.

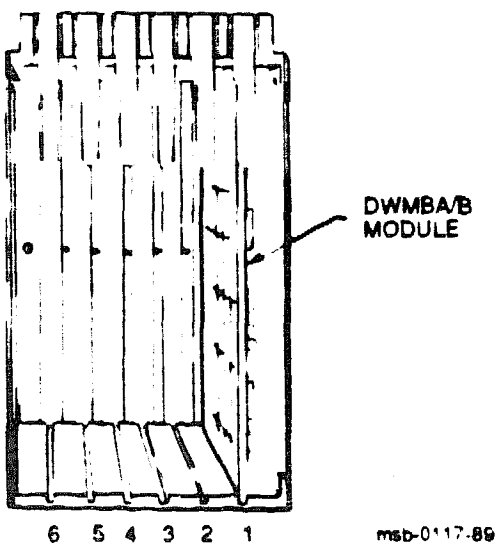
   CAUTION: *You must wear an antistatic wrist strap attached to the cabinet when you handle any modules.*
8. Insert the modules into the VAXBI card cages
9. Replace the clear door.
10. Turn on system power and check that all nodes pass self-test.
11. Rehang the front cabinet door.

    NOTE: *See the Verification chapter in the VAX 6000–400 Installation Guide for complete acceptance instructions.*

8.5 VAXBI Expansion and Configuration Rules

The system cabinet has two VAXBI cages configured to provide two VAXBI channels for I/O. One of the six slots holds the XMI-to-VAXBI adapter module, leaving five slots for I/O modules. Four more cages can be installed in a VAXBI expander cabinet to provide four additional VAXBI channels, for a total of six VAXBI channels. A total of 30 slots is available for I/O adapters.

Figure 8-11: Numbering of VAXBI Slots



The cage and backplane were designed so that any module or node can reside in any slot (except slot 1). On the VAXBI bus, the module that drives the clock must reside in the first slot (see Figure 8–11 for the numbering of VAXBI slots). In the VAX 6000–400 system the DWMBA/B module of the XMI-to-VAXBI adapter drives the clock and therefore must reside in slot 1.

VAXBI node numbers derive from node ID plugs that plug into the backplane. A node, which can be more than one module, is assigned the node number of the plug that is inserted into the slot of the module with the VAXBI Corner. Multimodule nodes must be in adjacent slots.

Constraints on adding VAXBI options include:

- Power requirements for the options
- Memory latency time needed to access MS62A memory

See the *VAX Systems and Options Catalog* for VAXBI option configurations in VAX 6000–400 systems. See Appendix B of the *VAXBI Options Handbook* for power requirements of various options. The DWMBA/B module requires 6 amps.

8.6 VAXBI Troubleshooting

When you install modules in the VAXBI card cages, several items need to be checked. Table 8–4 gives a checklist of items to troubleshoot.

Table 8–4: VAXBI Troubleshooting Checklist

Symptom	Possible Cause
No power to cages	Clear plastic door not in place or not latched.
Intermittent module response	Poor contact at connector
	Loose cabling at backplane
Module does not appear on self-test results	Loose cabling at backplane
	System not configured correctly

The XMI and VAXBI card cages are in back of clear plastic doors.

NOTE: *If these doors are opened when power is still on, a power interlock switch cuts off power from the regulators to either the VAXBI side or to the XMI side, depending on the door opened.*

Before turning power back on, make sure the clear plastic doors are in place and latched. You can then push the reset switch on the H7206 PAL unit (see Figure 9-9) to return power to the system.

If you receive intermittent module response, or the module does not show up on self-test as being present at all, make sure that the module is seated properly, and check the backplane cabling.

Modules may fail self-test because of poor contact at the connector. A thorough cleaning of the gold pads on the module and of the connector in the card cage corrects this contact failure. If the connections seem to be faulty, clean the contact areas of the connector and module. Table 8–5 lists tools and supplies for connector cleaning.

Table 8–5: VAXBI Connector Cleaning Supplies

Item	Part Number	Function
VAXBI tool kit	A2-M1094-10	Maintaining card cages
Paddle wipe handle	47-00116-02	Holding paddle wipes
Paddle wipes	12-26321-01	Cleaning contact area inside ZIF connectors
Gold-wipes™	49-01603-00	Cleaning module connector contact area
Protective goggles	29-16141-10	Eye protection
Nitrile gloves	29-26403-00	Hand protection

™Gold-wipes is a trademark of TEXWIPE

CHAPTER 9

Chapter 9

Control Subsystem Assemblies

This chapter describes the specifications and maintenance of the system control assembly and its subassemblies. Sections include:

- System Control Assembly Specifications
- System Control Assembly Removal and Replacement
- XTC Power Sequencer Specifications
- XTC Removal and Replacement
- Control Panel Assembly Specifications
- Control Panel Assembly Removal and Replacement
- TK Tape Drive Specifications
- TK Tape Drive Removal and Replacement
- Filter Board and TOY Clock Battery Specifications
- Filter Board and TOY Clock Battery Removal and Replacement

9.1 System Control Assembly Specifications

The system control assembly is located in the upper left front corner of the cabinet. It houses the separate FRUs of the control panel, TK tape drive, the XTC, and the battery powering the TOY clock. The system control assembly's part number is 70-24903-01.

Figure 9–1: System Control Assembly

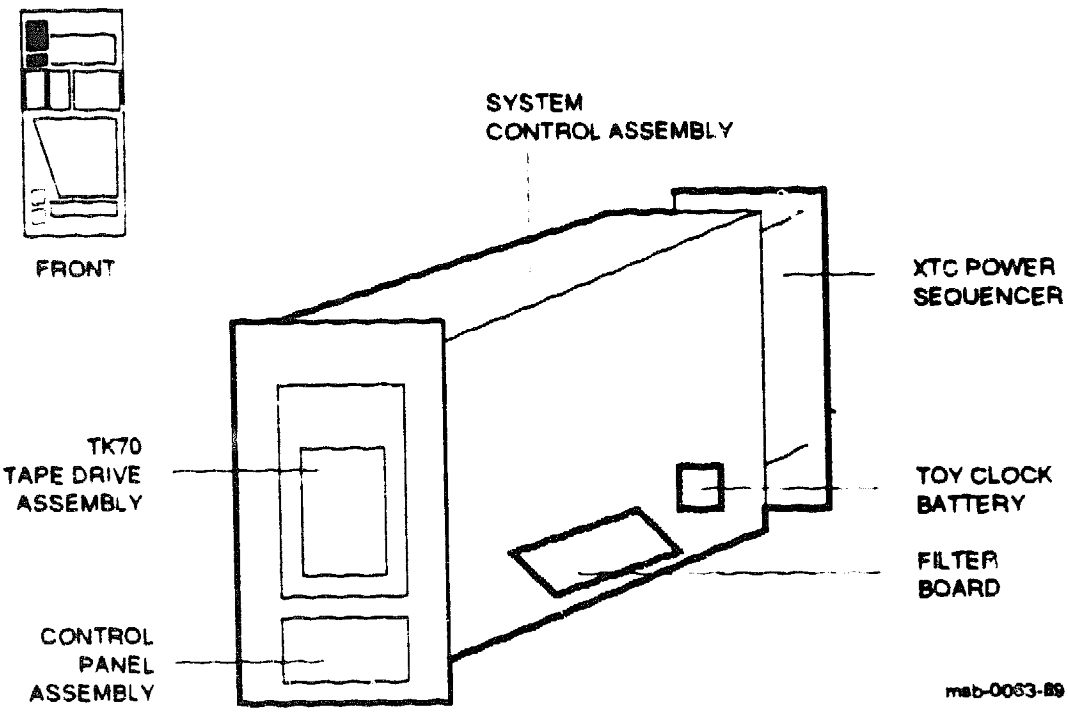


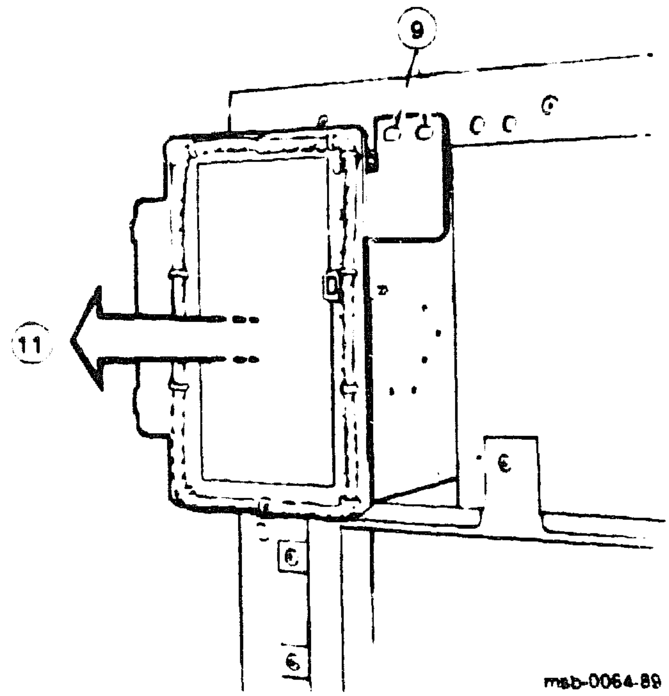
Table 9–1: System Control Assembly Specifications

Parameter	Description
Part Number:	70-24903-01
Location:	Upper left front
Dimensions:	11.25" H x 8.5" W x 17.5" D
Weight:	18 lbs, with TK and control panel installed
Signal Cables:	17-01814-01 from the control assembly shield leading to the TBK70 adapter's slot at VAXBI backplane segment D
Service From:	Front and rear of cabinet, front door removed
Tools Required:	Large and small Phillips screwdrivers
Subassemblies:	Control panel assembly (54-16574-01) XTC power sequencer (54-17243-01 or 20-29176-01) TK tape drive (TK70-AA) TOY 3-cell battery (12-19245-02)
Diagnostics:	Control panel assembly lights will light when the control assembly is correctly installed.

9.2 System Control Assembly Removal and Replacement

Working mainly from the front of the cabinet, remove or replace the system control assembly using a large and small Phillips screwdriver. The assembly has four screws on the front of the assembly, two screws on the back of the assembly, and one cable.

Figure 9–2: System Control Assembly Removal



REMOVAL

1. Perform an orderly shutdown of the system.
2. Turn the control panel upper key switch to the Off position.
3. Pull the circuit breaker switch and unplug the machine.
4. Open and remove the front door. (See Section 11.1.) Open the rear door.

5. Remove the four power cords (orange, black, red, and black) from the back of the console assembly using a large Phillips screwdriver. (See Section 7.2.)

6. Remove the four screws from the corners of the XTC power sequencer module (see Section 9.4), and lay the XTC down with all of its connections in place.

7. Remove signal cable 17-01814-01 from the upper right corner of the back of the console assembly. This cable is the control from the TK to VAXBI backplane segment D, at the slot housing the TK's TBK70 adapter.

8. Working from the rear of the cabinet, loosen the two #10-32 screws with a large Phillips screwdriver.

9. Move to the front of the cabinet. Remove the two #10-32 screws on the left side of the console assembly using a large Phillips screwdriver. See ❾ in Figure 9–2. Remove one of the two screws on the upper right support panel. Loosen the remaining screw.

10. Supporting the control assembly with one hand, remove the last loosened screw with your hand.

11. Using both hands, carefully pull the control assembly forward and out of the cabinet. See ⓫.

REPLACEMENT

1. Install the XTC and the control panel assembly (see Section 9.4 and Section 9.6).

2. As you guide the control assembly into the front of the cabinet, push the control assembly all the way to the left. This will align the screws with their holes in the structure. If you have trouble closing the cabinet door, check the assembly alignment.

3. Reverse steps 1 through 8 in the Removal section above.

9.3 XTC Power Sequencer Specifications

The XTC power sequencer is mounted on the back of the system control assembly. It is wired to the XMI backplane, the console terminal, the TK tape drive, and the H7214 power regulator.

Figure 9-3: XTC Power Sequencer

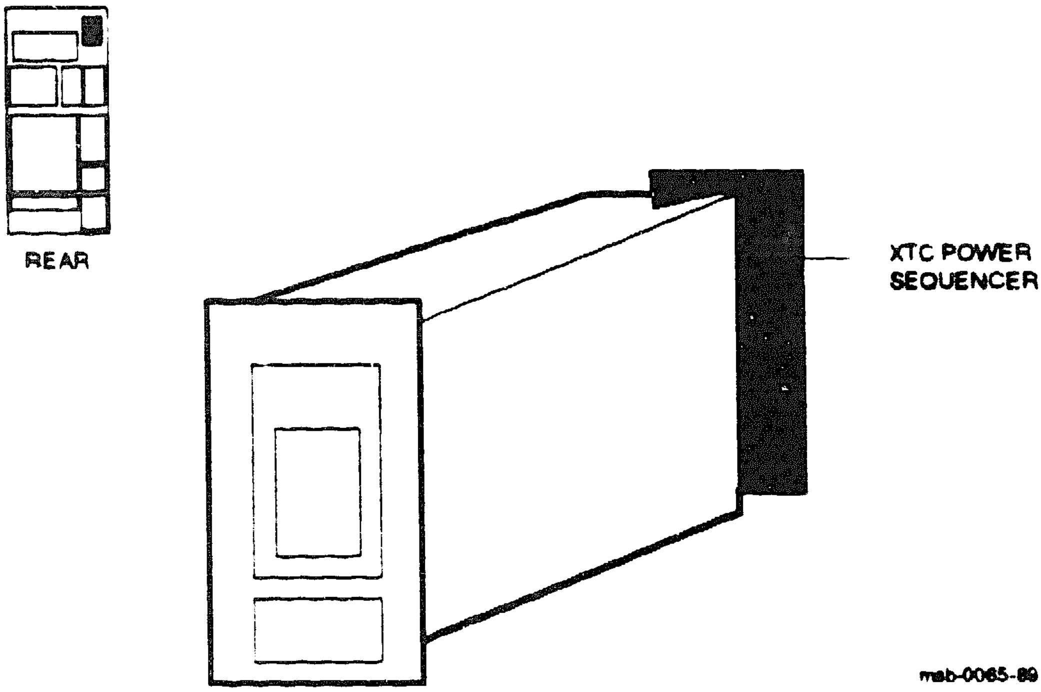


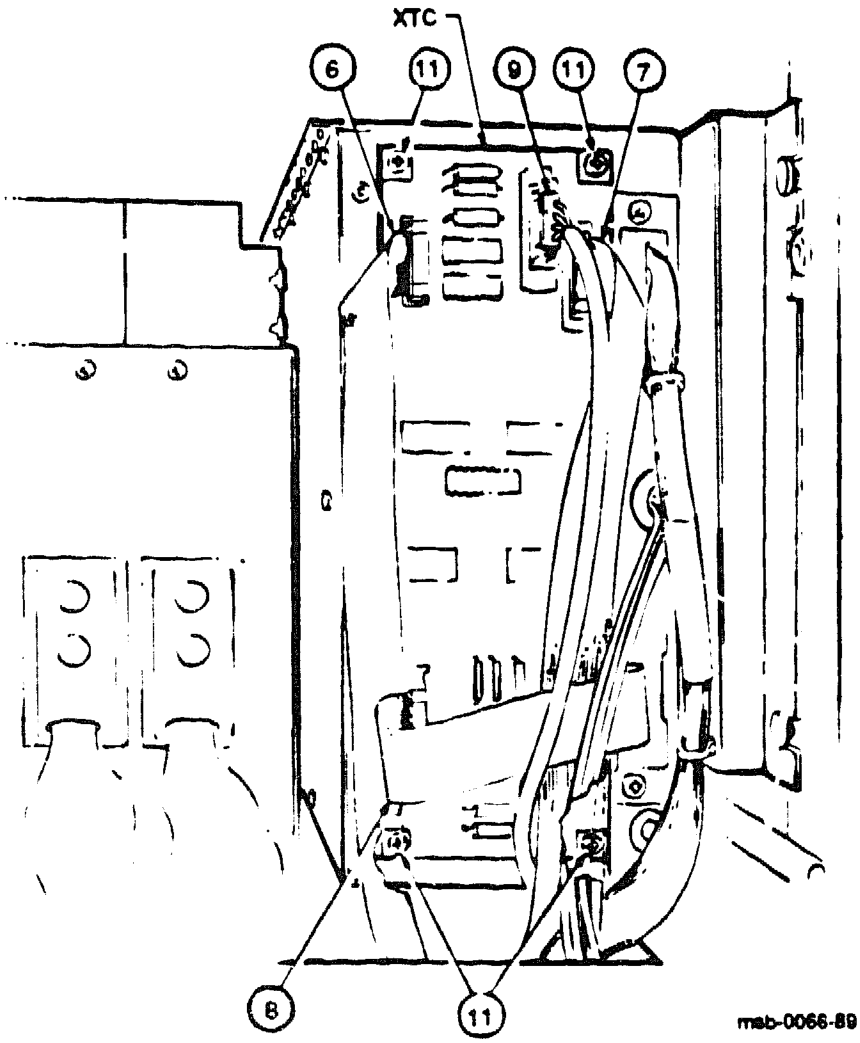
Table 9–2: XTC Power Sequencer Specifications

Parameter	Description
Part Number:	54-17243-01 or 20-29176-01
Location:	Upper right rear, mounted on the back of the system control assembly
Dimensions:	2.5" W x 8" H x .06" D
Weight:	Less than 1 lb
Power:	+5VBB at 0.6 amps +12V at 1.0 amps -12V at 0.1 amps
Cables:	Four ribbon cables and one TOY clock battery cable: 12-19245-02 battery cable, J1 connector with red plug end 17-01498-01 XTC to H7206, J3 14-pin connector 17-01567-01 XTC to console port, J5 10-pin connector 17-01568-02 XMI to XTC, J4 20-pin connector, 56" long 17-01816-01 XTC to control panel, J2 connector
Service From:	Rear of cabinet, door removed
Tools Required:	Large Phillips screwdriver
Subassemblies:	None
Diagnostics:	Power indicator lights on the control panel will light and the control panel key switches will turn when the XTC power sequencer is correctly installed

9.4 XTC Removal and Replacement

Remove or replace the XTC power sequencer from the rear of the cabinet.

Figure 9–4: XTC Power Sequencer Removal



REMOVAL

1. Execute an orderly shutdown of the system.
2. Turn the control panel upper key switch to the Off position.
3. Pull the circuit breaker switch.
4. Unplug the system.
5. Open the front and rear doors.
6. Wearing a ground strap, disconnect the 17-01568-02 ribbon cable at J4 which is a 20-pin connector cable leading to the XMI. See ❻ in Figure 9–4.
7. Disconnect the 17-01498-01 ribbon cable at J3 which is a 14-pin connector cable leading to the H7206 power and logic box. See ❼.
8. Disconnect the 17-01567-02 ribbon cable at J5 which is a 10-pin connector cable leading to the console port. See ❽.
9. Disconnect the 17-01816-01 ribbon cable at J2 which leads to the control panel on the system control assembly. See ❾.
10. Disconnect the 1[illegible]-19245-02 lead with a red plug end at the J1 connector; the cable leads to the TOY clock battery in the system control assembly.
11. Use a large Phillips screwdriver to remove the four #6-32 screws located on each corner of the XTC power sequencer. See ❿.
12. Pull the XTC toward you and remove.

REPLACEMENT

- Reverse steps 1 through 12 in the Removal section above.
- Reset the TOY clock.

9.5 Control Panel Assembly Specifications

The control panel assembly (54-16574-01) is in the upper left front of the cabinet.

Figure 9–5: Control Panel Assembly

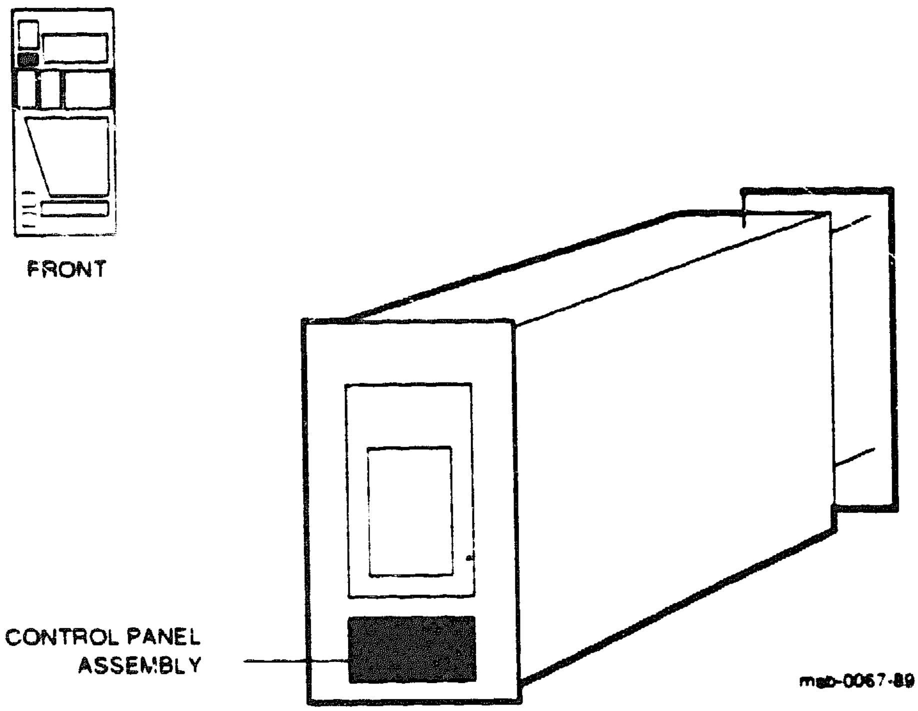


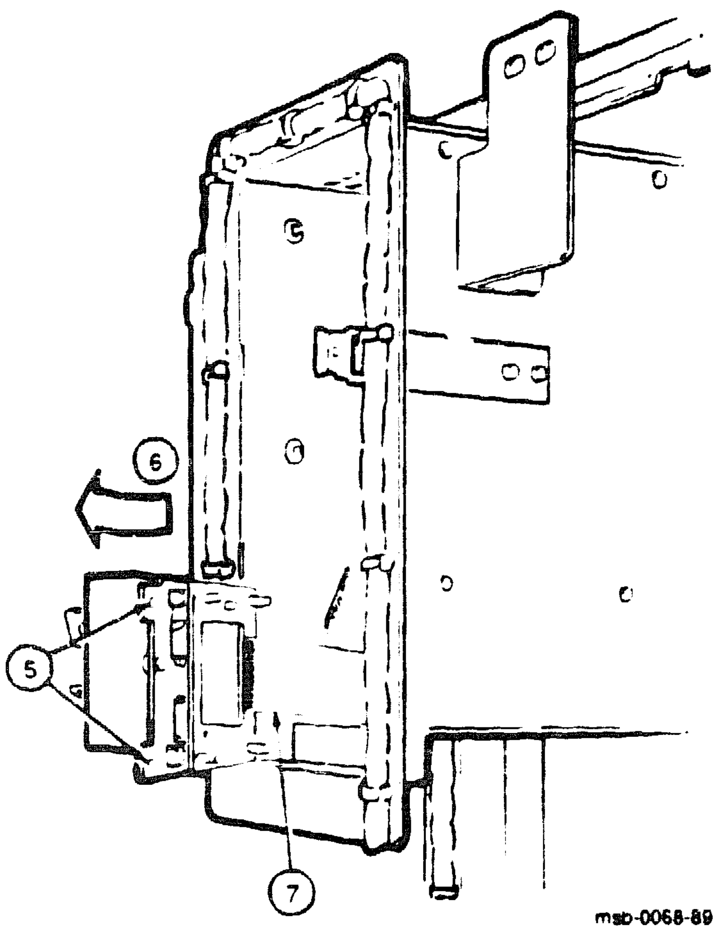
Table 9–3: Control Panel Assembly Specifications

Parameter	Description
Part Number:	54-16574-01
Location:	Front upper left corner
Dimensions:	4.25" W x 2.75" H x 1.75" D
Weight:	Less than 5 lbs
Cables:	17-01818-01 cable from the J1 20-pin connector to the assembly bulkhead
Service From:	Front of cabinet, door open
Tools Required:	Large Phillips screwdriver
Subassemblies:	None
Diagnostics:	Control panel assembly lights light when power is turned on by the control panel key switch.

9.6 Control Panel Assembly Removal and Replacement

Working from the front of the cabinet, remove the control panel assembly using a large Phillips screwdriver. The panel assembly has one cable, 17-01818-01.

Figure 9–6: Control Panel Assembly Removal



REMOVAL

1. Conduct an orderly shutdown of the system.
2. Turn the control panel upper key switch to the Off position.
3. Pull the circuit breaker switch.
4. Unplug the machine. Open the front door.
5. Using a large Phillips screwdriver, remove the two #6-32 screws on the right side of the panel. See ❺ in Figure 9–6.
6. Swing the unit out and to the left, and pull it toward you. See ❻.
7. Disconnect cable 17-01818-01 at the J1 20-pin connector. See ❼.

REPLACEMENT

1. Connect the power cord to J1. The connection is not keyed, so look at the pins and the receptacle and align them carefully as you connect the cord.
2. Place the tabs on the left edge of the control panel in the slots on the control assembly.
3. With the tabs inserted, swing the module into the opening.
4. Using a large Phillips screwdriver, insert and tighten two #6-32 screws.
5. Close the front door.

9.7 TK Tape Drive Specifications

The TK tape drive is located in the system control assembly in the upper left front of the cabinet, part number TK70-AA.

Figure 9–7: TK Tape Drive

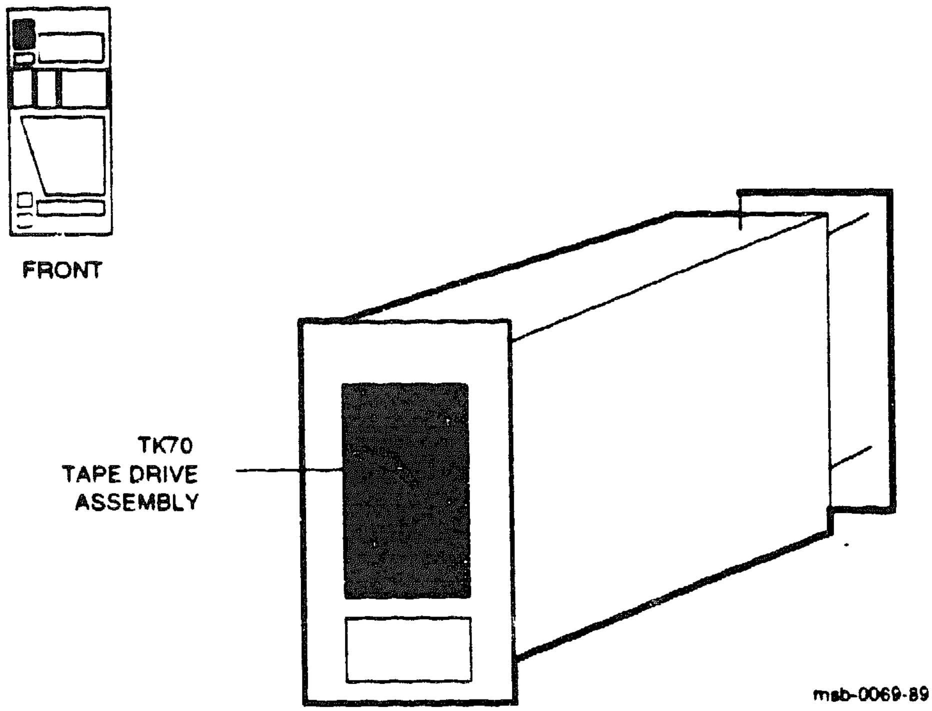


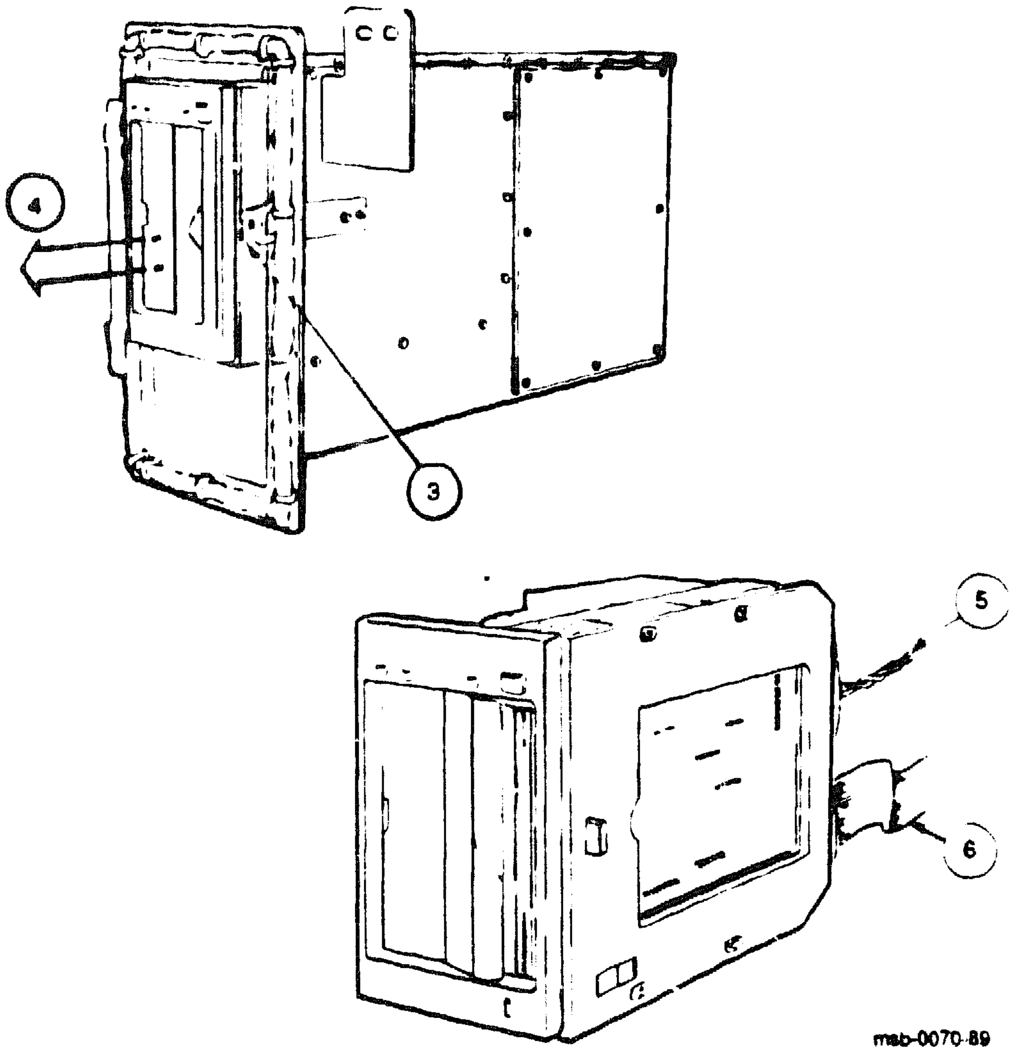
Table 9–4: TK Tape Drive Assembly Specifications

Parameter	Description
Part Number:	TK70-AA
Location:	Upper left front, housed in the system control assembly
Dimensions:	5.80" W x 3.38" H x 8.79" D
Weight:	5.13 lbs
Power:	One power cord 17-01817-01 to the system control assembly, which connects to 17-01814-01 leading to the TBK70 adapter in the VAXBI
Cable:	One signal cord 17-01813-01 from connector J7 to the filter board
Service From:	Front of cabinet, door removed
Tools Required:	None
Subassemblies:	None
Diagnostics:	All three LEDs on TK70 are lit when power-up diagnostic is in progress; tape-in-use LED (yellow) lights to indicate tape is ready for use.

9.8 TK Tape Drive Removal and Replacement

Working from the front of the cabinet, remove or replace the TK using the spring clip attached to the control assembly unit on the right. The TK has one power and one signal cable.

Figure 9–8: TK Tape Drive Removal



REMOVAL

1. Turn the control panel upper key switch to the Off position.
2. Open the front door.
3. Push the spring clip to the right. See ❸ in Figure 9–8.
4. Pull the TK out toward you. See ❹.
5. Holding the unit in your hand, disconnect power cord 17-01817-01 labeled P1. See ❺.
6. Disconnect the signal cable 17-01813-01 at J7 on the TK70. See ❻.

REPLACEMENT

- Reverse steps 1 through 6 above, being careful not to twist the signal cable.
- As you push the unit in, hold the signal cable flush to the left side of the unit so that the service loop remains untangled and is installed smoothly. Tuck the end loop in if it protrudes when the TK unit is installed.

9.9 Filter Board and TOY Clock Battery Specifications

The filter board and TOY clock battery are located on the inside floor of the control assembly in the upper left front of the cabinet. The battery is a 3-cell TOY clock battery, part number 12-19245-02, and it powers the time-of-year clock on the XTC power sequencer module. The filter board part number is 54-18547-01.

Figure 9-9: Filter Board and TOY Clock Battery

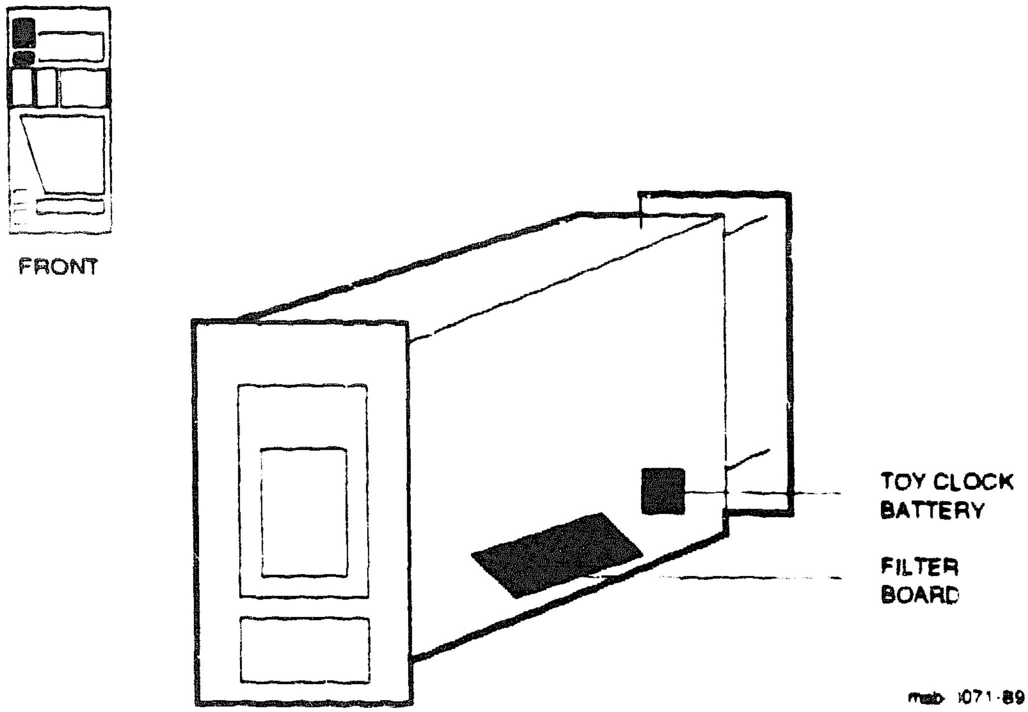


Table 9–5: Filter Board Specifications

Parameter	Description
Part Number:	54-18547-01
Location:	Inside of system control assembly
Dimensions:	3 1/4" x 5 1/4"
Weight:	Less than 1 lb
Cable:	17-01812-01 to XMI backplane 17-01813-01 to the TK70 tape drive
Service From:	Inside of system control assembly
Tools Required:	Large Phillips screwdriver
Diagnostics:	TK lights

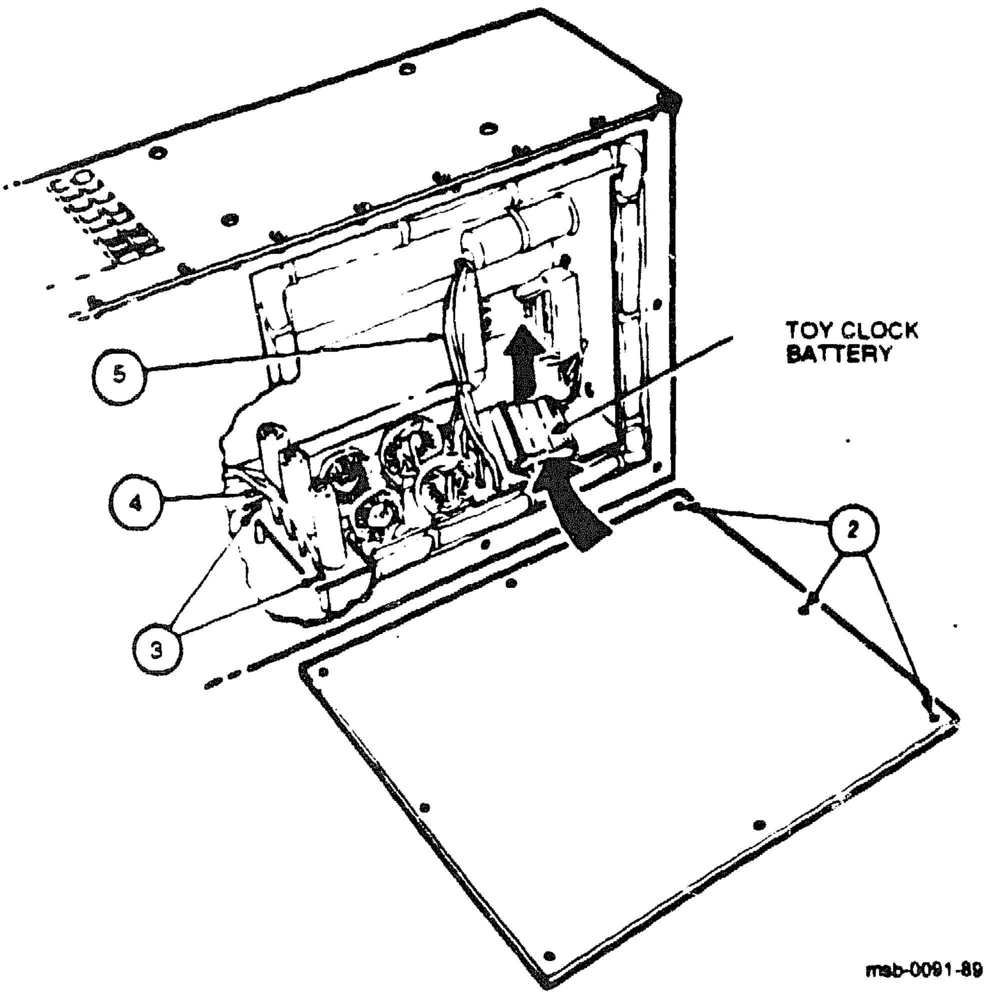
Table 9–6: TOY Clock Battery Specifications

Parameter	Description
Part Number:	12-19245-02
Location:	Inside of system control assembly
Dimensions:	1 3/4" x 1 1/2"
Weight:	Less than 1 lb
Power:	3-cell, 3.75V, .18mA
Cable:	Lead to XTC power sequencer
Service From:	Front of cabinet, door removed
Tools Required:	None
Diagnostics:	Time-of-year clock works

9.10 Filter Board and TOY Clock Battery Removal and Replacement

To remove or replace the filter board or the 3-cell time-of-year clock battery, first remove the system control assembly (see Section 9.2). Then remove the side panel of the system control assembly.

Figure 9–10: Filter Board and TOY Clock Battery Removal



REMOVAL OF FILTER BOARD

1. Remove the system control assembly (see Section 9.2).
2. Using a large screwdriver, unscrew the side panel of the system control assembly. See ❷ in Figure 9–10.
3. Remove the screw from each corner of the filter board, using a large screwdriver. See ❸.
4. Disconnect cable 17-01813-01 from J7 at the back of the TK70 tape drive. See ❹.
5. Disconnect cable 17-01812-01 which leads to the XMI backplane. See ❺. Working from the inside of the system control assembly, gently pull the cable through the ferrite bead at the rear of the system control assembly.
6. Lift the filter board up and out of the system control assembly.

REPLACEMENT OF FILTER BOARD

- Reverse steps 1 through 6 above.

REMOVAL OF TOY CLOCK BATTERY

1. Remove the system control assembly (see Section 9.2).
2. Using a large screwdriver, unscrew the side panel of the system control assembly. See ❷ in Figure 9–10.
3. To remove the battery, disconnect the 2-pin battery lead at J1 on the XTC power sequencer. Push the battery up and out of the plastic holder, pulling the lead through the system control assembly shielding.

REPLACEMENT OF TOY CLOCK BATTERY

1. To replace the battery, snap it into the holder and connect the lead at J1 on the XTC power sequencer.
2. Reverse steps 1 and 2 above.

CHAPTER 10

Chapter 10
Power Subsystem

This chapter gives specifications and removal and replacement procedures for the power modules. Figure 10–1 shows a block diagram of the power subsystem design.

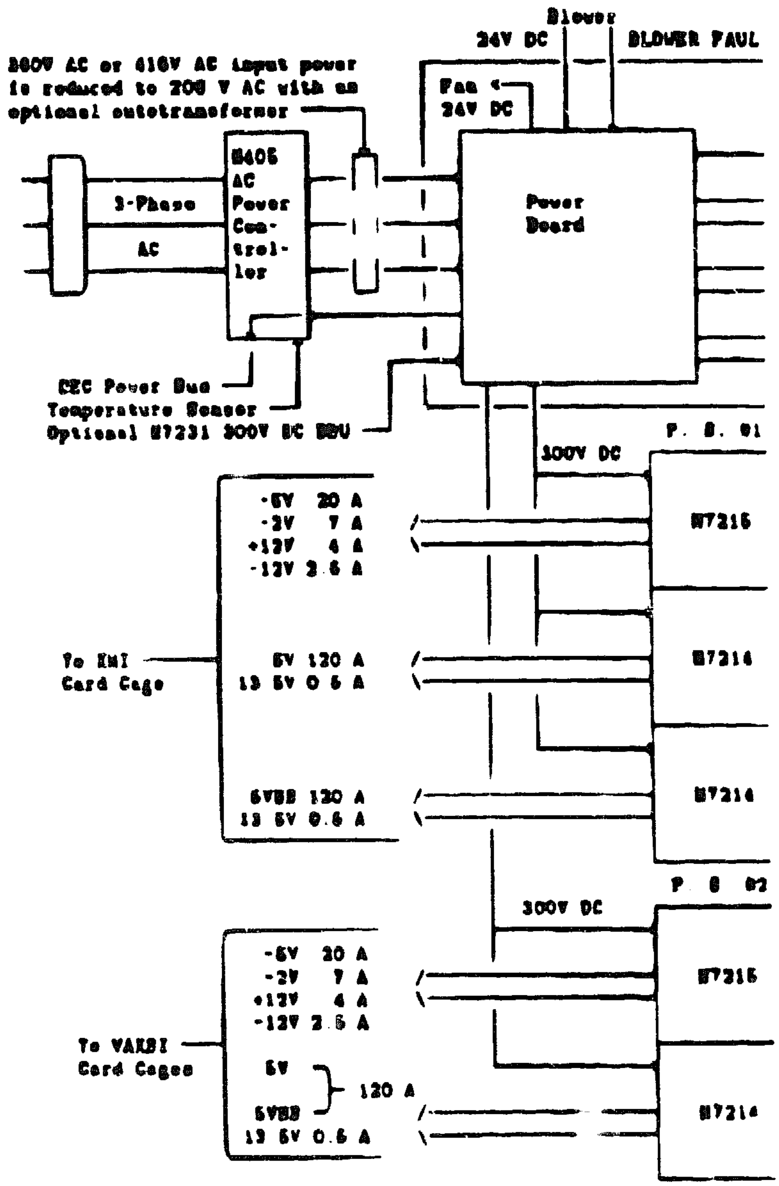
Sections in this chapter include:

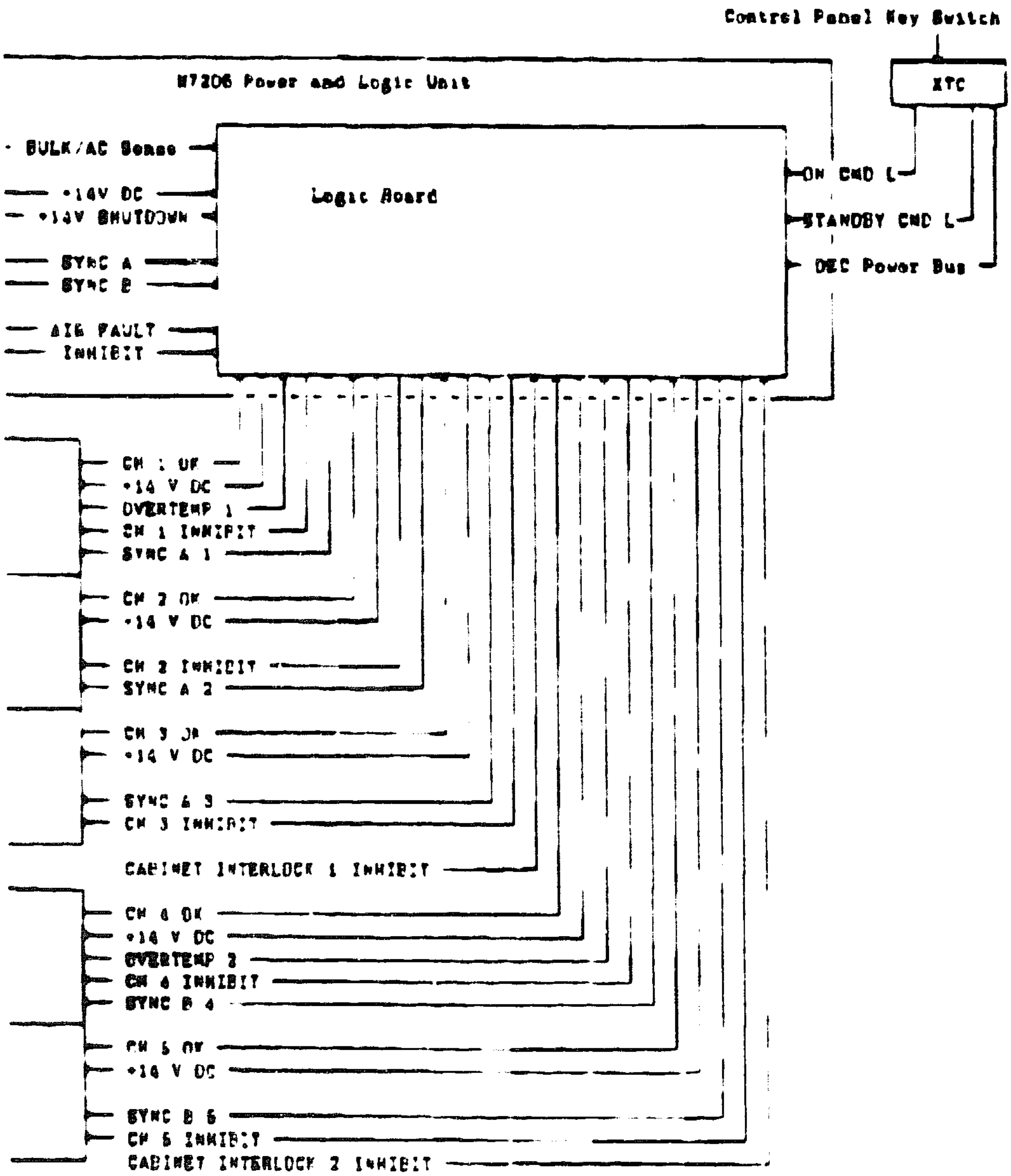
- Power Subsystem Design
- Power Specifications
- Power Modules
- H7214 Power Regulator
- H7214 Power Regulator Removal and Replacement
- H7215 Power Regulator
- H7215 Power Regulator Removal and Replacement
- H7206 Power and Logic Unit
- H7206 Power and Logic Unit Removal and Replacement
- H7206 Fan Removal and Replacement
- H405 AC Power Controller
- H405 AC Power Controller Removal and Replacement
- 50 Hz Transformer
- 50 Hz Transformer Removal and Replacement
- H7231-N Battery Backup Unit
- H7231-N Battery Backup Unit Removal and Replacement
- H7231-N Battery Backup Unit Installation

10.1 Power Subsystem Design

Figure 10–1 is a block diagram of the VAX 6000–400 power subsystem.

Figure 10–1: Power Subsystem Design





Control Panel Key Switch
H7206 Power and Logic Unit
XTC
Logic Board
BULK/AC Sense
+14V DC
+14V SHUTDOWN
SYNC A
SYNC B
AIR FAULT
INHIBIT
ON CMD L
STANDBY CMD L
DEC Power Bus
CH 1 OK
+14 V DC
OVERTEMP 1
CH 1 INHIBIT
SYNC A 1
CH 2 OK
+14 V DC
CH 2 INHIBIT
SYNC A 2
CH 3 OK
+14 V DC
SYNC A 3
CH 3 INHIBIT
CABINET INTERLOCK 1 INHIBIT
CH 4 OK
+14 V DC
OVERTEMP 2
CH 4 INHIBIT
SYNC B 4
CH 5 OK
+14 V DC
SYNC B 5
CH 5 INHIBIT
CABINET INTERLOCK 2 INHIBIT

msb-0072-89

10.2 Power Specifications

Figure 10–2 shows the physical arrangement of the power regulators in the cabinet. Table 10–1 and Table 10–2 list the DC output voltages the power regulators supply to the XMI and VAXBI card cages. AC output specifications are listed in Table 10–3.

Figure 10–2: DC Power Regulators In Cabinet (Rear View)

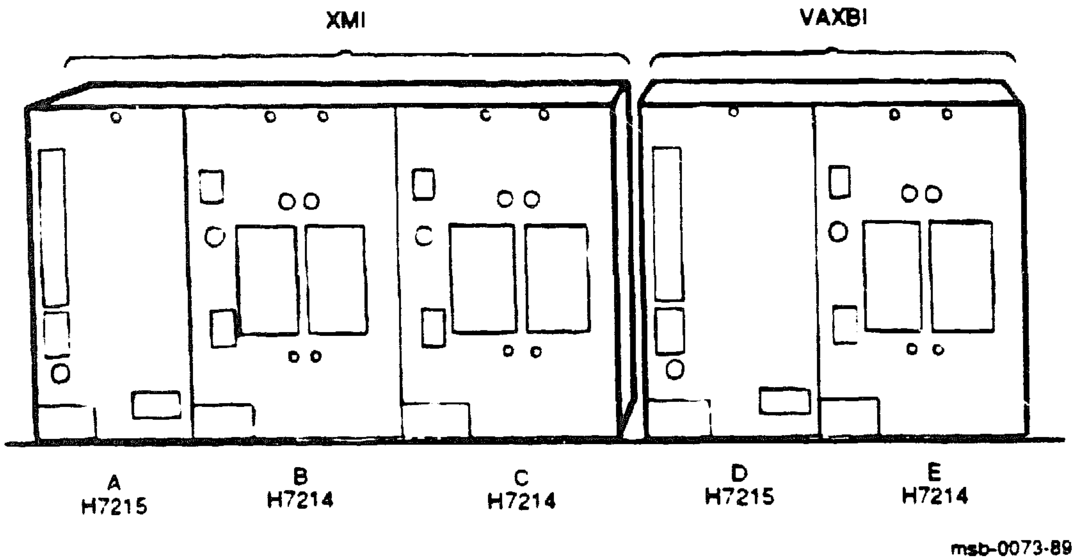


Table 10–1: XMI Side—DC Output Specifications

DC Voltage	Current	For:	From Regulator(s):
+12V	4 A	RS-232 and TK tape drive supply	A
-12V	2.5 A	RS-232 supply	A
-5V	20 A	ECL logic	A
-2V	7 A	ECL logic	A
+5V	120 A	Logic supply	B
+13.5V	0.5 A	Ethernet transceiver B	B
+5VBB	120 A	Memory supply	C
+13.5V	0.5 A	Ethernet transceiver C	C

Table 10–2: VAXBI Side—DC Output Specifications

DC Voltage [1]	Current	For:	From Regulator(s):
+12V	4 A	RS-232 and TK tape drive supply	D
-12V	2.5 A	RS-232 supply	D
-5V	20 A	ECL logic	D
-2V	7 A	ECL logic	D
+5V	120 A	Logic supply	E
+5VBB	120 A	Memory supply	E
+13.5V	0.5 A	Ethernet transceiver E	E

[1] The H7206 power and logic unit supplies 24VDC at 0-4 amps to the blowers and airflow sensor.

Table 10–3: AC Output Specifications

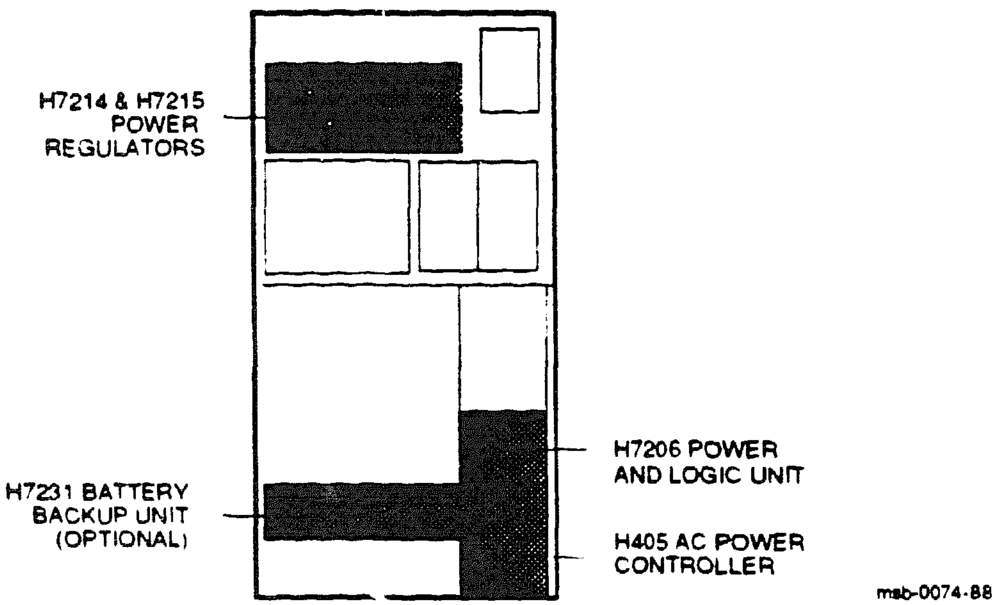
Type	For:
Two switched external IEC 320 receptacles fused at 10 amps [1]	Reserved
One unswitched internal IEC 320 receptacle fused at 2 amps	H7231-N battery backup option

[1] These receptacles are not included on some systems.

10.3 Power Modules

Most of the power modules can be seen from the rear of the cabinet.

Figure 10–3: Location of Power Modules (Rear View)



Power modules are listed in Table 10–4.

Table 10–4: Power Modules

Part Number	Module	Quantity	60 Hz System	50 Hz System
H7214	Power regulator	3	X	X
H7215	Power regulator	2	X	X
H7206	Power and logic unit	1	X	X
H7231-N	Battery backup unit	1	X	X
H405-E	AC power controller	1	X	–
H405-F	AC power controller	1	–	X
16-28393-01	50 Hz transformer	1	–	X

10.4 H7214 Power Regulator

The system has three H7214 power regulators; two supply power to the XMI backplane and one supplies power to the VAXBI backplane. Each power regulator can also supply +13.5V to an Ethernet transceiver. The regulators are located in the upper part of the cabinet.

Figure 10–4: H7214 Power Regulators (Rear View)

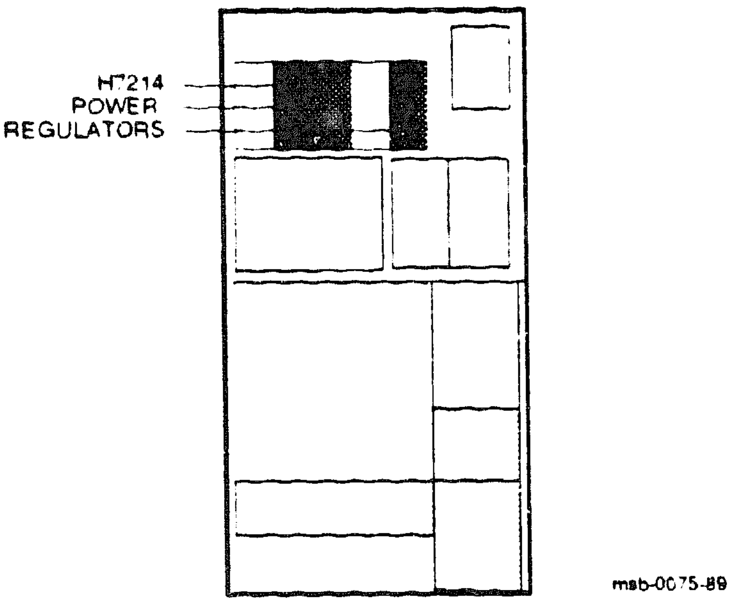


Table 10–5: H7214 Power Regulator Specifications

Parameter	Description
Part Number:	H7214
Location:	Upper part of cabinet
Dimensions:	6" H x 4.5" W x 12" D
Weight:	8 lbs
Cables for XMI:	17-01497-02 control/status cable, 34-pin connector 17-01446-01 bulk power cable 17-01525-01 remote sense cable +13.5V output cable, 2-pin connector (part of Ethernet cable 17-01496-01) +5VDC and -5VDC leads attached to XMI bus bar assembly
Cables for VAXBI:	17-01666-01 control/status cable, 24-pin connector, to H7206 power and logic unit 17-01447-01 bulk power cable to H7206 power and logic unit 17-01525-01 remote sense cable to VAXBI bus bar +13.5V output cable, 2-pin Mate-N-Lok connector (part of 17-01496-01 Ethernet cable) +5VDC and -5VDC leads attached to VAXBI bus bar assembly
Service From:	Front and rear of cabinet, doors open
Tools Required:	Flat screwdriver
Diagnostics:	Green LED lights when +5V output is within regulation

The H7214 power regulator develops two regulated DC outputs: +5V used to power system logic and memory loads, and the +13.5V, available for an Ethernet transceiver.

Each H7214 has one green LED that is visible from the rear of cabinet. The LED lights to indicate that the +5V output is properly regulated.

NOTE: *The green LED does not indicate the status of the +13.5V Ethernet output.*

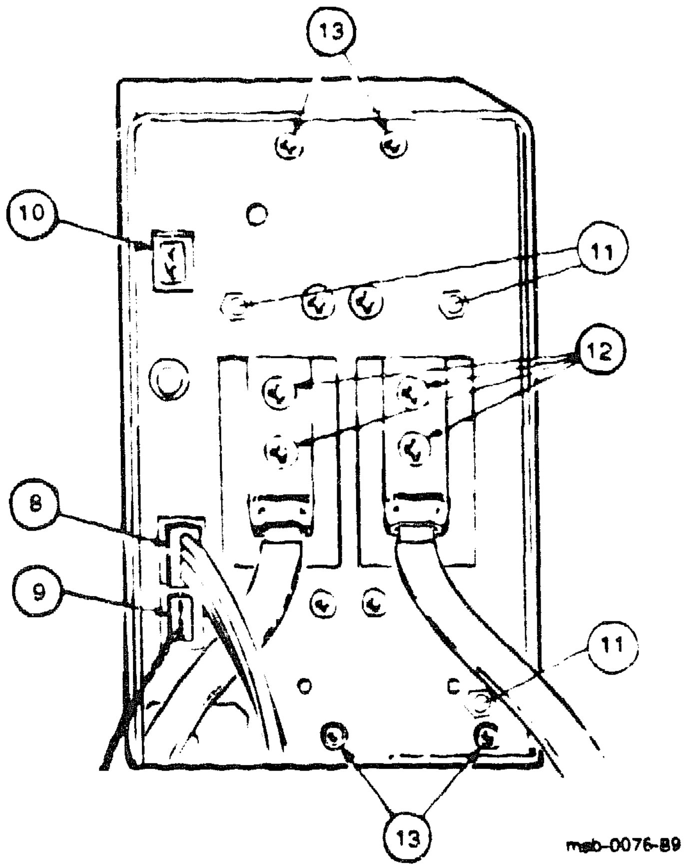
The power regulator consists of a single printed circuit board mounted on a right-angle bracket. The bracket has guiding edges for use when inserting the regulator into the cabinet.

10.5 H7214 Power Regulator Removal and Replacement

Remove or replace the H7214 power regulator from the rear of the cabinet.

WARNING: *High voltages are present in the H7214 power regulator. After power has been removed, wait at least 2 minutes before working on the unit.*

Figure 10–5: H7214 Power Regulator Removal



REMOVAL

1. Perform an orderly shutdown of the system.
2. Turn the upper key switch on the front control panel to Off.
3. Pull the main circuit breaker on the AC power controller to Off.
4. Unplug system power cord; wait 2 minutes for capacitors to discharge.
5. Open the front and rear doors.
6. At the front of the cabinet, disconnect the bulk power cord by releasing the fastener clip and pulling. On the XMI side, disconnect cable 17-01446-01 from J3. On the VAXBI side, disconnect cable 17-01447-01 from J3.
7. At front of cabinet, loosen one captive screw securing regulator.
8. At the rear of the cabinet, disconnect the control/status cable by releasing the fastener clip and pulling. See ❽ in Figure 10–5. On the XMI side, disconnect cable 17-01497-02 from J1. On the VAXBI side, disconnect cable 17-01666-01 from J1.
9. Disconnect the 17-01525-01 remote sense cable from J4. See ❾.
10. Disconnect the +13.5V cord [part of 17-01496-01] from J2 (if Ethernet connection is present). See ❿.
11. With a 5/16" nut driver, remove the three nuts and the plastic cover. See ⓫.
12. Disconnect the bus bar leads by removing the four screws. See ⓬. Work the bus bar leads down into the XMI service area.
13. Using a flat screwdriver, loosen the four slotted screws. See ⓭.
14. Support the bottom of the H7214 as you pull it from the cabinet.

REPLACEMENT

- **Reverse** steps 1 through 14 above.

NOTE: *Make sure the lugs connecting the bus bar leads do not contact the sheet metal bracket around the mounting points.*

The H7214 ground reference wire is connected to the regulator's circuit board and return bus bar by a screw and washer. Make sure the wire is intact and properly connected. Tuck the wire out of the way when inserting the regulator into the machine.

10.6 H7215 Power Regulator

The system has two H7215 power regulators, one for the XMI card cage and one for the VAXBI card cages. They are located in the upper part of the cabinet, along with the H7214 power regulators.

Figure 10–6: H7215 Power Regulators (Rear View)

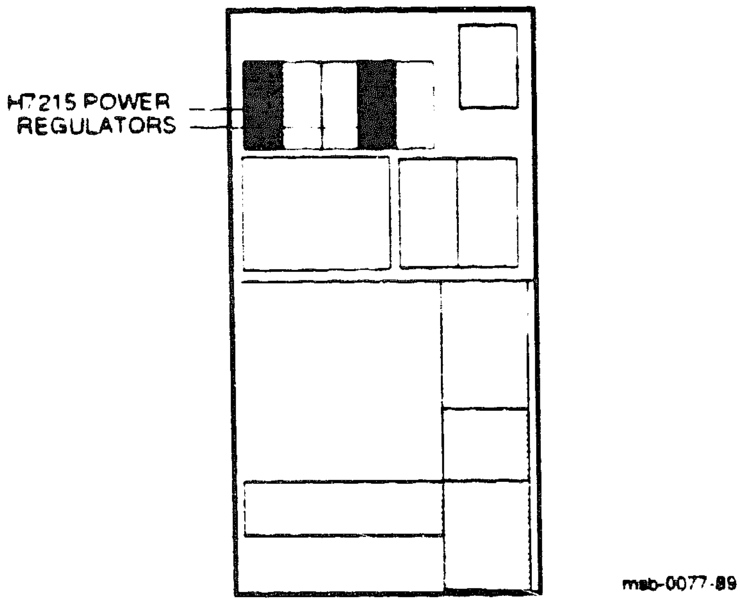


Table 10–6: H7215 Power Regulator Specifications

Parameter	Description
Part Number:	H7215
Location:	Upper part of cabinet
Dimensions:	6" H x 3.5" W x 12" D
Weight:	5 lbs
Cables for XMI:	17-01446-01 bulk power cable from H7206, 3-pin connector 17-01497-02 control/status cable from H7206, 10-pin connector for signals and 2-pin Mate-N-Lok connector for interlock switch 17-01566-01 power distribution cable to XMI, 32-pin connector
Cables for VAXBI:	17-01447-01 bulk power cable for H7206, 3-pin connector 17-01666-01 control/status cable from H7206, 10-pin connector for signals and 2-pin Mate-N-Lok connector for the interlock switch 17-01523-01 power distribution cable to VAXBI, 32-pin connector
Service From:	Front and rear of cabinet, doors open
Tools Required:	Flat screwdriver
Diagnostics:	Green LED lights when voltages are in regulation

The H7215 develops four regulated DC output voltages: -5V and -2V for ECL devices and +12V and -12V for communications devices and the TK tape drive.

The H7215 has a thermal sensor. If the H7215 overheats on the XMI side, an OVER TEMP signal is sent to the H7206 logic board. The H7206 will then inhibit all regulator outputs to the XMI. The same is true for the regulators on the VAXBI side.

Each regulator has a green LED that lights to indicate when all four output voltages are in regulation. The LEDs are visible from the rear of the cabinet.

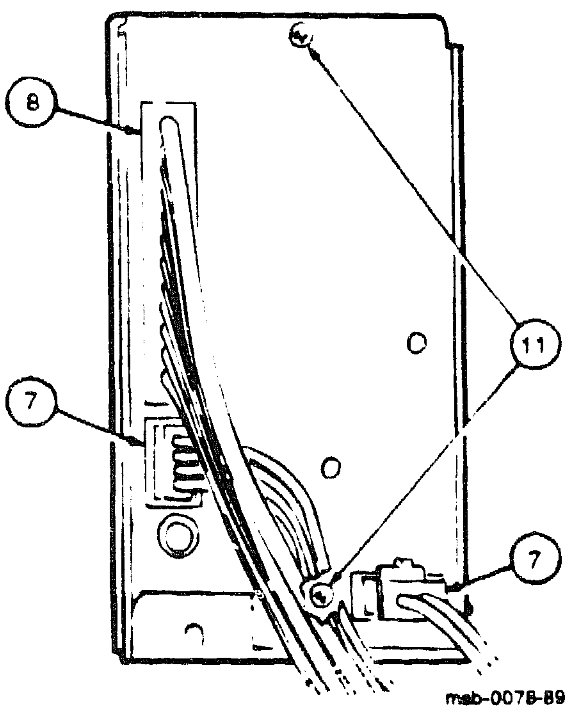
The power regulator consists of a single printed circuit board mounted on a right-angle bracket. The bracket has guiding edges for use when inserting the regulator into the system.

10.7 H7215 Power Regulator Removal and Replacement

Working mainly from the rear of the cabinet, remove or replace the H7215 power regulator using a flat screwdriver. The assembly has three captive screws, one control/status cable, and two power cables.

WARNING: *High voltages are present in the H7215 power regulator. After power has been removed, wait at least 2 minutes before working on the unit.*

Figure 10–7: H7215 Power Regulator Removal



REMOVAL

1. Perform an orderly shutdown of the system.
2. Turn the upper key switch on the front control panel to the Off position.
3. Pull the main circuit breaker on the AC power controller to the Off position.
4. Unplug the system power cord.
5. Wait 2 minutes for the capacitors to discharge.
6. Open the front and rear doors.
7. Working from the rear of the cabinet, disconnect the control/status cable by pulling out the 10-pin connector at J2 and the 2-pin Mate-N-Lok connector at INTERLOCK. See ❼ in Figure 10–7. On the XMI side, cable 17-01497-02 is disconnected. On the VAXBI side, cable 17-01666-01 is disconnected.
8. Remove the cable retainer and disconnect the power distribution cable from J3. See ❽. (Note that this 32-pin connector is keyed.) On the XMI side, cable 17-01566-01 is disconnected. On the VAXBI side, cable 17-01523-01 is disconnected.
9. At the front of the cabinet, disconnect the bulk power cable from J1. This cable has a 3-pin Mate-N-Lok connector. On the XMI side, cable 17-01446-01 is disconnected. On the VAXBI side, cable 17-01447-01 is disconnected.
10. At the front of the cabinet, loosen the one captive screw securing the H7215.
11. At the rear of the cabinet, use a flat screwdriver to loosen the screws at the top and bottom of the power regulator. See ⓫.
12. Support the bottom of the H7215 as you pull it out of the cabinet.

REPLACEMENT

- Reverse steps 1 through 12 above.
- Be sure to position the power regulator on the guide rail when you insert it into the cage.
- Note the gray dot on the control/status cable connector. When installing this cable, make sure the dot is on the top side.

10.8 H7206 Power and Logic Unit

10.8.1 Specifications

The H7206 power and logic unit is located in the lower right rear of the cabinet, just above the H405 AC power controller.

Figure 10–8: H7206 Power and Logic Unit (Rear View)

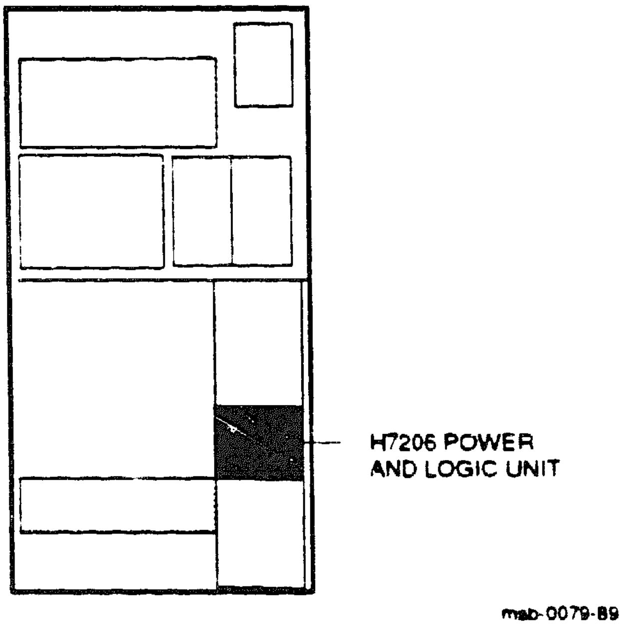


Table 10–7: H7206 Power and Logic Unit Specifications

Parameter	Description
Part Number:	H7206
Location:	Lower right rear of cabinet, just above the H405 AC power controller
Dimensions:	5" H x 5" W x 20.5" D
Weight:	13 lbs
Cables:	17-00962-01 to battery backup unit 70-20369-2F to battery backup unit 17-01498-01 to XTC module 17-01549-01 DEC power bus cable to H405 AC power controller 17-01569-01 AC/DC OK to DWMBA/B module 17-01666-01 control/status to regulators on VAXBI side 17-01497-02 control/status to regulators on XMI side 17-01447-01 bulk power to regulators on VAXBI side 17-01446-01 bulk power to regulators on XMI side 17-01570-01 power to front and rear blowers 17-01501-01 input from AC power controller
Service From:	Rear of cabinet, door open
Tools Required:	Flat screwdriver
Diagnostics:	AC input and power regulator indicator lights will light

The H7206 power and logic unit contains the fan/power and logic modules.

The fan/power module functions are:

- AC to 300VDC conversion
- 24VDC to blowers
- DEC power bus logic
- Control panel key switch interface

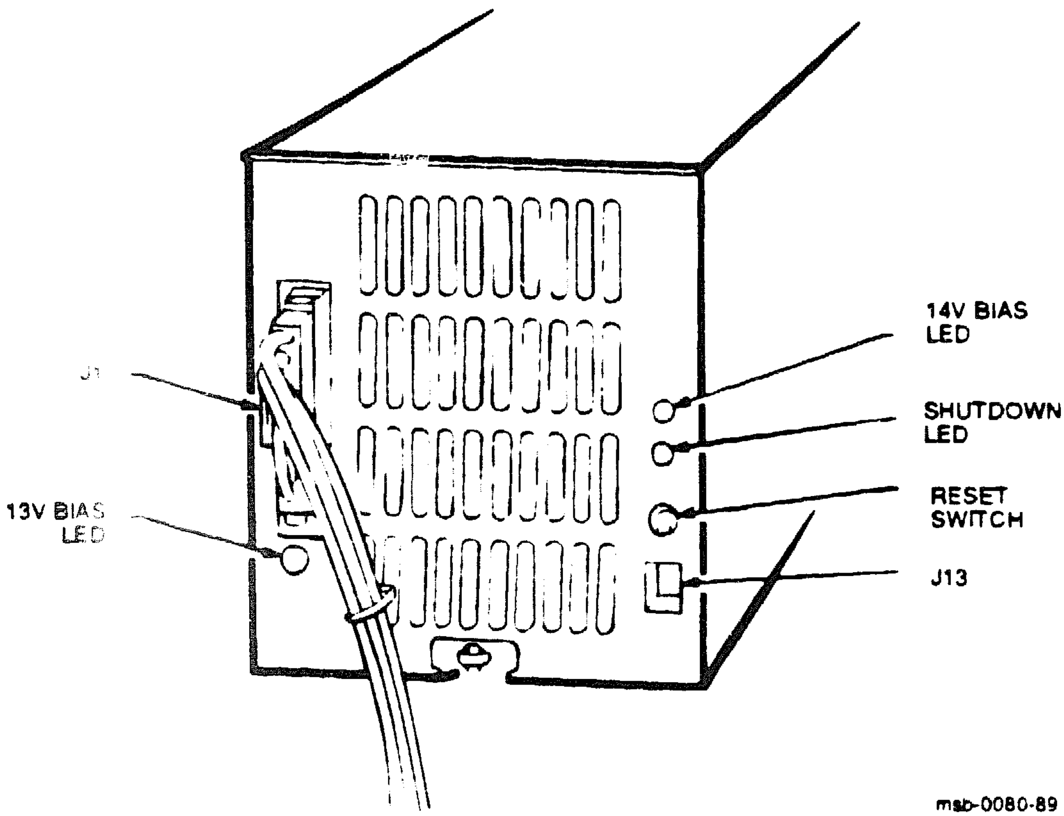
The logic module functions are:

- AC OK and DC OK control for system
- Battery backup unit control logic
- Door interlock logic

10.8.2 H7206 Power and Logic Unit Switches and Indicators

The H7206 power and logic unit has three indicators and one reset switch, visible from the front of the cabinet.

Figure 10–9: **H7206 Power and Logic Unit Switches and Indicators**



The power and logic unit consists of an AC to DC rectifier and filter, a fan/power module, and a logic module. The unit has three indicator LEDs and one reset switch.

The green +13V bias LED lights to indicate when the bias supply on the fan/power module is working.

WARNING: *When the +13V bias LED is unlit, do not assume that the 300V bulk supply is deenergized. This LED does not indicate the presence or absence of the 300V bulk supply.*

The green +14V bias LED lights to indicate that the bias supply is available to the logic board.

When lit, the red shutdown LED indicates a partial or complete power shutdown. Power shutdowns occur when there is an overtemperature condition, the VAXBI or XMI access door is open, or airflow in the cabinet is inadequate.

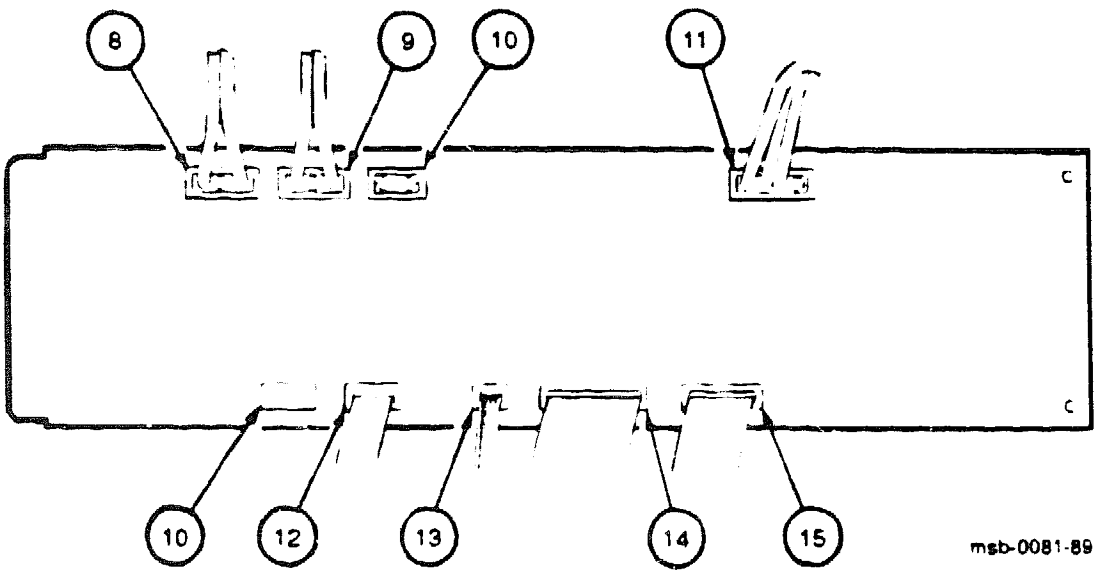
After determining the cause of the power shutdown, restart the system using the front control panel. The red shutdown LED should go off when the system is restarted.

10.9 H7206 Power and Logic Unit Removal and Replacement

Remove or replace the H7206 power and logic unit using a flat screwdriver. The assembly is held in place by six hex screws. There are 11 cables. You may want to mark the cables when removing them to simplify reconnection. If you cannot disconnect some cables from the front of the machine, remove the plenum to access the connectors (see Section 10.7).

WARNING: *High voltages are present in the H7206 power and logic unit. After power has been removed, wait at least 2 minutes before working on the unit.*

Figure 10–10: H7206 Power and Logic Unit Removal (Top View)



REMOVAL

1. Perform an orderly shutdown of the system.
2. Turn the upper key switch on the front control panel to the Off position.
3. Pull the main circuit breaker on the AC power controller to the Off position. Unplug the system power cord.
4. Wait 2 minutes for the capacitors to discharge.
5. Open the front and rear doors.
6. Working from the front of the cabinet, disconnect the 17-01501-01 AC input cable from J1 (see Figure 10–9).
7. Disconnect the 17-01549-01 DEC power bus cable from J13.
8. Disconnect the 17-01447-01 bulk power cable from J3. See ❽ in Figure 10–10.
9. Disconnect the 17-01446-01 bulk power cable from J4. See ❾.
10. If the system has a H7231-N battery backup unit, disconnect the 70-20396-2F cable from J6 and the 17-00962-01 cable from J12. See ❿.
11. Disconnect the 17-01570-01 blower cable from J2. See ⓫.
12. Disconnect the 17-01498-01 XTC cable from J16. See ⓬.
13. Disconnect the 17-01569-01 AC/DC OK cable from J11. See ⓭.
14. Disconnect the 17-01666-01 control/status cable from J9. See ⓮.
15. Disconnect the 17-01497-02 control/status cable from J14. See ⓯.
16. Working from the rear of the cabinet, use a flat screwdriver to remove the six hex screws.
17. Slide the unit out of the cabinet.

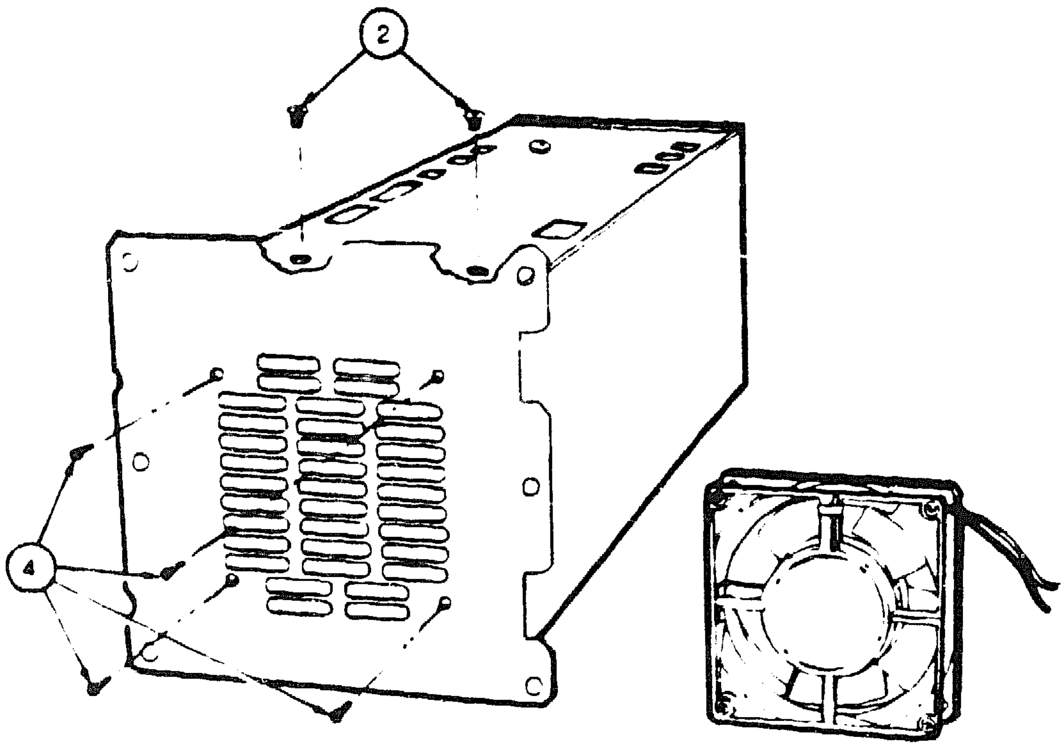
REPLACEMENT

- Reverse steps 1 through 17 above.
- When reinstalling the unit, make sure the locating tang on the front end of the unit engages the locating stud on the front shelf.

10.10 H7206 Fan Removal and Replacement

Remove the H7206 power and logic unit's top cover to access the fan (part number 12-24701-06). There are six screws and one cable. Use a flat screwdriver and a small Phillips screwdriver to remove the fan.

Figure 10–11: H7206 Fan Removal



REMOVAL

1. Remove the power and logic unit from the cabinet (see Section 10.9).
2. Using a flat screwdriver, remove the top cover by removing two screws. See ❷ in Figure 10–11.
3. Disconnect the fan cable from J8 on the power/fan module by pulling out the 2-pin connector.
4. Using a small Phillips screwdriver, remove the four screws that attach the fan to the rear panel of the power and logic unit. See ❹.
5. Remove the fan.

REPLACEMENT

- Reverse steps 1 through 5 above.

The fan is powered by the same +24VDC used to run the main system blowers. There is no fault indication if the fan stops.

When the cabinet doors are open, the power and logic unit depends entirely on its internal fan for cooling. When working on the machine, make visual checks to see if the fan is operating.

10.11 H405 AC Power Controller

The H405 AC power controller is located in the right lower rear corner of the cabinet. The assembly comes in two models: the H405-E for 60 Hz systems and the H405-F for 50 Hz systems.

Figure 10–12: H405 AC Power Controller (Rear View)

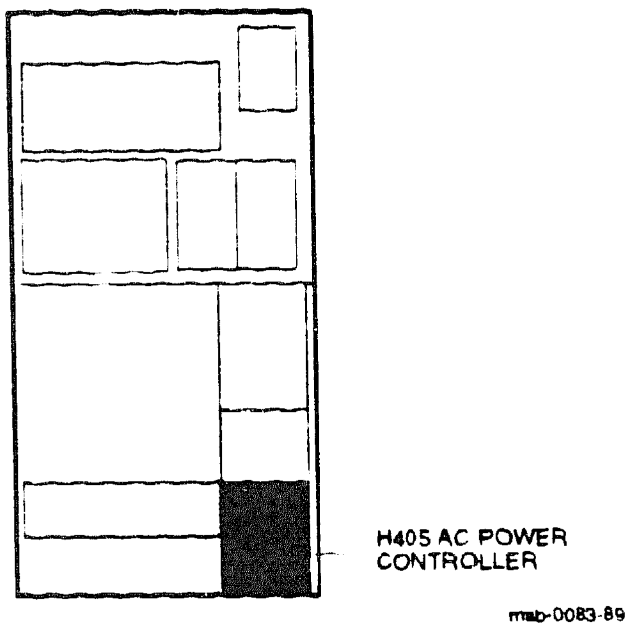


Table 10–8: H405 AC Power Controller Specifications

Parameter	Description
Part Number:	H405-E (60 Hz) H405-F (50 Hz)
Location:	Lower right rear corner of cabinet
Dimensions:	12.0 in. H x 7.5 in. W x 15 in. D
Weight:	34 lbs
Cables:	17-01501-01 AC input to power and logic unit 17-01549-01 DEC power bus to H7206 power and logic unit 17-01815-01 to 50 Hz transformer 17-00365-03 to battery backup unit 17-00365-03 to disks 17-01844-01 to temperature sensor
Service From:	Rear of cabinet, door open
Tools Required:	Large Phillips and flat screwdrivers
Diagnostics:	Three power phase indicator lights on the H405-E will light to indicate that three-phase power is present at power-up

In 60 Hz systems, the H405-E AC power controller routes 3-phase, 208VAC power to the output connector J2, used to connect power to the H7206 power and logic unit. For 50 Hz systems, the same output is first routed to the transformer (part number 16-28393-01) which lowers the phase voltages to the required input range of the H7206.

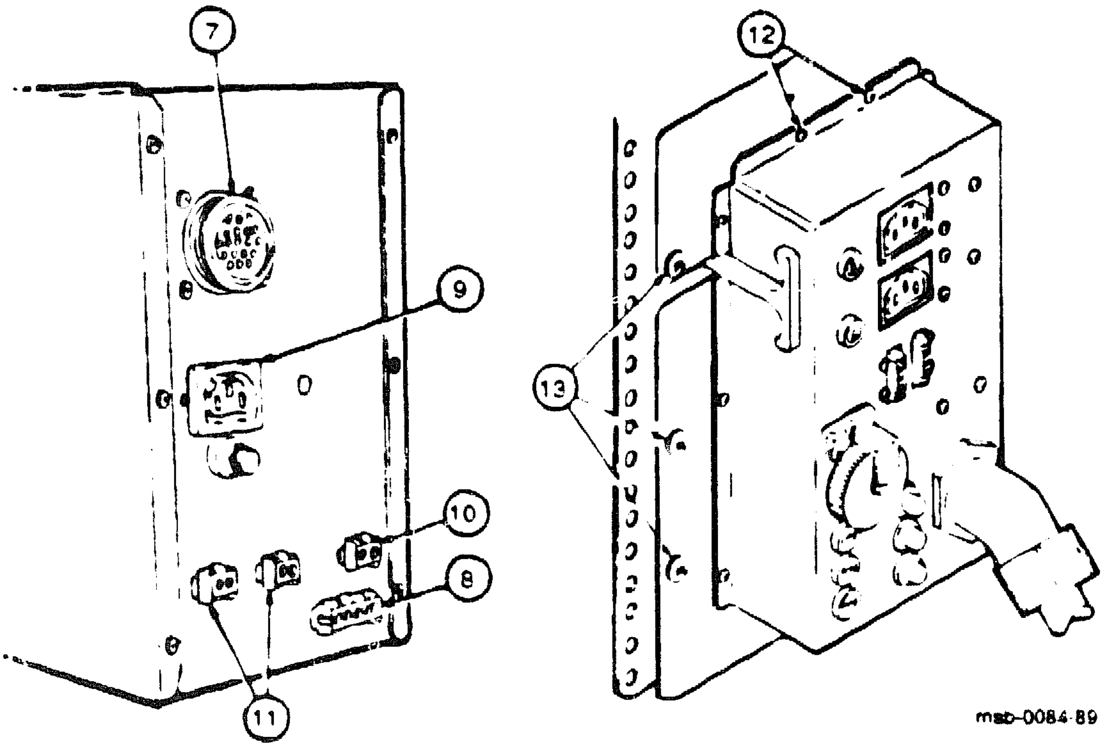
The H405 AC power controller monitors the state of the cabinet thermostat mounted at the top of the cabinet. The thermostat is a normally closed thermal switch. The H405 also monitors the sense switch integral to the main circuit breaker. The sense switch is normally closed when the circuit breaker is in the On position.

If the thermal switch opens (overtemperature condition) or the sense switch opens (main circuit breaker is Off), the H405 removes power from the cabinet by open circuiting its output signal, Fail Safe Enable. The battery backup unit, if included, is also disabled from delivering its 250VDC source to the H7206 power and logic unit.

10.12 H405 AC Power Controller Removal and Replacement

Working mainly from the rear of the cabinet, remove or replace the H405 AC power controller using a large Phillips screwdriver. The assembly has six captive screws and seven cables.

Figure 10–13: H405 AC Power Controller Removal



WARNING: *The H405 AC power controller is heavy. Exercise caution when lifting and moving this unit.*

REMOVAL

1. Perform an orderly shutdown of the system.
2. Turn the upper key switch on the front control panel to the Off position.
3. Pull the main circuit breaker on the AC power controller to the Off position.
4. Unplug the system power cord.
5. Wait 2 minutes for the capacitors to discharge.
6. Open the front and rear doors.
7. Working from the front of the cabinet, disconnect the 17-01501-01 AC input cable from J2 by twisting the black connector ring counterclockwise. If the system has a 50 Hz transformer, disconnect the 17-01815-01 cable from J2. See ❼ in Figure 10–13.
8. Disconnect the 17-01549-01 DEC power bus cable from J1. See ❽.
9. If the power system includes an H7231-N battery backup unit, disconnect the 17-00365-03 cable from J5. See ❾.
10. Disconnect the 17-01844-01 temperature sensor cable from J9. See ❿.
11. Disconnect the 17-01833-01 fail safe enable cable from J6 and J7. See ⓫.
12. At the rear of the cabinet, use a flat screwdriver to remove the two hex screws at the top of the subassembly. See ⓬.
13. Using a large Phillips screwdriver, remove the six screws that hold the AC power controller in place. See ⓭.
14. Pull the AC power controller toward you and remove it.

REPLACEMENT

- Reverse steps 1 through 14 above.

NOTE: *Route the 17-01844-01 and 17-01833-01 cables away from the transformer (50 Hz systems only).*

10.13 50 Hz Transformer

A transformer is required for 50 Hz systems. The transformer is located on the floor of the cabinet, directly below the power and logic unit.

Figure 10-14: 50 Hz Transformer (Front View)

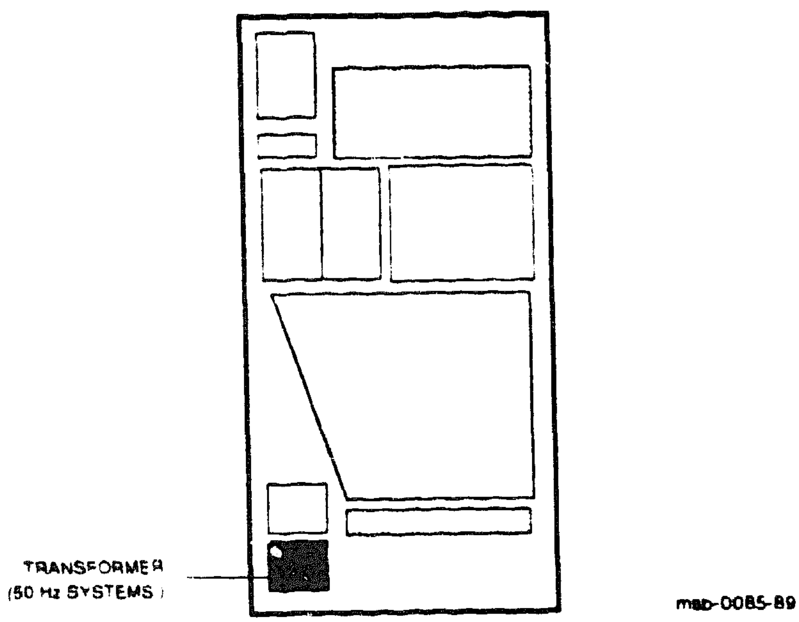


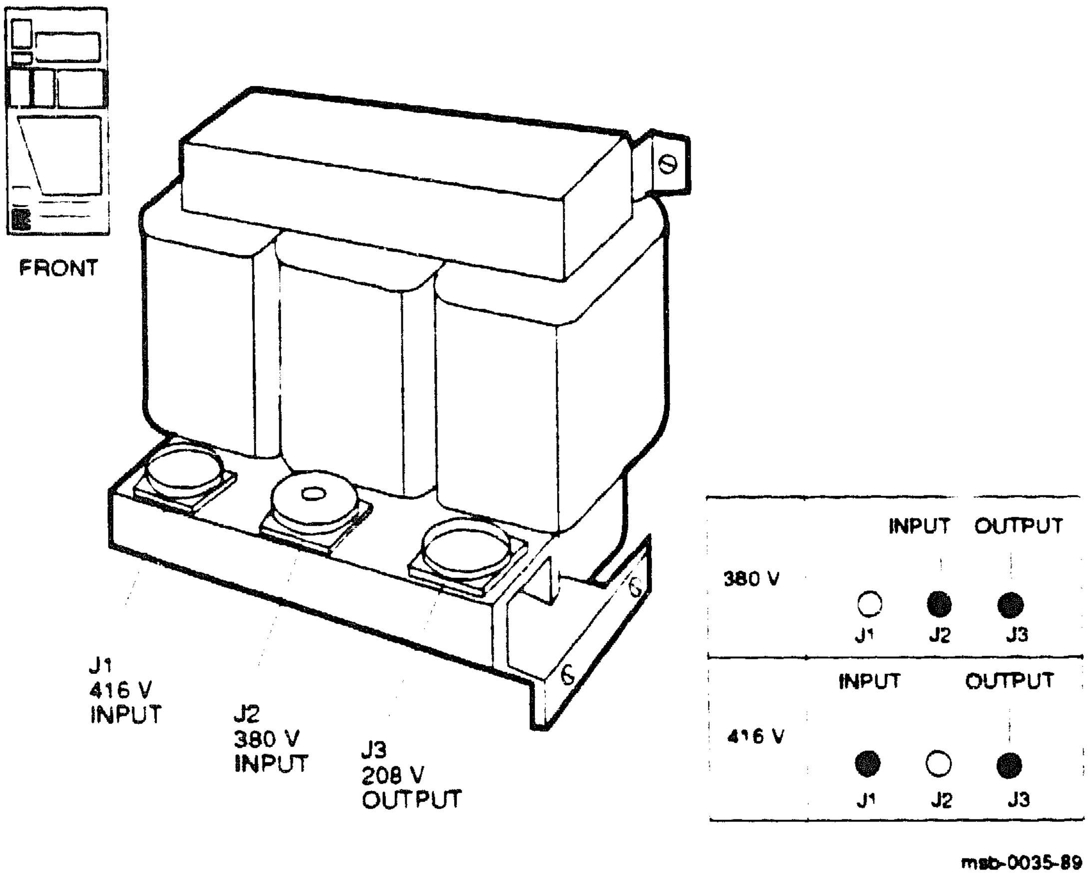
Table 10–9: 50 Hz Transformer Specifications

Parameter	Description
Part Number:	16-28393-01
Location:	Lower left front of cabinet
Dimensions:	6.5" H x 6" W x 10" D
Weight:	40 lbs
Cables:	18-01815-01 to H405-F AC power controller 17-01501-01 to H7206 power and logic unit
Service From:	Front of cabinet, door open
Tools Required:	Flat screwdriver

10.14 50 Hz Transformer Removal and Replacement

Working from the front of the cabinet, remove the transformer using a flat screwdriver. The transformer has six screws and two power cables.

Figure 10–15: 50 Hz Transformer Removal



WARNING: *To avoid high voltage shock, a round, threaded cap is provided to cover the unused inlet connector. When replacing, rewiring, or reconnecting the transformer, make sure that the cap is properly installed. The cap fits onto either the 380V (J2) or the 416V (J1) inlet connector.*

WARNING: *The 50 Hz transformer is heavy. Exercise caution when lifting and moving this unit.*

REMOVAL

1. Perform an orderly shutdown of the system.
2. Turn the upper key switch on the front control panel to the Off position.
3. Pull the main circuit breaker on the AC power controller to the Off position.
4. Unplug the system power cord.
5. Wait 2 minutes for the capacitors to discharge.
6. At the front of the cabinet, use a flat screwdriver to remove the six #10-32 screws securing the sheet metal panel. This panel is located below the power and logic unit.
7. Disconnect the 17-01815-01 power input cable from J1 (416V) or J2 (380V). See Figure 10–15.
8. Disconnect the 17-01501-01 power output cable from J3.
9. Remove the six screws that attach the transformer to the cabinet rails.
10. Remove the transformer.

REPLACEMENT

- Reverse steps 1 through 10 above.

10.15 H7231-N Battery Backup Unit

The optional H7231-N battery backup unit supplies 300V power to the system upon power failure. It is located in the horizontal mounting space just below the system blower, and to the left of the power and logic unit as viewed from the rear of the cabinet.

Figure 10–16: H7231-N Battery Backup Unit (Rear View)

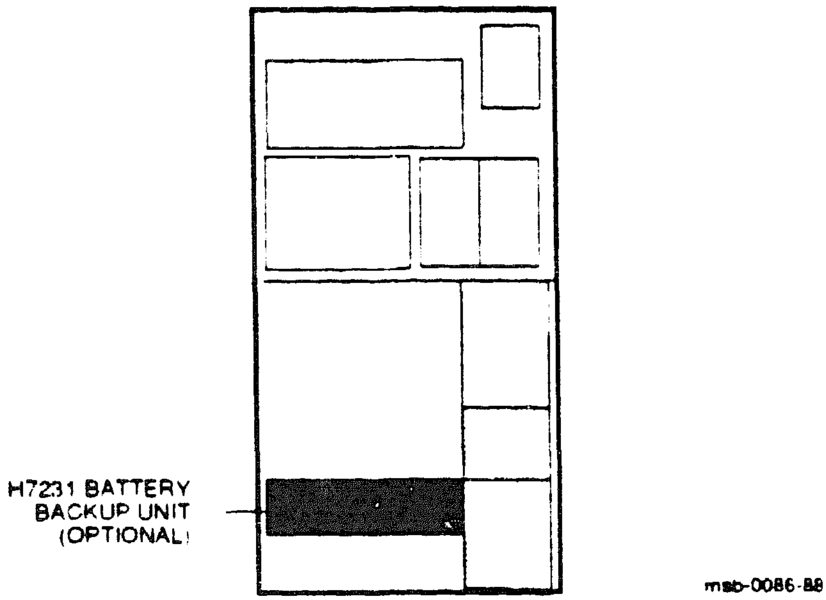


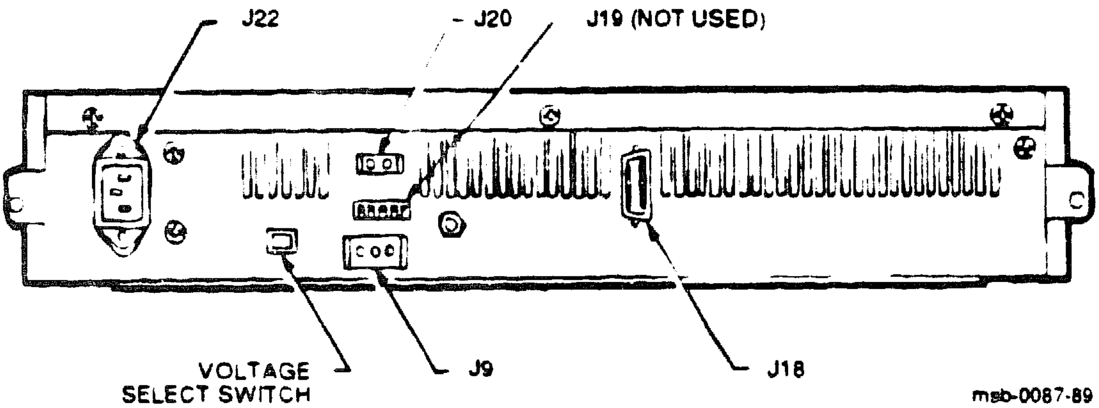
Table 10–10: H7231-N Battery Backup Unit Specifications

Parameter	Description
Part Number:	H7231-N
Location:	Lower third of cabinet, just below the system blower and next to the H7206 power and logic unit
Dimensions:	3" H x 17" W x 15" D
Weight:	35 lbs
Cables:	17-00962-01 control /status cable to power and logic unit 17-01833-01 fail safe enable cable to AC power controller 70-20396-2F power cable to power and logic unit 17-00365-03 AC line to AC power controller
Service From:	Front and rear of cabinet, doors open
Tools Required:	3/8" nutdriver, flat screwdriver, pliers

10.16 H7231-N Battery Backup Unit Removal and Replacement

Working from the front and rear of the cabinet, remove or replace the H7231-N battery backup unit using a flat screwdriver. The assembly has two screws and four cables.

Figure 10–17: H7231-N Battery Backup Unit Removal



WARNING: *The H7231-N battery backup unit is heavy. Exercise caution when lifting or moving this unit.*

REMOVAL

1. Perform an orderly shutdown of the system.
2. Turn the upper key switch on the front control panel to the Off position.
3. Pull the main circuit breaker on the AC power controller to the Off position.
4. Unplug the system power cord.
5. Wait 2 minutes for the capacitors to discharge.
6. Open the front and rear doors.
7. If necessary, remove the air intake grill and plenum to access the cable connections (see Section 10.7).
8. Using a flat screwdriver, remove the two screws that attach the 17-00962-01 control/status cable to J18.
9. Disconnect the 70-20396-2F power cable from J9. Using a 3/8 inch nutdriver, disconnect the ground strap.
10. Disconnect the 17-00365-03 AC line cable from J22.
11. Disconnect the 17-01833-01 fail safe enable cable from J20.
12. At the front of the cabinet, use a 3/8 inch nutdriver to remove the two nuts that secure the battery backup unit in its mounting bracket.
13. Slide the battery backup unit toward you and lift it out of the mounting bracket.

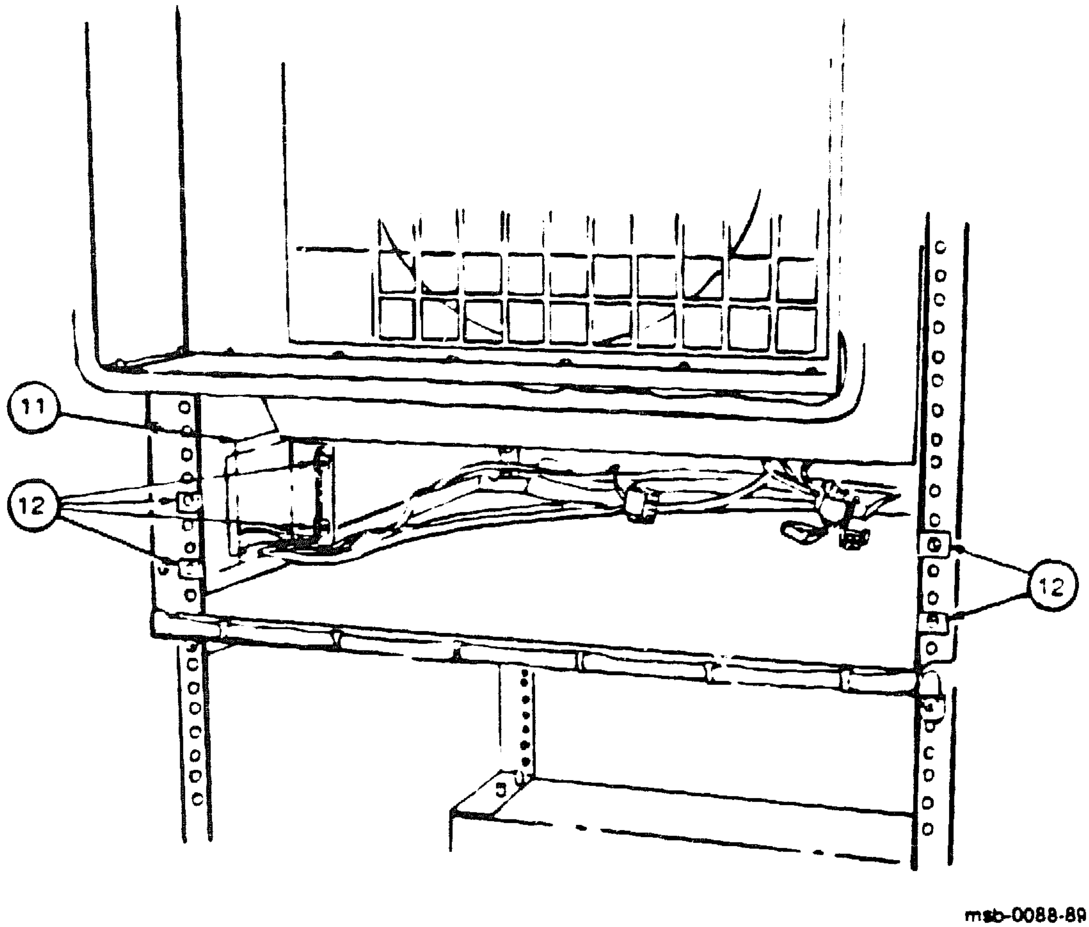
REPLACEMENT

- Reverse steps 1 through 13 above.

10.17 H7231-N Battery Backup Unit Installation

The H7231-N battery backup unit is a field-installable option. The unit, mounting bracket, hardware, and cables are included in the H7231-P Installation Kit.

Figure 10–18: Battery Backup Unit Cable Installation



10.17.1 Install the Battery Backup Unit Cables

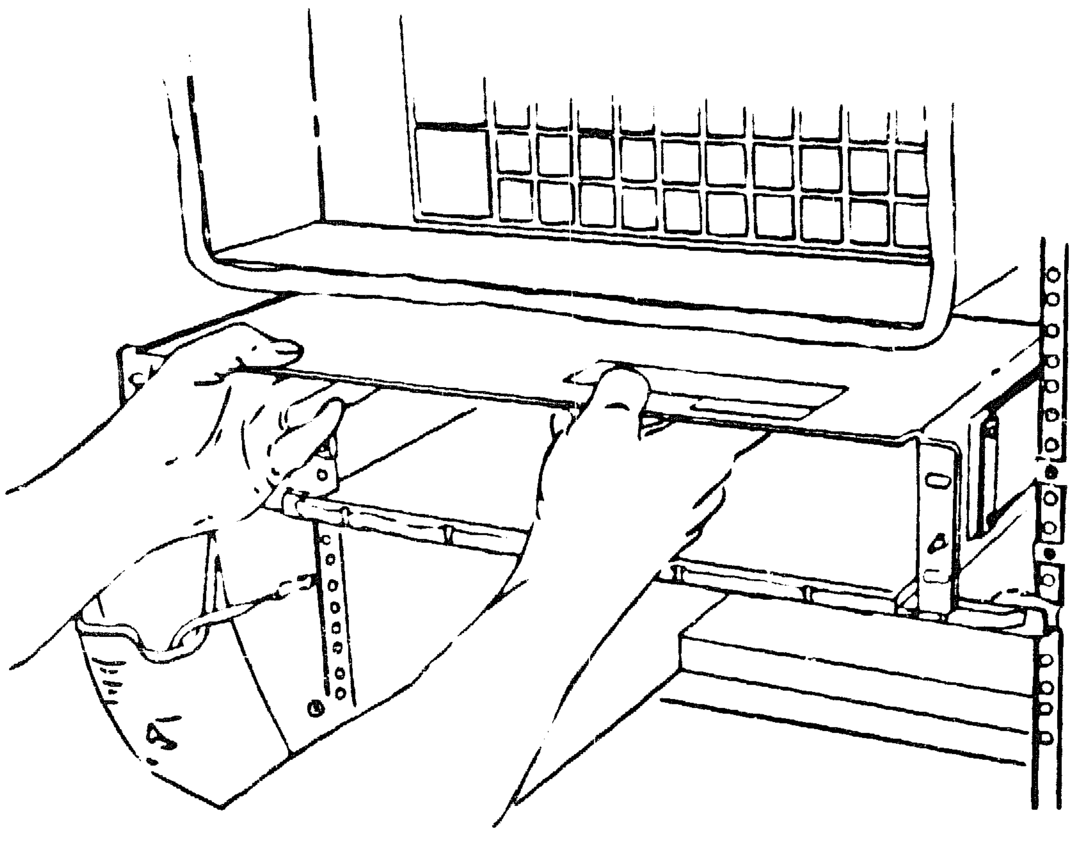
1. Perform an orderly shutdown of the system.
2. Turn the upper key switch on the front control panel to the Off position.
3. Pull the main circuit breaker on the AC power controller to the Off position.
4. Unplug the system power cord.
5. Wait 2 minutes for the capacitors to discharge.
6. Open the front and rear doors.
7. Connect the 17-00365-03 AC input cable to J5 on the H405 AC power controller (see Figure 10–13).
8. Connect the 17-00962-01 cable to J12 on the H7206 power and logic unit
9. Connect the 70-20396-2F cable to J6 on the H7206 power and logic unit.

   NOTE: *Be sure that this cable is never connected to any unit other than the H7206 or the battery backup unit.*
10. Find the fail safe enable cable. It is shipped with the system and is located underneath the H405 AC power controller. Connect the 17-01833-01 fail safe enable cable to J6 and J7 on the H405 AC power controller.
11. Route the cables through the clearance space at the right of the H7206 power and logic unit. See ⓫ in Figure 10–18.
12. Install the eight Tinnerman nuts. See ⓬. Four nuts are installed on the front rails, two nuts on each side rail.

10.17.2 Install the Mounting Bracket

1. At the front of the cabinet, slide in the mounting bracket (see Figure 10–19) and secure it by installing four Phillips screws into the Tinnerman nuts on the front rails. Do not tighten.
2. Install the two long Phillips screws on the left side rail.
3. At the rear of the cabinet, install the two spacers and two flathead screws behind the right side rail. Use pliers to line the spacer up behind the rail so that you can install the flathead screw through the spacer, rail, and Tinnerman nut. Then tighten all screws.

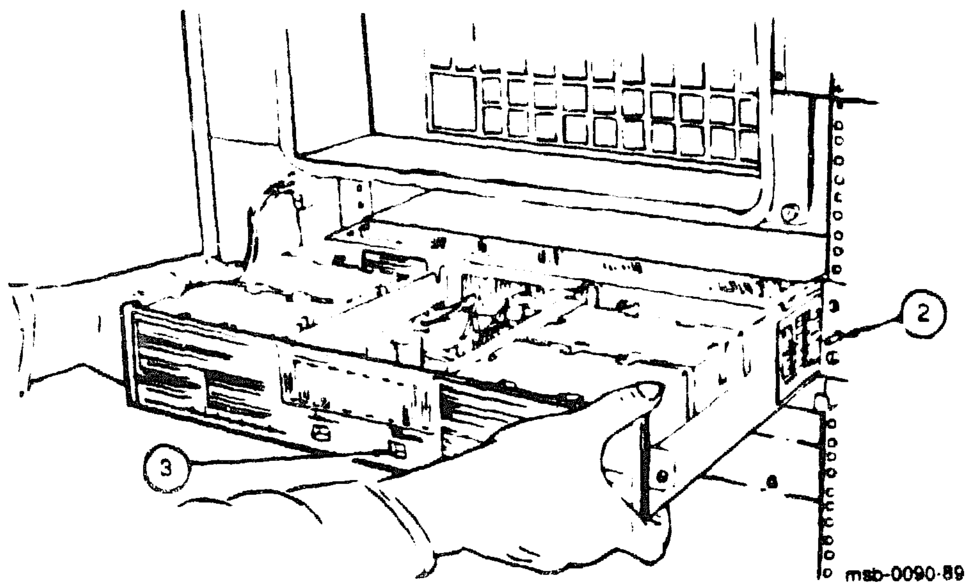
Figure 10–19: Mounting Bracket Installation



10.17.3 Install the Unit

1. At the front of the cabinet, slide the battery backup unit into the mounting bracket (see Figure 10–20).
2. Using a 3/8 inch nutdriver, install the two nuts on the mounting bracket studs to secure the unit. See ❷ in Figure 10–20.
3. Set the voltage select switch. See ❸. For 60 Hz systems, set the switch to the right (115V). For 50 Hz systems, set the switch to the left (230V).
4. At the rear of the cabinet, remove the plenum (see Section 10.7).
5. Using a flat screwdriver, install the two screws that attach the 17-00962-01 cable to J18 (see Figure 10–17).
6. Connect the 70-20396-2F cable to J9. Using a 3/8 inch nutdriver, connect the cable's ground strap.
7. Connect the 17-00365-03 cable to J22 and the 17-01833-01 cable to J20.
8. Set the voltage select switch as in step 3.
9. Replace the plenum. Shut the doors.

Figure 10–20: Battery Backup Unit Installation



CHAPTER 11

Chapter 11
Cabinet and Airflow Subsystem

This chapter describes the field-replaceable units of the cabinet and units that monitor and control the interior environment of the cabinet. Sections include:

- Door and Filter Removal and Replacement (Front)
- Door and Filter Removal and Replacement (Rear)
- Airflow Sensor Removal and Replacement
- Temperature Sensor Removal and Replacement
- Blower Assembly Specifications
- Blower Assembly, Front and Rear
- Blower Assembly Removal and Replacement
- Side Panel Removal

11.1 Door and Filter Removal and Replacement (Front)

Both the front and rear doors have air filters that need to be replaced periodically. Figure 11-1 shows the inside of the front door.

Figure 11-1: Front Door (Inside View)

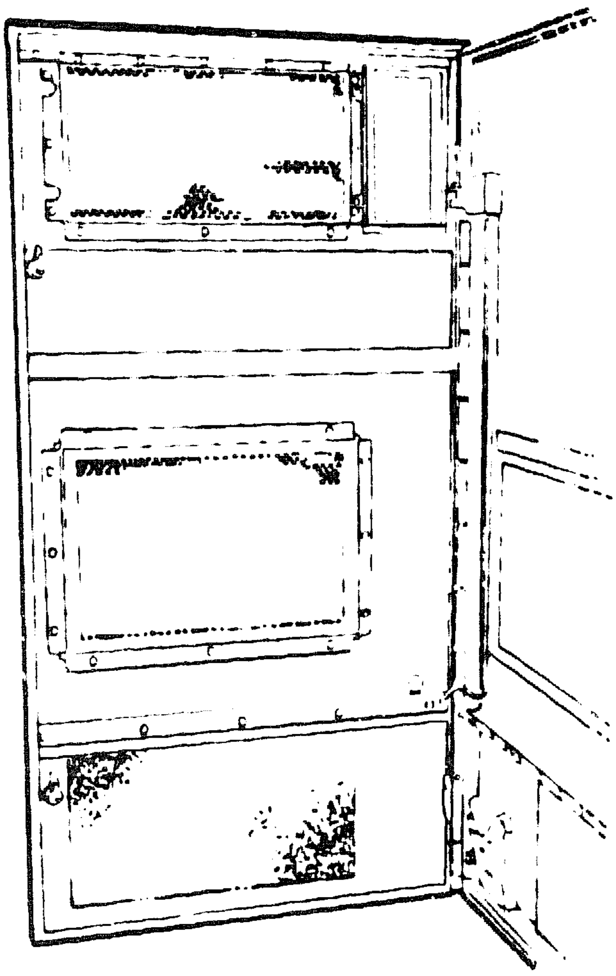


Table 11–1: Front Cabinet Door and Air Filter Specifications

Parameter	Description
Front Door:	70-24623-01
Dimensions:	28.25" W x 56" D
Weight:	31 lbs
Air Filters:	12-11255-23 — 17.5" W x 9" D 12-11255-24 — 18.5" W x 12.5" D (air intake) 12-11255-25 — 18.5" W x 10" D
Tools Required:	3/8" and 11/32" nutdrivers

REMOVAL OF DOORS

1. Remove the ground strap, which is attached to the front door, using a 3/8 inch nutdriver.
2. Pull up the pin in the top hinge and lock in place.
3. Pull up and hold the pin in the bottom hinge as you lift the door up to remove it from the cabinet.

REPLACEMENT OF DOORS

1. Put the door into position at the hinges and then release the lock holding the top pin.
2. Pull up the bottom pin and release it to secure the door.

REMOVAL AND REPLACEMENT OF AIR FILTERS

It is especially important that the filters in the center of the front door and at the bottom of the rear door be clean. These filters cover the air intake area.

Three filters are covered with a grill that must be removed to replace the air filter.

1. Use an 11/32 inch nutdriver to remove the grill.
2. Pull off the old filter and stick on the new one.
3. Reinstall the grills (they protect against electromagnetic interference).

11.2 Door and Filter Removal and Replacement (Rear)

Figure 11-2 shows the inside of the rear door.

Figure 11-2: Rear Door (Inside View)

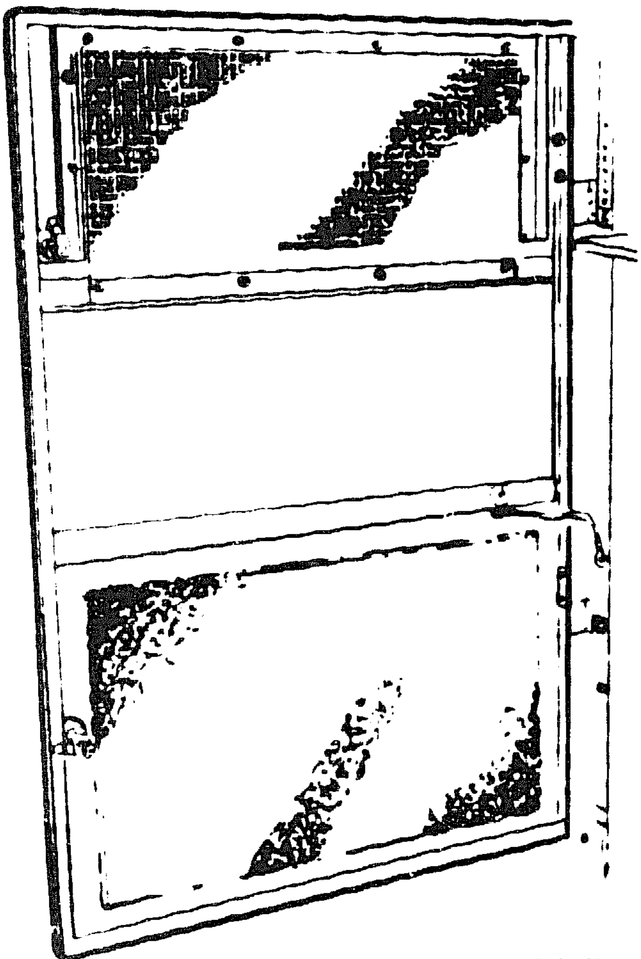


Table 11–2: Rear Cabinet Door and Air Filter Specifications

Parameter	Description
Rear Door:	70-24124-01
Dimensions:	28" W x 41.5" D
Weight:	20 lbs
Air Filters:	12-11255-17 — 26" W x 15.5" D (air intake) 12-11255-22 — 22" W x 9.5" D
Tools Required:	3/8" and 11/32" nutdrivers

For the removal and replacement procedures for the rear door and filters, see Section 11.1.

11.3 Airflow Sensor Removal and Replacement

The airflow sensor (see Figure 11-3) is mounted inside the cabinet above the XMI power regulators, to the left of the temperature sensor. The airflow sensor regulates the two blowers and shuts down the power regulators if the airflow in the cabinet is inadequate.

Figure 11-3: Airflow Sensor (Front View)

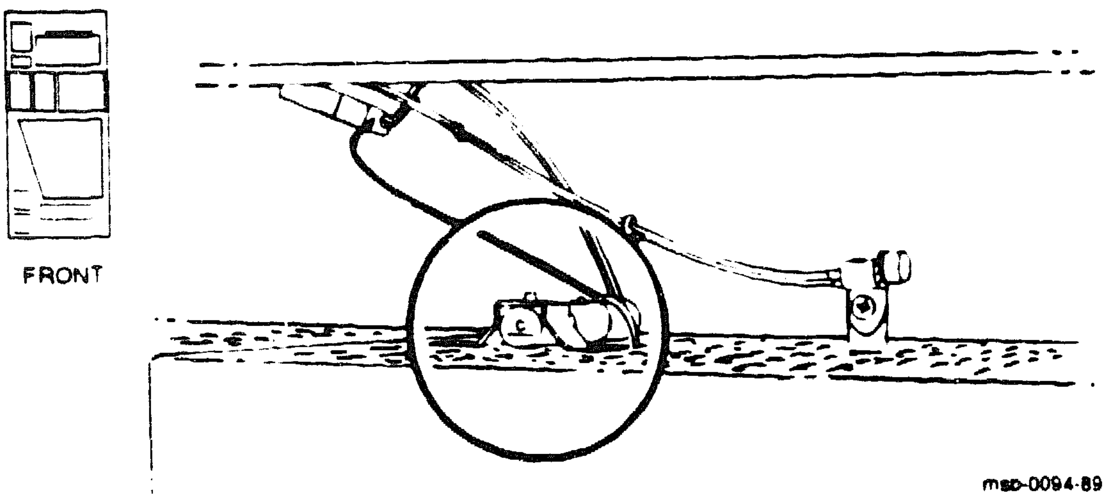


Table 11-3: Airflow Sensor Specifications

Parameter	Description
Part Number:	12-25024-11
Location:	From the front, the sensor is above the outlet grill of the XMI power regulators and to the left of the temperature sensor.
Signal Cable:	17-01570-01, to both blowers and to the H7206 PAL unit
Power:	+24 V (common to main blowers)
Service From:	Front of the cabinet, doors open
Tools Required:	Large and small Phillips screwdrivers Wire clipper

OPERATION

If the airflow sensor detects inadequate airflow, it signals the H7206 power and logic (PAL) unit. After 30 seconds the H7206 unit asserts the Interlock Inhibit signals to the XMI and VAXBI power regulators. The red LED on the H7206 PAL unit lights. The AC power is not affected.

Turn the system off at the control panel as you investigate the cause of the problem. To restart the system, use the front control panel. If the red LED on the H7206 stays on when one side of the system powers up, the problem may be an Interlock switch or the overtemperature switch in the H7215 regulator. If, however, both sides stay down, check the bias LEDs. If they are lit, check the airflow sensor signal. If it is low, indicating normal operating conditions, the H7206 PAL unit needs to be replaced.

REMOVAL

1. Perform an orderly shutdown of the system.
2. Turn the upper key switch on the front control panel to the Off position.
3. Pull the main circuit breaker on the AC power controller to the Off position.
4. Unplug the system power cord.
5. Wait 2 minutes for the capacitors to discharge.
6. Open the front and rear doors.
7. Unplug at the connector.
8. Clip and remove the tiewrap around the sensor.
9. Push down on top of the metal bracket to pop out one side so that you can remove the sensor. Leave the bracket in the grillwork or mark the exact location so that the new sensor is placed in the same spot.

REPLACEMENT

1. Slip the new sensor in under the bracket and push the end of the bracket back into the grill.
2. Secure in place with a tiewrap (90-07031-00).
3. Reattach at the connector.
4. Reverse steps 1 through 6 in the **REMOVAL** section above.

11.4 Temperature Sensor Removal and Replacement

The temperature sensor (see Figure 11-4) is mounted inside the cabinet above the XMI power regulators, to the right of the airflow sensor. When the system overheats, the sensor signals the H405 AC power controller to shut down the system.

Figure 11-4: Temperature Sensor (Front View)

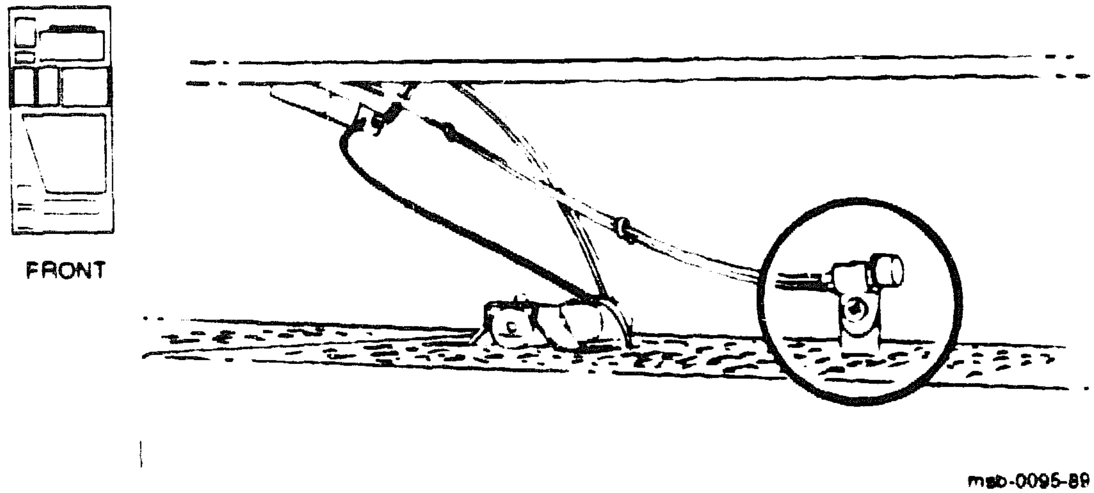


Table 11–4: Temperature Sensor Specifications

Parameter	Description
Part Number:	17-01844-01, sensor and cable to J9 on the H405 power controller
Location:	From the front, the sensor is above the outlet grill of the XMI power regulators and to the right of the airflow sensor.
Power:	H405 power controller
Threshold:	75°C (167°F)
Service From:	Inside the rear door
Tools Required:	Small Phillips screwdriver

OPERATION

When the temperature sensor reaches its threshold, it signals the H405 AC power controller to cut off all power. When the sensor cools down, the power is restored automatically.

REMOVAL AND REPLACEMENT

The temperature sensor is permanently attached to the cable that goes to the power controller.

To remove a temperature sensor:

1. Perform an orderly shutdown of the system.
2. Turn the upper key switch on the front control panel to the Off position.
3. Pull the main circuit breaker on the AC power controller to the Off position and unplug the system power cord.
4. Wait 2 minutes for the capacitors to discharge.
5. Open the front and rear doors.
6. Unplug the cable at J9 on the H405 power controller.
7. Pull the cable up through the system.
8. With a Phillips screwdriver remove the screw from the bracket that holds the sensor.

Install the new sensor in the same place. Reverse steps 1 through 7 above.

11.5 Blower Assembly Specifications

Two blowers are located in the center of the cabinet, just below the XMI and VAXBI card cages. The mounting plate with the four captive screws (see Figure 11-5) is part of the blower assembly (12-27848-01).

Figure 11-5: Blower Assembly

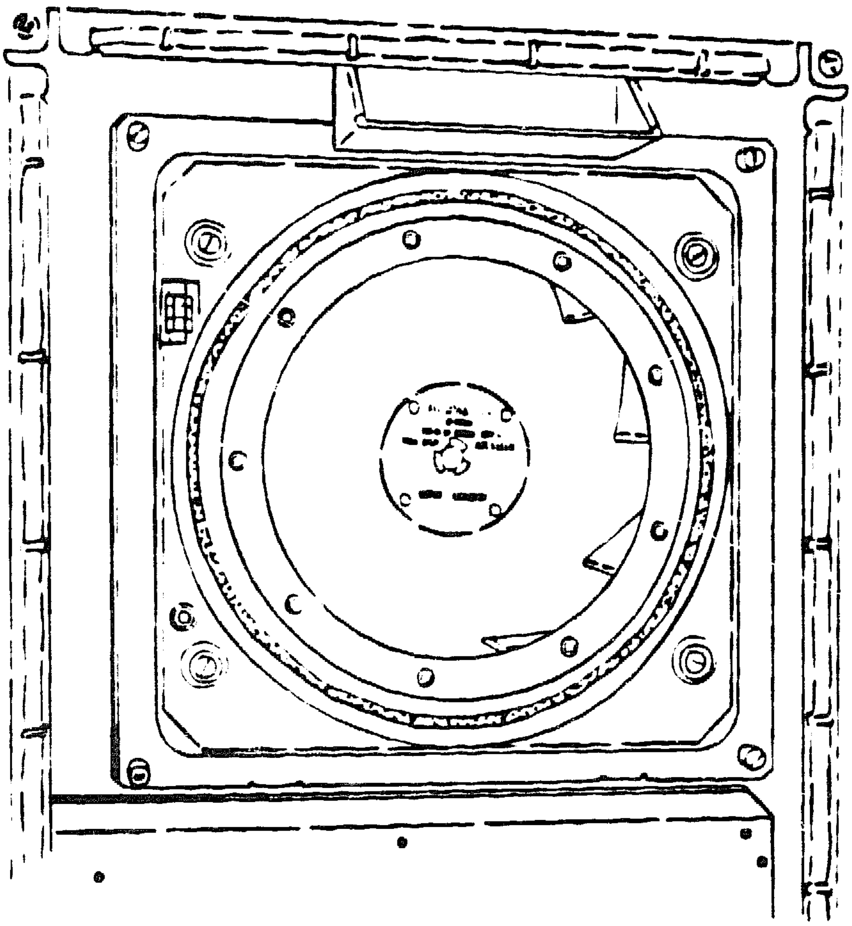


Table 11–5: Blower Assembly Specifications

Parameter	Description
Part Number:	12-27848-01, two used
Location:	Front and rear of the lower cabinet area
Dimensions:	15" x 15"
Weight:	9 lbs
Power:	+24 V
Signal Cable:	17-01570-01, to the H7206 PAL unit and to the airflow sensor
Service From:	Front and rear of cabinet doors open
Tools Required:	Large Phillips and 1/4" flat screwdrivers

Each system has two blowers to provide the required airflow within the cabinet. If the airflow sensor detects inadequate airflow, it signals the H7206 power and logic (PAL) unit. After 30 seconds the H7206 unit asserts the Interlock Inhibit signals to the XMI and VAXBI power regulators. The red LED on the H7206 PAL unit lights. The AC power is not affected.

11.6 Blower Assembly, Front and Rear

Figure 11–6 and Figure 11–7 show the two blowers, each with their protective grillwork in place. Although the mounting of the two units is somewhat different, once you remove the protective grillwork from the rear blower assembly the same removal procedures apply to both blowers.

Figure 11–6: Front Blower

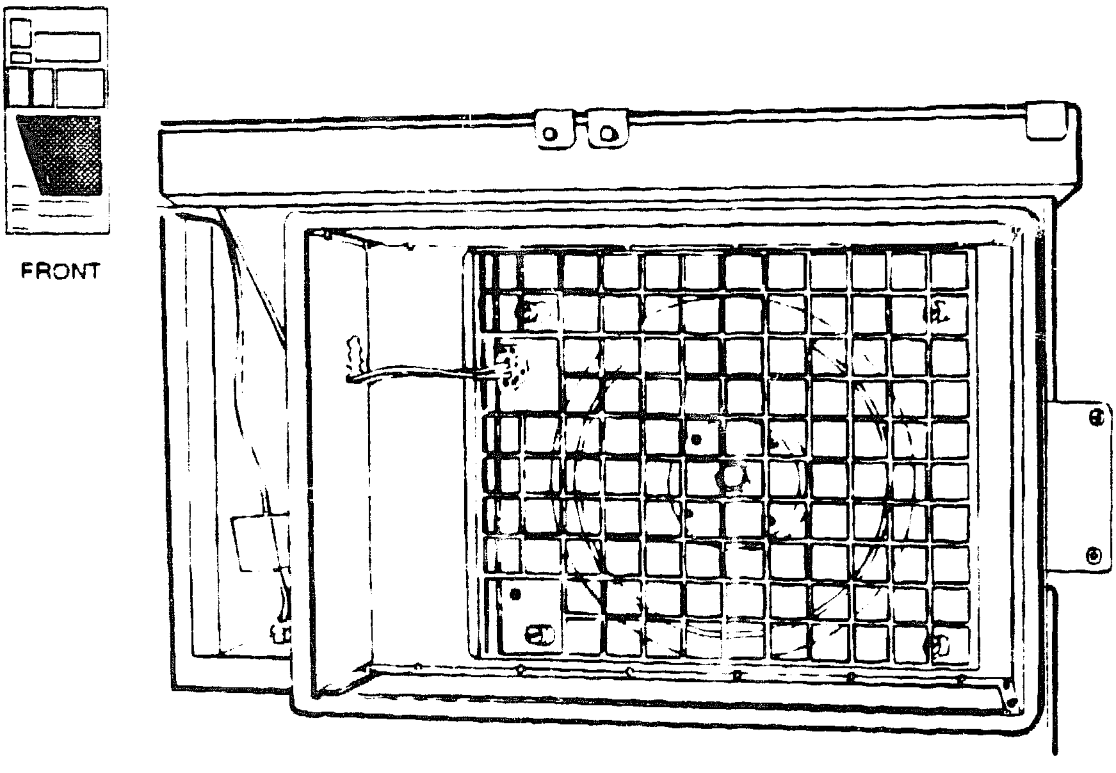
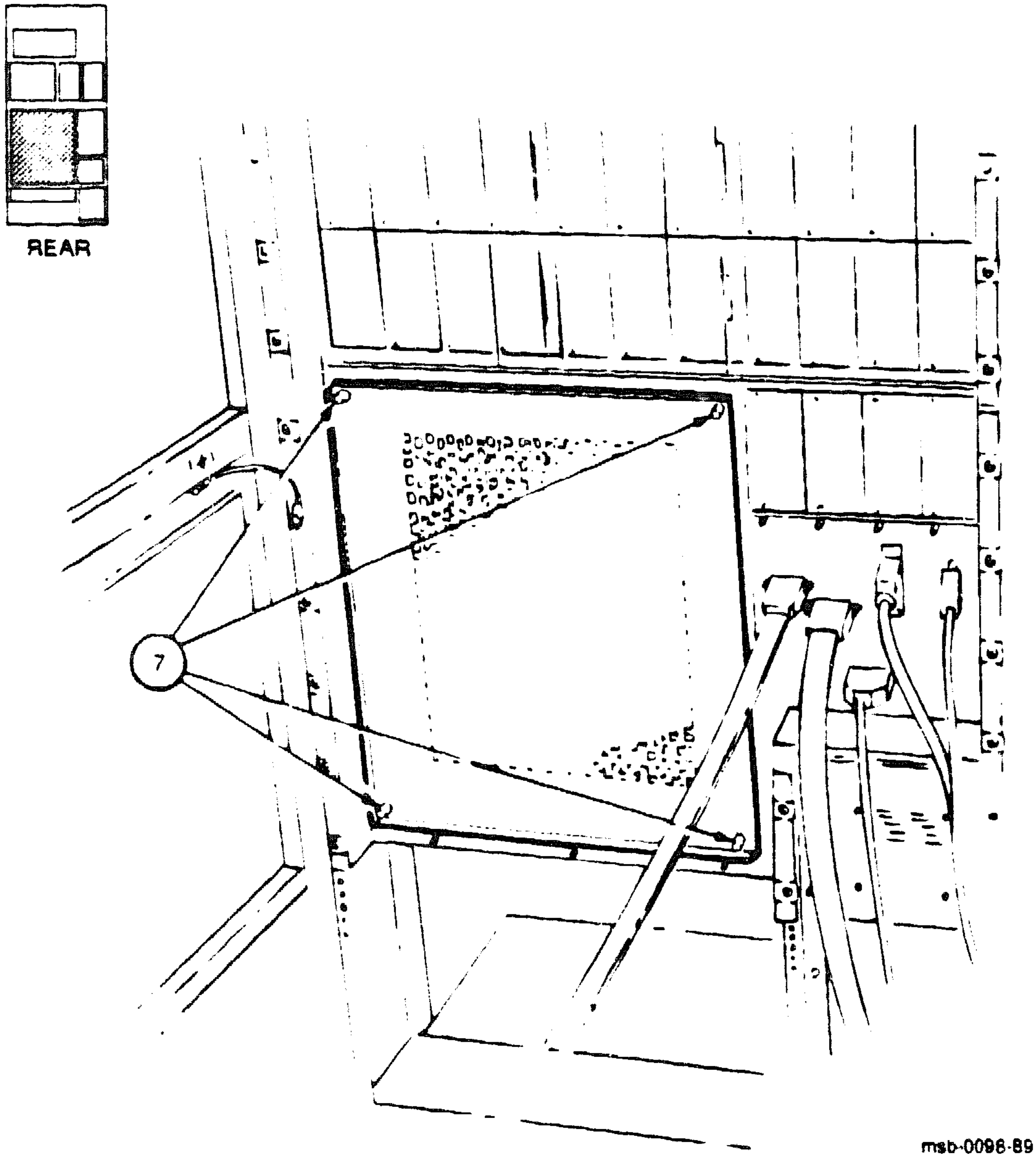


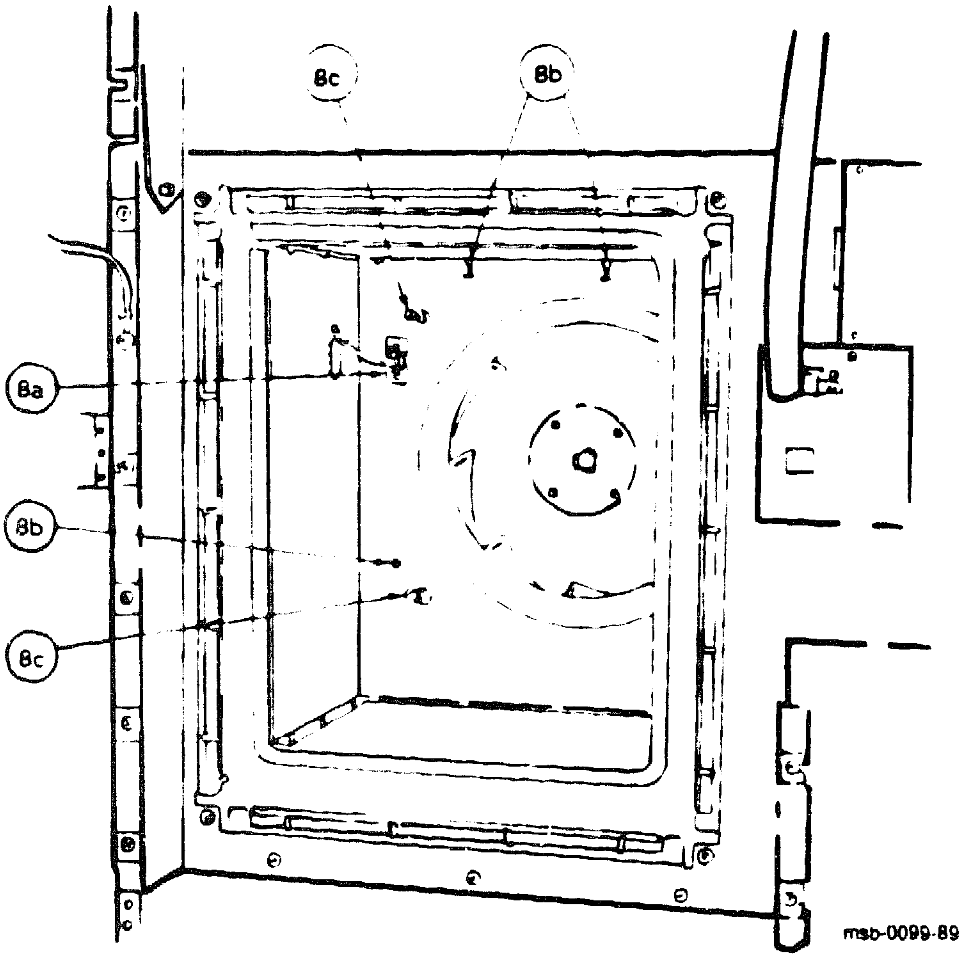
Figure 11–7: Rear Blower



11.7 Blower Assembly Removal and Replacement

To remove the rear blower, you must first remove the protective grillwork. You do not need to remove the grillwork from in front of the blower in front, as it can be lifted off with the plenum.

Figure 11-8: Blower Assembly Removal (Rear View)



REMOVAL

1. Perform an orderly shutdown of the system.
2. Turn the upper key switch on the front control panel to the Off position.
3. Pull the circuit breaker on the AC power controller to the Off position.
4. Unplug the system power cord.
5. Wait 2 minutes for the capacitors to discharge.
6. Open the front or rear door to access the blower to be replaced.
7. Callout ❼ in Figure 11–7 shows the four captive screws that must be loosened to lift off the metal grill in front of the rear blower. Figure 11–8 shows the rear blower with the metal grill removed.
8. The plenum must now be lifted off away from the blower.
   a. Unplug the power cord and push it through the hole on the left panel. See Figure 11–8.
   b. Remove the two #10-32 screws inside the top panel and one screw at the left on the panel at the back of the plenum.
   c. Shift the plenum to the left and lift it off from the four screws.

REPLACEMENT

To replace the blower, reverse the steps above. Note that the blower has two metal tabs at the bottom that slide into slots in the cabinet.

11.8 Side Panel Removal

The right side panel of the system cabinet is detachable, so that the cabinet can be bolted to an expander cabinet.

Figure 11–9: Side Panel Removal (Front View)

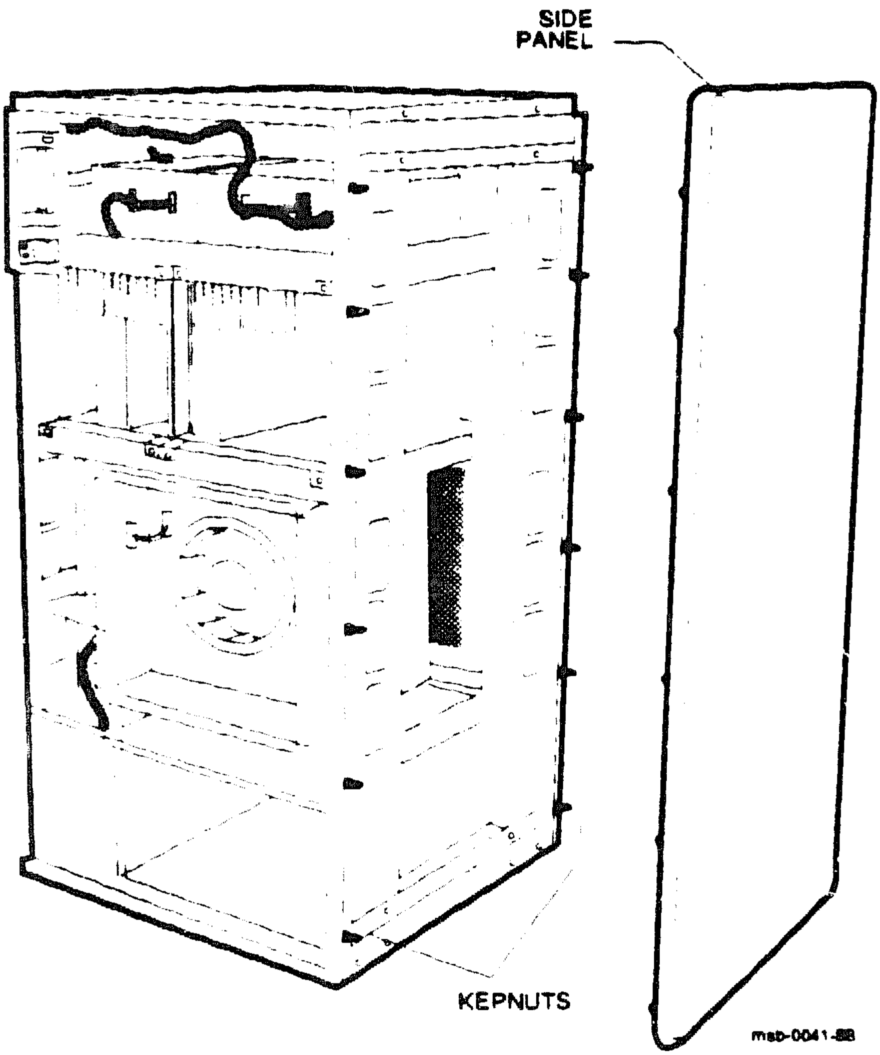


Table 11–6: Side Panel Specifications

Parameter	Description
Part Number:	70-19485-00
Location:	From the front, the panel on the right side is removable.
Dimensions:	30" W x 57" H x 3/4" D
Weight:	34.25 lbs
Service From:	Right side of cabinet, as viewed from the front
Tools Required:	7/16" socket wrench

For most configurations, expansion will be to the right of the system cabinet. To prepare for expansion, remove the side panel of the system cabinet as follows:

1. Open the front and rear doors of the system cabinet and remove the doors by lifting them off their hinges.
2. Using a 7/16 inch socket wrench, remove the system cabinet's side panel by removing the 12 kepnuts (see Figure 11–9). Carefully lift the panel when removing it so as not to damage the threaded bolts. Do not remove the bolts.
3. Before attaching another cabinet, make sure the braided RFI shielding and securing clips are not damaged or missing. Check that any flexible spring-strip type RFI gaskets are present in all the mounting holes.

The *VAX 6000–400 Installation Guide* describes how to attach the system cabinet to a VAXBI expander cabinet.

APPENDIX A

Appendix A
Troubleshooting the System

Table A–1 gives a checklist for troubleshooting a system that will not power-up and boot. For additional information on troubleshooting, see the following:

- Chapter 2, Diagnostics
- Section 3.6, KA64A Self-Test Results: Console Display
- Section 3.7, KA64A Self-Test Results: Module LEDs
- Section 3.8, KA64A Self-Test Results: XGPR Register
- Section 3.9, ROM-Based Diagnostics
- Section 3.10, KA64A Self-Test — RBD 0
- Section 3.11, CPU/Memory Interaction Tests — RBD 1
- Section 3.12, VAX/DS Diagnostics
- Section 4.3, FV64A Configuration Rules
- Section 4.5, Self-Test Results: Console Display and Self-Test LED
- Section 4.6, Self-Test Results: Scalar XGPR Register
- Section 4.7, Vector Processor Tests — RBD 0 and RBD 1
- Section 4.8, VAX/DS Diagnostics
- Section 5.2, MS62A Configuration Rules
- Section 5.8, Memory Self-Test
- Section 5.9, Memory Self-Test Errors
- Section 5.10, MS62A Memory Tests — RBD 3
- Section 5.13, MS62A Memory Installation
- Section 6.4, DWMBA Tests — RBD 2
- Section 7.6, XMI Troubleshooting

- Section 8.6, VAXBI Troubleshooting
- Appendix B, Console Error Messages
- *VAX 6000–400 Owner's Manual*
  Chapter 3, Controls and Indicators
  Chapter 6, System Self-Test and Troubleshooting

Table A–1: Troubleshooting the System

	Check	Comment	See also
	Control Panel Lights Don't Work		
1	Check the AC power.	Check lights on the AC power controller; check that the system is plugged in and power is present.	Section 10.11
2	Check the circuit breaker.	If the circuit breaker is tripped, your system may have experienced an AC overcurrent.	Sections 10.11 and 10.12
3	Check the H7206 LEDs.	The LEDs should be green, green, no red.	Section 10.8.2
		If red is lit, check the card cage doors and check for an overtemperature condition.	Sections 7.6, 8.6, and 11.4
4	Check the green LEDs on the regulators.	If the LEDs are not lit, you may have a bad regulator or power cabling problem.	Sections 10.4 and 10.6
	System Shuts Off 30 Seconds After Power-Up		
1	Check the airflow sensor.		Section 11.3
2	Check the blowers.	Look for obstructed or no motion. Check blower power and cable connections.	Sections 11.6 and 11.7

Table A–1 (Cont.): Troubleshooting the System

	Check	Comment	See also
	No Output on Console, Control Panel Fault LED Is On		
1	Check the XMI and VAXBI LEDs.		Section 3.7
2	Check the processors.	Use self-test and RBD diagnostics.	Sections 3.6 to 3.11
3	Check your configuration.	XMI node 1 or E must be populated; neither can house a memory.	Sections 3.2, 4.3, 5.2, and 6.3
4	Force a boot processor		Owner's Manual, Chapter 6
5	Check the H7206 power and logic unit.	LEDs should be lit.	Section 10.8.2
	No Output on Console, Control Panel Fault LED Is Off		
1	Check baud rate	Press BREAK on the console terminal keyboard.	Owner's Manual, Chapter 5
2	Check the cabling to the console.		Terminal owner's manual
3	Check the console terminal		Terminal owner's manual
	DWMBA Fails Self-Test		
1	Check the DWMBA hardware.	Failure can be caused by any of the following: DWMBA/A, DWMBA/B, cable connecting DWMBA/A and DWMBA/B, backplane.	Sections 6.1, 6.3, 7.5, 7.6, and 8.6
2	Check the boot processor if more than one DWMBA appears bad.	Change the boot processor with the SET CPU console command, then rerun RBD 2. If it fails, the problem is in the DWMBA; if it passes, the first boot processor is bad.	Sections 3.16 and 6.4

APPENDIX B

Appendix B
Console Error Messages

Table B–1 lists messages that appear when the processor halts and the console gains control. These messages are followed by:

- PC = xxxxxxxx — program counter = address at which the processor halted or the exception occurred
- PSL = xxxxxxxx — processor status longword = contents of the register
- –SP = xxxxxxxx — –SP is one of the following:
  ESP executive stack pointer
  ISP interrupt stack pointer
  KSP kernel stack pointer
  SSP supervisor stack pointer
  USP user stack pointer

Table B–2 lists other console error messages.

Table B–1: Console Error Messages Indicating Halt

Error Message	Meaning
?02 External halt (CTRL/P, break, or external halt).	CTRL/P or STOP command.
?03 Power-up halt.	System has powered up, had a system reset, or an XMI node reset.
?04 Interrupt stack not valid during exception processing.	Interrupt stack pointer contained an invalid address.
?05 Machine check occurred during exception processing.	A machine check occurred while handling another error condition.
?06 Halt instruction executed in kernel mode.	The CPU executed a Halt instruction.
?07 SCB vector bits <1:0> = 11.	An interrupt or exception vector in the System Control Block contained an invalid address.

Table B-1 (Cont.): Console Error Messages Indicating Halt

Error Message	Meaning
?08 SCB vector bits <1:0> = 10.	An interrupt or exception vector in the System Control Block contained an invalid address.
?0A CHMx executed while on interrupt stack.	A change-mode instruction was issued while executing on the interrupt stack.
?10 ACV/TNV occurred during machine check processing.	An access violation or translation-not-valid error occurred while handling another error condition.
?11 ACV/TNV occurred during kernel-stack-not-valid processing.	An access violation or translation-not-valid error occurred while handling another error condition.
?12 Machine check occurred during machine check processing.	A machine check occurred while processing a machine check.
?13 Machine check occurred during kernel-stack-not-valid processing.	A machine check occurred while handling another error condition.
?19 PSL <26:24>= 101 during interrupt or exception.	An exception or interrupt occurred while on the interrupt stack but not in kernel mode.
?1A PSL <26:24>= 110 during interrupt or exception.	An exception or interrupt occurred while on the interrupt stack but not in kernel mode.
?1B PSL <26:24>= 111 during interrupt or exception.	An exception or interrupt occurred while on the interrupt stack but not in kernel mode.
?1D PSL <26:24> = 101 during REI.	An REI instruction attempted to restore a PSL with an invalid combination of access mode and interrupt stack bits.
?1E PSL <26:24> = 110 during REI.	An REI instruction attempted to restore a PSL with an invalid combination of access mode and interrupt stack bits.
?1F PSL <26:24> = 111 during REI.	An REI instruction attempted to restore a PSL with an invalid combination of access mode and interrupt stack bits.

Table B–2: Standard Console Error Messages

Error Message	Meaning
?20 Illegal memory reference.	An attempt was made to reference a virtual address (/V) that is either unmapped or is protected against access under the current PSL.
?21 Illegal command.	The command was not recognized, contained the wrong number of parameters, or contained unrecognized or inappropriate qualifiers.
?22 Illegal address.	The specified address was recognized as being invalid, for example, a general purpose register number greater than 15.
?23 Value is too large.	A parameter or qualifier value contained too many digits.
?24 Conflicting qualifiers.	A command specified recognized qualifiers that are illegal in combination.
?25 Checksum did not match	The checksum calculated for a block of X command data did not match the checksum received.
?26 Halted	The processor is currently halted.
?27 Item was not found.	The item requested in a FIND command could not be found.
?28 Timeout while waiting for characters.	The X command failed to receive a full block of data within the timeout period.
?29 Machine check accessing memory	Either the specified address is not implemented by any hardware in the system, or an attempt was made to write a read-only address, for example, the address of the 33rd Mbyte of memory on a 32-Mbyte system.
?2A Unexpected machine check or interrupt.	A valid operation within the console caused a machine check or interrupt.
?2B Command is not implemented.	The command is not implemented by this console.
?2C Unexpected exception.	An attempt was made to examine either a nonexistent IPR or an unimplemented register in RSSC address range (20140000—20140800).

Table B–2 (Cont.): Standard Console Error Messages

Error Message	Meaning
?2D For Secondary Processor n.	This message is a preface to second message describing some error related to a secondary processor. This message indicates which secondary processor is involved.
?2E Specified node is not an I/O adapter.	The referenced node is incapable of performing I/O or did not pass its self-test.
?30 Write to Z command target has timed out.	The target node of the Z command is not responding.
?31 Z connection terminated by ^P.	A CTRL/P was typed on the keyboard to terminate a Z command.
?32 Your node is already part of a Z connection.	You cannot issue a Z command while executing a Z command.
?33 Z connection successfully started.	You have requested a Z connection to a valid node.
?34 Specified target already has a Z connection.	The target node was the target of a previous Z connection that was improperly terminated. Reset the system to clear this condition.
?36 Command too long.	The command length exceeds 80 characters.
?37 Explicit interleave list is bad. Configuring all arrays uninterleaved.	The list of memory arrays for explicit interleave includes no nodes that are actually memory arrays. All arrays found in the system are configured.
?39 Console patches are not usable.	The console patch area in EEPROM is corrupted or contains a patch revision that is incompatible with the console ROM.
?3B Error encountered during I/O operation.	An I/O adapter returned an error status while the console boot primitive was performing I/O.
?3C Secondary processor not in console mode.	The primary processor console needed to communicate with a secondary processor, but the secondary processor was not in console mode. STOP the node or reset the system to clear this condition.

Table B–2 (Cont.): Standard Console Error Messages

Error Message	Meaning
?3D Error initializing I/O device.	A console boot primitive needed to perform I/O, but could not initialize the I/O adapter.
?3E Timeout while sending message to secondary processor.	A secondary processor failed to respond to a message sent from the primary. The primary sends such messages to perform console functions on secondary processors.
?3F Microcode power-up self-test failed in REX520.	CPU chip failed its microcoded self-test.
?40 Key switch must be at "Update" to update EEPROM.	A SET command was issued, but the key switch was not set to allow updates to the EEPROM.
?41 Specified node is not a bus adapter.	A command to access a VAXBI node specified an XMI node that was not a bus adapter.
?42 Invalid terminal speed.	The SET TERMINAL command specified an unsupported baud rate.
?43 Unable to initialize node.	The INITIALIZE command failed to reset the specified node.
?44 Processor is not enabled to BOOT or START.	As a result of a SET CPU/NOENABLE command, the processor is disabled from leaving console mode.
?45 Unable to stop node.	The STOP command failed to halt the specified node.
?46 Memory interleave set is inconsistent. n n ...	The listed nodes do not form a valid memory interleave set. One or more of the nodes might not be a memory array or might be of a different size, or the set could contain an invalid number of members. Each listed array that is a valid memory will be configured uninterleaved.
?47 Insufficient working memory for normal operation.	Less than 256 Kbytes per processor of working memory were found. There is insufficient memory for the console to function normally or for the operating system to boot.

Table B-2 (Cont.): Standard Console Error Messages

Error Message	Meaning
?48 Uncorrectable memory errors—long memory test must be performed.	A memory array contains an unrecoverable error. The console must perform a slow test to locate all the failing locations.
?49 Memory cannot be initialized.	The specified operation was attempted and prevented.
?4A Memories not interleaved due to uncorrectable errors:	The listed arrays would normally have been interleaved (by default or explicit request). Because one or more of them contained unrecoverable errors, this interleave set will not be constructed.
?4B Internal logic error in console.	The console encountered a theoretically impossible condition.
?4C Invalid node for Z command.	The target of a Z command must be a CPU or an I/O adapter and must not be the primary processor.
?4D Invalid node for new primary.	The SET CPU command failed when attempting to make the specified node the primary processor.
?4E Specified node is not a processor.	The specified node is not a processor, as required by the command.
?4F System serial number has not been initialized.	No CPU in the system contains a valid system serial number.
?50 System serial number not initialized on primary processor.	The primary processor has an uninitialized system serial number. All other processors in the system contain a valid serial number.
?51 Secondary processor returned bad response message.	A secondary processor returned an unintelligible response to a request made by the console on the primary processor.
?52 ROM revision mismatch. Secondary processor has revision *x.xx*.	The revision of console ROM of a secondary processor does not match that of the primary.
?53 EEPROM header is corrupted.	The EEPROM header has been corrupted. The EEPROM must be restored from the TK tape drive.

Table B–2 (Cont.): Standard Console Error Messages

Error Message	Meaning
?54 EEPROM revision mismatch. Secondary processor has revision x.xx / y.yy.	A secondary processor has a different revision of EEPROM or has a different set of EEPROM patches installed.
?55 Failed to locate EEPROM area.	The EEPROM did not contain a set of data required by the console. The EEPROM may be corrupted.
?56 Console parameters on secondary processor do not match primary.	The console parameters are not the same for all processors .
?57 EEPROM area checksum error.	A portion of the EEPROM is corrupted. It may be necessary to reload the EEPROM from the TK tape drive.
?58 Saved boot specifications on secondary processor do not match primary.	The saved boot specifications are not the same for all processors.
?59 Invalid unit number.	A BOOT or SET BOOT command specified a unit number that is not a valid hexadecimal number between 0 and FF.
?5A System serial number mismatch. Secondary processor has xxxxxxxx.	The indicated serial number of a secondary processor does not match that of the primary.
?5B Unknown type of boot device.	The console program does not have a boot primitive to support the specified type of device or the device could not be accessed to determine its type.
?5C No HELP is available.	The HELP command is not supported when the console language is set to International.
?5D No such boot spec found.	The specified boot specification was not found in the EEPROM.
?5E Saved boot spec table full.	The maximum number of saved boot specifications has already been stored.
?5F EEPROM header version mismatch.	Processors have different versions of EEPROMs.
?61 EEPROM header or area has bad format.	All or part of the EEPROM contains inconsistent data and is probably corrupted. Reload the EEPROM from the TK tape.
?62 Illegal node number.	The specified node number is invalid.

Table B-2 (Cont.): Standard Console Error Messages

Error Message	Meaning
?63 Unable to locate console tape device.	The console could not locate the I/O adapter that controls the TK tape.
?64 Operation only applies to secondary processors	The command can only be directed at a secondary processor.
?65 Operation not allowed from secondary processor	A secondary processor cannot perform this operation.
?66 Validation of EEPROM tape image failed.	The image on tape is corrupted or is not the result of a SAVE EEPROM command. The image cannot be restored.
?67 Read of EEPROM image from tape failed.	The EEPROM image was not successfully read from tape.
?68 Validation of local EEPROM failed	For a PATCH EEPROM operation, the EEPROM must first contain a valid image before it can be patched. For a RESTORE EEPROM operation, the image was written back to EEPROM but could not be read back successfully.
?69 EEPROM not changed.	The EEPROM contents were not changed.
?6A EEPROM changed successfully	The EEPROM contents were successfully patched or restored.
?6B Error changing EEPROM.	An error occurred in writing to the EEPROM. The EEPROM contents may be corrupted.
?6C EEPROM saved to tape successfully	The EEPROM contents were successfully written to the TK tape.
?6D EEPROM not saved to tape.	The EEPROM contents were not completely written to the TK tape.
?6E EEPROM Revision = *x.xx* / *y.yy*.	The EEPROM contents are at revision *x.xx* with revision *y.yy* patches
?6F Major revision mismatch between tape image and EEPROM	The major revision of tape and EEPROM do not match. The requested operation cannot be performed.
?70 Tape image Revision = *x.xx* / *y.yy*.	The EEPROM image on the TK tape is at revision *x.xx* with revision *y.yy* patches.

Table B-2 (Cont.): Standard Console Error Messages

Error Message	Meaning
?73 System serial number updated	The EEPROM has been updated with the correct system serial number
?74 System serial number not updated.	The EEPROM has not been changed
?75 /CONSOLE_LIMIT value too small for proper operation. Value ignored	No change has been made
?76 Error writing to tape. Tape may be write-locked.	Tape has not been written. Check to see if tape is write-locked.
?77 CCA not accessible or corrupted	Attempt to find the console communications area (CCA) failed. The console then builds a local CCA, which does not allow for interprocessor communication
?78 Vector module configuration error at node *n*	The console detected a vector module configuration error. Problem can be that the vector node number is not one greater than the scalar CPU or that the module to the left of a vector processor is not a memory module
?79 Vector synchronization error	The console could not synchronize with the vector processor on a console entry. The Busy bit in the Vector Processor Status Register remained set after a timeout, or a vector processor error occurred.
?7A No vector module associated with CPU at specified node	No vector module is in the slot to the left of the specified CPU, or the VIB cable either is not attached or is bad.
?7B An error occurred while accessing the vector module	Attempt to access VCR, VLR, or VMR registers failed
?7D Vector module is disabled—check KA64A revision at XMI node *n*	The vector module is attached to a KA64A module that is not at the revision level required.
?83 Loading system software.[1]	The console is attempting to load the operating system in response to a BOOT command, power-up, or restart failure.
?84 Failure.[1]	An operation did not complete successfully. Should be issued with another message to clarify failure.

[1]No numbered prefix appears with these messages in English language mode. These numbers are used for these messages in International mode.

Table B-2 (Cont.): Standard Console Error Messages

Error Message	Meaning
?85 Restarting system software [1]	The console is attempting to restart the in-memory copy of the operating system following a power-up or serious error.
?A0 Initializing system [1]	The console is resetting the system in response to a BOOT command.
?A6 Console halting after unexpected machine check or exception.[1]	The console executed a Halt instruction to reset the console state after processing an unexpected machine check.
?A7 RCSR <WD> is set. Local CCA must be built.	When the <WD> bit is set, writes to memory are disabled. The processor must then build a CCA in local memory. Main memory cannot be written to or accessed with interlocked instructions.
?A8 Bootstrap failed due to previous error [1]	The previous attempt to bootstrap the system failed.
?A9 Restart failed due to previous error [1]	The previous attempt to restart the system failed.
Node n ?xx	Error message ?xx was generated on secondary processor *n* and was passed to the primary processor to be displayed.

[1]No numbered prefix appears with these messages in English language mode. These numbers are used for these messages in International mode.

APPENDIX C

Appendix C
Cable List

The following table lists the replaceable cables in the system.

Table C–1: Cable List

Part Number	Qty	Description
17-00365-03	1	H405 to battery backup unit and disks
17-00849-08	2	18" DWMBA/B to DWMBA/B AC/DC OK
17-00962-01	1	H7206 to H7231 battery backup unit (optional)
17-01149-01	1	Boot enable jumper for DEBNA module
17-01445-01	1	Power to logic board internal to H7206
17-01446-01	1	H7206 to three regulators' jumps (XMI side)
17-01447-01	1	H7206 to two regulators' jumps (VAXBI side)
17-01458-02	2	VAXBI ground strap
17-01496-01	1	VAXBI to Ethernet port and H7214
17-01497-02	1	H7206 to XMI H7215 and H7214, 72 in. long
17-01498-01	1	XTC to H7206 signal 14-pin
17-01499-01	2	Interlock cable
17-01501-01	1	H405 to H7206
17-01523-01	1	H7215 regulator to VAXBIs ±12V
17-01525-01	3	H7214 regulator to bus bars (+5V remote sense)
17-01549-01	1	H7206 to H405 DEC power bus
17-01566-01	1	H7215 regulator to the XMI
17-01567-01	1	XTC to console port, 10-pin ribbon
17-01568-02	1	XMI to XTC (XTC power) 20-pin ribbon, 56 in. long

Table C–1 (Cont.): Cable List

Part Number	Qty	Description
17-01569-01	1	DWMBA to H7206 power OK signals
17-01570-01	1	H7206 to both blowers and airflow sensor
17-01661-01	3	Jumper assembly (on H7214 regulator output)
17-01662-02	1	XMI ground strap
17-01663-01	3	Fuse cable (H7214 BTO)
17-01666-01	1	H7206 to VAXBI regulators' signal, 60 in. long
17-01812-01	1	XMI to filter board in system control assembly
17-01813-01	1	TBK70 board to system control assembly TK signal swapper
17-01815-01	2	H405 to transformer cable (240V systems only)
17-01816-01	1	XMI to system control assembly 20- to 26-pin
17-01817-01	1	TK to system control assembly 26-pin ribbon
17-01833-01	1	Fail safe enable cable, H7231 battery backup unit to H405 and the XMI
17-01844-01	1	Temperature sensor cable, to H405
17-01897-01	2	15' DWMBA/A to DWMBA/B connector, for VAXBI expander cabinet
17-01897-02	2	7' DWMBA/A to DWMBA/B cables, from XMI slot E
17-01897-03	2	25' DWMBA/A to DWMBA/B cables, from XMI slot D
17-01920-01	1	AC/DC OK cable, for VAXBI expander cabinet
17-02240-03	1	Scalar/vector intermodule VIB cable
70-20369-2F	1	H7206 to battery backup unit

APPENDIX D

Appendix D
XMI Backplane Connectors

Figure D–1 shows the numbering scheme used on the XMI backplane connectors. Note that the view is from the rear of the backplane.

Figure D–1: XMI Backplane Connector Numbering

46	16		31	1
47	17		32	2
48	18		33	3
49	19		34	4
50	20	M	35	5
51	21	o	36	6
52	22	d	37	7
53	23	u	38	8
54	24	l	39	9
55	25	e	40	10
56	26		41	11
57	27		42	12
58	28		43	13
59	29		44	14
60	30		4	15

APPENDIX E

Appendix E

Parse Trees

This appendix shows parse trees for the following:

- KA64A machine checks
- KA64A hard error interrupts
- KA64A soft error interrupts
- FV64A machine checks
- FV64A hard error interrupts
- FV64A soft error interrupts
- FV64A disable faults

Figure E–1: KA64A Machine Check Parse Tree

(select one)

Machine check code	Meaning
MCHK_FP_PROTOCOL_ERROR (01 hex)	F-chip protocol error
MCHK_FP_ILLEGAL_OPCODE (02 hex)	F-chip illegal opcode
MCHK_FP_OPERAND_PARITY (03 hex)	F-chip operand parity error
MCHK_FP_UNKNOWN_STATUS (04 hex)	F-chip unknown result status
MCHK_FP_RESULTS_PARITY (05 hex)	F-chip result parity error
MCHK_TBM_ACV_TNV (08 hex)	TB miss status during ACV/TNV processing
MCHK_TBH_ACV_TNV (09 hex)	TB hit status during ACV/TNV processing
MCHK_INT_ID_VALUE (0A hex)	Undefined interrupt ID value
MCHK_MOVC_STATUS (0B hex)	MOVCx status encoding error
MCHK_UNKNOWN_IBOX_TRAP (0C hex)	Unknown I-box trap

MCHK_BUSERR_READ_PCACHE
(select all)

Condition	Meaning
PCSTS<TAG_PARITY_ERROR> (PCSTS<8>)	P-cache tag parity error on D-stream read hit
PCSTS<P_DATA_PARITY_ERROR> (PCSTS<10>)	P-cache data parity error on D-stream read hit
neither	Inconsistent status (one or both bits must be set)

msb-p069-89

Figure E–1 Cont'd. on next page

Figure E–1 (Cont.): KA64A Machine Check Parse Tree

```
MCHK_BUSERR_READ_DAL (11 hex)
  (select one)
  PCSTS<DAL_DATA_PARITY_ERROR> (PCSTS<9>)
    (select one)
    PCSTS<B_CACHE_HIT> (PCSTS<12>)
      ---> Backup cache data parity error
           on D-stream read
    otherwise
      ---> REXMI data parity error on
           D-stream read
  PCSTS<BUS_ERROR> (PCSTS<11>)
    (select one)
    SSCBTR<RWT> (SSCBTR<30>)
      ---> RSSC bus timeout on D-stream read
    (XBER<FCMD> = read) AND (XFADR = PCERR) (select one)
    ((XBER<3:1> = 1 hex) AND (XFADR = IPR126))
      XBER<RSE> (XBER<17>)
        ---> XMI read sequence error on first
             quadword of D-stream read
      XBER<RER> (XBER<16>)
        ---> XMI read error response on first
             quadword of D-stream read
      XBER<TTO> (XBER<13>)
        (select one)
        XBER<CNAK> (XBER<15>)
          ---> NXM on first quadword of D-stream
               read
        XBER<NRR> (XBER<18>)
          ---> XMI no read response for first
               quadword of D-stream read
        otherwise
          ---> No XMI grant to D-stream read
      otherwise
        ---> Inconsistent status (no XBER
             error bits set)
    otherwise
      ---> Inconsistent status (machine
           check during error interrupt)
  otherwise
    ---> Inconsistent status (no PCSTS
         error bits set)
```

msb-p070-89

Figure E–1 Cont'd. on next page

Figure E-1 (Cont.): KA64A Machine Check Parse Tree

```
 |
 |  MCHK_BUSERR_WRITE_DAL (12 hex)
 |----(select one)
 |   |
 |   |  SSCBTR<RWT> (SSCBTR<30>)
 |   |--------------------------------> RSSC bus timeout on write or
 |   |                                  clear write buffer
 |   |  otherwise
 |   |--------------------------------> Inconsistent status (no error
 |                                      bits set)
 |  MCHK_UNKNOWN_BUSERR_TRAP (13 hex)
 |------------------------------------> Unknown bus error trap
 |
 |  MCHK_VECTOR_STATUS (14 hex)
 |------------------------------------> Vector module error
 |
 |  MCHK_UNKNOWN_CS_ADDR (0D hex)
 |------------------------------------> Unexpected control store address
 |
 |  otherwise
 |------------------------------------> Inconsistent status (unknown
                                        machine check code)
```

NOTES

(select one)	-	exactly one case must be true. If zero or more than one is true, the status is inconsistent.
(select all)	-	more than one case may be true.
otherwise	-	fall-through case for (select one) if no other options are true.
neither	-	fall-through case for (select all) if none of the options are true.

The parse tree assumes that retry is enabled (RCSR<ARD> = 0).

msb-p071-89

Figure E-2: KA64A Hard Error Interrupt Parse Tree

```
─┐ (select all)
 │
 │ XBER<XFAULT> (XBER<26>)
 ├──────────────────────────────────────► XMI XFAULT signal asserted
 │
 │ XBER<WEI> (XBER<25>)
 ├──────────────────────────────────────► WE IVINTR received
 │
 │ XBER<IPE> (XBER<24>)
 ├───┐ (select one)
 │   │
 │   │ XBER<PE> (XBER<23>)
 │   ├──────────────────────────────────► ACKed parity error
 │   │
 │   │ otherwise
 │   └──────────────────────────────────► Inconsistent status (PE not
 │                                         set)
 │ RCSR<WDPE> (RCSR<28>)
 ├──────────────────────────────────────► DAL write data parity error
 │
 │ RCSR<SE> (RCSR<4>)
 ├──────────────────────────────────────► Second error
 │
 │ VINTSR<VHE> (VINTSR<2>)
 ├──────────────────────────────────────► Vector hard error
 │
 │ VINTSR<VECTL VIB HERR> (VINTSR<4>)
 ├──────────────────────────────────────► VECTL detected VIB hard error
 │
 │ VINTSR<CCHIP VIB HERR> (VINTSR<6>)
 ├──────────────────────────────────────► C-chip detected hard error
 │
 │ VINTSR<Bus Timeout> (VINTSR<7>)
 ├──────────────────────────────────────► Scalar DAL bus timeout error
 │
 │ XBER<FCMD> (XBER<3:0>)
 ├───┐ (select one)
 │   │ write
 │   ├───┐ (select one)
 │   │   │
 │   │   │ XBER<TTC> (XBER<13>)
 │   │   ├───┐ (select one)
 │   │   │   │
 │   │   │   │ XBER<CNAK> (XBER<15>)
 │   │   │   ├──────────────────────────► NXM on write
 │   │   │   │
 │   │   │   │ XBER<WDNAK> (XBER<20>)
 │   │   │   ├──────────────────────────► Data NO ACK on write
 │   │   │   │
 │   │   │   │ otherwise
 │   │   │   └──────────────────────────► No XMI grant on write
 │   │   │
 │   │   │ otherwise
 │   │   └──────────────────────────────► Inconsistent status (no XBER
 │   │                                     error bits set)
 ▼   ▼
                                                         msb-p072-89
```

Figure E-2 Cont'd. on next page

Figure E-2 (Cont.): KA64A Hard Error Interrupt Parse Tree

```
 |  |
 |  |  IDENT
 |  |___ (select one)
 |      |
 |      |  XBER<RSE> (XBER<17>)
 |      |------------------------------> XMI read sequence error on
 |      |                                return of interrupt vector
 |      |  XBER<REP> (XBER<16>)
 |      |------------------------------> XMI read error response on
 |      |                                return of interrupt vector
 |      |  XBER<TTO> (XBER<13>)
 |      |___ (select one)
 |      |   |
 |      |   |  XBER<CNAK> (XBER<15>)
 |      |   |--------------------------> No adapter ACK to IDENT
 |      |   |
 |      |   |  XBER<NRR> (XBER<18>)
 |      |   |--------------------------> XMI no read response to
 |      |   |                            IDENT
 |      |   |  otherwise
 |      |   |--------------------------> No XMI grant on IDENT
 |      |
 |      |  otherwise
 |      |------------------------------> Inconsistent status (no XBER
 |                                       error bits set)
 |   otherwise
 |   ----------------------------------> Inconsistent status (machine
 |                                       check during error interrupt)
 |  neither
 |-------------------------------------> Inconsistent status (no XBER
                                         or RCSR error bits set)
```

NOTES

(select one) - only one case must be true. If none or more than one is true, the status is inconsistent.

(select all) - more than one case may be true.

neither - fall-through case for (select all) if none of the options are true.

otherwise - fall-through case for (select one) if no other options are true.

The parse tree assumes that retry is enabled (RCSR<ARD> = 0).

msb-p073-89

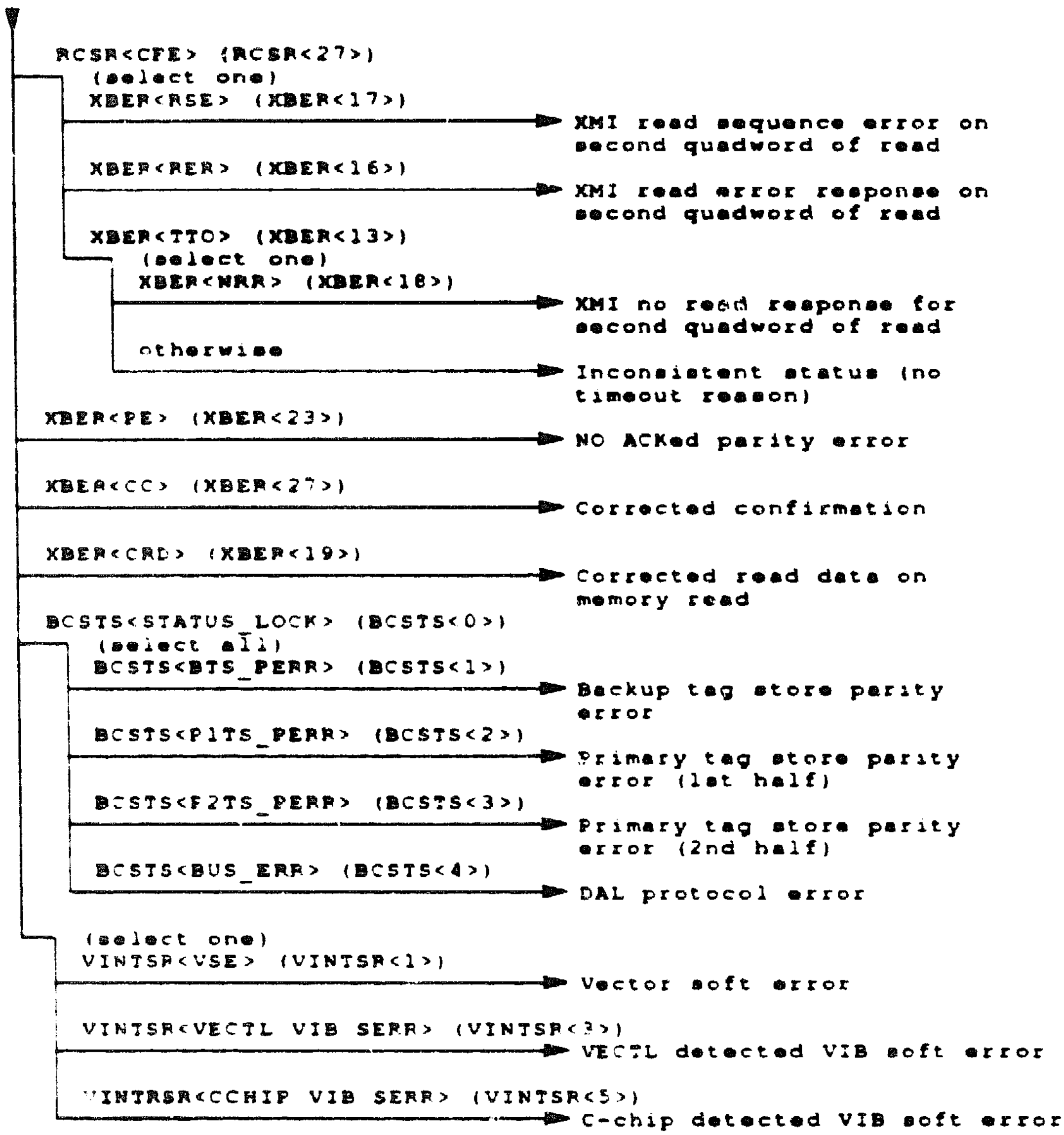
Figure E–3: KA64A Soft Error Interrupt Parse Tree

- (select all)
  - PCSTS<INTERRUPT> (PCSTS<5>) (select all)
    - PCSTS<P_TAG_PARITY_ERROR> (PCSTS<8>) → P-cache tag parity error on read, write, or invalidate
    - PCSTS<P_DATA_PARITY_ERROR> (PCSTS<10>) → P-cache data parity error on I-stream read hit
    - PCSTS<DAL_DATA_PARITY_ERROR> (PCSTS<9>) (select one)
      - PCSTS<B_CACHE_BIT> (PCSTS<12>) → Backup cache data parity error on I-stream read or nonrequested longword of D-stream read
      - otherwise → REXMI data parity error on I-stream read or nonrequested longword of D-stream read
    - PCSTS<BUS_ERROR> (PCSTS<11>) (select one)
      - SSCBTR<RWT> (SSCBTR<30>) → RSSC bus timeout on I-stream read
      - XBER<FCMD> = read (XBER<3:0>) (select one)
        - XBER<RSE> (XBER<17>) → XMI read sequence error on first quadword of I-stream read
        - XBER<RER> (XBER<16>) → XMI read error response on first quadword of I-stream read
        - XBER<TTO> (XBER<13>) (select one)
          - XBER<CNAK> (XBER<15>) → NXM on first quadword of I-stream read
          - XBER<NRR> (XBER<18>) → XMI no read response for first quadword of I-stream read
          - otherwise → No XMI grant to I-stream read
      - otherwise → Inconsistent status (no XBER error bits set)
    - otherwise → Inconsistent status (no PCSTS error bits set)

Figure E–3 Cont'd. on next page

msb-p074r-89

Figure E–3 (Cont.): KA64A Soft Error Interrupt Parse Tree



NOTES:

(select one) - exactly one case must be true. If none or more than one is true, the status is inconsistent.

(select all) - more than one case may be true.

otherwise - fall-through case for (select one) if no other options are true.

The parse tree assumes that retry is enabled (RCSR<ARD> = 0).

msb-p075r-89

Figure E–4: FV64A Machine Check Parse Tree

```
MCHK_VECTOR_STATUS
CODE = VA<8:7> (SP + 8 on stack frame)
  (select one)

  CODE = 00 (Unrecoverable VIB error)
  (select one)

    VINTSR<VECTL VIB HERR>  <4>
      ──► VECTL detected VIB hard error

    VINTSR<CCHIP VIB HERR>  <6>
      ──► C-chip detected VIB hard error

    VINTSR<Bus Timeout>  <7>
      ──► Scalar DAL bus timeout error

    VINTSR<Vector Module Reset>  <8>
      ──► Vector module is being reset

  CODE = 10, VINTSR<VHE> <2> (Unrecoverable vector hard error)

  VPSR<IMP>   <24>  (Vector hardware error)
    (select all)

    VCTL_CSR<CDH> <3>
      ──► CD bus hard error

    VCTL_CSR<ISE>  <6>
      ──► Illegal sequence error

      VCTL_CSR<VHE>  <11>  (Verse chip hard error)
        (select all)

        ALU_DIAG_CTL<ABE>  <8>
          ──► AB bus parity error

        ALU_DIAG_CTL<CPE>  <9>
          ──► C bus parity error

        ALU_DIAG_CTL<IFO>  <10>
          ──► Illegal opcode

      VCTL_CSR<LSH>  <1>  Load/Store Chip Hard Error
        (select all)

        LSX_CCSR<XHE>  <11> = 0
          ──► Hard CD bus error

        LSX_CCSR<XHE>  <11> = 1
          ──► XMI interface hard error
```

msb-p287-90

Figure E–5: FV64A Hard Error Interrupt Parse Tree

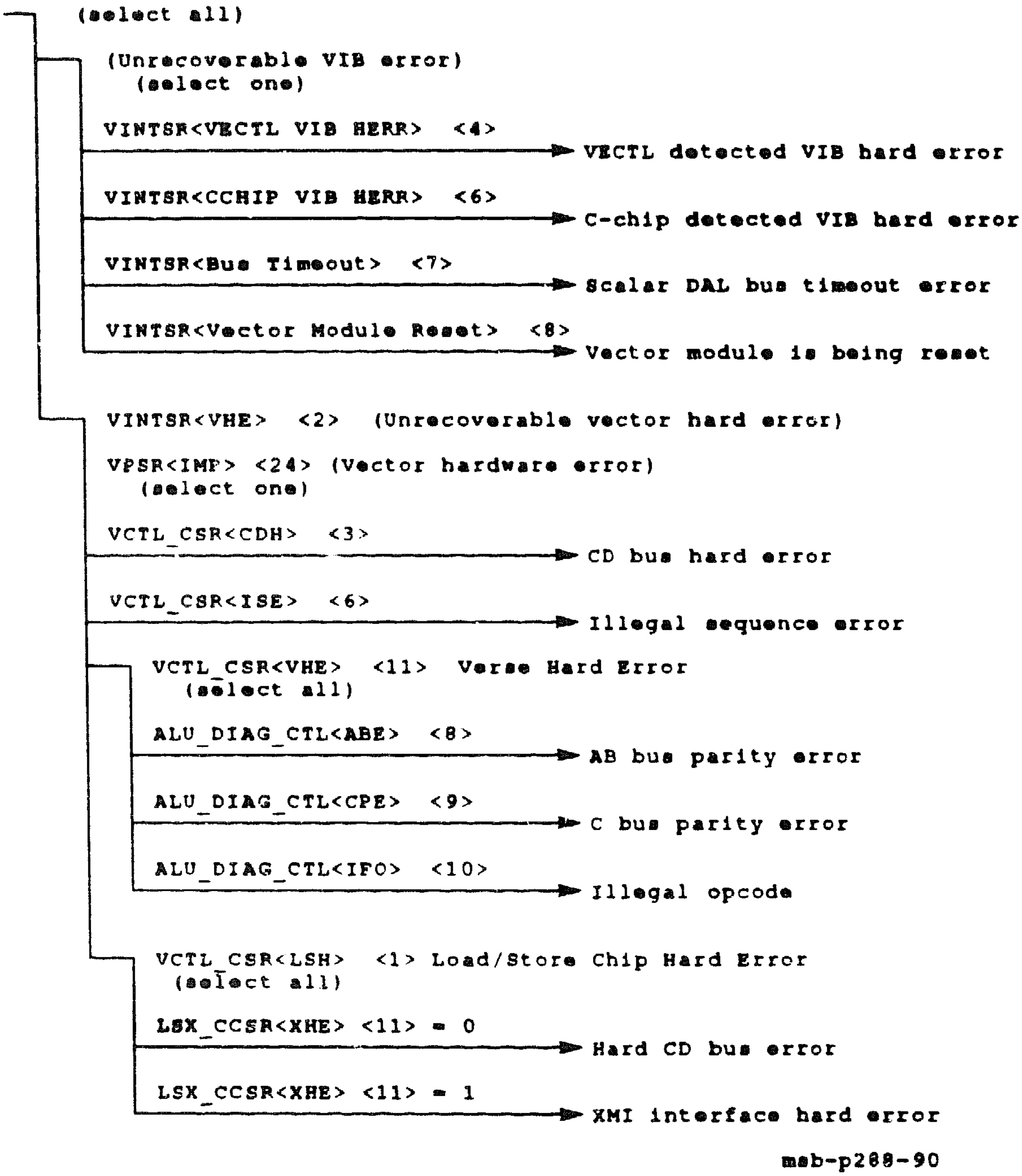


Figure E-6: FV64A Soft Error Interrupt Parse Tree

```
(select all)
  (Recoverable VIB error)
    (select one)
    VINTSR<VECTL_VIB_SERR>  <3>
    ----------------------------------> VECTL detected VIB soft error
    VINTSR<CCHIP_VIB_SERR  <5>
    ----------------------------------> C-chip detected VIB soft error

  VINTSR<Vector Soft Error>  <1>  (Recoverable vector error)
    (select one)
    VCTL_CSR<CDS>  <2>
    ----------------------------------> CD bus soft error
      VCTL_CSR<LSS> <0>  Load/Store Chip Soft Error
        (select all)
        LSX_CCSR<XSE>  <10>
        ------------------------------> XMI interface soft error
        LSX_CCSR<CPE>  <9>
        ------------------------------> Data cache parity error
  No error bits set
  --------------------------------------> Hard error interrupt
```

msb-p289-90

Figure E–7: FV64A Disable Fault Parse Tree

```
─┐ VPSR<VEN> <0> = 0, Vector disabled
 │   (select one)
 │
 │ VPSR<IVO>  <25>
 ├────────────────────────────────────────► Illegal vector opcode
 │
 ├──┐ VPSR<AEX>  <7> Vector arithmetic exception
 │  │   (select all)
 │  │
 │  │ VAER<FUN>  <0>
 │  ├─────────────────────────────────────► Floating Underflow
 │  │
 │  │ VAER<FDZ>  <1>
 │  ├─────────────────────────────────────► Floating Divide by Zero
 │  │
 │  │ VAER<FRS>  <2>
 │  ├─────────────────────────────────────► Floating Reserved Operand
 │  │
 │  │ VAER<FOV>  <3>
 │  ├─────────────────────────────────────► Floating Overflow
 │  │
 │  │ VAER<IOV>  <5>
 │  └─────────────────────────────────────► Integer Overflow
 │
 │  No error bits set
 └────────────────────────────────────────► Hard error interrupt
```

msb-p290-90

GLOSSARY

Glossary

Adapter

A node that interfaces other buses, communication lines, or peripheral devices to the VAXBI bus or the XMI bus.

Address space

The 1 Gbyte of physical address space supported by the VAXBI bus or the XMI bus.

Asymmetric multiprocessing

A multiprocessing configuration in which the processors are not equal in their ability to execute operating system code. In general, a single processor is designated as the primary, or master, processor; other processors are the slaves. The slave processors are limited to performing certain tasks, whereas the master processor can perform all system tasks. Contrast with *Symmetric multiprocessing*.

Bandwidth

The data transfer rate measured in information units transferred per unit of time (for example, Mbytes per second).

Boot device

Contains the bootblock and typically also contains the virtual memory boot program (VMB). A VAX 6000–400 system can be booted from one of four boot devices: the system TK tape drive, a local system disk connected through a KDB50, a disk connected to the system through a CI adapter (CIBCA), or a disk connected to the system through the Ethernet.

Boot primitives

Small programs stored in ROM on each processor with the console program. Boot primitives read the bootblock from boot devices. There is a boot primitive for each type of boot device.

Boot processor

The CPU module that boots the operating system and communicates with the console.

Bootblock

Block zero on the system disk; it contains the block number where the virtual memory boot (VMB) program is located on the system disk and contains a program that, with the boot primitive, reads VMB from the system load device into memory.

CIBCA

VAXBI CI port interface; connects a system to a Star Coupler.

Cold start

An attempt by the primary processor to boot a new copy of the operating system.

Console communications area (CCA)

Segment of system main memory reserved by the console program.

Console mode

A mode of operation allowing a console terminal operator to communicate with nodes on the XMI bus.

DEBNI

VAXBI adapter; Ethernet port interface.

DHB32

VAXBI adapter communication device; supports up to 16 terminals.

DMB32

VAXBI adapter interface for 8-channel asynchronous communications for terminals, one synchronous channel, and a parallel port for a line printer.

DRB32

VAXBI adapter; parallel port.

DSB32

VAXBI adapter communication device; provides two synchronous lines.

DWMBA

The XMI-to-VAXBI adapter; a 2-module adapter that allows data transfer from the XMI to the VAXBI; DWMBA/A is the module in the XMI card cage, and DWMBA/B is the VAXBI module. Every VAXBI on a VAX 6000–400 system must have a DWMBA adapter.

Interleaving memory

See Memory interleaving.

KDB50

VAXBI adapter for DSA disks; enables connection to disk drives.

Memory interleaving

Method to optimize memory access time; the VAX 6000–400 console program automatically interleaves the memories in the system unless the SET MEMORY command is used to set a specific interleave or no interleave (which would result in serial access to each memory module). Interleaving causes an even number of memories to operate in parallel.

Memory node

Also called the MS62A. Memory is a global resource equally accessible by all processors on the XMI. See also *MS62A*.

Module

A single VAXBI or XMI card that is housed in a single slot in its respective card cage. XMI modules (11.02" x 9.18") are larger than VAXBI modules (8.0" x 9.18").

MS62A

XMI memory array; a memory subsystem of the XMI. Memory is a global resource equally accessible by all processors on the XMI. Each memory module has 32 Mbytes of memory, with 1–Mbit MOS dynamic RAMs, ECC logic, and control logic.

Node

An XMI node is a single module that occupies one of the 14 logical and physical slots on the XMI bus. A VAXBI node consists of one or more VAXBI modules that form a single functional unit.

Node ID

A hexadecimal number that identifies the node location. On the XMI bus, the node ID is the same as the physical location. On the VAXBI the source of the node ID is an ID plug attached to the backplane.

Pended bus

A bus protocol in which the transfer of command/address and the transfer of data are separate operations. The XMI bus is a pended bus.

Primary processor

See *Boot processor*.

Processor node

Also called a KA64A; a single-board VAX processor that contains a central processor unit (CPU), executes instructions, and manipulates data contained in memory.

RBD

ROM-based diagnostics.

RBV20/RBV64

VAXBI adapter for write-once-read-many (WORM) optical disk drive. The RBV20 and RBV64 controllers use the KLESI-B adapter.

Secured terminal

Console terminal in program mode while the machine is processing.

Shadow set

Two disks functioning as one disk, each shadowing the information contained on the other, controlled by an HSC controller under the VMS operating system.

Symmetric multiprocessing

A multiprocessing system configuration in which all processors have equal access to operating system code residing in shared memory and can perform all, or almost all, system tasks.

System root

In a BOOT commmand, the argument to the /R5 qualifier.

TBK70

VAXBI adapter connecting the TK tape drive to the system.

TU81E

VAXBI adapter for a local (nonclustered) tape subsystem. The TU81E controller uses the KLESI-B adapter.

VAX Diagnostic Supervisor (VAX/DS)

Software that loads and runs diagnostic and utility programs.

VAXBI bus

The 32-bit bus used by the system for I/O.

VAXBI Corner

The portion of a VAXBI module that connects to the backplane and provides an electrically identical interface for every VAXBI node.

VMB

The virtual memory boot program (VMB.EXE) that boots the operating system. VMB is the primary bootstrap program and is stored on the boot device. The goal of booting is to read VMB from the boot device and load the operating system.

XBI

Lines in the self-test display that show the status of DWMBA adapters and of VAXBI nodes. See also *DWMBA*.

XMI

The 64-bit, high-speed system bus.

XMI Corner

The portion of an XMI module that connects to the backplane and provides an electrically identical interface for every XMI node.

INDEX

Index

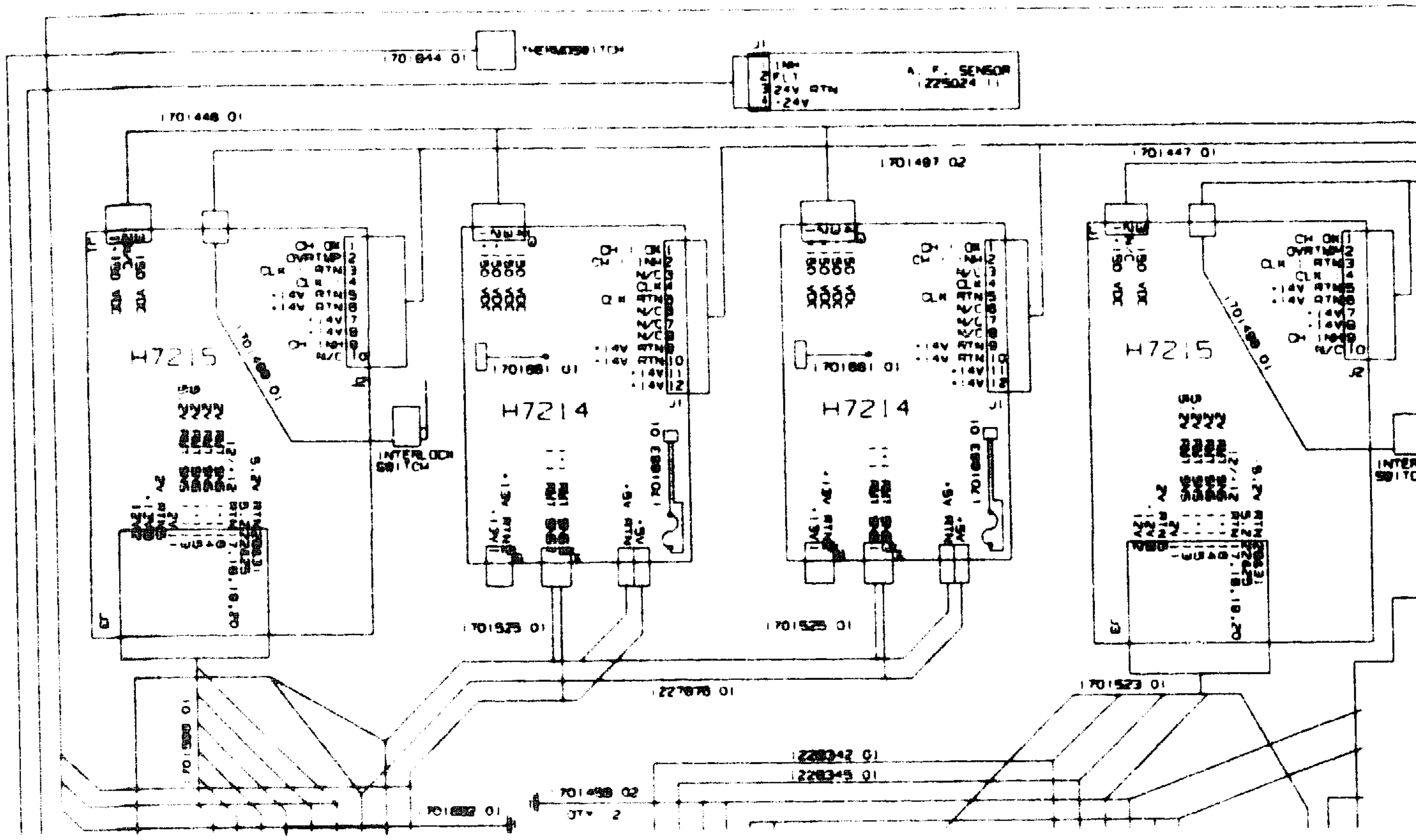
P

R

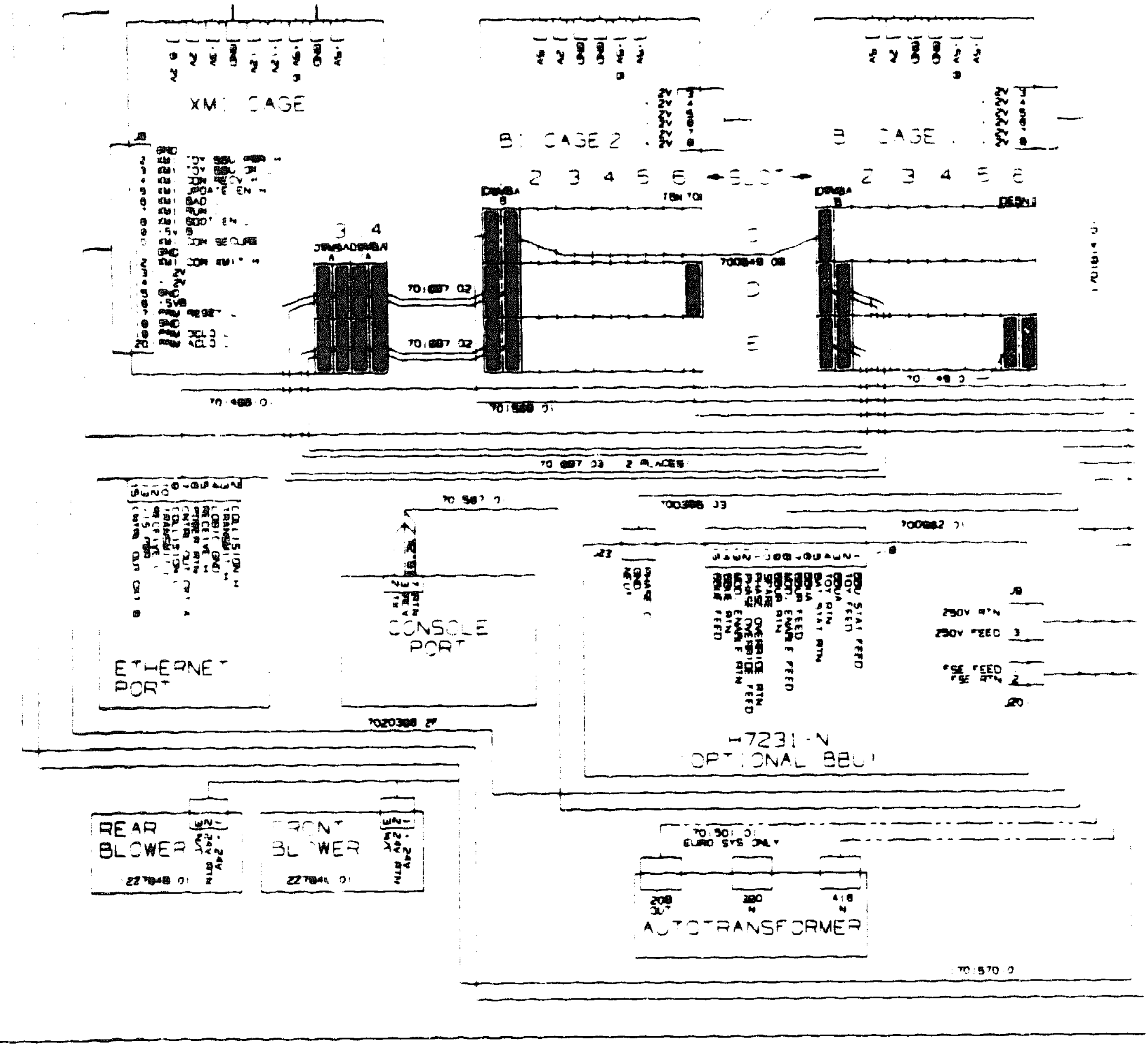
X

SYSTEM INTERCONNECT DIAGRAM

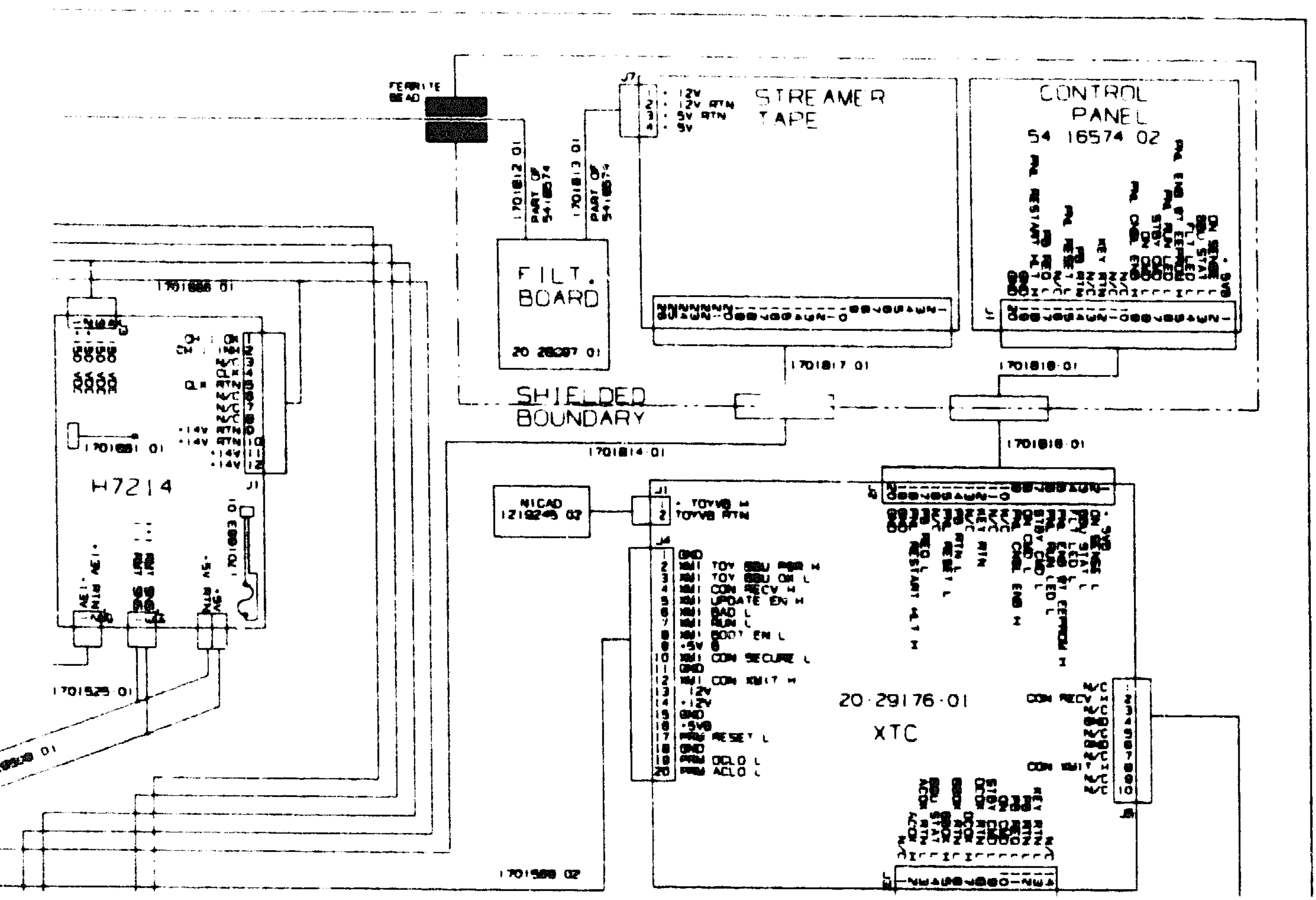
THIS PAGE
CONTINUED AND OR
ENLARGED TO
THE RIGHT



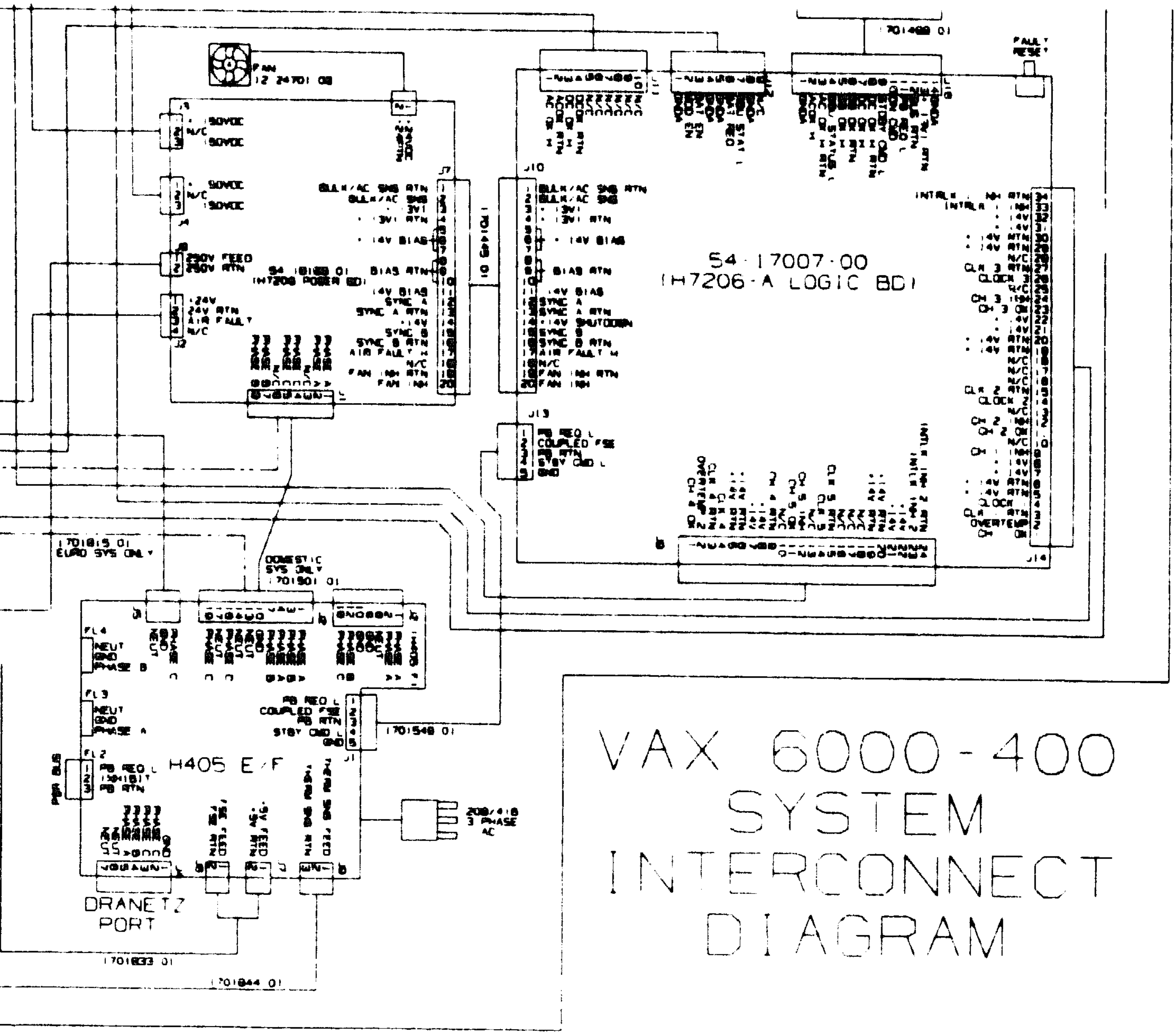
THIS PAGE
CONTINUED AND/OR
ENLARGED BELOW



THIS PAGE CONTINUED AND OR ENLARGED TO THE RIGHT



THIS PAGE CONTINUED AND/OR ENLARGED BELOW



VAX 6000-400 SYSTEM INTERCONNECT DIAGRAM

THIS PAGE CONTINUED FROM FRAME ABOVE