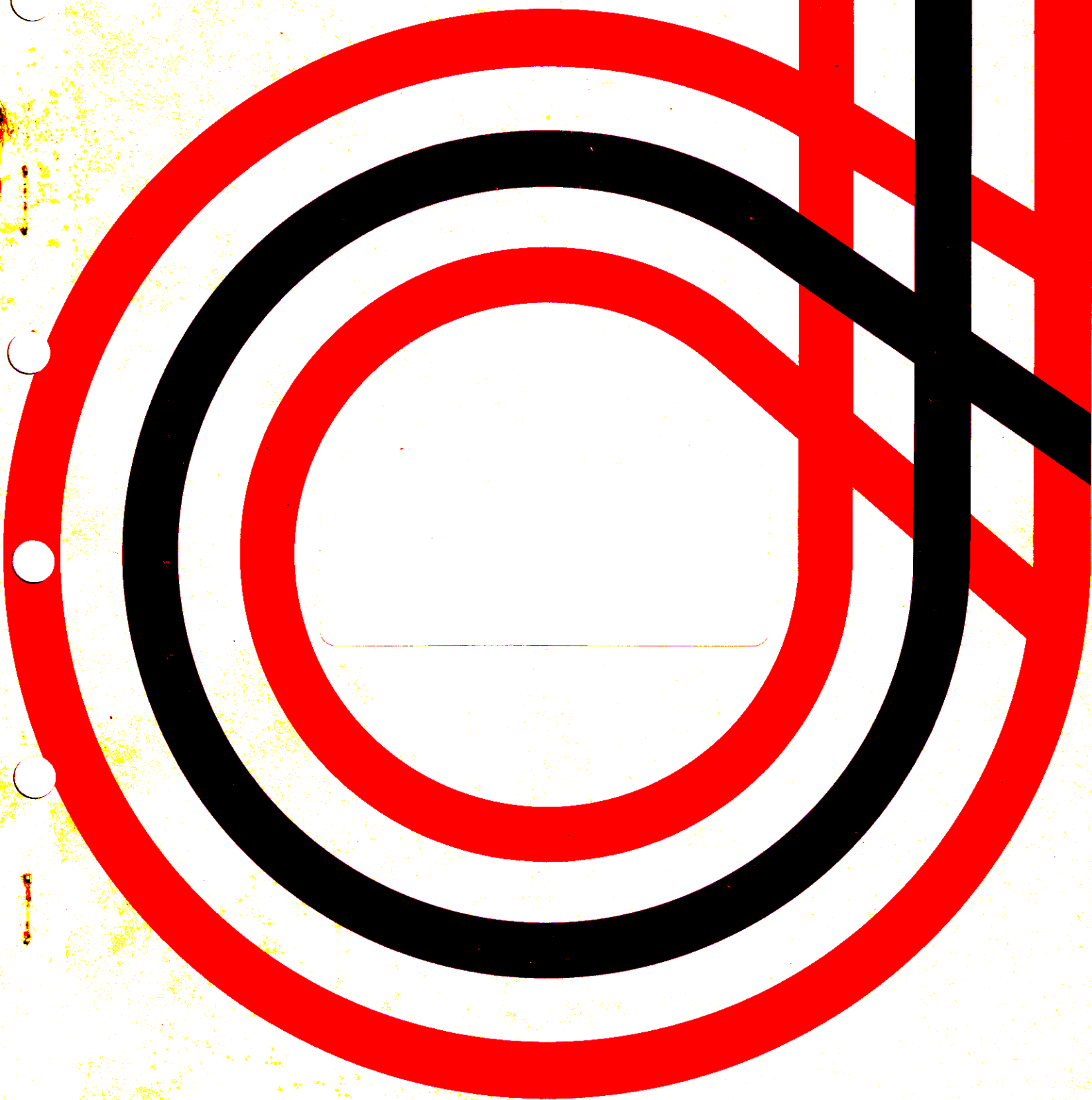


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digital

**MS11-A,B,C  
memory systems  
maintenance manual**

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# INTRODUCTION

This manual describes the MS11 options that constitute the PDP-11/45, 11/50 and 11/55 Semiconductor Memory System. Its primary purpose is to provide information for DIGITAL Field Service representatives and customer personnel, with similar PDP-11/45 training, to perform on-site maintenance of the MS11 options. The information is presented in four chapters.

Chapter 1 describes the MS11 Semiconductor Memory System structure and provides module specifications and system configuration information.

Chapter 2 describes semiconductor memory system access operations, interfacing and addressing.

Chapter 3 provides a detailed analysis of semiconductor memory logic operation.

Chapter 4 presents the procedures required for semiconductor memory calibration and maintenance.

All descriptions assume that the reader is familiar with basic digital computer theory and the operating characteristics of bipolar and metal-oxide semiconductor (MOS) digital integrated circuits. Because of the many recent advances in MOS technology concerning memory system applications, Appendix A contains a description of MOS and bipolar memory circuit theory.

Data, address, and control signals relevant to semiconductor memory operation are transmitted on the Unibus or the Central Processor Unit (CPU) Fastbus. This manual references the data, address, and control lines that interface the semiconductor memory system with other PDP-11/45 units according to the conventions established for Unibus and PDP-11/45 signals mnemonics. For example, SAPJ PA (17:06)H refers to the 12 physical-address (PA) inputs, named PA17 through PA06, which are generated as shown on drawing SAPJ. The prefix SAPJ indicates sheet J of the SAP module schematic. Complete details on data, address, and control signal origin and derivation are provided in the following related manuals:

*PDP-11/45 and PDP-11/50 System Maintenance Manual, EK-11045-MM-005*

*KB11-A Central Processor Unit Maintenance Manual, EK-KB11A-TM-001*

*KB11-D Central Processor Unit Maintenance Manual, EK-KB11D-TM-001*

*KT11-C Memory Management Option Manual, EK-KY11C-MM-003*

*KT11-CD Memory Management Option Manual, EK-KY11CD-MM-003*



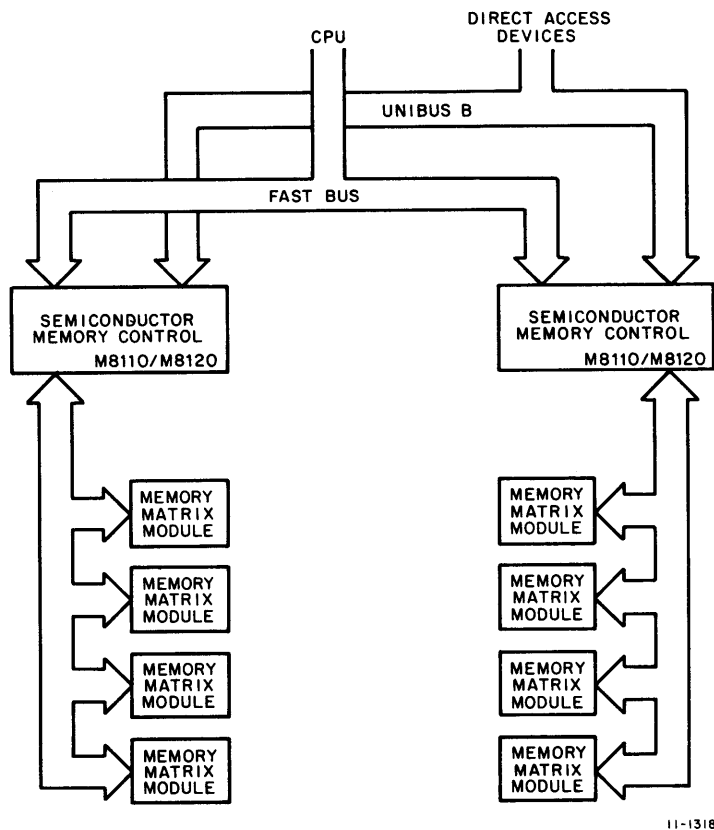


# CHAPTER 1

## SYSTEM DESCRIPTION

### 1.1 INTRODUCTION

Digital Equipment Corporation's MS11 Semiconductor Memory Systems for the PDP-11/45, 11/50 or 11/55 System are high-speed random access memories available in two basic solid-state types: bipolar (TTL) and metal-oxide semiconductor (MOS). The distinction between bipolar and MOS memory systems is made in the specific MSI components used to form the memory storage matrices. The MOS version of the MS11 uses the M8110 control module and the bipolar version of the MS11 uses an M8120 control module. The M8110 can control four 4096-word G401 MOS Memory Matrix modules (Figure 1-1). The M8120 can control either four 1024-word M8111 Bipolar Memory Matrix modules or four 4096-word M8121 Bipolar Memory Matrix modules. Both the MOS and bipolar systems provide storage for up to 16,384 16-bit words; both types of memory modules are available with or without byte parity.



11-1318

Figure 1-1 MS11 Semiconductor Memory System, Block Diagram

The bipolar and MOS semiconductor memories can be jointly or separately operated from either the KB11 Fastbus or the PDP-11 Unibus, or from both, depending on the specific system configuration. When operated from the Unibus, each semiconductor memory system functions as a PDP-11 compatible peripheral and can serve as the basic memory in a large-scale system. Operation under joint control of the Fastbus and Unibus provides direct high-speed memory access through the Fastbus for the KB11 Processor, while maintaining the processor/peripheral relationships characteristic of the Unibus. Whether operating jointly or separately with the Unibus and/or Fastbus, a semiconductor memory always assumes the role of a "slave" device to the processor. Under Unibus control, the memory also is "slave" to any peripheral (direct access) device currently designated "master".

Because readout from semiconductor memories is non-destructive, the write-after-read-cycle time associated with ferrite-core memories is eliminated. In addition, the switching speed for semiconductor memories is characteristically much faster than that for the ferrite-core memory. The extremely high switching speeds characteristic of bipolar memory cells permit typical memory cycle times of 300 ns for an operating bipolar memory system. MOS semiconductor memory systems have slower typical cycle times of 495 ns.

## **1.2 M8111 BIPOLAR MEMORY MATRIX MODULE**

The M8111 Bipolar Memory Matrix module is an 8-1/2 in. X 15 in. (21.59 cm X 38.1 cm) multilayer glass hex board, configured to store or not store byte parity. The M8111-YA parity-equipped modules contain seventy-two 256 X 1-bit TTL MSI memory circuits, interconnected to form a 1024 X 18-bit memory matrix. Each 18-bit word in this matrix is formed by two 8-bit bytes and two parity bits, one per byte. This module also contains appropriate address decoding and driving logic, 18 write-data inversion stages, and control-signal decoding logic. All decoding inversion and driving logic is formed by TTL integrated circuits. Address lines 14:13, 11:10 at each M8111 matrix module are jumper-connected so that in a given bipolar memory system each matrix module can be configured to decode a unique address. The M8111 Bipolar Memory Matrix module is identical to the M8111-YA in all respects, except that the M8111 contains sixty-four 256 X 1-bit MSI memory circuits interconnected to form a 1024 X 16-bit memory matrix without byte parity.

## **1.3 M8121 BIPOLAR MEMORY MATRIX MODULE**

The M8121-YA Bipolar Memory Matrix module is similar to the M8111 module just described. It is an 8-1/2 in. X 15 in. (21.59 cm X 38.1 cm) multilayer glass hex board, configured to store or not store byte parity. The M8121-YA parity-equipped modules contain seventy-two 1024 X 1-bit TTL MSI memory circuits interconnected to form a 4096 X 18-bit memory matrix. Each 18-bit word in this matrix is formed by two 8-bit bytes and two parity bits, one per byte. This module also contains appropriate address decoding and driving logic, 18 write-data buffering stages, and control-signal decoding logic. All decoding inversion and driving logic is formed by TTL integrated circuits. Address lines 14:13, 11:10 are decoded at this module to select the specific module and the group of 1024 words addressed within the selected module. Address bits MAD (14:13) are switch connected so that each 4096-word matrix can be selected for a unique address assignment.

Only the M8121-YA version is available; a version without byte parity is not manufactured.

## **1.4 G401 MOS MEMORY MATRIX MODULE**

The G401 MOS Memory Matrix module is an 8-1/2 in. X 15 in. (21.59 cm X 38.1 cm) double-sided, multilayer glass hex circuit board, also configured to store or not store byte parity. The G401-YA parity equipped module contains seventy-two 1024 X 1-bit MOS MSI circuits interconnected to form a 4096 X 18-bit memory. The 18-bit word configuration is exactly the same as the bipolar matrix, i.e., two 8-bit bytes and two parity bits, one per byte. This module also contains appropriate logic to level-shift addresses, data, and control signals from TTL to MOS and MOS to TTL voltage levels; and 16 or 18 integrated-circuit sense amplifiers, depending on whether parity is specified, one for each of the read-sense lines. The states of memory address (MAD) register bits (02:01) and (14:13) are decoded at this module to select the specific module and the group of 1024 words addressed within the selected module. Address bits MAD (14:13) are jumper-connected so that each 4096-word matrix can be selected and wired for a unique address assignment. The G401 MOS Memory Matrix module is identical in all respects to the G401-YA,

except that the G401 contains sixty-four  $1024 \times 1$ -bit MSI memory circuits interconnected to form a  $4096 \times 16$ -bit memory matrix without byte parity.

Operation of the MOS memory matrix is substantially different from the bipolar matrix in two respects. First, because of the nature of the dynamic MOS storage cell (Appendix A), each memory access must include a time interval for precharging the addressed cells prior to the actual access. Second, all memory locations in a MOS system must be periodically refreshed, usually every 1 ms, to assure data validity during any extended standby intervals.

### 1.5 M8110 AND M8120 SEMICONDUCTOR MEMORY CONTROL MODULES

The M8110 and M8120 Semiconductor Memory Control modules are fully integrated two-part memory controllers. The M8110 control is capable of controlling four G401 MOS Memory Matrix modules; the M8120 can control either four M8111 or four M8121 Bipolar Memory Matrix modules. (The controls are similar in most respects and will be described together in the following paragraphs. They will be referred to as the M8110/M8120 memory controls.)

The M8110/M8120 controls multiplex memory access addresses and associated data between the Fastbus and a Unibus, and direct the logic and timing sequences necessary for the storage or retrieval of each data word or byte associated with a given access cycle. A simplified block diagram of the M8110/M8120 is shown in Figure 1-2.

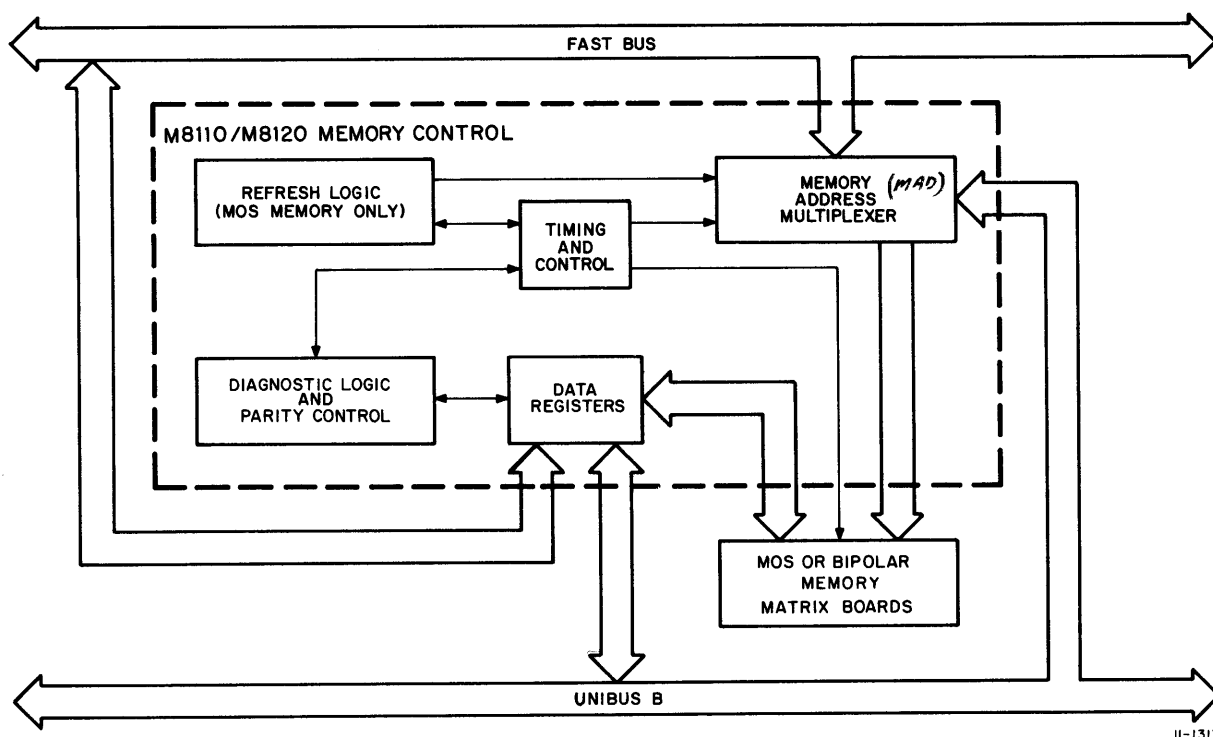


Figure 1-2 MS11 Semiconductor Memory Control Module, Block Diagram

#### 1.5.1 Memory Address Multiplexing

The memory address multiplexing function involves two sequential actions under direct control of the M8110/M8120 timing and control logic. First, based on priority, arbitration of memory access requests performed by the timing and control logic, Fastbus, Unibus, or refresh addresses (for M8110 MOS memory systems only) are multiplexed into the memory address (MAD) register. Second, through a parallel bit-to-bit connection scheme, Fastbus or Unibus addresses are mapped into the MAD register. Once mapped into the MAD register, an address is strobed into the associated bipolar or MOS memory matrix module selected by that address through action of the M8110/M8120 timing and control function.

### 1.5.2 Write and Read Data Registers

The M8110/M8120 contains two data registers: the write-data (Data In) Register, and the read-data (Data Out) Register. The Data In Register multiplexes a 16-bit data word (or two 8-bit data bytes), from either the Fastbus or Unibus, and stores that data until strobed into the associated bipolar or MOS memory matrix module by the M8110/M8120. The 18-bit Data In Register stores parity for the lower and upper data bytes in the most significant Data In Register stages. These parity bits are generated as part of word or byte storage in the Data In Register. Data from the Unibus is received at the M8110/M8120 Unibus interface for storage in the Data In Register. Fastbus data to be written is received directly at the Data In Register because of the proximity of the M8110/M8120 to the KB11 Processor. At the appropriate time, the data accompanying a Data In cycle is strobed into the memory location designated by the associated address.

The M8110/M8120 Data Out Register receives and stores data from the location addressed in the memory matrix as a direct result of a Unibus or Fastbus DATI cycle. At the end of a DATI cycle, data is strobed jointly onto the M8110/M8120 Unibus interface, and to the Fastbus for retrieval by the requesting bus. Fastbus data lines are unidirectional; Unibus data lines are bidirectional.

### 1.5.3 Timing and Control

The M8110/M8120 timing and control interprets control signals from the Fastbus or Unibus and derives the internal multiplexing priorities, timing, and the nature of the operation to be subsequently performed (DATO or DATI). In addition, specific portions of the address contained in the MAD register are decoded by the selection logic to identify the physical memory selected, the memory section to be addressed (one out of four 1024-word sections or one out of four 4096-word sections), the required byte configuration, and to determine if data words are to be interleaved. If the operation to be performed is a DATO, the timing and control logic develops the strobe levels necessary to load multiplex addresses and data, according to the priority of the request, into pertinent registers. The timing and control logic also enables the designated memory section for writing and performs the DATO operation.

Because readout from semiconductor memories is non-destructive, the timing and control logic strobes the addressed data onto the output lines which connect to both buses. In this case, the bus that initiated the read operation receives the data at the bus input as the data requested.

### 1.5.4 Refresh Logic

The nature of the dynamic MOS MSI circuits forming the G401 MOS Memory Matrix module requires that each storage cell, which is the circuit equivalent of a capacitive node, be periodically charged above the threshold of the data stored. Refreshing the data contained in each integrated-circuit memory requires that all states of the row address for that circuit be cycled each 1 ms. The M8110 refresh logic performs this function automatically by generating 32 sequential row addresses during each 1 ms period. These sequential addresses are then input to the address multiplexer. Coincident control levels from the refresh logic serve to enable the address priority portion of the timing and control logic to permit input of refresh addresses at the assigned priority level.

Each DATO or DATI operation (with the exception of the write portion of a write-after-read operation) also includes the precharging or refreshing of each address written into or read. When the M8110 is used with bipolar memory matrix modules, this refresh logic is inhibited and the precharge interval is ignored. The M8120 also contains refresh logic. It is always inhibited because the M8120 is used only to control bipolar modules.

### 1.5.5 Parity Control

Data to be written is transferred to the M8110/M8120 over 16 data lines. If the operation is a DATO cycle, parity is generated and stored in bit 16 for the low-order byte and in bit 17 for the high order byte. If the operation is a DATOB, parity is generated only for the byte written and stored in the corresponding parity.

During Fastbus DATI operations, parity is checked after each 16 bits of data read are transferred to the M8110/M8120 Data Out Register. If a parity error is detected, the Fastbus is notified. (Parity error checking is inhibited on Unibus DATI cycles.)

### 1.5.6 Diagnostic Logic

M8110/M8120 memory control diagnostic logic allows you to write data from the Unibus with parity selected as odd or even at any memory address, and to check the parity of data read from memory. Normal parity is even; odd parity generates a read parity error as a reliability check of the diagnostic logic. Each M8110/M8120 module contains a three flip-flop parity register that controls the parity function within that memory control module. A unique address, determined by the first memory address under the control of the M8110/M8120, is assigned as the parity register address and is decoded within the diagnostic logic; each M8110/M8120 has an addressable parity register that can be read or written to. These operations are conducted when a Unibus DATI or DATO is addressed to the parity register. Parity error indication, when enabled, is transmitted directly to the processor via the Fastbus.

### 1.6 SYSTEM SPECIFICATIONS

Characteristics	M8110/M8120 Semiconductor Memory Control Module	M8111 Bipolar Memory 1K Matrix Module	M8121-YA Bipolar Memory 4K Matrix Module	G401 MOS Memory 4K Matrix Module
Storage capacity	N/A	1024 18-bit words	4096 18-bit words	4096 18-bit words
Access time:				
DATO cycle	N/A	N/A	N/A	N/A
DATI cycle	N/A	200 ns (max) 190 ns (typical)	200 ns (max) 190 ns (typical)	410 ns (max) 395 ns (typical)
Cycle time:	N/A	330 ns (max) 300 ns (typical)	330 ns (max) 300 ns (typical)	510 ns (max) 495 ns (typical)
Operating voltages:				
VCC	+5 V, -15 V	+5 V	+5 V	±5 V
VBB				+23.7 V
VDD				+0.7 V
VSS				+19.7 V
Over-voltage regulation	±5%	±5%	±5%	±5%
Maximum dc power consumption: <sup>1</sup>				
Active	19.65 W	55 W	60 W	39.35 W
Inactive	19.65 W	55 W	60 W	16.01 W
Maximum ac power consumption: <sup>2</sup>	MS11-CC: 30 W, 130 Btu	110 W, 376 Btu/hr	MS11-AP: 120 W, 410 Btu	MS11-BM, BT 80 W, 273 Btu/hr
Environmental conditions:				
Temperature	50° to 104°F (10° to 40°C)	50° to 104°F (10° to 40°C)	50° to 104°F (10° to 40°C)	50° to 104°F (10° to 40°C)
Humidity	10% to 90%	10% to 90%	10% to 90%	10% to 90%
Mechanical parameters:				
Height	15 in. (38.1 cm)	15 in. (38.1 cm)	15 in. (38.1 cm)	15 in. (38.1 cm)
Width	8.5 in. (21.59 cm)	8.5 in. (21.59 cm)	8.5 in. (21.59 cm)	8.5 in. (21.59 cm)
Depth	1/2 in. (1.27 cm)	1/2 in. (1.27 cm)	1/2 in. (1.27 cm)	1/2 in. (1.27 cm)
Construction	Fiberglass/ multilayer	Fiberglass/ multilayer	Fiberglass/ multilayer	Fiberglass/ multilayer
Cooling	CPU (internal) fan	CPU (internal) fan	CPU (internal) fan	CPU (internal) fan
Mounting	Dedicated plug-in slot in CPU	Dedicated plug-in slot in CPU	Dedicated plug-in slot in CPU	Dedicated plug-in slot in CPU

<sup>1</sup>Maximum power per module of each type.

<sup>2</sup>Includes regulator efficiency and total power consumed with this option.

## 1.7 SEMICONDUCTOR MEMORY SYSTEM CONFIGURATIONS

Tables 1-1, 1-2, and 1-3 list the number of options that are required as a result of a selected memory type (MOS or Bipolar) and size. The module complement that comprises the corresponding option is also shown. If, for example, a 24K capacity bipolar memory is desired, the required configuration will consist of two MS11-CC options (each consisting of one M8120 module and two H744 modules) and six MS11-AP options (M8121-YA modules). The second M8120 control (MS11-CC option) is necessary for the 8K of memory in excess of 16K controlled by the first M8120.

**Table 1-1**  
**M8121 (4K) Bipolar Memory System Configuration**

Installed Memory Capacity (with Parity)	Option Type Number	
	MS11-CC	MS11-AP
	Module Complement	
	(1) M8120 (2) H744	(1) M8121-YA
4K	1	1
8K	1	2
12K	1	3
16K	1	4
20K	2	5
24K	2	6
28K	2	7
32K	2	8

**Table 1-2**  
**M8111 (1K) Bipolar Memory System Configuration**

Installed Memory Capacity		Option Type Number		
		MS11-CC	MS11-CM	MS11-CP
		Module Complement		
With Parity	Without Parity	(1)M8120* (2)H744A	(1)M8111	(1)M8111-YA
1K		1		1
	1K	1	1	
2K		1		2
	2K	1	2	
3K		1		3
	3K	1	3	
4K		1		4
	4K	1	4	
5K		2		5
	5K	2	5	
6K		2		6
	6K	2	6	
7K		2		7
	7K	2	7	
8K		2		8
	8K	2	8	

\*Early revisions use the M8110. 4K bipolar modules (Table 1-1) must use the M8120.

**Table 1-3**  
**G401(4K) MOS Memory System Configuration**

Installed Memory Capacity		Option Type Number			
		MS11-BC	MS11-BD	MS11-BR, BM*	MS11-BT, BP*
		Module Complement			
With Parity	Without Parity	(1)M8110 (1)H746A (1)H744A	(1)M8110 (1)H746A	(1)G401	(1)G401-YA
4K		1			1
	4K	1		1	
8K		1			2
	8K	1		2	
12K		1			3
	12K	1		3	
16K		1			4
	16K	1		4	
20K		1	1		5
	20K	1	1	5	
24K		1	1		6
	24K	1	1	6	
28K		1	1		7
	28K	1	1	7	
32K		1	1		8
	32K	1	1	8	

\*High performance versions of the BR and BT options (available on special order).





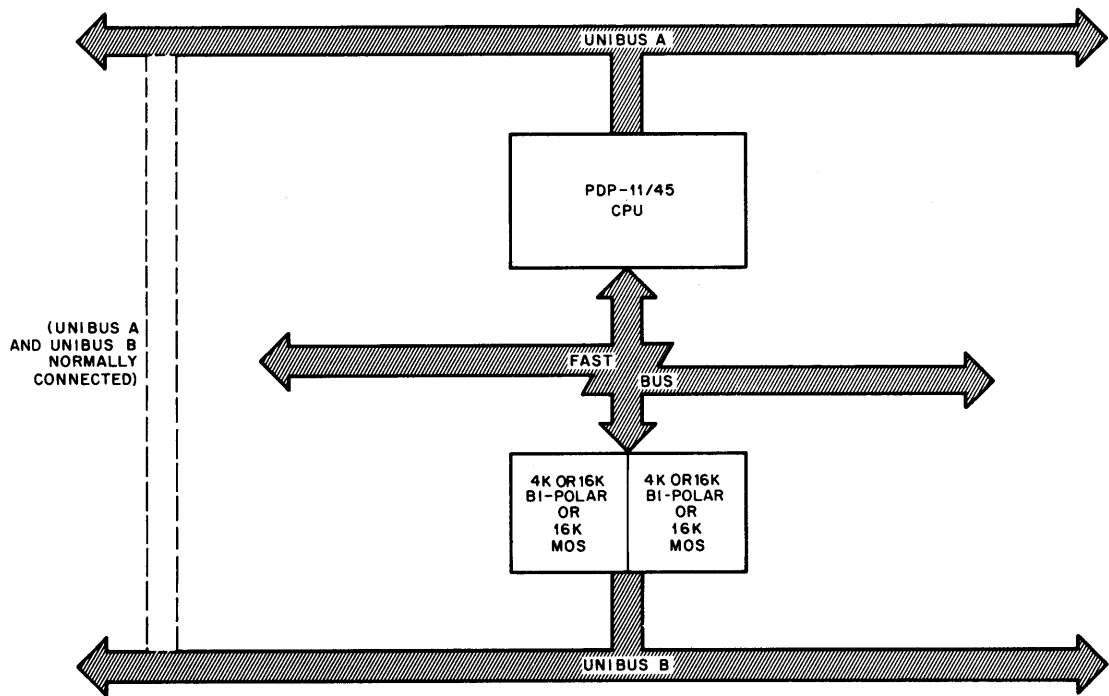
# CHAPTER 2

## MEMORY SYSTEM

### INTERFACE OPERATIONS

#### 2.1 INTRODUCTION

A PDP-11/45 System can be equipped with one or two M8110 or M8120 Semiconductor Memory Control modules. Each M8110/M8120 module, in turn, can exercise control of up to four M8111 or M8121 Bipolar Memory Matrix modules, or up to four G401 MOS Memory Matrix modules. Since the memory capacity of these three matrix module types is different (the M8111 provides 1K and the G401 and M8121 provide 4K of memory) the total memory capacity available to the user is determined by the selected configuration. A typical two-M8110 module arrangement can consist of up to 8K of bipolar memory in 1K increments (32K in 4K increments) or up to 32K of MOS memory in 4K increments. The two-controller configuration might also have one of the controllers directing bipolar matrices while the other is connected to MOS matrices. However, memory matrices of different types cannot be connected to the same M8110 control. As indicated in Tables 1-1/1-2, and 1-3 the memory capacity determines the number of M8110/M8120 modules required (the maximum configuration is 16K of MOS or Bipolar memory per module). Figure 2-1 illustrates the memory system, bus, and processor relationship. Within a PDP-11/45 computer system, the CPU communicates with associated semiconductor memory controls through an extremely high-speed information path which is internal to the CPU and under control of the CPU Fastbus. One Unibus in the system, normally Unibus A, also communicates with the two M8110/M8120 controls.



11-0833

Figure 2-1 Semiconductor Memory Configuration within PDP-11/45 Systems

Each M8110/8120 control, in turn, communicates with up to four bipolar or four MOS memory matrix modules. Therefore, an operating M8110/M8120 Semiconductor Memory Control has three active interfaces: the Fastbus interface, the Unibus interface, and the memory bus. The relationship of a typical PDP-11/45 Semiconductor Memory System to these interfaces is shown in Figure 2-2. Because the M8110/M8120 control and associated memory matrix modules are physically located in the PDP-11/45 processor, connection to the Fastbus is by direct-wiring the control and matrix module connectors to the PDP-11/45 CPU backplane. However, the potentially remote location of a second Unibus, with respect to the M8110/M8120 control, requires a defined Unibus interface on the control to drive and receive information and control signals to and from that Unibus. Like the Fastbus connection, memory bus connection between an M8110/M8120 control and associated M8111 or M8121 bipolar or G401 MOS memory modules involves physically adjacent connectors, so that control-matrix module information and signals are direct-wire connected.

Discussion of semiconductor memory system interfaces will involve a description of memory access operation, a definition of each interface in terms of information and signals exchanged, and an explanation of the conventions used to address semiconductor memories.

## **2.2 BASIC MEMORY ACCESS OPERATIONS**

MS11 Semiconductor Memory Systems operate in four accessing modes: read, write, optional byte handling, and pause for a write following a read. These operations are designated as follows:

- a. Read data (DATI)
- b. Read data and pause (DATIP)
- c. Write data (DATO)
- d. Write data bytes (DATOB)

Each of these modes is briefly discussed in the following paragraphs.

### **2.2.1 Data In (DATI) Cycle**

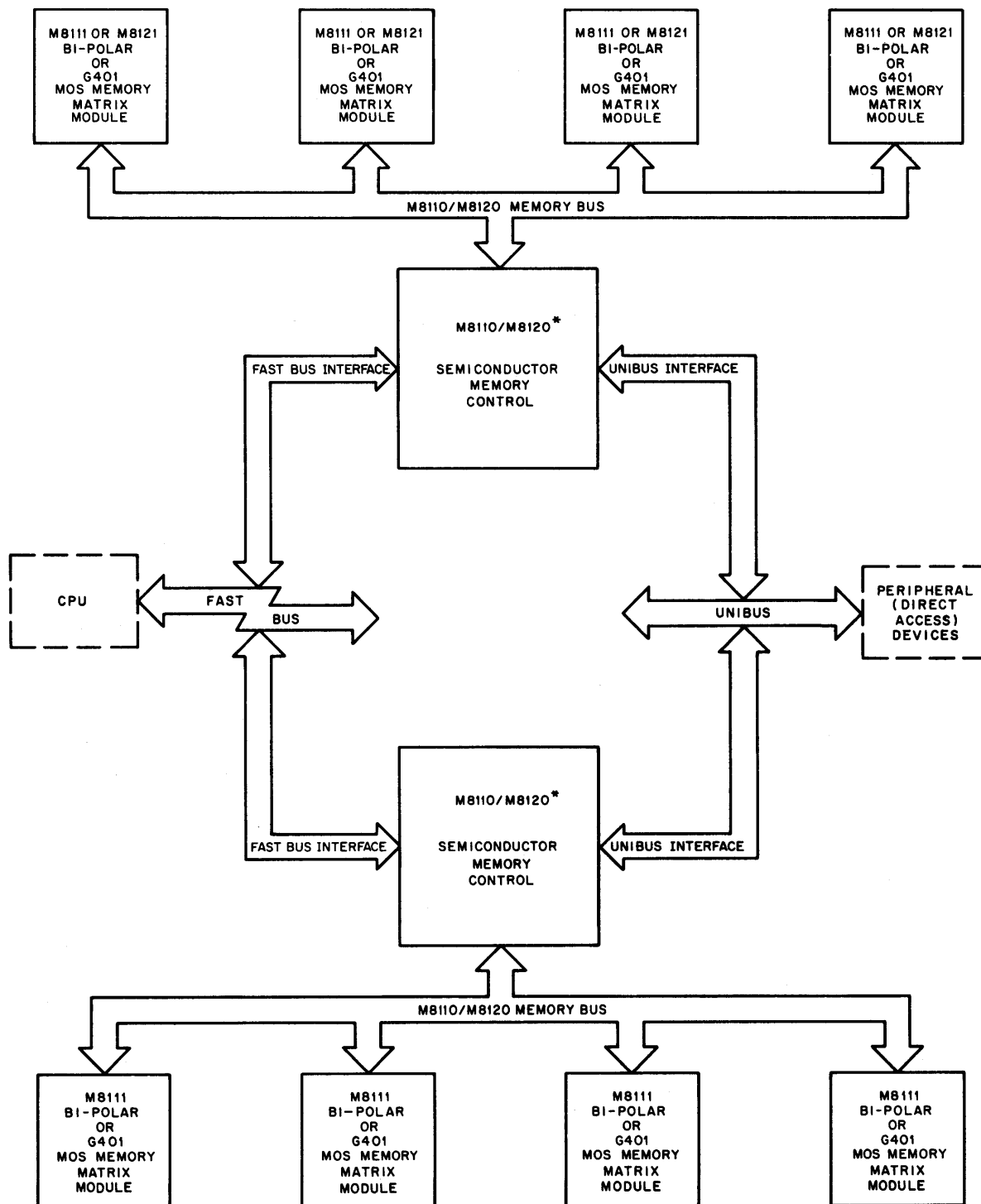
During a DATI cycle, data in the locations addressed at the memory matrix module is loaded into the M8110/M8120 output data latch for retrieval by the initiating bus (Unibus or Fastbus). Readout of semiconductor memories is non-destructive; thus, the restore portion of the conventional core memory read cycle is not required.

### **2.2.2 Data In, Pause (DATIP) Cycle**

The purpose of this reading mode is to hold memory secure after data is read from a set of memory addresses until that data can be revised and then written again. PDP-11 convention requires that execution of a DATIP be followed always by the execution of a DATO or DATOB operation, except when parity error is sensed in DATIP. A DATIP is a duplicate of a DATI operation except for a pause for initiation of the impending DATO or DATOB.

### **2.2.3 Data Out (DATO) Operation**

A DATO, or write operation, causes data outgoing from the Unibus or Fastbus to be written one word at a time (16 bits) at the address order designated. The nature of semiconductor memories is such that locations to be written in do not require prior clearing. As a consequence, the writing of data begins immediately after cycle initiation, with no prior clearing required.



\* A SINGLE M8110/M8120 CAN DIRECT EITHER FOUR G401 MODULES, FOUR M8121 MODULES OR FOUR M8111 MODULES BUT NOT A MIXTURE OF THE THREE MODULE TYPES.

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Figure 2-2 Semiconductor Memory System Interfaces

### 2.2.4 Data Out, Byte (DATOB) Cycle

A DATOB cycle is a duplicate of a DATO cycle, except that data is written as 8-bit bytes rather than as a 16-bit word. Decoding of each address designates whether the corresponding byte transferred from the Unibus or Fastbus is to be written as a low- or high-order byte in the 16 bits available at each memory location. Therefore, data to be written in memory as bytes must be received on the data lines corresponding to the byte position designated by the address.

## 2.3 FASTBUS INTERFACE

The Fastbus interface provides a high-speed, full-duplexed, dedicated data path between the processor and the M8110/M8120 Semiconductor Memory Control. The Fastbus address, data, and control lines are defined in Table 2-1.

**Table 2-1**  
**Fastbus-M8110/M8120 Interface and Control Signals**

Name	Mnemonic	Source Drawing	Destination Drawing	Function
Address	DAPB BAMX (05:00) H SAPJ PA (17:06) H	DAPB SAPJ	SMCC, SMCF	Selects memory location
Data In	SMCE MEM D (15:00) H	SMCE	PDRA	DATI lines from Fastbus
Data Out	PDRB BR (15:00) B L	PDRB	SMCD	DATO lines to Fastbus
Bus Start	TMCE BUST OUT L	TMCE	SMCA	Starts Fastbus-initiated memory access cycle
Memory Selected	SMCF MEM L	SMCF	TMCF	Informs Fastbus that address is in semiconductor memory
Control OK	UBCA CONTROL OK H	UBCA	SMCA	Informs control that current access cycle can be completed
Memory Sync	SMCA MEM SYNC (B) L	SMCA	TIGA	Informs Fastbus that current memory access cycle is being completed
Control	UBCC MEM BUS C0 L	UBCC	SMCA	Specifies type of memory access cycle (Table 2-2)
Control	UBCC MEM BUS C1 L	UBCC	SMCA	Specifies type of memory access cycle (Table 2-2)
Bus End Clear	TMCE BEND CLR L	TMCE	SMCA	Terminates current memory access cycle at M8110 control if Fastbus anticipated address is incorrect
Parity Error Flag	SMCB PERF L	SCMB	UBCB	Sets processor parity error flag
Parity Error Acknowledge	UBCD PERF ACKN H	UBCD	SMCB	Acknowledgment by processor of receipt of parity error indication

### 2.3.1 Fastbus DATO Cycle

Initiation of a semiconductor memory access cycle via the Fastbus occurs when the processor places the desired memory address on the address lines (Figure 2-3, numbers indicate order of occurrence). Data to be stored at this address is present on the DATO lines at the same time. The address bits are decoded in the memory selection logic and the resultant MEM signal to the processor denotes receipt of a valid address. Although the address is transmitted to both M8110/M8120 controls, only that controller having this address within its assigned range of addresses will acknowledge with the MEM signal. The response (internal to the processor) to MEM is TMCF FAST L, which

**Table 2-2**  
**Fastbus and Unibus Control Bit States**

Input from Fastbus		Input from Unibus		Access Cycle to be Performed
UBCC MEM BUS C1 L	UBCC MEM BUS C0 L	BUSB C1 L	BUSB C0 L	
Usable Signal		Usable Signal		
SMCA MEM C1L	SMCA MEM C0L	SMCH UBC1, H, L	SMCH UBC0, H, L	
0	0	0	0	DATI
0	1	0	1	DATIP
1	0	1	0	DATO
1	1	1	1	DATOB

results in the CPU inhibiting MSYN and clearing BUSY; Unibus memory addressing is inhibited. TMCE BUST OUT L, also from the processor, asserts PREQ (1) H. This latter signal, together with MEM H, initiates memory timing. The memory address is now latched into the MAD register and a usable address is presented to the memory module. Required timing signals are also furnished to the memory logic. MEM BUS C0 and C1, received prior to CONTROL OK, are now decoded to indicate a DATO operation. Table 2-2 lists the four access cycle types that are decoded from these two control bits. With the subsequent CONTROL OK signal, the processor verifies the current memory access cycle. Since this is a request from the processor (PREQ), SMCA D, or in early versions ACCESS READY LATCH H, (a product of the timing operation), together with CONTROL OK, generates MEM SYNC. This latter signal performs several functions; it is returned to Fastbus to inform the processor that data is to be stored, and with MEM C1, develops DATA LATCH. The final steps are accomplished with DATA LATCH; the data to be written (Data Out) is latched into the Data In Register, placed on the bus to the memory module and then stored at the specified location with the concurrent WRITE PULSE.

#### NOTE

The KB11 Processor, during execution of a current instruction, attempts to predict the address of the word needed next for purposes of increased operating efficiency. After each instruction fetch, the processor initiates another bus cycle to fetch the word following the current instruction cycle. If the instruction currently being executed requires data, not from the next word but from a different address, then the processor terminates that bus cycle aimed at retrieving the next word. This terminating process results in the processor issuing TMCE BEND CLR L to the semiconductor memory control. At the control that previously acknowledged the address associated with the discontinued bus cycle by responding with SMCF MEM L, TMCE BEND CLR L terminates the memory access cycle initiated by TMCE BUST OUT L.

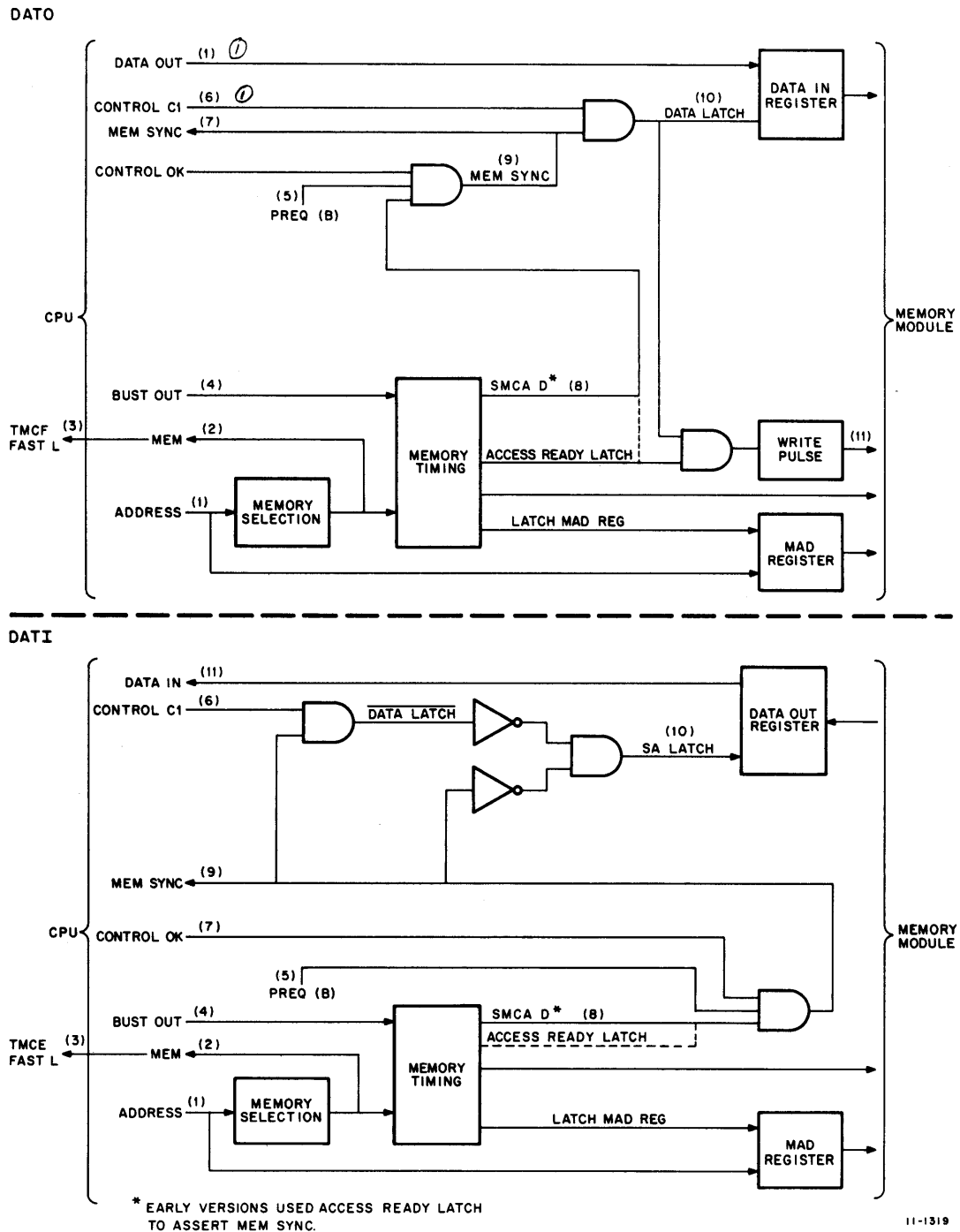


Figure 2-3 Fastbus Interface

### 2.3.2 Fastbus DATI Cycle

If the Fastbus-initiated access cycle is a DATI or DATIP (Figure 2-3), the sequence is essentially the same as when DATO was executed. When the memory address from the Fastbus is decoded, MEM is returned to the processor. The BUST OUT signal from the processor that follows asserts PREQ (1) H. This latter signal, together with MEM H, initiates memory timing, the memory address is placed on the lines to the memory module. After CONTROL OK is received, the timing sequence continues without further processor interruption. SMCA D, or in early versions ACCESS READY LATCH, a product of the timing process, generates the MEM SYNC signal. Unlike the DATO operation, MEM BUS C1 (Table 2-2) is a 0 for DATI and DATA LATCH is inhibited. However, due to the signal levels used, SA LATCH is set at the termination of the MEM SYNC pulse. The data from the desired address in the memory matrix is then transmitted as DATA IN, from the Data Out Register via Fastbus to the processor.

Although the M8110/M8120 parity diagnostic register is addressed and loaded through the Unibus interface, the parity error indicator signal PERF is relayed to the processor through the Fastbus. The processor looks for PERF at the time it drops CONTROL OK; if set, it responds with PERF ACK.

## 2.4 UNIBUS INTERFACE

Data transfers through the Unibus between the semiconductor memory system and the processor (or other devices) are conducted on a master/slave basis with the memory in all circumstances having slave status (refer to the *PDP-11 Peripherals Handbook*). Unlike the Fastbus interface, data lines between the Unibus and the M8110/M8120 control are bidirectional. The information and control signals passed between the Unibus and the M8110/M8120 Semiconductor Memory Control module are defined in Table 2-3.

**Table 2-3**  
**Unibus/M8110 Interface Information and Control Signals**

Name	Mnemonic	Source	Destination	Function
Address	BUSB A <17:00> L	BUSB	SMCH	Selects memory location
Data	BUSB D <15:00> L	BUSB	SMCH	Provides for bidirectional data transfer between Unibus and semiconductor memory
Master SYNC	BUSB MSYNC L	BUSB	SMCH	Initiates memory access cycle specified by state of UBCC C0 and C1
Slave SYNC	BUSB SSYNC L	SMCF	BUSB	Acknowledges connection
Control	BUSB C0 L	BUSB	SMCH	Specifies type of memory access cycle (Table 2-2)
Control	BUSB C1 L	BUSB	SMCH	Specifies type of memory access cycle (Table 2-2)
DC power low (Bus A)	BUSA DCLO L	BUSA power control modules	SMCH	Indicates dc voltage out of tolerance on bus A
DC power low (Bus B)	BUSB DCLO L	BUSB power control modules	SMCH	Indicates dc voltage out of tolerance on bus B

At the M8110/M8120, all information and control-signal interchange with the Unibus is routed through the SMCH logic on the M8110/M8120 control. This logic consists of a drive/receiver interface designed for high-speed information and control-signal transmission and receipt from remote locations over the Unibus cable module.



### 2.4.1 Unibus DATO Cycle

A memory access cycle is initiated (Figure 2-4) from the Unibus when the processor or direct access device places the memory address on the input lines to both M8110/M8120 controls. Only that control where the address falls within the established address range will have its memory selection logic activated. Control bits C0 and C1 are also present at the control input at this time; they are decoded (Table 2-2) to determine the type of memory access cycle to be executed. The data to be stored is concurrently available on the DATA lines. Enabling of the address decoding circuitry occurs with the arrival of MSYNC from the Unibus. The subsequent BREQ initiates the memory timing sequence. One of the first signals generated, BREQ IN PROG, provides a required condition for DATA LATCH. Latching of the memory address into the MAD Register occurs next; the memory matrix module is thereby presented with a usable storage address prior to the data being strobed over the memory bus. Following a delay, ACCESS READY LATCH simultaneously produces DATA LATCH and MEM SSYNC. The latter signal is returned, via the Unibus, as BUSB SSYNC, informing the processor that the selected control has accepted and stored the data. DATA LATCH results in the DATA being gated into the Data In Register and then placed on the bus to the memory matrix. Concurrent with this, DATA LATCH produces the WRITE PULSE, the function of which is to store the data at the prescribed memory location. The advent of SSYNC disables MSYNC and the access cycle is complete with respect to the Unibus and M8110/M8120 interfacing.

### 2.4.2 Unibus DATI Cycle

A DATI memory access operation (Figure 2-4) is similar to the Unibus DATO procedure just described. The access cycle is initiated in the M8110/M8120 logic on receipt of the memory address. Control bits C0 and C1 are input at the same time; C1 is a 0. However, unlike DATO, DATA is not sent from the processor in a DATI operation; the bidirectional data lines will be used to carry the data retrieved from memory back to the processor. MSYNC results in BREQ, which triggers the timing sequence that follows. BREQ IN PROG fulfills the second requirement for MEM SSYNC and the memory address is latched into the MAD register. The selected memory address is then delivered to the memory matrix along with required timing signals. MEM SSYNC is brought up, after a delay, by ACCESS READY LATCH. MEM SSYN notifies the processor that the timing sequence is completed and that the data requested is available for acceptance. Although SA LATCH is not set, the read data bypasses the Data Out Register en route to the Unibus.

## 2.5 MEMORY BUS

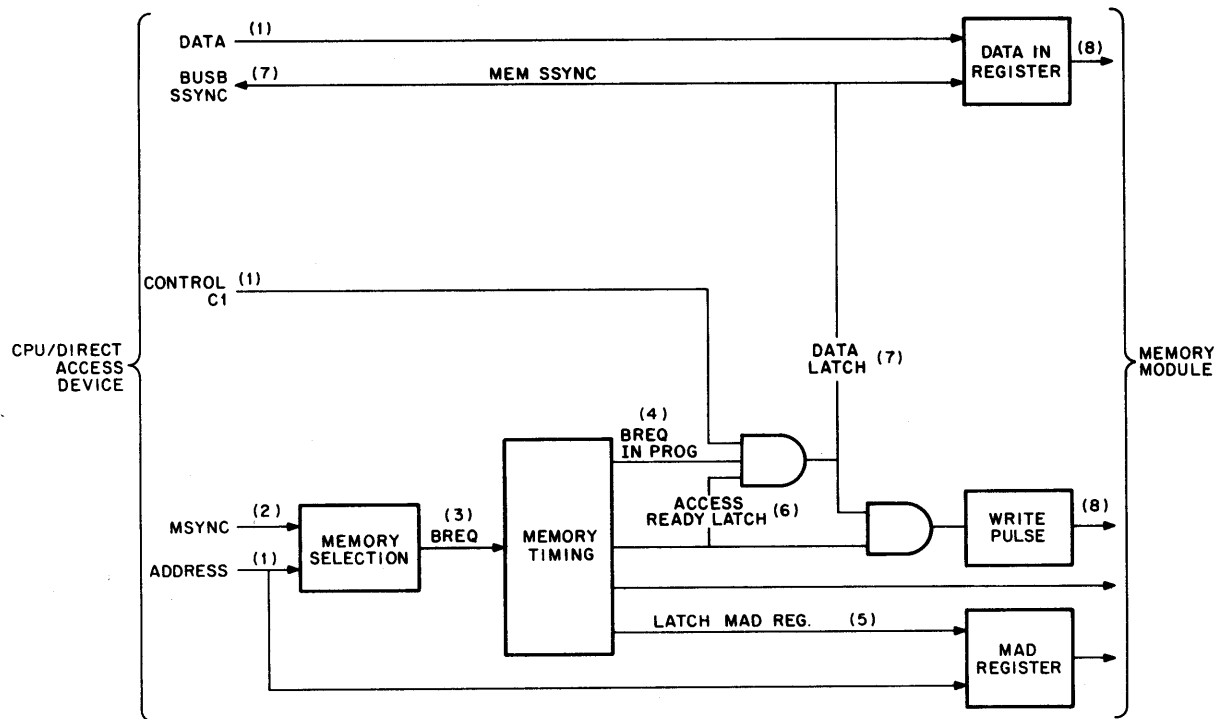
Figure 2-5 is a simplified block diagram of the semiconductor memory bus. This bus is part of the M8110/M8120 Semiconductor Memory Control module and implements the multiplexing of DATO and DATI operations between the Fastbus, Unibus, and semiconductor memory system storage.

The multiplexing of memory access operations over the memory bus is governed by priority arbitration logic on the M8110/M8120 control. This logic arbitrates memory access requests only when simultaneous requests are received from the Unibus and Fastbus. In such arbitration, Unibus memory access cycles have higher priority. In all other cases, memory is multiplexed between the Fastbus and the Unibus on a "first come, first served" basis. In addition, any memory access cycle, once started, locks out all other bus requests until completed. The DATI side of the M8110/M8120 memory bus is coupled to both the Fastbus data-in lines and the Unibus interface so that disposition of data on this portion of the memory bus is handled by the requesting bus.

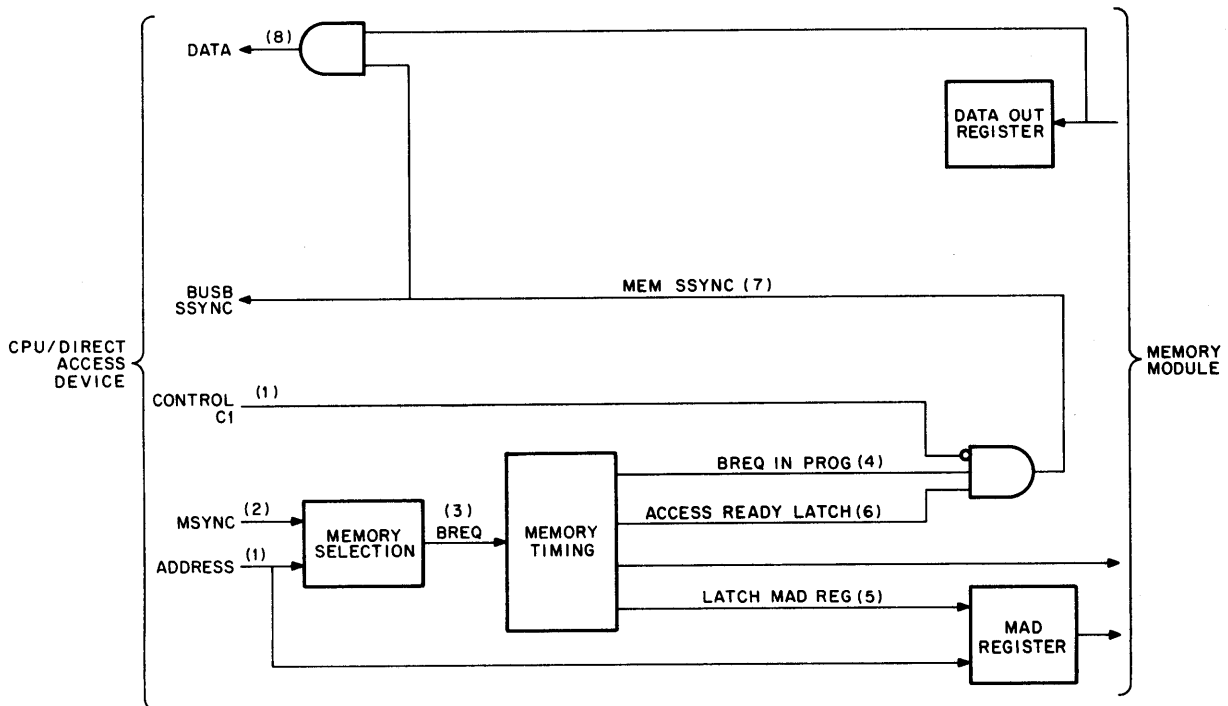
## 2.6 SEMICONDUCTOR MEMORY ADDRESSING

The M8110/M8120 Semiconductor Memory Control module, whether directing bipolar or MOS memories, always processes an incoming Fastbus or Unibus address in the same manner. This process involves two simultaneous actions by each M8110/M8120 control: address examination and address mapping. In order to clarify the effects of these actions, the specific description of each action is preceded by a brief description of the PDP-11 addressing scheme.

DATA



DATI



11-1320

Figure 2-4 Unibus Interface

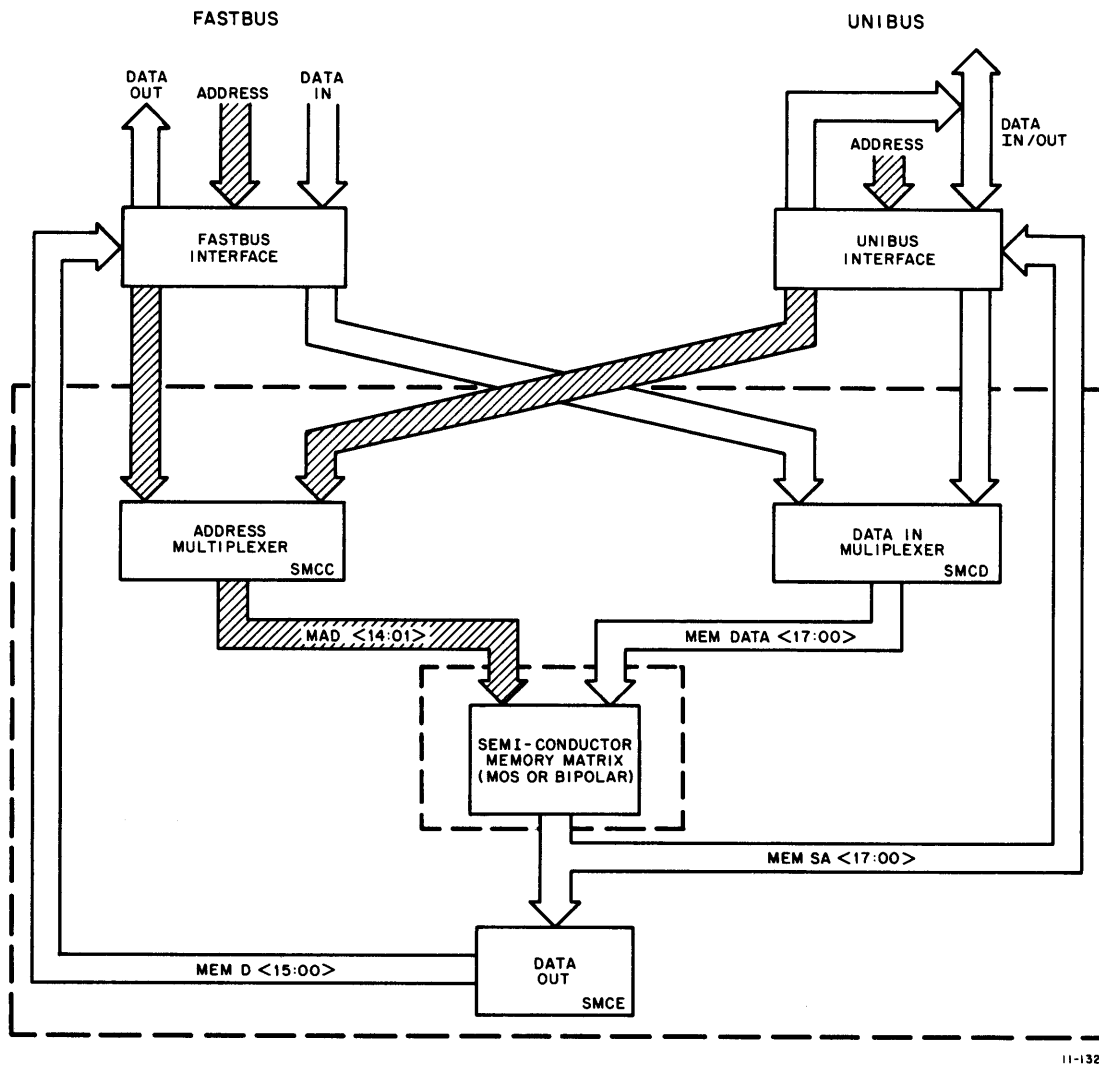


Figure 2-5 Semiconductor Memory Bus, Simplified Block Diagram

In the PDP-11 System, a 16-bit word is addressed by an even binary number. The high-order byte in that word is addressed by the next higher number in the binary address count, which is an odd number. In this manner, the state of the least-significant bit in an address (bit 0) determines whether a full word (or low-order byte) or the high-order byte is being addressed. Consequently, the address for a 16-word (or the low order byte in any word) is always even, and the address for a high-order byte in any word is always odd.

For example:

Typical address for a full 16-bit word or low-order byte	173346 <sub>8</sub>
Address for the high-order byte in the same word	173347 <sub>8</sub>

### 2.6.1 Address Decoding at the M8110/M8120 Control

Figure 2-6 shows how each M8110/M8120 control examines Unibus and Fastbus address. At each control, the states of address bit <17:13> are compared with equivalent jumper-wired states to decode the address. Address bits <17:16> designate up to 32K of semiconductor memory locations out of a total memory capacity of 128K. Decoding of address bit 15 designates the specific M8110/M8120 control being addressed. Therefore, that control whose

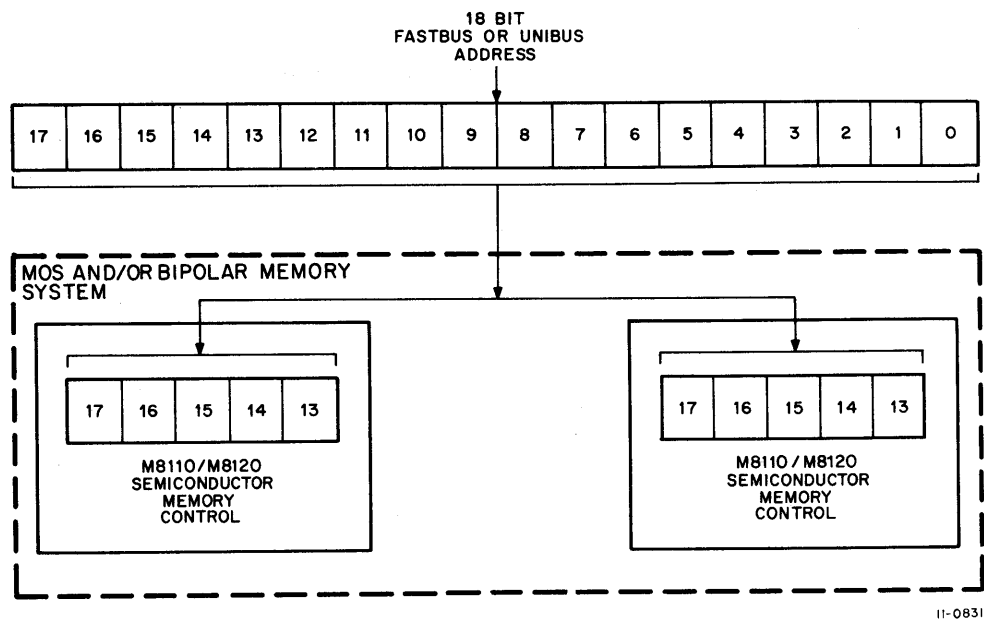


Figure 2-6 Semiconductor Memory Address Examination

jumper-wired states of bits <17:15> match the states of address bits <17:15> has the location being addressed within its total range of memory locations. Decoding address bits <14:13>, as compared with jumpered states at each module, designate that the memory location specified by the address being examined is within one of the 4K-word pages comprising the semiconductor memory. When all conditions of address decoding, as specified by jumper connections at either control, are satisfied, then mapping of that address is enabled at the selected controls.

### 2.6.2 Address Mapping at the M8110/M8120 Control

The manner in which addresses are examined by the M8110/M8120 requires that each incoming Fastbus or Unibus address must be mapped into MAD register. This mapping action, as illustrated in Figure 2-7, amounts to the shifting of address bits <12:02> one position to the right, and the routing of address bits 01 and 12 according to specific jumper configurations. The installation of required address jumpers is described in detail in Paragraph 3.2.1.

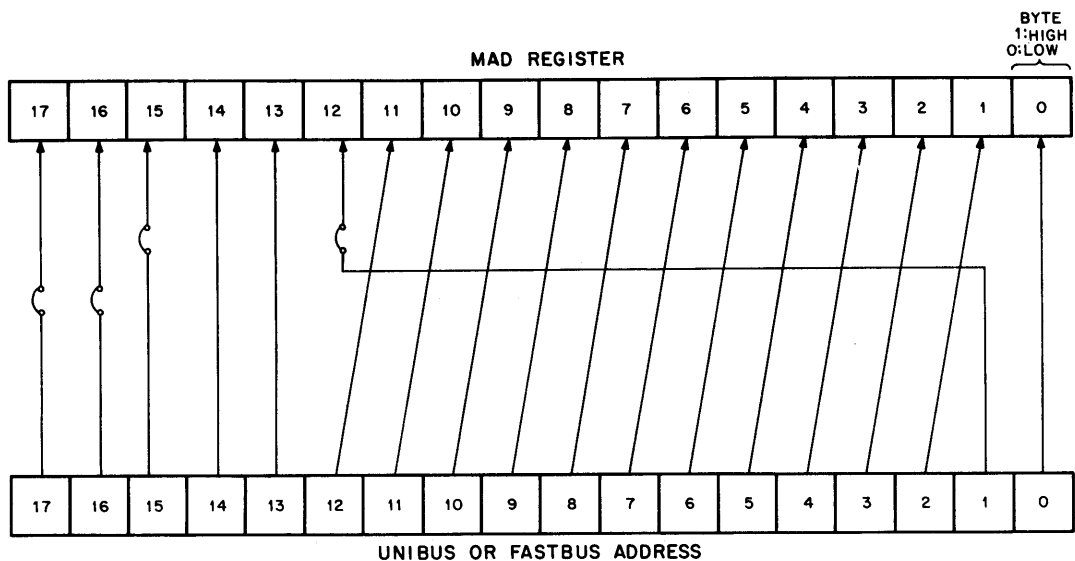


Figure 2-7 Semiconductor Memory Address Mapping

### 2.6.3 4K Bipolar Memory Matrix Module Address Decoding

In addition to being part of the addressing scheme on the M8110/M8120 control, MAD bits (14:13) are decoded on each M8121 4K Memory Matrix module attached to the selected M8110/M8120 (Figure 2-8). The states of MAD (14:13) are compared with a unique switch configuration on each M8121 module. The module with the matching states is the one to be accessed. This equality at the addressed M8121 module, in turn, enables examination of MAD (11:10). The states of these two bits are decoded, by a logic network on the M8121, to identify which one of four 1K word rows contains the 16-bit word location to be addressed. Finally, MAD bits (12,09:01) are decoded on the M8121 to select the particular word within the chosen 1K section.

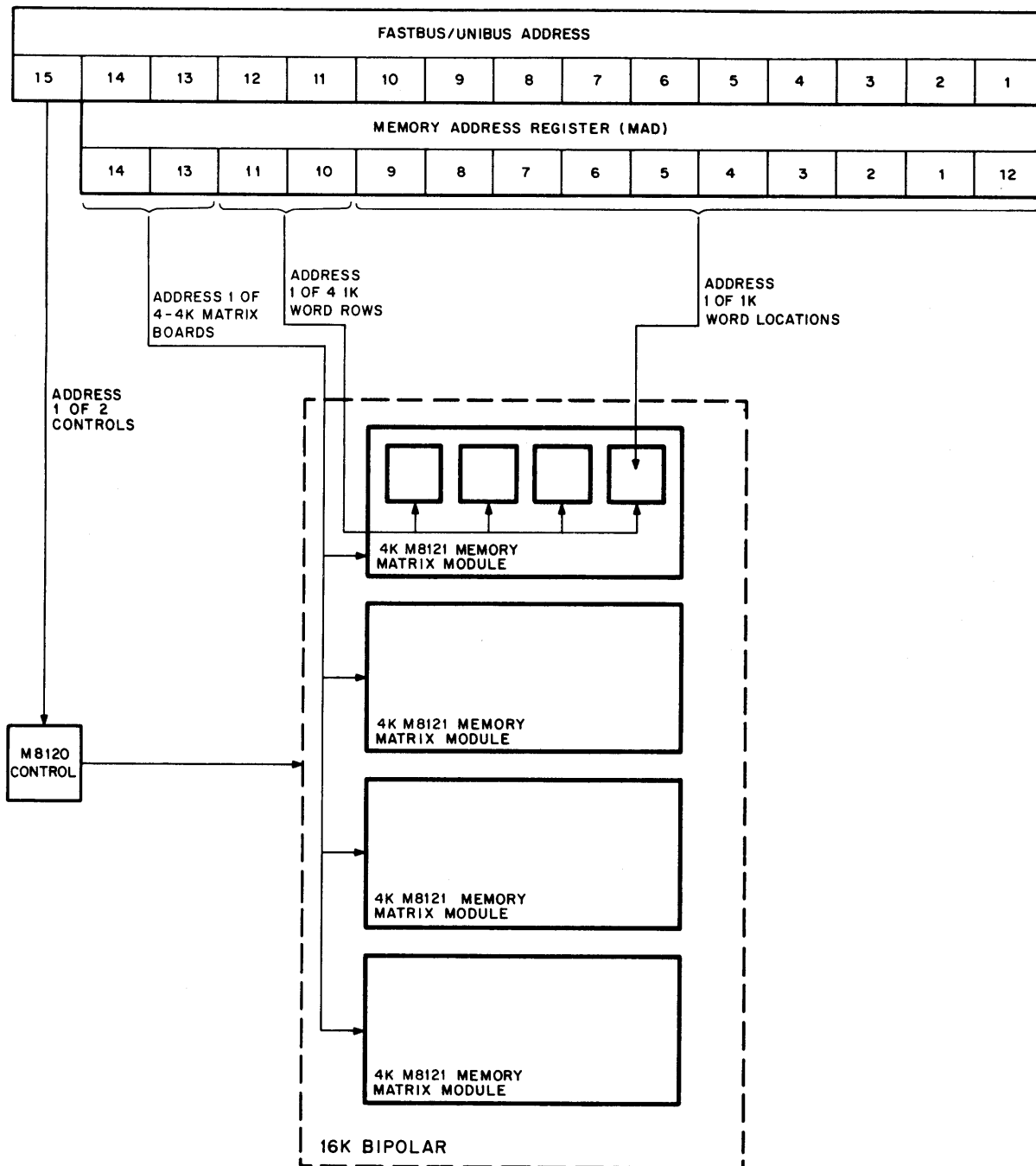
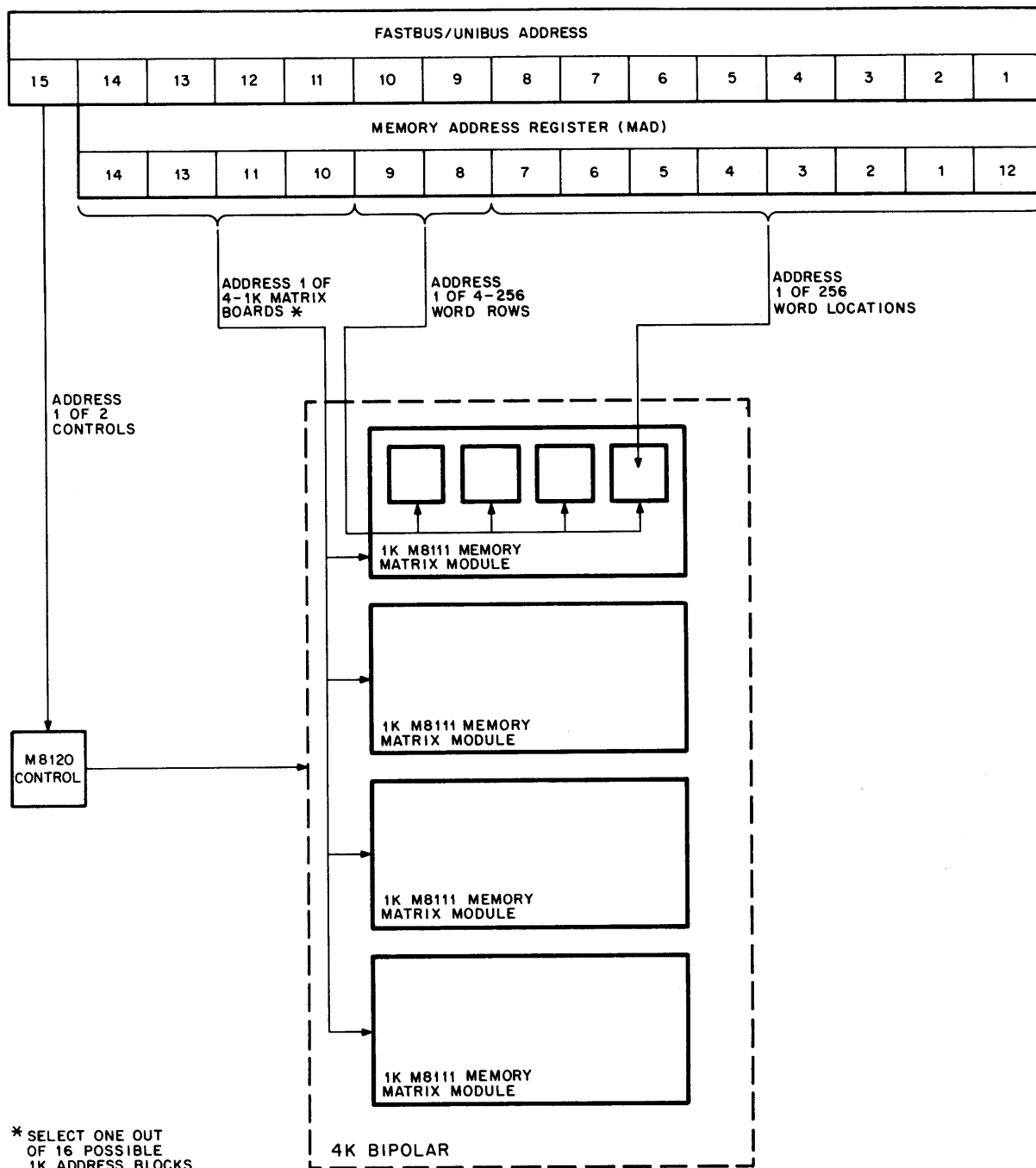


Figure 2-8 4K Bipolar Memory Matrix Addressing (M8121)

11-3634

## 2.6.4 1K Bipolar Memory Matrix Module Address Decoding

Address decoding in the 1K M8111 Memory Matrix module is similar to that performed in the 4K M8121 module just described. The difference is in the function of the individual MAD bits (Figure 2-9). In the M8111, MAD bits (14:13, 11:10) are compared with a unique jumper configuration. The M8111 with the jumpers that match the MAD bit configuration is the one to be accessed. This bit comparison on an M8111 then allows MAD bits (09:08) to identify which one of four 256-word rows contains the word location to be addressed. The particular word in this 256-word row is selected by MAD bits (12,07:01).



11-1323

Figure 2-9 1K Bipolar Memory Matrix Addressing (M8111)

### 2.6.5 4K MOS Memory Matrix Module Address Decoding

The MAD <14:13> and <02:01> bits are decoded at each G401 MOS Memory Matrix module when the directing M8110/M8210 control is addressed (Figure 2-10). Because the states of MAD <14:13> are compared to jumpered states unique to each module, the module with matching states is the module to be accessed. This equality at the addressed G401 module, in turn, enables examination of MAD <02:01>. The states of these bits are decoded at a logic structure on the G401 module to determine which of the four 1024 X 16-bit word block contains the location being addressed. Output from this structure enables addressing of the pertinent 1024-word blocks and implements access to the address location.

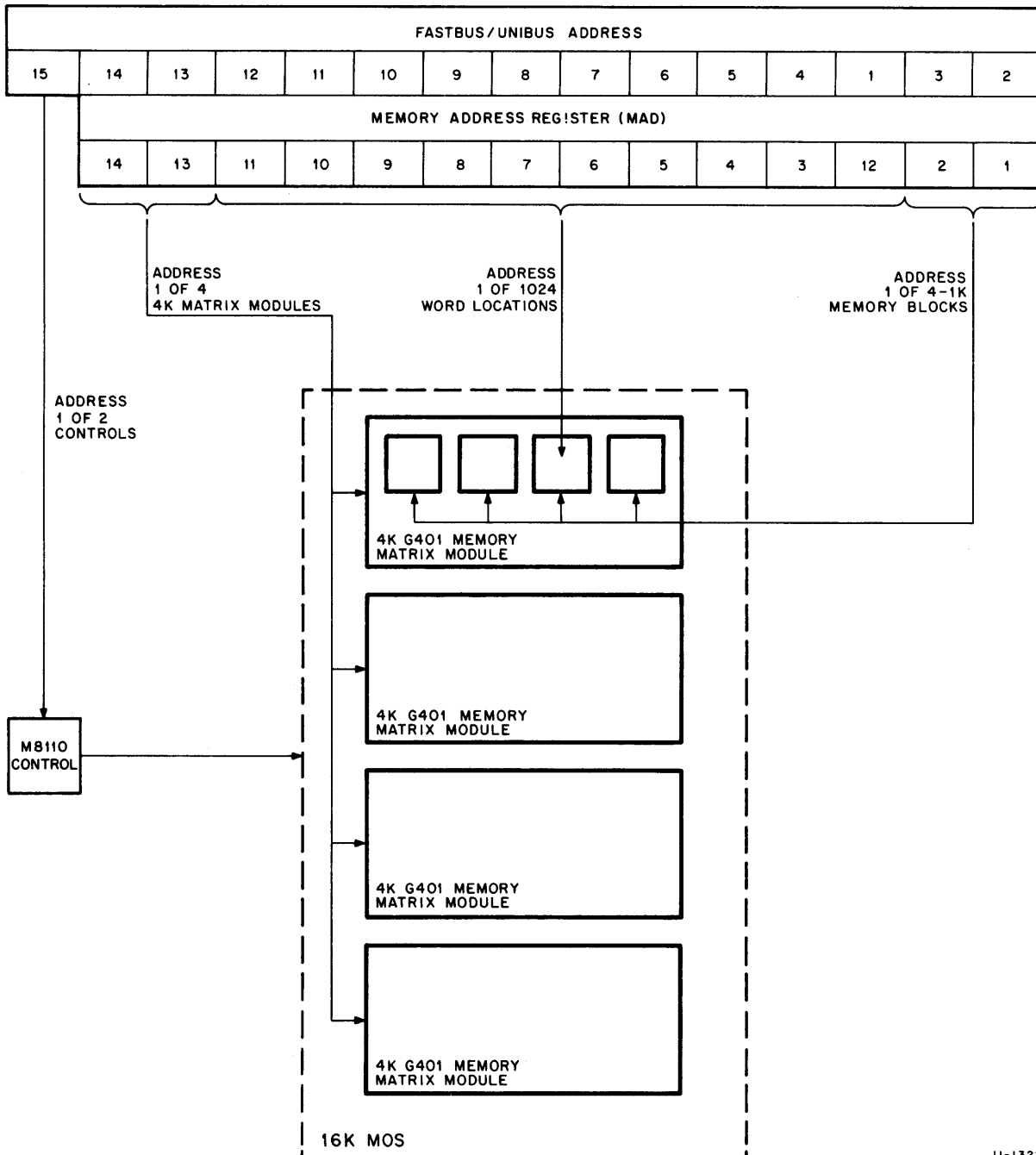


Figure 2-10 4K MOS Memory Matrix Address Examination (G401)

# CHAPTER 3

## LOGIC DESCRIPTION

### 3.1 INTRODUCTION

As described in Paragraph 1.1, an MS11 Semiconductor Memory System can take two forms: bipolar and MOS. Systems with bipolar memory use the M8120 control; MOS systems use the M8110 control. Both types of control are described in the following paragraphs. The descriptions of semiconductor modules follow this system structure.

The narrative begins with the M8110/M8120 control selection, memory bias, and interface logic. This is followed by a description of the M8110/M8120 parity function and the refresh logic, which pertains only to the MOS semiconductor memory system. Finally, there is a description of the three memory matrix modules: M8121, M8110 and G401.

### 3.2 M8110/M8120 SEMICONDUCTOR MEMORY CONTROL MODULE

Figure 3-1 is detailed block diagram of the M8110/M8120 control. Note that transfer of data through the M8110/M8120 to and from the Unibus or Fastbus and the associated memory matrix module is directed by the timing and control logic shown on drawing SMCA. This logic within the M8110/M8120 interprets control signals from the Fastbus or Unibus, controls communication with these buses, and implements DATO and DATI cycles when requested. The MOS memory refresh logic on the M8110 control is enabled through a jumper connection so that this logic is operational only when MOS memory matrix modules are controlled by the M8110 control.

Detailed descriptions of M8110/M8120 logic operation are divided into the following sections:

1. The selection, interface, bus, and multiplexing subfunctions, manipulated by the M8110/M8120 control logic to perform memory access cycles (Paragraphs 3.2.1 – 3.2.5)
2. The M8110/M8120 control logic (Paragraph 3.2.6)
3. The M8110/M8120 parity logic (Paragraph 3.2.7)
4. The M8110 refresh logic (Paragraph 3.2.8)

#### 3.2.1 Memory Selection Logic

Memory addresses from the Fastbus or Unibus are received in the M8110/M8120 control address selection logic (drawing SMCF) where they are decoded at a jumper-wired decoding matrix. Decoding of the states of address bits 11 through 17 determines if an address is within the previously established address range, i.e., the address is valid at this controller and memory will be accessed. In a PDP-11/45 System, address bits 17 and 16 address one of four 32K-word sections of memory. Because bit 15 addresses one of two 16K-word groups within a 32K-word section, the state of this bit designates the specific control being addressed. Address bits 14 and 13 specify, for a control with 16K words of MOS or bipolar memory, that the location being addressed is within one of the four G401 MOS or M8121 bipolar matrix modules. For a control with 4K of bipolar memory, the jumpered states of address bits 11 through 14 allow selection of 1K of contiguous addresses out of a 16K address block, i.e., they select one of 4-1K M8111 matrix modules.





Table 3-1 correlates the states of address bits 13 through 17 to the associated memory areas. The required jumper configurations are also shown.

A valid or acceptable memory address from the Fastbus is indicated by SMCF MEM L being returned to the processor via the Fastbus. This signal is the output of a wired AND configuration whose inputs are five exclusive-NOR gates, E89 and E76, and four NAND gates, E77. The address configuration and the absence or presence of jumpers C, D, E, F, H, J, K, L, and M determines SMCF MEM L generation. The jumpers are located at the input to the exclusive-NOR gates and the output of the NAND gates.

As indicated in Table 3-1, retaining or removing the jumpers establishes the memory range controlled by Fastbus and Unibus address bits 13 through 17. Removal of jumper C, D, E, F, or H will cause the associated Fastbus address bit, when equal to a 1 (high), to disable the exclusive-NOR gate and provide one of the required (high) "AND" inputs for SMCF MEM L. Likewise, retaining a jumper results in a 0 address bit disabling the particular exclusive-NOR gate to provide another high input to the wired AND. A simplified version of the address decoder is depicted in Figure 3-2. The assertion of SMCF MEM L results from all high inputs to the wired AND. Highs from the exclusive-NOR gates result when both inputs are low or both inputs are high, thereby disabling the gates. It can be concluded from this that jumper presence (a low) allows a 0 bit (a low) to disable the gate; the gate is wired to accept a 0 address bit. Likewise, jumper absence allows 1 bits to be accepted. A high from a NAND gate results from one of two conditions: 1. The output from the NAND gate enabled by an address *within* the desired range, is blocked by a cut jumper, or 2. The NAND gate, with a jumper intact, is disabled by an address that is *outside* the desired range.

#### NOTE

**Jumpers F and H are applicable to 1K bipolar memory only; they are left intact for 4K bipolar and MOS memory addressing.**

Table 3-2 lists those address bits (11 and 12 for 1K bipolar and 13 and 14 for 4K bipolar and MOS) and jumpers that pertain to the memory address range assignment of individual MOS and bipolar matrix modules. The removal of any one jumper assigns the corresponding address range to a MOS or bipolar module. However, most memory configurations consist of more than one memory module. Table 3-3 lists those jumpers that must be removed to assign memory addresses to the given capacity memory. These addresses are relative to the address block assigned by jumpers C, D, E, F and H. For example, an 8K bipolar memory of two modules would be assigned addresses 0–8191 by removing jumpers J and K in this group of jumpers and leaving the other jumpers (C, D, E, F, and H) intact. However, if this same 8K memory were to be assigned Fastbus addresses 16384 to 24575 (16-24k) then jumper E would also have to be cut. Note that these jumpers (J, K, L, and M for Fastbus addresses; N, P, R, and S for Unibus addresses) are used to assign addresses to individual matrix modules under the direction of a particular M8110/M8120 control, whereas jumpers C, D, E, F, and H are used to assign a 4K or a 16K memory block to a M8110/M8120 control from the total (128K) address area.

The aforementioned jumpers are physically located on the M8110/M8120 module at locations E87 and E75. For example, as indicated on drawing SMCF, jumper J can be found at E75, between terminals 01 and 16.

The inputs to the four NAND gates, E77, in the Fastbus address decoding circuit are SMCF FB MUX 14/12 H and SMCF FB 13/11 H. They are derived from a jumper-wired multiplexer, E67, located on the M8110/M8120 module. Whether address bits 11 and 12 or 13 and 14 are used is determined by the memory type; bits 11 and 12 select a 1K section out of a 4K memory area for 1K bipolar, while bits 13 and 14 select a 4K section out of a 16K area for a 4K bipolar or MOS module. Figure 3-3 illustrates the required jumper connections for both memory types. Memory address bits 13 and 14 (SMCF FB MUX DEC 13, 14 H) are also input to decoder NOR gates E76 and E89 from this same multiplexer, E67. Again, the memory type determines the address bit origin.

#### NOTE

**When installing a 4K matrix board, cut E67 jumpers at pins 1, 3, 5, and 7. For a 1K matrix board, cut E67 jumpers at pins 2, 4, 6, and 8.**

**Table 3-1**  
**Fastbus/Unibus Memory Address (Assign and Decode)**

Fastbus/Unibus Address Decoder Bits					Memory Address Assignment		M8110 Jumpers (E87) (NOTE 1, NOTE 2)				
17	16	15	14	13	1K Bipolar	4K MOS or 4K Bipolar	C	D	E	F	H
0	0	0	0	0	0-4K	0-16K					
0	0	0	0	1	4-8K						X
0	0	0	1	0	8-12K					X	
0	0	0	1	1	12-16K					X	X
0	0	1	0	0	16-20K	16-32K			X		
0	0	1	0	1	20-24K				X		X
0	0	1	1	0	24-28K				X	X	
0	0	1	1	1	28-32K				X	X	X
0	1	0	0	0	32-36K	32-48K		X			
0	1	0	0	1	36-40K			X			X
0	1	0	1	0	40-44K			X		X	
0	1	0	1	1	44-48K			X		X	X
0	1	1	0	0	48-52K	48-64K		X	X		
0	1	1	0	1	52-56K			X	X		X
0	1	1	1	0	56-60K			X	X	X	
0	1	1	1	1	60-64K			X	X	X	X
1	0	0	0	0	64-68K	64-80K	X				
1	0	0	0	1	68-72K		X				X
1	0	0	1	0	72-76K		X			X	
1	0	0	1	1	76-80K		X			X	X
1	0	1	0	0	80-84K	80-96K	X		X		
1	0	1	0	1	84-88K		X		X		X
1	0	1	1	0	88-92K		X		X	X	
1	0	1	1	1	92-96K		X		X	X	X
1	1	0	0	0	96-100K	96-112K	X	X			
1	1	0	0	1	100-104K		X	X			X
1	1	0	1	0	104-108K		X	X		X	
1	1	0	1	1	108-112K		X	X		X	X
1	1	1	0	0	112-116K	112-128K	X	X	X		
1	1	1	0	1	116-120K		X	X	X		X
1	1	1	1	0	120-124K		X	X	X	X	
1	1	1	1	1	124-128K		X	X	X	X	X

- NOTES: 1. "X" denotes jumper to be cut.  
2. Jumpers F and H are left intact for all 4K memory assignments, i.e., when assigning addresses to G401 and M8121 modules.

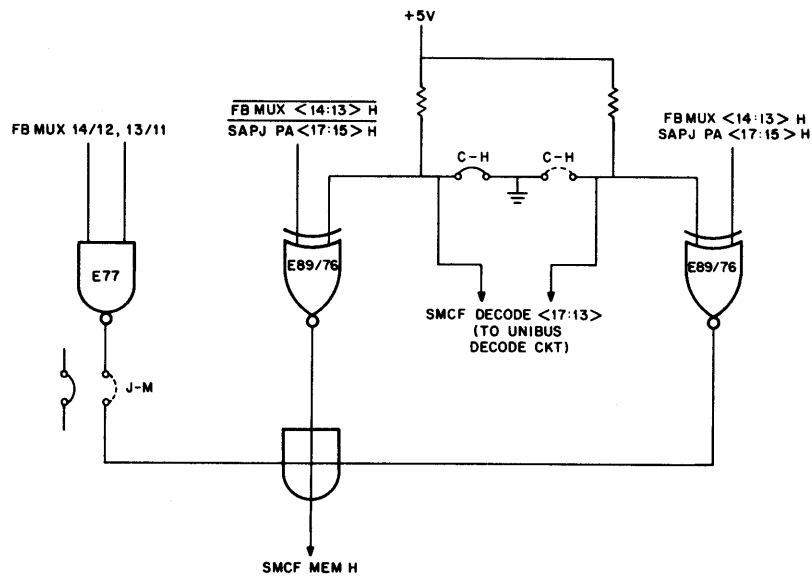


Figure 3-2 Simplified Memory Address Decode (SMCF)

11-1326

Table 3-2  
MOS/Bipolar Module Addressing

Fastbus/Unibus Memory Address Bits		Memory Address Assignment (within 128K area)		Remove Jumpers	
FB MUX 14/12	FB MUX 13/11	4K MOS or 4K Bipolar	1K Bipolar	Fastbus Address Select	Unibus Address Select
0	0	0-4095	0-1023	J	N
0	1	4096-8191	1024-2047	K	P
1	0	8192-12287	2048-3071	L	R
1	1	12288-16383	3072-4095	M	S

Table 3-3  
MOS/Bipolar Memory Addressing

No. of Memory Modules in Memory*	Memory Capacity		Remove Jumpers	
	4K MOS or 4K Bipolar	1K Bipolar	Fastbus Address Select	Unibus Address Select
1	4K	1K	J	N
2	8K	2K	JK	NP
3	12K	3K	JKL	NPR
4	16K	4K	JKLM	NPRS

\*Connected to one M8110/M8120 Control.

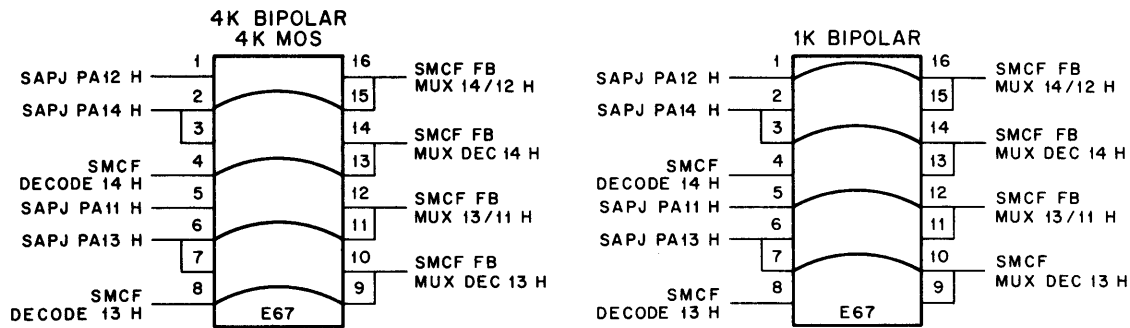


Figure 3-3 Fastbus Address Multiplexing (14:11) Required E67 Jumpers

Note that in the 4K module configuration, with jumpers F and H retained, the jumper inputs to NOR gates E76 and E89 (bits 13 and 14) are always at ground. The address bit inputs to these same gates are jumpered, at E67, to the F and H jumper inputs (SMCF DECODE 13, 14 H), thereby disabling the gates (all inputs are at ground). Since the output from these two NOR gates is always high, effectively removing them from the decoder, the influence of bits 13 and 14 in 4K memory addressing depends on the absence or presence of jumpers J, K, L, and M.

Figure 3-4 shows the signals used by the Fastbus and Unibus Address decoders.

An effective Unibus memory address, together with SMCH MSYNC (B) L, generates the SMCF BREQ L signal that initiates a Unibus DATO or DATI operation. The Unibus address decoder (SMCF) is a wired-AND circuit, similar to the Fastbus address decoder just described, that consists of five NAND gates (E74 and E85) and five exclusive-NOR gates (E76 and E88). Inputs to the exclusive-NOR gates are: Unibus address bits 15, 16, and 17; Unibus MUX DEC address bits 13 and 14 from E78; a jumper-wired multiplexer on the M8110/M8120 module; and the outputs (SMCF DECODE (17:13) H) from five of the jumpers in the Fastbus address decoder. E78 is wired (Figure 3-5) according to the memory type installed; it performs the same function for Unibus addressing as E67 does for Fastbus addressing. Inputs to four of the NAND gates (E74) are SMCF UB MUX 13/11 H and SMCF UB MUX 14/12 H, also from E78. Unibus decoder bits 13 through 17 use the same jumper (C, D, E, F, and H) configuration established for Fastbus addressing. In addition, jumpers N, P, R, and S at the outputs of NAND gates E74 must be selectively removed (Tables 3-2 and 3-3) to establish the desired memory addresses for the matrix modules. Jumpers N, P, R, and S are located at the same physical location (E75) as jumpers J, K, L, and M of the Fastbus address decoder.

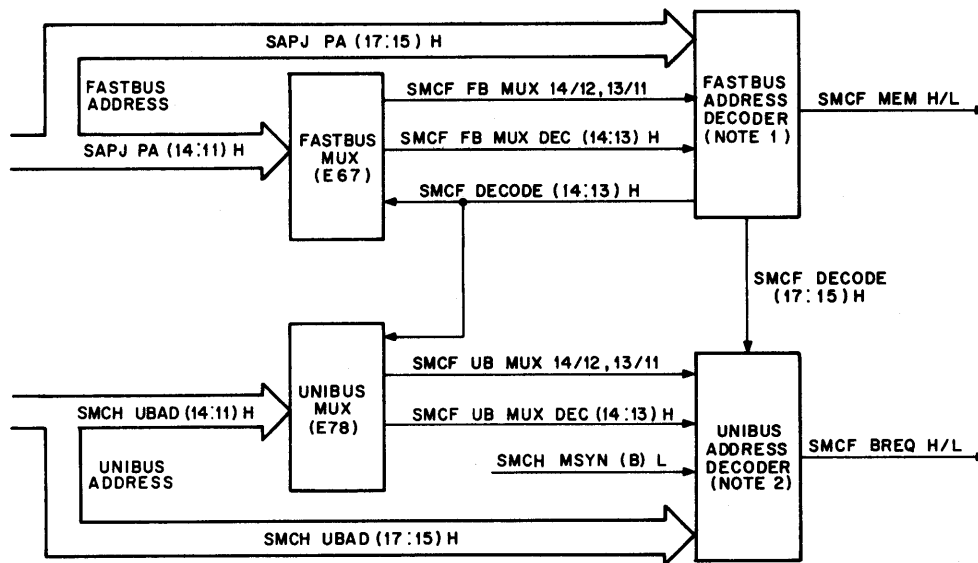
#### NOTE

When installing a 4K matrix board, cut E78 jumpers at pins 1, 3, 5, and 7. For a 1K matrix, cut E78 jumpers at pins 2, 4, 6, and 8.

### 3.2.2 Unibus Interface (SMCH)

Figure 3-1 shows the Unibus data and address paths. In contrast to the Fastbus, which, along with a semiconductor memory, is a physical component of the PDP-11/45 processor, the Unibus can be located remotely. As a consequence, the M8110/M8120 can connect to the full-duplexed Unibus through long lines which must be driven and received. The Unibus receiver and driver logic (shown on drawing SMCH) includes: the address receiving logic involved in both DATO and DATI cycles, the data receiving logic which operates only on a DATO, the data driving logic which responds to a DATI operation, and specific logic signals controlling Unibus DATO and DATI operations.

The 18-bit Unibus address received at SMCH on the lines BUSB A (17:00) L is input to an 18-stage buffer formed by type 380 line receivers. The second input to each receiver is conditioned by a common line to ground. Therefore, each Unibus address received is terminated at the characteristic line impedance and inverted to assert SMCH UBAD (17:00) H. These outputs are applied to the MAD register shown on SMCC.



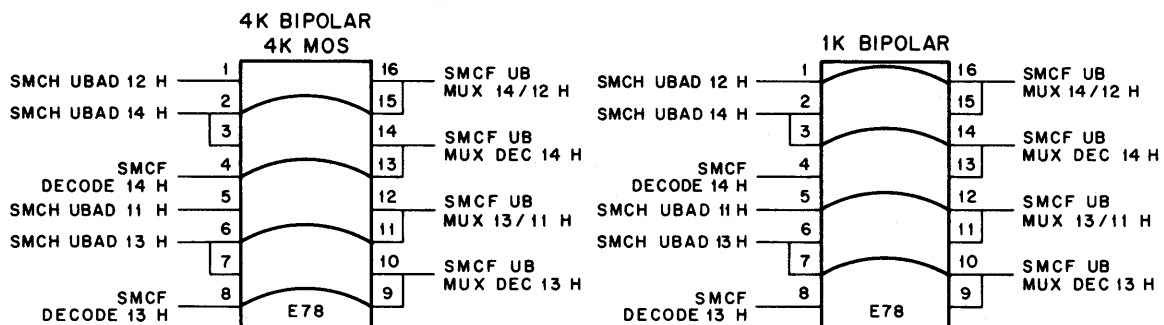
NOTES:

1 - Jumpers C,D,E,F and H (E87)  
Jumpers J,K,L and M (E75)

2 - Jumpers N,P,R and S (E75)

11- 2185

Figure 3-4 Address Decoding (Drawing SMCF)



11- 1329

Figure 3-5 Unibus Address Multiplexing (14:11) Required E78 Jumpers

The 16-bit Unibus data input is received at SMCH on the lines **BUSB D (15:00) L** as input to a 16-stage buffer which consists of type 380 line receivers. The second input to each receiver is conditioned by a common line to ground. As a result, each data word received from the Unibus is terminated at the characteristic line impedance and inverted to assert **SMCH UB DATA (15:00) H**. These outputs are applied to the data in the multiplexer shown on **SMCD**.

The data word read during a given **DATI** cycle is asserted at the Unibus interface as **SMCE MEM SA (15:00) H**. This data is input to a 16-stage drive network formed by type 8881 open collector NAND gates, AND gates **E45**, **E46**, **E47**, and **E48**. This gating network is enabled by the ANDing of **SMCB MEM SSYNC L** and **SMCH UBC1 H**. **SMCH UBC1 H** is low during **DATI** operations and **SMCB MEM SSYNC L** is asserted during each **DATI** cycle at the point where the data word addressed during that cycle is stable. The output of this gating network, when enabled, asserts the line **BUSB D (15:00) L** on the Unibus.

All Unibus control signals to the **M8110/M8120** are received and buffered at **SMCH**. **BUSB MSYNC L** is received at the Unibus interface and inverted to assert **SMCH MSYN (B) H (E96)**. This level is, in turn, inverted to assert the complementary signal **SMCH MSYNC (B) L** at **E100**.

**BUSB C0 L** and **C1 L** define the nature of each Unibus access cycle. They are received and inverted to generate **SMCH UBC0 H, L** at **E37** and **E39** and **SMCH UBC1 H, L** at **E49** and **E39**. The latter signal is inhibited until **SMCH MSYNC (B) L (E100)** is received 150 ns after the processor raises **BUS BUSY**. The states of **SMCH UBC0** and **SMCH UBC1**, along with the memory operation initiated by each state, are listed in Table 2-2. Note that the levels of **UBC0 L** and **UBC1 L** correspond directly with the **C0L** and **C1L** levels from the Unibus, while the **UBC0 H** and **UBC1 H** levels are complementary to the Unibus inputs.

**PWRS MEM DC LO L** is received at the interface and inverted to assert one of the OR conditions for **SMCH POWER CLR L**. **BUSB INIT L** is received at the Unibus and gated with the AND of **SMCB REF REQ L** and **SMCA RREQ (B) L**. The result, when true, is the other OR condition that asserts **SMCH POWER CLR L**. The purpose of this level is to clear all condition-sensitive logic following a power-up cycle and to initialize this logic at start-up time. Note that if a refresh cycle is in process, **SMCH POWER CLR L** is inhibited, except when a power failure causes **PWRS MEM DC LO L** to be asserted.

#### **NOTE**

Fastbus address and data interfacing are shown, respectively, on drawings **SMCC** and **SMCD**. These drawings are described in Paragraphs 3.2.3 and 3.2.4.

### **3.2.3 Address Multiplexing (SMCC)**

The semiconductor memory bus is part of the **M8110/M8120** control and includes the multiplexing of memory address and data from the Fastbus and Unibus to the memory matrix modules (Figure 2-5). Data addressed on a **DATI** cycle is bused directly from the matrix modules to both the Fastbus and Unibus interfaces to be received by the requesting bus (Fastbus or Unibus). Refer to the data and address path block diagram shown in Figure 3-1. The **M8110/M8120** address multiplexing logic, shown on drawing **SMCC**, is shared by three classes of addresses: the Unibus address, the Fastbus address, and the refresh address.

#### **NOTE**

Refresh addresses are generated only when an **M8110** is controlling **G401 MOS Memory Matrix** modules. When an **M8110** is controlling **M8111** or **M8121 Bipolar Memory Matrix** modules, the logic that generates refresh addresses is disabled.

Out of each 18 address bits received at the control from either the Unibus or Fastbus, 15 bits are multiplexed and mapped as shown in Figure 2-7 and Table 3-4. The refresh address **SMCB RFAD (04:00) H** is a row address only and internally generated (Paragraph 3.2.8).

Address multiplexing occurs asynchronously, based either on demand, as with isolated access requests, or on priority arbitration, as in the case of several simultaneous access requests. However, when the multiplexing strobe levels are asserted at the address multiplexing logic, all priority claims have been arbitrated; subsequent requests are locked out. The previous address is output until the leading edge of SMCA REQ LATCH PULSE L, when it is unlatched from the buffer.

**Table 3-4**  
**Multiplexed Address Inputs to MAD (SMCC)**

Unibus Address	Fastbus Address		Refresh Address		Memory Address
SMCH UBAD XX H	SAPJ PA XX H	DAPB BAMX XX H	SMCB RFAD XX H		SMCC MAD XX (1) H, L
00		00		→	00
02		02		→	01
03		03		→	02
04		04	00	→	03
05		05	01	→	04
06	06		02	→	05
07	07		03	→	06
08	08		04	→	07
09	09			→	08
10	10			→	09
11	11			→	10
12	12			→	11
01		01		→	12
13	13			→	13
14	14			→	14
15	15				
(Note)	(Note)				
16	16				
17	17				

NOTE: Fastbus/Unibus address bits 15, 16, and 17 are used in the bus address decoders (SMCF). They are not included in the MAD configuration output to the memory matrix modules.

**3.2.3.1 Unibus Address Multiplexing** – SMCA BREQ (B) H and SMCA REQ LATCH PULSE H (drawings SMCA and SMCC) assert SMCA BREQ ADDR EN L to gate SMCH UBAD <14:00> H into the latching buffer. This address from the Unibus is latched into the buffer on the trailing edge of SMCA REQ LATCH PULSE L. This serves to map the address so that SMCH UBAD <12:02> corresponds to MAD <11:01> (1) H, SMCH UBAD 01 H corresponds to SMCC MAD 12 (1) H, SMCH UBAD <14:13> H corresponds to SMCC MAD <14:13> (1) H, and SMCH UBAD 00 H corresponds to SMCC MAD 00 (1) H.

**3.2.3.2 Fastbus Address Multiplexing** – Fastbus addresses are multiplexed onto the address latching bus by SMCA PREQ ADDR EN L, which is asserted by SMCA BREQ (B) L, SMCA RREQ (B) L, and SMCA REQ LATCH PULSE H. This action gates the Fastbus address inputs onto the address latching bus. This address data is latched into the buffer on the trailing edge of REQ LATCH PULSE L. Fastbus addresses are mapped in the same manner as Unibus addresses.



**3.2.3.3 Refresh Address Multiplexing** – The 5-bit internally generated refresh address SMCB RFAD <04:00> H is multiplexed into the address latching buffer by the assertion of SMCA RREQ (B) L and latched on the trailing edge of SMCA REQ LATCH PULSE L. Each refresh address loaded into the buffer is mapped so that SMCB RFAD <04:00> H corresponds to MAD <07:03> (1) H.

### 3.2.4 Data Multiplexing (SMCD)

In executing a DATO operation from the Fastbus or Unibus, a data word or byte accompanies the memory address. Multiplexing of the data takes place in a 16-stage memory data buffer, with each stage driving the corresponding stage of a 16-stage latching data register. Logic is shown on drawing SMCD. Four 74S158 multiplexers comprise the data buffer; the latching data register is composed of three elements of a 3404 latch (E1, E3, and E13).

During a Fastbus DATO operation, data (PDRB BR <15:00> B L) is gated into the data buffer with SMCA PREQ (B) H. However, during a Unibus DATO, the absence of this signal (SMCA PREQ (B) H) enables the data (SMCH UB DATA <15:00> H) entry. The output of each multiplexer stage is delivered to the data (D) input of the corresponding data latching register stage. SMCB DATA LATCH H is the common latching pulse to all the L inputs of this register for both Fastbus and Unibus write operations.

The (1) outputs from the 3404 latches follow the D inputs as long as the L inputs are low (SMCB DATA LATCH H). These latches are latched when SMCB DATA LATCH H is asserted. The (1) outputs are thus locked, i.e., the information present at the D inputs, at the time of the positive-going transition at the L input, is retained at the (1) outputs.

SMCD MEM DATA <15:00> H is output to memory for storage. The output of the data buffer, SMCD MBD <15:00> is also input to two parity generators, E2 and E4, whose outputs are the parity bits SMCD MEM DATA <17:16> H to memory (Paragraph 3.2.7.4). The resultant output of E2 and E4 is latched into two latching register stages, E13, with SMCB DATA LATCH H. During DATO, both outputs of the parity generator are stored; bit 17 with the high-order byte and bit 16 with the low-order byte. Only one of the two bits will be generated and stored when a DATOB is executed.

### 3.2.5 Data Output (SMCE)

Read data, destined for the Fastbus during DATI operation, is retained in the Data Out Register shown on drawing SMCE. This 18-stage logic circuit, composed of a latching register and an output buffer, functions as the interface when memory is read out to the Fastbus. Read data to the Unibus, bypassing this logic, is routed directly from memory to the Unibus drivers (drawing SMCH).

The 16 low-order stages of the Data Out Register are formed by three 3404 latch elements (E102, E111, and E122) and four 74S03 open-collector NAND GATE CHIPS (E101, E112, E113, and E123). Stages 16 and 17, which latch the lower and upper byte parity bits for input to the parity checking circuits (E103 and E124), are formed by two of the latches in E122.

The data (SMCE MEM SA <17:00> H) from the addressed memory location is inverted in the latching register and output to the parity checking logic as SMCE DATA OUT <17:00> L. Latching of the input data into the latching register occurs once during each DATI cycle when SMCA SA LATCH (1) H is raised. SMCE DATA OUT <15:00> L is, in turn, inverted in the output buffer and gated by SMCA PREQ (1) L onto the Fastbus as SMCA MEM D <15:00> H. The parity checker, E103 and E124, provides a parity check for each 8-bit byte (Paragraph 3.2.7.5).

### 3.2.6 M8110/M8120 Control Logic

The M8110/M8120 control logic (drawing SMCA) directs all aspects of a given memory access cycle, including priority arbitration, in response to a specific Fastbus or Unibus request. Description of SMCA control logic operation is based on the logic event sequence characteristic of DATO and DATI bus transactions. These event sequences apply to M8110/M8120 controls with either MOS or bipolar memory, with or without optional parity. In a system without byte parity, M8110/M8120 parity and diagnostic logic is ignored.

Because the semiconductor memory system can be accessed from either the Unibus or Fastbus, a DATO operation necessarily has two sources of data access initiation: one in response to Unibus DATO requests, and the other in response to Fastbus DATO requests. Both modes of DATO execution generally share a common control logic structure, with entrances to the logic being a function of the specific request. This same structure also serves to implement the internally initiated refresh cycle, which is applicable only to a MOS memory system.

In a DATI cycle, the location is addressed and the data in that location is read and transferred to the Unibus or Fastbus. However, a DATIP implements a pause after the data is read and transferred, which locks out all other access cycle requests until the next access cycle is initiated. This next access cycle must be a DATO or DATOB unless a parity error is detected during a Fastbus DATIP. In other cases, the DATO following a DATIP will occur within one processor machine cycle. Like the DATO cycle, a DATI operation has two modes of initiation: one in response to a Unibus DATI request, and one in response to a Fastbus DATI request. Both modes of DATI execution generally share a common control logic structure with entrances to this logic being a function of the specific request.

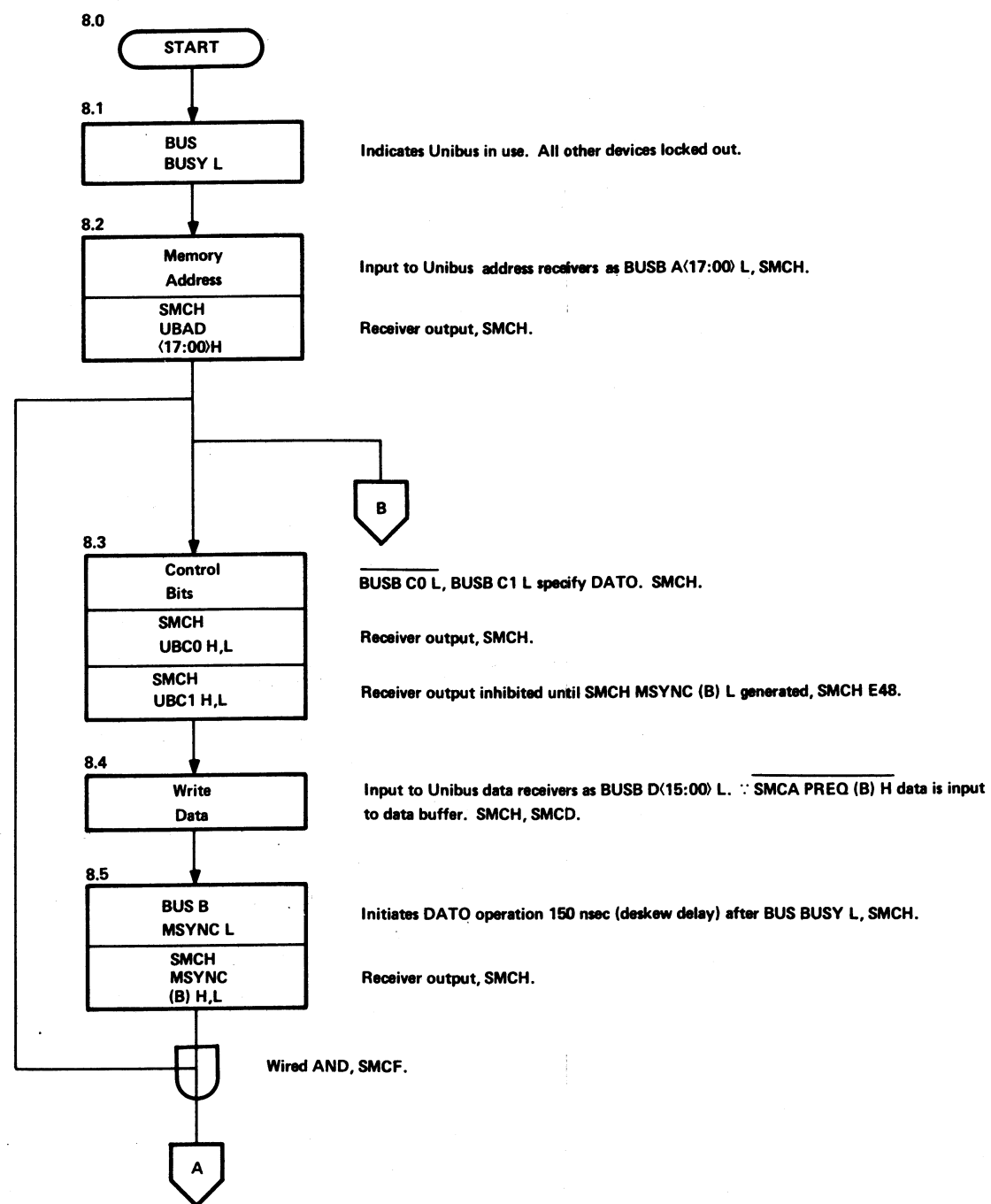
Figures 3-6, 3-7, 3-8, and 3-9 are flowcharts illustrating the sequential steps during DATO and DATI cycles from the Unibus and Fastbus to a bipolar or MOS memory location. Figure 3-10 provides a similar description of a Fastbus DATIP operation followed by the necessary DATO. The individual steps in the flowcharts itemize events or conditions that are necessary for the completion of the entire DATO/DATI/DATIP cycle. Required operations are shown by rectangular blocks, while necessary decisions are depicted by diamond-shaped blocks. A decision is resolved on the basis of the particular condition prevailing at the time the decision block is entered. AND and OR functions are shown, where necessary, to emphasize the requisites for certain operations; off-page connectors provide intra-figure continuity. The remarks section contains comments relative to the particular steps, signal requirements, and the logic drawing where the circuits can be found. Timing (as it pertains to bipolar memory) for the five types of cycles covered by the flowcharts is shown in Figures 3-11, 3-12, 3-13, 3-14 and 3-15. Figure 3-16 depicts the timing for a Unibus DATO operation when the M8110/M8120 is connected to a MOS memory (timing for other operations to MOS memory is similar). Table 3-5 lists the timing requirements relative to the two memory types.

### 3.2.7 Parity Logic

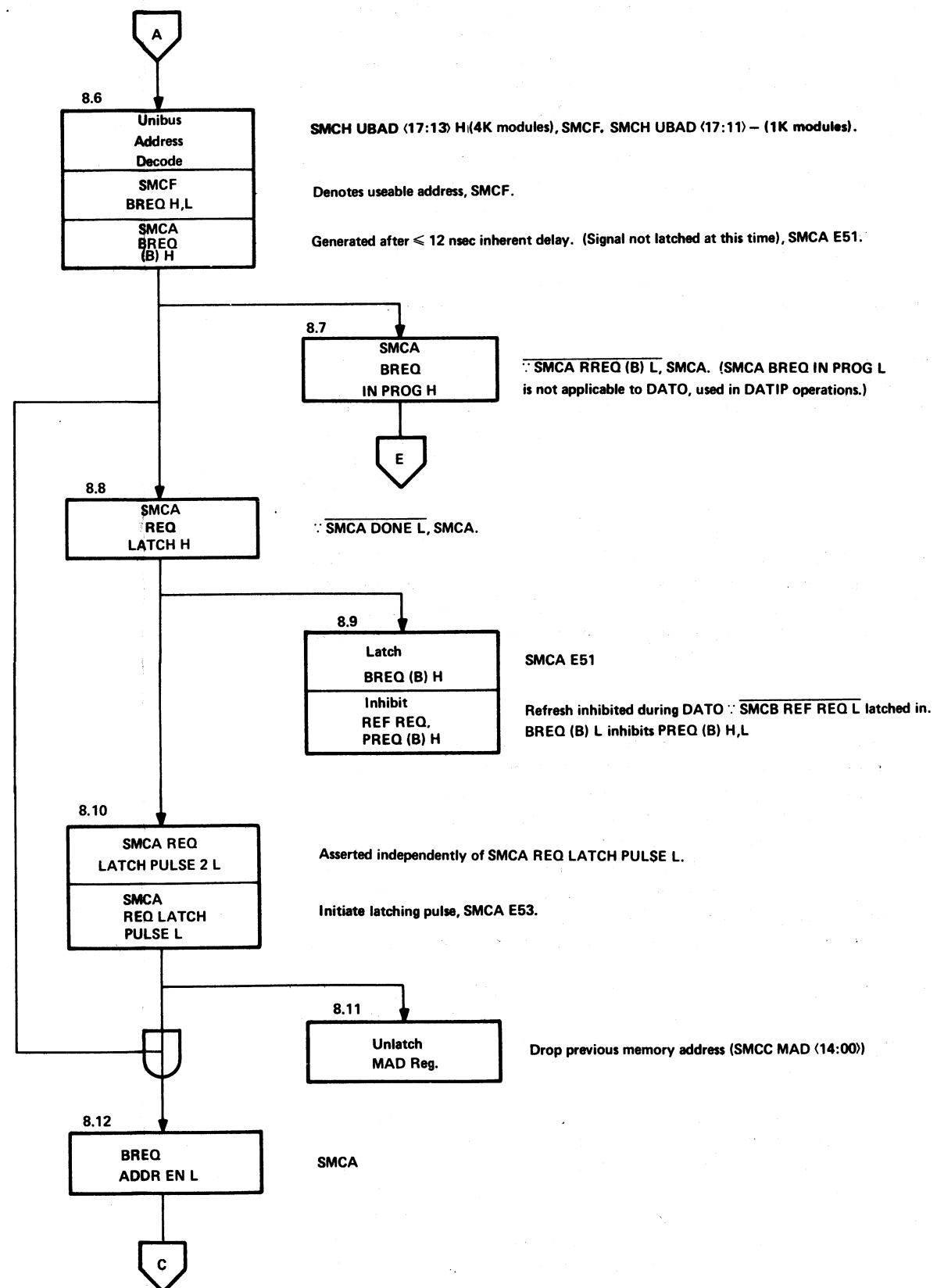
The parity generating and detection circuits in the MS11 provide the means for the operating system and the diagnostic software to control and test for correct memory data parity. The parity detection circuit determines when a (Fastbus) read parity error occurs and then notifies the operating system of the fact. The operating system can then remove the faulty memory module from use. There is a provision to disable the parity detection function when parity checking is not desired. This would be the case if it is necessary to execute a diagnostic out of a memory with known errors. The parity error checking function is normally enabled only when looking for errors. Another portion of the parity logic is used to assign correct parity to write data. The appropriate parity bit or bits are asserted and sent to the addressed memory module. A write-wrong parity bit is also available for diagnostic checking of the parity trap logic. This bit causes odd parity to be stored in memory so that when it is read back a parity error is generated.

The parity logic is contained on the M8110/M8120 module (drawings SMCB, SMCD, SMCE, and SMCF). The principal circuits are the parity register address decoder, the parity register, the parity generator, and the parity checker. Figure 3-17 shows the relationship of these circuits to the read and write data routed through respectively, the Data Out Register and the Data In Multiplexer.

**3.2.7.1 Parity Register Address Decoding** – The parity register (Paragraph 3.2.7.2) is assigned one of 16 addresses in the range 772100-772136<sub>8</sub>. The function of the parity register address decoder (drawing SMCF) is to check all addresses on the Unibus and compare them to the address assigned to the parity register in this M8110/M8120 module. The logic is hard-wired to decode only one of the 16 possible addresses. (The address selection jumper configuration in the address selection logic and a jumper in the parity register address decoder decode the two low-order octal digits in the parity register address. The high order digits, 7721xx, are decoded separately.) If the address on the Unibus is the same as the one assigned to the parity register, and master sync is asserted, one of two signals is asserted: 1) if a read (DATI or DATIP) is indicated, the signal SMCF PAR REG OUT H is asserted and the

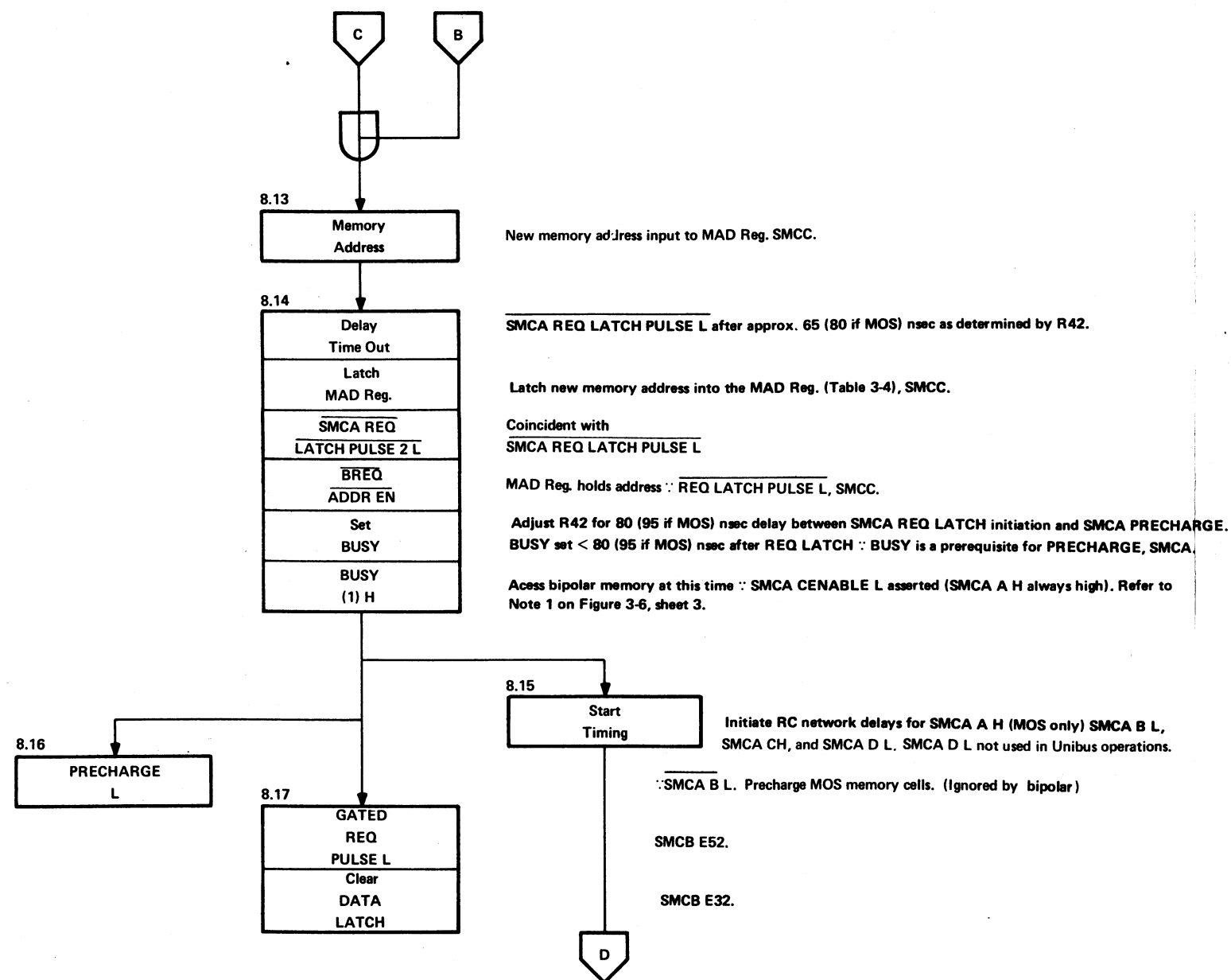


11-1297

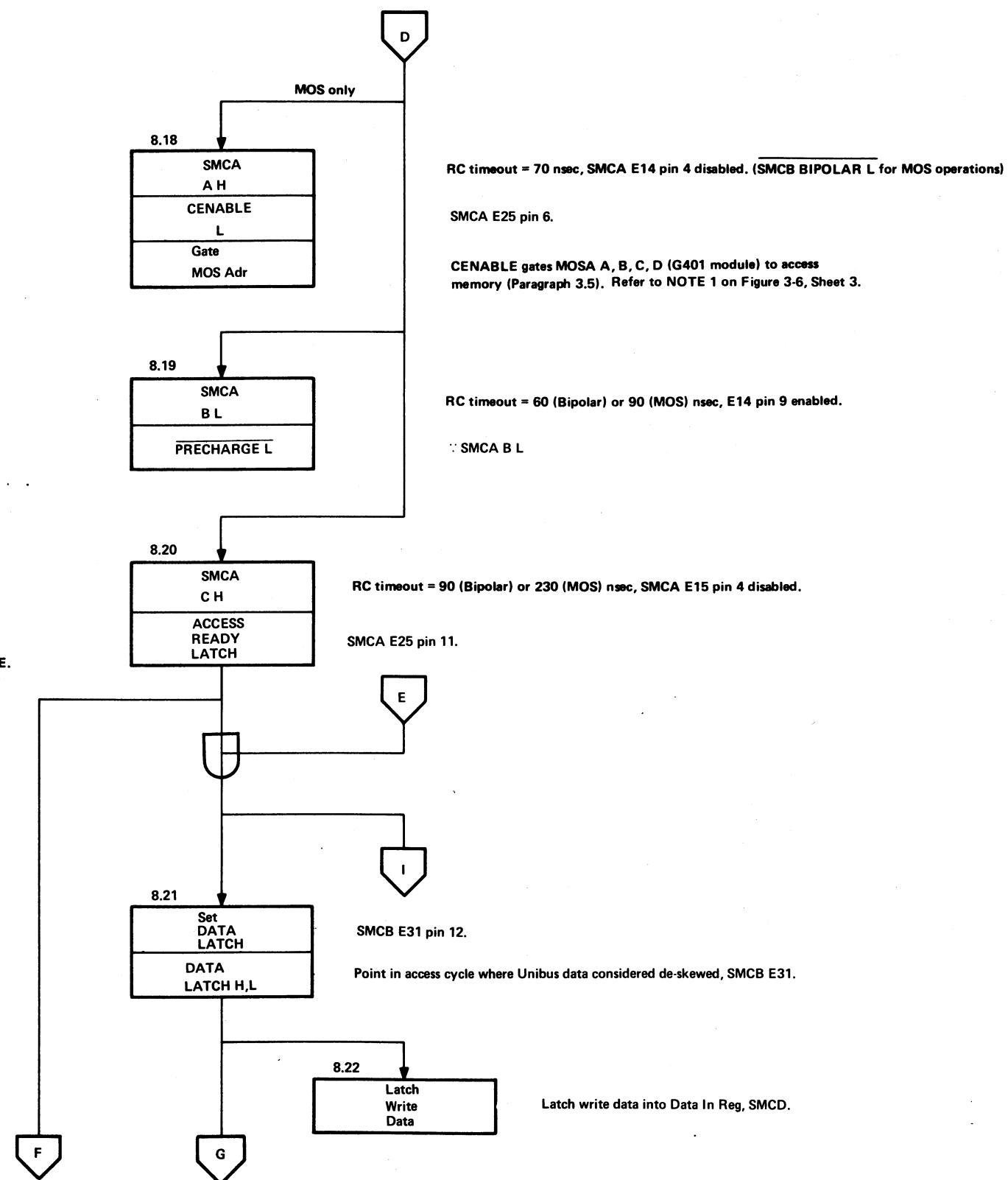


11-1298

Figure 3-6 Unibus DATO Logic Flow (Sheet 1 of 3)

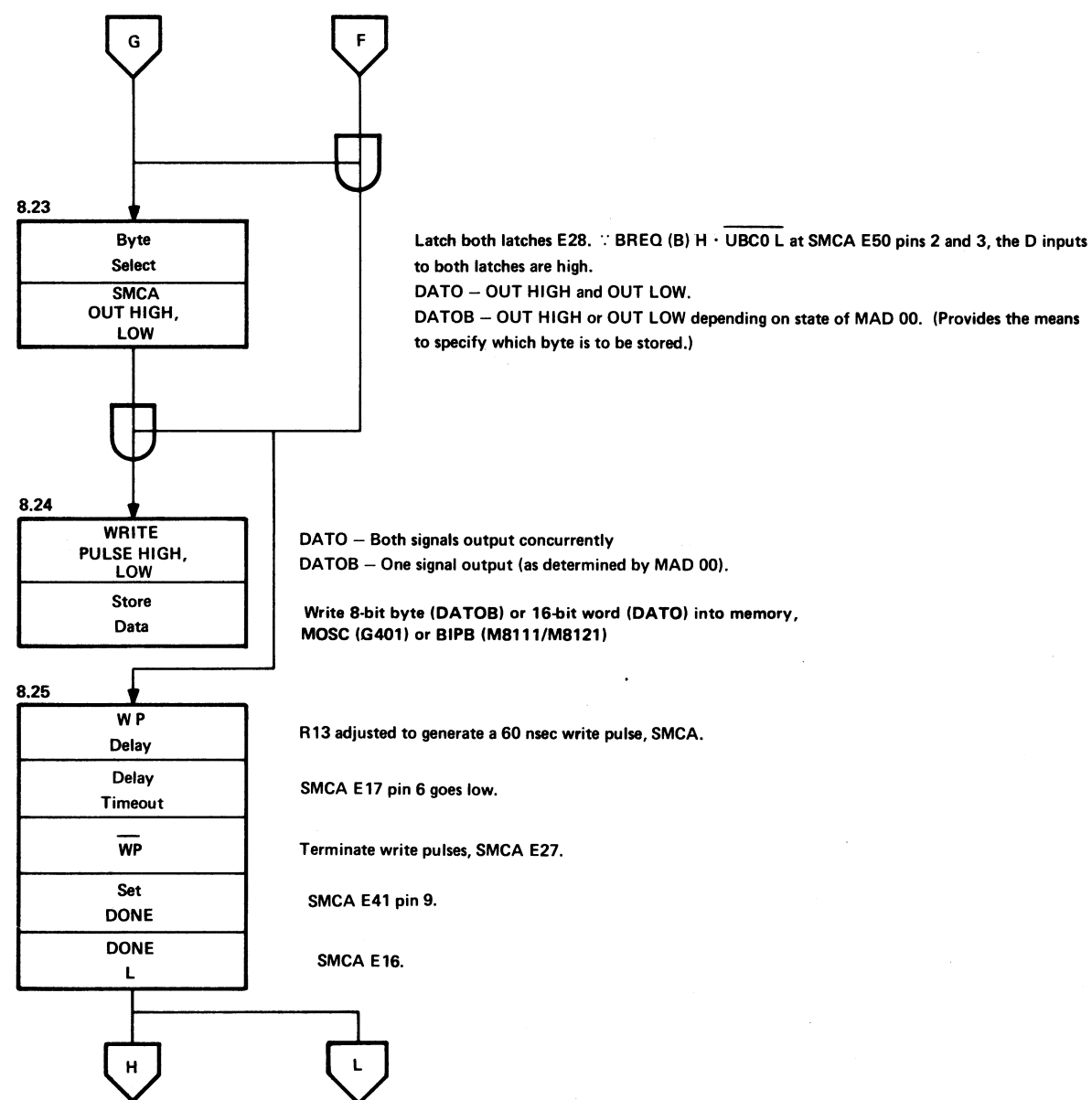


11-1299

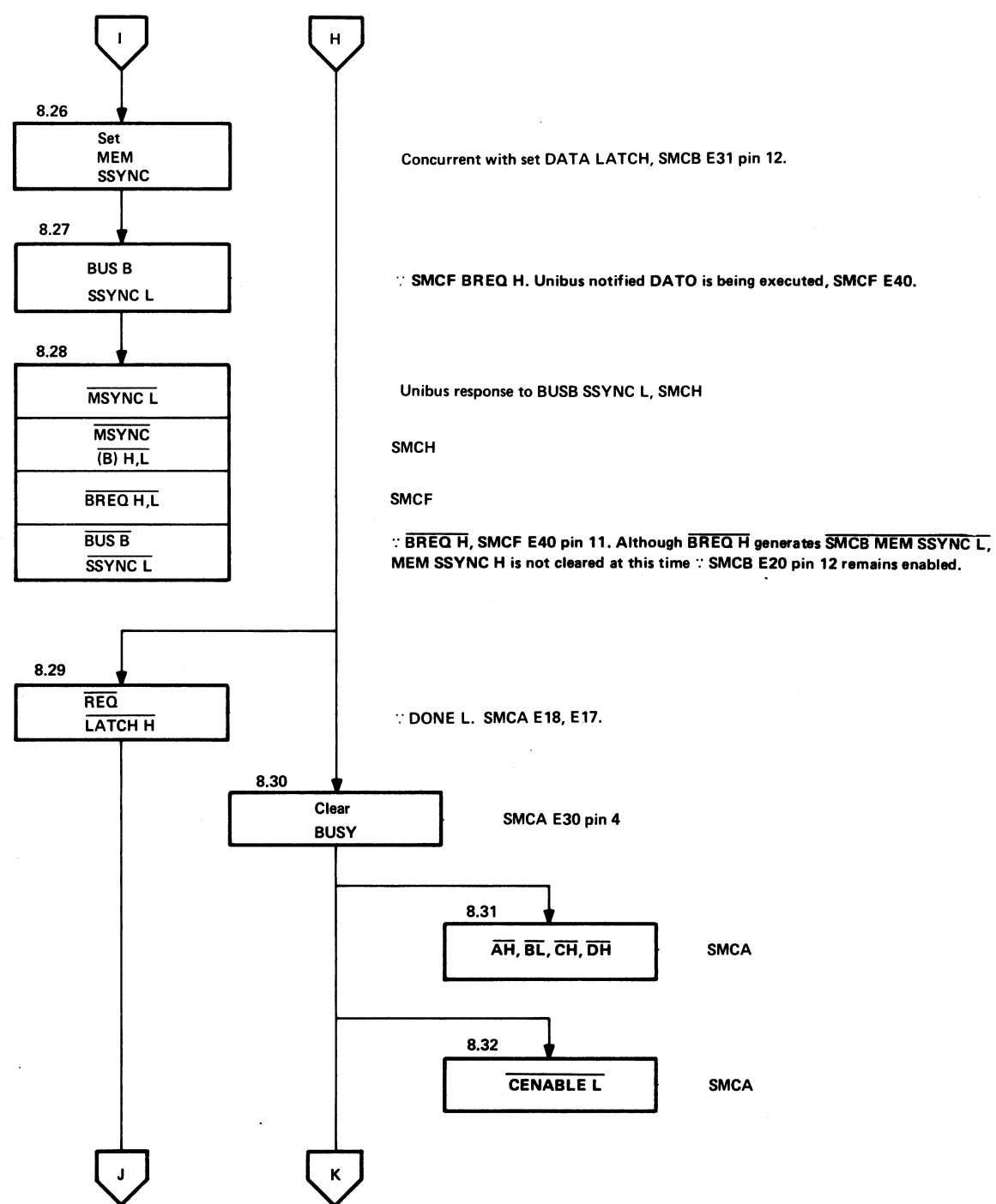


11-1300

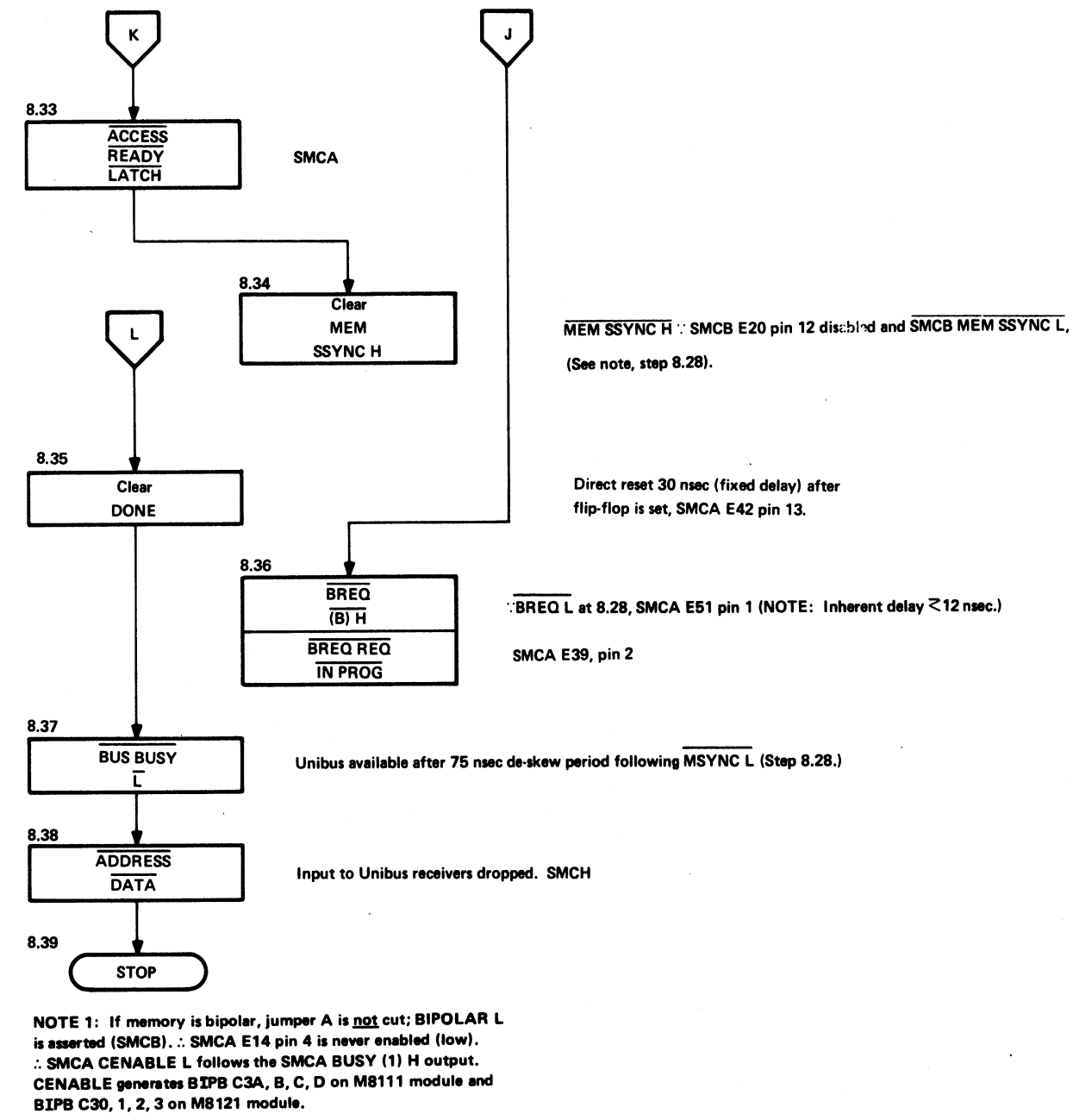
Figure 3-6 Unibus DATO Logic Flow (Sheet 2 of 3)



11-1301



11-1302



11-1303

Figure 3-6 Unibus DATO Logic Flow (Sheet 3 of 3)

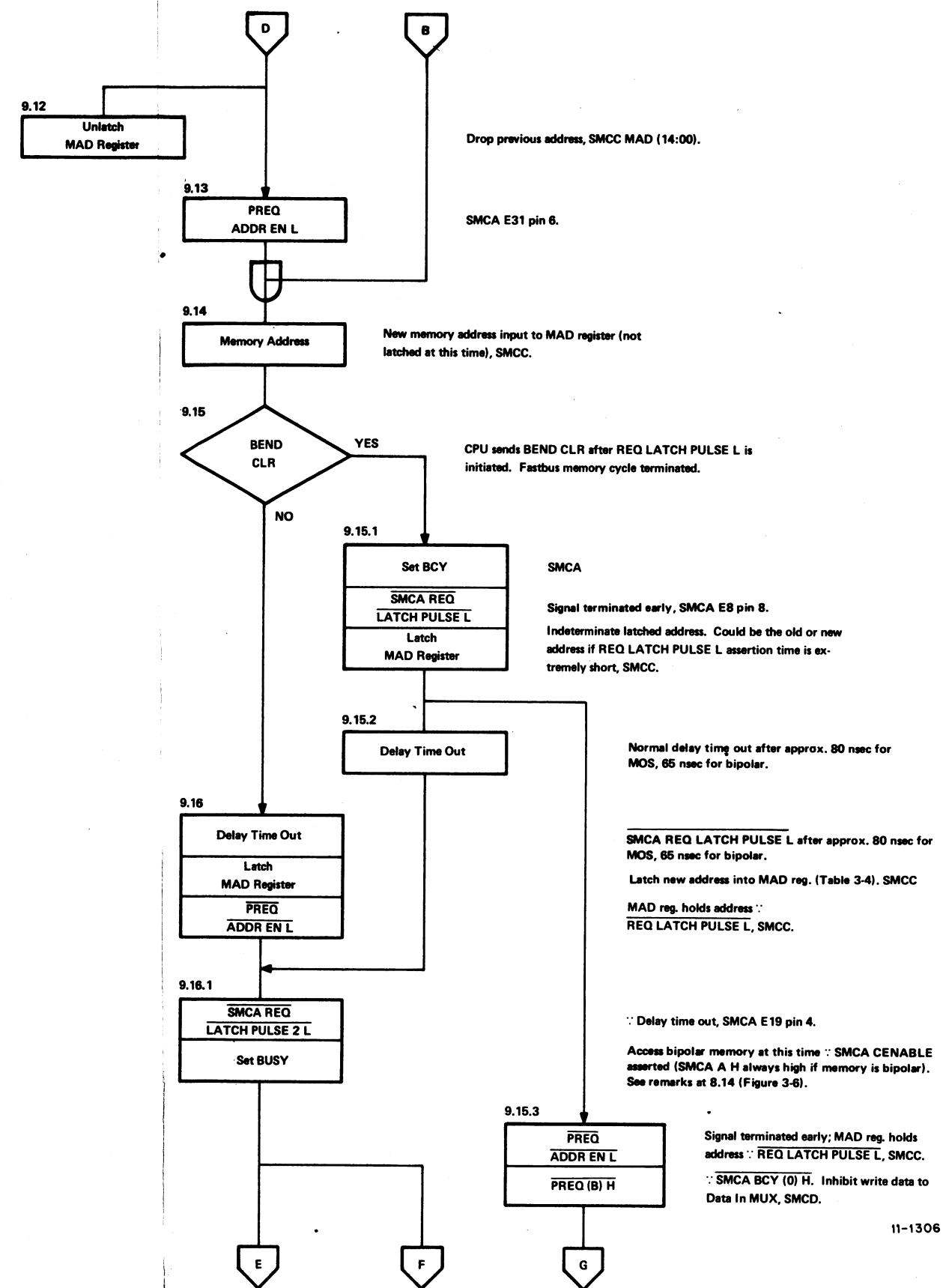
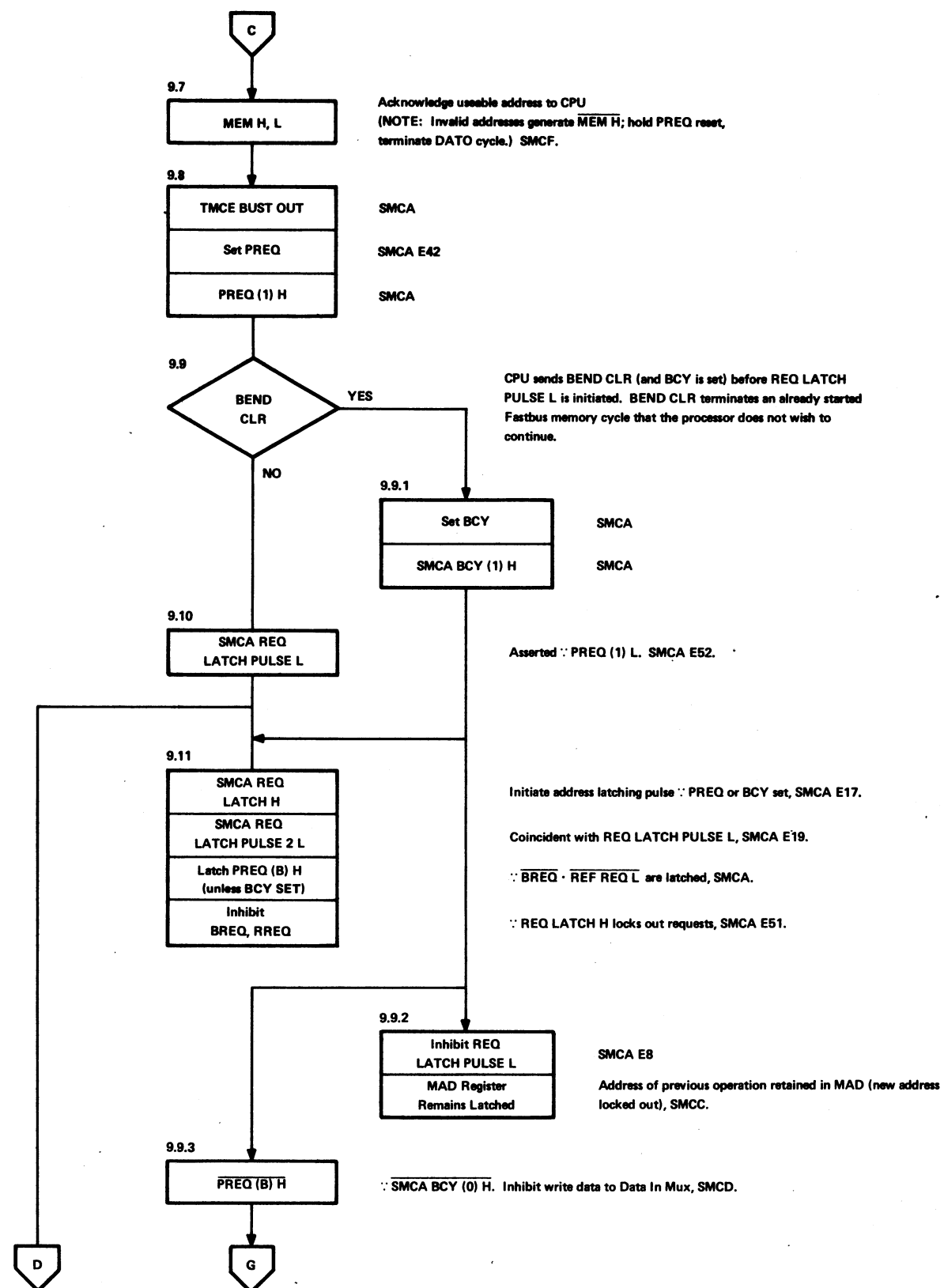
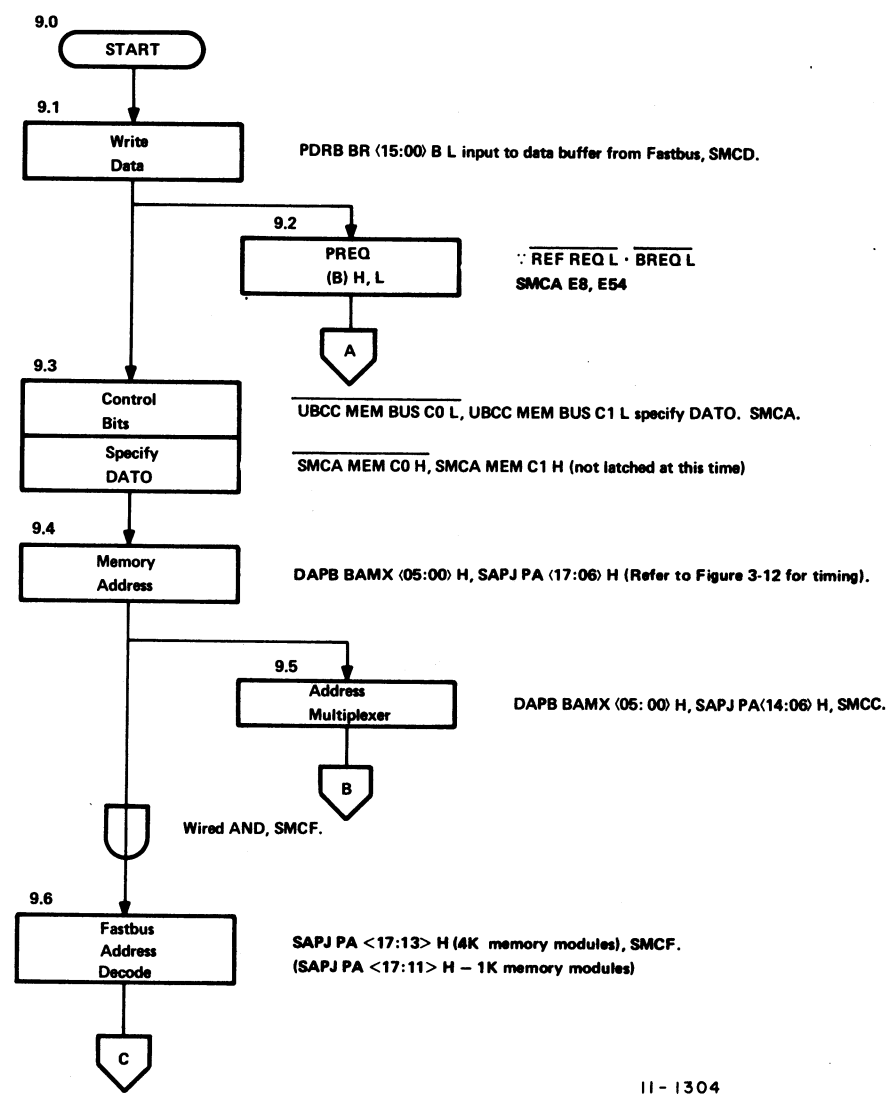
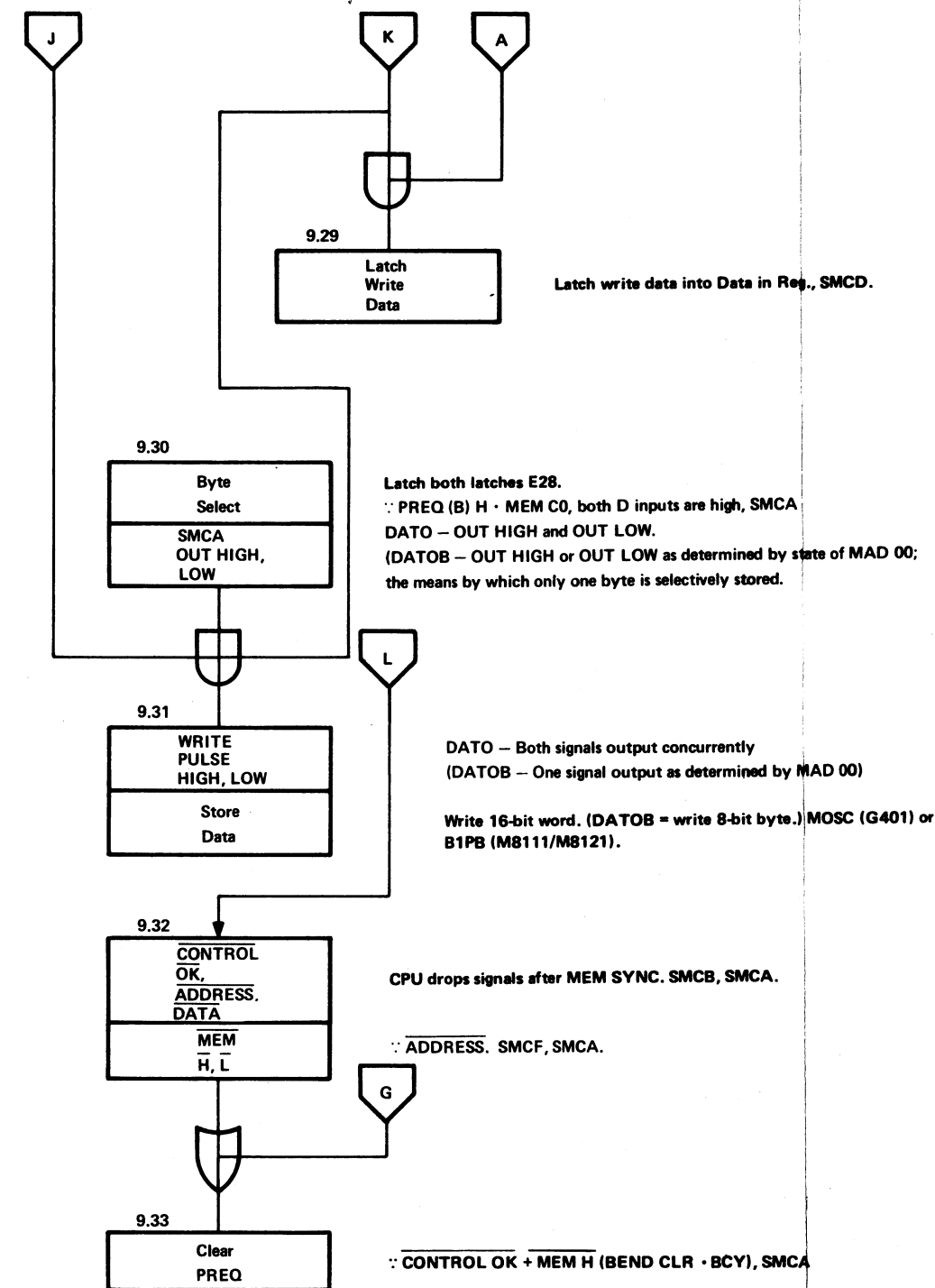
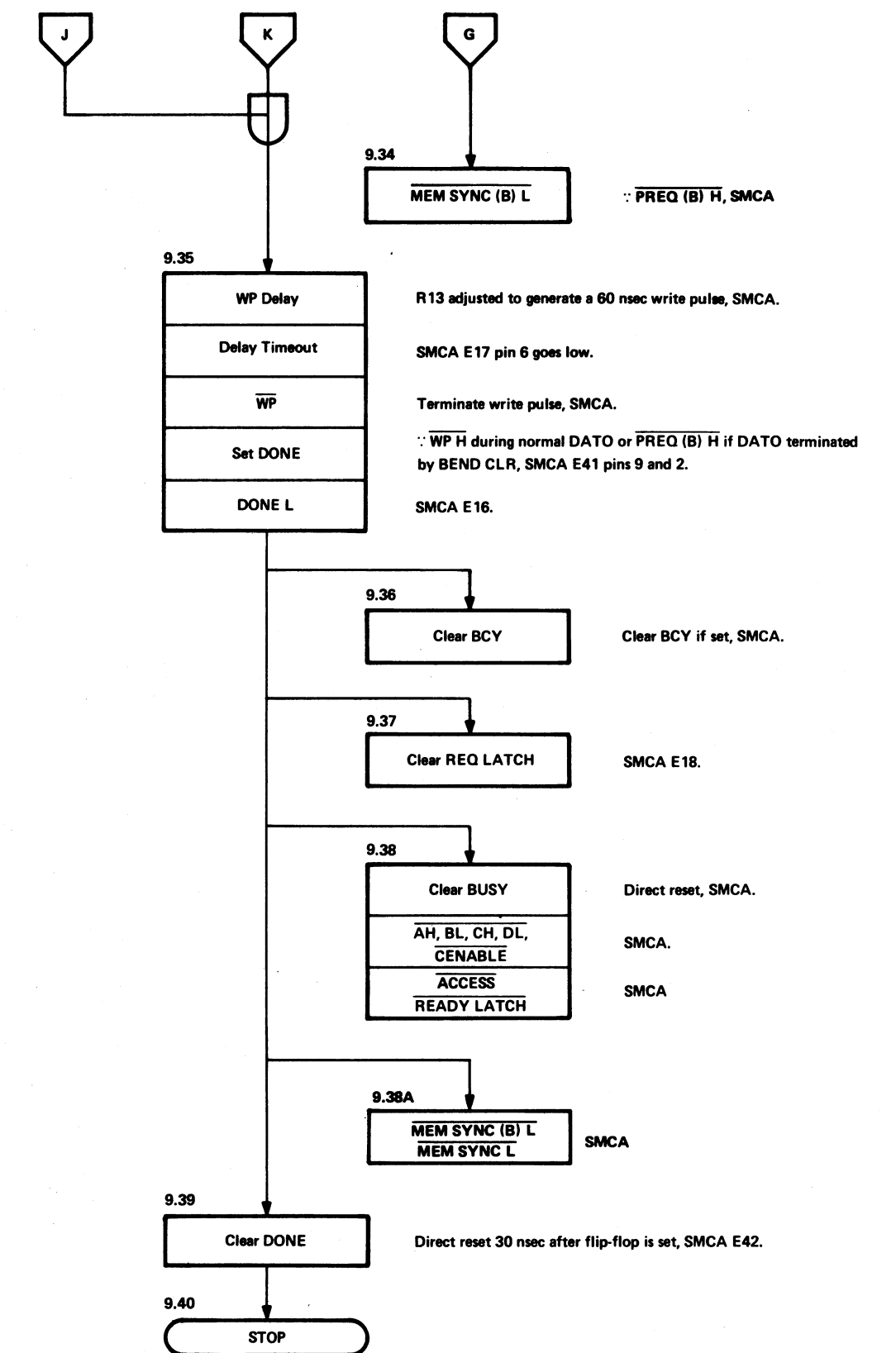


Figure 3-7 Fastbus DATO Logic Flow (Sheet 1 of 3)





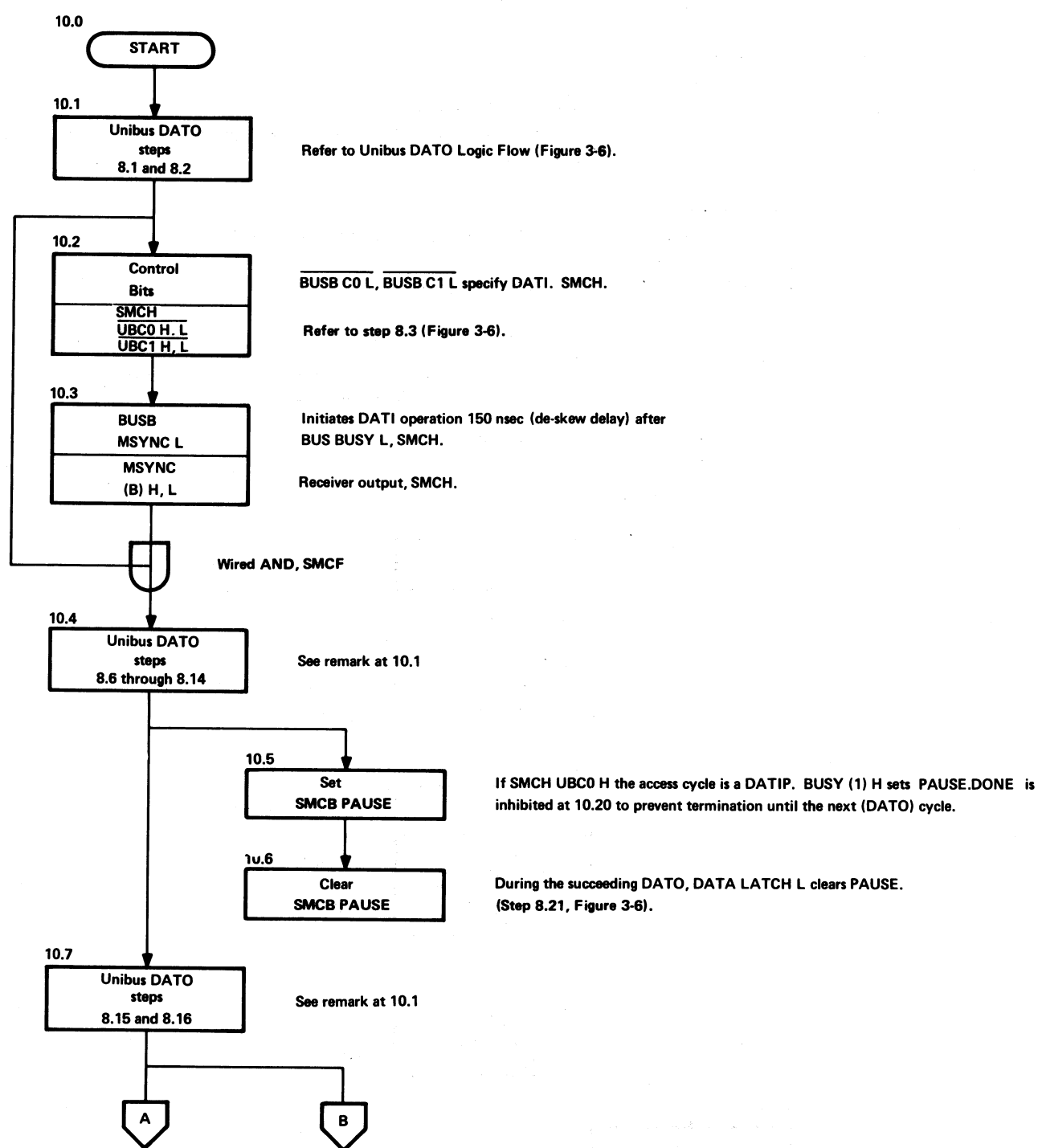
11-1309



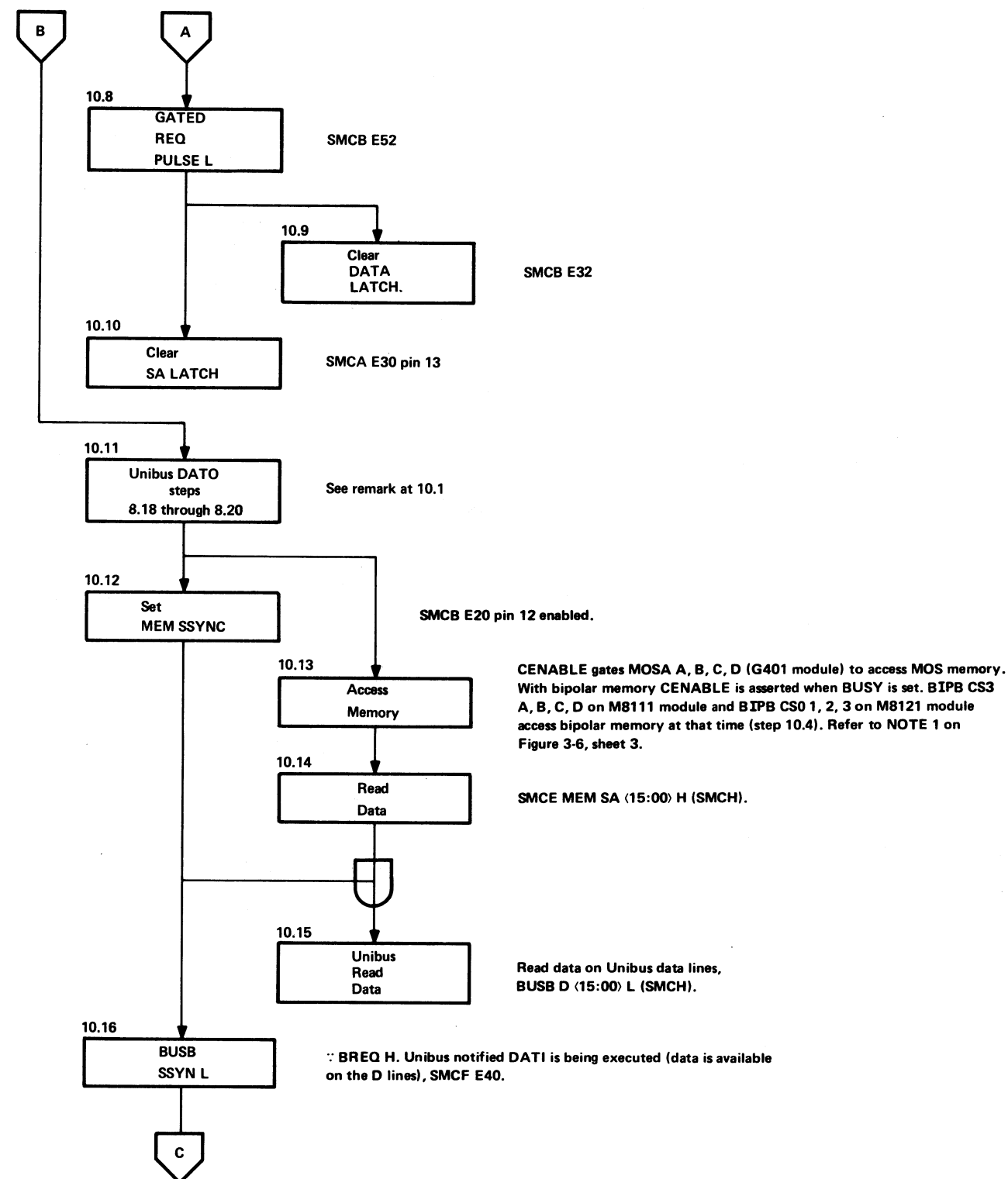
11-1310

Figure 3-7 Fastbus DATO Logic Flow (Sheet 3 of 3)

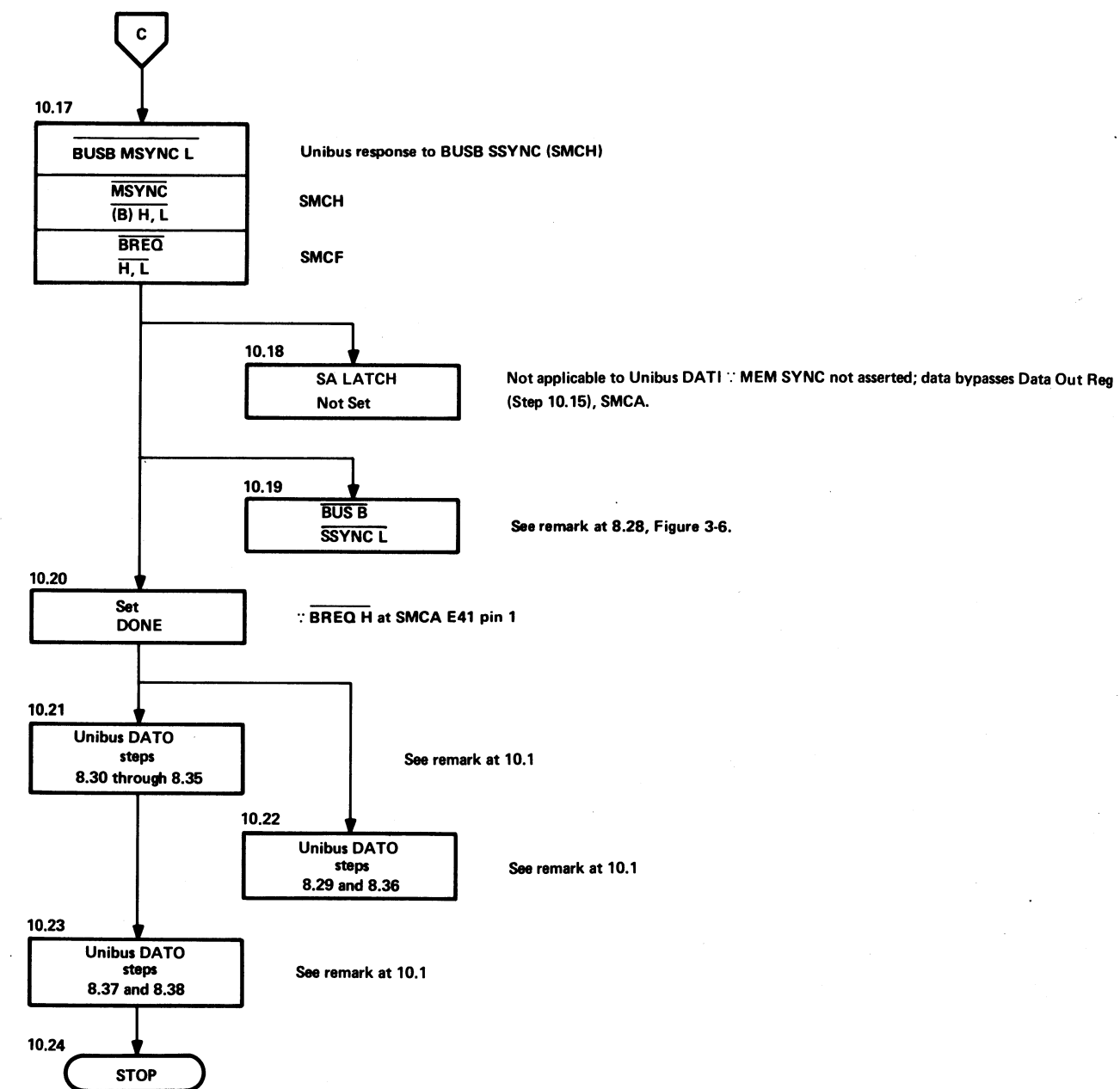




11-1311

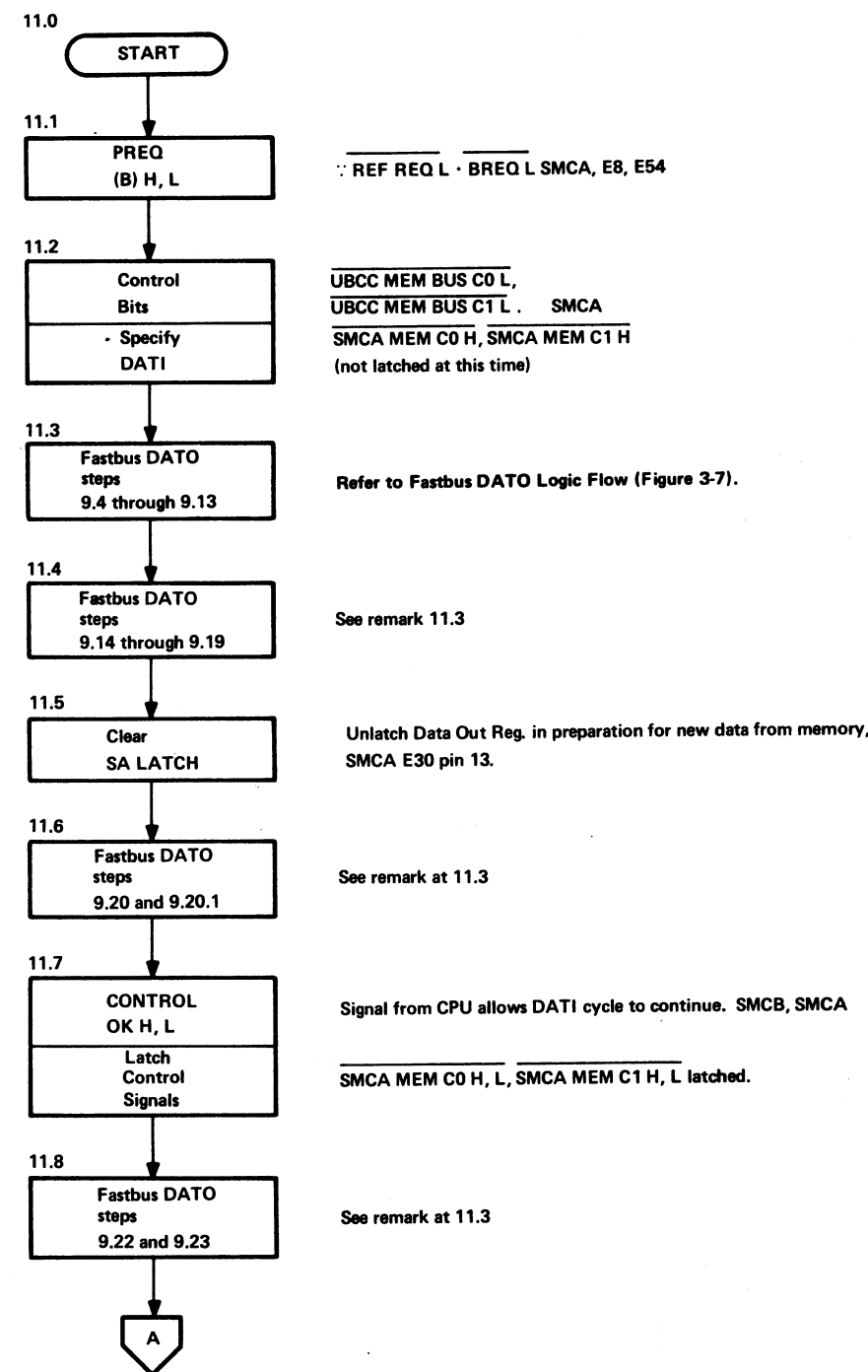


11-1312

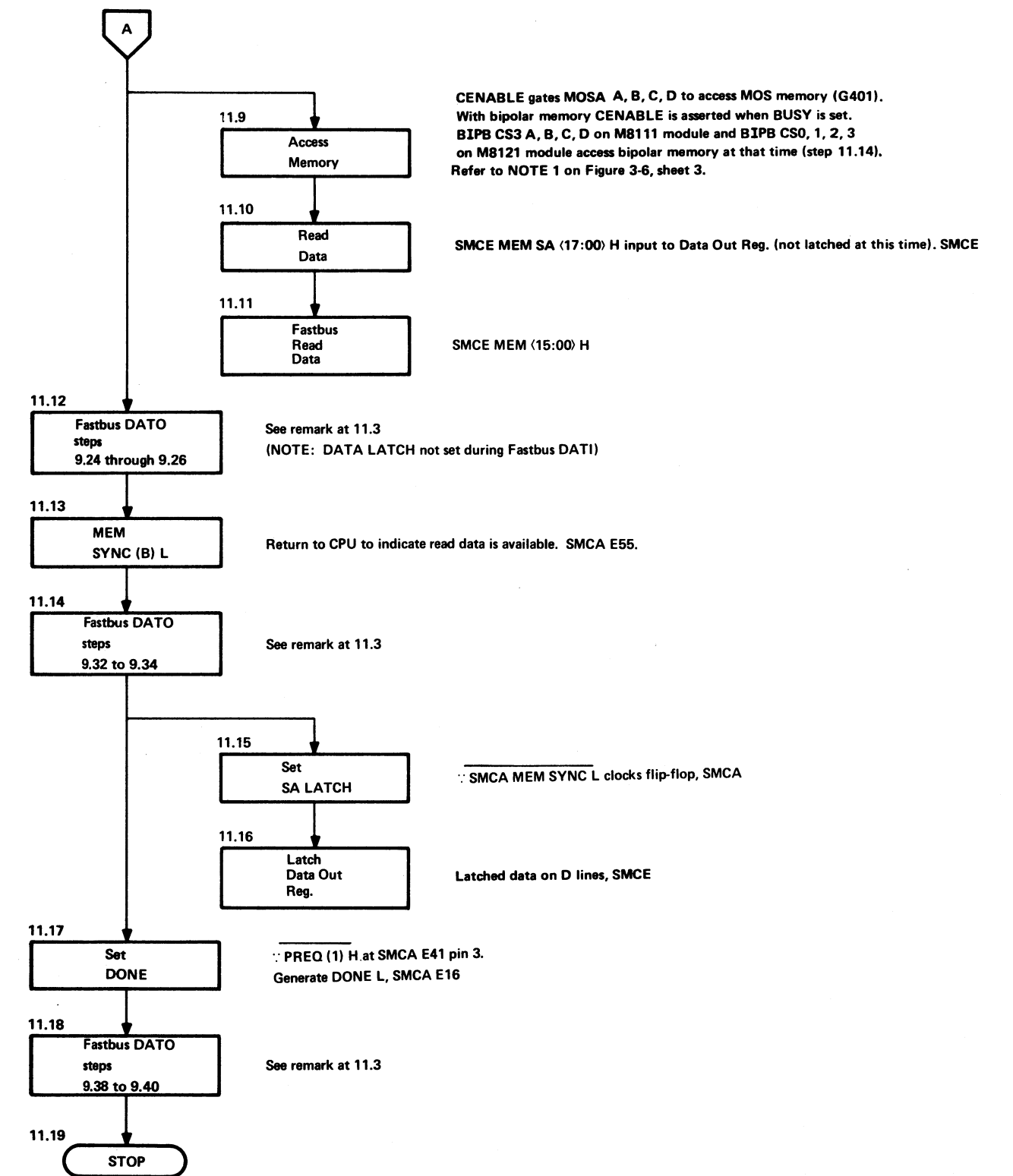


11-1313

Figure 3-8 Unibus DATI Logic Flow

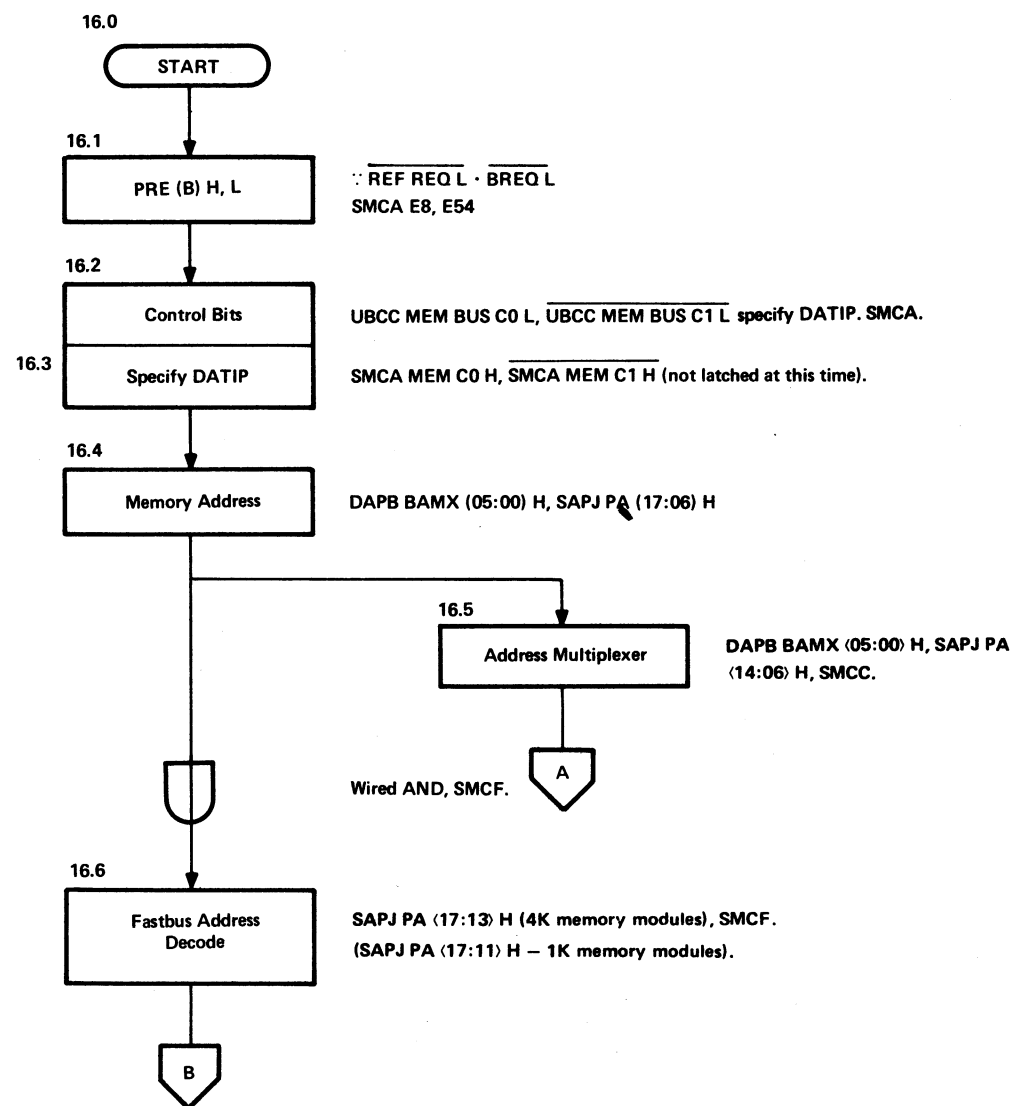


11-1314

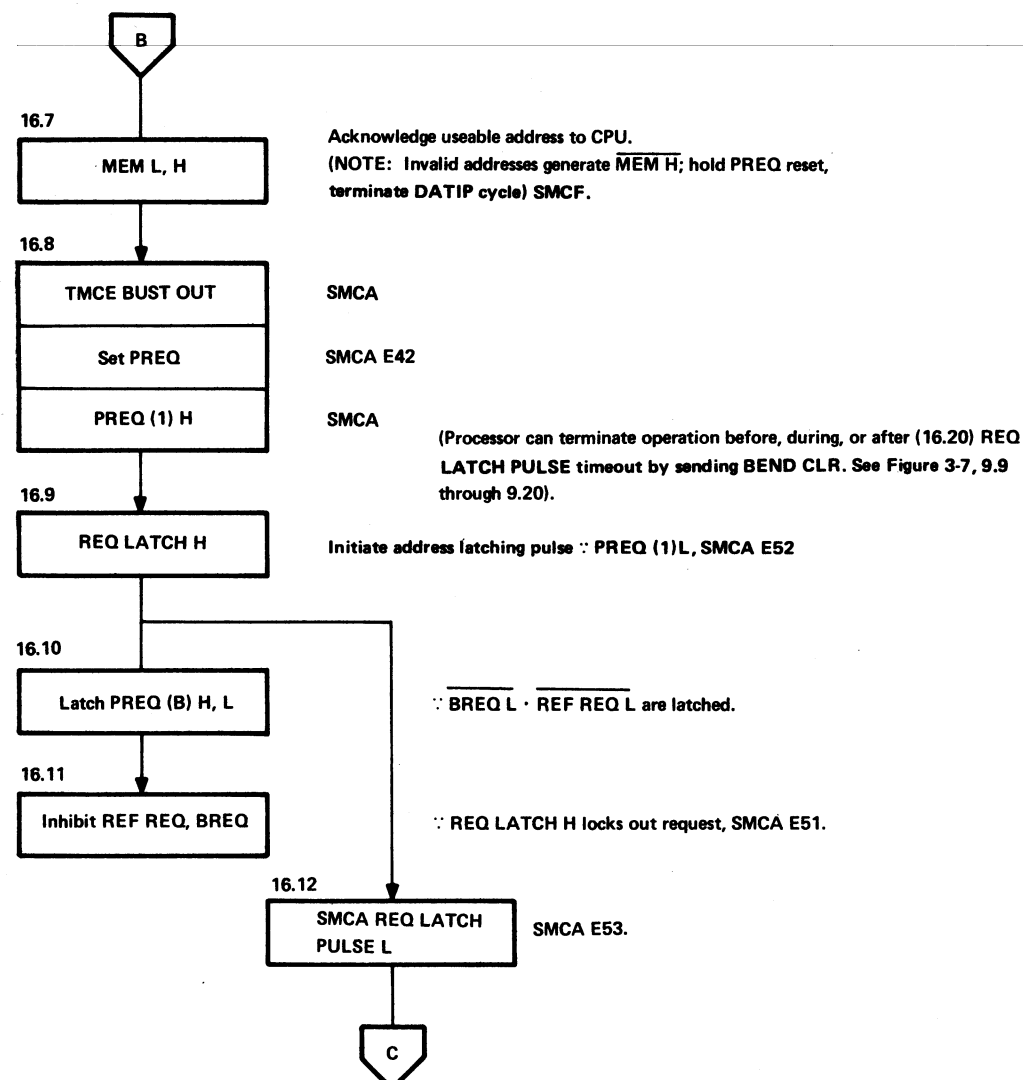


11-1315

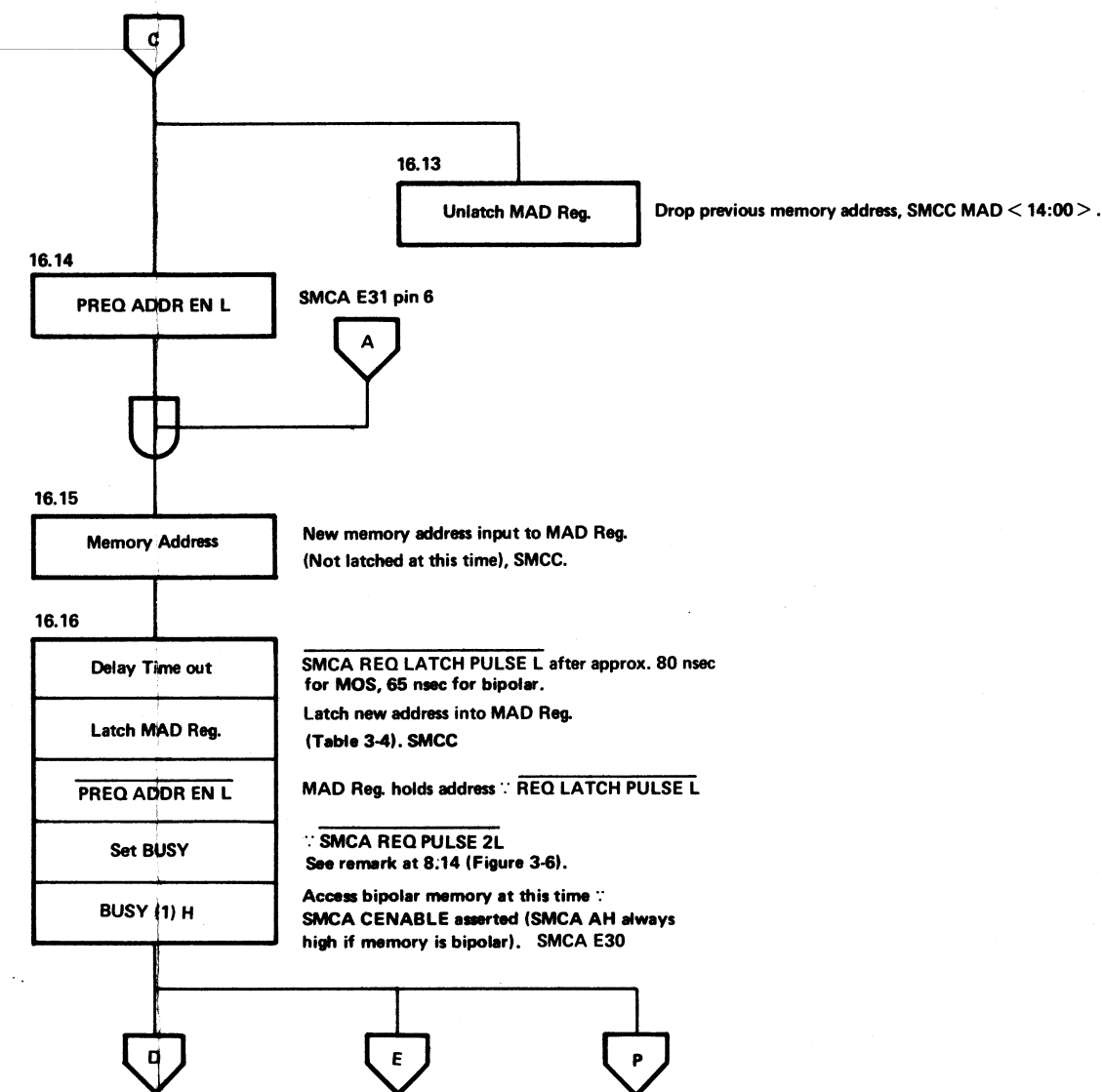
Figure 3-9 Fastbus DATI Logic Flow



11-2141

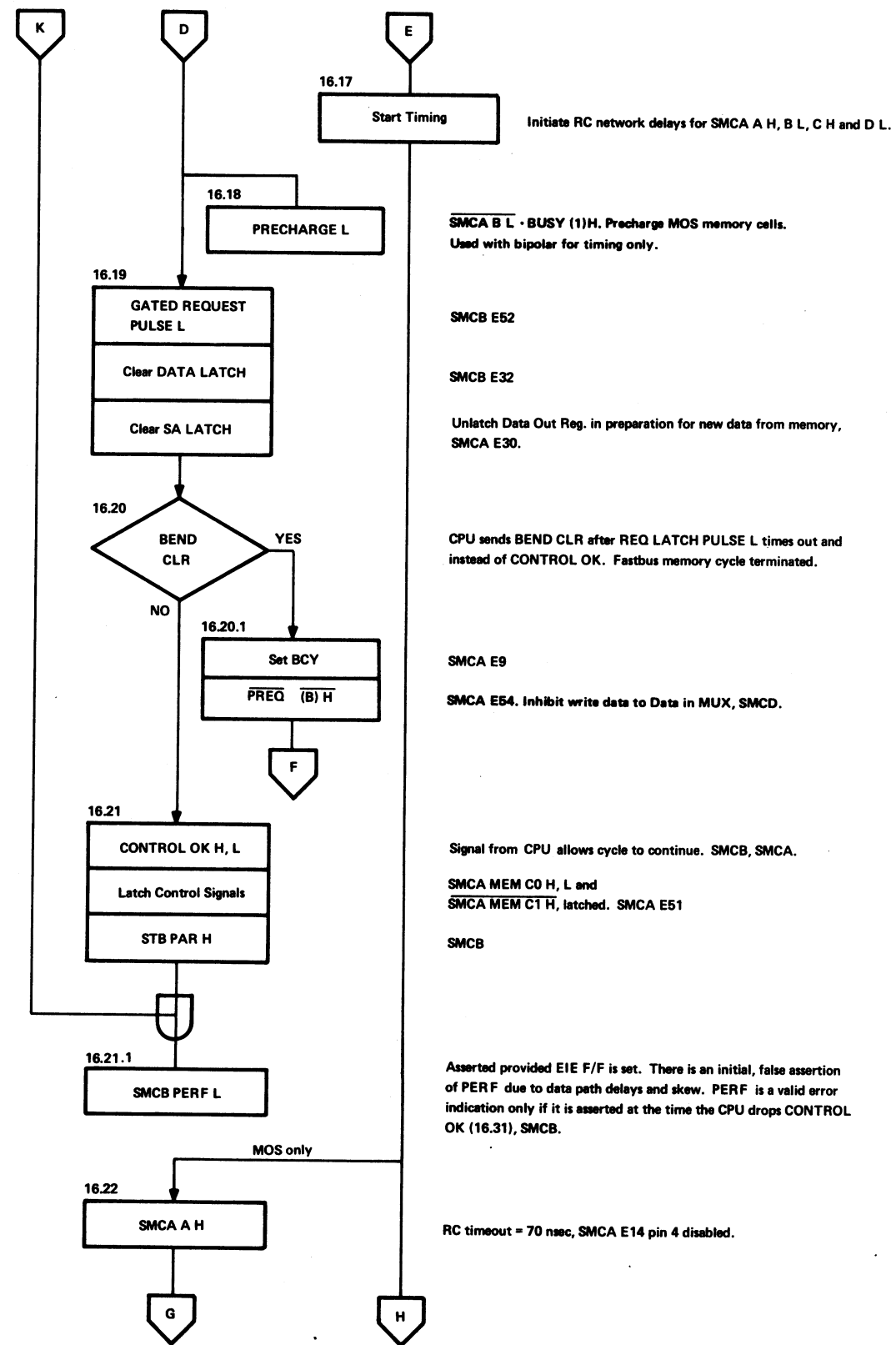


11-2175

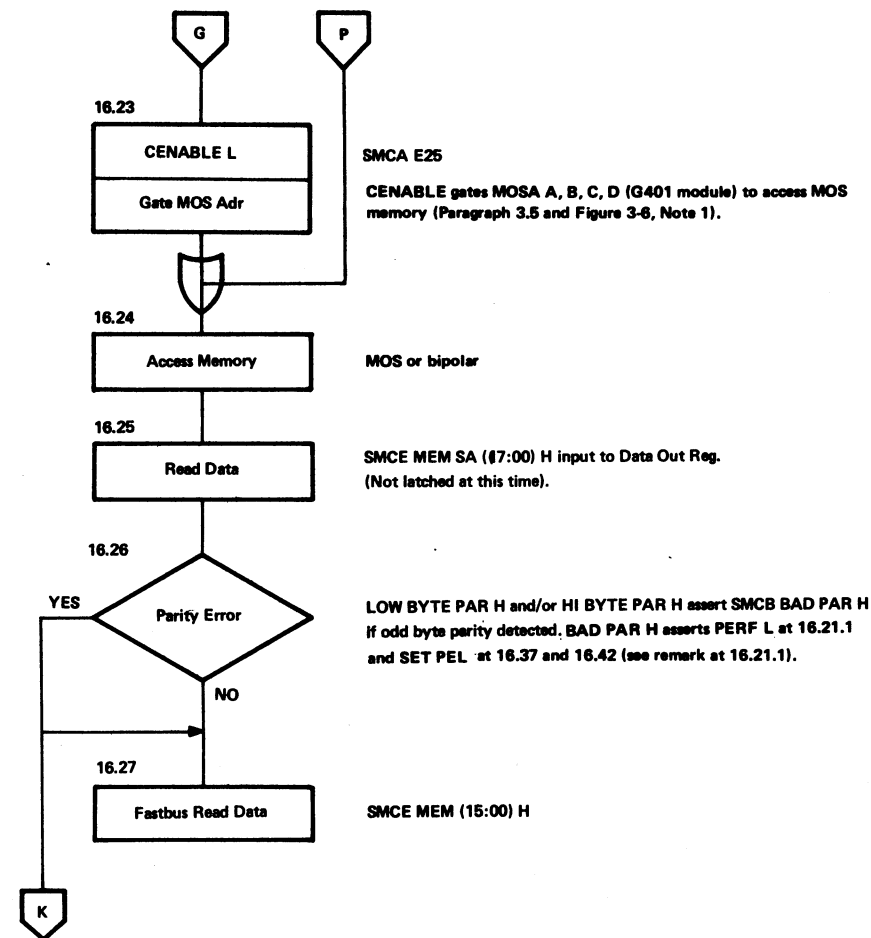


11-2176

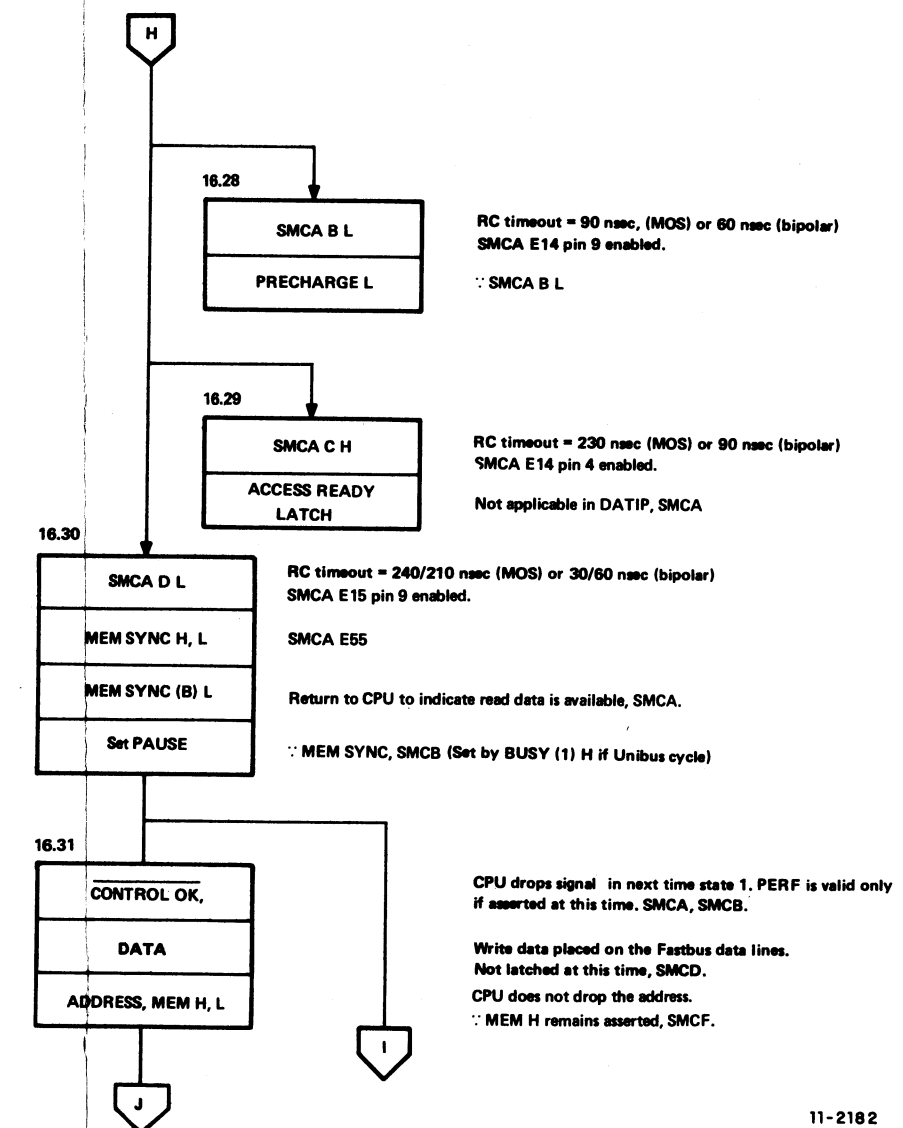
Figure 3-10 Fastbus DATI-DATO Logic Flow (Sheet 1 of 4)



11-2192

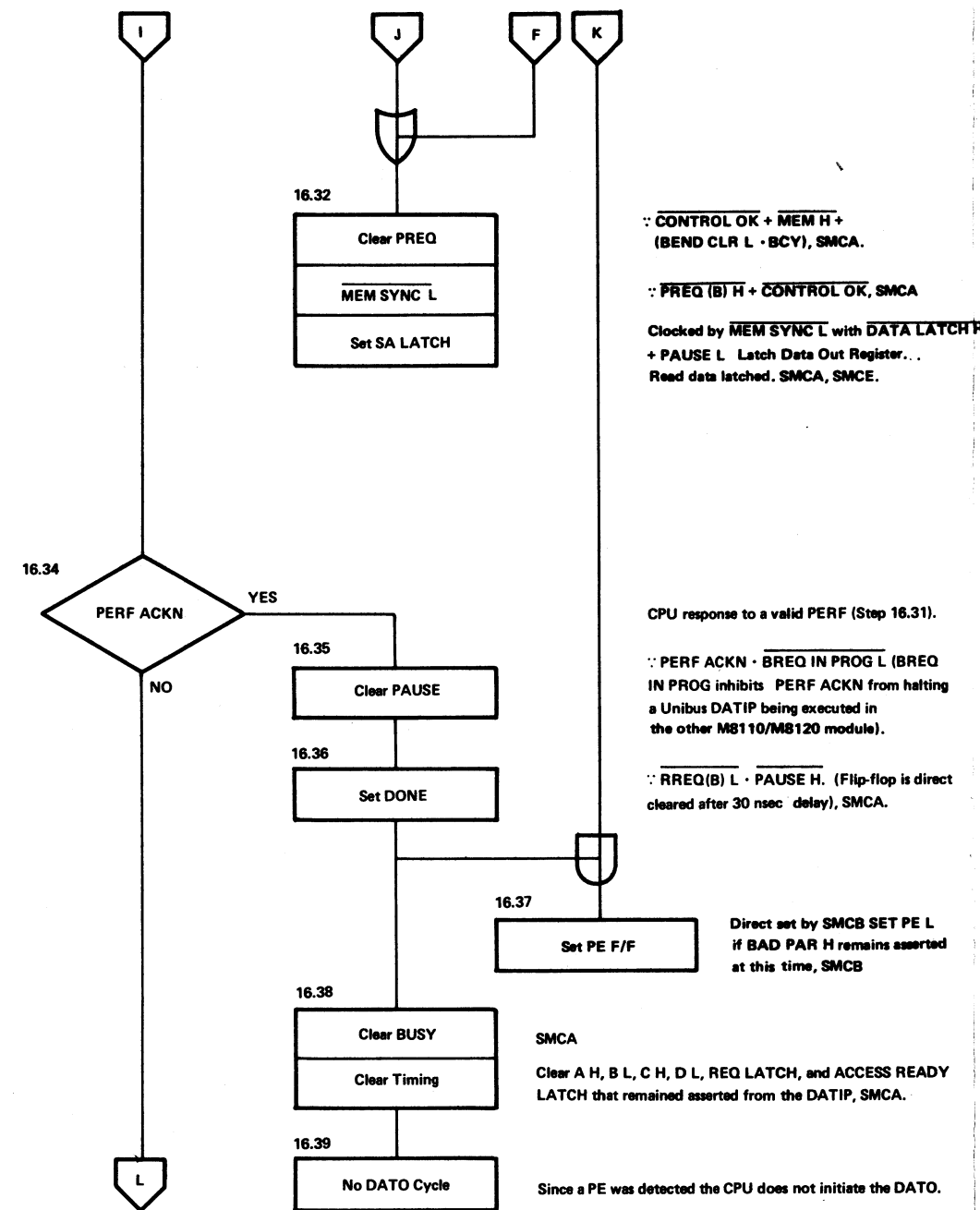


11-2245

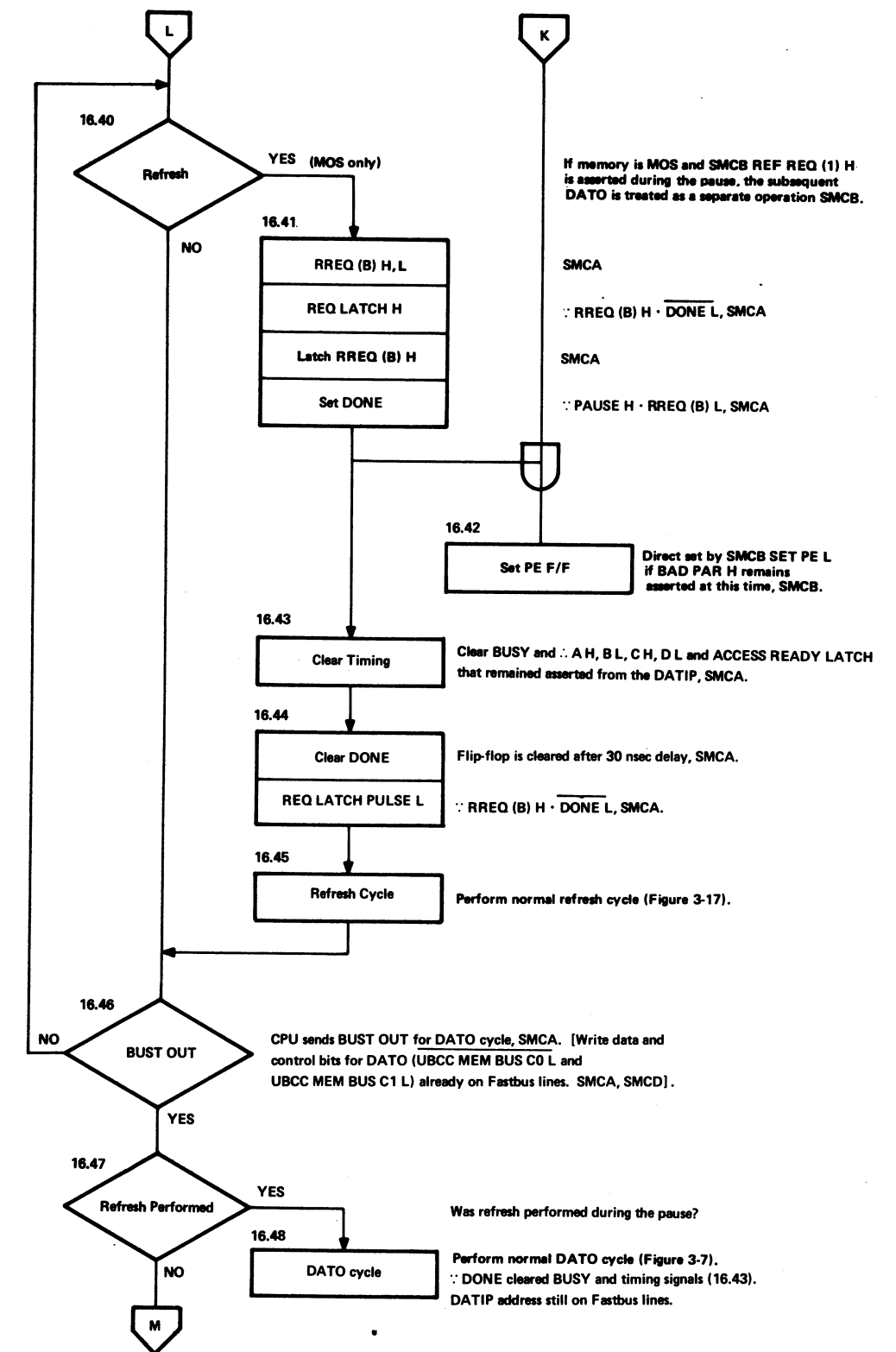


11-2182

Figure 3-10 Fastbus DATI-DATO Logic Flow (Sheet 2 of 4)



11-2183



11-2189

Figure 3-10 Fastbus DATI-DATO Logic Flow (Sheet 3 of 4)

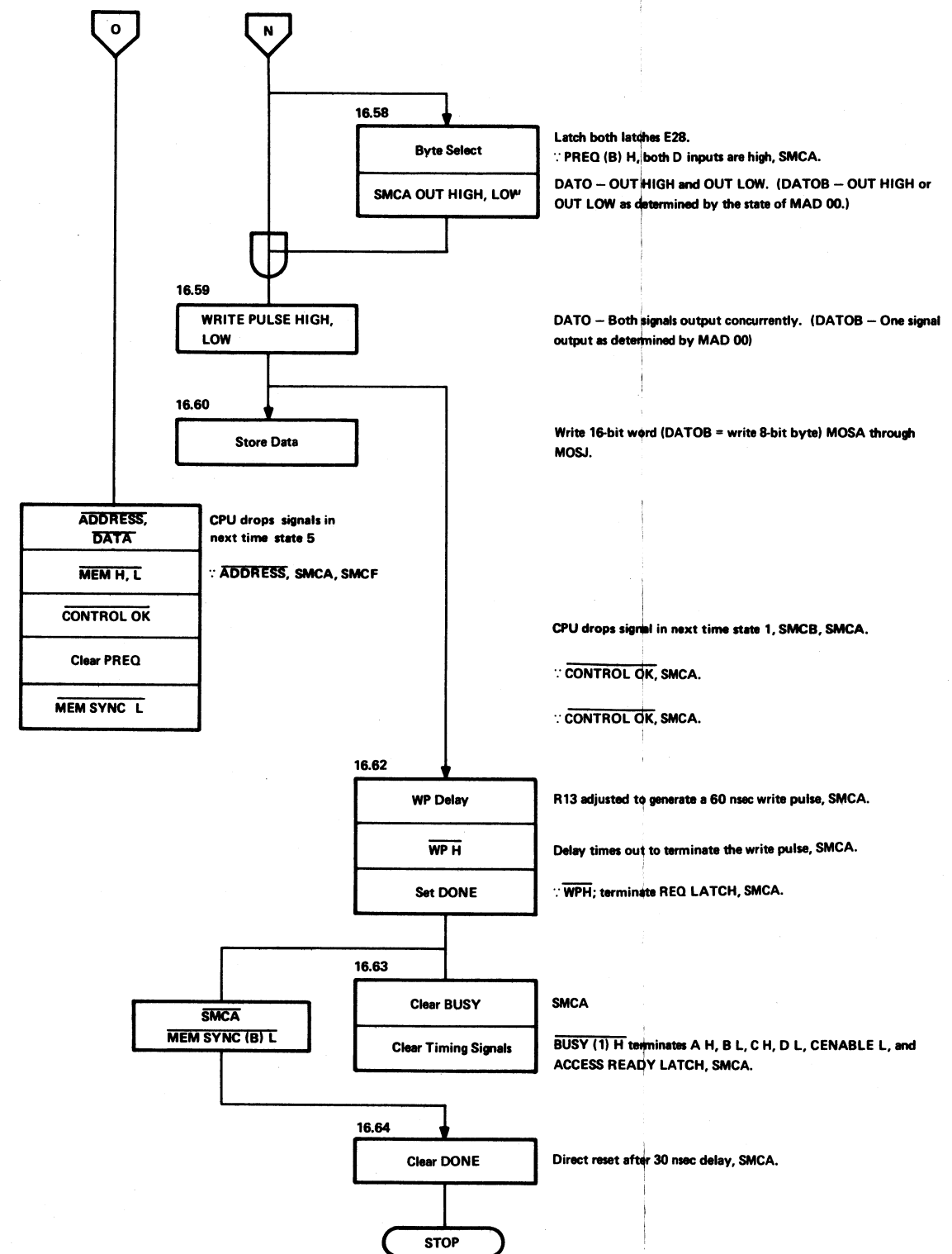
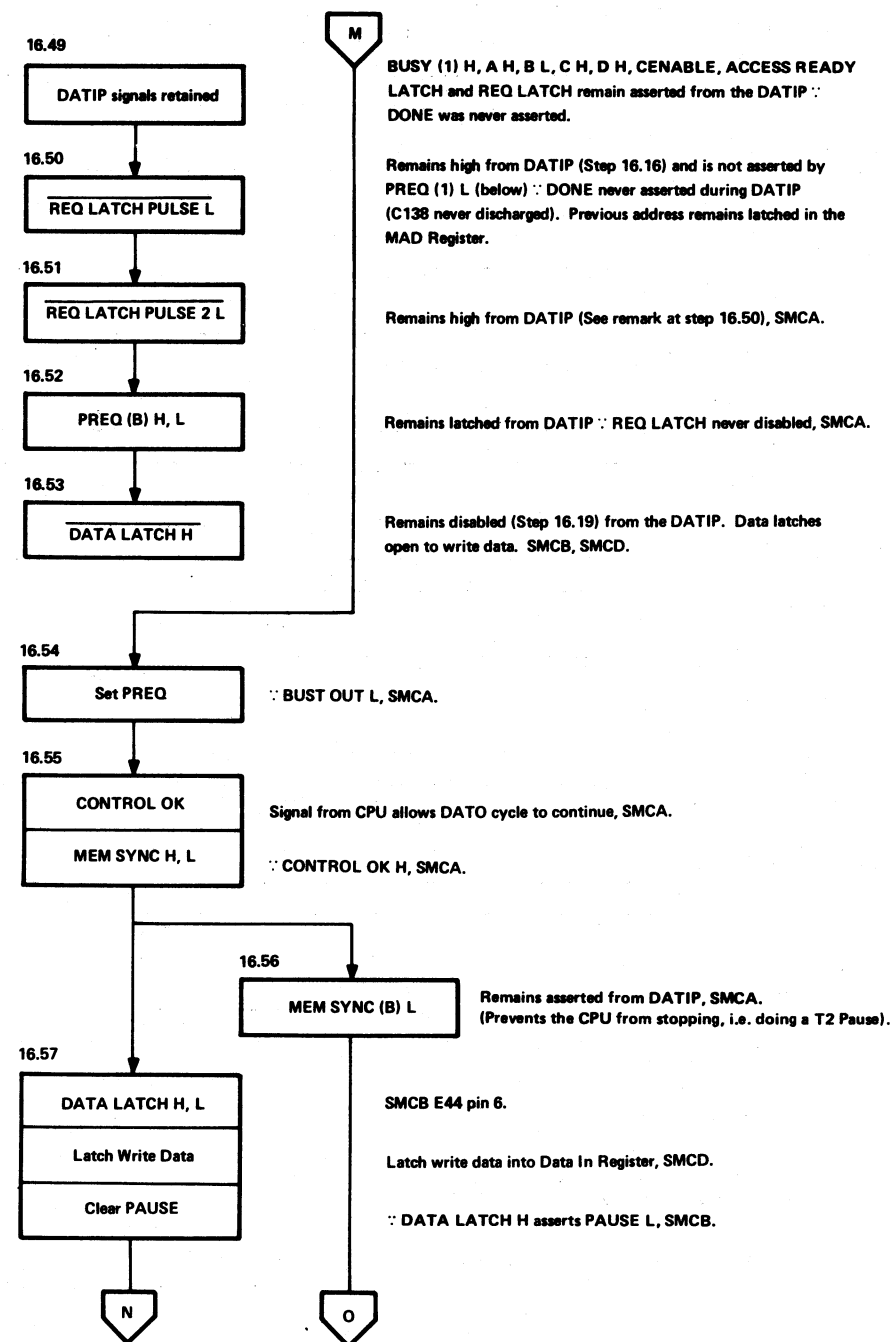


Figure 3-10 Fastbus DATI-DATO Logic Flow (Sheet 4 of 4)

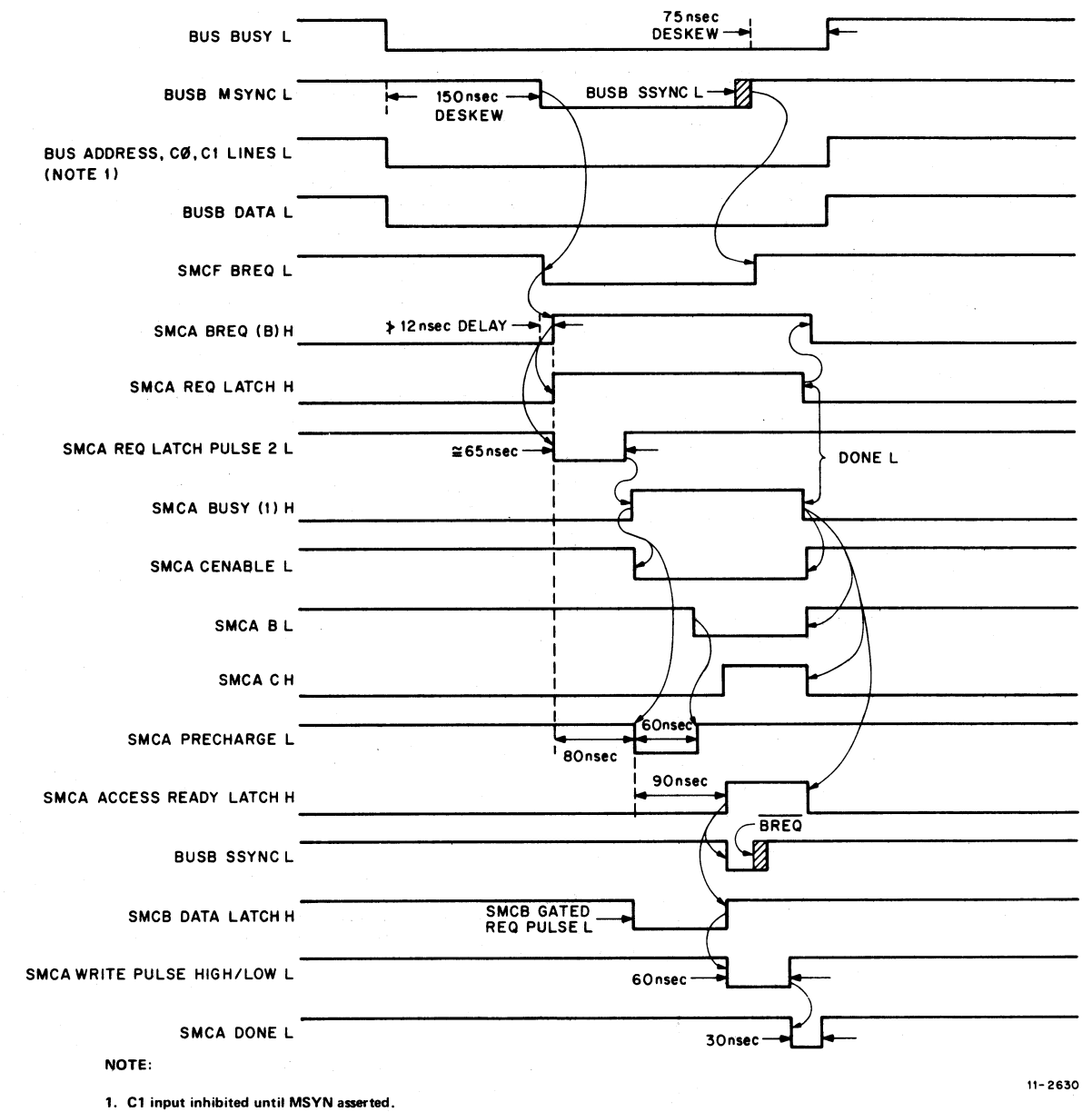
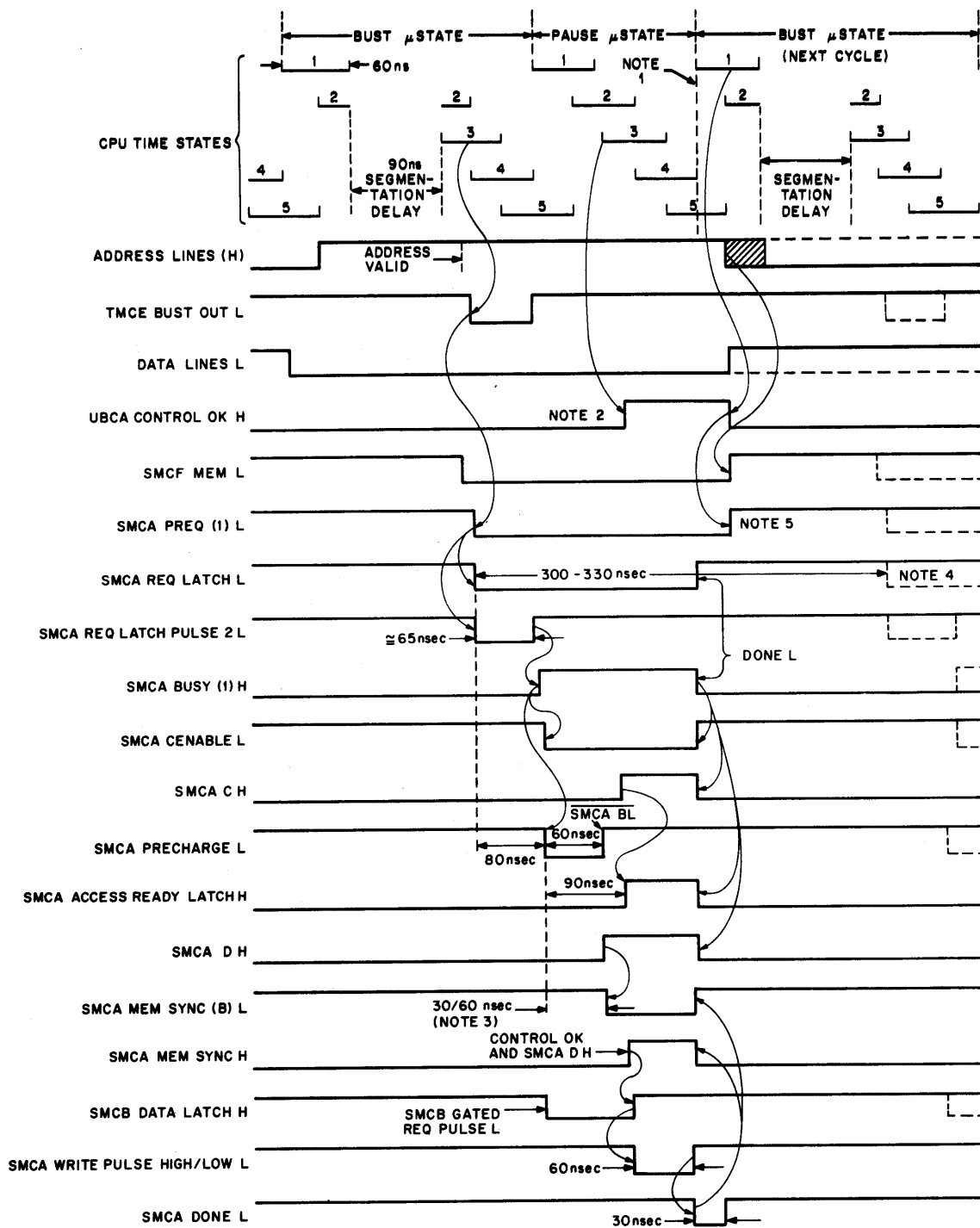


Figure 3-11 Unibus DATO Timing (Bipolar)



NOTES:

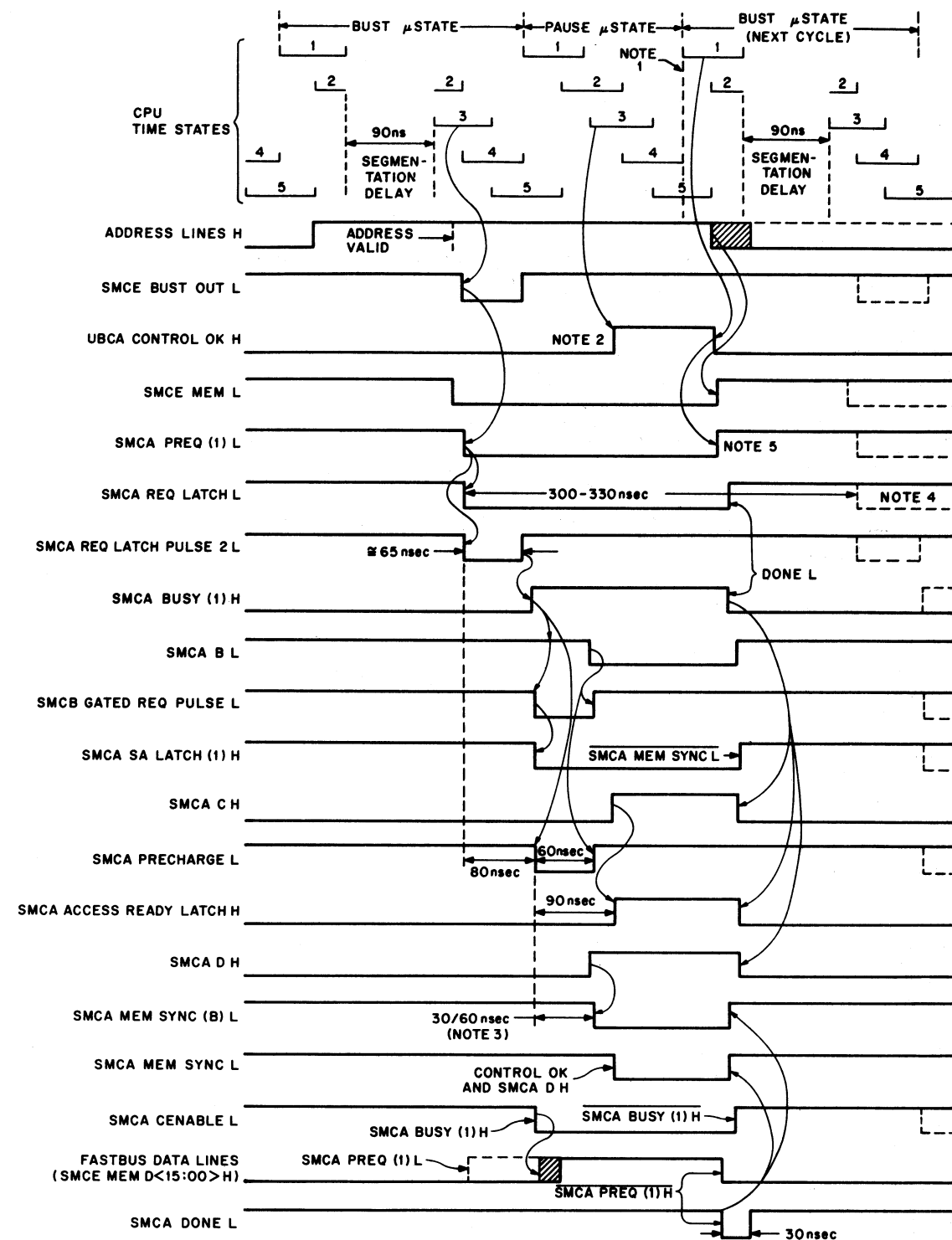
1. CPU timing may stop in time state 5 for 30 nsec if MEM SYNC is not stable on TIG board.
2. CPU may send BEND CLEAR in place of CONTROL OK. See Figure 3-7 (9.9, 9.15 and 9.20).
3. REV 60 nsec if M8109 jumper W5 out, W6 in.  
F 30 nsec if M8109 jumper W5 in, W6 out.  
  
REV 60 nsec if flip-flop at E8 (M8109) not used.  
C 30 nsec if flip-flop at E8 (M8109) has jumpers at pins 11 and 12.
4. Adjust R42 for 300 to 330 nsec between cycles (represented by dotted lines). Refer to Paragraph 4.3.2.2.
5. Cleared either by CONTROL OK or MEM L

11-3629

Figure 3-12 Fastbus DATO Timing (Bipolar)





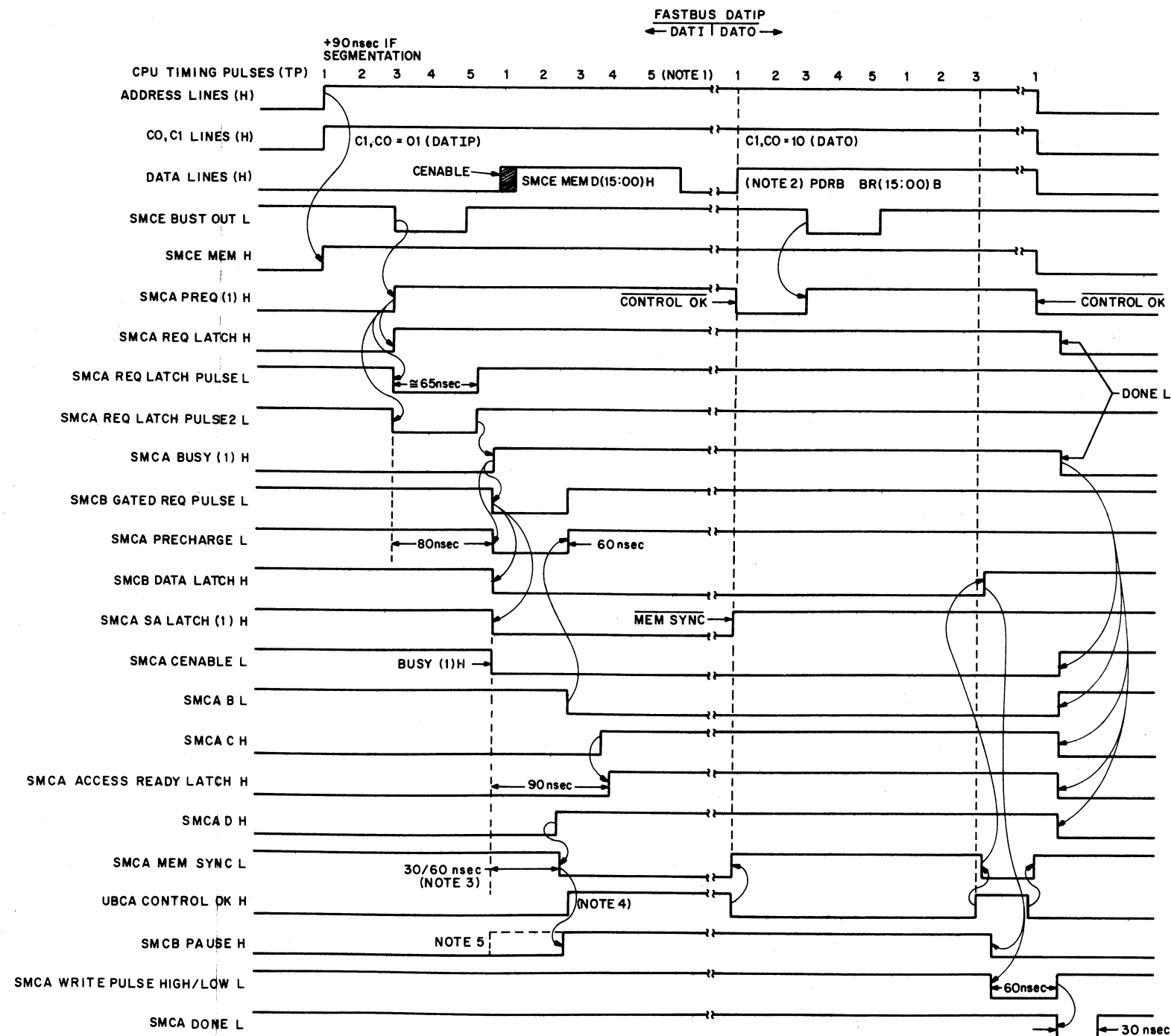


NOTES:

1. CPU timing may stop for 30 nsec in time state 5 if MEM SYNC is not stable on TIG board.
2. CPU may send BEND CLEAR in place of CONTROL OK. See Figure 3-7 (9.9, 9.15 and 9.20).
3. REV { 60 nsec if M8109 jumper W5 out, W6 in.  
F { 30 nsec if M8109 jumper W5 in, W6 out.  
REV { 60 nsec if flip flop at E8 (M8109) not used.  
C { 30 nsec if flip flop at E8 (M8109) has jumpers at pins 11 and 12.
4. Adjust R42 for 300 to 330 nsec between cycles (represented by dotted lines). Refer to Paragraph 4.3.2.2.
5. Cleared either by CONTROL OK or MEM L

11-3627

Figure 3-14 Fastbus DATI Timing (Bipolar)

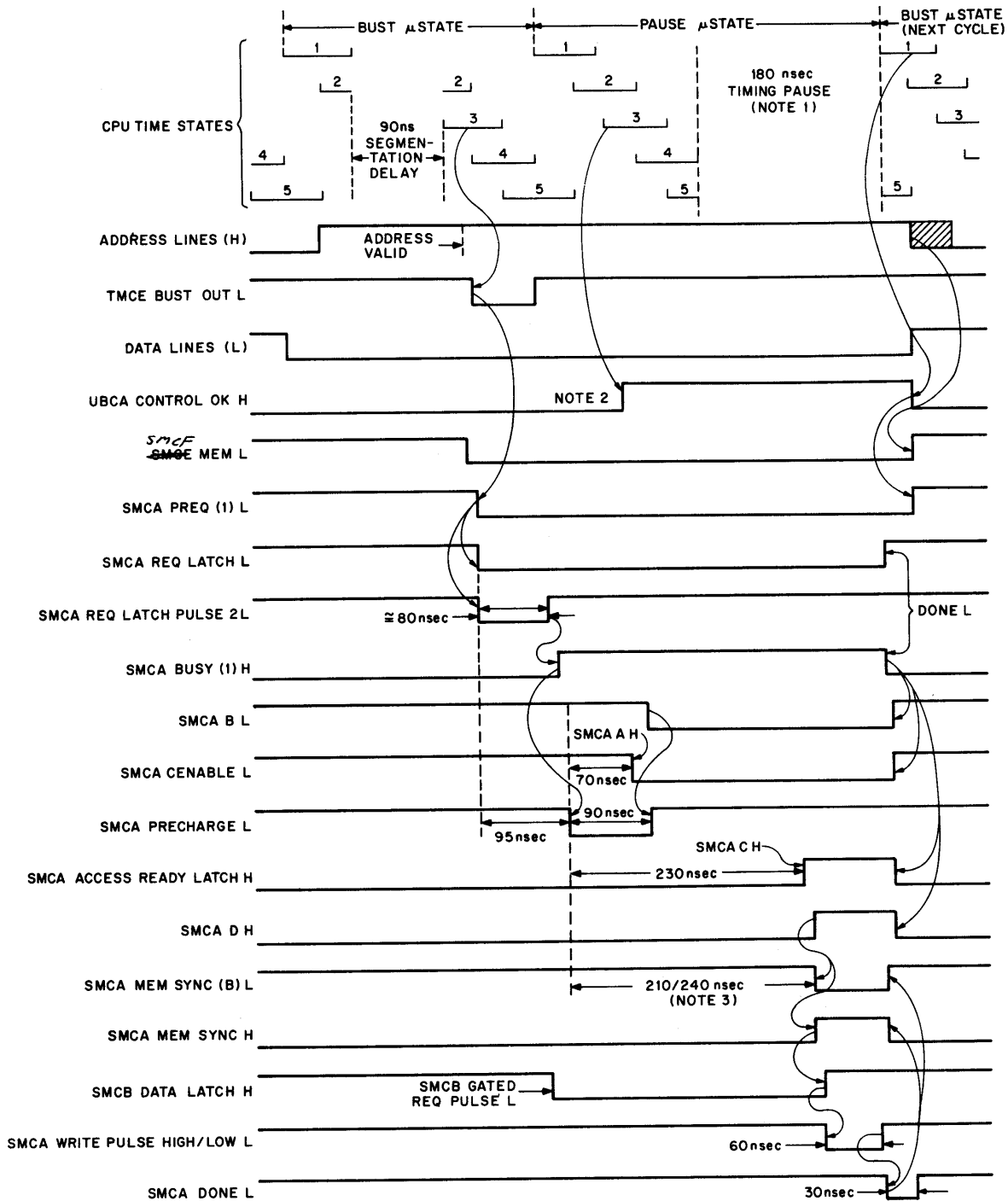


#### NOTES:

1. Memory waits for CPU's next T1, T3 (BUSTOUT) following completion of the DATI (a pause may not occur with Bipolar due to receipt of MEM SYNC (B) L at TIG board (E27) before time pulse T5).
2. Data clocked into the BR.
3. REV { 60 nsec if M8109 jumper W5 out, W6 in.  
F { 30 nsec if M8109 jumper W5 in, W6 out.  
REV { 60 nsec if flip flop at E8 (M8109) not used.  
C { 30 nsec if flip flop at E8 (M8109) has  
jumpers at pins 11 and 12.
4. CPU may send BEND CLEAR in place of CONTROL OK. See Figure 3-7 (9.9, 9.15 and 9.20).
5. SMCB PAUSE H is asserted by SMCA BUSY (1) H if Unibus DATIP.

11-3625

Figure 3-15 Fastbus DATIP-DATO Timing (Bipolar)



NOTES:

1. CPU timing may remain stopped for an additional 30 nsec if MEM SYNC is not stable on the TIG board at the end of the 180 nsec delay.
2. CPU may send BEND CLEAR in place of CONTROL OK. See Figure 3-7 (9.9, 9.15 and 9.20).

3. REV { 240 nsec if M8109 jumper W5 out, W6 in.  
F { 210 nsec if M8109 jumper W5 in, W6 out.  
REV { 240 nsec if flip flop at E8 (M8109) not used.  
C { 210 nsec if flip flop at E8 (M8109) has jumpers at pins 11 and 12.

11-3626

Figure 3-16 Fastbus DATO Timing (MOS)

**Table 3-5**  
**MOS and Bipolar Memory Timing (M8110/M8120)**

Function or Signal	Assertion Time (nanoseconds)		Measured	
	Bipolar	MOS	From	To
Address Set-Up	80	95	SMCA REQ LATCH ↑	SMCA PRECHARGE L ↓
SMCA PRECHARGE L	60	90	SMCA PRECHARGE L ↓	SMCA PRECHARGE L ↑
Access Time	90	230	SMCA PRECHARGE L ↓	SMCA ACCESS READY LATCH H ↑
MEM Sync	30 or 60 (Note 1)	210 or 240 (Note 2)	SMCA PRECHARGE L ↓	SMCA MEM SYNC (B) L ↓
SMCA WRITE PULSE HIGH L	60	60	SMCA WRITE PULSE HIGH L ↓	SMCA WRITE PULSE HIGH L ↑

NOTES: 1. Refer to Note 3 on Figure 3-12.  
2. Refer to Note 3 on Figure 3-16.

(1) H outputs from the parity register flip-flops are gated to the Unibus; 2) if a write (DATO) is decoded, the signal SMCF PAR REG STB H is asserted. This signal clocks the parity register and new data is written into the parity register flip-flops. Note that both these signals are inhibited, and consequently all parity functions are disabled, if jumper B (E87) is in place. Access to the parity register can only be gained by cutting this jumper. As a result of decoding the assigned parity register address, the parity register can either be read or written into. (The parity register is not byte addressable.) The access cycle that accomplishes this reading or writing is the same as any other Unibus access cycle except for the unique address.

The parity register address is assigned according to the starting address, i.e., the lowest address to which this M8110 responds. Table 3-6 shows the starting addresses, from 000000 through 740000<sub>8</sub> in 8K increments because the memory must be located on 8K boundaries in order to meet parity register addressing specifications. (This restriction can be disregarded if MS11 parity functions are not enabled.) Thus, in a system configuration with no local memory, 000000<sub>8</sub> is the lowest Unibus address that the M8110/M8120 responds to and therefore the parity register is assigned address 772100<sub>8</sub>. The capacity of the memory controlled by the M8110/M8120 is not a factor in address determination; it could consist of for example, 1K (minimum bipolar) or 16K (maximum MOS or bipolar) memory locations and the parity register address would remain the same. Every parity memory unit on the Unibus is assigned a unique parity register address. For example, address 772100<sub>8</sub> would be assigned to a 12K (0-057776<sub>8</sub>) local memory. If, in addition, a 16K MS11 were connected to the same Unibus, its assigned address range would be from 16 to 32K (100000 – 177776<sub>8</sub>) in order to comply with the 8K boundary restriction. Accordingly, with a starting address of 100000<sub>8</sub>, the assigned parity register address for the MS11 is 772104<sub>8</sub>. The same parity register address would be used regardless of the MS11 memory size provided the starting Unibus address remains the same. If a second M8110 module with additional memory (starting address = 200000<sub>8</sub>) were included in the MS11, its parity register address would be 772110<sub>8</sub>.

The 13 most significant bits (17:05) of the parity register address are always decoded as 7721XX<sub>8</sub>. Two NAND gates in the parity address decoding logic (drawing SMCF) decode bits (17:06); address bit 05 is input to a third NAND gate in the same circuit. Four 8242 exclusive-NOR gates in the decoder determine address bits (04:01). Inputs to these gates consist of four Unibus address bits, SMCH UBAD (04:01) H, three signals from the address selection jumper network, SMCF DECODE (17:15) H, and a high or low input from jumper T(E87) in the parity register address decoder. SMCH UBAD (04:02) H are exclusively ORed with SMCF DECODE (17:15) H to define parity register address bits (04:02). Likewise SMCH UBAD 01 H is exclusively ORed with the jumper T output to decode address bit 01. If this jumper is in place, bit 01 is a 0; if it is cut, bit 01 is a 1. The 8242 gates in the parity

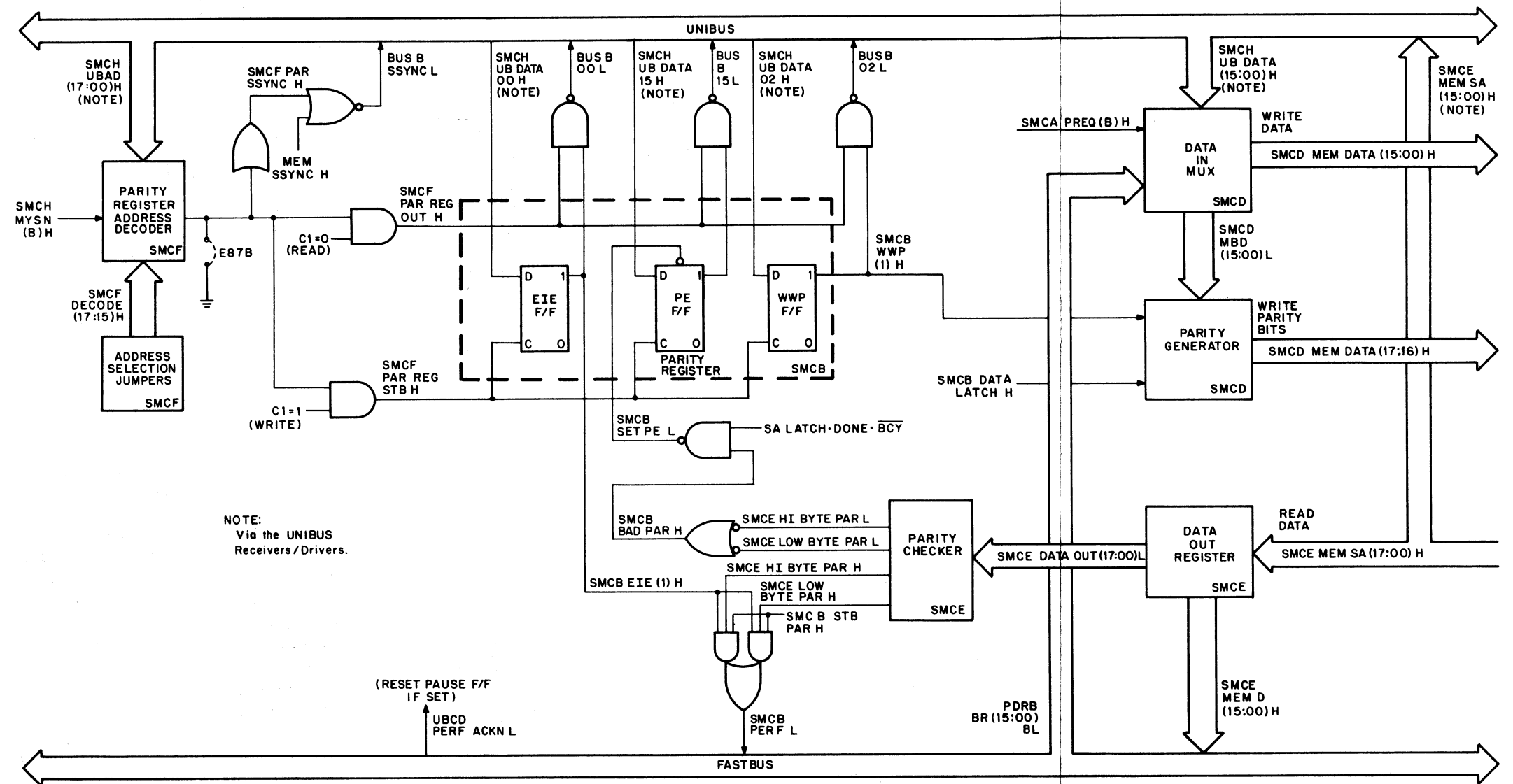


Figure 3-17 Parity Logic, Block Diagram

Table 3-6  
Parity Register, Assigned Addresses

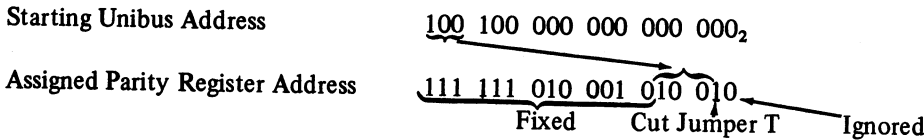
SMCF DECODE XX L			Jumper E87 "T" (Note 1)	Starting Unibus Address		Assigned Parity Register Address
17	16	15		Decimal	Octal	
0	0	0	0	0K	000000	772100
0	0	0	1	8K	040000	772102
0	0	1	0	16K	100000	772104
0	0	1	1	24K	140000	772106
0	1	0	0	32K	200000	772110
0	1	0	1	40K	240000	772112
0	1	1	0	48K	300000	772114
0	1	1	1	56K	340000	772116
1	0	0	0	64K	400000	772120
1	0	0	1	72K	440000	772122
1	0	1	0	80K	500000	772124
1	0	1	1	88K	540000	772126
1	1	0	0	96K	600000	772130
1	1	0	1	104K	640000	772132
1	1	1	0	112K	700000	771134
1	1	1	1	120K	740000	772136
				(Note 2)		

NOTES: 1. Jumper IN = 0, Jumper OUT = 1.  
2. Unibus address space 124–128K is reserved for peripheral registers.

register address decoder operate in the same manner as they do in the address decoder (Paragraph 3.2.1). If both inputs to a single gate are either high or low, the output is high and one leg of the decoder is enabled. Therefore if a jumper is in place (a low), the corresponding address bit must be a 0 (also a low) to disable the 8242 gate and generate the necessary high output. Likewise, if a jumper is cut, the resultant high input to the 8242 gate must be accompanied with an address bit = 1 (high) in order to disable the gate. A jumper in place decodes a 0 bit in the address; an excluded jumper decodes a 1 bit. (Note that the polarity of the address bits at this point is opposite the Unibus line polarity; 1 bits are high and 0 bits are low.) Two other inputs to the parity register address decoder are required before the register can be accessed. The master sync signal derivative, SMCH MSYNC (B) H, must be high and the output from jumper B (E87) must also be high (the jumper must be cut to enable parity functions).

Two outputs from the parity register address decoder, SMCF PAR REG STB H and SMCH PAR REG OUT H, are described above. A third output, SMCF PAR SSYN H, is asserted regardless of the bus cycle in effect. This signal asserts BUSB SSYN L on the Unibus, thus acknowledging acceptance of the request for access to the parity register.

**3.2.7.2 Parity Register Address Set-up** – It is easy to determine the parity register address since it is dependent on the starting Unibus address for the memory. Bits (04:02) of the parity register address are equal to bits (17:15) of the Unibus address. Jumper T is then cut or left in place to decode parity register address bit 01 (jumper cut decodes a 1; jumper left in place decodes a 0). The other parity register address bits, (17:06), are fixed; they are always decoded as 7721XX. For example, if a 4K bipolar memory uses the 72-76K memory space, the starting Unibus address is 440000<sub>8</sub>. Therefore, the parity register address is 772122<sub>8</sub>.



**3.2.7.3 Parity Register** – This register consists of three 74H74 D-Type flip-flops shown on drawing SMCB: parity error (PE), write wrong parity (WWP), and error indication enable (EIE). Table 3-7 lists their bit assignments and functions.

**Table 3-7**  
**Parity Register Flip-Flops, Bit Identity and Function**

Flip-Flop Name	Input Data	Output Data	Parity/Diagnostic Function Performed
EIE (error indication enable)	SMCH UB DATA 00 H	BUSB 00 L	Enables parity-initiated aborts when set (SMCB PERF L); disables when reset.
WWP (write wrong parity)	SMCH UB DATA 02 H	BUSB 02 L	Odd (bad) parity is stored when set; even (normal) parity when reset.
PE (parity error)	SMCH UB DATA 15 H	BUSB 15 L	Error flag, direct set upon detection of a parity error by SMCB SET PE L.

The EIE flip-flop is used to control the parity error checking function by allowing or inhibiting the parity error flag (SMCB PERF L) to the Fastbus when an error is detected. When a word is read during a Fastbus DATI cycle, both bytes are checked for even parity; either (or both) SMCE HI BYTE PAR H or SMCE LO BYTE PAR H is asserted if odd parity is detected. If the EIE flip-flop is set, SMCB EIE (1) H gates the asserted parity error signal(s) to the Fastbus as SMCB PERF L. This latter signal sets the processor parity error flag (Paragraph 3.2.7.5).

The signal SMCH UB DATA 00 H from the Unibus data receivers controls the state of the EIE flip-flop which is clocked set or reset when a DATO is addressed to the parity register. The flip-flop output, SMCB EIE (1) H, is gated to the Unibus as BUSB 00 L when a DATI or DATIP is directed to the parity register.

A check of the parity logic itself can be made by forcing a parity error when the memory is read. The write wrong parity bit is used for this purpose. By generating incorrect (odd) parity when a byte or word is stored, it forces the generation of a parity error when the same location is subsequently read. Failure of the parity logic would be indicated if the error is not detected. The WWP flip-flop is set when clocked by SMCF PAR REG STB H and the D input, SMCB UB DATA 02 H, is high. The (1) H output is then routed to the parity generator (drawing SMCD) where it controls the parity mode. If SMCB WWP (1) H is high, the asserted parity is odd; if low, the parity is even (Paragraph 3.2.7.4).

The PE flip-flop is used to record the fact that a Fastbus read parity error occurred; it serves no other function in the MS11. When an error is detected (SMCE HI BYTE PAR L and/or SMCE LO BYTE PAR L are asserted), the flip-flop is direct set by SMCB SET PE L. SMCB PERF L is also asserted to the Fastbus if the EIE flip-flop is in the set state when the read error is detected. However, the two operations (set PE and assert PERF) are performed independently. The PE flip-flop is set on detection of an error, regardless of the state of the EIE flip-flop, but EIE must be set for a Fastbus error to assert SMCB PERF L. In addition to the direct set input, the PE flip-flop can be set or cleared by Unibus data bit 15 when a DATO addresses the parity register. Normally, the flip-flop is direct set on error detection and then reset (bit 15 is a 0) by the processor.

**3.2.7.4 Parity Generator** – The parity generator (drawing SMCD) provides one (DATOB) or two (DATO) parity bits which are stored with the write data. These two bits, SMCD MEM DATA 16 H for the low byte and SMCD MEM DATA 17 H for the high byte, are asserted to maintain either odd or even byte parity when data is written into



memory. Two 82S62,9 input parity generator/parity checker chips and two 3404 latches make up the circuit. Each 82S62 produces one of the two parity bits as necessary to maintain the desired parity; the state of SMCB WWP (1) H determines whether the generated parity is odd or even. The (1) outputs from the 3404 latches follow the D inputs during the time the L inputs are low (SMCB DATA LATCH H). They are then locked (i.e., not influenced by any subsequent changes at the D inputs) when the latches are latched on the assertion of SMCB DATA LATCH H.

Normally, SMCB WWP (1) H is low and even parity data is stored. However, when SMCB WWP (1) H is high, the generated parity is odd. The data is then read and the resultant bad parity indications (PE flip-flop set and SMCB PERF L asserted) verify the reliability of the parity checking logic.

**3.2.7.5 Parity Checking** – The parity checker consists of two other 82S62 chips (drawing SMCE) on the M8110/M8120 module. Inputs to this circuit are the two 8-bit data bytes, SMCE DATA OUT (07:00) L and SMCE DATA OUT (15:08) L, and their respective parity bits, SMCE DATA OUT 16 L and SMCE DATA OUT 17 L, from the Data Out Register latches. Read data, as a result of both Fastbus DATI and DATIP cycles, is latched into the Data Out Register. Unibus DATI/DATIP read data is not latched into these latches because SA LATCH is not set during Unibus cycles (MEM SYNC is never asserted).

Each of the two 82S62 chips checks a data byte and its parity bit for even parity. If an odd number of 1 bits is found in either 9-bit data group, the respective bad parity indication signal, SMCE LOW BYTE PAR H (and L) or SMCE HI BYTE PAR H (and L), is asserted. (Both signals are asserted if both bit groups are found to have bad parity. However, the second error indication signal is redundant; the consequences of bad parity in one or both bytes are the same.)

SMCE LOW BYTE PAR L or SMCE HI BYTE PAR L asserts SMCB BAD PAR H. This latter signal, in turn, asserts SMCB SET PE L if bad parity exists at the conclusion of the memory cycle when the DONE flip-flop is set. SMCB SET PE L direct sets the PE flip-flop in the parity register (Paragraph 3.2.7.3).

The parity error indication signals of the opposite polarity, SMCE LOW BYTE PAR H and HI BYTE PAR H, serve an additional function. The diagnostic program has two options available with respect to specifying processor action when a Fastbus error is detected. If the EIE flip-flop is reset (Unibus data bit 00 = 0), all parity errors are ignored. However, if EIE is set, the parity error flag (SMCB PERF L) is asserted to the processor, via the Fastbus, and a processor abort is enabled; SMCB PERF L causes a trap to location 114. Parity errors on the Unibus are ignored. SMCB PERF L is inhibited during a Unibus DATI cycle since SMCB STB PAR H, another requisite for the signal, requires the assertion of both PREQ (1) H and UBCA CONTROL OK; neither of these signals are asserted during a Unibus cycle. It should be noted that there are false assertions of PERF during the time CONTROL OK (and therefore SMCB STB PAR H) is asserted. Initially, this is due to the absence of data in the parity checker, and later to the presence of skewed data on the data lines from the memory module, i.e., at the input to the parity checker. Erroneous assertions of SMCE LOW BYTE PAR H and/or SMCE HI BYTE PAR H result from these conditions. Therefore, PERF will fluctuate during the period when CONTROL OK is asserted. The CPU checks for the presence of PERF when it drops CONTROL OK. Consequently, PERF is a valid error indicator only when it is asserted at the time CONTROL OK goes low.

### 3.2.8 Refresh Logic

The M8110 control contains refresh logic that charges each G401 MOS memory cell above the threshold of the data stored there once every millisecond. (The M8120 also contains the same refresh logic. However, it is inoperative since the M8120 is used only with M8111 and M8121 bipolar modules. Bipolar memory does not need to be refreshed.)

A refresh cycle can occur under three different sets of operational conditions:

1. Refresh cycle during normal access operation
2. Refresh/Cycle intervention during processor single-step instruction mode
3. Refresh cycle during power-down periods

Each of these conditions is described separately in the following paragraphs.

**3.2.8.1 Normal Refresh Cycle** — A normal refresh cycle (Figure 3-18) consists of simultaneously addressing one of 32 rows at each G401 MOS Memory Matrix module (drawing SMCB). Each row addressing cycle is timed by a 30  $\mu$ s free running clock. This clock is formed by the RC network C140 and R62, which is base-collector coupled to the NPN switching transistor Q1. The emitter of Q1 is coupled through three inverter stages and fed back to the base of Q1. The 30  $\mu$ s square-wave output of the clock, SMCB REF CLOCK H, is taken off the output from the first inverter stage as a 30  $\mu$ s square wave. SMCB REF CLOCK H is a continuous clocking input to the REF REQ flip-flop. The D input to this flip-flop is +3 V; therefore, when clocked, the output of this flip-flop is REF REQ (1) H a signal with a 30  $\mu$ s repetition rate. REF REQ (1) H is gated with BIPOLAR L to assert REF REQ L.

#### NOTE

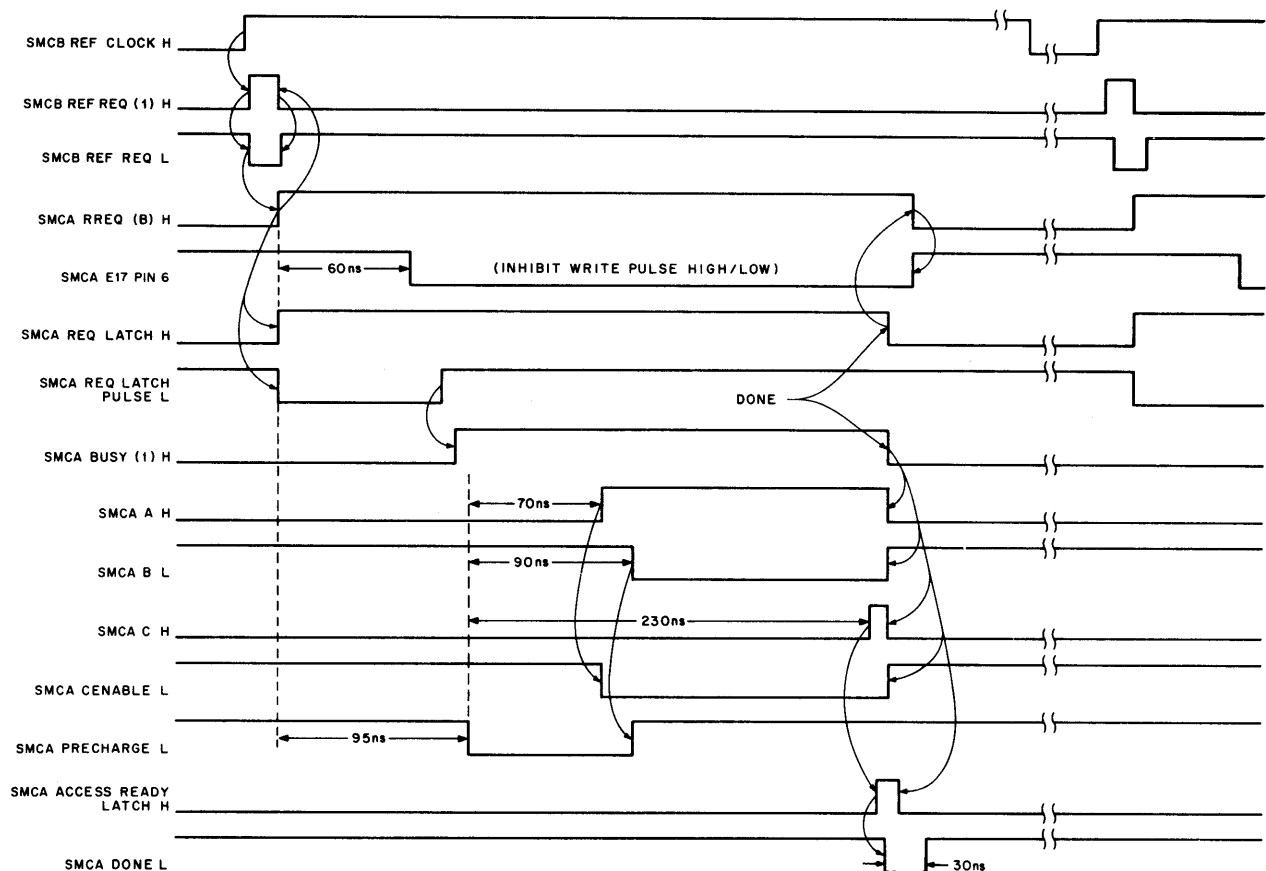
**Jumper A (SMCB) must be cut for MOS memories. Therefore, BIPOLAR L is always high for MOS memories and always low for bipolar memories. The purpose of this level is to disable the refresh cycle when an M8120 control is directing an M8111 or M8121 Bipolar Memory Matrix module.**

SMCB REF REQ L is input to a latch (E51) which asserts SMCA RREQ (B) H (drawing SMCA). SMCA RREQ (B) H initiates an access cycle in the same manner as the Unibus or Fastbus, resulting in the assertion of SMCA REQ LATCH PULSE L. SMCA REQ LATCH PULSE H is ANDed (SMCA) with SMCA RREQ (B) H to generate SMCA RREQ ADDR EN L. This pulse multiplexes the current refresh address SMCB RFAD <04:00> H onto SMCC MAD <07:03> to the memory plane (Table 3-4). Note that if an access cycle from the Unibus or Fastbus is underway, coincident with one of the synchronous assertions of RREQ L, all subsequent assertions of PREQ L will be locked out until the current access cycle is complete. This lock-out action is affected by SMCA REQ LATCH H, which is asserted during all access cycles. SMCA REQ LATCH inhibits the output of the latching element responsible (E51, pin 4) for assertion of SMCA RREQ (B) L, SMCA RREQ (B) H, and SMCA RREQ IN PROG L.

When SMCA RREQ (B) L is generated, a 60 ns delay is initiated at the termination of which a logic low is produced at SMCA E17, pin 6. This signal will inhibit any write pulse from NAND gates E27 (SMCA) when ACCESS READY LATCH H is asserted at the end of the timing cycle. The REF REQ flip-flop is cleared (SMCB E127, pin 13) as the result of its own outputs. SMCB REF REQ L (derived from REF REQ (1) H) raises SMCA RREQ (B) H which, in turn, generates SMCA REQ LATCH PULSE H via SMCA E17, pin 9. This latter signal is ANDed (SMCB E128, pin 3) with RREQ (B) H to clear the REF REQ flip-flop; SMCB REF REQ L is inhibited until the next REF CLOCK signal.

The refresh address is output from a 5-stage binary counter, formed by a 4-bit synchronous binary counter (E129) and a D flip-flop (E130), which forms the fifth and most significant stage. This 5-stage counter, shown on drawing SMCB, is clocked by REF CLOCK H.

SMCA RREQ IN PROG L forces the memory gating control levels (MOSA A, B, C, and D) simultaneously high at each 3207 TTL/MOS level shifting gate, so that as G401 module CENABLE AND PRECHARGE are asserted, these levels are gated to every 1103 MSI memory circuit comprising each G401. In addition, the current 5-bit row address SMCC MAD <07:03> (1) H is gated into the two address inputs to all G401 MOS memory modules at the same time.



11-1293

Figure 3-18 Normal MOS Refresh Cycle Timing

Therefore, with the coincidence of a given row address, SMCA CENABLE L, and SMCA PRECHARGE L, 32 corresponding data words are refreshed simultaneously in each 1024-word section of the four G401 MOS memory modules for a total of 128 words per refresh cycle. When SMCA ACCESS READY LATCH H is asserted in the refresh cycle, SMCA DONE L is asserted and the cycle is complete. The next refresh cycle will not start until the next positive-going transition of SMCB REF CLOCK H.

**3.2.8.2 Refresh Cycle Intervention During Single-Step Mode** – During the single-step execution of processor instructions resulting in a DATO or DATI from either the Unibus or Fastbus, it is possible that a given access cycle could encompass two or more processor microstate (or machine) cycles. In such cases, the access cycle can be initiated from the Unibus or Fastbus during one cycle, with address and data being propagated to the addressed M8110 control on the next cycle. Because execution time of this next cycle in the single-step mode is dependent upon human response, a long time could elapse between two such cycles. In order to maintain validity during these periods, the refresh logic is structured to permit intervention in single-step-initiated access cycles to refresh data. This intervention has no affect on the current access cycle.

In the normal refresh cycle, the REF REQ flip-flop is clocked on the positive-going edge of SMCB REF CLOCK H to assert SMCB REF REQ (1) H and, thereby, start a refresh cycle. However, if after memory is selected there is a single-step (mode) initiation of a Unibus or Fastbus access cycle, SMCA ACCESS READY LATCH will remain high for longer than normal if the access cycle is split between two processor cycles. Consequently, DONE L is not asserted for an inordinately long period and SMCA REQ LATCH H remains high. This latter signal locks up the 3404 latching element at E51, preventing SMCB REF REQ L from initiating a normal refresh cycle (Paragraph 3.2.8.1). This characteristic of a memory access cycle in the single-step mode is detected at a logic circuit shown on drawing

SMCB. This structure is an integrating one-shot multivibrator formed by one element of a 75107 line receiver (E125), combined with an external RC network made up of discrete resistors R20, R21, and capacitor C139. The period of this one-shot is 15  $\mu$ s. When SMCB REF REQ L is asserted, this one-shot is triggered so that 15  $\mu$ s later, if conditioned by SMCA ACCESS READY LATCH H, SMCB REF TIME OUT L becomes true. The effect of asserting this level is as follows: when a refresh cycle is requested but not successfully completed within 15  $\mu$ s after SMCB REF REQ L becomes true, the logic sequence for initiating a refresh cycle, regardless of memory state, is enabled. When asserted, SMCB REF TIME OUT L activates the termination logic and SMCA DONE L is asserted. SMCA DONE L then unlatches the 74S64 logic (E18) enabled by the current single-step mode access cycle and forces SMCA REQ LATCH false. With SMCA REQ LATCH false, SMCB REF REQ L can change the state of the 3404 latching element at SMCA E51 to assert SMCA RREQ (B) H, thereby enabling SMCA E17 and restarting a refresh cycle.

Because activity in the single-step mode is based on a human, rather than machine, time reference, the state of an access cycle is, for all practical effect, frozen. As a consequence, the approximately 450 ns refresh cycle is performed on a cycle-steal basis with respect to the current access cycle. All control levels pertinent to the current single-step mode access cycle remain asserted, so that upon completion of the subject refresh cycle, the addressed M8110 reverts to the state specified by that access cycle. In addition, completing the subject refresh cycle, results in resetting the REF REQ flip-flop and disabling SMCB REF REQ L. At this point, the 15  $\mu$ s delay is terminated.

**3.2.8.3 Refresh Cycle During Power-Down Periods** – The free-running clock (SMCB E104) will continue to cycle during power down situations and (30  $\mu$ s) REF CLOCK H signal production is maintained. Unless PWRS MEM DC LO L is received (SMCH E37), +5 V will be present at the collector of Q1 and the clock generator will function as in normal power-up periods. Response of the memory refresh logic to REF CLOCK H is the same as during the normal refresh cycle (Paragraph 3.2.8.1 and Figure 3-18).

### 3.3 M8121 BIPOLAR MEMORY MATRIX MODULE LOGIC

The maximum storage capability of an M8121-YA Bipolar Memory Matrix module is formed by 72 fully decoded, random-access, 1024-bit bipolar TTL memory integrated circuits, all interconnected to form a 4096-word  $\times$  18-bit memory (Figure 3-19). Each memory chip is organized as 1024 1-bit words. Therefore, eighteen ICs comprise a 1024  $\times$  18-bit memory, and four rows of 1024  $\times$  18 bits provide the 4K capacity.

A16-bit (no parity) version of the M8121-YA is not manufactured.

The M8121-YA module logic functionally divides into two sections, as shown in the drawings for the matrix control BIPA and BIPB, and the memory matrix proper, BIPC, BIPD, BIPE, BIPF, BIPH, BIPJ, BIPK, and BIPL. The description of the detailed logic which follows is based on this functional division.

#### 3.3.1 Memory Matrix Control

The BIPA and BIPB matrix control logic performs four basic functions with respect to the memory matrix portion of an M8121 module. First, address lines from the M8120 control are buffered to provide the fanout necessary to address the bipolar memory circuits. Second, DATA lines from the M8120 control are buffered before being input to the memory matrix, with accompanying write pulses being buffered for necessary fanout. Third, address bits MAD (14:13) (equivalent to Fastbus or Unibus address bits (14:13)) are decoded to enable the specific 4096-word module out of the four 4096-word bipolar modules directed by the M8120 control (Figure 2-8). Fourth, CENABLE from the M8120 and MAD (11:10), equivalent to Fastbus or Unibus address bits (12:11), are decoded to enable the 1024-word section at the selected module containing the addressed location.

**3.3.1.1 Address Buffer** – The M8121 address buffer (drawing BIPA) is a 10-stage parallel buffer which expands each of the ten address lines MAD (09:01) and MAD 12 into four separate lines per bit, thereby providing necessary fanout to the matrix. For each address line input to the buffer from the M8120 control, four lines are output to the memory matrix, one line for each 1024-word row of a 4096-word bipolar memory module. Each stage consists of an input inversion stage (one element of a 74S04 hex inverter) and two 74S40 dual 4-input buffer NAND gates (shown

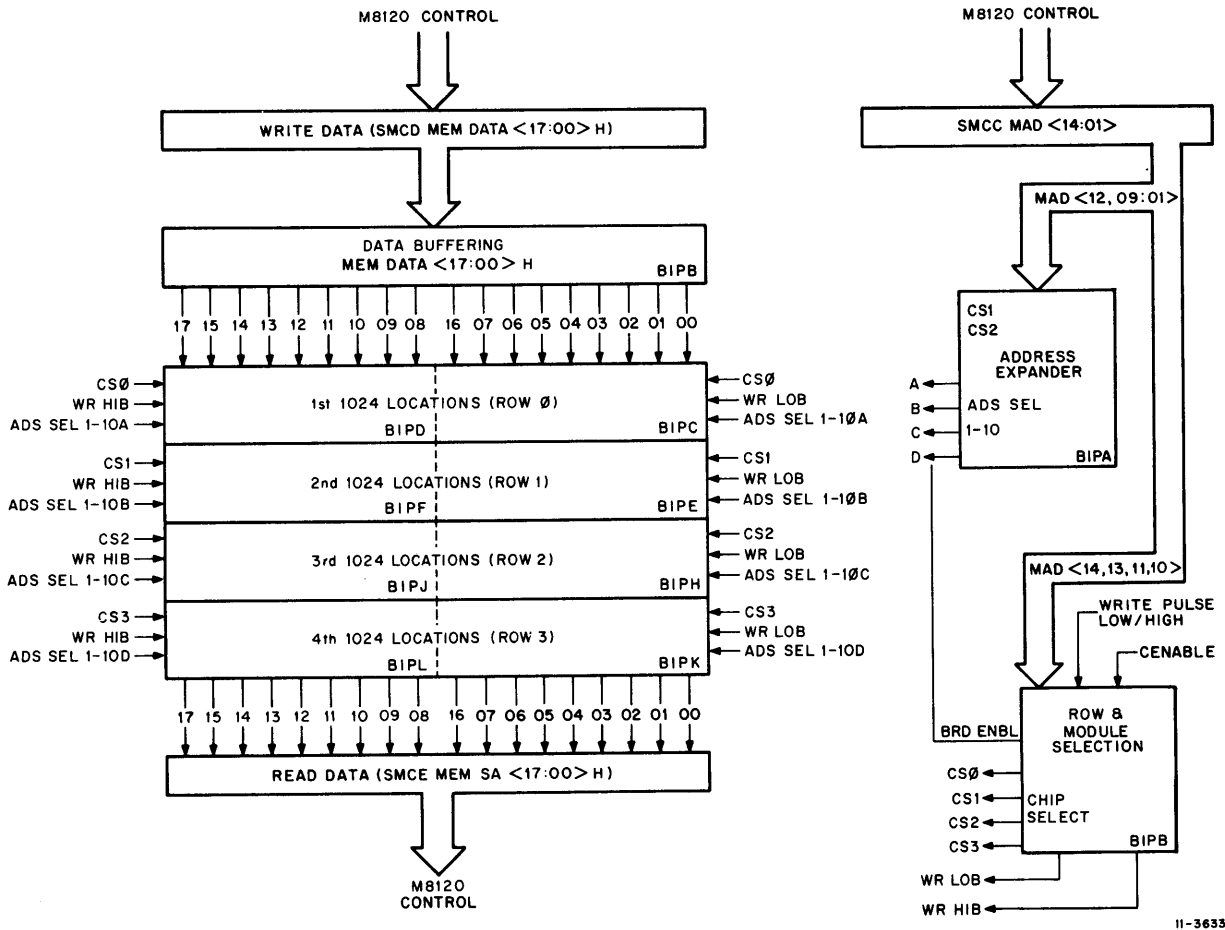


Figure 3-19 M8121 4K Bipolar Memory Matrix, Block Diagram

as negative input OR gates). All four buffer gates in each buffer stage are inhibited at three inputs by a common line to approximately +3.5 V in a voltage divider (drawing BIPA). The enabling input to the buffer is the inverted address so that the polarity of the expanded output address matches that of the input address. The expanded addresses connect to a corresponding 1024-word section of M8121 bipolar memory as shown in Table 3-8.

Table 3-8  
Expanded M8121 Memory Address Allocation

Expanded Addresses	Memory Area Addressed
BIPA ADRS SEL (10A:1A)	0 to 1023 <sub>10</sub>
BIPA ADRS SEL (10B:1B)	1024 to 2047 <sub>10</sub>
BIPA ADRS SEL (10C:1C)	2048 to 3071 <sub>10</sub>
BIPA ADRS SEL (10D:1D)	3072 to 4095 <sub>10</sub>

**3.3.1.2 Data Buffering and Write Pulse Fanout Logic** – Input to the data buffering logic consists of the DATO lines from the M8120 control SMCD MEM DATA (17:00) H (drawing BIPB). This 18-stage circuit, formed by five triple element 74S11 AND gates, buffers the non-inverted data lines to the bipolar memory matrix. Note, however, that the DATI (sense) lines from the M8121 bipolar module to the M8120 control are propagated directly from each memory circuit sense line, SMCE MEM SA (17:00) H, as shown on drawings BIPC through BIPL. Each of the 18 sense lines in a 1024-word section is wire-ORed (to the M8120 control) with the same lines from the other three 1024-word sections.

The two write-enabling pulses that can be asserted at the M8121 module (BIPB) during a DATO are SMCA WRITE PULSE LO L and WRITE PULSE HI L, which enable writing of low-order and/or high-order bytes, respectively, at the addressed location. If a full 18-bit word is being written, both levels will be asserted simultaneously. Each write pulse is buffered in parallel by two identical buffer networks to provide the necessary fanout capability. For example, SMCA WRITE PULSE LO L, when asserted, is first inverted by one stage of a 74S04 hex inverter. The inverter output then enables one gate in two 74540 NAND buffers (E6 and E7). With SMCA WRITE PULSE LO L asserted, the buffer gate outputs are BIPB WR LOB A L and BIPB WR LOB B L. When SMCA WRITE PULSE HI L is asserted, BIPB WR HIB A L and BIPB WR HIB B L are asserted. BIPB WR LOB A L and BIPB WR LOB B L enable writing a low-order byte and BIPB WR HIB A L and BIPB WR HIB B L enable writing a high-order byte. When all four pulses are asserted simultaneously, a full 18-bit word is stored at the addressed location.

**3.3.1.3 Address Examination Logic** – The M8121 Bipolar Memory Matrix module decodes Unibus or Fastbus address bits <14:11> (drawing BIPB). The relationship of address bits to MAD register bits is shown in Table 3-9.

**Table 3-9**  
**Address Bit to MAD Bit Translation (M8121)**

Fastbus or Unibus Address Bit	MAD Register Bit
ADR 14	MAD 14
ADR 13	MAD 13
ADR 12	MAD 11
ADR 11	MAD 10

MAD register bits 14 and 13, in both states at switch S1, MAD <11:10> (1) H, and chip select signal SMCA CENABLE are input to four 74540 NAND gates, E3 and E4 (BIPB). Unibus or Fastbus address bits <14:11> place a given address within a unique 1K section of a 16K group of addresses. (Unibus or Fastbus address bits <17:15> select the 16K address group out of the total 128K address space. Refer to Table 3-1 and Figure 2-8). The selection of this 1K section of addresses is determined by the position of the four switches in S1 (MAD bits <14:13>) and the high or low state of MAD bits <11:10>. Table 3-10 lists the switches that must be closed along with the Unibus/Fastbus address configuration that are necessary to access a 1K address section on the 4K M8121 module. For example, if S1 switches B and C are closed (A and D must then be open), then the 4K address area XX4096 through XX8191 is assigned to this M8121 module. If a Unibus or Fastbus address is within this range, e.g., MAD 14 = 0, MAD 13 = 1, MAD 11 = 1, and MAD 10 = 1, then the 1K section of memory XX7168 through XX8191 will be accessed.

The outputs of the four 74S40 NAND gates (E3 and E4) are BIPB CS<3:0>L. Each output drives one (1K) row of memory chips.

The discrete location in the selected 1K row is determined by BIPA ADRS SEL <10:00> that is derived from SMCA MAD <12,09:01> H (Figure 2-8).

### 3.3.2 Bipolar Matrix

The 4096-word bipolar storage matrix contained on the M8121 memory module is organized as four rows with 1024 words in each row. Each of these four rows is made up of 1024 18-bit words. A bipolar matrix including parity, is formed by 72 memory circuits. Each of the circuits in a given 1024-word row is enabled by a unique enabling level as shown in Table 3-10. In addition to the 1024 X 1-word storage capacity, each memory circuit contains integral write and sense amplifiers so that data is written directly into, or read directly from, each circuit in the matrix as addressed. If the current memory access cycle is a DATO, the M8120 control would, following assertion of SMCA CENABLE L, assert one or both of the pulses SMCA WRITE PULSE LO L and SMCA WRITE PULSE HI L, depending upon whether a byte or a full word is being written. At this point in a DATO, the specific memory location is addressed, and the data to be written is present so that assertion of WR LOB A L and WR LOB B L and/or WR HIB A L and WR HIB B L will enable the write amplifiers on the memory circuits addressed.

**Table 3-10**  
**M8121 Bipolar Matrix Selected Address Configuration (1 of 16K)**

Unibus/Fastbus				S1 Switches Closed (Denoted by X)				Memory Address Assignment (Within Any 16K Block of Memory)	Chip Select Signal Asserted (Enabling Level)	1K Row
14	13	12	11							
MAD				A	B	C	D			
14	13	11	10							
0	0	0	0		X		X	0 to 1023	BIPB CS0L	0
0	0	0	1		X		X	1024 to 2047	BIPB CS1L	1
0	0	1	0		X		X	2048 to 3071	BIPB CS2L	2
0	0	1	1		X		X	3072 to 4095	BIPB CS3L	3
0	1	0	0		X	X		4096 to 5119	BIPB CS0L	0
0	1	0	1		X	X		5120 to 6143	BIPB CS1L	1
0	1	1	0		X	X		6144 to 7167	BIPB CS2L	2
0	1	1	1		X	X		7168 to 8191	BIPB CS3L	3
1	0	0	0	X			X	8192 to 9215	BIPB CS0L	0
1	0	0	1	X			X	9216 to 10,239	BIPB CS1L	1
1	0	1	0	X			X	10,240 to 11,263	BIPB CS2L	2
1	0	1	1	X			X	11,264 to 12,287	BIPB CS3L	3
1	1	0	0	X		X		12,288 to 13,311	BIPB CS0L	0
1	1	0	1	X		X		13,312 to 14,335	BIPB CS1L	1
1	1	1	0	X		X		14,336 to 15,359	BIPB CS2L	2
1	1	1	1	X		X		15,360 to 16,383	BIPB CS3L	3

If the current memory access operation is a DATI, the action of addressing a given location enables the memory circuits comprising that location and places the data stored in the addressed location on lines MEM SA <17:00> to the M8120 control.

### 3.4 M8111 BIPOLAR MEMORY MATRIX MODULE LOGIC

The maximum storage capability of an M8111-YA Bipolar Memory Matrix module is formed by 72 fully decoded, random-access, 256-bit bipolar TTL memory integrated circuits, interconnected to form a 1024-word X 18-bit memory (Figure 3-20). Each memory chip is organized as 256 1-bit words. Therefore, eighteen ICs comprise a 256 X 18-bit memory, and four rows of 256 X 18 bits provide the 1K capacity.

The M8111 Bipolar Memory Matrix module is identical to the M8111-YA in every respect, except that the memory word is 16 bits without byte parity. Therefore, the maximum memory capacity of an M8111 is formed by 64 memory circuits.

The module logic functionally divides into two sections, as shown in the drawings for the matrix control BIPA and BIPB, and the memory matrix proper, BIPC, BIPD, BIPE, BIPF, BIPH, BIPJ, BIPK, and BIPL. The description of the detailed logic which follows is based on this functional division; it is applicable to both the M8111 and M8111-YA modules.

#### 3.4.1 Memory Matrix Control

The BIPA and BIPB matrix control logic performs five basic functions with respect to the memory matrix portion of an M8111 module. First, address lines from the M8120 control are buffered to provide the fanout necessary to address the bipolar memory circuits. Second, DATA lines from the M8120 control are inverted providing the proper

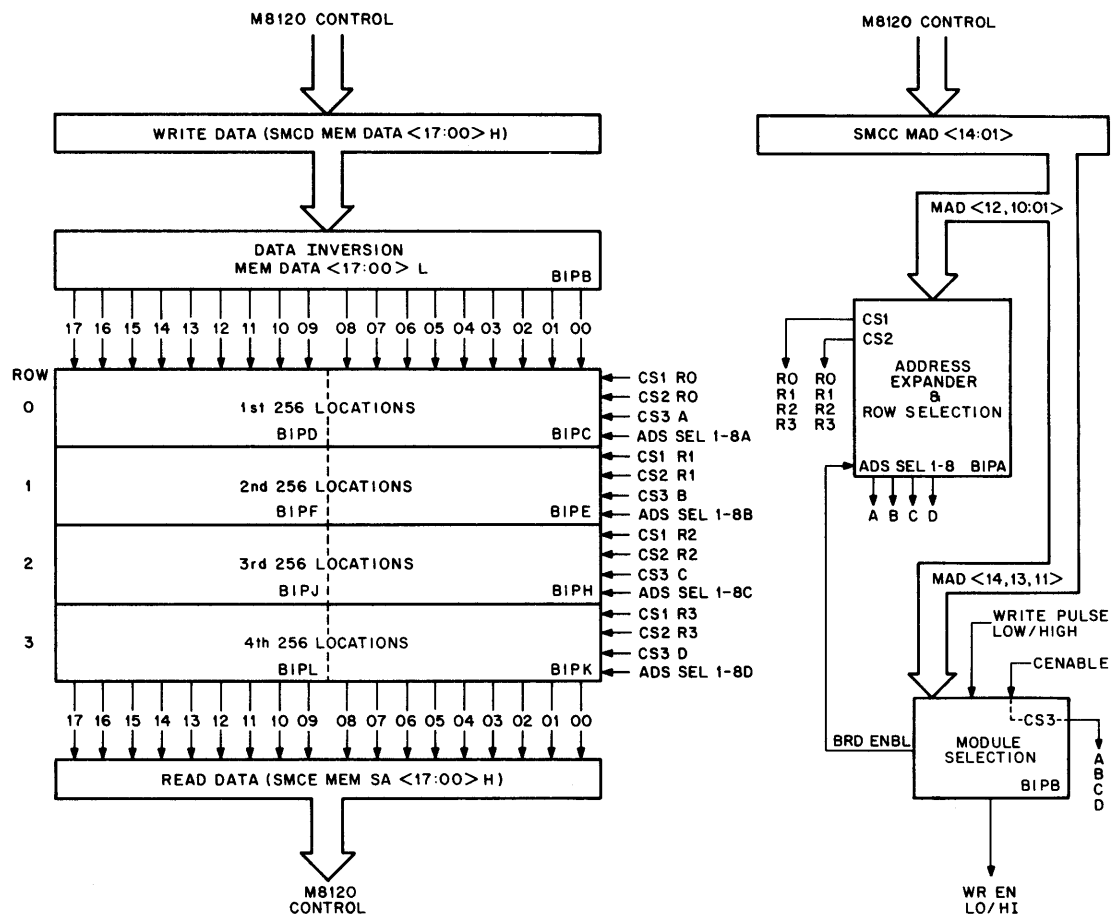


Figure 3-20 M8111 1K Bipolar Memory Matrix, Block Diagram

logic level polarity to the memory matrix, with accompanying write pulses being buffered for necessary fanout. Third, address bits MAD <14:13> and <11:10> (equivalent to Fastbus or Unibus address bits <14:11>) are decoded to enable the specific 1024-word matrix out of the four 1024-word bipolar modules directed by the M8120 control (Figure 2-9). Fourth, CENABLE from the M8120 is buffered to provide required fanout. Fifth, MAD <09:08> are decoded to enable the 256-word section at the selected module containing the addressed location.

**3.4.1.1 Address Buffer** – The M8111 address buffer (drawing BIPA) is an 8-stage parallel buffer which expands each of the eight address lines MAD <07:01> and MAD 12 into four separate lines per bit, thereby providing necessary fanout to the matrix. For each address line input to the buffer from the M8120 control, four lines are output to the memory matrix, one line for each 256-word section of a 1024-word bipolar memory module. Each stage consists of an input inversion stage (one element of a 74S04 hex inverter) and two 74S40 dual 4-input buffer NAND gates (shown as negative input AND gates). All four buffer gates in each buffer stage are conditioned at three inputs by a common line to +3V (drawing BIPA). The enabling input to the buffer is the inverted address so that the polarity of the expanded output address matches that of the input address. The expanded addresses connect to a corresponding 256-word section of M8111 bipolar memory as shown in Table 3-11.



**Table 3-11**  
**Expanded M8111 Memory Address Allocation**

Expanded Addresses	Memory Area Addressed
BIPA ADRS SEL (8A:1A)	0 to 255 <sub>10</sub>
BIPA ADRS SEL (8B:1B)	256 to 511 <sub>10</sub>
BIPA ADRS SEL (8C:1C)	512 to 767 <sub>10</sub>
BIPA ADRS SEL (8D:1D)	768 to 1023 <sub>10</sub>

**3.4.1.2 Data Inversion and Write Pulse Fanout Logic** – Input to the data inversion logic are the DATA lines from the M8120 control SMCD MEM DATA (17:00) H (drawing BIPB). This 18-stage inversion logic, formed by four 74S04 hex inverters, drives inverted data lines to the bipolar memory matrix. Note that DATI (sense) lines from the M8111 bipolar module to the M8120 controls are propagated directly from each memory circuit as MEM SA (17:00) H. Each sense line in a 256-word section is wire-ORed (to the M81110 control) with the same lines from the other three 256-word sections.

The two write-enabling pulses that can be asserted at the M8111 module (BIPB) during a DATO are SMCA WRITE PULSE LOW L and WRITE PULSE HIGH L, which enable writing of low-order and/or high-order bytes, respectively, in the addressed location. If a full 16-bit word is being written, both levels will be asserted simultaneously. Each write pulse is buffered in parallel by two identical buffer networks to provide the necessary fanout capability. For example, SMCA WRITE PULSE LOW L, when asserted, is first inverted by one stage of a 74S04 hex inverter. Inverter output then enables both gates of a 74S40 NAND buffer (E13). With SMCA WRITE PULSE LOW L asserted, buffer gate outputs are BIPB WR EN LO A L and BIPB WR EN LO B L. When WRITE PULSE HIGH L is asserted, BIPB WR EN HI A L and BIPB WR EN HI B L are asserted. BIPB WR EN LO A and BIPB WR EN LO B enable writing a low-order byte and BIPB WR EN HI A and BIPB WR EN HI B enable writing a high-order byte. When all four pulses are asserted simultaneously, writing a full word at the addressed location is enabled.

**3.4.1.3 Address Examination Logic** – The M8111 Bipolar Memory Matrix module decodes Unibus or Fastbus address bits (14:11) (drawing BIPB). The relationship of address bits to MAD register bits is shown in Table 3-12.

**Table 3-12**  
**Address Bit to MAD Bit Translation (M8111)**

Fastbus or Unibus Address Bit	MAD Register Bit
ADR 14	MAD 14
ADR 13	MAD 13
ADR 12	MAD 11
ADR 11	MAD 10
ADR 10	MAD 09
ADR 09	MAD 08

MAD register bits 14 and 13 in both states, along with MAD 11 (1) H, are jumpered at BIPB for input to a triple 3-input NAND gate, E8. Unibus or Fastbus address bits (14:11) serve to place a given address within a 16K set of addresses. Therefore, the selective jumpering of these address bit inputs at an M8111 memory module can designate that memory module as having a unique 1K set of consecutive addresses within the total set of 16K addresses. Table

3-13 lists jumper connections and corresponding address set selected by each connection configuration, along with the (MAD) address bit configuration necessary to access the module. For example, if jumpers D, E, J, and A are installed, the memory module is assigned addresses XX7168 through XX8191. Then a Fastbus or Unibus address within this range (MAD 14 = 0, MAD 13 = 1, MAD 11 = 1, and MAD 10 = 1) will cause this memory module to respond.

**Table 3-13**  
**M8111 Bipolar Matrix Selected Address Configuration (1 of 16K)**

UNIBUS				Required Jumpers				Memory Address Assignment (Within Any 16K Block of Memory)
14	13	12	11					
MAD								
14	13	11	10	(MAD 14)	(MAD 13)	(MAD 11)	(MAD 10)	
0	0	0	0	D	F	H	B	0 to 1023
0	0	0	1	D	F	H	A	1024 to 2047
0	0	1	0	D	F	J	B	2048 to 3071
0	0	1	1	D	F	J	A	3072 to 4095
0	1	0	0	D	E	H	B	4096 to 5119
0	1	0	1	D	E	H	A	5120 to 6143
0	1	1	0	D	E	J	B	6144 to 7167
0	1	1	1	D	E	J	A	7168 to 8191
1	0	0	0	C	F	H	B	8192 to 9215
1	0	0	1	C	F	H	A	9216 to 10,239
1	0	1	0	C	F	J	B	10,240 to 11,263
1	0	1	1	C	F	J	A	11,264 to 12,287
1	1	0	0	C	E	H	B	12,288 to 13,311
1	1	0	1	C	E	H	A	13,312 to 14,335
1	1	1	0	C	E	J	B	14,336 to 15,359
1	1	1	1	C	E	J	A	15,360 to 16,383

Fastbus or Unibus address bits <10:09> are translated by the M8120 control, as shown in Table 3-12, as MAD <09:08>. The states of these address bits designate which 256-word section of the 1024-word matrix contains the location being addressed. These bits are received at each M8111 module and inverter-buffered by two parallel, dual-stage inverter networks to assert the corresponding levels BIPA A 09 L, BIPA A 09 H, BIPA A 10 L, and BIPA A 10 H. These levels are then input to an 8-stage logic network formed by four dual power gate units: E6, E7, E14, and E15. This network is conditioned by the four state combinations of BIPA <A 10:A09> and +3 V. The network is enabled when the level BIPB BRD ENBL and the appropriate state of MAD 10 are asserted as a consequence of address decoding. Enabled output from this network consists of one of four pairs of enabling levels being true, as listed in Table 3-14, to enable the 256-word section of bipolar memory being addressed. These enabling levels are low when asserted and constitute two of the three required chip-select inputs. The third chip-select input is generated by SMCA CENABLE L from the M8120 control. This signal is received by E9 on BIPB that drives four gates (E4 and E5) in parallel to provide the required fanout. The outputs are BIPB CS3 <A, B, C, D> L. Each set of chip-select signals, e.g., BIPA CS1 RO L, BIPA CS2 RO L, and BIPB CS3 A L, drives one row of memory chips.

**Table 3-14**  
**Address Decoding for Memory Circuit Enabling**

<b>BIPA A10 (MAD 09)</b>	<b>BIPA A09 (MAD 08)</b>	<b>Enabling Levels</b>	<b>Memory Locations Selected</b>
0	0	BIPA CS1 R 0 L BIPA CS2 R 0 L	0–255 (Row 0)
0	1	BIPA CS1 R 1 L BIPA CS2 R 1 L	256–511 (Row 1)
1	0	BIPA CS1 R 2 L BIPA CS2 R 2 L	512–767 (Row 2)
1	1	BIPA CS1 R 3 L BIPA CS2 R 3 L	768–1023 (Row 3)

Using the example given above, further definition of the memory location within the 1K memory block (addresses XX7168 through XX8191) is effected using the states of MAD 08 and MAD 09. If MAD 08 = 1 and MAD 09 = 0, then the respective BIPA A09 and BIPA A10 signals generate BIPA CS1 R1L and BIPA CS2 R1L. These signals, together with CENABLE generated BIPB CS3 BL, will address the second 256 group of locations within the 1K block, i.e., locations XX7424 through XX7679. MAD 12 <7:1> (BIPA ADRS SEL <8:1>) select the discrete location from this 256 location group.

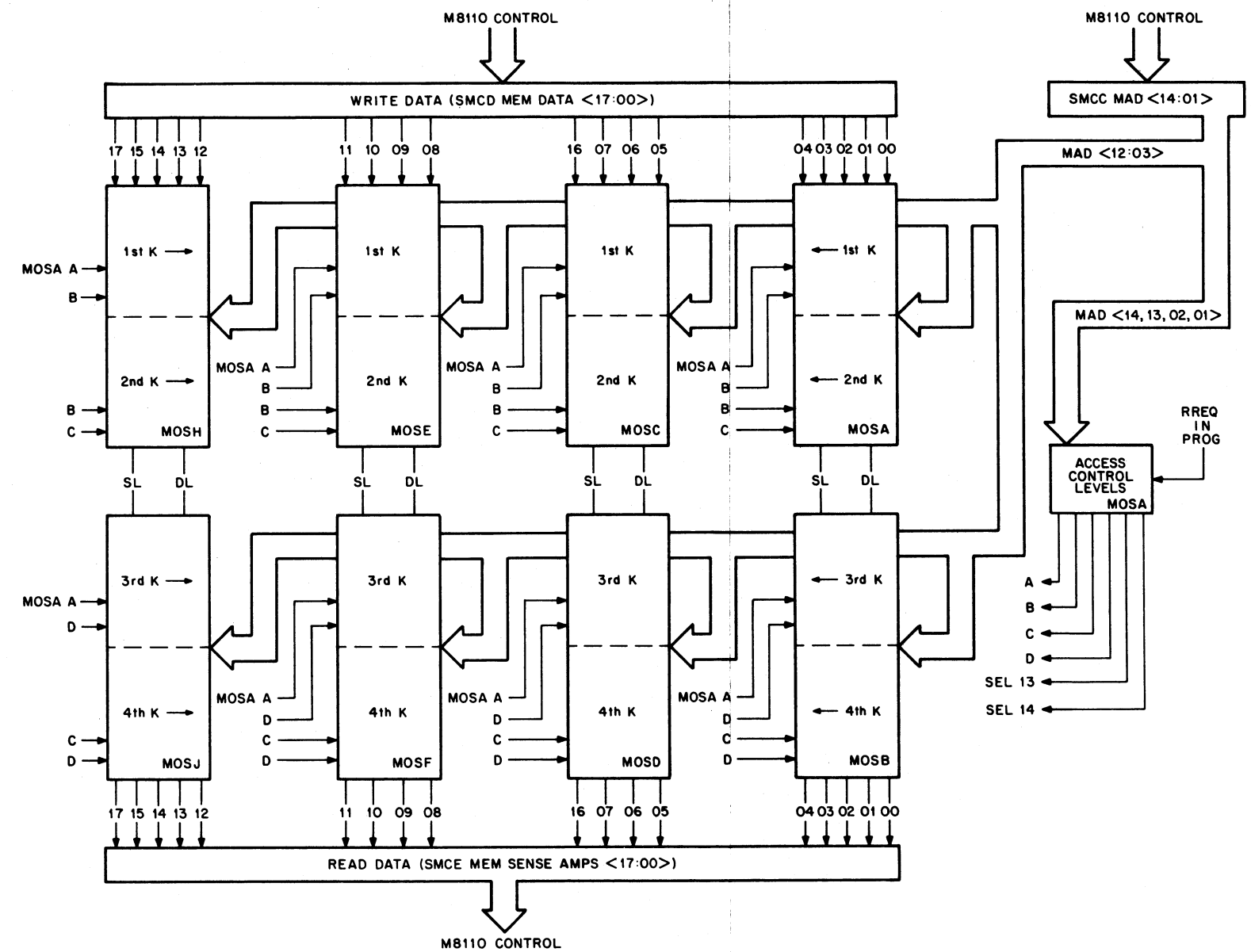
#### 3.4.2 Bipolar Matrix

The 1024-word bipolar storage matrix contained on the M8111 memory module is organized as four rows with 256 words in each row. If the module is equipped for parity, each of these four rows is made up of 256 18-bit words. If the module is not equipped for parity, each row is made up of 16-bit words. A bipolar matrix with parity is formed by 72 memory circuits; a non-parity matrix is formed by 64 memory circuits. Each of the circuits in a given 256-word row is enabled by a unique set of enabling levels as shown in Table 3-14, in coincidence with BIPB BRD ENBL H. In addition to the 256 × 1-word storage capacity, each memory circuit contains integral write and sense amplifiers so that data is written directly into, or read directly from, each circuit in the matrix as addressed. If the current memory access cycle is a DATO, the M8120 control would, following assertion of SMCA CENABLE L, assert one or both of the pulses SMCA WRITE PULSE LOW L and SMCA WRITE PULSE HIGH L, depending upon whether a byte or a full word is being written. At this point in DATO, the specific memory location is addressed, and the data to be written is present so that assertion of WR EN LO A L/WR EN LO B L, and/or WR EN HI A L/WR EN HI B L will enable the write amplifiers on the memory circuits addressed.

If the current memory access operation is a DATI, the action of addressing a given location enables the memory circuits comprising that location and places the data stored in the addressed location on lines MEM SA <17:00> to the M8120 control.

### 3.5 G401 MOS MEMORY MATRIX MODULE LOGIC

The memory capacity of the G401 is formed by seventy-two 1103-type fully decoded, random-access, 1024 × 1-bit dynamic memory circuits. These 4096-word memories are directly addressed on the basis of 1024 18-bit words (Figure 3-21). The specific set of 1024 words addressed is determined by the states of MAD register bits 01 and 02. The states of these bits, asserted as MAD 01 (1) H and MAD 02 (1) H on drawing MOSA, are decoded to enable the control levels CENABLE and PRECHARGE to the specific set of 1024 words to be addressed for a DATO or DATI. The result of MAD 01 (1) H and MAD 02 (1) H decoding is a set of gating control levels designated MOSA A H, MOSA B H, MOSA C H, and MOSA D H.



11-1324

Figure 3-21 G401 4K MOS Memory Matrix, Block Diagram

Decoding of MAD 01 (1) H and MAD 02 (1) H is performed by the logic shown on drawing MOSA. This logic is enabled by the states of address bits MAD 13 and MAD 14, that specify which of the four G401 MOS memory modules directed by a given control (Figure 2-10) is being addressed. The states of MAD 13 and MAD 14 are uniquely jumper-connected at each G401 module to condition the gating of control levels MOSA A H, B H, C H, and D H only at the memory module addressed. The states of MAD (14:13), as jumpered, also assert levels MOSA SEL 13 H and MOSA SEL 14 H to enable the G401 read amplifiers at the addressed memory module in case the current access cycle is a DATI.

Table 3-15 lists the required jumper configuration for the assignment of the associated 4K block of MOS memory addresses, while Table 3-16 indicates the control levels generated, and the 1K memory block selected, from MAD 01 and MAD 02. Control levels MOSA A, MOSA B, MOSA C, and MOSA D gate SMCA PRECHARGE, SMCA CENABLE, and WRITE PULSE HIGH/LOW to access one of four sets of 1024 words. For example, if a G401 MOS matrix has jumpers C and B installed, then that matrix contains memory locations XX4096 through XX8191. (Since there are 131,072<sub>(10)</sub> possible addresses, XX equals 00 to 13. As described in Paragraph 3.2.1, Fastbus/Unibus address decoder bits (17:15) determine these higher range address assignments.) Any address, directed to this memory module, where MAD 14 is a 0 and MAD 13 is a 1 will cause the matrix to recognize and respond to the address. Further definition of the same address is made by the MAD 01 and MAD 02 configuration. If MAD 02 is a 1 and MAD 01 is a 0, then control levels MOSA D and MOSA A are generated. As indicated by Table 3-16, these two control levels will select the third 1K memory segment, in this case locations XX6144 through XX7167.

Table 3-15  
MOS Matrix Selected Address Configuration (4 of 16K)

MAD		Required Jumpers		MOS Matrix Memory Address Assignment
14	13	(MAD 14)	(MAD 13)	
0	0	C	A	0—4095
0	1	C	B	4096—8191
1	0	D	A	8192—12,287
1	1	D	B	12,288—16,383

Table 3-16  
MOS Matrix Control Level Generation and Selected Memory Address Block (1 of 4K)

MAD		Control Levels Generated		Memory Address Block Selected
02	01	(MAD 02)	(MAD 01)	
0	0	MOSA B	MOSA A	0—1023
0	1	MOSA B	MOSA C	1024—2047
1	0	MOSA D	MOSA A	2048—3071
1	1	MOSA D	MOSA C	3072—4095

The discrete location in the 1K block of addresses is determined by A(12:03), for the low byte, and B(12:03) for the high byte. These G401 address bits are derived from the M8110 address bits SMCC MAD (12:03) (1) H (Figure 2-10).

### 3.5.1 MOS Memory Writing

Address lines MAD <12:03> (drawings MOSA through MOSJ) are input to the MOS memory module and enable a level-shifting NAND gate structure formed by 3-input 3207 type level shifters. Outputs are the MOS levels +1 V and +19 V, so that a +3 V TTL input is level-shifted to +1 V, and TTL ground input is level-shifted to +19 V. Each gate output is propagated through a series-damping resistor to the corresponding 1103 type MOS memory circuit address input terminal. The access control levels PRECHARGE, CENABLE, WRITE PULSE HIGH, and/or WRITE PULSE LOW are also input to this level-shifting NAND gate structure and are propagated to the corresponding 1103 input terminals in the same manner. The use of damping resistors at the gate output effectively eliminates any potential ringing problems.

As shown on drawings MOSA through MOSJ, the level-shifting NAND gate structure is configured to form two duplicate level-shifting gate structures: one to access the low-order byte and one to access the high-order byte. The only logical difference in these duplicate structures is that WRITE PULSE LOW H conditions the structure accessing the low-order byte, and WRITE PULSE HIGH H conditions the structure accessing the high-order byte. The outputs from each gate structure connect in parallel to the address and control terminals for the 36 circuits storing the four groups of 1024 bytes. With these gating structures conditioned by the appropriate access control levels, the state of gating control levels MOSA A H, MOSA B H, MOSA C H, and MOSA D H (Table 3-16) enable accessing the specific 1024 bytes or words designated by the current address.

The access levels CENABLE L, PRECHARGE L, WRITE PULSE LOW L, and WRITE PULSE HIGH L are inverted and buffered by two buffer gates (MOSC E10 and E11) to provide the drive necessary to access the MOS memory.

Write data from the M8110 control consists of the data bits SMCD MEM DATA <16,07:00> H for the low byte and SMCD MEM DATA <17,15:08> H for the high byte. Input to the memory matrix is through type 3207 level shifters just described.

### 3.5.2 MOS Memory Reading

At the selected G401 MOS memory module, the states of MAD bits 13 and 14 will assert MOSA SEL 13 H and MOSA SEL 14 H from gates E7. These levels enable a parallel sense-amplifier network made up of 18 sense amplifiers, one for each memory bit. Each sense amplifier consists of one element of a 75108 dual-line receiver with open collector output. The input to each sense amplifier is wire-ORed to the output of four memory circuits. As a result, the input to each sense amplifier is the wire-OR of 1024 memory bit locations. Therefore, when a given word is addressed, the content of the addressed location is input to the sense amplifiers. Note that the second input to each sense amplifier is an unterminated line paralleling the first input. The purpose of this line is to cancel common-mode noise generation on the adjacent sense line. The DATA output from each 1103 memory circuit functions as an active current source so that output is 900  $\mu$ A for logic 1 and 0  $\mu$ A for logic 0. In addition, the sensed output from each sense amplifier is a TTL output; therefore, output logic levels are 3 V = 1 and 0 V = 0.

In summary, during a given DATI cycle, as the location to be retrieved is addressed, the data stored in that location is placed on the internal lines MEM SA <17:00> to the output data multiplexing logic shown on drawing SMCE.



# CHAPTER 4

## CALIBRATION AND MAINTENANCE

### 4.1 INTRODUCTION

This chapter concerns the calibration procedures and maintenance requirements necessary to maintain an MS11 Semiconductor Memory System. Paragraph 4.3 presents the detailed procedures necessary to perform all memory system adjustment and calibration. The section on maintenance includes lists and descriptions of the diagnostic program set required to perform memory system troubleshooting. Also included are references to specific maintenance requirements contained in associated PDP-11/45 System documentation.

### 4.2 SEMICONDUCTOR MEMORY SYSTEM PRECALIBRATION PROCEDURES

Certain steps must be taken prior to actual memory calibration to assure valid results. These include loading a simple memory cycling program, assembling the correct tools and equipment, and verifying that all portions of the memory system and the overall PDP-11/45 System are operational. These steps are presented in the following paragraphs.

#### 4.2.1 Memory Cycling Program

Proper performance of the adjustments listed in Table 4-1 requires that the semiconductor memory be continuously cycling during actual calibration. While the memory refresh function automatically (during a power-up or power-down condition) provides this requirement for MOS memory configuration, bipolar installations require the input of a simple two-step program to implement continuous memory cycling. This program forces a DATI to the memory system being calibrated every four KB11 bus cycles. Load this program into the processor through the console switches as outlined in the following steps:

1. Set the octal address NNN 200 in the console switch register.

#### NOTE

**The three leading digits of this address defines a core or semiconductor memory area other than the semiconductor memory being calibrated.**

2. Press the console LOAD ADRS switch.
3. Set 13700<sub>8</sub> in the console switch register and press DEP.
4. Place any address from within the semiconductor memory area being calibrated in the console switch register and press DEP.
5. Set 000775<sub>8</sub> in the console switch register and press DEP.
6. Repeat Steps 1 and 2, then press START.



**Table 4-1**  
**Semiconductor Memory Adjustments**

Adjustment	Pin Nos.	Purpose
R42 REQ L LATCH PULSE L	E18 pin 8 to E25 pin 8	Delays start of memory access cycle until address lines are stable.
R7 AH/CENABLE	E25 pin 8 to E25 pin 6	Times the assertion of AH, which, in turn, asserts CENABLE to enable the memory chips addressed.
R9 BL/PRECHARGE	E25 pin 8	Times the assertion of BL, which defines the trailing edge of PRECHARGE to complete recharging of MOS memory prior to accessing.
R11 CH/ACCESS READY LATCH	E25 pin 8 to E27 pin 13	Times the assertion of CH, which asserts ACCESS READY LATCH to implement the current access cycle.
R1 SMCA D L	E25 pin 8 to E55 pin 6	Times the assertion of SMCA D L, which, in turn, asserts SMCA MEM SYNC L. (Effectively controls the start of the write pulse. Figure 3-12.)
R13	E27 pin 8	Adjusts WRITE PULSE HIGH L assertion period.

At this point, a continuous DATI cycle will be performed at the M8110 control to be calibrated. Note that this program originates from a memory area remote from the memory being calibrated so that the test program will be unaffected by the calibration procedure. Upon completion of a calibration procedure, the test program can be terminated by pressing the console HALT switch.

#### 4.2.2 Test Equipment Required

Calibration of M8110 control timing is best performed with a Tektronix 453 oscilloscope or an equivalent equipped with P6000-type probes. Also required for this calibration procedure are three, dual height, DEC W900 multilayer extender boards and two IC chip clips.

#### 4.2.3 Calibration Setup

Before adjusting the semiconductor memory system, perform the following steps:

1. Verify that all semiconductor system modules are properly installed in the correct CPU backplane slots as shown in Drawing E-MU-KB11-A-01 in the *PDP-11/45 System Engineering Drawings*.
2. Visually check modules for such obvious defects as broken wires and connectors.
3. Turn on primary power and verify that the overall computer system is operational.

### 4.3 MEMORY SYSTEM CALIBRATION

The characteristically different operating speeds of MOS and bipolar memory systems, and the resulting difference in timing, requires separate calibration procedures for the system adjustments listed in Table 4-1.

#### 4.3.1 MOS Memory System Calibration

The following procedures delineate all necessary adjustments to an M8110 memory control directing G401 MOS Memory Matrix modules.

**4.3.1.1 Address Set Up, Precharge, CENABLE, and Access Ready Timing Adjustments** – To perform address set up, precharge CENABLE, and access ready timing, proceed as follows:

1. Remove the M8110 control from the processor and install the W900 extender boards in its place.
2. Plug the M8110 control into the W900 extenders.
3. Load the program described in Paragraph 4.2.1.
4. Set the oscilloscope as follows: place SLOPE switch in the minus (–) position; set the SOURCE switch to INT SOURCE; press the INT TRIGGER button on CHANNEL 1 only; set the TIME BASE switch to 20 ns/cm; and set the VOLTS/DIV switch to 0.5 V/cm. All time measurements are made from the –1.5 V point on the displayed waveforms.
5. Locate IC 18 and IC 25 on the M8110 module and place an IC chip on each device.
6. Place the oscilloscope A probe on pin 8 of IC E18 (input); place the B probe on pin 8 of IC E25 (output).
7. Refer to Figure 4-1, which shows the relationship of the oscilloscope A Trace to the B Trace.
8. Locate R42 on the M8110 module and adjust the delay until the leading edge of B Trace occurs approximately 95 ns after the leading edge of A Trace.

**NOTE**

The size of the slotted-head adjusting screw on R42 requires a small screwdriver with a thin blade. Such a tool can be made by grinding or filing the blade of a 3-inch pocket-type screwdriver until it fits the delay-adjusting screw.

9. Remove the oscilloscope probes; attach the A probe to pin 8 of IC E25 and the B probe to pin 6 of IC E25.
10. Refer to Figure 4-1, then locate and adjust R9 until the A Trace shows a 90 ns negative-going waveform,  $\pm 1$  ns.
11. Refer to Figure 4-1, then locate and adjust R7 until the negative-going leading edge of B Trace occurs 70 ns after the negative-going leading edge of the A Trace.
12. Remove the IC chip clip from IC E18 and place it on IC E27.
13. Attach the B probe to pin 13 of IC E27. This is ACCESS READY LATCH H; it is used to define the access time.
14. Refer to Figure 4-1, then locate and adjust R11 until the positive-going leading edge of B Trace occurs 230 ns  $\pm 1$  ns, after the leading edge of A Trace.
15. Remove the IC chip clip from IC E27.
16. Locate IC 55 and place an IC chip clip on it.
17. Attach the B probe to pin 6 of IC 55. Adjust R1 so that the leading edge of the B Trace occurs 240 ns after the leading edge of the A Trace.

### NOTE

Adjustment of R1 for single/double synchronizing.

**M8109 Rev F Etch:** Observe jumpers W6 and W5 on the M8109. If W6 is IN and W5 is OUT, adjust R1 of the M8110 to 240 ns. If W6 is OUT and W5 is IN adjust R1 to 210 ns.

**M8109 Rev C Etch:** If jumpers have been installed on the previously unused half (pins 11, 12, etc.) of the flip-flop at E8 of the M8109, R1 of the M8110 should be adjusted to 210 ns. If the flip-flop is unused, adjust R1 to 240 ns.

18. Remove both IC chip clips from IC 25 and IC 55.
19. Place an IC chip clip on IC 27.
20. Attach probe A to pin 8 of IC 27. Adjust R13 so that the A Trace (SMCA WRITE PULSE HIGH L) shows a pulse width of 60 ns.
21. Remove the probe and the chip clip.
22. Reinstall the M8110 Semiconductor Memory Control in its original connector slot.

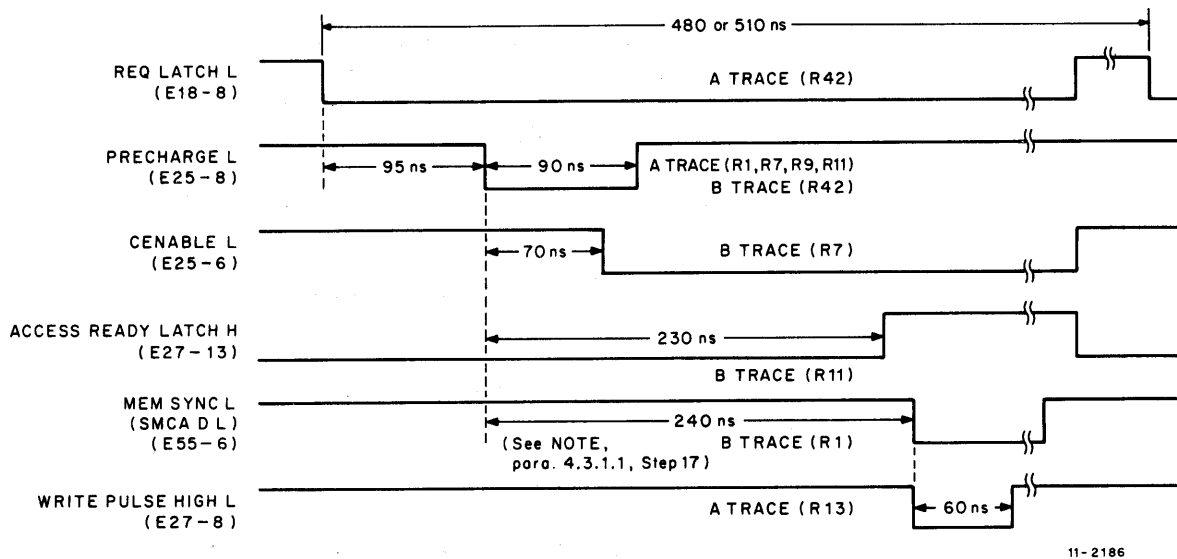


Figure 4-1 M8110 Timing and Termination Delay Adjustment for MOS Memory (Logic Drawing SMCA)

#### 4.3.2 Bipolar Memory System Calibration

The high speed of bipolar memory systems requires that several M8120 control delay adjustments be calibrated differently than for a MOS memory system (M8110). The procedures for these adjustments are exactly the same as the equivalent MOS memory system adjustment, except for the actual duration of the delay.

**4.3.2.1 Address Set Up, Precharge, and Access Ready Timing Adjustments** — To perform address set up, precharge, and access ready timing adjustments, proceed as follows:

1. Remove the M8120 control from the processor and install the W900 extender boards in its place.
2. Plug the M8120 control into the W900 extenders.
3. Load the program described in Paragraph 4.2.1.
4. Set the oscilloscope as follows: Place SLOPE switch in the minus (–) position; set the SOURCE switch to INT SOURCE; press the INT TRIGGER button on CHANNEL 1 only; set the TIME BASE switch to 20 ns/cm; and set the VOLTS/DIV switch to 0.5 V/cm. All time measurements are made from the –1.5 V point on the displayed waveforms.
5. Locate IC 18 and IC 25 on the M8120 module and place an IC chip clip on each device.
6. Place the oscilloscope A probe on pin 8 of IC 18 (input); place the B probe on pin 8 of IC E25 (output).
7. Refer to Figure 4-2, which shows the relationship of the oscilloscope A Trace to the B Trace.
8. Locate R42 on the M8120 module and adjust the delay until the leading edge of B Trace occurs approximately 80 ns after the leading edge of A Trace.

**NOTE**

The size of the slotted-head adjusting screw on R42 requires a small screwdriver with a thin blade. Such a tool can be made by grinding or filing the blade of a 3-inch pocket-type screwdriver until it fits the delay-adjusting screw.

9. Remove the oscilloscope probes; attach the A probe to pin 8 of IC E25.
10. Refer to Figure 4-2, then locate and adjust R9 until the A Trace shows a 60 ns negative-going waveform,  $\pm 1$  ns.
11. Remove the IC chip clip from IC E18 and place it on IC E27.
12. Attach the B probe to pin 13 of IC E27. This is ACCESS READY LATCH H; it is used to define the access time.
13. Refer to Figure 4-2, then locate and adjust R11 until the positive-going leading edge of B Trace occurs 90 ns,  $\pm 1$  ns, after the leading edge of A Trace.
14. Remove the IC chip clip from IC 27.
15. Locate IC 55 and place an IC chip clip on it.
16. Attach the B probe to pin 6 of IC 55. Adjust R1 so that the leading edge of the B Trace occurs 60 ns after the leading edge of the A Trace.

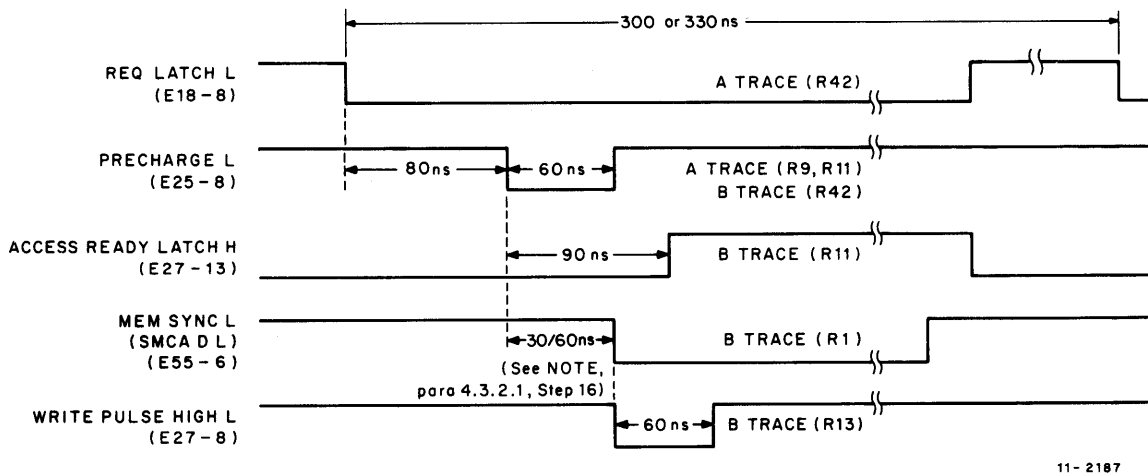
#### NOTE

Adjustment of R1 for single/double synchronizing.

**M8109 Rev F Etch:** Observe jumpers W6 and W5 on the M8109. If W6 is IN and W5 is OUT, adjust R1 of the M8120 to 60 ns. If W6 is OUT and W5 is IN adjust R1 to 30 ns.

**M8109 Rev C Etch:** If jumpers have been installed on the previously unused half (pins 11, 12, etc.) of the flip-flop at E8 of the M8109, R1 of the M8120 should be adjusted to 30 ns. If the flip-flop is unused, adjust R1 to 60 ns.

17. Remove both IC chip clips from IC 25 and IC 55.
18. Place an IC chip clip on IC 27.
19. Attach probe A to pin 8 of IC 27. Adjust R13 so that the A Trace (SMCA WRITE PULSE HIGH L) shows a pulse width of 60 ns.
20. Remove the probe and the chip clip.
21. Reinstall the M8120 Semiconductor Memory Control in its original connector slot.



11-2187

Figure 4-2 M8120 Timing and Termination Delay Adjustment  
for Bipolar Memory (Logic Drawing SMCA)

#### 4.3.3 Cycle Time Adjustment

To perform the cycle time adjustment, proceed as follows:

1. Remove the M8120 (M8110 for MOS) control from the processor and install the W900 extender boards in its place.
2. Plug the M8110/M8120 control into the W900 extenders.
3. With power on, zero the first 200<sub>8</sub> locations (trap vectors) using the following procedure: Set the SR to 0, press the LOAD ADRS switch and DEP switch. Repeatedly press DEP until the address indicators equal 200<sub>8</sub>. The following steps will load 1000<sub>8</sub> locations with MOV R0, R0 instructions.

4. Set SR = 0  
 Press LOAD ADRS switch  
 Set SR = 10000. (MOV R0, R0)  
 Press REG DEP  
 Set SR = 00001<sub>8</sub>  
 Press LOAD ADRS  
 Set SR = XXXXX<sub>8</sub>. The lowest address on the control whose timing is to be checked. If the control uses the lowest memory addresses, then XXXXX<sub>8</sub> should be  $\geq 300_8$ .  
 Press REG DEP  
 (GPR 0 now contains the instruction MOV R0, R0; GPR 1 now contains an address  $\geq 300_8$ .)
5. Set SR = 200<sub>8</sub>  
 Press LOAD ADRS  
 Set SR = 10021<sub>8</sub> (MOV R0, R1+)  
 Press DEP  
 Set SR = 00776<sub>8</sub> (BR.-2)  
 Press DEP  
 Set SR = 200<sub>8</sub>  
 Press LOAD ADRS  
 Place the ENABL/HALT switch in the ENABL position  
 Press START. CPU will run an instant HALTing at location 00002<sub>8</sub>. (All of memory, starting at address XXXXX<sub>8</sub>, is now loaded with MOV R0, R0 instructions.)
6. Place the ENABL/HALT switch in the HALT position.  
 Set SR = XXXXX<sub>8</sub> + 1000<sub>8</sub>. (Address in GPR 1 at Step 4 + 1000<sub>8</sub>)  
 Press LOAD ADRS  
 Set SR = 00137<sub>8</sub>. (JMP instruction)  
 Press DEP  
 Set SR = XXXXX<sub>8</sub>. (Address in GPR 1 at Step 4)  
 Press DEP  
 Press LOAD ADRS  
 Place the ENABL/HALT switch in the ENABL position.  
 Press START  
 (MOV R0, R0 instructions are now executed continuously.)
7. Set the oscilloscope as follows: Place SLOPE switch in the minus (—) position; set the source switch to INT SOURCE; press the INT TRIGGER button on Channel 1 only; set the TIME BASE to 50 ns/cm (100 ns/cm for MOS); set the VOLTS/DIV switch to 0.5 V/cm. All time measurements are made from the +1.5 V point on the displayed waveform.
8. Locate IC E18 on the M8110/M8120 module and place an IC chip clip on it.

9. Place the oscilloscope A probe on pin 8 of IC 18. The period between cycles should be constant at either 300 or 330 ns (480 or 510 ns for MOS). (See Figures 4-1 and 4-2.) If the cycle time fluctuates between 300 and 330 ns (480 and 510 ns for MOS) adjust R42 on the M8110/M8120 until the displayed signal is stable. (Some MOS modules may operate error-free only when adjusted to 510 ns.)
10. Remove the probe and the chip clip.
11. Reinstall the M8110/M8120 Semiconductor Memory Control in its original connector slot.

#### 4.4 SEMICONDUCTOR MEMORY SYSTEM DIAGNOSTICS

The *PDP-11/45 System Maintenance Manual* presents a brief abstract for each diagnostic, describing program function and application.

#### 4.5 MEMORY MATRIX MODULE STRUCTURE

The relationship of G401 MOS Memory Matrix Module ICs to function is shown in Figure 4-3. Figures 4-4 and 4-5 provide similar information for M8111 and M8121 Bipolar Memory Matrix Modules.

##### 4.5.1 Isolation of Malfunctions to Module Component

Various means are available to maintenance personnel to identify the source of memory errors: Signal tracing using the oscilloscope and other test devices, diagnostic software that exercises selected areas of logic, and replacement of suspected modules with identical spares that are known to be operational. The method (or methods) used is determined by such factors as the nature of the problem, availability of on-line time and test equipment, applicable maintenance directives, and instructions from supervisory (maintenance) personnel.

Isolation of memory problems to the module level involves identifying the failing address(es) and determining which module has been assigned this address. As previously described (Paragraph 3.2.1) the jumper configurations on the M8110/M8120 Semiconductor Memory Control(s) and the G401/G401-YA, M8111/M8111-YA and M8121 Memory Matrix Modules determine this memory address assignment (refer to Tables 3-1, 3-2, 3-3, 3-9, 3-12, 3-14, and 3-15). The processor, through software, is able to identify the failing address(es); this is accomplished by such means as the ability to generate and check the parity (odd or even) of data stored in memory and to write 8-bit bytes in addition to 16-bit words. (It should be noted that parity testing operations require the presence of a memory with the parity option.) These selective methods of storage, in conjunction with the processors "error halt" facility, provide a very positive means for processor identification of failing memory address.

Identification of the faulty IC in the memory matrix module is the logical conclusion of this procedure where known data is stored at and read from known locations, with the processor halting when errors are discerned. As indicated in Figures 4-3, 4-4, and 4-5, 256 or 1K word memory areas (high byte and low byte), storage bits, and control circuits are identifiable to the component (IC) level. (The "E" numbers for these ICs can be found on drawings D-CS-G401-1 (MOS), D-CS-M8111-0-1 and D-CS-M8121-YA-1 (bipolar).)

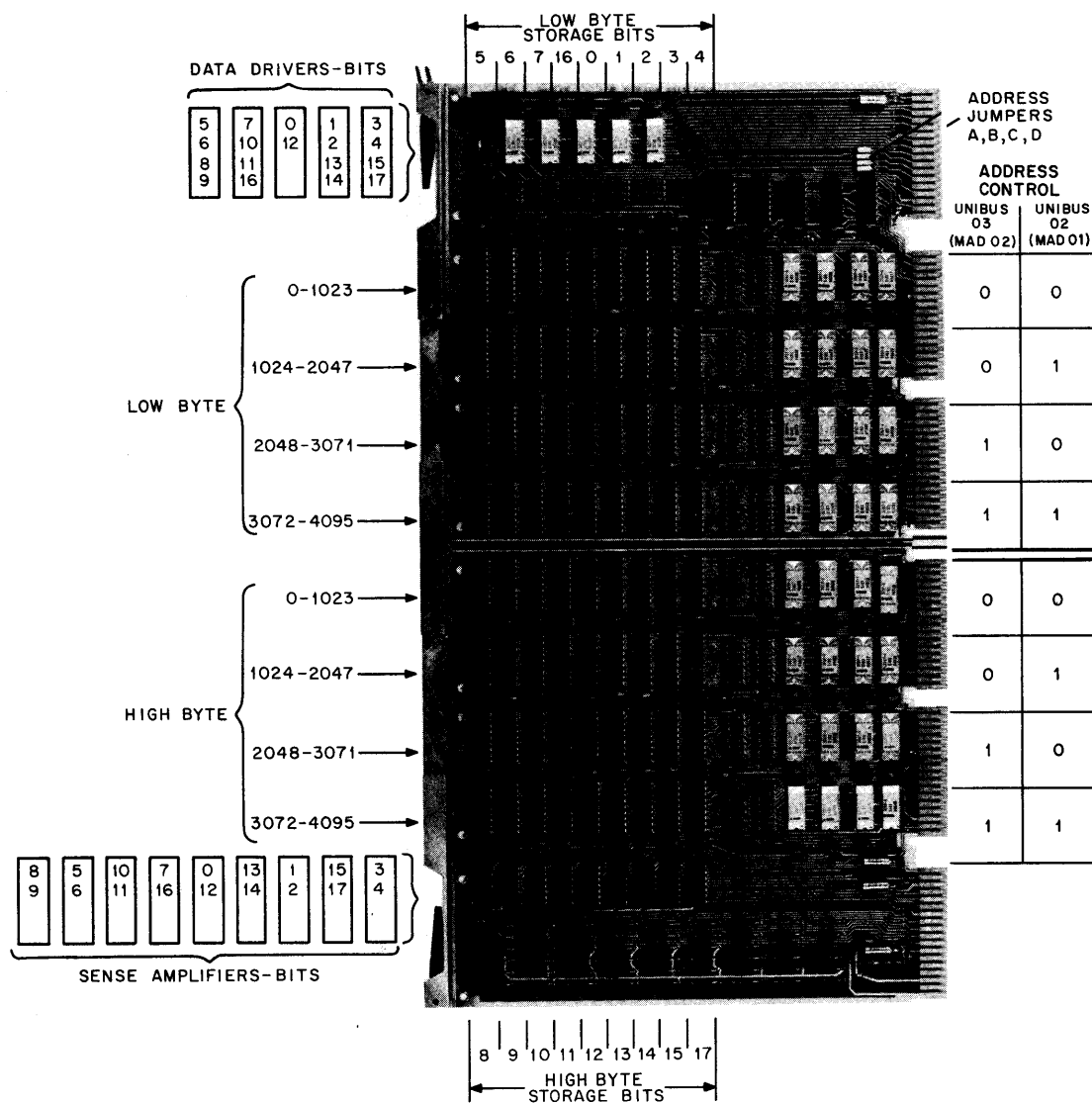


Figure 4-3 G401-YA MOS Memory Matrix Module -- Relationship of ICs to Bits



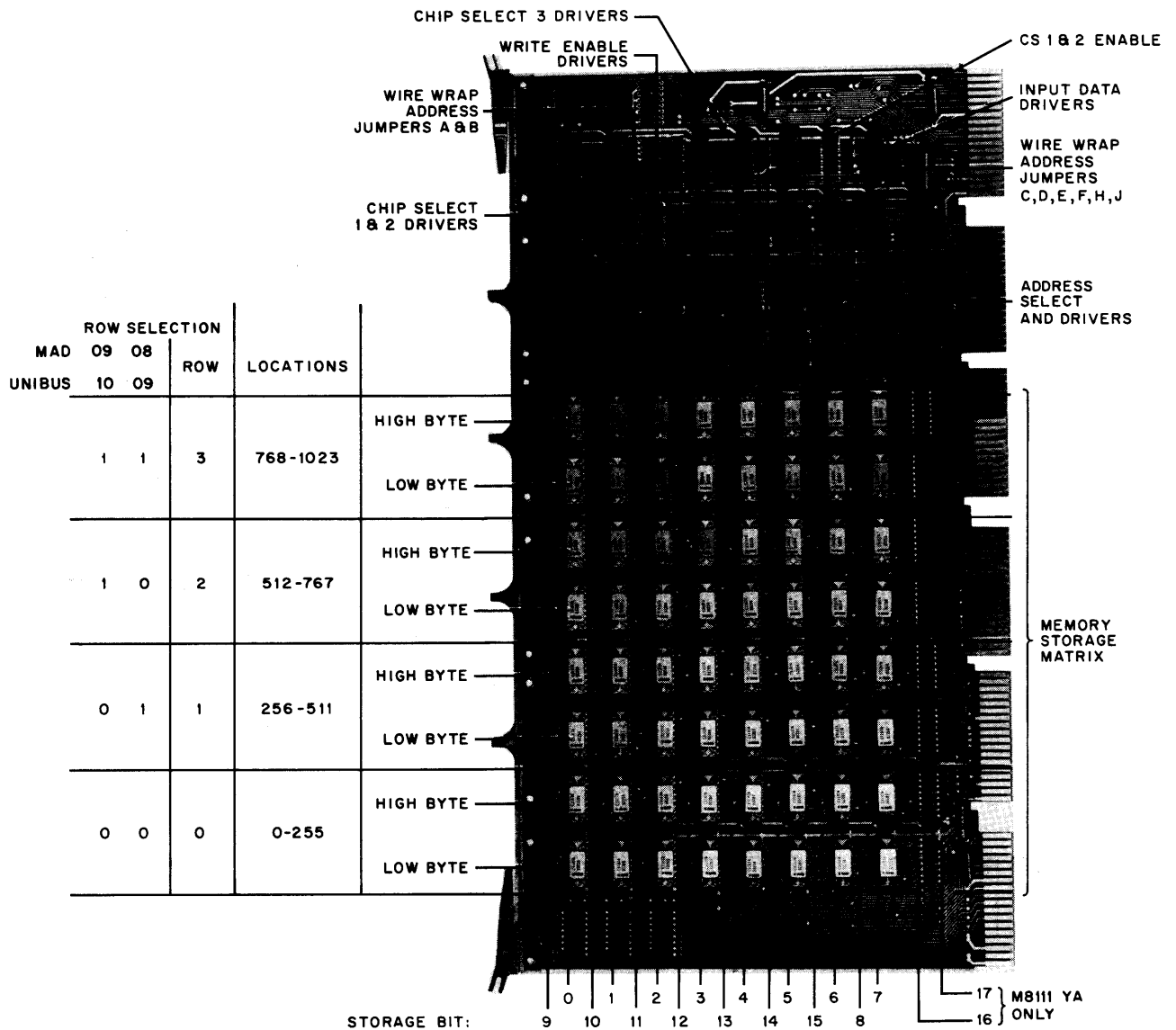


Figure 4-4 M8111 Bipolar Memory Matrix Module –  
Relationship of ICs to Bits

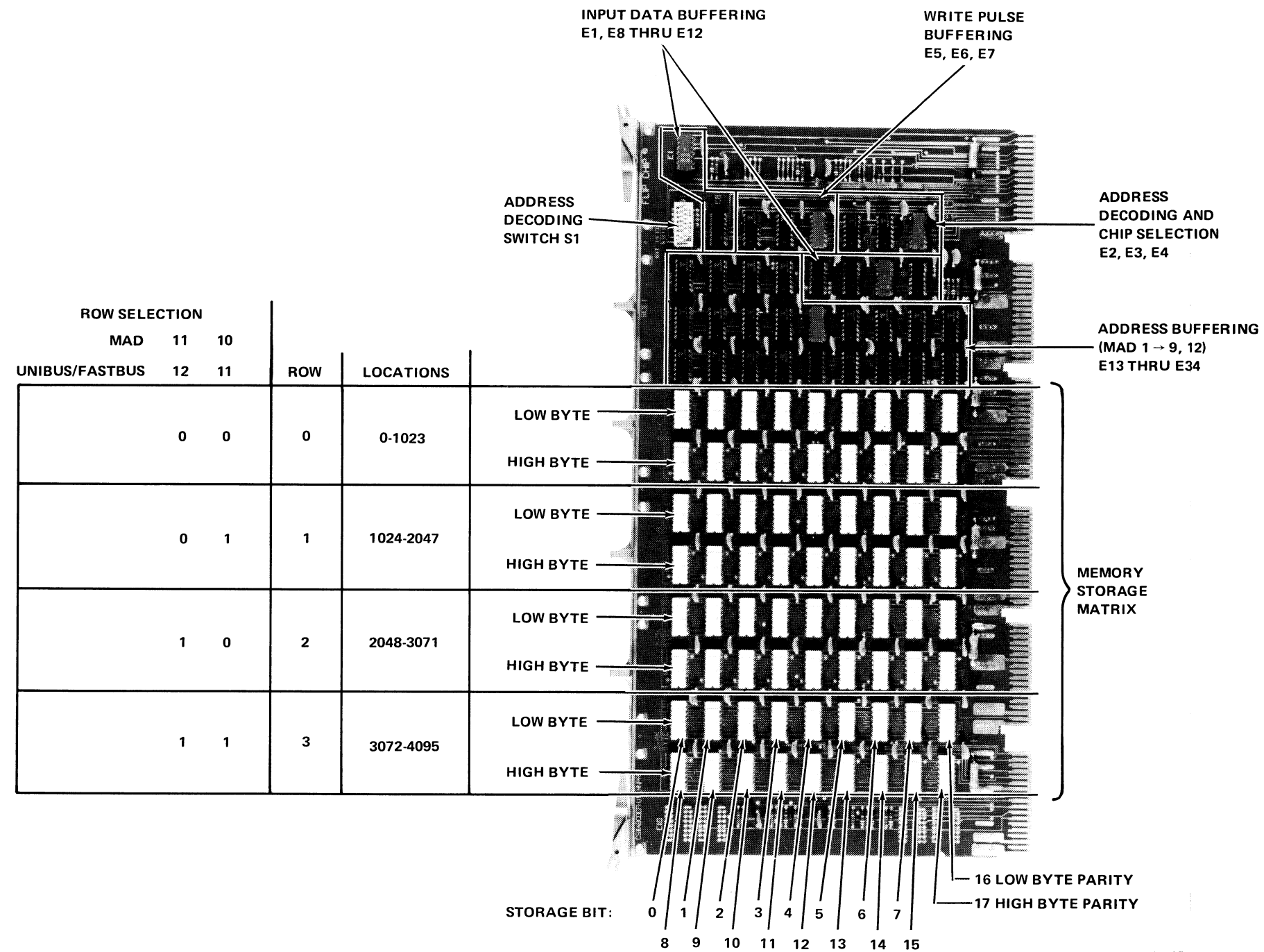


Figure 4-5 M8121-YA Bipolar Memory Matrix Module —  
Relationship of ICs to Bits

# APPENDIX A

## SEMICONDUCTOR MEMORIES

### A.1 INTRODUCTION

The purpose of the following description is to provide the reader with a general overview of the construction, operation, and use of semiconductor memories. It is a general discussion of these devices and does not necessarily reflect the operation of the MOS and bipolar memory modules used in the MS11 Semiconductor Memory system. Bipolar memories are described first, followed by metal-oxide-semiconductor (MOS) storage devices. A basic understanding of transistor terms and operation is assumed.

Various types of semiconductor memories, based on both MOS and bipolar technologies, are presently being used. These memories differ in cost, organization, and performance. In general, MOS technology offers higher density (and is therefore more economical) but lower performance memories than bipolar. The use of dynamic MOS circuits permits retention of data at very low power. Thus, when volatility of memory data is a problem, dynamic MOS devices, with batteries as a back-up power source, are more suitable than bipolar devices.

### A.2 BIPOLAR MEMORIES

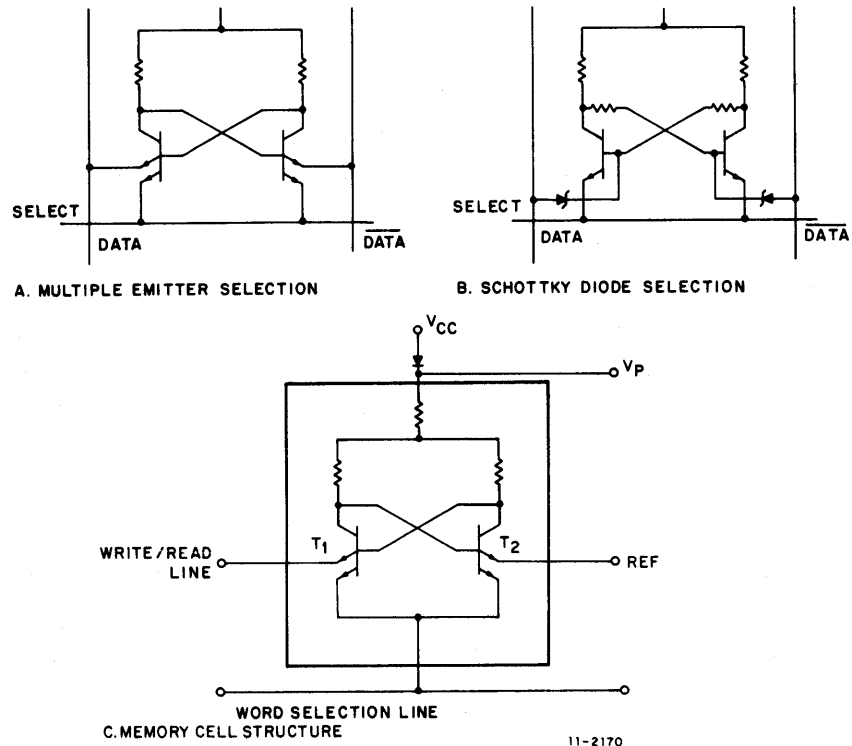
Most bipolar memories use a relatively standard flip-flop as the storage element. Variations in process techniques include the use of an epitaxial layer for resistors and the use of Schottky-barrier diodes to improve response speed and for memory selection. Two basic bipolar memory cells are shown in Figure A-1. Detail A is a cell that uses multiple emitter transistors. In detail B, Schottky diode selection is used.

In the MS11-CC, a monolithic semiconductor bipolar 256-bit memory chip is used as the basic element in fabricating 1024-word random-access-memory (RAM) arrays. (The MS11-AP uses a similar chip containing 1024 bits.)

This high speed 256-bit random-access-memory element is organized into a 1024-word by 18-bit array. On-chip address decoding, along with chip enable, write enable, and uncommitted collector outputs, provide for connection of these memory elements into the larger array. The entire chip, including address decoding, write and sense circuitry, typically dissipates 450 mW. A word is accessible in less than 60 ns, the write recovery time is less than 35 ns, while the write pulse width required is 60 ns.

Each one-bit memory element is a latch flip-flop. This simple form of flip-flop, used for bit storage, comprises two 2-emitter transistors and three resistors. One emitter on each transistor is used for word selection, one emitter remains at a reference voltage, while the remaining emitter is used for writing information into the cell and reading information from the cell (Figure A-1, detail C).

The monolithic memory cell also contains the "write enable" which controls data to be written into the flip-flop, allowing only selected data into the cell when its input is low. No data can be written into the flip-flop when the input to the write enable is high. Conversely, no data can be read out of the flip-flop when the write enable input



11-2170

Figure A-1 Bipolar Memory Cells

is low. The write amplifier will write selected data into the flip-flop only when the write enable input and the chip enable are low. The sense amplifier will only read selected data out of the flip-flop when the chip enable is low and the write enable input is high.

To analyze the memory operation in more detail, a simplified 16-word by 4-bit matrix is used as an example (Figure A-2). Beginning with the read operation, assume that a logic 1 is stored in the flip-flop. This means that transistor  $Q_1$  is on and conducting current. As long as the word selection line is low, the current path will be through this line. However, if the word selection line is high and the write enable line is high, the current will switch to the second emitter and flow down into the appropriate data sense amplifier, activating a logic 1 at the data output of this amplifier.

Now, let us examine the write operation in more detail by writing a logic 0 into the flip-flop. First, chip enable and write enable must be low and the cell is selected through the appropriate binary code at the address inputs. Then, the output to the selected write amplifier is reduced to a low, turning off the output of the amplifier. This will, in turn, raise the voltage on the write/read line to a high, causing transistor  $Q_1$  to turn off and  $Q_2$  to turn on.

Now the flip-flop is said to have a logic 0 stored. In order to write a logic 1 into the flip-flop, the chip enable and write enable remain the same, but in this case, the input to the selected write amplifier is increased to a high. This will, in turn, lower the voltage on the write/read line to a low, causing transistor  $Q_1$  to turn on and  $Q_2$  to turn off.

A reduction in the number of inputs required for this memory element example can be accomplished by the addition of an address decoder (Figure A-3). The addition of a decoder reduces the inputs of this 16-word by 4-bit memory element from 16 address lines to 4. This decoder has five inputs; four inputs,  $A_0$ ,  $A_1$ ,  $A_2$ ,  $A_3$ , act as addresses to produce an output at a corresponding output terminal, while the fifth input, chip enable (C/E), is used primarily in larger memory arrays to select a 64-bit memory element chip. The  $A_0$  input terminal of the decoder is considered the least significant so that an input configuration such as 1000 on inputs  $A_0$ ,  $A_1$ ,  $A_2$ ,  $A_3$ , respectively, will produce a logic 1 on output 1.

To analyze the address decoding operation in more detail, place a logic 0 at the chip enable input and  $A_1$ ,  $A_2$ ,  $A_3$  inputs while placing a logic 1 at the  $A_0$  input (1000). This will cause gate B to turn off and gate C to turn on, resulting in logic 1 at point  $B_0$  and logic 0 at point  $B_1$ , presenting logic 1s at all the inputs of gate 1. Gate 1 will now be turned off, resulting in logic 1 at output 1, while gates 0 and 2 through 15 have at least one logic 0 at their input, leaving their outputs at logic 0 as indicated by the truth table.

Looking further, the truth table shows the  $A_2$  input terminal of this decoder to be the most significant bit. An input configuration such as 1000 on inputs  $A_0$ ,  $A_1$ ,  $A_3$ , respectively, would produce a logic 1 on output 1. An input configuration such as 0001 would produce a logic 1 at output 8.

Now that the various sections of the 64-bit memory array have been discussed, the entire element can be connected together (Figure A-4). To read the sixteenth word out of this 16-word by 4-bit memory element, example, the chip enable and write enable input must be placed at logic 0 and all inputs  $A_0$ ,  $A_1$ ,  $A_2$ ,  $A_3$  must be at logic 1. This code will cause the correct word selection line (15) to go high, resulting in data from all four bit locations of the sixteenth word to be read out simultaneously at  $D_0$ ,  $D_1$ ,  $D_2$ , and  $D_3$  outputs.

To write data into the ninth 4-bit word of this memory element, the write enable input must be placed at logic 0, the chip enable and write amplifier inputs must be at logic 0, and the inputs  $A_0$ ,  $A_1$ ,  $A_2$ ,  $A_3$  must be placed in logic 1, 0, 0, 1, respectively. This configuration will cause the correct word selection line (8) to go high, allowing data at the write inputs ( $W_0$ ,  $W_1$ ,  $W_2$ ,  $W_3$ ) to be written into the four bit locations of this word.

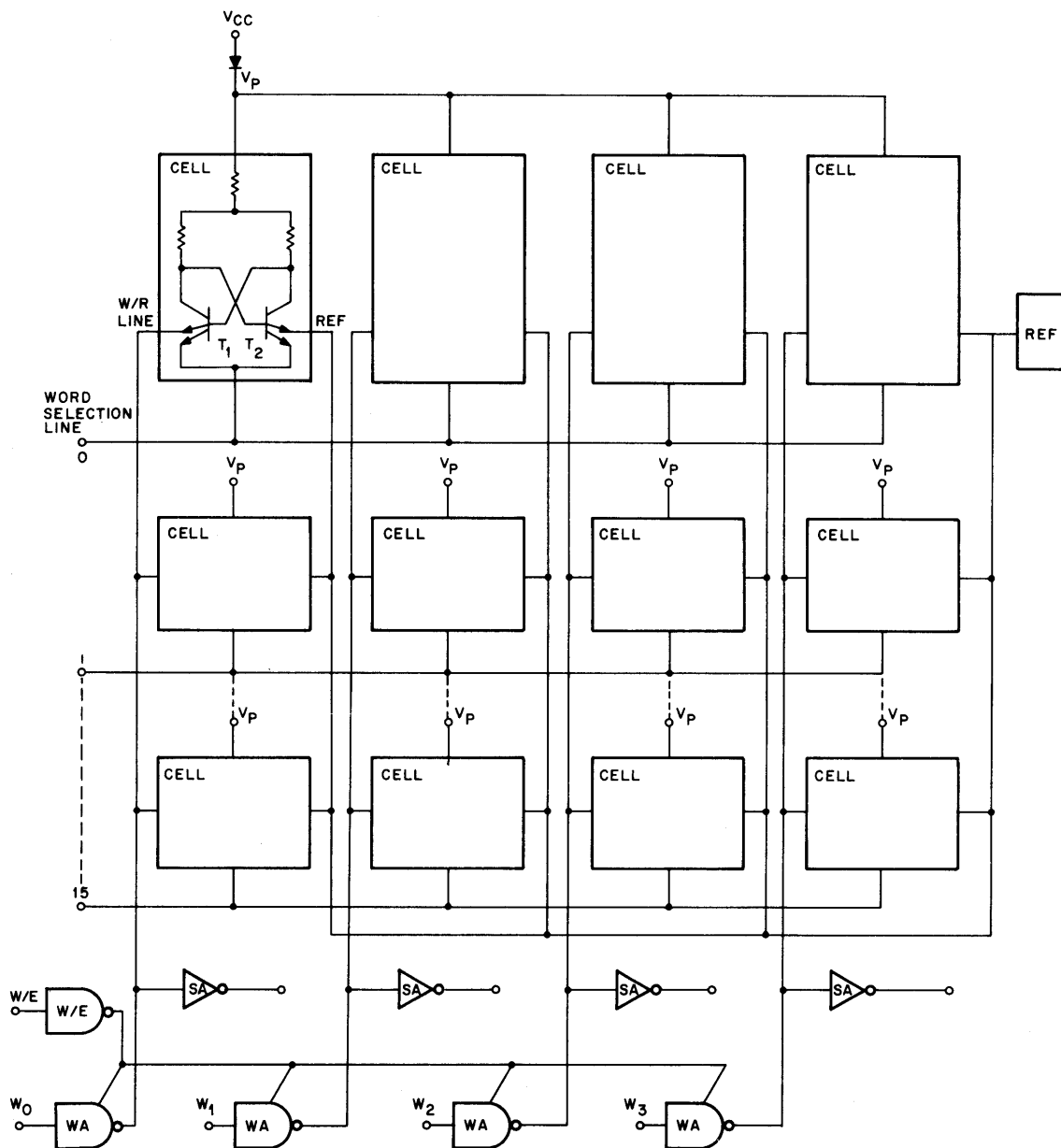
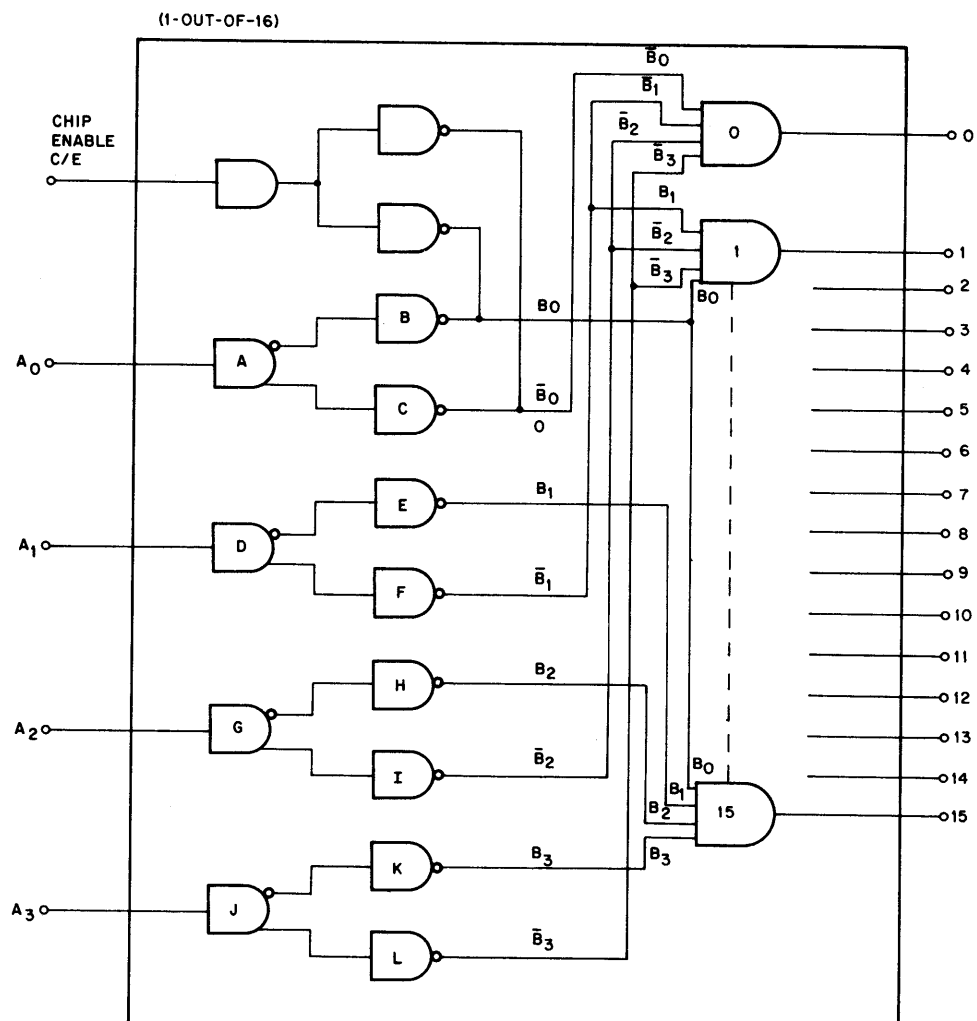


Figure A-2 16-Word by 4-Bit Memory

11-2171



11-2172

Figure A-3 1 Out of 16 Address Decoder (Sheet 1 of 2)

				Truth Table															
Input				Output															
A <sub>0</sub>	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
0	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
0	1	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Figure A-3 1 Out of 16 Address Decoder (Sheet 2 of 2)





A-7

### A.3 MOS DEVICES

One of the most important features of the MOS (metal-oxide-semiconductor) device is its simplicity. An electric field, applied through an oxide-insulated gate electrode, is used to control the conductance of a channel layer of semiconductor material under the gate. The channel is a lightly doped region between two highly doped areas called the source and the drain.

There are four basic types of MOS structure. The channel can be a p- or n-type, depending on whether the majority carriers are holes or electrons, and the mode of operation can be enhancement or depletion, depending on the state of the channel region at zero gate bias. If a conducting channel exists at zero bias, the device is called depletion mode, because current flows unless the channel is depleted by an applied gate field. If a channel must be formed by the gate field before current can flow, the device is termed enhancement mode.

The enhancement mode is attractive in digital circuits, because it provides inherent noise immunity – input voltage must exceed a threshold voltage before the device turns on. This mode is also suitable for self-biasing circuitry schemes, and is used in linear ICs.

Depletion mode devices, on the other hand, which conduct at zero gate voltage, are especially attractive for tuner input stages. The high-impedance gate is simply connected to an antenna coil, and the input signal modulates the conductance between source and drain. Since the depletion mode device is formed of material that has a higher doping level than in the enhancement mode device, and channel mobility is also higher, it can operate at higher frequencies.

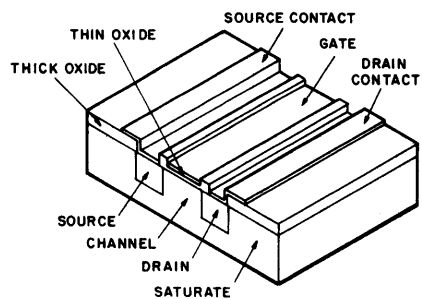
The most common device, the p-type enhancement mode, is built on a substrate of n-type silicon, into which are diffused two p-regions: the source and the drain (Figure A-5, detail A). These are normally formed by diffusing two wells of n-type impurity (phosphorous) into the substrate, and in operation are connected by an induced p-region, which is the channel.

The gate or control element covers the region between the source and the drain and is insulated from the semiconductor material by a layer of silicon oxide. The input resistance of the gate is extremely high – on the order of  $10^{18}$  ohms – and the input impedance at high frequencies is almost purely capacitive. The gate is a layer of metal, usually aluminum, as are the contacts to the source and the drain. Normally the oxide layer under the gate is made much thinner than the protective oxide on the rest of the chip, to enhance the effect of the gate field on the conductance of the channel region.

If the gate, source and substrate are grounded and a negative voltage is applied to the drain, no current will flow between the source and drain because they are isolated from each other by the reverse-biased drain-to-body pn junction.

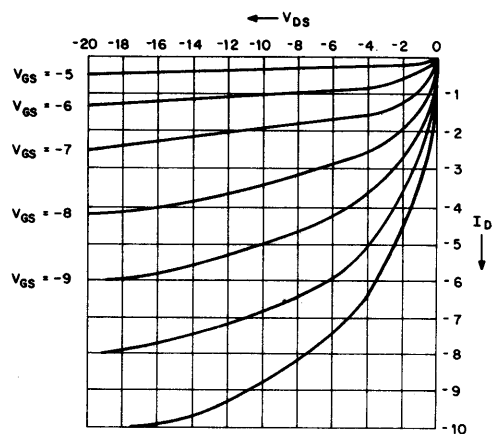
If a negative voltage is applied to the gate, the surface of the n-type silicon inverts, becoming essentially p-type. The negative gate voltage attracts holes from the n-type substrate to the surface. The channel area, very near the surface, initially has an excess of electrons, because the material is n-type, but the holes drawn into the area by the gate field neutralize these electrons. At some gate voltage, the attracted holes just compensate for the excess electrons, and the channel behaves like the intrinsic semiconductor. At higher gate voltages, the holes predominate. The channel area, a few microns deep, is referred to as “inverted” – it now behaves like a p-type semiconductor, providing a current path from source to drain.

The surface region under the gate does not invert, and no conduction can occur until the gate voltage is more negative than the threshold voltage  $V_T$ , which is about  $-5$  V for most p-channel enhancement mode devices. This effect results, in part, from the presence of impurity charge in the silicon, which must be neutralized before the channel region can invert. In general, the thinner the gate oxide, the lower the threshold voltage.



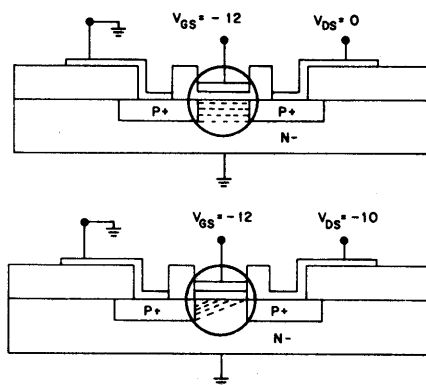
A. THE MOS TRANSISTOR: A SIMPLE CONFIGURATION OF SOURCE, DRAIN AND GATE ELECTRODES.

11-2177



B. THE DC CHARACTERISTIC: CHANNEL CONDUCTANCE IS DETERMINED BY THE GATE-TO-SOURCE VOLTAGE.

11-2178



C. THE SATURATION PHENOMENON: DRAIN TO SOURCE VOLTAGE EFFECTS ARE LIMITED BY CHANNEL PINCH-OFF.

11-2179

Figure A-5 Structure of MOS Devices

As the gate voltage becomes more negative than the threshold  $V_T$ , the conducting channel is formed, and its depth increases with increasingly negative gate voltage. For low-drain current, the channel is an ohmic resistance, and the current,  $I_D$ , is directly proportional to the drain-to-source voltage  $V_{DS}$ . As  $V_{DS}$  becomes more negative, however, the channel saturates, and the current levels off (Figure A-5, Detail B).

The saturation phenomenon is easily understood. Assume that the device is operated with the source grounded and the gate at  $-12$  V. If the drain voltage is zero volts, no current flows, even though a channel exists. As the drain voltage is made negative, current flows from the source to the drain through the resistive channel (Figure A-5, Detail C). The voltage difference between the gate and the body of the device is  $-12$  V at the left and decreases along the length of the channel, due to the resistive voltage drop, to a minimum of  $(-12 - (-V_{DS}))$  at the drain. This voltage difference determines the extent to which a channel is formed in the substrate material.

If the negative voltage  $-V_{DS}$  increases enough, the gate-to-body voltage at the drain  $(-12 - (-V_{DS}))$  approaches the threshold voltage  $V_T$ , and the voltage near the drain is just sufficient to form a channel at that point. If  $V_{DS}$  is made still more negative, the inversion channel terminates short of the drain; the drain current is limited and becomes independent of further changes in  $V_{DS}$ .

#### A.4 MOS MEMORIES

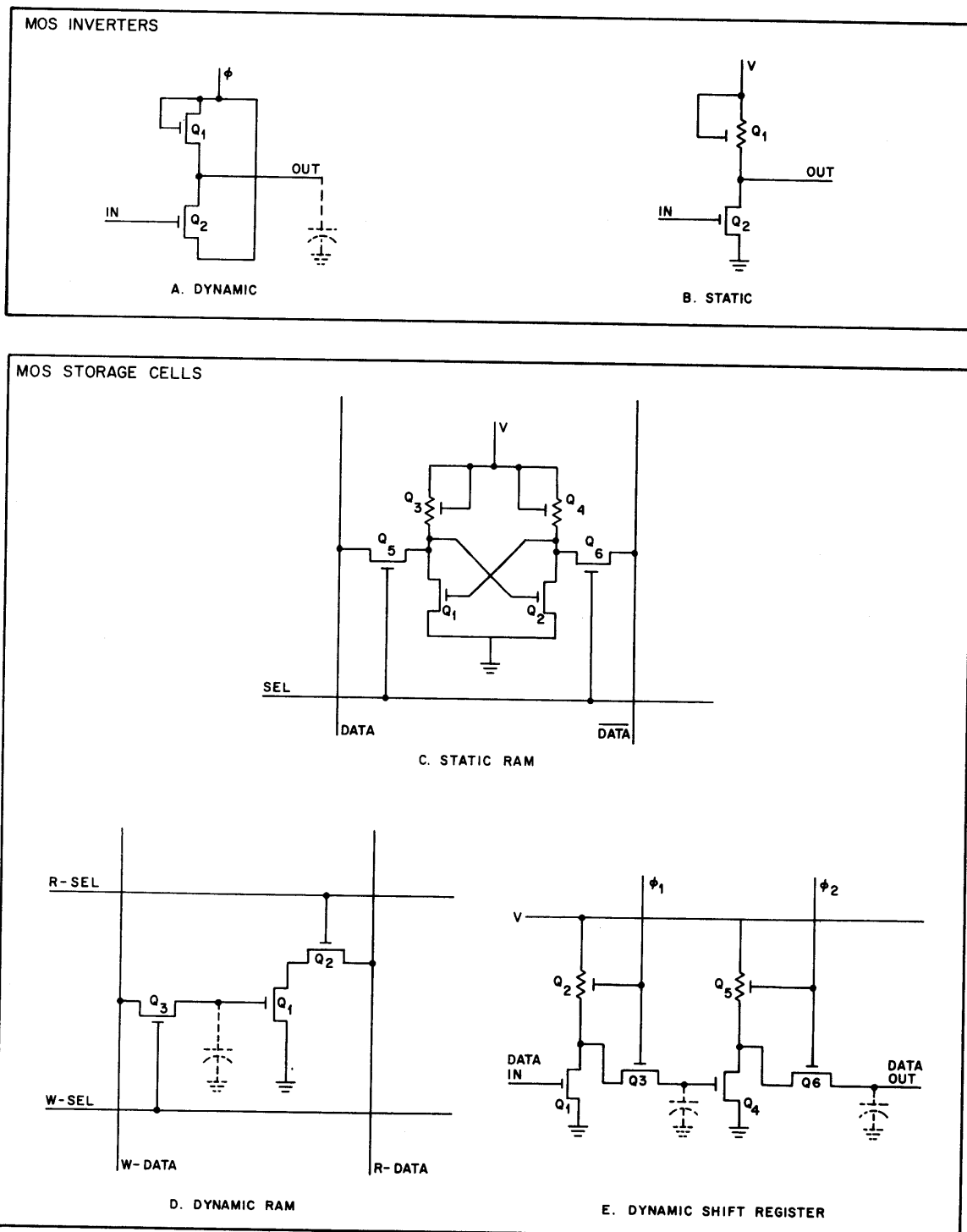
Many different MOS memories are available or in development. Both static and dynamic storage cells may be realized in MOS, and either type of MOS storage may be organized as random-access memory (RAM) or as serial (shift register) memory. Dynamic MOS shift register memories usually offer the lowest cost per bit. Very little chip area is wasted, since the shift register permits small memory cells, requires no decoder, and uses very few leads. Static MOS memories usually show poorer performance and higher costs, but may be easier to drive, for in general, dynamic memories require clock signals in addition to power supplies.

Dynamic MOS circuits, such as those used in the MS11, make use of the very low leakage current associated with the gate circuits and junctions of well-designed MOS devices. These leakage currents are small enough to permit the circuit parasitic capacitances to exhibit time constants from milliseconds to seconds.

To illustrate the basic differences between dynamic and static MOS circuits, a dynamic inverter is compared with a static inverter in Figure A-6, detail A and B.

In the static inverter, a MOS transistor is used for the resistor-like device,  $Q_1$ . When the input signal is a 1 (negative voltage), the output must be a 0. Thus the resistance of  $Q_1$  must be very high when compared with that of the lower transistor,  $Q_2$ , or the output voltage will be too great to be considered a 0. As this resistor device is turned on harder than the lower device, certain geometric relationships between the two devices must be maintained. The resistor must have a long narrow channel, and the lower device must have a short wide channel. As the minimum channel dimension tends to be determined by the minimum tolerance possible, both devices are larger than a minimum-sized device (approximately square channel). In addition, far less current is available for charging an output load capacitance than discharging. Part of the load capacitance is due to the parasitics of the inverter devices. Because these devices are larger than the minimum device, the load capacitance is greater, reducing the speed of the circuit.

In the dynamic circuit, when an input  $\Phi$  goes negative (for p-channel devices) the output is charged, via  $Q_1$ , to a negative potential. The only loads permitted are capacitive (except for junction leakage), so when  $\Phi$  returns to ground potential, the output will remain negative unless  $Q_2$  conducts. Device  $Q_2$  will conduct only if the input is a 1. Therefore, after applying a pulse on line  $\Phi$ , the output, after a short delay, will represent the logical inverse of the input. Because circuit operation does not depend upon the ratio of device resistances, both devices



11-2180

Figure A-6 MOS Memory Circuits

can be of minimum geometry. Thus, some of the tradeoffs between static and dynamic become obvious: the dynamic circuit is less expensive and faster but requires more elaborate drive signals.

The basic MOS storage cells are shown in Figure A-7, details C, D, and E. A static storage cell using transmission gate selection is shown in detail C; a dynamic memory cell for use in random access memories is depicted in detail D; and detail E shows a dynamic shift register stage.

In the static RAM stage of detail C, two static inverters are wired together to make a flip-flop. Devices  $Q_5$  and  $Q_6$  are used as (2-way) transmission gates. When reading, the conducting side of the flip-flop pulls the data line toward ground through these gates. Writing is accomplished by forcing the data lines to the value desired in the cell, thereby overriding the contents of the cell. Because of the small current capability of devices  $Q_3$  and  $Q_4$ , it is important that neither of the data lines be near ground when the transmission gates are turned on, or the charge associated with the capacitance of the data lines may flip the cell.

The organization of a 1024-bit dynamic random-access memory chip employing the memory cell of Figure A-6, detail D, is shown in Figure A-7, detail A.

The dynamic RAM is organized as a 1024-bit memory plane. The input address is fully decoded on the chip. For input/output, a single dual purpose lead is used. Operation of the memory shown consists of transferring the data from one row of cells (as selected by the X address) to the refresh amplifiers, then reading the output of one amplifier (as selected by the Y address). To write, the contents of the refresh amplifiers are rewritten into the rows of cells, and then the contents of the selected cell are changed by the input data.

It can be seen from Figure A-6, detail D that storage within the cell is achieved by charge storage on the parasitic capacitance of the gate circuit of storage device  $Q_1$ . The data may be non-destructively read by precharging the R-DATA lead, then turning on  $Q_2$  with the R-SEL line. If the gate of  $Q_1$  has been charged, the R-DATA lead will be discharged. The refresh amplifier inverts the signal on the R-DATA lead and applies the result to the corresponding W-DATA lead. This data may then be written into the cell by activating the W-SEL lead.

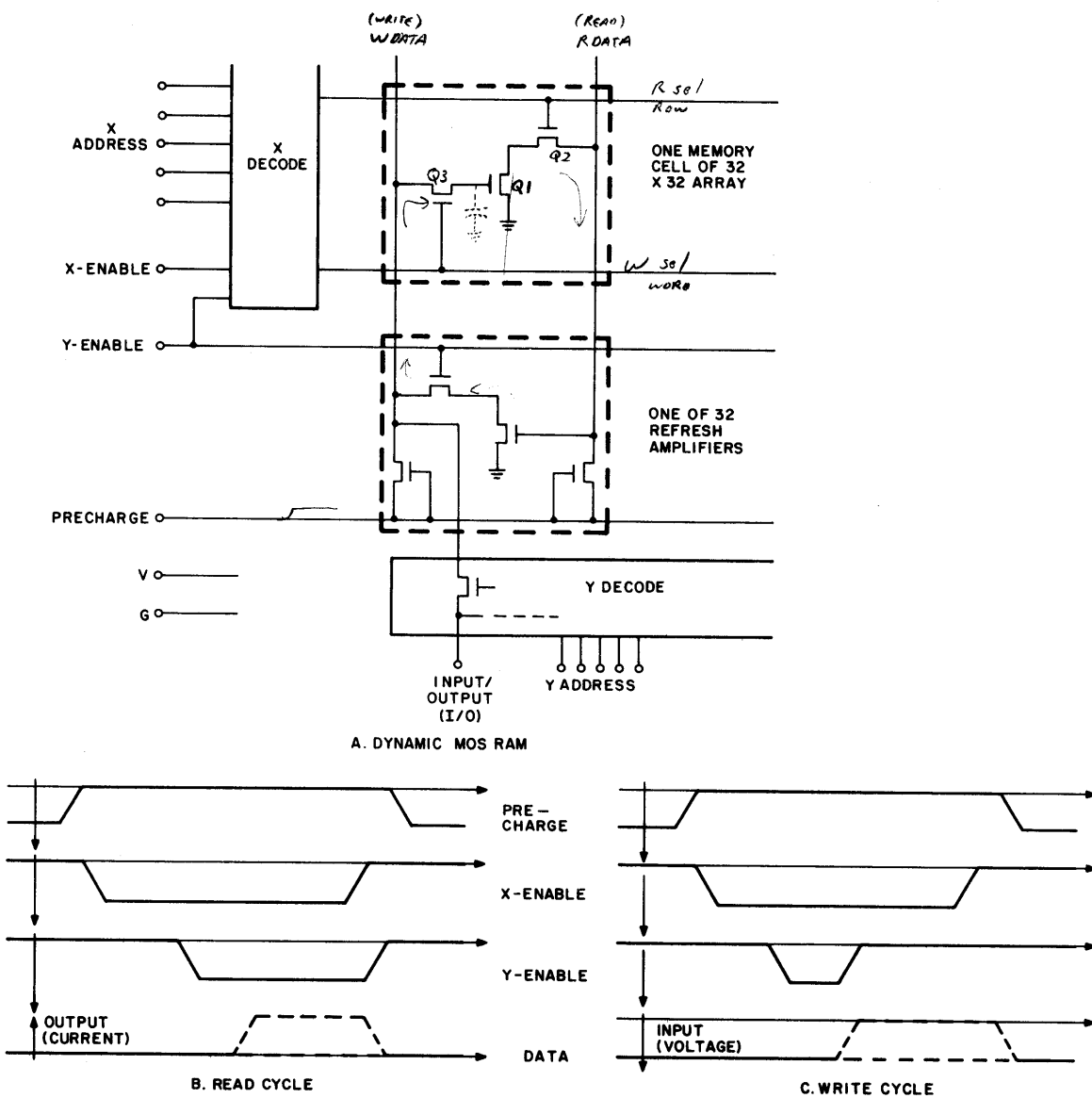
In the organization shown in Figure A-7, detail A, reading and writing occur for all cells of one row simultaneously. Because only one bit at a time is available for writing, an internal read operation must be performed prior to writing, so that the refresh amplifiers contain data corresponding to the contents of the row into which writing will take place.

There are three clock-like signals associated with the dynamic RAM. These are shown in Figure A-7, details B and C. Prior to the start of the cycle, the precharge signal is present (negative), and X and Y enables are absent (at their most positive value). Upon receipt of the address, the cycle starts by removing the precharge signal and then turning on the X enable. After waiting a specified period of time, Y enable may be turned on. After a specified delay, an output current from the device indicates whether the selected bit contained a 1 or a 0. To read this current, the output terminal must be held negative.

If writing is to take place, the Y enable is removed while the X enable remains on. The data to be written is then placed on the data input/output lead. To complete the memory cycle, both X enable and Y enable must be turned off, and then the precharge signal must be turned on for a minimum period before starting the next cycle.

X enable and Y enable both act as a chip select for both reading and writing. Several chips may have the input/output lead OR-tied to build larger than 1024-bit planes.

Using silicon-gate MOS technology, the clock signals and addresses are nominally 20 V peak-to-peak. Memory cycle times depend upon chip organization and drive signal rise and fall time.



11-2181

Figure A-7 Dynamic MOS RAM Circuits

#### A.4.1 Refresh Action

The memory array must be driven by a control circuit which includes provision for refresh action. Because the storage in the memory cells is dynamic, the data must be periodically read from the cells and rewritten. With the chip organization shown in Figure A-7, detail A, executing a read/refresh cycle restores the data in one row of cells. To refresh the entire chip, 32 refresh cycles must be executed, i.e., one for each of the 32 possible X address states.

To accomplish refresh action, a refresh controller may be constructed and attached to the memory as a high-priority cycle-stealing device. Since the longest time a cell may retain data without refreshing is approximately 1 ms, the cycle-stealing refresh control should steal one cycle every 1/32 ms, or approximately one cycle every 30  $\mu$ s. The stolen refresh cycles operate the X address states in sequence so that in any 1 ms period, all cells are refreshed. To refresh the entire memory, the decoding associated with the X enables (and precharge, etc.) is overridden. Data on the data lines is ignored during these refresh cycles.

Refresh cycle control need not be provided if the memory is operated sequentially with a high enough cycle rate. Other refresh control techniques may also be used. For example, separate circuits, either analog or digital, may be provided to determine which X address rows have not been refreshed by normal operation. In general, this technique is more expensive. Even if all refresh cycles can be saved, the total represents only 1 percent of the available memory time.



## APPENDIX B

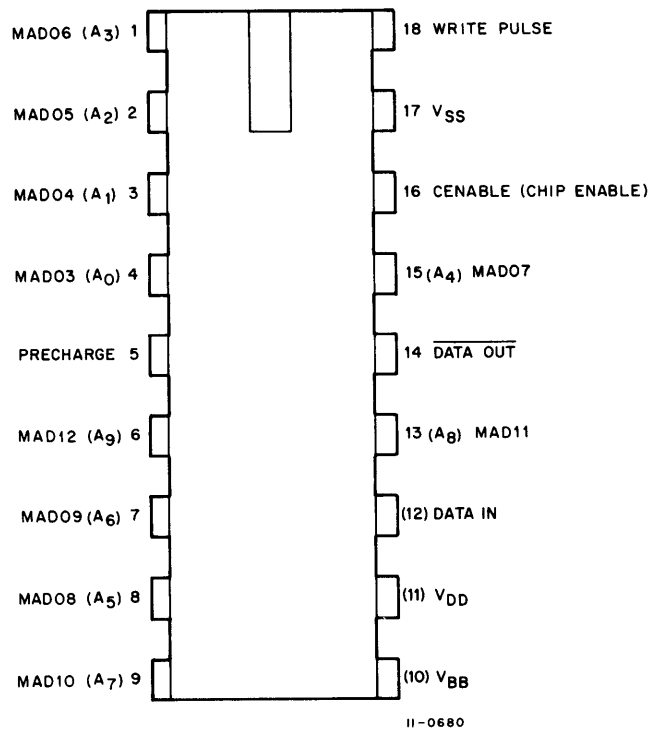
# INTEGRATED CIRCUIT DESCRIPTIONS

This appendix contains descriptions of integrated circuits used only in the M8110, M8111, or G401 modules. Descriptions of other integrated circuits used throughout the PDP-11/45 System, as well as in the MS11 Semiconductor Memory System, are provided in Appendix A of the *PDP-11/45 System Maintenance Manual*.

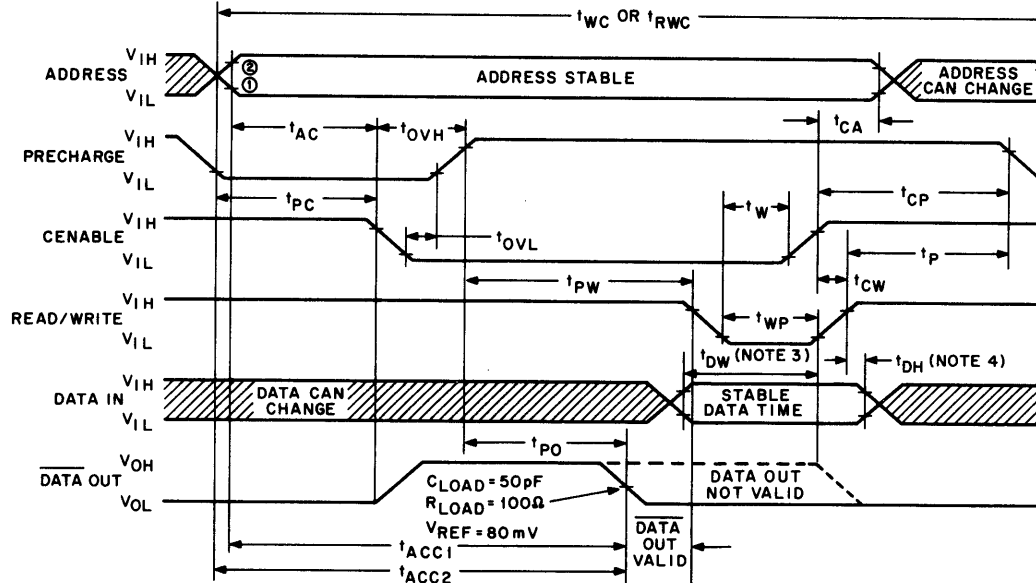
### 1103 RANDOM ACCESS 1024-BIT MEMORY

The 1103 random access 1024-bit dynamic metal-oxide semiconductor (MOS) memory is an MSI circuit characterized by high speed and extremely low power dissipation. The circuit is organized as a  $1024 \times 1$ -bit memory with integral address decoding, OR-tie capability at the outputs, and integral refresh logic. Data, once written, is read non-destructively. Refreshing of all 1024 bits in a circuit is accomplished in 32 read cycles, which are required every 2 ms. Data written into an 1103 memory is inverted when read so that a high, when written, is read as a 0 current, and a low, when written, is read as 0.9 mA (typical).

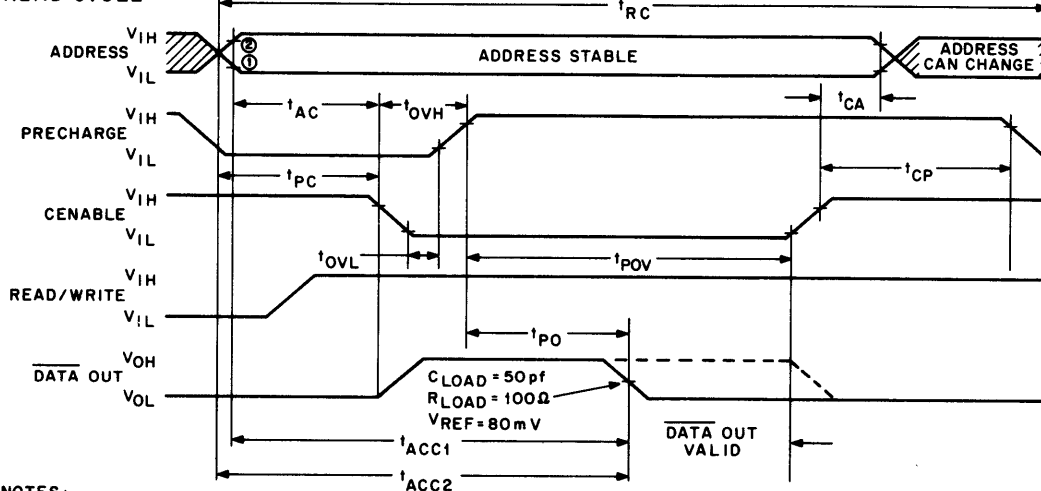
With reference to the block diagram and timing diagrams, access begins  $T_{AC}$  before the negative transition of CENABLE. During this period, PRECHARGE is active, and the address becomes stable in row and column decoders. After the CENABLE transition, the contents of the 32 cells along the selected row are written into the 32 on-chip refresh amplifiers, one of which is required for each column in the array. At the positive transition of PRECHARGE, the contents of the refresh amplifiers are written back into their respective columns, and the output appears  $T_{PO}$  later.  $T_{PW}$  after the positive edge of PRECHARGE, new data on the data input lead may be written into the selected cell, using a READ/WRITE pulse of minimum duration  $T_{WP}$ .



# WRITE CYCLE OR READ/WRITE CYCLE



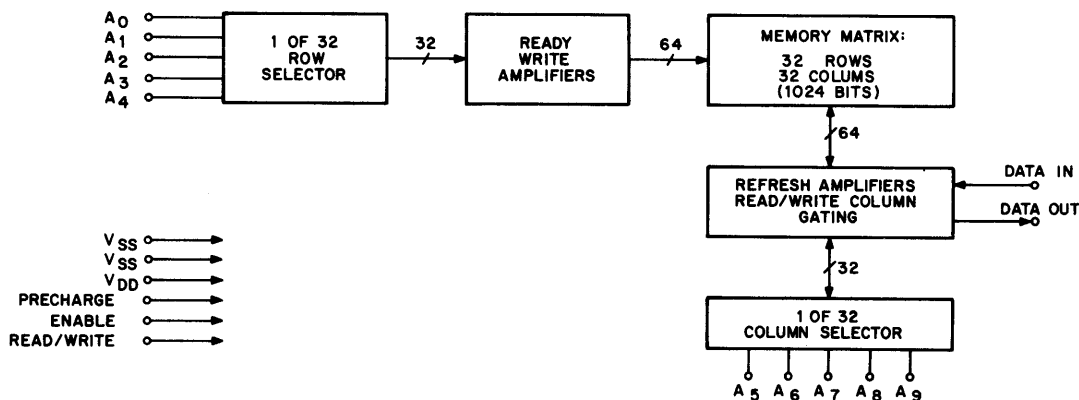
## READ CYCLE



### NOTES:

- ①  $V_{DD} = 2V$
- ②  $V_{SS} = 2V$
- $t_t$  is defined as the transitions between these two points.
3.  $t_{DW}$  is referenced to point ① of the rising edge of chip enable or read/write, which ever occurs first.
4.  $t_{DH}$  is referenced to point ② of the rising edge of chip enable or read/write, which ever occurs first.

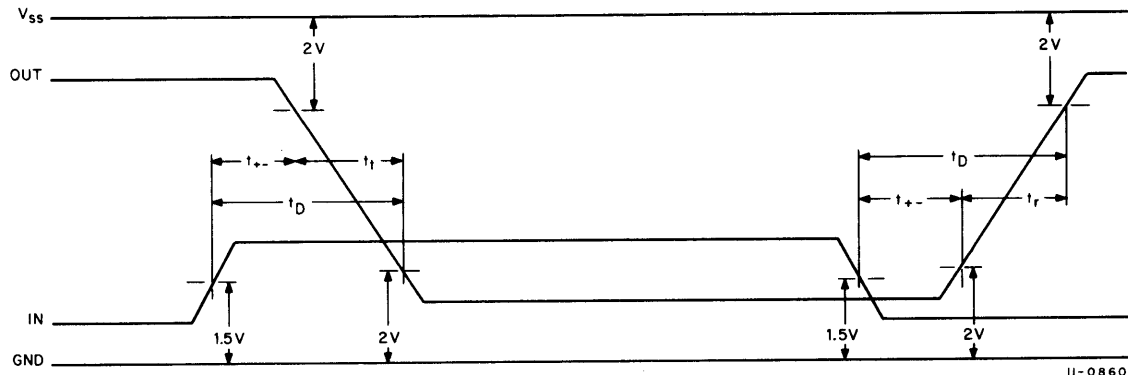
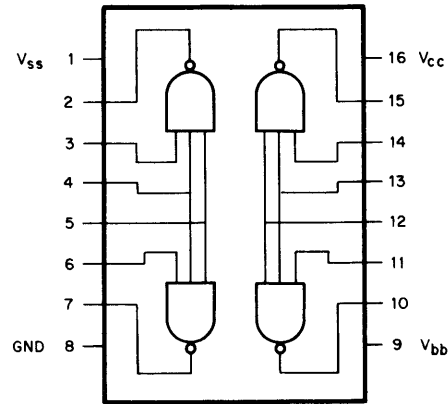
11-0859



11-0882

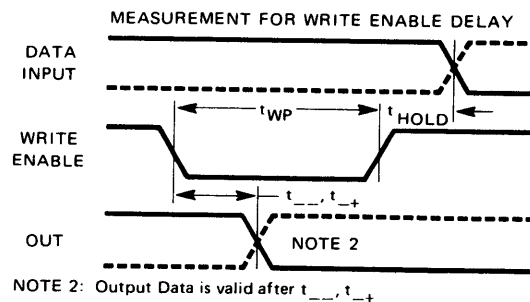
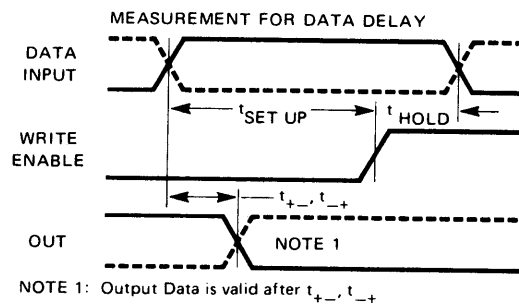
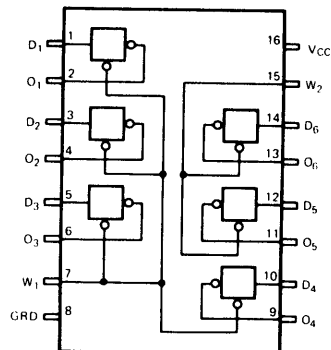
### 3207 QUAD 3-INPUT NAND TTL/MOS LEVEL SHIFTER

The 3207 TTL/MOS level-shifting integrated-circuit NAND gate provides an operational interface between TTL control circuits and MOS data storage circuits. Each gate in a unit is enabled by the coincidence of three +3V input levels. Enabled output is +19V. Inputs are connected so that each group of two gates has two common inputs with one unique input for each gate. This connection scheme permits cascaded level-shifting logic structures which are conditioned in common by the coincidence of several control levels, with the output of each gate being enabled by a single input.



### 3404 HIGH SPEED HEX LATCH

The individual latching elements in the 3404 6-bit high-speed latching circuit are organized as separate 4-bit and 2-bit latches with each section having a common write line. This device is directly compatible with both DTL and TTL logic and provides an output sink capability of 10 mA minimum. The latches in this device can also act as high-speed inverters when the write input is held low.



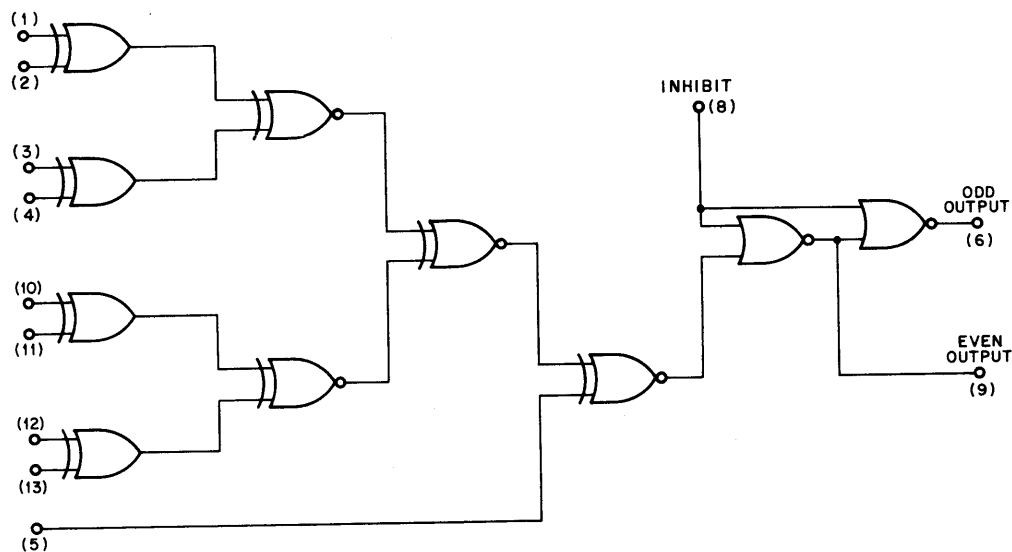
## 82S62 9-BIT PARITY GENERATOR AND CHECKER

The 82S62 9-Input Parity Generator/Parity Checker is a versatile MSI device commonly used to detect errors in data transmission or in data retrieval two outputs, EVEN and ODD, provide versatility. The INHIBIT input disables both outputs of the 82S62 (a logic 1 at the INHIBIT input forces both outputs to a logic 0).

When used as a parity generator, the 82S62 supplies a parity bit which is transmitted together with the data word.

Read data is input to the 82S62 when it is used as a parity checker. The outputs then indicate that data has been received correctly or that an error has been detected.

LOGIC DIAGRAM



11-2184

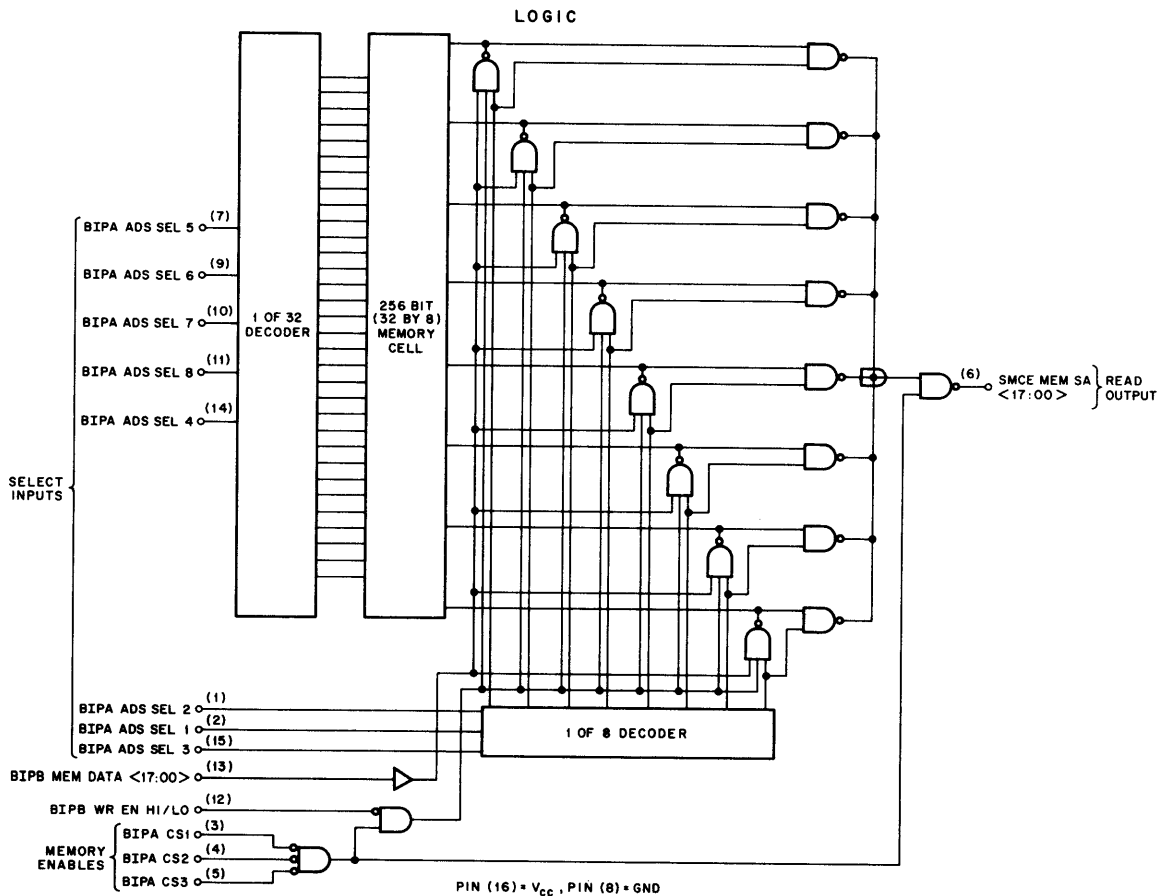
## 74200 BIPOLAR 256-BIT RANDOM ACCESS MEMORY

The 74200 integrated-circuit memory is a high-speed, fully decoded, static bipolar 256-bit RAM, organized as a  $256 \times 1$ -word memory. The circuit contains integral write and sense amplifiers with sense amplifier output being uncommitted collector output. Each circuit is addressed through the ADS SEL 1 to ADS SEL 8 inputs which select one of the 256 words. A circuit is enabled by placing all three CS inputs to logic 0. If the WR EN HI/LO (write enable) is at logic 0, the data at pin 13 is written into the addressed word in the complementary form. When WR EN HI/LO returns to logic 1, the data that was written can be read out. However, a bit as read is the complement of the same bit as written. The figure below shows the functional logic for one bit (a single IC on the M8111 module). Pin numbers are shown in parenthesis.

### RATINGS

#### Tri-State Drive:

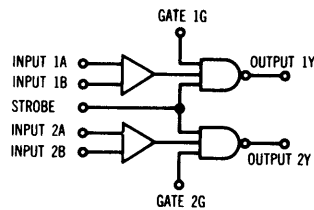
$I_{OH}$ —High Level ON @ $V_{OH}$	-10 mA (min)	Input load factor	0.67
Output OFF @ $V_{off}$	$\pm 40 \mu A$ (max)	$P_T$ (typical)	510 mW
$I_{OL}$ —Low Level ON @ $V_{OL}$	16 mA (min)	Access Time (typical)	40 ns
$V_{OH}$ minimum @ $I_{OH}$	2.4 V	Enable Time (typical)	20 ns
$V_{off}$ (forced)	0.4 to 2.4 V	Sense Recovery Time (typical)	30 ns
$V_{OL}$ maximum @ $I_{OL}$	0.4 V	Write Pulse Width (typical)	20 ns



11-1316

## 75107/75108 DUAL-LINE RECEIVERS

The 75107 and 75108 dual-line receivers are linear integrated circuits consisting of two independent channels per circuit. Each receiver channel is formed by a differential input stage, a level shifting stage, and a TTL NAND gate output stage. The 75107 NAND gate stage provides the familiar totem pole output; the 75108 provides an open collector output at the NAND gate stage for wire-ORing.



TYPICAL CHARACTERISTICS		DIFFERENTIAL INPUT VOLTAGE	HIGH-LEVEL INPUT CURRENT	MAXIMUM COMMON-MODE INPUT VOLTAGE RANGE	TOTAL POWER DISSIPATION	PROPAGATION DELAY TIME (DIFFERENTIAL INPUTS)
		mV	$\mu$ A	V	mW	ns
75107	DUAL LINE RECEIVER WITH (TTL) GATE OUTPUT	3	30	$\pm 3$	134	17
75108	DUAL LINE RECEIVER WITH (OPEN-COLLECTOR) GATE OUTPUT	3	30	$\pm 3$	134	19

11-1074

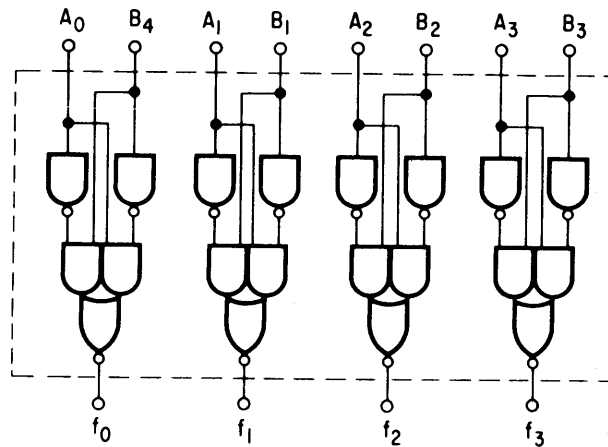


### 8242 EXCLUSIVE-NOR 4-BIT DIGITAL COMPARATOR

The 8242 digital comparator circuit consists of four independent exclusive-NOR gates with each gate structure having an open collector output to permit multiple bit comparisons. A 4-bit comparator network is formed by connecting the independent outputs; such a network is easily expanded by cascading the outputs.

TRUTH TABLE

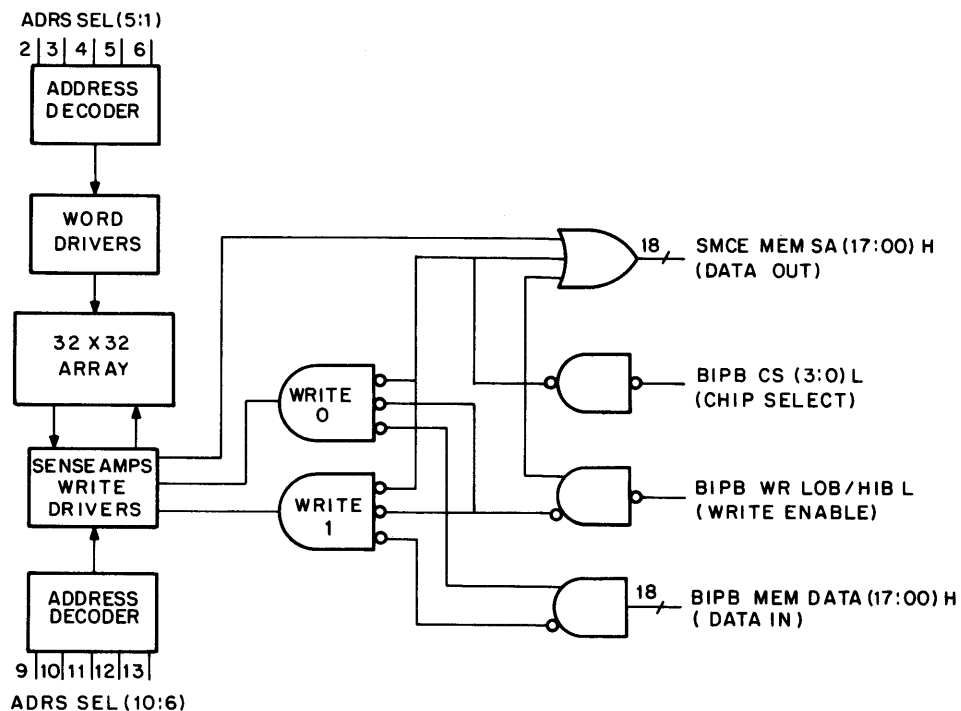
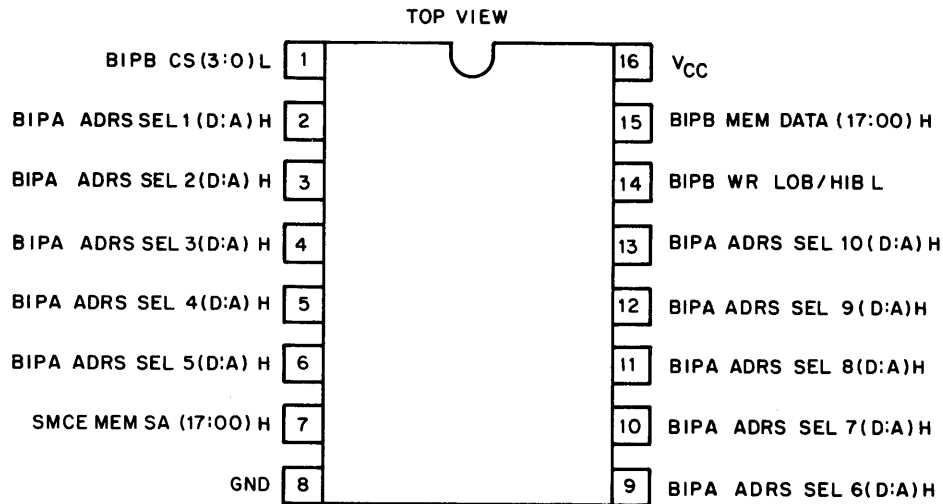
A	B	f
0	0	1
1	0	0
0	1	0
1	1	1

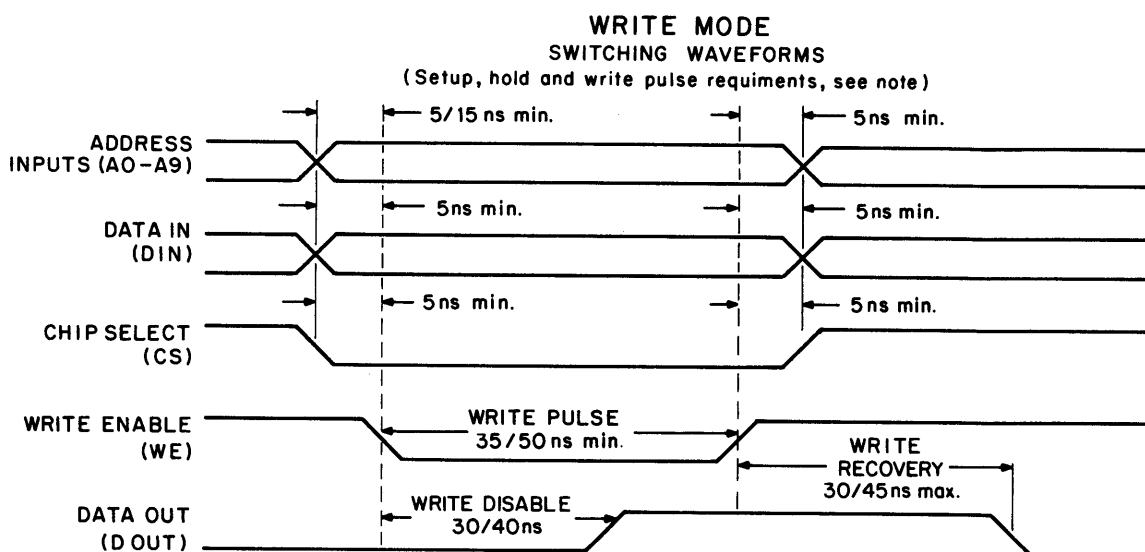
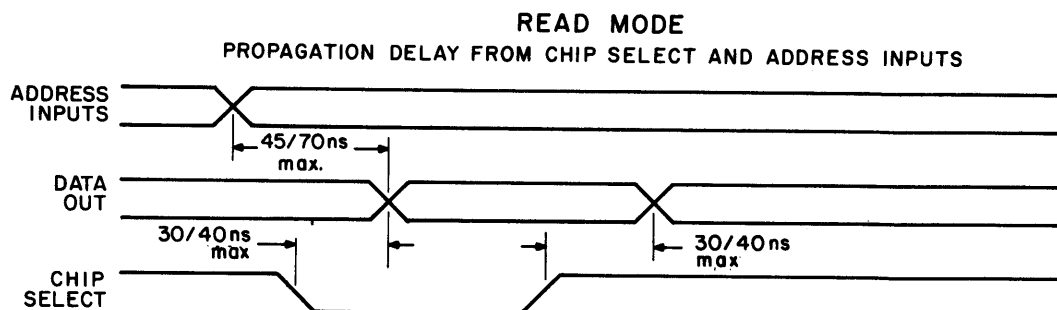


## 82S10/93415 1024-BIT RANDOM ACCESS MEMORY

The 82S10/93415 random access 1024-bit bipolar memory is organized as a 1024 X 1 word memory. It is fully compatible with standard DTL and TTL families. Bit selection is achieved by means of a 10-bit address input BIPA ADRS SEL (10:01) A, B, C, D, H, pins 2–6, 9–13. A chip select (CS) input (BIPB CS (3:0) L, pin 1) provides for memory array expansion; the fast chip select time permits the decoding of CS from the address without affecting system performance.

The read and write operations are controlled by the state of the active *low* write enable (WE) input (BIPB WR LOB/HIB L, pin 14). With WE held low and the chip selected, the data (BIPB MEM DATA (17:00) H, pin 15) is written into the addressed location. To read data at a memory location, WE is held high and the chip is selected. Noninverted data (SMCE MEM SA (17:00) H) is then read out to pin 7.





**NOTE:**  
If two times are indicated the shorter one is for the -01 variation and the longer one is for the -00 variation.

TRUTH TABLE

INPUTS			OUTPUT	MODE
$\overline{\text{CS}}$	WE	D <sub>IN</sub>	OPEN COLLECTOR	
H	X	X	H	NOT SELECTED
L	L	L	H	WRITE 0
L	L	H	H	WRITE 1
L	H	X	D <sub>OUT</sub>	READ

H = HIGH VOLTAGE LEVEL  
L = LOW VOLTAGE LEVEL  
X = IRREVELANT

11-3624



MS11-A, B, C  
MEMORY SYSTEMS  
MAINTENANCE MANUAL  
EK-MS11A-MM-006

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What features are most useful? \_\_\_\_\_

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CUT OUT ON DOTTED LINE

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**Fold Here** -----

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**Do Not Tear - Fold Here and Staple** -----

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