pdp11

MK11 MOS memory technical manual

digital

EK-0MK11-TM-001

MK11 MOS memory technical manual

digital equipment corporation • maynard, massachusetts

1st Edition, June 1978

Printed in U.S.A.

This document was set on DIGITAL's DECset-8000 computerized typesetting system.

CONTENTS

CONTENTS (Cont)

CONTENTS (Cont)

FIGURES

FIGURES (Cont)

TABLES

CHAPTER 1
INTRODUCTION

1.1 MEMORY SYSTEM OVERVIEW

1.1.1 General Description

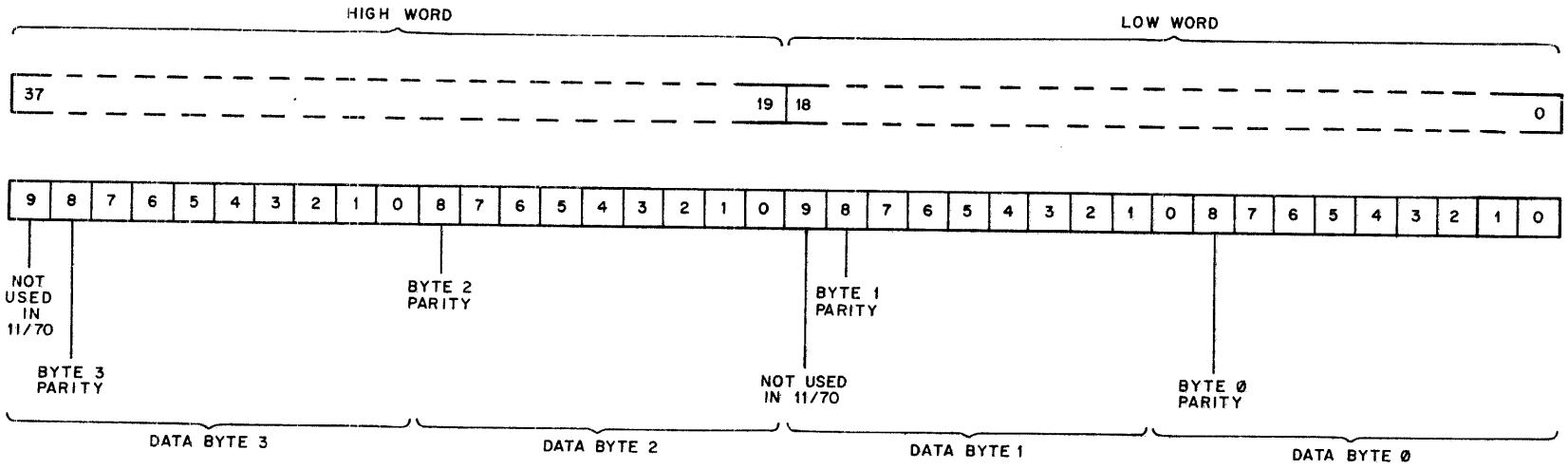
The MK11 provides up to 4 megabytes of main memory storage for the PDP-11/70 system. Dynamic MOS random-access arrays store the data as 39-bit double-word blocks. Each double word consists of 4 8-bit bytes and 7 internally generated check bits. The memory's error correction scheme uses the 7 check bits to reconstruct any 1 erroneous bit detected in the 39-bit double word and detect any double-bit errors.

The memory interfaces to the PDP-11/70 cache memory via the main memory bus. In PDP-11/70 systems, the cache is the sole bus master for the memory. Data transfers to and from the cache are formatted as shown in Figure 1-1. Cache memory selects which word or bytes to be accessed by placing a 22-bit address plus 4 mask bits on the main memory bus. The 22-bit address selects the double word and the mask bits select the desired byte(s). Two control bits (C1 and C0) determine the type of operation performed on the addressed memory location. The various combinations of the control bits, MAIN C0 and MAIN C1, and the corresponding operations are listed below.

C1	C0	Operation
0	0	Read
0	1	Not used (defaults to read)
1	0	Write
1	1	Exchange

Read – A read operation transfers a 36-bit double word from main memory to cache. The double word consists of 4 data bytes and 4 parity bits. The data stored in the addressed memory location remains unaltered. Prior to the transfer, the double word is checked for errors. Seven check bits are generated for the double word taken from the storage arrays. These are checked against the 7 check bits stored with the double word producing syndrome bits which detect any errors in the data. Single-bit errors are corrected before the transfer; double-bit errors are flagged as bad parity on all 4 bytes transferred to cache.

Write – A write operation transfers data from cache to main memory. Any combination of from 1 to 4 bytes may be transferred. For a 4-byte write operation, the memory accepts the data and generates the 7 error-correction-code check bits. The double word and its associated check bits are then stored in the storage arrays. Any data previously stored in the addressed memory location is lost. For a 1- to 3-byte write operation, the memory executes an internal read-modify-write cycle. During this cycle, the memory accepts the byte(s) transferred from cache and latches the byte(s) in a register. The memory then reads the data stored in the addressed memory location into a register and checks it for errors. The transferred byte(s) modify the byte(s) in the register to form a new double word. Error-correction-code check bits are generated for the double word and then the memory writes the modified word into the storage arrays.



NOTES
BIT 9 OF DATA BYTES 3 AND 1 ARE IMPLEMENTED ON THE MAIN MEMORY BUS BUT ARE NOT USED IN THE PDP-11/70.
BIT 8 OF EACH DATA BYTE IS THE BYTE PARITY BIT IN PDP-11/70 APPLICATIONS.

11-2986

Figure 1-1 Data Format

Exchange – An exchange operation swaps data between cache and main memory. Just as in a write operation, the cache may transfer any combination of from 1 to 4 bytes. The cache, however, receives a full 4-byte double word. The memory accepts the data from cache and latches the data in a register. Then it reads the addressed double word to cache as in a read operation. If the cache sends from 1 to 3 bytes, an internal read-modify-write cycle combines the byte(s) in the register with the addressed double word and generates new check bits. If the cache sends 4 bytes, check bits are generated for those 4 bytes. The storage arrays store the double word and its associated check bits, completing the exchange.

1.1.2 Packaging

The MK11 main memory system is packaged in three separate assemblies (Figure 1-2): the BA11 box, the box controller, and the battery backup units. The three assemblies mount in a 48.26 cm (19 in) memory cabinet.

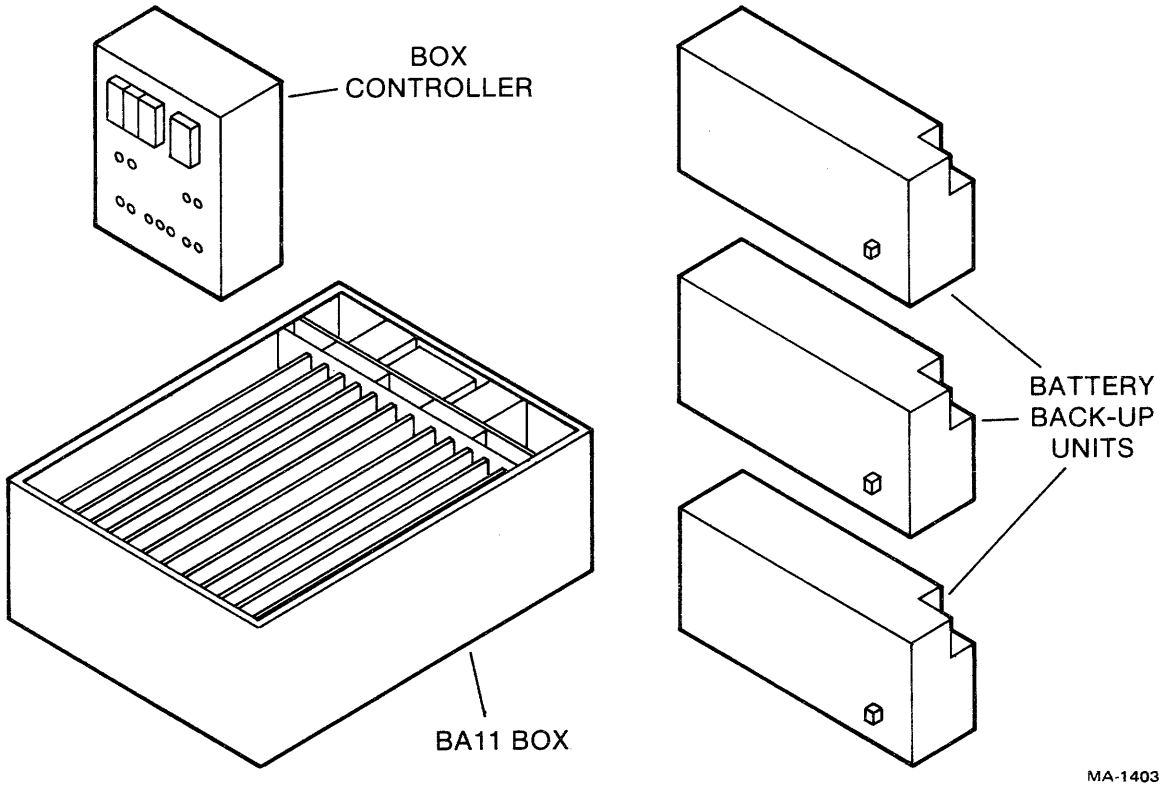


Figure 1-2 Major Assemblies

BA11 Box

The BA11 box (Figure 1-3) houses the memory system's power supply and regulators, and the buffer, control, and storage-array module printed circuit boards. A 26-slot multilayer backplane forms the bottom of the box. The front of the box is open to allow air flow. The box takes up 26.7 cm (10-1/2 in) of cabinet space and mounts in the memory cabinet on slide rails. These slide rails extend the box from the cabinet and tilt to three positions for access to the printed circuit boards, power supply, and backplane wire-wrap pins.

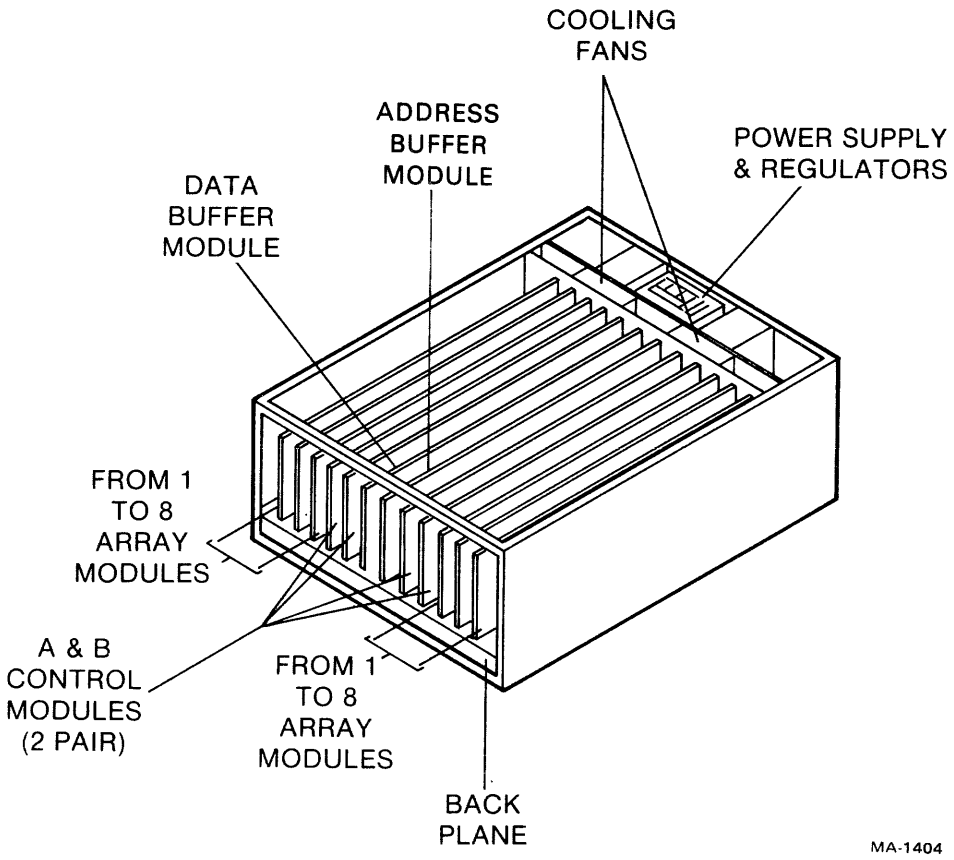


Figure 1-3 BA11 Box

The four power supply regulators mount in the rear of the box, two on either side of the transformer. Two fans, positioned between the regulators and the backplane, force air among the printed circuit boards and across the regulators. The printed circuit board modules slide into the box on guides and plug into the backplane. Tab locks secure these modules inside the box.

Box Controller

The BA11 box controller houses the memory system's operator and maintenance control switches and indicators. One box controller controls one BA11 box. Up to four controllers mount on a panel which mounts in the memory cabinet. Unused mounting locations on the panel are covered with blank panels.

Battery Backup Units

The battery backup unit is packaged in a 13.3 cm (5-1/4 in) chassis which mounts in the memory cabinet. The chassis contains two 12 V batteries and battery-charging and voltage-regulating circuitry. Each BA11 box requires three battery backup units. These units provide ride-through protection during line transients. The batteries will supply power to refresh the memory for a minimum of 5 minutes.

1.1.3 Memory System Configurations

The basic MK11 MOS memory system consists of a memory cabinet, a BA11 memory box, a box controller, and three battery backup units. The memory box may contain from 64K to 512K words, depending on the number of array modules installed. A typical basic system is shown in Figure 1-4. The memory cabinet is always positioned to the right of the processor cabinet.

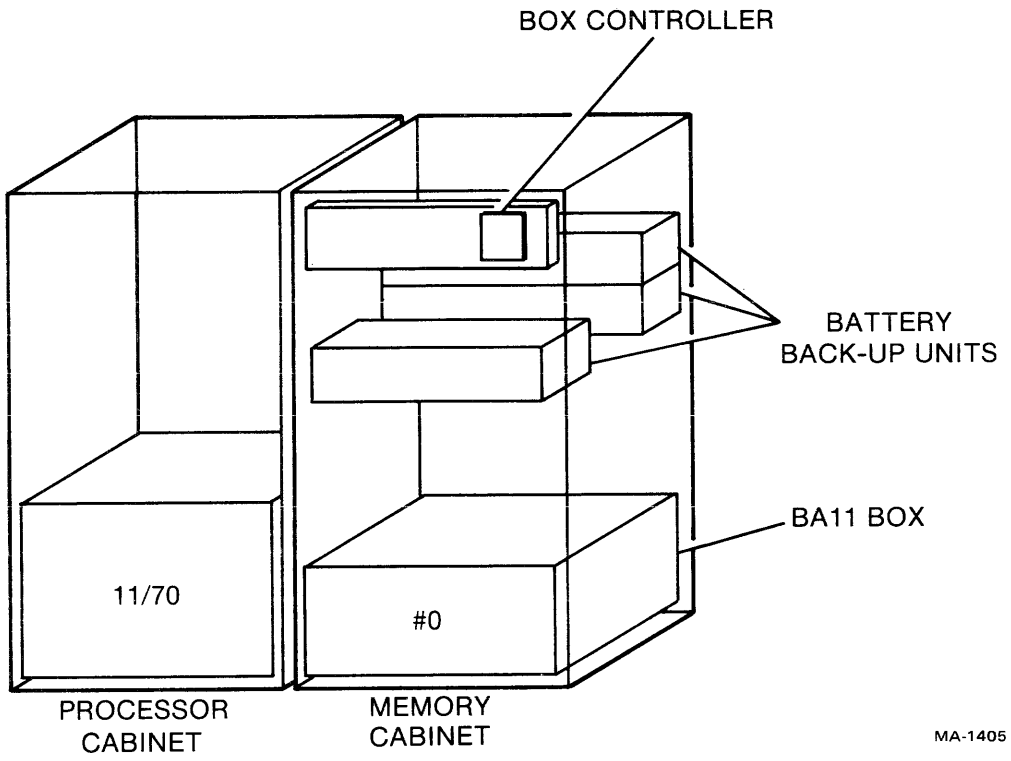


Figure 1-4 Basic Memory System

Expanded memory systems can have storage capacities of up to 2 million words. Each additional memory box adds one more box controller and three more battery backup units. Memory cabinets accommodate one or two BA11 boxes and their controllers and battery backup units. Examples of expanded systems appear in Figures 1-5 and 1-6.

1.1.4 Options

Numeral	Option Includes
11/70 MK (for 115 Vac)	PDP-11/70 processor Processor cabinet Memory cabinet Main memory bus cable A (Figure 1-7) and bus terminators Boot enable cable BA11 memory box* with 64K words MOS memory Box controller, mounting panel, and cables Three battery backup units and cables
11/70 ML (for 230 Vac)	Same as 11-70 MK but for 230 Vac operation
MK11-BC (for 115 Vac)	Memory cabinet Main memory bus cable C (Figure 1-7) BA11 memory box* with 64K words MOS memory Box controller, mounting panel, and cables Three battery backup units and cables

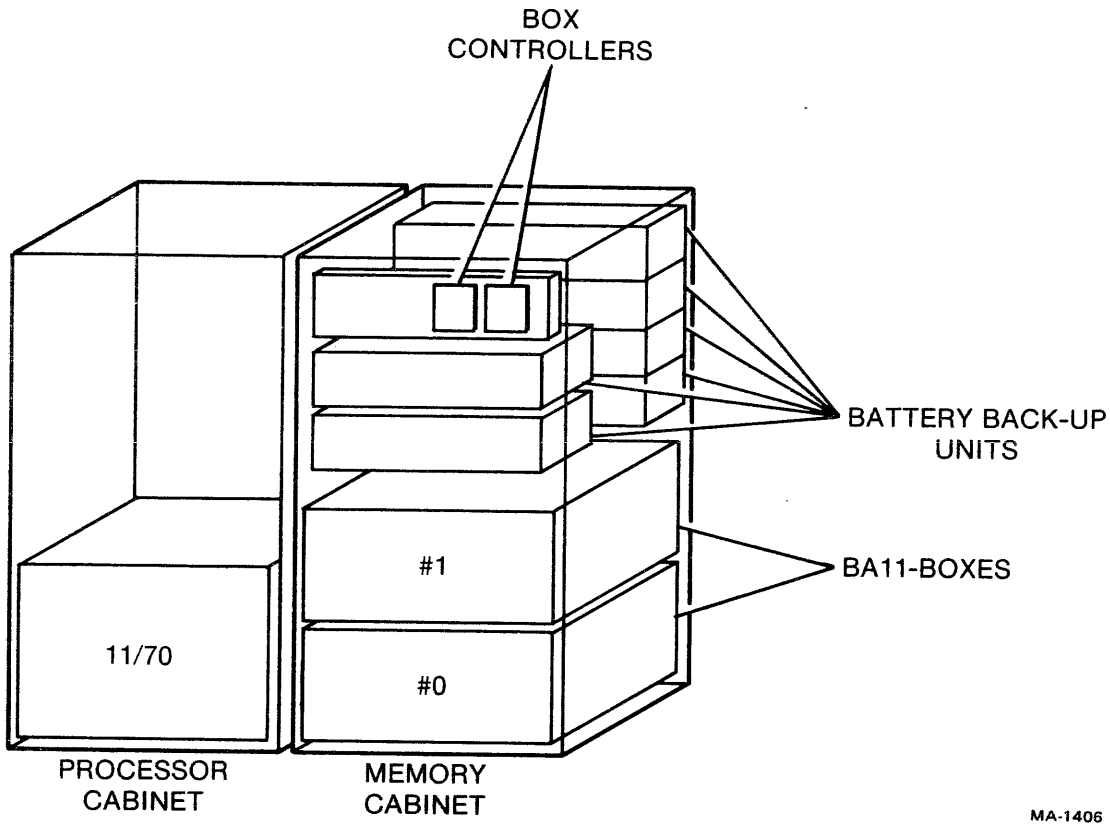


Figure 1-5 Expanded Memory System

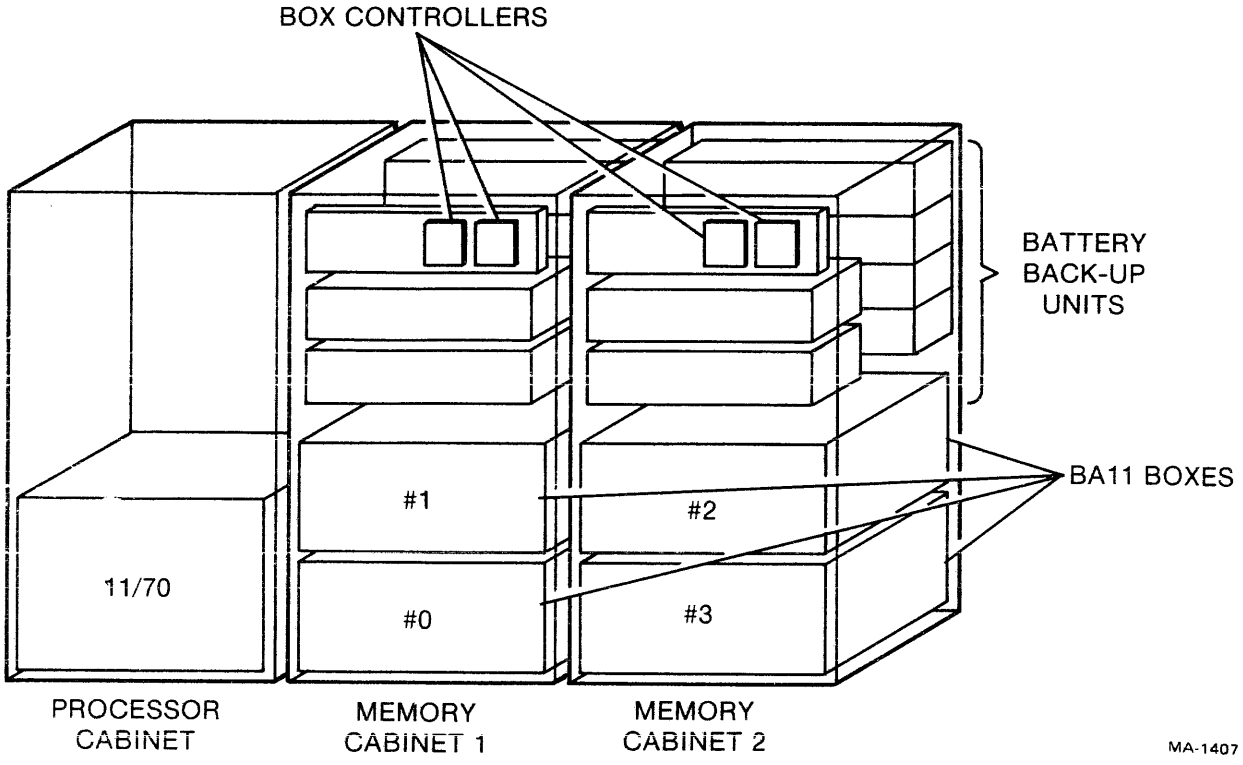


Figure 1-6 Expanded Memory System with Two Memory Cabinets

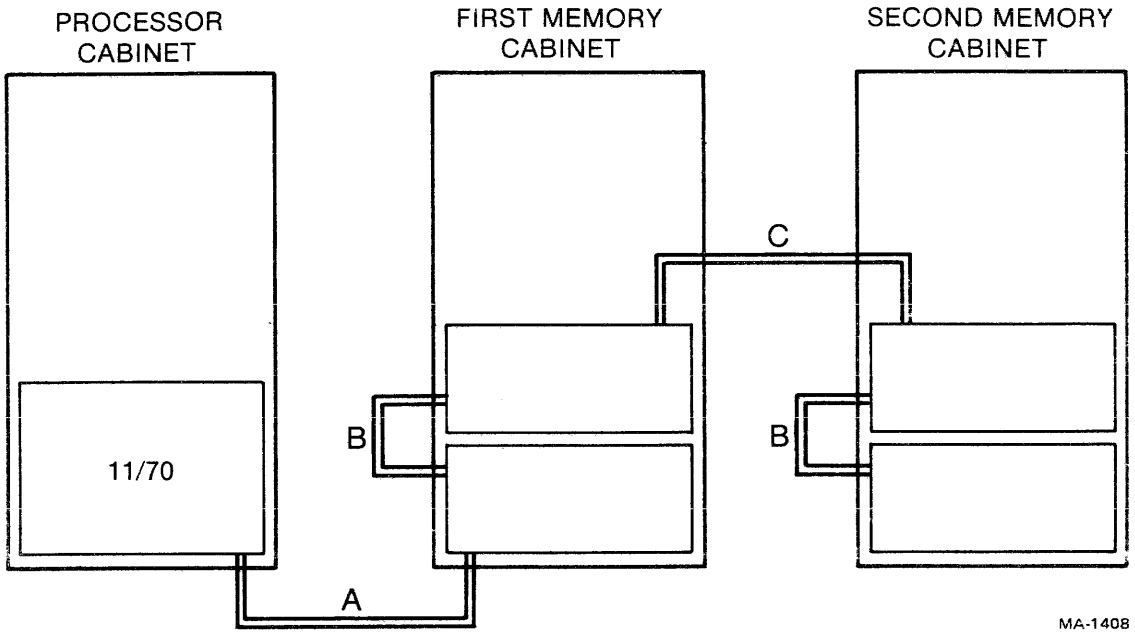


Figure 1-7 Memory Bus Designator

Numeral	Option Includes
MK11-BD (for 230 Vac)	Same as MK11-BC but for 230 Vac operation
MK11-BA (for 115 Vac)	Main memory bus cable B (Figure 1-7) BA11 memory box* with 64K words MOS memory Box controller and cables Three battery backup units and cables
MK11-BB (for 230 Vac)	Same as MK11-BA but for 230 Vac operation
MK11-BE	64K word expansion (2 MS11-KE)
MK11-BF	256K word expansion (8 MS11-KE)
MK11-BG	MK11-BA with 512K words MOS memory
MK11-BH	Same as MK11-BG but for 230 Vac operation
MK11-BY	MK11-BA without cables, box controller, or battery backup units
MK11-BZ	MK11-BB without cables, box controller, or battery backup units
MS11-KE	32K words MOS memory array module (4K MOS chips)
M8158	Address buffer module

Numeral	Option Includes
M8159	Data buffer module
M8160	Control A module
M8161	Control B module

*Includes one M8158, one M8159, two M8160, and two M8161 modules.

1.2 MEMORY SYSTEM ORGANIZATION (Figure 1-8)

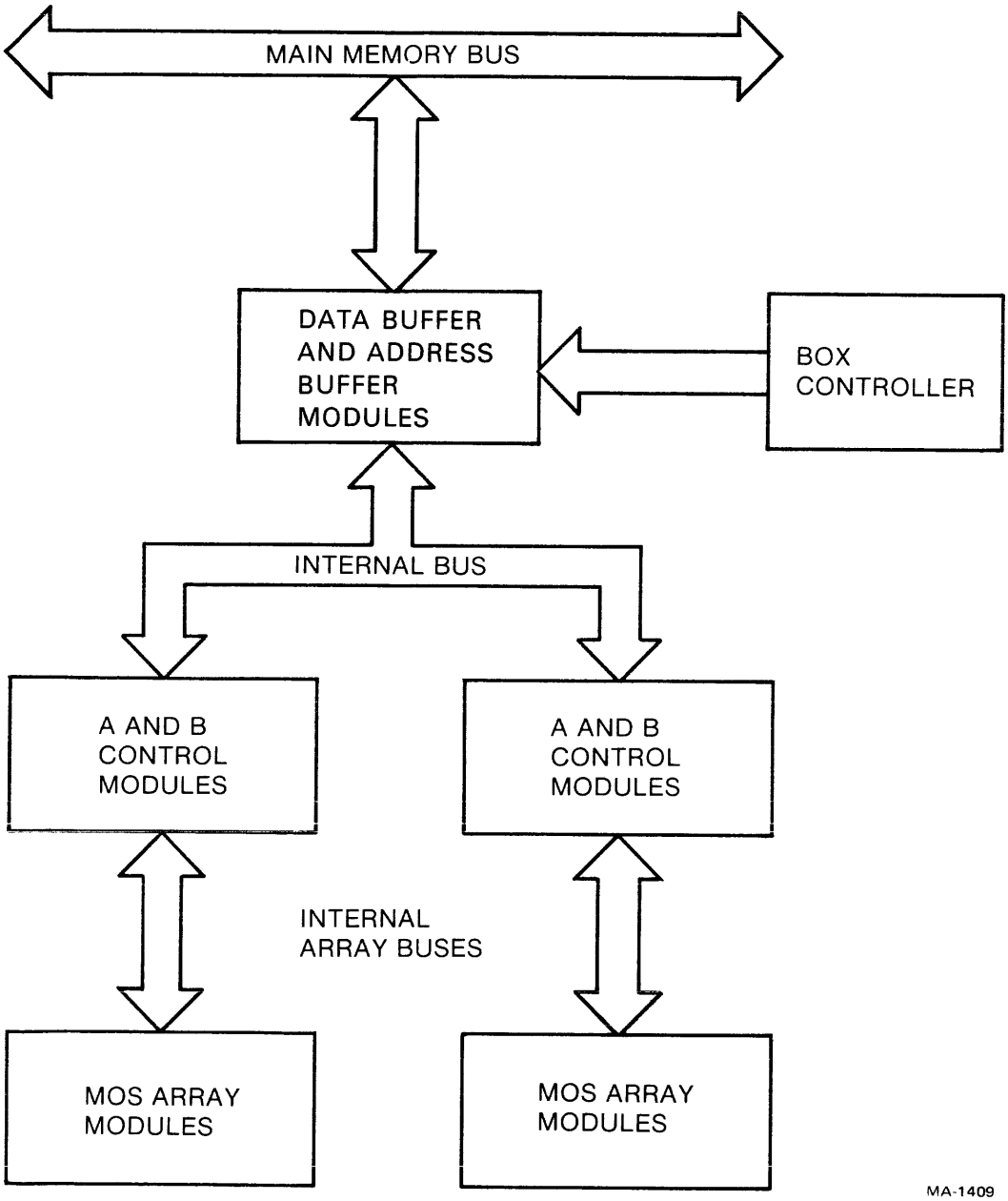


Figure 1-8 Internal Organization of Memory System

1.2.1 Main Memory Bus

The main memory bus interfaces the processor's cache with main memory. In PDP-11/70 systems, the cache is the sole master of the main memory bus. Data, address, and control signals transmit along the bus between cache and from one to four memories. In response to the control signals from cache, one of the memories receives data from or asserts data onto the bus.

1.2.2 Address Buffer Module

The address buffer module is a hex-multilayer printed circuit board. It receives address and control signals from the main memory bus and checks the address parity. It modifies the 22-bit address to select a control module, array module, and word, and interleaves the addresses of the arrays. A tri-state internal bus carries the modified address to the control modules.

The main memory bus plugs into four connectors on this module. Two connectors connect the module to the address and control bus cables. Two connectors connect the module to the next memory on the daisy chain or to terminators if it is in the last memory on the daisy chain. The module plugs into slot 13 of the backplane (Figure 1-9).

1.2.3 Data Buffer Module

The data buffer module is a hex multilayer printed circuit board. It transmits and receives data to and from the main memory bus and contains the control and status register (CSR). The data buffer places data from the main memory bus onto a tri-state internal bus which connects to the control modules. It also receives data from the internal bus to be transmitted to the main memory bus.

The main memory bus plugs into four connectors on this module. Two connectors connect the module to the data bus cables. Two connectors connect the module to the next memory on the daisy chain or to the terminators if it is in the last memory on the daisy chain. The module plugs into slot 15 of the backplane (Figure 1-9).

1.2.4 Control A and B Modules

The control A and B modules are hex multilayer printed circuit boards. The control A module generates the timing signals for the memory's cycles. It latches the modified address and selects the appropriate array module and word. It repeatedly refreshes the data in the MOS RAM chips and checks the configuration of the array modules.

The control B module transmits and receives data to and from the memory-array modules. It latches the data for modification, performs error detection and correction functions on the data, and checks the parity.

The control A modules plug into slots 11 and 16 of the backplane. The control B modules plug into slots 10 and 17 (Figure 1-9).

1.2.5 MOS Memory Array Modules

The MS11-K MOS memory array modules are hex-multilayer printed circuit boards. Each module stores 16,384 39-bit words in 4K MOS RAM chips. Each module transmits and receives these data words to and from the control modules. Each set of control A and B modules controls from one to eight array modules.

The array modules plug into slots 2–9 and slots 18–25 of the backplane.

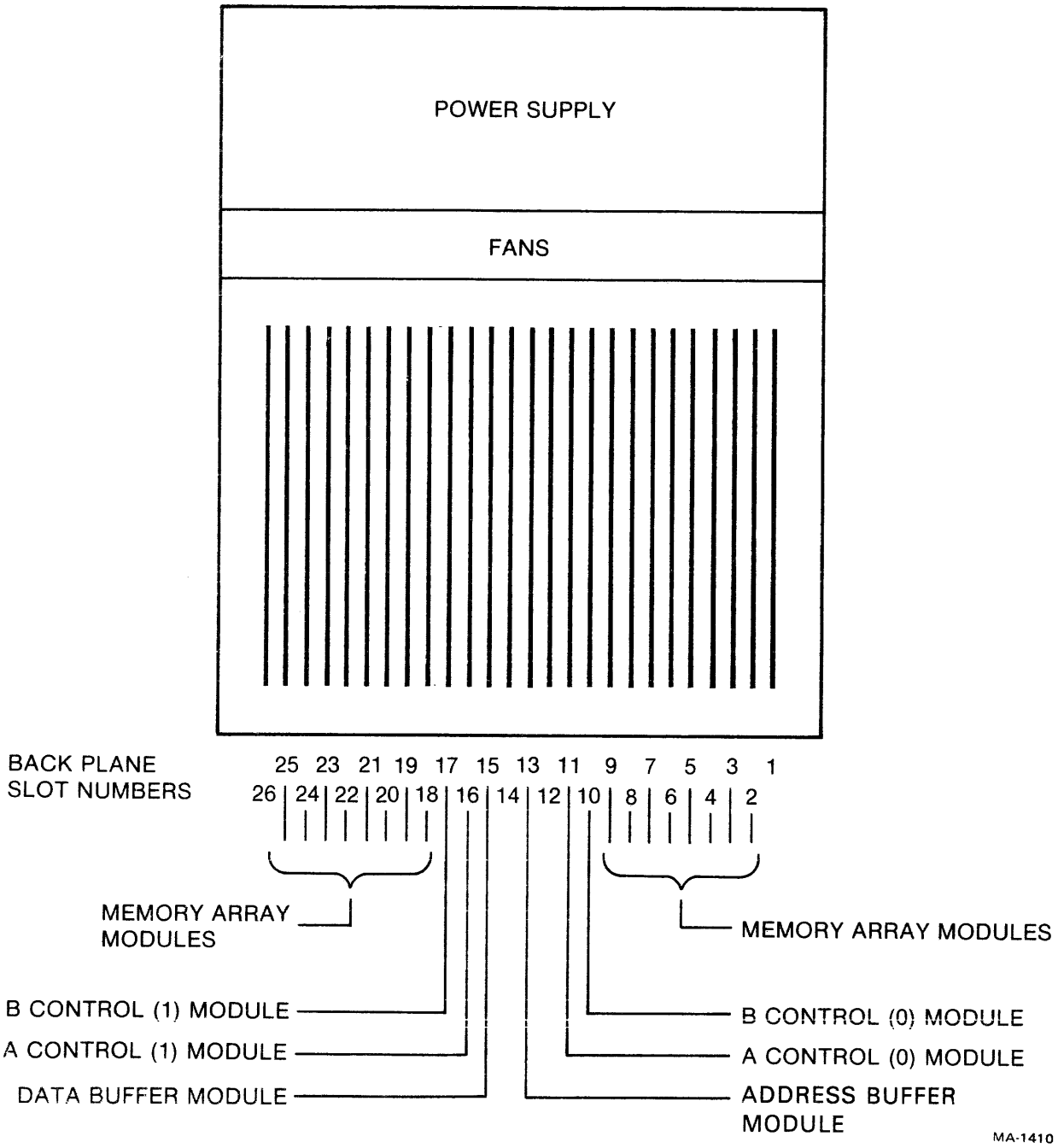


Figure 1-9 Module Locator

1.3 RELATED HARDWARE MANUALS

Title	Document No.
PDP-11/70 Maintenance and Installation Manual	EK-11070-MM-001
PDP-1134A Power System Description	EK-1134A-TM-002

These documents can be ordered from:

Digital Equipment Corporation
444 Whitney Street
Northboro, MA 01532
Attention: Communications Services (NRZ/M15)
Customer Services Section

CHAPTER 2
MAIN MEMORY BUS

2.1 GENERAL DESCRIPTION

The main memory bus (Figure 2-1) consists of four BC06R cables. These ribbon cables contain 40 conductors each. Two of the bus cables carry the main memory data between the processor and the memory and two of the bus cables carry the address and control signals between the processor and the memory.

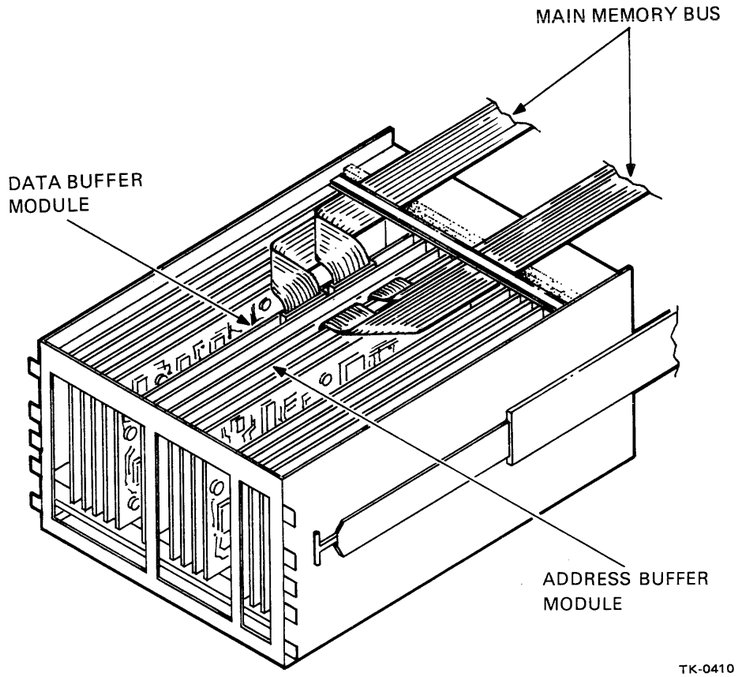


Figure 2-1 Main Memory Bus

The main memory bus between the processor and the memory closest to the processor extends from the back of the processor chassis and plugs into the top of the memory box on the data buffer and address buffer modules. Other memory boxes are daisy-chained together by bus cables connected to data buffer and address buffer modules of adjacent memory boxes. A maximum of four memory boxes can be daisy-chained together.

Since the main memory bus is characteristically a transmission line, it must be properly terminated at both ends. Four type H873 terminators are plugged into the bus cable connectors on the data buffer and address buffer modules of the last memory on the bus. The terminators are secured to the buffer modules with two small screws which also provide dc power to the terminators.

Tables 2-1 and 2-2 list the signal names and describe the types of signals on the main memory bus.

Table 2-1 Memory Bus Signal Pin Connections

Memory Bus Cable Conductor No.	Bus Master or Memory Controller "OUT" Connector Pin	Data Cable A (J1, J2)	Data Cable B (J3, J4)	Address Cable A (J1, J2)	Address Cable B J3, J4)
1	B	MAIN DATA BYTE 0–0 L	MAIN DATA BYTE 2–0	MAIN A02 L	MAIN A22 L
2	A	Ground	Ground	Ground	Ground
3	D	MAIN DATA BYTE 0–1 L	MAIN DATA BYTE 2–1 L	MAIN A03 L	MAIN A23 L
4	C	Ground	Ground	Ground	Ground
5	F	MAIN DATA BYTE 0–2 L	MAIN DATA BYTE 2–2 L	MAIN A04 L	MAIN A24 L
6	E	Ground	Ground	Ground	Ground
7	J	MAIN DATA BYTE 0–3 L	MAIN DATA BYTE 2–3 L	MAIN A05 L	MAIN A PAR L
8	H	Ground	Ground	Ground	Ground
9	L	MAIN DATA BYTE 0–4 L	MAIN DATA BYTE 2–4 L	MAIN A06 L	MAIN C0 L
10	K	Ground	Ground	Ground	Ground
11	N	MAIN DATA BYTE 0–5 L	MAIN DATA BYTE 2–5 L	MAIN A07 L	MAIN C1 L
12	M	Ground	Ground	Ground	Ground
13	R	MAIN DATA BYTE 0–6 L	MAIN DATA BYTE 2–6 L	MAIN A08 L	MAIN BYTE MASK 00 L
14	P	Ground	Ground	Ground	Ground
15	T	MAIN DATA BYTE 0–7 L	MAIN DATA BYTE 2–7 L	MAIN A09 L	MAIN BYTE MASK 01 L
16	S	Ground	Ground	Ground	Ground
17	V	MAIN DATA BYTE 0–8 L	MAIN DATA BYTE 2–8 L	MAIN A10 L	MAIN BYTE MASK 02 L
18	U	Ground	Ground	Ground	Ground
19	X	MAIN DATA BYTE 1–0 L	MAIN DATA BYTE 3–0 L	MAIN A11 L	MAIN BYTE MASK 03 L
20	W	Ground	Ground	Ground	Ground
21	Z	MAIN DATA BYTE 1–1 L	MAIN DATA BYTE 3–1 L	MAIN A12 L	MAIN ACK L
22	Y	Ground	Ground	Ground	Ground
23	BB	MAIN DATA BYTE 1–2 L	MAIN DATA BYTE 3–2 L	MAIN A13 L	MAIN PAR ERR L
24	AA	Ground	Ground	Ground	Ground
25	DD	MAIN DATA BYTE 1–3 L	MAIN DATA BYTE 3–3 L	MAIN A14 L	MAIN START L
26	CC	Ground	Ground	Ground	Ground
27	FF	MAIN DATA BYTE 1–4 L	MAIN DATA BYTE 3–4 L	MAIN A15 L	MAIN BOCC L
28	EE	Ground	Ground	Ground	Ground
29	JJ	MAIN DATA BYTE 1–5 L	MAIN DATA BYTE 3–5 L	MAIN A16 L	MAIN MARGIN 0 L

Table 2-1 Memory Bus Signal Pin Connections (Cont)

Memory Bus Cable Conductor No.	Bus Master or Memory Controller "OUT" Connector Pin	Data Cable A (J1, J2)	Data Cable B (J3, J4)	Address Cable A (J1, J2)	Address Cable B (J3, J4)
30	HH	Ground	Ground	Ground	Ground
31	LL	MAIN DATA BYTE 1-6 L	MAIN DATA BYTE 3-6 L	MAIN A17 L	MAIN MARGIN 1 L
32	KK	Ground	Ground	Ground	Ground
33	NN	MAIN DATA BYTE 1-7 L	MAIN DATA BYTE 3-7 L	MAIN A18 L	MAIN MARGIN 2 L
34	MM	Ground	Ground	Ground	Ground
35	RR	MAIN DATA BYTE 1-8 L	MAIN DATA BYTE 3-8 L	MAIN A19 L	MAIN AC LOW L
36	PP	Ground	Ground	Ground	Ground
37	TT	MAIN BOOT EN L	MAIN DATA BYTE 3-9 L	MAIN A20 L	MAIN DC LOW L
38	SS	Ground	Ground	Ground	Ground
39	VV	MAIN DATA READY L	SPARE	MAIN A21 L	MAIN 4.3 V
40*	UU	Ground	Ground	Ground	Ground

*Cable Shield

Table 2-2 Main Memory Bus Signals

Signal	Function
MAIN A (24:02) L	This is the address of the 32-bit double word located in main memory. The address is gated onto the main memory bus by the cache. (Main memory bus address lines MAIN A (24:22) are not used in the PDP-11/70, and are always maintained in the negated state.)
MAIN BYTE MASK 3 L MAIN BYTE MASK 2 L MAIN BYTE MASK 1 L MAIN BYTE MASK 0 L	These bits define which of the 4 bytes within the double word addressed by MAIN A (24:02) will be operated on during a write cycle to one correspondence between bytes 0 to 3 and byte mask 0 to 3. If MAIN BYTE MASK "X" is asserted, byte "X" will be operated on. The main memory ignores the mask bits on all read operations.
MAIN C (1:0) L	These bits, gated from cache, determine which operation is to be performed by main memory. They are decoded as follows: **C1 C0 Operation** 0 0 Read 0 1 Read pause write (defaults to read in single processor systems) 1 0 Write 1 1 Exchange (not used in PDP-11/70)
MAIN A PAR L	This is an odd parity bit generated by the cache for the control word consisting of MAIN A (24:02), MAIN C (1:0), and MAIN BYTE MASK (3:0). This bit is received and checked by each address buffer module.
MAIN START L	This signal is asserted by cache to initiate the main memory cycle designated by the MAIN C (1:0) bits on the main memory address locations designated by the address and byte mask bits.
MAIN PAR ERR L	This signal is asserted by the address buffer module if it detects a parity error in the control word described above, when START is asserted.
MAIN ACK L	This signal is asserted by the addressed memory controller within main memory when it has actually started execution of the commanded memory cycle. Receipt of MAIN ACK by the cache, allows it to alter MAIN A (24:02), MAIN C (1:0), MAIN BYTE MASK (3:0), and MAIN A PAR lines on the main memory bus, and to negate MAIN START. If a write operation was just initiated, MAIN ACK indicates that the main memory bus transaction is terminated.

Table 2-2 Main Memory Bus Signals (Cont)

Signal	Function
MAIN BOCC L	During a read operation, this signal is asserted coincidentally with MAIN ACK by the active memory controller within main memory, and is kept asserted until read data is removed from the main memory bus data lines (MAIN DATA BYTE (0–0:0–8, 1–0:1–8, 2–0:2–8, 3–0:3–8). The cache may gate data onto the main memory bus data lines only when MAIN BOCC is not asserted.
MAIN DATA BYTE (0–0:0–8) L MAIN DATA BYTE (1–0:1–8) L MAIN DATA BYTE (2–0:2–8) L MAIN DATA BYTE (3–0:3–8) L	These are the data and data parity lines of the main memory bus. Odd parity is utilized. In the PDP-11/70 implementation, MAIN DATA 1–9 and 3–9 L are not used as data bits. The MAIN DATA BYTE lines are organized as follows: MAIN DATA BYTE (0–0:0–7) – Byte 0 data MAIN DATA BYTE 0–8 – Byte 0 parity MAIN DATA BYTE (1–0:1–7) – Byte 1 data MAIN DATA BYTE 1–8 – Byte 1 parity MAIN DATA BYTE (2–0:2–7) – Byte 2 data MAIN DATA BYTE 2–8 – Byte 2 parity MAIN DATA BYTE (3–0:3–7) – Byte 3 data MAIN DATA BYTE 3–8 – Byte 3 parity During a write operation, the cache gates out data and data parity bits onto these lines while MAIN BOCC is negated and then asserts MAIN START. Which bytes are written is determined by the main byte mask bits. During a read or exchange operation, main memory brings up all four bytes, generates the parity bits, and places the information on the MAIN DATA BYTE lines.
MAIN DATA READY L	This signal is asserted by the active memory controller during a read operation, after it has placed data on the MAIN DATA BYTE lines, to indicate to cache that the requested data is available.
MAIN AC LOW L	This signal asserted by main memory to inform the bus master that the ac power input to a main memory power supply is below operating limits, or that the memory is performing an ECC initialization.
MAIN DC LOW L	This signal is asserted by the cache or main memory to inform the rest of the system that input power to a power supply somewhere in the system is below the point that guarantees dc outputs to be in regulation.
MAIN MARGIN (0–2) L	These signals alter the internal timing for maintenance purposes.
MAIN BOOT ENABLE L	This signal is asserted by the memory to reboot the processor after the memory is initialized.
MAIN 4.3 V	This signal provides power for bus disable circuits.

2.2 PROTOCOL AND TIMING

Three types of operations occur on the main memory bus: read, write, and exchange. Read and write operations may be performed on data in the memory or in the control and status register (CSR). Figures 2-2 through 2-7 illustrate the various main memory bus cycles. Table 2-3 lists the typical and maximum access and the cycle times, with no refresh conflicts.

Table 2-3 Access and Cycle Times

Memory	Typical	Maximum
Read Access Time (no errors)	590 ns	650 ns
Read Access Time (single error)	690 ns	750 ns
Read Cycle Time (no errors)	750 ns	800 ns
Read Cycle Time (single error)	850 ns	900 ns
Write Cycle Time (1 to 3 bytes)	1100 ns	1200 ns
Write Cycle Time (4 bytes)	740 ns	800 ns
Exchange Cycle Time	1360 ns	1500 ns
Control and Status Register		
CSR Read Cycle Time	800 ns	800 ns
CSR Write Cycle Time	800 ns	800 ns

2.2.1 Initiation of a Memory Cycle

To initiate a memory cycle, the bus master places the address of the desired memory location, 6 control bits defining the type of memory cycle to be executed (MAIN C1:C0 and MAIN BYTE MASK 3:0), the address and control word parity bit (odd parity) on the main memory bus. After a deskew and access delay for the above signals, START is issued by the cache. If the memory cycle being initiated is an exchange or write operation, the data to be written into the addressed memory location must be placed on the main memory bus prior to the issuance of START, to allow sufficient data deskew.

2.2.2 Response of the Memory System

Each memory examines the address and control lines for correct address parity. If wrong address parity is detected for the address and control word received by the address buffer, a latch is set by the leading edge of START, which, in turn, asserts MAIN PAR ERR on the main memory bus. Any memory address buffer is capable of generating MAIN PAR ERR, whether it is being addressed or not. If the memory being addressed detects wrong parity, further memory activity by the controller is inhibited during this memory cycle; the controller will not respond with MAIN ACK and the address buffer will assert MAIN PAR ERR.

If correct parity is determined, the address received is found by a memory to be within its address range, and the memory controller is not currently active, a memory cycle is initiated and MAIN ACK is returned to the bus master. If the controller is currently active, the requested memory cycle is deferred until the current memory cycle is completed, at which time the requested memory cycle is initiated and MAIN ACK is asserted.

When MAIN ACK is received by cache, it unasserts START and signals on the address, control, and data (if applicable) lines of the bus. The bus master is then free to assert address and control signals for the next memory cycle. START, however, must not be issued until MAIN ACK is unasserted by the memory controller.

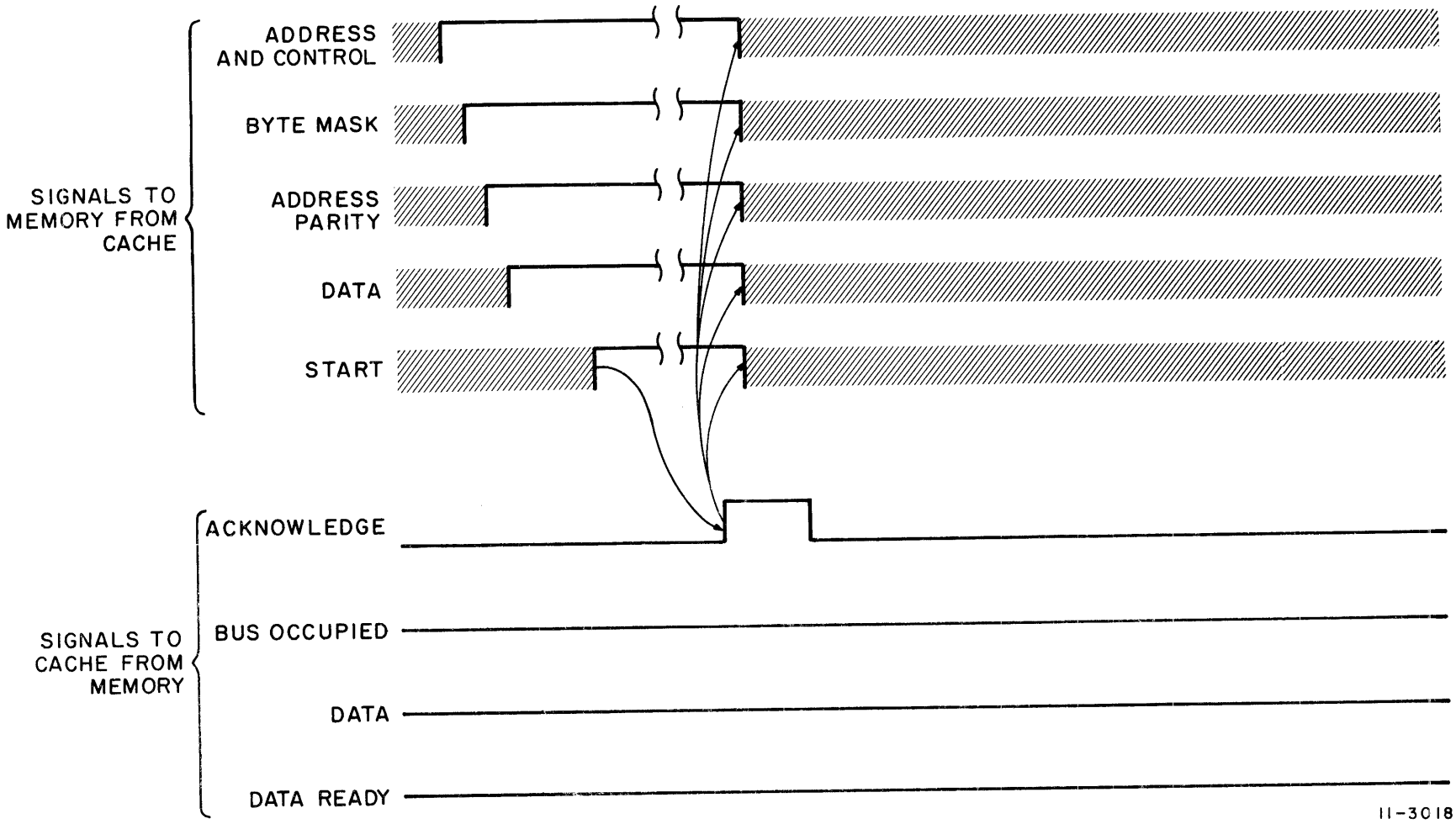


Figure 2-2 Write Operation Main Memory Bus Protocol

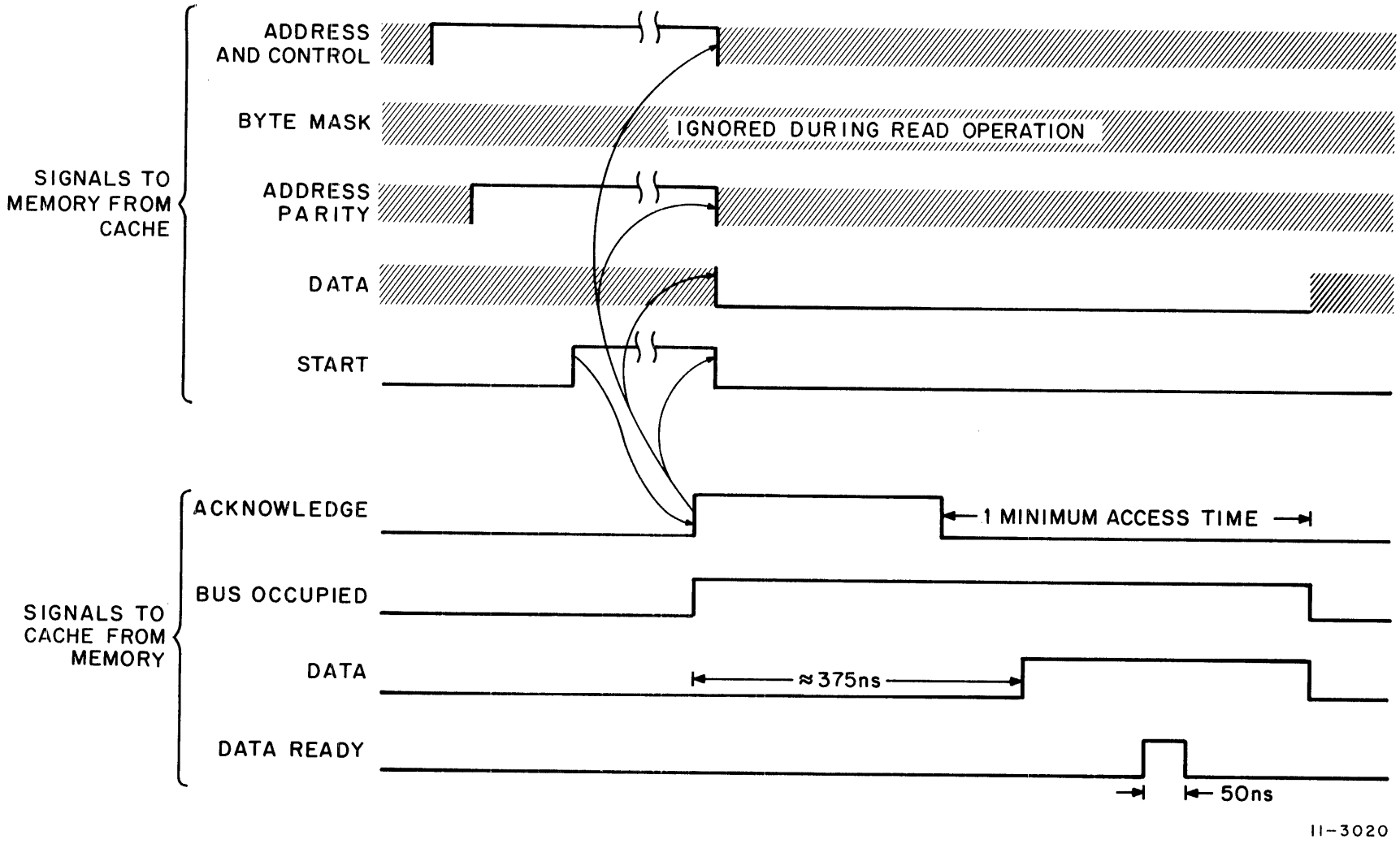


Figure 2-3 Read Operation – Main Memory Bus Protocol

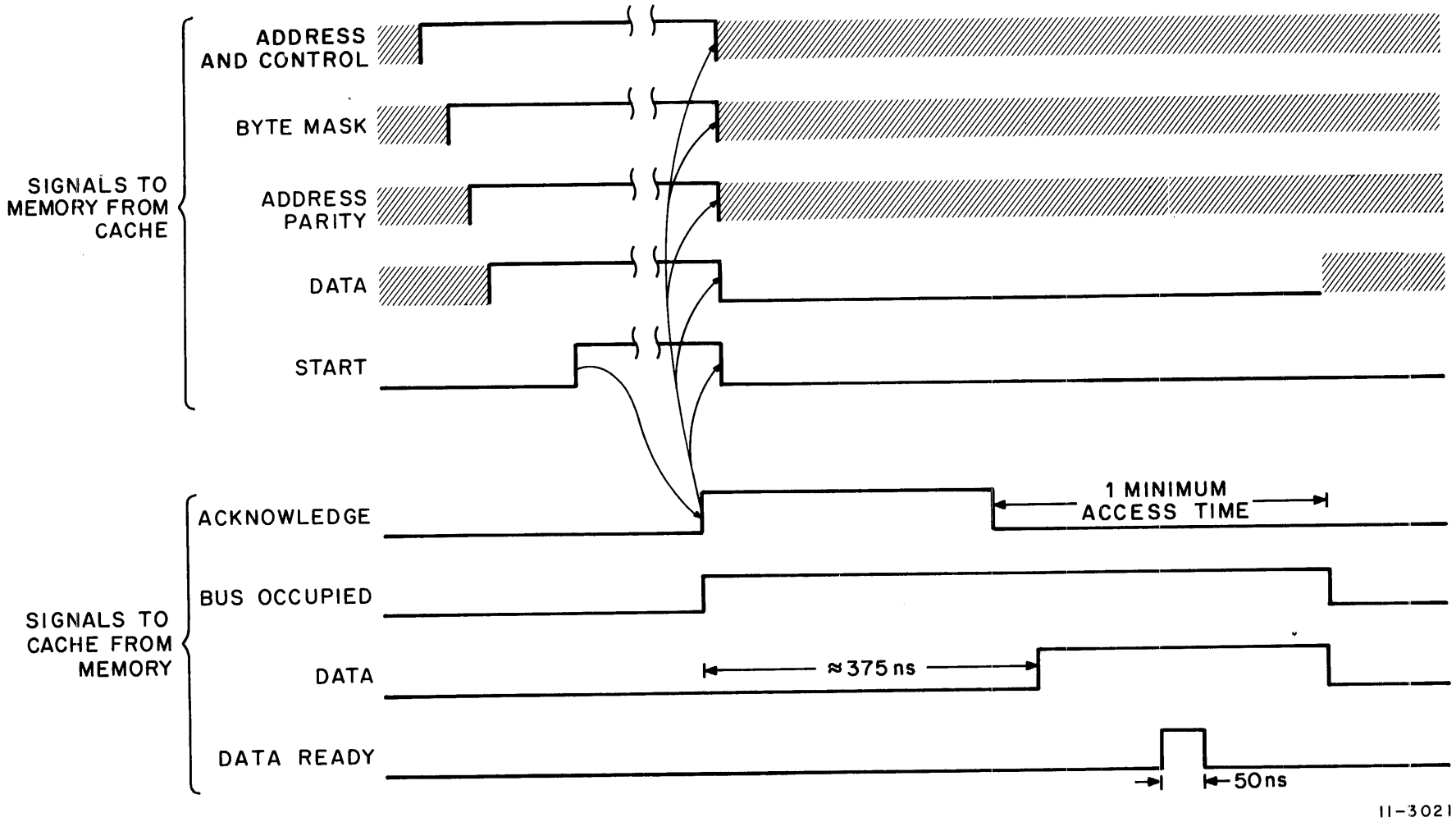


Figure 2-4 Exchange Operation Main Memory Bus Protocol

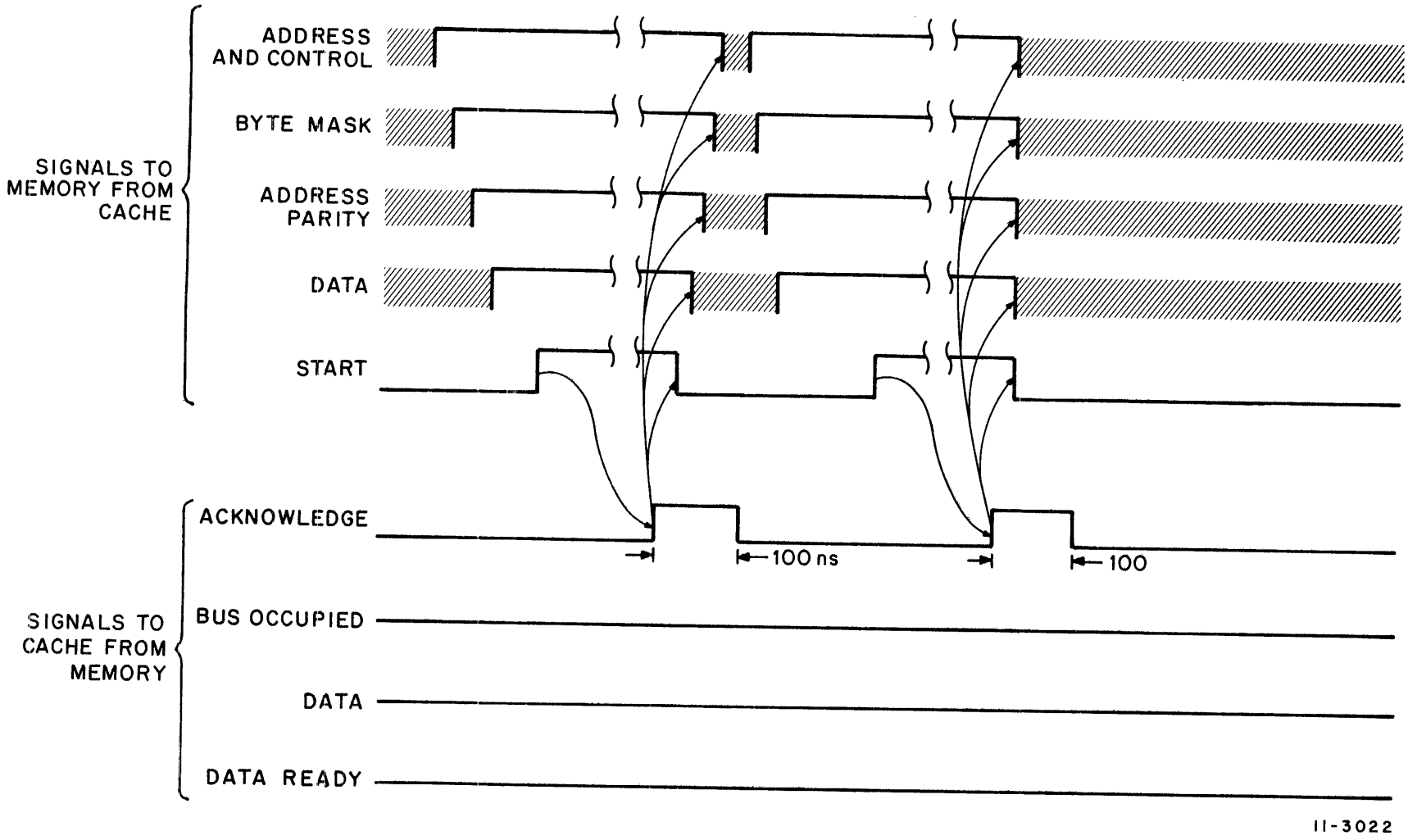


Figure 2-5 Write Overlapped by Write – Main Memory Bus Protocol

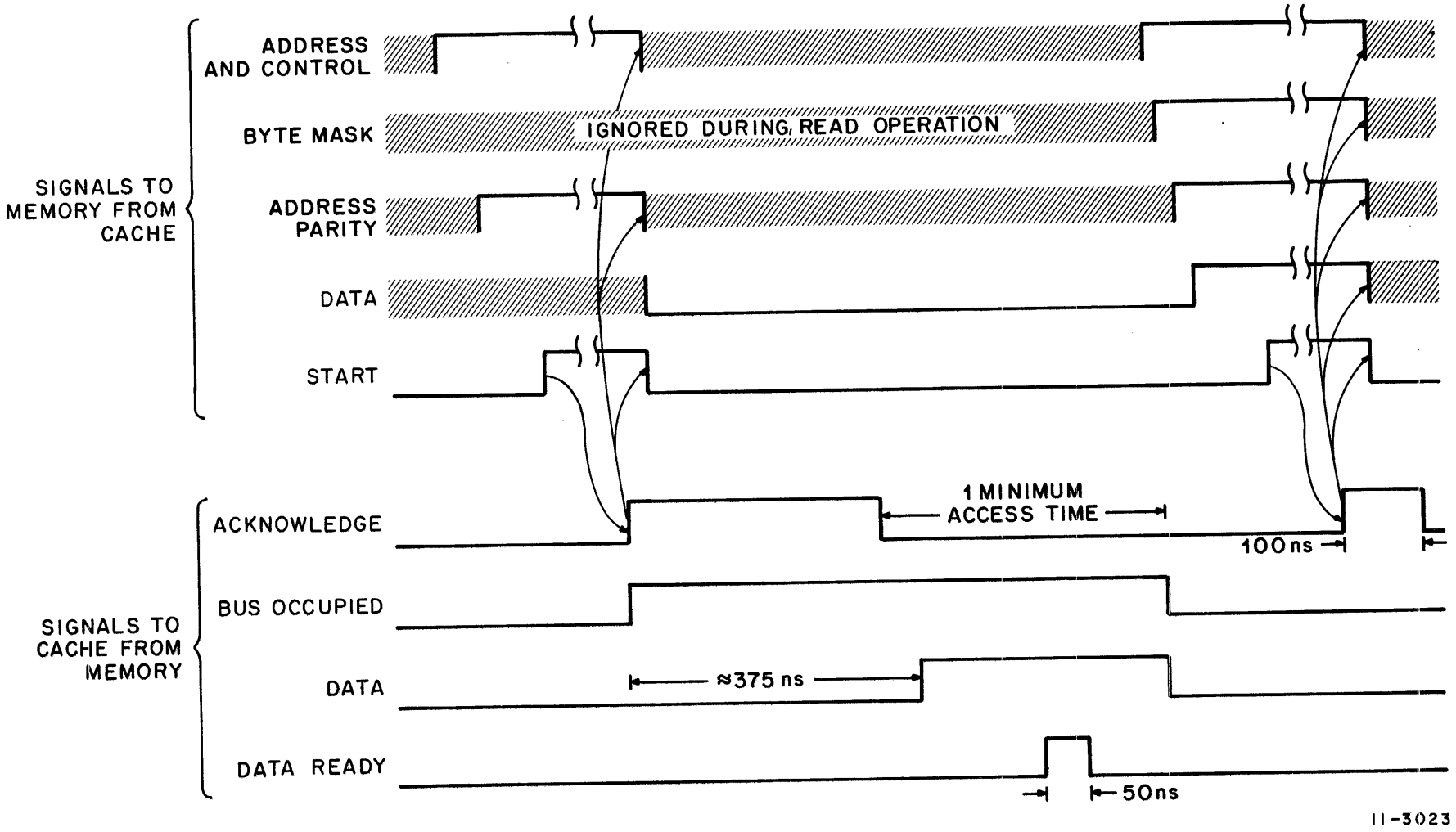


Figure 2-6 Read Overlapped by Write Main Memory Bus Protocol

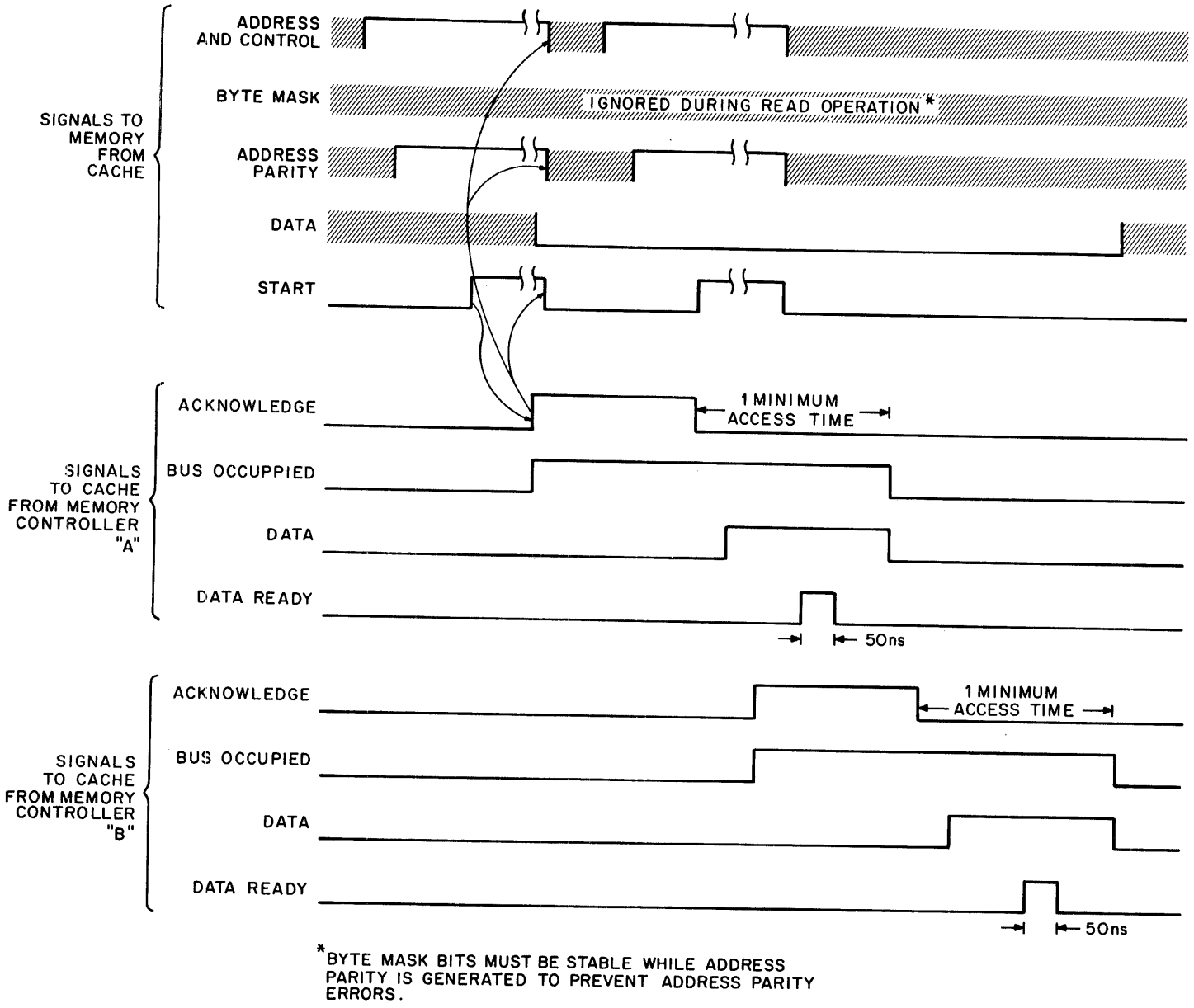


Figure 2-7 Read Overlapped by Read – Main Memory Bus Protocol

Data returned from an active memory controller is asserted at the memory data buffer's bus drivers after the memory controller starts executing the requested memory cycle and remains asserted for approximately 225 ns. After the assertion of data, DATA READYD is pulsed. Data from the main memory bus is clocked into the bus master by the leading edge of DATA READY.

Whenever a memory controller is executing a memory cycle during which read data will be asserted on the main memory bus (exchange or read), the controller also asserts MAIN BOCC. This indicates that the data lines of the main memory bus are "occupied," and that the bus data lines must not be driven by the bus master.

2.2.3 CSR Cycles

Read and write operations directed to the control and status register occur on the bus in the same sequence as read and write operations directed to address locations in the memory.

2.2.4 Initiation of "Overlapped" Memory Cycles

The bus master need not wait for the assertion of DATA READY during a read or exchange operation before it can initiate the next memory cycle. If the next cycle is a read operation, the cache may assert START as soon as MAIN ACK becomes unasserted (providing, of course, that the address and control lines have been stable for the required time period). If the next cycle is an exchange or write operation, the cache must also wait for MAIN BOCC to become unasserted, indicating that the memory is no longer driving the bidirectional data lines of the main memory bus. At this time, the cache may assert the write data on the bus, wait the required data deskew delay, and then issue START for the next memory cycle.

As noted above, the duration of MAIN ACK and MAIN BOCC limit the extent of cycle overlap. The duration of MAIN ACK is a function of the memory access time and the type of cycle being executed. If the operation is a read or exchange (or, in general, whenever data is to be returned on the main memory bus from the memory during the read portion of the cycle), MAIN ACK is asserted until one minimum access time before the latest time that data is removed from the bus by the addressed memory. This ensures that the data transferred to the bus master during the read or exchange operation will not interfere with data transferred during the next memory operation. During a write operation, however, where no data is returned from the active memory, MAIN ACK is asserted for approximately 100 ns following the start of the memory cycle.

CHAPTER 3
BOX CONTROLLER

3.1 GENERAL DESCRIPTION

The MK11 box controller (Figure 3-1) selects the starting addresses and operating modes for the memory system and indicates certain status conditions. Each box controller controls one memory box. A switch on the controller switches primary power and battery power to the memory.

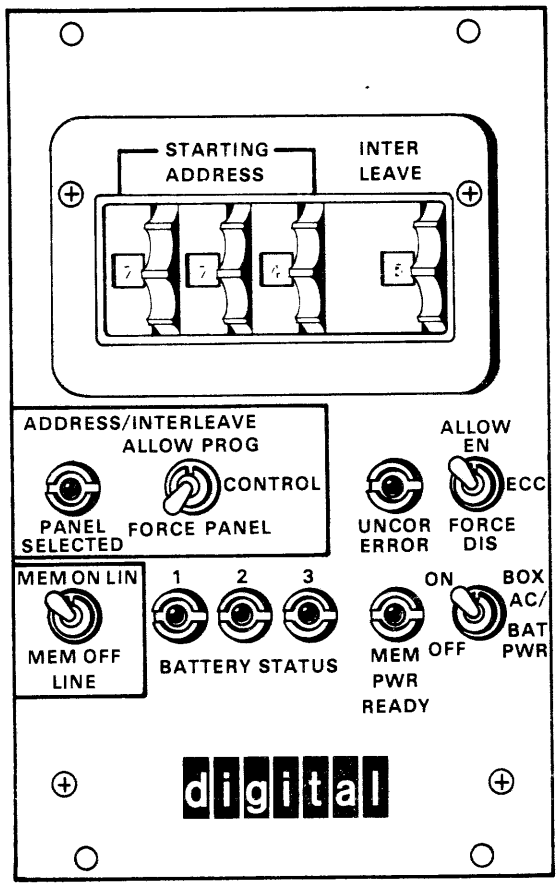


Figure 3-1 Box Controller

3.2 CONTROL SWITCHES AND INDICATORS

Switch/Indicators	Function/Indication
STARTING ADDRESS Select Switches	Select octal address (in 32K × 16-bit blocks) of first memory location of box.
INTERLEAVE Select Switch	Selects type of external interleaving. 0 No external interleaving 1 Not used 2 First box of 2-way interleaved system 3 Second box of 2-way interleaved system 4 First box of 4-way interleaved system 5 Second box of 4-way interleaved system 6 Third box of 4-way interleaved system 7 Fourth Box of 4-way interleaved system
ADDRESS/INTERLEAVE Switch	ALLOW PROG Control – Operating system selects starting address and type of interleaving through the CSR. FORCE PANEL Control – Forces the memory's starting address and external interleaving to be those selected by the controller's starting address and interleave select switches.
PANEL SELECTED Indicator	When on, starting address and external interleaving are selected by the box controller.
ECC Enable/Disable Switch	ALLOW EN – Allows correction of all single-bit data errors. FORCE DIS – Disables all error correction (except in protected memory blocks).
UNCOR ERROR Indicator	Indicates uncorrectable multiple-bit error detected.
MEM ON LINE/OFF LINE Switch	When ON LINE, memory is on-line with the main memory bus and will respond to commands from cache. When OFF LINE, memory is off-line with the main memory bus and will not respond to commands from cache.
BATTERY STATUS Indicators 1, 2, and 3	When off, battery is discharged or disconnected from memory. Slow blink indicates battery is charging. Fast blink indicates battery is supplying power to memory. When on, battery is fully charged and receiving trickle charge.
MEM PWR READY Indicator	When on, indicates memory is on and dc voltages are within operating limits (BOX DC LOW and MAIN DC LOW not asserted).
BOX AC/BAT PWR Switch	Enables primary ac and battery backup power to power supply and regulators.

3.3 STARTING ADDRESS AND EXTERNAL INTERLEAVING

When the ADDRESS/INTERLEAVE switch is in the FORCE PANEL control position, the box controller sets the starting address and the type of interleaving desired for the memory.

The STARTING ADDRESS select switches set the starting address, the first address to which the memory will respond. The address displayed by the three switches represents an octal address in units of 32K × 16-bit blocks of memory. A 32K × 16-bit block of memory (32K words) corresponds to one MS11-K array module, the smallest increment of memory expansion.

For an example, consider a memory system with two MK11 memory boxes (and two box controllers), with both boxes fully populated with 16 MS11-KE array modules (512K words) and with no external interleaving. For no external interleaving, the INTERLEAVE switch is turned to 0. Setting the starting address to 0 on one of the box controllers causes that memory to respond to the first 512K words (byte addresses 0 to 3777777_8). Then determine the capacity of the first box in units of 32K × 16-bit blocks. Either divide the box capacity in 32-bit words by 16K or count the number of array cards if they are all MS11-K modules. In this case, the box capacity is 16, which is 20_8. Therefore, set the starting address to 020. The second memory will respond to the second 512K words (byte addresses 40000000_8 to 7777777_8).

The INTERLEAVE switch selects the number of memory boxes externally interleaved and the order in which the interleaving is performed. The following rules must be followed for external interleaving.

- Only an even number of boxes may be externally interleaved.
- Only boxes with the same capacity may be externally interleaved.
- Externally interleaved boxes must have the same starting address.

Refer to Figure 3-2 for examples of externally interleaved memory systems. The 2-way externally interleaved memory depicted consists of two memory boxes, each with the same memory capacity. Note that both starting addresses have been set to the same value (000). In order to 2-way interleave the two boxes, set the INTERLEAVE switch to 2 on one of the box controllers and to 3 on the other box controller.

The 4-way interleaved system consists of four memory boxes with four box controllers. The starting addresses and the storage capacities of all four boxes are the same. Four-way externally interleaved systems are configured using INTERLEAVE switch settings 4, 5, 6, and 7 as shown in Figure 3-2. The addresses on the main memory bus to which each memory responds is shown beneath the memory boxes.

When the ADDRESS/INTERLEAVE switch is in the ALLOW PROG control position, the starting address and the type of interleaving can be program selected by setting or clearing bits in the CSR. Table 3-1 lists the CSR bits, switch settings, and the type of interleaving that they select. For a description of addressing the CSR to alter the type of interleaving and starting address, see Chapter 6.

3.4 DISABLING ERROR CORRECTION

In this memory, single-bit errors in the stored data are allowed to accumulate. That is, any data word with 1 bit in error is corrected by the memory. The memory appears to be functioning without errors even though one or several memory locations have 1 faulty bit. Setting the ECC enable/disable switch to FORCE DIS uncovers these accumulated single-bit errors. When a memory location with a faulty bit is accessed, bad parity will be generated for the data byte containing the single-bit error.

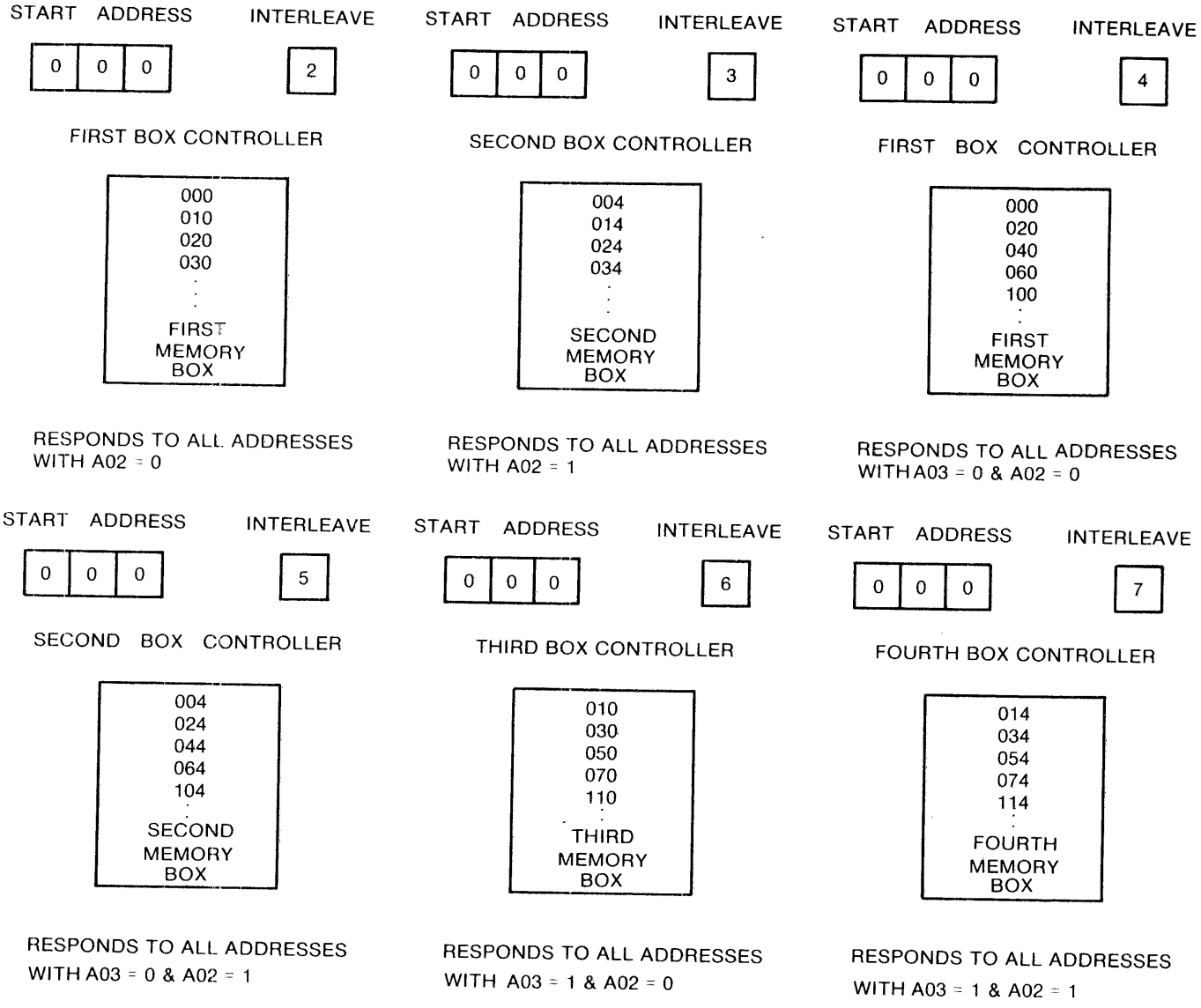


Figure 3-2 Interleave Switch Settings

Table 3-1 External Interleaving

INTERLEAVE Switch	CSR Bits			External Interleaving
	3-5 (4-way)	3-4 (2-way)	3-6 (Ext 02)	
0	0	0	0	No external interleaving
1	0	0	1	Not used
2	0	1	0	First of 2-way, memory selected if A02 = 0
3	0	1	1	Second of 2-way, memory selected if A02 = 1
4	1	0	0	First of 4-way, memory selected if A03 = 0 and A02 = 0
5	1	0	1	Second of 4-way, memory selected if A03 = 0 and A02 = 1
6	1	1	0	Third of 4-way, memory selected if A03 = 1 and A02 = 0
7	1	1	1	Fourth of 4-way, memory selected if A03 = 1 and A02 = 1

CHAPTER 4
MS11-KE MOS ARRAY MODULES

4.1 GENERAL DESCRIPTION

The MS11-KE storage array module is a hex-multilayer printed circuit board containing 156 16-pin 4K MOS RAM chips and their associated drive circuitry. It communicates with the A and B control modules via internal array buses on connectors A and B. One internal array bus carries data, address, and control signals between control 0 pair and backplane slots 2 through 9; the other carries signals between controller 1 and backplane slots 18 through 25. Figure 4-1 shows the physical layout of the printed circuit board.

The MOS chips are arranged in four rows of 39 chips. Each column of four chips stores data associated with one bit position of the 39-bit data word. The 39-bit double words contain 4 8-bit bytes and 7 check bits used for error detection and correction. The module transfers 39 bits in parallel to the Control B module during read and internal read-modify-write operations. During write operations, the 7 check bits and from 1 to 4 bytes are transferred in parallel to the array.

Address signals on the internal array bus select one of the array modules, one of the four rows of MOS chips on the array, and one cell of the 64 by 64 cell matrix within the chips. Timing signals demultiplex the chip column and row addresses which share the same six address lines. Other control signals enable the chip's output and strobe data into selected chips. All timing for the arrays is provided by the controllers. Figure 4-2 lists the signals of the internal array bus, which carries these address and data signals between the array and the controllers.

4.2 FUNCTIONAL DESCRIPTION

4.2.1 Data Receivers and Drivers

The data input pins of the MOS memory chips are always connected to the internal array bus data lines through buffer inverters. Refer to the block diagram of the array module, Figure 4-3. During a write operation and the write portion of an internal read-modify-write operation, 39 bits of data appear at the input pins of all four rows of chips. The controller strobes data only into the chips corresponding to the selected row and bytes. The data output lines of the MOS chips are gated to the internal array bus through line drivers. During a read operation and during the read portion of an internal read-modify-write, 39 bits of data from the selected row of chips are placed on the internal array bus. The Driver Enable Low signal, from the controller enables the line drivers of the selected row of chips to assert data onto the bus.

4.2.2 Addressing and Control

Address and timing control signals enable the addressed MOS chips during read, write, and refresh operations. The interface and control modules modify the main memory bus addresses and generate signals that access the selected memory location.

BYTE 2

DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	
E184	E172	E160	E148	E135	E122	E110	E97	ROW 11
E183	E171	E159	E147	E134	E121	E109	E96	ROW 10
E182	E170	E158	E146	E133	E120	E100	E95	ROW 01
E181	E169	E157	E145	E132	E119	E107	E94	ROW 00

BYTE 3

DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24
E88	E77	E67	E56	E46	E35	E24	E12
E87	E76	E66	E55	E45	E34	E23	E11
E86	E75	E65	E54	E44	E33	E22	E10
E85	E74	E64	E53	E43	E32	E21	E9

BYTE 0

DB07	DB06	DB05	DB04	DB03	DB02	DB01	DB00	
E180	E168	E156	E144	E131	E118	E100	E93	ROW 11
E179	E167	E155	E143	E130	E117	E105	E92	ROW 10
E178	E166	E154	E142	E129	E116	E104	E91	ROW 01
E177	E165	E153	E141	E128	E115	E103	E90	ROW 00

BYTE 1

DB15	DB14	DB13	DB12	DB11	DB10	DB09	DB08
E84	E73	E63	E52	E42	E31	E20	E8
E83	E72	E62	E51	E41	E30	E19	E7
E82	E71	E61	E50	E40	E29	E18	E6
E81	E70	E60	E49	E39	E28	E17	E5

CHECK BITS

CBT	CB32	CB16	CB8	CB4	CB2	CB1	
E176	E164	E152	E140	E127	E114	E102	ROW 11
E175	E163	E151	E139	E126	E113	E101	ROW 10
E174	E162	E150	E138	E125	E112	E100	ROW 01
E173	E161	E149	E137	E124	E111	E99	ROW 00

DB16-19	DB28-31	DB12-15	DB24-27	DB8-11
E80 DAT DR. REC	E69 ADD DR	E59 DAT DR. REC	E38 DAT DR. REC	E27 CS DR CAS DR	E16 DAT DR. REC	E4 DAT DR. REC

DB0-3

E79 DAT DR. REC	E68 ADD DR	E58 RAS DR	E48 WR DR	E37 ADD DR	E26 ADD DR	E15 ADD BUFF	E3 MEM SEL

E57 CS DR CAS DR	E47 WR DR	E36 ADD.BUF. RAS TIM BUF.	E25 INV.	E14 ADD DR	E2 RAS DEC.

E13 RAS DR	E1 RAS SEL

CB1,2,4,8

E89 ADD DR	E78 DAT DR. REC

CB16,32,T	DB20-23	DB4-7
E136 DAT DR. REC	E123 DAT DR. REC	E98 DAT DR. REC

F E D C B A

TK-0415

Figure 4-1 Layout Array Card

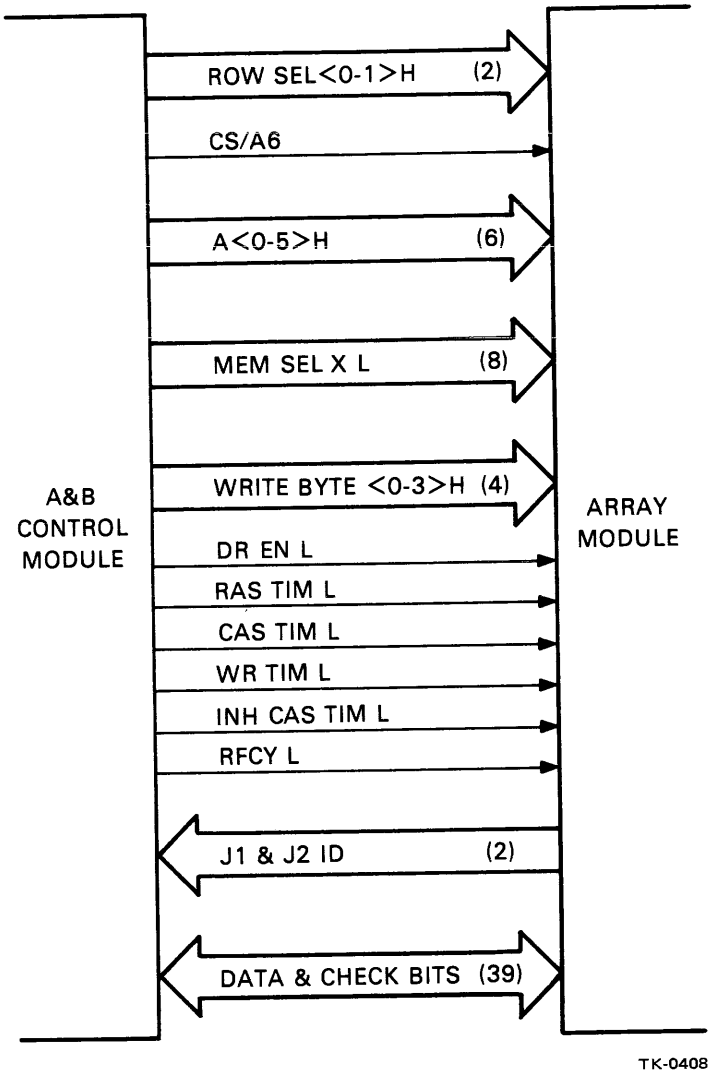


Figure 4-2 Internal Array Tri-State Bus

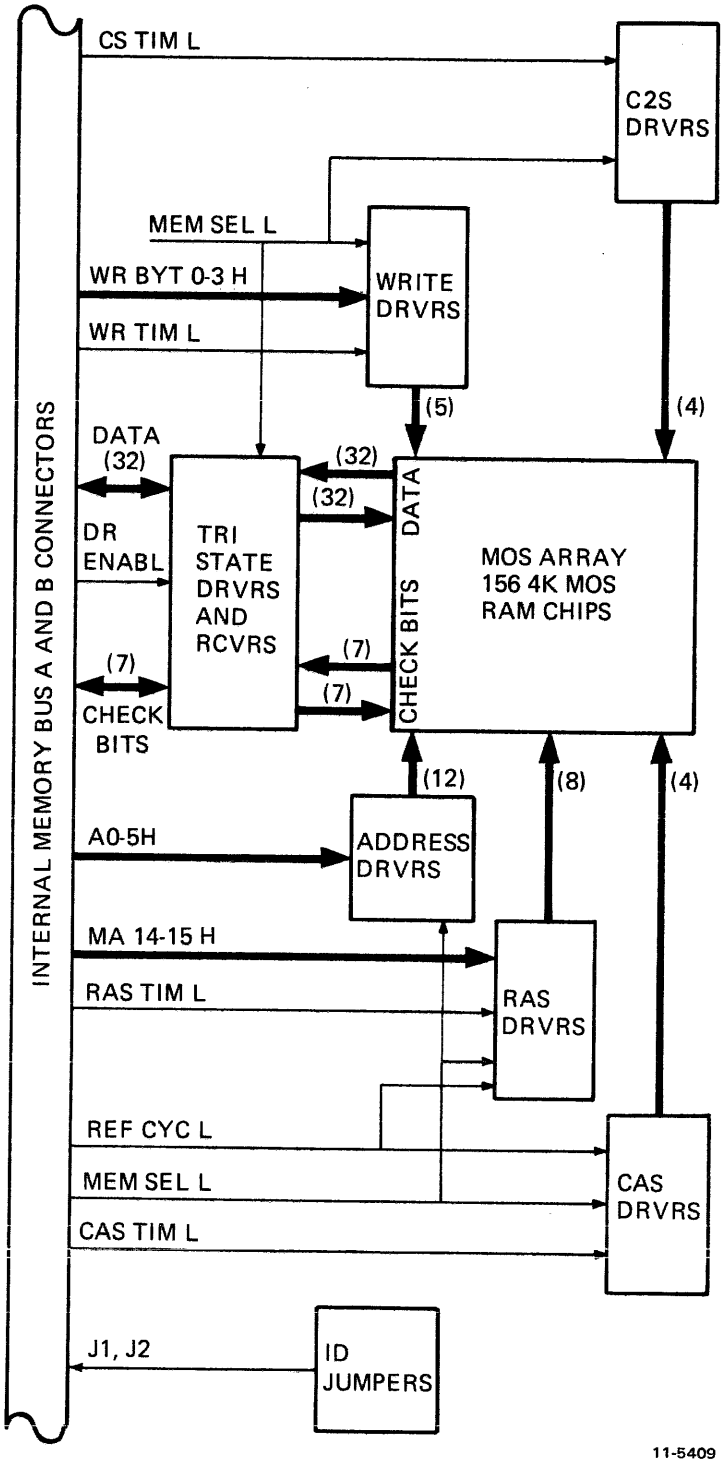


Figure 4-3 MS11-K M7984 32K × 16-Bit MOS Memory Array Card

Memory Select – There are eight Memory Select lines (MEM SEL <0–7>L) on each internal array bus. One line connects to pin AE2 on each of the array module slots of the backplane. The controller selects one array module by sending the Memory Select signal to one of the array slots. The absence of Memory Select Low disables all the functions of the array, except for refreshing the chips.

Chip Select – A Chip Select signal (CS) is strobed to all the array slots. On the selected array, this signal is fed to the CSL pin of all the MOS chips. The CSL input is one of the enable signals which allows transferring data to and from the chip.

Row Select – The Row Select signals (ROW SEL <0,1>H) select one of the four rows of 39 MOS memory chips. The two signals are decoded to enable one of the rows at Row Address Select Time. If the array is selected (MEM SEL LO), the enable signal, RASL <A,B,C,D>, selects one row while RAS TIM L is asserted on the internal array bus.

Multiplexed Row and Column Address – The controller multiplexes the row and column onto six address lines (A<0–5>H). The 4K storage cells of the MOS chips are organized as a 64 by 64 cell matrix. The address lines select a row and then a column within the MOS chips of the selected row. At Row Select Time (RAS TIM L), the 6-bit address is strobed into the MOS chip's row address register. Later, at Column Select Time (CAS TIM L), the address is strobed into the MOS chip's column address register.

Write Byte – Four Write Byte signals (Write Byte <0–3>H) select the MOS chips associated with the bytes being written in memory as specified by the byte mask bits on the main memory bus. The Write Byte signals are strobed to the MOS chips at Write Time (WR TIM L). The chips storing the check bits are enabled by WR BYTE CK, which is always strobed to the chips when the Write Time signal is low. In order to write data into a MOS chip, MEM SEL L, RASL, CS, and Write Byte L must all be true.

Driver Enable – The Driver Enable signal (DR EN L) enables the internal bus drivers to assert data into the internal array bus during read operations. In order to read data from a chip, MEM SEL L, RAS L, CS, CAS L, and DR EN L must all be true.

Refresh – The Refresh signal (RFCY) forces a Memory Select on all arrays and selects all four rows of chips with the RASL <A,B,C,D> lines. This allows refreshing of all four rows on all the array modules at the same time.

J1 and J2 ID Jumpers – The two ID Jumpers signify that an array module is plugged into a backplane slot and identify the type of array module present in the slot. All of the ID Jumper lines, from the arrays on both sides of the box, are routed to the control A0 module. This control module uses the ID information to calculate memory capacities and to flag a configuration error if the arrays are improperly installed. For the MS11-KE array modules, the jumper configuration is:

- J1 – Jumper Inserted
- J2 – Jumper Removed.

CHAPTER 5
CONTROL MODULES

5.1 GENERAL DESCRIPTION

The controller consists of two hex-multilayer printed circuit boards, one control A module, and one control B module. There are two controllers per memory box, each controls up to eight storage arrays. The A and B control modules, located in the right side of the memory box, backplane slots 11 and 10 respectively, are designated as control A0 and control B0. They control the even-numbered storage arrays in backplane slots 2 through 9. The A and B control modules located in the left side of the memory box, slots 16 and 17, are control A1 and control B1. The A1 and B1 modules control the odd-numbered storage arrays, slots 18 through 25.

5.1.1 Control A Module

The control A module is associated with address, control, and timing functions. Delay line timing chains generate the timing signals which control the various memory cycles: read, write, exchange, refresh, and initialization. This module receives addresses from the address buffer module and sends address, control, and timing signals to a storage array and control B, enabling selected MOS chips on the array for data transfers. Refresh circuitry periodically refreshes the data stored in the MOS chips. During the power-up sequence, control A initializes the memory by writing all zero data patterns into all storage array addresses. Configuration and memory sizing circuits calculate the memory capacity and check for proper installation of the array modules. The controller adapts the address and control signals to make them compatible with storage arrays implemented with either 4K MOS RAM chips or 16K MOS RAM chips.

5.1.2 Control B Module

The control B module is associated with data and error detection and correction. Drivers, receivers, and data registers control the flow of data between the storage array module and the data buffer module. The module checks and generates parity on the data received from and sent to the data buffer; parity is not stored in the arrays. Error detection and correction circuitry generate check bits which are stored with the data in the arrays. The check bits are used during read operations to detect errors in the data. Single-bit errors are corrected by the error correction circuitry. Multiple-bit errors cause four wrong parity bits to be transferred with the data to the data buffer module.

5.2 FUNCTIONAL DESCRIPTION

Figures 5-1 and 5-2 are functional block diagrams of the control A and control B modules. They represent the controller 0 pair, even though the pairs are identical and interchangeable. The control A1 module, however, does not receive J1 ID Jumper signals from all the arrays as shown in the diagram. Its configuration circuitry is inoperative; it does not compute memory capacity or check for configuration errors. Timing diagrams for all six controller memory cycles are included in Appendix C of this manual.

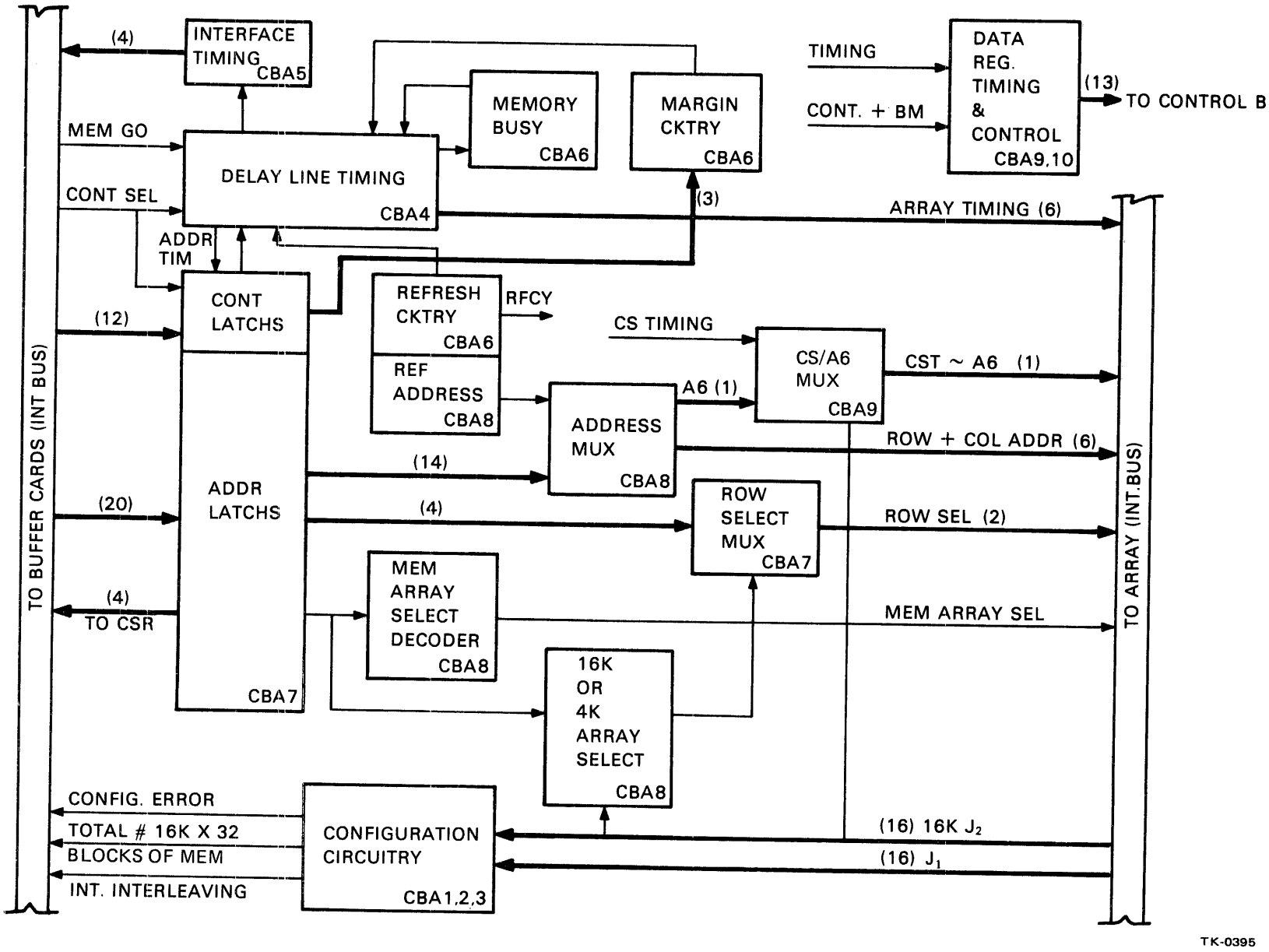


Figure 5-1 Control A Block Diagram

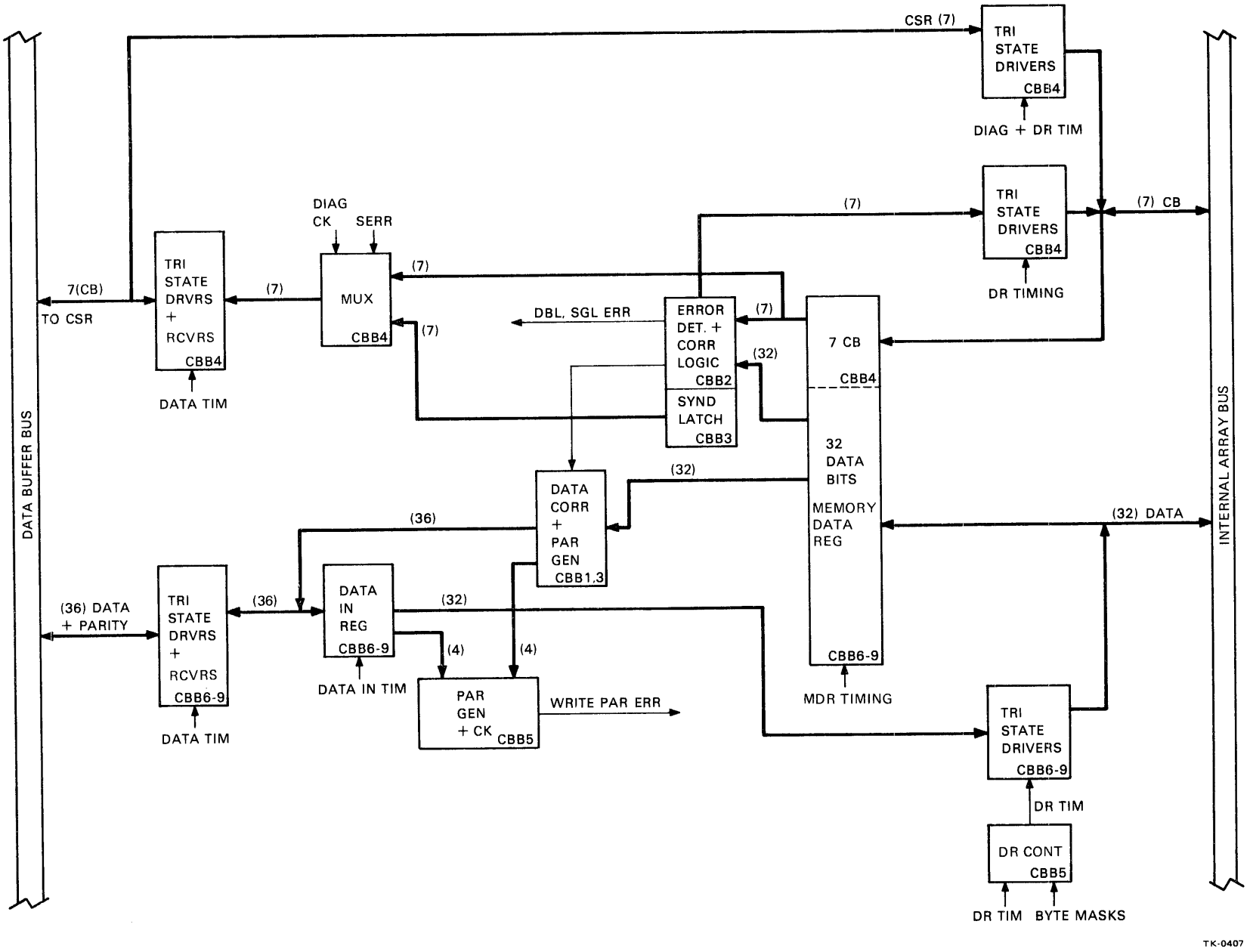


Figure 5-2 Control B (Data and ECC Circuitry) Block Diagram

5.2.1 Timing

A delay line timing chain generates the timing signals which control the memory's cycles. The timing chain begins a timing sequence when triggered by a GO signal from the address buffer module, or a refresh request from the refresh oscillator. There is no priority arbitration on the controller; it services requests from the interface or the refresh oscillator on a first-come/first-served basis. When a memory cycle starts, a memory busy flip-flop is set and the start of another cycle is prevented until the present cycle is completed. For diagnostic purposes, the timing may be altered by the margin control bits, which advance the timing pulses to the data registers.

5.2.2 Address and Control

Address and control signals are asserted onto the internal interface bus by the address buffer module. If the controller is selected by the address buffer, it stores these signals in the address and control latches. The control signals (C0, C1, byte masks, margin, and CSR control functions) in conjunction with the timing signals determine the cycle executed and control the data paths. The address (A<17:02>, Control Select, and Array Select) is strobed onto the internal array bus to select the memory location involved in the data transfer.

Figures 5-3 and 5-4 show how the address on the main memory bus is altered during the addressing process. The bit positions indicated inside the blocks represent the address bits with respect to the address on the main memory bus. The bit positions labeled below the boxes indicate their signal names on the internal buses. Figure 5-3 is an example of 2-way external and internal interleaving. Figure 5-4 is an example of 4-way external and internal interleaving. Addressing in non-interleaved systems is straightforward since no bit position swapping is performed by the address buffer module.

The array selection is computed on the address buffer module from address bits A16 through A21. An array select decoder on control A enables one of the array modules with a Memory Select signal decoded from Array Select <0–2>. This allows only one array to respond to the addresses asserted on the internal array bus by the row select and address select multiplexers. The row select multiplexer selects address bits A14 and A15 and asserts them onto the internal array bus as Row Select A<0,1>. The address multiplexer strobes to the arrays a 6-bit row address and then a 6-bit column address via the same six address lines on the internal array bus. Refer to Appendix A for the timing requirements of these address signals.

If the selected array is implemented with 16K MOS chips, the addressing differs from the addressing of the 4K MOS chips described above. Figure 5-5 illustrates the origin of the array addresses when the 16K ID lines (J2 jumpers) indicate that the array is a 16K MOS chip array. The row select multiplexer uses address bits A16 and A17 to select the row of MOS chips on the array. The address multiplexer strobes a 7-bit row and then a 7-bit column address to the arrays. The A6 address bit is fed through the CS/A6 multiplexer for 16K MOS chips. The 4K MOS chips require only a 6-bit row and column address, but require a Chip Select signal. For the 4K MOS chips, the CS/A6 multiplexer asserts the Chip Select signal (CS) onto the internal array bus rather than the A6 address bit.

Note that the controller does not place sequential addresses into sequential locations on the array module while interleaving. Refer to Figure 5-3. The row of chips on the array is not selected by the most significant address bits, but by A14 and A15. The most significant bits, in this case, become the least significant bits of the chip's row address.

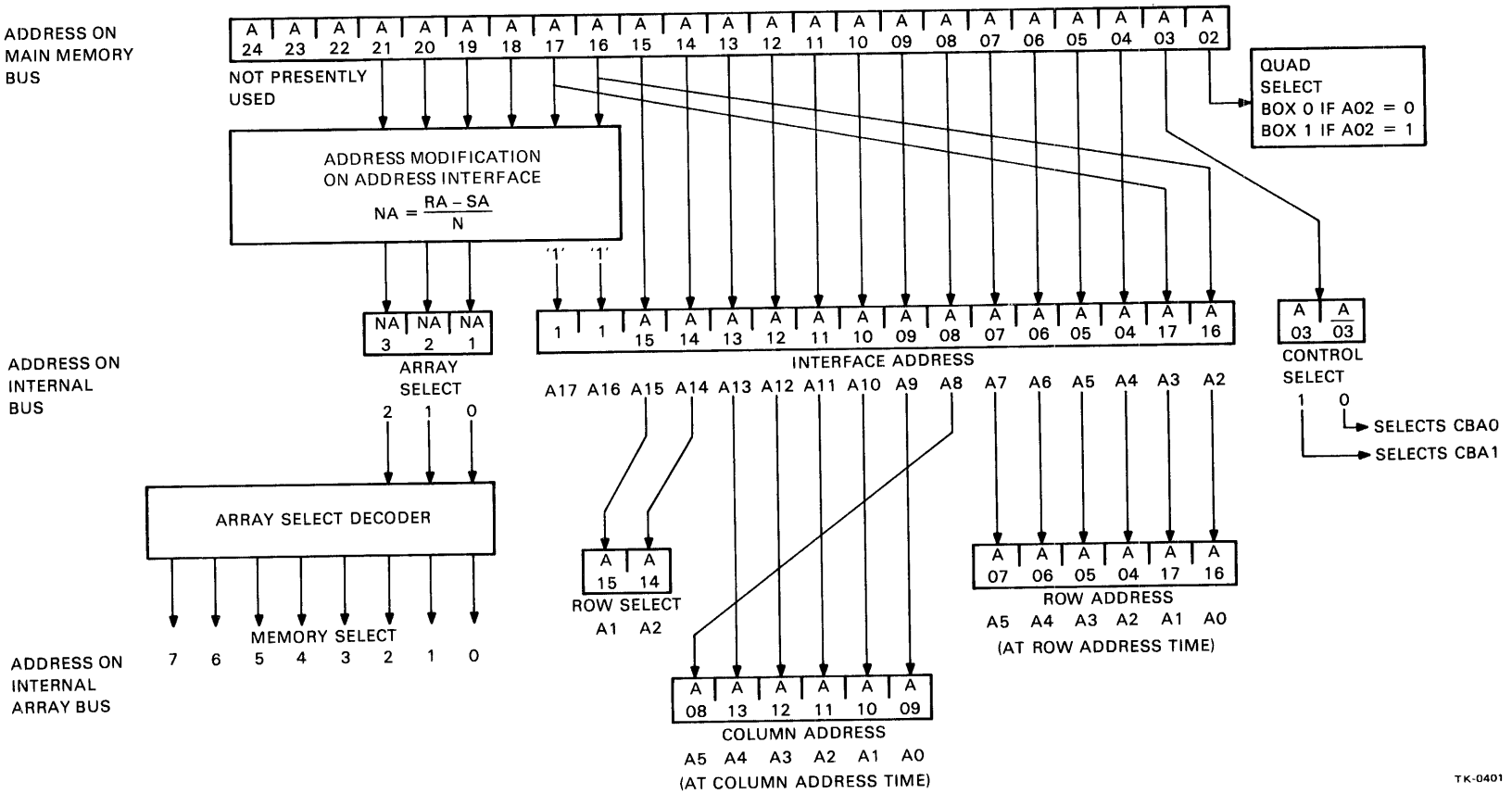


Figure 5-3 Memory Addressing with 2-Way External and Internal Interleaved System

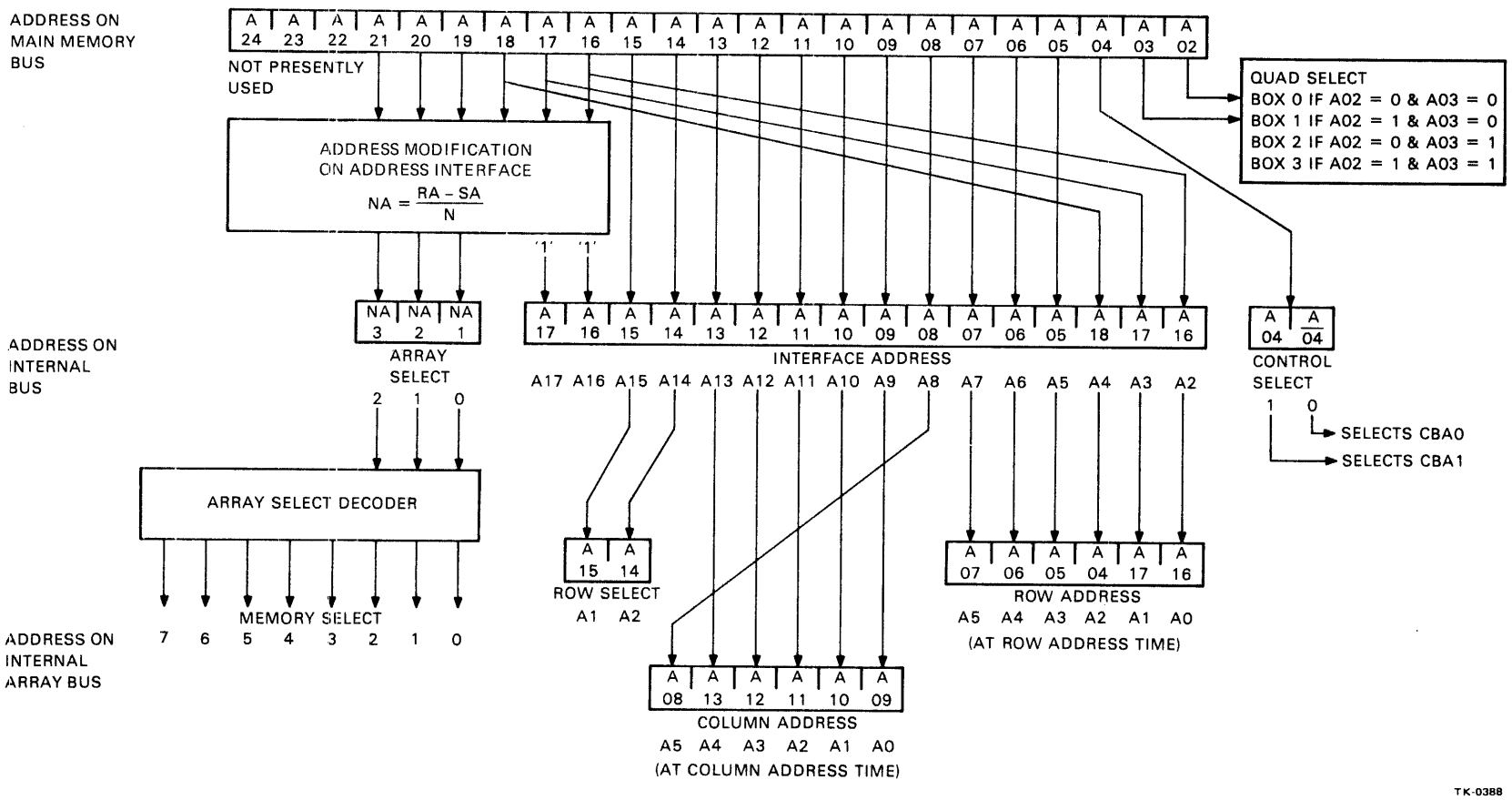


Figure 5-4 Memory Addressing with 4-Way External and Internal Interleaved System

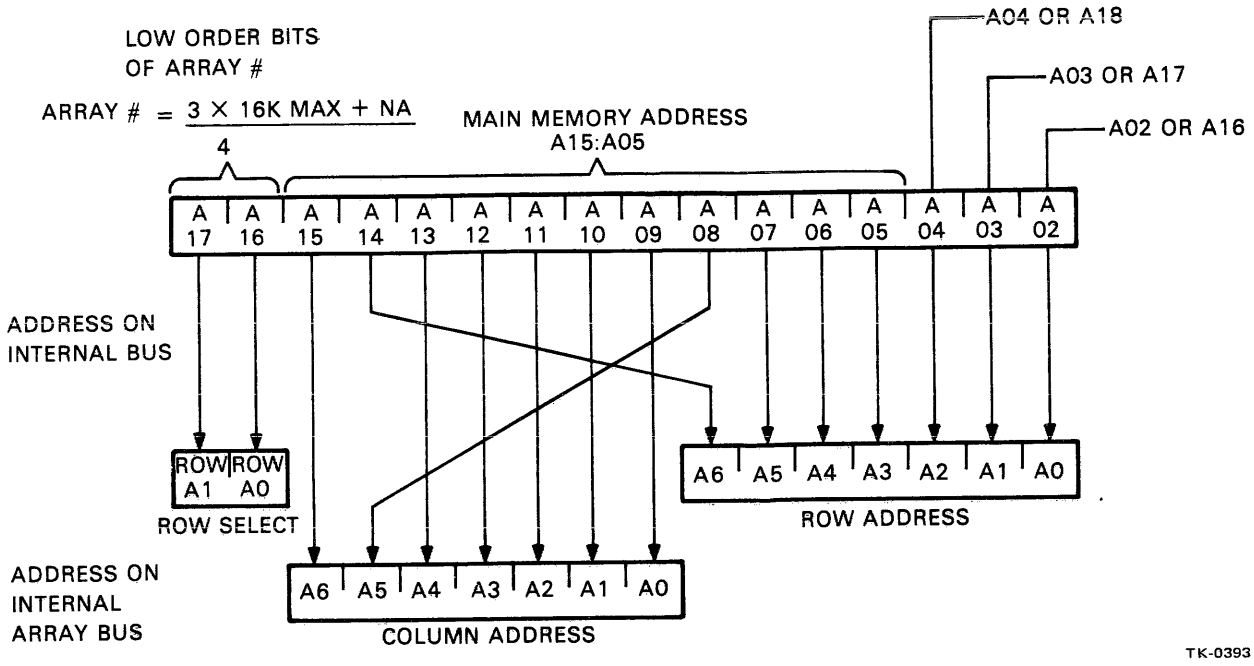


Figure 5-5 Row Select, Row Address, and Column Address For Arrays with 16K MOS RAM Chips

5.2.3 Data Paths

Tri-state driver and receivers interface the registers on the control B module to the internal buses. The controller has two major data registers, the data-in register (DIR) and the memory data register (MDR). A simplified 1-bit slice of the data path through the memory is depicted in Figure 5-6. The data-in register latches data and parity from the data buffer module. This data, stripped of its parity, is loaded into the MDR where parity bits and check bits are computed. Parity, generated from the data in MDR, is compared to the parity stored in the DIR. A mismatch in the parity bits indicates a parity error. An even number of check bits will be inverted to simulate a double-bit error code stored with the data. After the check bits are generated, the data on the internal array bus is clocked into the addressed MOS array chips.

Data and check bits on the internal array bus, asserted by drivers on the arrays, are loaded into the MDR. The data is held in the MDR during the error detection and correction process. If a single-bit error is detected, the erroneous bit is inverted at the XOR gate (COR DXL). After the error detection and correction process, the tri-state drivers assert the data and the parity bits generated during error detection onto the internal bus.

5.2.4 Error Detection and Correction

Seven check bits are computed from combinational parity checks on the data latched in the MDR. The check bits are computed from parity generated on the data bits indicated in Table 5-1. For example, check bit C32 is an odd parity bit determined by the number of data bits 8 through 31 which are equal to one. Each bit of the 32-bit data double word is involved in the computation of 3, 5, or 7 of the check bits. Data bit 0, for example, is one of the bits used to generate check bit C_8, check bit C_{16}, and check bit C_T. Changing the value of bit 0 will, therefore, change the value of check bits C_8, C_{16}, and C_T. Likewise, changing the value of any 1 bit alters a unique combination of either 3, 5, or 7 check bits. Conversely, the data bit that changed can be deduced by examining the check bits that have changed.

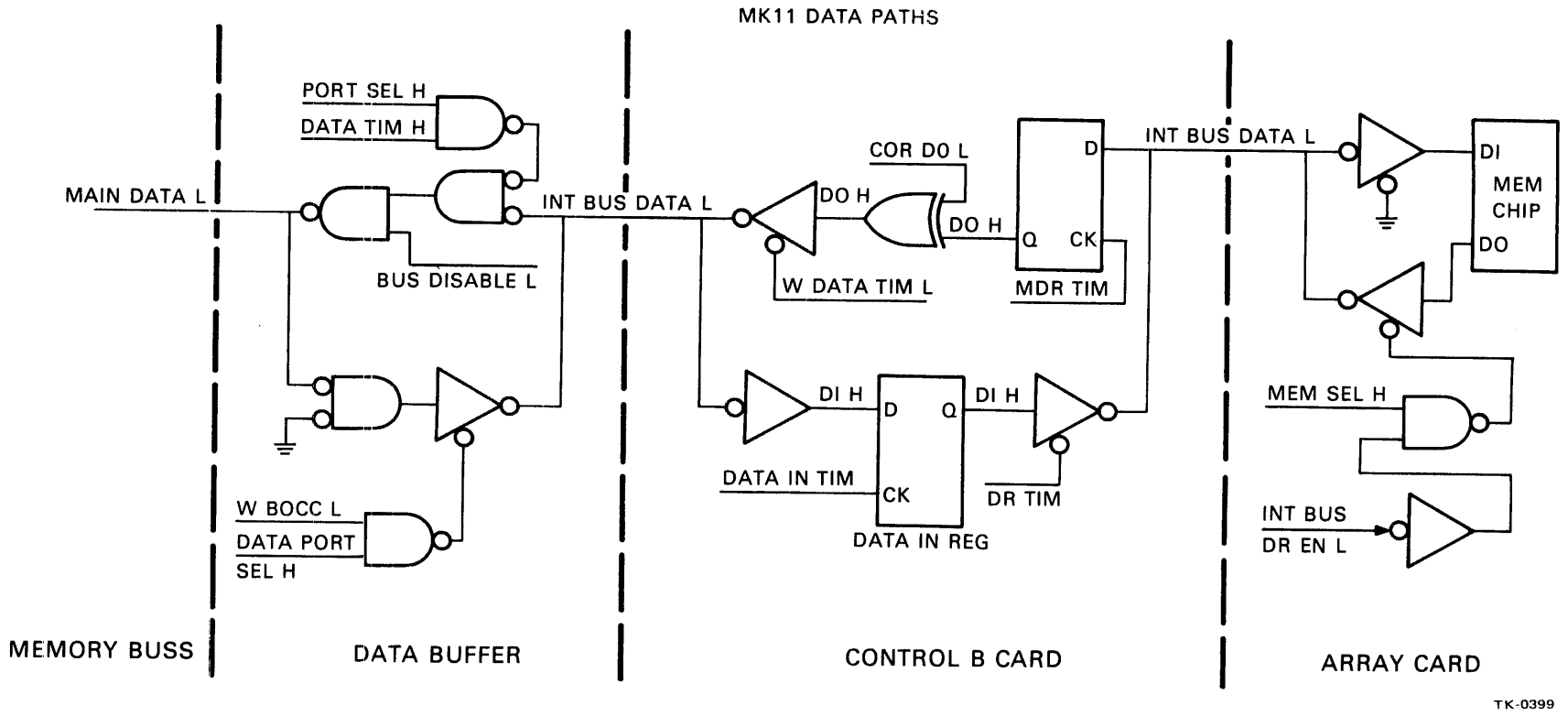


Figure 5-6 MK11 Data Paths

Table 5-1 Generation of ECC Check Bits

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C_1 is Odd Parity on Bits	X		X		X		X		X		X		X		X		X		X		X		X		X		X		X		X	
$C_2$is Odd Parity on Bits	X	X			X	X			X	X			X	X			X	X			X	X			X	X			X	X		
C_4 is Odd Parity on Bits	X	X	X	X					X	X	X	X					X	X	X	X					X	X	X	X	X	X		
C_8 is Odd Parity on Bits	X	X	X	X	X	X	X	X									X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
C_{16} is Odd Parity on Bits	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X									X	X	X	X	X	X	X	X
C_{32} is Odd Parity on Bits	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X								
C_T is Odd Parity on Bits	X			X		X	X			X	X		X			X		X	X		X			X		X	X		X			X
	3-7	3-6	3-5	3-4	3-3	3-2	3-1	3-0	2-7	2-6	2-5	2-4	2-3	2-2	2-1	2-0	1-7	1-6	1-5	1-4	1-3	1-2	1-1	1-0	0-7	0-6	0-5	0-4	0-3	0-2	0-1	0-0
	Byte 3								Byte 2								Byte 1								Byte 0							

Changing the value of 2 bits of the 32-bit data double word alters the value of an even number of check bits. For example, if data bits 0 and 1 change, the values of check bits C_8 and C_{16} remain the same since both data bit 0 and data bit 1 are involved in the parity checks that generate C_8 and C_{16}. Check bits C_1 and C_T, however, will change since they are not involved with both data bits. Whenever an even number of check bits change, it can be assumed that 2 data bits have changed values. Table 5-1 shows that several other combinations of 2 data bits changing value cause check bits C_1 and C_T to change (for instance, data bits 6 and 7 or data bits 8 and 9). Observing an even number of check bits changing indicates that 2 data bits have changed, but it is impossible to determine from the check bits which 2 data bits caused the change.

During write operations, the byte parity bits generated on the data in the MDR are compared with the byte parity bits stored in the DIR. If the parity bits differ, a write parity error is flagged. The byte parity bits and other parity checks are combined to form the 7 check bits: C_1, C_2, C_4, C_8, C_{16}, C_{32}, and C_T. A write parity error inverts an even number (4) of check bits, simulating a double-bit error code. The 7 check bits are then stored with the data in an array module.

During read operations, data and check bits from an array are latched into the MDR. Again, 7 check bits and byte parity bits are generated on the data in the MDR. These check bits are compared (XORed) with the check bits latched in the MDR creating syndrome bits. The syndrome bits indicate changes in the 2 check bit patterns. An even number of syndrome bits indicate a double-bit error, an odd number of syndrome bits indicate a correctable single-bit error, and no syndrome bits indicate valid data. When no errors are detected in the data, the byte parity bits and the data are transferred to the data buffer. If a double-bit error is detected, the 4-byte parity bits are inverted in order to force a parity error on the memory bus. If a single-bit error is detected, the bit in error and the parity bit for the byte in error are corrected.

Table 5-2 shows the decoding of syndrome bits for correcting single-bit errors. Syndrome bits S_{32}, S_{16}, and S_8 indicate the byte containing the bit in error. Syndrome bits S_4, S_2, and S_1 point to the bit in error. For example, syndrome bit pattern 1011000, points to bit 0 of byte 0. In this case, bit 0 and the parity bit for byte 0 are inverted, correcting both the bit in error and the parity.

Any odd number of syndrome bits formed tht do not point to a byte (that is, S_{32}, S_{16}, $S_8 \neq$ 011, 101, 110, or 111) indicate a check bit error. It is then assumed that only the check bits are in error and that the data is valid. No attempt is made to correct the data; correct byte parity is generated, and the data and parity are transferred to the data buffer. The single-bit error information will be loaded into the CSR.

Table 5-2 Decoding Syndrome Bits for Single-Bit Errors

	If Syndrome Bits Equal							Then Single-Bit Error is:	
	S_T	S_{32}	S_{16}	S_8	S_4	S_2	S_1		
Byte 0	1	0	1	1	0	0	0	0	0-0
	0	0	1	1	0	0	1	1	0-1
	0	0	1	1	0	1	0	2	0-2
	1	0	1	1	0	1	1	3	0-3
	0	0	1	1	1	0	0	4	0-4
	1	0	1	1	1	0	1	5	0-5
	1	0	1	1	1	1	0	6	0-6
	0	0	1	1	1	1	1	7	0-7
Byte 1	1	1	0	1	0	0	0	8	1-0
	0	1	0	1	0	0	1	9	1-1
	0	1	0	1	0	1	0	10	1-2
	1	1	0	1	0	1	1	11	1-3
	0	1	0	1	1	0	0	12	1-4
	1	1	0	1	1	0	1	13	1-5
	1	1	0	1	1	1	0	14	1-6
	0	1	0	1	1	1	1	15	1-7
Byte 2	1	1	1	0	0	0	0	16	2-0
	0	1	1	0	0	0	1	17	2-1
	0	1	1	0	0	1	0	18	2-2
	1	1	1	0	0	1	1	19	2-3
	0	1	1	0	1	0	0	20	2-4
	1	1	1	0	1	0	1	21	2-5
	1	1	1	0	1	1	0	22	2-6
	0	1	1	0	1	1	1	23	2-7
Byte 3	0	1	1	1	0	0	0	24	3-0
	1	1	1	1	0	0	1	25	3-1
	1	1	1	1	0	1	0	26	3-2
	0	1	1	1	0	1	1	27	3-3
	1	1	1	1	1	0	0	28	3-4
	0	1	1	1	1	0	1	29	3-5
	0	1	1	1	1	1	0	30	3-6
	1	1	1	1	1	1	1	31	3-7
		Byte Error			Bit in Error				

5.3 MEMORY CYCLES

The memory performs six separate cycles: read, 4-byte write, internal read-modify-write (for writing 1 to 3 bytes), exchange, refresh, and ECC initialization. Read, write, and exhange cycles are initiated by the cache. Refresh and initialization cycles are initiated within the memory. The following describes each cycle through flow diagrams and simplified block diagrams. Signal names and chip numbers included on the flow diagrams indicate the signals associated with the function or decision and point to the schematic diagram page that contains the circuitry involved. Timing diagrams of the six cycles are found in Appendix A of this manual. Use the flow diagrams and timing diagrams in conjunction with the schematics to follow the sequence of events that occurs during a memory cycle.

5.3.1 Read

In a read operation, the controller fetches 4 bytes of data and 7 check bits from an array and transfers 4 bytes of data and 4-byte parity bits to the data buffer. Refer to Figures 5-7 and 5-8, the block and flow diagrams for the read cycle. The address buffer module initiates the read cycle by selecting one of the two controllers and issuing a GO command. Control signals C0 and C1 equal to 0 define the operation as a read. If the controller is not presently executing a cycle (indicated by the memory busy flip-flop), it will start the read timing sequence by triggering the delay line. If the controller is busy, the request will be serviced as soon as the memory busy flip-flop is cleared. When the timing sequence begins, the controller sets its memory busy flip-flop and answers the request by asserting the Bus Occupied and Acknowledge signals onto the main memory bus via the address buffer.

The syndrome latch is reset before each transfer of data to the controller from an array. This ensures that the error information in the syndrome latch reflects the condition of the most recent data transfer.

Thirty-nine bits of data and error correction code (ECC), placed on the internal array bus by the addressed MOS chips, load into the MDR. The bits are latched at MDR time and remain at the output of the MDR until another cycle loads new data into the MDR.

Parity generated on the data latched in the MDR is combined to form 7 check bits. These generated check bits, exclusively ORed with the check bits latched in the MDR, form the syndrome bits. If none of the syndrome bits equal 1, the data is valid. Data drivers gate the 4 bytes of data and 4-byte parity bits, generated during the check bit calculation, onto the internal array bus.

The data and parity is passed to the data buffer module via the internal array bus which, in turn, passes the data and parity to the main memory bus. The controller issues a Data Ready signal to inform the bus master that the data on the main memory bus is valid. The memory releases control of the bus by dropping Acknowledge and Bus Occupied, and turning off the data drivers. Resetting the memory busy flip-flop terminates the cycle, allowing the controller to respond to another memory request.

If the comparison of the check bits produces any error syndrome bits, an error signal is flagged. An error signal inserts a 100 ns delay into the read cycle timing. This is indicated by the dotted lines in the timing diagram in Appendix C. The delay is necessary to allow enough time to detect and correct the error.

The latched syndrome bits, fed into an odd/even parity checker, determine if the error is correctable or not. An odd number of syndrome bits indicates a correctable single-bit error. An even number of syndrome bits indicates an uncorrectable double-bit error.

Single-bit errors are corrected by decoding the syndrome bits that point to the bit and byte in error. The parity bit for the byte in error and the bit in error are corrected (inverted) by XOR gates in the data path.

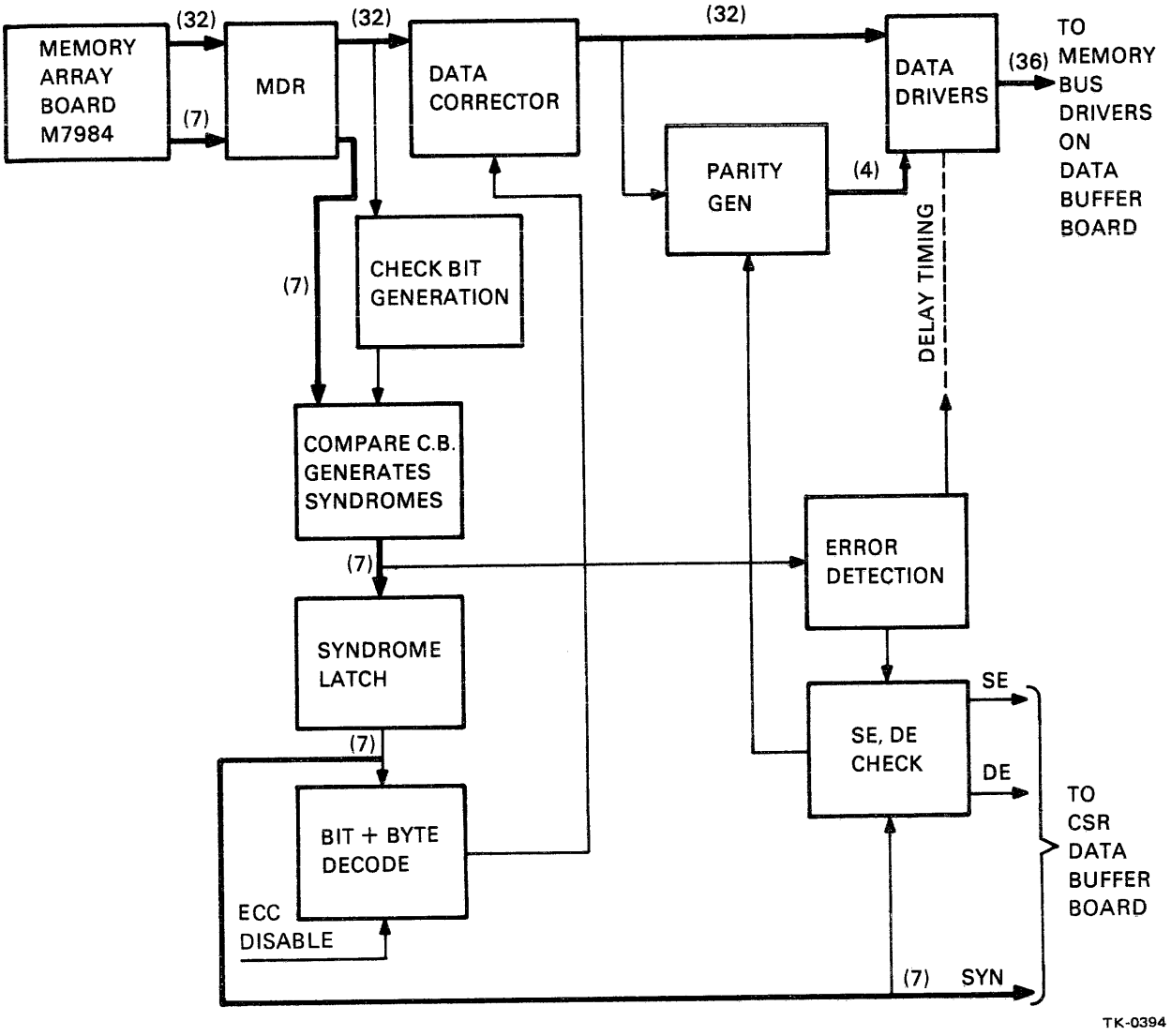


Figure 5-7 Error Correction (Read Cycle)

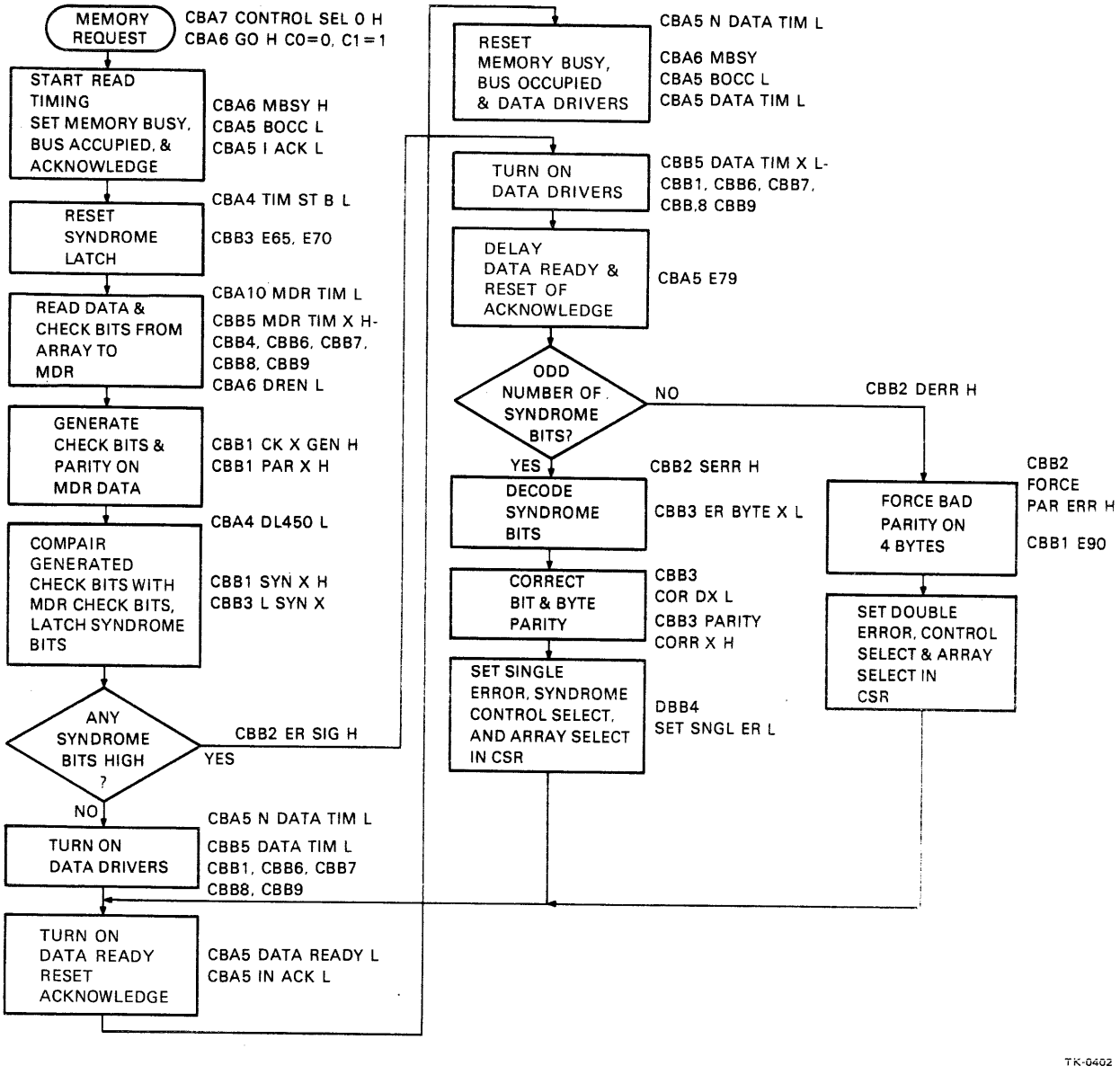


Figure 5-8 Read Cycle Flow Diagram

The CSR stores the error information. Bit 4, first word flags the single-bit error. Setting the single-bit error flag loads the latched syndrome bits into bits 8 through 14 of the first word, the array number into bits 5 through 7 of the first word, and the controller number into bit 9 of the CSR second word. Following the error logging, the controller issues the Data Ready pulse to the bus master and completes the cycle.

Double-bit errors are not correctable. When the number of latched syndrome bits is even, a double-bit error is flagged and all 4-byte parity bits are inverted. This causes 4 parity errors on the main memory bus. Bit 15 in both CSR words is set to flag the double-bit error. The array number and the control number are latched into the CSR. The Data Ready pulse and the other bus control signals follow the same way as above.

The error correction function of the memory can be disabled, either by the CSR or the box controller. With ECC disabled, single-bit errors are handled as double bit errors; the error condition and addresses are logged in the CSR, but the controller makes no attempt to correct the error.

5.3.2 Write

The memory performs two different write cycles, a 4-byte write and a 1- to 3-byte write. Both write cycles are requested by control bits C0 and C1 equal to 0 and 1 respectively. After receiving the write request, the controller examines the byte mask bits. If 4 bytes are transferred, the controller executes a regular (4-byte) write cycle. If less than 4 bytes are transferred, the controller executes an internal read-modify-write (1- to 3-byte) cycle. Refer to Figures 5-9, 5-10, and 5-11.

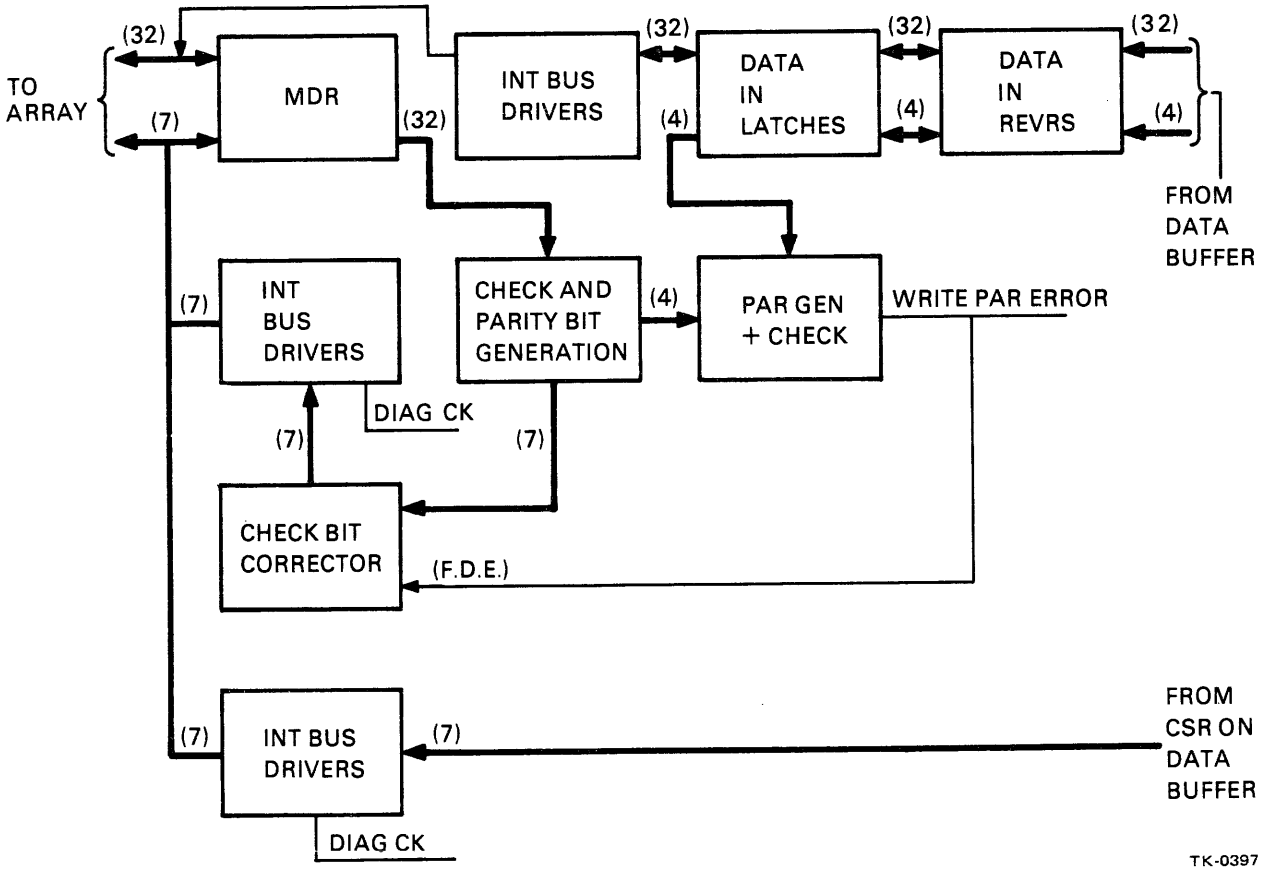


Figure 5-9 4-Byte Write Cycle

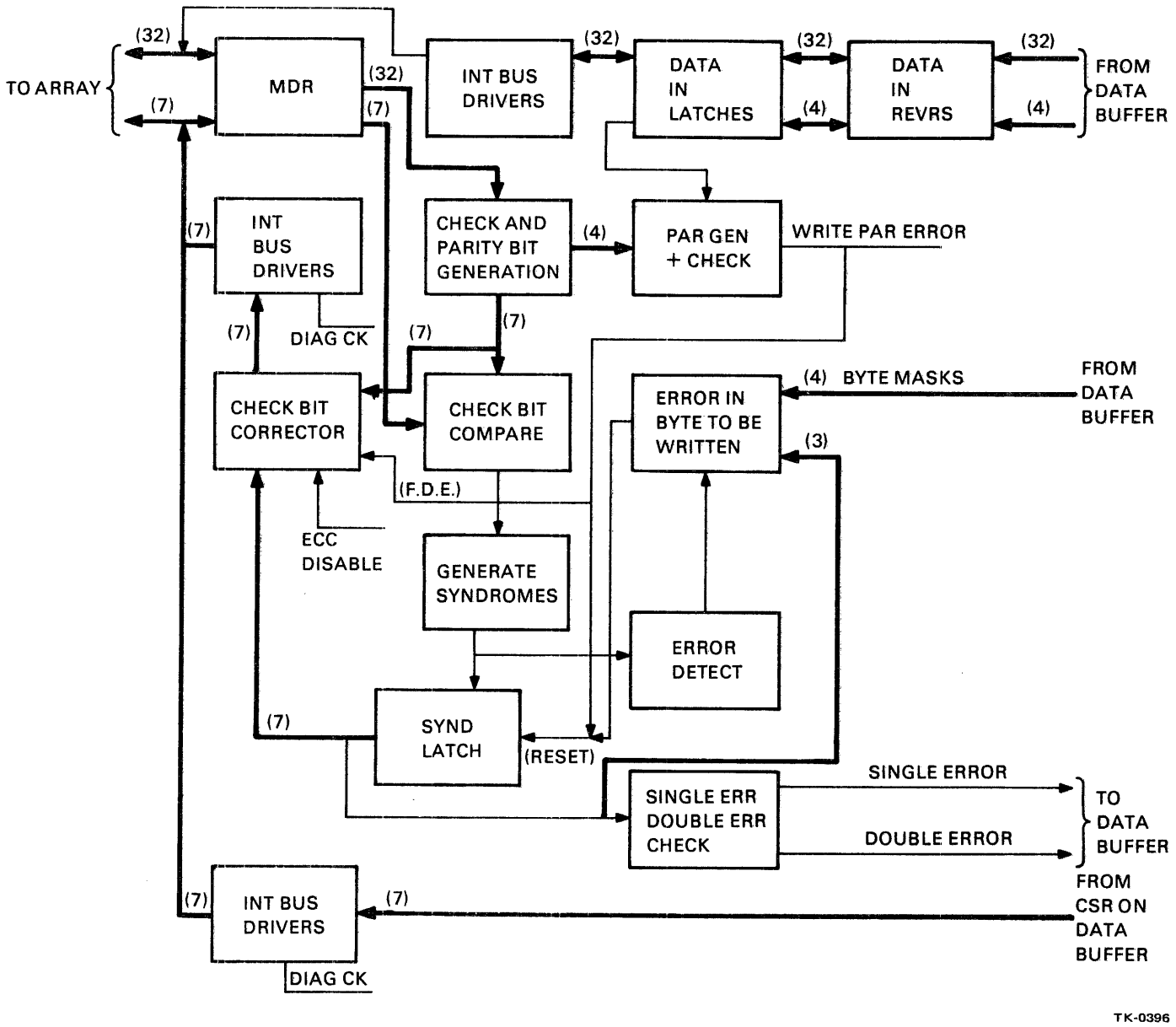


Figure 5-10 Internal RMW Cycle

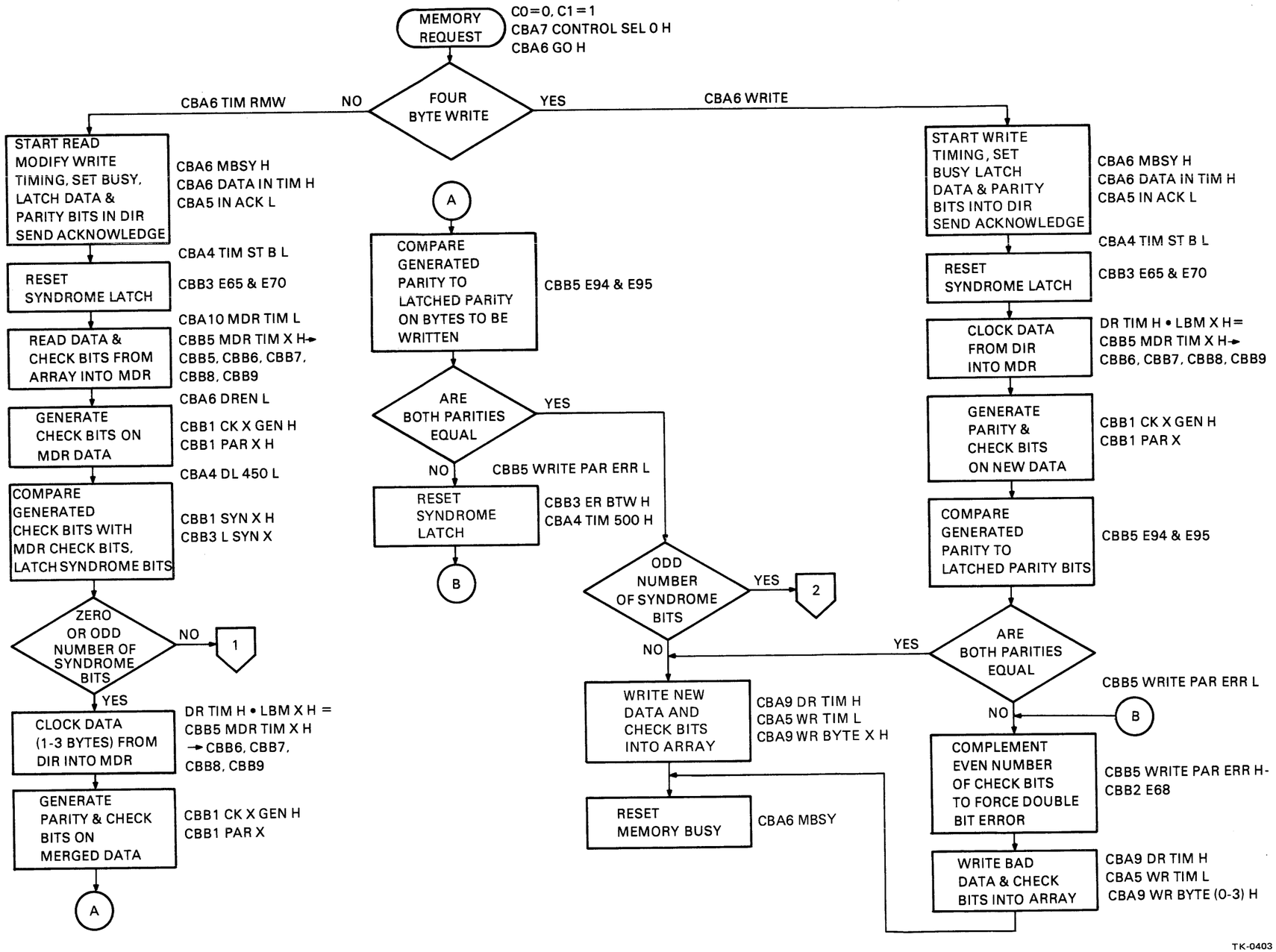


Figure 5-11 Write Cycle Flow Diagram (Sheet 1 of 2)

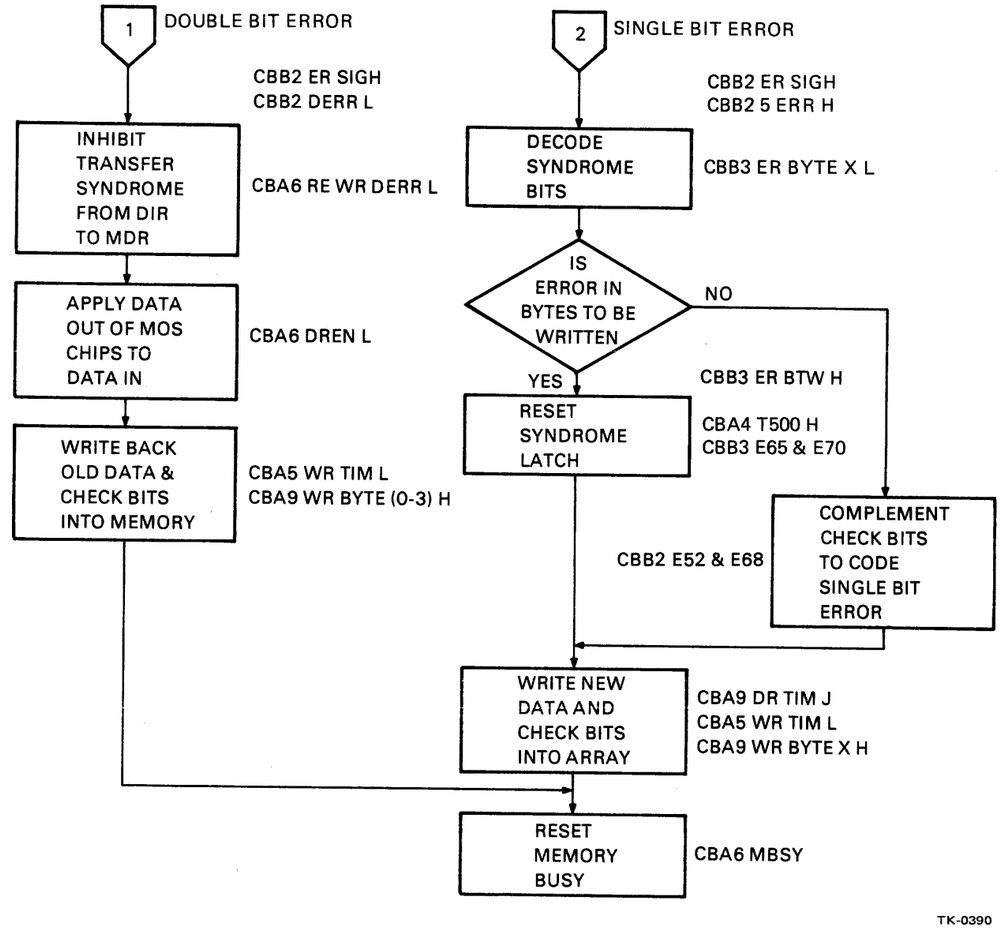


Figure 5-11 Write Cycle Flow Diagram (Sheet 2 of 2)

5.3.2.1 Four-Byte Write – In a regular write operation the controller takes 4 bytes of data and 4 parity bits from the data buffer module and stores the 4 bytes of data plus generated ECC check bits into an array. If the memory busy flip-flop is cleared, the controller is selected, and all 4 byte masks are present. The controller starts the write timing sequence upon reception of the GO signal. The controller sets the memory busy flip-flop to prevent the controller from answering any other cycle requests until the present cycle is completed. At data-in time, the DIR latches the 4 data bytes and parity bits asserted onto the internal interface bus by the data buffer. When the data is loaded into the DIR, the controller sends the Acknowledge signal to the cache via the address buffer and the main memory bus, freeing the bus for another memory request.

Error information from the previous memory cycle is cleared from the syndrome latch. No errors are reported during the 4-byte write cycle; the latch is cleared because latched syndrome bits from a previous memory cycle will affect the check bit generation during this cycle.

Data drivers apply the 4 bytes of data (but not the parity bits) onto the internal array bus. The MDR takes the data from the internal array bus and stores the 4 bytes in its registers. Output lines from the MDR apply the latched data to the ECC parity generators.

Parity generators generate 4-byte parity bits on the latched MDR data. Other parity generators combine their outputs to form the 7 ECC check bits. The 4-byte parity bits generated from the latched MDR data, XORed with the 4-byte parity bits stored in the DIR, perform a parity check on the transferred data.

If the parity from the main memory bus matches the parity bits generated in the controller, then the data is considered valid. Internal array bus check bit drivers assert the 7 generated check bits onto the internal array bus. The 4 bytes of data, latched in the DIR, plus the 7 check bits, generated on the data latched in the MDR, are strobed into a selected array module.

After the data and check bits are stored in the addressed MOS chips, the controller resets its memory busy flip-flop, ending the write cycle. This controller is now ready to execute another memory cycle.

If, however, the parity bits transferred via the main memory bus and latched in the DIR do not match the parity bits generated by the controller, a write parity error is flagged. The write parity error flag forces a simulated double-bit error code in the ECC check bits. The controller inverts 4 of the generated check bits and the internal bus drivers assert the altered check bits onto the internal array bus. The 4 bytes of data and the erroneous check bits are then strobed into the addressed MOS array chips.

When the memory location containing the 4 inverted check bits is accessed during a read or exchange operation, the altered check bits create an even number of syndrome bits. The syndrome bits are interpreted as a double-bit error. This double-bit error causes bad parity to be asserted onto the main memory bus simulating a parity error discovered during the write cycle.

5.3.2.2 Internal Read-Modify-Write – Since the 7-bit check bit code stored in memory must be computed on 4 bytes of data, writing 1 to 3 bytes of data to memory causes an internal read-modify-write cycle. The bytes transferred to memory are merged with the bytes previously stored in memory to create a new 32-bit double word. The controller generates new check bits on the merged 4 bytes and then stores the new data and check bits in the addressed MOS array. Refer to Figure 5-10 and 5-11. An internal read-modify-write cycle begins when the selected controller receives a write-to-memory request with only 1-, 2-, or 3-byte masks present.

The read-modify-write flip-flop sets when less than 4-byte mask bits accompany the control signals from the address buffer module. The controller inserts two additional delay lines into the timing chain; both a read operation and a write operation are performed during a 1- to 3-byte write cycle. At the beginning of the cycle, the controller sets the memory busy flip-flop to prevent the address buffer or the refresh oscillator from initiating another cycle on this controller. The data-in pulse loads the data bytes and their parity bits into the DIR. Once the data is loaded into the DIR, the controller sends its acknowledge to the bus master via the main memory bus, releasing the bus for other tasks.

The syndrome latch clears out the old error information. Data and parity latched in the DIR wait there while the controller begins the read portion of the read-modify-write cycle.

Just as in a read cycle, drivers on the addressed array module assert 39 bits of data and check bits onto the internal array bus. The controller latches the data and check bits into the MDR. The MDR applies the latched data to even/odd parity generators which calculate 7 new check bits. These generated check bits are compared with the check bit latched in the MDR from the array. Syndrome bits formed by comparing the two sets of check bits are then clocked into the syndrome latch in order to check the validity of the 4 bytes of data read from the array.

The latched syndrome bits, if any, determine how the data is handled during the modify portion of the internal read-modify-write cycle. The check bits that the controller writes into the array are formed after merging bytes from the main memory bus with bytes from the addressed array location. Any errors in the data read from the array, therefore, could affect the validity of the data and check bits written into the array. There are four possibilities.

1. If there are no syndrome bits (no errors), check bits are generated on the merged 4-byte double word.

2. If the syndrome bits indicate a single-bit error in a byte that will be written over by a new data byte, the syndrome latch is cleared and check bits are generated on the merged 4-byte double word.

3. If the syndrome bits indicate a single-bit error in a byte that will not be written over, check bits that point to the bit in error are generated for the double word.

4. If the syndrome bits indicate a double-bit error, the write operation is aborted.

If no errors are detected in the data read from the array, the bytes written into the DIR are clocked onto the internal array bus and into the MDR. For this discussion, assume that 2 new bytes, bytes 0 and 1, have been transferred to memory. The process can easily be generalized to a 1- or 3-byte transfer.

The data stored in the MDR now consists of bytes 0 and 1 from the main memory bus and bytes 2 and 3 of the double word from the addressed array. Parity and ECC check bits are generated on the 4 bytes in the MDR. The controller compares the generated parity bits on the new bytes 0 and 1 to the byte parity bits transferred via the main memory bus. If there are no parity errors associated with the data bytes transferred to memory, the controller writes the new bytes, 0 and 1, and the new check bits into the array.

At write time, the data bytes latched in the DIR are strobed into the array bytes selected by the byte masks. The 7 check bits generated on the 4 bytes of data latched in the MDR, are also strobed into the array. The memory busy flip-flop is reset completing the cycle.

An even number of syndrome bits in the syndrome latch sets the double-bit error signal. A read-modify-write double error inhibits the drivers at the output of the DIR, preventing the controller from transferring data to the internal array bus or to the MDR. Drivers on the array module gate the data and check bits at the output of the MOS chips to their input pins via the internal array bus. At write time, the 4 bytes of data and the 7 check bits are written back into the addressed memory location. The next read operation to this address detects the double-bit error and causes a parity trap. The bytes that were to be written during this write cycle are lost.

An odd number of syndrome bits in the syndrome latch signals a single-bit error in the data read from the array. The latched syndrome bits are decoded to find which byte contains the error. If the single-bit error is in a byte that will not be rewritten via the DIR into the array, the controller alters the check bits. The latched syndrome bits invert an odd number of the check bits generated on the 4 bytes latched in the MDR. These inverted check bits code a single-bit error in the addressed double word, which will be detected during the next read operation to this address. If the single-bit error is in a byte that will be overwritten by the data in the DIR, the syndrome latch is cleared. The check bits generated on the valid 4 bytes of data latched in the MDR will be written into an array.

When the parity check discovers a parity error in the bytes transferred on the main memory bus, a write parity error is flagged and the syndrome latch is cleared. Resetting the syndrome latch clears out error information on the data read from the array which might affect coding of the check bits. An even number of check bits are inverted to code a double-bit error. The controller then writes 4 bytes of data and the double-bit error code into the addressed array. The parity error will be detected as a double-bit error during the next read operation to that memory location.

5.3.3 Exchange Cycle

An exchange cycle is similar to the internal read-modify-write cycle. In the exchange cycle, however, the data read from the array is transferred to the data buffer and then asserted on the main memory bus. Prior to transferring the data to the data buffer, any single-bit errors are corrected. Refer to the flow diagram, Figure 5-12.

Control bits C0 and C1 equal to one code an exchange cycle. The GO signal starts the internal read-modify-write timing sequence and the controller reads the data from the main memory bus. Memory busy is set and the data bytes and parity on the main memory bus are latched into the DIR. The memory acknowledges the receipt of the data and sets its bus occupied flag. The timing chain then clears the syndrome latch.

Four bytes of data and 7 check bits are read from the addressed array. The array module asserts 39 bits onto the internal array bus and the controller loads the data and check bits into the MDR. Parity generators calculate byte parity and 7 new check bits which are compared with the latched check bits for error detection. Any syndrome bits formed by the comparison are stored in the syndrome latch. If a single-bit error is detected, the controller delays the timing, corrects the error, and logs the error in the CSR. The double-bit error case will be covered later.

Data drivers on the controller gate 4 bytes of valid data and 4-byte parity bits to the data buffer. A data ready flag signals that the data is on the main memory bus. The Acknowledge signal resets and then the Bus Occupied signal is dropped, releasing the main memory bus for other memory cycles.

The data bytes written to memory merge with the data from the array in the MDR. A parity check tests the parity on the new bytes loaded into the MDR. If a parity error is detected, the syndrome latch resets and the check bits code a double-bit error. At write time, the controller writes the data and the double-bit error check bit code into the array.

If the parities are equal and no errors are detected in the double word read from the array, the controller writes the new bytes and the new check bits into memory. A single-bit error detected in the data from the array is handled as in the internal read-modify-write cycle. When the single-bit error resides in a byte that will be overwritten by the write, the syndrome latch is cleared and correct check bits are written into the array. If the single-bit error remains in the array after the write, the latched syndrome bits complement check bits in order to code a single-bit error. At write time, the bytes selected by the mask bits and the ECC check bits are written into the selected array location.

When the latched check bits indicate a double-bit error, the write portion of the exchange cycle is aborted and parity errors are forced on the main memory bus. The controller generates 4 bad byte parity bits on the data latched in the MDR from the array. The CSR logs the double-bit error information. Control signals on the main memory bus transfer the data and bad parity and then release the bus for other cycles. No data is transferred from the DIR to the MDR, and the controller is inhibited from asserting data onto the internal array bus. At write time, the 4 bytes of data and check bits at the output of the selected MOS array chips are strobed back into the inputs.

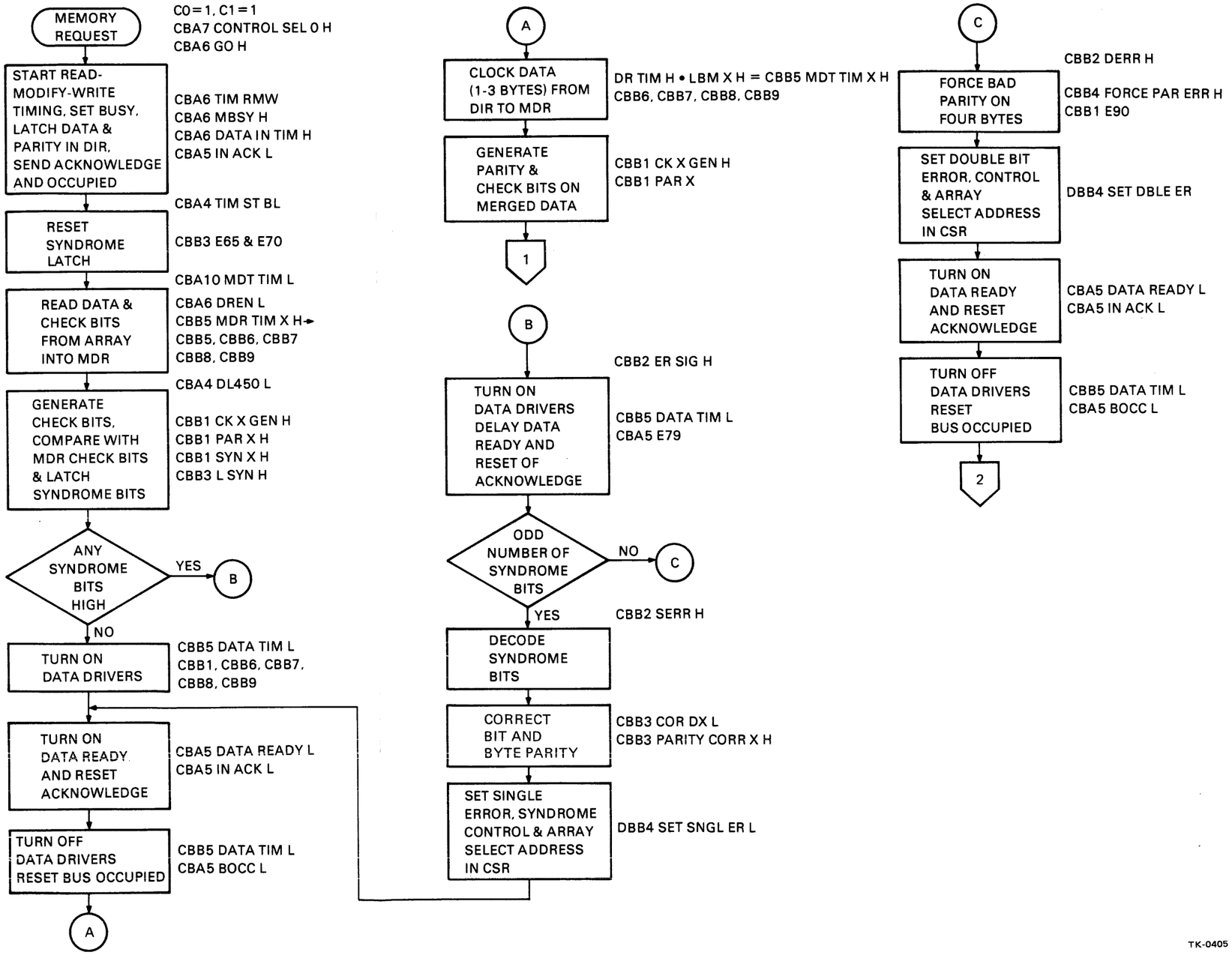


Figure 5-12 Exchange Cycle Flow Diagram (Sheet 1 of 2)

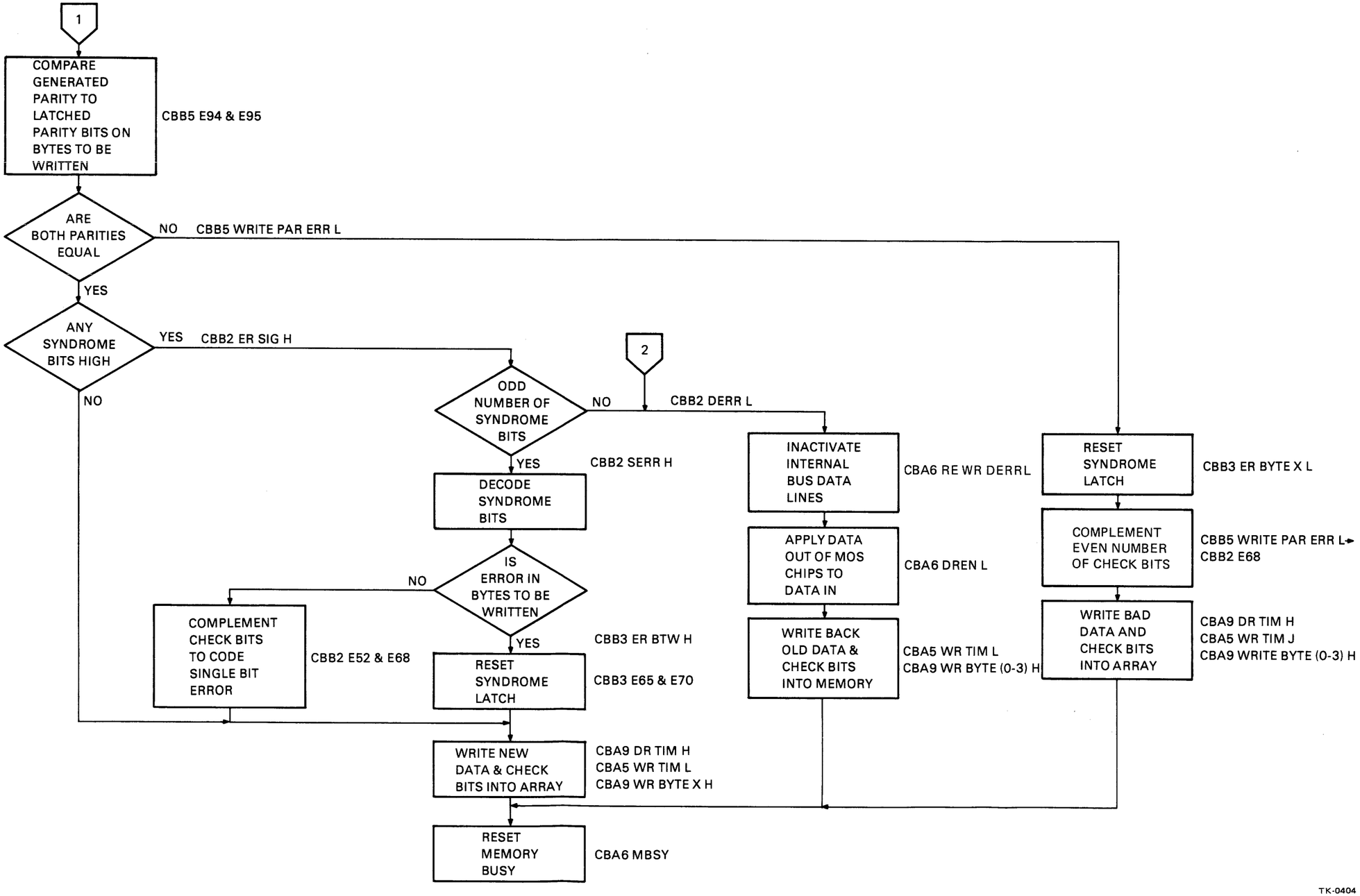


Figure 5-12 Exchange Cycle Flow Diagram (Sheet 2 of 2)

5.3.4 Refresh

A refresh cycle restores the data held in an entire row of the MOS chip cell matrix. The 4K MOS chips are internally organized as a 64- by 64-bit cell matrix. Normally, data is accessed by selecting one bit cell in the matrix with both a column and a row address. During refresh cycles, however, only a row address is supplied, and all columns in the row are refreshed simultaneously. The refresh address selects a cell matrix row on all four rows of MOS chips on all the array modules connected with the controller. A refresh cycle occurs every 25 μs; all 64 cell rows are refreshed every 2 ms or less, depending on the number of memory cycles performed.

The 16K MOS chips are internally organized as a 128- by 128-bit cell matrix. When the controller recognizes an array with 16K MOS chips, the refresh rate is increased to approximately 12.5 μs. At this faster rate, all cell rows are refreshed in the same period of time (<2 ms).

The refresh oscillator triggers the delay line timing chain every 25 μs (or 12.5 μs with 16K chips) if the memory is not busy. The timing sequence sets the memory busy flip-flop, delaying any memory cycle requests until the refresh cycle ends. Row addresses for the refresh come from the refresh address counter, which clears to 0 on power-up and increments after each refresh cycle. The address multiplexer (Figure 5-1) selects the refresh address count and asserts the address onto the internal array bus. A Refresh signal, sent to the arrays, overrides the array select and row select addresses. All MOS chips on all arrays are enabled, and the addressed matrix row is refreshed. The refresh address counter then increments and the memory busy flip-flop resets, ending the cycle.

5.3.5 ECC Initialization

The memory is initialized upon power-up to produce correct check bit codes in all memory locations prior to accessing any memory locations. ECC initialization performs several 4-byte writes of all 0 data, plus generated check bits, to every address on all the arrays. As in the refresh cycle, all rows of MOS chips on all arrays connected to the controller are enabled simultaneously.

Initialization cycles are initiated by the refresh oscillator. Addresses are derived from the address latches (Figure 5-1) which operate as counters during initialization. The count in the address latches increments after each cycle until the counter overflows. When address bit 15 of the address latches toggles, an overflow signal is clocked from the refresh address counter, which ends the initialization. The refresh oscillator initiates 32K cycles, writing data to every location eight times in 4K MOS chips, and twice in 16K MOS chips.

On power-up, the ECC INIT flip-flop (CBA10) is set, starting initialization, forcing an AC Low signal, and clearing the address latches to 0.

When the refresh oscillator fires, a cycle resembling a 4-byte write cycle begins, clearing the syndrome latch and generating check bits on the all 0 data. The all 0 data check bit pattern is 0111111. The array select and row select signals are overridden to select all rows and all arrays associated with the controller. The count in the address latches is multiplexed by the address multiplexer to form the chip matrix row and column addresses. Four bytes of 0s and 7 check bits are then strobed to every array. One is added to the count in the address latches, and another cycle begins when the refresh oscillator triggers again.

5.3.6 Configuration Circuitry

The J1 and J2 ID Jumper lines (fingerprints) from all 16 array slots route through the backplane to the control A0 module. Configuration circuitry on the controller scans through the array slots, calculating memory capacity and flagging any configuration errors. It enables internal interleaving if the capacities of both sides of the memory box are balanced. A configuration error is flagged if an empty array slot is discovered between array modules or if a 64K array module is found between 16K array modules. In order to normalize the addresses on the address buffer module, there must be no empty array slots before the last array and all 16K arrays must precede the 64K arrays. Refer to the configuration circuitry block diagram, Figure 5-13 and the flow diagram, Figure 5-14. All the configuration circuitry appears on pages CBA1, CBA2, and CBA3 of the schematic diagrams.

A master clock causes the address counter to sequence through the array slot numbers. Multiplexers on the controller look at the ID lines of each array slot in the memory box. The ID signals, decoded by the decoder, increment the array summing counters which keep track of the number of 16K arrays and 64K arrays.

When the multiplexers have scanned all the array slots, the totals of the 16K arrays and the 64K arrays latch into their respective summing latches. From these latches, the total capacity, in 16K × 32-bit blocks, is computed in the adder. The 16K and 64K summing counters are cleared and the multiplexers scan the array slots again. This continues as long as the memory is powered up. Configuration circuitry on the control A module plugged into the control A1 slot location is not allowed to compute memory capacity or to flag configuration errors.

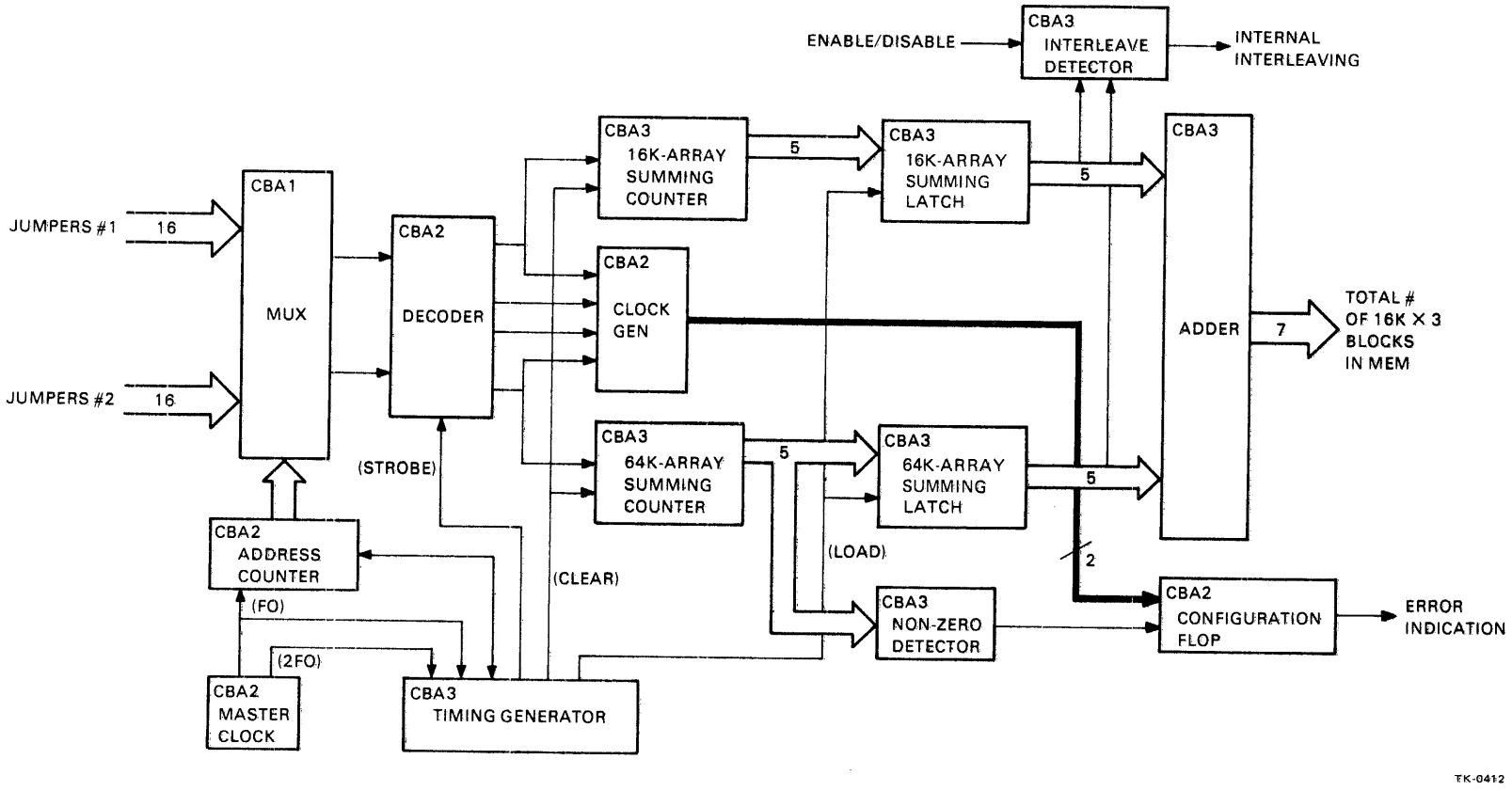


Figure 5-13 Configuration Verification Circuit Block Diagram

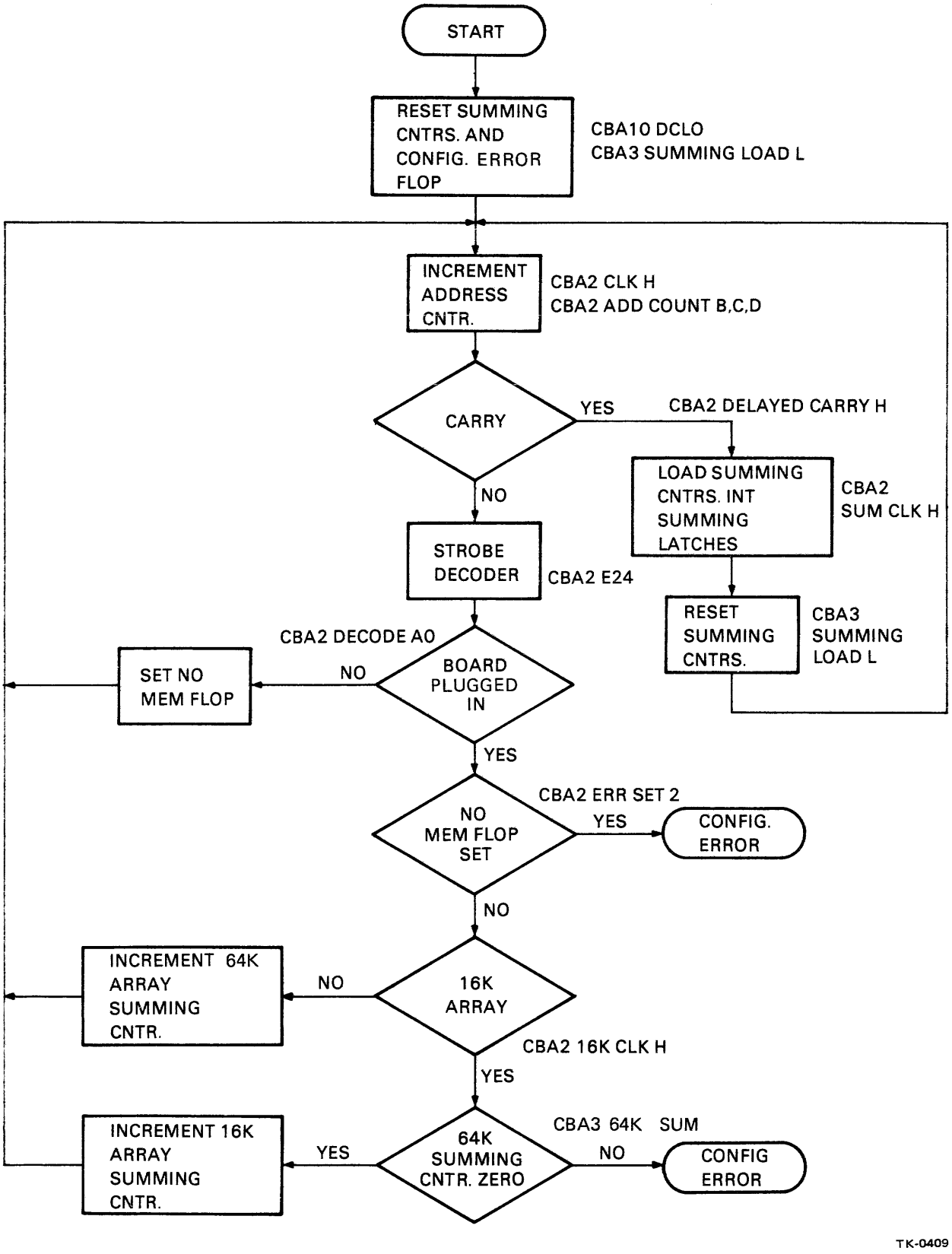


Figure 5-14 System Configuration Circuit Flow Diagram

CHAPTER 6
ADDRESS BUFFER AND DATA BUFFER MODULES

6.1 GENERAL DESCRIPTION

The address buffer module receives addresses from the main memory bus and modifies these addresses to select the corresponding control modules and array module. It uses starting address, memory capacity, and interleaving information to determine if an address is within the range of addresses serviced by the module. It examines the addresses to determine if they match the address of the control and status register (CSR) set by switches on this module. Every address buffer module connected to the main memory bus checks each bus address for correct parity and can assert a parity error signal onto the bus if the parity is in error. There are two fault indicator lights on this module; one signals an address parity fault, and one signals a configuration error. A configuration error indicates that the array modules have been improperly installed in the memory box.

The data buffer module contains the data paths between the main memory bus and the control modules and between the main memory bus and the CSR. It contains the registers and gates that make up the CSR and timing circuits that control the memory's cycle timing during reads and writes directed to the CSR. A ribbon cable carries starting address and interleaving information to the data buffer module from the box controller. A bank of switches is provided on the module to override the switches in the box controller. An indicator light on this module signals a double-bit error condition in a word being read from memory.

Figure 6-1 shows a simplified block diagram of the data and address paths between the main memory bus and the control modules via an internal tri-state bus.

6.2 ADDRESS BUFFER MODULE (M8158)

6.2.1 Main Memory Bus Interface

Main memory bus address and control cables plug directly into connectors on this module. All of the address and control signals except three are buffered by tri-state line receivers. The exceptions, Main Acknowledge, Main Parity Error, and Main Bus Occupied are transmitted signals that are driven by open collector line drivers. These drivers are prevented from asserting signals onto the Main Memory Bus by Bus Disable if the dc power is below tolerance. The receivers are always enabled by Input Enable Low, which is forced low in single-port memories.

6.2.2 Address Parity Checking

The address and control signals are checked for even parity. If the parity is incorrect, Wrong Parity disables the GO signal which normally triggers a memory cycle on the control module. When cache issues a start command to memory, the parity fault indicator lights and Main Parity Error is asserted on the main memory bus. A parity fault can only be cleared by powering up the memory.

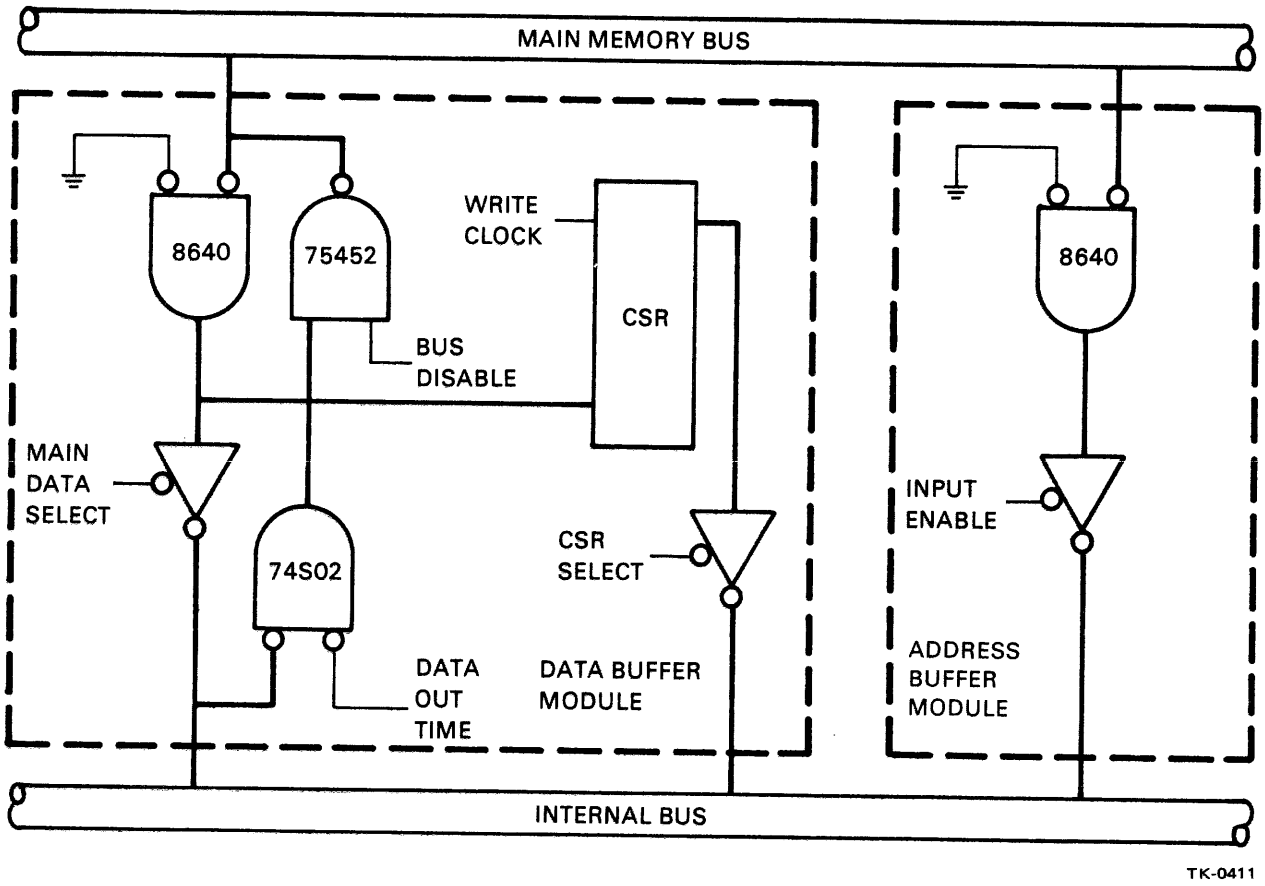


Figure 6-1 Simplified Diagram of the Data and Address Paths Through the Data Buffer Module and the Address Interface Module

6.2.3 Address Modification

From the time an address appears on the main memory bus and before start is issued, the address buffer module modifies the bus address to select a control module and array module within the memory box. The modified address is then placed on an internal bus where it is available to the control modules. The modification is a function of the starting address assigned to the box, the type of interleaving within the memory system, and the number and types of storage arrays installed in the box. The module normalizes each address and tests it to find if the address is:

- Greater than the starting address of the box
- Less than the highest address in the box
- Included in the set of addresses serviced by the box due to external interleaving
- Located on a 16K × 32-bit or a 64K × 32-bit storage array module.

If the address is within the range of addresses assigned to the box, the address buffer module generates a GO signal upon reception of the start command. The modified address selects a pair of control modules and an array module. The GO signal initiates a memory cycle on the selected controller.

When the bus address equals the address of the CSR, the address buffer module initiates a CSR cycle. Upon reception of start, the module sends a Clocked CSR Select to the data buffer module which controls the timing during CSR read and write cycles.

Starting address, box capacity, and the number of 16K × 32-bit array modules are present on the address buffer prior to receiving addresses on the main memory bus. The control A module computes the box capacity (MAX 4:0) and the number of 16K × 32-bit arrays (16K MAX 4:0), and sends them to the address buffer. The starting address (SA 8:0) comes either from the box controller or from the CSR. Refer to the flow diagram, Figure 6-2, which shows the flow of the box capacity, starting address, number of 16K × 32-bit arrays, and the bus address through the address buffer module.

Greater Than Starting Address? – To find if the bus address (RA 24:16) is greater than the starting address, a normalized address (NA) is computed. The 2's complement of the starting address (–SA) is divided by the number of ways externally interleaved, N. This is then added to the bus address divided by N. If the addition generates a carry-out, then the normalized address, RA – SA/N, is positive and the bus address is greater than the starting address. The carry-out generates the Above SA signal if SA ≠ 0.

If the starting address is 0, the bus address will always be greater than the starting address. Taking the 2's complement of 0 sets the carry-out to 1. The carry-out generates the signal SA = 0 which indicates that the bus address is above the starting address.

Less Than Highest Address? – To find if the bus address is less than the highest address of the box, the normalized address is compared to the capacity of the box. The 2's complement of the box capacity (–MAX) is added to the 2's complement of SA divided by N (–SA/N). When an address appears on the bus, it is divided by N and added to the above sum. This forms –SA/N – MAX + RA/N or NA – MAX. The carry-out generated when this sum is positive, OVER TOP, indicates that the address is beyond the range of this box.

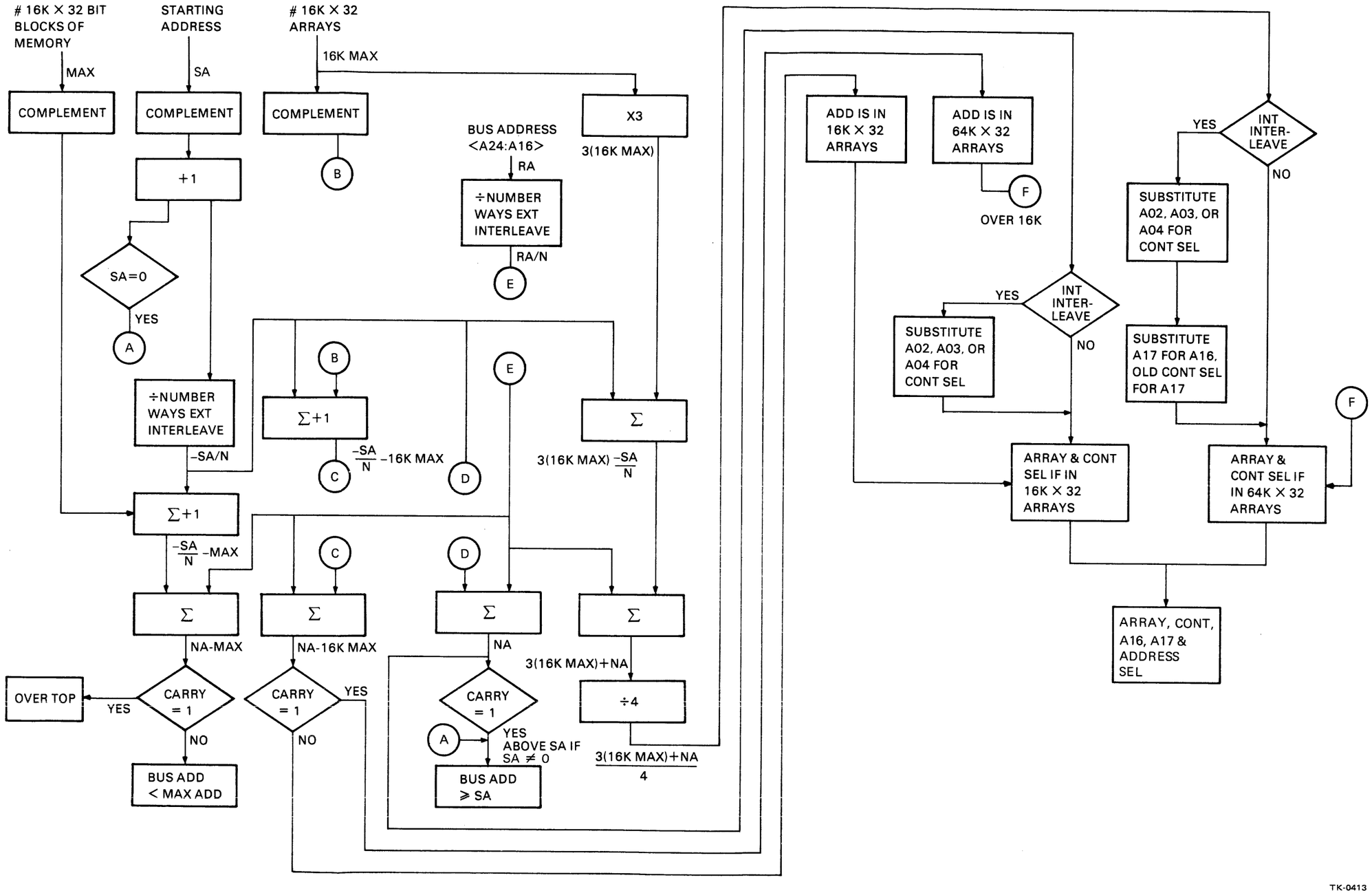
The normalized address, NA, since it is in terms of 16K × 32-bit blocks, can be used to select a controller and an array if each array contains one 16K × 32-bit block. If there is internal interleaving, bits are swapped to alternately select controllers. When the box contains 64K × 32-bit storage arrays, the address must be further modified since four 16K × 32-bit blocks reside on these arrays.

Is Address on a 64K × 32-Bit Array? – To find if the bus address is located on a 64K × 32-bit array, the normalized address is compared to the highest address located on a 16K × 32-bit array. In all boxes, the lower addresses associated with each controller are located on 16K × 32-bit arrays. The 64K × 32-bit arrays, if any, contain the higher addresses. The 2's complement of the number of 16K × 32-bit arrays (–16K MAX) is added to – SA/N (computed in the above example.) This sum is then added to the bus address divided by N (RA/N) to form –16K MAX – SA/N + RA/N or NA – 16K MAX. If NA is greater than 16K MAX, a carry-out is generated, called OVER 16K. The signal, OVER 16K, indicates that the address is not on a 16K × 32-bit array. When this is true, there no longer is a one-to-one correspondence between the array slot number and the 16K × 32-bit blocks of addresses. The array slot must then be found using the following expression:

$$\text{Array No.} = \frac{3(16\text{K MAX}) + \text{NA}}{4}$$

The hardware implements this function by first multiplying 16K MAX by 3 and adding it to –SA/N. This sum is then added to the bus address divided by N to form 3(16K MAX) – SA/N + RA/N or 3(16K MAX) + NA. The array number is then found by dividing the above by 4.

If there is no internal interleaving, the array number can then be used to select a controller and an array. With internal interleaving, bits are swapped to alternately select controllers.



TK-0413

Figure 6-2 Flow Diagram of Address Interface Module, Address Modification

Does Interleaving Place Address in This Box? – Each address buffer responds to every address, every other address, or every fourth address depending on the number of ways external interleaved. The module compares the interleaving number to the bus address low order bits A03 and A02 and signals Quad Select if the address is associated with the box. Since the bus address indicates which box will respond to the given address, these bits are substituted with higher order bits. Refer to the flowchart in Figure 6-3. As an example, if a controller responds to every other sequential address because of 2-way interleaving, address bit A16 is substituted for A02. This swapping maps contiguous address locations within the box to alternating addresses on the bus.

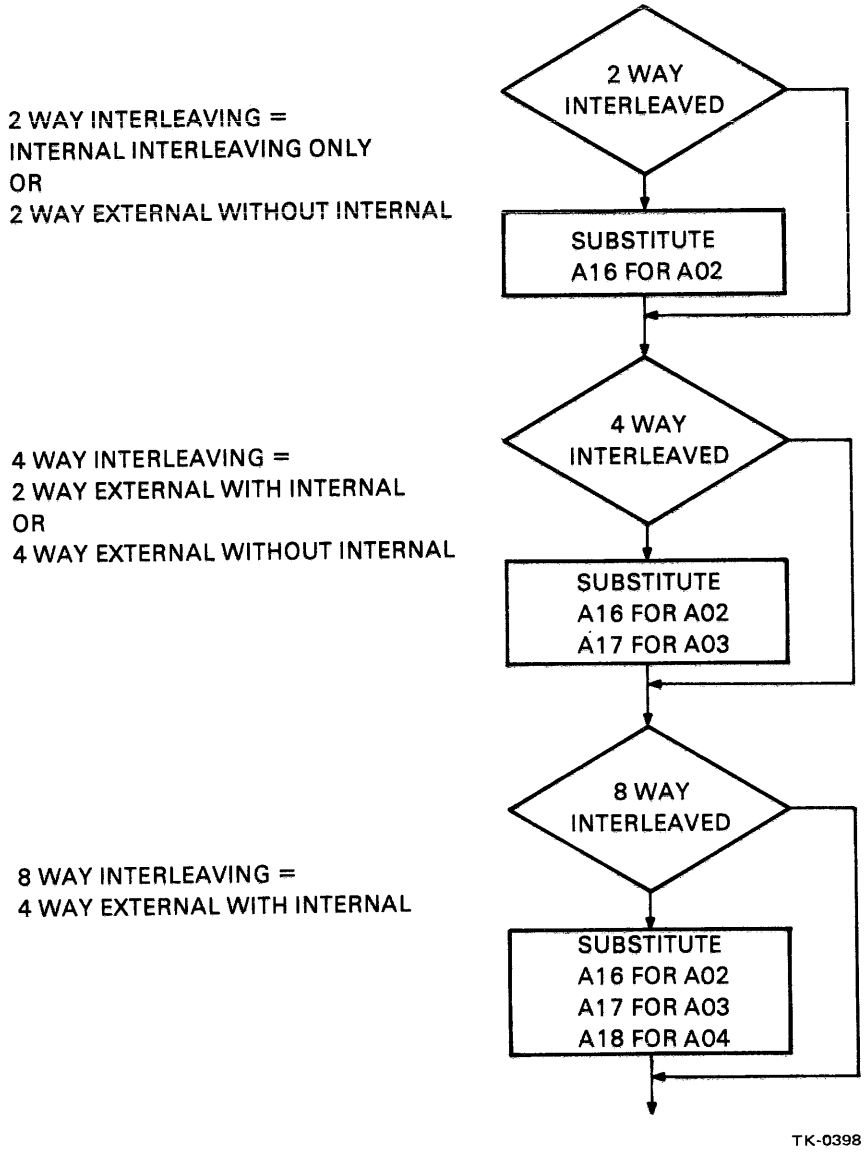


Figure 6-3 Flow Diagram of Address Interface Module, Address Low Order Bits

Figure 6-4 shows the logical steps used to determine whether or not the address buffer issues a GO signal, or a Clocked CSR Select in the case of CSR addresses, depending on the tests performed on the bus address.

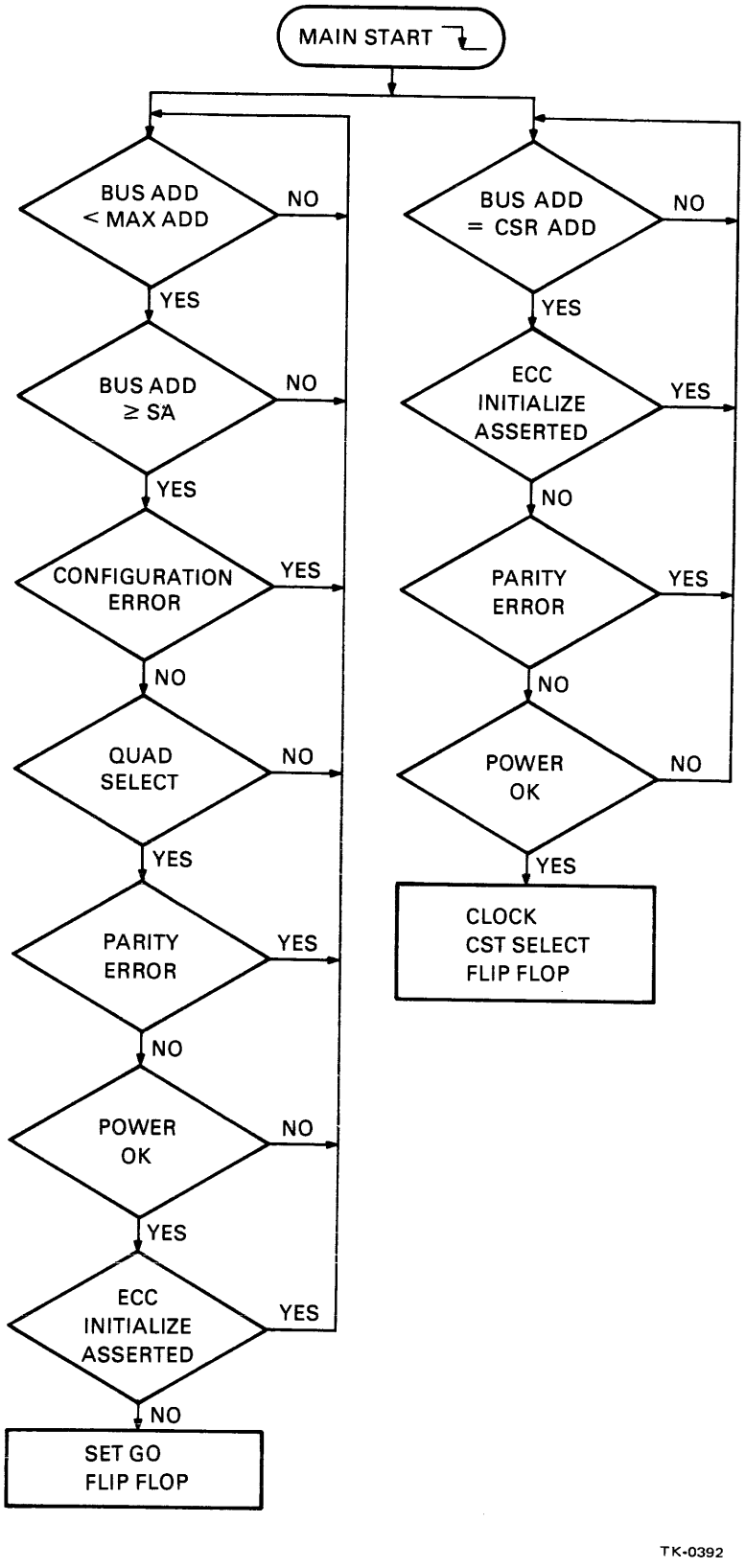


Figure 6-4 Flow Diagram of Address Interface Module GO and Clocked CSR Select Signals

6.3 DATA BUFFER MODULE (M8159)

6.3.1 Main Memory Bus Interface

The interface is bidirectional, switching the flow of data to and from the main memory bus. A 1-bit slice of the data paths is shown in Figure 6-1. The flowchart in Figure 6-5 illustrates the sequence of events during writes and reads to and from the memory and the CSR.

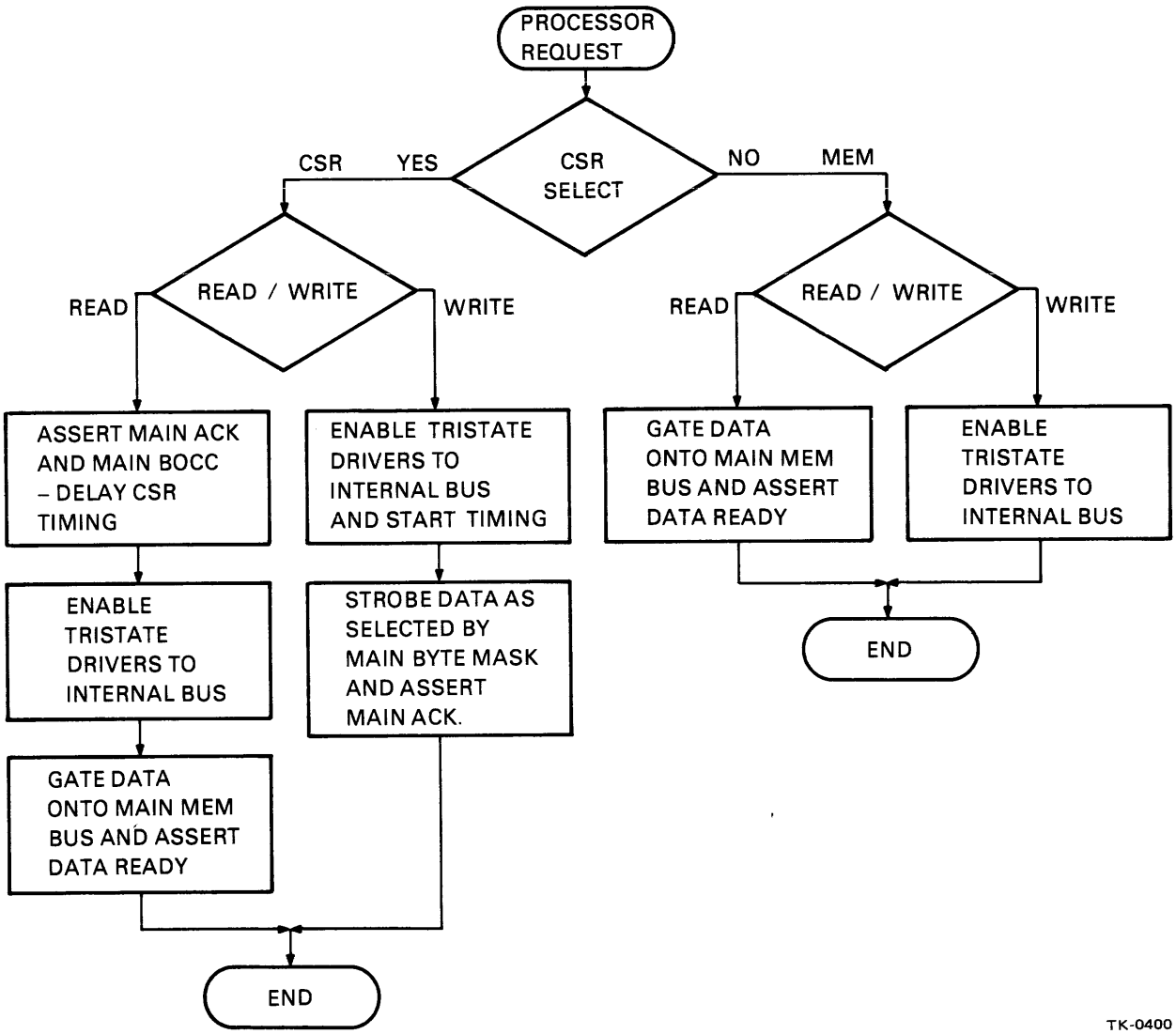


Figure 6-5 Flow Diagram of Data Buffer Board

Memory Access - Control bit C1, of the address and control word, selects a read or write operation (C1M = 0 = read, C1M = 1 = write). If the operation is a read from memory, the data on the internal bus is gated to the main memory bus. This path is enabled at Data Out Time Low by the controller when the data is valid on the internal bus. When the data buffer module receives a Data Ready signal from the controller, it asserts its Data Ready onto the main memory bus to inform cache that the data on the bus is valid. During reads, a Bus Occupied signal defeats the Main Data Select, disabling the normally enabled data path from the main memory bus to the internal bus. During write operations to memory, Main Data Select remains enabled and the data on the Main Memory Bus is channeled to the internal bus.

CSR Access - If the address buffer module sends a Clocked CSR Select signal to this module, the delay line timing chain begins its timing sequence. The timing chain on the data buffer module generates timing pulses only during reads and writes directed to the CSR. For a write operation, data from the main memory bus is loaded into the CSR registers by a Write Clock signal. The Write Clock signals are a function of the byte mask bits to allow writing selected bytes of the CSR double word. A write operation is disabled when a parity error is detected in the incoming CSR word (Write Parity Error Low.)

Data is read from the CSR through the internal bus. The outputs of the CSR registers are placed onto the internal bus by a CSR Select signal. The timing chain on the data buffer module disables Main Data Select and signals Data Out Time. At Data Out Time, the CSR data on the internal bus is gated through to the main memory bus. Note that when the box capacity is read, the box capacity comes from the control A module rather than the CSR registers. The read box capacity command (INT 0–1 = L, CSR 0–2 = L, CSR 0–3 = H) disables the CSR outputs CSR 1–0 through 1–6 via the enable signal CSR Data Select. In CSR read operations, other than a read box capacity, CSR Data Select is equivalent to CSR Select.

6.3.2 Control and Status Register

The CSR stores operating mode commands and error information. Through the CSR, the program can control the operation of the memory and read error messages for maintenance purposes. Figure 6-6 shows the CSR formatted as two 16-bit words. Switches on the address buffer module select the address of the CSR.

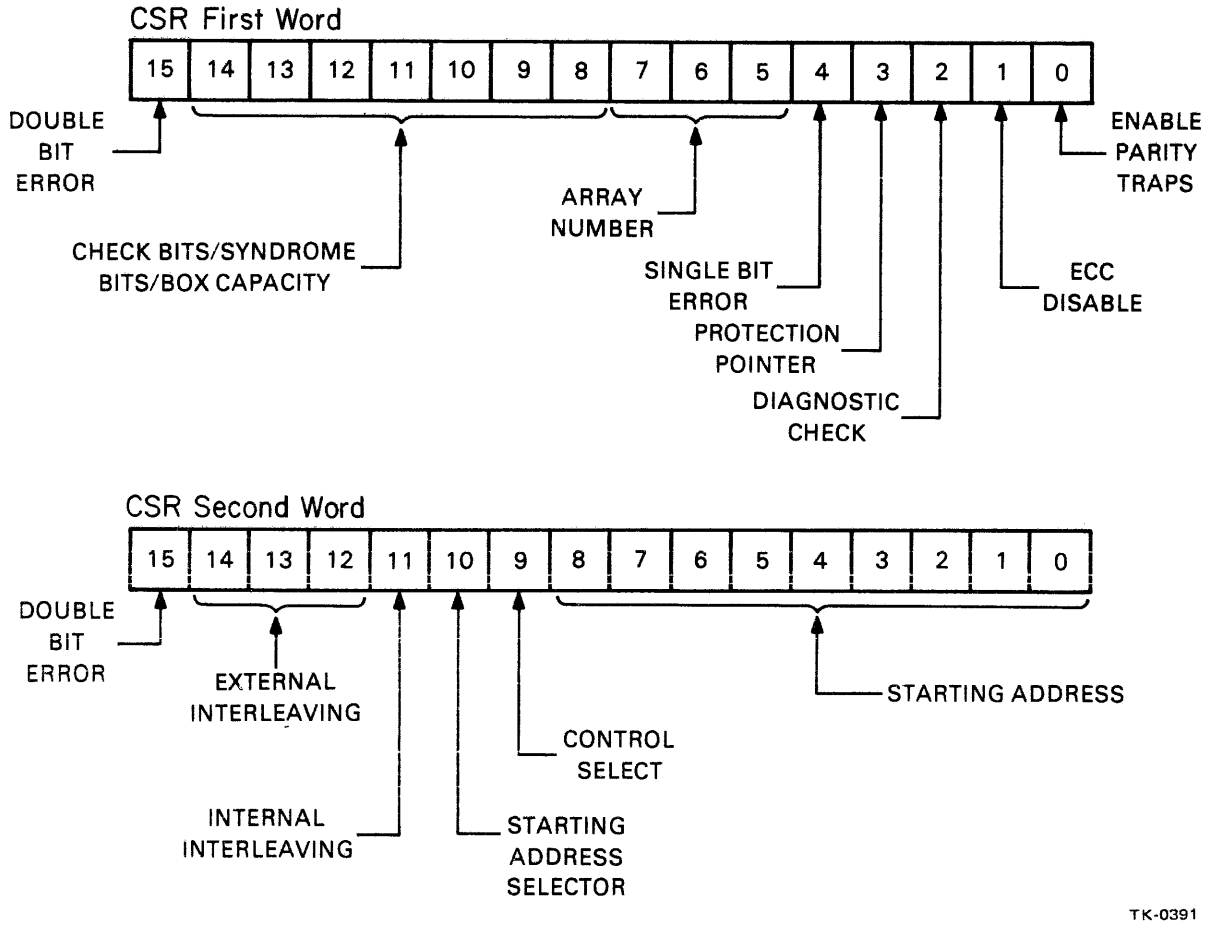


Figure 6-6 Control and Status Register Format

6.3.3 Control and Status Bit Allocation

First Word

Bit 0 Enable Parity Traps	When set to 1, allows assertion of bad parity onto main memory bus if errors are detected during a read. With ECC enabled, asserts bad parity on double-bit errors. With ECC disabled, asserts bad parity on double-and single-bit errors. Bit is set to 1 on power-up and can be written and read.
Bit 1 ECC Disabled	When set to 1, disables single-bit error correction. Does not disable error detection or logging of errors in CSR. Bit is cleared to 0 on power-up and can be written and read.
Bit 2 Diagnostic Check	When set to 1, allows transfer of data between the CSR and the ECC check bits of the addressed double word. During a write, CSR bits (14:8) are loaded into the check bits. During a read, check bits are loaded into CSR bits (14:8). Bit is cleared to 0 on power-up and can be written and read.
Bit 3 Protection Pointer	Selects a protected 16K × 32-bit section of memory that will not be affected by CSR bits 1 and 2. When cleared to 0, selects the first 16K section associated with each controller. When set to 1, selects the second 16K section associated with each controller. Bit is cleared to 0 on power-up and can be written and read.
Bit 4 Single Bit Error Indication	When 1, indicates detection of a single bit error during a read. Storage array number, controller number, and syndrome bits are loaded into CSR on single-bit errors. Bit is cleared to 0 on power-up and can be written and read.
Bits 7:5 Array Select	Stores array select number on detection of single-bit or double-bit errors during a read. Array numbers of protected memory space are not stored on single-bit errors. Bits are cleared to 0 on power-up and can be read only.
Bits 14:8 Check Bit/Syndrome Bit/Box Capacity	Check Bit Storage – When diagnostic check, bit 2 equals 1, stores check bits read from memory or bits to be written into the check bit field of the addressed memory location. Syndrome Bit Storage – Stores the syndrome bits, indicating which bit failed, on detection of a single-bit error during a read. Box Capacity – When CSR bits (3:1) equal 100, stores the box capacity in sections of 16K × 32-bit blocks. To read box capacity, load 100 into CSR bits (3:1) with a write prior to the read. Bits may be in any state at power-up and can be written and read.

Bit 15 Double Error Indication	When 1, indicates detection of a double-bit error during a read. Storage array number and controller number are latched into CSR on double-bit errors. Bit is cleared to 0 on power-up and can be written and read.
Second Word	
Bits 8:0 Starting Address	Stores Starting Address in 16K × 32-bit blocks. The source of the starting address can either be the program or the box controller. When starting address selector (bit 10 second word) equals 0, source is the switches of the box controller (or switches on data buffer module). When starting address selector (bit 10, second word) equals 1, source is the starting address written into CSR. Bits are loaded with starting address from box controller on power-up and can be read at any time but written only when starting address selector is 1.
Bit 9 Control Select	Stores the control select number on detection of single-bit or double-bit errors. Bit is cleared to 0 on power-up and can be read only.
Bit 10 Starting Address Selector	When cleared to 0, the source of the starting address and external interleaving is the box controller (or switches on the data buffer module). When set to 1, the source of the starting address and external interleaving is the program via a write to CSR bits <14:12> and <8:0> second word. Bit is cleared on power-up and can be read at any time but only written when the Panel Address Override switch is in the Allow Program Control position.
Bit 11 Internal Interleaving	When 0, indicates no internal interleaving; when 1, indicates internal interleaving. Bit is set to 1 on power-up if each controller has identical memory capacity. Bit can be read at any time but can only be written if each controller has identical memory capacity.
Bits 14:12 External Interleaving	Stores the number of ways externally interleaved. The source of the interleaving can either be the program or the box controller. When starting address selector (bit 10 second word) equals 0, source is the box controller (or switches on data buffer module). When starting address selector (bit 10 second word) equals 1, source is the number of ways externally interleaved written into CSR. Bits are loaded with the interleaving selected on the box controller on power up and can be read at any time but written only when starting address selector is 1. Bit values and the corresponding number of ways externally interleaved are listed below.

CSR Bits

14	13	12	Number of ways externally interleaved
x	0	0	No external interleaving
0	0	1	First of 2-way, selected if A02 = 0
1	0	1	Second of 2-way, selected if A02 = 1
0	1	0	First of 4-way, selected if A03 = 0, A02 = 0
1	1	0	Second of 4-way, selected if A03 = 0, A02 = 1
0	1	1	Third of 4-way, selected if A03 = 1, A02 = 0
1	1	1	Fourth of 4-way, selected if A03 = 1, A02 = 1

Bit 15
Double Error Indication

When 1, indicates detection of a double-bit error during read. Bit is set to 1 simultaneously with bit 15 first word. Clearing bit 15 in one word has no effect on bit 15 of the other word.

Bit is cleared to 0 on power-up and can be written and read.

6.3.4 CSR Addressing

There are two methods of addressing the CSR: direct and indirect. A switch on the address buffer selects the method of addressing. Direct addressing is implemented only with modified PDP-11/70 processors. Indirect addressing requires no modification of the processor.

Direct Addressing – On a modified processor, switches on the address buffer module select one of the following CSR addresses. A unique address is selected for each memory box. (Switch 1–8 on M8158 is off.)

	Switch				Switch		
Address	**1–1**	**1–2**	**1–3**	**Address**	**1–1**	**1–2**	**1–3**
177772100	On	On	On	177772120	On	On	Off
177772104	Off	On	On	177772124	Off	On	Off
177772110	On	Off	On	177772130	On	Off	Off
177772114	Off	Off	On	177772134	Off	Off	Off

Indirect Addressing – Switches on the address buffer module select one of the following addresses. Normally these addresses are part of reserved address space and are not directly accessible by the processor. These CSR locations may be accessed for diagnostic purposes through the Unibus map with cache turned off. It is not recommended to use this method in an operating system environment since the Unibus map is required for other non-processor request activities. (Switch 1–8 on M8158 is on.)

	Switches				Switches		
Address	**1–1**	**1–2**	**1–3**	**Address**	**1–1**	**1–2**	**1–3**
17772100	On	On	On	17772120	On	On	Off
17772104	Off	On	On	17772124	Off	On	Off
17772110	On	Off	On	17772130	On	Off	Off
17772114	Off	Off	On	17772134	Off	Off	Off

The CSR may then be accessed in the following manner:

1. Halt all NPR activity in the system
2. Turn cache off
3. PAR 6 ← 177400 (other PARs normal)
4. Enable memory management in 22-Bit mode
5. Map 36 ← 17760000 (other maps are 0)
6. Turn on Unibus map
7. Access virtual addresses 152100 through 152136 as CSR addresses.

CHAPTER 7
POWER SUPPLY AND DISTRIBUTION

7.1 GENERAL DESCRIPTION

Each memory contains its own power supply system. The power supply converts 115 Vac or 230 Vac line voltage into the various dc voltages required to operate the memory. Input ac power is obtained from an 861-D, E power controller which supplies one phase of its 3-phase input power to the memory.

The power supply consists of an ac input box (7014420-1, 2), a transformer assembly (7011486), a +5 V regulator (H7441), three ±12 V and +5 V regulators (7014251), and three battery backup units (H775-D). A chassis, mounted at the back of the memory box, houses the ac input box, transformer assembly, the four voltage regulators, and two cooling fans. The three battery backup units and their battery packs are each housed in their own boxes, separate from the other power supply assemblies. Figure 7-1 identifies the major assemblies of the memory's power supply.

7.2 POWER SUPPLY CABLES

7.2.1 External Power Cables

The external power cables interconnect the memory box, the box controller, and battery backup units within the memory cabinet. Figure 7-2 is a simplified block diagram of these cables. For the actual cable routing, see Chapter 8.

Box Controller Power Cable (7014311) – This cable harness connects the ON/OFF power switch on the box controller to the memory's power supply for controlling power to the memory. This harness also carries signals to the battery status indicators which show the operating mode of the three battery backup units.

Battery Backup Power Cable (7014520-08) – These three cables connect the battery backup units to their regulators. Power to charge the batteries or power from the batteries to run the memory is carried by these cables, along with Control and Battery Status signals.

7.2.2 Internal Power Harnesses

The internal power harnesses connect the power supply assemblies to the memory backplane. These harnesses are shown in Figure 7-3.

Power Distribution Harness (7014228) – This harness carries low-voltage ac power to the four regulator modules and connects the regulated output voltages to the backplane. Power Fail and Boot Enable signals from the backplane are also sent by the 7014251 regulators via this harness.

Power Monitor Harness (7010581) – This harness carries the Power Fail signals to the memory backplane from the ac input box.

Box Controller Harness (7014312) – This harness connects the box controller power cable (7014311) to the power supply. It carries the Power On signal to the ac input box, and Power On and Battery Status signals between the three 7014251 regulators and P31.

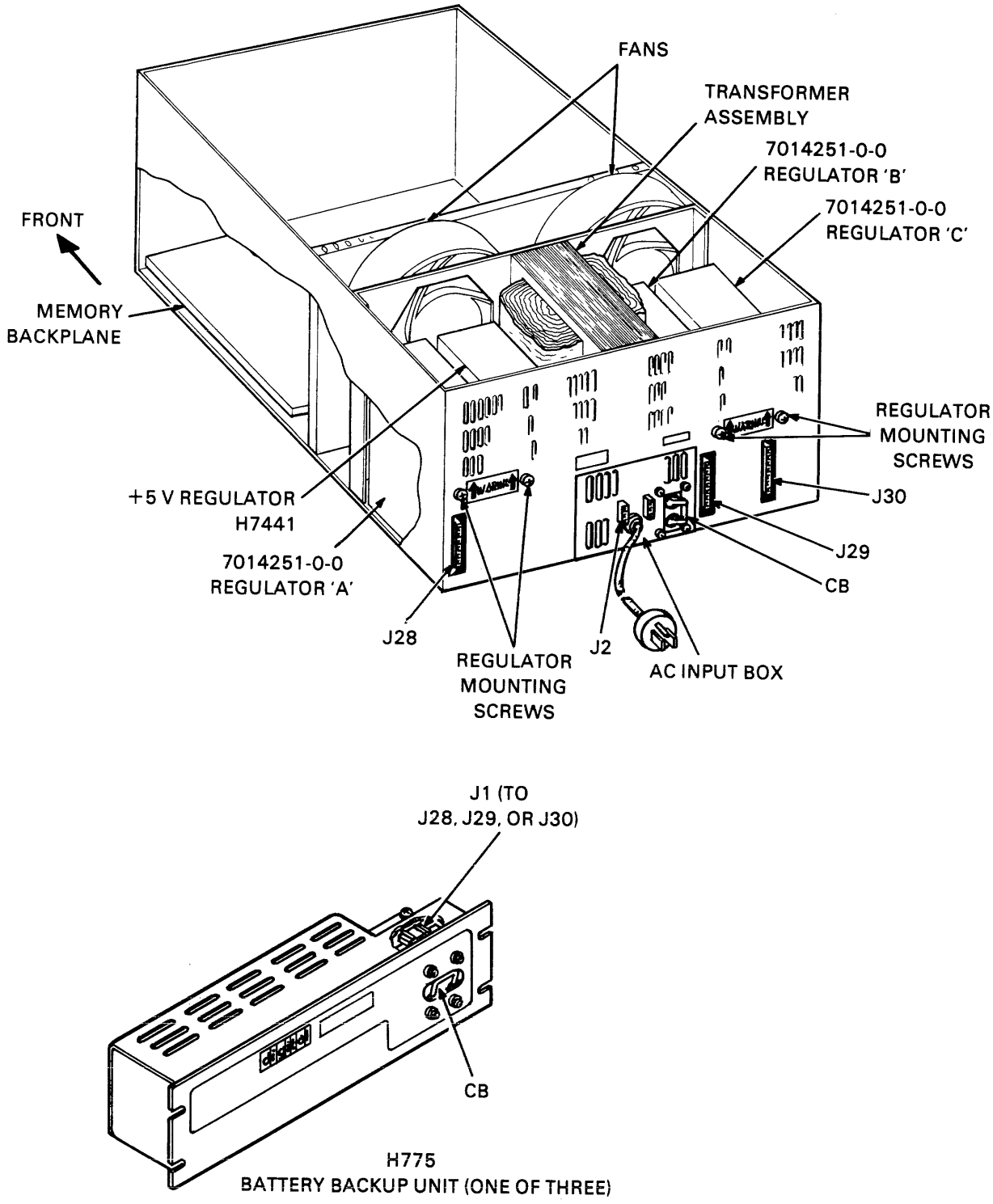


Figure 7-1 Power Supply Major Assemblies

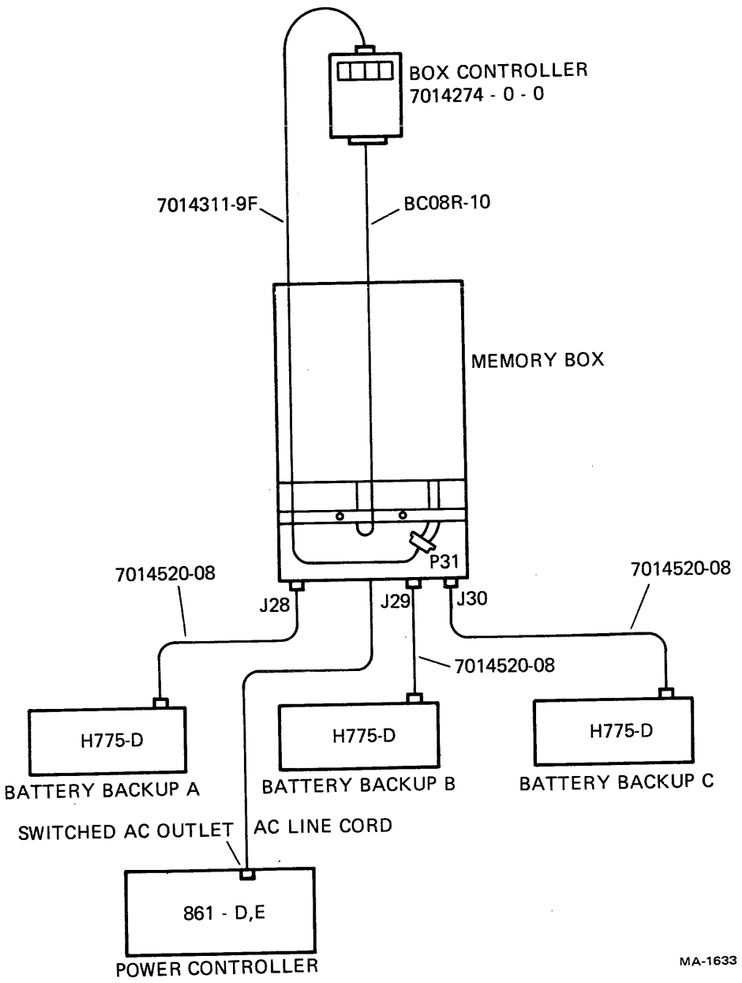


Figure 7-2 Power Supply External Cabling

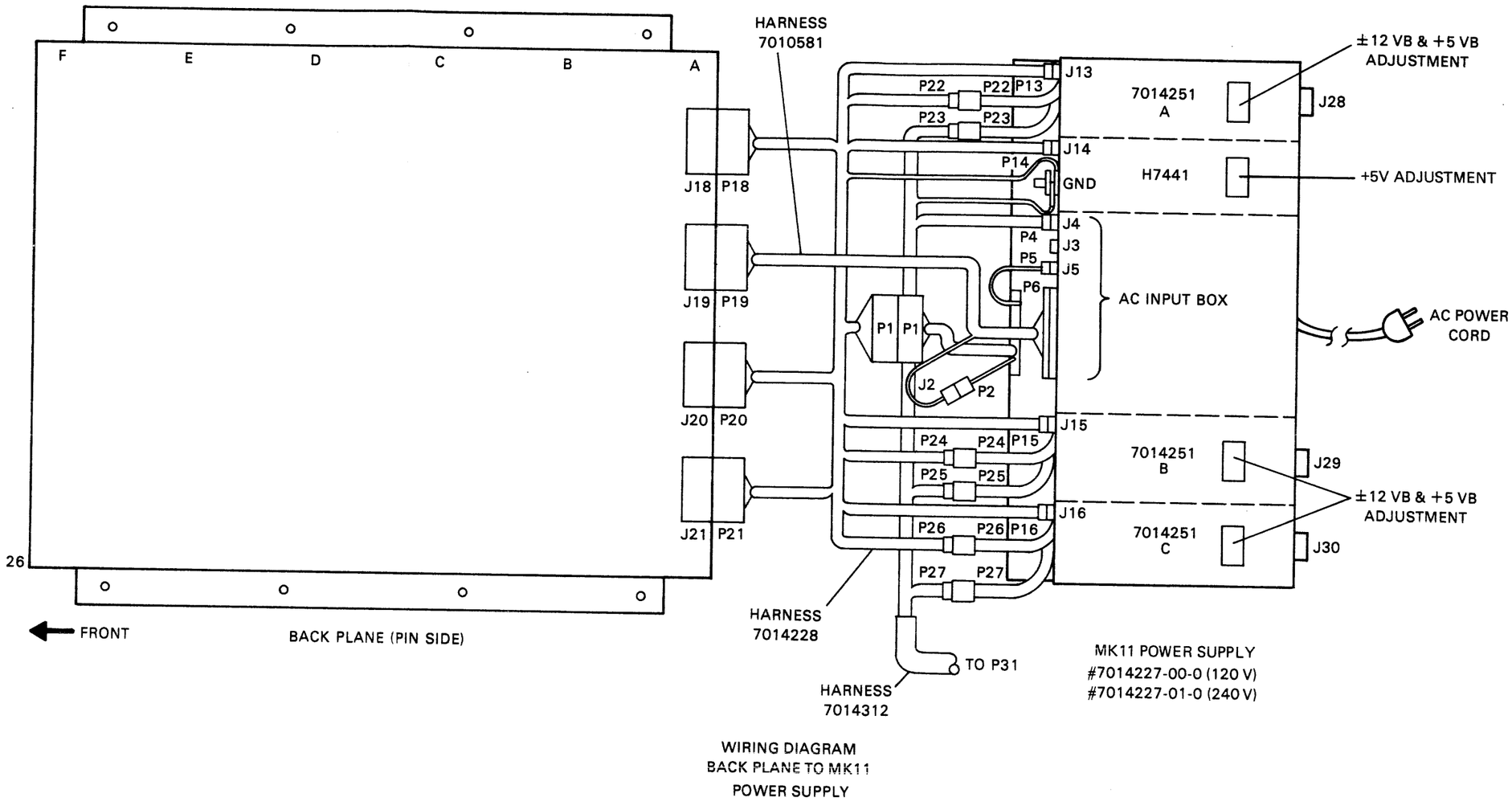


Figure 7-3 Power Supply Internal Cabling

7.3 POWER SUPPLY MAJOR ASSEMBLIES

7.3.1 Power Controller (861-D, E)

The power controller supplies primary ac input power to the memories located in the memory cabinet. The 861-D, E mounts in the bottom of the memory cabinet. Its input is 3-phase line power; the 861-D is used with 3-phase 115 Vac, and the 861-E is used with 3-phase 230 Vac power. Memory boxes in the memory cabinet plug into the switched outlets of the power controller. These switched outlets are controlled by a remote power cable which connects the power controller with the processor. In this system, the 861's LOCAL/REMOTE switch is in the LOCAL position, disabling the power request function. A ground on the emergency shutdown line, in either the LOCAL or REMOTE position, deenergizes the switched ac outlets. The remote power control cable contains three conductors:

- Pin 1, Power Request – Active Low
- Pin 2, Emergency Shutdown – Active Low
- Pin 3, Ground Return.

7.3.2 AC Input Box (7009811-1, 2)

The ac input box is mounted in the center of the power supply chassis with three Phillips-head screws. A portion of the rear of the power supply chassis is cut out, making the ac input box visible from the back of the memory. The ac power cord and a circuit breaker extend through the cutout. The primary function of the ac input box is to switch power to the transformer's primary windings. This assembly consists of a circuit breaker, a power control relay, an ac power control board (5410993), and a power line monitor board (5411086-YA).

The ac power control board operates the power relay which switches primary ac power to the transformer assembly. This allows remote power control for the power supply from the box controller power switch.

The power line monitor board receives a low-voltage ac output from the transformer assembly. Sensing circuits monitor the ac voltage and generate the AC Low and DC Low signals for the memory if power is lost. Two LEDs indicate the generation of the Power Fail signals by turning off and flagging the memory which is the source of the AC Low and DC Low signals. Under normal conditions (AC Low and DC Low not asserted) these LEDs are lit.

7.3.3 Transformer Assembly (7011486)

The transformer assembly is located in the center of the power supply chassis. Two capacitors, two varistors, and two terminal boards are mounted directly on the transformer. Single-phase 115 Vac or 230 Vac is stepped down by the transformer to approximately 30 Vac. There are five separate secondary windings, one for each regulator module and one for the power line monitor board. The cooling fans receive 115 Vac from the primary windings. The two capacitors filter the input line voltage and the varistors suppress voltage spikes which occur on the ac input voltage.

7.3.4 +5 Vdc Regulator (H7441)

The H7441 module mounts in the power supply chassis to the right of the transformer assembly (as viewed from the front). It is secured in the chassis by three Phillips-head screws. The input to the regulator is 30 Vac from one of the transformers secondary windings; its output is a regulated +5 Vdc at up to 32 A.

The H7441 is a switching regulator and provides both over-current and over-voltage protection. An over-current sensing circuit protects the regulator from shorted loads. The current overload is a fold-back type; the output voltage is decreased by limiting the duty cycle of the switching regulator in order to decrease the output current. Over-voltage protection is provided by an over-voltage crowbar circuit which shunts the output current to ground through an SCR when the output voltage exceeds 6 V.

A LED, visible from the bottom of the regulator (near the voltage adjustment potentiometer), lights whenever +5 V is present at the output of the regulator.

7.3.5 ±12 VB and +5 VB Battery Backup Regulators (7014251) and Battery Backup Units (H775D)

The three 7014251 modules mount in the power supply chassis in the locations shown in Figure 7-1. Each regulator is secured in the chassis by three Phillips-head screws. The regulators are cabled to their battery backup units through cutouts at the rear of the power supply chassis. The battery backup units are housed in their own enclosures which mount in the memory cabinet. Figure 7-4 is a block diagram of one of the regulator/backup unit pairs.

The ±12 VB and +5 VB regulator consists of a regulator board (5413075), an input rectifier board (5412411), and a controller board (5413073). The rectifier board rectifies the low voltage output from the transformer's secondary windings, supplying the raw dc voltage to the rectifier. Raw dc from the rectifier also goes to the battery backup unit to supply the charging current for the batteries. In the regulator, the raw dc is modulated by a switching circuit. Energy in the switched dc waveform is transformer coupled to rectifiers which produce the +12, -12, and +5 V outputs. Regulation is accomplished by changing the duty cycls of the switched raw dc to keep +5 VB at 5 V. The regulator is over-current protected by a foldback current limiter and over-voltage protected by a crowbar circuit. The controller monitors the Power Fail and Charge Mode signals to control the operation of the batteries and indicate the battery status with the lights in the box controller. Operation of the regulator is enabled by the power switch on the box controller via the DC ON signal. A normally closed thermal switch in the DC ON path, opens and shuts off the regulator if an over-temperature condition exists.

The battery backup unit contains a battery charger printed circuit board (5411625) and two 12 V batteries (1212499). The battery charger consists of a regulator which supplies the charging current, charge status circuitry, and a relay which connects the batteries to the charger. When the memory is powered up, the controller in the 7014251 regulator connects the batteries to the charging regulator through the relay. The regulator supplies the charging current from the raw dc input, supplying a full charging current until the battery voltage reaches approximately 22 V. After this level is reached, the regulator supplies a trickle charge to maintain the charge on the batteries. The rate of charging is sensed by the charge status indicator circuitry which sends the Charge Mode signals to the 7014251 regulator.

Loss of ac input power causes the loss of the rectified raw dc from the 7014251 regulator. When this happens, the batteries supply the dc voltage to the regulator in the 7014251 instead of the rectifier board. The regulator continues to produce +12, -12, and +5 V until the batteries discharge past 18 V. An 18 V reference is used by the relay to disconnect the batteries from the regulator to prevent the batteries from discharging completely.

7.4 POWER DISTRIBUTION

The block diagram, Figure 7-5, shows the interconnection of all the power supply assemblies identified in the previous sections. Distribution of the power can be traced from the ac line input to the memory backplane with this diagram; specific pin numbers and color coding of wires are found in the *Field Maintenance Print Set.* Locations of the regulated inputs to the backplane are called out in Figure 7-6 which shows the backplane as viewed from the bottom (wire-wrap pin side).

Single-phase ac line voltage is present at the ac input box from the 861-D, E power controller. Turning the power switch on the box controller activates the power relay through the ac power control board. The power relay switches 115 Vac or 230 Vac to the primary windings of the transformer and to the two cooling fans. From the transformer secondary windings, the stepped-down 30 Vac is routed to the four regulator modules via harness 7014228. The power switch on the box controller also switches on the three 7014251 regulators and the battery backup units.

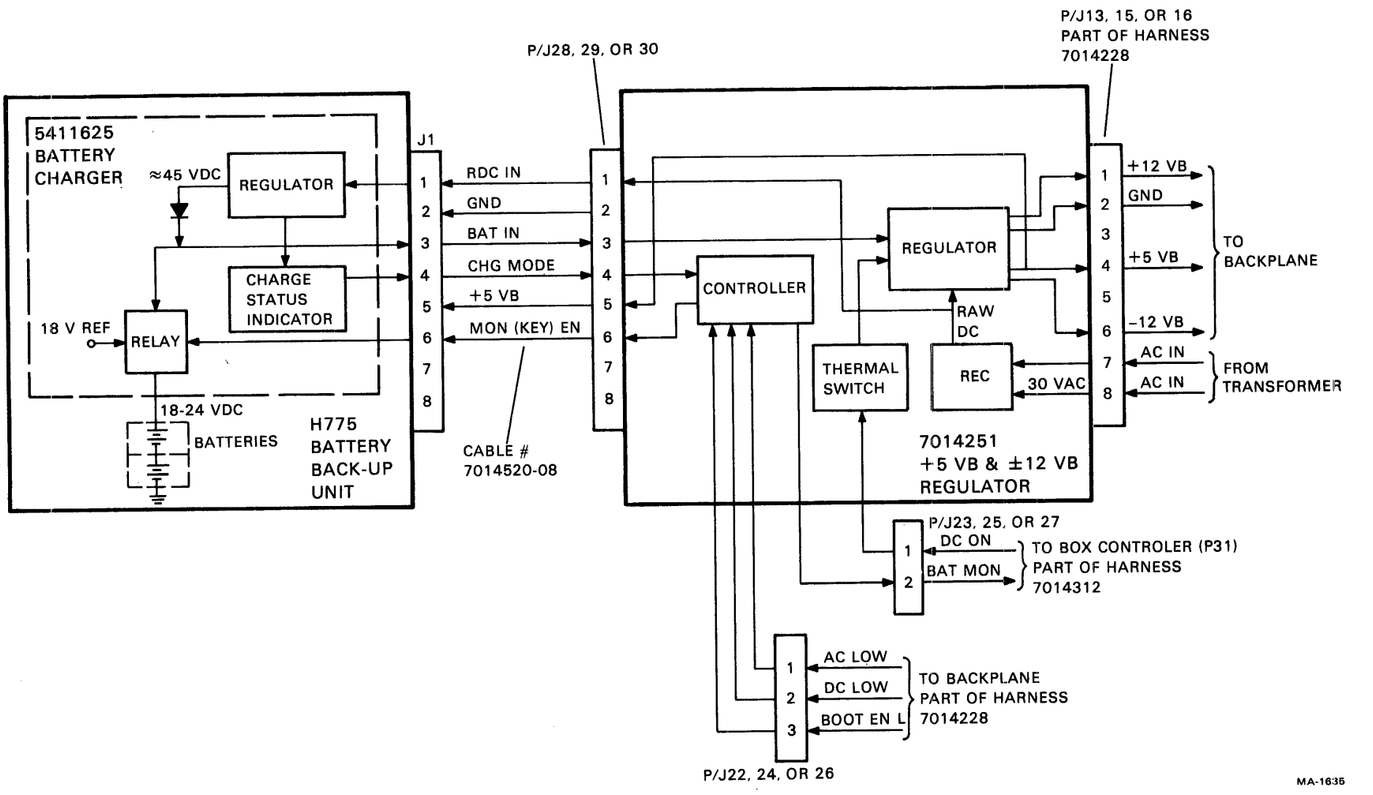


Figure 7-4 Battery Backup Regulator Block Diagram

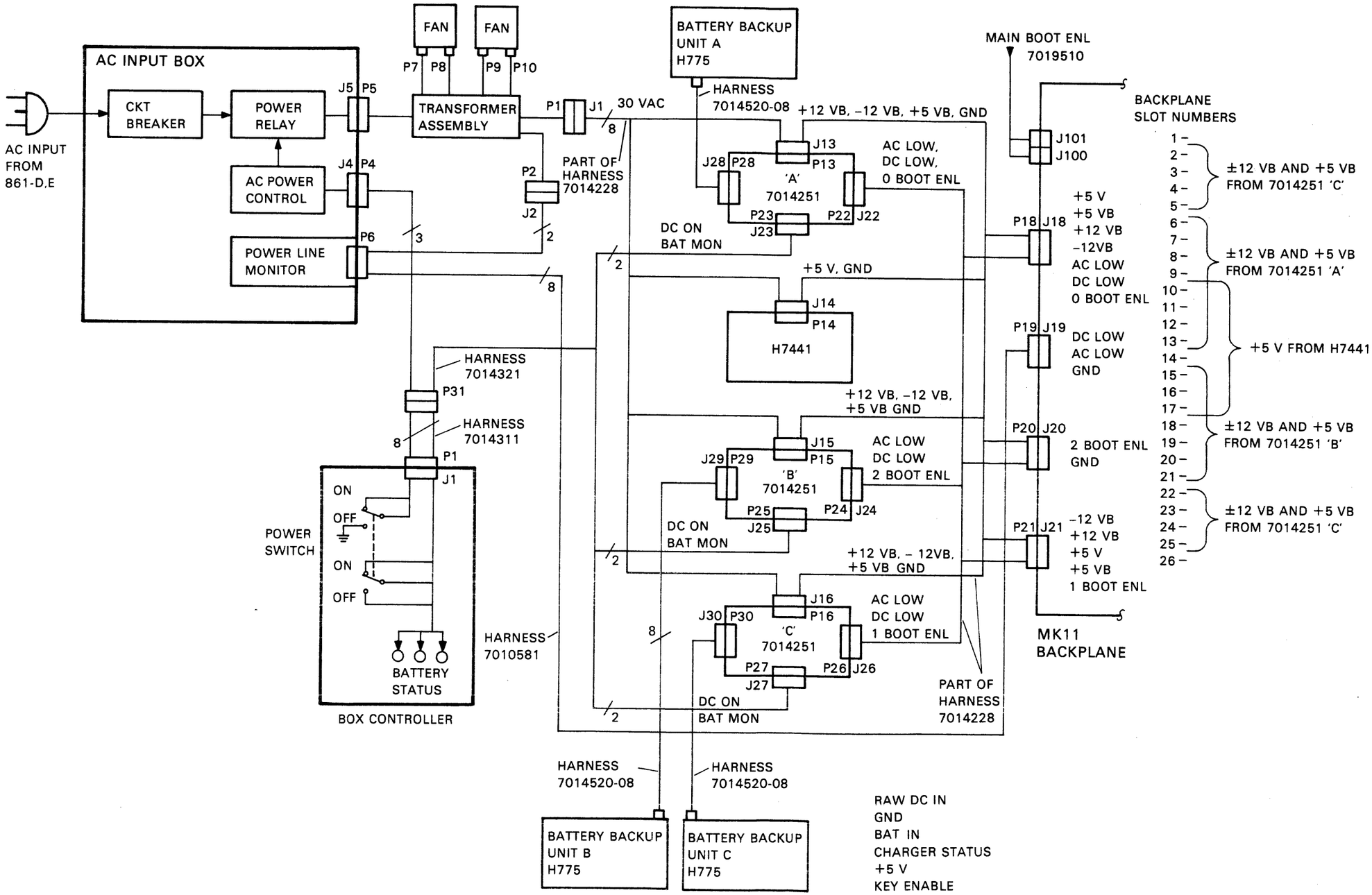


Figure 7-5 Power Distribution and Control

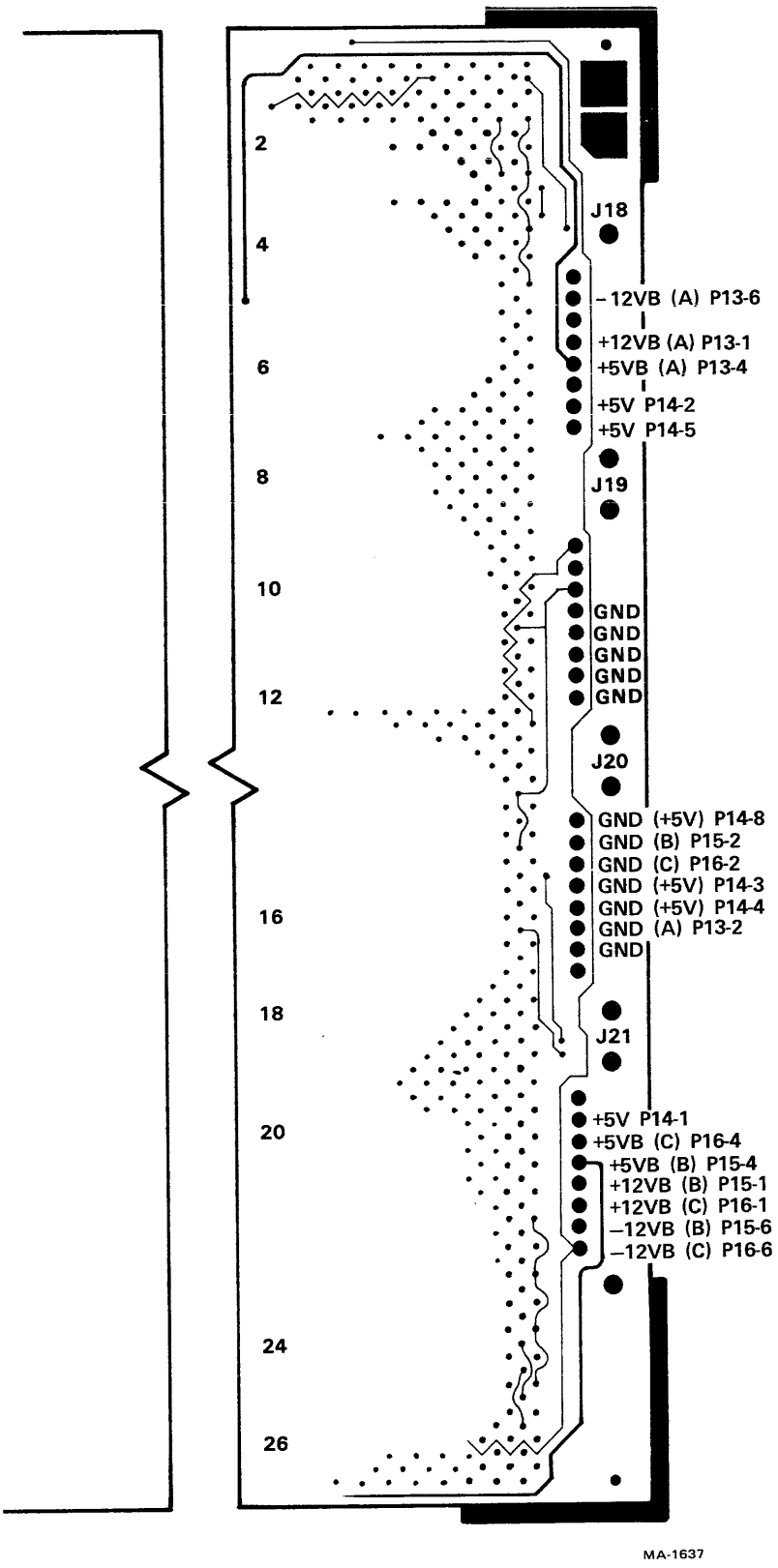


Figure 7-6 Backplane Power Connections

The four regulator modules rectify and regulate 30 Vac from one of the transformer's secondary windings. The H7441 +5 V regulated output is carried by harness 7014228 from J14 on the regulator module to backplane connectors J18 and J21 (ground return to J20). From these connectors, the +5 V is routed to all the backplane slots. The +5 V powers all the devices on the address buffer, data buffer, and the four control modules not flagged with asterisks in the schematic diagrams. An LED, on the bottom of the regulator near the adjustment potentiometer, illuminates while the H7441 is producing +5 V.

Three more secondary windings supply 30 Vac to the three 7014251 modules via harness 7014228. Regulator A produces +12, -12, and +5 Vdc (±12 VB, +5 VB) which are carried through harness 7014228 (J13) to the memory backplane connector J18 (ground returns to J20). From J18, regulator A's voltages go the backplane slots 6 through 13. Regulator A provides power to all the devices indicated with asterisks on the address interface module, the control 0 pair of control A and B modules, and to the array modules in backplane slots 6, 7, 8, and 9.

Regulator B produces +12, -12, and +5 Vdc which enter the memory backplane via harness 7014228 to connector J21 (ground returns to J20.) Regulator B powers backplane slots 14 through 21 which contain the data buffer module, the control 1 pair of control A and B modules, and the arrays in slots 18, 19, 20, and 21. Only the devices indicated with asterisks on the schematic diagrams are powered by regulator B.

Regulator C sends its ±12 VB and +5 VB voltages to the backplane via harness 7014228 to connector J21 (ground returns to J20.) Its regulated outputs power the array modules in backplane slots 2 through 5 and 22 through 25. Figure 7-6 locates the backplane connector pins which carry the regulated voltages and the source connectors and pin numbers.

A fifth secondary winding on the transformer supplies low voltage ac to the power line monitor located in the ac input box. When power is switched on, the power line monitor switches the DC Low signal to a high level and then the AC Low signal to a high level. Harness 7010581 carries these DC Low and AC Low signals to the memory backplane connector J19. The memory monitors the Power Fail signals from its own power line monitor and Power Fail signals from the main memory bus. From the backplane, DC Low and AC Low signals go to the 7014251 regulators (J22, J24, and J26) via harness 7014228. These same cables carry the Boot Enable signals to the 7014251 regulators. The source of the Boot Enable signal is cable 7019510 which plugs into connectors J100 and J101 on memory box number 0. Other memories in the system obtain the Boot Enable signal from the main memory bus.

Raw dc voltage, rectified from the 30 Vac, is sent to the battery backup units by the 7014251 regulators via harness 7014520-08. This voltage powers the battery charger and supplies the charging current for the battery pack. The regulated output, +5 VB, also goes to the battery charger. The battery backup units send charger status information to the regulators which send coded status signals to the box controller via harness 7014312 (P31). These battery monitor signals operate the battery status indicator LEDs in the box controller. The coding is as follows.

- OFF - Battery off
- SLOW FLASH - Battery receiving full charge
- FAST FLASH - Battery supplying power to memory
- ON - Battery receiving trickle charge

In the event of a power failure, the batteries in the backup units supply current to the 7014251 regulators which continue to produce their regulated output voltages for a minimum of 5 minutes. Power is then supplied only to the array modules and the devices flagged with asterisks on the schematic diagrams of the address interface, data buffer, and control A and B modules. Battery power is used by the memory for refresh cycles only; no other memory cycles are allowed to run.

7.5 VOLTAGE MEASUREMENTS AND ADJUSTMENTS

Turn on power and measure the +12 VB, -12 VB, +5 VB, and +5 V voltages at J18 and J21 of the memory backplane with a DVM (Figure 7-6). All voltages must be within ±5 percent tolerance. If a voltage is found to be out of tolerance, perform the required voltage adjustment.

7.5.1 H7441 Voltage Regulator Adjustment, +5 V

1. Using a digital voltmeter, measure the voltage at J18 pin 1 or J21 pin 7 under normal load conditions.

2. Adjust the voltage to +5 V. See Figure 7-7 for location of adjustment potentiometer.

If the voltage cannot be adjusted to +5 V, check for faulty regulator or harness.

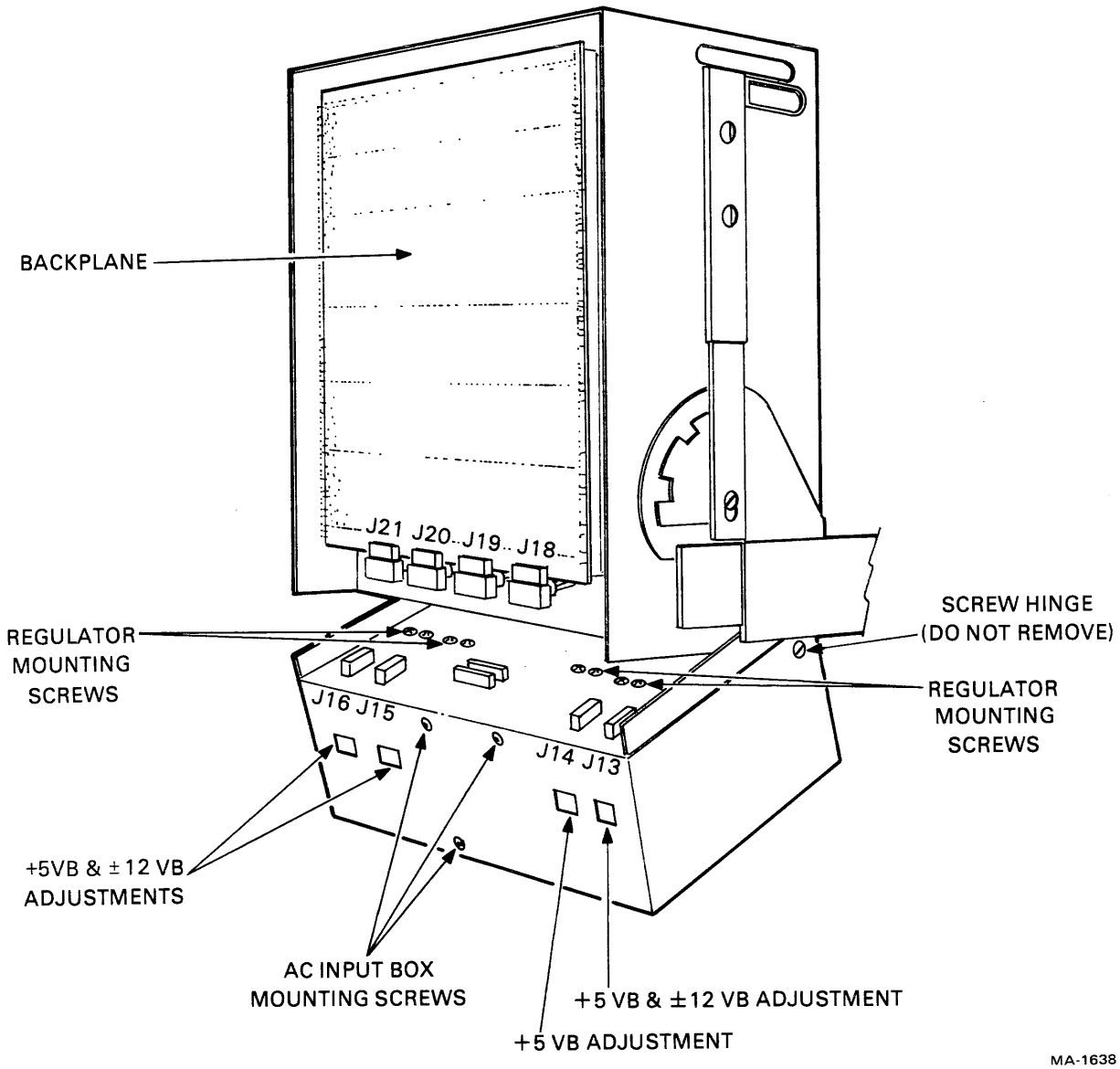


Figure 7-7 Power Supply in Maintenance Position

7.5.2 7014251 Voltage Regulator Adjustment, ±12 VB and +5 VB

1. Using a digital voltmeter, measure the voltage of +5 VB (A) at the backplane under normal load conditions. Figure 7-6 shows the backplane pin connections.

2. Adjust the voltage to +5 V. See Figure 7-7 for the location of the adjustment potentiometer.

3. Measure the voltage of +12 VB (A) and -12 VB (A).

4. Repeat steps 1-3 for the +5 VB (B), ±12 VB (B) and +5 VB (C), ±12 VB (C) voltages.

If the +5 VB voltages cannot be adjusted to +5 V or if the ±12 VB voltages are out of tolerance, check for faulty regulators or harness.

7.6 POWER SUPPLY SUBASSEMBLY REMOVAL PROCEDURE

The power supply access procedure enables the supply to be accessed for adjustments and subassembly removal. The removal procedures include:

1. Power supply access procedure
2. H7441 and 7014251 regulator removal
3. AC power input box and 5411086-YA power line monitor board removal
4. Fan removal
5. Transformer assembly removal.

7.6.1 Power Supply Access Procedure (Figure 7-7)

1. Remove ac power by disconnecting the ac line cord from the ac power source.

2. Fully extend the memory frame from the rack, ensuring that cables do not bind.

3. Remove the memory frame's top cover by removing six screws.

4. Remove the cable clamps by removing four screws.

5. To remove the top cover of the power supply, loosen the top three screws and remove the back four screws.

7.6.2 H7441 and 7014251 Regulator Replacement (Removal and Installation)

1. Perform the power supply access procedure (Paragraph 7.6.1).

CAUTION

Do not remove the power supply hinge screws when performing the next step (Figure 7-7).

2. Remove the two power system screws on each side of the power supply.

3. Carefully rotate the memory frame 90 degrees and tilt the power supply.

4. Remove the bottom cover of the memory frame.

WARNING

Power must be removed prior to removing regulators.

5. Disconnect the Mate-N-Loks from the regulator to be removed.

6. Remove three screws, two on the top (Figure 7-7) and one on the bottom (Figure 7-1) of the regulator.

7. Rotate the memory frame 90 degrees back to the horizontal position.

8. To remove the regulator, slide it out.

9. Verify that the power to the power supply is off.

10. Install the new regulator.

11. Carefully rotate the memory frame 90 degrees and tilt the power supply to install the regulator mounting screws (three).

CAUTION

Use the correct length screws when installing regulator.

12. Remove loads from the regulator by disconnecting the four Mate-N-Loks from the backplane.

13. Turn on power to the regulator.

NOTE

If the regulator crowbars, turn power off and rotate the regulator voltage adjustments potentiometer fully counterclockwise (below crowbar voltage.) Turn on power.

14. Using a digital voltmeter, measure the voltage at the removed Mate-N-Lok connector of the replaced regulator to ensure that the voltage is within limits specified in Paragraph 7.5. Adjust voltage if necessary.

15. Turn off power and reconnect the four Mate-N-Loks to the backplane.

16. Turn on power and check the regulator voltage at the backplane per Paragraph 7.5. Adjust voltage if necessary.

7.6.3 AC Input Box and 5411086-YA Power Line Monitor Board

1. Perform the power supply access procedure (Paragraph 7.6.1).

CAUTION

Do not remove the power supply hinge screws when performing the next step.

2. Remove the two power system screws on each side of the power supply.

3. Carefully rotate the memory 90 degrees and tilt the power supply (Figure 7-7).

WARNING

Ensure that ac power is removed prior to removing the ac input box or 5411086-YA power line monitor board.

4. Disconnect all the Mate-N-Loks connected to the ac input box.

5. Disconnect the card edge connector from the 5411086-YA power line monitor board.

CAUTION
Hold the ac input box in place while performing the next step.

6. Remove three screws and slide out the ac input box.

7. Remove 5411086-YA power line monitor board from the ac input box.

7.6.4 Fan Removal

1. Perform the power supply access procedure (Paragraph 7.6.1).

NOTE
The memory frame should be in a horizontal position when removing fans.

WARNING
Ensure that ac power is removed.

2. Remove all modules.

3. On the module side of the fan, remove the two screws holding the fan.

4. Slide the fan up and out of the power supply chassis and disconnect the jack (Figure 7-8) from the fan.

CAUTION
When installing the fan, do not tighten the screws beyond 10 in-lb. Tightening screws beyond 10 in-lb may cause the fan to bind.

7.6.5 Transformer Assembly Removal

WARNING
Remove ac power before performing this procedure.

1. Remove the H7441 and 7014251 regulators per Paragraph 7.6.2.

2. Remove the ac input box per Paragraph 7.6.3.

3. Remove both fans per Paragraph 7.6.4.

4. Disconnect the transformer assembly's Mate-N-Loks.

5. Remove both screws from the transformer assembly's cable clamp (Figure 7-9).

6. Rotate the memory frame to the horizontal position.

7. Remove the transformer assembly's four mounting screws and nuts and lift out the transformer assembly.

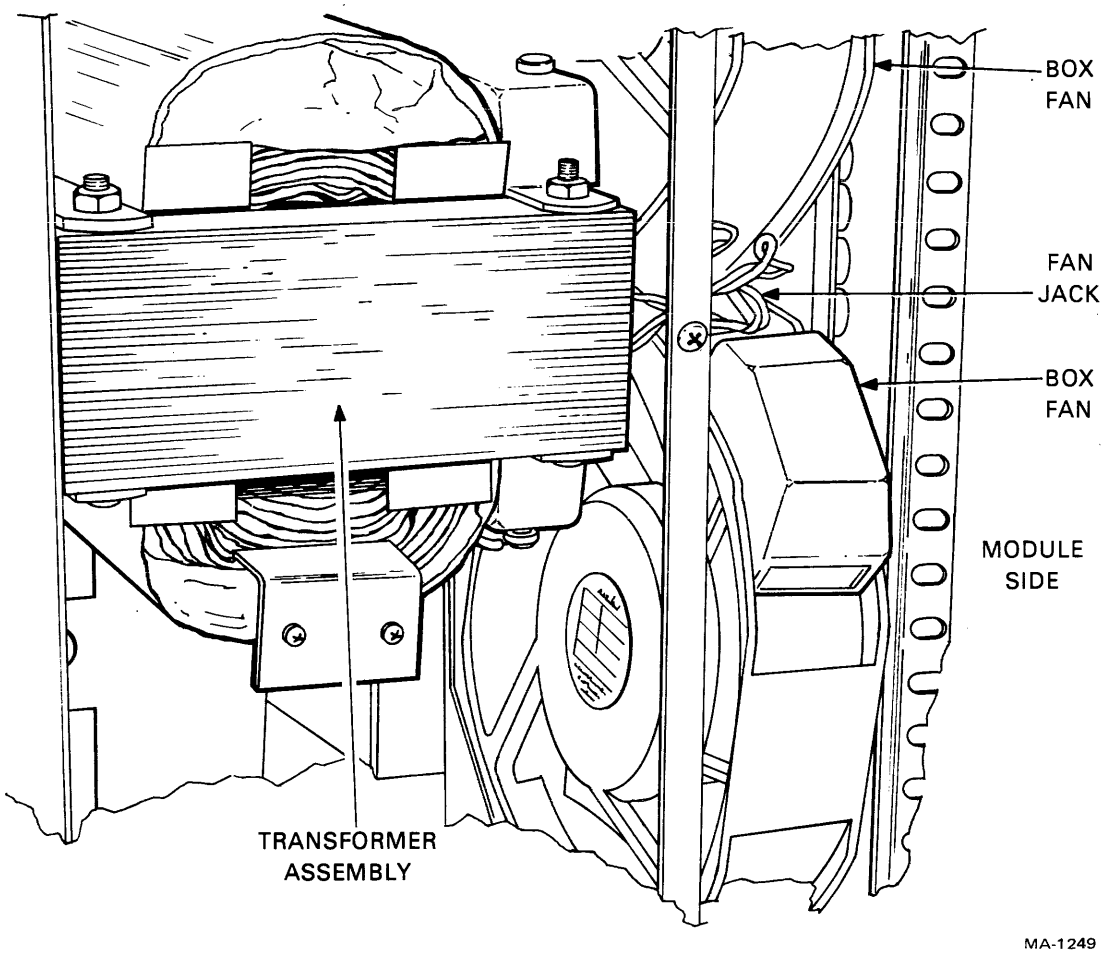


Figure 7-8 Fan Removal

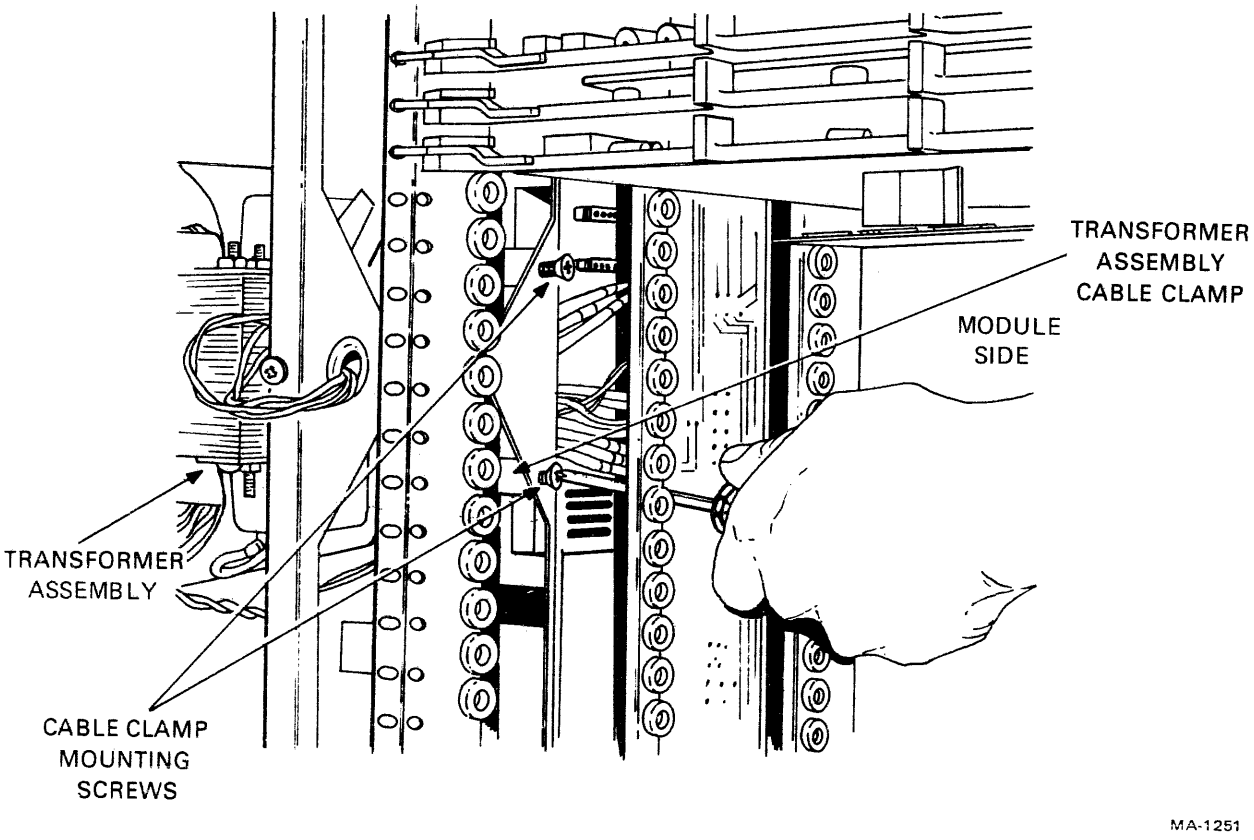


Figure 7-9 Transformer Assembly Removal

CHAPTER 8
INSTALLATION

8.1 INTRODUCTION

This chapter describes the procedures involved in expanding existing MK11 memory systems. Memory systems may be expanded in three ways: by adding storage array modules to the memory boxes, by installing a second memory box in a memory cabinet, and by adding a second memory cabinet to the system. Refer to the unit assembly drawings, UA-11/70-0-0, UA-MK11-B-0, and the PDP 11/70 system expansion drawings E-AR-11/70-4-5 for detailed drawings and parts lists during installation of memory expansions.

NOTE

The system size register must be reconfigured whenever the memory capacity is altered. Refer to the PDP-11/70 Installation and Maintenance Manual for a description of this procedure.

8.2 ADDING ARRAY MODULES

The memory capacity can be expanded in increments of 32K words by installing additional storage array modules. Each memory box holds up to 16 arrays. Additional arrays must be added in the order specified in Figure 8-1. For example, if a memory box contains two array modules, one in slot 9 (no. 0) and one in slot 18 (no. 1), the next array must be installed in the array 2 position, backplane slot 8. Subsequent expansions will add arrays to slots 19, 7, 20, 6, 21, etc., in that order.

Do not leave empty backplane slots between storage array modules. Empty array slots cause configuration errors which prevent the memory from operating.

An odd number of array modules prohibit internal interleaving. If internal interleaving is desired, the memory must be balanced, that is, have the same number of arrays on both sides of the memory box.

8.3 ADDING A MEMORY TO AN EXISTING MEMORY CABINET

Placement of cables is critical in the memory cabinet. The cables will be damaged if the following procedure is not followed carefully. The steps below refer specifically to adding memory box 1 to the first memory cabinet. The procedure for installing expansion box 3 to the second memory cabinet is similar, and can be generalized from the steps given in this section if the following guidelines are observed.

- Cable from lower-numbered memory box to higher numbered box. Take up excess cable slack inside of higher numbered memory box.
- Keep smooth side up on incoming ribbon cables. Keep ribbed side up on outgoing ribbon cables.
- Memory boxes 0 and 2 have their incoming cables on the left-hand side of box. Memory boxes 1 and 3 have their incoming cables on the right.

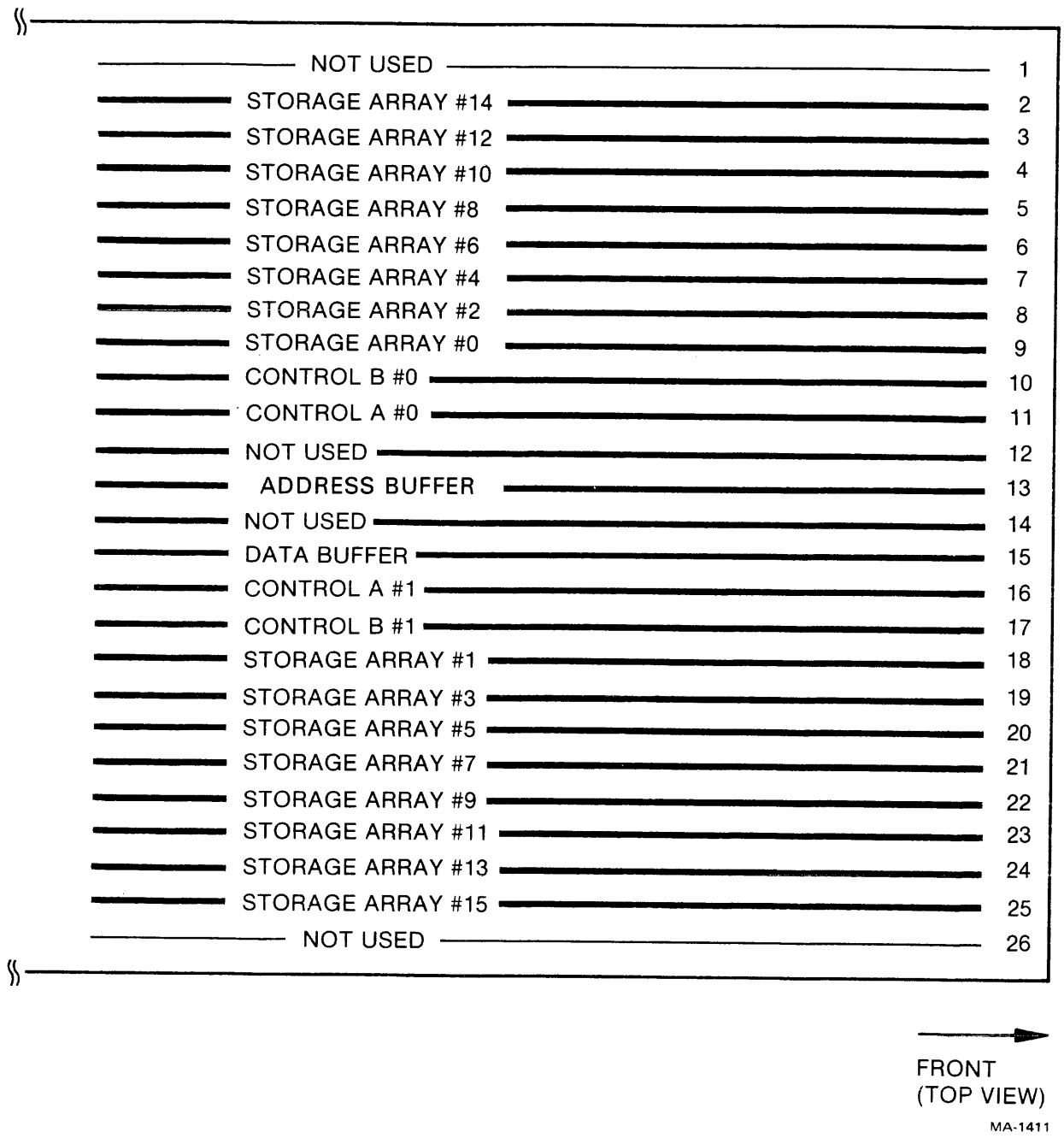


Figure 8-1 Backplane Slot Allocation

Prior to installation, check contents of shipment against packing list, unpack containers, and inspect for obvious shipping damage. Remove the memory cabinet's front and rear doors.

Configure the power fail jumpers on the address buffer module (M8158) as shown in Table 8-1. This allows any memory except the last memory box of the main memory bus to be switched off-line and powered down without affecting the other memories or the processor.

Table 8-1 Power Fail Jumpers

Memory	W1	W2	W3	W4
Last Memory Box on Bus	Out	In	Out	In
All Other Memory Boxes	In	Out	In	Out

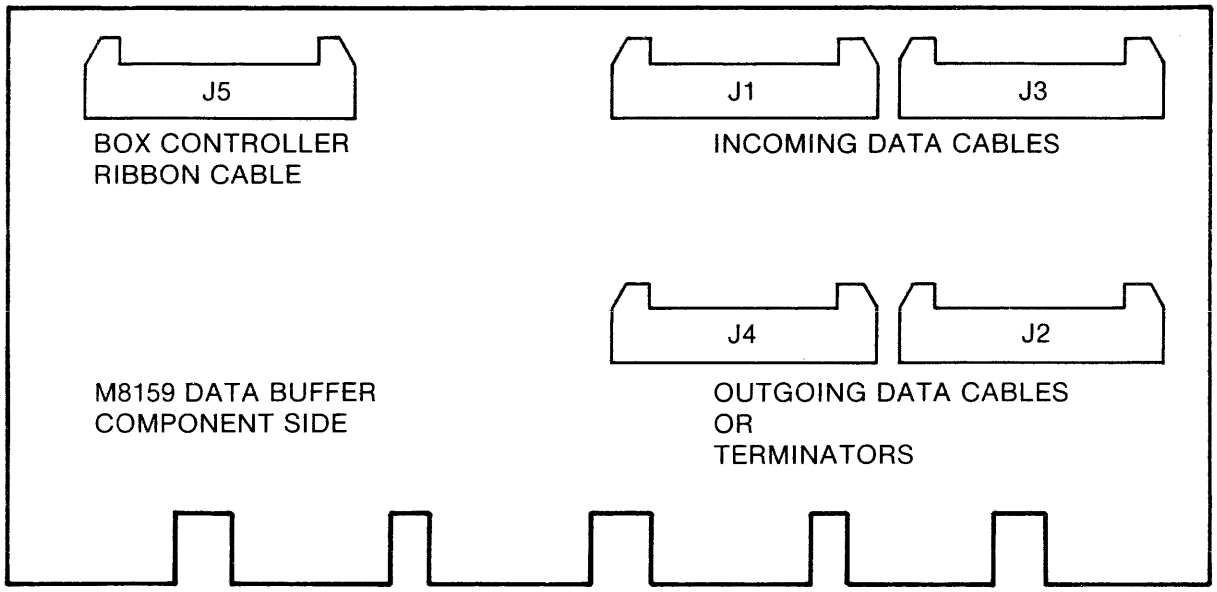
The CSR address select switches must select the address corresponding to the memory's unit number. Consult Table 8-2 for the proper CSR address and set the switches on the address buffer module. Apply unit number decal to memory box.

Table 8-2 CSR Address Selection

Unit Number	CSR Address	Switch Position		
		S1-3	S1-2	S1-1
0	X772100	Closed	Closed	Closed
1	X772104	Closed	Closed	Open
2	X772110	Closed	Open	Closed
3	X772114	Closed	Open	Open

X = 106 for direct addressing mode
X = 17 for indirect addressing mode

1. Extend memory box 0 from the cabinet. Remove the top cover and remove the strain relief bar. Remove address buffer and data buffer modules (slots 13 and 15). Unplug memory bus terminators from J2 and J4; see Figure 8-2 for their location. Configure power fail jumpers as in Table 8-1. Plug in address and data bus cables, keeping ribbed side up and red stripe to the left on the component side of board. Replace address and data buffer modules.
2. Fold outgoing bus cables. Lay cables, ribbed side up, on right-hand side of memory box. Replace the strain relief bracket, keeping cables between retaining screws. Flatten outgoing cables and pull them toward rear of box to take up any slack inside the box. Tighten strain relief bracket. Tie-wrap outgoing cables to power supply assembly.
3. Tilt memory box 0 to the 90-degree service position. Align cables so they extend straight back into cabinet, parallel to the slide rails. Tie-wrap cables to front cable retractor bar as shown in Figure 8-8, taking up slack in cables between memory box and retractor. Route bus cables over cable retractor and into cabinet. Use tape to tie-wrap the four cables together between memory box and front cable retractor. Place floating restraint under cables mid-way between memory box and cable retractor and tie-wrap to cables.



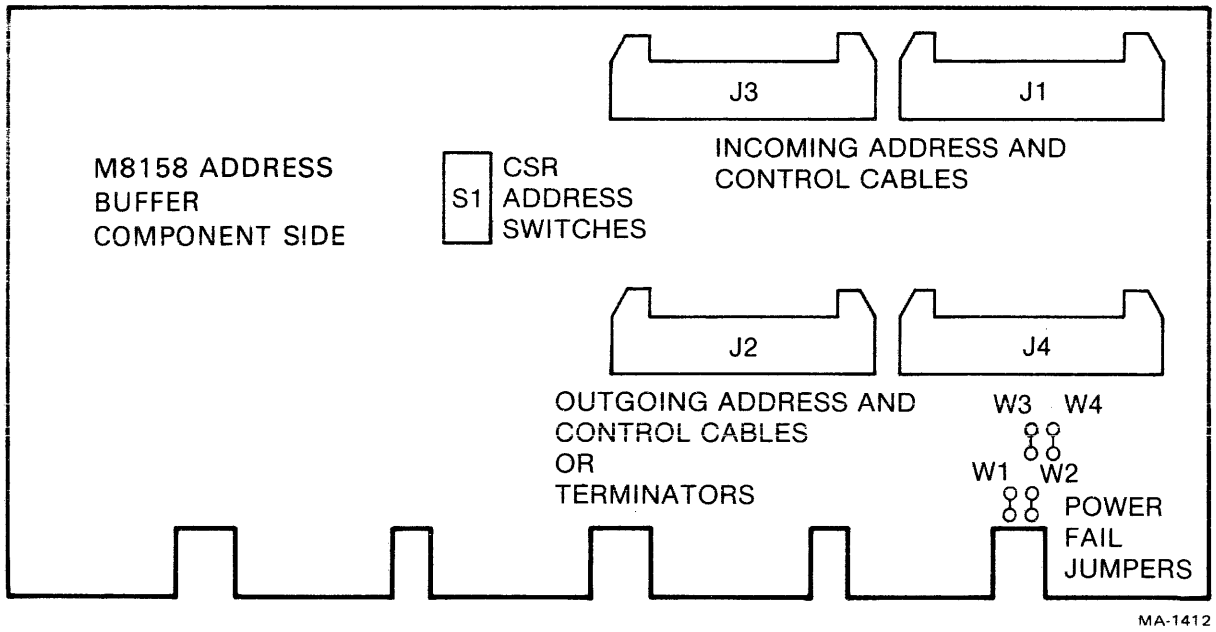


Figure 8-2 Address and Data Buffer Plug Locator. Plug In Cables with Ribbed Side Up and Red Stripe to the Left.

4. Tilt memory box 0 to its level position and replace top cover. Slide box 0 into cabinet, guiding cables by hand if necessary.

5. Mount memory box 1 in cabinet, position slide rails at height indicated in Figure 8-3.

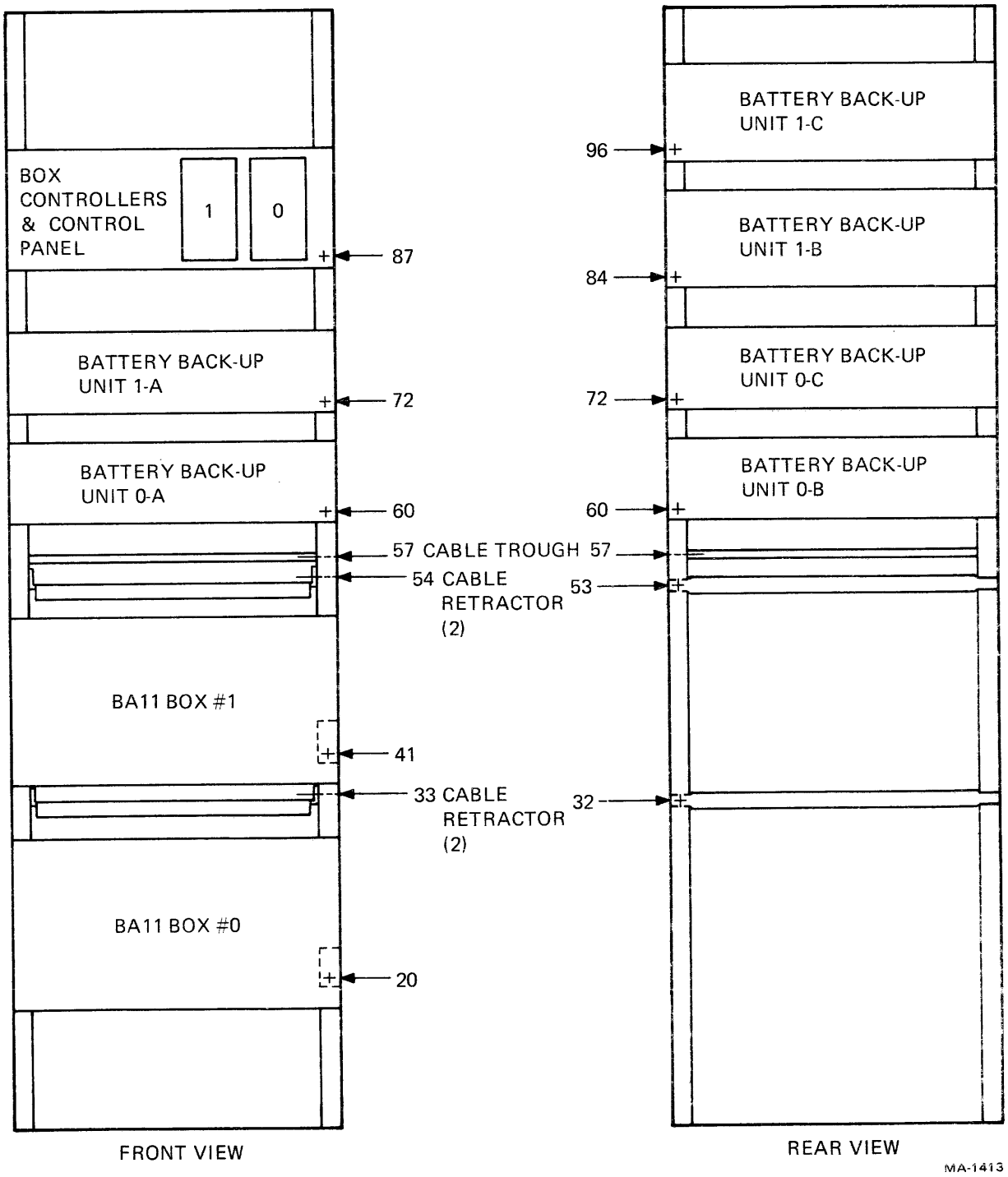


Figure 8-3 Memory Cabinet Configuration

6. Route power cables (Figure 8-4). Tilt box 1 to the 90-degree service position. Plug in battery backup and box controller power cables and tie-wrap to power supply chassis. Overlap the two power cables on left side of box and tie-wrap them to the front cable retractor, taking up any slack and keeping the cables parallel to the slide rails. Route cables straight back through the cabinet, under and around the rear cable retractor bar. Tie-wrap power cables to cable retractor. On right side of box, route and tie-wrap power and controller cables in the same fashion. Tie-wrap cable bundles every 15 cm (6 in). Use tape to tie-wrap cables between memory box and front cable retractor.

7. Install battery backup units 1B and 1C in the rear of the cabinet at the heights shown in Figure 8-3. Plug power cables into battery backup units. Take up slack in cables by tie-wrapping loops into the cables as shown in Figure 8-5.

8. Remove blank control panel cover. Pull controller power cable through cutout on top of control panel and out through front of panel. Plug cable into box controller and mount controller in control panel. Install battery backup unit 1A in cabinet and plug in power cable. Tie-wrap loops into cables to take up slack as shown in Figure 8-6.

9. Return memory box 1 to level position. Remove top cover and strain relief bar. Lay the four incoming bus cables, from box 0, on the right-hand side of box, keeping smooth side of cables up. Replace strain relief bar (do not tighten) and position cables justs to the left of the retaining screw. Pull bus cables forward under strain relief, taking up enough slack in cables to allow service loop (Figures 8-7 and 8-8). Cables should be snug when memory box is pushed back into cabinet. If box is pushed into cabinet to check length of service loop, push box carefully and guide cable by hand to avoid damage to cables.

10. Remove data buffer and address buffer modules. Configure power fail jumpers and CSR address switches as indicated in Tables 8-1 and 8-2. Plug terminators and bus cables into modules as in Figure 8-2. Secure terminators with two screws. Keep red stripe to left on component side of modules. Replace address and data buffer modules. Fold incoming bus cables to take up slack inside of memory box. Tie-wrap incoming bus cables every 15 cm (6 inches).

11. Plug box controller ribbon cable into data buffer board, fold, and lay on top of incoming bus cables, keeping smooth side up. Lift strain relief bar and slide cable under bar. Position cable on top of bus cables (do not alter position of incoming bus cables). Flatten controller cable to remove slack and tighten strain relief bar. Replace top cover and tilt box to the 90-degree service position.

12. Route controller ribbon cable over front cable retractor bar, then under and around rear cable retractor (Figure 8-6.) Take up slack in cable and tie-wrap to cable retractors as shown. Keep cable path parallel to slide rails. Bring cable across to front of cabinet and plug into box controller (Figure 8-7.) Plug cable in with smooth side of cable up on bracket behind controller. Take up slack in cable with folds and tie-wrap to bottom of control panel. Install strain relief bracket behind controller panel. Tie-wrap floating strain relief to cables mid-way between memory box and front retractor bar.

13. Return memory box to level position. Tie-wrap power cord to rear cable retractor. Plug power cord into switched receptacle of the 861 power controller. Attach memory unit number decal corresponding to CSR address to memory box. Push memory box into cabinet, guiding cables by hand if necessary.

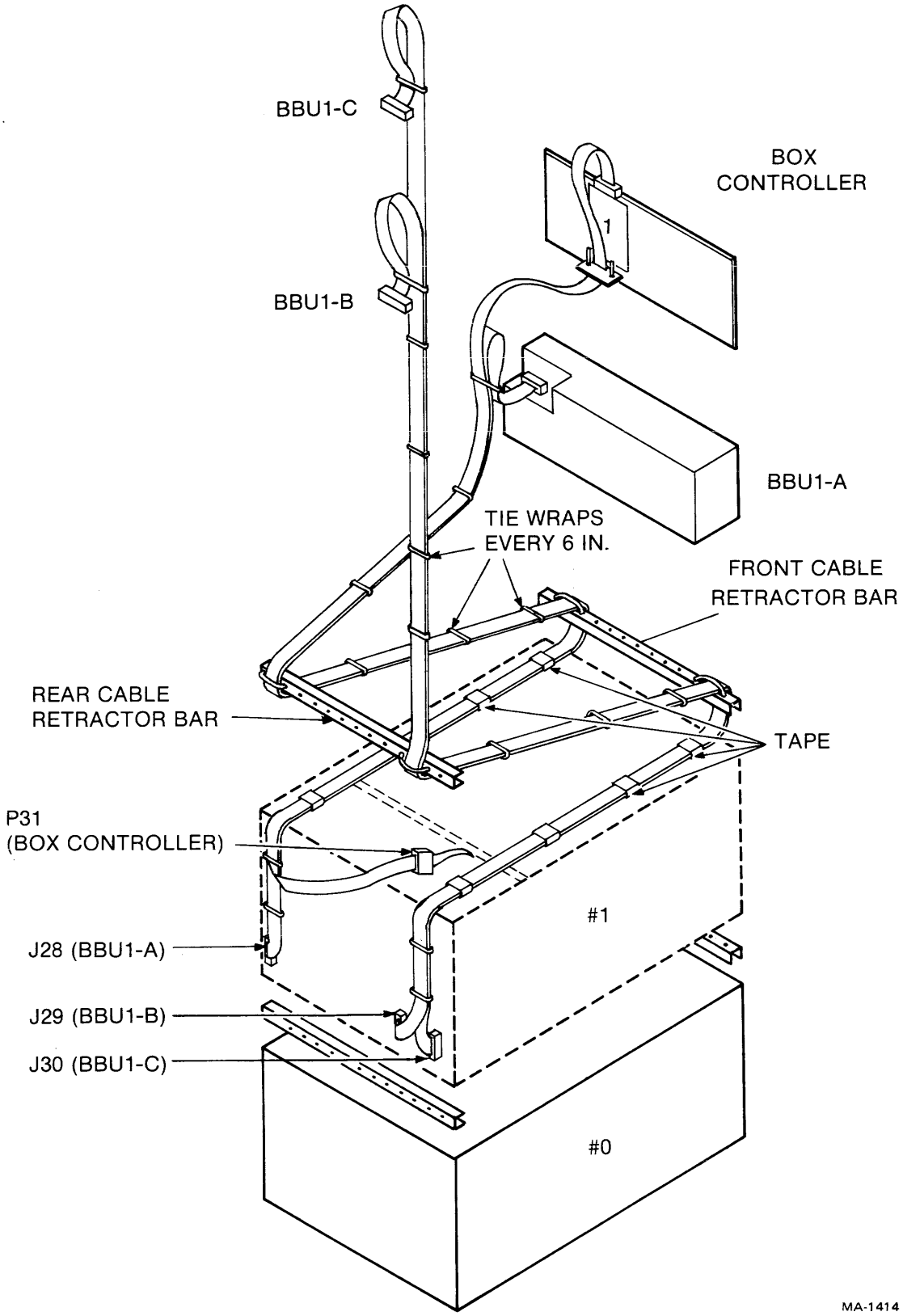


Figure 8-4 Box Controller and Battery Backup Power Cables Box 1

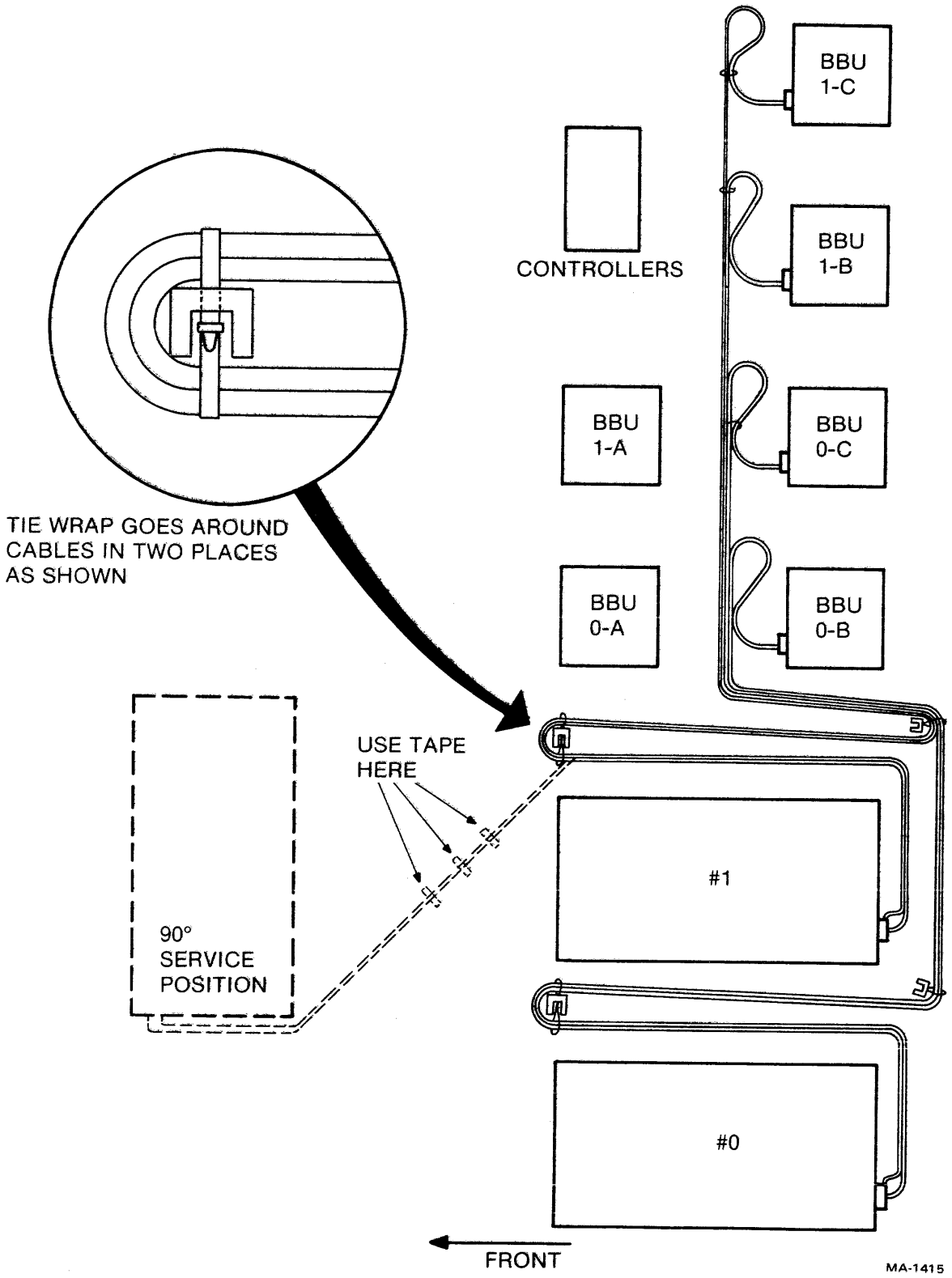


Figure 8-5 Battery Backup Power Cable Routing
First Memory Cabinet (Left Side)

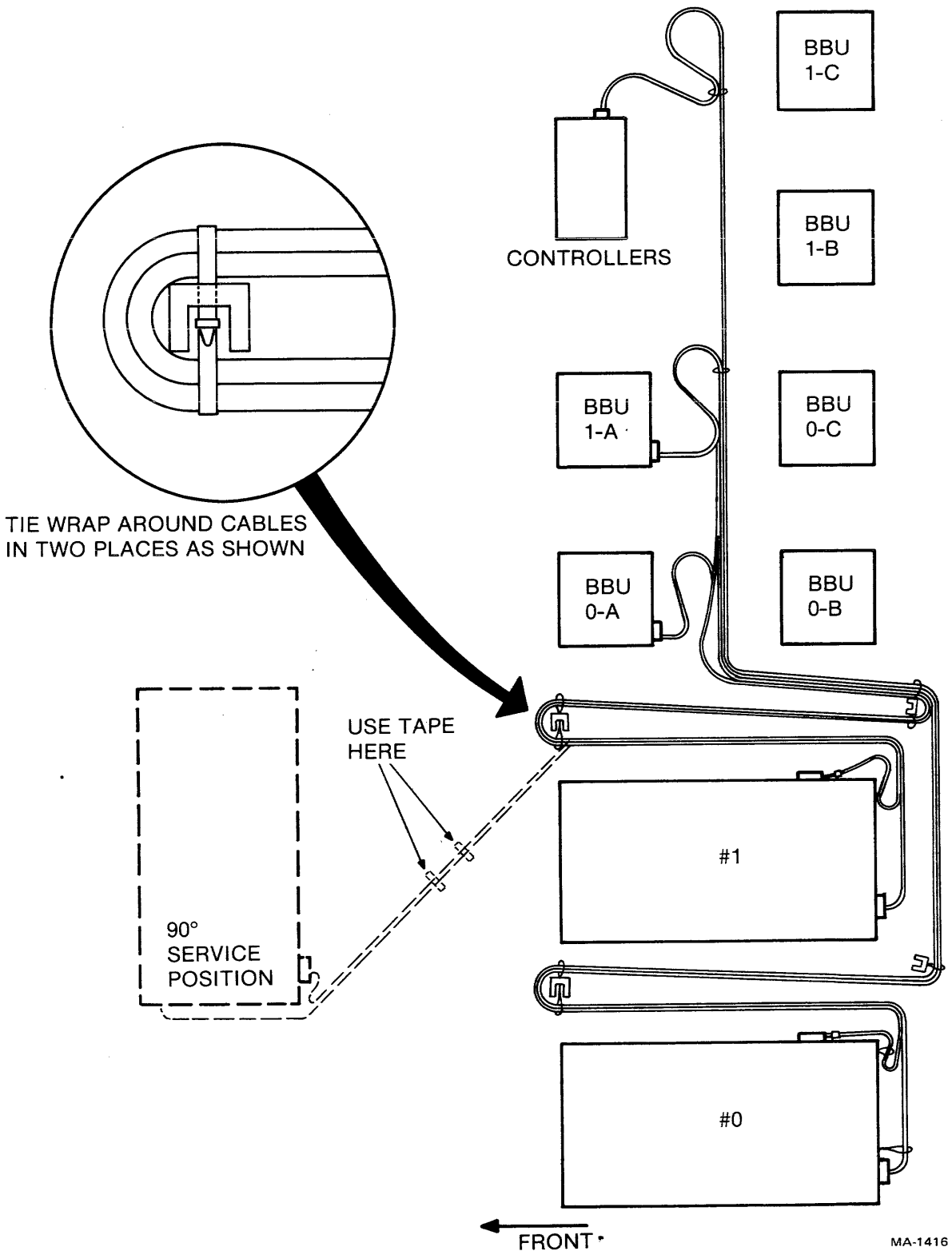


Figure 8-6 Box Controller and Battery Backup Power Cable Routing
First Memory Cabinet (Left Side)

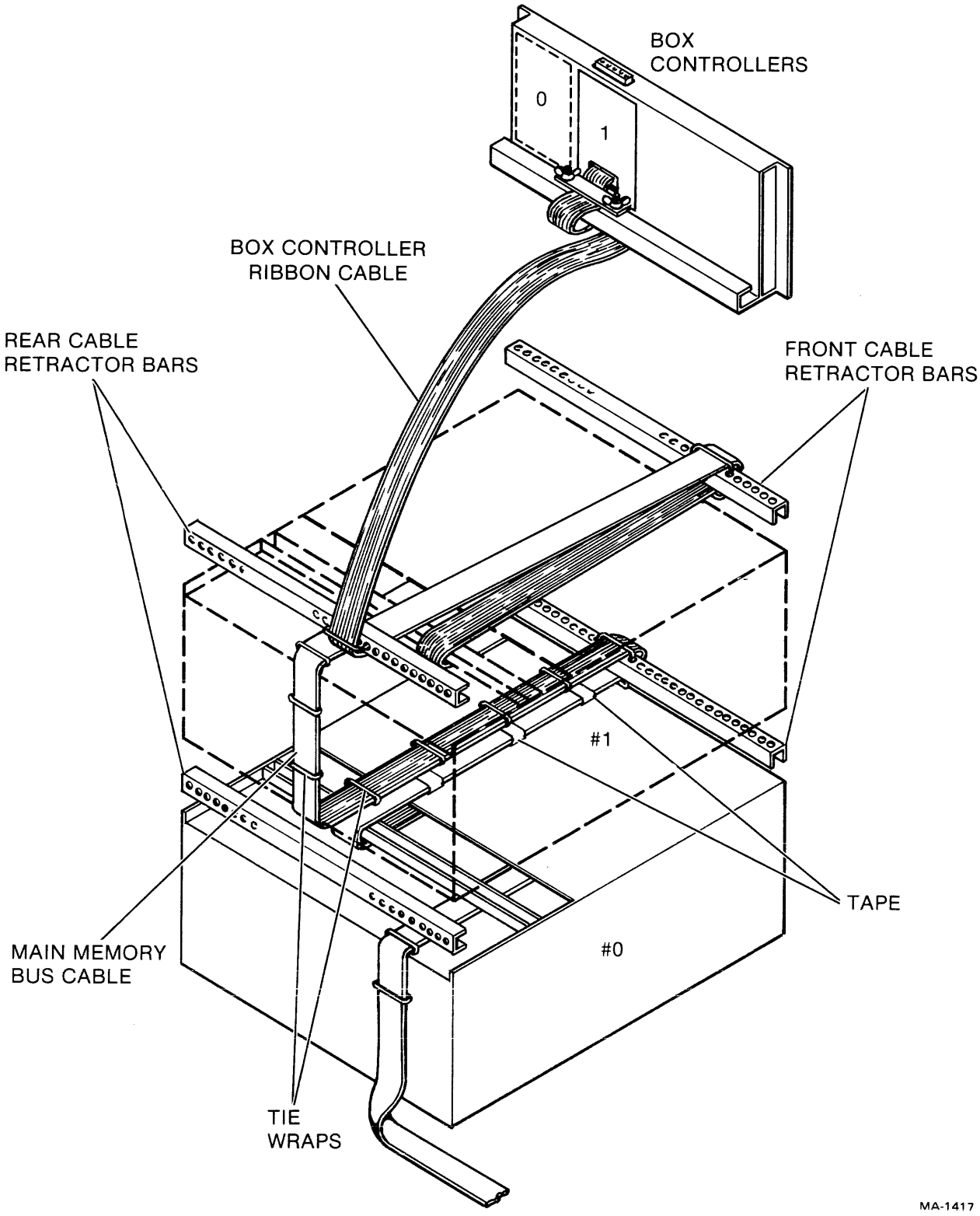


Figure 8-7 Main Memory Bus and Box Controller Cables, Box 1

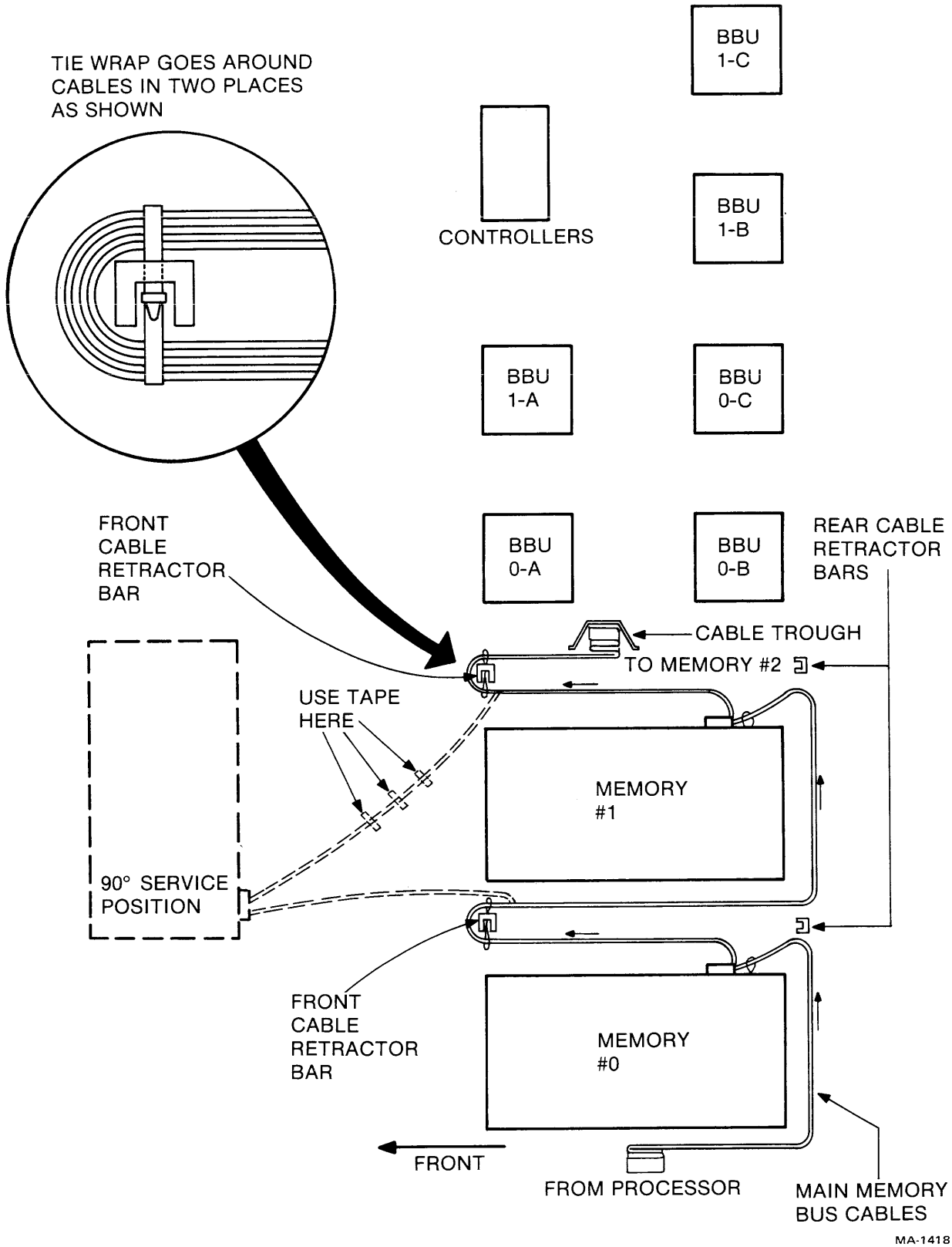


Figure 8-8 Main Memory Bus Cable Routing
First Memory Cabinet (Left Side)

8.4 INSTALLING SECOND MEMORY CABINET

Expansion memory cabinets are shipped with the memory box, battery backup units, and the box controller, installed and cabled. The second memory cabinet is installed immediately to the right of the first memory cabinet. At most sites, this requires repositioning the tape or disk drive cabinet since these cabinets are positioned to the right of the memory cabinet(s).

Prior to installation, check contents of shipment against packing list and inspect for obvious shipping damage.

1. Remove shipping container and polyethylene covers from cabinet. Remove tape, plastic shipping pins, and securing bolts from cabinet. Remove side panel from right side of first memory cabinet.

2. Raise leveling feet so that cabinet rests on its casters. Roll cabinet onto floor, using suitable ramp. Push cabinet into position along side the first memory cabinet.

3. Install filler strips between memory cabinets. Lower leveling feet to align height of second memory cabinet to first memory cabinet. Tighten bolts securing cabinets together. Install ground strapping between cabinets. Remove shipping bracket from memory box.

4. Install memory bus cable trough at height indicated in Figure 8-3.

5. Extend memory box 1 to service position. Remove top cover. Remove strain relief bracket. Remove address buffer and data buffer modules. Note cable positions, and do not alter folds in ribbon cables. Configure power fail jumpers per Table 8-1. Unplug memory bus terminators. Connect main memory bus cables to modules keeping ribbed side up and red stripe to left on component side of board. Replace address buffer and data buffer modules.

6. Fold outgoing bus cables, keeping ribbed side up, and lay them on left side of memory box just to the right of strain relief bracket-retaining screw. Return incoming cables to original position. Replace strain relief bracket; do not tighten. Pull outgoing cables backward to take slack out of memory box. Tighten strain relief bracket.

7. Replace top cover. Tilt memory box 1 to the 90-degree service position. Tie-wrap outgoing bus cables to front cable retractor bar as shown, taking up slack between memory box and cable retractor. Keep path of cables parallel to slide rails. Wrap cables together with tape. Tilt memory box 1 back to level position and push memory box back into cabinet.

8. Extend memory box 2 to service position. Remove top cover. Remove strain relief bracket. Note position of controller ribbon cable.

9. Fold and route memory bus cables through cable trough into second memory cabinet (Figure 8-9). Exit cables with smooth side up through front of second memory cabinet on top of front cable retractor bar. Lay cables on left side of memory box just to the right of retaining screw. Straighten cables and tie-wrap to front cable retractor bar.

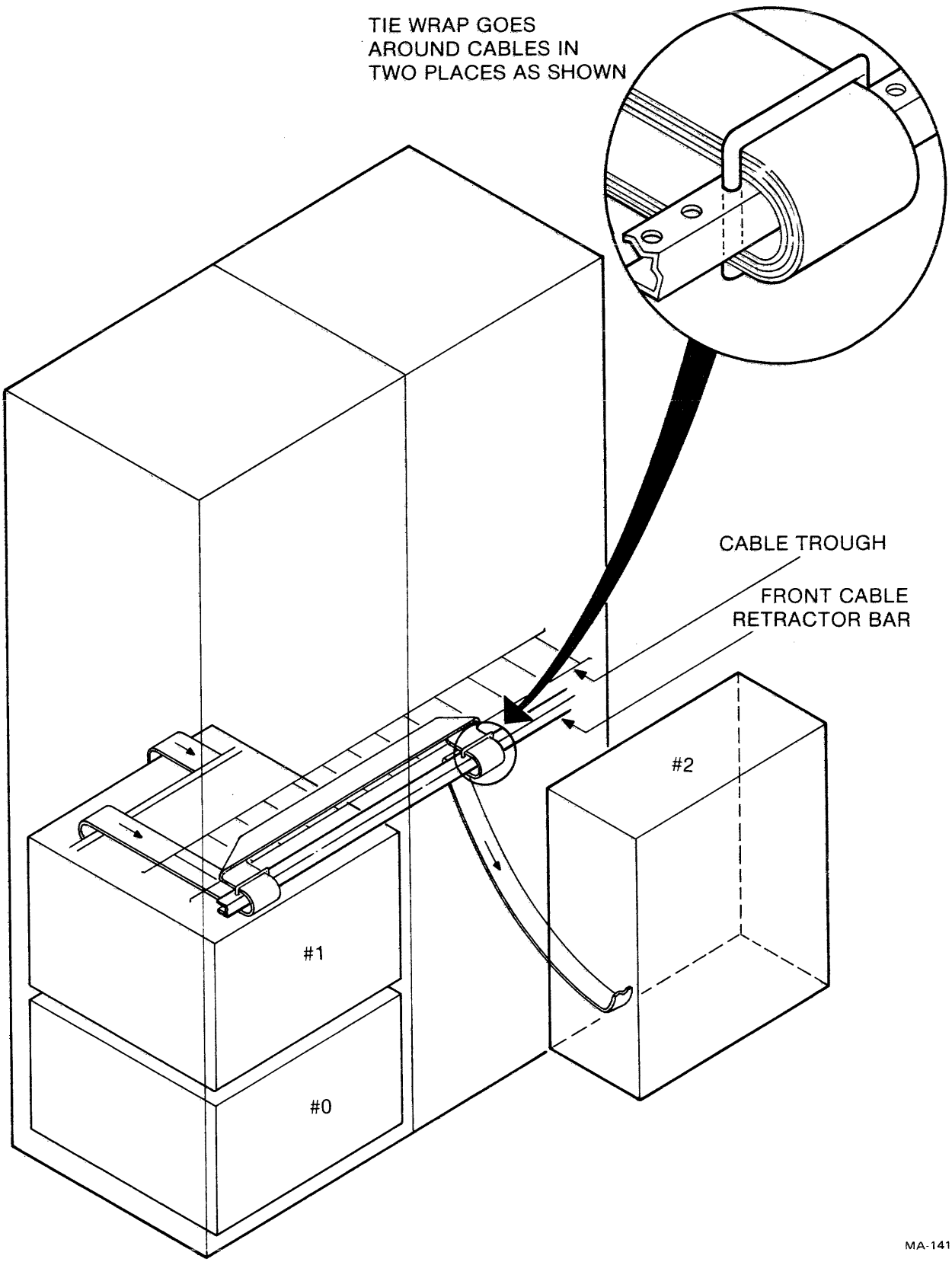


Figure 8-9 Main Memory Bus Cable Routing
Box 1 to Box 2

10. Remove address buffer and data buffer modules. Configure power fail jumpers and CSR address select switches per Tables 8-1 and 8-2. Connect memory bus terminators and incoming bus cables. Secure terminators with two screws each. Replace address buffer and data buffer modules. Replace strain relief bracket; do not tighten.

11. Tilt memory box 2 to the 90-degree service position. Pull upward on incoming bus cables to take up slack between front cable retractor and memory box. Ensure that controller ribbon cable is returned to former position. Tighten strain relief bracket. Tape incoming cables together between cable retractor and memory box. Tie-wrap cables to floating restraint.

12. Return memory box 2 to level position. Fold incoming cables to take up slack inside of memory box. Replace top cover.

13. Place unit number decal on memory box to indicate CSR address as in Table 8-2. Plug in power cord. Verify cabling with diagrams.

CHAPTER 9
MAINTENANCE

9.1 INTRODUCTION

This chapter describes the use of the memory diagnostic program and contains a troubleshooting flowchart for isolating faults in the memory system. For a detailed description of the diagnostic program, refer to the diagnotic's documentation, AC-C644A-MC. If the power supply is suspected as the cause of a malfunction, refer to Chapter 7 of this manual.

9.2 DIAGNOSTIC PROGRAM

The diagnostic program tests the memory and provides a configuration map and error reports to isolate faults in the memory. A faulty array module can be located directly from the diagnostic's printouts. If a fault occurs in the buffer or control modules, it can be isolated by interpreting the diagnostic's error printouts. The operation of the diagnostic can be tailored by selecting options with the CPU console switch register. A special field service mode allows control of certain diagnostic routines from the terminal.

The diagnostic requires a minimum of 32K words of core memory (MJ11) or 64K words of MOS memory (MK11) residing in a single memory box. Also, there must be no response to Unibus addresses 17772100 through 17772136. The lower 16K words of memory, where the program resides, must have no uncorrectable errors (double-bit errors). The diagnostic runs stand-alone or under any of the following monitors:

- XXDP
- ACT
- APT

9.2.1 Operating Instructions

Quick Start

1. Load Address 200.
2. Set switch register to select options.
3. Start.

Stopping

1. Lift console switch 8.
2. Type control C.

Restarting (Preserves Configuration Map)

1. Load Address 202.
2. Set switch register to select options.
3. Start.

9.2.2 Console Switch Register Options

Prior to starting the diagnostic, select the desired options with the switch register. If no console switch register exists, a software switch register may be accessed by typing control G. This displays the current data in the switch register and accepts new software switch register data (in octal) from the terminal.

Console Switch	Select Option
15	Halt on error
14	Loop on test
13	Inhibit error printouts
12	Inhibit relocation
11	Quick verify test/Inhibit margin tests
10	Bell on error
9	Loop on error
8	Halt program
7	Detailed error reports
6	Print configuration map
5	Limit number of error prints per bank
4	Fat terminal (132 columns or wider)
3	Test mode
2	Test mode
1	Test mode
0	Detect single bit-errors

Switch 15 (Halt on Error) – Halts program on error. Allows changing options in switch register prior to continuing.

Switch 14 (Loop on Test) – Causes looping on present test or looping on present pattern for entire bank of memory.

Switch 13 (Inhibit Error Printouts) – Stops error messages from being printed on terminal.

Switch 12 (Inhibit Relocation) – Prevents program from being relocated out of lowest bank of memory. Program is normally relocated in order to test bank 0.

Switch 11 (Quick Verify Test/Inhibit Margin Tests) – Shortens time required for each pass, no margining test performed.

Switch 10 (Bell on Error) – Causes bell at terminal on each error trap.

Switch 9 (Loop on Error) – Cause looping from failure point back to last correctly initialized area of current test.

Switch 8 (Halt Program) – Initiates following sequence.

1. Clears margins in program's MAINT register
2. Moves relocated program back to bank 0
3. Flushes out any double-bit errors
4. Turns off memory management
5. Restores loaders
6. Unmaps Unibus map
7. Halts if under APT or ACT branch select

Switch 7 (Detailed Error Reports) – After printing normal error message, terminal prints contents of registers: R1, R2, R3, R4, R5, SP, MEMERR, MAINT, CONTROL, LOADRS, HIADRS, and CPUERR.

Switch 6 (Print Configuration Map) – After sizing memory, configuration map is printed. (Paragraph 9.2.3).

Switch 5 (Limit Number of Error Printouts per Bank) – Limits number of error printouts per bank to ten.

Switch 4 (Fat Terminal) – For terminals of 132 columns or wider.

Switches 3–1 (Test Mode) – Determines the recursion algorithm used during pattern tests.

Mode Number	Test Mode
0	BAFPAF – Banks forward, patterns forward
1	BAFPAR – Banks forward, patterns reverse
2	BAWPAF – Banks worst first, patterns forward
3	BAWPAR – Banks worst first, patterns reverse
4	PAFBAF – Patterns forward, banks forward
5	PAFBAW – Patterns forward, banks worst first
6	PARBAF – Patterns reverse, banks forward
7	PARBAW – Patterns reverse, banks worst first

For details on patterns, see diagnostic documentation. Initially, start with test mode 0 for a complete test. If errors are isolated to one or a few blocks, use test modes that test worst banks first. Test mode 7 runs the most difficult pattern on the bank with the most errors first, which is a fast way to see if the suspected fault has been corrected.

Switch 0 (Detect Single Bit Errors) – Disables error correction for reporting single-bit errors. Switch should be off for field service purposes.

9.2.3 Memory Configuration Map

With console switch 6 up, the diagnostic prints the memory configuration map after sizing the memory. The configuration map can also be printed by entering the field service mode and typing command number 6. The map shows the memory capacity in 16K banks, the type of interleaving, the type of memory (MOS or core), the box numbers, and the protected banks. The map flags all banks in which errors were found during the sizing routine. Figures 9-1 through 9-5 are examples of configuration maps.

The top row of numbers (Figure 9-1), 0 through 167_8, represents a possible 120 16K word banks of memory.

ERRORS – An X in this row indicates that a single-bit or double-bit error occurred in that bank while the sizing routine was writing 0s and 1s.

ACCESSED – A 1 means that the indicated bank of memory exits, or at least the CPU could access it during the sizing routine. A 0 means no memory was found at that bank.

INTRLV – The number in this row (0, 2, 4, or 8) is the number of ways internally and externally interleaved. A question mark is printed in nonexistent banks.

- 64K OF MEMORY
- INTERNALLY INTERLEAVED
- NO ERRORS

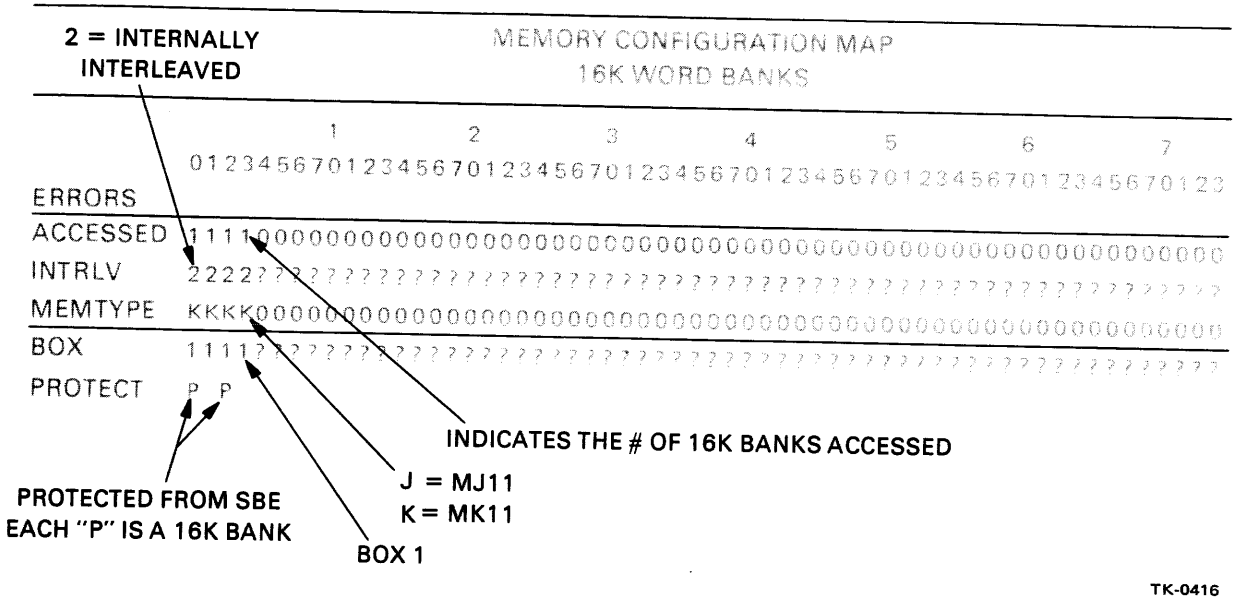


Figure 9-1 Diagnostic Configuration Map Example 1

- 96K OF MEMORY
- NO INTERNAL INTERLEAVING
- WITH ERRORS

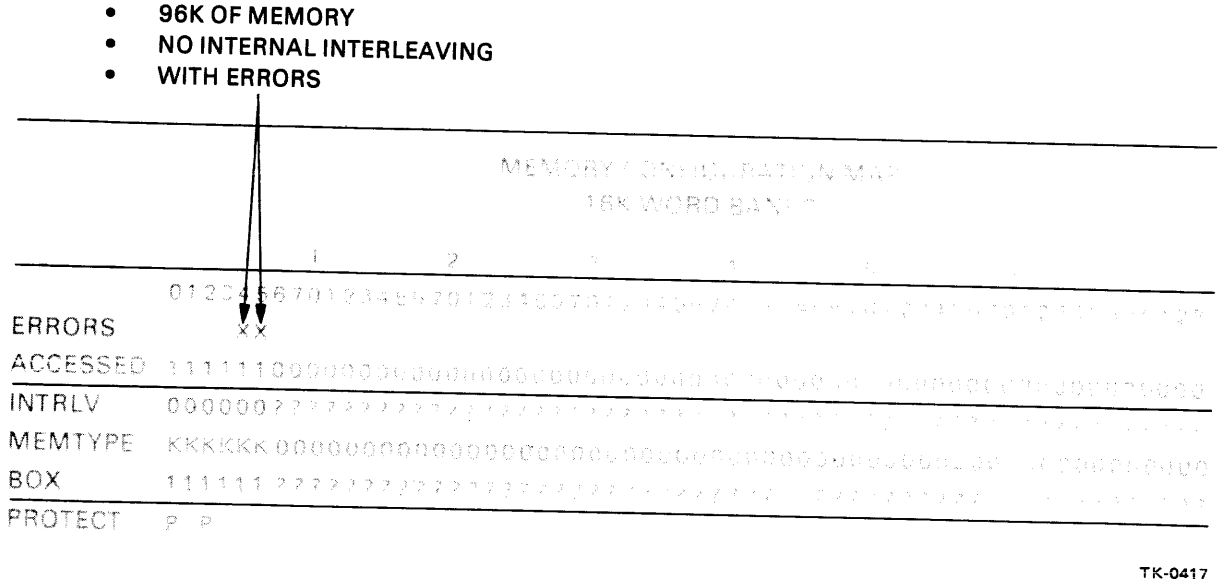


Figure 9-2 Diagnostic Configuration Map Example 2

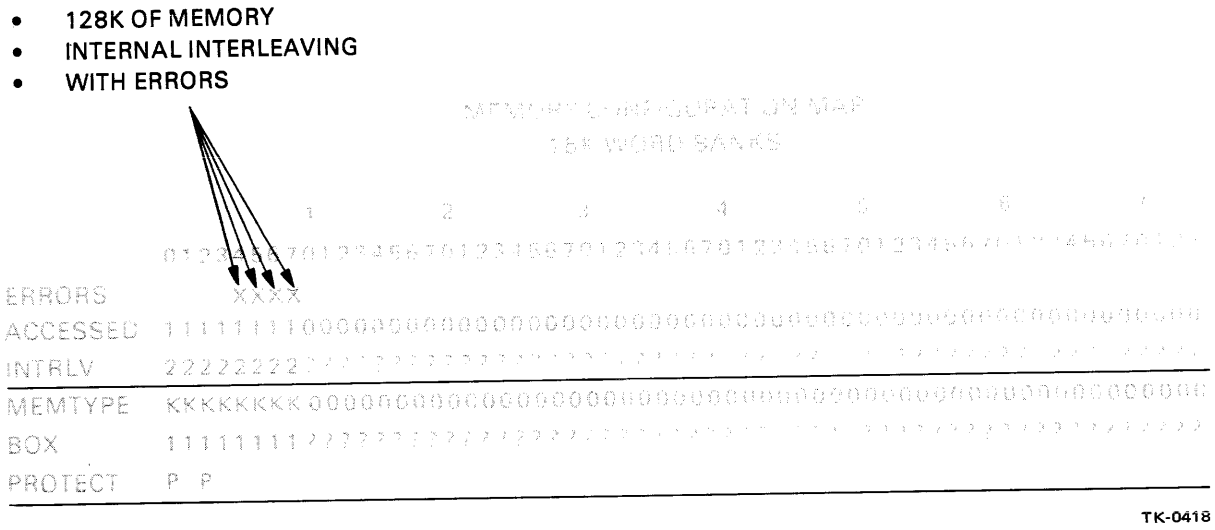


Figure 9-3 Diagnostic Configuration Map Example 3

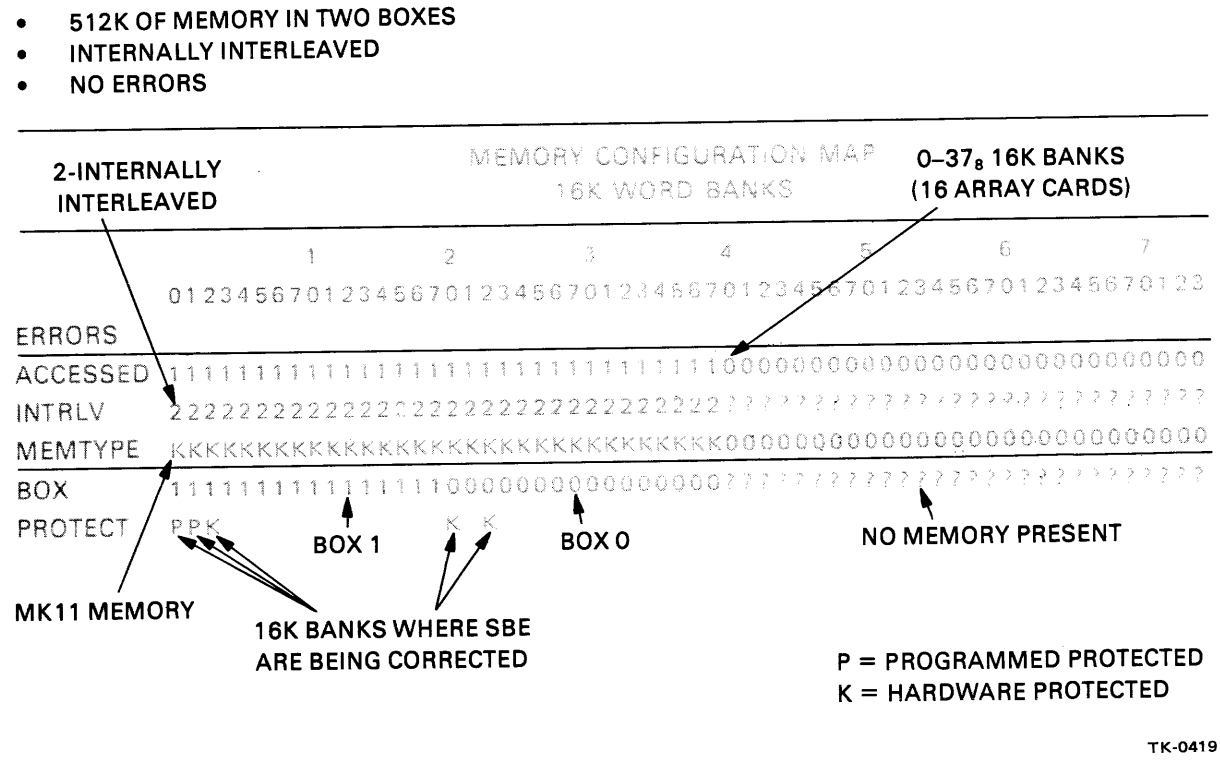


Figure 9-4 Diagnostic Configuration Map Example 4

- 512K OF MEMORY IN TWO BOXES
- INTERNALLY INTERLEAVED IN BOX 1
- WITH ERRORS

BAD CONTROL "B" (M8161) ON RIGHT SIDE
X = SBE (DBE ARE IDENTIFIED THE SAME WAY)

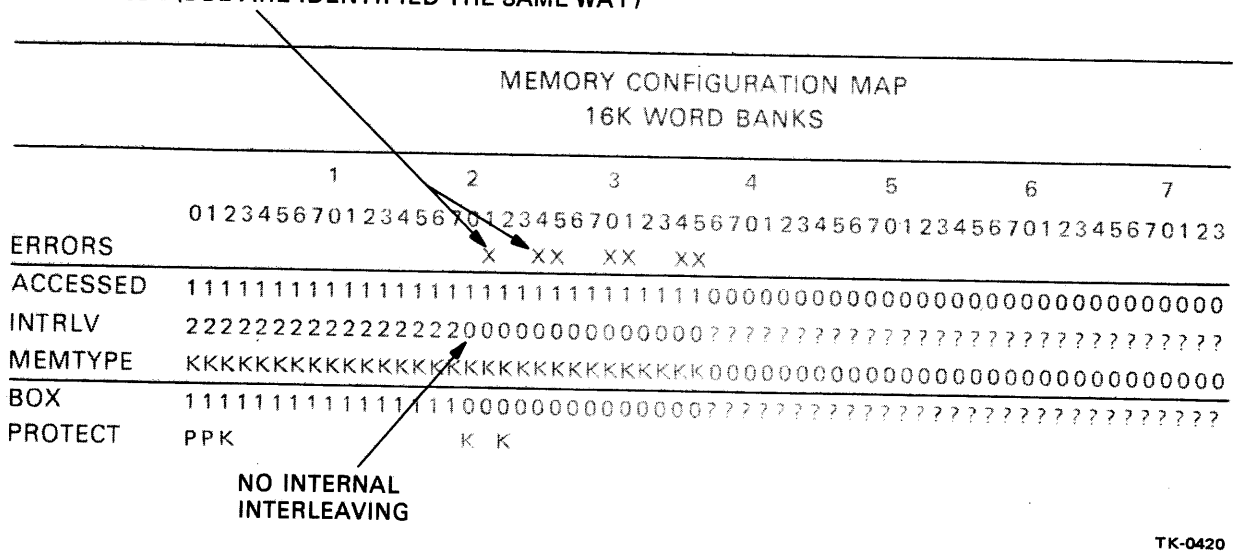


Figure 9-5 Diagnostic Configuration Map Example 5

MEMTYPE – The letter K or J is printed in this row to indicate the type of memory. K is for MK11 memory, J is for MJ11 core memory. A 0 indicates no memory present.

BOX – The box number (0 through 3) corresponding to the CSR address of the box is printed in this row. A question mark indicates either no memory or no CSR in that memory (MJ11 memories have no CSR).

PROTECT – P or K indicates that the banks are part of protected memory space. P is printed for program protected space (where the diagnostic resides.) K is printed for the MK11 hardware protected memory space (lower 16K of each controller.) No errors are reported in these banks.

Example 1 (Figure 9-1) shows an error-free configuration map of 64K words of MOS memory contained in a single memory box. Since the memory is contained in one box (box 1), the 2 in the INTRLV row indicates that the box is internally interleaved. Banks 0 and 2 are protected memory space; the program resides in these banks, and they will not be tested until the program relocates.

In example 2 (Figure 9-2), errors were found in banks 4 and 5 of a single box MOS memory. Since there is no internal or external interleaving (INTRLV = 0), banks 4 and 5 are located on array 2. Array 2 is the second array module on the right-hand side of the memory box; suspect this array as the cause of the errors.

In example 3 (Figure 9-3), one array module has been added to the memory box of example 2. The memory box is now balanced; there are two MS11K arrays on each side of the box and the box is internally interleaved (INTRL = 2).

Errors were found in banks, 4, 5, 6, and 7. These four banks, because of interleaving, reside on array modules 2 and 3. Since these two arrays are controlled by different control module pairs, the control modules can be assumed good. Look for faults in the two buffer modules (M8158 and M8159) or possibly faults on both arrays 2 and 3.

A configuration map for a 2-memory box system is shown in Figure 9-4, example 4. Both boxes are MK11 MOS memories (indicated by the K in the MEMTYPE row.) One, box 1, has a starting address of 0, the other, box 0, has a starting address of 10 (bank 20). Both boxes are internally interleaved, and there is no interleaving between the boxes. Both boxes are filled with eight arrays (total of 512K words); no errors were found in any of them.

The same memory system, this time with errors, is shown in the configuration map of Figure 9-5, example 5. Note, however, that outside the array module on the left side of the box (array 7) was removed to unbalance the box, defeating the internal interleaving. Unbalancing the memory is often useful in isolating faults in the memory. With no internal interleaving, errors were found in block 21 (array 0), blocks 24 and 25 (array 2), blocks 30 and 31 (array 4), and blocks 34 and 35 (array 6). All these arrays are located in the right side of the box. Since the control 0 pair of control modules is associated with only the right side of the box, they are suspect as the cause of the errors.

In order to isolate the faulty module, the control B modules (M8161) were swapped and another configuration map printed. (Figure 9-6, example 6). The errors now occur in banks 23, 26, 27, 32, and 33. These banks are all located in array modules on the left side of the memory box. Therefore, it can be assumed that the faulty module is the control B module which is now in the left side of the box.

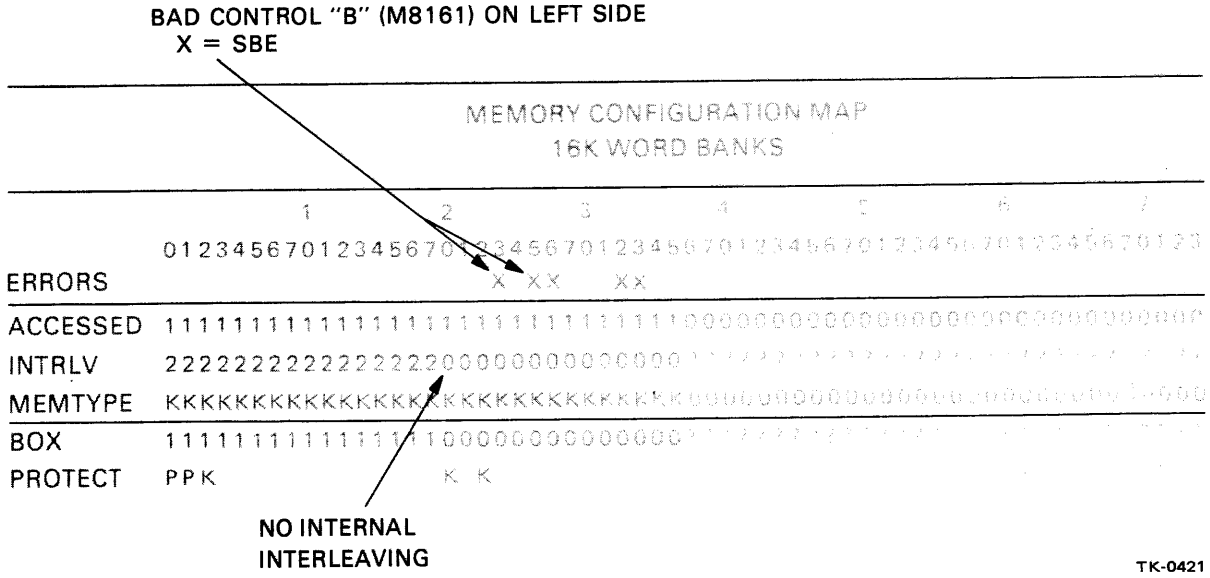


Figure 9-6 Diagnostic Configuration Map Example 6

9.2.4 Error Printout

The diagnostic program provides error printouts for each memory data error uncovered. The error printout is formatted as shown in Figure 9-7. The headings are defined as follows.

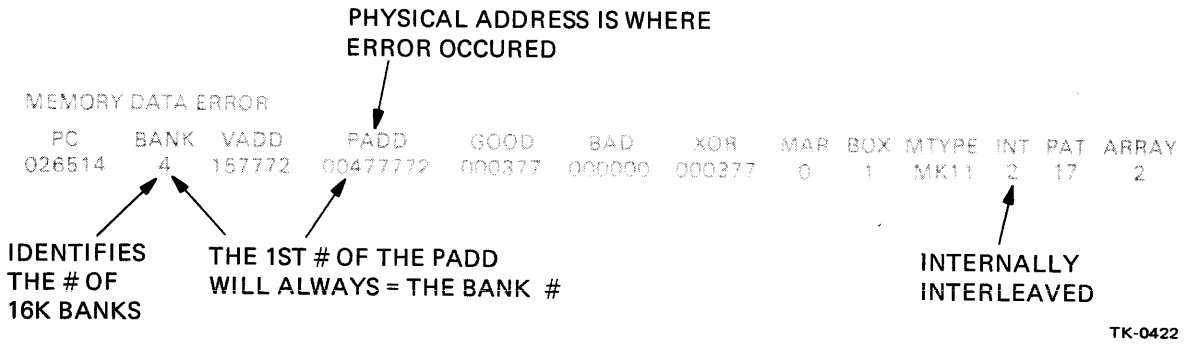


Figure 9-7 Error Printout

MEMORY PC	Program counter
BANK	16K bank in which error was found
VADD	Virtual address of error, always between 60000 and 157776 for maping purposes
PADD	Physical address in memory, bank number followed by physical address within bank
GOOD	Data pattern program expected to retrieve from memory location
BAD	Data actually read from memory
XOR	An exclusive ORing of the good and bad data to indicate which bits failed
MAR	Margin test number Margin = 0, 4, or 5, normal operation Margin = 2, early MDR load Margin = 3, late refresh
BOX	Box number corresponding to CSR address
MTYPE	Memory type, MK11 (MOS) or MJ11 (core)
INT	Number of ways interleaved
PAT	Test pattern number
ARRAY	Array module number that contains error

In the sample printout, an error was found while testing bank 4, physical address 477772. The program expected to read 000377 from that location but retrieved an all 0 data pattern. The printout points to array 2 as the array containing physical address 477772. There may be instances, however, when the number under the ARRAY heading points to a protected array slot if a single-bit error exists in the program space. An alternative method for finding the array using Figure 9-8 is suggested. This figure shows the correlation between physical addresses and arrays in the memory. In this example, using Figure 9-8, bank 4 is divided between array 2 and array 3. From the error printout, it is found that the box is internally interleaved (INT = 2). Since the physical address ends in 2, the array is on the right side of the box, or on the array 2 rather than array 3.

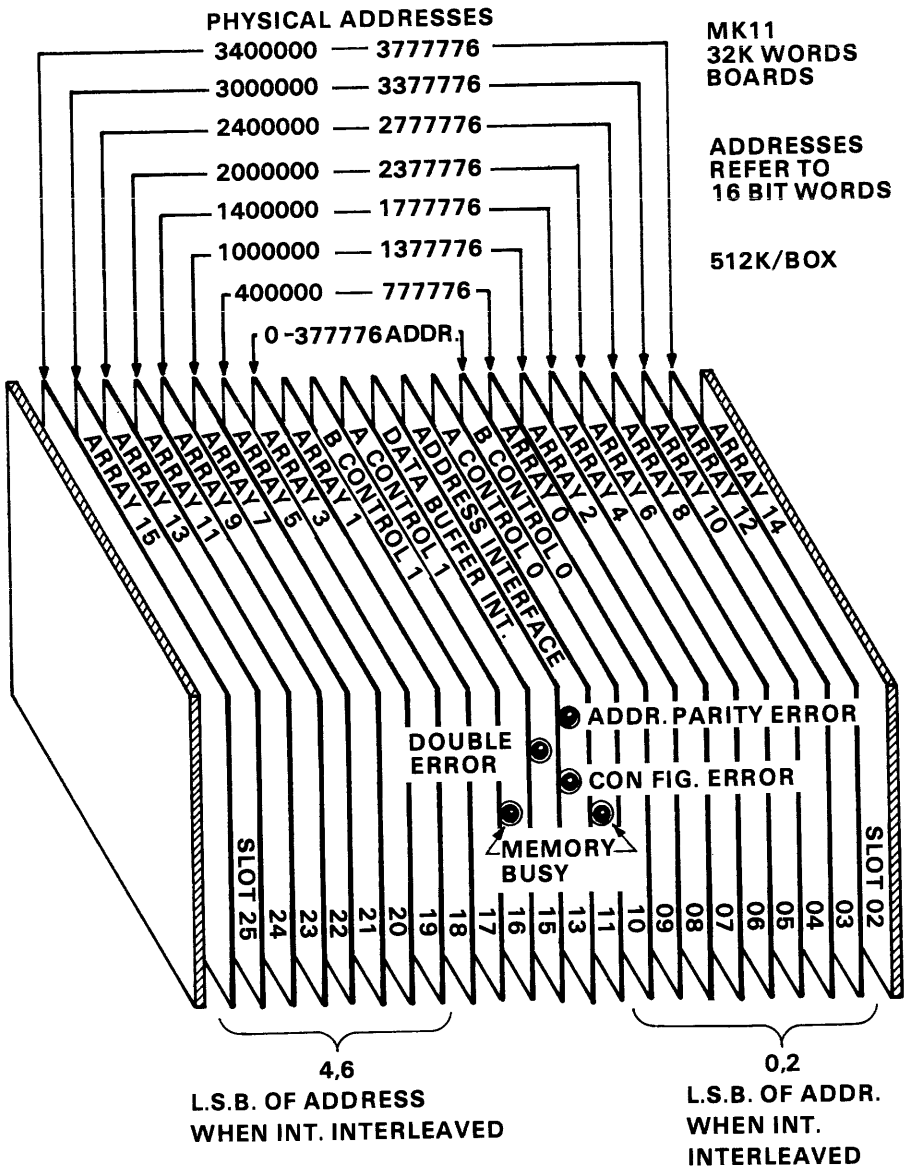


Figure 9-8 Relating an Array Number to a Physical Address (PADD)

9.2.5 Field Service Mode

The field service mode is entered by typing control F on the terminal. To execute any command, type the command and a carriage return. The default value for any carriage return not preceded by a number is 0. The commands are numbered as follows.

Field Service Mode Commands

0 Exit field service mode
1 Read CSR
2 Load CSR
3 Examine memory
4 Modify memory
5 Select bank, margin, and pattern
6 Type configuration map
7 Battery backup test
8 Sob-A-Long test
9 Super tight scope loop
10 Error summary
11 Refresh test

Command 0 (Exit Field Service Mode) - This command causes an exit from the field service mode. The diagnostic returns to the task it was executing prior to entering the field service mode (Control F).

Command 1 (Read CSR) - This command prints the contents of the CSR in octal (Figure 9-9). If there is more than one CSR, the terminal prints:

WHICH CSR (0-7).

Answer with the desired CSR number, 0 through 7.

Command 2 (Load CSR) - This command is used to load data into the memory's CSR from the terminal. If there is more than one CSR, the terminal prints:

WHICH CSR (0-7).

Answer with the desired CSR number, 0 through 7. The terminal then prints the contents of the CSR in octal, followed by:

FIRST CSR WORD.

Type, in octal, the new contents of the first CSR word. The terminal then prints:

2ND CSR WORD.

Enter the contents of the second CSR word, in octal. The new contents of the CSR is printed by the terminal.

Command 3 (Examine Memory) - This command allows the examination of any physical address. The terminal prints:

PHYSICAL ADDRESS (0-16777776).

Respond by typing the octal physical address. The contents of the address are then printed by the terminal.

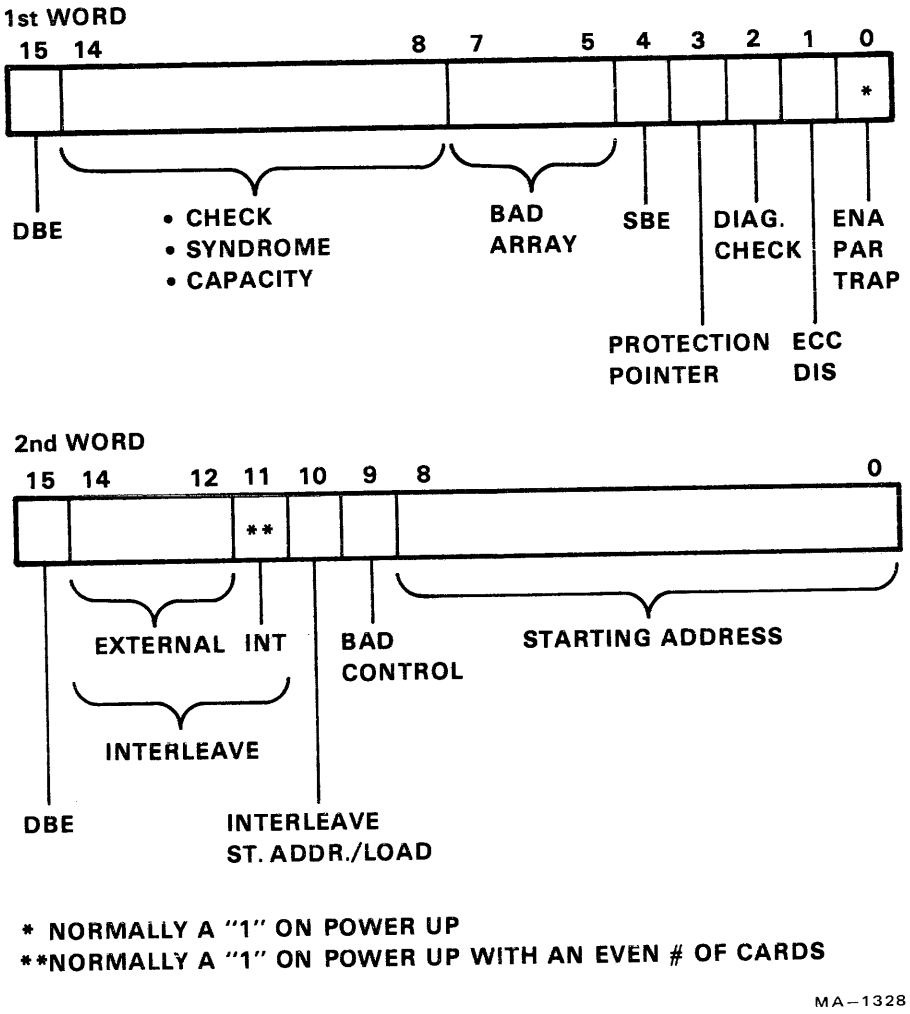


Figure 9-9 Control and Status Registers (CSRs)

Command 4 (Modify Memory) – This command allows the modification of any physical address. The terminal prints:

PHYSICAL ADDRESS (0–16777776).

Respond by typing the octal physical address. The terminal prints:

OLD DATA WAS

followed by the contents of the memory location and then the words

INPUT NEW DATA.

Respond by entering the new data, in octal. The terminal prints:

DATA IS NOW

followed by the new data just entered.

Command 5 (Select Bank, Margin, and Pattern) – This command runs any test pattern at any margin on any bank of memory. The test continues until stopped by pressing any key on the terminal. The terminal first prints:

BANK (0–167).

Respond with the bank number to be tested. The terminal then prints:

PATTERN (0–37).

Respond with the desired pattern number, 0 through 37_8. If pattern 0 is selected, the terminal prints:

PATTERN 0 DATA IS ?

The data entered (in octal) is written to and read from all locations in the specified bank. Refer to the diagnostic documentation for descriptions of all the test patterns. After entering the pattern number, the terminal prints:

MARGIN (0, 2, 3, 4, 5) ?

Respond by typing a margin number. Console switch 5 must be down to select margins.

0, 4, 5 = No margining
2 = Early MDR load
3 = Late refresh

When the margin number has been entered, the terminal prints:

TO ESCAPE TYPE ANY KEY !

The test on the bank runs until any terminal key is pressed.

Command 6 (Type Configuration Map) – This command prints the memory configuration map. See Paragraph 9.2.3.

Command 7 (Battery Backup Test) – This command is used to test the battery backup units which supply power for refreshing when the memory loses ac input power. The terminal prints:

REMOVE SYSTEM POWER FOR 10 SECONDS MAX !

If the control switch on the 861-D, E is placed in the REMOTE position, the console key can be used to power down and power up the memory for this test. Return the control switch to the LOCAL position after testing battery backup units. When the test is finished, the terminal prints:

TEST COMPLETE.

Command 8 (Sob-A-Long Test) – This command performs the sob-a-long test on all non-protected banks of memory. Each pass rings the bell on the terminal.

Command 9 (Super Tight Scope Loop) – This command enters a program loop in which data from the switch register is moved to a memory location and then moved from the memory to a display register. The terminal asks:

PHYSICAL ADDRESS.

Respond with the desired physical address, in octal. After entering the address, the terminal prints:

MARGIN (0,2,3,4,5) ?

Enter the margin number to be used with this test. The terminal returns with the message:

SWR → MEM, MEM → DISPLAY

which shows the data path. The program enters the loop and types:

TO ESCAPE TYPE ANY KEY.

The program remains in the loop until interrupted by typing any key on the terminal.

Command 10 (Error Summary) – This command types the number of passes made and the total number of errors per bank.

Command 11 (Refresh Test) – This command runs the refresh test on all non-protected bank. Each pass causes a bell at the terminal.

9.3 TROUBLESHOOTING

The most powerful tool available for troubleshooting the memory is the diagnostic program. However, there will be instances when faults in the memory will prevent running the diagnostic or booting the system. A troubleshooting flowchart is included (Figure 9-10) to direct troubleshooting efforts in order to isolate the problem. If the diagnostic program cannot be run, follow the suggestions in the flowchart. Take full advantage of the information given by the various fault and indicator lights; their locations are called out in Figure 9-8 for the memory box and Figure 9-11 for the box controller. If the power supply is suspected as the source of the fault, turn to Chapter 7. Chapter 7 contains procedures for checking the voltages and removal and replacement procedures for changing faulty power supply modules.

Sheet 1 of the flowchart seeks problems that prevent booting the system. Indicator lights and switch positions are checked to give clues to the source of the problem. The cabling in this memory is more complex than previous memory systems and should always be suspected as a probable cause of malfunctions. Memory problems also tend to be interactive. In memory systems with more than one memory box, concentrate troubleshooting efforts to one box at a time as in sheet 2 of the flowchart. Confusion can be minimized by uninterleaving the boxes to separate them. Turn all the external interleave switches to 0 and select the proper starting addresses as shown on the control panel decal. Boxes can be removed from the system simply by switching the box off-line at the box controller (except for the memory box which contains the bus terminators).

On sheet 3 of the flowchart, the fault has been isolated to one memory box. If the diagnostic still does not run at this point, the switch register can be used to test for the location of the error. When corrections to the system allow running the diagnostic program, run the program to locate any other errors, then reconnect all the boxes to the system and run the diagnostic again.

9.4 TEST PROCEDURE FOR ECC INITIALIZATION AND BOOT CHARACTERISTICS

The following procedure checks the memory's ECC initialization which writes all 0 data patterns into the arrays after a power-up boot operation. If power is lost to the memory, the data will remain in the memory for at least 5 minutes while the backup batteries supply power to refresh the MOS chips. Upon recovery from a power fail, the memory is not initialized, but retains the data stored previous to the failure. Perform this procedure if the memory fails the battery backup test in the field service mode (command 7) or if the batteries or power supply modules are installed or replaced.

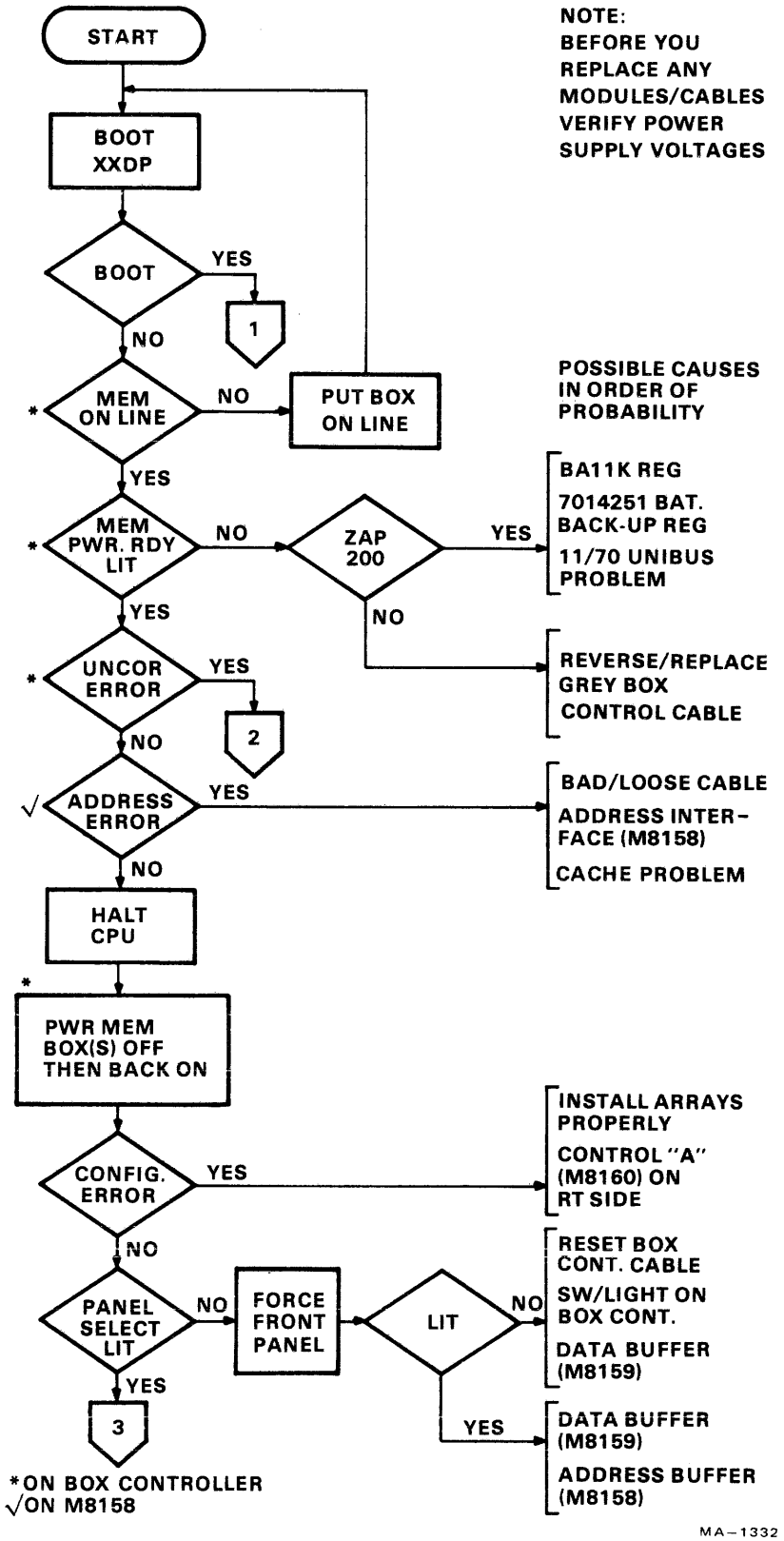


Figure 9-10 MK11 Troubleshooting Chart (Sheet 1 of 3)

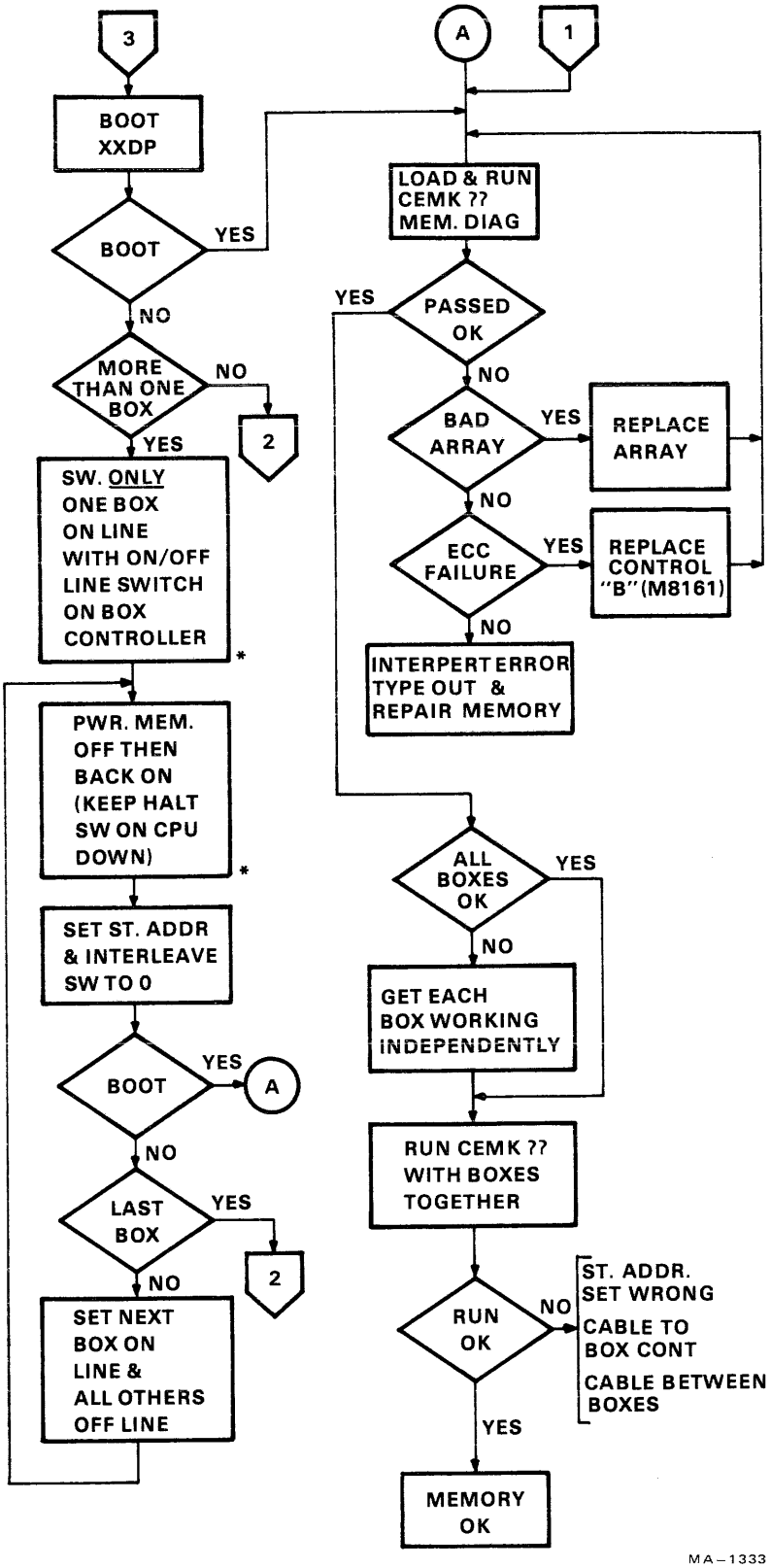


Figure 9-10 MK11 Troubleshooting Chart (Sheet 2 of 3)

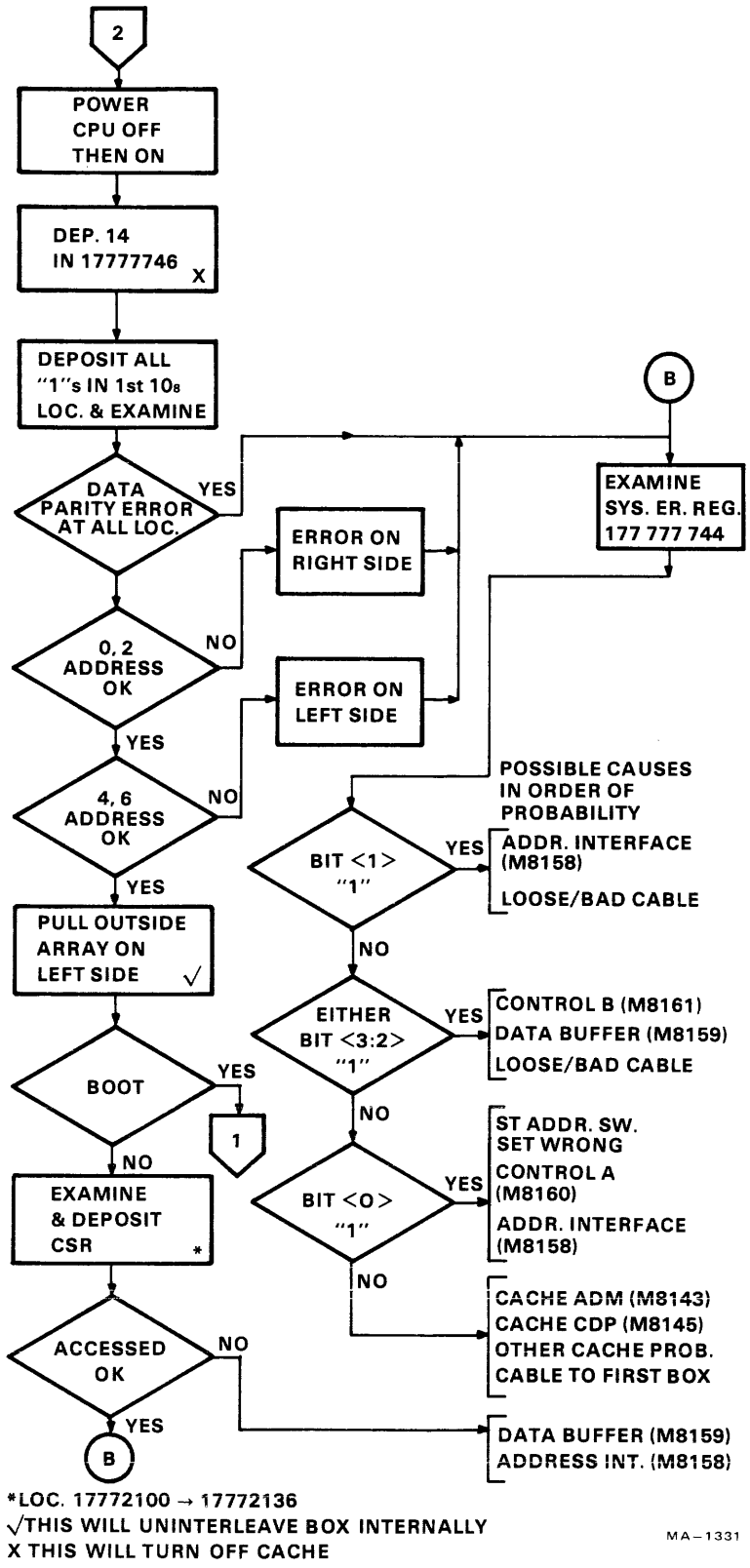


Figure 9-10 MK11 Troubleshooting Chart (Sheet 3 of 3)

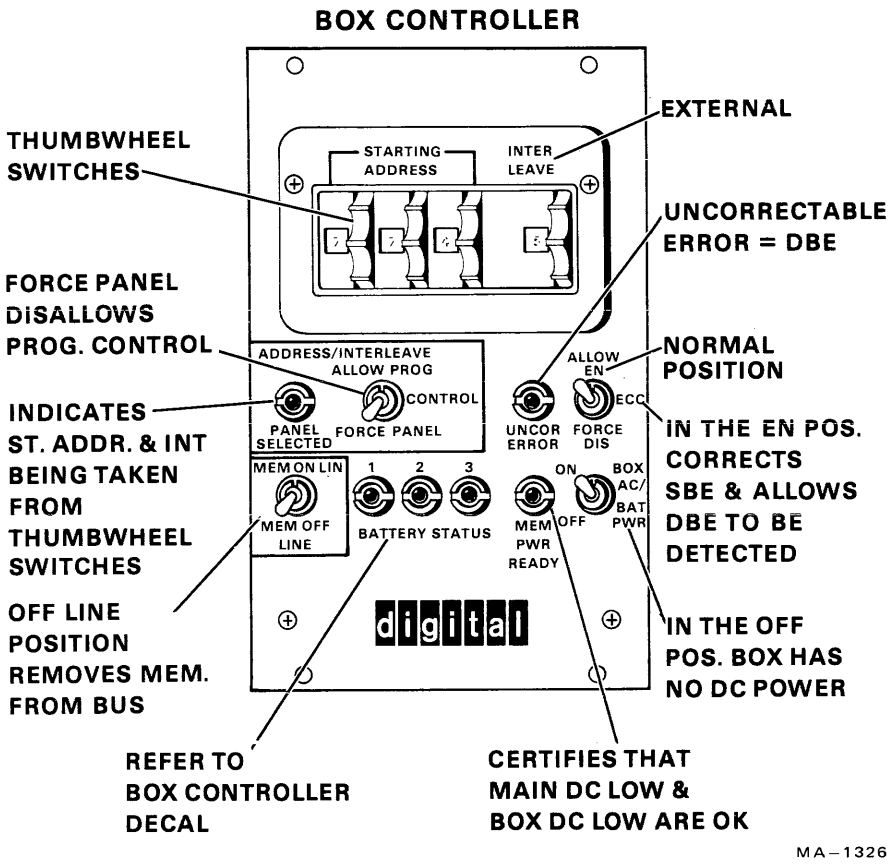


Figure 9-11 Box Controller

Checkout Procedure for Box ECC Initialization

1. Power box on, ensure battery backup (H775) units are on.
2. Examine locations $0–20_8$ for all 0s.
3. Deposit all 1s in locations $0–20_8$.
4. Examine locations $0–20_8$ for all 1s.
5. Place HALT ENABLE to HALT. (HALT switch will remain in HALT position for remainder of test.)
6. Turn memory box breaker off, then on.
7. Examine locations $0–20_8$ for all 1s.
8. Turn memory box breaker off; turn battery backup 1-A off.
9. Turn memory box breaker on; turn battery backup 1-A on.

10. Press START switch on PDP-11/70; load address 0.

11. Examine locations 0–20_8 with data below:

Address	0 = 0s
	2 = 0s
	4 = 1s
	6 = 1s
	10 = 0s
	12 = 0s
	14 = 1s
	16 = 1s

12. Deposit all 1s in locations 0–20_8

13. Turn memory box breaker to off position; turn battery backup 1-B to off position.

14. Turn memory box breaker to on position, turn battery backup 1-B to on position.

15. Press START switch on PDP-11/70; load address 0.

16. Examine locations 0–20_8 with data below:

Address	0 = 1s
	2 = 1s
	4 = 0s
	6 = 0s
	10 = 1s
	12 = 1s
	14 = 0s
	16 = 0s

17. Deposit all 1s in locations 0–20_8.

18. Turn memory box breaker to off position; turn battery backup 1-C to off position.

19. Turn memory box breaker to on position; turn battery backup 1-C to on position.

20. Press START switch on PDP-11/70; load address 0.

21. Examine locations 0–20_8 and check that all locations are 0s.

Checkout Procedure for Box BOOT Operation

1. Power box on, ensure battery backup (H775) units are on.

2. Get a 50_8 in the PDP-11/70 switches.

3. Place the HALT ENABLE switch to the ENABLE position. (HALT switch will remain in the ENABLE position for the remainder of the test.)

4. Turn memory box breaker off, then on.

5. Check physical address of the PDP-11/70, and ensure that the processor stopped at address 2_8.

6. Turn memory box breaker off; turn battery backup 1-A off.

7. Turn memory box breaker on; turn battery backup 1-A on.

8. Ensure that the PDP-11/70 BOOTS, and that the processor stops at the correct physical address, (50_8) loaded in the switches).

9. Turn memory box breaker off; turn battery backup 1-B off.

10. Turn memory box breaker on; turn battery backup 1-B on.

11. Ensure that the same results happen as in step 8.

12. Turn memory box breaker off; turn battery backup 1-C off.

13. Turn memory box breaker on; turn battery backup 1-C on.

14. Ensure that the same results happen as in step 8.

APPENDIX A
MOS CHIP DESCRIPTION

A.1 PHYSICAL DESCRIPTION

The MOS memory device used with the MS11-KE array modules is a 4096-bit, dynamic, random-access memory circuit. The circuit is packaged in a standard 16-pin DIP that provides high system bit density and is compatible with available automatic testing and insertion equipment. Figure A-1 is an outline drawing of the chip, showing pin connections. Table A-1 lists the chip supply voltages.

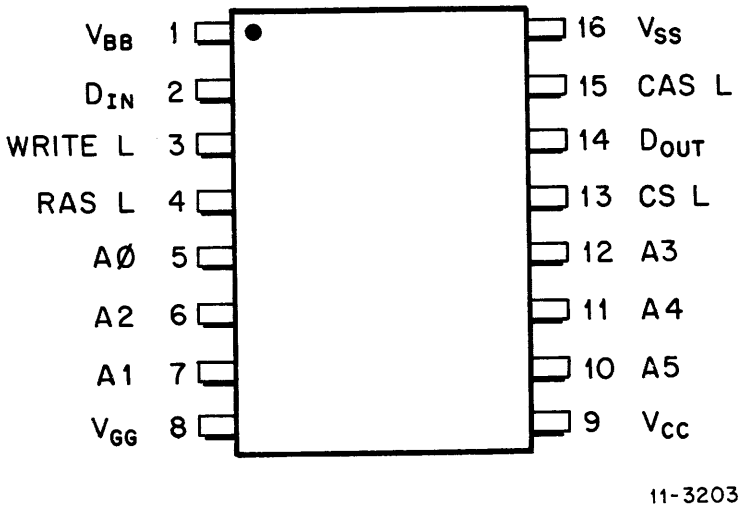


Figure A-1 MOS RAM Chip Pin Connections

Table A-1 Chip Supply Voltages

Voltage	Operation
VGG	+12 Vdc
VCC	+5 Vdc
VSS	Ground
VBB	-9 V/-5 V*

*Depending on chip type.

A.2 FUNCTIONAL DESCRIPTION

A functional block diagram of the chip is shown in Figure A-2. The 4096 storage locations are arranged in a 64-row by 64-column array. Thus, a cell location can be specified by a 6-bit row address and a 6-bit column address. Because address information is latched into on-chip registers, the chip can be driven by six address lines. The controller multiplexes 12 address bits, 6 at a time, onto the A0–A5 lines. The RAS L (Row Address Strobe) signal causes row address information to be latched into a 6-bit register, while the CAS L (Column Address Strobe) signal causes column address information, as well as the CS L (Chip Select) signal, to be latched into a 7-bit register. Enable signals applied to 1-of-64 decoders result in the selection of one of the 4096 cell locations for a data transfer.

A.2.1 The Cell Storage Element

A simplified representation of the chip is shown in Figure A-3. (All the switches are merely symbolic of more detailed chip operation.) The basic cell storage element is a capacitor; a charge voltage of 0–6 V represents logic 0, while a voltage of 6–12 V represents logic 1. Because the charge on the capacitor dissipates with time, it is continually refreshed so that the data it represents remains valid. Any read or write cycle results in a refresh of the data in the addressed locations. During such a cycle, the row address is latched first, and then the 1-of-64 decoder closes all the switches in the selected row. The charge voltage on each capacitor in the row is applied to a sense amplifier (SA), which refreshes the data by restoring the charge voltage to its original level. For example, the maximum charge voltage on a cell capacitor is 12 V, representing logic 1. When the cell is addressed, a portion of the full charge may have leaked off so that the voltage has decreased to, for example, 8 V. The SA forces the voltage back to its full-charge value of 12 V. Similarly, any voltage between 0 and 6 V is restored to a logic 0 level of 0 V.

A.2.2 Read, Write, and Refresh

After the data in the selected row is accessed and refreshed, the column address is latched: the multiplexer selects one of the 64 columns, and the amplified charge voltage on a single capacitor is applied to point A in Figure A-3. If the cycle is a read, the data is strobed into the tri- state output latch and remains valid until the next time CAS L goes low. If the cycle is a write, the input buffer/latch drives point A, overriding the SA output and charging the selected cell capacitor. Since a cell may be addressed infrequently, if at all, during normal read/write operations, a specially timed refresh cycle is carried out at regular intervals. In the MK11 memory, such a cycle occurs approximately every 25 μs. A different row address is supplied by the controller during each refresh cycle so that the data in all 64 row addresses is refreshed about every 2 ms. The refresh operation is similar to a read or write cycle, i.e., the row address is latched and the data in each cell of the row is refreshed. The column address strobe is inhibited during refresh cycles. The CS L signal is disabled so that neither the input circuit nor the output circuit is enabled. The output latch will go to its high impedance state, ensuring that power consumption is minimal.

A.2.3 Timing

The timing of both a read cycle and a write cycle is illustrated in Figure A-4. The RAS L signal starts the timing cycle internally. To reduce the overall system power, RAS L is decoded in the MS11-K logic and supplied to only the selected bank of chips. The CAS L signal is supplied to all chips, but chips that do not receive a RAS L signal will go to their high-impedance output states.

If data is to be read from the addressed location, the WRITE L signal must be high and the CS L signal must be asserted. The data is strobed into the output latch/buffer at access time (after RAS L is asserted) and remains valid until CAS L goes negative during a subsequent timing cycle. A write cycle requires that the WRITE L signal go low before access time; the WRITE L command is accepted by the chip only if CS L has been asserted. The data on the D IN line is strobed into an input latch by the negative transition of the CAS L signal. Note that the output latch/buffer goes to logic 1 at access time.

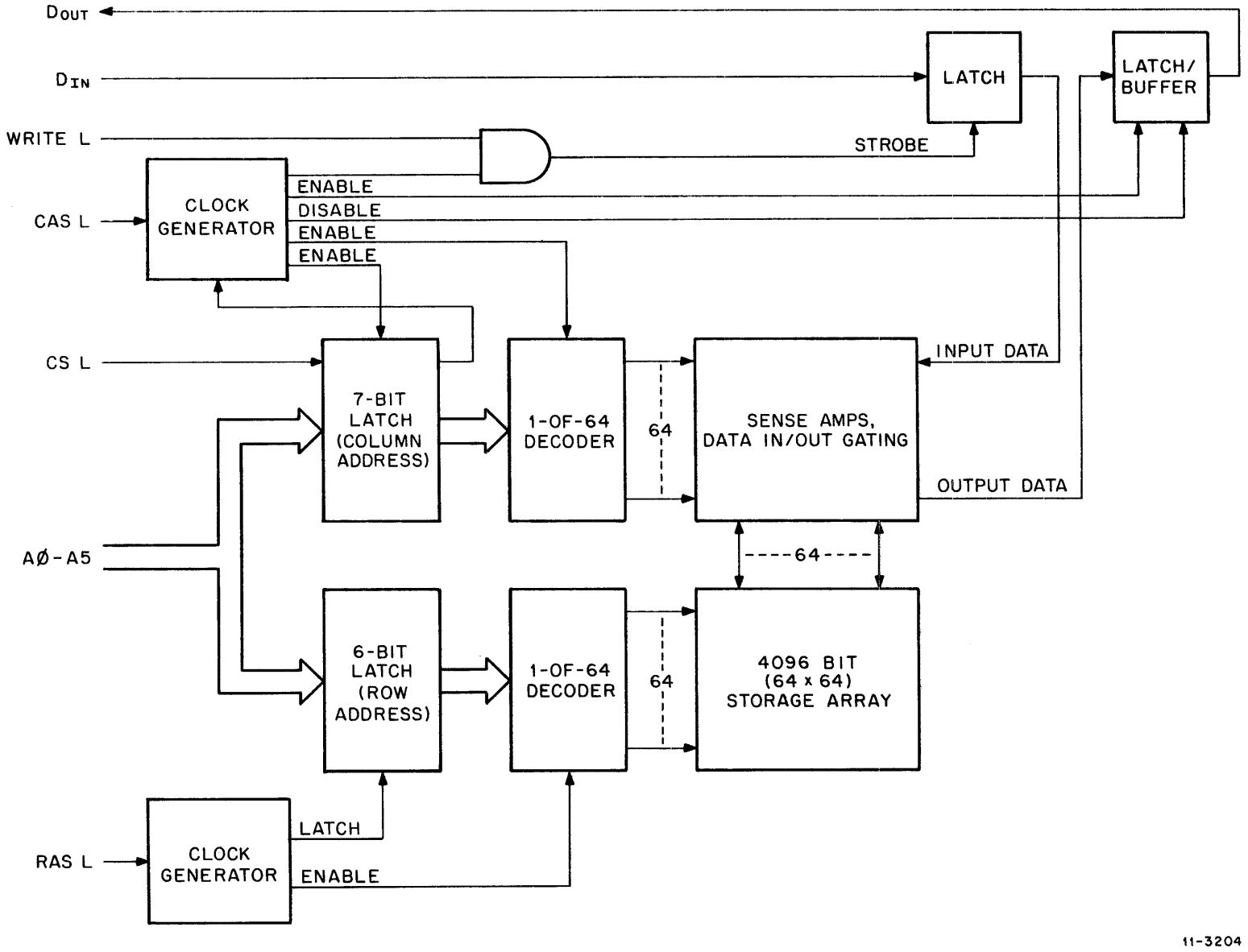


Figure A-2 4096 × 1-Bit MOS Chip Block Diagram

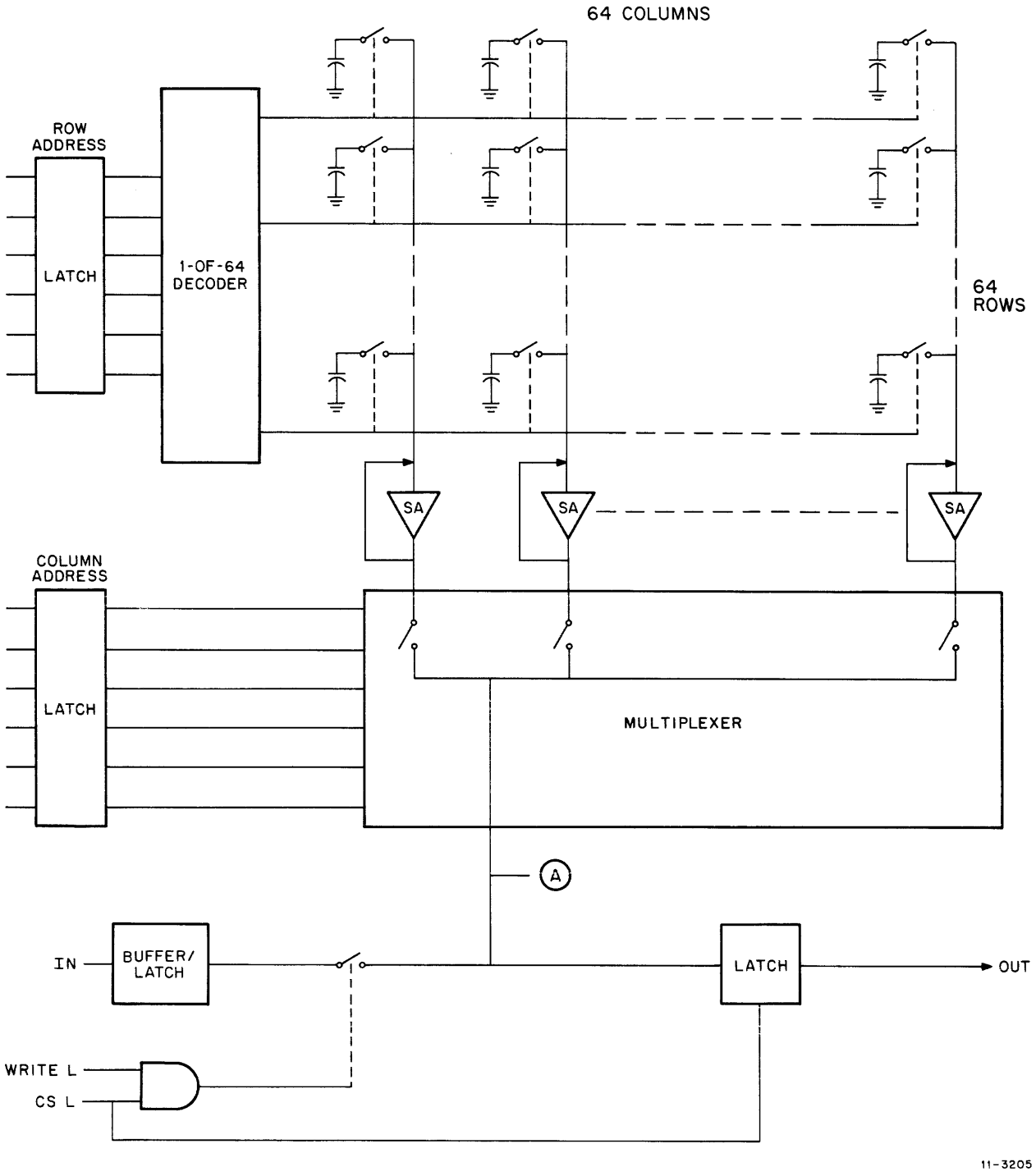


Figure A-3 MOS Chip, Simplified Data Gating

READ CYCLE (minimum timing)

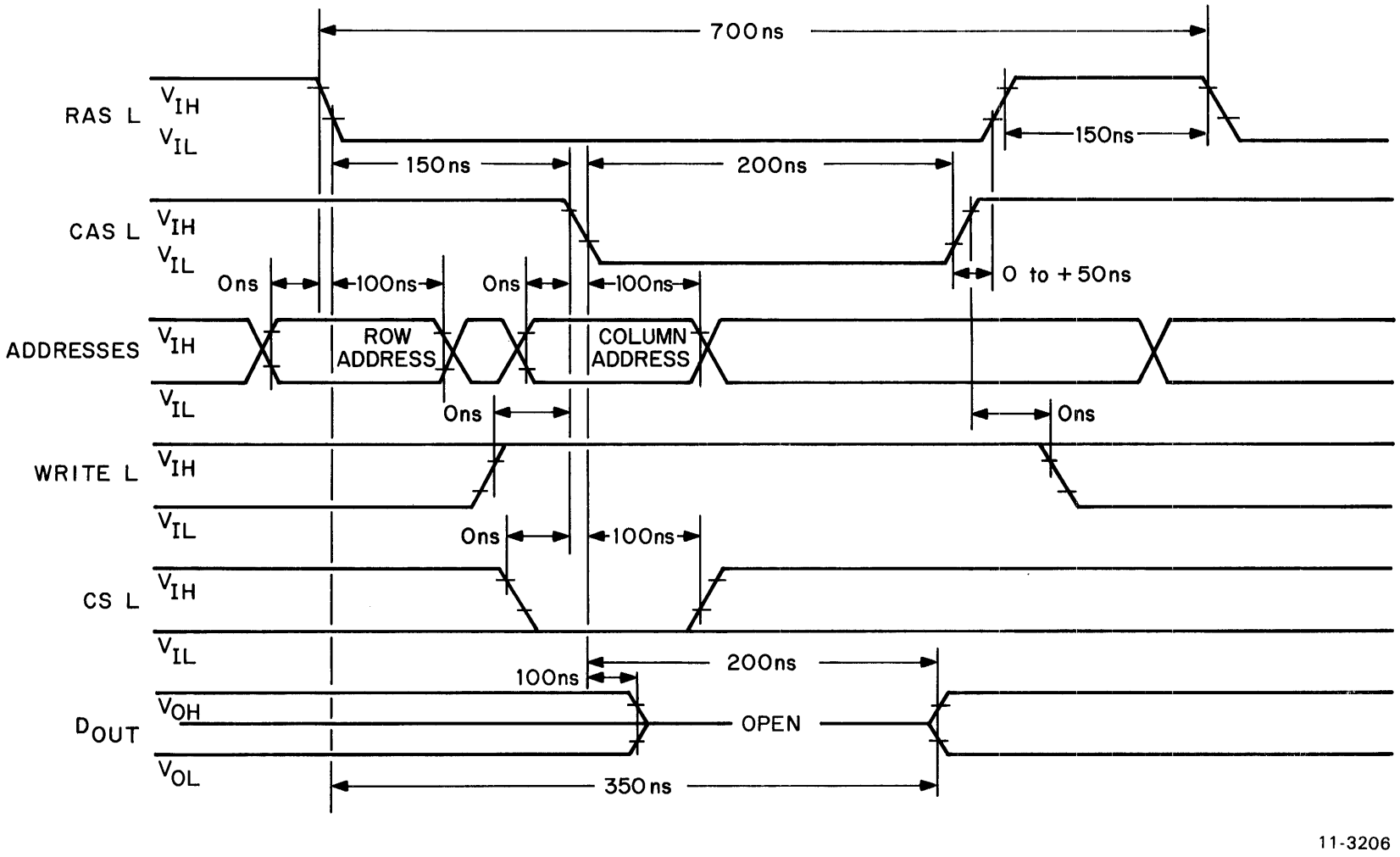


Figure A-4 Chip Read-Write Timing (Sheet 1 of 2)

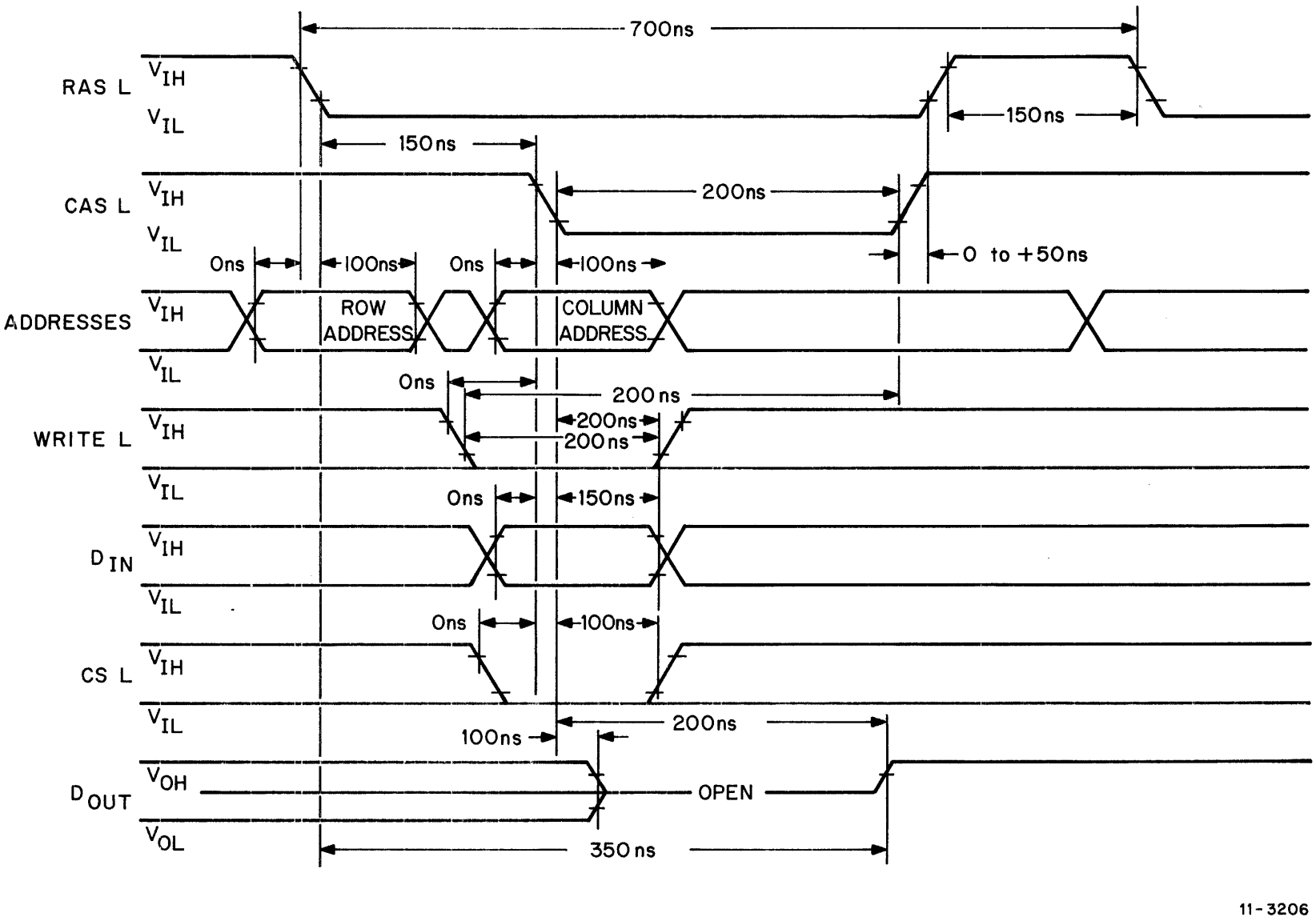
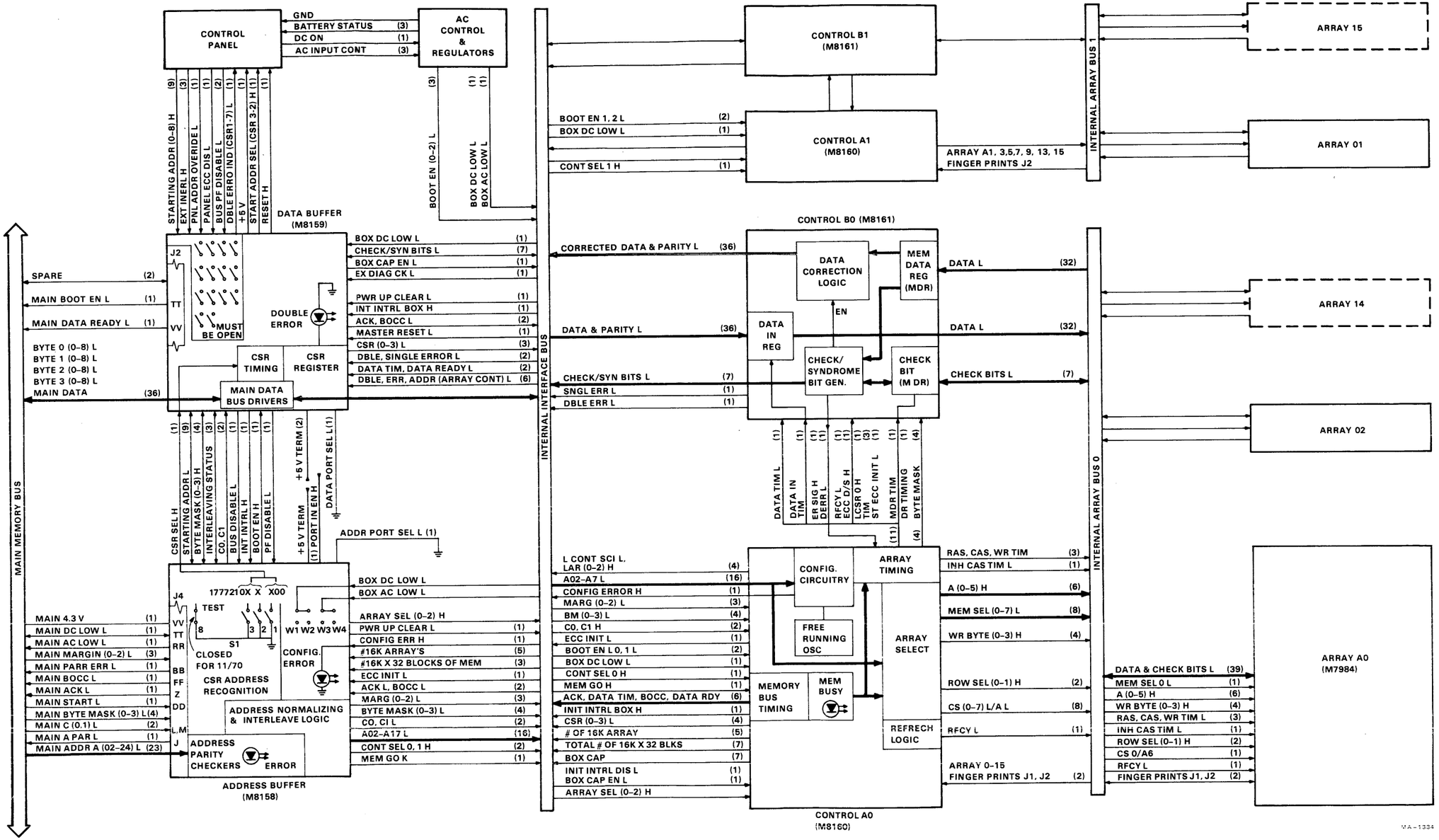


Figure A-4 Chip Read-Write Timing (Sheet 2 of 2)

APPENDIX B
MK11 MEMORY SYSTEM BLOCK DIAGRAM


CONTROL PANEL
GND
BATTERY STATUS (3)
DC ON (1)
AC INPUT CONT (3)
AC CONTROL & REGULATORS
STARTING ADDR (0–8) H (9)
EXT INERL H (3)
PNL ADDR OVERIDE L (1)
PANEL ECC DIS L (1)
BUS PF DISABLE L (2)
DBLE ERRO IND (CSR1-7) L (1)
+5 V (1)
START ADDR SEL (CSR 3-2) H (1)
RESET H (1)
BOOT EN (0–2) L (3)
BOX DC LOW L (1)
BOX AC LOW L (1)
DATA BUFFER (M8159)
J2
TT
VV
MUST BE OPEN
DOUBLE ERROR
SPARE (2)
MAIN BOOT EN L (1)
MAIN DATA READY L (1)
BYTE 0 (0–8) L
BYTE 1 (0–8) L
BYTE 2 (0–8) L
BYTE 3 (0–8) L
MAIN DATA (36)
CSR TIMING
CSR REGISTER
MAIN DATA BUS DRIVERS
BOX DC LOW L (1)
CHECK/SYN BITS L (7)
BOX CAP EN L (1)
EX DIAG CK L (1)
PWR UP CLEAR L (1)
INT INTRL BOX H (1)
ACK, BOCC L (2)
MASTER RESET L (1)
CSR (0–3) L (3)
DBLE, SINGLE ERROR L (2)
DATA TIM, DATA READY L (2)
DBLE, ERR, ADDR (ARRAY CONT) L (6)
CSR SEL H (1)
STARTING ADDR L (9)
BYTE MASK (0–3) H (4)
INTERLEAVING STATUS (3)
C0, C1 (2)
BUS DISABLE L (1)
INT INTRL H (1)
BOOT EN H (1)
PF DISABLE L (1)
+5 V TERM (2)
+5 V TERM (1) PORT IN EN H
DATA PORT SEL L (1)
ADDR PORT SEL L (1)
J4
VV
TT
RR
BB
FF
Z
DD
L,M
J
1777210X X X00
TEST
S1
CLOSED FOR 11/70
CSR ADDRESS RECOGNITION
CONFIG. ERROR
W1 W2 W3 W4
ADDRESS NORMALIZING & INTERLEAVE LOGIC
ADDRESS PARITY CHECKERS
ERROR
ADDRESS BUFFER (M8158)
MAIN 4.3 V (1)
MAIN DC LOW L (1)
MAIN AC LOW L (1)
MAIN MARGIN (0–2) L (3)
MAIN PARR ERR L (1)
MAIN BOCC L (1)
MAIN ACK L (1)
MAIN START L (1)
MAIN BYTE MASK (0–3) L (4)
MAIN C (0.1) L (2)
MAIN A PAR L (1)
MAIN ADDR A (02–24) L (23)
BOX DC LOW L (1)
BOX AC LOW L (1)
ARRAY SEL (0–2) H
PWR UP CLEAR L (1)
CONFIG ERR H (1)
#16K ARRAY'S (5)
#16K X 32 BLOCKS OF MEM (3)
ECC INIT L (1)
ACK L, BOCC L (2)
MARG (0–2) L (3)
BYTE MASK (0–3) L (4)
C0, C1 L (2)
A02–A17 L (16)
CONT SEL 0, 1 H (2)
MEM GO K (1)
MAIN MEMORY BUS
INTERNAL INTERFACE BUS
CONTROL B1 (M8161)
CONTROL A1 (M8160)
BOOT EN 1, 2 L (2)
BOX DC LOW L (1)
CONT SEL 1 H (1)
ARRAY A1, 3,5,7, 9, 13, 15
FINGER PRINTS J2
INTERNAL ARRAY BUS 1
ARRAY 15
ARRAY 01
CONTROL B0 (M8161)
CORRECTED DATA & PARITY L (36)
DATA CORRECTION LOGIC
MEM DATA REG (MDR)
EN
DATA L (32)
DATA & PARITY L (36)
DATA IN REG
CHECK/ SYNDROME BIT GEN.
CHECK BIT (M DR)
CHECK BITS L (7)
CHECK/SYN BITS L (7)
SNGL ERR L (1)
DBLE ERR L (1)
ARRAY 14
ARRAY 02
DATA TIM L (1)
DATA IN TIM (1)
ER SIG H (1)
DERR L (1)
RFCY L (1)
ECC D/S H (1)
LCSR 0 H TIM (1)
ST ECC INIT L (1)
MDR TIM (1)
DR TIMING (3)
BYTE MASK (4)
INTERNAL ARRAY BUS 0
L CONT SCI L, LAR (0–2) H (4)
A02–A7 L (16)
CONFIG ERROR H (1)
MARG (0–2) L (3)
BM (0–3) L (4)
C0, C1 H (2)
ECC INIT L (1)
BOOT EN L 0, 1 L (2)
BOX DC LOW L (1)
CONT SEL 0 H (1)
MEM GO H (1)
ACK, DATA TIM, BOCC, DATA RDY (6)
INIT INTRL BOX H (1)
CSR (0–3) L (4)
OF 16K ARRAY (5)
TOTAL # OF 16K X 32 BLKS (7)
BOX CAP (7)
INIT INTRL DIS L (1)
BOX CAP EN L (1)
ARRAY SEL (0–2) H
CONFIG. CIRCUITRY
ARRAY TIMING
FREE RUNNING OSC
ARRAY SELECT
MEMORY BUS TIMING
MEM BUSY
REFRECH LOGIC
RAS, CAS, WR TIM (3)
INH CAS TIM L (1)
A (0–5) H (6)
MEM SEL (0–7) L (8)
WR BYTE (0–3) H (4)
ROW SEL (0–1) H (2)
CS (0–7) L/A L (8)
RFCY L (1)
ARRAY 0–15
FINGER PRINTS J1, J2 (2)
CONTROL A0 (M8160)
DATA & CHECK BITS L (39)
MEM SEL 0 L (1)
A (0–5) H (6)
WR BYTE (0–3) H (4)
RAS, CAS, WR TIM L (3)
INH CAS TIM L (1)
ROW SEL (0–1) H (2)
CS 0/A6 (1)
RFCY L (1)
FINGER PRINTS J1, J2 (2)
ARRAY A0 (M7984)
MA-1334

APPENDIX C
MK11 MEMORY TIMING DIAGRAMS

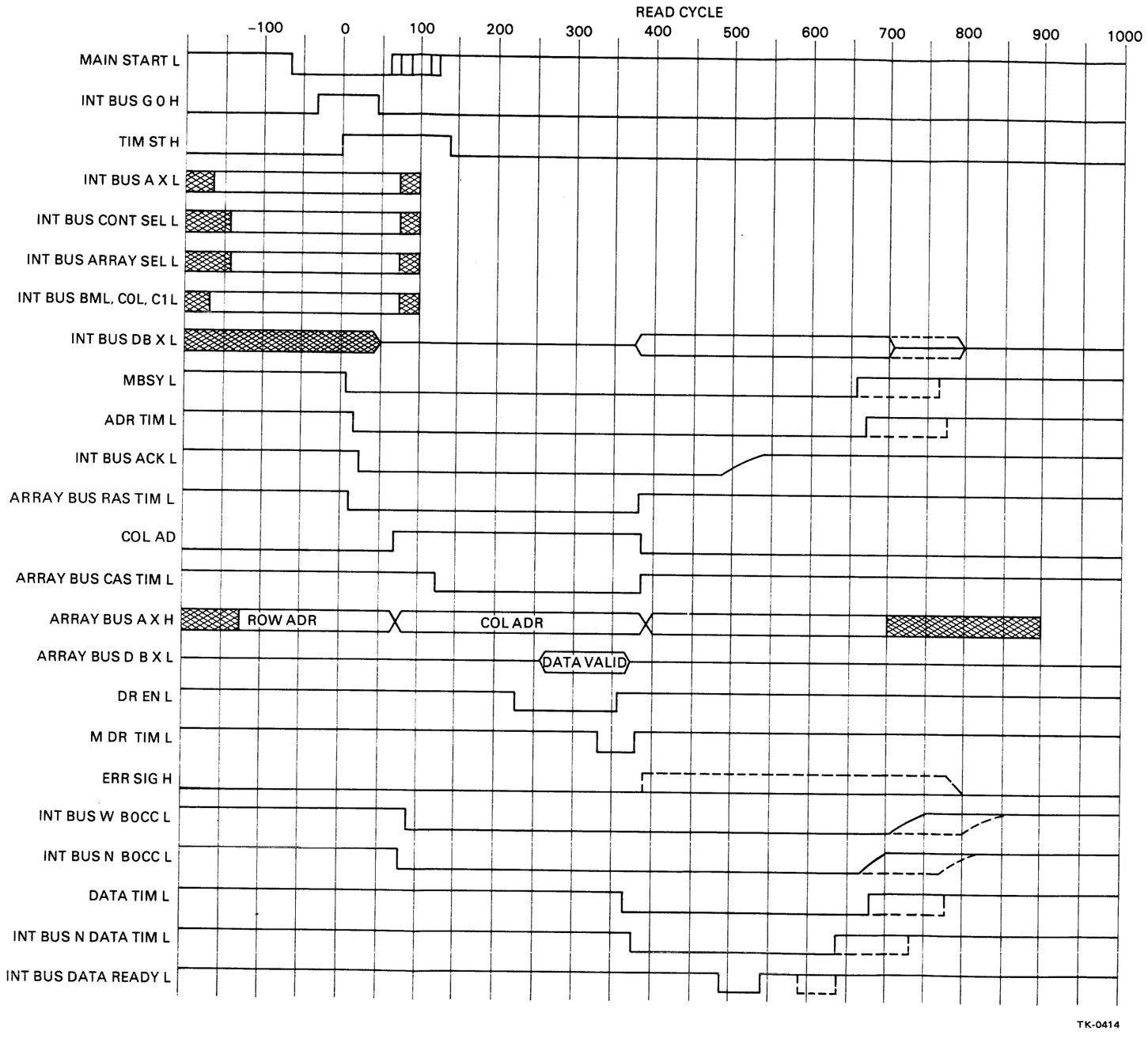


Figure C-1 Read Cycle Timing Diagram

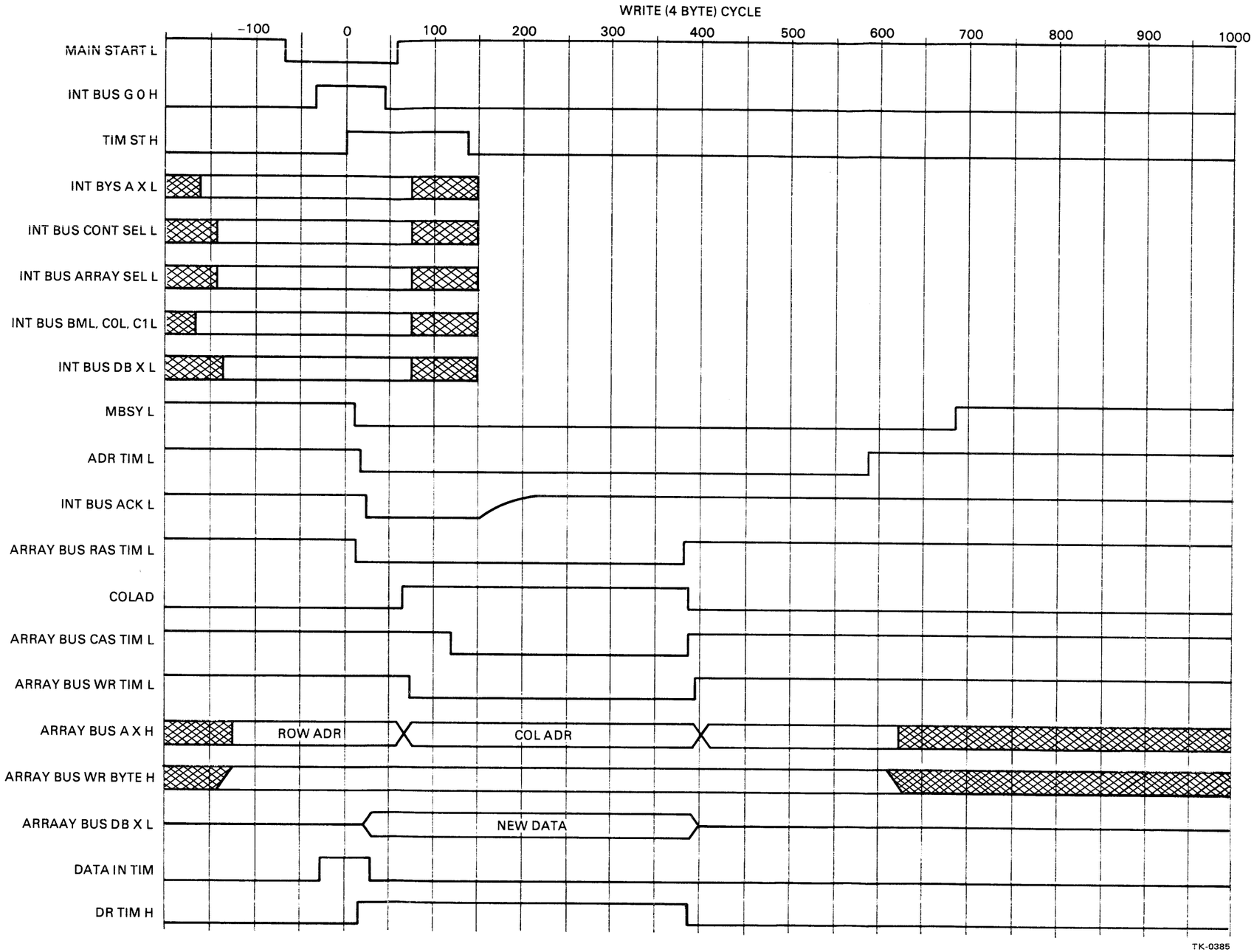


Figure C-2 Four-Byte Write Cycle Timing Diagram

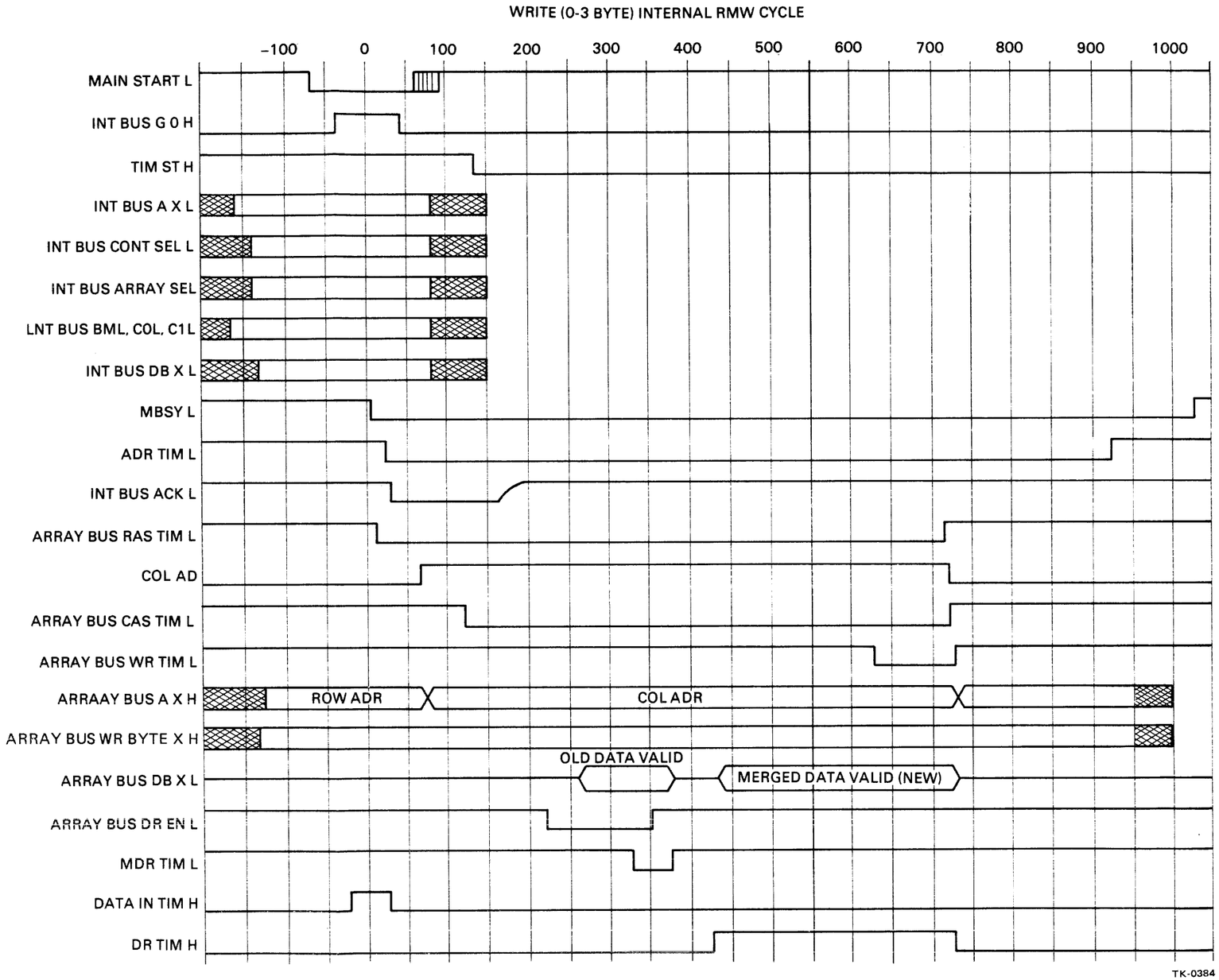


Figure C-3 One-to-Three Byte Write Cycle Timing Diagram

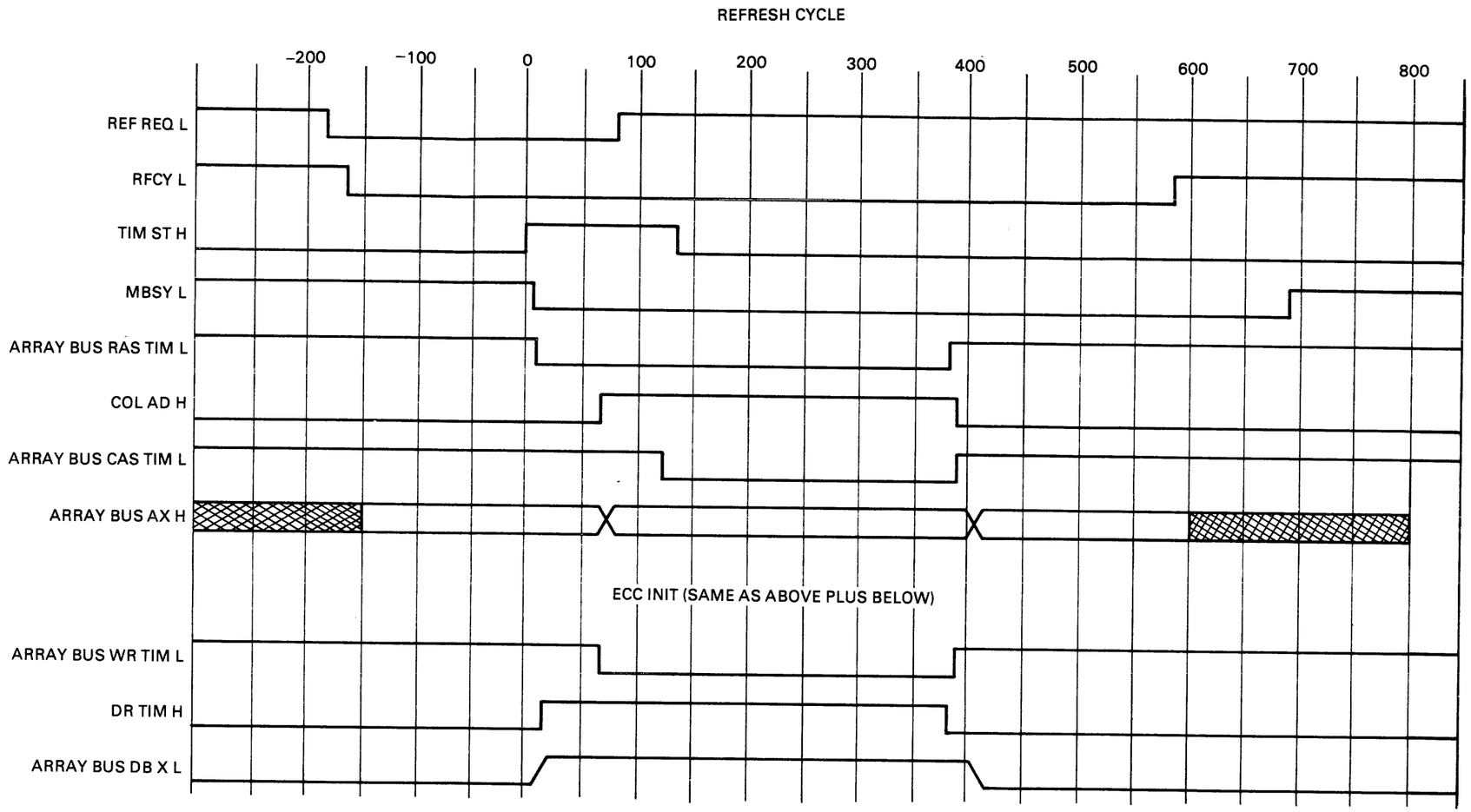


Figure C-4 Exchange Cycle Timing Diagram (Sheet 1 of 2)

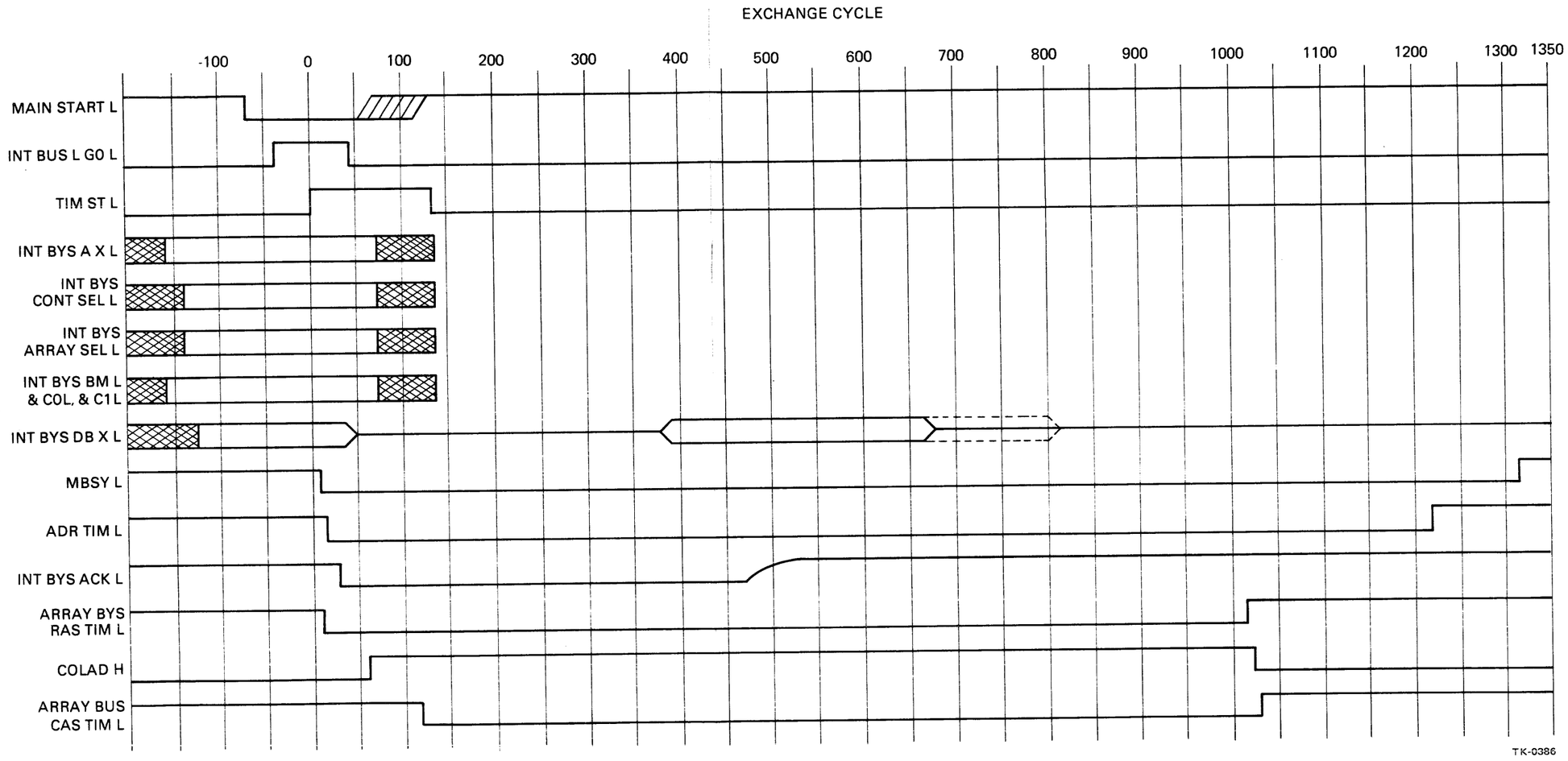


Figure C-4 Exchange Cycle Timing Diagram (Sheet 2 of 2)

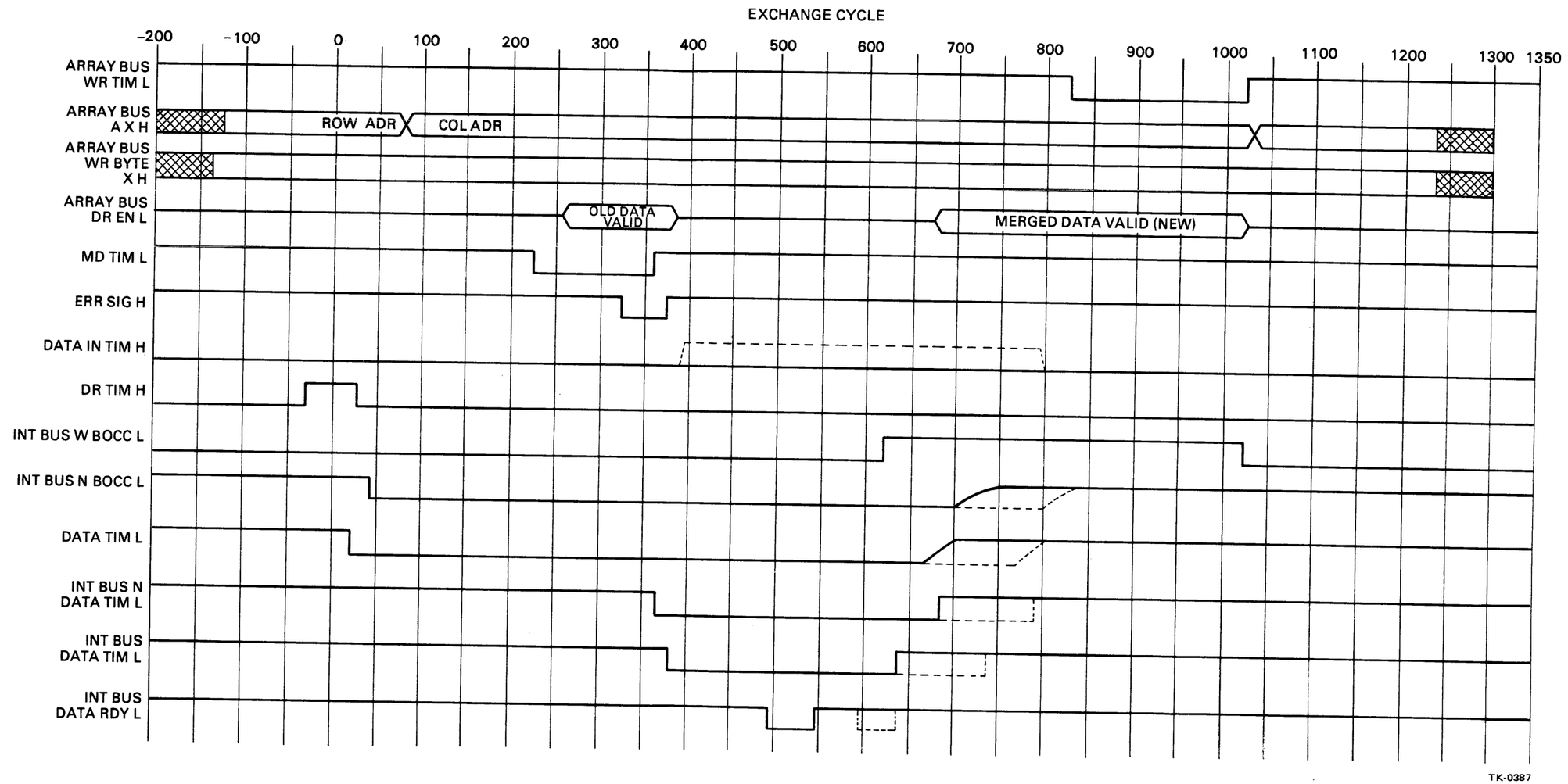


Figure C-5 Refresh Cycle and ECC Initialization Cycle Timing Diagrams

MK11 MOS MEMORY
TECHNICAL MANUAL
EK-0MK11-TM-001

Reader's Comments

Your comments and suggestions will help us in our continuous effort to improve the quality and usefulness of our publications.

What is your general reaction to this manual? In your judgment is it complete, accurate, well organized, well written, etc.? Is it easy to use? _____

_____

_____

_____

What features are most useful? _____

_____

_____

_____

What faults or errors have you found in the manual? _____

_____

_____

_____

Does this manual satisfy the need you think it was intended to satisfy? _____

Does it satisfy *your* needs? _____ Why? _____

_____

_____

_____

☐ Please send me the current copy of the *Technical Documentation Catalog*, which contains information on the remainder of DIGITAL's technical documentation.

Name _____ Street _____
Title _____ City _____
Company _____ State/Country _____
Department _____ Zip _____

Additional copies of this document are available from:

Digital Equipment Corporation
444 Whitney Street
Northboro, Ma 01532
Attention: Communications Services (NR2/M15)
Customer Services Section

Order No. EK-0MK11-TM-001

— — — — — — — — — — — — Fold Here — — — — — — — — — — —

— — — — — — — — — Do Not Tear - Fold Here and Staple — — — — — — — — —

FIRST CLASS
PERMIT NO. 33
MAYNARD, MASS.

BUSINESS REPLY MAIL
NO POSTAGE STAMP NECESSARY IF MAILED IN THE UNITED STATES

Postage will be paid by:

Digital Equipment Corporation
Technical Documentation Department
Maynard, Massachusetts 01754

digital equipment corporation

Printed in U.S.A.