PDP-11/94-E System
User and Maintenance Guide

Order Number EK-PDP94-MG-001

Digital Equipment Corporation

September 1990

FCC NOTICE: The equipment described in this manual generates, uses, and may emit radio frequency energy. The equipment has been type tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such radio frequency interference when operated in a commercial environment. Operation of this equipment in a residential area may cause interference, in which case the user at his own expense may be required to take measures to correct the interference.

This document was prepared and published by Educational Services Development and Publishing, Digital Equipment Corporation.

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About This Guide

This guide provides installation, operation, and maintenance information on the PDP-11/94-E computer system. Procedures for upgrading a PDP-11/84 to a PDP-11/94 and a detailed functional description of the standard PDP-11/94-E system are also included. This guide is intended for Digital Customer Services personnel and qualified self-maintenance customers.

This guide contains the following information:

Chapter 1, System Overview	Includes a general description of the PDP-11/94-E system and its components and explains the system features. This chapter also lists the available system configurations, system specifications, and related documentation.
Chapter 2, Unpacking and Installing	Explains how to prepare the site for installation and how to unpack, install, and check the system.
Chapter 3, Operation	Describes the front panel controls and indicators and explains how to modify the system using the menus.
Chapter 4, Configuration	Describes the location of the modules in the backplane. Chapter 4 also provides the module switch and jumper information you need to configure the modules for specific requirements.
Chapter 5, Functional Description	Describes each of the major logic elements of the PDP-11/94-E systems.
Chapter 6, Diagnostics and Troubleshooting	Contains information on troubleshooting, interpreting error codes and messages, and using the diagnostic LED indicators on the modules.
Chapter 7, Removal and Replacement Procedures	Describes how to remove and replace the field replaceable units (FRUs). At the beginning of this chapter there is a list of FRUs for the PDP-11/94-E system.
Chapter 8, Upgrading a PDP-11/84 System	Provides the removal and installation procedures required to upgrade the PDP-11/84-A and PDP-11/84-E systems.
Appendix A, Setup Parameters Worksheet	Contains a worksheet for you to record the setup parameters selected in the EEPROM.
Appendix B, Backplane Pin Assignments	Contains diagrams of the backplane pin assignments.
Appendix C, Optional Battery Backup Unit	Contains the installation information for the optional H7231 battery backup unit used in the PDP-11X94-E and PDP-11W94-E systems.
Appendix D, PDP-11/94 Hardware/Software Differences	Describes the differences between the UNIBUS power-up protocol for the PDP-11/94-E and other PDP-11 systems.
Appendix E, Optional Expander Cabinet	Contains installation information for the optional expansion cabinet.

Appendix F, CPU Instruction Timing	Describes the method of calculating the execution time for CPU instructions.
Appendix G, Floating-Point Instruction Timing	Contains information necessary to calculate the floating-point instruction timing.

Conventions

The following conventions are used in this guide:

Convention	Meaning
Warning	Provides information to prevent personal injury.
Caution	Provides information to prevent damage to equipment or software.
Note	Provides general information about the current topic.
Keyboard function keys	Are enclosed in a box ( ). For example, the carriage return key is represented as Return.
Screen display examples	The text you enter is in **boldface** type.
Bits	Are shown in angle brackets (<>). Two numbers separated by a colon indicate a set of bits, or bit field. For example, <15:08> stands for bits 15 through 8.
❶	Refers to a number in a black circle within a screen display or example.

Some functions may be labeled differently depending on your keyboard. If you have a question, refer to your terminal user's guide.

1
System Overview

1.1 Introduction

The PDP-11/94-E system is a high-performance computer containing a KDJ11-E CPU module with the following features:

- DCJ-11 microprocessor
- Two or four Mbyte parity memory
- Time of year (TOY) clock
- Seven asynchronous serial line units (SLUs)
- Console/Serial Line Unit port
- Floating point accelerator (FPJ11)

The processor runs the PDP-11 instruction set. The system operates on Digital's 18-bit UNIBUS with a 22-bit memory addressing capability.

1.2 System Components

The system block diagram for the PDP-11/94-E products is shown in Figure 1–1. The kernel system consists of:

- One KDJ11-E (M8981) processor module
- One KTJ11-B (M8191) UNIBUS adapter module (UBA)
- One UNIBUS terminal module (M9302)
- One Minimum load module (M9713)
- One power supply
- One Console/serial line unit (SLU) panel
- One Alternate power source (APS) module (M9714)
- One CPU backplane assembly
- One front panel assembly
- One cabinet power controller
- Three fans

The modules communicate through the high-speed private memory interconnect (PMI) bus using 22-bit address and 16-bit data lines.

There are eight SLUs, one of which is the console SLU.

The KTJ11-B UBA interfaces with the PMI bus and the UNIBUS. The UBA module supports all address and data communications between the processor memory and all UNIBUS peripherals (options). In addition, the UBA serves as a terminator for the CPU end of the UNIBUS. Table 1–1 specifies the system variations.

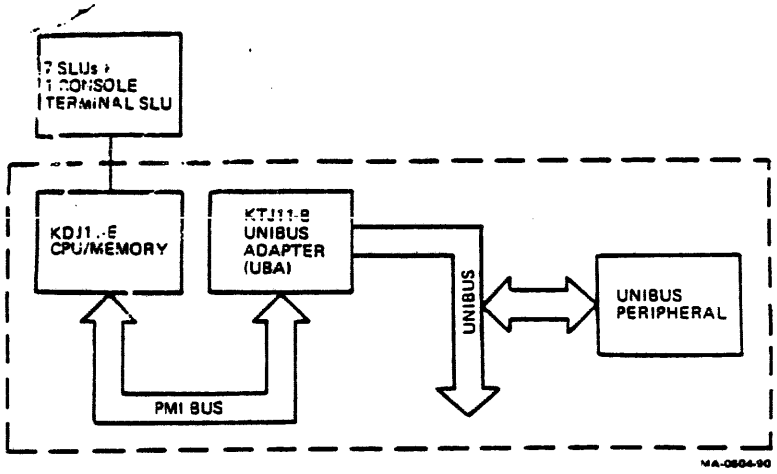


Figure 1–1 PDP-11/94-E Simplified Block Diagram

Table 1–1 PDP-11/94-E Product Variations

Variation	Description
120 Vac Systems	
PDP-11/94-EC	Includes KDJ11-EA CPU module (two Mbytes) and KTJ11-B UBA module.
PDP-11/94-EE	Includes KDJ11-EB CPU module (four Mbytes) and KTJ11-B UBA module.
PDP-11X94-EC,EE	PDP-11/94-EC or PDP-11/94-EE mounted in an H9642 (single-width, 42-inch-high cabinet).
PDP-11W94-EC,EE	PDP-11/94-EC or PDP-1194-EE mounted in an H9645 (42-inch-high wide-body cabinet).
240 Vac Systems	
PDP-11/94-ED	Includes KDJ11-EA CPU module (two Mbytes) and KTJ11-B UBA module.
PDP-11/94-EF	Includes KDJ11-EB CPU module (four Mbytes) and KTJ11-B UBA module.
PDP-11X94-ED,EF	PDP-11/94-ED or PDP-11/94-EF mounted in an H9642 (single-width, 42-inch-high cabinet).
PDP-11W94-ED,EF	PDP-11/94-ED or PDP-11/94-EF mounted in an H9645 (42-inch-high wide-body cabinet).

1.2.1 KDJ11-E Processor Module (M8981)

The KDJ11-E processor module (M8981) is a quad CPU module with the complete functionality of a PDP-11 processor. The module features:

- DCJ-11 microprocessor
- Floating-point accelerator (FPJ11)
- 22-bit memory management
- Programmable line frequency clock
- Console serial line unit
- Seven SLUs
- Boot and diagnostic ROMs
- TOY clock
- Two or four Mbytes onboard parity memory
- Console programmable setup features
- Comprehensive self-test capability
- LED status indicator

1.2.2 KTJ11-B UNIBUS Adapter Module (M8191)

The KTJ11-B UNIBUS adapter (M8191) is a hex module that interfaces the KDJ11-E processor with the UNIBUS. The module features:

- UNIBUS mapping
- Four M9312-compatible boot sockets

1.2.3 UNIBUS Terminator Module (M9302)

The UNIBUS terminator (M9302) is a resistive network with a characteristic impedance of 120 ohms. The module terminates one end of the UNIBUS and provides the SACK turnaround feature.

1.2.4 Minimum Load Module (M9713)

The minimum load module (MLM) provides a 2.75A load on +5V and a 750mA load on -15V to ensure that the minimum load requirements of the power supply are met.

1.2.8 CPU Backplane Assembly

The CPU backplane assembly is a 9-module slot backplane as shown in Figure 1–2.

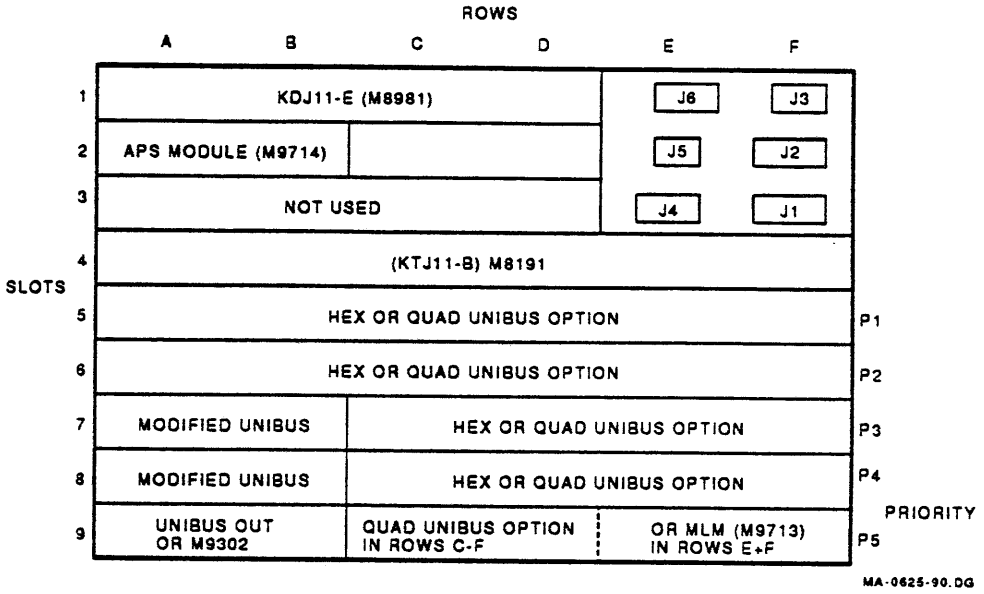


Figure 1–2 Backplane Assembly

Table 1–2 describes the slot functions of the CPU backplane assembly.

Table 1–2 CPU Backplane Assembly Slot Functions

Slots	Function
1 through 4	Dedicated to the system kernel.
5 through 8	Support hex or quad small peripheral controllers (SPCs).
7 and 8	Modified UNIBUS device (MUD) slots.
9	Supports only quad SPC option modules.

Backplane NPG jumper functions for slots 5 through 9 are implemented by replaceable links located on side two (bottom) of the backplane.

1.2.9 Front Panel Assembly

The front panel assembly includes:

- Switches and indicators for status display and operator control of the system
- A keylock rotary switch that allows you to select one of four power states

- A toggle switch that allows you to select system restart, run, or halt modes
- Three LEDs display the system status
- A status display

1.2.10 Cabinet Power Controller

The PDP-11X94-E and PDP-11W94-E cabinet contains either an 877-DB power controller for 120 Vac operation or an 877-F controller for 240 Vac operation.

The unit controls all ac power entering the cabinet. It provides primary power for all the power supplies and the two ac outlets located in the top peripheral enclosure.

1.2.11 Cooling

Each product is cooled by three fans mounted behind the card cage. The fans draw air through the front bezel, and a plenum directs the air horizontally through the card cage and power supply, and out the rear of the box.

1.2.12 Additional Expansion Options

The system supports the following options:

- H7231-H, cabinet battery backup unit for PDP-11X94-E system
- H7231-J, cabinet battery backup unit for PDP-11W94-E and PDP-11/94-E box systems
- DD11-CK, 4-slot expansion backplane
- DD11-DK, 9-slot expansion backplane

1.2.13 System Configuration

The system is available in three configurations:

- **PDP-11/94-E**—A kernel system box configuration packaged in a 26.7 centimeter (10.5 inch) rack mountable enclosure (Figure 1–3).

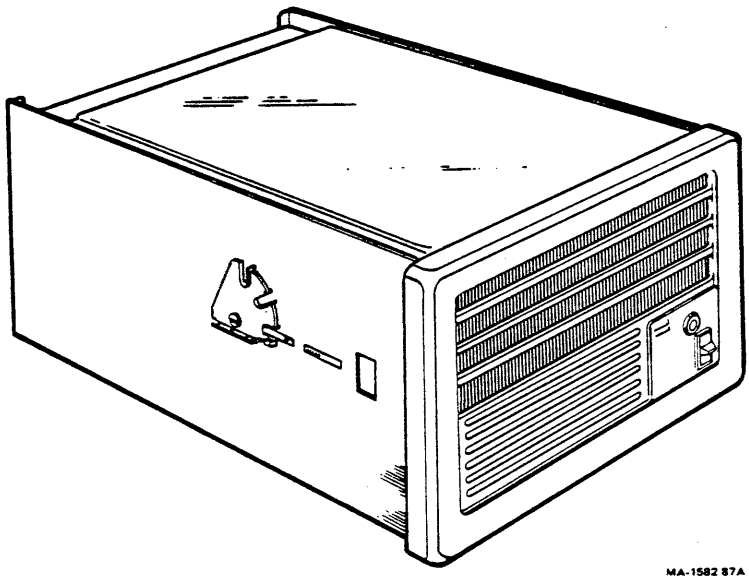


Figure 1–3 PDP-11/94-E Kernel System

- **PDP-11X94-E**—A kernel system configuration packaged in a 105.7 centimeter (42 inch) high cabinet (Figure 1–4). The top portion of the cabinet provides a 26.7 centimeter (10.5 inch) enclosure for installing peripherals.

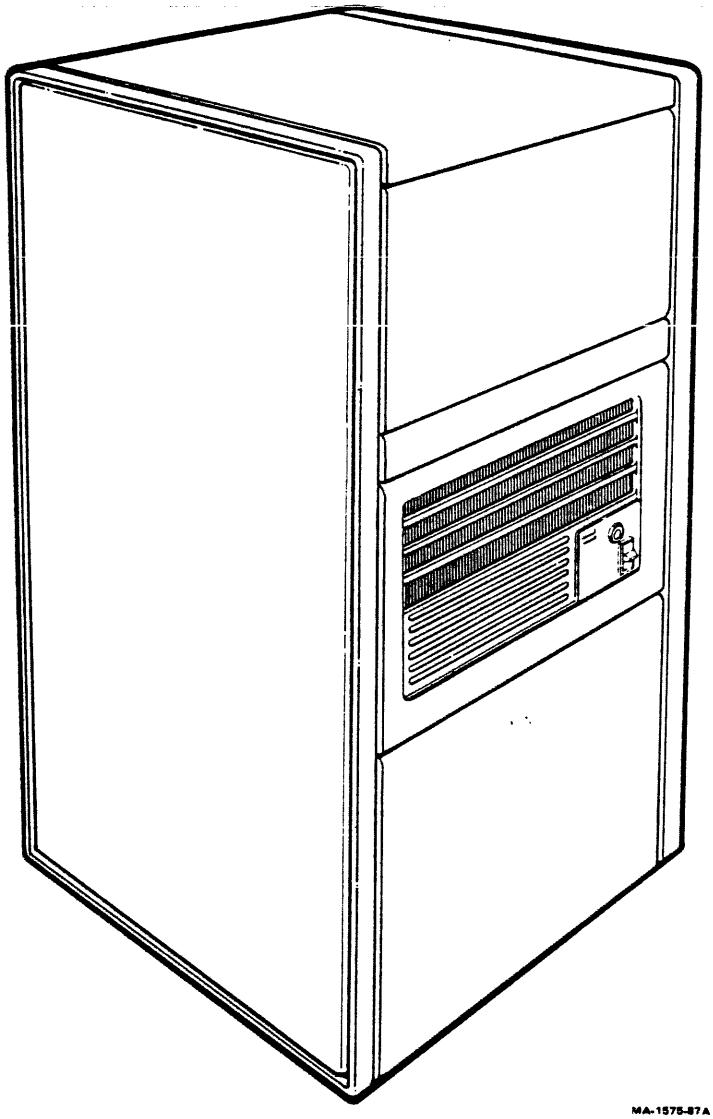


Figure 1–4 PDP-11X94-E Cabinet System

- **PDP-11W94-E**—A kernel system configuration packaged in a 105.7 centimeter (42 inch) high, wide-body cabinet (Figure 1–5). The top and bottom portion of the cabinet provides a 26.7 centimeter (10.5 inch) enclosure for installing peripherals.

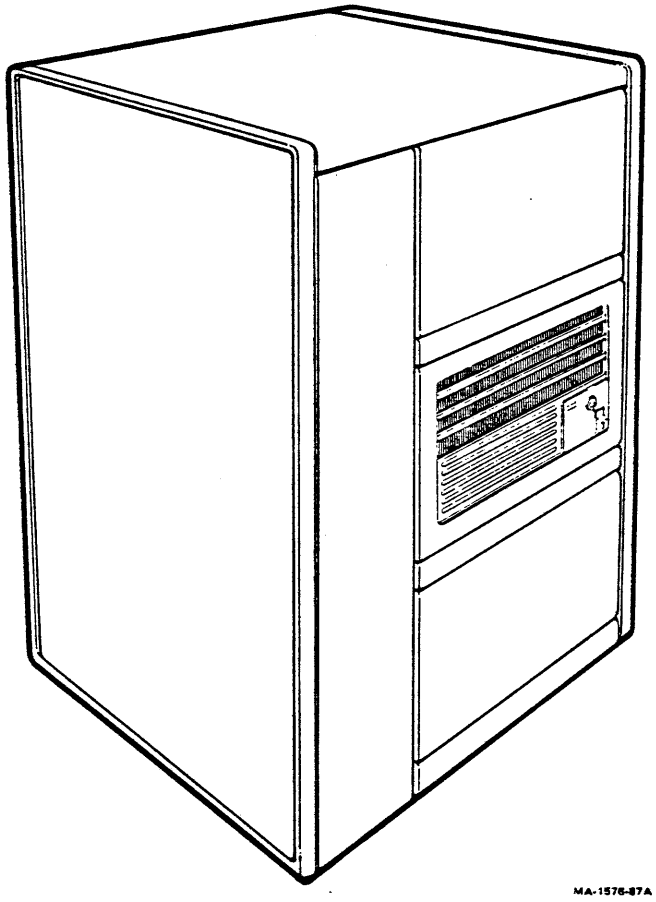


Figure 1–5 PDP-11W94-E Wide-Body Cabinet System

1.3 System Specifications

Tables 1–3 through 1–4 list the PDP-11/94-E system specifications. Supported peripheral device specifications are included in the user's guide for each device.

Table 1–3 lists the PDP-11/94-E environmental requirements.

Table 1–3 PDP-11/94-E Environmental Requirements

Condition	Operating	Nonoperating
Temperature range*	5° to 50°C (41° to 122°F)	-40° to 66°C (-40° to 151°F)
Relative humidity	10% to 95%	Less than 10% to 95%
Maximum altitude	2.4 km (8000 ft)	4.9 km (16,000 ft)
Maximum heat dissipation	3750 BTU	N/A
Acoustics		
—LNPE	6.8 B	N/A
—LPA	56 dB	N/A

*Reduce the temperature specification by 1.8° C (1° F) for each 1000 m (3300 ft) above sea level.

Table 1–4 lists the PDP-11/94-E electrical requirements.

Table 1–4 PDP-11/94-E Electrical Requirements

Parameter	120 V	240 V
Voltage range	90 to 128 Vac	180 to 256 Vac
Power phase	Single	Single
Nominal frequency	60 Hz	50 Hz
Frequency range	47 to 63 Hz	47 to 63 Hz
Maximum current	15 A	7.5 A
Inrush current	270 A	150 A
Power factor	Greater than 0.6	Greater than 0.6
Maximum power consumption	1100 W	1100 W
NEMA receptacle	5-20R	6-15R

Table 1–5 lists the PDP-11/94-E environmental requirements.

Table 1–5 PDP-11X94-E and PDP-11W94-E Environmental Requirements

Condition	Operating	Nonoperating
Temperature range*	10° to 40°C (50° to 104°F)	-40° to 66°C (-40° to 151°F)
Relative humidity	10% to 90%	Less than 10% to 95%
Maximum altitude	2.4 km (8000 ft)	4.9 km (16,000 ft)
Maximum Heat dissipation	3750 BTU	N/A
Acoustics		
LNPE	6.8 B	N/A
LPA	56 dB	N/A

*Reduce the temperature specification by 1.8° C (1° F) for each 1000 m (3300 ft) above sea level.

Table 1–6 lists the PDP-11/94-E electrical requirements.

Table 1–6 PDP-11X94-E and PDP-11W94-E Electrical Requirements

Parameter	120 V	240 V
Voltage range	90 to 128 Vac	180 to 256 Vac
Power phase	Single	Single
Nominal frequency	60 Hz	50 Hz
Frequency range	47 to 63 Hz	47 to 63 Hz
Nominal current	24 A	12 A
In rush current	270 A	150 A
Power factor	Greater than 0.6	Greater than 0.6
Maximum power consumption*	1728 W	1728 W
NEMA receptacle	L5-30R	6-15R

*Based on a fully loaded power controller, may not represent a typical system.

1.4 Related Documents

Table 1–7 lists documents that contain information related to the PDP-11/94-E or its operating systems.

Table 1–7 Related Documents

Title	Order Number
PDP-11/94-E Field Maintenance Print Set	MP-02637-01
H7204-C Field Maintenance Print Set	MP-01948-01
877 Field Maintenance Print Set	MP-01598-01
PDP-11/94-E Illustrated Parts Breakdown	EK-1194E-IP
PDP-11 UNIBUS Processor Handbook	EB-26077-41
PDP-11 Architecture Handbook	EB-23657-18
DCJ11 Microprocessor User Guide	EK-DCJ11-UG
KDJ11-E CPU Module User Guide	EK-KDJ11E-UG-001 Available 12/90
H7231-A Battery Backup Unit Users Guide	EK-H7231-UG
Supermicrosystems Handbook	EB-27713-41
Chipkit Handbook	EK-01387-92
Communications Handbook	EB-30066-42
Terminals and Printers Handbook	EB-23909-54
PDP-11 Software Handbook	EB-25398-41
RSX-11 Handbook	EB-25742-41
RSTS/E Handbook	EJ-23534-18
DD11-DK General Purpose UNIBUS Backplane Technical Manual	EK-DD11D-TM-001

1.4.1 Digital Personnel Ordering Information

Additional copies of this document and printed copies of the documents listed in Table 1–7 can be obtained from:

Digital Equipment Corporation
10 Forbes Road
Northboro, Massachusetts 01532
ATTN: Printing and Circulation Services (NR03/AW5)
Customer Services Section

1.5 Customer Ordering Information

Forward purchase orders for documentation and spare parts to:

Digital Equipment Corporation
Post Office Box CS2008
Nashua, New Hampshire 03061

2
Unpacking and Installing

2.1 General

This chapter describes how to prepare the site for installation, how to unpack, install, and check out the PDP-11/94-E system. Be sure the site conforms to the environmental, electrical, and physical requirements described in this chapter.

If you are upgrading a PDP-11/84 system, go to Chapter 8.

2.2 Site Considerations

The PDP-11/94-E, PDP-11X94-E, and PDP-11W94-E systems are designed for use primarily in a computer room rather than in an office. The three factors you need to consider when preparing the site are system location, environmental and electrical requirements.

NOTE
Digital recommends that the system be installed by a Digital Customer Services Engineer.

2.2.1 Physical Requirements

When selecting a location for the PDP-11/94-E, be sure there is enough room in the area where the system is to be unpacked, then remove the system from its shipping container. Allow adequate space around the cabinet for air circulation and servicing. Use the following guidelines for spacing requirements:

- Leave a minimum of 2 meters (6.5 feet) at the front of the system so the system box can be extended.
- Leave a minimum of 1 meter (3 feet) at the rear of the system so the rear door of the cabinet can be opened or removed.
- Allow 1 meter (3 feet) on each side of the system to remove the side panels of the cabinet or service the system box.

The PDP-11/94-E system comes with a 7.6 meters (25 feet) BC22D-25 EIA serial line unit (SLU) cable for connecting the system to a terminal. There is also a 2.74 meters (9 feet) power cord for connecting the system to an ac outlet.

2.2.2 System Dimensions

Figure 2–1 shows the dimensions of the unpacked PDP-11/94-E system and the dimensions of the shipping container.

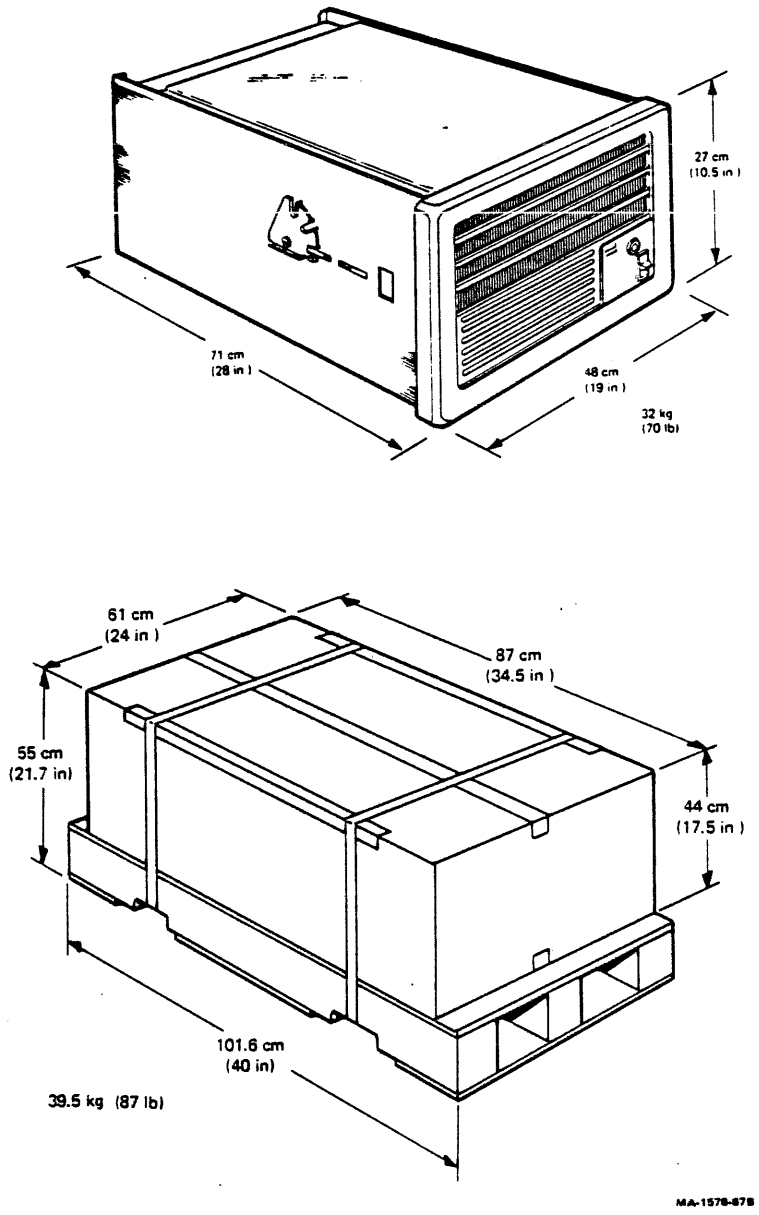


Figure 2–1 PDP-11/94-E Kernel System Dimensions

Figure 2–2 shows the dimensions of the PDP-11X94-E system. This system is enclosed in a standard system cabinet. When additional units are included in the system configuration, refer to the respective user's guide for the space requirements of each cabinet. The dimensions of the shipping container as well as the dimensions of an unpacked system as shown in Figure 2–2.

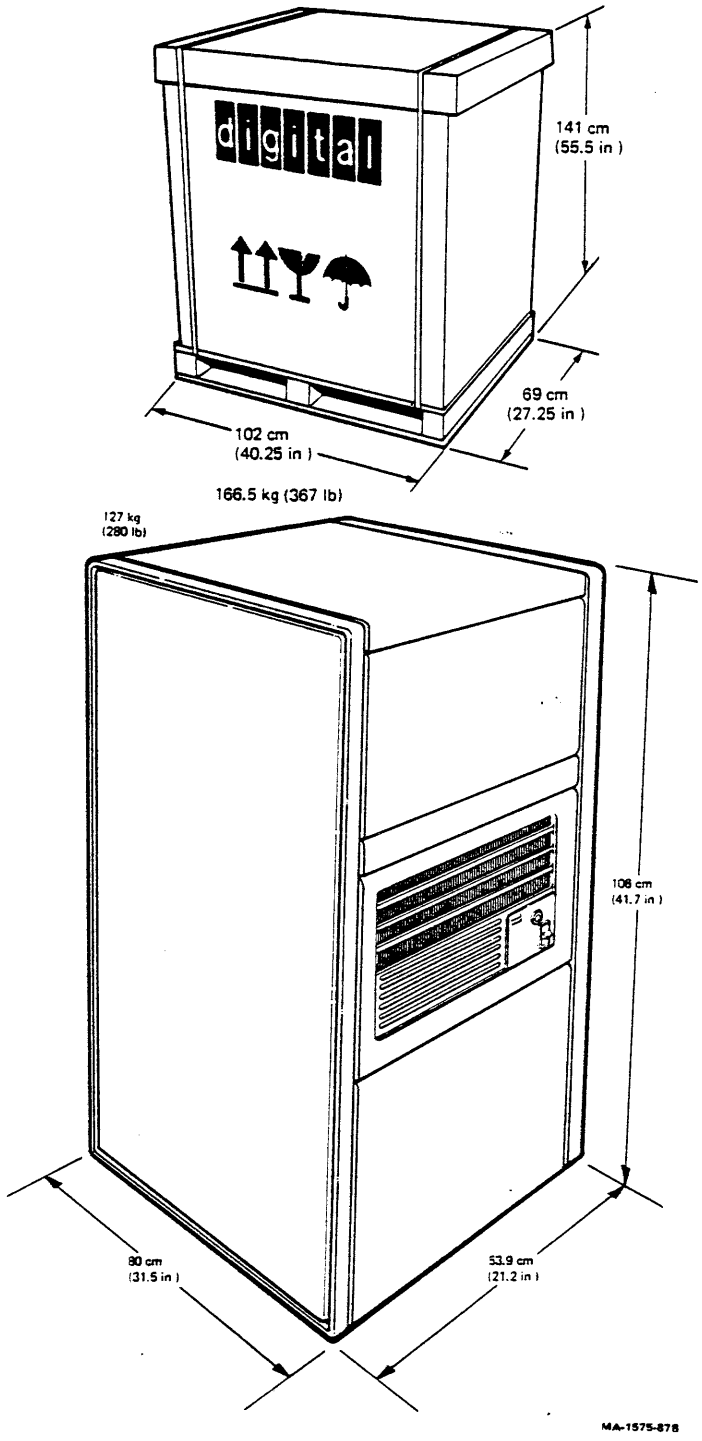


Figure 2–2 PDP-11X94-E Cabinet System Dimensions

Figure 2–3 shows the dimensions of the PDP-11W94-E system. This system is enclosed in a standard system cabinet. When additional units are included in the system configuration, refer to the respective user's guide for the space requirements of each cabinet. The dimensions of the shipping container as well as the dimensions of an unpacked system are shown in Figure 2–3.

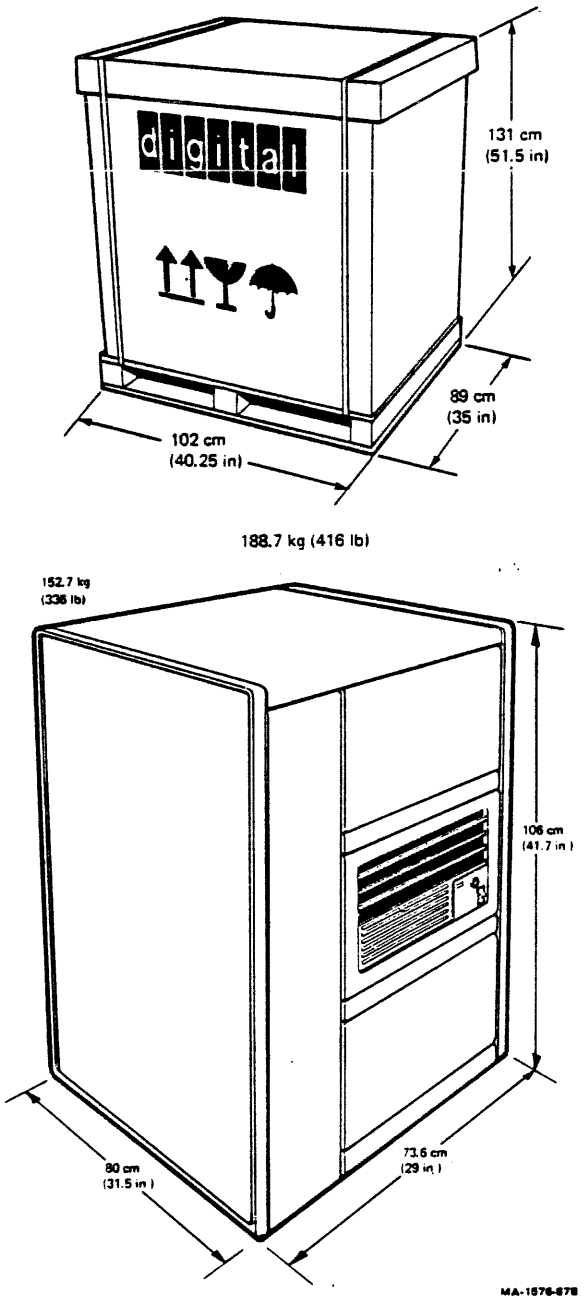


Figure 2–3 PDP-11W94-E Cabinet System Dimensions

2.2.3 Temperature and Humidity

Temperature cycling and thermal gradients can cause changes in materials which affects system performance. High temperatures also increase the rate of material deterioration. An environment of high absolute humidity can cause dimensional changes in paper tapes and line printer papers and cards. Low humidity can produce static electricity, resulting in dust accumulation on magnetic tape and disk devices, which will adversely affect the system operation.

The PDP-11/94-E systems are designed to operate in a temperature range of 5 to 50 °C (41 to 122°F) at a relative humidity of 10 to 95 percent without condensation. PDP-11X94-E and PDP-11W94-E system configurations require an operating temperature range from 10 to 40 °C (50 to 104°F) at a relative humidity of 40 to 66 percent without condensation. The nominal operating conditions for a system configuration are a temperature of 20°C (70°F) and a relative humidity of 45 percent.

The computer equipment should be operated in an environment that is controlled by an air conditioning system which provides temperature controlled, filtered air at the specified levels of humidity. The air conditioning system should also increase the air pressure in the computer area to prevent the infiltration of dust and other contaminants from adjacent areas.

The air conditioning equipment should conform to the requirements of the Standard for the Installation of Air Conditioning and Ventilating Systems (non-residential), N.F.P.A. No. 90A, as well as the requirements of the Standard for Electronic Computer Systems, N.F.P.A. No. 75.

2.2.4 Acoustical Dampening

When operating, some peripheral devices such as character printers, line printers and magnetic tape transports will generate noise. When many of these units are located in an area, use sound absorbent materials to reduce the noise level. Sound absorbent ceiling materials are available and antistatic carpets may be installed. In addition, the wall areas may be covered with drapes or other suitable material which will reduce the reflected noise.

2.2.5 Lighting

When video displays (CRTs) are used with the system, a reduced lighting level at the site can prevent excessive reflection from the face of the CRT and let the operator view the display with greater ease. The light levels may be controlled by dimmers or by installing translucent materials between the light source and the surrounding areas.

2.2.6 Static Electricity

Static electricity is a common problem for computer systems. It can cause system failure and loss of data. The most common source of static buildup is contact between people and carpeting or clothing. Low humidity allows the greatest buildup of static charges.

To minimize static buildup:

- Maintain relative humidity of at least 40 percent.
- Locate the system away from busy office corridors.
- Avoid using carpeting in the computer area (if possible). If carpeting is to be installed, use antistatic carpeting. If carpeting is already in place, place an antistatic mat around the system.
- Follow the manufacturer's recommendations if the site has antistatic carpeting or mats.

2.2.7 Electrical Interference

Several types of electrical interference may be caused by normal equipment operation at the site. Special filtering may be necessary to prevent equipment malfunctions.

The interference transmitted through the air is electromagnetic interference (EMI) and may be caused by TV and radio waves, radar transmissions, lightning discharges, ignition systems, and power line transmissions. Interference may also be transmitted through the ac power lines. If you suspect that interference is causing problems with equipment operation, the equipment may require shielding, or filtering of the ac power to the site. Contact your local Digital Sales office or Customer Services representative for information related to interference problems.

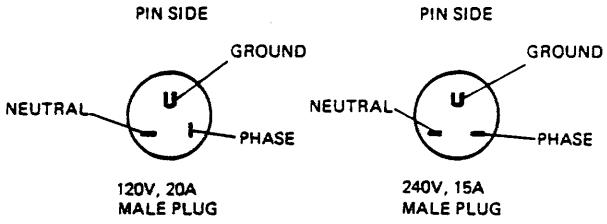
2.2.8 AC Input Power Requirements

A separate power circuit dedicated only to the system should supply ac input power to the PDP-11/94-E system.

Tables 1–4 and 1–6 list the power requirements for the three basic system configurations. Refer to the respective user guide for the power requirements of the peripheral devices supplied with the system.

2.2.9 Power Connections (AC)

The PDP-11/94-E units are supplied with a 2.74 meter (9 foot) line cord attached to the rear of the unit. The line cord plug may be connected to an 877 power controller unit (or equivalent) or may be connected directly to the ac power receptacle at the site location. Figure 2–4 shows the type of connector plugs and receptacles used and the Digital part numbers for the connectors. The NEMA 5-20 P plug is attached to the PDP-11/94-E (120 Vac) cable and the NEMA 6-15 P is attached to the PDP-11/94-E (240 Vac) cable. The NEMA 5-20 R and 6-15 R are dual-receptacle outlets that can be installed within a wall outlet box or in a power distribution unit.



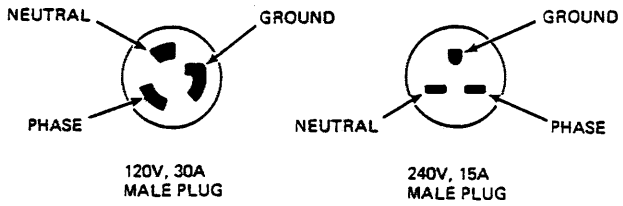
NEMA * DESIGNATION	POWER RATING	DIGITAL PART NO.
5–20 P	120V, 20A	12–15183–00
5–20 R		12–12265–00 * *
6–15 P	240V, 15A	90–08853–00
6–15 R		12–11204–01 * *

* P = PLUG
R = RECEPTACLE
** DUAL RECEPTACLE OUTLET

TK-4390
MA-1608-87

Figure 2–4 PDP-11/94-E Connector Specifications

A power controller unit that controls and distributes the ac power to the units within the cabinet is mounted at the lower rear of the PDP-11X94-E and PDP-11W94-E cabinet. The 120 Vac PDP-11X94-E and PDP-11W94-E systems contain an 877-DB (120 Vac) power controller, and the 240 Vac PDP-11X94-E and PDP-11W94-E systems contain an 877-F (240 Vac) power controller. Each controller is supplied with a 4.57 meter (15 foot) cord and plug that connects to a receptacle at the site location. Figure 2–5 shows the connector configurations and Digital part number for the receptacles.



USED WITH THE 877-DB OR 877-F POWER CONTROLLER

CONNECTOR SPECIFICATIONS

MODEL NUMBER	POWER	RATING	PLUG NEMA CODE	RECEPTACLE (SUPPLIED BY CUSTOMER)	
				NEMA CODE	DEC PART NO.
877-DB	120V	30 A	L5-30P	L5-30R	12-11194
877-F	240V	15A	6-15P	6-15R	12-11204-01

TK-4391
MA-1609-87

Figure 2–5 PDP-11X94-E and PDP-11W94-E Power and Connector Specifications

NOTE
The Digital part number for the PDP-11X94-E and PDP-11W94-E 120 Vac plug (L5-30P) is 12-11193-00. The part number for the 240 Vac plug (6-15P) is 90-08853-00.

2.2.10 System Grounding

The PDP-11/94-E, PDP-11X94-E, and PDP-11W94-E systems are commonly grounded to the main power lines through the ac power cord. To ensure the integrity of the grounding network, all units that are part of the system should be connected to a separate and common ac power distribution source. If a grounding problem is evident, check the potential of the cabinet or mounting box grounds by connecting a voltmeter between two cabinet frames or between the cabinet frames and the PDP-11/94-E system box. Contact your local Digital Customer Services office for information related to grounding problems.

2.3 Unpacking

The PDP-11/94-E is shipped in reinforced cartons on a skid and is protected by foam inserts and polyethylene bags. Accessories and supplies such as documentation, connecting cables, and hardware are packed in the container also. Before unpacking any carton, remove the packing list from the container and check that the items ordered are listed. When the items are unpacked, use the list to check that all the items are in the package. The unpacking information for consoles, printers, disk drives, and magnetic tape is contained in the user's guide supplied with each device.

NOTE
Keep the packing materials and shipping containers in case reshipping is required.

2.3.1 PDP-11/94-E Unpacking Instructions

CAUTION
Read the warning labels on the outside of the container to avoid injury during unpacking.

To open and remove the PDP-11/94-E system from the shipping container:

1. Cut and remove the plastic strapping.
2. Carefully cut the sealing tape.
3. Open the folded top of the container.
4. Remove the PDP-11/94-E system box, as shown in Figure 2–6.

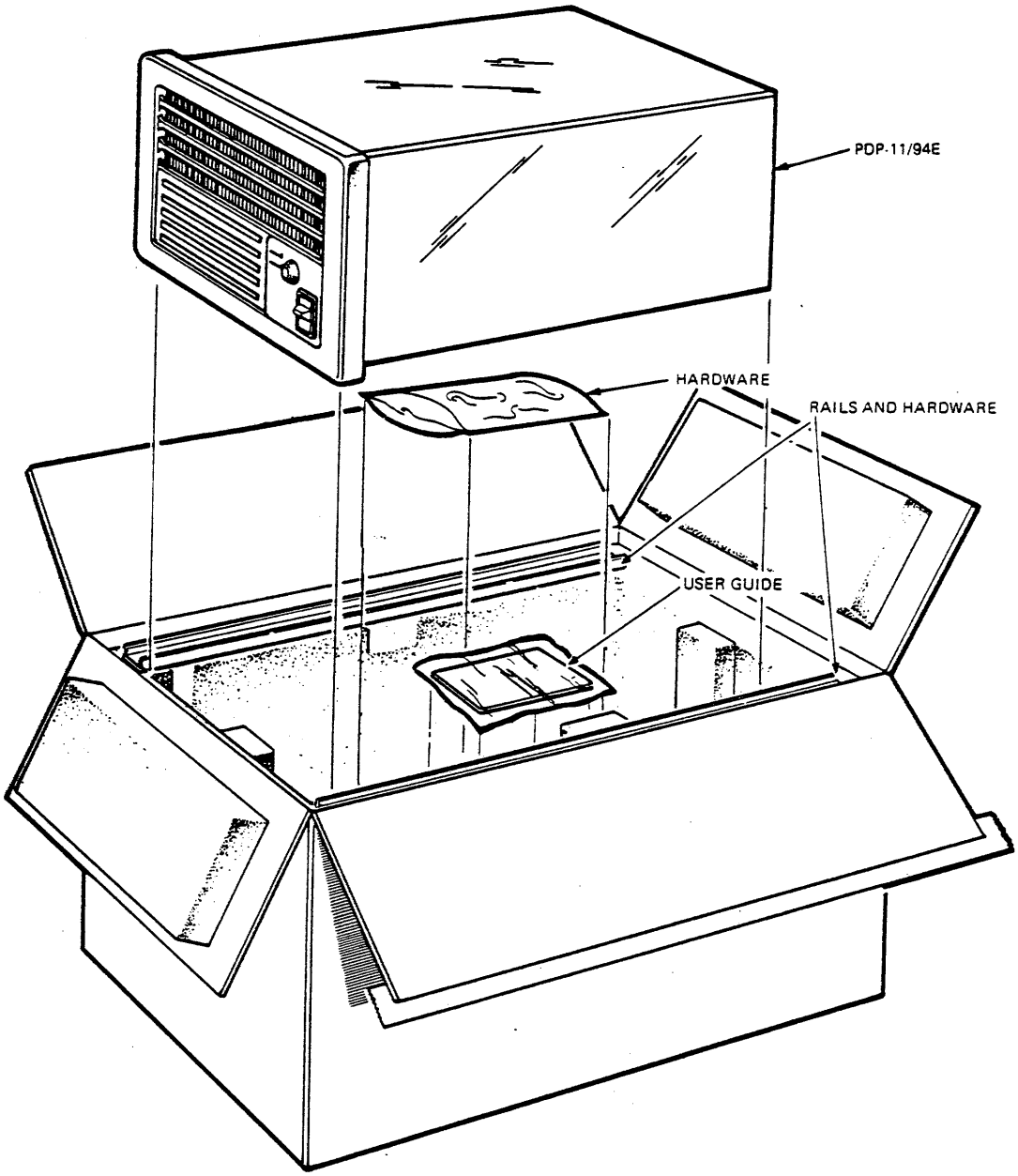


Figure 2–6 PDP-11/94-E System Box Unpacking

2.3.2 PDP-11X94-E and PDP-11W94-E Unpacking

CAUTION
Read the warning labels on the outside of the container to avoid injury during unpacking.

To open the shipping container:

1. Cut and remove the plastic strapping.

2. Remove the top cover.
3. Remove the PDP-11X94-E or PDP-11W94-E system cabinet from its shipping container by following the step-by-step procedure illustrated in Figure 2–7.

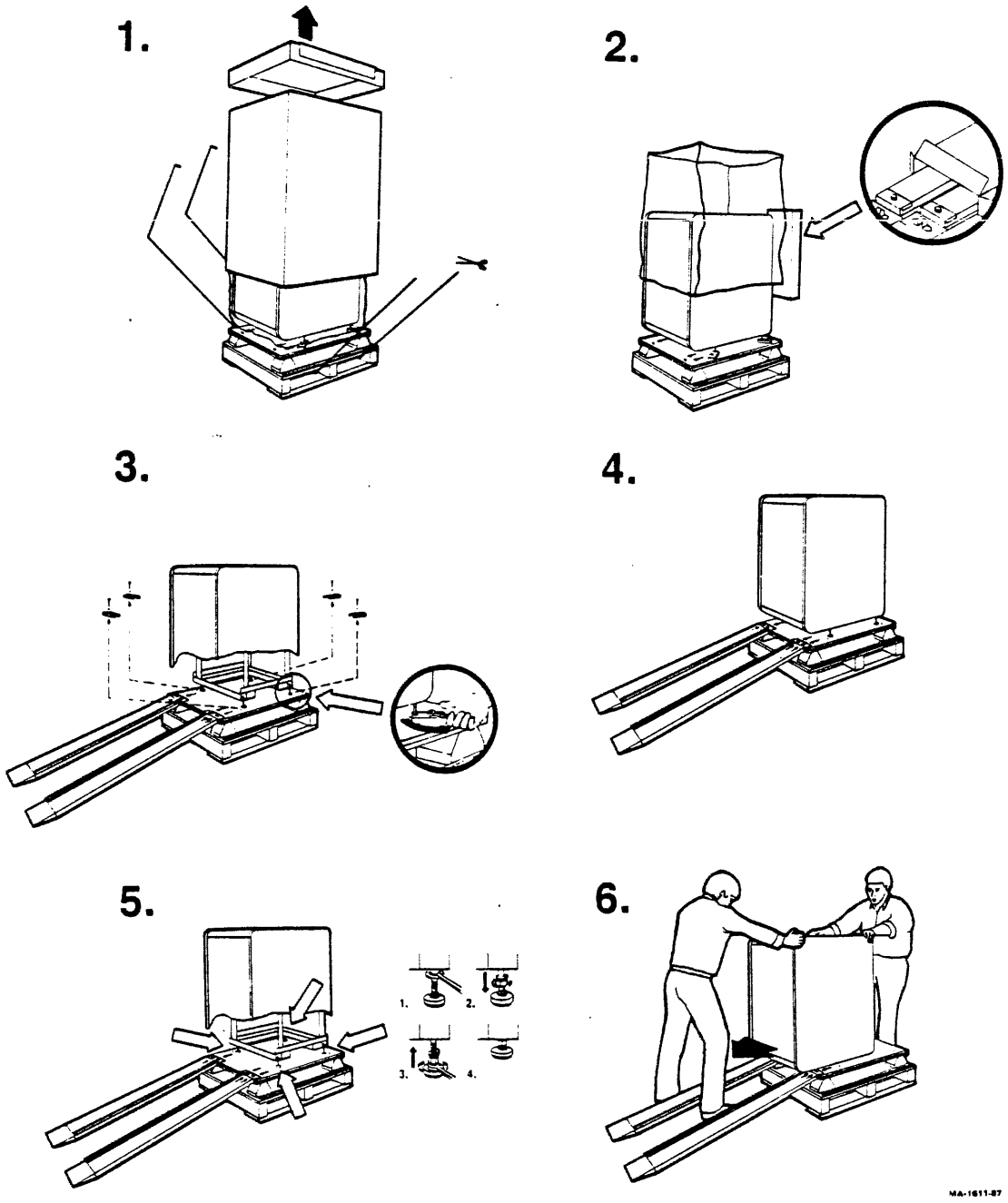


Figure 2–7 PDP-11X94-E and PDP-11W94-E Cabinet System Unpacking

2.4 Installation

To install a PDP-11/94-E system box refer to Section 2.4.1.

To install a PDP-11X94-E or PDP-11W94-E systems, refer to Section 2.4.2.

NOTE
These sections do not cover option installation. For option installation, refer to the manual that is supplied with the option.

2.4.1 PDP-11/94-E Installation

The PDP-11/94-E system box is designed to be installed in a standard NEMA 48.26 centimeter (19 inch) customer supplied rack or cabinet on slide-mounting assemblies.

2.4.1.1 Slide Assembly Mounting

A double-channel slide assembly kit is supplied with the PDP-11/94-E system. The slide kit includes the following items: left and right slide assembly and mounting hardware. The mounting location of the slides varies depending on the type of customer supplied cabinet. Figure 2–8 shows a double-channel slides assembly.

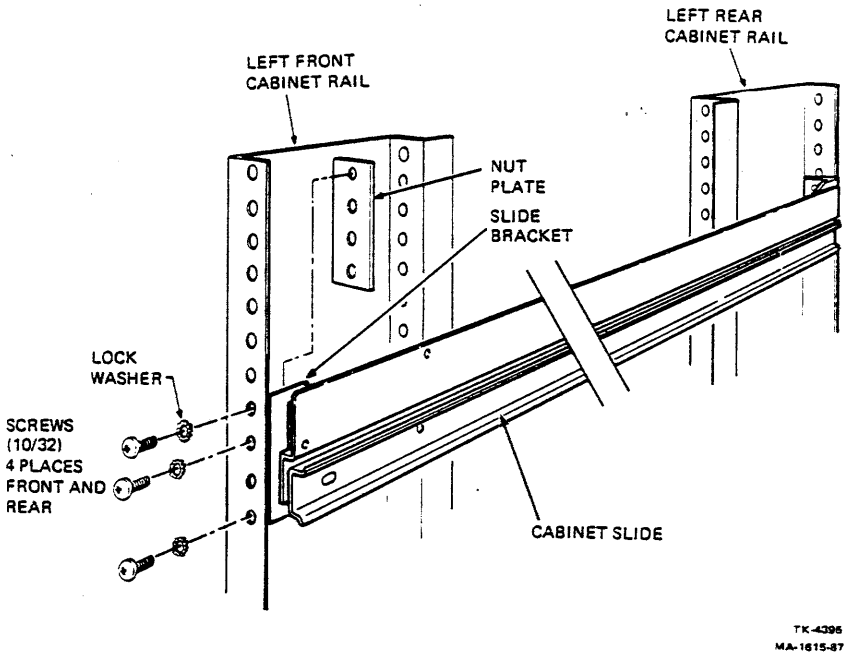


Figure 2–8 Cabinet Slide Installation

To install the slide:

1. Use the screws provided and attach two of the slide brackets to the left cabinet slide (one at each end of the slide).
2. Do not fully tighten the four slide bracket screws.
3. Repeat steps 1 and 2 to attach the remaining two slide brackets to the right cabinet slide.
4. Position the left slide against the left front and left rear cabinet rail as shown in Figure 2–8.
5. Insert one 10/32 screw and washer through the bottom hole of the left front rail, the slide bracket, and the nut plate. Do not fully tighten the screw (Figure 2–8).
6. Repeat step 5 for the left rear rail of the cabinet.
7. Insert one 10/32 screw and washer through the top hole of the left front rail, the slide bracket, and the nut plate. Do not fully tighten the screw (Figure 2–8).
8. Repeat step 7 for the left rear rail of the cabinet.
9. Insert one 10/32 screw and washer through the hole under the top screw of the left front rail, the slide bracket, and the nut plate. Tighten the three screws in the front rail (Figure 2–8).
10. Repeat step 9 for the left rear rail of the cabinet.
11. Fully tighten the four slide bracket screws.
12. Repeat steps 4 through 11 to install the remaining slide on the right side of the cabinet.

2.4.1.2 Mounting the System Box to the Slide Assembly

Figure 2–9 shows the method and hardware used to install the system box on the slide mounting bracket.

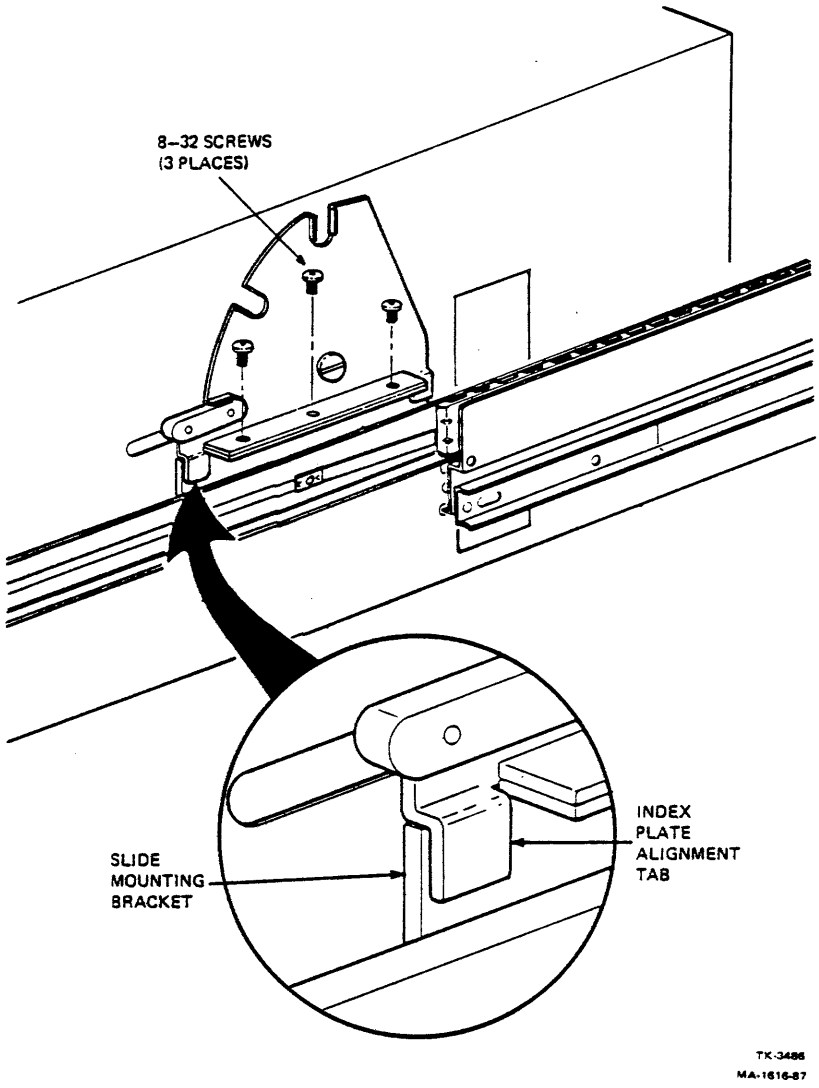


Figure 2–9 Mounting Box to Slide Installation

WARNING

Extend the cabinet stabilizer bar (if one is present) before placing the box on the slide assemblies (Figure 2–10).

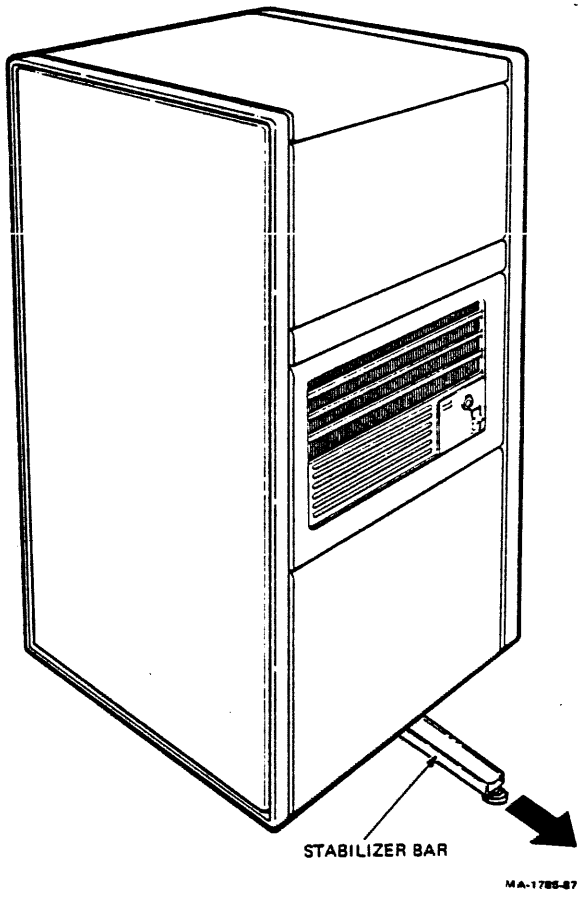
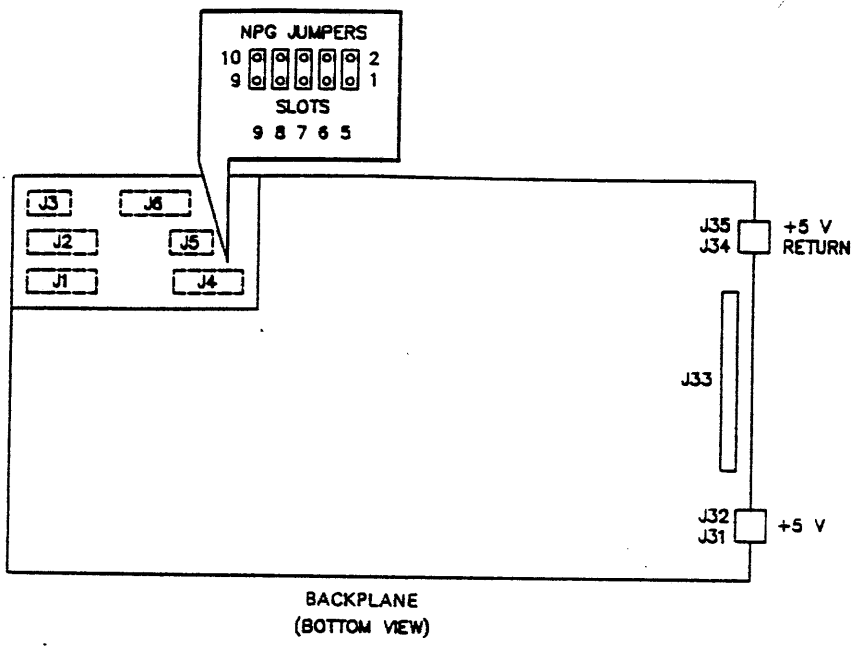


Figure 2–10 Stabilizer Bar Installation

To install the system box onto the slide mounting bracket:

1. Extend the left and right double-channel slides to their maximum position at the front of the cabinet.

   When fully extended, the channels will be held in place by the slide hold lever shown in Figure 2–11.



NOTE: JUMPERS ARE SHOWN IN THE INSTALLED POSITION.

MA-X1638-87

Figure 2–11 Double Channel Slide Assembly

2. Carefully lift the mounting box over and above the extended slides and set the index plate over the slide mounting bracket on each slide of the box. The index plate alignment tabs will engage the sides of the slide mounting bracket (Figure 2–9).

   NOTE
   When the slides are fully extended, it may be necessary to force the ends of the slides inward toward the sides of the mounting box.

3. Insert the three 8/32 screws through the left index plate tab and into the threaded holes of the slide mounting bracket.

4. Repeat step 3 for the right index plate.

2.4.1.3 Mounting the Console/Serial Line Unit Panel

To mount the console/SLU panel:

1. Remove four screws from the top cover of the system box. Remove the cover.

2. Remove the console/SLU from the polyethylene bag inside the system box.

3. Attach the two CPU signal cables to the connector on the back of the console/SLU panel (Figure 2–12). Cables are keyed for ease of installation.
4. Mount the console/SLU panel to the bulkhead on the cabinet.

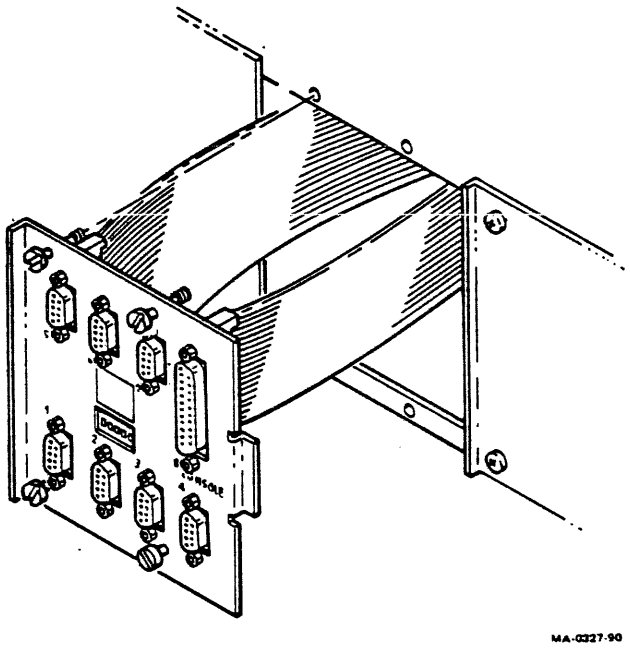


Figure 2–12 Mounting the Console/SLU Panel

5. Replace the system cover.
6. Press in the slide hold lever (Figure 2–11) on both sides of the system box.
7. Slide the system box into the cabinet until the system box latches.

NOTE
To pull the system box forward, release the latch that locks the system box into the cabinet. To operate the release lever, insert a small screwdriver blade into the hole behind the slot located at the top, right side of the front bezel and slide the screwdriver to the left as shown in Figure 2–13.

Once the latch is released, pull the front of the system box forward until it is fully extended and the slide levers are engaged.

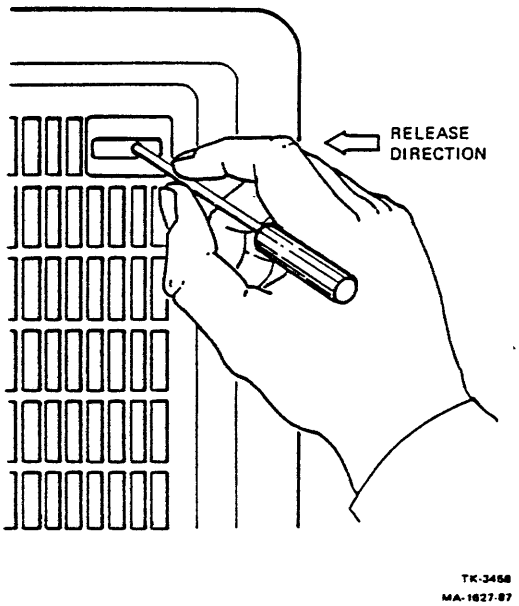


Figure 2–13 Release Lever Operation

2.4.1.4 Console/SLU Terminal Connection

To connect the console terminal:

1. Locate and connect one end of the 7.6 meter (25 foot) BC22D-25 EIA serial line cable (shipped with each system) to the customer supplied console terminal. Connect the other end to the console/SLU connector on the back of the system (Figure 2–14).

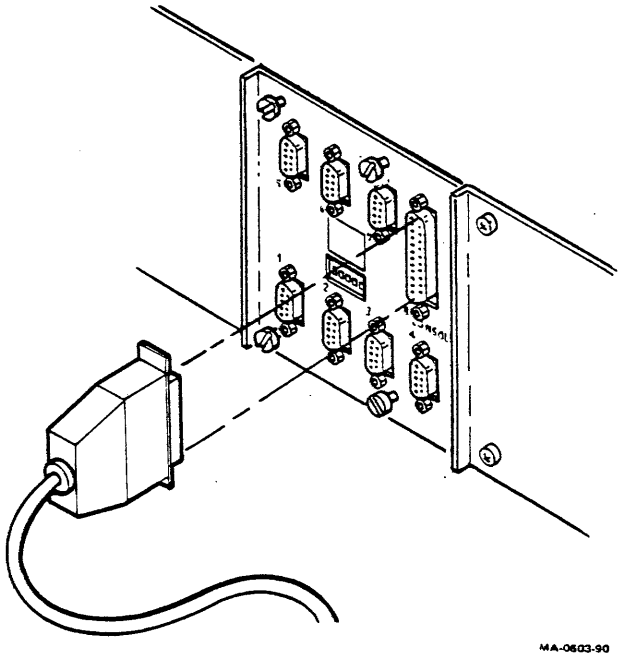


Figure 2–14 BC22D-25 Cable Connection

2. Set the baud rate switches to match the baud rate on the console terminal (Figure 2–15 and Table 2–1).

Table 2–1 Baud Rate Chart

SLU Baud Rate	6	7	8
300	OFF	OFF	OFF
600	OFF	OFF	ON
1200	OFF	ON	OFF
2400	OFF	ON	ON
4800	ON	OFF	OFF
9600	ON	OFF	ON
19200	ON	ON	OFF
38400	ON	ON	ON

3. Set the console terminal to eight data bits, no parity, and one stop bit.
4. Set the forced dialog switch (on the console/SLU panel) to the enable position (S5 on) (Figure 2–15).

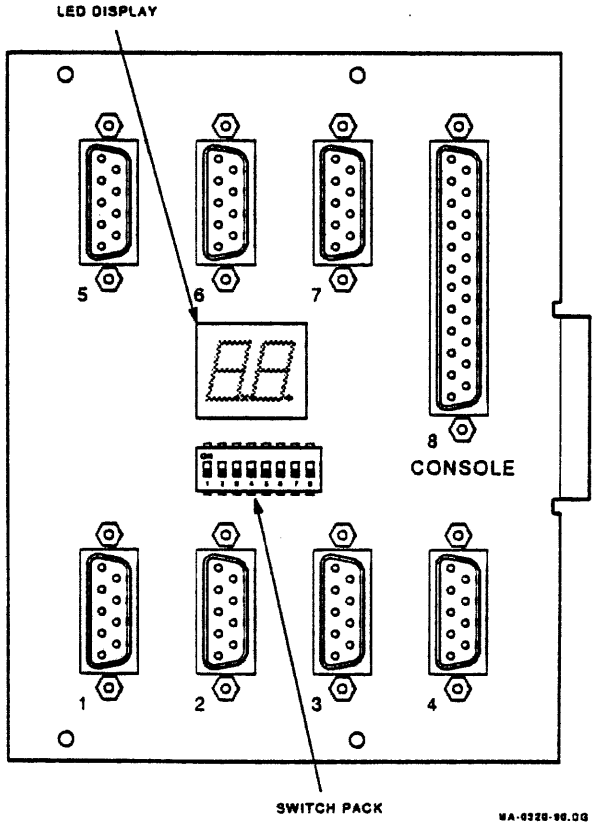


Figure 2–15 Console/SLU Panel Switches

2.4.1.5 AC Power Cord Connection

To connect the AC power cord:

1. Set the circuit breaker on the back of the system box to the off position (Figure 2–16).

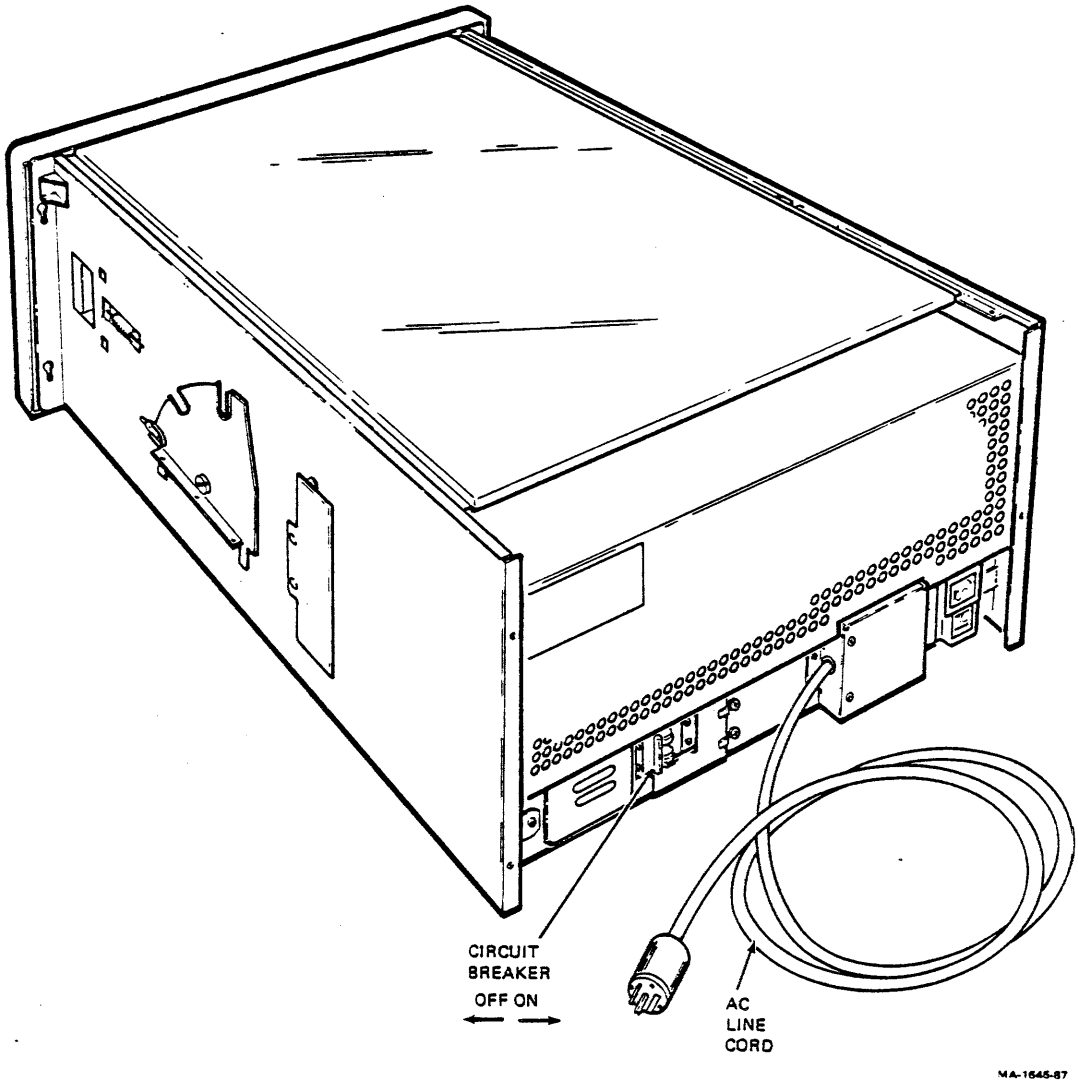


Figure 2–16 Circuit Breaker and AC Power Cord Location

2. Locate the red key in the hardware polyethylene bag. Insert the key in the front panel keylock switch and turn it to the off position, if it is not already in the off position (Figure 2–17).

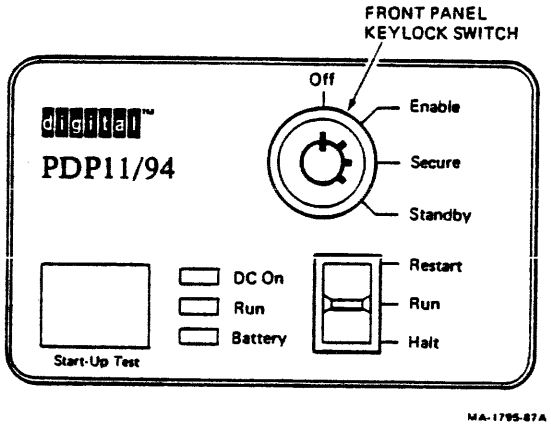


Figure 2–17 Front Panel Keylock Switch Location

3. Plug the system ac line cord into the wall receptacle or into an unswitched receptacle on the power controller.
4. Set the circuit breaker on the system box and the power controller (where applicable) to the on positions.
5. Go to Section 2.4.4.

2.4.2 PDP-11X94-E and PDP-11W94-E Cabinet System Installation

To install a PDP-11X94-E cabinet or a PDP-11W94-E cabinet system:

1. Roll and position the system cabinet where there is ample space for servicing the system.
2. Level the system cabinet by adjusting the leveling feet at each corner of the cabinet base, as shown in Figures 2–18 and 2–19.

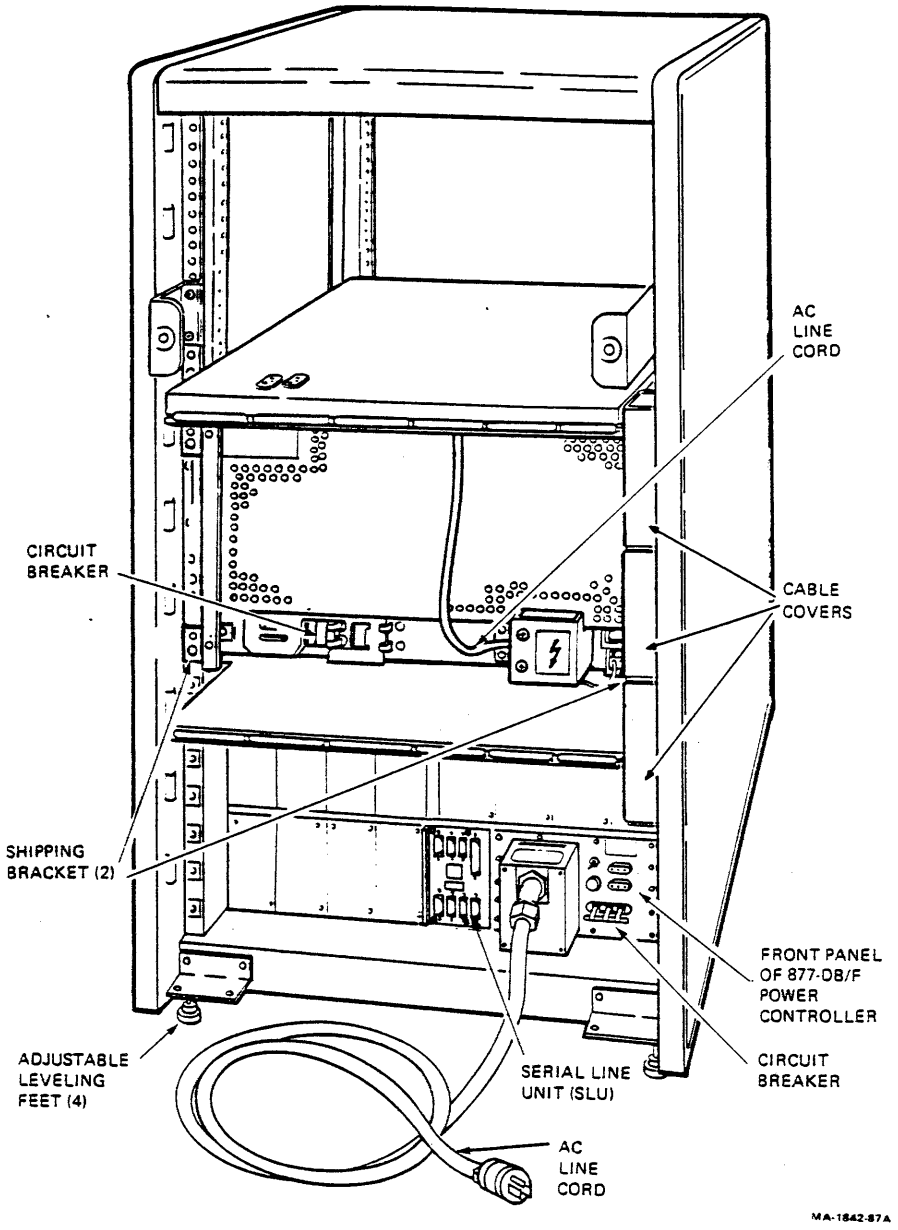


Figure 2–18 PDP-11X94-E Rear View

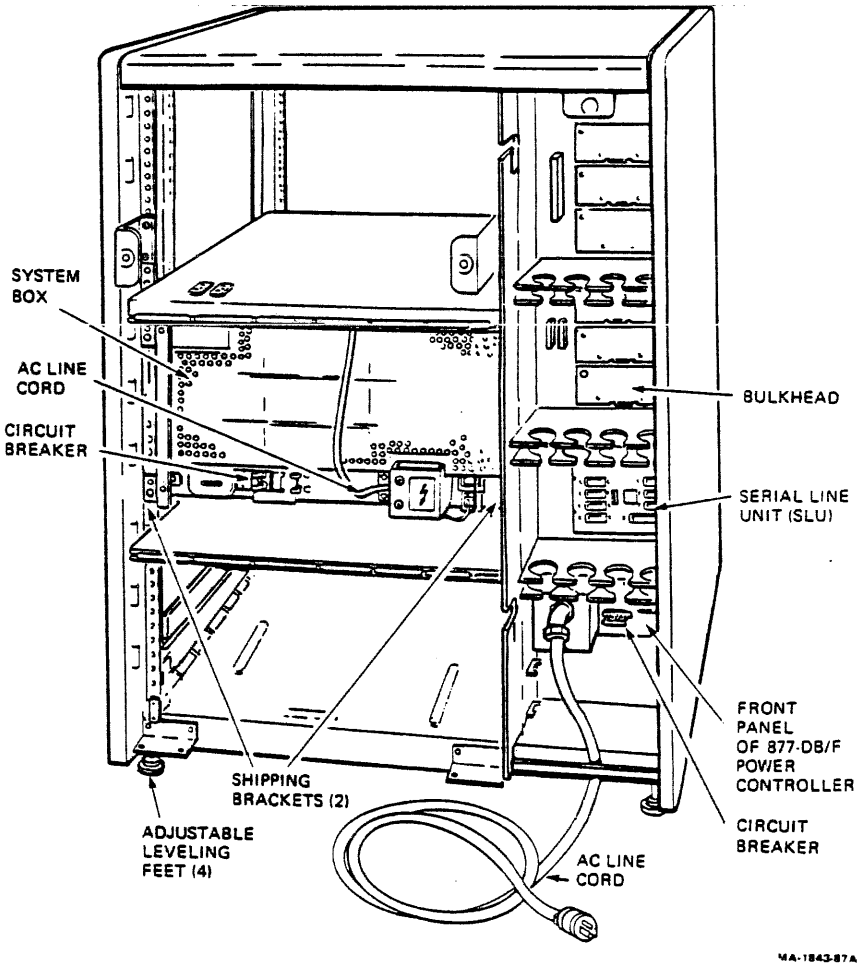


Figure 2–19 PDP-11W94-E Rear View

3. Remove the rear panel using a 5/32 allen wrench (not supplied) (Figure 2–20).

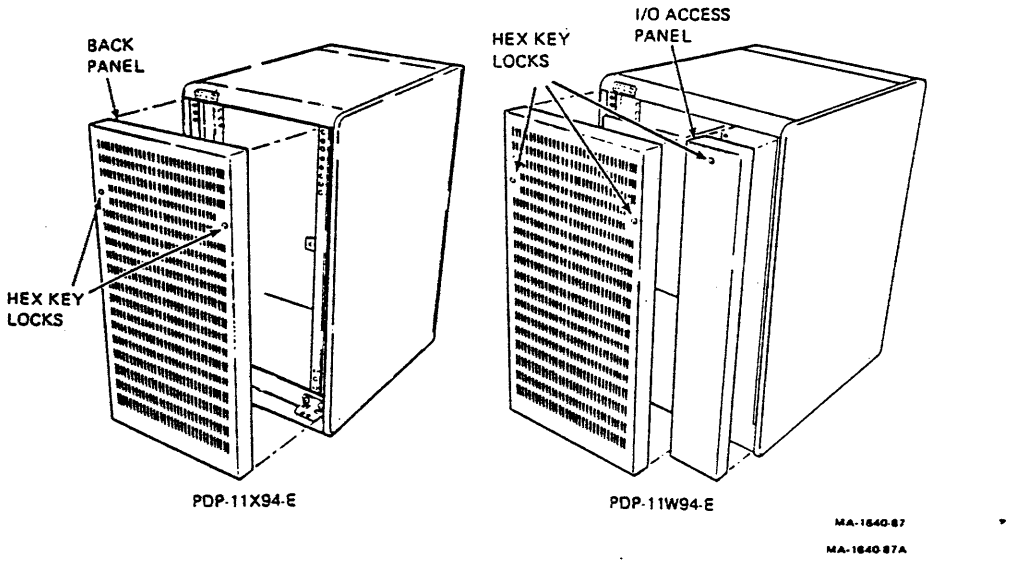


Figure 2–20 PDP-11X94-E and PDP-11W94-E System Rear Panels

4. Remove the eight screws holding the two red shipping brackets on the back of the system box. Replace the four screws (two on each side) removed on the system box.

   NOTE
   To remove the right shipping bracket, you must remove the two bottom cable covers at the right rear (viewing the system from the rear). To remove the shipping bracket screws, insert the screwdriver through the two holes.

5. Remove the red key from the hardware polyethylene bag. Insert the key in the front panel keylock switch and turn it to the off position, if it is not already in the off position (Figure 2–17).
6. Set the circuit breakers at the rear of the power supply and power controller unit to their off positions (Figures 2–18 and 2–19).
7. Set the **Remote/Off/Local** switch on the front of the power controller unit to the Remote position.
8. Set the forced dialog switch (on the console/SLU panel) to the enable position (S5 on) (Figure 2–15).
9. Set the baud rate switches to match the baud rate on the customer-supplied console terminal (Figure 2–15).
10. Set the console terminal to eight data bits, no parity, and one stop bit.
11. Connect the 7.6 meter (25 foot) BC22D-25 EIA serial line cable (shipped with the system) to the customer-supplied console terminal and to the console/SLU connector on the back of the system (Figures 2–18 and 2–19).
12. Insert the system ac power cord into the wall receptacle.
13. Set the circuit breaker at the rear of the power supply and the power controller unit to their on positions.

2.4.3 Cable Management

CAUTION
The system cables must be routed and dressed properly in the system cabinet to avoid cable damage.

Ensure that:

- All cables are routed so that they do not touch any sharp edges.
- All cables are secured (latched) with the plastic cable fasteners in the cabinet.
- There is enough slack in the cables (connected to the CPU box) to extend the CPU box to its service and maintenance positions. This also applies to cables connected to disk drives installed in the system cabinet.
- The system cables are dressed so that they do not become crimped or pinched when the cabinet panels are removed or installed.
- All flat signal cables making connections in the CPU box are secured (latched) with the metal cable clamps at the top of the box. The flat signal cable may be folded at a 45 degree angle to make connections to modules installed in the box.
- All round cables exiting the module area below the module retainer bar are secured with the metal cable clamps on top of the box.

2.4.4 Operation Check

To ensure that the PDP-11/94-E is operating correctly:

1. Set the **Restart/Run/Halt** switch to the Run position.
2. Ensure that the forced dialog switch is set to the Enable position (S5 on).
3. Turn the front panel keylock switch to the Enable position.

   This powers up the system. At this time, the Setup Menu displays on the console terminal.
4. Execute Self-test. Refer to Section 6.3.1 and run Test 30, All Selected Tests.

   The results of this test are shown in a digital display in the Start-Up Test display area of the front panel. If the test is successful, the digital display shows number 4. Also, as each test is running, the number and name of the test is displayed on the screen.

   If the test fails, an error code is displayed. For an explanation of the error codes, see Tables 6–3 and 6–2.

   After installing the system, refer to Chapter 3 which explains how to use the setup commands to list, change, and store the setup features. Record the setup feature selections on the worksheet in Appendix A.
5. Replace the rear panel.

3
Operation

3.1 General

This chapter describes the system controls and indicators. It also explains the menus and how to use them. The addresses assigned to the internal registers and detailed descriptions of the register bit functions are in Chapter 5, Functional Description.

You can develop user boot programs for the PDP-11/94-E using the information in this chapter.

3.2 Front Panel

The front panel consists of a keylock power switch, a **Restart/Run/Halt** switch, a Status display, and power and Run LED indicators. Figure 3–1 shows the front panel controls and indicators.

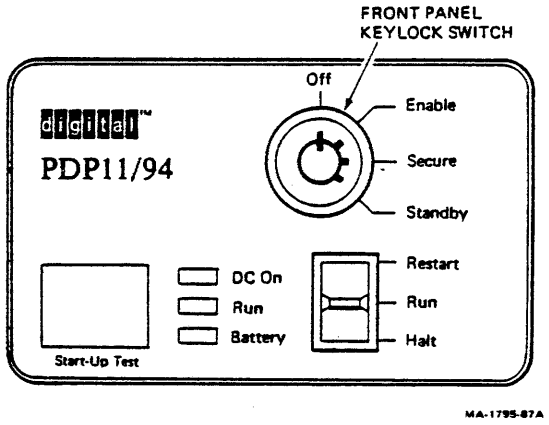


Figure 3–1 Front Panel Controls and Indicators

The keylock switch is a four-position rotary switch used to select one of four power states. Table 3–1 describes the keylock switch selections.

Table 3–1 Keylock Switch

Position	Function
Off	The power supply is turned off. DC power to the logic and fan assemblies is off; however, AC power to the power supply is present. Battery backup voltages are disabled.
Enable	The on position. Power supply voltages are present to the logic and fan assemblies.
Secure	Same as the Enable position except that the console terminal halt-on-break feature and the **Restart/Run/Halt** switch are disabled.
Standby	Power is supplied to the CPU module and fans, but other voltages are turned off. The optional battery back-up unit (if present) is not utilized in the Standby position.

The **Restart/Run/Halt** switch functions are enabled only when the keylock switch is in the enable position. Table 3–2 describes the **Restart/Run/Halt** switch functions.

Table 3–2 Restart/Run/Halt Switch

Position	Function
Halt	The CPU program is stopped and the incremented content of the program counter is displayed on the console terminal. The CPU enters DCJ-11 micro ODT.
Run	Entering Run from Restart enables CPU operations to run. Entering Run from Halt causes the processor to remain in micro ODT awaiting a command from the console terminal.
Restart	This momentary switch position initiates processor execution of bootstrap program instructions, located in the boot ROM, according to the setup configuration in the EEPROM.

The two-digit Status display provides the self-test and system startup messages. The codes are described in Chapter 6.

Three LED indicators are located on the front panel. Table 3–3 describes the functions of the LEDs.

Table 3–3 Front Panel Indicators

LED	Status	Function
Run	On	The DCJ-11 processor is fetching and executing instructions. This is the normal condition.
	Off	The processor is halted or waiting for an interrupt. When the processor is in micro ODT, the Run indicator blinks for each console keystroke. The Run LED also turns off during extended DMA activity.
DC On	On	The DC power is available to the logic, and all voltages are within specified levels.
	Off	The DC voltages are not available to the logic, or voltages are present but not within tolerances.
Battery	On	The battery is present and charged to 80% or greater capacity.
	Slow blink	The battery is at less than 80% capacity and is charging.
	Fast blink	The AC power has failed; the battery is discharging, but the memory content remains valid.
	Off	The battery is either fully discharged or is not present in the system. Memory content will not be preserved if AC power fails.

3.3 Console/Serial Line Unit Panel Switches

The console/serial line unit (SLU) panel has one switch pack which contains eight DIP switches (Figure 3–2). Table 3–4 describes the switches on the switch pack.

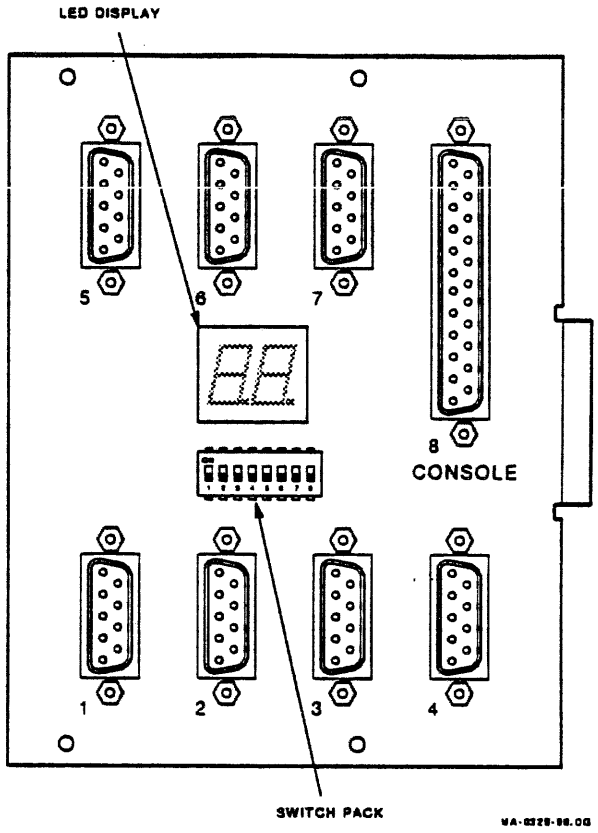


Figure 3–2 Console SLU Panel Switches

Table 3–4 SLU Switches - ROM Mode Only

Description	Switch Number		
Boot	**2**	**3**	**4**
1	ON	ON	OFF
2	ON	OFF	ON
3	ON	OFF	OFF
4	OFF	ON	ON
5	OFF	ON	OFF
6	OFF	OFF	ON
SLU Baud Rate	**6**	**7**	**8**
300	OFF	OFF	OFF
600	OFF	OFF	ON
1200	OFF	ON	OFF
2400	OFF	ON	ON
4800	ON	OFF	OFF
9600	ON	OFF	ON
19200	ON	ON	OFF
38400	ON	ON	ON
Console SLU	**1**		
Disable SLU	ON		
Enable SLU	OFF		
Force Dialog	**5**		
Enable (on) force dialog	ON		
Disable (off) force dialog	OFF		

3.4 Operation Overview

The CPU contains EEPROMs which store the programs (ROM code) that comprehensively test the CPU, UBA and memory at power-up. The ROM code also provides:

- Starting of the user's software on various devices
- Memory size display
- Time and date of TOY clock
- Boot device selection
- The ability to define parameters for SLUs
- Self-test selection
- User boot area on EEPROM
- Support for:
  - — Hard copy terminals
  - — Video display terminals

The CPU automatically starts the ROM code each time you power up the system or restart it with the **Restart/Run/Halt** switch on the front panel. The action the ROM code takes is determined by the parameters stored in the EEPROM.

The parameters in the EEPROM determine the tests to be run, the general mode entered after testing is complete, and the final configuration of certain registers on the CPU and UBA module before the system software is started. Parameters in the EEPROM can easily be changed through a program in the ROM code called *Setup Mode* without removing the CPU or UBA modules. The EEPROM can also store customer bootstrap programs.

The ROM code runs tests selected by parameters in the EEPROM. After testing is complete, parameters in the EEPROM determine what action is to be taken next by the ROM code. Typically, the ROM code will automatically load and start a program from the user's disk or tape. This is commonly referred to as booting a program or automatic boot mode.

After the software is started, the ROM code is not entered again until the system is powered up or restarted. In some cases, after testing is complete, the ROM code enters *Dialog Mode* which allows you to select the actions entered through keyboard commands via the console terminal.

Dialog mode allows you to do the following:

- Boot a device
- List boot programs available
- Run ROM resident tests
- List a map of the I/O page locations
- Enter setup mode to list or change all parameters in the EEPROM.
- Enter time and date for TOY clock.

Hard copy terminal support is described in Section 3.5.

Video terminal support is described in Section 3.6.

3.5 Hard Copy Terminal Support

This section describes the hard copy ROM commands.

When dialog mode is entered, the ROM code prints out the Main Menu at the console terminal and waits for you to select a command.

An example of the Main Menu is provided in Example 3–1.

```
                ❶
KDJ11-E Monitor  Version 1.06 23-May-1990
(C) Digital Equipment Corporation 1990
Unibus System
Memory     2048 KW❷
EEprom        4 KW❸
Time      15:44:37 30-May-90 Wed❹

❺
Commands are: [Boot, Diagnostic, Help, List, Map, Setup, Toy]
Type a command then press the RETURN key:
```

Example 3–1 Main Menu

The ROM code heading contains:

❶ Version number of the ROM code and date created.

❷ Memory size in Kilowords.

❸ EEPROM area for USERBOOT programs.

❹ Time and date from TOY Clock.

❺ Command line for selecting the 7 hard copy ROM commands:

Boot	Map
Diagnostic	Setup
Help	TOY
List	

These commands are described in the following sections.

3.5.1 Boot Command

The Boot Command allows a device to be booted. The primary boot program normally reads 256 words from the device into memory starting at location 0. If the secondary bootstrap "block 0"is loaded without any errors, the ROM code transfers control to location 0 with the MMU off, R0 equal to the unit number of the device booted and R1 equal to the base address of the device CSR. For some devices, R1 is the base address plus an offset.

The format for the Boot Command is:

```
B XXN
```

Where:

B	Is the Boot Command.
XX	Is the two letter mnemonic representing the device to be booted. The device name must be letters from A to Z.
N	Is the unit number to be booted.

When the ROM code has a device name, it searches for the first boot program with the same device name. The ROM code looks for matches from these sources in the following sequence:

1. EEPROM
2. CPU ROM
3. UBA module
4. M9312 module (if present)

There are two optional switches that can be used with the boot command:

Switch	Description
/U	Tells the ROM code to search for the boot program in the UBA ROMs first, then the M9312 (if present). This overrides the standard sequence of searching first in the EEPROM, then the CPU ROM.
/A	Overrides the default address allowing you to enter a new address.

Table 3–5 provides examples of how the ROM code interprets user input.

Table 3–5 ROM Code Interpretation of User Input

User Input	ROM Code Action
B DL1	Boots DL1.
B DU7	Boots DU unit 7.
B DU3/U	Boots DU3 using UBA or M9312. ROM boot instead of CPU ROM code.
B DU7/U	Boots DU unit number 7 using UBA or M9312 ROM boot instead of CPU ROM.
B B	Transfers control to an external boot module.
B/A 160100 DK0	Boots RK05 with a CSR address of 160100.
B D U 0	Invalid format. No space allowed in the device name DU.
BDU0	Invalid format. There must be a space between the Boot command and the device name.

A list of the default boot programs is provided in Table 3–6.

NOTE
For a complete list of all the boot programs, execute the List Command on the Main Menu.

Table 3–6 Default Boot Programs

Device Name	Unit Numbers	Source	Device Type
DU	0-255	ROM	MSCP (RAxx, RDxx, RX50, RC25, ...)
DL	0-3	ROM	RL01/RL02
DX	0-1	ROM	RX01
DY	0-3	ROM	RX02
MS	0-1	ROM	TK25, TS04/05/11, TU80
MT	0-1	ROM	TU10, TE10, TS03
MU	0-255	ROM	TMSCP (TK50, TU81, ...)

3.5.1.1 Transferring Control to Non-Digital Boot Modules

The single-letter device name B implements a method of supporting non-Digital boot devices on the UNIBUS.

B causes the ROM code to transfer control to the address contained in location 17773024 of a ROM on the UNIBUS (if any) as long as the value in location 17773024 is not odd.

When the CPU ROM passes control:

- The CPU ROMs and the UBA ROMs are disabled.
- R0 contains a unit number.
- R1 contains 0.

The ROM code types out an *invalid device message* if:

- The address in location 17773024 on the UNIBUS is odd.
- The boot module does not respond to all addresses from 17773000 to 17773776.

Typically the single-letter device name **B** is used when you have a module which has a switch pack that responds at address 17773024 similar to a M9312 module. Usually the start address of the program desired is set in the switch pack on the module.

3.5.1.2 Error Detection During the Boot Command

The ROM code boot programs attempt to detect errors during the boot process and take the appropriate action. Table 3–7 lists the possible errors that the ROM code tries to detect. Not all errors are applicable for all boot programs.

Table 3–7 Boot Command Errors

LED Code	Description
21	Drive error.
20	Controller error.
17	Boot device selection was invalid.
16	Invalid unit number selected.
15	Non-existent drive.
14	Non-existent controller.
13	No tape.
12	No disk.
11	Invalid boot block.
10	Drive not ready.
07	No bootable device found while in Auto Boot Mode.

NOTE

After successful completion of the loading of a secondary bootstrap, the display is set to 00. Before transferring control to the secondary boot, the ROM code prints out *Starting System*. At this time, parameters saved in the ROMs are loaded into the CPU registers.

The following is an example of a Boot Command:

```
KDJ11-E Monitor  Version 1.06 08-May-1990
(C) Digital Equipment Corporation 1990
Unibus System
Memory     2048 KW
EEprom        4 KW
Time      15:41:52 16-May-90 Wed

Commands are: [Boot, Diagnostic, Help, List, Map, Setup, Toy]
Type a command then press the RETURN key: B DL0

   Trying
   Starting System
```

Example 3–2 Boot Command

3.5.2 Diagnostic Command

The Diagnostic Command allows you to test the CPU, on-board memory and the KTJ11-B. Tests can be run individually or as a group (Test 30, All Selected Tests).

You are prompted for the following information:

Prompt	Action
Test Number	Select a test from the list displayed on the terminal
	Test 30, All Selected Tests, runs all tests selected in Setup Mode Command 3. See Section 3.5.6.3 for more information.
	Test 32, Serial line Unit Loopback Test requires that loopback connectors be installed on all SLUs on the console/SLU panel.
Repeat Counter	Type the number of desired iterations in decimal, or type 0 to run the test(s) continuously.

After selecting the test number and number of iterations, testing starts. The ROM code displays the test number, description of the test, error count and iteration number.

If continuous testing is selected, no information is printed except errors. This allows the Diagnostic Command to run for extended periods of time without requiring additional printer paper.

To terminate testing, type Ctrl C or Ctrl P.

To execute the Diagnostic Command:

1. At the command line on the Main Menu, type D.
2. Press Return.

In the following example, test 67 is selected to be run once.

```
KDJ11-E Monitor  Version 1.06 23-May-1990
(C) Digital Equipment Corporation 1990
Unibus System
Memory     2048 KW
EEprom        4 KW
Time      15:44:37 30-May-90 Wed

Commands are: [Boot, Diagnostic, Help, List, Map, Setup, Toy]
Type a command then press the RETURN key: D

KDJ11-E Monitor  Version 1.06 08-May-1990
(C) Digital Equipment Corporation 1990

Single diagnostic test repeat

67 CPU Test
66 MMU Test
65 Pre-Console Test
64 MSER Test
63 CCR r/w Test
62 HIT/MISS-Reg Test
61 LTC Speed Test
60 Add-Stat-Reg Test
57 CPU-Err-Reg Test
55 UBA reg. resp. Test
54 Address 0 Test
53 Pre-Memory (0-4KW) Test
52 FPA Register Test
51 FPA Function Test
50 Int Mem Address Test
47 Int Mem Data Test
46 PIRQ-Reg Test
45 LTC Int Test
44 Lines Config. Test
43 Serial Lines Test
40 Memory parity Test
37 UBA map reg Test
36 UBA NPR Cycle Test
32 Loopback SLU Test
31 Extended Memory Test
30 All Selected Tests

Type CTRL Z to exit

Test number    = 67                                New = 67

Type 0 for endless loop; break loop with CTRL C

Repeat counter = 000001                            New = 1

67 CPU Test  No Errors found
```

Example 3–3 Diagnostic Command

NOTE
If the repeat counter is set to 0 to run continuously, only errors are printed.

3.5.3 Help Command

The Help Command prints out a brief description of all the commands. At the end of this command, you are returned to the Main Menu.

To execute the Help Command:

1. At the command line on the Main Menu, type H.
2. Press Return.

The following is an example of the Help Command:

```
KDJ11-E Monitor  Version 1.06 23-May-1990
(C) Digital Equipment Corporation 1990
Unibus System
Memory     2048 KW
EEprom        4 KW
Time      15:44:37 30-May-90 Wed

Commands are: [Boot, Diagnostic, Help, List, Map, Setup, Toy]
Type a command then press the RETURN key: H

KDJ11-E Monitor  Version 1.06 08-May-1990
(C) Digital Equipment Corporation 1990

Command      Description

Help         Type this message
Boot         Load and start a program from a device
Diagnostic   Execute a self-test single or repetitive
List         List boot programs
Map          Map memory and I/O page
Setup        Enter Setup mode
Toy          Set time and date

Commands are: [Boot, Diagnostic, Help, List, Map, Setup, Toy]
Type a command then press the RETURN key:
```

Example 3–4 Help Command

3.5.4 List Command

The List Command prints out a list of all available boot programs found in the CPU ROM, the CPU EEPROM (User Boot), ROM sockets on the UNIBUS adapter, or an M9312 (if present).

To execute the List Command:

1. At the command line on the Main Menu, type L.
2. Press Return.

The following is an example of the List Command:

```
KDJ11-E Monitor  Version 1.06 23-May-1990
(C) Digital Equipment Corporation 1990
Unibus System
Memory     2048 KW
EEprom        4 KW
Time      15:44:37 30-May-90 Wed

Commands are: [Boot, Diagnostic, Help, List, Map, Setup, Toy]
Type a command then press the RETURN key: L

KDJ11-E Monitor  Version 1.06 18-May-1990
(C) Digital Equipment Corporation 1990
❶      ❷
Device  Unit      ❸      ❹
Name    Numbers Source Device Type

AB      0       USR
TT      0       USR
DU      0-255   ROM    MSCP (RAxx, RDxx, RX50, RC25, ...)
DL      0-  3   ROM    RL01/RL02
DX      0-  1   ROM    RX01
DY      0-  3   ROM    RX02
MS      0-  1   ROM    TK25, TS04/05/11, TU80
MT      0-  1   ROM    TU10, TE10, TS03
MU      0-255   ROM    TMSCP (TK50, TU81, ...)
DL      0-  3   UBA    RL01/RL02

Press RETURN key when ready to continue
```

Example 3–5 List Command

❶ The device name is a two-letter mnemonic. The device name must be the letters from A to Z. At input, the ROM code converts all lower case letters to upper case.

❷ The unit number range is the allowable range of unit numbers that is valid for a particular boot program.

❸ The source lists where the actual boot program is located:

Physical Location of Boot ROM	Source
CPU ROM	ROM
ROM Sockets on the UNIBUS adapter module	UBA
M9312	M93
User Boot Area	USR

❹ The Device Type is a description of the device to be booted.

NOTE
There is no description (Device Type) provided for M9312-type ROMs.

At the completion of the List Command, you are returned to the Main Menu.

3.5.5 Map Command

The Map Command prints out all addresses in the I/O page that respond. The I/O page starts at address 17760000.

In addition, all addresses that are on the CPU or on the UBA that respond, are briefly described. There is no description for optional device addresses that respond. At completion of the Map Command, you are returned to the Main Menu.

To execute the Map Command:

1. At the command line on the Main Menu, type M.
2. Press Return.

The following is an example of the Map Command:

```
KDJ11-E Monitor  Version 1.06 23-May-1990
(C) Digital Equipment Corporation 1990
Unibus System
Memory     2048 KW
EEprom        4 KW
Time      15:44:37 30-May-90 Wed

Commands are: [Boot, Diagnostic, Help, List, Map, Setup, Toy]
Type a command then press the RETURN key: M

KDJ11-E Monitor  Version 1.06 18-May-1990
(C) Digital Equipment Corporation 1990

I/O page Map
Starting     Ending
Address      address

17765000    17765776    CPU ROM or EEPROM
17772100                Memory CSR
17772200    17772276    Supervisor I and D PDR/PAR's
17772300    17772376    Kernel I and D PDR/PAR's
17772516                MMR3
17773000    17773776    CPU ROM
17776500    17776566    SLU's
17777200    17777376    UBA map REG's
17777520    17777526    CSR, PCR, BCR/BDR ASR
17777546                Clock CSR
17777560    17777566    Console SLU
17777572    17777576    MMR0,1,2
17777600    17777676    User I and D PDR/PAR's

Press RETURN key when ready to continue
```

Example 3–6 Map Command

3.5.6 Setup Command

The Setup Command has fourteen commands as shown in Example 3–7. These commands allow you to list and/or change all parameters in the EEPROM. Setup also allows you to create or edit USERBOOT programs stored in the EEPROM.

The EEPROM contains information needed by the ROM code to configure the KDJ11-E (CPU) and the KTJ11-B (UBA) and to determine the boot device, diagnostic test selections and restart modes.

NOTE

Changes made under Setup Mode are ignored unless they are saved in EEPROM using Setup Mode Command 8.

To execute the Setup Command:

1. At the command line on the Main Menu, type S.
2. Press Return.

The following is an example of the Setup Command:

```
KDJ11-E Monitor  Version 1.06 23-May-1990
(C) Digital Equipment Corporation 1990
Unibus System
Memory     2048 KW
EEprom        4 KW
Time      15:44:37 30-May-90 Wed

Commands are: [Boot, Diagnostic, Help, List, Map, Setup, Toy]
Type a command then press the RETURN key: S

KDJ11-E Monitor  Version 1.06 08-May-1990
(C) Digital Equipment Corporation 1990

Setup Mode Commands

1   Exit
2   Select configuration parameters
3   Select diagnostic configuration
4   Select serial line parameters
5   Select boot parameters
6   List available boot programs
7   Factory setting
8   Save the setup table in the EEPROM
9   Load EEPROM data into the setup table
10  Load EEPROM boot program into memory
11  Edit or create EEPROM boot program
12  Save a boot program in the EEPROM
13  Delete a saved EEPROM boot program
14  Enter ROM ODT

Commands are: [1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14]
Type a command then press the RETURN key:
```

Example 3–7 Setup Command

3.5.6.1 Setup Mode Command 1 - Exit

Setup Mode Command 1 exits Setup Mode and returns to the Main Menu. You can also return to the Main Menu by pressing Ctrl C.

To execute the Setup Mode Command 1:

1. At the command line on the Setup Menu, type 1.
2. Press Return.

The following is an example of Setup Mode Command 1:

```
KDJ11-E Monitor  Version 1.06 08-May-1990
(C) Digital Equipment Corporation 1990
Unibus System
Memory     2048 KW
EEprom        4 KW
Time      15:44:37 16-May-90 Wed

Commands are: [Boot, Diagnostic, Help, List, Map, Setup, Toy]
Type a command then press the RETURN key:
```

Example 3–8 Setup Mode Command 1

3.5.6.2 Setup Mode Command 2 - Select Configuration Parameters

The Setup Mode Command 2 prints out the current status of various parameters and allows you to change them.

When Setup Mode Command 2 is executed, the ROM code prints out the current status of all parameters, repeats the first parameter, and then waits for your input.

There are two methods you can use to position the program at the parameter you want to change:

- Press Return until positioned at the parameter to be changed.
- To go directly to the parameter to be changed, enter the letter to the left of the parameter.

To change a parameter, enter the new value and press Return. The ROM code proceeds to the next parameter.

NOTE

Changes made under Setup Mode are ignored unless they are saved in the EEPROM using Setup Mode Command 8 (see Section 3.5.6.8).

To execute Setup Mode Command 2:

1. At the command line on the Setup Menu, type 2.
2. Press Return.

The following is an example of Setup Mode Command 2:

```
KDJ11-E Monitor  Version 1.06 18-May-1990
(C) Digital Equipment Corporation 1990

A  Memory Intern                (0) =   2MB  (1) =   4MB      = 1

B  Rom on 173000                (0) =    No  (1) =   Yes      = 1

C  Rom on 165000                (0) =    No  (1) =   Yes      = 0

D  Power-up Mode                (0) = Dialog
                                (1) =   Odt
                                (2) = Trap24
                                (3) =  Auto                   = 0

E  Restart Mode                 (0) = Dialog
                                (1) =   Odt
                                (2) = Trap24
                                (3) =  Auto                   = 0

F  Power-on Self-tests          (0) =    No  (1) =   Yes      = 1

G  Alternate Boot Block         (0) =    No  (1) =   Yes      = 0

H  LTC Register                 (0) =    No  (1) =   Yes      = 1

I  Force Clock Interrupt        (0) =    No  (1) =   Yes      = 0

J  Clock Frequency              (0) =   P/S
                                (1) =  50Hz
                                (2) =  60Hz
                                (3) = 800Hz                   = 2

K  Halt on Break                (0) =    No  (1) =   Yes      = 0

L  Trap on Halt                 (0) =    No  (1) =   Yes      = 0

M  Ignore Battery               (0) =    No  (1) =   Yes      = 0

N  Lines on                     (0) =   DIS
                                (1) = 176500
                                (2) = 176600                  = 1

O  Disable UBA ROM              (0) =    No  (1) =   Yes      = 1

P  Enable UBA 18-Bit Mode       (0) =    No  (1) =   Yes      = 0

Type CTRL Z to exit or press Return key to proceed
```

Example 3–9 Setup Mode Command 2

The following describes each parameter that can be changed using Setup Mode Command 2.

A - Memory Intern

The KDJ11-E CPU module contains the following on-board memory:

KDJ11-EA Contains 2MB of on-board memory.

KDJ11-EB Contains 4 MB of on-board memory.

If the amount of memory selected does not match the memory on-board, the message *Mem mismatch* prints. This parameter has no effect on the KDJ11-EA.

The KDJ11-EB contains 4MB of on-board memory. For some applications it may be desirable to disable the top 2MB of memory.

Table 3–8 describes the variations of this parameter.

Table 3–8 Memory Intern Parameter Variations

Setting	Description
0	2MB
1	4MB. **Factory setting.**

B - Rom on 173000

This parameter sets/resets bit 7 of the CSR at address 17777520 just before transferring control to another boot program.

The KDJ11-E ROM code responds to the addresses from 17773000 to 17773777. This address can be disabled after a successful boot to allow another device on the UBA or UNIBUS to respond to this address range. This address range is automatically enabled at power up or after the restart switch is enabled regardless of this parameter.

Table 3–9 describes the variations of this parameter.

Table 3–9 ROM on 173000 Parameter Variations

Value	Description
0	KDJ11-E ROM code disabled.
1	KDJ11-E responds to addresses 17773000 - 17773777. **Factory setting.**

C - Rom on 165000

This parameter allows you to disable the ROM. It sets/resets bit 6 of the CSR at address 17777520 just before transferring control to another boot program.

Table 3–10 describes the variations of this parameter.

Table 3–10 ROM on 165000 Parameter Variations

Value	Description
0	The KDJ11-E does not respond to address 17765000-17765777. **Factory setting.**
1	Enables internal EEPROM or the BOOT EPROM to respond to addresses 17765000-17765777.

D - Power-up Mode and E - Restart Mode

There are four mode choices for either the Power-up Mode or the Restart Mode:

- Dialog Mode
- ODT Mode
- 24 Mode
- Automatic Boot Mode

When the ROM code is started, it checks a status bit to determine if the unit is powering-up or if the restart switch was activated. The ROM code then uses the appropriate mode selected. You can define the action taken by the ROM code at power-up or restart to be the same or different.

- Dialog Mode

  In Dialog Mode, all selected tests are executed at power-up unless power-up Self-tests are disabled. Dialog Mode allows you to:

  - Boot a device
  - List boot programs available
  - Run ROM resident tests
  - Print a map of all I/O page locations
  - Enter Setup Mode to list and change all parameters in the EEPROM.
  - Enter time and date for TOY clock.

- ODT Mode

  At completion of a very limited set of tests, the ROM code executes a halt instruction and passes control to J11 micro ODT. This mode is used in debug environments. The ROM code does not change any locations in memory before entering ODT mode. See Section 3.7.

- 24 Mode

  At completion of a limited set of tests, the ROM code loads the PSW with the contents of location 26 and then transfers control to the address located in location 24. This mode is used when power fail recovery is desired.

  Power fail recovery is possible if the battery backup option is present or the standby position of the front panel key switch is being used.

- Automatic Boot Mode

  In Automatic Boot Mode, all selected tests are executed at power-up unless power-up Self-tests are disabled.

  NOTE
  If the force dialog switch (S5 on the console/SLU panel assembly) is on, the ROM code enters Dialog Mode at power-up or restart regardless of the selections in the EEPROM.

  The ROM code enters an automatic boot routine that tries to boot a previously selected device or devices. The list of devices can be from 1 to 6 devices long. Each device is tried sequentially until a successful boot occurs or the end of the boot table is reached.

  ROM Mode is a special Automatic Boot Mode that is entered as a power-up/ restart option to boot specific devices when one or more of switches 2-4 on the console/SLU panel are set.

  When switches 2-4 of the console/SLU panel are set to one of the six combinations shown in Table 3–11 and force dialog mode is not selected, ROM mode is entered. The mode attempts to boot only the one device selected by this command. If the boot is unsuccessful, the ROM code prints out the normal error message and enters dialog mode.

Table 3–11 ROM Mode Switch Settings

Switches	Settings	Description
2 3 4	off off off	Normal Automatic Boot Mode.
2 3 4	on on off	Device 1 in list/change boot parameters.
2 3 4	on off on	Device 2 in list/change boot parameters.
2 3 4	on off off	Device 3 in list/change boot parameters.
2 3 4	off on on	Device 4 in list/change boot parameters.
2 3 4	off on off	Device 5 in list/change boot parameters.
2 3 4	off off on	Device 6 in list/change boot parameters.

NOTE
See Section 3.5.6.5 to add or delete devices from the boot device block.

F - Power-on Self-tests

After a power-up sequence, the diagnostic tests contained in the ROM code are executed. Control is passed to the ROM code and a comprehensive set of diagnostic tests check the KDJ11-E and UNIBUS Adapter. Upon completion of the on-board diagnostics, control is passed to the previously selected power-up mode option.

NOTE
The force dialog switch (S5) on the console/SLU panel must be off.

Table 3–12 describes the variations of this parameter.

Table 3–12 Power-on Self-tests Parameter Variations

Value	Description
0	No Self-tests performed after a power-up.
1	Self-testing performed after a power-up. **Factory setting.**

NOTE
Power-on Self-tests are not executed if:

- **If the Power-up Mode is set to Trap-24.**
- **If the Power-up Mode is set to ODT.**
- **If the ROM code is entered via the RESTART switch on the front panel.**

G - Alternate Boot Block

When you attempt to boot a device, the ROM code does not transfer control to the booted device unless the device looks *bootable.*

Some *poking around* is done by the ROM code to ensure control is never passed to unbootable media. For example, a blank pack may have been mounted in a disk drive by mistake.

The boot block on all bootable PDP-11 software distributed by Digital Equipment Corporation has the following format:

- Location 0 can range from 240 to 277. Normally this location contains a no operation command (240).

- Location 2 can range from 400 to 777. This is an unconditional branch instruction.

Table 3–13 describes the variations of this parameter.

Table 3–13 Alternate Boot Block Parameter Variations

Value	Description
0	Standard format bootblock. **Factory setting.** If this parameter is set to 0, the ROM code looks for memory location 0 to be a value of 240 to 277 and for memory location 2 to be 400 to 777. If the data found is within the the preceding ranges, the ROM code assumes that bootable media is present. At this point, the ROM code passes control to the secondary boot program starting at memory address 0. If the data in memory location 0-2 is not within the range specified above, the ROM code will type out an error message indicating that the media is not bootable. (Bootblock Error)
1	Non-standard format for the bootblock. No poking around is done by the ROM code to determine if the media is bootable. All the ROM code does is verify that memory location 0 does not contain a halt instruction. (000000) When this parameter is set to 1 the ROM code looks for location 0 of the Bootblock to be any non zero number. If a non zero number if found control is passed unconditionally to the secondary boot starting at memory location 0. This allows you to boot media that is in non-standard format.

NOTE
The Rom code checks location 0-2 after the bootblock (normally block 0) is loaded into memory.

NOTE
USERBOOT programs are not checked to see if they are bootable.

H - LTC Register

Table 3–14 describes the variations of this parameter.

Table 3–14 LTC Register Parameter Variations

Value	Description
0	Disables the KDJ11-E Line Time Clock Register to allow you to place a customer time clock at this address.
1	Enables the KDJ11-E Line Time Clock Register. **Factory setting.**

I - Force Clock Interrupt

Table 3–15 describes the variations of this parameter.

Table 3–15 Force Clock Interrupt Parameter Variations

Value	Description
0	**Factory setting.** The clock can request interrupts only if: • The clock CSR is enabled, parameter H LTC Register = 1 • The interrupt enable bit, CSR bit 6, is set at address 17777546. • The processor priority is 5 or less.
1	The clock unconditionally requests interrupts when the processor priority is 5 or less.

NOTE

If Force Clock Interrupt is selected, always disable the clock CSR, since the CSR has no control over the clock.

J - Clock Frequency

This parameter determines the source of the clock to be used.

Table 3–16 describes the variations of this parameter.

Table 3–16 Clock Frequency Parameter Variations

Value	Source
0	Clock sourced from power supply, at backplane pin BR1. The power supply drives this signal at 50 or 60 Hz. **Factory setting.**
1	Clock sourced internally at 50 Hz from KDJ11-E.
2	Clock sourced internally at 60 Hz from KDJ11-E.
3	Clock sourced internally at 800 Hz from KDJ11-E.

K - Halt on Break

Table 3–17 describes the variations of this parameter.

Table 3–17 Halt on Break Parameter Variations

Value	Description
0	Console breaks are ignored from the Break key on terminal. **Factory setting.**
1	Enables the processor to halt if the console SLU detects a break condition from the Break key on terminal.

L - Trap on Halt

Table 3–18 describes the variations of this parameter.

Table 3–18 Trap on Halt Parameter Variations

Value	Description
0	**Factory setting.** The processor enters J11 micro ODT if a halt instruction is executed in kernel mode.
1	The processor traps to location 4 if a halt instruction is executed in kernel mode.

M - Ignore Battery

This parameter is used only when the current power up or restart mode is set to 24 (3).

Table 3–19 describes the variations of this parameter.

Table 3–19 Ignore Battery Parameter Variations

Value	Description
0	**Factory setting.** The battery OK signal must be present to execute mode 24. Battery OK indicates that the memory contents were not corrupted as a result of a power failure. If BOK is not set, TRAP24 mode is not executed and Dialog Mode is entered.
1	TRAP24 mode is executed regardless of the status of the battery OK bit. This mode is used if you have custom battery back-up hardware. In this case, the battery OK bit may not reflect the actual state of the memory on the KDJ11-E.

N - Lines on

This parameter allows you to select the starting address/vector of serial lines 1-7. The priority level is set to 4 and cannot be changed.

To select other parameters for SLUs 1-7 (such as baud rate, number of data bits, stop bits or parity), use Setup Mode Command 4 (Section 3.5.6.4).

Table 3–20 describes the variations of this parameter.

NOTE

After selecting and saving the desired starting address, the system must be powered down and then rebooted for the change to occur.

Table 3–20 Lines On Parameter Variations

Value	Description
0	Disables SLUs 1-7. SLUs do not respond to any address and cannot be accessed.
1	SLUs respond to the following addresses/vectors:

UNIBUS Address	Vector	SLU Number
176500	300	1
176510	310	2
176520	320	3
176530	330	4
176540	340	5
176550	350	6
176560	360	7
176570	*370*	*8*
		Line 8 is included in the list **only** if the console/SLU is disabled. The console/SLU is disabled if Switch 1, Disable Console Serial Line Unit, located on the Console/SLU Panel is set to the on position. In this case a console SLU, a DL11 for example, must be provided by the user.

2	SLUs respond to the following addresses/vectors:

UNIBUS Address	Vector	SLU Number
176600	400	1
176610	410	2
176620	420	3
176630	430	4
176640	440	5
176650	450	6
176660	460	7
176670	*470*	*8*
		Line 8 is included in the list **only** if the console/SLU is disabled. The console/SLU is disabled if Switch 1, Disable Console Serial Line Unit, located on the Console/SLU Panel is set to the on position. In this case a console SLU, a DL11 for example, must be provided by the user.

O - Disable UBA ROM

Table 3–21 describes the variations of this parameter.

Table 3–21 Disable UBA ROM Parameter Variations

Value	Description
0	Enables the UBA ROMs. **Factory setting.**
1	Disables the UBA ROMs. This allows other ROM boards on the UNIBUS to show up in the UBA ROM address range of 17773000 to 17773776.

NOTE

If the ROM code is booting directly from a M9312 type boot ROM located on the M9312 module, the ROM code automatically disables the CPU ROM in the 17773nnn address range and the ROMs on the UBA module and uses the ROMs on the M9312 module. This action is taken regardless of the status of the disable UBA ROM parameter and the disable ROM parameter.

P - Enable UBA 18-Bit Mode

Table 3–22 describes the variations of this parameter.

Table 3–22 Enable UBA 18-Bit Mode Parameter Variations

Value	Description
0	Selects 22-bit addressing. **Factory setting.**
1	Selects 18-bit addressing.

3.5.6.3 Setup Mode Command 3 - Select Diagnostic Configuration

This parameter allows you to select or deselect individual tests from Example 3–10. The tests selected here are run when Power-on Self-tests (Section 3.5.6.2) and the Diagnostic Command (Section 3.5.2) are enabled.

NOTE

To run the Diagnostic Command, changes to the Self-test Menu do not need to be saved.

To execute the Setup Mode Command 3:

1. At the command line on the Setup Menu, type 3.
2. Press Return.

The following is an example of Setup Mode Command 3:

```
KDJ11-E Monitor  Version 1.06 18-May-1990
(C) Digital Equipment Corporation 1990

A  Nr. 67 CPU Test                  (0) =  No  (1) =  Yes    = 1
B  Nr. 66 MMU Test                  (0) =  No  (1) =  Yes    = 1
C  Nr. 65 Pre-Console Test          (0) =  No  (1) =  Yes    = 1
D  Nr. 64 MSER Test                 (0) =  No  (1) =  Yes    = 1
E  Nr. 63 CCR r/w Test              (0) =  No  (1) =  Yes    = 1
F  Nr. 62 HIT/MISS-Reg Test         (0) =  No  (1) =  Yes    = 1
G  Nr. 61 LTC Speed Test            (0) =  No  (1) =  Yes    = 1
H  Nr. 60 Add-Stat-Reg Test         (0) =  No  (1) =  Yes    = 1
I  Nr. 57 CPU-Err-Reg Test          (0) =  No  (1) =  Yes    = 1
J  Nr. 55 UBA reg. resp. Test       (0) =  No  (1) =  Yes    = 1
K  Nr. 54 Address 0 Test            (0) =  No  (1) =  Yes    = 1
L  Nr. 53 Pre-Memory (0-4KW) Test   (0) =  No  (1) =  Yes    = 1
M  Nr. 52 FPA Register Test         (0) =  No  (1) =  Yes    = 1
N  Nr. 51 FPA Function Test         (0) =  No  (1) =  Yes    = 1
O  Nr. 50 Int Mem Address Test      (0) =  No  (1) =  Yes    = 1
P  Nr. 47 Int Mem Data Test         (0) =  No  (1) =  Yes    = 1
Q  Nr. 46 PIRQ-Reg Test             (0) =  No  (1) =  Yes    = 1
R  Nr. 45 LTC Int Test              (0) =  No  (1) =  Yes    = 1
S  Nr. 44 Lines Config. Test        (0) =  No  (1) =  Yes    = 1
T  Nr. 43 Serial Lines Test         (0) =  No  (1) =  Yes    = 1
U  Nr. 40 Memory parity Test        (0) =  No  (1) =  Yes    = 1
V  Nr. 37 UBA map reg Test          (0) =  No  (1) =  Yes    = 1
W  Nr. 36 UBA NPR Cycle Test        (0) =  No  (1) =  Yes    = 1
X  Nr. 32 Loopback SLU Test         (0) =  No  (1) =  Yes    = 0
Y  Nr. 31 Extended Memory Test      (0) =  No  (1) =  Yes    = 0
Z  Nr. 30 All Selected Tests        (0) =  No  (1) =  Yes    = 0
Type CTRL Z to exit or press Return key to proceed
```

Example 3–10 Setup Command 3 - Self-Test Menu

3.5.6.4 Setup Mode Command 4 - Select Serial Line Parameters

This command prints out the current status of selectable parameters for SLUs 1-7 and then allows you to change them if desired.

The following parameters can be modified for SLUs 1-7:

Parameter	Values
Baud rate	300, 600, 1200, 2400, 4800, 9600, 19200, 38400
Number of data bits	7, 8
Number of stop bits	1 or 2
Parity	Even, odd, or disabled

To execute the Setup Mode Command 4:

1. At the command line on the Setup Menu, type 4.
2. Press Return.

The following is an example of Setup Mode Command 4:

```
>KDJ11-E Monitor  Version 1.06 08-May-1990
 (C) Digital Equipment Corporation 1990

A  Line 1  Baudrate              (0) =   300
                                 (1) =   600
                                 (2) =  1200
                                 (3) =  2400
                                 (4) =  4800
                                 (5) =  9600
                                 (6) = 19200
                                 (7) = 38400                    = 5

   Line 1  Data bits             (0) =  8      (1) =  7         = 0

   Line 1  Stop bits             (0) =  2      (1) =  1         = 1

   Line 1  Parity                (0) = Even
                                 (1) =  Odd
                                 (2) =  Dis                     = 2
.
.
.
.
.

G  Line 7  Baudrate              (0) =   300
                                 (1) =   600
                                 (2) =  1200
                                 (3) =  2400
                                 (4) =  4800
                                 (5) =  9600
                                 (6) = 19200
                                 (7) = 38400                    = 5

   Line 7  Data bits             (0) =  8      (1) =  7         = 0

   Line 7  Stop bits             (0) =  2      (1) =  1         = 1

   Line 7  Parity                (0) = Even
                                 (1) =  Odd
                                 (2) =  Dis                     = 2

Type <CTRL> Z to exit or press Return key to proceed
```

Example 3–11 Setup Mode Command 4

3. If you do not want to change any parameters, enter Ctrl Z to return to the Setup Menu.

4. If you want to change parameters, there are two methods you can use to position the program at the parameter you want to change:
   a. Press [Return] until positioned at the parameter to be changed.
   b. Type one of the following letters:
      A To change parameters for line 1.
      B To change parameters for line 2.
      C To change parameters for line 3.
      D To change parameters for line 4.
      E To change parameters for line 5.
      F To change parameters for line 6.
      G To change parameters for line 7.
5. Press [Return]. The ROM code proceeds to the next parameter.

NOTE
The following parameters are fixed for the console/SLU:

Baud rate	Set by using switches 6,7,8 of the console/SLU panel.
Number of data bits	8
Number of stop bits	1
Parity	None

3.5.6.5 Setup Mode Command 5 - Select Boot Parameters

This parameter allows you list current boot parameters for the Powerup/Restart mode of Autoboot and to modify the Autoboot table.

To execute the Setup Mode Command 5:

1. At the command line on the Setup Menu, type 5.
2. Press [Return].

The following is an example of Setup Mode Command 5:

```
KDJ11-E Monitor  Version 1.06 18-May-1990
(C) Digital Equipment Corporation 1990

List/change boot parameter

                                        Device Unit Address
Boot 2: Switches 2,3,4 on  off on   = DL ROM   0  Default
Boot 3: Switches 2,3,4 on  off off  = TT USR   0  000000
Boot 4: Switches 2,3,4 off on  on   = DL UBA   0  Default
Boot 5: Switches 2,3,4 off on  off  = blank
Boot 6: Switches 2,3,4 off off on   = blank

Type CTRL Z to exit or press Return key to proceed
```

Example 3–12 Setup Mode Command 5 - Boot Parameters Menu

3. If you want to return to the Setup Menu, enter [Ctrl] [Z].
4. To proceed, press [Return].

The following is an example:

```
Boot 1: Switches 2,3,4 on  on  off  = DM ROM   0  Default
❶Device name   =
❷Boot location  (0) = USR  (1) = ROM  (2) = UBA  (3) = M93  = 1
❸Unit number   = 0
❹Address       =

Boot 2: Switches 2,3,4 on  off on   = DL ROM   0  Default
Device name   =
```

❶ Device Name

The ROM Code prompts you for a device name. The previous mnemonic is displayed. You can change the device by typing a new two-letter mnemonic associated with the device to be selected. Pressing [Return] leaves the parameter unchanged.

Table 3–23 lists the default boot programs in the CPU ROM. Your system may contain boot programs that are not on this list.

Table 3–23 Default Boot Programs

Device Name	Unit Numbers	Source	Device Type
DU	0-255	ROM	MSCP (RAxx, RDxx, RX50, RC25, ...)
DL	0-3	ROM	RL01/RL02
DX	0-1	ROM	RX01
DY	0-3	ROM	RX02
MS	0-1	ROM	TK25, TS04/05/11, TU80
MT	0-1	ROM	TU10, TE10, TS03
MU	0-255	ROM	TMSCP (TK50, TU81, ...)

NOTE
To print a complete list of all available bootstraps and associated mnemonics, use the List Command.

❷ Boot Location

The ROM code requires you to enter the location of the boot code. The default is the the standard on-board ROM.

Where:

USR	User previously created a User Boot. Boot code is located in the User Boot area.
ROM	Standard default area.
UBA	M9312-type ROMs located in the ROM sockets of the UNIBUS Adapter Module.
M93	M9312-type ROMs located in the ROM sockets of the optional M9312 module on the UNIBUS.

❸ Unit Number

The ROM code prompts for the unit number. Type in the unit number of the device to be booted.

❹ Address

To select the default address press Return.

Enter an address if the device CSR is set at a non-standard or floating address.

The ROM code continues to prompt for all six boot entries in Example 3–12.

If you do not want to change any items in Example 3–12, press Ctrl Z to return to the Setup Command Menu. You can also skip any entry by pressing Return for each entry you want to skip.

The ROM code continues to prompt for all six entries in Example 3–12.

Autoboot Mode

This parameter allows you to select the devices to be tried in the automatic boot sequence. You can create a list that defines the devices and the order in which they are tried. One entry is needed to define a device and its unit number. If the same device is used more than once with different unit numbers, then one entry is needed for each unit number. The ROM code attempts to boot the devices you have defined in Example 3–12, starting with boot 1. If the Autoboot is unsuccessful, an error message is printed and the ROM code enters Dialog Mode.

ROM Mode

ROM Mode is entered when Autoboot is selected as a Powerup/Restart option and one or more of switches 2-4 of the console/SLU panel are set.

When switches 2-4 of the console/SLU panel are set to one of the six combinations shown in Table 3–24 and force dialog mode is not selected, the ROM code enters a special Autoboot Mode called ROM Mode. ROM mode attempts to boot only the one device selected by this command. If the boot is unsuccessful, the ROM code prints out the normal error message and enters dialog mode.

Table 3–24 ROM Mode

Switches	Settings	Description
2 3 4	off off off	Normal Automatic Boot Mode.
2 3 4	on on off	Device 1 in list/change boot parameters.
2 3 4	on off on	Device 2 in list/change boot parameters.
2 3 4	on off off	Device 3 in list/change boot parameters.
2 3 4	off on on	Device 4 in list/change boot parameters.
2 3 4	off on off	Device 5 in list/change boot parameters.
2 3 4	off off on	Device 6 in list/change boot parameters.

3.5.6.6 Setup Mode Command 6 - List Available Boot Programs

To execute the Setup Mode Command 6:

1. At the command line on the Setup Menu, type 6.
2. Press Return.

The following is an example of Setup Mode Command 6:

```
KDJ11-E Monitor  Version 1.06 18-May-1990
(C) Digital Equipment Corporation 1990
❶       ❷
Device  Unit     ❸      ❹
Name    Numbers Source Device Type

AB      0        USR
TT      0        USR
DU      0-255    ROM    MSCP (RAxx, RDxx, RX50, RC25, ...)
DL      0-  3    ROM    RL01/RL02
DX      0-  1    ROM    RX01
DY      0-  3    ROM    RX02
MS      0-  1    ROM    TK25, TS04/05/11, TU80
MT      0-  1    ROM    TU10, TE10, TS03
MU      0-255    ROM    TMSCP (TK50, TU81, ...)
DL      0-  3    UBA    RL01/RL02

Press RETURN key when ready to continue
```

Example 3–13 Setup Mode Command 6

❶ The device name is a two-letter mnemonic. The device name must be the letters from A to Z. At input, the ROM code converts all lower case letters to upper case.

❷ The unit number range is the allowable range of unit numbers that is valid for a particular boot program. The range varies from 0 to 255, depending on the device. If the unit name range information is blank, the ROM code assumes the range limit is 0 to 255.

❸ The source lists where the actual boot program is located:

Physical Location of Boot ROM	Source
CPU ROM	ROM
ROM Sockets on the UNIBUS adapter module	UBA
M9312	M93
User Boot Area	USR

❹ The Device Type is a description of the device to be booted. It is the name on the outside of the device to be booted. For example, the description for a device name DL is RL02, which is the name on the outside of the physical device.

The mnemonic for each ROM found on either the UBA or the M9312 is checked against the list of mnemonics in the ROM code. If the mnemonic matches an item in this list, the ROM code prints out a description of that device. If no match is found, the description is left blank for that mnemonic.

3.5.6.7 Setup Mode Command 7 - Factory Setting

This command initializes the current contents of the values in the Setup Menu table to the default factory settings.

To execute the Setup Mode Command 7:

1. At the command line on the Setup Menu, type 7.
2. Press Return.

The following is an example of Setup Mode Command 7:

```
KDJ11-E Monitor  Version 1.06 08-May-1990
(C) Digital Equipment Corporation 1990

Factory setting
```

Example 3–14 Setup Mode Command 7

3. If you want to save the values in the Setup table into the EEPROM, execute Setup Mode Command 8.

3.5.6.8 Setup Mode Command 8 - Save The Setup Table In The EEPROM

This command permanently saves the current parameters of the Setup table in memory into the EEPROM.

To execute the Setup Mode Command 8:

1. At the command line on the Setup Menu, type 8.
2. Press Return.

The following is an example of Setup Mode Command 8:

```
KDJ11-E Monitor  Version 1.06 08-May-1990
(C) Digital Equipment Corporation 1990

Saving setup table in the EEPROM, please wait
```

Example 3–15 Setup Mode Command 8

3.5.6.9 Setup Mode Command 9 - Load EEPROM Data Into The Setup Table

This command restores the Setup table in memory with the values stored in the EEPROM during the last save. You can also restore the Setup table after making temporary changes.

To execute the Setup Mode Command 9:

1. At the command line on the Setup Menu, type 9.
2. Press Return.

The following is an example of Setup Mode Command 9:

```
KDJ11-E Monitor  Version 1.06 08-May-1990
(C) Digital Equipment Corporation 1990

Load EEPROM data into the setup table
```

Example 3–16 Setup Mode Command 9

3.5.6.10 Setup Mode Command 10 - Load EEPROM Boot Program Into Memory

When this command is executed, the ROM code loads a previously created user boot program. The ROM code asks for the device name of an EEPROM boot to be loaded in memory.

To execute the Setup Mode Command 10:

1. At the command line on the Setup Menu, type 10.
2. Press Return.

The following is an example of Setup Mode Command 10:

```
KDJ11-E Monitor  Version 1.06 08-May-1990
(C) Digital Equipment Corporation 1990

Loading EEprom boot program

Type CTRL Z to exit or press Return key to proceed
```

Example 3–17 Setup Mode Command 10

3. Enter the two-letter mnemonic of the boot program to load:

```
Device name        =        New = TT
```

NOTE
Setup Mode Command 10 loads the program only. To examine or edit the userboot program, use Setup Mode Command 11.

3.5.6.11 Setup Mode Command 11 - Edit or Create EEPROM Boot Program

This command is used to either create a new EEPROM boot program or to edit a program previously loaded using Setup Mode Command 10.

You can change or enter:

- Device name

  CAUTION
  Do not assign the same device name for any boot programs.

- Beginning address of the user boot program
- Ending address of the user boot program
- Start address
- Highest unit number
- Device description

When these changes are complete, the ROM code enters ROM ODT which is a ROM code version of J11 micro ODT. When this command is first entered, it lists the available space in the EEPROM for boots.

CAUTION
After creating or editing a user boot program, use Setup Mode Command 12 to save it. If you do not save the program, it is lost.

To execute the Setup Mode Command 11:

1. At the command line on the Setup Menu, type 11.
2. Press Return.

The following is an example of Setup Mode Command 11:

```
KDJ11-E Monitor  Version 1.06 08-May-1990
(C) Digital Equipment Corporation 1990

User boot editor

Type CTRL Z to exit or press Return key to proceed

11630 Bytes free in the EEPROM

❶Device name                          = TT            New =

❷Beginning address                    = 01000         New =

❸Last byte address                    = 01010         New =

❹Start address                        = 01000         New =

❺Highest unit number                  = 000           New =

❻Device description                   =               New = test

❼Enter ROM ODT

xxxxxx/ = open word location xxxxxx if address even; byte if odd
RETURN  = close location
. or LF = close location and open next
  -     = close location and open previous

ROM ODT >
```

Example 3–18 Setup Mode Command 11

❶ *Device name* is a two-letter Mnemonic for the boot program to be created.

❷ *Beginning address* is the first location of the program in memory. The Address range is 1000-17544.

The ROM code prints out the old starting address and prompts you for a new starting address. Type in a new address or press Return to accept the old starting address.

❸ *Last byte address* is the address of the last byte of code used in memory. If in doubt, use the last address of data + 2 for this value. Do not use a much larger number to avoid wasting EEPROM space.

The ROM code prints out the old ending address and prompts you for a new ending address. Type in a new address or press Return to accept the old ending address.

❹ *Start address* is the address that the ROM code passes control to. The start address does not have to be the same as the beginning address but it must be even and a value in the range defined by the beginning and ending addresses.

5. *Highest unit number* defines the allowable range of valid unit numbers for this device. If the value is set to 3, the allowable range is 0 to 3. If a unit number is typed in at boot time and it is not in range, an invalid unit number error occurs.

6. *Device description* is an optional but recommended description of the device name. The name should be the name that is physically marked on the outside of the device (i.e. RA82).

NOTE
After entering the device description, ROM ODT is automatically entered.

7. *Enter ROM ODT* - At this time, a new program can be entered or an existing program can be edited/examined using ROM ODT. ROM ODT uses the commands in Table 3–25.

Table 3–25 ROM ODT Commands

Command	Symbol	Description
Slash	/	Prints contents of specified location or if no address is defined, then the contents of the last location that was opened prints. If the location opened is an odd number, then only the contents of the byte prints. If location is even, the mode is word. If location is odd, the mode is byte. Leading zero's are assumed. Only bits 15 through zero of the address are used.
Return	<CR>	Closes an open location.
Line Feed	<LF>	Closes an open location and opens the next location. If the mode is word, the address is incremented by 2. If the mode is bytes, the address is incremented by 1.
Period	.	Alternate character for line feed. This command is useful when the terminal is a VT2xx series terminal. It is also convenient to use with the keypad.
Minus	-	Alternate character for the up arrow on the cursor control keypad. This command is useful when the terminal is a VT2xx series terminal. It is also convenient to use with the keypad.
Delete	DELETE	Deletes the previously typed character.
CTRL Z	^Z	Exits ROM ODT and returns to Setup mode.

CAUTION
After creating or editing a user boot program, use Setup Mode Command 12 to save it. If you do not save the program, it is lost.

To exit ROM ODT mode, press Ctrl Z.

3.5.6.12 Setup Mode Command 12 - Save a Boot Program In The EEPROM

This command allows you to save the user boot program created or edited in Setup Mode Command 11 into the EEPROM. This is the only command that actually writes a boot into the EEPROM.

When saving a boot program into memory, the device name of the program **must not** match the name of an existing program in the EEPROM. If the program name already exists, you must delete that program first or change the name of the program to be saved. If two or more programs are written into the EEPROM with the same name, only the first one is bootable.

CAUTION
If you create or edit a program and do not save it, the program is lost.

NOTE
The save procedure can take up to two minutes at the full length of 8 Kbytes.

To execute the Setup Mode Command 12:

1. At the command line on the Setup Menu, type 12.
2. Press Return.

The following is an example:

```
KDJ11-E Monitor  Version 1.06 08-May-1990
(C) Digital Equipment Corporation 1990

Saving boot program

Are you sure  Y/N ? Y

Saving Boot,wait
```

3.5.6.13 Setup Mode Command 13 - Delete a Saved EEPROM Boot Program

This command allows you to delete an EEPROM boot. If this command is executed the ROM code ask for the device name of the EEPROM boot to be deleted. After the device name is inputted, the ROM code looks for the first boot program in the EEPROM and if found, deletes it.

To execute Setup Mode Command 13:

1. At the command line on the Setup Menu, type 13.
2. Press Return.

   The following is an example of Setup Mode Command 13:

```
KDJ11-E Monitor  Version 1.06 08-May-1990
(C) Digital Equipment Corporation 1990

Del saved boot

Type CTRL Z to exit or press Return key to proceed

Device name       = TT        New = JP
```

Example 3–19 Setup Mode Command 13

3. Press Return. The following displays:

```
Are you sure?  Y/N?
```

3.5.6.14 Setup Mode Command 14 - Enter ROM ODT

This command enters ROM ODT. The ROM code opens up the address defined by the beginning address of the program. ROM ODT is not the same as J11 micro ODT. The only purpose of ROM ODT is to allow the user to create or edit a small bootstrap program to be stored in the EEPROM.

In ROM ODT, the only allowable addresses that can be examined are the addresses of memory from 0-28 KW (0-00157776). Any other addresses and any attempt to access the I/O page or any registers are not allowed.

Rom ODT uses the commands in Table 3–25.

To execute the Setup Mode Command 14:

1. At the command line on the Setup Menu, type 14.
2. Press Return.

   The following is an example of Setup Mode Command 14:

```
KDJ11-E Monitor  Version 1.06 08-May-1990
(C) Digital Equipment Corporation 1990

Enter ROM ODT

xxxxxx/ = open word location xxxxxx if address even; byte if odd
RETURN  = close location
. or LF = close location and open next
  -     = close location and open previous

ROM ODT >
```

Example 3–20 Setup Mode Command 14

3. To exit ROM ODT mode and return to the Setup Menu, press Ctrl Z.

3.5.7 TOY Command

The TOY Command allows you to change the time and date of the TOY clock. The time is in 24 hour format.

To execute the TOY command:

1. Enter T.
2. Press Return.

The following is an example of the TOY Command:

```
KDJ11-E Monitor  Version 1.06 23-May-1990
(C) Digital Equipment Corporation 1990
Unibus System
Memory    2048 KW
EEprom       4 KW
Time     15:44:37 30-May-90 Wed

Commands are: [Boot, Diagnostic, Help, List, Map, Setup, Toy]
Type a command then press the RETURN key: T

KDJ11-E Monitor  Version 1.06 08-May-1990
(C) Digital Equipment Corporation 1990

Set time and date

Use following format:
For time: HH:MM:SS          For date: DD-MMM-YY

Time:  15:45:20
Input:
Date:  16-May-90
Input:

Commands are: [Boot, Diagnostic, Help, List, Map, Setup, Toy]
Type a command then press the RETURN key:
```

Example 3–21 TOY Command

3.6 Video Terminal Support

This section describes how to operate the PDP-11/94-E using video terminal support.

3.6.1 Moving Through the Menus

Table 3–26 describes how to move through or execute instructions in the menus.

Table 3–26 Moving Through Menus

Key	Function
Return	Executes a Do or an Edit.
Space bar	Selects the next value for a parameter.
Backspace	Selects the previous value for a parameter.
Tab	In the Setup Menu, moves the cursor to the Save parameter. To save changes, enter Return.
	In the Self-test Menu, moves the cursor to the Monitor parameter. To return to the Setup Menu, enter Return.
	In the User Boot Menu, moves the cursor to the Exit parameter. To return to the Setup Menu, enter Return.
	In the Map Menu, returns you to the Setup Menu.
↑	Moves the cursor up to the next parameter.
↓	Moves the cursor down to the next parameter.
→	Moves the cursor to the next parameter on the right.
←	Moves the cursor to the next parameter on the left.
H	Displays a list of all boot programs while in the boot device block.
Ctrl C or Ctrl P	Ends Self-test and returns you to the Setup Menu.

3.6.2 Types of Function Fields - Video Terminal

Each menu contains function fields which allow you to perform a specific operation. There are three types of function fields which are described in Table 3–27.

Table 3–27 Types of Function Fields

Field	Function
Edit	This is an executable function. When entered, Edit brings you to a sub-menu such as Self-test, User Boot, or Map. You can make modifications through the sub-menu. Not all fields can be edited.
Do	This is an executable function. When selected, Do executes a specific operation after pressing Return.
Addresses	Allows you to enter addresses directly in an octal format.

3.6.3 Setup Menu

The Setup Menu lists all the parameters in the EEPROM including boot parameters. Use the Setup Menu to modify these parameters. A Setup Menu is show in the Example 3–22, Setup Menu.

```
KDJ11-E Monitor  Version 1.06 18-May-1990
(C) Digital Equipment Corporation 1990
Unibus System
Memory     2044 KW
EEprom        4 KW
❶Time      16:17:45 18-May-90 Fri

❷Nr Device Unit Address
 1 DU ROM   0  Default Do
 2 DL ROM   0  Default Do
 3 TT USR   0  000000  Do
 4                     Do
 5                     Do
 6                     Do

❸Lines  Address/Vec  Baud   Data  Stop  Par
Line 1  176500/300   9600   8     1     Dis
Line 2  176510/310   9600   8     1     Dis
Line 3  176520/320   9600   8     1     Dis
Line 4  176530/330   9600   8     1     Dis
Line 5  176540/340   9600   8     1     Dis
Line 6  176550/350   9600   8     1     Dis
Line 7  176560/360   9600   8     1     Dis
```

❹

```
Disable UBA ROM                 No
Enable UBA 18-Bit Mode          No
Memory Intern                 4MB
Rom on 173000                 Yes
Rom on 165000                  No
Power-up Mode              Dialog
Restart Mode               Dialog
Power-on Self-tests            Yes
Select Self-tests             Edit
User Boot                     Edit
Alternate Boot Block            No
LTC Register                   Yes
Force Clock Interrupt           No
Clock Frequency                P/S
Halt on Break                   No
Trap on Halt                    No
Ignore Battery                  No
Lines on                   176500
Map                             Do
Factory Setting                 Do
Save                            Do
```

Example 3–22 Setup Menu

❶ The time and date of the TOY is displayed here. To change the time/date:

1. Move the cursor to the Time field and press Return.
2. Enter the new time/date in the following format:

   NOTE
   Use the → to move from the time to the date.

   HH:MM:SS DD-MMM-YY

3. Press Return. The day is automatically entered.

❷ The boot device block contains 6 lines which are divided into 5 sections:

Nr	Represents the sequence number.
Dev	A two letter mnemonic which represents a boot program and its location.
Unit	represents the unit number to be booted from. The spacebar moves you to the next unit number.
Address	Default is the standard address. If the device is set at a non-standard address, enter a new address.
Do	Executes the boot for that line.

Each line of this boot device block provides you with 12 different boot devices with corresponding units and the source where the actual boot program is located. As a default setting, 3 boot devices have been set at the factory. To change the boot device, move the cursor to the device and press the space bar to display a different device.

A list of resident supported boot devices can be displayed by positioning the cursor any where within the boot device block and pressing [H]. An example follows:

```
KDJ11-E Monitor  Version 1.06 18-May-1990
(C) Digital Equipment Corporation 1990

Device  Unit
Name    Numbers Source Device Type

AB      0       USR
DU      0-255   ROM    MSCP (RAxx, RDxx, RX50, RC25, ...)
DL      0-  3   ROM    RL01/RL02
DX      0-  1   ROM    RX01
DY      0-  3   ROM    RX02
MS      0-  1   ROM    TK25, TS04/05/11, TU80
MT      0-  1   ROM    TU10, TE10, TS03
MU      0-255   ROM    TMSCP (TK50, TU81, ...)
XH      0       ROM    ETHERNET
DL      0-  3   UBA    RL01/RL02

Press RETURN key when ready to continue
```

Example 3–23 Resident Supported Boot Devices

In the previous display:

- AB represents a user boot program that is named AB.
- The second DL represents the ROM location on the UBA module.

❸ The SLU setup block individually sets the baud rate and character format for each channel as follows:

Baud rate range	300-38400
Data bits	Eight bits* Seven Bits
Stop bits	Two stop bits One stop bit*
Parity	Even Odd No parity*

*Default setting

NOTE
The status of the setup is only read during power-up or an INIT. Changes in the SLU settings are not implemented until completion of a successful boot.

❹ Configuration parameters allow you to enable or disable various functions or change the values of others. Table 3–28 describes each parameter.

Table 3–28 Setup Menu Configuration Parameters

Parameter	Description	Values
Disable UBA ROM	Controls the ROMs located on the UBA.	**Yes** disables the four ROM sockets. **No (factory setting)** enables the UBA ROMs. It is ignored when you try to boot the UBA or the M9312 boot ROMs.
Enable UBA 18-Bit Mode	Selects 18- or 22-bit addressing modes. Its status is copied into bit 5 of the UBA KTJ11 Memory Configuration Register (KMCR).	**Yes** enables the memory to use 18-bit addressing. **No (factory setting)** enables the memory to use 22-bit addressing.
Memory Intern	Allows you to disable the top 2MB of memory on a 4MB board. If the amount of memory selected does not match the memory onboard, the message *Mem mismatch* displays. This parameter has no effect on a 2MB board.	2MB 4MB
ROM on 173000	Enables or disables the CPU ROM code at address 1730000.	**Yes (factory setting)** enables the internal Boot EPROM on the KDJ11-E. When enabled, the Boot EPROM occupies the address area from 173000 to 173777. This area consists of 512 words which represents one page out of the EPROM. This parameter sets/resets bit 7 of the CSR at address 17777520 just before transferring control to another boot program. The page number can be selected through the bits 15-9 of the PCR register. **No** disables the internal Boot EPROM on the KDJ11-E.
Rom on 165000	Enables or disables the CPU ROM code at address 165000.	**Yes** enables the internal EEPROM or Boot EPROM depending on Bit 6 of the CSR register (17777520). The ROM code uses an address area from 165000 to 165776 for EEPROM or for the Boot EPROM, depending on Bit 6 of the CSR register. **No (factory setting)** disables the internal EEPROM.
Power-up Mode	When the ROM code is started, it checks a status bit to determine if the unit is powering up or if the front panel RESTART switch was activated. The ROM code then uses the appropriate mode selected. There are four power-up modes which you can select.	**Dialog Mode (factory setting)** - Force dialog must be disabled (S5 off). The Setup Menu is entered when Dialog Mode is selected.

Table 3–28 (Cont.) Setup Menu Configuration Parameters

Parameter	Description	Values
		Auto Mode - At the completion of the diagnostics the ROM code enters an automatic boot routine that tries to boot a previously selected device or devices. The list of devices can be from 1 to 6 devices long. Each device is tried sequentially until a successful boot occurs or the end of the boot table is reached. *ROM Mode* is a special Automatic Boot Mode that is entered as a power-up/ restart option to boot specific devices when one or more of switches 2-4 on the console/SLU panel are set. When switches 2-4 of the console/SLU panel are set to one of the six combinations shown in Table 3–11 and force dialog mode is not selected, ROM mode is entered. The mode attempts to boot only the one device selected by this command. If the boot is unsuccessful, the ROM code prints out the normal error message and enters dialog mode. See Table 3–11 for switch settings. **ODT Mode** - At completion of a very limited set of tests, the ROM code executes a halt instruction and passes control to J11 micro ODT. This mode is used in debug environments. The ROM code does not change any locations in memory before entering ODT mode. See Section 3.7. **Trap 24 Mode** - The ROM code loads the PSW with the contents of locate 26 and then transfers control to the address located in location 24. This mode is used when power-fail recovery is desired. The ROM code does not change any locations in memory before executing mode 24.
Restart Mode	See Power-up Mode.	See Power-up Mode.
Power-on Self-tests	Enables or disables power-on self-tests.	**Yes (factory setting)** executes all self-tests during a power-on. The force dialog switch (S5) must be set to off. During a restart the self-tests are not performed. **No** disables all self-tests.
Select Self-tests	Allows you to enter the Self-tests Menu.	**Edit**
User Boot	Allows you to enter the User Boot Menu.	**Edit**
Alternate Boot Block	After the boot block of a device is loaded into memory, the ROM code looks at word locations 0 and 2 to see if the device looks bootable. If the data is not correct, the ROM code types out an error message indicating that the media is not bootable.	**Yes** sets the ROM code to look for location 0 to be any non-zero number. **No (factory setting)** sets the ROM code to look for location 0 to be a value of 240 to 277 and for location 2 to be 400 to 777.

Table 3–28 (Cont.) Setup Menu Configuration Parameters

Parameter	Description	Values
LTC Register	Enables/disables the LTC register.	**Yes (factory setting)** enables the clock CSR at address 17777546. **No** disables the clock CSR at address 17777546.
Force Clock Interrupt	Allows you to unconditionally force LTC interrupts.	**Yes** enables the clock to unconditionally request interrupts when the processor priority is 5 or less. **No (factory setting)** enables the clock to request interrupts only if the clock CSR is enabled, clock CSR bit 6 is 1, and the processor priority is 5 or less.
Clock Frequency	Determines the source of the clock to be used.	**PS** determines the source of the clock to be from backplane pin BR1. The power supply normally drives this signal at 50 or 60 Hz. **50 Hz (factory setting)** determines the source of the clock to be from the KDJ11-E at 50 Hz. **60 Hz** determines the source of the clock to be from the KDJ11-E at 60 Hz. **800 Hz** determines the source of the clock to be from the KDJ11-E at 800 Hz.
Halt on Break	Enables the processor to halt when Break is pressed.	**Yes** halts the processor when Break is pressed. **No (factory setting)** tells the processor to ignore any break request.
Trap on Halt	Enables or disables a trap on halt.	**Yes** - If a halt instruction is executed in kernel mode, the processor traps to location 4 if a halt. **No (factory setting)** - If a halt instruction is executed in kernel mode, the processor enters J-11 micro-ODT.
Ignore Battery	This is used only when the current power-up or restart mode is set to 24.	**Yes** executes mode 24 regardless of the status of the battery. **No (factory setting)** - The battery OK signal must be present to execute mode 24. Battery OK indicates that the memory contents were not corrupted as a result of a power failure. If BOK is set, TRAP24 mode is not executed and Dialog Mode is entered.
Lines on	Changes the addresses of the serial interfaces 1-7 from 176500-176600 to 176600-176660.	**176500 (factory setting)** selects address 176500, vector 300. **176600** selects address 176600, vector 400. **DIS** disables all SLUs. **NOTE** **After selecting and saving the desired starting address, the system must be powered down and then rebooted for the change to occur.**
Map	Maps all locations in the I/O page.	To execute the Map parameter, move the cursor to **Do** and press Return. Upon execution, the Map Menu is displayed (Example 3–26). After the valid I/O page addresses displays, the Setup Menu displays.
Factory Setting	Resets all parameters to their factory settings.	Move the cursor to **Do** and press Return to execute Factory Setting.

Table 3–28 (Cont.) Setup Menu Configuration Parameters

Parameter	Description	Values
Save	Saves all modifications made to the Setup Menu.	Press Tab to move the cursor to **Do**. Press Return to execute Save. You are prompted "Are you sure? Y/N". Press Y to save the modifications. Press N if you do not want to save the modifications.

NOTE
If you want to save all function modifications, you must execute Save *before* leaving the Setup Menu.

3.6.4 Self-test Menu

When you execute Select Self-tests on the Setup Menu, the Self-test Menu is displayed (Example 3–24). This menu is used to determine which tests are executed on power-up and also allows individual tests to be selected and executed. The factory settings are shown in this example.

```
KDJ11-E Monitor  Version 1.06  18-May-1990
(C) Digital Equipment Corporation 1990

67 CPU Test                     Yes   44 Lines Config. Test      Yes
66 MMU Test                     Yes   43 Serial Lines Test       Yes
65 Pre-Console Test             Yes   40 Memory parity Test      Yes
64 MSER Test                    Yes   37 UBA Map Reg Test        Yes
63 CCR r/w Test                 Yes   36 UBA NPR Cycles Test     Yes
62 HIT/MISS-Reg Test            Yes
61 LTC Speed Test               Yes
60 Add-Stat-Reg Test            Yes   32 Loopback SLU Test        No
57 CPU-Err-Reg Test             Yes   31 Extended Memory Test     No
55 UBA Reg. Resp. Test          Yes
54 Address 0 Test               Yes
53 Pre-Memory (0-4KW) Test      Yes
52 FPA Register Test            Yes
51 FPA Function Test            Yes
50 Int Mem Address Test         Yes
47 Int Mem Data Test            Yes
46 PIRQ-Reg Test                Yes
45 LTC Int Test                 Yes    30 All Selected Tests       No

Monitor     Do              Test 00     Repeat 00000              Do
```

Example 3–24 Self-test Menu

NOTE
Test 30, All Selected Tests, runs all tests selected (parameter = Yes) as a group.

Test 32, Loopback SLU Test, requires loopback connectors installed on all SLUs on the console/SLU panel.

3.6.4.1 Selecting or Deselecting Tests Executed Upon Power-Up

To select or deselect tests that are executed upon power-up:

1. Move the cursor to the test to be changed.
2. Press Return to select Yes or No.
3. Press Tab to select the Monitor field.

4. Press Return to return to the Setup Menu.
5. Press Tab to select the Save field.
6. Press Return to save the Self-test parameters.

3.6.4.2 Selecting and Executing an Individual Test

To select and execute an individual test:

1. Move the cursor to the Test field.
2. Type in the test number of the test to be run.
3. Move the cursor to the Repeat field.
4. Type in the number of iterations to run the test or 0 to run continuously.
5. Move the cursor to Do.
6. Press Return to execute testing.

NOTE
Ctrl C terminates testing.

3.6.4.3 Selecting and Executing a Group of Tests (Test 30)

To select and execute a group of tests using Test 30:

1. Move the cursor to each test to be changed.
2. Press Return to select Yes or No.
3. Move the cursor to the Test field.
4. Enter *30* to select Test 30, All Selected Tests.
5. Move the cursor to the Repeat field.
6. Type in the number of iterations to run the tests or 0 to run continuously.
7. Move the cursor to Do.
8. Press Return to execute testing.

NOTE
Ctrl C terminates testing.

3.6.5 User Boot Menu

A sample User Boot Menu is shown in Example 3–25. The addressing scheme shown is for clarity only. Normally the boot routine resides here.

```
KDJ11-E Monitor  Version 1.06 08-May-1990
(C) Digital Equipment Corporation 1990

                                                    ❸Exit                Do
❶Device name          DK  ❷Beginning addr    1000  ❹Save boot           Do
❺Dev Description  RK05    ❻Last byte addr    1016  ❼Load saved boot    Do
❽Highest Unit          7  ❾Start addr        1000  ❿Del saved boot     Do

Addrs.  000000 000002 000004 000006 000010 000012 000014 000016⓫
001000  012737 000005 177404 105737 177404 100375 000774 000000
001020  000000 000000 000000 000000 000000 000000 000000 000000
001040  000000 000000 000000 000000 000000 000000 000000 000000
001060  000000 000000 000000 000000 000000 000000 000000 000000
001100  000000 000000 000000 000000 000000 000000 000000 000000
001120  000000 000000 000000 000000 000000 000000 000000 000000
001140  000000 000000 000000 000000 000000 000000 000000 000000
001160  000000 000000 000000 000000 000000 000000 000000 000000
001200  000000 000000 000000 000000 000000 000000 000000 000000
001220  000000 000000 000000 000000 000000 000000 000000 000000
001240  000000 000000 000000 000000 000000 000000 000000 000000
001260  000000 000000 000000 000000 000000 000000 000000 000000
001300  000000 000000 000000 000000 000000 000000 000000 000000
001320  000000 000000 000000 000000 000000 000000 000000 000000
001340  000000 000000 000000 000000 000000 000000 000000 000000
001360  000000 000000 000000 000000 000000 000000 000000 000000
```

Example 3–25 User Boot Menu

❶ *Device name* is a two-letter mnemonic name for the boot program.

❷ *Beginning addr* refers to the the first address of the boot routine. The address range is 1000-17544. The ROM code prints out the old beginning address and prompts you for the new beginning address. Type in a new address or press Return to accept the old beginning address.

❸ *Exit* returns you to the Setup Menu.

❹ *Save boot* saves the boot program in the EEPROM. This function can take up to two minutes at the full length of 8 Kbytes.

❺ *Dev Description* is an optional but recommended description of the device name. The name is usually the name that is physically marked on the outside of the device (i.e., RA82).

❻ *Last byte addr* is the address of the last byte of code used in memory.

❼ *Load saved boot* reloads previously saved boot program. This allows additional changes to be made to the boot routine.

❽ *Highest Unit* defines the allowable range of valid unit numbers for this device. If the value is set to 3, the allowable range is 0 to 3. If a unit number is typed in at boot time and it is not in range, an invalid unit number error occurs.

❾ *Start addr* is the address that the ROM code passes control to.

❿ *Del saved boot* deletes the boot program from the EEPROM.

NOTE

The beginning address and last byte address refer to physical addresses in memory for the program. Permitted values are between 1000 and 17544.

Return closes a location. To select a different address, use the cursor control arrows.

3.6.6 Map Menu

The Map Menu displays all addresses in the I/O page that respond. The I/O page is from addresses 17760000-17777776. In addition, all addresses on the CPU or the UBA that respond, are described. There is no description for optional device addresses that respond.

The Setup Menu is displayed at the completion of the Map function. The ROM code waits for you to press Return rather than scrolling data forward on video screen terminals. The ROM code always assumes the terminal can display at least 24 lines of 80-column data.

A sample Map Menu is shown in Example 3–26.

```
KDJ11-E Monitor  Version 1.06 18-May-1990
(C) Digital Equipment Corporation 1990

I/O page Map
Starting    Ending
Address     address

17765000   17765776   CPU ROM or EEPROM
17772100              Memory CSR
17772200   17772276   Supervisor I and D PDR/PAR's
17772300   17772376   Kernel I and D PDR/PAR's
17772516              MMR3
17773000   17773776   CPU ROM
17776500   17776566   SLU's
17777200   17777376   UBA map REG's
17777520   17777526   CSR, PCR, BCR/BDR ASR
17777546              Clock CSR
17777560   17777566   Console SLU
17777572   17777576   MMR0,1,2
17777600   17777676   User I and D PDR/PAR's

Press RETURN key when ready to continue

KDJ11-E Monitor  Version 1.06 18-May-1990
(C) Digital Equipment Corporation 1990

I/O page Map
Starting    Ending
Address     address

17777730   17777736   DCSR, DDR, KMCR
17777744   17777752   MSER, CCR, MREG, Hit/Miss
17777766              CPU Error
17777772              PIRQ
17777776              PSW

Press RETURN key when ready to continue
```

Example 3–26 Map Menu

3.7 DCJ-11 Micro ODT

The console octal debugging technique (ODT) allows the KDJ11-E to respond to commands and information entered on the console terminal. The console interface uses addresses 17 777 560 through 17 777 566 to communicate with the DCJ11 microprocessor.

3.7.0.1 ODT Notes

1. When entering addresses or data, you do not need leading zeros. ODT fills them in.
2. When entering addresses in the I/O page, you must enter all 22 bits (for example, 17 776 100).
3. A ? (question mark) is printed whenever you enter illegal characters, addresses are accessed that result in a timeout, or a parity error is detected.

Table 3–29 summarizes the ODT commands. Examples 3–27 through 3–30 show some of the commands.

Table 3–29 DCJ-11 Micro ODT Command Summary

Command	Symbol	Description
Slash	n/	Opens and outputs the contents of a memory location, I/O device register, internal processor register, or processor status (PS) register. The slash (/) must be preceded by octal digits (n) to specify the register or location (Example 3–27).
Return	Return	Closes an open location. If a location's contents are to be changed, precede the Return with the new data. If no change is desired, Return closes the location without altering its contents (Example 3–27).
Line feed	Line Feed	Closes an open location and opens the next contiguous location. Memory addresses are incremented by two, and processor registers are incremented by one. If the PS is opened, it is closed and no new location is opened (Example 3–28).
Internal register	$n or Rn	Either character—when followed by a register number 0 to 7 or by the PS designator (S)— opens the specified processor register. If you type more than one number after R or $, the last number typed is used.
Processor status word designator	S	Opens the processor status register. The designator must follow $ or R.
Go	G	Starts program execution at the location typed immediately before the G. If G is issued with the **Restart/Run/Halt** switch set to Halt, the system is initialized, ODT reentered, and the PC displayed. G truncates the address typed in the last 16 bits. For example, 7 777 773 000G would be read as 173 000G. Since memory management is disabled by G, the starting address is always in the lower 28 K of memory or the I/O page (Example 3–29).
Proceed	P	Resumes program execution. The command corresponds to CONTINUE on other PDP-11 consoles. Program execution resumes at the address pointed to by the PC. If P is issued with the **Restart/Run/Halt** switch set to Halt, it is recognized at the end of instruction execution, ODT is reentered, and the PC displayed. You can thus single-instruction step through a program and obtain a PC trace on the console terminal (Example 3–30).
Binary dump	Ctrl Shift S	Manufacturing use only. It is not recommended that this command be used.

An example of the Slash Command is provided in Example 3–27.

```
@1000/ 012737    [Return]
                                ;Open memory location 00001000.
                                ;The contents (01273) are
                                ;displayed. [Return] closes the
                                ;location without modification.
@100/ 000200 7422 [Return]
                                ;Open memory location 00000100.
                                ;and deposit data (7422) and
                                ;close the location.
@/ 007422 6422 [Return]
                                ;Reopen the location and deposit
                                ;new data.
```

Example 3–27 Slash (/) Command

An example of the Line Feed Command is provided in Example 3–28.

```
@1000/ 012737 [Line Feed]
                                ;Location 1000 is opened, the
                                ;contents are displayed, and
                                ;then closed with [Line Feed].
00001002 100200 0 [Line Feed]
                                ;The [Line Feed] caused the next
                                ;location to be opened and the
                                ;contents to be displayed. In
                                ;this case the contents are
                                ;changed by the operator.
00001004 176100 [Return]
                                ;The next location is opened
                                ;to examine the contents and
                                ;then closed with [Return].
```

Example 3–28 Line Feed Command

An example of the Go Command is provided in Example 3–29.

```
@1000G          ;The program is started at location 1000.
@1000G          ;The program is started with the Halt switch
                        ;on. The CPU initializes registers and then
                        ;halts without executing the first instruction.
@1000           ;The PC is displayed and then the ODT prompt
                        ;is displayed.
```

Example 3–29 Go Command

An example of the Proceed Command is provided in Example 3–30.

```
@R7/ 002464 1000 Return
                                ;R7 (PC) is opened and the
                                ;contents displayed. The new
                                ;address is entered in R7.
@P                              ;The proceed command is issued
                                ;and the program continues at
                                ;location 1000.
@P                              ;The proceed command is issued
                                ;with the front panel switch in the
001004                          ;Halt position. The PC is
                                ;displayed.
@P                              ;
                                ;Etc.
001010                          ;
@                               ;
```

Example 3–30 Proceed Command

4
Configuration

4.1 General

This chapter provides the information necessary to configure the PDP-11/94-E, PDP-11X94-E, and PDP-11W94-E systems. It describes the backplane configuration and lists the switch settings, jumper settings, and the power consumption of the modules.

4.2 Backplane Configuration

Figure 4–1 shows the location of the modules in the backplane.

- Slots 1 through 4 are dedicated to the system kernel.
- Slots 5 through 8 support the quad or hex small peripheral controller (SPC) option modules.
- Slot 9 supports only the quad SPC option modules.

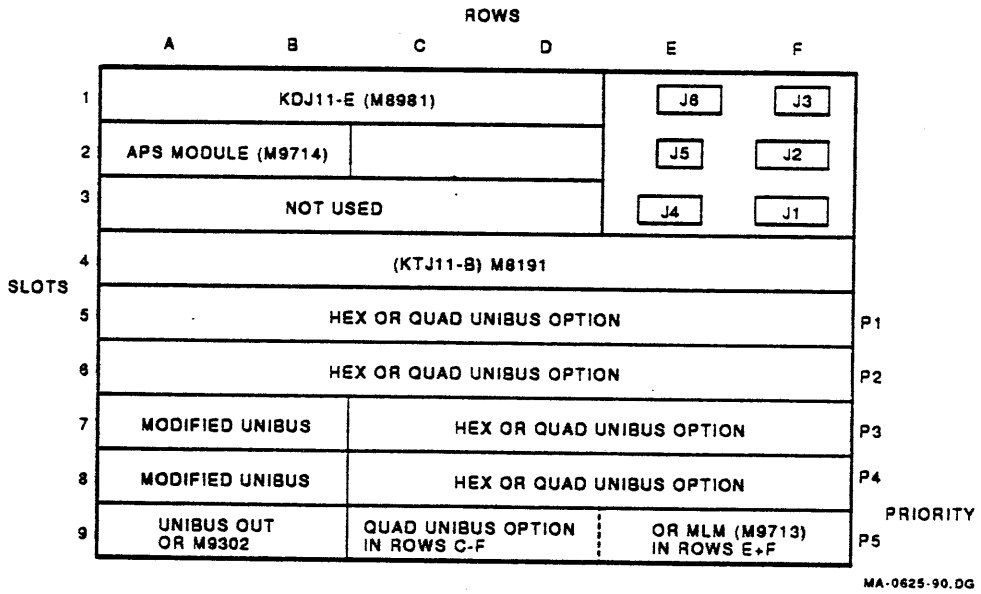


Figure 4–1 Backplane Configuration

There are five nonprocessor grant (NPG) jumpers on the backplane used to select NPG status for slots 5 through 9. Each jumper is connected to one SPC slot. The NPG jumpers

are located on side 2 (the bottom) of the backplane. Figure 4–2 shows the location of the NPG jumpers and the corresponding slot numbers.

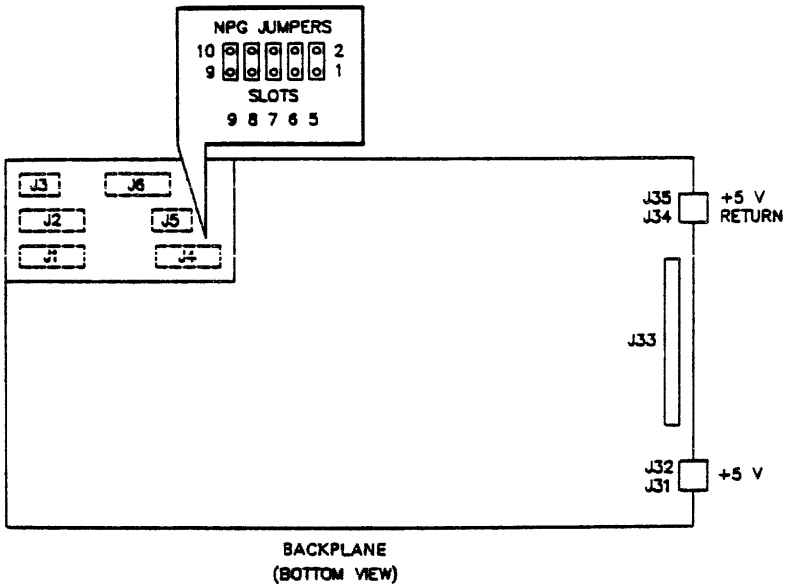


Figure 4–2 NPG Jumper Locations (Side 2 of Backplane)

These jumpers are installed for non-direct memory access (DMA) devices. When installed, the jumpers connect pins CA1 to CB1 of the respective slot. The system is shipped with all the NPG jumpers installed. When a DMA device is added to the backplane, the NPG jumper for that device must be removed.

4.2.1 Backplane Configuration Rules

Follow these configuration rules when installing modules:

- The KDJ11-E CPU (M8981) module is installed in slot 1.
- The KTJ11-B (M8191) UNIBUS adapter module is installed in slot 4.
- The APS (M9714) module is installed in slot 2, rows A and B.
- Slot 3 is unused.
- A G7273 bus grant continuity card must be installed in rows C and D of all unoccupied SPC slots. If an SPC slot is left open, bus grant continuity is lost and the system will not operate.
- An M9713 minimum load module must be installed in an unused SPC slot in rows E and F if either of the following conditions have not been met:
  - — If the combined -15V load of the options in the CPU box is not equal to 700mA or greater on the -15V regulator.

— If the combined +5V load of the options (excluding the KTJ11) in the CPU box is not equal to 3A or greater on the +5V regulator.

NOTE
Ensure that W1, W2, and W3 are installed on the MLM. See Section 4.5.

- Modified UNIBUS devices (MUD) can only be installed in slots 7 and 8.
- A UNIBUS terminator module or UNIBUS out cable is installed in slot 9, rows A and B.

4.3 KDJ11-E CPU Module Configuration

The KDJ11-E CPU module has two jumpers (W1 and W2) and one DIP switch pack for hardware configuration (Figure 4–3). The dip switches on the KDJ11-E CPU module should be set to the off position and the two jumpers *must* be removed.

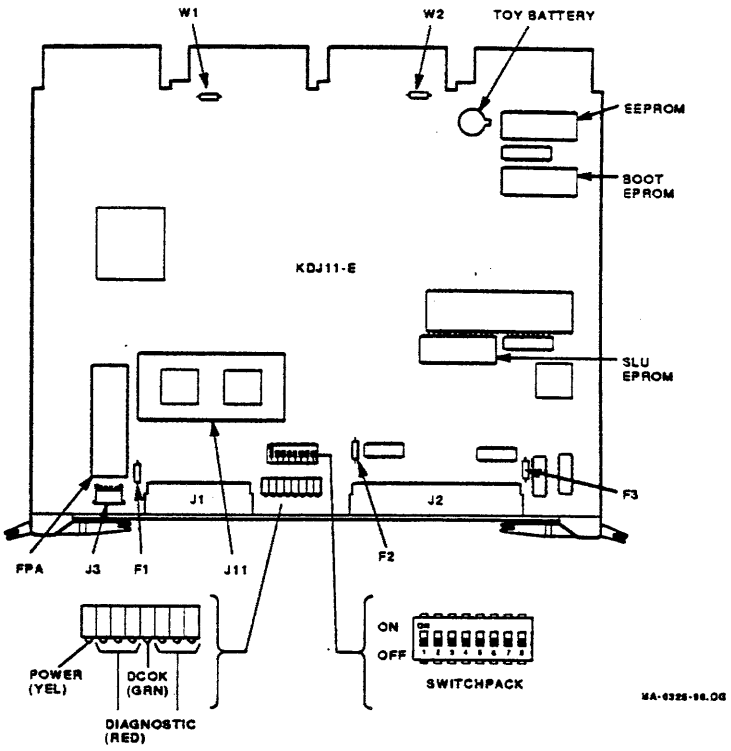


Figure 4–3 KDJ11-E Jumper and DIP Switch Locations

CAUTION
To prevent damage to the power supply, jumpers W1 and W2 must be removed from the KDJ11-E CPU module before powering up the system.

The two jumpers, W1 and W2, connect +5V from backplane pins AA2, BA2, CA2 and DA2 to the logic on the KDJ11-E CPU module. In a PDP11/94 system, the KDJ11-E CPU module uses +5.1VBB as its only source for +5V power. The APS module supplies voltage to the KDJ11-E through connector J3 on the KDJ11-E. Jumpers W1 and W2 *must* be removed, otherwise +5V and +5.1VBB will be shorted together which can result in damage to the power supply.

4.3.1 KDJ11-E Power Consumption

The following table lists the KDJ11-E power consumption requirements:

Voltage	Typical	Maximum
5.0V	0.0A	0.0A
5.1VBB	4.0A	4.5A
15V	.4A	.6A

4.4 KTJ11-B UNIBUS Adapter Module Configuration

The UNIBUS adapter (UBA) module does not have any hardware jumpers or switches for configuration. The UBA module has four sockets for the installation of M9312-compatible user ROMs. Figure 4–4 shows the ROM socket locations.

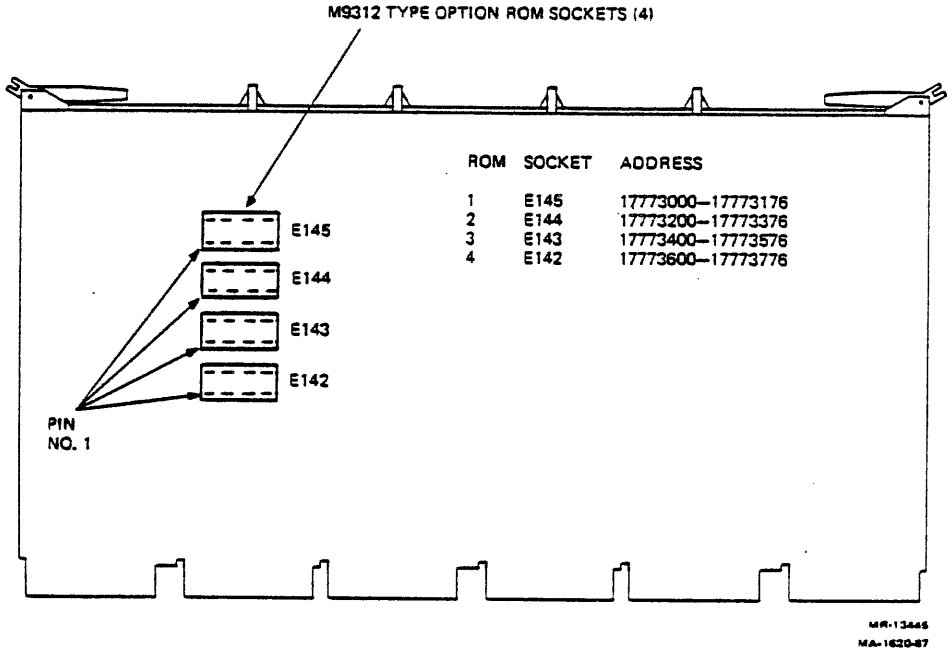


Figure 4–4 KTJ11-B ROM Socket Locations

The M9312-compatible user ROMs are installed with pin 1 of the chip toward the left edge of the component side of the module. Table 4–1 describes the M9312-type boot ROMs that are available.

Table 4–1 Available M9312-Type ROMs

Mnemonic	Part Number	Supported Devices
MU	23-E39A9-00	TU81, TK50 tape drives
CT	23-761A9-00	TU60 cassette tape drive
DB	23-755A9-00	RP04, RP05, RP06, RM02, RM03 disk drives
DD	23-765A9-00	TU58 cartridge tape drive
DK	23-756A9-00	RK03, RK05 disk drives
DL	23-751A9-00	RL01, RL02 disk drives
DP	23-755A9-00	RP02, RP03 disk drives
DS	23-759A9-00	RS03, RS04 disk drives
DT	23-756A9-00	TU55, TU56 tape drives
DU	23-767A9-00	(General boot for all Disk MSCP devices) RA80, RA81, RA60, RC25, RX50 disk drives
DX	23-753A9-00	RX01 floppy disk drive
DY	23-811A9-00	RX02 floppy disk drive
MM	23-757A9-00	TU16, TE16, TU45, TM02, TM03, TU77 tape drives
MS	23-764A9-00	TS04, TS11, TU80, TS05 tape drives
MT	23-758A9-00	TU10, TE10, TS03 tape drives
PR	23-760A9-00	PC05 high-speed paper reader
TT	23-760A9-00	Low-speed paper reader (Teletype)
XL	23-926A9-00 23-927A9-00 23-928A9-00	DL11-E (DECnet DDCMP)*
XM	23-862A9-00 23-863A9-00 23-864A9-00	DMC11, DMR11 (DECnet DDCMP)*
XU	23-868A9-00 23-869A9-00 23-870A9-00	DU11 (DECnet DDCMP)*
XW	23-865A9-00 23-866A9-00 23-867A9-00	DUP11 (DECnet DDCMP)*

*Three ROMs are required to implement this bootstrap

4.4.1 KTJ11-B UNIBUS Adapter Power Consumption

The following table lists the KTJ11-B UNIBUS adapter power consumption requirements:

Voltage	Typical	Maximum
5.0V	7.4A	8.5A

4.5 Minimum Load Module

The minimum load module (M9713) has three jumpers (W1, W2 & W3) that are used to enable or disable the loads that the MLM provides on +5V and -15V. The MLM module provides 2.75A of load on +5V and 750mA of load on -15V if the three jumpers are installed. Follow the guidelines in Table 4–2 to configure the jumpers.

Table 4–2 Minimum Load Module Jumper Configuration Guidelines

Jumper	Description
W1 (+5V load)	Calculate the +5V current usage for all of the modules installed in the CPU box (remember that the UBA draws 7.4A on +5V). If it is less than 10A, W1 must be installed. If it is greater than 10A, remove W1.
W2 & W3 (-15V load)	Calculate the -15V current usage for all of the options installed in the CPU box. If it is less than 700mA, then jumpers W1 and W2 must be installed. If it is greater than 700mA, remove jumpers W2 and W3.

NOTE

If the power supply minimum loads of 10A on +5V AND 700mA on -15V are met by the options installed in the CPU box (i.e., W1, W2 and W3 removed), then the MLM is not necessary and can be removed.

The M9713 MLM has three LED indicators (Figure 4–5):

- D1 (green) - Indicates that W1 is installed on MLM.
- D2 (green) - Indicates that W2 is installed on MLM.
- D3 (green) - Indicates that W3 is installed on MLM.

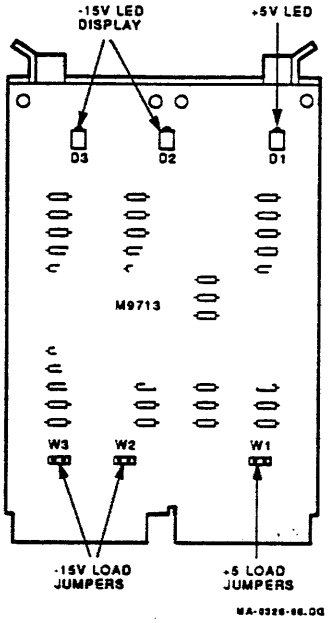


Figure 4–5 Minimum Load Module Layout

Table 4–3 describes the functions of the jumpers.

Table 4–3 MLM Jumper Functions

Jumper	Function
W1 installed	+5V load provided by MLM is 2.75A.
W1 removed	No +5V load is provided by MLM.
W2 and W3 installed	-15V load provided by MLM is 750mA.
W2 or W3 removed	-15V load provided by MLM is 375mA.
W2 and W3 removed	No -15V load is provided by MLM.

4.6 Power Supply

The H7204-CA and H7204-CB power supplies (Figure 4–6) provide dc system power .

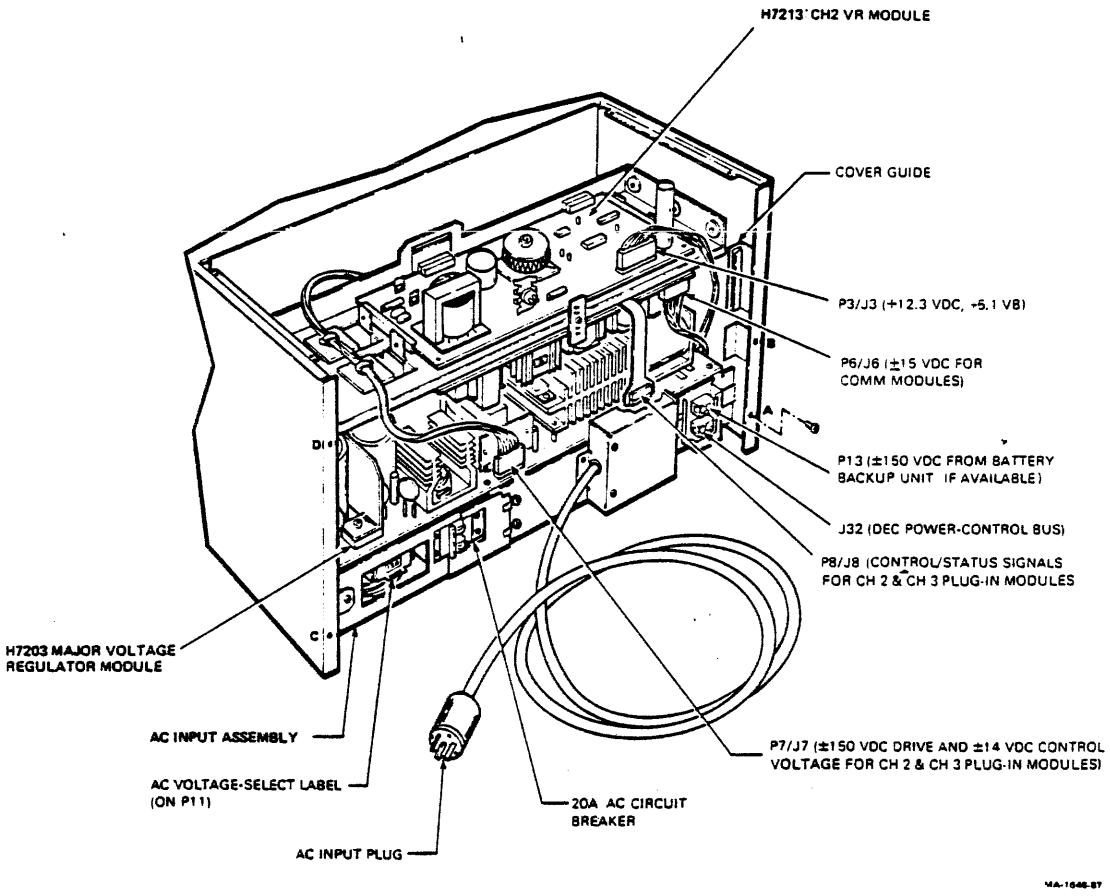


Figure 4–6 H7204-C Power Supply (Rear View)

The H7204-CA (120 Vac) power supply provides 100A at +5 Vdc, 5A at +15 Vdc, and 6A at −15 Vdc. It also provides 3A at +12 Vdc for fan operation and up to 15A at +5.1 Vdc (5.1 VB memory voltage), which is backed up by an optional battery backup unit. This power supply features overvoltage and overheating protection. To ensure proper regulation, the power supply must have a minimum load of 700 mA on the −15V and 10A on the +5V regulators.

The H7204-CB is a 240 Vac version of the H7204-CA.

5
Functional Description

5.1 Introduction

The PDP-11/94 functional block diagram is shown in Figure 5–1. The system contains the KDJ11-E CPU and KTJ11-B UNIBUS adapter (UBA).

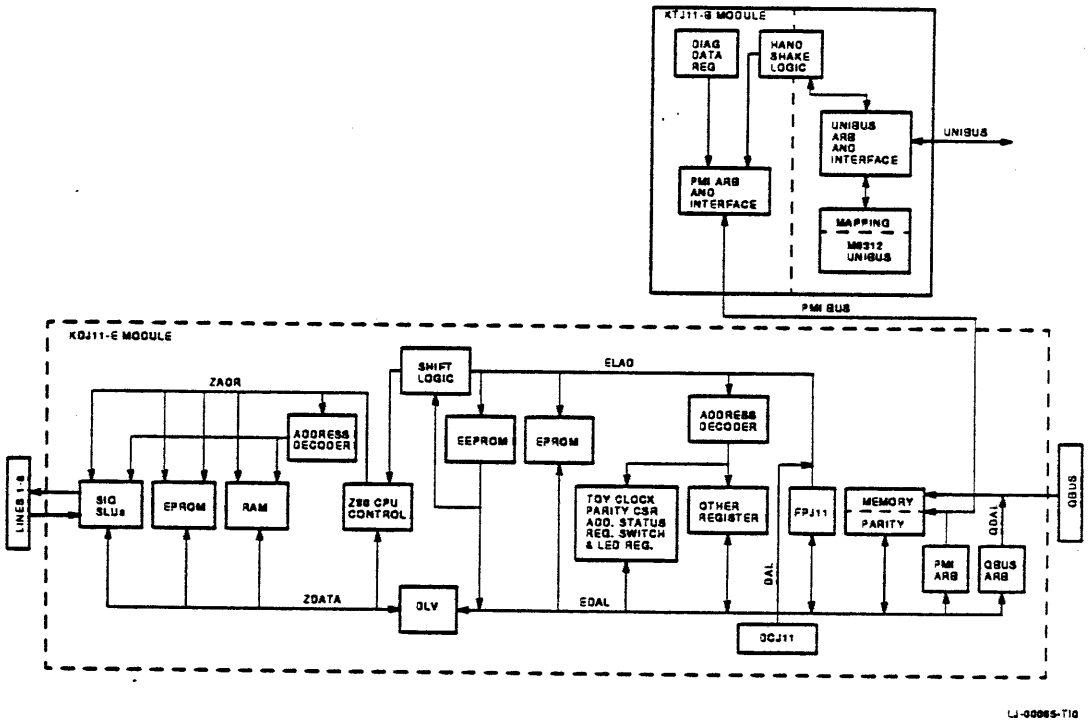


Figure 5–1 PDP-11/94 Functional Block Diagram

The KDJ11-E module contains the following:

- DCJ-11 microprocessor
- Floating-point accelerator (FPJ11)
- 22-bit memory management
- Programmable line frequency clock
- Console serial line unit

- Seven SLUs
- Boot and diagnostic ROMs
- TOY clock
- Two or four Mbyte onboard parity memory
- Console programmable setup features
- Comprehensive self-test capability
- LED status indicator

The KTJ11-B UNIBUS adapter (M8191) contains:

- UNIBUS mapping
- Four M9312-compatible boot sockets

The KTJ11-B UNIBUS adapter module is divided into a PMI section and a UNIBUS section. The handshake logic enables data transfers to occur between PMI and UNIBUS devices. The PMI section has diagnostic registers and PMI arbitration/interface logic. The UNIBUS section has UNIBUS mapping logic, sockets for M9312-type user ROMs, and UNIBUS arbitration and interface logic.

The modules transfer data using the PMI. Data transfers between the PMI and UNIBUS devices use the handshaking logic on the KTJ11-B module. PMI read operations (DATI, DATIP, and DATBI) can be word or block mode. PMI write operations (DATO, DATOB) can be word or byte mode.

NOTE
The PDP-11/94 UNIBUS power-up protocol is slightly different from most PDP-11 systems. See Appendix D for a protocol description.

All communications between UNIBUS devices and the UBA occur through standard UNIBUS protocol. No Q-bus devices may be configured on the system.

5.2 PMI Bus Description

The PMI bus provides a high-performance communication path between the KDJ11-E CPU and the KTJ11-B UBA. The PMI consists of 14 signals that are unique to PMI protocol. The signal lines are described in Table 5–1.

The KDJ11-E CPU module is also used in systems that contain Q-bus devices; therefore, some of the signals retain their Q-bus names. The functionality of these signals changes, however, when a KTJ11-B UBA is part of the system. Data and address information is multiplexed and uses the same data/address lines as Q-bus protocol.

Table 5–1 PMI Signal Line Descriptions

Signal Line	Description
BDAL <21:00>	Contains 22 multiplexed bidirectional data/address lines. During the address phase of a data transfer cycle, the PMI master gates address information onto these lines. During the data phase of the cycle, the slave (DATI) or the master (DATO) gates data onto BDAL <15:00> and parity error/control information onto BDAL <17:16>.
BBS7	Bank 7 Select (I/O Page Select). When the PMI master gates an address onto BDAL <21:00>, it asserts BBS7 to reference the I/O page (including the I/O page addresses reserved as nonexistent memory). When BBS7 is asserted, BDAL <12:00> specifies the I/O page address; Negation of BBS7 selects the memory address space.
BRPLY	Reply. This signal is asserted by the UBA as a slave response during the PMI DATO(B) cycle and during the interrupt vector DATI cycle.
BDIN	Data Input. This signal is used by PMI protocol during UNIBUS interrupt grant cycles. The CPU asserts BDIN after gating the interrupt priority onto BDAL <03:00>. The UBA latches the interrupt priority on the leading edge of BDIN.
BIACKI	Interrupt Acknowledge. This signal is used by PMI protocol during UNIBUS interrupt grant cycles. When the UBA receives the assertion of BIACKI (from the CPU), it asserts one of the UNIBUS grant (BGn) signals.
BPOK	Power OK. This signal is asserted and negated by the UBA in response to AC LO on the UNIBUS following standard UNIBUS power-up/power-down protocol. UNIBUS devices may, during power-up, prolong the assertion of AC LO/BPOK.
The following signals are asserted (low) and negated (high) by the PMI master:	
PBCYC	PMI Bus Cycle. The PMI master asserts this signal at the start of a PMI cycle and negates this signal at the end of that cycle.
PBYT BWTBT	PMI Byte and Write Indication. When the PMI master gates an address onto BDAL <21:00>, it asserts or negates these signals to indicate what type of data transfer will occur during the next bus cycle: **BWTBT PBYT Bus Cycle Type** H H DATI or DATBI H L DATIP L H DATO L L DATOB
PBLKM	PMI Block Mode.

Table 5–1 (Cont.) PMI Signal Line Descriptions

Signal Line	Description
	When a PMI master wants to read more than two words of data, it uses both PBCYC and PBLKM to control the timing of the block mode data in (DATBI) cycle. It asserts both PBCYC and PBLKM at the start of the DATBI cycle. It negates PBLKM after reading two data words and then reasserts PBLKM (unless the next two words will end the cycle). After reading the last two words, the PMI master negates PBCYC (PBLKM is already negated).
PWTSTB	PMI Write Strobe. The PMI master asserts this signal after gating data onto BDAL <15:00>. The PMI slave latches the data into its write buffer on the leading edge of the PWTSTB pulse.
QSACK	The UBA asserts this signal on the PMI in response to QSACK from the UNIBUS.
DMR	The UBA asserts this signal on the PMI in response to NPR from the UNIBUS or when the UBA is performing a DMA cycle in its own behalf.
DMG	The CPU asserts this signal when PMI master status has been granted to the UBA in response to a DMG.
QBR7-4	The UBA asserts one of these signals in response to one of the BR7-4 lines being asserted on the UNIBUS during interrupt request cycles.
The following signals are asserted and negated by the PMI slave:	
PSSEL	PMI Slave Selected. The PMI slave (CPU or memory only) asserts this signal whenever it decodes a valid address on BDAL <21:00>.

NOTE
When PUBMEM is asserted, the PMI slave does not respond to PMI control signals. PUBMEM is asserted by the UBA to indicate that UNIBUS memory space is being addressed. The UBA does not assert PSSEL. The CPU ignores the assertion of PSSEL if PUBMEM is asserted.

NOTE
Memory address space on the UNIBUS is not supported on the KDJ11-E.

PHBPAR	PMI High Byte Data Parity. This signal is generated by PMI memory during DATI and DATBI cycles and provides odd parity for the high byte data (on BDAL <15:08>).
PLBPAR	PMI Low Byte Data Parity. This signal is generated by PMI memory during DATI and DATBI cycles and provides even parity for the low byte data (on BDAL <07:00>).
PRDSTB	PMI Read Strobe. The PMI slave asserts and negates this line to control data transfers during DATI and DATBI cycles. The PMI master latches the first word of the received data on the negating edge of this signal. The PMI master latches the second data word a specified time after this signal is negated.
PSBFUL	PMI Slave Buffer Full.

Table 5–1 (Cont.) PMI Signal Line Descriptions

Signal Line	Description
	A PMI slave asserts PSBFUL during a write cycle, indicating that its write buffer is full and that it cannot respond to another cycle request. The new PMI master may gate an address onto BDAL <21:00> while PSBFUL is asserted, but it must not assert PBCYC until PSBFUL is negated.

The following signals are used for communication between the CPU and the UNIBUS adapter. PMI memory modules do not use these signals.

PMAPE	PMI UNIBUS Map Enable. The CPU module asserts this signal if memory management register 3 (MMR3) bit <5> is set and negates this signal if MMR <05> is clear. The UBA module enables the UNIBUS map if PMAPE is asserted and disables the UNIBUS map if PMAPE is negated.
PUBSYS	PMI UNIBUS System. This signal is a static signal that indicates whether the system is a UNIBUS system or a Q-bus system and is asserted by the UBA. The CPU follows PMI protocol for data transfers whether PSSEL is asserted or not.
PUBMEM	PMI UNIBUS Memory. This signal line is asserted by the UBA to indicate that the UNIBUS memory space is being addressed. The UBA asserts PUBMEM during the assertion of PBCYC.

NOTE
When PUBMEM is asserted, the PMI slave does not respond to PMI control signals. PSSEL is asserted by PMI memory when addressed. The CPU ignores the assertion of PSSEL if PUBMEM is asserted. The UBA does not assert PSSEL.

NOTE
Memory address space on the UNIBUS is not supported on the KDJ11-E.

PUBTMO	PMI UNIBUS Timeout. This signal is asserted by the UBA in response to any of the following conditions: • A nonexistent memory timeout occurs when the UBA sends an address out on the UNIBUS. • A SACK timeout occurs during an interrupt cycle. • An interrupting UNIBUS device has been granted UNIBUS master status but does not execute an interrupt transaction.
PBSY	PMI Busy. This signal is asserted by the PMI master (CPU or UBA) when it gains PMI master status and is negated by the PMI master when it relinquishes PMI master status. The CPU is the PMI master on power-up.

5.2.1 PMI Bus Acquisition

In the PDP-11/94 system, the CPU is the default PMI bus master; the UBA is the default UNIBUS master. These conditions are always present at the PDP-11/94 system power-up. When the UBA is not requesting the PMI bus, the CPU arbitrates to become PMI master and holds PBSY asserted.

Unlike previous PDP-11 systems, when no device on the UNIBUS is requesting use of the bus, the UBA arbitrates to become UNIBUS master and holds PBSY asserted.

The CPU relinquishes PMI master status when responding to a DMA request or an interrupt cycle from the UBA. Once the CPU has relinquished control of the PMI, it can regain PMI master status only when the following conditions are met.

- QSACK has been negated for 75 ns minimum.
- PBSY has been negated for 0 ns minimum.

When the CPU, as PMI master, references an I/O page address on the UNIBUS, the UBA responds as the slave on the PMI. The UBA continues to control the UNIBUS side of the data transfer as bus master.

The UBA becomes PMI master when the CPU issues a DMA grant (DMG) or performs an interrupt cycle. The UBA may accept the DMG or interrupt grant, thus becoming both PMI and UNIBUS master at the same time. Alternatively, the UBA may pass the DMG or interrupt grant on to a requesting UNIBUS device, which would then become UNIBUS master.

Master status of the UNIBUS and/or PMI bus is requested as follows:

- A UNIBUS device can become UNIBUS master through an NPR request and control data transfers over the UNIBUS. During these data transfers, the UBA is PMI master and responds as UNIBUS slave if the UNIBUS device accesses a PMI memory location, a PMI I/O page location, or a UBA I/O page location.
- A UNIBUS device can become UNIBUS master through a BR7-4 request. As UNIBUS master, the device can control data and/or interrupt vector transfers. In both cases the UBA will respond as UNIBUS slave. The device may perform an interrupt vector cycle or access a PMI memory location, a PMI I/O page location, or a UBA I/O page location.
- The UBA can become both PMI and UNIBUS master at the same time through DMG and interrupt requests. As PMI and UNIBUS master, the UBA has direct access to the PMI.

5.2.2 DMA Requests

Through an NPR request to the UBA, a UNIBUS DMA device can perform UNIBUS DATI, DATIP, DATO, and DATOB cycles. The UBA controls the PMI portion of the data transfer.

When placed in diagnostic test mode, the UBA can perform DMA transfers without a requesting UNIBUS device. In this case, the UBA itself is the requesting device. When the UBA performs a DMA cycle, it becomes master of the PMI and the UNIBUS simultaneously, and has complete control of the PMI.

The following PMI protocol flow is observed by the CPU and UBA when arbitrating a nonprocessor request from a UNIBUS device.

PMI Bus	UNIBUS
	1. The UNIBUS device asserts NPR.
	2. If the UBA is UNIBUS master, it negates BBSY after removing address, data, and control information from the bus.
3. The UBA asserts DMA request (DMR) on the PMI bus.	
4. The CPU bus arbitration logic asserts DMG on the PMI after receiving DMR and 75 ns minimum after the negation of QSACK from a previous PMI bus transaction.	
5. The UBA receives the assertion of DMG.	
	6. The UBA asserts nonprocessor grant (NPG).
	7. The requesting device with the highest priority asserts SACK and negates nonprocessor request (NPR).
8. The UBA asserts QSACK on the PMI.	
NOTE **The UBA asserts PUBTMO instead of QSACK (indicating no SACK timeout) if SACK is not received within 10 μs after it asserts BGn on the UNIBUS. The CPU then cancels the DMA cycle and resumes arbitration.**	
9. The CPU arbitration logic receives QSACK and negates DMG.	

PMI Bus	UNIBUS
NOTE **Because the UBA provides the No SACK Timeout function on the PMI, the CPU always asserts DMG until it receives QSACK or UBTMO.**	
	10. The UBA negates NPG on the UNIBUS.
11. The UBA asserts PBSY after receiving the negation of PBSY from the previous PMI cycle, and becomes PMI master.	
	12. After receiving the negation of BBSY from the previous bus master, the UNIBUS device asserts BBSY and negates SACK.
When a UNIBUS DMA device becomes UNIBUS master through an NPR request, it can perform UNIBUS DATI, DATIP, DATO, and DATOB cycles. If the device accesses a PMI memory location, a PMI I/O Page location, or a UNIBUS I/O page location, on the UBA, the UBA responds as the UNIBUS slave. For PMI memory and PMI I/O page accesses, the UBA—as the PMI master—controls the PMI portion of the data transfer. Data transfer cycles are described in Section 5.2.5.	
13. The UBA negates QSACK.	
14. The CPU resumes arbitration 75 ns minimum after receiving the negation of QSACK.	
	15. The UNIBUS device removes address, data, and control information from the bus and negates BBUSY.
16. After the PMI slave or the UBA has removed all data and control information from the bus, the UBA negates PBSY.	

5.2.3 UNIBUS Device Interrupt Requests

The CPU and UBA observe the following protocol flow when arbitrating interrupt requests.

PMI Bus	UNIBUS
	1. The UNIBUS device asserts the appropriate interrupt request line BR7-4.
2. The CPU receives the appropriate request level on QBR7-4.	
3. The CPU arbitration logic asserts one of the four lines, DAL <03:00>, to indicate the level of the granted interrupt.	
4. The CPU asserts BDIN 150 ns minimum after gating DAL <03:00> onto the bus.	
5. The CPU asserts BIAK 225 ns minimum after it asserts BDIN.	
6. The UBA latches DAL <03:00> on the asserting edge of BDIN.	
7. The CPU receives the assertion of IACK on the PMI.	
NOTE **The UBA compares the interrupt level being granted with its own interrupt level and can block the grant. In this case, the UBA performs an interrupt or data transfer cycle and has complete control of the PMI and the UNIBUS simultaneously. In this case, the BGn line would not be asserted on the UNIBUS.**	
	8. The UBA asserts the selected UNIBUS grant (BGn) line. DAL <03>= BG7, DAL <02> = BG6, etc.
	9. If the UBA was the UNIBUS master, it removes address, data, and control information from the bus and negates BBSY.
	10. The highest priority-requesting device receives the assertion of BGn and asserts SACK.
	11. The device negates its BRn.

PMI Bus	UNIBUS

12. The UBA asserts QSACK.

NOTE
The UBA asserts PUBTMO (indicating No SACK Timeout) if SACK is not received on the UNIBUS within 10 μs after it asserts BGn. When the CPU receives the assertion of PUBTMO, it cancels the interrupt cycle and resumes arbitration.

13. The UBA negates BGn.

14. After receiving the negation of BBSY from the previous bus master, the UNIBUS device asserts BBSY and negates SACK.

15. After the UBA receives the negation of PBSY from the previous PMI cycle, the UBA asserts PBSY and negates QSACK.

16. The UBA now has control of the PMI bus and may initiate a PMI data transfer cycle(s) and/or an interrupt cycle.

NOTE
The CPU resumes NPR arbitration 75 ns after the negation of QSACK but does not resume BR arbitration until it has updated the PC and PSW to complete the interrupt cycle or has aborted the interrupt request.

When a UNIBUS device becomes UNIBUS master through an interrupt request, it can perform interrupt vector cycles or UNIBUS DATI, DATIP, DATO, and DATOB cycles. If the device accesses a PMI memory location, a PMI I/O page location, or a UNIBUS I/O page location, the UBA responds as UNIBUS slave. For PMI memory and PMI I/O page accesses, the UBA, as the PMI master, controls the PMI portion of the data transfer. BDIN and BIACK being asserted does not effect the data transfer.

Data transfer cycles are described in Section 5.2.5.

The following sequence describes the interrupt transfer cycle:

17. The interrupting device, as bus master, gates its vector onto the data lines and asserts INTR.

PMI Bus	UNIBUS
18. The UBA, as PMI master, asserts BRPLY on the PMI.	
	19. The UBA as slave receives the assertion of INTR and latches the interrupt vector.
	20. The UBA asserts SSYN.
21. The UBA gates the vector onto the DAL lines.	
22. The CPU latches the interrupt vector 200 ns minimum after receiving BRPLY.	
23. The CPU negates BDIN and BIAK.	
24. The UBA receives the negation of BIACK and negates BRPLY.	
	25. After receiving SSYN, the device removes its vector from the data lines and negates INTR and BBSY.
26. The UBA negates PBSY.	

5.2.4 PMI Data Transfer Address Cycle

The addressing phase of the PMI cycle starts immediately after the CPU or UBA has gained PMI master status and has asserted PBSY on the PMI.

The PMI bus acquisition phase is described in Section 5.2.1.

PMI Master	PMI Slave

1. The address is gated out on BDAL <21:00>, and BS7 is asserted if the address is in the I/O page. The signal lines BWTBT and PBYT are asserted to indicate the cycle to be performed:

BWTBT	PBYT	Bus Cycle Type
H	H	DATI or DATB
H	L	DATIP
L	H	DATO
L	L	DATOB

2. When a valid address is decoded by a slave, it responds as follows:

   a. The UBA asserts PUBMEM if the address is UNIBUS memory or UNIBUS I/O page.

   b. PMI memory and the CPU assert PSSEL.

PMI Master	PMI Slave
3. PBCYC is asserted.	
4. How the cycle proceeds is dependent on whether the CPU or UBA is master, and on what the response was from the slave as follows:	
a. When the CPU is PMI master:	
If PSSEL is asserted and PUBMEM is negated, the CPU proceeds with a PMI memory cycle.	
If PSSEL is negated, the CPU performs a PMI cycle with the UBA responding as the PMI slave.	
b. When the UBA is PMI master:	
If PSSEL is negated, then the UBA aborts the PMI cycle and does not respond as the UNIBUS slave.	

5.2.5 PMI Data Transfer Protocol

After the data transfer address cycle ends, the data transfer cycle begins. The transfer of data on the PMI can be grouped into three general types of PMI data transfer cycles:

- The data in (DATI) and data in pause (DATIP) cycles. These are used to read one or two words.
- The block data in (DATBI) cycle. This is used to read up to 16 words.
- The data out (DATO) and data out byte (DATOB) cycles. These cycles are used to write a single word or byte.

The following sections describe each of the data transfer cycles.

5.2.6 DATI and DATIP Cycles

When accessing the PMI memory address space, a PMI master uses the DATI(P) cycle to read either one or two words of data. When accessing the I/O page, a PMI master reads single words only.

The PMI DATIP cycle is identical to the DATI cycle with one exception: PBYT is asserted with the address to indicate that the next cycle (immediately following the current cycle) will be a DATO cycle to the same address.

The following flow is a description of a DATI(P) data transfer cycle.

PMI Master	PMI Slave
PBCYC is asserted during the addressing phase of the cycle (described in Section 5.2.4).	
	1. Data from the specified address is gated onto the bus.
	2. If the slave is PMI memory, PHBPAR and PLBPAR are generated and gated onto the bus.
	3. PRDSTB is asserted.
	4. PRDSTB is negated.
5. The first data word, with PHBPAR and PLBAR, is latched on the negating edge of PRDSTB. If only one word is to be read, PBCYC is negated and the cycle ends. If two words are to be read, PBCYC remains asserted. If a read-modify-write (DATIP) is being performed, a DATO cycle will take place here. The DATO(B) cycle is described in Section 5.2.8.	
	6. The second data word is gated onto the bus 80 ns maximum after the negation of PRDSTB.
	7. PHBPAR and PLBPAR are generated for the second data word and are gated onto the bus 100 ns after the negation of PRDSTB.
8. The second data word, along with PHBPAR and PLBAR, are received 145 ns maximum after the negating edge of PRDSTB. PBCYC is negated and the cycle ends. If a read-modify-write (DATIP) is being performed, PBCYC remains asserted, and a DATO cycle is performed here. The DATO(B) cycle is described in Section 5.2.8.	

PMI Master	PMI Slave
	9. Data is removed from the bus after receiving the negation of PBCYC.

5.2.7 DATBI

When accessing the memory address space, a PMI master uses the PMI block mode data in (DATBI) cycle to read up to 16 words of data. A PMI master does not use the DATBI cycle when accessing the I/O page.

The PMI master can start DATBI data transfers on even word boundaries only and does not cross 16 word boundaries. This means that at the transfer start, address bits <01> and <00> must both equal zero, and the master terminates the transfer when address bits <04:01> are all equal to one.

The following flow describes the DATBI cycle.

PMI Master	PMI Slave
PBCYC is asserted during the addressing phase of the cycle. The addressing phase is described in Section 5.2.4	
1. PBLKM is asserted.	
	2. Data from the specified address is gated onto the bus.
	3. If the slave is PMI memory, PHBPAR PLBPAR are generated and gated onto the bus.
	4. PRDSTB is asserted.
	5. PRDSTB is negated, and the data is removed from the bus.
6. The first data word, with PHBPAR and PLBAR, is latched on the negating edge of PRDSTB.	
	7. The second data word is gated onto the bus 80 ns maximum after the negation of PRDSTB.
	8. PHBPAR and PLBPAR are generated for the second word and gated onto the bus 100 ns maximum after the negation of PRDSTB.
9. The second data word, with PHBPAR and PLBPAR, is received 145 ns maximum after the negating edge of PRDSTB.	
10. PBLKM is negated after latching the second data word.	
	11. The second data word is removed from the bus after receiving the negation of PBLKM.

PMI Master	PMI Slave
12. Data transfer cycles continue in the same manner as steps 1 through 11 above until two words are left to be transferred. The last two words are transferred with the same timing, but the signal PBLKM is not asserted by the master.	
13. PBCYC is negated after latching the last data word.	
	14. Data is removed from the bus after receiving the negation of PBCYC.

5.2.8 DATO and DATOB

The PMI master uses the PMI Data Out (DATO or DATOB) cycles to transfer a single word or byte to a PMI slave.

The following flow describes a DATO(B) cycle.

PMI Master	PMI Slave
PBCYC is asserted during the addressing phase of the cycle. The addressing phase is described in Section 5.2.4	
1. PBCYC is asserted and data is gated onto the bus.	
2. PWTSTB is asserted.	
	3. The assertion of PWTSTB is received, and the data is latched in.
	4. PSBUFL is asserted.
5. PWTSTB is negated.	
6. PBCYC is negated.	
	7. PSBUFL is negated.

5.3 Map of Registers

Table 5–2 lists the register addresses in numeric sequence and the section in this chapter where complete information is available.

Table 5–2 Map of Registers

Address	Description	Section
	Page address registers	5.4.1
	Page descriptor registers	5.4.2
1777xxx0	Receiver status register	5.10.1
1777xxx2	Receiver data buffer register	5.10.2
1777xxx4	Transmitter status register	5.10.3
1777xxx6	Transmitter data buffer register	5.10.4
17772516	Memory management register 3	5.4.6
17777520	Control/status register (CSR)	5.6.3
17777522	Page control register	5.6.4
17777524	Boot and diagnostic configuration register	5.6.5
17777526	Additional status registers	5.6.6
17777546	Clock status register	5.6.7
17777572	Memory management register 0	5.4.3
17777574	Memory management register 1	5.4.4
17777576	Memory management register 2	5.4.5
17777730	Diagnostic controller status register	5.13.1
17777732	Diagnostic data register	5.13.2
17777734	Memory configuration register	5.12.2
17777744	Memory system error register	5.5.1
17777746	Cache control register	5.5.2
17777750	Maintenance register	5.6.8
17777752	Hit/miss register	5.5.3
17777766	CPU error register	5.6.9
17777772	Program interrupt request register	5.6.10
17777776	Processor status word	5.6.11

5.4 Memory Management

Memory management is located on the KDJ11-E and is used to relocate a 16-bit virtual address. The PMI function of memory management is address modification. The modification of addresses is called relocation because it consists of adding a fixed constant to a virtual address to create a physical address.

Using the process of relocation, a user can load a program into one area of physical memory and execute it as if it were located in another area of memory. Several user programs, for example, can be simultaneously stored in memory. When any one program is running, it must be accessed by the processor as if it were located in the set of addresses beginning at 0.

When the processor accesses virtual bus address 0, a base address is added to the virtual bus address. The relocated 0 location of the program is accessed. Typically, this base address is added to all references while the program is running. A different base address is used for each of the other programs in memory.

Memory management also allows the user to protect a section of memory from access by programs located in another section. Memory management divides memory into individual sections called pages.

Each page has a protection or access key associated with it. The key defines the type of access allowed on a particular page. With the memory management unit, a page can be keyed either nonresident that is memory is neither readable nor writable, or memory readable, for no write operations. These two types of protection, in association with other features, enable the user to develop a secure operating system.

Memory management specifies relocation on a page basis. A large program can then be loaded into nonadjacent pages in memory. This capability eliminates the need to shuffle programs to accommodate a new one. It also minimizes unusable memory fragments, thus allowing more users to be loaded into a specific memory size.

A program and its data can occupy as many as 16 pages in the memory. The size of each page may vary and can be any multiple of 32 words up to 4096 words in length. This feature allows small areas of memory to be protected (stacks, buffers, etc.). In addition, the last page of a program, exceeding 4K words, can be of adequate length to protect and relocate the remainder of the program.

As a result, the memory fragmentation problem inherent with fixed-length pages is eliminated. The base address of each page can be any multiple of 32 words in the physical address space, thus ensuring efficient use of PMI memory. The variable page length also allows the pages to be dynamically changed at run time.

Memory management provides three separate sets of pages for use in the processor kernel, supervisor, and user modes. These sets of pages increase system protection by physically isolating user programs from service supervisor programs and the kernel program.

The service programs are also separated from the kernel program. Separate relocation register sets greatly reduce the time necessary to switch context between mapping. The three sets of registers also aid the user in designing an operating system that has clearly defined communications, is modular, and is able to be easily debugged and maintained.

The virtual bus address space is further divided, within each of the kernel, supervisor, and user pages, into instruction space and data space (I and D space). The I space contains code, that is, any word that is part of the program such as instructions, index words, and immediate operands. The D space contains information that can be modified, such as data buffers.

By using this feature, memory management can relocate data and instruction references with separate base address values. It is possible, therefore, to have a user program of 64K words consisting of 32K of instructions and 32K of data.

The memory management registers consist of 48-page address registers (PARs), 48-page descriptor registers (PDRs), and four memory management registers (MMR0-3). These registers are located on the KDJ11-E module. The following sections describe each of the registers.

5.4.1 Page Address Registers

The page address registers (PARs) contain the 16-bit page address field (PAF). The PAR specifies the base address of the page, see Figure 5–2. All bits are read/write. These registers are not affected by console start or a RESET instruction. Their state at power-up is undefined.

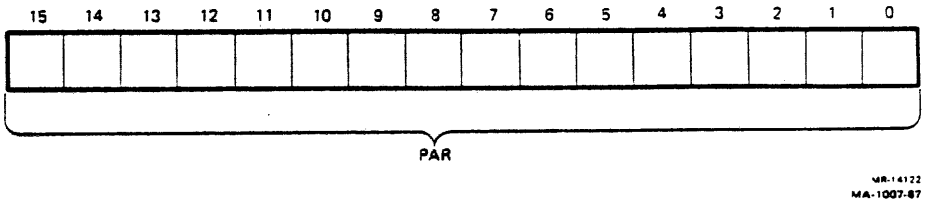


Figure 5–2 Page Address Register Format

5.4.2 Page Descriptor Registers

The page descriptor registers (PDRs) contain information relative to page expansion, page length, and access control. These registers are not affected by console start or a RESET instruction. Their state at power-up is undefined. All unused bits are read as zero and cannot be written. The register format is shown in Figure 5–3.

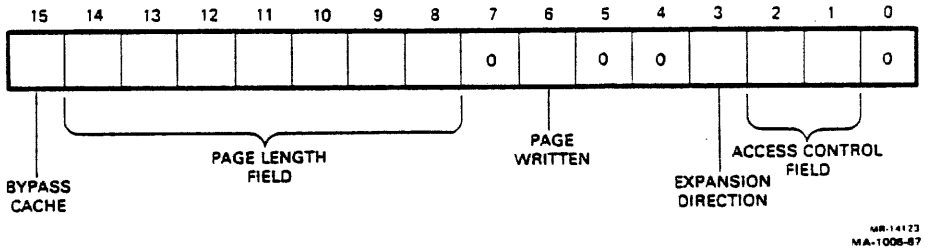


Figure 5–3 Page Descriptor Register Format

Table 5–3 provides page descriptor register bit descriptions.

Table 5–3 Page Descriptor Register Bit Descriptions

Bit(s)	Name	Function
15	Bypass Cache (R/W)	This bit is for compatibility purposes only and should always remain reset.
14:8	Page Length Field (R/W)	This field specifies the block number that defines the boundary of the current page. The block number of the virtual address is compared against the page length field to detect length errors. An error occurs when expanding upwards if the block number is greater than the page length field; an error occurs when expanding down if the block number is less than the page length field.
06	Page Written Field (R/W)	This bit indicates whether or not this page has been modified (written into) since either the PAR or PDR was loaded (1 is affirmative). It is useful in applications which involve disk swapping and memory overlays. It is used to determine which pages have been modified and hence must be saved in their new register bit and which pages have not been modified and can simply be overlaid. Whenever the PDR or the associated PAR is written into, this bit is reset to 0.
03	Expansion Direction (R/W)	This bit specifies in which direction the page expands. If ED=0, the page expands upwards from block number 0 to include blocks with higher addresses. If ED=1, the page expands downwards from block number 127 to include blocks with lower addresses. Upward expansion is usually used for program space while downward expansion is used for stack space.
2:1	Access Control	This field contains the access rights to this particular page. The access codes, or "keys," specify the manner in which a page may be accessed and whether or not a given access should result in an abort of the current operation. The access codes are: 00 Nonresident - abort all accesses 01 Read only - abort on writes 10 Not used - abort all accesses 11 Read/write

5.4.3 Memory Management Register 0 (17777572)

Memory management register 0 (MMR0), at address 17777572, contains error flags, that is the page number whose reference caused the abort, and various other status flags. MMR0 is cleared at power-up by a console start and by a RESET instruction. Figure 5–4 shows the register format.

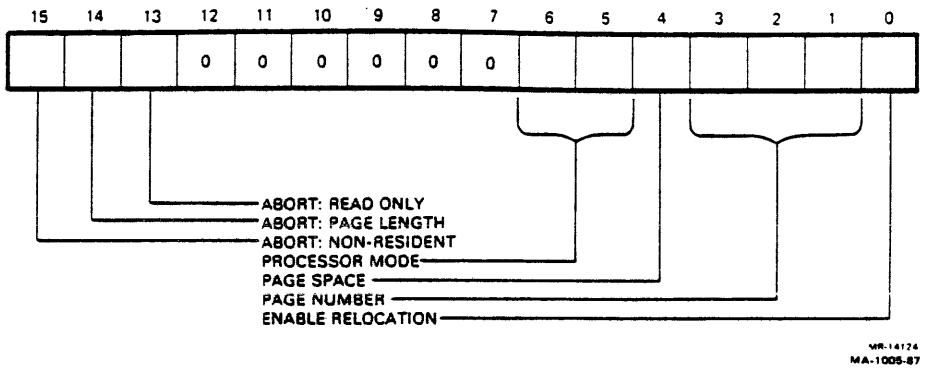


Figure 5–4 Memory Management Register 0 Format (17777572)

Table 5–4 provides memory management register 0 bit descriptions.

Table 5–4 Memory Management Register 0 Bit Descriptions

Bit(s)	Name	Function
15	Abort—Nonresident (R/W)	Bit 15 is set by attempting to access a page with an access control field key equal to 0 or 2. It is also set by attempting to use memory relocation with a mode (PS <15:14>) of 2.
14	Abort—Page Length (R/W)	This bit is set by attempting to access a location in a page with a block number (virtual address bits <12:6>) that is outside the area authorized by the page-length field of the page descriptor register for that page.
13	Abort—Read Only (R/W)	This bit is set by attempting to write in a "read only" page. Read only pages have access keys of 1.

NOTE
Bits <15:13> can be set by an explicit write. This action, however, does not cause an abort. Whether set explicitly or by an abort, bits <15:13> cause memory management to freeze the contents of MMR0 <6:1>, MMR1, and MMR2. The status registers remain frozen until MMR0 <15:13> is cleared by an explicit write or any initialization sequence.

6:5	Processor Mode (RO)	These bits indicate the processor mode (kernel/supervisor/user /illegal) associated with the page causing the abort (kernel = 00, supervisor = 01, user = 11, illegal = 10). If the illegal mode is specified, an abort is generated and bit <15> is set.
4	Page Space (RO)	This bit indicates the address space (I or D) associated with the page causing the abort (0 = I space, 1 = D space).
3:1	Page Number (RO)	These three bits contain the page number of the page causing the abort.
00	Enable Relocation (R/W)	This bit allows address relocation. When set to 1, all addresses are relocated. When bit 0 is set to 0, memory management is inoperative and addresses are not relocated.

5.4.4 Memory Management Register 1 (17777574)

Memory management register 1 (MMR1) at address 17777574 records any auto increment or decrement of the general purpose registers. This register supplies the information necessary to recover from a memory management abort. MMR1 is read only. Its state at power-up is undefined. Figure 5–5 shows the register format.

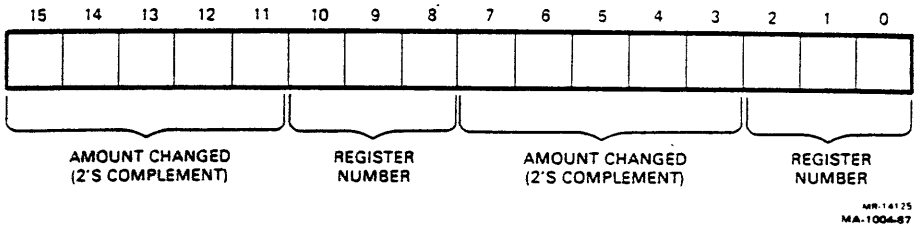


Figure 5–5 Memory Management Register 1 Format (17777574)

5.4.5 Memory Management Register 2 (17777576)

Memory management register 2 (MMR2) at address 17777576 is loaded with the virtual address at the beginning of each instruction fetch. MMR2 is read only. Its state at power-up is undefined. Figure 5–6 shows the register format.

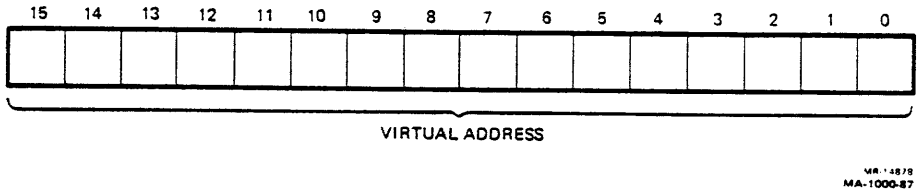


Figure 5–6 Memory Management Register 2 Format (17777576)

5.4.6 Memory Management Register 3 (17772516)

Memory management register 3 (MMR3) at address 17772516 enables or disables D space, 22-bit mapping, the CSM instruction, and the I/O map (when applicable). MMR3 is cleared at power-up by a console start and by a RESET instruction. Figure 5–7 shows the register format.

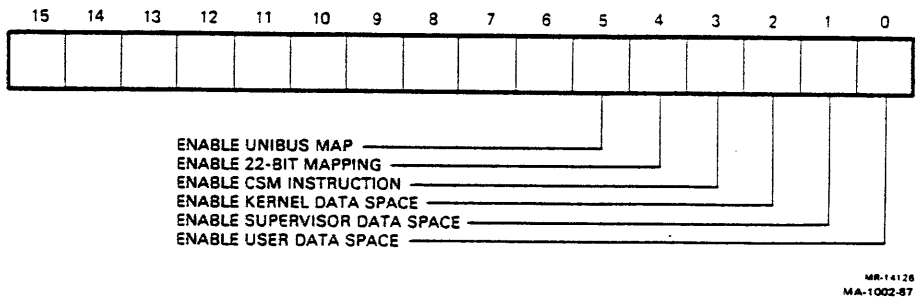


Figure 5–7 Memory Management Register 3 Format (17772516)

Table 5–5 provides memory management register 3 bit descriptions.

Table 5–5 Memory Management Register 3 Bit Descriptions

Bit(s)	Name	Function
15:06	–	Unused.
05	Enable UNIBUS Map (R/W)	This bit enables the I/O map for the UNIBUS adapter.
04	Enable 22-bit Mapping (R/W)	This bit, when set, selects 22-bit memory addressing. When this bit is clear, 18-bit addressing is selected. (Only when MMR0 bit <0> is set is 18- or 22-bit addressing actually enabled.)
03	Enable CSM Instruction (R/W)	This bit enables recognition of the Call Supervisor Mode (CSM) instruction.
2:0	Enable Data Space (R/W)	These three bits enable data space mapping for kernel, supervisor, and user mode, respectively.

5.4.7 Physical Address Construction

If UNIBUS map relocation is enabled (MMR3 bit <05> = 1), UNIBUS address bits <17:13> select one of 31 mapping register pairs (corresponding to octal codes 00 through 36). The content of the selected mapping register pair is added to UNIBUS address bits <12:00> to produce the memory address. If UNIBUS address bits <17:13> are all 1s (octal code 37), the I/O page is selected. Memory address bits <21:18> are all set equal to zero, memory address bits <17:00> are identical to UNIBUS address bits <17:00>, and BBS7 is asserted (Figure 5–8).

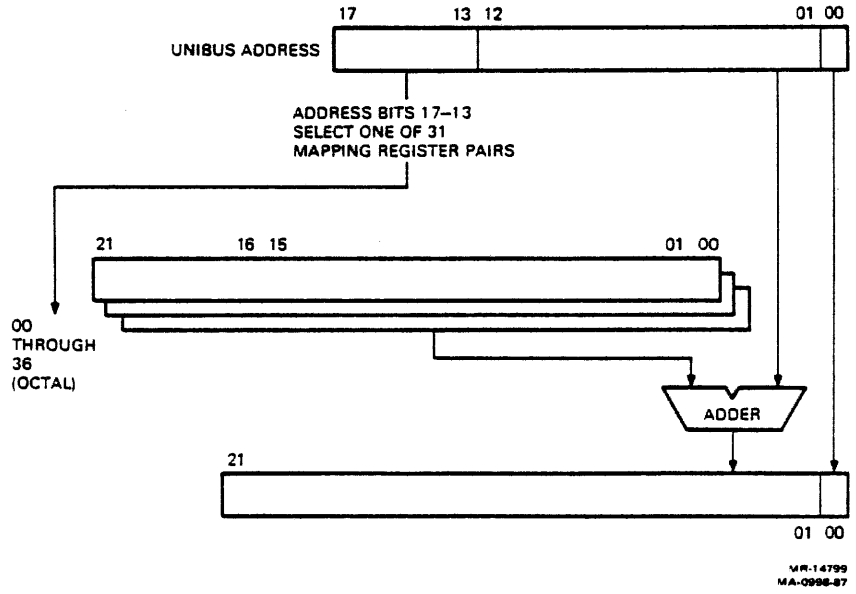


Figure 5–8 Physical Address Interpretation

5.4.8 Memory Relocation

When memory management is enabled, the normal 16-bit direct-byte address is no longer interpreted as a direct physical address. Instead, this address is interpreted as a virtual bus address containing information to be used in constructing a new 22-bit physical address. The information contained in the virtual bus address is combined with relocation information contained in the page address register to make a 22-bit physical address. Using memory management, memory can be dynamically allocated in pages composed of from 1 to 128 blocks of 32 words each.

The starting physical address for each page is a multiple of 32 words. Each page has a maximum size of 4096 words. Pages may be located anywhere within the physical address space. The set of 16 PARs to be used to create the physical address is determined by the current mode of operation of the CPU (kernel, supervisor, or user modes).

5.5 KDJ11-E Cache Implementation

Technological advances implemented on the KDJ11-E allow the onboard memory to perform at cache-like speeds, eliminating the need for cache. The KDJ11-E cache register set has been implemented for compatibility purposes only and all bits should remain cleared at all times.

5.5.1 Memory System Error Register (17777744)

The memory system error register (MSER) at address 17777744 reflects the status of cache and main memory parity errors. MSER bits <14> and <13> are used by the KDJ11-E boot and diagnostic programs to test the cache DMA tag store. Figure 5–9 shows the register format.

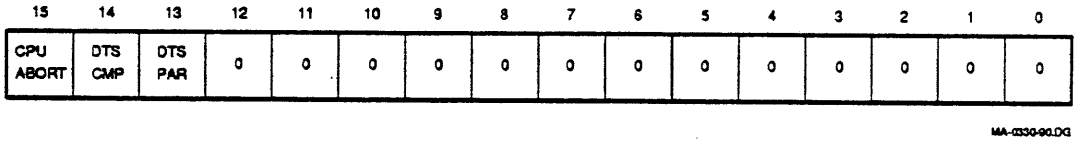


Figure 5–9 Memory System Error Register Format (17777744)

Table 5–6 provides memory system error register bit descriptions.

Table 5–6 Memory System Error Register Bit Descriptions

Bit(s)	Name	Function
15	CPU Abort(RO)	This bit is set if a main memory parity error results in an instruction abort (only during the demand read cycle). Main memory parity errors always cause an abort.
14	DMA Tag Store Comparator (DTS CMP) (RO)	In standalone mode (CSR <8> set), this bit indicates the output of the cache DMA tag store comparator for the previous non-I/O page reference with cache miss. When CSR <8> is clear, DTS CMP reads as a 0.
13	DMA Tag Store Parity (DTS PAR) (RO)	In standalone mode (CSR <8> set), this bit indicates the output of the DMA tag store parity check Logic for the previous non-I/O page reference with cache miss. When CSR <8> is clear, DTS PAR reads as a 0.

Table 5–6 (Cont.) Memory System Error Register Bit Descriptions

Bit(s)	Name	Function
12:00	Unused	These bits always read as 0.

Main memory parity errors always cause the CPU to abort the current instruction, to set MSER <15>, and to trap through vector location 114.

5.5.2 Cache Control Register (17777746)

The cache control register (CCR) is at address 17777746. This register is used for compatibility with former designs only. All bits should be cleared at all times. Figure 5–10 shows the register format.

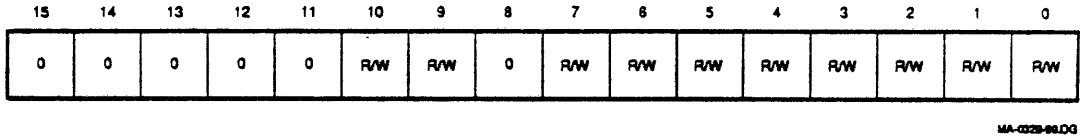


Figure 5–10 Cache Control Register Format (17777746)

NOTE
All bits should be cleared at all times.

5.5.3 Hit/Miss Register (17777752)

This register, at address 17777752, is for compatibility purposes only.

5.6 General Purpose Registers

There are 16 general purpose registers (GPR). Only eight are visible to the user Table 5–7. All registers can be used as accumulators, indirect addresses (with autoincrement and autodecrement), index addresses, and stack pointers.

Table 5–7 General Purpose Registers

Register	Description
0	R0 or R0' (depends on PSW bit 11)
1	R1 or R1' (depends on PSW bit 11)
2	R2 or R2' (depends on PSW bit 11)
3	R3 or R3' (depends on PSW bit 11)
4	R4 or R4' (depends on PSW bit 11)
5	R5 or R5' (depends on PSW bit 11)
6	KSP or SSP,USP (depends on PSW bit 15, 14)
7	PC

5.6.1 Registers

There are two groups of registers that are referred to as R0-R5 and R0'-R5'. The group currently used is selected through bit 11 in the processor status word (PSW). If bit 11 is set to 1, the R0'-R5' group is selected. If bit 11 is reset (0), the R0-R5 group is selected.

5.6.2 Parity CSR Register (17772100)

The parity CSR register is used to control parity checking. Parity checking should only be enabled after the entire memory has been written to and the right parity has been generated. Wrong parity can also be written for test purposes (WWPAR). Figure 5–11 shows the register format.

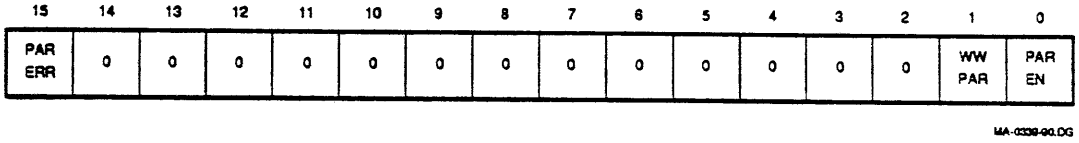


Figure 5–11 Parity CSR Register (17772100)

Table 5–8 describes the parity CSR register (17772100).

Table 5–8 Parity CSR Register (17772100)

Bit(s)	Name	Status	Function
15	PAR ER	R/W	Parity error. Bit 15 is set when a parity error is detected in the main memory. Bit 15 is reset by a power-up, INIT command. This bit can also be written.
14:03	–	–	Not used. These bits are always set at 0.
02	WWPAR	R/W	Write wrong parity. When set, "wrong" parity bits are written in to the main memory with each write access made. This provokes a parity error with each read access that follows.
01	–	–	Not used. This bit is always set at 0.
00	PAREN	R/W	Parity checking enable. When set, parity checking is enabled. When enabled, parity errors detected will cause a parity trap. This bit is reset by a power-up or INIT command.

5.6.3 Control/Status Register (17777520)

The control/status register (CSR), at address 17777520, is both word and byte addressable. Figure 5–12 illustrates the register format. The CSR allows the boot and diagnostic ROM programs to test battery backup status, to set parameters for the line clock, to enable the console halt-on break feature, and to enter or exit from standalone mode.

The CSR also allows these programs to selectively disable the response of the boot and diagnostic ROMs at addresses 17765000–17765776 and/or at addresses 17773000–17773776 and to control read/write access to the EEPROM memory.

Programs that access the I/O page can use the CSR to alter the line clock parameters, to enable or disable the halt-on-break feature, and to control access to the ROM and EEPROM memories.

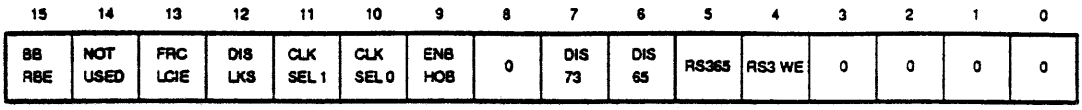


Figure 5–12 Control/Status Register Format (17777520)

Table 5–9 provides the control/status register bit descriptions.

Table 5–9 Control/Status Register Bit Descriptions

Bit(s)	Name	Function
15	BB RBE	Battery Backup Reboot Enable. When set, this bit indicates that battery backup failed to maintain voltages to the memory system during the previous power failure. When this bit is clear, it indicates that the system does not feature battery backup, or that battery backup maintained voltages during the previous power failure. This signal is received from backplane pin BH1 and latched when DC OK is asserted.
14	–	Unused.
13	FRC LCIE	Force Line Clock Interrupt Enable. If this bit is set, assertion of the signal selected by CSR <11> and <10> (clock select bits <1> and <0>) will unconditionally request interrupts. If FRC LCIE is clear, assertion of the selected signal will request interrupts only if the line clock status register bit <6> (LCIE) is set under program control. FRC LCIE is cleared by the negation of DCOK.
12	DIS LKS	Line Clock Status Register Disable. If this bit is set, the line clock status register (LKS) is disabled. If this bit is clear, LKS is enabled and responds to bus address 17777546. LKS DIS is cleared by the negation of DCOK.
11 10	CLK SEL1 CLK SEL0	Clock Select Bits 1 and 0. These two bits select the source of the line clock interrupt request:

CLK SEL1	CLK SEL0	Source of Interrupt
0	0	Power supply
0	1	On-board 50 Hz
1	0	On-board 60 Hz
1	1	On-board 800 Hz

Both bits are cleared by the negation of DCOK.

09	ENB HOB (R/W)	Enable Halt on Break. When this bit is set, the console serial line unit halt-on-break feature is enabled. When this bit is clear, the feature is disabled. ENB HOB is cleared by the negation of DCOK.
08		Not used.

Table 5–9 (Cont.) Control/Status Register Bit Descriptions

Bit(s)	Name	Function
07	DIS 73 (R/W)	Disable 17773000. When this bit is set, response of the 16-bit ROM memory to addresses 17773000–17773776 is disabled, allowing the operation of an external ROM that uses those addresses. When DIS 73 is clear, the 16-bit ROMs respond to those addresses, using the high byte of the page control register as the most significant address bits. DIS 73 is cleared by the negation of DCOK.
06	DIS 65 (R/W)	Disable 17765000. When this bit is set, response of the boot and diagnostic 16-bit and 8-bit ROM memory to addresses 17765000–17765776 is disabled; this allows the operation of external ROM which uses those addresses. When DIS 65 is clear, the ROM memory selected by CSR <5> responds to those addresses, using the low byte of the page control register as the most significant address bits. DIS 65 is cleared by the negation of DCOK.
05	RS365	When this read/write bit is set (1), the EEPROM responds to addresses between 17765000 and 17765776, provided that bit 6 of the CSR is reset. When this bit 5 is reset (0), then the ROM at these addresses is selected instead. In both cases, the high byte of the ROM address is made up of the low byte of the PCR. The bit is reset through the negation of the DCOK inputs.
04	RS3 WE	When this read/write bit is set and the CSR bit 5 is set with the CSR bit 6 reset, then the program is able to write into the EEPROM. This bit is reset through power-up and initialization routines.
03:00	–	Unused. These bits always read as 0.

5.6.4 Page Control Register (17777522)

The PCR is a read/write register that can be addressed by words and bytes. Only the bits <15:9> and <7:1> can be used. The remaining bits will always be read as zeros. This register is reset through the negation of the DCOK input.

The PCR bits <15:9> become the ROM address bits <15:9> for the address area from 17773000 to 17773776 and together with the current address bits <8:0>, they make up a 16-bit address for the ROM on base U106. The PCR bits <7:1> becomes the ROM/EEPROM address bits <15:9> for the addresses from 17765000 TO 17765766 and together with the current address bits <8:0> they make up a 16-bit address for the ROM/EEPROM on socket U105.

The control/status register (CSR) bits <7:4> control the access to the ROM and EEPROM sockets and memory.

Figure 5–13 shows the register format.

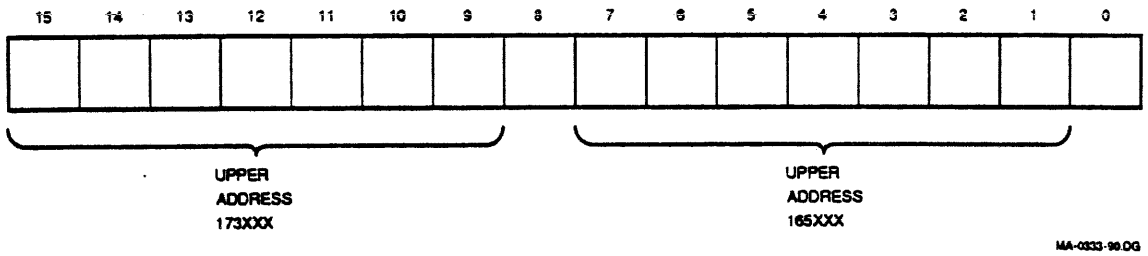


Figure 5–13 Page Control Register Format (17777522)

Table 5–10 provides the page control register bit descriptions.

Table 5–10 Page Control Register Bit Descriptions

Bit(s)	Name	Function
15:09	Upper address 173xxx	Used for address area 17773000 to 17773776.
08	Unused.	This bit always reads as 0.
07:00	Upper address 165xxx	Used for address area 17765000 to 17766766.

5.6.5 Configuration and Display Register (17777524)

The configuration and display register (CDR) consists of two independent registers which are pointed to by the same address:

- Read-only boot and diagnostic configuration register:

  The read-only boot and diagnostic configuration register specifies the status of the configuration switches (8 to 1) that are located on the module. When switches 8 to 1 on the KDJ11-E are set to off, the state of the register bits can be controlled using switches 8 to 1 on the external console/SLU panel. Figure 5–14 shows the register format.

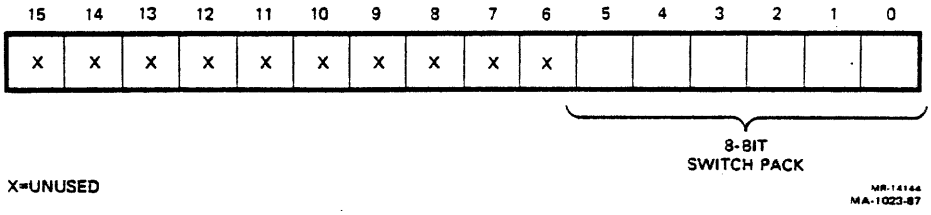


Figure 5–14 Boot and Diagnostic Configuration Register Format (17777524 - Write Only)

- Write-only boot and diagnostic display register:

  The write-only boot and diagnostic display register (BDR), at address 17777524, allows the boot diagnostic programs to light the front panel start-up test LED display and the LEDs on the KDJ11-E module. These display bits are also available on

an external connector. Bits <05:00> are cleared on power-up (all LEDs on) by the negation of DCOK. Figure 5–15 shows the register format.

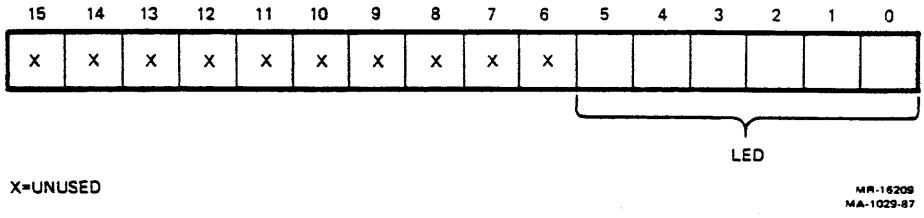


Figure 5–15 Boot and Diagnostic Display Register (17777524 - Write Only)

Table 5–11 provides the display register bit descriptions.

Table 5–11 Display Register Bit Descriptions

Bit(s)	Name	Function
15:06	–	Unused
05:00	LED 5–0	These bits enable the boot and diagnostic programs to light the LEDs located at the top of the CPU module. Clearing any of these bits lights the corresponding LED.

5.6.6 Additional Status Register (17777526)

The additional status register controls board-internal functional units such as memory and interfaces. It is used by the boot and test firmware to test the functions specified and to configure the corresponding setup setting. Basic processor functions are performed here. Figure 5–16 shows the register format.

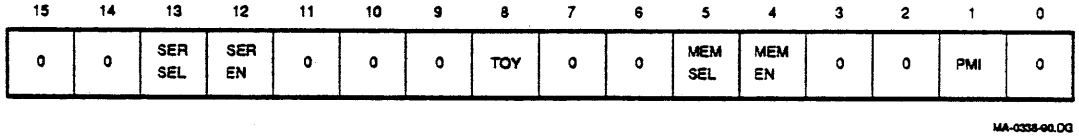


Figure 5–16 Additional Status Register (17777526)

Table 5–12 describes the additional status register.

Table 5–12 Additional Status Register

Bit(s)	Status	Function		
15, 14	–	Not used. These bits always read as 0.		
13, 12	R/W	Selects interfaces internally as follows:		
		SERSEL	**SEREN**	**Serial lines address/vector**
		13	12	
		0	1	7/8 SLUs on 176500/300
		1	1	7/8 SLUs on 176600/400

Table 5–12 (Cont.) Additional Status Register

Bit(s)	Status	Function		
		0	0	No serial lines selected.
11-9	–	Not used. These bits always read as 0.		
8	R/W	This bit is used for serial communication to the TOY.		
7, 6	–	Not used. These bits always read as 0.		
5, 4	R/W	Selects internal memory as follows:		
		MEMSEL	**MEMSEN**	**Function**
		0	0	0 Mbyte memory
		0	1	0-2 Mbyte memory
		1	1	0-4 Mbyte memory
3, 2	–	Not used. This bit always reads as 0.		
1	R/W	Flag for PMI-Cycle (set by system).		
0	–	Not used. This bit always reads as 0.		

5.6.7 Line Frequency Clock and Status Register (17777546)

The line clock provides the system with timing information at fixed intervals determined by the UNIBUS LTC line or by one of the on-board KDJ11-E frequency signals. The signals are programmed by boot and diagnostic controller status register bits <11> and <10>. Typically, LTC cycles at the AC line frequency, producing intervals of 16.7 ms (60 Hz line) or 20.0 ms (50 Hz line). The three on-board frequencies are 50 Hz, 60 Hz and 800 Hz.

The LKS, at address 17777546, allows line clock interrupts to be enabled and disabled under program control. Alternatively, line clock interrupts can be unconditionally enabled by setting CSR <13> (FRC LCIE). Program recognition of the clock status register can be disabled by setting CSR <12> (LKS DIS).

The normal KDJ11-E configuration is FRC LCIE and LKS DIS both clear. These bits are set up by the boot and diagnostic ROM programs from the KDJ11-E configuration data. Figure 5–17 shows register format.

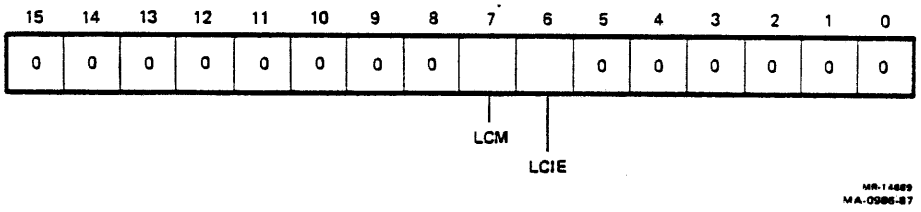


Figure 5–17 Clock Status Register Format (17777546)

Table 5–13 provides the clock status register bit descriptions.

Table 5–13 Clock Status Register Bit Descriptions

Bit(s)	Name	Function
15:08	–	Unused. Always read as 0.
07	LCM (R/W)	Line Clock Monitor. This bit is set by the leading edge of the external BEVENT line (or of one of the three on-board clock frequencies) and by bus initialization. LCM is cleared automatically on processor interrupts acknowledge. It is also cleared by writes to the LKS with bit <7> = 0.
06	LCIE (R/W)	Line Clock Interrupt Enable. This bit, when set, causes the set condition of LCM (LKS <7>) to initiate a program interrupt request at a priority level of 6. When LCIE is clear, line clock interrupts are disabled. LCIE is cleared by power-up and by bus initialization. LCIE is held set INIT. LCIE is held set when CSR <13> (FRC LCIE) is set.
05:00	–	Unused. Always read as 0s.

5.6.8 Maintenance Register (17777750)

The DCJ-11 microcode addresses the maintenance register at address 17777750 and reads BPOK H, the power-up option code, and the halt/trap option bit. Other bits in the maintenance register, not used by DCJ-11 microcode, contain information on the module type and system parameters useful to operating system and diagnostic software. Figure 5–18 shows the register format.

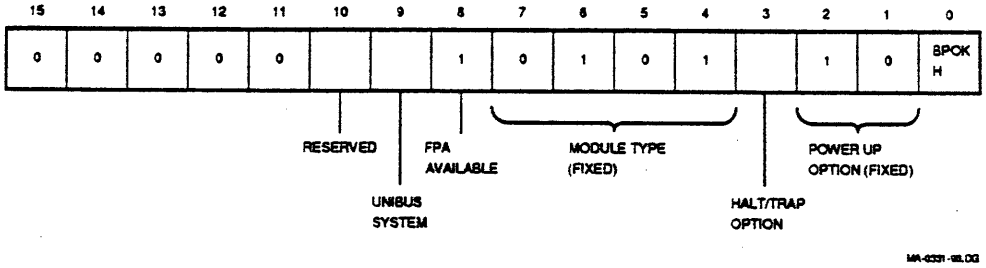


Figure 5–18 Maintenance Register Format (17777750)

The power-up option code is hard-wired for standard bootstrap operation (code 2). The PSW is set to 340, and the processor begins program execution at address 173000. The boot and diagnostic code, which starts at that location, configures the KDJ11-E. The code runs standalone diagnostics before acting on the user-specified power-up option stored as part of the EEPROM configuration data.

Table 5–14 provides the maintenance register bit descriptions.

Table 5–14 Maintenance Register Bit Descriptions

Bit(s)	Name	Function
15:11	–	Unused. Reserved for future expansion. Read as 0s.
10	–	Unused. Reserved for future use.

Table 5–14 (Cont.) Maintenance Register Bit Descriptions

Bit(s)	Name	Function
09	UNIBUS System (RO)	This bit reflects the status of the externally applied UNIBUS adapter line. A 1 indicates that the system includes a UNIBUS adapter.
08	FPA Available (RO)	This bit should be read as 1.
07:04	Module Type	This 4-bit code is hard-wired as a 5, indicating a KDJ11-E module.
03	Halt/Trap (R/W)	This read/write bit determines the response of a processor to a kernel mode halt instruction. Setting the bit selects the trap option, causing the CPU to trap to location 4. Clearing the bit selects the halt option, causing the CPU to halt and enter ODT. This bit is cleared by the negation of DCOK and is set by the boot and diagnostic ROM code if the trap option is selected by a bit in the configuration RAM. The trap option is not intended for normal use and is reserved for controller applications.
02:01	Power-Up Code	This 2-bit code is hard-wired as a 2. At power-up, the processor sets the PC to 173000 and sets the PSW to 370. It then starts program execution at location 173000, which is the starting location for the KDJ11-E boot and diagnostic ROM program. These programs test the KDJ11-E module and then implement the user-selected power-up option specified in the configuration data.
00	BPOK H	This bit is set (1) if the PMI bus signal BPOK H is asserted, indicating that AC power is acceptable.

5.6.9 CPU Error Register (17777766)

The error register, at address 17777766, identifies the source of any abort or trap that caused a trap through location 4. The CPU error register is cleared when it is written. It is also cleared at power-up or by console start. It is unaffected by a RESET instruction. Figure 5–19 shows the register format.

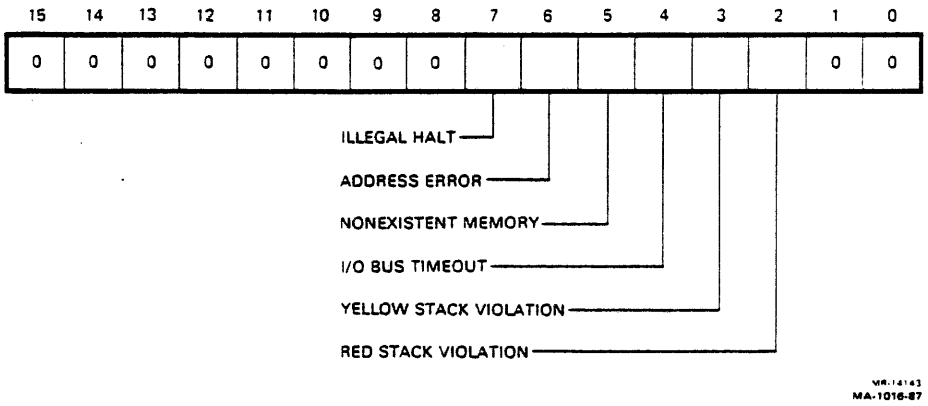


Figure 5–19 CPU Error Register Format (17777766)

Table 5–15 provides the CPU error register bit descriptions.

Table 5–15 CPU Error Register Bit Descriptions

Bit(s)	Name	Function
7	Illegal HALT	Set when execution of a HALT instruction is attempted in user or supervisor mode.
6	Address Error (RO)	Set when word access to an odd byte address or an instruction fetch from an internal register is attempted.
5	Nonexistent Memory (RO)	Set when a reference to main memory times out.
4	I/O Bus Timeout (RO)	Set when a reference to the I/O page times out.
3	Yellow Stack Violation (RO)	Set on a yellow zone stack overflow trap.
2	Red Stack Violation (RO)	Set on a red zone stack overflow trap.

5.6.10 Program Interrupt Request Register (17777772)

The program interrupt request register (PIRQ), at location 17777772, implements a software interrupt facility. When a program interrupt request is granted, the processor traps through location 240. It is the responsibility of the interrupt service routines to clear the appropriate bit in PIRQ before exiting. PIRQ is cleared at power-up by a console start and by the RESET instruction. Figure 5–20 illustrates the register.

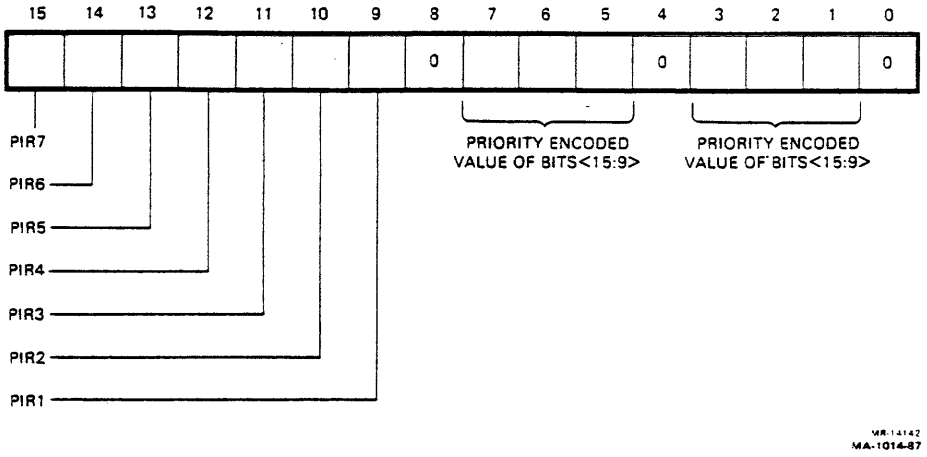


Figure 5–20 Program Interrupt Request Register (17777772)

Table 5–16 provides the program interrupt register bit descriptions.

Table 5–16 Program Interrupt Register Bit Descriptions

Bit(s)	Name	Function
15:09	PIR 7–1	Each bit, when set, provides one of seven levels of software interrupt, corresponding to interrupt priority levels 7 through 1.

Table 5–16 (Cont.) Program Interrupt Register Bit Descriptions

Bit(s)	Name	Function
08	–	Unused.
07:05	Priority encoded value of bits <15:09>	These three bits are set by the CPU to the encoded value of the highest pending interrupt request (bits <15:09>).
04	–	Unused.
03:01	Priority encoded value of bits <15:09>	The function of these bits is identical to bits <07:05>.

5.6.11 Processor Status Word (17777776)

The processor status word (PSW) at location 17777776 contains information on the status of the processor. The PSW is initialized at power-up (depending on EEPROM CONFIGURATION options) and is cleared at console start. The RESET instruction does not affect the PSW. Figure 5–21 illustrates the register.

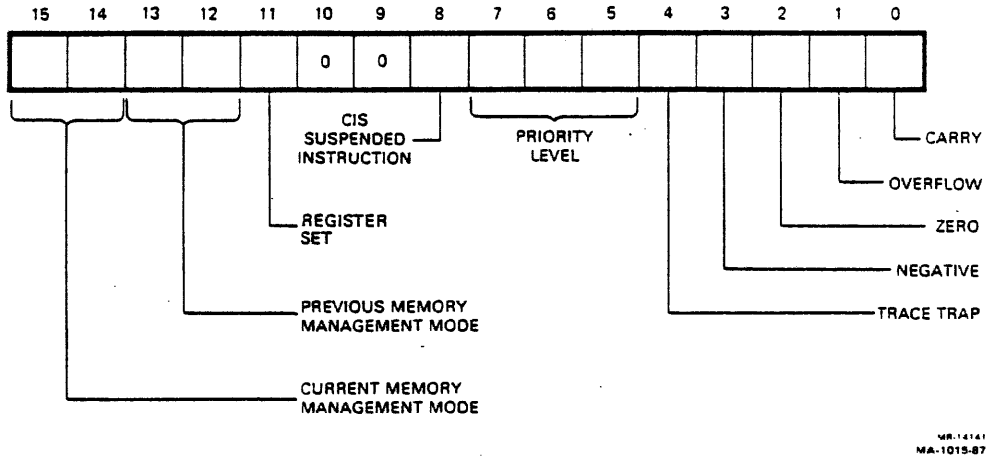


Figure 5–21 Processor Status Word Register (17777776)

Table 5–17 provides the processor status word bit descriptions.

Table 5–17 Processor Status Word Bit Descriptions

Bit(s)	Name	Function
15:14	Current Mode (R/W, protected)	Current processor mode: 00 = kernel 01 = supervisor 10 = illegal (traps) 11 = user
13:12	Previous Mode (R/W, protected)	Previous processor mode, same encoding as current mode.

Table 5–17 (Cont.) Processor Status Word Bit Descriptions

Bit(s)	Name	Function
11	Register Set (R/W, protected)	General register set select: 0 = register set 0 1 = register set 1
08	Suspended Instruction (R/W)	Reserved for future use.
7:5	Priority (R/W, protected)	Processor interrupt priority level.
04	Trace Trap (R/W, protected)	Set to force a trace trap.
03	Negative (R/W protected)	Flag N is set when the result of the previous operation is negative.
02	Zero (R/W protected)	Flag Z is set when the result of the previous operation is zero.
01	Overflow (R/W protected)	Flag V is set when the result of the previous operation is an arithmetic overflow.
00	Carry (R/W protected)	Flag C is set when the previous operation has caused a carry-over.

5.7 Stack Limit Protection

The KDJ11-E checks kernel stack references against a fixed limit of 400(8). If the virtual address of the stack reference is less than 400(8), a yellow stack trap occurs at the end of the current instruction.

A stack trap can only occur in kernel mode and only on a stack reference. A stack reference is defined as a mode 4 or 5 through R6, or a JSR, trap, or interrupt stack push.

In addition, the DCJ-11 checks for kernel stack aborts during interrupt, trap, and abort sequences. If during one of these sequences a kernel stack push causes an abort, the DCJ-11 initiates a red zone stack trap. The DCJ-11 sets CPU error register bit <2>, loads virtual address 4 into the kernel stack pointer (R6), and traps through location 4 in kernel data space. The old PC and PS are saved in kernel data space locations 0 and 2, respectively.

NOTE
The DCJ-11 microprocessor treatment of yellow stack trap is identical to that of the PDP-11/44 system. The PDP-11/70 system includes a stack limit register and a more inclusive definition of stack reference. The DCJ-11 processor's definition of a red stack trap is unique.

5.8 Kernel Protection

To protect the kernel operating system against interference, the KDJ11-E incorporates the following protection mechanisms:

- In kernel mode, HALT, RESET, and set processor level (SPL) execute as specified. In supervisor or user mode, HALT causes a trap through location 4, while RESET and SPL are treated as NOPs.

- In kernel mode, return from interrupt (RTI) and RTT can freely alter PSW <15:11> and PSW <7:5>. In supervisor or user mode, RTI and RTT can only set PSW <15:11> and cannot alter PSW <7:5>.
- In kernel mode, MTPS can alter PSW <7:5>. In supervisor or user mode, MTPS cannot alter PSW <7:5>.
- All trap and interrupt vector references are classified as kernel space references, irrespective of the memory management mode at the time of the trap or interrupt.
- Kernel stack references are checked for stack overflow. Supervisor and user stack references are not checked.

5.9 Trap and Interrupt Service Priorities

In both traps and interrupts, the currently executing program is interrupted. A new program is then executed, the starting address of which is specified by the trap or interrupt vector. The hardware process for traps and interrupts through a vector V is identical:

```
PS --> temp 1                    !save PS, PC in temporaries
PC --> temp 2
0 --> PS <15:14>                 !force kernel mode

M[V] --> PC                      !fetch PC from vector, data space
M[V+2] --> PS                    !fetch PS from vector, data space
temp1<15:14> --> PS<13:12>       !set previous mode
SP-2 --> SP                      !selected by new PS
temp1 --> M[SP]                  !push old PS on stack, data space
SP-2 --> SP
temp2 --> M[SP]                  !push old PC on stack, data space
                                 !go execute next instruction
```

NOTE
If an abort occurs during either the vector fetch or the stack push, the PS and PC are restored to their original state before trap sequence execution.

5.9.1 Priority Order for Traps and Interrupts

The priority order for traps and interrupts is:

1. Red stack trap
2. Address error
3. Memory management violation
4. Timeout/nonexistent memory
5. Parity error
6. Trace (T-bit) trap
7. Yellow stack trap
8. Power fail
9. Floating-point trap
10. PIRQ 7
11. Interrupt level 7
12. Event (LTC) line time clock

13. PIRQ 6
14. Interrupt level 6
15. PIRQ 5
16. Interrupt level 5
17. PIRQ 4
18. SLU 1, receive
19. SLU 2, receive
20. SLU 3, receive
21. SLU 4, receive
22. SLU 5, receive
23. SLU 6, receive
24. SLU 7, receive
25. Console\SLU
26. SLU 1, transmit
27. SLU 2, transmit
28. SLU 3, transmit
29. SLU 4, transmit
30. SLU 5, transmit
31. SLU 6, transmit
32. SLU 7, transmit
33. Console/SLU
34. Interrupt level 4
35. PIRQ 3
36. PIRQ 2
37. PIRQ 1
38. Halt line

5.10 Console Serial Line Unit

The KDJ11-E has eight serial line units. As a factory setting, SLU 8 is configured as the console port, with the address 177560 to 177566/vector 60. Optionally, SLU 8 can follow in ascending order after SLUs 1 - 7 as the eighth SLU or it can be set independently from the other 7 SLUs as the console/SLU. Table 5–18 describes SLU 8.

Table 5–18 Console/SLU Panel - SLU 8

Switch 1 Setting	Function	Address	Vector
Off	Console enabled.	177560	60
On	Console disabled.	176570 (176670)	370 (470)

NOTE
Console SLU (8) has fixed parameters of eight data bits, no parity, and one stop bit. The baud rate is determined by the console/SLU panel switches 6, 7, and 8.

SLU lines 1-7 can be set independently from each other. See Chapter 3, Operation for information on using the Setup Menu.

There are four serial line unit registers: the receiver status register, the receiver data buffer, the transmitter status register, and the transmitter data buffer. These registers are described in the following sections.

5.10.1 Receiver Status Register (1777xxx0)

Figure 5–22 shows the Receiver Status Register (RCSR) format at address 1777xxx0.

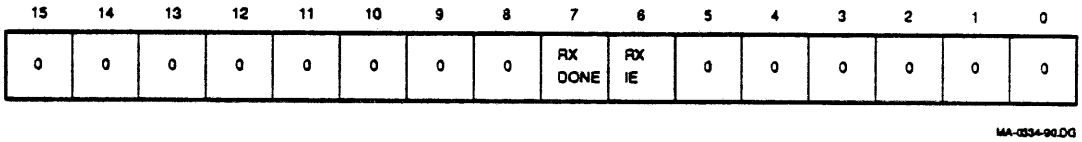


Figure 5–22 Receiver Status Register Format (1777xxx0)

Table 5–19 provides the receiver status register bit descriptions.

Table 5–19 Receiver Status Register Bit Descriptions

Bit(s)	Name	Function
15:08	–	Unused. These bits should always read as 0s.
07	RX DONE (RO)	Receiver Done. This bit is set when an entire character has been received and is ready to be read from the RBUF register. This bit is automatically cleared when RBUF is read. It is also cleared by power-up.
06	RX IE (R/W)	Receiver Interrupt Enable. This bit is cleared by power-up and bus initialization. If both RCVR DONE and RCVR INT ENB are set, a program interrupt is requested.
05:00	–	Unused. Read as 0s.

5.10.2 Receiver Data Buffer (1777xxx2)

Figure 5–23 shows the receiver data buffer register (RBUF) format at address 1777xxx2.

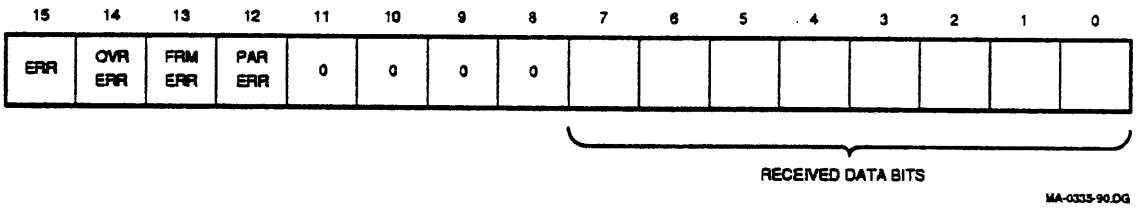


Figure 5–23 Received Data Buffer Register Format (1777xxx2)

Table 5–20 provides the received data buffer register bit descriptions.

Table 5–20 Received Data Buffer Register Bit Descriptions

Bit(s)	Name	Function
15	ERR (RO)	Error. This bit is set if RBUF <14> or <13> is set. ERR is cleared if these two bits are cleared. This bit cannot generate a program interrupt.
14	OVR ERR (RO)	Overrun Error. This bit is set if a previously received character is not read before being overwritten by the present character.
13	FRM ERR (RO)	Framing Error. This bit is set if the present character has no valid stop bit. This bit is used to detect break.

NOTE
Error conditions remain present until the next character is received. At that point, the error bits are updated. The error bits are not necessarily cleared by power-up.

12	Receiver Parity Error	Is set when the parity received does not match the parity expected.
11:08	–	Unused. These bits always read as 0.
07:00	Received Data Bits	These read-only bits contain the last received character.

5.10.3 Transmitter Status Register (1777xxx4)

Figure 5–24 shows the transmitter status register (XCSR) format at address 1777xxx4.

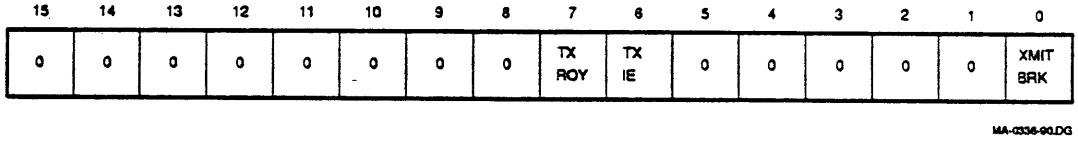


Figure 5–24 Transmitter Status Register Format (1777xxx4)

Table 5–21 provides the transmitter status register bit descriptions.

Table 5–21 Transmitter Status Register Bit Descriptions

Bit(s)	Name	Function
15:08	–	Unused. Read as 0s.
07	TX RDY (RO)	Transmitter Ready. This bit is cleared when XBUF is loaded. The bit sets when XBUF can receive another character. XMT RDY is set by power-up and by bus initialization.
06	TX IE (R/W)	Transmitter Interrupt Enable. This bit is cleared by power-up and by bus initialization. If both TX RDY and TX IE are set, a program interrupt is requested.
05:01	–	Unused. These bits always read as 0s.
00	XMIT BRK (R/W)	Transmit Break. When this bit is set, the serial output is forced to the space condition. XMIT BRK is cleared by power-up and by bus initialization.

5.10.4 Transmitter Data Buffer Register (1777xxx6)

Figure 5–25 shows the transmitter data buffer register (XBUF) format at address 1777xxx6.

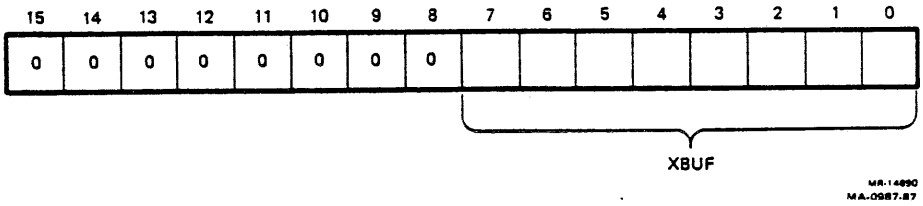


Figure 5–25 Transmitter Data Buffer Register Format (1777xxx6)

Table 5–22 contains the bit descriptions.

Table 5–22 Transmitter Data Buffer Register Bit Descriptions

Bit(s)	Name	Function
15:08	–	Unused. Always read as 0s.
07:00	XBUF (WO)	These eight bits are used to load the transmitted character.

Table 5–23 describes the console/SLU register settings for a data base address set at 176500.

Table 5–23 Console/SLU Register Settings - Data Base Address 176500

SLU	Address	Register	Vector
1	176500	RCSR1	300
	176502	RBUF1	
	176504	XCSR1	304
	176506	XBUF1	
2	176510	RCSR2	310
	176512	RBUF2	
	176514	XCSR2	314
	176516	XBUF2	
3	176520	RCSR3	320
	176522	RBUF3	
	176524	XCSR3	324
	176526	XBUF3	
4	176530	RCSR4	330
	176532	RBUF4	
	176534	XCSR4	334

Table 5–23 (Cont.) Console/SLU Register Settings - Data Base Address 176500

SLU	Address	Register	Vector
	176536	XBUF4	
5	176540	RCSR5	340
	176542	RBUF5	
	176544	XCSR5	344
	176546	XBUF5	
6	176550	RCSR6	350
	176552	RBUF6	
	176554	XCSR6	354
	176556	XBUF6	
7	176560	RCSR7	360
	176562	RBUF7	
	176564	XCSR7	364
	176566	XBUF7	
8	177560	RCSR8	60
	177562	RBUF8	
	177564	XCSR8	64
	177566	XBUF8	

Table 5–24 describes the console/SLU register settings for a data base address set at 176600.

Table 5–24 Console/SLU Register Settings - Data Base Address 176600

SLU	Address	Register	Vector
1	176600	RCSR1	400
	176602	RBUF1	
	176604	XCSR1	404
	176606	XBUF1	
2	176610	RCSR2	410
	176612	RBUF2	
	176614	XCSR2	414
	176616	XBUF2	
3	176620	RCSR3	420
	176622	RBUF3	
	176624	XCSR3	424
	176626	XBUF3	
4	176630	RCSR4	430

Table 5–24 (Cont.) Console/SLU Register Settings - Data Base Address 176600

SLU	Address	Register	Vector
	176632	RBUF4	
	176634	XCSR4	434
	176634	XBUF4	
5	176640	RCSR5	440
	176642	RBUF5	
	176644	XCSR5	444
	176646	XBUF5	
6	176650	RCSR6	450
	176652	RBUF6	
	176654	XCSR6	454
	176656	XBUF6	
7	176660	RCSR7	460
	176662	RBUF7	
	176664	XCSR7	464
	176666	XBUF7	
8	177560	RCSR8	60
	177562	RBUF8	
	177564	XCSR8	64
	177566	XBUF8	

5.10.5 Break Response

The KDJ11-E console serial line unit may be configured either to perform a halt operation or to have no response when a break condition is received. A halt operation will cause the processor to halt and enter the octal debugging technique (ODT) microcode. The halt-on-break option is selected via bit 9 of the boot and diagnostic controller status register. During power-up or restart, the boot and diagnostic ROM program will always set bit <9> to a <1>. This enables the halt-on-break condition if the Keylock switch is in the enable position.

5.11 Kernel/Supervisor/User Mode Descriptions

The PDP-11/94 processor family offers three modes of execution: kernel, supervisor, and user. These modes enhance the memory protection scheme and increase the flexibility and functionality of timesharing and multiprogramming environments.

Kernel mode is the most privileged of the three modes and allows execution of any instruction. In an operating system featuring multiprogramming, the ultimate control of the system is implemented in code that executes in kernel mode. Typically, this includes control of physical I/O operations, job scheduling, and resource management.

Memory management mapping and protection allows these executive elements to be protected from inadvertent or malicious tampering by programs executing in the less privileged processor modes. If the I/O page is only mapped in kernel mode, then only the kernel has access to the memory management registers to re-map or modify the protection. This limited access results because the memory management registers themselves exist in the I/O page.

In order for a user program to have sensitive functions performed in its behalf, a request must be made of the executive program. This request is typically in the form of a software trap that vectors the processor into kernel mode. Thus the executive code remains in control and can verify that the function requested is consistent with the operation of the system as a whole.

The supervisor mode is the next most privileged mode. It may be used to provide for the mapping and execution of programs shareable by users but still requiring protection from them. Supervisor mode might include command interpreters, logical I/O processors, or run-time systems.

User mode is the least privileged mode. It prohibits the execution of instructions such as HALT and RESET, as does supervisor mode. A multiprogramming operating system typically restricts execution of user programs to user mode. This restriction prevents a single user from having a negative effect on the system as a whole. The user's virtual address space is set up such that the only areas of memory that can be written are those that belong to that user. Areas shared among users are protected for read-only, execute-only, or for both read and execute access.

5.12 UNIBUS Mapping

The UNIBUS map is the interface between the UNIBUS and the PMI memory. It responds as a slave to UNIBUS signals and is used to convert 18-bit UNIBUS addresses to 22-bit memory addresses. The 22-bit memory address is accompanied by an additional signal line, BBS7 L. The assertion of BBS7 L disables the PMI address decoding and selects the I/O page.

UNIBUS address space is 256 Kbyte; the top 8 Kbyte addresses of this space always reference the I/O page. The lower 248 Kbyte of UNIBUS address space can be used by the UNIBUS map to reference physical memory (Figure 5–26).

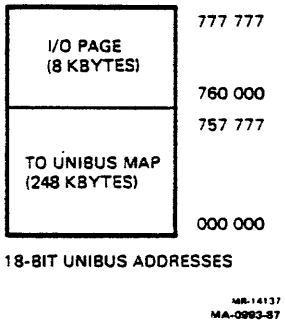


Figure 5–26 UNIBUS Address Space

The UNIBUS map can be programmed, via Memory Management Register 3, (MMR3) bit <05>, to run with relocation enabled or relocation disabled.

If relocation is disabled (MMR3 bit <05> = 0), the UNIBUS map appends four leading zeros (address bits <21:18>) to the UNIBUS address. This produces the 22-bit memory address. Memory address bits <17:00> are identical to UNIBUS address bits <17:00>. If memory address bits <17:13> are all ones, the BBS7 L signal is asserted, selecting the I/O page.

If relocation is enabled (MMR3 bit <05> = 1), the UNIBUS map decodes UNIBUS address bits <17:13> to select one of 31 mapping register pairs (corresponding to octal codes 00 through 36). The content of the selected mapping register pair is added to UNIBUS address bits <12:00> to produce the memory address. If UNIBUS address bits <17:13> are all 1s (octal code 37), the I/O page is selected. The BBS7 L signal to the memory is asserted, memory address bits <17:00> are identical to UNIBUS address bits <17:00> and memory address bits <21:18> are not asserted.

5.12.1 UNIBUS Mapping Registers

The UNIBUS map contains 32 mapping register pairs. Of these pairs, only 31 are actually used for address relocation. Figure 5–27 illustrates the high-address register format.

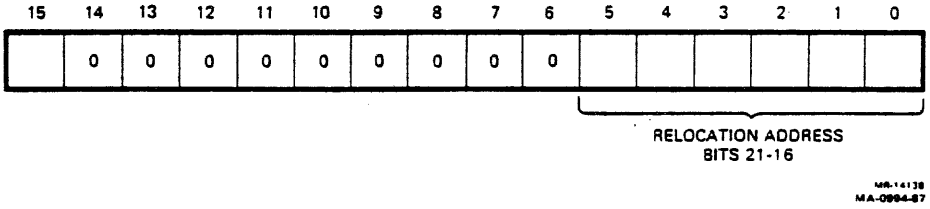


Figure 5–27 High-Address Register Format

Figure 5–28 illustrated the low-address register format.

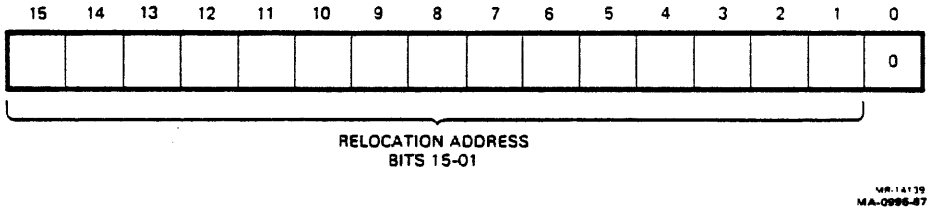


Figure 5–28 Low-Address Register Format

The mapping register pairs can be accessed directly or indirectly as explained in the following list.

1. Direct Access—The mapping registers are accessed individually through their I/O page addresses. Each mapping register pair consists of a high-address register which contains relocation address bits <21:16>, and a low-address register which contains relocation address bits <15:01>.
2. Indirect Access—When UNIBUS map relocation is enabled, UNIBUS address bits <17:13> select the appropriate mapping register pair to be used in relocating the 18-bit UNIBUS address.

Table 5–25 shows the UNIBUS map register pairs.

Table 5–25 UNIBUS Map Register Pairs

Register Pair No.	Low-Register	High-Register	UNIBUS Addresses Mapped Through Register Pair
0	17 770 200	17 770 202	000 000—017 777
1	17 770 204	17 770 206	020 000—037 777
2	17 770 210	17 770 212	040 000—057 777
3	17 770 214	17 770 216	060 000—077 777
4	17 770 220	17 770 222	100 000—117 777
5	17 770 224	17 770 226	120 000—137 777
6	17 770 230	17 770 232	140 000—157 777
7	17 770 234	17 770 236	160 000—177 777
10	17 770 240	17 770 242	200 000—217 777
11	17 770 244	17 770 246	220 000—237 777
12	17 770 250	17 770 252	240 000—257 777
13	17 770 254	17 770 256	260 000—277 777
14	17 770 260	17 770 262	300 000—317 777
15	17 770 264	17 770 266	320 000—337 777
16	17 770 270	17 770 272	340 000—357 777
17	17 770 274	17 770 276	360 000—377 777
20	17 770 300	17 770 302	400 000—417 777
21	17 770 304	17 770 306	420 000—437 777
22	17 770 310	17 770 312	440 000—457 777
23	17 770 314	17 770 316	460 000—477 777
24	17 770 320	17 770 322	500 000—517 777
25	17 770 324	17 770 326	520 000—537 777
26	17 770 330	17 770 332	540 000—557 777
27	17 770 334	17 770 336	560 000—577 777
30	17 770 340	17 770 342	600 000—617 777
31	17 770 344	17 770 346	620 000—637 777
32	17 770 350	17 770 352	640 000—657 777
33	17 770 354	17 770 356	660 000—677 777
34	17 770 360	17 770 362	700 000—717 777
35	17 770 364	17 770 366	720 000—737 777
36	17 770 370	17 770 372	740 000—757 777

Table 5–25 (Cont.) UNIBUS Map Register Pairs

Register Pair No.	Low-Register	High-Register	UNIBUS Addresses Mapped Through Register Pair
37*	17 770 374	17 770 376	I/O Page (No Relocation)

* Can be read or written into, but not used for mapping.

5.12.2 Memory Configuration Register (17777734)

The KTJ11-B memory configuration register (KMCR), at address 17777734, allows the KDJ11-E boot and diagnostic programs to configure the KTJ11-B for the distribution of UNIBUS and main memory within the system. Additional KMCR bits provide information on the system reboot status and select 18-Bit Mode. Figure 5–29 shows the register format.

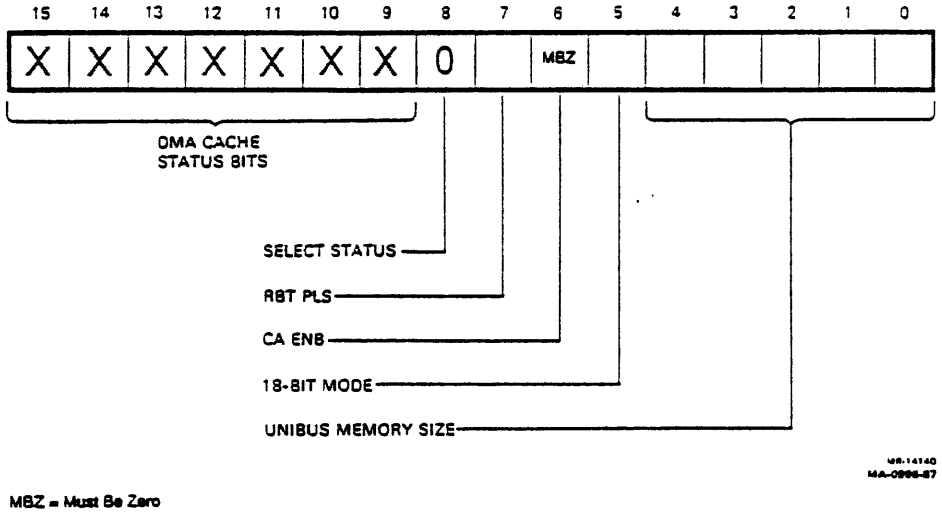


Figure 5–29 Memory Configuration Register (KMCR)

Table 5–26 provides the memory configuration register bit descriptions.

Table 5–26 Memory Configuration Register Bit Descriptions

Bit(s)	Name	Function
15:09	Unused	May be read as ones or zeros.
08	Unused	This bit should be zero.
07	Reboot Pulse (RBT PLS) (RO)	This bit is set by the front panel reboot pulse which also generates a KTJ11-B power-down/power-up cycle. RBT PLS is not cleared by the assertion of DC LO during the KTJ11-B power-down/power-up cycle initiated by the front panel reboot pulse; but it is cleared by any other DC LO assertion.

Table 5–26 (Cont.) Memory Configuration Register Bit Descriptions

Bit(s)	Name	Function
06	Cache Enable (CA ENB) (R/W)	MUST BE ZERO. This bit, when set, enables the DMA cache on the UBA. This feature is not supported on the 11/94. Setting this bit to a one will cause data corruption. **CAUTION** **If bit 6 of the KMCR is set to a one, data corruption will result.**
05	18-Bit Mode (R/W)	When this bit is set, the CPU can access UNIBUS memory only when address bits <21:18> = 00. When this bit is clear, UNIBUS memory can be accessed if address bits <21:18> = 17. This bit is cleared by the assertion of DC LO. Write access to this bit is disabled when DCSR <08> (diagnostic mode) is clear.
04:00	UNIBUS Memory Size	If the system contains main memory only (no UNIBUS memory), these five bits, as well as KMCR <05>, must be cleared. If the system contains UNIBUS memory only (no main memory), then KMCR <05:00> must be set. If the system contains both main memory and UNIBUS memory, KMCR <04:00> indicate the number of 8 Kbyte address segments assigned to UNIBUS memory. UNIBUS memory is assigned downward, starting with the segment below the I/O page. These bits are cleared by assertion of DC LO. Write access to these bits is disabled when DCSR <08> (diagnostic mode) is clear. UNIBUS memory address space is not supported on the KDJ11-E.

5.13 KTJ11-B Diagnostic and Configuration Registers

The KTJ11-B diagnostic and configuration registers are used with diagnostic programs to check the KTJ11-B in diagnostic mode with the UNIBUS disabled.

When operating in diagnostic mode, the KTJ11-B can be programmed to perform diagnostic NPR cycles. These cycles test the KTJ11-B address and data paths along with the UNIBUS map.

5.13.1 Diagnostic Controller Status Register (17777730)

Diagnostic programs use the diagnostic controller status register (DCSR) at address 17777730 to enter and exit from diagnostic mode, to select the source of the Diagnostic Data Register (DDR), and to perform diagnostic NPR cycles that test the UNIBUS map along with the KTJ11-B address and data paths. Figure 5–30 shows the register format.

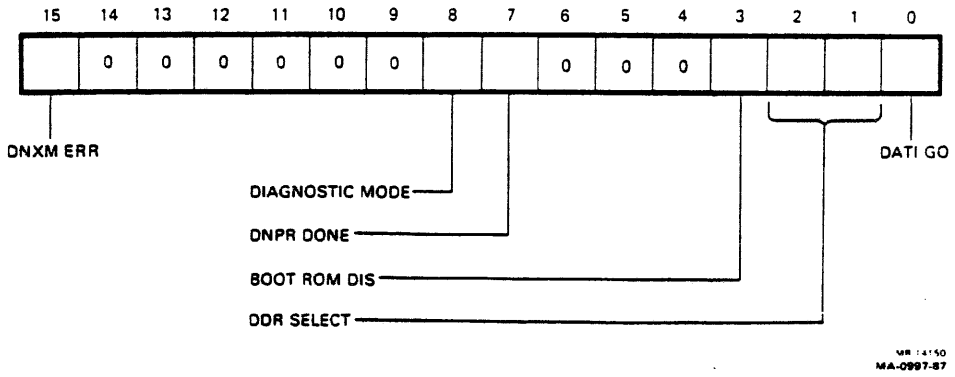


Figure 5–30 Diagnostic Controller Status Register Format (17777730)

Table 5–27 provides the diagnostic controller status register bit descriptions.

Table 5–27 Diagnostic Controller Status Register Bit Descriptions

Bit(s)	Name	Function
15	DNXM ERR	Diagnostic nonexistent memory error register. This bit is cleared at the start of a diagnostic NPR cycle and set if there is a nonexistent memory timeout during that cycle. DNXM ERR is also cleared when DCSR <08> (diagnostic mode) is cleared.
14:09	–	Unused. These bits always read as 0.
08	Diagnostic Mode (R/W)	When this bit is set, the UNIBUS is disabled and the KTJ11-B is configured for diagnostic mode. When this bit is clear, the UNIBUS is enabled and the KTJ11-B is configured for normal operation. This bit is set by the assertion of DC LO.
07	DNPR Done	This bit is set when there are no diagnostic NPR cycles pending. DNPR Done is cleared by a write to DCSR with a 1 in bit <00>, and by any write to the DDR. DNPR Done is set by bus initialization or by completion of a diagnostic NPR cycle.
06:04	–	Unused. These bits always read as 0.
03	Boot ROM Disable (R/W)	When this bit is set, response of the UBA boot ROM at addresses 177773000–177773776 is disabled, allowing operation of any external ROM which uses those addresses on the UNIBUS. When this bit is cleared, the UBA boot ROM responds to those addresses. This bit is cleared by the assertion of DC LO.
02:01	DDR Select (R/W)	These two bits select the contents of the diagnostic data register during read operations. The DDR select bits are cleared by bus initialization.

Table 5–27 (Cont.) Diagnostic Controller Status Register Bit Descriptions

Bit(s)	Name	Function
00	DATI GO (WO)	Writing a 1 into this bit sets up a diagnostic data-in NPR cycle and clears DCSR bit <07>. The NPR cycle is actually initiated by the next CPU read cycle which accesses the PMI. That cycle provides the address used in the NPR cycle. The data fetched during that cycle is loaded into the DDR.

5.13.2 Diagnostic Data Register (17777732)

Diagnostic programs use the diagnostic data register at address 17777732, along with the diagnostic controller status register (DCSR). The programs perform diagnostic NPR cycles and monitor the state of various UNIBUS data, address, and control signals.

Diagnostic NPR cycles test the UNIBUS map and many of the KTJ11-B address and data paths. During diagnostic NPR cycles, DCSR <02:01> are set equal to 0, thus selecting the diagnostic NPR register. Following a diagnostic data-in NPR cycle, the diagnostic NPR register contains the transferred data. The data can then be read through the DDR. Diagnostic programs set up a diagnostic data-out NPR cycle by writing the data to be transferred into the DDR. Figure 5–31 shows the register format.

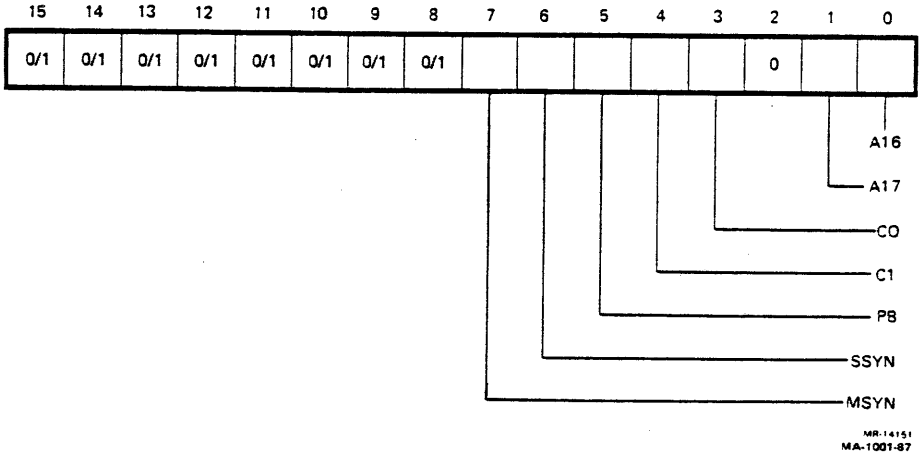


Figure 5–31 Diagnostic Data Register Format (17777732)

All writes to the DDR access the diagnostic NPR register. The information accessed during read operations from the DDR depends on DCSR <02:01>.

NOTE
Contents of the DDR when select code = 11

Table 5–28 provides the diagnostic data register content descriptions.

Table 5–28 Diagnostic Data Register Content Descriptions

Bit 02	Bit 01	Content of Diagnostic Data Register
0	0	Diagnostic NPR register
0	1	UNIBUS data lines D15–00
1	0	UNIBUS address lines A15–00[1]
1	1	UNIBUS address lines A17–A16 and various UNIBUS control lines

[1]Asserted address line A16 during the diagnostic UNIBUS address lines read operation may cause a parity error abort.

5.13.3 Diagnostic DATI NPR Cycles

The execution procedure for diagnostic DATI cycles is as follows:

1. The KTJ11-B must be running in diagnostic mode with DDR select bits (DCSR <02:01>) = 0.
2. The diagnostic program writes a 1 into DCSR bit <00>.
3. The diagnostic program writes the test data pattern into the target memory location. The KTJ11-B latches address bits <A17:00> of this cycle.
4. The KTJ11-B then executes its diagnostic DATI NPR cycle, storing the fetched data in the diagnostic data register. The address used in this cycle is produced by the UNIBUS map, using the latched 18-bit address. The 18-bit address may be used directly (UNIBUS map relocation disabled) or it may be relocated to produce a 22-bit address (UNIBUS map enabled).
5. The diagnostic program verifies that the diagnostic data register contains the correct data.

5.13.4 Diagnostic DATO NPR Cycles

The execution procedure for diagnostic DATO NPR cycles is as follows.

1. The KTJ11-B must be running in diagnostic mode.
2. The diagnostic program loads the data for the NPR cycle into the diagnostic data register. Loading this register primes the KTJ11-B for a diagnostic NPR cycle.

   NOTE
   At this point, any UNIBUS memory read access or non-PMI I/O page read or write access results in a bus timeout.

3. The KTJ11-B latches address bits <A17:00> from the next KDJ11-E external write to memory address space.
4. The KTJ11-B then executes its diagnostic DATO NPR cycle, using the data stored in the diagnostic data register. The address used in this cycle is produced by the UNIBUS map, using the latched 18-bit address.
5. The diagnostic program verifies that the target memory location contains the correct data. If it wants to check the diagnostic data register, it must do so before performing an external write operation which would alter the contents of that register.

6
Diagnostics and Troubleshooting

6.1 Introduction

This chapter contains information on troubleshooting, interpreting diagnostic error messages, and using system troubleshooting aids.

6.2 Troubleshooting Guidelines

The following are guidelines to follow when troubleshooting the system.

- Verify that the DC ON light on the front panel is on. When on, this light indicates that all voltages are within specified levels.
- Be sure that the fans are operating.

  NOTE
  If the fans are not operating, the system automatically turns off.
- The corrective maintenance strategy is field replaceable unit (FRU) replacement (Chapter 7).
- Verify the symptoms reported before removing any components.
- The troubleshooting information in this guide assumes that only one FRU has failed.
- Check the system cables for loose connections and any damaged cables or wires. Replace them if necessary.
- Symptoms displayed on the console terminal or LEDs can indicate multiple failures; therefore, the symptoms may change as FRUs are replaced. Always troubleshoot the current symptoms.
- If you are reconfiguring the system for troubleshooting purposes, make sure that minimum loads on +5.0 V and –15 Vdc are maintained using the MLM module.
- If an error occurs during Self-test, refer to Table 6–3.

6.3 Diagnostic Programs

PDP-11/94-E systems support three types of diagnostic programs.

Table 6–1 Diagnostic Programs

Diagnostic Program	Function	
DECX11	DECX11 is a system level exerciser. DECX11 tests all parts of the PDP-11/94 subsystem. The following DECX11 modules should be configured for a basic system:	
	MON E	Monitor E supports the memory management unit and mapping.
	KWA	Line time clock.
	CPA	KDJ11-E instruction set.
	CPB	KDJ11-E extended instruction set.
	FPB	Floating point unit.
	DLA	Serial line units.
Device level diagnostics (XXDP+)	Provides tests that check individual options and localize hardware failures to the function level.	
Read-only memory (ROM) resident diagnostics	CPU ROM resident startup diagnostics test various functions specific to the CPU and UBA modules.	

A comprehensive set of diagnostics can be executed during a system power-up by selecting the Power-On Self-Test on the Set-Up Menu. A failure during diagnostic execution halts the testing and displays one of the following:

- If tests 30-67 fail, an error code and an error message on the console terminal (if connected).
- A test number on the front panel status display and SLU panel status display (Figure 6–1).

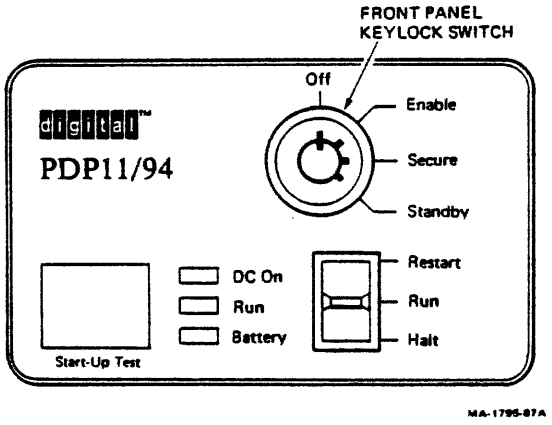


Figure 6–1 PDP-11/94-E Front Panel

- A test number in the KDJ11-E CPU module diagnostic LEDs

Normally, the system displays the same error information in all three locations. If the console terminal is not working, refer to the status display. If neither location is working, refer to Section 6.4.2.

6.3.1 KDJ11-E Self-Test

The KDJ11-E Self-Test allows you to comprehensively test:

- CPU
- Memory management
- On-board memory
- Serial line units
- Console/SLU bulkhead
- UNIBUS signals
- KTJ11-B

The Self-test Menu allows you to select and execute tests individually or as a group using either video terminal mode or hard copy terminal mode.

- To select and execute Self-tests using the video terminal mode, proceed to Section 6.3.1.1.
- To select and execute Self-tests using the hard copy terminal mode, proceed to Section 6.3.1.2.

Chapter 3 provides additional information on operating in video terminal mode and hard copy terminal mode.

6.3.1.1 Video Terminal Mode

NOTE

Test 30, All Selected Tests, runs all tests selected (parameter = Yes) as a group.

Test 32, Loopback SLU Test, requires loopback connectors installed on all SLUs on the console/SLU panel.

Selecting or Deselecting Tests Executed Upon Power-Up

To select or deselect tests that are executed upon power-up:

1. Move the cursor to the test to be changed.
2. Press Return to select Yes or No.
3. Press Tab to select the Monitor field.
4. Press Return to return to the Setup Menu.
5. Press Tab to select the Save field.
6. Press Return to save the Self-test parameters.

Selecting and Executing Individual Tests

To select and execute an individual test:

1. Move the cursor to the Test field.
2. Type in the test number of the test to be run.
3. Move the cursor to the Repeat field.
4. Type in the number of iterations to run the test or 0 to run continuously.
5. Move the cursor to Do.
6. Press Return to execute testing.

NOTE

Ctrl C terminates testing. To return to the Setup Menu, move the cursor to the Monitor field and press Return.

Selecting and Executing a Group of Tests

To select and execute a group of tests using Test 30:

1. Move the cursor to each test to be changed.
2. Press Return to select Yes or No.
3. Move the cursor to the Test field.
4. Enter *30* to select Test 30, All Selected Tests.
5. Move the cursor to the Repeat field.
6. Type in the number of iterations to run the tests or 0 to run continuously.
7. Move the cursor to Do.
8. Press Return to execute testing.

NOTE

Ctrl C terminates testing. To return to the Setup Menu, move the cursor to the Monitor field and press Return.

An example of the Self-test Menu follows:

```
KDJ11-E Monitor  Version 1.06 18-May-1990
(C) Digital Equipment Corporation 1990

67 CPU Test                          Yes  44 Lines Config. Test          Yes
66 MMU Test                          Yes  43 Serial Lines Test           Yes
65 Pre-Console Test                  Yes  40 Memory parity Test          Yes
64 MSER Test                         Yes  37 UBA map reg Test            Yes
63 CCR r/w Test                      Yes  36 UBA NPR cycles Test         Yes
62 HIT/MISS-Reg Test                 Yes
61 LTC Speed Test                    Yes
60 Add-Stat-Reg Test                 Yes  32 Loopback SLU Test           No
57 CPU-Err-Reg Test                  Yes  31 Extended Memory Test        No
55 UBA reg. resp. Test               Yes
54 Address 0 Test                    Yes
53 Pre-Memory (0-4KW) Test           Yes
52 FPA Register Test                 Yes
51 FPA Function Test                 Yes
50 Int Mem Address Test              Yes
47 Int Mem Data Test                 Yes
46 PIRQ-Reg Test                     Yes
45 LTC Int Test                      Yes  30 All Selected Tests          No

Monitor    Do              Test 00   Repeat 00000                       Do
```

Example 6–1 Self-test Menu

6.3.1.2 Hard Copy Terminal Mode

Selecting and Executing Individual Tests

To select and execute an individual test:

1. Enter **D** on the Main Menu,.
2. Press Return to execute the Diagnostic Command.
3. The Self-test Menu displays (See Example 6–2).

```
KDJ11-E Monitor  Version 1.06  15-Feb-1990
Licensed to Digital Equipment Corporation
❶
67 CPU Test
66 MMU Test
65 Pre-console Test
64 MSER Test
63 CCR r/w Test
62 HIT/MISS-Reg Test
61 LTC Speed Test
60 Add-Stat-Reg Test
57 CPU-Err-Reg Test
55 UBA Reg. Resp. Test
54 Address 0 Test
53 Pre-Memory (0-4KW) Test
52 FPA Register Test
51 FPA Function Test
50 Int Mem Address Test
47 Int Mem Data Test
46 PIRQ-Reg Test
45 LTC Int Test
44 Lines Config. Test
43 Serial Lines Test
40 Memory parity Test
37 UBA Map Reg Test
36 UBA NPR Cycle Test
32 Loopback SLU Test ❷
30 All Selected Tests

Test number = 67❸   New =❹

Repeat counter = 000000 ❺   New =❻
```

Example 6–2 Self-test Menu

❶ List of tests that can be selected.

❷ **32 Loopback SLU Test** requires that turnarounds are installed on the SLU's (1-7).

❸ **Test number** lists the currently selected test.

❹ **New** allows you to change the currently selected test by entering a new test number.

❺ **Repeat counter** lists the currently selected number of times to repeat a test.

❻ **New** allows you to change the currently selected number of times to repeat a test by entering a new number.

4. Enter the number of the new test to be run.
5. Enter the number of the times the new test is to be repeated. Enter **0** if you want the test to run continuously.
6. Press Return to start the testing.

   During the testing, the test number, description of the test, error count and repeat number are displayed and printed. If continuous testing is selected, no information will be printed except for errors to allow the Diagnostic Command to run for an extended period of time.
7. Ctrl C or Ctrl P stops the testing.

Selecting and Executing a Group of Tests

To select and execute a group of tests:

1. Type **S** on the command line on the Main Menu.
2. Press Return to execute the Setup command.
3. The Setup Menu displays (Example 6–3).

```
KDJ11-E Monitor Version 1.06 30-Mar-1990
(C) Digital Equipment Corporation 1990

Setup Mode Commands

1 Exit
2 Select configuration parameters
3 Select diagnostic configuration
4 Select serial line parameters
5 Select boot parameters
6 List available boot programs
7 Factory setting
8 Save the setup table in the EEPROM
9 Load EEPROM data into the setup table
10 Load EEPROM boot program into memory
11 Edit or create EEPROM boot program
12 Save a boot program in the EEPROM
13 Delete a saved EEPROM boot program
14      Enter ROM ODT
Commands are: [1, 2, 3, 4, 5, 6, 7,8 ,9 10, 11, 12, 13}
type a command then press the RETURN key:
```

Example 6–3 Setup Menu

4. Type 3 on the command line of the Setup Menu.
5. Press Return to execute the Setup Mode Command 3. The following list displays:

```
KDJ11-E Monitor Version 1.06 30-Mar-1990
(C) Digital Equipment Corporation 1990
A Nr. 67 CPU Test                       (0) = No   (1) = Yes   = 1
B Nr. 66 MMU Test                       (0) = No   (1) = Yes   = 1
C Nr. 65 Pre-Console Test               (0) = No   (1) = Yes   = 1
D Nr. 64 MSER Test                      (0) = No   (1) = Yes   = 1
E Nr. 63 CCR r/w Test                   (0) = No   (1) = Yes   = 1
F Nr. 62 HIT/MISS-Reg Test              (0) = No   (1) = Yes   = 1
G Nr. 61 LTC Speed Test                 (0) = No   (1) = Yes   = 1
H Nr. 60 Add-Stat_Reg Test              (0) = No   (1) = Yes   = 1
I Nr. 57 CPU-Err-Reg Test               (0) = No   (1) = Yes   = 1
J Nr. 55 UBA Reg. Resp. Test            (0) = No   (1) = Yes   = 1
K Nr. 54 Address 0 Test                 (0) = No   (1) = Yes   = 1
L Nr. 53 Pre-Memory (0-4KW) Test        (0) = No   (1) = Yes   = 1
M Nr. 52 FPA Register Test              (0) = No   (1) = Yes   = 1
N Nr. 51 FPA Function Test              (0) = No   (1) = Yes   = 1
O Nr. 50 Int Mem Address Test           (0) = No   (1) = Yes   = 1
P Nr. 47 Int Mem Data Test              (0) = No   (1) = Yes   = 1
Q Nr. 46 PIRQ-Reg Test                  (0) = No   (1) = Yes   = 1
R Nr. 45 LTC Int Test                   (0) = No   (1) = Yes   = 1
S Nr. 44 Lines Config. Test             (0) = No   (1) = Yes   = 1
T Nr. 43 Serial Lines Test              (0) = No   (1) = Yes   = 1
U Nr. 40 Memory parity Test             (0) = No   (1) = Yes   = 1
V Nr. 37 UBA Map Reg Test               (0) = No   (1) = Yes   = 1
W Nr. 36 UBA NPR Cycle Test             (0) = No   (1) = Yes   = 1
X Nr. 32 Loopback SLU Test              (0) = No   (1) = Yes   = 1
Y Nr. 31 Extended Memory Test           (0) = No   (1) = Yes   = 1
Z Nr. 30 All Selected Tests             (0) = No   (1) = Yes   = 1
Type CTRL\Z to exit or press Return key to proceed
```

Example 6–4 Selecting Individual Tests

6. To deselect a test, enter **0** at the appropriate test number.
7. To select a test, enter **1** at the appropriate test number.
8. Press Return to return to the Main Menu.
9. Enter **D** on the Main Menu to select and execute the Diagnostic Command.
10. The Self-test Menu displays (See Example 6–2).
11. Enter **30** as the number of the new test to be run. Test 30 runs the group of tests previously selected in Setup Command 3.
12. Enter the number of the times test 30 is to be repeated. Enter **0** if you want test 30 to run continuously.
13. Press Return to start the testing.

    During the testing, the test number, description of the test, error count and repeat number are displayed and printed. If continuous testing is selected, no information will be printed except for errors to allow the Diagnostic Command to run for an extended period of time.
14. Ctrl C or Ctrl P stops the testing.

Table 6–2, LED Display Messages and Descriptions describes the test numbers, status display numbers, and boot error numbers, that can display on the front panel LED during testing.

Table 6–3 provides recommendations to correct any errors that can occur during testing.

Table 6–2 LED Display Messages and Descriptions

Number	Function	Description
77	Test	CPU or halt switch. When the CPU is powered up or restarted, the DCOK signal causes the display to be set to 77. If the CPU hangs with the display set to 77, either the halt switch is on or the CPU does not have enough logic functioning to execute an instruction out of the ROM.
76	Test	CPU and MMU (CPU module failure). Sets the LED display to 76 to indicate the first instruction has been executed without hanging up the processor. Enters standalone mode, sets PSW to priority 7 and turns off the MMU. Clears the PCR and sets up SP. Jumps to the high page of the ROM if it is not already there (173xxx). Executes a few simple CPU tests, General Register writes and reads, branch instructions, and a simple JSR instruction.
75	Test	CPU ROM checksum and Page Control Register (17777522). Uses the high byte PCR area (17773000-17773776) as the program area to checksum the ROM. The low byte of the PCR enables the ROM pages into address area 17765000-17765776. The PCR is validated each time it is loaded by checking the next to last location in each page and verifying that each byte contains the selected page number. Uses the low byte PCR area (17765000-17765776) as the program area to read each of the pages into the high byte PCR area at 17773000-17773776 and to verify that the page number is in each byte of the next to last word in each page.
74	Test	Turn MMU on. Run MMU and CPU tests. Tests all PAR's using a floating 0 and 1 pattern. Checks all PDR read/write bits (14:8 and 3:1) using a floating 0 and 1 pattern. To verify address uniqueness, writes par address into par register.

Table 6–2 (Cont.) LED Display Messages and Descriptions

Number	Function	Description
73	Test	Checks UBA reboot bit. Tests the state of Bit 7 of the Memory Configuration Register. Determines if the ROM code is started by the CPU being powered up or restarted by using the RESTART switch on the front panel. Bit 7 = 1 System is being started by the RESTART switch on the front panel. Bit 7 = 0 System is being powered up.
72	Test	Verifies EEPROM checksum. If a checksum error is found, enters dialog mode to do a factory setting.
71	Status Display	This is not a test. It is the display that indicates that the selected Power-up/Restart mode is ODT. If the operator proceeds from ODT without changing any registers, the ROM code continued to run selected tests and enters dialog mode when testing is complete.
70	Status display.	This is not a test. System start mode TRAP24. If the selected startup/restart mode is 24/26, check the status of the Ignore Battery status parameter in the EEPROM. **Ignore Battery parameter = NO.** If the Battery Backup Reboot Enable Bit in the Control Status Register (17777520 bit 15) is cleared, the battery backup maintains voltages during a power fail. Transfers control to the address specified in memory location 24 and sets the PSW with the contents of location 26. If BBRE is set, Battery Backup fails to maintain memory voltages. Go to Dialog Mode. **Ignore Battery parameter = Yes.** Unconditionally transfers control to the address specified in memory location 24 and sets the PSW with the contents of location 26.
67	Test	Miscellaneous CPU (M8981) test.
66	Test	MMU Modes and Aborts. Tests the Memory Management Unit in Kernel, Supervisor, and User mode. All three modes are read and write with byte/word access. Tests Memory Management violation and error bits. Tests that the protection bits in the PDRs will cause aborts when the conditions are violated. Verifies that abort occurs through virtual address 250. Verifies that MMR1 properly records changes in the general purpose registers affected by the abort.
65	Test	Pre-console. Tests the Transmitter Ready Bit. To prevent unwanted characters from printing on the screen, the SLU test transmits characters which are non printing.
64	Test	Tests the Memory System Error Register (17777744).
63	Test	CCR read/write timeout. Rotates the pattern through the Cache Control Register.
62	Test	Hit/Miss Register. Tests force miss condition.
61	Test	Tests the Line Time Clock and the on-board 50HZ, 60HZ and 800HZ clock source. An internal software loop is used to verify clock speeds. The Interrupt logic is not tested here.

Table 6–2 (Cont.) LED Display Messages and Descriptions

Number	Function	Description
60	Test	Tests the: • Additional Status Register (17777526). • Functionality of ASR bits 12 and 13, Serial Line Address/vector Selection logic. • Functionality of ASR bits 4 and 5, internal memory address encoding.
57	Test	CPU error conditions (CPU Error Register). Verifies that the error detection logic is functioning. Error conditions are created to test the error detection logic.
56	Reserved.	
55	Test	UBA register response. Tests that the DCSR, KMCR and DDR respond properly on the UBA. Tests the KMCR with a data pattern. Enables the UBA diagnostic mode and reads the following UNIBUS lines: • UNIBUS Address Lines 17:00 • UNIBUS Data Lines 15:00 • UNIBUS Control Lines; C0, C1, PB, SSYN, MSYN
54	Test	Verifies that memory exists at location 0. Rotates pattern through memory location 0. Tests read modify write with bus lock.
53	Test	Memory locations 0 to 4KW. Can be looped on with the dialog mode test command. Fully checks out the first four KW of memory before the main memory tests are loaded and run. This test: • Enables Parity Trapping. • Writes 1010101010101010 pattern onto memory 0-4KW. • Complements the data pattern. • Reads and compares verify data. • Verifies address uniqueness. • Writes the physical address as data into memory 0-4KW and verify data.
52	Test	FPA register. Selects Double Precision Mode. Rotates a bit through AC0-AC5.
51	Test	FPA function. 1. Clears AC0-AC5 and memory space. 2. Sets double precision mode. 3. Tests the following instructions: LDFPS, STFPS, SETD, CLRD, STD, LDD, LDFPS, LDCID, ADDD, DIVD, MULD, SUBD, STCDI, and CFCC.

Table 6–2 (Cont.) LED Display Messages and Descriptions

Number	Function	Description
50	Test	Internal memory address. Writes segment addresses into memory in ascending order. Compares segment addresses in descending order.
47	Test	Intern memory data. Parity is enabled for this test. This test: • Verifies all memory with data patterns. • Writes a pattern in ascending order into memory. • Compares all data in descending order. • Complements all data in ascending order. • Compares complemented data in descending order. If a memory error occurs, the following information displays: • The memory address. • Expected pattern. • Pattern read.
46	Test	PIRQ Interrupt Level (M8981). Waits for an unexpected interrupt while decrement PSW to level 0.
45	Test	LTC interrupt. Tests the ability of the clock to interrupt to location 100 and at the correct BR Level. On an interrupt, once the clock is in sync, checks that bit 7 (LCM) is cleared.
44	Test	SLU Configuration. Checks transmitter ready bit and looks for correct configuration of all Serial Line Units.
43	Test	SLU Function. Tests the receiver and transmitter interrupt ability of all the Serial Line Units. Shows received characters with corresponding port number if turnaround connectors installed.
42	Test	Reserved.
41	Test	Reserved.
40	Test	The Memory Parity Error bit is tested by creating parity errors. Memory is tested in 4KW segments.
37	Test	Tests all 32 UNIBUS map register pairs with a rotating one's and zero's pattern and an address uniqueness pattern. All 32 register pairs are tested.

Table 6–2 (Cont.) LED Display Messages and Descriptions

Number	Function	Description
36	Test	UBA NRP read/write cycles. Tests that the UNIBUS can write and read all zero's and ones. 1. Disables mapping. 2. Executes a floating 1's and 0's test through a floating address pattern using diagnostic data in and out cycles for 124 K words of memory (if present). 3. Enables mapping. 4. Executes a floating 1's and 0's test through a floating address pattern using diagnostic data in and out cycles for up to 2044 K words of memory (if present). Floats a one and zero across both inputs to the UBA address adder.
35	Reserved.	
34	Reserved.	
33	Reserved.	
32	Test	Serial Line Unit test. Assumes that all SLUs have turnaround connectors installed. Transmits and receives an ASCII test pattern. All Serial Line Unit error detection logic is tested.
31	Test	Extended memory test. Same as test number 47 but more intensive. Parity is enabled.
30	Test	Runs All Selected Tests. Any tests that are selected are executed as a whole.
27	Reserved.	
26	Reserved.	
25		Reserved for MDM. This is not used by the ROM code. This code is driven by the MDM module on UNIBUS systems. Applicable to "A" series only.
24	Reserved.	
23	Reserved.	
22	Reserved.	
21	Boot Error	Drive error occurred while attempting to boot drive.
20	Boot Error	Controller error. The UNIBUS controller for the device the customer is attempting to boot is displaying an error code in its CSR. Make sure that the NPG jumper was removed if the device is a direct memory access (DMA) controller. Consult the device's technical manual for more information.
17	Boot Error	The mnemonic typed in for the boot device is either incorrect or the boot ROM for that device is not installed. Enter dialog mode and "List" the valid devices.
16	Boot Error	Invalid unit number selection. The unit number after the mnemonic is not within acceptable range for that device. See that device's technical manual for help.
15	Boot Error	Nonexistent drive. The drive number the user is trying to boot from is not on the PDP-11/94-E.

Table 6–2 (Cont.) LED Display Messages and Descriptions

Number	Function	Description
14	Boot Error	Nonexistent controller. The controller for the device the user is trying to boot from is not on the UNIBUS or is addressed incorrectly.
13	Boot Error	No tape is installed in the drive. Install a tape.
12	Boot Error	No media in drive or the drive LOAD button is not in.
11	Boot Error	The bootstrap data from the device does not conform to the boot block specifications. Make sure that media is bootable. Change setup mode to accept nonstandard boot blocks.
10	Boot Error	No media present in the drive or the disk drive has not completed its spinup function.
7	Boot Error	No bootable device found in automatic boot mode.
6	Reserved.	
5	Reserved.	
4	Status Display	Indicates that you have entered the Setup Menu.
3	Status Display	UBA ROM boot in progress. May take a few seconds.
2	Status Display	EEPROM boot in progress. May take a few seconds.
1	Status Display	CPU ROM boot in progress. May take up to five minutes for some devices.
00	Status Display	Indicates a successful boot. Control is transferred from the ROM code to the booted device. The display blanks when it receives a code of 00.

Table 6–3 Error Messages

LED Display	Probable Cause	Recommended Action
77	1. Halt Switch in halt position. 2. CPU module failure. 3. UNIBUS failure.	1. Check run/halt switch. 2. Replace the CPU module. 3. Replace UBA, verify devices on UNIBUS.
76	CPU module failure.	Replace the CPU module.
75	CPU module failure.	Replace the CPU module.
74	CPU module failure.	Replace the CPU module.
73	1. UBA module failure. 2. CPU module failure.	1. Replace the UBA. 2. Replace the CPU module.
72	CPU module failure.	Replace the CPU module.
70	1. UBA failure. 2. CPU module failure.	1. Replace the UBA. 2. Replace the CPU module.
67	CPU module failure.	Replace the CPU module.
66	CPU module failure.	Replace the CPU module.
65	CPU module failure.	Replace the CPU module.
64	CPU module failure.	Replace the CPU module.

Table 6–3 (Cont.) Error Messages

LED Display	Probable Cause	Recommended Action
63	CPU module failure.	Replace the CPU module.
62	CPU module failure.	Replace the CPU module.
61	Line Time Clock failure.	Replace the CPU module.
57	CPU module failure.	Replace the CPU module.
55	1. UBA failure. 2. CPU module failure.	1. Replace the UBA. 2. Replace the CPU module.
54	CPU module failure.	Replace the CPU module.
53	CPU module failure.	Replace the CPU module.
52	CPU module failure.	Replace the CPU module.
51	CPU module failure.	Replace the CPU module.
50	CPU module failure.	Replace the CPU module.
47	CPU module failure.	Replace the CPU module.
46	CPU module failure.	Replace the CPU module.
45	CPU module failure.	Replace the CPU module.
44	CPU module failure.	Replace the CPU module.
43	1. CPU module failure. 2. SLU panel failure. 3. Cables from SLU to CPU.	1. Replace CPU module. 2. Replace SLU panel. 3. Check cables from SLU to CPU.
40	CPU module failure.	Replace the CPU module.
37	UBA failure.	Replace the UBA.
36	UBA failure.	Replace the UBA.
32	1. CPU module failure. 2. Turnarounds. 3. Cables from SLU to CPU.	1. Replace CPU module. 2. Check turnarounds. 3. Check cables from SLU to CPU.
31	CPU module failure.	Replace CPU module.
25	1. PDP11X94-A: Blower assembly. 2. PDP11/94-A: Fan assembly.	1. PDP11X94-A: Replace blower assembly. 2. PDP11/94-A: replace fan assembly.
21	Boot error indicating that the media you are trying to to boot from is not bootable.	Reboot from another media.
20	Boot error.	Make sure that the NPG jumper was removed if the device is a direct memory access (DMA) controller. Consult the device's technical manual for more information.
17	Boot error indicating that the mnemonic typed in for the boot device is either incorrect or the boot ROM for that device is not installed.	Enter dialog mode and "List" the valid devices.

Table 6–3 (Cont.) Error Messages

LED Display	Probable Cause	Recommended Action
16	Boot error indicating an invalid unit number selection.	The unit number after the mnemonic is not within acceptable range for that device. See that device's technical manual for help.
15	Boot error indicating a nonexistent drive.	The drive number you are trying to boot from is not on the PDP-11/94-E. Enter a drive number that is on the PDP-11/94-E.
14	Boot error indicating a nonexistent controller.	The controller for the device you are trying to boot from is not on the UNIBUS or is addressed incorrectly.
13	Boot error indicating that no tape is installed in the drive.	Install a tape.
12	Boot error indicating that no media in drive or the drive LOAD button is not in.	Boot from a drive in which media is installed. Push the drive LOAD button in.
11	Boot error indicating that the bootstrap data from the device does not conform to the boot block specifications.	Make sure that media is bootable. Change setup mode to accept nonstandard boot blocks.
10	Boot error indicating no media is present in the drive or the disk drive has not completed its spinup function.	Boot from a drive in which media is installed. Wait until the disk drive has completed its spinup function.
7	Boot error indicating no bootable device is found in automatic boot mode.	Check devices in Auto boot list.

CAUTION
Do not bypass errors unless all user software has been removed or write protected.

6.4 System Troubleshooting Aids

The system has LED indicators on the front panel, power supply, SLU panel, CPU module, APS module, and MLM module. Use these indicators as troubleshooting aids.

6.4.1 Front Panel

Three LED indicators are on the front panel. Figure 6–1 shows the location of the LEDs. Table 6–4 describes the function of the LEDs.

The two-digit status display provides the test number in progress or the system startup status. The codes are described in Table 6–2.

Table 6–4 Front Panel LED Indicators

LED	Status	Function
Run	On	The J11 processor is fetching and executing instructions. This is the normal condition.
	Off	The processor is halted or waiting for an interrupt. When the processor is in micro ODT, the Run LED blinks for each console keystroke. The Run LED also turns off during extended DMA activity.
DC On	On	DC power is available to the logic, and all voltages are within specified levels.
	Off	DC voltages are not available to the logic, or voltages are present but not within tolerances.
Battery	On	Battery is present and charged to 80% or greater capacity.
	Slow blink	Battery is at less than 80% capacity and is charging.
	Fast blink	The AC power has failed. The battery is discharging, but the memory content remains valid.
	Off	Battery is either fully discharged or not present in the system. Memory content will not be preserved if AC power fails.

6.4.2 KDJ11-E CPU Module

The KDJ11-E module contains:

One green power OK (DCOK) LED	Which indicates DCOK status.
One yellow LED	Which indicates that DC power to the CPU module is present.
Six red LEDs	Which correspond to the status display shown in Figure 6–2

If the CPU module is the suspected problem, before replacing the module:

- Check the TOY battery.
- Ensure that jumpers W1 and W2 are removed (Figure 6–2).

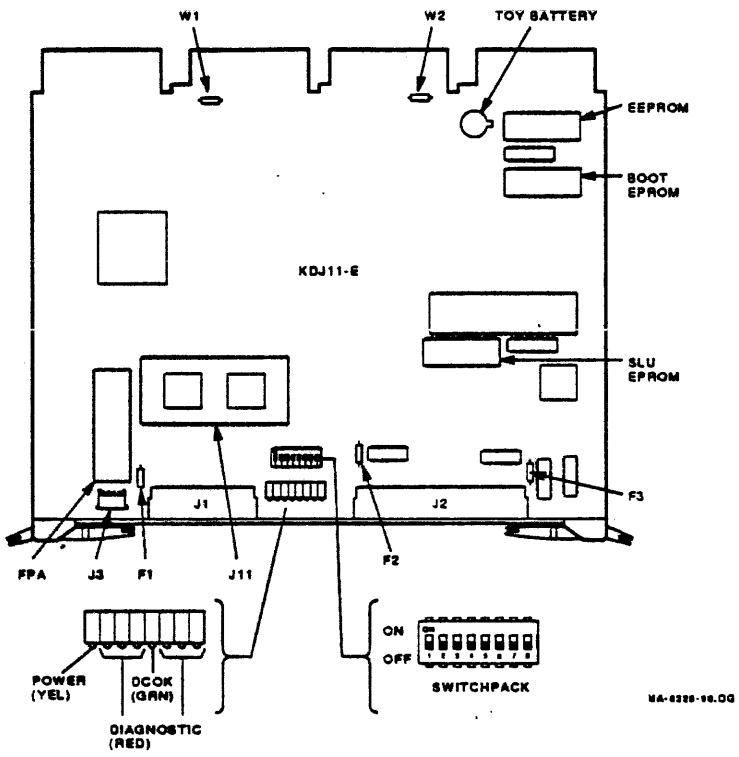


Figure 6–2 KDJ11-E CPU Module Layout

- Ensure that the dual in-line package (DIP) switches are off.
- The 3 1A fuses (F01, F02 and F03). F01 and F02 protect +12 V on the connectors JO1 (pins 30, 40, 50, and 60) and JO2 (pins 10, 20, 30, and 40). F03 protects +5 V on JO2 (pin 1).

Table 6–5 describes some failure symptoms, the probable causes, and corrective actions.

Table 6–5 CPU Troubleshooting

Symptom	Possible Cause	Corrective Action
TOY fails.	Defective battery.	Replace battery.
SLU ports 1-4 fail.	Defective fuse.	Replace F2.
SLU ports 5-8 fail.	Defective fuse.	Replace F1.
LED display on the SLU panel is not lit.	Defective fuse.	Replace F3.
Power LED is not lit.	No +5.1VBB present on the CPU module.	Check the APS cable to CPU module and verify the presence of +5.1VBB.

6.4.3 KTJ11-B UNIBUS Adapter Module

The UNIBUS adapter (UBA) module provides four sockets to support M9312 compatible ROMs. If this module is the suspected problem, check the ROMs and their orientation as shown in Figure 6–3.

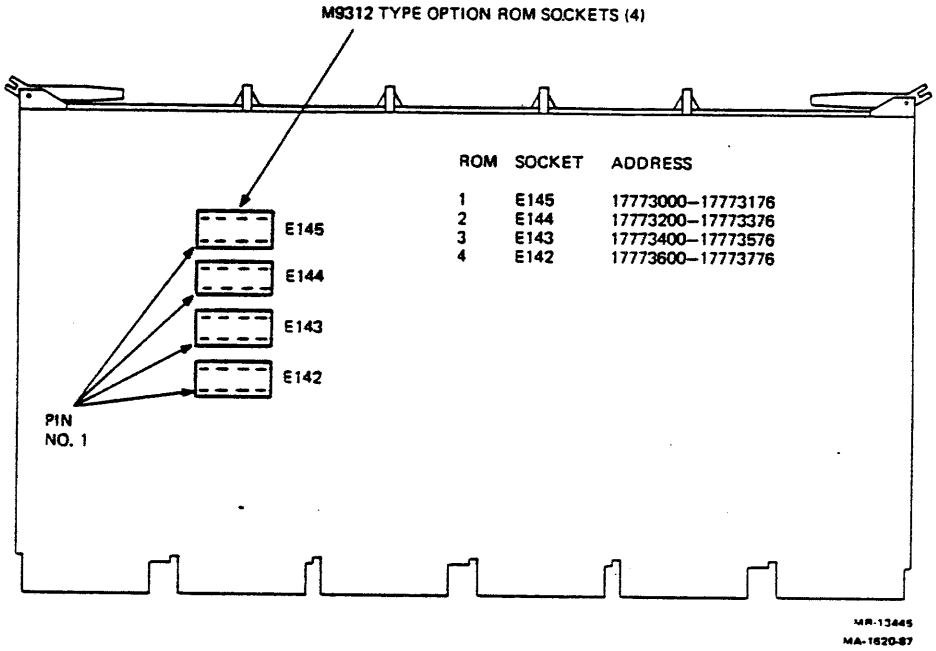


Figure 6–3 KTJ11-B UBA Module Layout

6.4.4 Minimum Load Module

If you are reconfiguring the system for maintenance purposes, be sure minimum current drain requirements are met by using the M9713 MLM module. For more information, refer to Section Section 4.2.1.

6.4.5 APS Module

Ensure that LED D1 is on. This indicates that +5.1VBB is present on the APS module.

If LED D1 is off, check the backplane pin AA2 in slot 2 for the presence of +5.1VBB.

6.4.6 Power Supply

The PDP-11/94-E systems use the H7204-C power supply , which contains three regulator modules. See Figure 6–4. Two of the regulator modules (H7213 and H7217) are FRUs. Be sure that the regulator modules are not defective before replacing a power supply. The H7203 module is not an FRU; therefore, if you find it defective, you must replace the power supply.

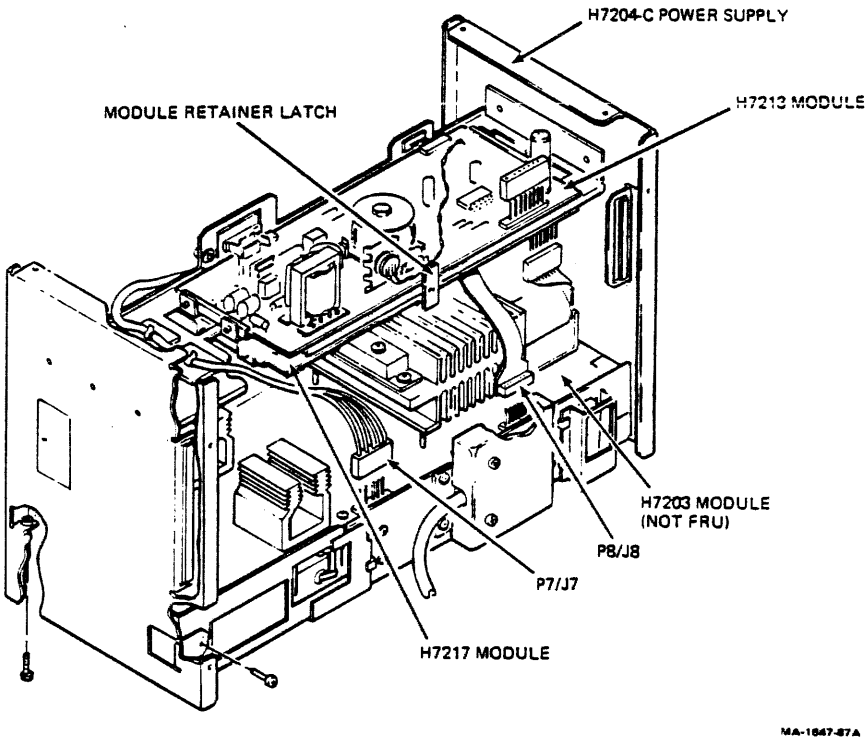


Figure 6–4 Power Supply Modules Location

Troubleshooting for the H7204 power supply consists of:

- Fault diagnosis based on a three-LED status display (Figure 6–5)
- Replacement, in order of increasing difficulty (refer to Chapter 7), of:
  - — One or both of the plug-in voltage regulator modules.
  - — The power distribution board.
  - — The entire power supply.

To diagnose a voltage regulator malfunction in the H7204-C power supply, refer to Figure 6–5 and Table 6–6.

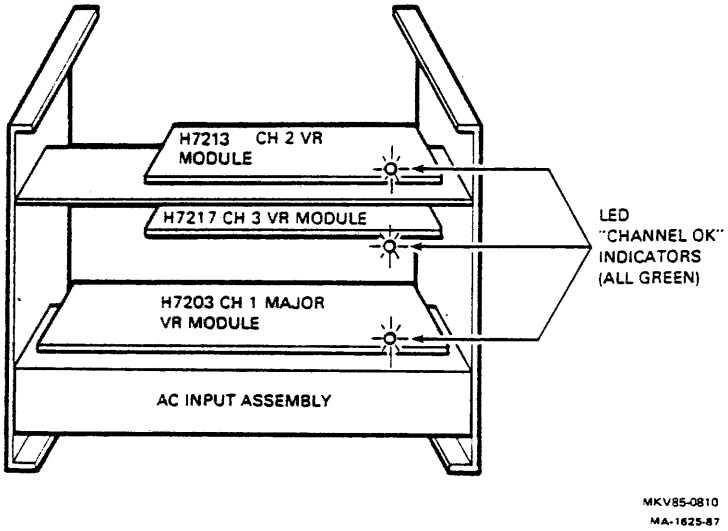


Figure 6–5 H7204-C Power Supply LED Indicators

Table 6–6 H7204-C Power Supply Fault Diagnosis

Symptom/Indication	Corrective Action
All LED indicators unlit	1. Be sure the power supply circuit breaker (CB) is set to on. 2. Be sure the AC power cord is plugged in and power is available (from bench receptacle, cabinet power controller, building power panel, and so forth). 3. Replace the H7204-C power supply (Chapter 7).
CH 1 LED not lit	1. Check for shorts or overloads. 2. Replace the H7204-C power supply.
CH 2 LED not lit	1. Check for shorts or overloads. 2. Replace the H7213 CH 2 VR. 3. Replace the H7204-C power supply.
CH 3 LED not lit	1. Check for shorts or overloads. 2. Replace the H7217 CH 3 VR. 3. Replace the H7204-C power supply.
All three fans not turning, but CH 2 LED is lit	1. Be sure the fan assembly cable is plugged in and not reversed. 2. Check the fans for physical obstruction. 3. Replace the PDB (PN 54-17928-01). 4. Replace the H7204-C power supply.

6.4.7 SLU Panel

To troubleshoot the SLU panel, refer to Table 6–3 and Figure 2–15, Console/SLU Panel Switches.

Before replacing the SLU panel, ensure that all cables are firmly seated in their respective connectors.

7
Removal and Replacement Procedures

7.1 General

This chapter describes how to remove and replace the field replaceable units (FRUs) for the PDP-11/94-E. Table 7–1 lists the FRUs and their part numbers.

Each section describes the removal procedures for that FRU. Unless otherwise specified, you can install a FRU by reversing the steps in the removal procedure.

WARNING
To avoid electric shock when performing maintenance procedures, always shut off the system power and disconnect all power cords from the wall outlets before accessing the system enclosure or any of its components.

Table 7–1 FRU Part Numbers and Descriptions

FRU	Part Number	Section
KDJ11-EA, CPU/2Mbyte memory module	M8981-AA	7.3.1 and 7.3.3
KTJ11-EB, CPU/4Mbyte memory module	M8981-BA	7.3.1 and 7.3.3
Minimum load module	M9713-AA	7.3.1
APS module	M9714-AA	7.3.1 and 7.3.2
Terminator module	M9302	7.3.1
Cable, APS to CPU	17-02783-01	7.3.2
Power supply (120 V)	H7204-CA	7.6
Power supply (240 V)	H7204-CB	7.6
+15 V, −15 V regulator module	H7217	7.6.2.2
+12 V, +5.1 VB regulator module	H7213	7.6.2.1
Power distribution module	54-17928-01	7.6.3
Fans (3)	12-22271-03	7.7
H9277-B CPU backplane	54-17228-01	7.8
4-slot backplane	DD11-CK	7.8
9-slot backplane	DD11-DK	7.8
Front panel assembly	54-16196-01	7.9
Console/SLU panel	70-27974-01	7.10

Table 7–1 (Cont.) FRU Part Numbers and Descriptions

FRU	Part Number	Section
Power controller (120 V)	877-DB	7.10
Power controller (240 V)	877-F	7.10
1A Pico fuse	12-10929-02	7.4
TOY battery	12-34185-01	7.5
Options:		
Battery backup unit (PDP-11X94-E)	H7231-H	Appendix C
Battery backup unit (PDP-11W94-E)	H7231-J	Appendix C

7.2 PDP-11/94-E System Box in System Cabinet

In the PDP-11X94-E and PDP-11W94-E systems, the PDP-11/94-E system box is located in the middle of the system cabinet. A release mechanism (Figure 7–1) allows you to slide the system box out of the cabinet in a horizontal (service) position (Figure 7–2), or raise the system box to a vertical (maintenance) position (Figure 7–3) in the PDP-11X94-E and PDP-11W94-E or a customer-supplied system cabinet. In either position, all field replaceable units listed in Table 7–1 can be replaced by following the steps in this chapter.

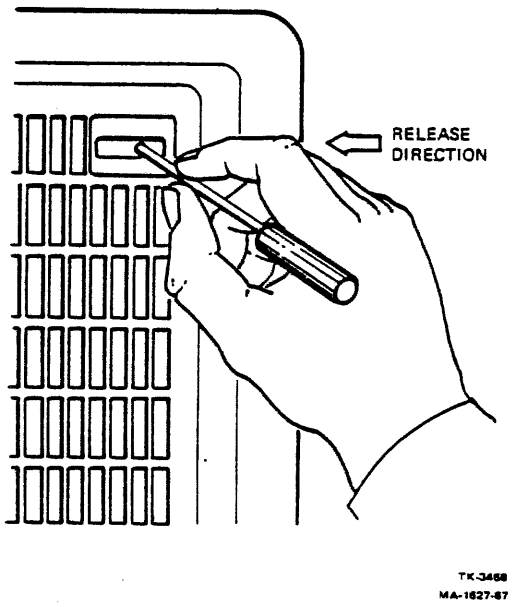


Figure 7–1 System Latch Release Lever

Figure 7–2 shows the extended system box in the service position.

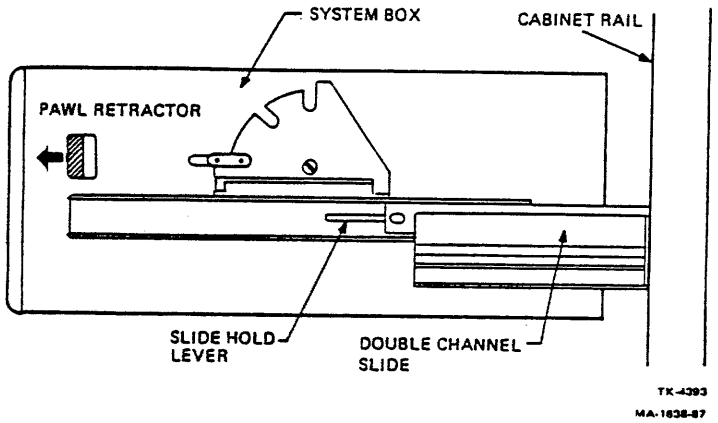


Figure 7–2 Extended System Box in Service Position

Figure 7–3 shows the cabinet-installed PDP-11/94-E in the maintenance position.

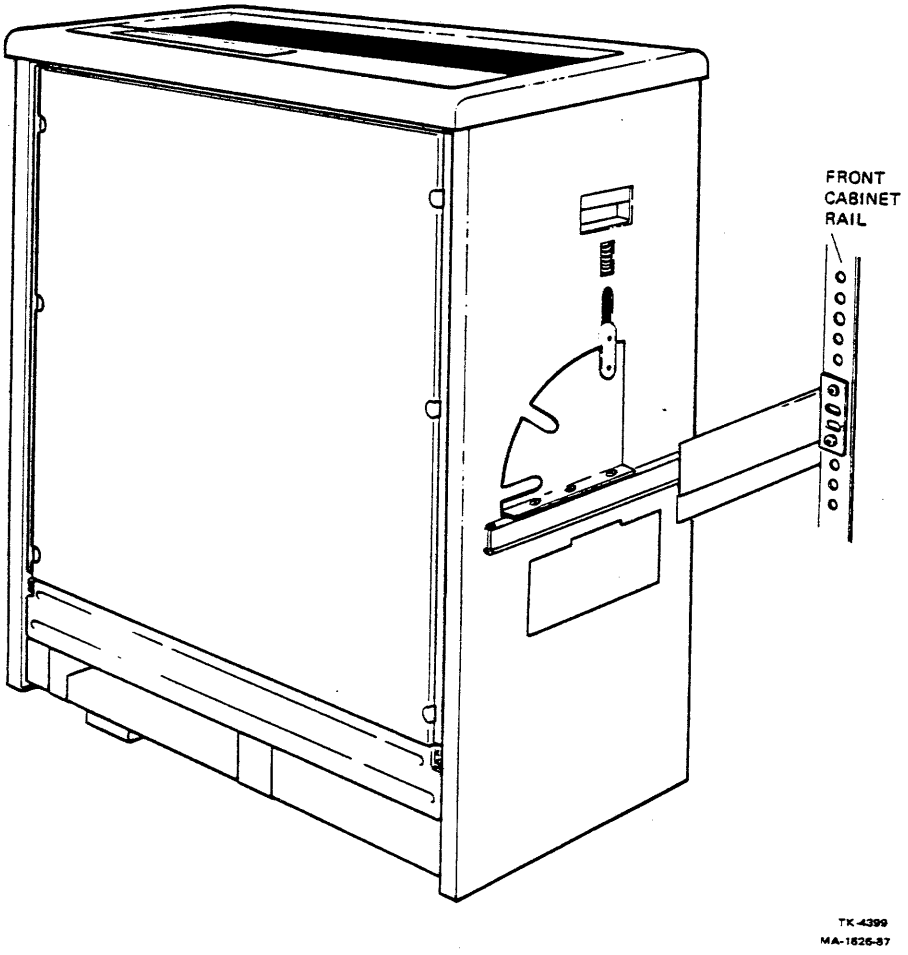


Figure 7–3 Cabinet Installed PDP-11/94-E in Maintenance Position

7.2.1 System Service Position and Maintenance Position

To place the PDP-11/94-E system box in the service position (Figure 7–2) or in the maintenance position (Figure 7–3) in the PDP-11X94-E and PDP-11W94-E system cabinets:

1. Use a 4 millimeter (5/32 inch) hex wrench to release the panel fastener. Remove the rear panel of the cabinet.
2. Shut off the AC power from the power controller by setting the circuit breaker to the down (0) position. Figure 7–4 shows the PDP-11X94-E circuit breaker location.

   WARNING
   To prevent the cabinet from tipping forward, always extend the front stabilizer bar before sliding the system box or an option out of the top portion of the cabinet (Figure 2–10).

3. Release the latch that holds the system box by:
   a. Inserting the blade of a small screwdriver into the hole behind the slot, which is located at the top right side of the front bezel.
   b. Sliding the screwdriver in the direction shown in Figure 7–1.
4. Pull the front of the system box until it is fully extended and the slide hold levers are engaged (Figure 7–2). The system box is now in the service position.
5. Remove and retain the four 6/32 Phillips screws that secure the top cover to the system box.
6. Remove the top cover. In this position, all system modules are accessible.
7. Release the pawl retractor on each side of the system box (Figure 7–2) and tilt the box 90 degrees to the maintenance position (Figure 7–3). In the maintenance position, the power supply and the bottom of the backplane are accessible.

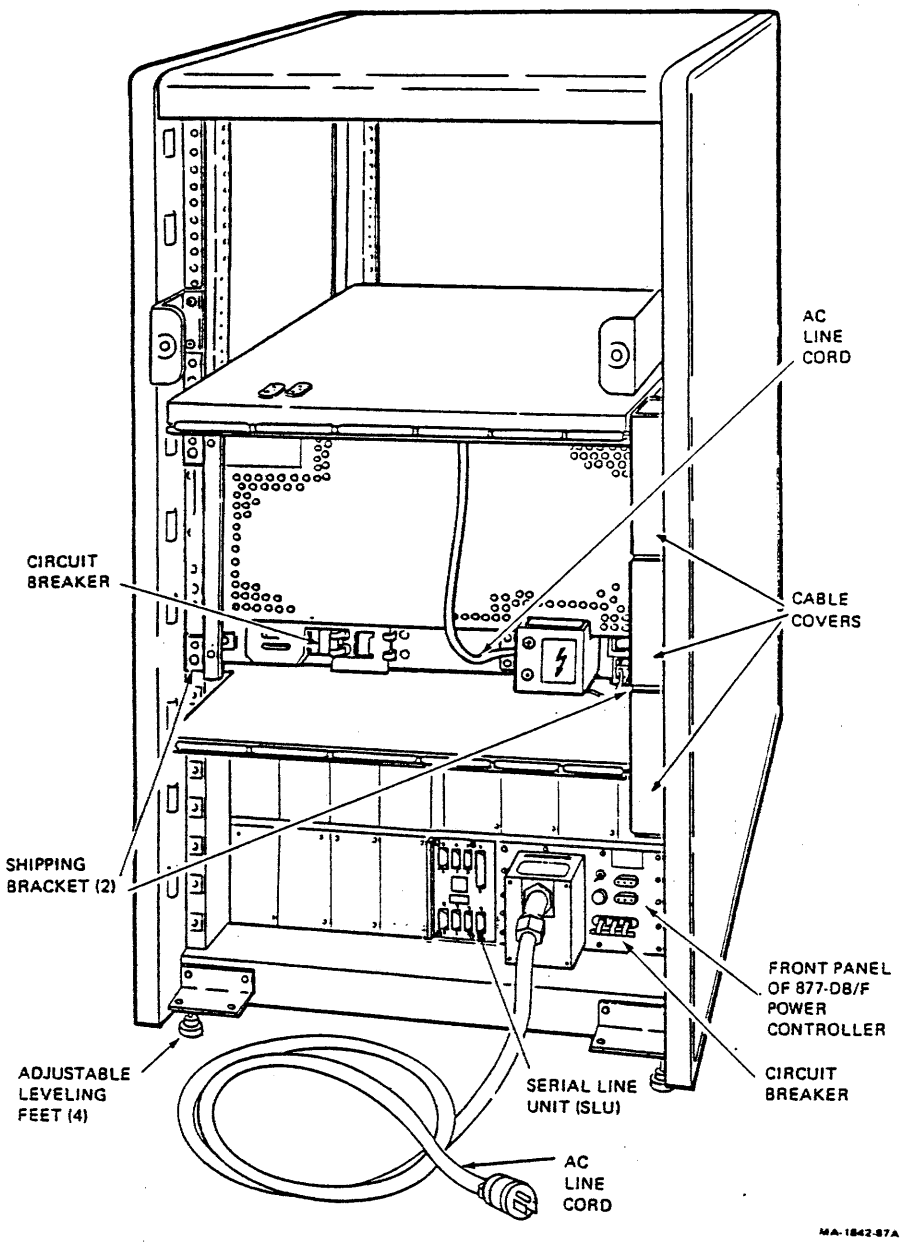


Figure 7–4 PDP-11X94-E Circuit Breaker Location

Figure 7–5 shows the PDP-11W94-E circuit breaker location.

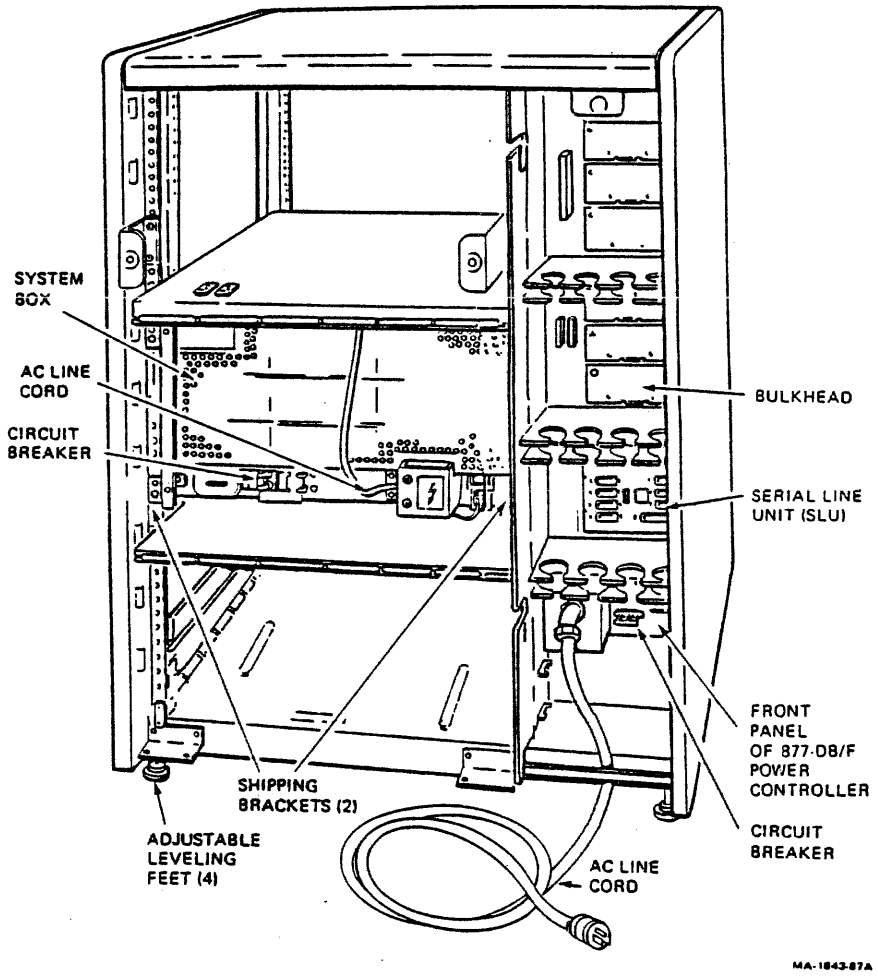


Figure 7–5 PDP-11W94-E Circuit Breaker Location

7.3 Modules

This section describes how to remove the system modules.

CAUTION
Modules are static sensitive. To prevent damage to the modules, you should:

- **Always wear a properly connected ground strap when handling modules.**
- **Place modules on a static mat when you remove them from a backplane or the shipping static bags.**

7.3.1 Remove the Modules

NOTE
It is not necessary to place the system in the maintenance position; extending the system box is sufficient.

To remove any module listed in Table 7–1:

1. Shut off the system power as follows:
   - For cabinet installed systems, set the power supply and power controller circuit breakers to the off position.
   - For systems not installed in cabinets, set the power supply circuit breaker to the off position.
2. Unplug the AC power cord from the outlet.
3. If the system is in a cabinet, slide the system box out of the cabinet in the service position as described in Section 7.2.1.
4. Be sure the ground strap is properly connected.
5. Remove all cables from the module and label each cable.

6. Pull the module handles out and slide the module from the backplane. See Figure 7–6.

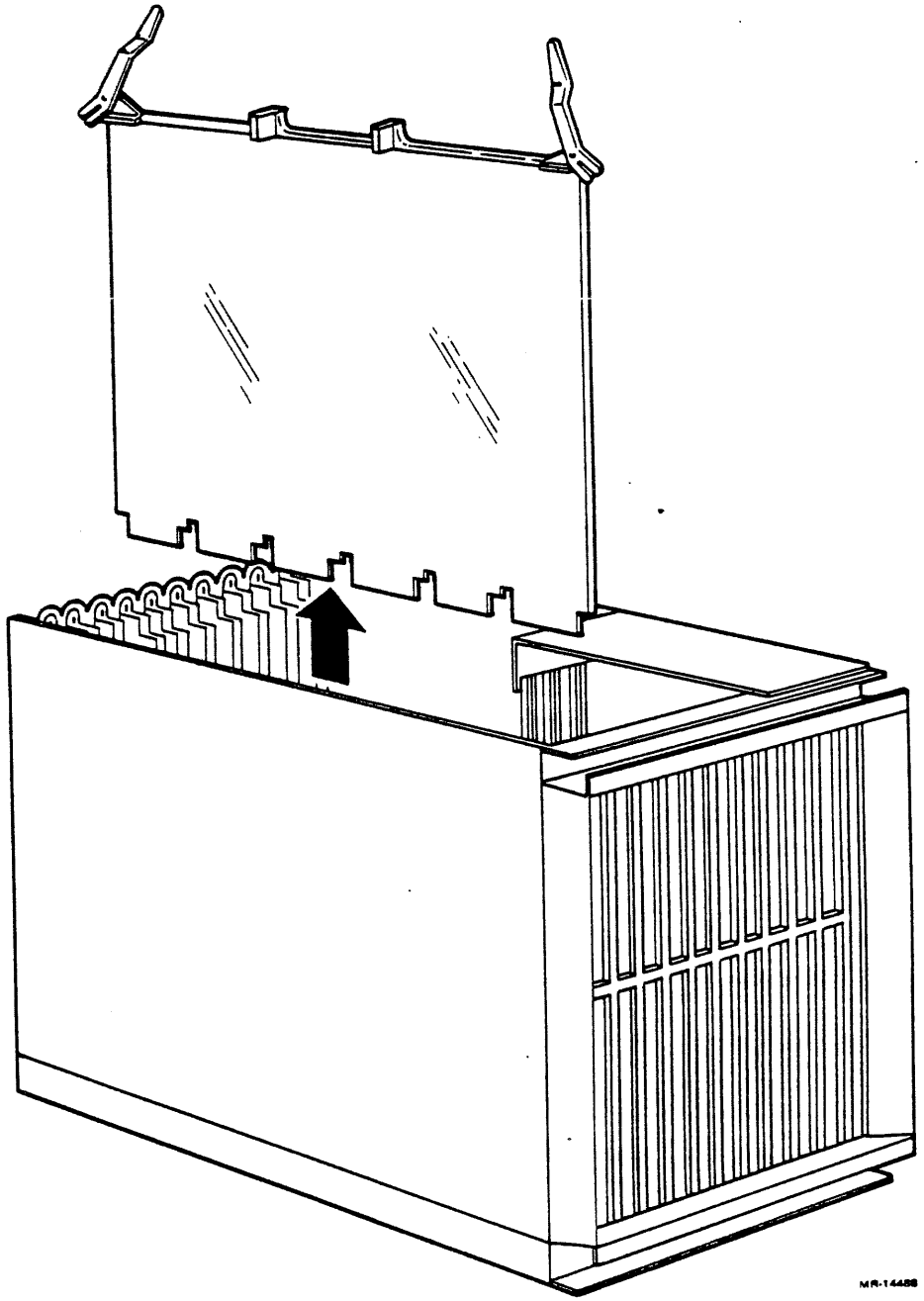


Figure 7–6 Removing Modules

7. Place the module on a static mat which should be on a flat surface.

To reinstall a module, reverse the steps in Section 7.3.1.

NOTE
Ensure the switch and jumper settings on the replacement module are set the same way as the switch and jumper settings on the old module.

7.3.2 APS Module

When you replace the APS module, ensure that the cable to the CPU is connected correctly. See Figure 7–7.

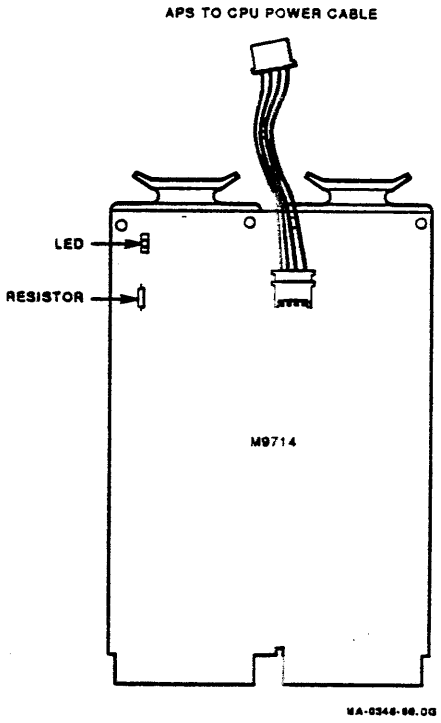


Figure 7–7 APS Module Cable to CPU

7.3.3 CPU Module

When you replace the CPU module, you must confirm the replacement module's setup features and, if necessary, revise the setup features to the original CPU parameters and selections.

During the initial system installation, the setup feature selections should been have been recorded on the worksheet supplied in Appendix A of this guide. Retrieve this form and compare the selections of the original CPU module (as specified on the worksheet) with the factory-set defaults of the replacement module.

NOTE
Dialog and setup mode commands are described in Section 3.4.

To confirm and/or revise the setup features:

1. Remove the CPU module as described in Section 7.3.1.
2. Ensure that the replacement CPU module has W1 and W2 removed and all DIP switch settings are set to off.
3. Install the replacement CPU module.
4. Replace the top cover.

5. Press in the slide hold lever and slide the system box into the cabinet.
6. Ensure that the forced dialog switch on the console SLU panel to the enable position (S5 on).
7. Restore the system power connections and set the circuit breakers to the on position.
8. Power up the system.
9. Execute test 30, all Selected Tests, for five passes. Refer to Section 6.3.1 for instructions.
10. Upon successful completion of Self-tests, return to the Setup Menu.
11. Restore the Setup Parameters recorded on the worksheet.
12. Reset the forced dialog switch (S5) to the original setting.

You have completed the CPU module replacement and setup procedure.

7.4 KDJ11-E 1A Pico fuse

Three 1A pico fuses are located in sockets on the KDJ11-E. To remove the fuses, carefully pull them up and out of their respective sockets. Reverse the procedure to replace them.

7.5 KDJ11-E TOY battery

To remove the TOY battery from the KDJ11-E (Figure 7–8):

1. Use a flat-head screwdriver and carefully press the edge of the TOY battery down.
2. Slide the battery out from under the bracket that holds it in place.

CAUTION
Take care not to bend the battery bracket.

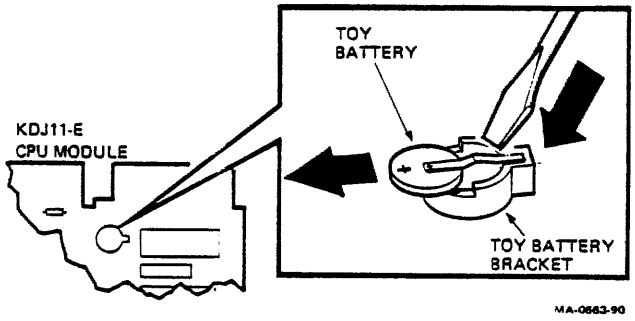


Figure 7–8 TOY Battery Removal

To install the TOY battery on the KDJ11-E (Figure 7–9):

1. Slide the new battery under the bracket and gently press until it is firmly seated in the holder (Figure 7–9).

NOTE
Ensure that the + on the battery faces up.

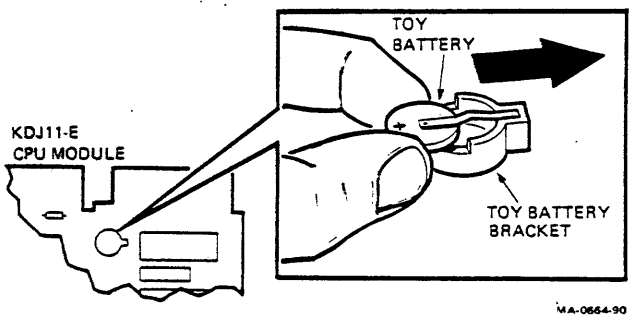


Figure 7–9 TOY Battery Replacement

7.6 Power Supply

The PDP-11/94-E products have an H7204-C power supply that contains three regulator modules: the H7213, H7217, and H7203. The H7213 and H7217 regulator modules are FRUs. If the H7203 regulator module is defective, you must replace the entire H7204-C power supply.

The repair strategy for the H7204-C power supply is compatible with its modular design and consists of the following:

- Fault diagnosis based on a three-LED status display (see Figure 6–5).
- Replacement, in order of increasing difficulty, of the following:
  - One or both of the plug-in voltage regulator modules (H7213 and/or H7217)
  - The power distribution board
  - The entire power supply

Replacing either of the plug-in modules does not require you to remove the power supply from the system box. Replacement can be easily done with the system in the service position (Figure 7–2).

If the fault diagnosis (Figure 6–5 and Table 6–6) leads to a decision to remove and replace the complete H7204-C power supply, this can be easily done by unplugging all power distribution board (PDB) connectors (with the system box in the maintenance position) and removing the six Phillips screws that secure the power supply to the box.

NOTE
If the fans are defective, the power supply shuts off. If the minimum load is insufficient, the power supply runs intermittently.

7.6.1 Fault Diagnosis

Diagnose a voltage-regulator malfunction in the H7204-C power supply by referring to Figure 6–5 and the procedural steps of Table 6–6. Perform the corrective action steps in sequence until all three LED indicators are lit upon reapplication of AC input power to the supply.

7.6.2 Power Supply Modules

The plug-in voltage-regulator modules H7213 and H7217 are field replaceable units.

7.6.2.1 H7213 Voltage Regulator Removal/Replacement

To replace a faulty H7213 voltage regulator:

1. Face the rear of the system box (the front of the power supply).
2. Set the circuit breaker of the AC input assembly to the 0 (off) position.
3. Ensure that you have removed the AC input plug from its AC source receptacle.
4. If a separate battery backup (BBU) power supply is used with the computer system in which the H7204 is being serviced, unplug the 2-wire BBU input jack at P13, located at the right end of the AC input assembly front panel.

   WARNING
   The H7204-C power supply generates hazardous electrical potentials. Treat it with caution when handling.

5. Remove the four 6/32 Phillips screws securing the screen mesh top front cover of the power supply to the H-frame chassis.

6. Lift the cover vertically on its right- and left-edge guides (Figure 7–10).

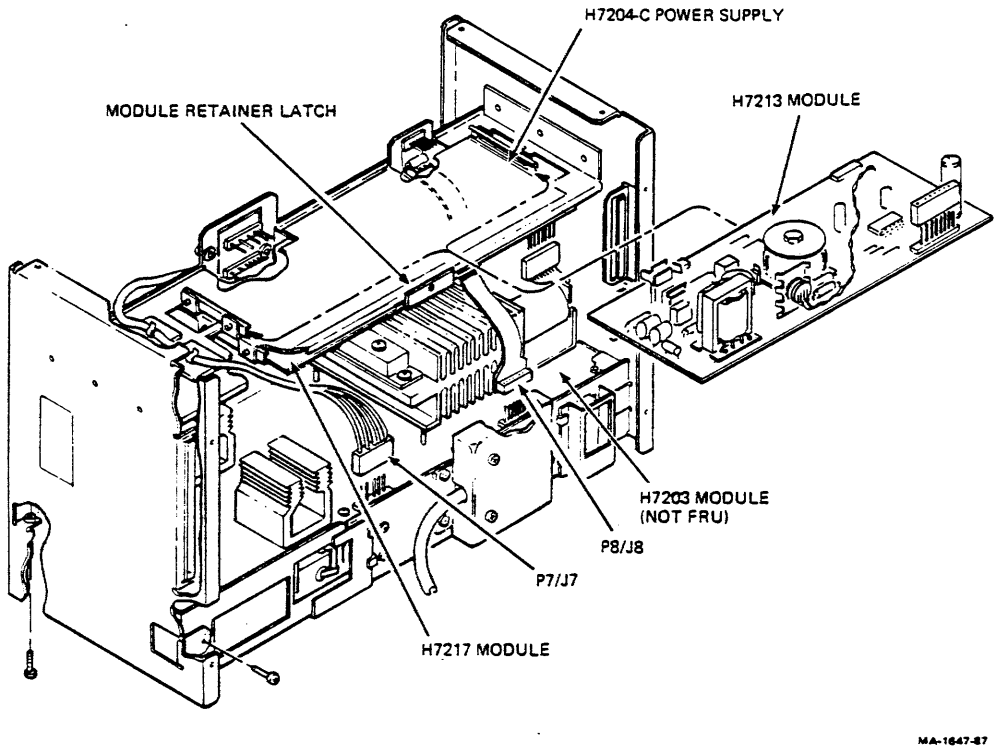


Figure 7–10 Power Supply Module Removal

7. Set the top front cover aside.
8. Unplug the 8-pin connector P7/J7 and the 7-pin connector P8/J8, both at the top front edge of the H7203 major module (Figure 7–10).
9. Unplug the 10-pin connector P3/J3 at the right front edge of the H7213 channel 2 voltage-regulator module (Figure 7–10).
10. Loosen the 6/32 Phillips screw that holds the module retainer latch (Figure 7–10) for the channel 2 module (on the top side) and the H7217 channel 3 module (on the underside) of the chassis H-frame cross member.
11. Rotate the latch 90 degrees (to its horizontal position), and tighten its screw just enough to prevent latch interference with module removal.
12. Withdraw the channel 2 (H7213) module along its plastic guides.

CAUTION
Use both hands to remove the module. Take care not to damage the components.

13. Insert a replacement channel 2 (H7213) voltage regulator module into the guides. Press firmly on the front edge of the module with both thumbs to seat both rear edge connectors.
14. Reconnect connectors P7/J7 and P8/J8 at the front edge of the major module.
15. Reconnect connector P3/J3 at the top front edge of the channel 2 module.
16. Loosen the module retainer latch screw and rotate the latch to its vertical position. Be sure each of the two plug-in modules is seated firmly in its latch slot.
17. Tighten the latch screw snugly to secure the new module, and the H7217 channel 3 module below it, in their installed locations.
18. Replace the top front cover, securing it in place with the four 6/32 Phillips screws you previously removed.
19. Reconnect the battery backup cable (if used) at P13 on the right front of the AC input assembly.
20. Plug the AC input connector of the power supply into its AC source receptacle.
21. Set the circuit breaker to the 1 (on) position.
22. Ensure that the green LED indicator mounted on connector J3 is lit, indicating that module +12.3 Vdc output is within specification.

NOTE
For the location and identification of the LED fault-indicators, see Figure 6–1.

7.6.2.2 H7217 (Channel 3) Voltage Regulator (VR) Module

To replace a faulty channel 3 H7217 VR module:

NOTE
This corrective maintenance procedure can be done without removing the power supply or the major module from the system box.

1. Face the rear of the system box (the front of the power supply).
2. Follow steps 1 through 6 in Section 7.6.2.1.
3. Unplug the 8-pin connector P6/J6 at the right front edge of the H7217 module.
4. Unplug the 7-pin connector P8/J8 at the front edge of the H7203 major module and fold the flexible cable back over the top of the H7213 channel 2 module.
5. Unplug the 8-pin connector P7/J7 at the front edge of the H7203 major module. Move the cable aside so you can remove the faulty H7217 channel 3 module.

6. Loosen the 6/32 Phillips screw securing the module retainer latch (Figure 7–10) for the H7213 channel 2 module (on the top side) and the H7217 channel 3 module (on the underside) of the chassis H-frame cross member.
7. Rotate the latch 90 degrees (to its horizontal position), and tighten the latch screw just enough to prevent latch interference with module removal.
8. Withdraw the plug-in H7217 module along its plastic guides.

CAUTION
Use both hands to remove the module. Take care not to damage the components.

9. Insert a replacement H7217 module into the empty guides. Press firmly on the front edge of the module with both thumbs to seat both rear edge connectors.
10. Reconnect connectors P7/J7 and P8/J8 at the front edge of the H7203 major module.
11. Reconnect connector P6/J6 at the front of the H7217 module (Figure 7–10).
12. Follow steps 15 through 20 in Section 7.6.2.1.
13. Ensure that the green LED indicator at the right front of the H7217 module is lit, indicating that the ±15 Vdc outputs from this module are within specification. LED failure to illuminate was the fault indication leading to module replacement.

NOTE
For the location and identification of the LED fault indicators, see Figure 6–1.

7.6.2.3 H7203 Voltage Regulator

If the fault diagnosis indicates a faulty H7203 voltage regulator module, you must replace the entire power supply (Section 7.6.4).

7.6.3 Power Distribution Board Replacement

To replace a faulty power distribution board (PN 54-17928-01) (PDB):

1. Set the circuit breaker (Figures 7–4 and 7–5) of the AC input assembly to the 0 (off) position.
2. Ensure that the AC power cord has been unplugged from its receptacle.
3. If a separate battery backup (BBU) power supply is used in the computer system in which the H7204 is being serviced, unplug the two-wire BBU input jack at P13, located to the right end of the AC input assembly front panel.
4. Withdraw the box to full extension and rotate it to the maintenance position (Figure 7–3).
5. Remove the cover plate.

6. Unplug all connectors on the power distribution board (Figure 7–11).

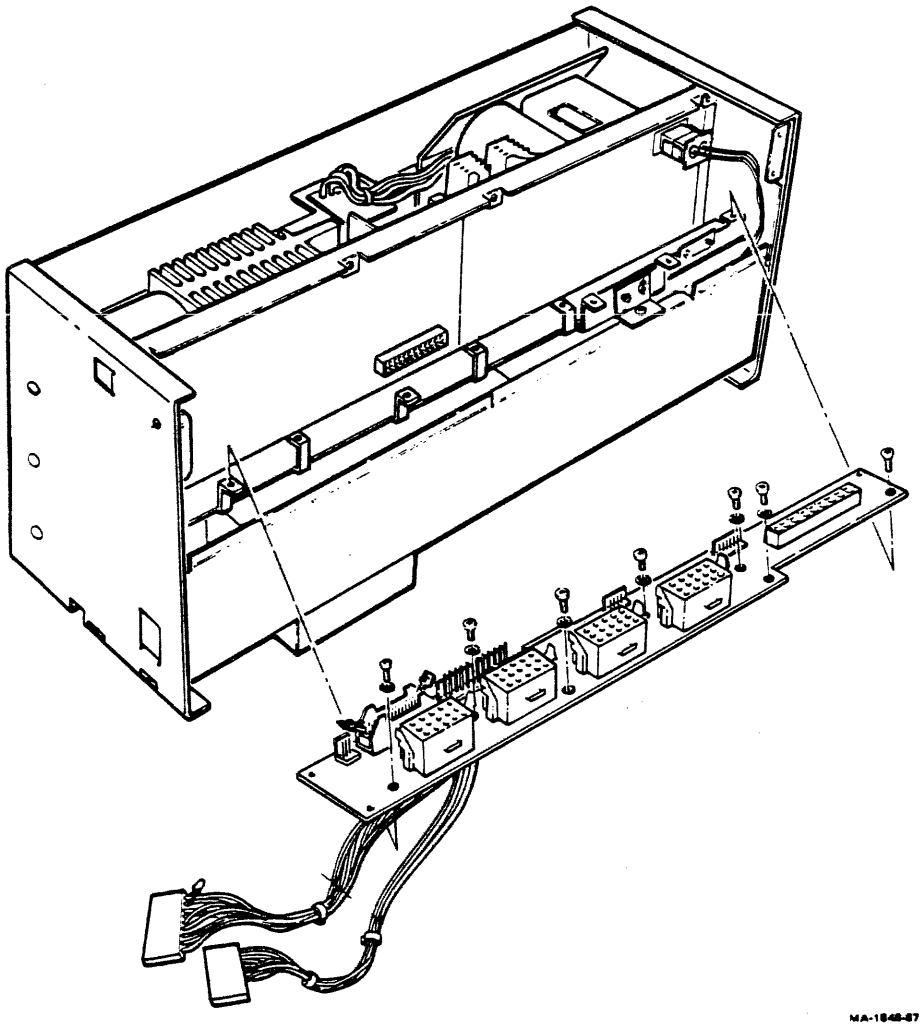


Figure 7–11 Power Distribution Assembly Removal

7. Remove the six 5/16 Phillips screws that secure the power supply H-frame to the system box (Figure 7–12). The sixth screw (not shown in the figure) is located on the other side of the system box.
8. Slide the H-frame power supply assembly free of the system box and set the power supply assembly aside.
9. Remove the seven 8/32 Phillips screws that secure the PDB to the bus bar assembly (Figure 7–11). Remove the power distribution board PDB from the power supply.
10. Reverse the above steps to install the new power distribution board.

NOTE
Ensure that all seven screws in step 9 above are tightened, securing the power distribution board to the bus-bar assembly.

7.6.4 H7204-C Power Supply

To replace the H7204-C power supply:

1. Set the circuit breaker (Figures 7–4 and 7–5) of the AC input assembly to the 0 (off) position.
2. Ensure the AC power cord is removed from its AC receptacle.
3. If a separate battery backup (BBU) power supply is used in the computer system in which the H7204 is being serviced, unplug the two-wire BBU input jack at P13, located to the right end of the AC input assembly front panel.
4. Withdraw the box to its full extension and remove the top cover.
5. Rotate the box to its maintenance position and remove the bottom cover.
6. Remove the PDB access cover, as described in the procedure for replacing the H7217 module (Section 7.6.2.2).
7. Unplug all connectors on the power distribution board (PN 54-17928-01).

8. Remove the six 5/16 Phillips screws that secure the power supply H-frame to the system box (Figure 7–12). The sixth screw (not shown in the figure) is located on the other side of the system box.

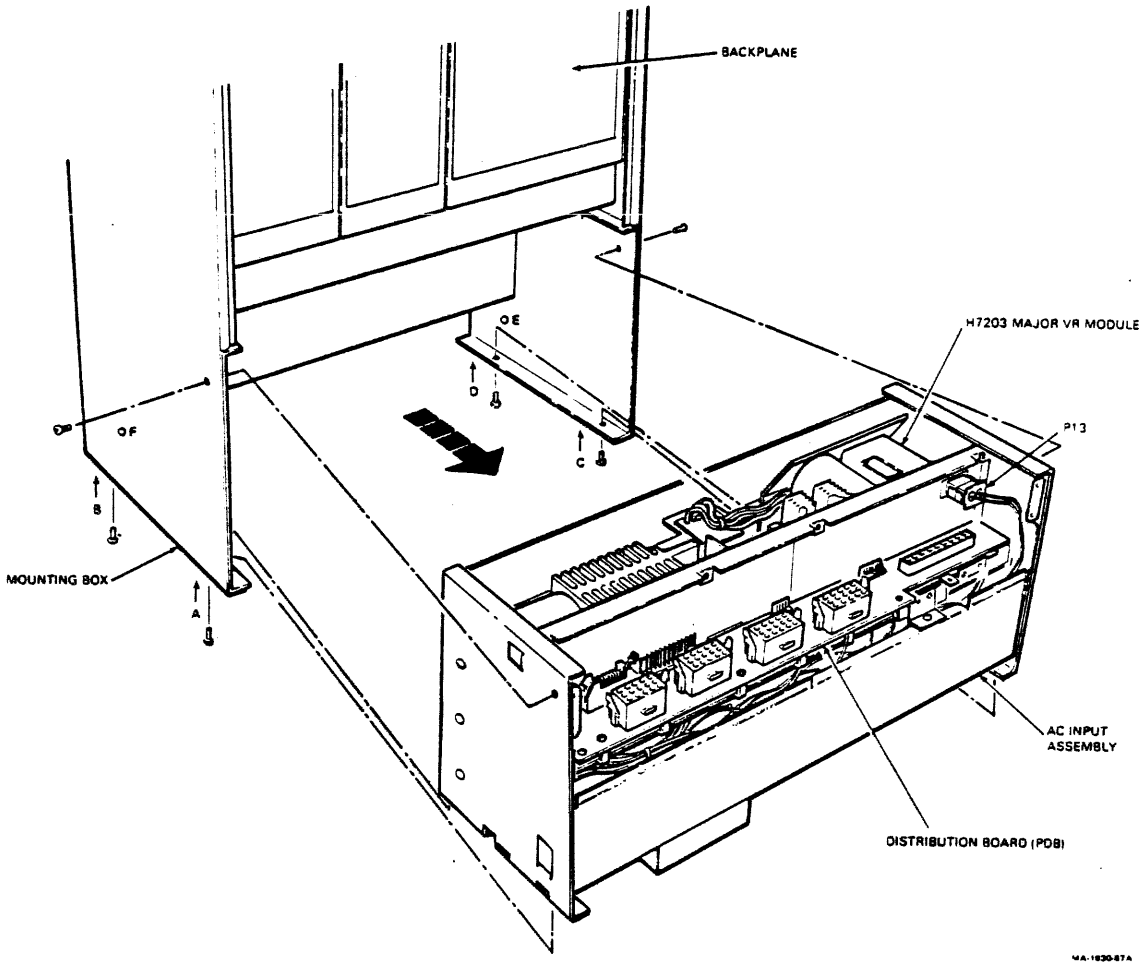


Figure 7–12 Power Supply Removal

9. Slide the H-frame power supply assembly free of the system box and set the power supply aside.
10. Replace the faulty H7204-C power supply by reversing the steps to remove the faulty unit.

7.7 Fan Assembly

To remove and replace the fan assembly (Figure 7–13):

1. Remove the two 6/32 Phillips screws that secure the fan assembly into the side of the system box.
2. Slide the fan assembly approximately 5 centimeters (2 inches) away from the box.
3. Unplug connector P1 from J1 at the outboard side of the fan assembly.
4. Slide the fan assembly free of its system box compartment.

5. If a complete fan assembly is not available, but specified replacement fans are available, you can replace any defective fan of the assembly. To replace a defective fan:

   a. Remove the fan assembly from its compartment.

   b. Remove the four 6/32 Phillips screws.

   c. Remove the individual spade connectors on the red +12.3 Vdc and black ground wires at the fan casing.

   d. Mount the new fan with the four previously removed 6/32 Phillips screws.

   e. Replace the spade connectors.

   CAUTION
   Follow the polarity indicated on the label adjacent to each spade connector on the fan casing.

   f. Reinstall the fan in the system box by sliding the fan assembly into its system box compartment to a depth where the main fan connector P1 can be plugged into J1. Push the assembly all the way in and secure the assembly to the side of the system box with the two 6/32 Phillips screws you previously removed.

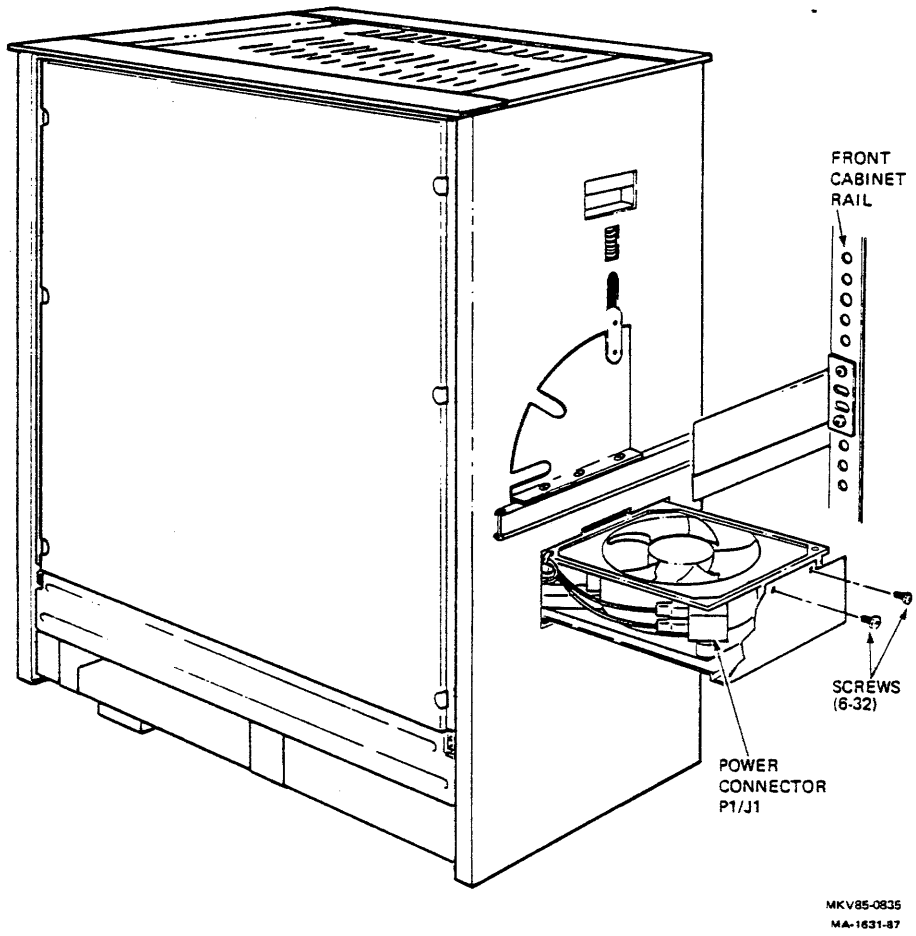


Figure 7–13 Fan Assembly Removal

7.8 CPU Backplane

To remove the CPU backplane:

1. Turn off the power circuit breaker.
2. Unplug the AC power cord from the outlet.
3. Place the system box in the maintenance position (Figure 7–3).
4. Unplug all the module cables and label them with their module numbers.
5. Unplug all the modules. Label each module with its slot number.
6. Remove the two nuts securing the +5 Vdc power cable (red) and +5 return cable (black). Unplug the backplane ribbon cable (Figure 7–14).

NOTE
Mark the power cables for easy installation.

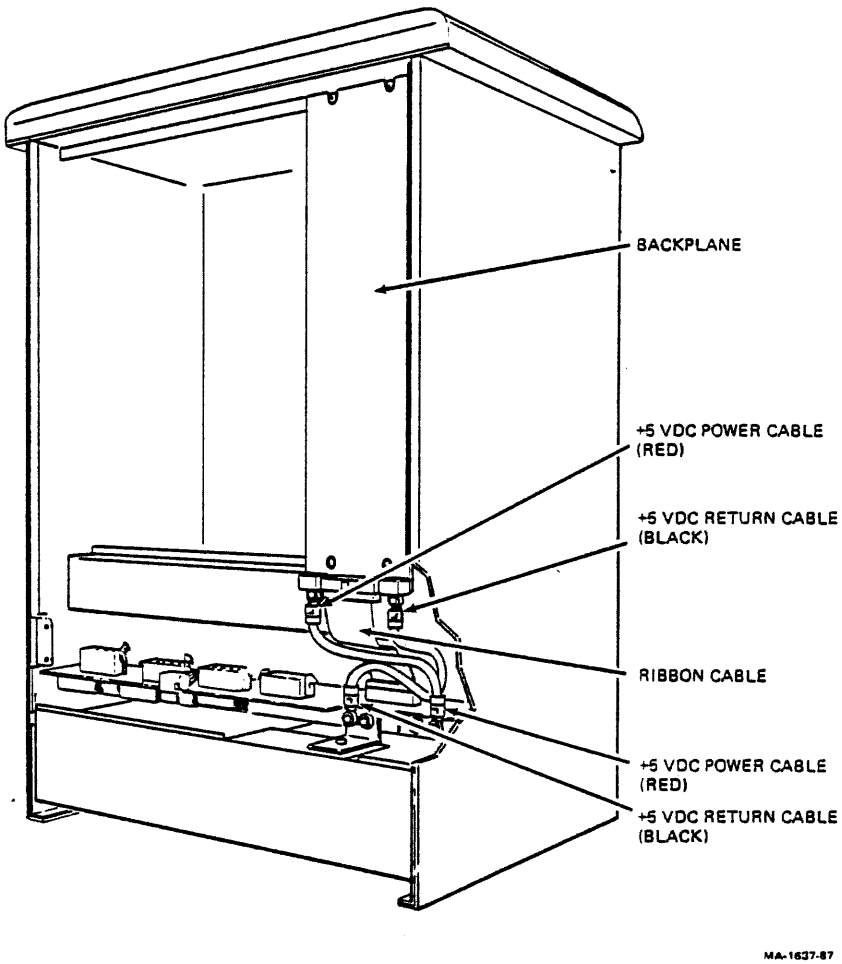


Figure 7–14 Backplane Removal

7. Remove the two screws at the top of the backplane.
8. Remove the two screws at the bottom of the backplane.
9. Remove the backplane from the system box.

This completes the removal procedure for the CPU backplane. To reinstall the backplane, reverse the above steps. Be sure the NPG jumpers on the replacement backplane match those of the original backplane configuration.

7.9 Front Panel Module

To remove the front panel module (Figure 7–15):

1. Turn off the power supply circuit breaker.
2. Unplug the AC power cord from the wall outlet.
3. Remove the front bezel by loosening (do not remove) the four screws from the bezel rear side. Lift the bezel up and away from the box.

   CAUTION
   Do not pull the bezel far from the system box. Doing so may cause stress to the ribbon cable attached to the front panel.

4. Remove the cable that is plugged into the front panel module.

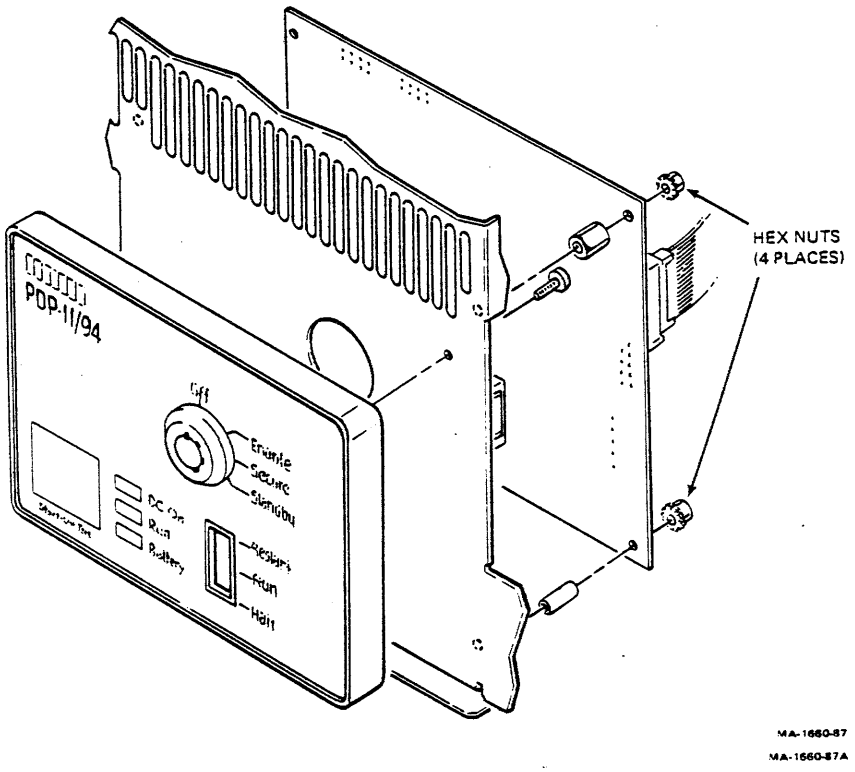


Figure 7–15 Front Panel Removal

5. Loosen and remove the four nuts securing the front panel module to the front bezel.
6. Remove the front panel module.

This completes the front panel module removal. To reinstall the box front panel, reverse the above steps.

7.10 877-DB/F Power Controller

The 877-DB/F power controller is a bulkhead-mounted unit attached from its front panel by ten mounting screws (Figure 7–16). Facing the rear of the system, locate the power controller in the lower right corner of the cabinet (Figures 7–4 and 7–5).

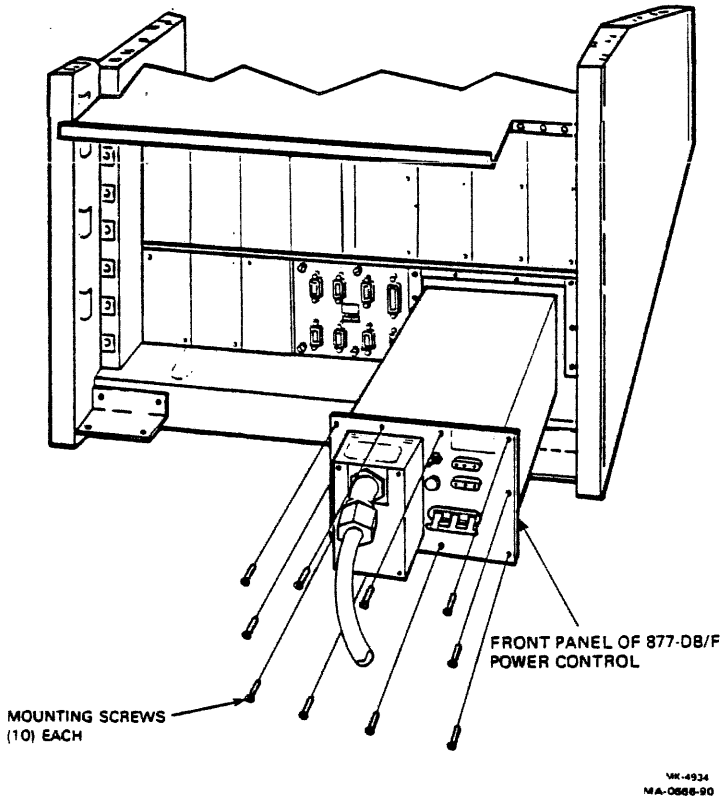


Figure 7–16 Mounting the 877-DB/F Power Controller

7.10.1 Removal

To remove the 877-DB/F power controller.

1. Ensure that the **Remote/Off/Local** switch is in the off position.
2. Ensure that the main circuit breaker on the power controller is in the off position (down).
3. Disconnect the AC connector connected to the facility's power (Figure 7–17).

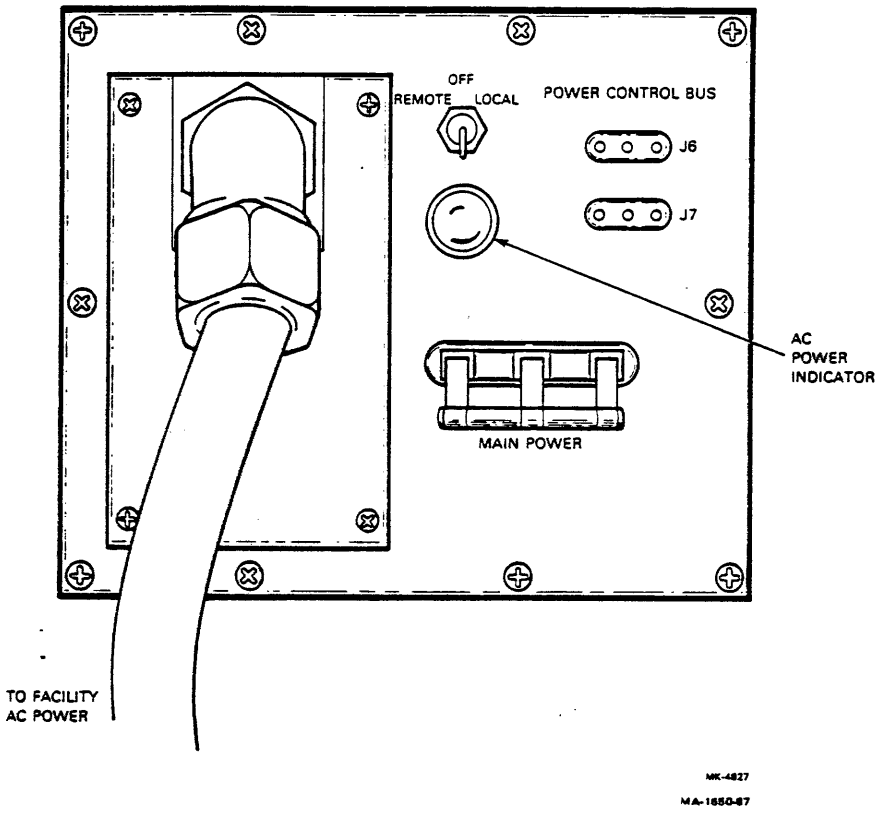


Figure 7–17 877-DB/F Power Controller (Front View)

4. Disconnect connector P2 (accessible through the front of the system cabinet) of the cable assembly to connector J8 or J9 of the power controller (Figure 7–18).

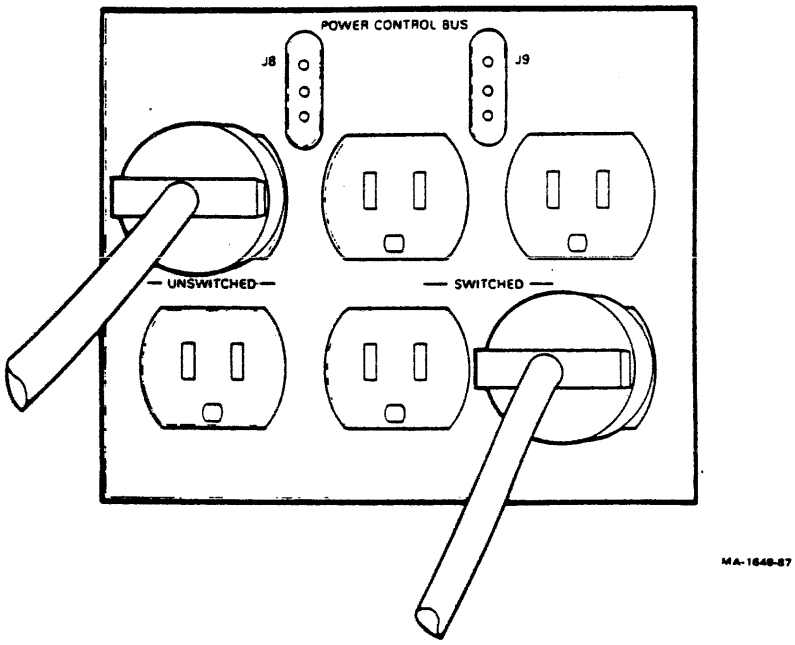


Figure 7–18 877-DB/F Power Controller (Rear View)

5. Disconnect the AC connectors (accessible through the front of the system cabinet) from the switched and unswitched receptacles on the back panel of the power controller (Figure 7–18).
6. Remove the ten mounting screws and slide the power controller from the bulkhead (Figure 7–18).

7.10.2 Replacement

To replace the 877-DB/Fpower controller:

1. Place the power controller into the bulkhead and replace the ten mounting screws securing the controller to the bulkhead (Figure 7–16).
2. Connect the AC connectors to the rear panel of the controller (Figure 7–18).
3. Connect all options to the four switched receptacles. The system box is connected to one of the two unswitched receptacles. The battery backup unit (if supplied) is connected to the other unswitched receptacles.
4. Attach connector P2 of cable assembly to J8 or J9 of the power controller (Figure 7–18).
5. Set the circuit breaker of the power controller to the on (up) position (Figure 7–17).
6. Place the **Remote/Off/Local** switch on the controller in the remote position (Figure 7–17).

8

Upgrading a PDP-11/84 System

This chapter describes how to upgrade a:

- PDP-11X84-A cabinet system
- PDP-11/84-A box system
- PDP-11/84-E system

Go to Section 8.1 and verify the contents of the upgrade kit. Then, refer to the appropriate upgrade section listed below to complete the upgrade:

- If you are upgrading a PDP-11X84-A cabinet system, go to Section 8.2.
- If you are upgrading a PDP-11/84-A box system, go to Section 8.3.
- If you are upgrading a PDP-11/84-E system, go to Section 8.4.

8.1 Checking the Contents of the Upgrade Kit

Before beginning the upgrade procedure, check the contents of your upgrade kit with the items listed in Table 8–1 and Figure 8–1.

Table 8–1 Upgrade Kit Contents

Part Number	Quantity	Description
KDJ11-EA	1	M8981-AA CPU Module for 2Mbyte upgrades
or		
KDJ11-EB	1	M8981-BA CPU Module for 4Mbyte upgrades
M9713-AA	1	Minimum Load Module (MLM)
M9714-AA	1	Alternate Power Source (APS) Module with APS cable (17-02783-01)
CK-KDJ1E-KB	1	Cabinet Kit: • one console/SLU panel assembly (70-27974-01) • seven 9-pin loopback connectors (12-27351-01) • one 40-pin ribbon cable (120 inches) (17-02786-03) • one 60-pin ribbon cable with 20-pin ext. (120 inches) (17-02785-02) • one cover plate for 11/84A SLU cutout • one conversion label
EK-PDP94-MG-001	1	PDP-11/94-E System User and Maintenance Guide (this book)
36-24101-04	1	Module utilization sticker
36-21232-12	1	FTZ postcard
36-21989-04	1	11/94 front panel label
36-21989-05	1	11/94 front panel international label

NOTE

If you are upgrading a PDP-11/84-A box system, you must order a kit (part number: BS20A-03) which contains shorter cables. The upgrade kit does not contain these cables.

The kit contents are:

- **one 36-inch 40-pin cable (17-02786-02).**
- **one 36-inch 60-pin cable (17-02784-02)(This cable is not needed for the PDP-11/84-A box upgrade.)**
- **one 36-inch 60-pin cable with a 20-pin extension (17-02785-01).**

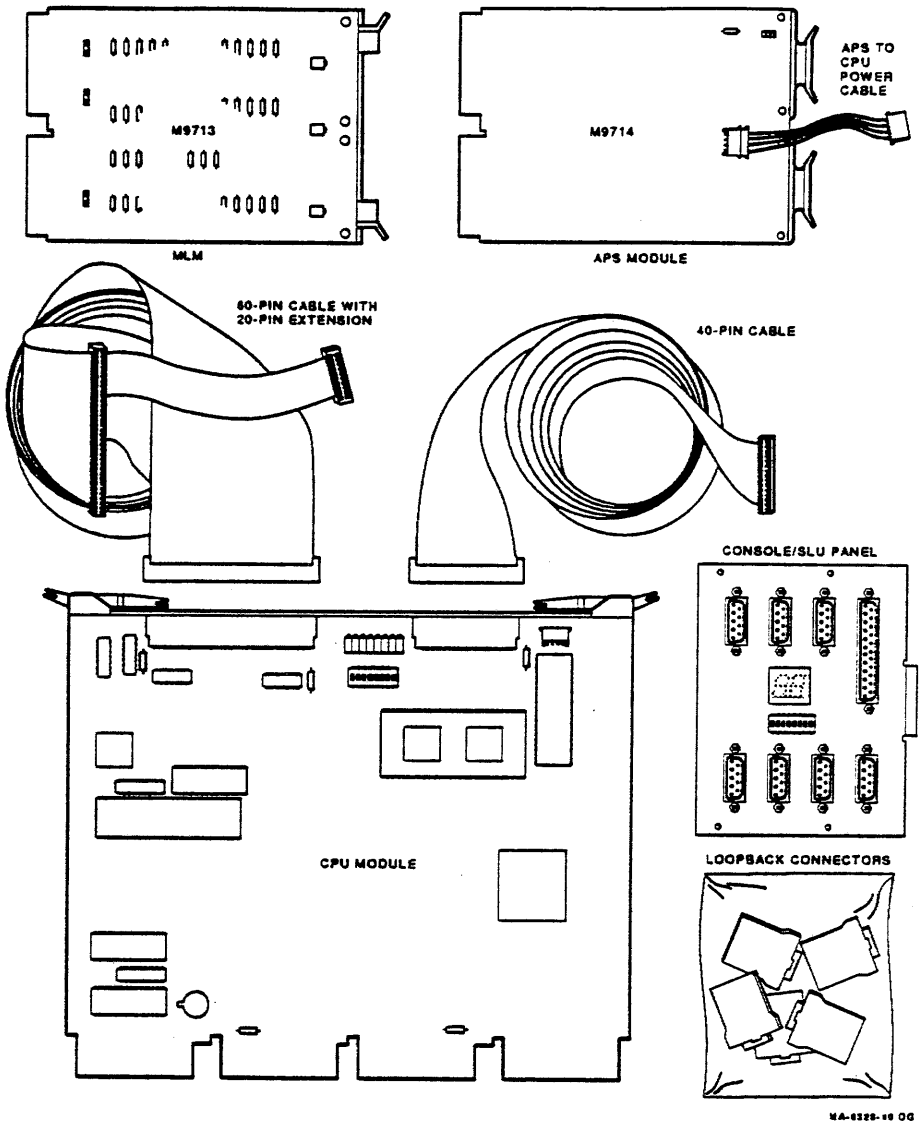


Figure 8–1 Contents of PDP-11/94-E Upgrade Kit

8.2 Upgrading a PDP-11X84-A Cabinet System

This section describes how to upgrade a PDP-11X84-A cabinet system to a PDP-11X94-A.

CAUTION

Modules and components are static sensitive. Always wear a properly connected ground strap during handling of the equipment. Modules and components must be placed on a static mat when they are removed from a backplane or shipping static bag.

8.2.1 Removal Procedures

Disconnect Power

1. Turn the power off on all peripherals connected to the system.
2. On the front panel, turn the key to the off position.
3. Unplug all ac power cords that connect the system to the wall outlets.

WARNING
To avoid electric shock when upgrading the system, ensure that all power to the system and connected peripherals is shut. Ensure that all power cords are disconnected from the wall outlets before accessing the system enclosure or any of its components.

4. Use the key to open the front and rear doors.
5. Remove the module cover from the card cage (Figure 8–2).

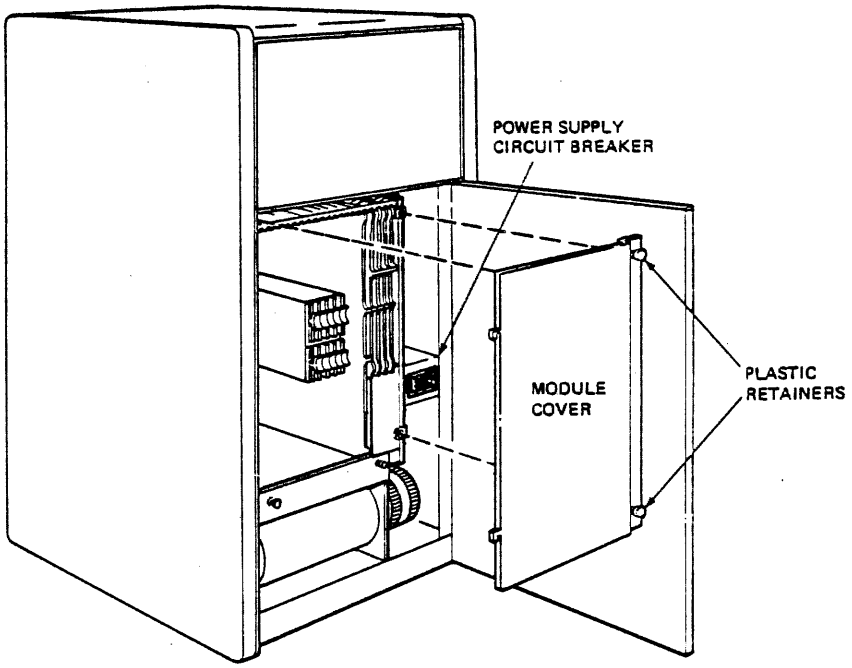


Figure 8–2 PDP-11X84-A Cabinet Module Cover/Circuit Breaker

6. On the rear of the system, set the main power controller circuit breaker to the down position to disconnect ac power (Figure 8–3).

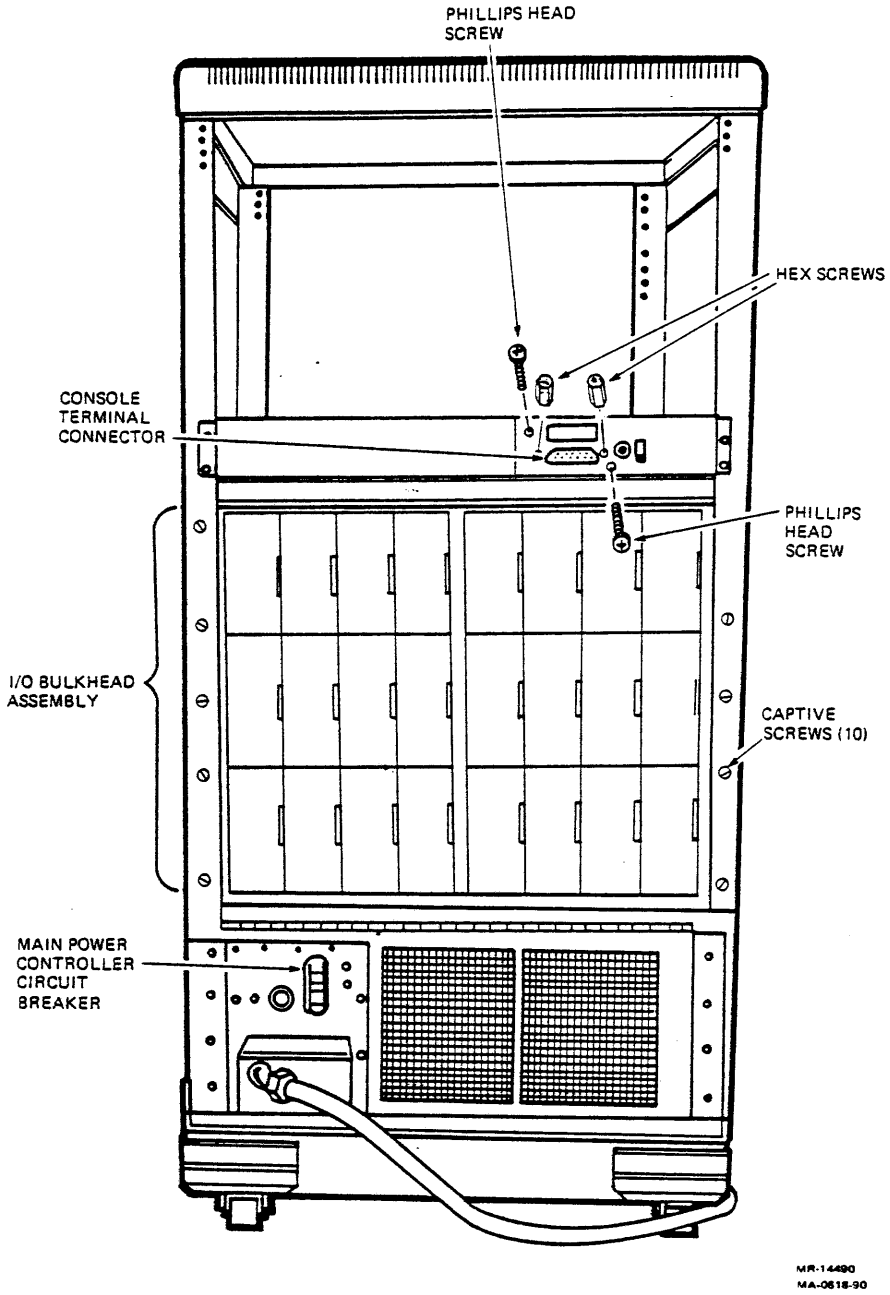


Figure 8–3 PDP-11X84-A Cabinet SLU Assembly Removal

7. On the front of the system, set the power supply circuit breaker to the down position to disconnect ac power (Figure 8–2).

Remove the Console/SLU Panel Assembly

To remove the console/SLU panel assembly:

1. Loosen the ten captive screws securing the I/O bulkhead assembly to the frame (Figure 8–3).
2. Carefully pull the top of the I/O bulkhead assembly away from the cabinet to create a partial opening. This opening provides access to the rear of the console/SLU panel assembly.

   CAUTION
   Cables are still connected to the rear of the I/O bulkhead assembly. To avoid damage to the cables and modules, *carefully pull* the I/O bulkhead down until there is enough room for your hand to fit behind the console/SLU panel assembly.
3. Unplug the console terminal cable from the connector on the front of the console/SLU panel assembly.
4. On the front of the console/SLU panel assembly, loosen and remove the two hex screws (standoffs) securing the connector to the cross member (Figure 8–3).
5. Slide your hand through the bulkhead assembly opening and hold it against the back of the console/SLU panel assembly.
6. Remove the two Phillips head screws that secure the console/SLU panel assembly to the cross member. Save the screws.
7. Unplug the SLU signal cable from the connector on the back of the console/SLU panel assembly.
8. Remove the console/SLU panel assembly from the cabinet and set aside.
9. Install the cover plate from the upgrade kit behind the console/SLU panel assembly opening using the two previously removed Phillips head screws.

Remove the Cables

NOTE
One end of the SLU signal cable is split into two 10-pin connectors, one is connected to J1 on the CPU module and the other is connected to J4 on the MDM module.

1. Unplug the SLU signal cable (10-pin connector) from J1 on the CPU module (M8190) (Figure 8–4).

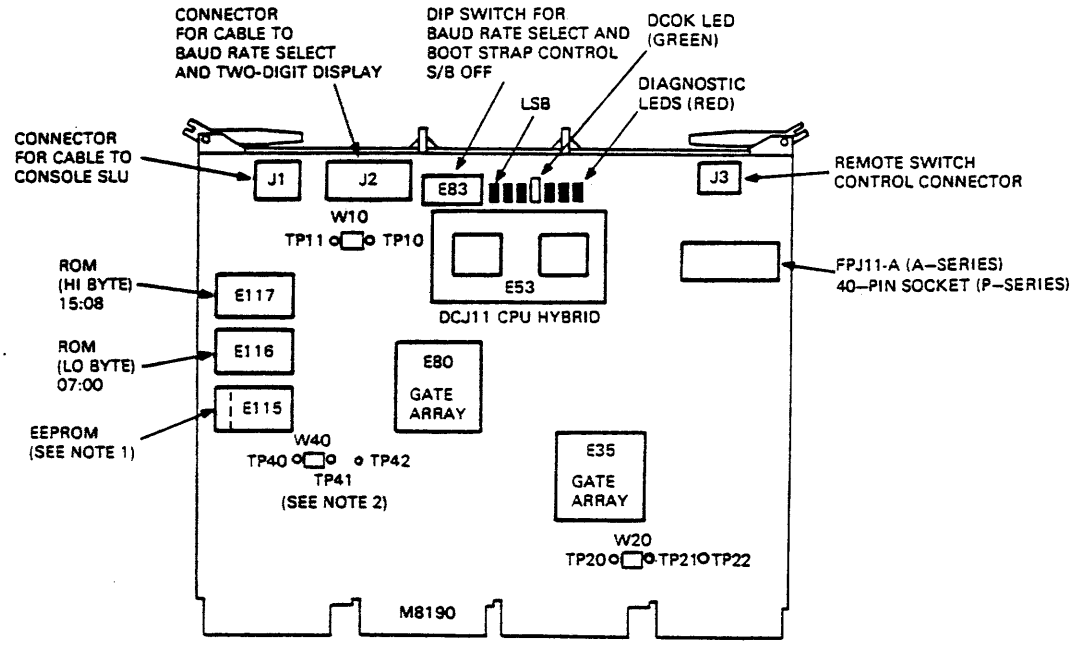


Figure 8–4 KDJ11-B CPU Module (M8190)

2. Unplug the SLU signal cable (10-pin connector) from J4 on the MDM (Figure 8–5).

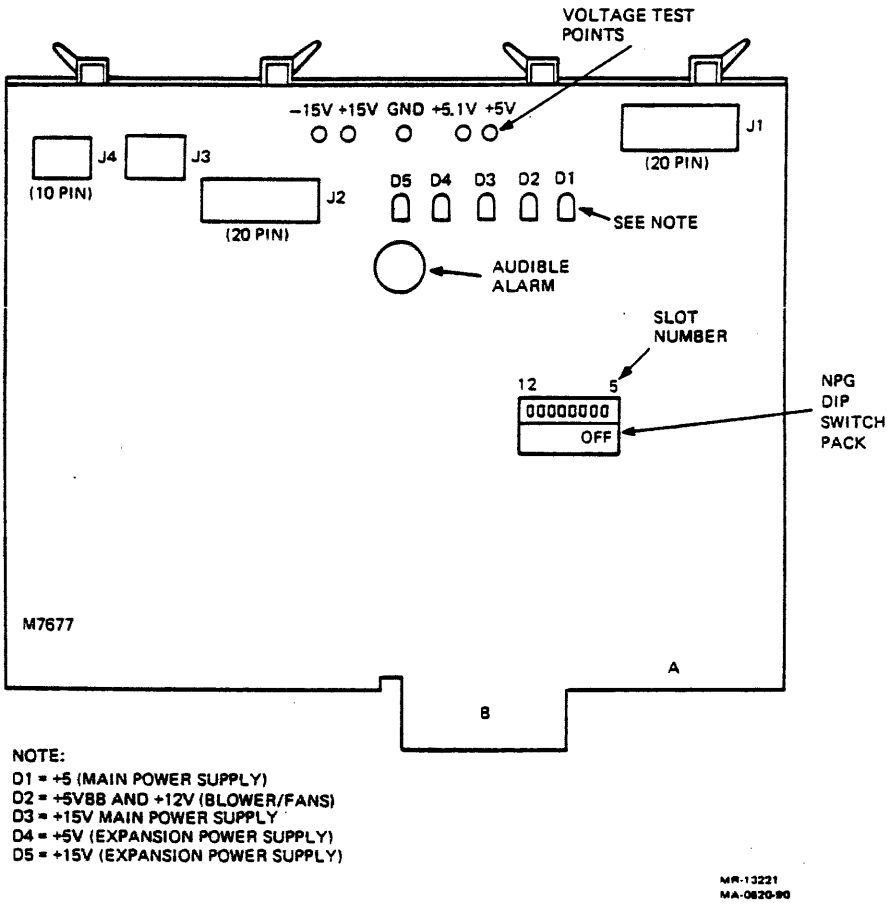


Figure 8–5 MDM Module (M7677)

3. Remove the SLU signal cable from the cabinet.
4. Unplug the MDM ribbon cable connected to J2 on the CPU module (M8190).
5. Unplug the other end of the MDM ribbon cable from J2 on the MDM.
6. Remove this cable from the cabinet.

Remove the Modules

1. Remove the CPU module (M8190) from slot 1 of the CPU backplane.
2. Remove any memory modules from slots 2 and 3 of the CPU backplane.

3. Remove all MLM modules (M7556) from the *CPU backplane only*. MLM modules can be located in slot 3, rows C and D or any SPC slot, in rows E and F of the CPU backplane (Figure 8–6).

NOTE
If the MLM module (M7556)is installed, do not remove it from the expansion backplane.

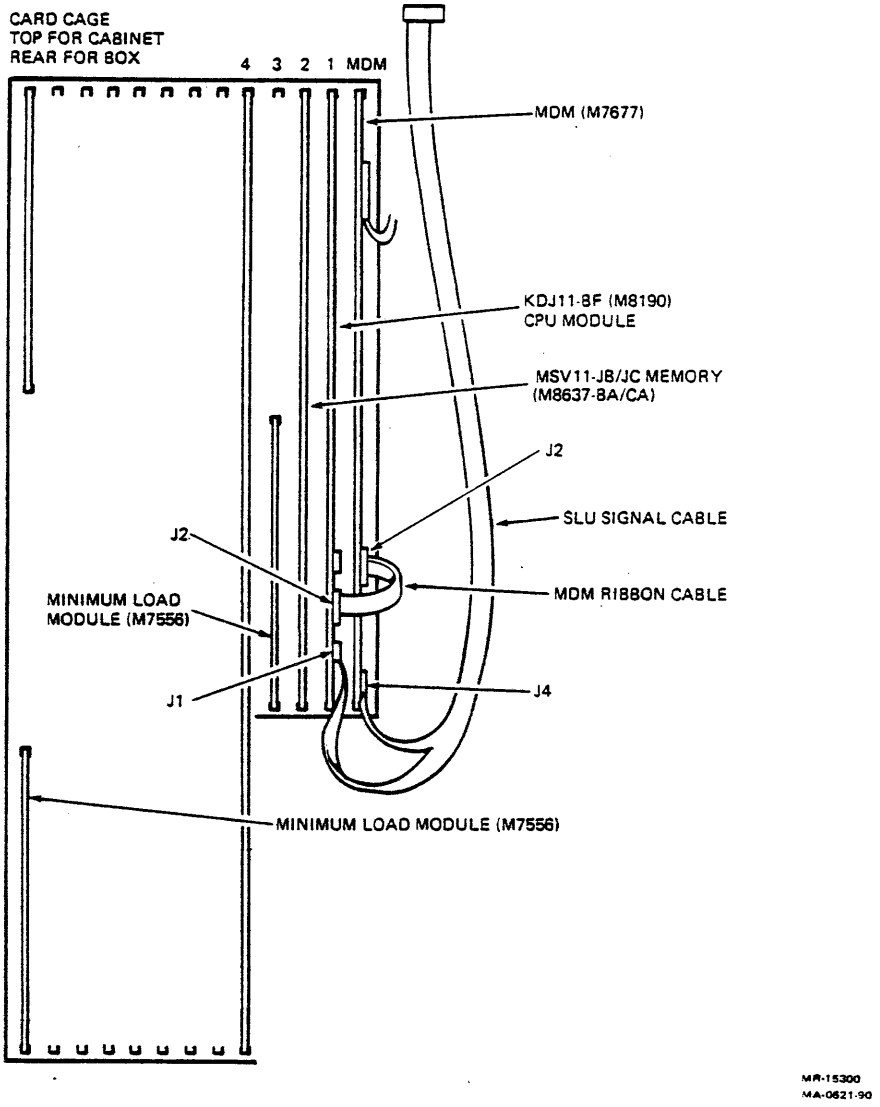


Figure 8–6 PDP-11/84-A CPU Backplane Layout

8.2.2 Installation Procedures

Install the Modules

1. Remove jumpers W1 and W2 from the KDJ11-E CPU module (M8981) in the upgrade kit. See Figure 8–7.

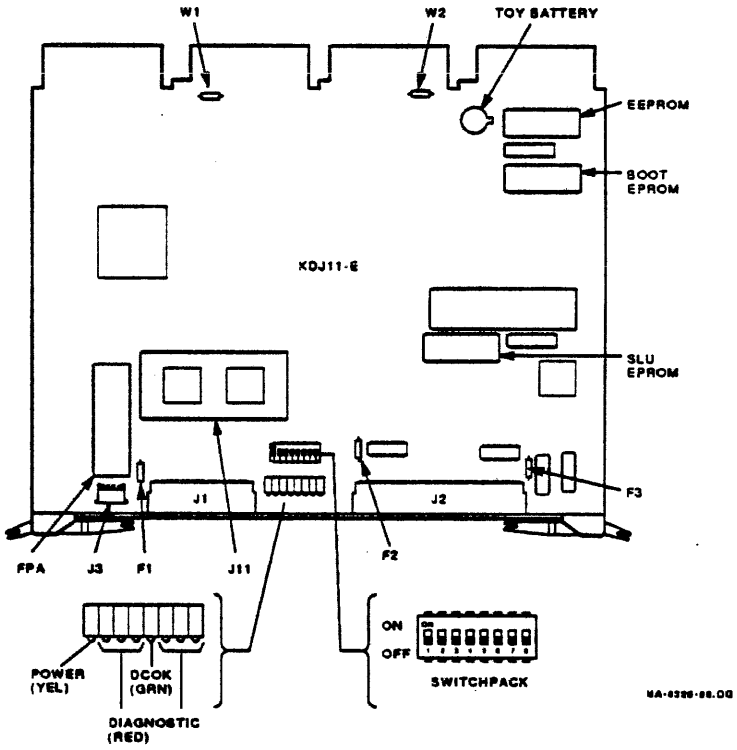


Figure 8–7 KDJ11-E CPU Module (M8981) - Jumpers W1 and W2

CAUTION
To prevent damage to the power supply, ensure that jumpers W1 and W2 are removed from the KDJ11-E CPU module (M8981) before installing the module in the CPU backplane.

2. Ensure that all switches on the DIP switch pack are set to the off position.
3. Install the KDJ11-E CPU module (M8981), provided in the upgrade kit, in slot 1 of the CPU backplane.
4. Install the APS module (M9714) ,provided in the upgrade kit, in slot 2, rows A and B of the CPU backplane.

5. Remove jumpers W1 and W3 on the MLM (Figure 8–8).

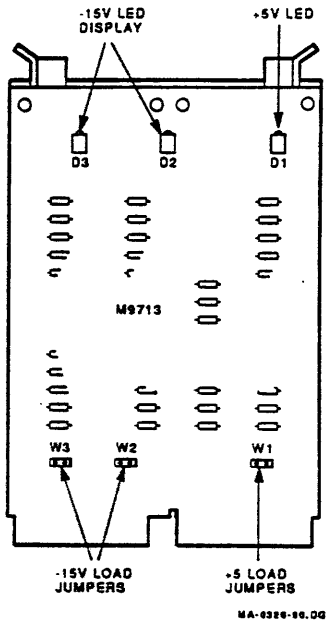


Figure 8–8 MLM Module (M9713) - Jumpers W1 and W3

6. To determine if jumper W2 should be installed, refer to Table 8–2.

Table 8–2 Minimum Load Requirements for a PDP-11X94-A

2A of +5.1VBB	No load module required. This requirement is met by the M8981 CPU which draws 4.0A of +5.1VBB.
7A of +5V	No additional 5V load is required. This requirement is met by the UBA module which draws 7.4A of +5V. Ensure that W1 on the MLM module (M9713) is removed.
300mA of -15V	Calculate the current usage for -15V for all the options in the CPU backplane. If it does not exceed 300mA, ensure that jumper W2 is installed on the MLM module. If the current usage exceeds 1A, remove jumper W2 on the MLM module.

7. Install the MLM module (M9713), provided in the upgrade kit, in any unused SPC slot in rows E and F of the CPU backplane.

Install the Console/SLU Panel Assembly

To install the KDJ11-E console/SLU panel assembly in the I/O bulkhead assembly:

1. Select any two adjacent I/O panels and remove the covers.
2. Mount the KDJ11-E console/SLU panel assembly into the two open, adjacent I/O slots.
3. Secure the console/SLU panel assembly by tightening the four captive screws.

Connect the Cables

NOTE
All cable connectors are keyed for ease of installation.

1. Connect one end of the APS cable to the connector on the APS module (M9714).
2. Connect the other end of the APS cable to J3 on the CPU module (M8981).
3. Connect one end of the 40-pin cable (17-02786-03) to J1 on the KDJ11-E CPU module (M8981).
4. Thread the other end of the 40-pin cable through to the rear of the system and connect it to J1 on the back of the console/SLU panel assembly.

NOTE
One end of the SLU signal cable (17-02785-02) has a single 60-pin connector. The other end has a 60-pin connector with a 20-pin extension connector (Figure 8–9).

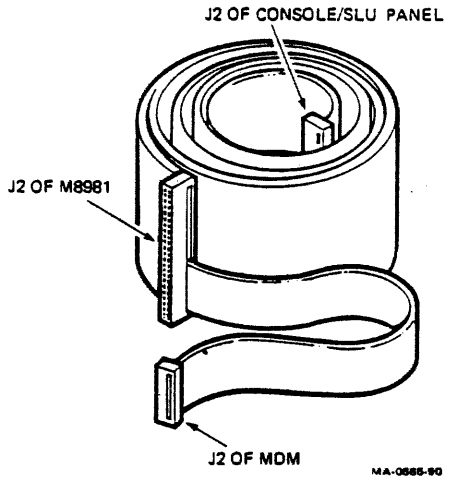


Figure 8–9 SLU Signal Cable (17-02785-02)

5. Connect the end with the single 60-pin connector to J2 on the console/SLU panel assembly.
6. Connect the other 60-pin end to J2 of the CPU module (M8981) (Figure 8–7).
7. Connect the 20-pin extension connector to J2 of the MDM module (Figure 8–5).

Connect the Power

1. Close the I/O bulkhead assembly and tighten the ten captive screws to secure the assembly to the frame.
2. On the front of the system, set the power supply circuit breaker to the up position to connect ac power.
3. On the rear of the system, set the main power controller circuit breaker to the up position to connect ac power.
4. Replace the module cover from the card cage.

5. Connect the console terminal cable to the console port on the back of the console/SLU assembly.
6. Set the console/SLU switch pack according to the settings shown in Table 8–3 and Table 8–4.

Table 8–3 Console/SLU Switch Settings

Switch	Setting	Function
1	Off	Console SLU enabled.
2, 3, 4	Off	ROM mode not selected.
5	On	Forced dialog enabled.
6, 7, 8	See Table 8–4	

Table 8–4 Baud Rate Chart

SLU Baud Rate	6	7	8
300	OFF	OFF	OFF
600	OFF	OFF	ON
1200	OFF	ON	OFF
2400	OFF	ON	ON
4800	ON	OFF	OFF
9600	ON	OFF	ON
19200	ON	ON	OFF
38400	ON	ON	ON

7. Set the console terminal to eight data bits, no parity, and one stop bit.
8. Close the front and rear doors.
9. Install the appropriate front panel label, provided in the upgrade kit, over the old front panel label.
10. Plug the AC power cord into the wall outlet.

Run Diagnostics

1. Turn the key on the keylock power switch on the front panel to the Enable position.
2. Execute test 30, **All Selected Tests**, for 5 passes. Refer to Section 6.3.1 for instructions.

You have successfully completed the upgrade for the PDP-11X84-A cabinet system.

8.3 Upgrading a PDP-11/84-A

This section describes how to upgrade a PDP-11/84-A system (box product) to a PDP-11/94-A system.

CAUTION
Modules and components are static sensitive. Always wear a properly connected ground strap during handling of the equipment. Modules and components must be placed on a static mat when they are removed from a backplane or shipping static bag.

8.3.1 Removal Procedures

Disconnect the Power

1. Turn the power off on all peripherals that are connected to the system.
2. On the front panel, turn the key to the off position.
3. Unplug all ac power cords that connect the system to the wall outlets.

   WARNING
   To avoid electric shock when upgrading the system, ensure that all power to the system and connected peripherals is shut off. Ensure that all power cords are disconnected from the wall outlets before accessing the system enclosure or any of its components.

4. Set the circuit breaker on the right side of the box to the down position to disconnect the ac power.

Remove the Console/SLU Panel Assembly

1. Loosen the four captive screws on the top cover (Figure 8–10).
2. Lift the cover off.

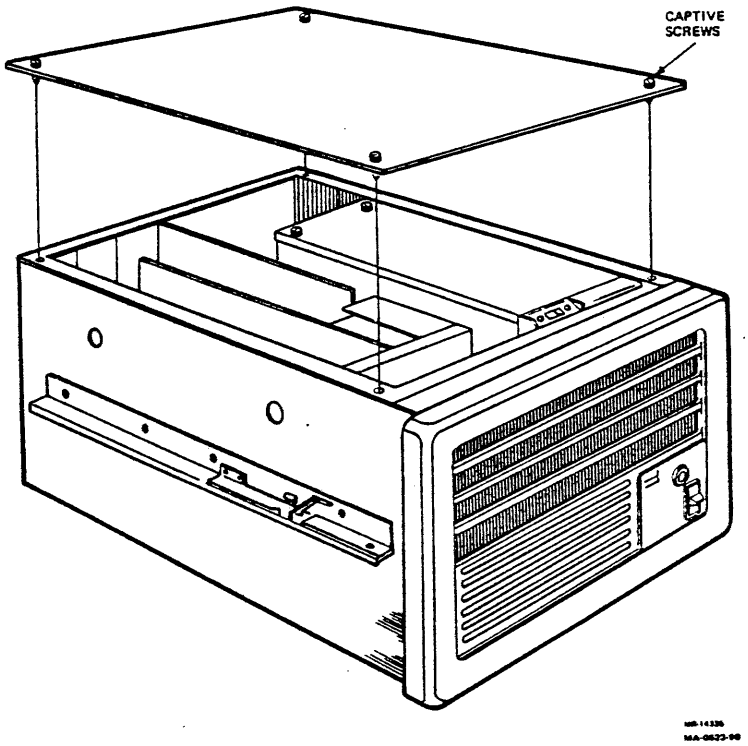


Figure 8–10 Removing the PDP-11/84-A Box Cover

3. Unplug the SLU signal cable from the console/SLU panel assembly board.
4. Unplug the console terminal cable from the connector on the front of the console/SLU panel assembly.

5. Remove the two hex screws (standoffs) securing the console/SLU panel assembly connector to the back panel (Figure 8–11).

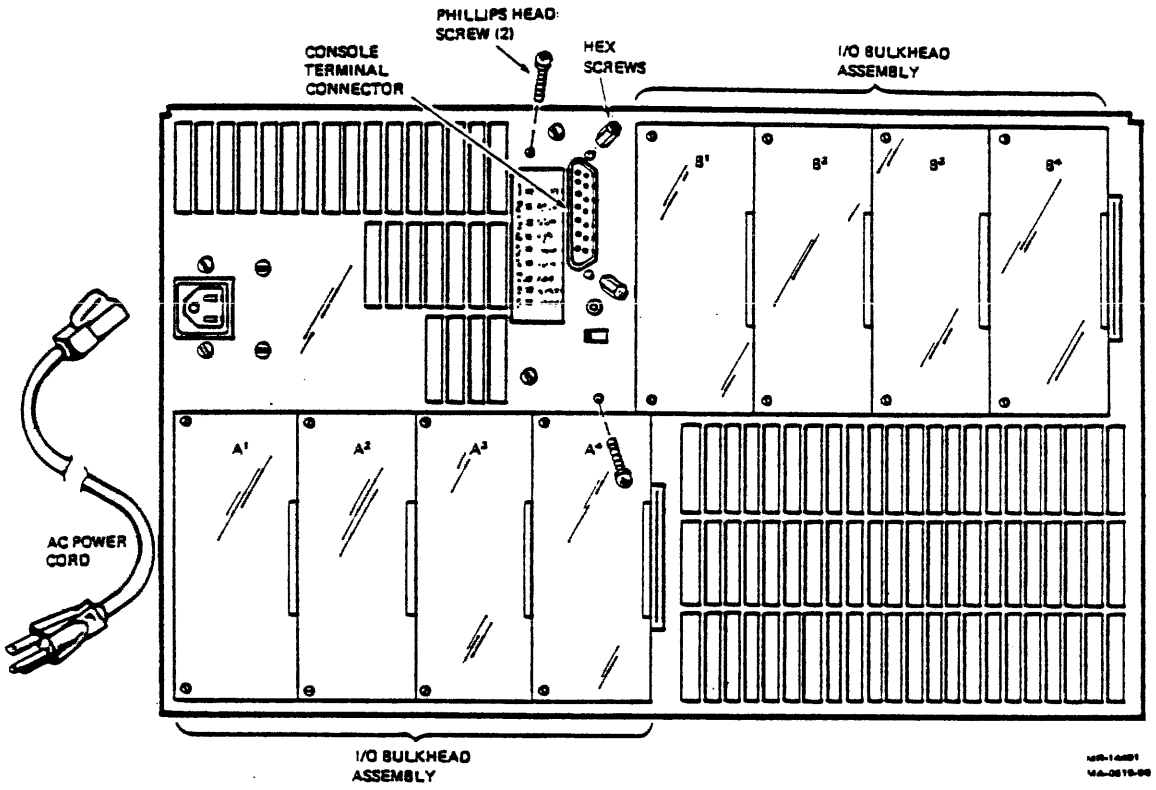


Figure 8–11 PDP-11/84-A Box Console/SLU Panel Assembly Removal

6. Remove the two Phillips head screws from the rear of the box (Figure 8–11). Save the screws.
7. Remove the console/SLU panel assembly from the box.
8. Install the cover plate from the upgrade kit behind the console/SLU panel assembly opening using the two previously removed Phillips head screws.

Remove the Cables

NOTE
One end of the SLU signal cable is split into two 10-pin connectors, one is connected to J1 on the CPU module and the other is connected to J4 on the MDM module.

1. Unplug the SLU signal cable (10-pin connector) from J1 on the CPU module (M8190) (Figure 8–4).
2. Unplug the SLU signal cable (10-pin connector) from J4 on the MDM (Figure 8–5).
3. Remove the SLU signal cable from the cabinet.
4. Unplug the MDM ribbon cable connected to J2 on the CPU module (M8190).
5. Unplug the other end of the MDM ribbon cable from J2 on the MDM.
6. Remove this cable from the cabinet.

Remove the Modules

1. Remove the CPU module (M8190) from slot 1 of the CPU backplane.
2. Remove any memory modules from slots 2 and 3 of the CPU backplane.
3. Remove all MLM modules (M7556) from the CPU backplane. MLM modules can be located in slot 3 in rows C and D or any SPC slot in rows E and F of the CPU backplane (Figure 8–6).

8.3.2 Installation Procedures

Install the Modules

1. Remove jumpers W1 and W2 from the KDJ11-E CPU module (M8981) in the upgrade kit. See Figure 8–7.

   CAUTION
   To prevent damage to the power supply, ensure that jumpers W1 and W2 are removed from the KDJ11-E CPU module (M8981) before installing the module in the CPU backplane.

2. Ensure that all switches on the DIP switch pack are set to the off position.
3. Install the KDJ11-E CPU module (M8981), provided in the upgrade kit, in slot 1 of the CPU backplane.
4. Install the APS module (M9714), provided in the upgrade kit, in slot 2 in rows A and B of the CPU backplane.
5. Remove jumpers W1 and W3 on the MLM (Figure 8–8).
6. Install the MLM module (M9713), provided in the upgrade kit, in any unused SPC slot in rows E and F of the CPU backplane.
7. To determine if jumper W2 should be installed, refer to Table 8–5.

Table 8–5 Minimum Load Requirements for a PDP-11/94-A

2A of +5.1VBB	No load module required. This requirement is met by the M8981 CPU which draws 4.0A of +5.1VBB.
7A of +5V	No additional 5V load is required. This requirement is met by the UBA module which draws 7.4A of +5V. Ensure that W1 on the MLM module (M9713) is removed.
300mA of -15V	Calculate the current usage for -15V for all the options in the CPU backplane. If it does not exceed 300mA, ensure that jumper W2 is installed on the MLM module. If the current usage exceeds 1A, remove jumper W2 on the MLM module.

Install the Console/SLU Panel Assembly

To install the KDJ11-E console/SLU panel assembly in the I/O bulkhead assembly:

1. Select any two adjacent I/O panels and remove the covers.
2. Mount the KDJ11-E console/SLU panel assembly into the two open, adjacent I/O slots.

3. Secure the console/SLU panel assembly by tightening the four captive screws.

Connect the Cables

NOTE
All cable connectors are keyed for ease of installation. Use the 36-inch, 40-pin cable (17-02786-02) and the 36-inch 60-pin cable with the 20-pin extension (17-02785-01), if ordered.

1. Connect one end of the APS cable to J3 on the APS module (M9714).
2. Connect the other end of the APS cable to J3 on the CPU module (M8981).
3. Connect one end of the 40-pin cable (17-02786-02) to J1 on the KDJ11-E CPU module (M8981).
4. Thread the other end of the 40-pin cable through to the rear of the system and connect it to J1 on the back of the console/SLU panel assembly.

NOTE
One end of the SLU signal cable (17-02785-01) has a single 60-pin connector. The other end has a 60-pin connector with a 20-pin extension connector (Figure 8–12).

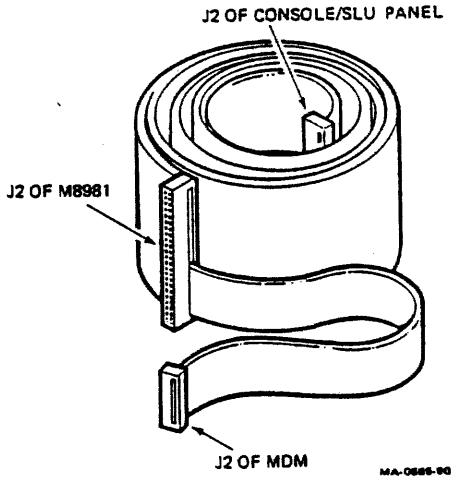


Figure 8–12 SLU Signal Cable (17-02785-01)

5. Connect the end with the single 60-pin connector to J2 on the console/SLU panel assembly.
6. Connect the other 60-pin end to J2 of the CPU module (M8981) (Figure 8–7).
7. Connect the 20-pin extension connector to J2 of the MDM module (Figure 8–5).

Connect the Power

1. Replace the top box cover and tighten the four captive screws.
2. Set the circuit breaker on the right side of the box to the up position to connect ac power.
3. Connect the console terminal cable to the console port on the back of the console/SLU assembly.

4. Set the console/SLU switch pack according to the settings shown in Table 8–3 and Table 8–4.
5. Set the console terminal to eight data bits, no parity, and one stop bit.
6. Install the appropriate front panel label, provided in the upgrade kit, over the old front panel label.
7. Plug the ac power cord into the wall outlet.

Run Diagnostics

1. Turn the key on the keylock power switch on the front panel to the Enable position.
2. Execute test 30, **All Selected Tests**, for 5 passes. Refer to Section 6.3.1 for instructions.

You have now successfully completed the upgrade for the PDP-11/84-A system.

8.4 Upgrading a PDP-11/84-E

This section describes how to upgrade a PDP-11/84-E system to a PDP-11/94-E system.

CAUTION
Modules and components are static sensitive. Always wear a properly connected ground strap during handling of the equipment. Modules and components must be placed on a static mat when they are removed from a backplane or shipping static bag.

8.4.1 Removal Procedures

Disconnect the Power

1. Turn the power off on all peripherals that are connected to the system.
2. On the front panel, turn the key to the off position.
3. Unplug all ac power cords from the wall outlets.

   WARNING
   To avoid electric shock when upgrading the system, ensure that all power to the system and connected peripherals is shut off. Ensure that all power cords are disconnected from the wall outlets before accessing the system enclosure or any of its components.

4. To remove the rear door, use a four millimeter (5/32 inch) hex wrench and release the panel fastener.
5. Remove the rear panel(s) of the cabinet.
6. For this step, refer to Figure 8–13, if you are upgrading a PDP-11X84-E system. If you are upgrading a PDP-11W84-E system, refer to Figure 8–14.
   a. Set the main power controller circuit breaker to down position to disconnect ac power.

b. Set the power supply circuit breaker to down position to disconnect ac power.

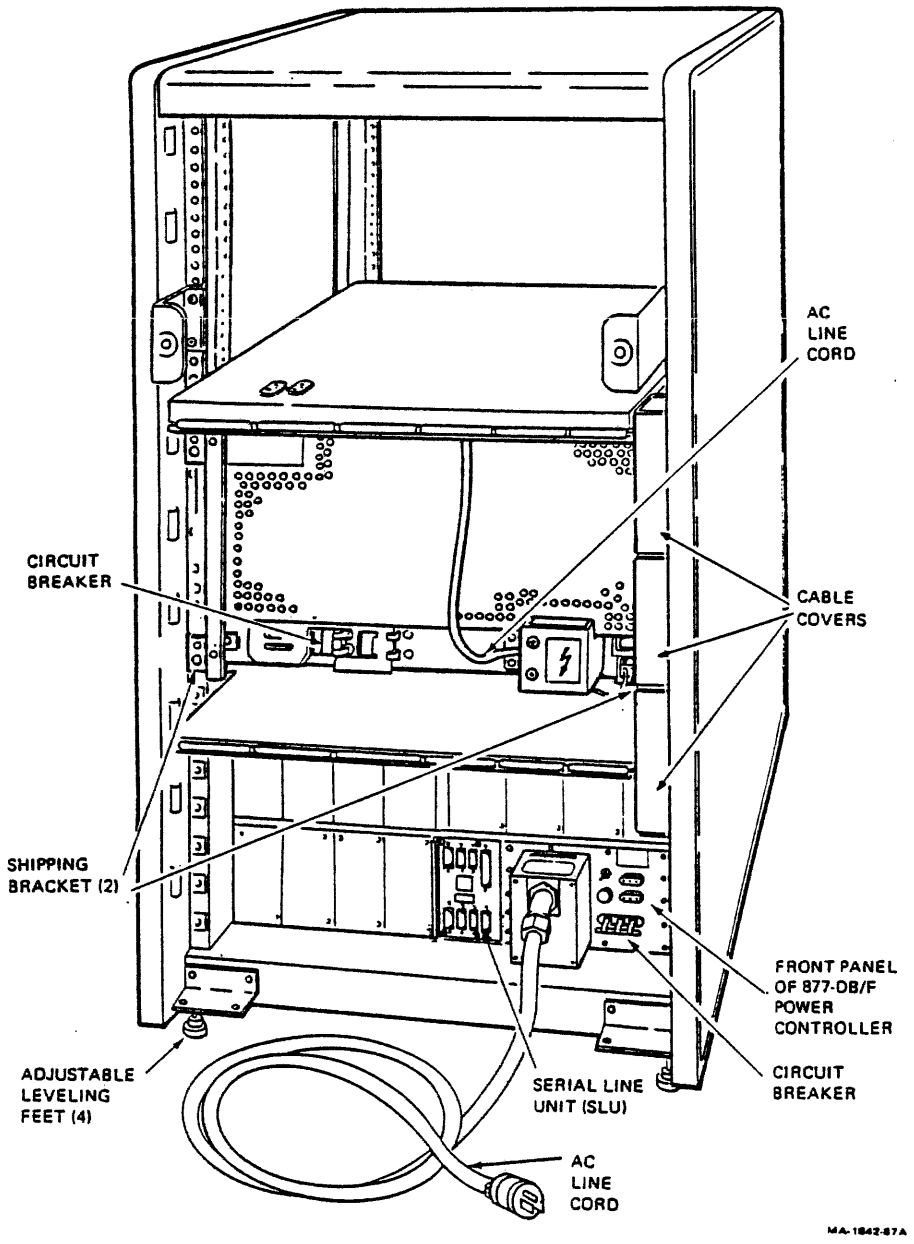


Figure 8–13 PDP-11X84-E Circuit Breakers

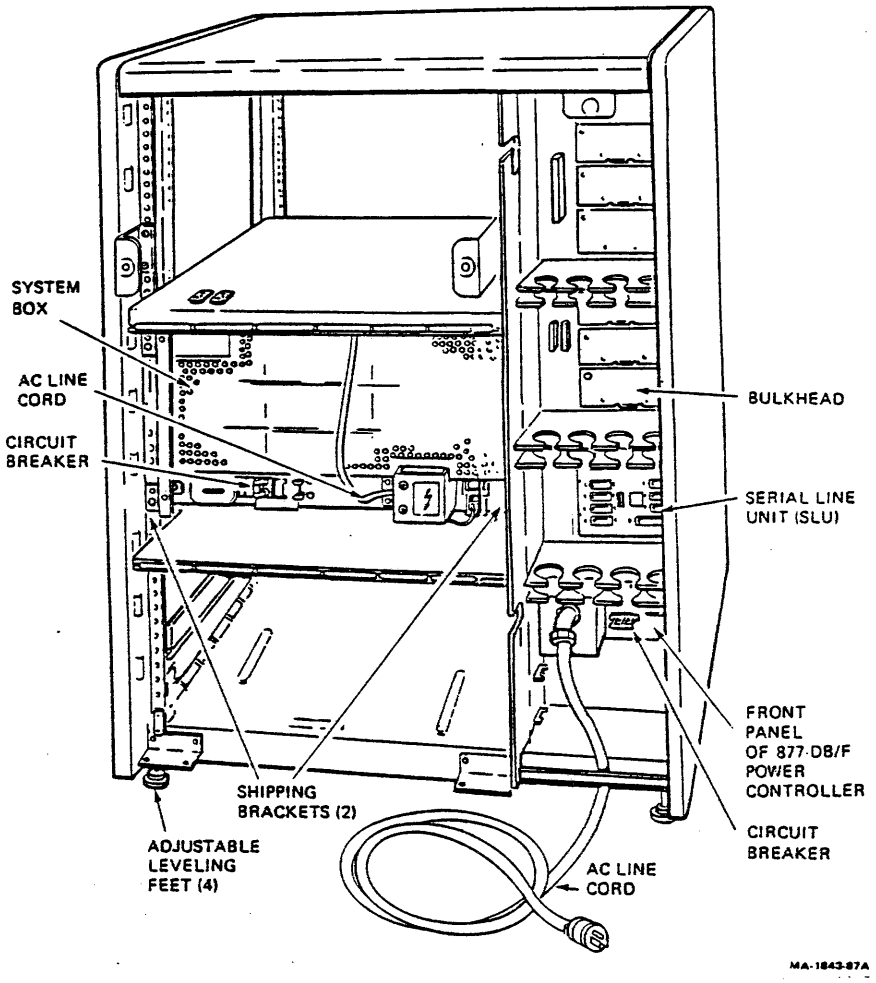


Figure 8–14 PDP-11W84-E Circuit Breakers

System Service Position and Maintenance Position

WARNING
Pull the stabilizer bar forward to prevent the cabinet from sliding forward during the upgrade procedure. Refer to Figure 8–15

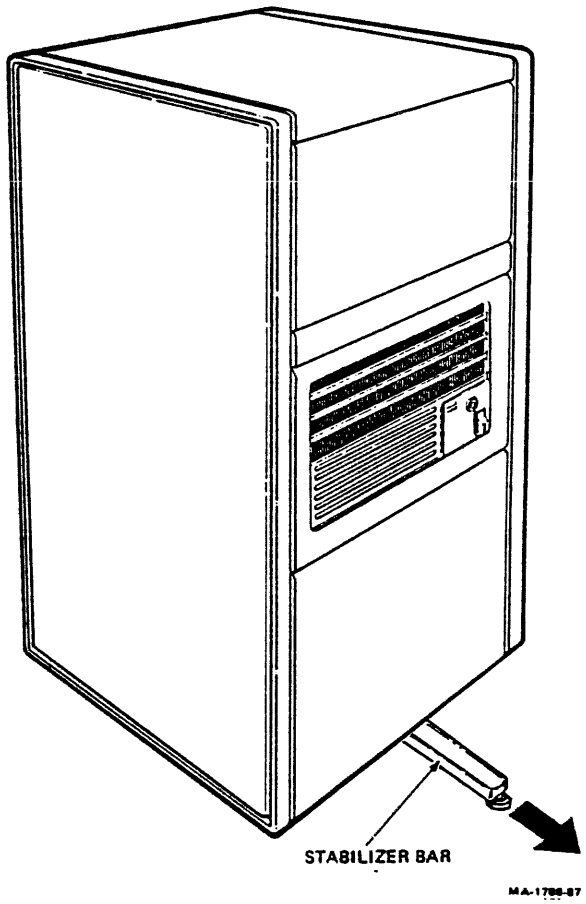


Figure 8–15 Extending the PDP-11/84-E Stabilizer Bar

1. To release the system latch:
   a. Insert the tip of a small flat-head screwdriver into the slot located on the top right side of the front bezel (Figure 8–16).
   b. Slide the screwdriver to the left.

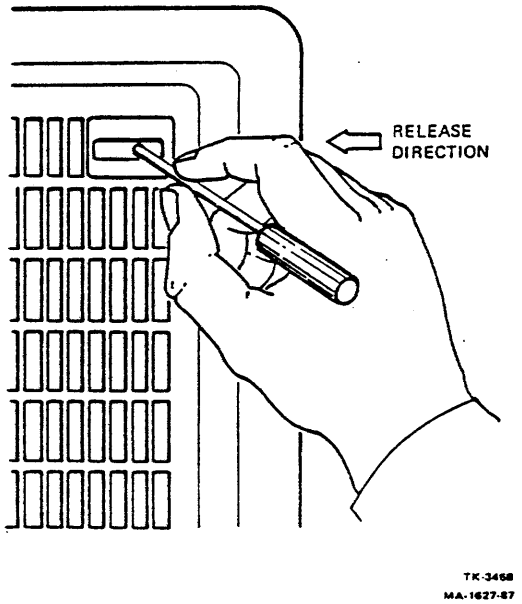


Figure 8–16 Releasing the System Latch - PDP-11/84-E

2. Pull the front of the system box forward until it is fully extended and the slide hold levers are engaged.

   The system box is now in the service position (Figure 8–17).

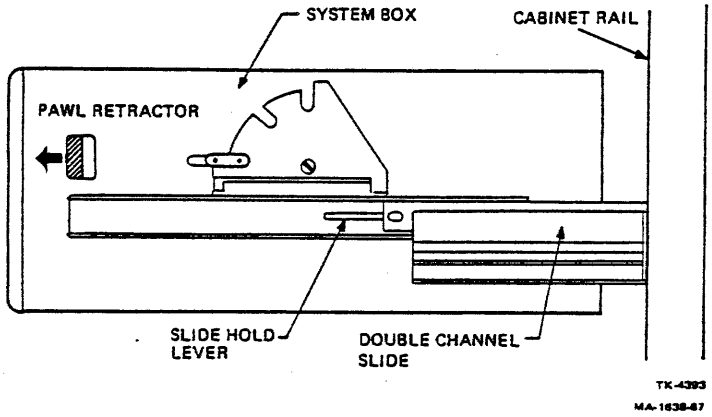


Figure 8–17 Releasing the Pawl Retractor - PDP-11/84-E

3. Remove and save the four 6/32 Phillips screws that secure the top cover to the system.
4. Remove the top cover.

Remove the Console/SLU Panel Assembly

1. Remove the two screws that secure the console/SLU panel assembly to the I/O bulkhead assembly (Figure 8–18).

2. Pull the console/SLU panel assembly slightly away from the I/O bulkhead assembly (Figure 8–18).

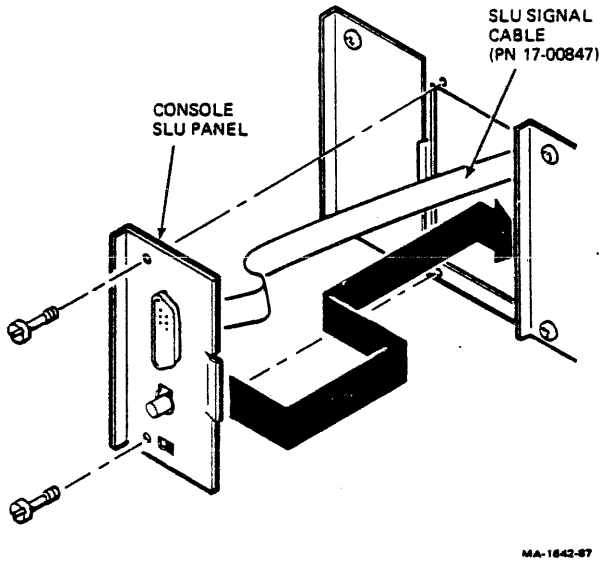


Figure 8–18 Removing the PDP-11/84-E Console/SLU Panel Assembly

3. Unplug the SLU signal cable from the connector on J3 on the back of the console/SLU panel assembly.
4. Remove the console/SLU panel assembly from the cabinet and set it aside.
5. Remove the cover from one of the adjacent I/O panels.

Remove the Cables

1. Unplug the SLU signal cable from J2 on the backplane (Figure 8–19).
2. Remove the SLU signal cable.

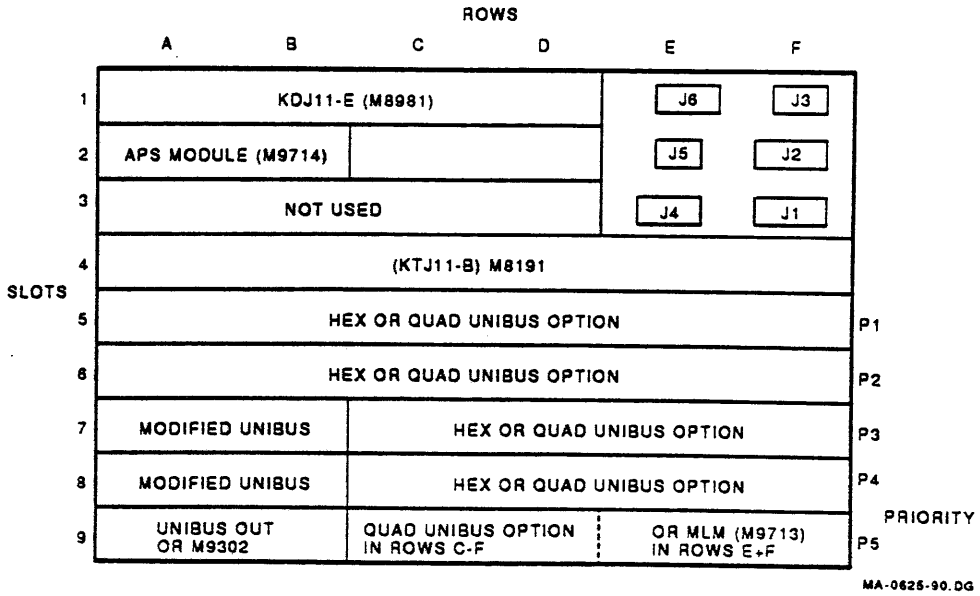


Figure 8–19 PDP-11/84-E Backplane Configuration

3. Unplug the cable connected to J2 on the CPU module (M8190) (Figure 8–20).
4. Unplug the cable connected to J6 on the backplane (Figure 8–19).
5. Remove this cable.
6. Unplug the cable connected to J1 on the CPU module (M8190) (Figure 8–20).
7. Unplug the cable connected to J5 on the backplane (Figure 8–19).
8. Remove this cable.

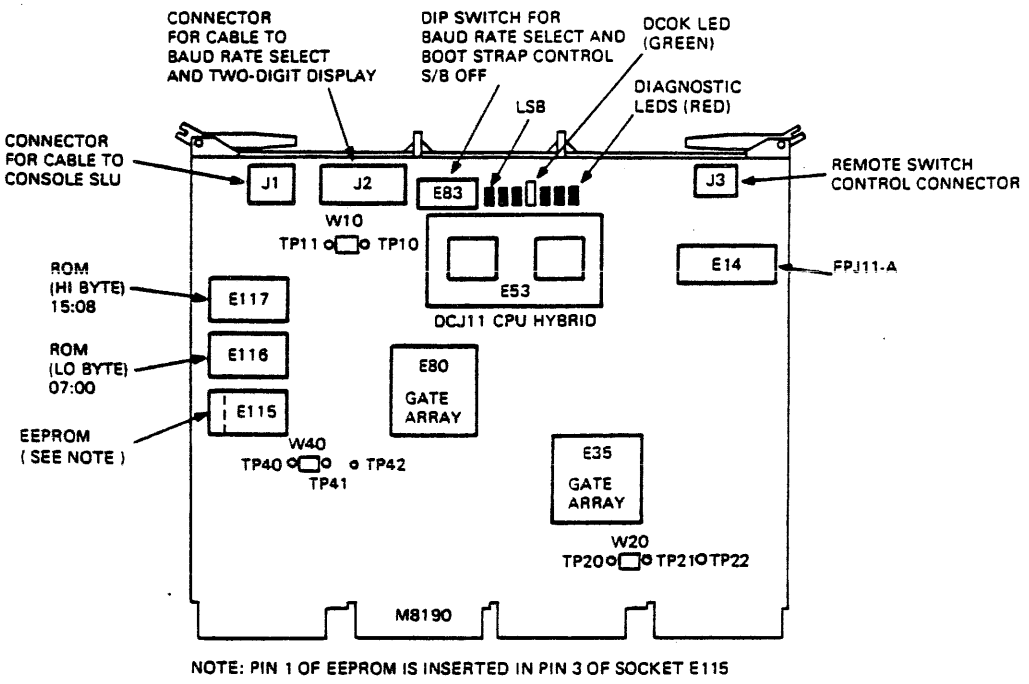


Figure 8–20 KDJ11-BF CPU Module (M8190)

Remove the Modules

1. Remove the CPU module (M8190) from slot 1 of the CPU backplane.
2. Remove any memory modules from slots 2 and 3 of the CPU backplane.
3. Remove the MLM module (M7556), if installed, from slot 3, rows C and D.
4. Remove the MLM module (M9049) in any backplane in the CPU box, if installed.

8.4.2 Installation Procedures

Install the Modules

1. Remove jumpers W1 and W2 from the KDJ11-E CPU module (M8981) in the upgrade kit. See (Figure 8–7).

   CAUTION
   To prevent damage to the power supply, ensure that jumpers W1 and W2 are removed from the KDJ11-E CPU module (M8981) before installing the module in the CPU backplane.

2. Install the KDJ11-E CPU module (M8981), provided in the upgrade kit, in slot 1 of the CPU backplane.

3. Install the APS module (M9714), provided in the upgrade kit, in slot 2, rows A and B of the CPU backplane.
4. Install the MLM module (M9713) in the CPU backplane, slot 9, rows E and F or any other unused SPC slot in the CPU backplane in rows E and F.
5. Refer to Table 8–6 to configure the jumpers on the MLM module.

Table 8–6 Minimum Load Requirements for the PDP-11/84-E

2A of +5VBB	No load module required. This requirement is met by the M8981 CPU which draws 3.9A of +5VBB.
10A of +5 V	The UBA module draws 7.4A of +5V. Calculate the current usage for +5V for all options including the UBA in the CPU box. If it does not exceed 10A, ensure that jumper W1 on the MLM (M9713) module is installed. If the current usage exceeds 10A, remove W1 on the MLM module.
700mA of -15 V	Calculate the current usage for -15V for all the options in the CPU box. If it does not exceed 700mA, ensure that jumpers W2 and W3 are installed on the MLM module. If the current usage exceeds 700mA, remove jumpers W2 and W3 on the MLM module.

Install the Console/SLU Panel Assembly

To install the KDJ11-E console/SLU panel assembly in the I/O bulkhead assembly:

1. Slide the KDJ11-E console/SLU panel assembly into the two open, adjacent I/O slots.
2. Mount the KDJ11-E console/SLU panel assembly into the two open, adjacent I/O slots.
3. Secure the console/SLU panel assembly by tightening the four captive screws provided in the upgrade kit.

Connect the Cables

NOTE
All cable connectors are keyed for ease of installation.

1. Connect one end of the APS cable to the connector on the APS module (M9714).
2. Connect the other end of the APS cable to J3 on the CPU module (M8981).
3. Connect one end of the 40-pin cable (17-02786-03) to J1 on the KDJ11-E CPU module (M8981).
4. Thread the other end of the 40-pin cable through to the console/SLU panel assembly on the rear of the cabinet.
5. Connect this 40-pin cable to J1 on the console/SLU panel assembly.

NOTE
One end of cable (17-02785-01) has a single 60-pin connector. The other end has a 60-pin connector with a 20-pin extension connector (Figure 8–21).

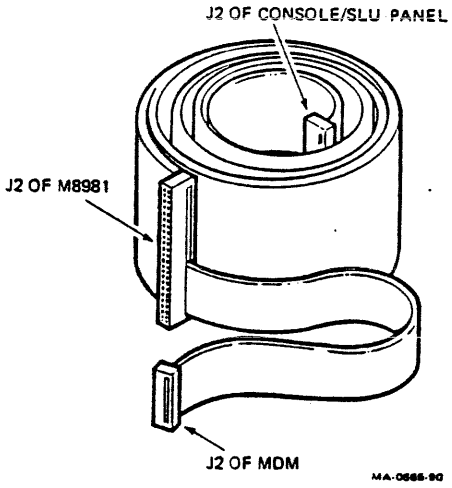


Figure 8–21 60-Pin Cable With 20-Pin Extension (17-02785-01)

6. Connect the end with the single 60-pin connector to J2 on the console/SLU panel assembly.
7. Connect the other 60-pin end to J2 of the CPU module (M8981).
8. Connect the 20-pin extension connector to J6 of the backplane.

Connect the Power

1. Replace the top cover.
2. Press in the slide hold lever and slide the system box into the cabinet (Figure 8–17).
3. Set the power supply circuit breaker to the up position to connect ac power.
4. Set the main controller circuit breaker to the up position to connect to ac power.
5. Replace the rear panel of the cabinet.
6. Use a four millimeter (5/32 inch) hex wrench and secure the panel fastener.
7. Push the stabilizer bar back under the system cabinet (Figure 8–15).
8. Connect the console terminal cable to the console port on the back of the console/SLU assembly.
9. Set the console/SLU switch pack according to the settings shown in Table 8–3 and Table 8–4.
10. Set the console terminal to eight data bits, no parity, and one stop bit.
11. Install the appropriate front panel label, provided in the upgrade kit, over the old front panel label.
12. Plug all ac power cords in the wall outlets.

Run Diagnostics

1. Turn the key on the keylock power switch on the front panel to the Enable position.
2. Execute test 30, **All Tests Selected**, for 5 passes. Refer to Section 6.3.1 for instructions.

You have now successfully completed the upgrade for the PDP-11/84-E systems.

A
Setup Parameters Worksheet

Two worksheets for each mode (video terminal or hardcopy) are provided for you to record the original setup parameter selections and the new setup parameters selections contained in the EEPROM of the KDJ11-E CPU module:

- Fill out the original worksheet when you install a KDJ11-E CPU module.
- Fill out the new worksheet when you change the parameter selections.

The information on these worksheets is used for programming any future replacement KDJ11-E CPU module.

Leave the worksheets with the system for future use.

Refer to Chapter 3, Operation for more information on setup.

A.1 Original Setup Menu Worksheet - Video Terminal Support

KDJ11-E Monitor Version 1.06

Licensed to Digital Equipment Corporation

Unibus System

Memory

EEprom

Time

Boot	Dev.	Unit	Address
1			
2			
3			
4			
5			
6			

Disable UBA ROM	Yes/No
Enable UBA 18-Bit Mode	Yes/No
Memory Intern	Do not change
Rom on 173000	Yes/No
Rom on 165000	Yes/No
Power up Mode	Rom/Auto/ODT/Trap 24
Restart Mode	Rom/Auto/ODT/Trap 24
Power-on Self-tests	Yes/No
Select Self-tests	Edit
User Boot	Edit
Alternate Boot Block	Yes/No
LTC Register	Yes/No
Force Clock Interrupt	Yes/No
Clock Frequency	PS/50Hz/60Hz/800Hz
Halt on Break	Yes/No
Trap on Halt	Yes/No
Ignore Battery	Yes/No
Lines on	176500/176600/DIS

Lines	Address / Vec	Baud	Data	Stop	Par
Line 1	/				
Line 2	/				
Line 3	/				
Line 4	/				
Line 5	/				
Line 6	/				
Line 7	/				

A.2 New Setup Menu Worksheet - Video Terminal Support

KDJ11-E Monitor Version 1.06		Disable UBA ROM	Yes/No
Licensed to Digital Equipment Corporation			
Unibus System		Enable UBA 18-Bit Mode	Yes/No
Memory		Memory Intern	Do not change
EEprom		Rom on 173000	Yes/No
Time		Rom on 165000	Yes/No
		Power up Mode	Rom/Auto/ODT/Trap 24
Boot Dev. Unit Address		Restart Mode	Rom/Auto/ODT/Trap 24
1		Power-on Self-tests	Yes/No.
		Select Self-tests	Edit
2		User Boot	Edit
3		Alternate Boot Block	Yes/No
		LTC Register	Yes/No
4		Force Clock Interrupt	Yes/No
5		Clock Frequency	PS/50Hz/60Hz/800Hz
		Halt on Break	Yes/No
6		Trap on Halt	Yes/No
		Ignore Battery	Yes/No
		Lines on	176500/176600/DIS

Lines	Address / Vec	Baud	Data	Stop	Par
Line 1	/				
Line 2	/				
Line 3	/				
Line 4	/				
Line 5	/				
Line 6	/				
Line 7	/				

A.3 Original Worksheet - Hard Copy Printer Support

```
KDJ11-E Monitor  Version 1.06 18-May-1990
(C) Digital Equipment Corporation 1990

A  Memory Intern                (0) =   2MB  (1) =   4MB      =

B  Rom on 173000                (0) =    No  (1) =   Yes      =

C  Rom on 165000                (0) =    No  (1) =   Yes      =

D  Power-up Mode                (0) = Dialog
                                (1) =   Odt
                                (2) = Trap24
                                (3) =  Auto                   =

E  Restart Mode                 (0) = Dialog
                                (1) =   Odt
                                (2) = Trab24
                                (3) =  Auto                   =

F  Power-on Self-tests          (0) =    No  (1) =   Yes      =

G  Alternate Boot Block         (0) =    No  (1) =   Yes      =

H  LTC Register                 (0) =    No  (1) =   Yes      =

I  Force Clock Interrupt        (0) =    No  (1) =   Yes      =

J  Clock Frequency              (0) =   P/S
                                (1) =  50Hz
                                (2) =  60Hz
                                (3) = 800Hz                   =

K  Halt on Break                (0) =    No  (1) =   Yes      =

L  Trap on Halt                 (0) =    No  (1) =   Yes      =

M  Ignore Battery               (0) =    No  (1) =   Yes      =

N  Lines on                     (0) =   DIS
                                (1) = 176500
                                (2) = 176600                  =

O  Disable UBA ROM              (0) =    No  (1) =   Yes      =

P  Enable UBA 18-Bit Mode        (0) =    No  (1) =   Yes      =
```

A.4 New Worksheet - Hard Copy Printer Support

```
KDJ11-E Monitor  Version 1.06 18-May-1990
(C) Digital Equipment Corporation 1990

A  Memory Intern                (0) =   2MB  (1) =   4MB      =

B  Rom on 173000                (0) =    No  (1) =   Yes      =

C  Rom on 165000                (0) =    No  (1) =   Yes      =

D  Power-up Mode                (0) = Dialog
                                (1) =   Odt
                                (2) = Trap24
                                (3) =  Auto                   =

E  Restart Mode                 (0) = Dialog
                                (1) =   Odt
                                (2) = Trab24
                                (3) =  Auto                   =

F  Power-on Self-tests          (0) =    No  (1) =   Yes      =

G  Alternate Boot Block         (0) =    No  (1) =   Yes      =

H  LTC Register                 (0) =    No  (1) =   Yes      =

I  Force Clock Interrupt        (0) =    No  (1) =   Yes      =

J  Clock Frequency              (0) =   P/S
                                (1) =  50Hz
                                (2) =  60Hz
                                (3) = 800Hz                   =

K  Halt on Break                (0) =    No  (1) =   Yes      =

L  Trap on Halt                 (0) =    No  (1) =   Yes      =

M  Ignore Battery               (0) =    No  (1) =   Yes      =

N  Lines on                     (0) =   DIS
                                (1) = 176500
                                (2) = 176600                  =

O  Disable UBA ROM              (0) =    No  (1) =   Yes      =

P  Enable UBA 18-Bit Mode       (0) =    No  (1) =   Yes      =
```

B
Backplane Pin Assignments

Figures B–1 through B–3 show the backplane pin assignments for the PDP-11/94-E systems.

Figure B–1 shows the SPC backplane pin assignments.

SIDE / PIN	ROW C 1	ROW C 2	ROW D 1	ROW D 2	ROW E 1	ROW E 2	ROW F 1	ROW F 2
A	NPG (IN)	+5V	TP	+5V	GND A	+5V	ABG OUT	+5V
B	NPG (OUT)	-15V	TP	-15V	ASSYN IN H	-15V	ABG IN	-15V
C	PA L	GND	A SEL 6	GND	A12 L	GND	SSYN L	GND
D	LTC	D15 L	A OUT LOW	BR7 L	A17 L	A15 L	BBSY L	FO1 N1
E	TP	D14 L	A SEL 4	BR6 L	MSYN L	A16 L	FO1 V2	D02 L
F	TP	D13 L	A SEL 0	BR5 L	A02 L	C1 L	D05 L	D06 L
H	D11 L	D12 L	A IN	BR4 L	A01 L	A00 L	D07 L	A INT ENB B
J	A INT B	D10 L	A SEL 2	A BR OUT	SSYN L	C0 L	NPR L	GND A
K	TP	D09 L	A OUT	BG7 SO	A14 L	A13 L	D08 L	A INT B
L	A INT ENBB	D08 L	INIT L	BG7 OUT	A11 L	TP	D03 L	FO1 L2
M	TP	D07 L	AINT ENBA	BG6 SO	AIN	AOUT HIGH	INTR L	FO1 M2
N	DC LO	D04 L	A INT A	BG6 OUT	A OUT LOW	A08 L	FO1 N1	D04 L
P	HALT REQ	D05 L	TP	BG5 SO	A10 L	A07 L	ABR OUT	FO1 P2
R	HALT GRT	D01 L	TP	BG5 OUT	A09 L	ASEL 4	FO1 L2	FO1 N1
S	PB L	D00 L	TP	BG4 SO	ASEL 6	ASEL 0	FO1 M2	FO1 P2
T	GND	D03 L	GND	BG4 OUT	GND	ASEL 2	GND	SACK L
U	+15	D02 L	TP	ABG IN	A06 L	A04 L	A INT A	ABR OUT
V	AC LO	D06 L	ASSYN IN H	ABG OUT	A05 L	A03 L	A INT ENB A	FO1 FO1

MR-16203
MA-1008-87

Figure B–1 SPC Backplane Pin Assignments

STANDARD UNIBUS
PIN DESIGNATIONS

Side / Pin	ROW A 1	ROW A 2	ROW B 1	ROW B 2
A	INIT L	+5V	BG6 H	+5V
B	INTR L	GND	BG5 H	GND
C	D00 L	GND	BR5 L	GND
D	D02 L	D01 L	GND	BR4 L
E	D04 L	D03 L	GND	BG4 H
F	D06 L	D05 L	AC LO L	DC LO L
H	D08 L	D07 L	A01 L	A00 L
J	D10 L	D09 L	A03 L	A02 L
K	D12 L	D11 L	A05 L	A04 L
L	D14 L	D13 L	A07 L	A06 L
M	PA L	D15 L	A09 L	A08 L
N	GND	PB L	A11 L	A10 L
P	GND	BBSY L	A13 L	A12 L
R	GND	SACK L	A15 L	A14 L
S	GND	NPR L	A17 L	A16 L
T	GND	BR7 L	GND	C1 L
U	NPG H	BR6 L	SSYN L	C0 L
V	BG7 H	GND	MSYN L	GND

MODIFIED UNIBUS
PIN DESIGNATIONS
(EXPANSION BACKPLANE)

SIDE / PIN	ROW A 1	ROW A 2	ROW B 1	ROW B 2
A	INIT L	+5V	RESV PIN	+5V
B	INTR L	TP	RESV PIN	TP
C	D00 L	GND	BR5 L	GND
D	D02 L	D01 L	+5 BAT	BR4 L
E	D04 L	D03 L	INT SSYN	PAR DET
F	D06 L	D05 L	AC LO L	DC LO L
H	D08 L	D07 L	A01 L	A00 L
J	D10 L	D09 L	A03 L	A02 L
K	D12 L	D11 L	A05 L	A04 L
L	D14 L	D13 L	A07 L	A06 L
M	PA L	D15 L	A09 L	A08 L
N	PAR P1	PB L	A11 L	A10 L
P	PAR P0	BBSY L	A13 L	A12 L
R	+15 BAT	SACK L	A15 L	A14 L
S	-15 BAT	NPR L	A17 L	A16 L
T	GND	BR7 L	GND	C1 L
U	+20 (CORE)	BR6 L	SSYN L	C0 L
V	+20 (CORE)	+20 (CORE)	MSYN L	-5 (CORE)

NOTE: ◪ INDICATES A REDESIGNATED PIN.

MR-16204
MA-1009-87

Figure B–2 Standard and Modified Backplane Pin Assignments

Figure B–3 shows the modified backplane pin assignments.

MODIFIED UNIBUS
PIN DESIGNATION
(SLOTS 7 AND 8)

	ROW A		ROW B	
SIDE / PIN	1	2	1	2
A	INIT L	+5V	RESV PIN	+5V
B	INTR L	TP	RESV PIN	TP
C	D00 L	GND	BR5 L	GND
D	D02 L	D01 L	+5.1 BAT	BR4 L
E	D04 L	D03 L	INT SSYN	PAR DET
F	D06 L	D05 L	AC LO L	DC LO L
H	D08 L	D07 L	A01 L	A00 L
J	D10 L	D09 L	A03 L	A02 L
K	D12 L	D11 L	A05 L	A04 L
L	D14 L	D13 L	A07 L	A06 L
M	PA L	D15 L	A09 L	A08 L
N	PAR P1	P8 L	A11 L	A10 L
P	PAR P0	BBSY L	A13 L	A12 L
R	+15 *	SACK L	A15 L	A14 L
S	-15 *	NPR L	A17 L	A16 L
T	GND	BR7 L	GND	C1 L
U	+20 **	BR6 L	SSYN L	C0 L
V	+20 **	+20 **	MSYN L	-5 **

* CONNECTED TO +15V AND -15V
NOT CONNECTED TO +(-) 15V BATTERY

** NO BACKPLANE CONNECTION; STANDALONE PINS
(DESIGNATED FOR CORE MEMORY)

MR-16204
MA-1009-87A

Figure B–3 Modified Backplane Pin Assignments

Table B–1 lists the modified Q22-bus backplane pin assignments.

Table B–1 Modified Q22-Bus Backplane Pin Assignments

Row A		Row B	
Pin	**Signal**	**Pin**	**Signal**
A1	BIRQ5 L—BR 5 L	A1	BDCOK H—DCLO L
A2	+5 V[1]	A2	+5 V[1]
B1	BIRQ6 L—BR6 L	B1	BPOK H/ ACLO L[2]
B2		B2	
C1	BDAL 16 L	C1	BDAL 18 L
C2	GND	C2	GND
D1	BDAL 17 L	D1	BDAL 19 L
D2	+12 V RESV	D2	
E1		E1	BDAL 20 L
E2	BDOUT L	E2	BDAL 02 L
F1	SRUN L/ S SPARE[3]	F1	BDAL 21 L
F2	BRPLY L	F2	BDAL 03 L
H1		H1	BOOT ENA L/ S SPARE[3]
H2	BDIN L	H2	BDAL 04 L
J1	GND	J1	GND
J2	BSYNC L	J2	BDAL 05 L
K1	MRESV A[4]	K1	MRESV B[5]
K2	BWTBT L	K2	BDAL 06 L
L1	MRESV A[4]	L1	MRESV B[5]
L2	BIRQ4 L—BR4 L	L2	BDAL 07 L
M1	GND	M1	GND
M2	BIAKI L	M2	BDAL 08 L
N1	BDMR L	N1	BSACK L
N2	BIAK0 L	N2	BDAL 09 L
P1	BHALT L	P1	BIRQ7 L—BR7 L
P2	BBS7 L	P2	BDAL 10 L
R1	BREF L	R1	BEVNT L—LTC
R2	BDMGI L	R2	BDAL 11 L
S1	VRESV	S1	

[1]Slots 2 and 3 pins AA2, BA2, and BV1 are only connected to +5.1 VB.

[2]BPOK is connected to slots 1 and 4. ACLO is connected to slots 2 and 3.

[3]SRUN and BOOT ENA are connected to slot 1 only. All other slots are S SPARE (standalone).

[4]MRESV A pins are wired together on each individual slot.

[5]MRESV B pins are wired together on each individual slot.

Table B–1 (Cont.) Modified Q22-Bus Backplane Pin Assignments

Row A		Row B	
Pin	**Signal**	**Pin**	**Signal**
S2	BDMG0 L	S2	BDAL 12 L
T1	GND	T1	GND
T2	BINIT L—INIT L	T2	BDAL 13 L
U1	+15 V / P SPARE[6]	U1	
U2	BDAL 00 L	U2	BDAL 14 L
V1[1]		V1	
V2	BDAL 01 L	V2	BDAL 15 L

[1]Slots 2 and 3 pins AA2, BA2, and BV1 are only connected to +5.1 VB.

[6]+15 V is connected to slot 1 only. All other slots are P SPARE (standalone).

Table B–2 lists the private memory interconnect backplane pin assignments.

Table B–2 Private Memory Interconnect Backplane Pin Assignments (Slots 1 to 3)

Row C		Row D	
Pin	**Signal**	**Pin**	**Signal**
A1		A1	
A2	+5 V*	A2	+5 V*
B1	PSSEL L	B1	PWTSTB L
B2		B2	
C1	SRUN L†	C1	PBYT L
C2	GND	C2	GND
D1	PUBMEM L	D1	PMAPE L
D2		D2	
E1	PBCYC L	E1	PRESV 3
E2		E2	
F1	PUBSYS L	F1	PRESV 4
F2		F2	
H1	PHBPAR L	H1	PRESV 5
H2		H2	
J1	PSBFUL L	J1	PRESV 6
J2		J2	

*Slots 2 and 3 pins CA2 and DA2 are connected to +5.1 VB only.

†SRUN L is connected to slot 1 only. It also connects to slot 1, AF1.

Table B–2 (Cont.) Private Memory Interconnect Backplane Pin Assignments (Slots 1 to 3)

Row C		Row D	
Pin	**Signal**	**Pin**	**Signal**
K1	PLBPAR L	K1	PRESV 7
K2		K2	
L1	CRESV 1	L1	
L2		L2	
M1	PRDSTB L	M1	PRESV B
M2		M2	
N1	PRESV 1	N1	CONSOLE LOCK L
N2		N2	
P1	PBLKM L	P1	PRESV 9
P2		P2	
R1	PBSY L	R1	PRESV 10
R2		R2	
S1	PRESV 2	S1	BBSY L
S2		S2	
T1	GND	T1	GND
T2		T2	
U1	CRESV 2	U1	+5 BRESV‡
U2		U2	+5 BRESV‡
V1	PUBTMO L	V1	+5 BRESV‡
V2		V2	+5 BRESV‡

‡+5 BRESV is a common connection between slots 2 and 3 only, with no external power connection.

Table B–3 lists the dedicated UBA backplane pin assignments.

Table B–3 Dedicated UBA Backplane Pin Assignments (Slot 4)

Row C		Row D		Row E		Row F	
Pin	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**
A1	BDMG0 L	A1	LTC	A1		A1	
A2	+5 V	A2	+5 V	A2	+5 V	A2	+5 V
B1	PSSEL L	B1	PWTSTB L	B1		B1	D11 L*
B2		B2	-15 V	B2		B2	

*Standard UNIBUS signal at the UBA

Table B–3 (Cont.) Dedicated UBA Backplane Pin Assignments (Slot 4)

Row C		Row D		Row E		Row F	
Pin	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**
C1	NPG OUT*	C1	PBYT L	C1		C1	SSYN L*
C2	GND	C2	GND	C2	GND	C2	GND
D1	PUBMEM L	D1	PMAPE L	D1	A17 L*	D1	D10 L*
D2		D2	BR7 L*	D2	A16 L*	D2	D09 L*
E1	PBCYC L	E1	PRESV 3	E1	A15 L*	E1	D08 L*
E2		E2	BR6 L*	E2	A14 L*	E2	D07 L*
F1	PUBSYS L	F1	PRESV 4	F1	MSYN L*	F1	D06 L*
F2		F2	BR5 L*	F2	C1 L*	F2	D05 L*
H1	PHBPAR L	H1	PRESV 5	H1		H1	D04 L*
H2		H2	BR4 L*	H2	A13 L*	H2	FP REBOOT L
J1	PSBFUL L	J1	PRESV 6	J1	A12 L*	J1	NPR L*
J2		J2	INIT L*	J2	C0 L*	J2	D03 L*
K1	PLBPAR L	K1	PRESV 7	K1	A11 L*	K1	D02 L*
K2		K2		K2	A10 L*	K2	D01 L*
L1	CRESV 1	L1		L1	A09 L*	L1	D00 L*
L2		L2	BG7 OUT*	L2	A08 L*	L2	
M1	PRDSTB L	M1	PRESV 8	M1	A07 L*	M1	INTR L*
M2		M2		M2	A06 L*	M2	
N1	PRESV 1	N1	CONSOLE LOK	N1	A05 L*	N1	SACK L*
N2		N2	BG6 OUT*	N2	A04 L*	N2	
P1	PBLKM L	P1	PRESV 9	P1	A03 L*	P1	
P2		P2		P2	A02 L*	P2	
R1	PBSY L	R1	PRESV 10	R1	A01 L*	R1	

*Standard UNIBUS signal at the UBA

Table B–3 (Cont.) Dedicated UBA Backplane Pin Assignments (Slot 4)

Row C		Row D		Row E		Row F	
Pin	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**
R2		R2	BG5 OUT*	R2	A00 L*	R2	
S1	PRESV 2	S1	BBSY L*	S1		S1	
S2		S2		S2	PA L*	S2	
T1	GND	T1	GND	T1	GND	T1	GND
T2		T2	BG4 OUT*	T2	PB L*	T2	
U1	+15 V	U1	DRESV 1	U1	D15 L*	U1	
U2		U2	DCLO L*	U2	D14 L*	U2	
V1	PUBTMO L	V1	DRESV 2	V1	D13 L*	V1	
V2		V2	ACLO L*	V2	D12 L*	V2	

*Standard UNIBUS signal at the UBA

C
Optional Battery Backup Unit

C.1 Installation

The optional battery backup unit (BBU) can be installed in a PDP-11X94-E or a PDP-11W94-E system (kit number H7231-J). This section describes how install the BBU for each system.

For detailed information on the BBU, refer to the *H7231A Battery Backup Unit User's Guide* (EK-H7231-UG).

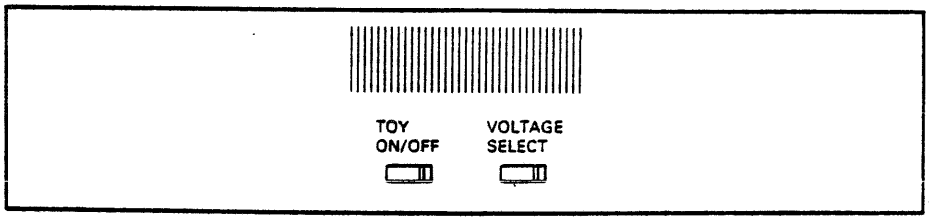
WARNING
The battery backup unit weighs 19 kg (42 lb). It is recommended that two people lift and position the unit.

C.1.1 PDP-11W94-E BBU Installation

To install the BBU in the PDP-11W94-E system:

1. Unpack the BBU installation kit (H7231-J).
2. Ensure that the installation kit contains the following:
   - One battery backup unit with casing
   - Two mounting brackets
   - Two hex nuts
   - Six Phillips screws
   - One signal cable (PN 17-00411-01)
   - One 300 V cable (PN 70-20396-6L)
   - One failsafe jumper
3. Remove the BBU from the shipping container and place the BBU on a flat surface.

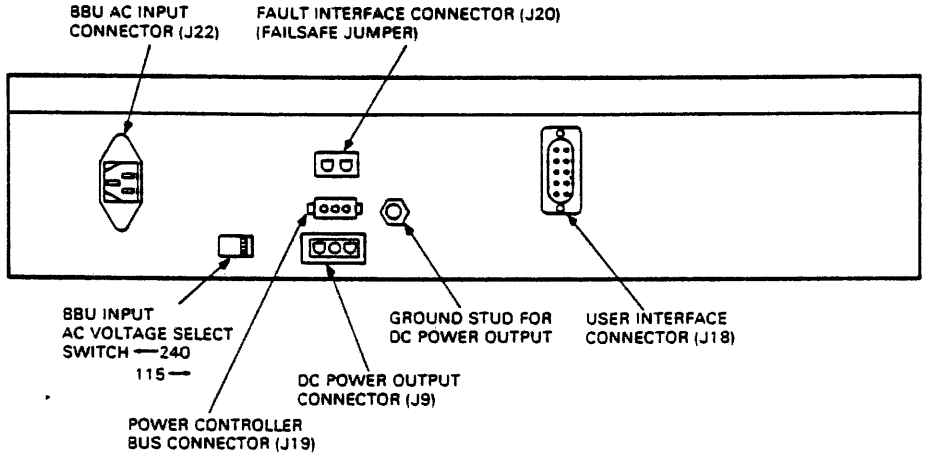
4. Set the front panel time-of-year switch to the off position (Figure C–1). You should see a zero on the switch.
5. Set the BBU voltage select switch to match the AC line voltage at the wall outlet (Figure C–1).



MR-15497
MA-0323.90

Figure C–1 Battery Backup Unit Front Panel

6. Set the rear BBU voltage select switch to match the front panel voltage select switch setting (Figure C–2).



MR-15498
MA-1846-87

Figure C–2 Battery Backup Unit Rear Panel

7. On the PDP-11W94-E cabinet:
   a. Turn the system keylock switch on the front panel to off.
   b. Use a 4 millimeter (5/32 inch) hex wrench to unlock the large rear panel and the single narrow vertical front panel.
   c. Remove both panels and set them aside.
   d. Turn the circuit breakers at the power supply and power controller units to off.
   e. Unplug the AC power cord from the wall outlet.
   f. Extend the cabinet stabilizer bar.
   g. Unlatch the CPU box release lever.
   h. Pull the CPU box forward to the service position.
   i. Remove the CPU box top cover.

8. To install the BBU in the PDP-11W94-E cabinet:

   a. Use the two Phillips screws (one for each bracket) to secure the mounting brackets to the cabinet outer frame. Remove the two screws (one for each bracket) from the cabinet inner frame (Figure C–3).

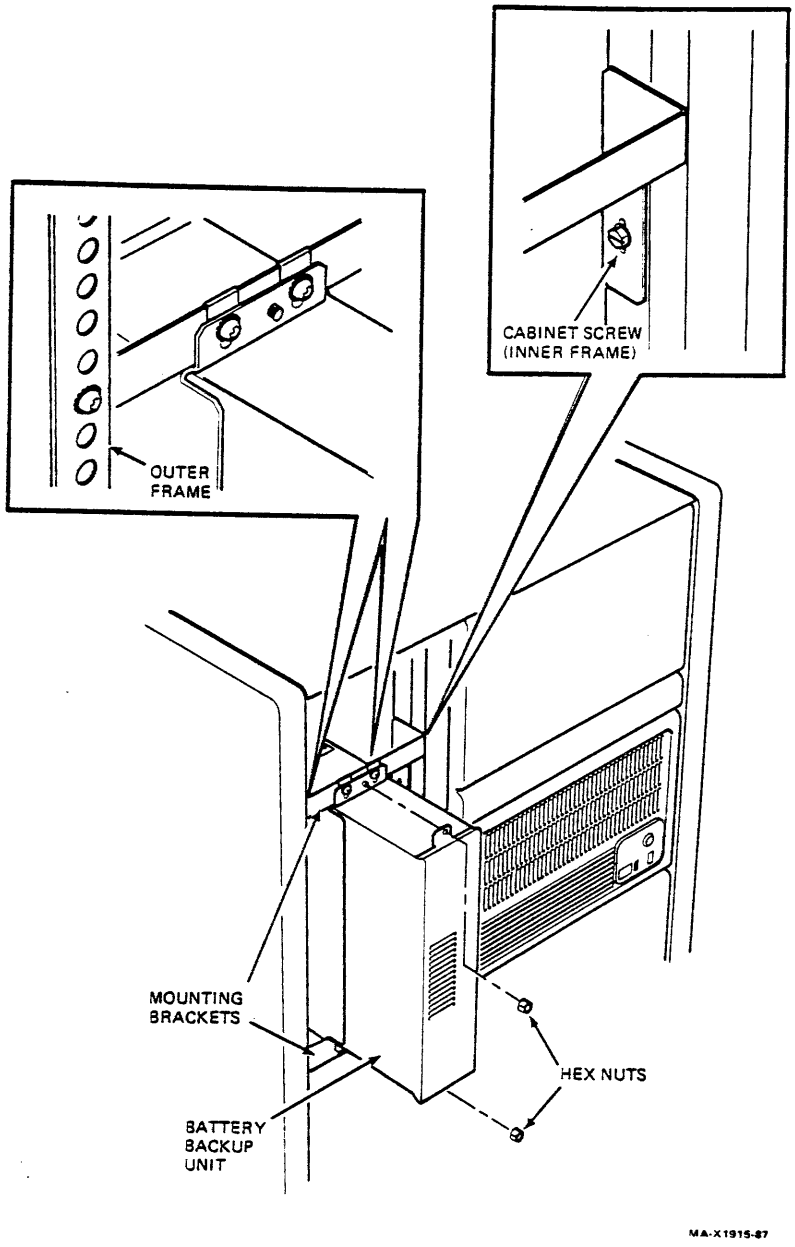


Figure C–3 Mounting the BBU in a PDP-11W94-E System

b. Align the holes in the brackets to the screw holes on the inner frame. Use the two previously removed screws to secure the brackets to the inner frame.

c. If the BBU is not removed, remove it from its casing.

d. Align the holes in the BBU casing with the holes in the two brackets.

e. Secure the casing to the mounting brackets with four Phillips screws from the kit.

f. Lift and position the BBU at the casing. Slide the BBU into the casing.

g. Use the two hex nuts to secure the BBU to the casing.

WARNING
The BBU weighs 19 kg (42 lb). Use two people to lift and position the BBU.

h. Install the 2-position keyed failsafe jumper into mating connector J20 on the BBU rear panel (Figure C–2).

i. Plug one end of the keyed 300 V cable (PN 70-20396-6L) with ground wire into mating connector J9 on the BBU rear panel.

j. Remove the hex nut on the BBU ground stud. Place the ground wire from the 300 V cable on the stud, and secure the ground wire with the hex nut.

k. Plug the other end of the 300 V cable into connector P13 (top connector) at the rear of the power supply at the CPU box. Use the hex nut to secure the cable ground wire to the power supply ground stud.

l. Plug the signal cable (PN 17-00411-01) into mating connector J18 on the BBU rear panel.

m. Feed the signal cable to the CPU box (under the cable holder) and connect the signal cable to connector J10 on the power distribution board. Connect the cable ground wire to the CPU box chassis (Figure C–4).

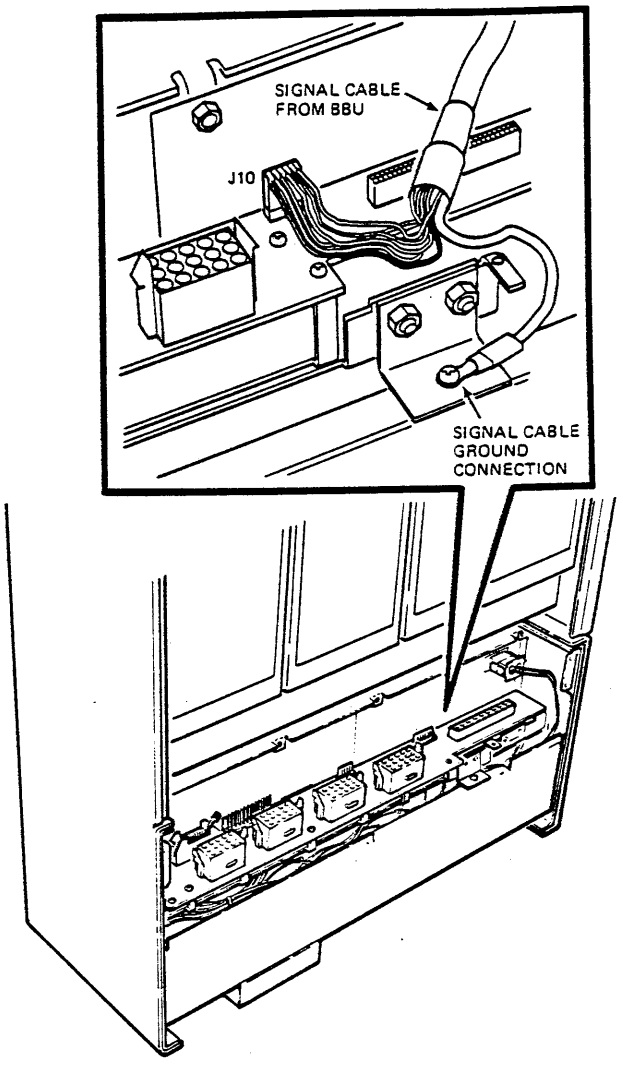


Figure C–4 Signal Cable Connection at CPU Box

n. Plug the BBU AC power cord into mating connector J22 on the rear of the unit.

o. Plug the other end of the BBU power cord into the *unswitched* outlet on the power controller unit.

9. Ensure that all cables are routed away from sharp edges and secured with cable holders.

10. Reinstall the CPU box top cover.

11. Push in on the CPU box until it latches in place.

12. Position the circuit breakers on the power supply and power controller units to the on position.

13. Reinstall the large rear panel and the single narrow vertical front panel.

14. Plug the system AC power cord into the wall outlet.

C.1.2 PDP-11X94-E Installation

To install the BBU in the PDP-11X94-E system:

1. Unpack the BBU installation kit (H7231-H).
2. Ensure that the installation kit contains:
   - One battery backup unit with casing
   - Eight U-nuts
   - Two hex nuts
   - Eight Phillips screws
   - One signal cable (PN 17-00411-01)
   - One 300 V cable (PN 70-20396-6L)
   - One failsafe jumper
3. Remove the BBU from the shipping container and place it on a flat surface.
4. Set the front panel time-of-year switch to the off position (Figure C–1). You should see a zero on the switch.
5. Set the BBU voltage select switch to match the AC line voltage at the wall outlet (Figure C–1).
6. Set the rear BBU voltage select switch to match the front panel voltage select switch setting (Figure C–2).
7. On the PDP-11X94-E cabinet:
   a. Turn system keylock switch on the front panel to off.
   b. Unlock the rear panel (using a 4 millimeter [5/32] inch hex wrench) and the bottom front panel (below the CPU box).
   c. Remove both panels and set them aside.
   d. Turn the circuit breakers at the power supply and power controller units to off.
   e. Unplug the AC power cord from the wall outlet.
   f. Extend the cabinet stabilizer bar.
8. To install the BBU in the PDP-11X94-E cabinet:
   a. Place the eight U-nuts over the holes in the cabinet frame under the CPU box.
   b. If the BBU is not removed, remove it from its casing.
   c. Align the holes in the BBU casing with the holes in the frame (with U-nuts).

d. Use four Phillips screws to secure the casing to the cabinet frame (side). Use the other four Phillips screws to secure the casing to the front of the frame (Figure C–5).

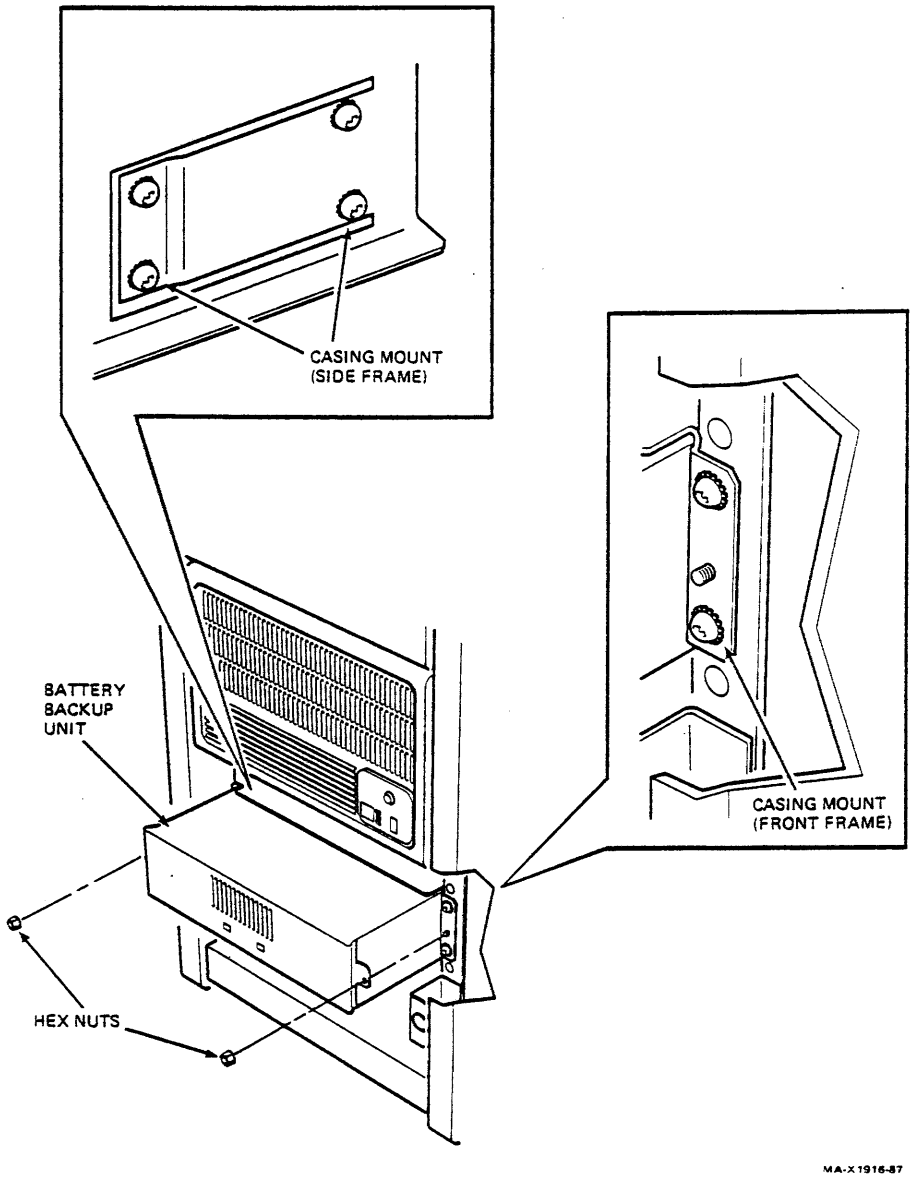


Figure C–5 Mounting the BBU in a PDP-11X94-E System

e. Lift and position the BBU at the casing. Slide the BBU into the casing.

f. Use the two hex nuts to secure the BBU to the casing.

WARNING
The BBU weighs 19 kg (42 lb). Use two people to lift and position the BBU.

g. Unlatch the CPU box release lever.

h. Pull the CPU box forward to the service position.

i. Remove the CPU box top cover.

j. Install the 2-position keyed failsafe jumper into mating connector J20 on the BBU rear panel (Figure C–2).

k. Plug one end of the keyed 300 V cable (PN 70-20396-6L) with ground wire into mating connector J9 on the BBU rear panel.

l. Remove the hex nut on the BBU ground stud. Place the ground wire from the 300 V cable on the stud, and secure the ground wire with the hex nut.

m. Plug the other end of the 300 V cable into connector P13 (top connector) at the rear of the power supply (at the CPU box). Using the hex nut, secure the cable ground wire to the power supply ground stud.

n. Plug the signal cable (PN 17-00411-01) into mating connector J18 on the BBU rear panel.

o. Feed the signal cable to the CPU box (under the cable holder) and connect the signal wire to connector J10 on the power distribution board. Connect the cable ground wire to the CPU box chassis (Figure C–4).

p. Plug the BBU AC power cord into mating connector J22 on the rear of unit.

q. Plug the other end of the BBU power cord into the *unswitched* outlet on the power controller unit.

9. Ensure that all cables are routed away from sharp edges and secured with cable holders.
10. Reinstall the CPU box top cover.
11. Push in on the CPU box until it latches into place.
12. Position the circuit breakers on the power supply and power controller units to the on position.
13. Reinstall the rear panel and the front bottom panel.
14. Plug the system AC power cord into the wall outlet.

C.1.3 Testing the Battery Backup

To ensure that the BBU is functioning properly:

1. Select the Setup Menu at the terminal.
2. Set Ignore Battery to No.
3. Set Powerup Mode to Trap 24.
4. Disable forced dialog (S5 off).
5. Save all the Set-Up parameters.
6. Run DECX11.
7. *While DECX11 is running*, set the power controller circuit breaker to off.
8. Leave the circuit breaker off for a minimum of 10 seconds. Check that the battery indicator on the front panel is flashing fast, indicating that the battery is discharging.
9. Set the circuit breaker to on. DECX11 should resume running, indicating that the BBU is functioning properly.

D

PDP-11/94 Hardware/Software Differences

D.1 UNIBUS Power-up Protocol Differences

The UNIBUS power-up protocol on PDP-11/94 systems is slightly different than on most PDP-11 systems (see Figure D–1). With most PDP-11 systems, the UNIBUS signal INITIALIZE (INIT) L is held asserted for a minimum of 10 milliseconds after the negation of DC LINE LOW (DC LO L) on power-up. However, on PDP-11/94 systems the UNIBUS signal INIT L is held asserted for a minimum of 16 microseconds after the negation of DC LO L on power-up. This difference will not affect system operations.

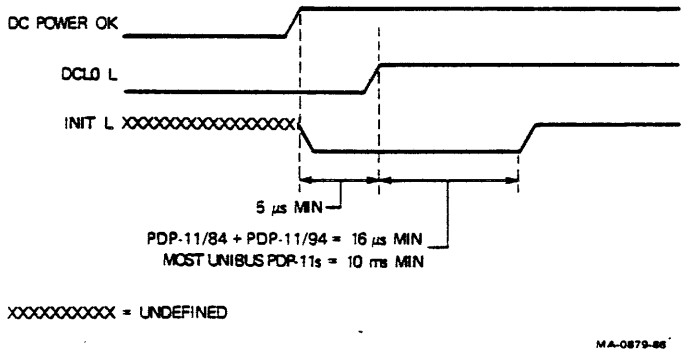


Figure D–1 Power-Up Protocol Timing Differences

D.2 PDP-11/94 and PDP-11/84 Hardware Differences

Onboard Main Memory

The PDP-11/94 main memory resides on the KDJ11-E CPU module for increased system speed and reliability. External memory modules used in the PDP-11/84 are no longer required.

The KDJ11-E main memory is available in two capacities:

KDJ11-EA (M8981-AA)	2Mb memory module.
KDJ11-EB (M8981-BA)	4Mb memory module.

Terminal Support

The KDJ11-E provides two modes of terminal support:

- Hard Copy Mode (line edit)
- Soft Copy Mode (video terminal)

Cache Memory

The KDJ11-E does not implement cache memory because the on-board parity memory acts as a cache memory with a 100% hit rate.

Eight Serial Line Units (SLUs)

Eight on-board SLUs are present on the PDP-11/94. One is used as the console. The following features are standard on the remaining seven SLUs:

- Programmable baud rate, stop bits and parity.
- Error detection for incoming characters.
- Five character silo prevents overrun errors.

Time of Year Clock (TOY)

The KDJ11-E incorporates a TOY clock with an on-board lithium battery backup. The clock provides:

- Hundredths of seconds
- Seconds
- Minutes
- Hours
- Day of week
- Month
- Year

Adjustments for months with less than 31 days and leap year are automatic. The time and date can be set from dialog mode.

Self-Test

The KDJ11-E contains an extensive set of self-tests. The on-board diagnostics tests the:

- CPU
- Memory management unit
- Memory
- Serial Line Units
- Console/SLU bulkhead through turnaround
- UNIBUS adapter
- UNIBUS signals

Register Differences

Table D–1 summarizes the hardware differences between products based on the PDP-11/84 and products based on the PDP-11/94.

Table D–1 Register Differences

Register	PDP-11/94	PDP-11/84
17770200 to 17770376	UNIBUS Map Register Pairs	No difference.
17772100	Parity Memory CSR	ECC Control and Status Register.
17772200 to 17772276	Supervisor I and D PDR/PAR's	No difference.
17772300 to 17772376	Kernel I and D PDR/PAR's	No difference.
17772516	MMR3	No difference.
17776500 to 1776566	Serial Line Units 0-6 New feature.	Not present.
17777520	Control Status Register	Control Status Register.
	Present but not used.	Present and used. The following register bit definitions are implemented: • CSR Bit 8 SA Mode • CSR Bit 2 PMG CNT2 • CSR Bit 1 PMG CNT1 • CSR Bit 0 PMG CNT0
17777522	Page Control Register. See Chapter 5. PCR Bit 15 and PCR Bit 7 are implemented.	Page Control Register. PCR Bit 15 and PCR Bit 17 are not implemented.
17777524	Configuration and Display Register	No difference.
17777526	Additional Status Register The following bit definitions are implemented: • ASR Bits 13:12 SLU address/vector selection. • ASR Bit 8 TOY Clock. • ASR Bits 05:04 On-board memory select. • ASR Bit 1 PMI cycle.	Not present.
17777546	Line Clock Register	No difference.
17777560	Console SLU Receiver Status Register RSR Bit 12 Receiver Active is not implemented.	Console SLU Receiver Status Register RSR Bit 12 Receiver Active is implemented.
17777562	Console SLU Receiver Data Buffer RDB Bit 11 Received Break is not implemented.	Console SLU Receiver Data Buffer Bit definition RDB Bit 12 Receiver Parity Error is not implemented.

Table D–1 (Cont.) Register Differences

Register	PDP-11/94	PDP-11/84
17777564	Console SLU Transmitter Status Register TSR Bit 2 Maintenance is not implemented.	Console SLU Transmitter Status Register Bit definition TSR Bit 2 Maintenance is implemented.
17777566	Console SLU Transmitter Data Buffer	No difference.
17777572	Memory Management Register 0	No difference.
17777574	Memory Management Register 1	No difference.
17777576	Memory Management Register 2	No difference.
17777600 - 17777676	User I and D PDR/PAR's	No difference.
17777730	Diagnostic Controller Status Register	No difference.
17777732	Diagnostic Data Register	No difference.
17777734	Memory Configuration Register Does not use MCR bits 04:00 (UNIBUS memory size), Bit 06 (cache enable) MUST be zero, Bit 08 (Select Status) is not used, and bits 09:15 (DMA Cache Status Bits) are not used.	Memory Configuration Register All bits are used.
17777744	Memory System Error Register The following bits: • MSER CSR Bit 4 Cache DMA Tag Parity Error. • MSER CSR Bit 5 Cache CPU Tag Parity Error. • MSER CSR Bit 6 Cache LB Data Parity Error. • MSER CSR Bit 7 Cache HB Data Parity Error. • MSER CSR Bit 13 DTS PAR. • MSER CSR Bit 14 DTS CMP. • MSER CSR Bit 15 CPU Abort is different. The Main memory parity errors results in an abort.	Memory System Error Register. The following bits are implemented: • MSER CSR Bit 4 Cache DMA Tag Parity Error. • MSER CSR Bit 5 Cache CPU Tag Parity Error. • MSER CSR Bit 6 Cache LB Data Parity Error. • MSER CSR Bit 7 Cache HB Data Parity Error. • MSER CSR Bit 13 DTS PAR. • MSER CSR Bit 14 DTS CMP. • MSER CSR Bit 15 CPU Abort is different. The Main memory and cache parity errors result in an abort.
17777750	Maintenance Register Module ID Bits 07:04 = 0101 (5).	Maintenance Register Module ID Bits 07:04 = 0010 (2).
17777752	Hit/Miss Register Bits 05:00 Cache Hit are not implemented.	Hit/Miss Register Bit definitions 05:00 Cache Hit are implemented.
17777766	CPU Error Register	No difference.
17777772	Program Interrupt Request Register.	No difference.
17777776	Processor Status Word	No difference.

D.3 Software Differences

Table D–2 summarizes the programming differences, at the assembly language level, between the DCJ11 and other processors in the PDP-11 family.

Table D–2 Programming Difference for PDP-11 Family Processors

Item	Processors 23/24	44	04	34	LSI-11	05/10	15/20	35/40	45	70	60	J-11	T-11	VAX
1. OPR %R, (R) +; OPR %R, - (R) using the same register as both source and destination: contents of R are incremented (decremented) by 2 before being used as the source operand.	x						x	x			x	x	x	
OPR %R, (R) +: OPR %R, - (R) using the same register as both register and destination: initial contents of R are used as the source operand.		x	x	x	x	x			x	x				x
2. OPR %R, @(R) +; OPR %R, @ - (R) using the same register as both source and destination: contents of R are incremented (decremented) by 2 before being used as the source operand.	x						x	x			x	x	x	
OPR %R, @ (R) +; OPR %R, @ - (R) using the same register as both source and destination: initial contents of R are used as the source operand.		x	x	x	x	x			x	x				x
3. OPR PC, X (R); OPR PC, @ X (R); OPR PC, @ A; location A will contain the PC of OPR +4.	x						x	x			x	x	x	
OPR PC, X (R); OPR PC, @ X (R), OPR PC, A; OPR PC, @ A: location A will contain the PC of OPR +2.		x	x	x	x	x			x	x				x
4. JMP (R) + or JSR reg, (R) +: contents of R are incremented by 2, then used as the new PC address.						x	x							
JMP (R) + or JSR reg, (R) +: initial contents of R are used as the new PC.	x	x	x	x	x			x	x	x	x	x	x	x

Table D–2 (Cont.) Programming Difference for PDP-11 Family Processors

Item	Processors 23/24	44	04	34	LSI-11	05/10	15/20	35/40	45	70	60	J-11	T-11	VAX
5. JMP %R or JSR reg. %R traps to 10 (illegal instruction).	X		X	X	X	X	X	X			X		X	NA
JMP %R or JSR reg. %R traps to 4 (illegal instruction).		X							X	X		X		NA
6. SWAB does not change V.							X							
SWAB clears V.	X	X	X	X		X	X		X	X	X	X	X	X	X
7. Register addresses (177700-177717) are valid program addresses when used by CPU.						X							1	1
Register addresses (177700-177717) time out when used as a program address by the CPU. Can be addressed under console operation.		X	X	X			X	X	X	X	X				NA
Register addresses (177700-177717) time out when used as an address by CPU or console.	X				X							X		
8. Basic instructions noted in PDP-11 processor handbook.	X	X	X	X	X	X	X	X	X	X	X	X	X	X
SOB, MAR, RTT, SXT instructions[2]	X	X		X	X			X	X	X	X	X	X	3
ASH, ASHC, DIV, MUL, XOR	X	X		X	X			X	X	X	X	X		X
Floating Point Instructions in base machine.											X	X		
MFPT Instruction	X	X										X		
The external option KE11-A provides MUL, DIV, SHIFT operation in the same data format.						X	X							
The KE11-E (Expansion Instruction Set) provides the instructions MUL, DIV, ASH, and ASHC. These new instructions are 11/45 compatible.								X						

[1]Register addresses (177700-177717) are handled as regular memory addresses in the I/O page.

[2]RTT instruction is available in 11/04 but is different than other implementations.

[3]All but MARK.

Table D–2 (Cont.) Programming Difference for PDP-11 Family Processors

Item	Processors 23/24	44	04	34	LSI-11	05/10	15/20	35/40	45	70	60	J-11	T-11	VAX
The KE11-F (Floating Instruction Set) adds unique stack ordered oriented point instructions: FADD, FSUB, FMUL, FDIV.								x						
The KEV-11 adds EIS/FIS instructions					x									
MFP, MTP instructions	x	x		x				x		x	x	x		
SPL Instruction		x							x	x		x		
CSM Instruction		x										x		
9. Power fail during RESET instruction is not recognized until after the instruction is finished (70 milliseconds). RESET instruction consists of 70 millisecond pause with INIT occurring during first 20 milliseconds.							x	x			x			
Power fail immediately ends the RESET instruction and traps if an INIT is in progress. A minimum INIT of 1 microsecond occurs if instruction aborted. PDP-11-04/34/44 are similar with no minimum INIT time.		x	x	x					x	x				
Power fail acts the same as 11/45 (22 milliseconds with about 300 nanoseconds minimum). Power fail during RESET fetch is fatal with no power-down sequence.						x								
RESET instruction consists of 10 microseconds of INIT followed by a 90 microsecond pause. Reset instruction consists of a minimum 8.4 microseconds followed by a minimum 100 nanosecond pause. Power fail not recognized until the instruction completes.	x				x							x		
10. No RTT instruction						x	x							
If RTT sets the "T" bit, the "T" bit trap occurs after the instruction following RTT.	x	x	x	x	x			x	x	x	x	x	x	x

Table D–2 (Cont.) Programming Difference for PDP-11 Family Processors

Item	Processors 23/24	44	04	34	LSI-11	05/10	15/20	35/40	45	70	60	J-11	T-11	VAX
11. If RT1 sets "T" bit, "T" bit trap is acknowledged after instruction following RT1.						x	x							x
If RT1 sets "T" bit, "T" bit trap is acknowledged immediately following RT1.	x	x	x	x	x			x	x	x	x	x	x	
12. If an interrupt occurs during an instruction that has the "T" bit set, the "T" bit trap is acknowledged before the interrupt.	x	x	x	x	x	x	x	x			x	x	x	[4]
If an interrupt occurs during an instruction and the "T" bit is set, the interrupt is acknowledged before "T" bit trap.									x	x				NA
13. "T" bit trap will sequence out of WAIT instruction.	x	x	x	x		x	x	x			x		x	NA
"T" bit trap will not sequence out of WAIT instruction. Waits until an interrupt.					x				x	x				
14. Explicit reference (direct access) to PS can load "T" bit. Console can also load "T" bit.			x			x	x							
Only implicit references (RT1, RTT, traps and interrupts) can load "T" bit. Console cannot load "T" bit.	x	x		x	x			x	x	x	x	x	x	x
15. Odd address/ nonexistent references using the SP cause a HALT. This is a case of double bus error with the second error occurring in the trap servicing the first error. Odd address trap not implemented in LS1-11, 11/23 or 11/24.		x	x	x	x	x	x							
Odd address/nonexistent references using the stack pointer cause a fatal trap. On bus error in trap service, new stack created at 0/2.	x							x	x	x	x	x	[5]	[6]

[4]Interrupts not visible to VAX compatibility mode.

[5]Odd address/nonexistent references using SP do not trap.

[6]Odd address aborts to native mode.

Table D–2 (Cont.) Programming Difference for PDP-11 Family Processors

Item	Processors 23/24	44	04	34	LSI-11	05/10	15/20	35/40	45	70	60	J-11	T-11	VAX
16. The first instruction in an interrupt routine will not be executed if another interrupt occurs at a higher priority level than assumed by the first interrupt.	x	x	x	x	x	x		x	x	x	x	x	x	x
The first interrupt in an interrupt service is guaranteed to be executed.							x							
17. Single general purpose register set implemented.	x	x	x	x	x	x	x	x			x		x	x
Dual general purpose register set implemented.									x	x		x		
18. PSW address. 177776. not implemented; must use instructions MTPS (move to PS) and MFPS (move from PS).					x								x	[7]
PSW address implemented. MTPS and MFPS not implemented.		x	x			x	x	x	x	x	x			
PSW address and MTPS and MFPS implemented.	x			x								x		
19. Only one interrupt level (BR4) exists.					x									
Four interrupt levels exist.	x	x	x	x		x	x	x	x	x	x	x	x	NA
20. Stack overflow not implemented.					x								x	x
Some sort of stack overflow implemented.	x	x	x	x		x	x	x	x	x	x	x		
21. Odd address trap not implemented.	x				x								x	
Odd address trap implemented.		x	x	x		x	x	x	x	x	x	x		x
22. FMUL and FDIV instructions implicitly use R6 (one push and pop); hence R6 must be set up correctly.				x										
FMUL and FDIV instructions do not implicitly use R6.								x						NA

[7] Can reference PSW only from native mode.

Table D–2 (Cont.) Programming Difference for PDP-11 Family Processors

Item	Processors 23/24	44	04	34	LSI-11	05/10	15/20	35/40	45	70	60	J-11	T-11	VAX
23. Due to their execution time. EIS instructions can abort because of a device interrupt.					X									X
EIS instructions do not abort because of a device interrupt.	X	X		X				X		X	X	X	X	NA
24. Due to their execution time. FIS instructions can abort because of a device interrupt.					X			X						NA
25. Due to their execution time. FP11 instructions can abort because of a device interrupt.[8]	X													
FP11 instructions do not abort because of a device interrupt.		X		X					X	X	X	X		NA
26. EIS instructions do a DATIP and DATO bus sequence when fetching source operand.					X									
EIS instructions do a DATI bus sequence when fetching source operand.	X	X		X				X	X	X	X	X		NA
27. MOV instruction does just a DATO bus sequence for the last memory cycle.	X	X		X	X			X	X	X	X	X		9
MOV instruction does a DATIP and DATO bus sequence for the last memory cycle.			X			X	X						10	
28. If PC contains nonexistent memory and a bus error occurs. PC will have been incremented.	X	X	X	X	X	X	X		X	X		X		
If PC contains nonexistent memory address and a bus error occurs. PC will be unchanged.								X					11	X
29. If register contains nonexistent memory address in mode 2 and a bus error occurs. register will be incremented.	X				X	X	X	X	X	X		X	11	

[8]Integral floating point assumed on 11/23 and 11/24, FP11E assumed on 11/60.

[9]Implementation dependent.

[10]MOV instruction does a DATI and a DATO bus sequence for last memory cycle.

[11]Does not support bus errors.

Table D–2 (Cont.) Programming Difference for PDP-11 Family Processors

Item	Processors 23/24	44	04	34	LSI-11	05/10	15/20	35/40	45	70	60	J-11	T-11	VAX
Same as above but register is unchanged.		X	X	X										
30. If register contains an odd value in mode 2 and a bus error occurs, register will be incremented.	X				X			X	X	X		X	[11]	[12]
If register contains an odd value in mode 2 and a bus error occurs, register will be unchanged.		X	X	X		X	X							
31. Condition codes restored to original values after FIS interrupt abort (EIS doesn't abort on 35/40).							X							
Condition codes that are restored after EIS/FIS interrupt abort are indeterminate.					X									NA
32. Opcodes 075040 through 075377 unconditionally trap to 10 as reserved opcodes.	X	X	X	X	X	X	X	X	X	X	X	X	X	[13]
If KEV-11 option is present, opcodes 75040 through 07533 perform a memory read using the register specified by the low order 3 bits as a pointer. If the register contents is a nonexistent address, a trap to 4 occurs. If the register contents is an existent address, a trap to 10 occurs.					X									
33. Opcodes 210 through 217 trap to 10 as reserved instructions.	X	X	X	X		X	X	X	X	X	X	X	X	[13]
Opcodes 210 through 217 are used as a maintenance instruction.					X									
34. Opcodes 75040 through 75777 trap to 10 as reserved instructions.	X	X	X	X		X	X	X	X	X	X	X	X	[11]

[11] Does not support bus errors.

[12] Unpredictable.

[13] Traps to native mode.

Table D–2 (Cont.) Programming Difference for PDP-11 Family Processors

Item	Processors 23/24	44	04	34	LSI-11	05/10	15/20	35/40	45	70	60	J-11	T-11	VAX
If KEV-11 option is present, opcodes 75040 through 75577 can be used as escapes to user microcode. If no user microcode exists, a trap to 10 occurs.					x									
35. Opcodes 170000 through 177777 trap to 10 as reserved instructions.			x			x	x	x					x	11
Opcodes 170000 through 177777 are implemented as floating point instructions.	x	x		x					x	x	x	x		
Opcodes 170000 through 177777 can be used as escapes to user microcode. If no user microcode exists, a trap to 10 occurs.					x									
Opcode 076600 used for maintenance.														
36. CLR and SXT do just a DATO sequence for the last bus cycle.	x											x		12
CLR and SXT do DATIP-DATO sequence for the last bus cycle.		x	x	x	x	x	x	x	x	x	x		14	
37. MEM MGT maintenance mode MMR0 bit 8 is implemented.		x		x				x	x	x	x			
MEM MGT maintenance mode MMR0 bit 8 is not implemented.	x											x		NA
38. PS<15:12>, nonkernel mode, nonkernel stack pointer and MTPx and MFPx instructions exist even when MEM MGT is not configured.	x	x							x	x	x	x		
PS<15:12>, nonkernel mode, nonkernel stack pointer, and MTPx and MFPx instructions exist only when MEM MGT is configured.								x						NA

[11]Does not support bus errors.

[12]Unpredictable.

[14]CLR and SXT do DATI-DATO.

Table D–2 (Cont.) Programming Difference for PDP-11 Family Processors

Item	Processors 23/24	44	04	34	LSI-11	05/10	15/20	35/40	45	70	60	J-11	T-11	VAX
39. Current mode PS bits <15:14> set to 01 or 10 will cause a MEM MGT trap upon any memory reference.	X		X					X						
Current mode PS bits <15:14> set to 10 will be treated as kernel mode (00) and not cause a MEM MGT trap.	X													NA
Current mode PS bits <15:14> set to 10 will cause a MEM MGT trap upon any memory reference.		X							X	X		X		
40. MTPS in user mode will cause MEM MGT trap if PS address 177776 not mapped. If mapped, PS <7:5> and <3:0> affected.			X											
MTPS in nonuser mode will not cause MEM MGT trap and will only affect PS <3:0> regardless of whether PS address 177776 is mapped.	X											X		NA
41. MFPS in user mode will cause MEM MGT if PS address 177776 not mapped. If mapped, PS <7:0> are accessed.			X											
MTPS in user mode will not trap regardless of whether PS address 177776 is mapped.	X											X		NA
42. Programs cannot execute out of internal processor registers.												X		
Programs can execute out of internal processor registers.	X	X	X					X	X	X	X			
43. A HALT instruction in user or supervisor mode will trap through location 4.		X							X	X		X		
A HALT instruction in user or supervisor mode will trap through location 10.	X		X					X			X		13	15

[13]Traps to native mode.

[15]HALT pushes PC and PSW to stack, loads PS with 340 and PC with <powerup address> +40.

Table D–2 (Cont.) Programming Difference for PDP-11 Family Processors

Item	Processors 23/24	44	04	34	LSI-11	05/10	15/20	35/40	45	70	60	J-11	T-11	VAX
44. PDR bit <0> implemented.									x	x				
PDR bit <0> not implemented.	x	x	x					x			x	x	x	x
45. PDR bit <7> (any access) implemented.									x	x				
PDR bit <7> (any access) not implemented.	x	x	x					x			x	x	x	x
46. Full PAR <15:0> implemented.	x	x								x		x		
Only PAR <11:0> implemented.			x					x	x		x		x	x
47. MMR0 <12> - trap-memory management implemented.									x	x				
MMR0 <12> not implemented.	x	x	x					x			x	x	x	x
48. MMR3 <2:0> - D space enable implemented.		x							x	x		x		
MMR3 <2:0> not implemented.	x		x					x			x		x	x
49. MMR3 <5:4> - IOMAP, 22-bit mapping enabled implemented.	x	x								x		x		
MMR3 <5:4> not implemented.			x					x	x		x		x	x
50. MMR3 <3> - CSM enable implemented.		x										x		
MMR3 <3> not implemented.	x		x					x	x	x	x		x	x
51. MMR2 tracks instruction fetches and interrupt vectors.									x	x				
MMR2 tracks only instruction fetches.	x	x	x					x			x	x	NA	NA

Table D–2 (Cont.) Programming Difference for PDP-11 Family Processors

Item	Processors 23/24	44	04	34	LSI-11	05/10	15/20	35/40	45	70	60	J-11	T-11	VAX
52. MFPx %6, MTPx when PS <13:12> = 10 gives unpredictable results.	X	X	X					X	X	X	X			
MTPx %6, MTPx %6 when PS <13:12> = 10 uses user stack pointer.												X	NA	NA
55. The ASH instruction with a source operand of octal 37 (shift left 31 decimal times) causes the register to be shifted right instead of left.												X		
56. The ASHC instruction with an octal value of 37 (shift left 31 decimal times) in source operand bits <5:0> and bits <15:6> of the operand being nonzero, causes the register to be shifted right instead of left.												X		

E
Optional Expander Cabinet

E.1 Installation

To add a shielded (FCC-compliant) H9642 expander cabinet to a PDP-11X94-E or PDP-11W94-E CPU cabinet:

1. Move the expansion cabinet next to the CPU cabinet.
2. On the expansion and CPU cabinets:
   a. Unlock the rear panels, using a 4 millimeters (5/32 inch) hex wrench to release the two panel fasteners of each cabinet and the single narrow vertical panel (PDP-11W94-E only) (Figure E–1).

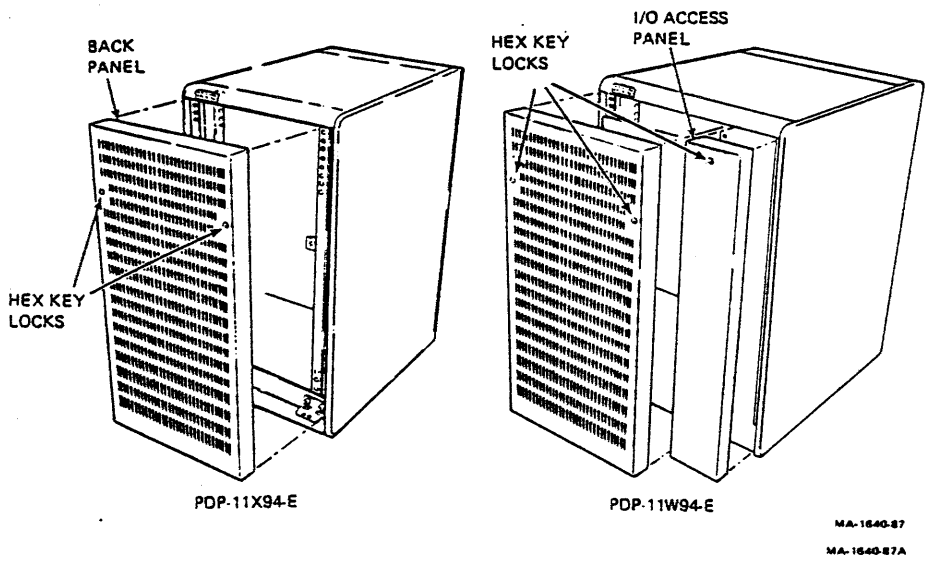


Figure E–1 PDP-11X94-E and PDP-11W94-E Cabinet Panels (Rear View)

   b. To remove each of the rear panels, tilt the top of each panel away from the cabinet while lifting the panel. Lift until the two pins projecting below the bottom lip of each panel are clear of their respective brackets.
   c. Set the panels aside.
   d. On the two cabinets, loosen the two 1/4 × 20 screws and washers that attach each panel bracket to the cabinet frame.

e. Remove and retain the two brackets of each cabinet.

f. To remove the narrow vertical panel covering the I/O space at the rear of the CPU cabinet, use a 4 millimeter (5/32 inch) hex wrench to unlatch the single fastener at the top of the panel.

g. Lift the panel off its mounting buttons and set the panel aside.

3. To prepare the CPU cabinet for mating with the H9642 expander cabinet:

a. Remove the top cover by:

- Removing the two screws located beneath the back of the cover.
- Disconnecting the top cover ground strap.
- Lifting the top cover off the cabinet frame.

NOTE
For safe keeping, replace the two screws into their respective holes.

b. Remove the decorative end panel from the side of the cabinet where expansion is to occur. Grasp the panel at the front and back and lift it about 2.54 centimeters (1 inch). Pull the panel away from the cabinet and set the panel aside.

NOTE
For PDP-11X94-E systems, the expander cabinet can be installed on either the left or the right side of the CPU cabinet. For PDP-11W94-E systems, the expander must be installed on the left side of the CPU cabinet (as seen from the front).

c. If the CPU cabinet is on wheels, skip step d and go to step e.

d. Loosen the locking nuts on the four leveler feet located at the bottom corners of the cabinet (Figure E–2) and raise the feet until the cabinet is resting on its wheels.

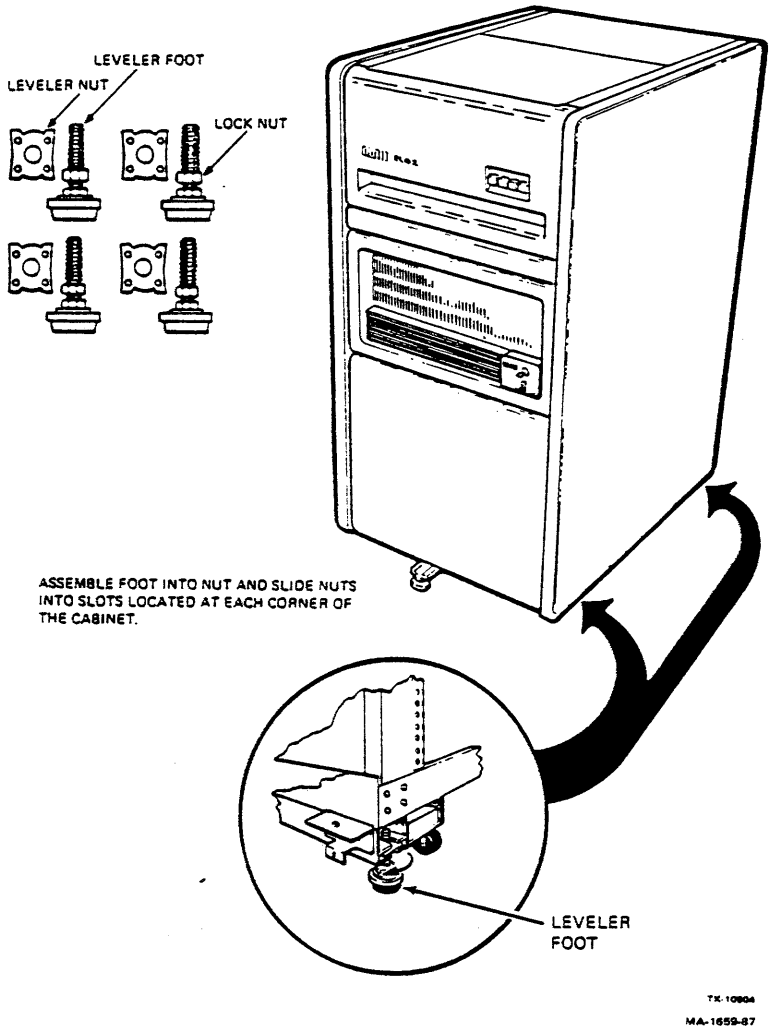


Figure E–2 Adjusting Leveler Feet

e. Remove the RFI shield panel from the side of the CPU cabinet (Figure E–3).

CAUTION
Use care when handling the RFI shields. Careless handling can damage the RFI gasket springs located on its front and back edges.

- Remove and save the two round-head screws with lock washers.
- Remove and save the four key-button screws.
- Grasp the top of the RFI shield and pull the shield away from the cabinet approximately 30.48 centimeters (12 inches).
- Lift the shield panel up and away until the projecting legs located at the bottom of the panel are clear of the structural cross member at the bottom of the cabinet.

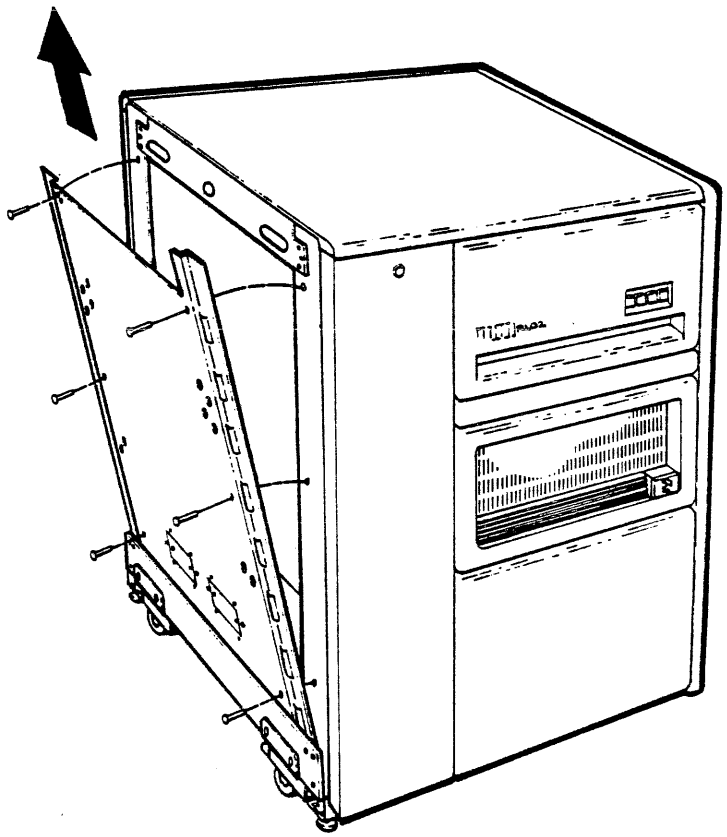


Figure E–3 RFI Shield Panel Removal

f. Remove the copper tape on the RFI shield panel.

g. Install a cable port flange in each of the two port holes formerly filled by the copper tape on the RFI shield panel (Figure E–4).

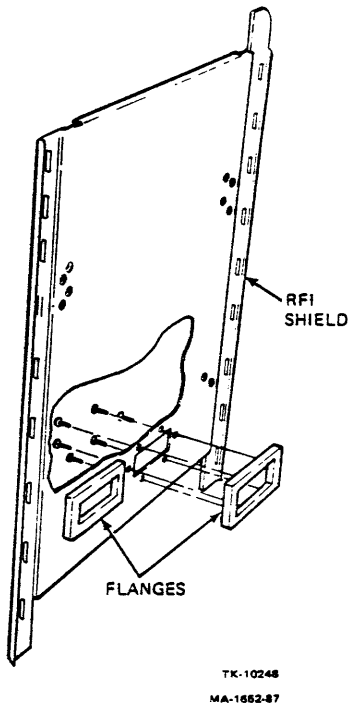


Figure E–4 Installation of Cable Port Flange

- Place one of the flanges from the cabinet joiner bar kit (PN H9645-JE) over a port hole on the outside of the shield panel.
- Align the screw holes in the flange with the screw holes in the shield panel. Press the lip of the flange into the port hole.
- Insert six 8/32 × 1/4 inch screws into the flange screw holes from the inside of the shield panel. Tighten the screws.
- Repeat the above steps to install the second flange.
- Carefully position the shield panel upright, leaning it against the side of the CPU cabinet. *Do not* install the panel onto the CPU cabinet at this time.

h. To prepare the H9642 expander cabinet for mating with the CPU cabinet:

- Remove the expander panel attached to the side of the expander cabinet. Grasp the panel at its front and back, then lift the panel up and away from the cabinet (Figure E–5).

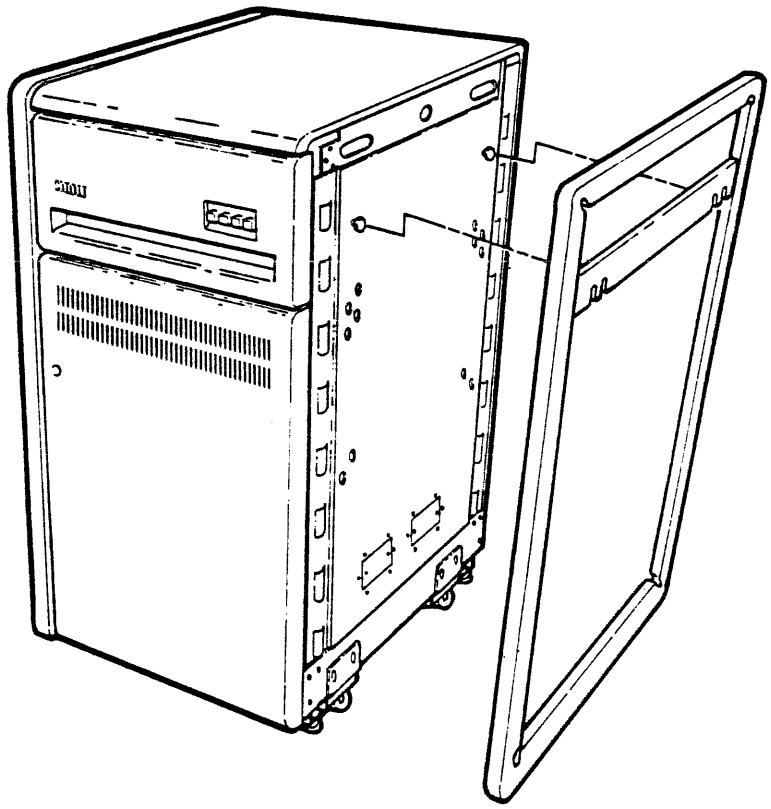


Figure E–5 Expander Panel Removal

- Install the four leveler feet. Raise the feet to their upper position so that the cabinet is resting on its wheels (Figure E–2).
- Remove the expander cabinet front door.
- Remove the RFI shield panel from the right side of the expander cabinet. Follow the procedure outlined in step 3.e of the previous section.
- Remove the two copper tapes from the RFI shield panel. Use the procedure in step 3.f of the previous section.
- Replace the RFI shield panel in its former position on the side of the expander cabinet by reversing the order of the procedure given in step 3.e.

CAUTION
Use care when inserting the projecting legs of the shield panel over the lower front and back of the cabinet frame. Careless insertion may damage the RFI gasket springs on the shield panel.

- Install the expander panel on the side of the expander cabinet.

CAUTION
Be sure to use the expander panel shipped with the expander cabinet. This panel has a single (upper) locking bar. DO NOT use an expander panel that has both upper and lower locking bars.

NOTE
The longer set of key slots on the expander panel should be attached to the expander cabinet.

- Move the expander cabinet so that its side is approximately 0.9 meters (3 feet) from the side of the CPU cabinet. This separation permits easy access through either of the facing sides.
- Locate, inside the expander cabinet, the ribbon cable(s) that must be routed to the CPU cabinet by way of the cable ports at the bottom of the cabinets (Figure E–6).

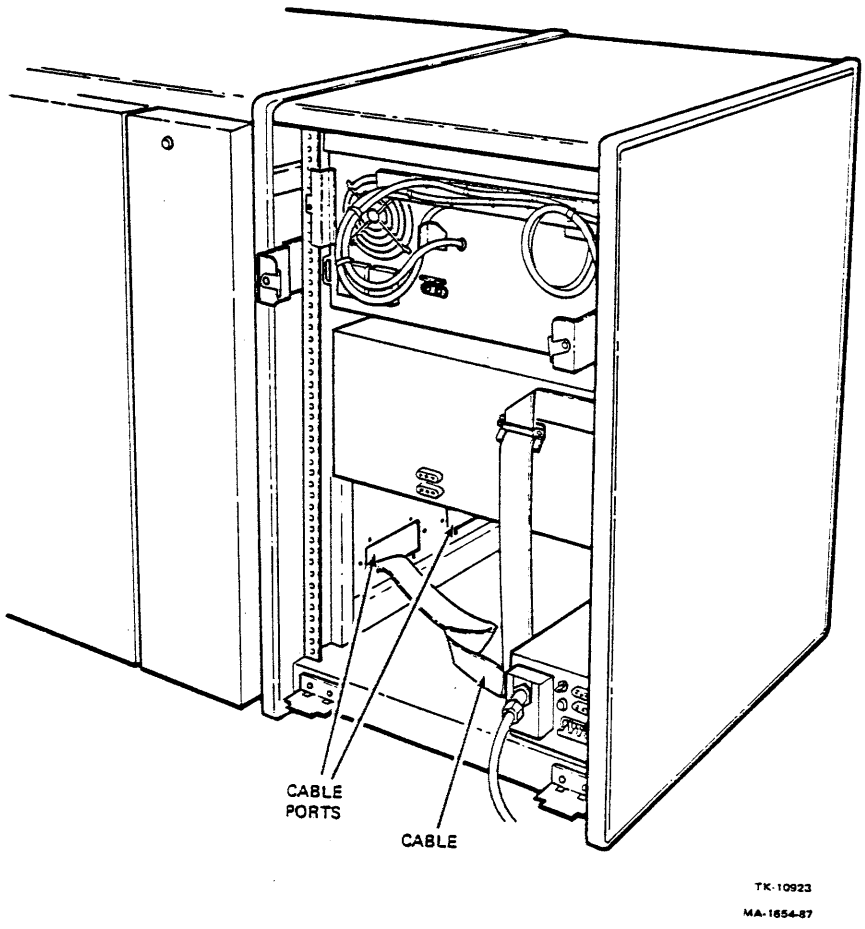


Figure E–6 Cable and Cable Ports Location

- Route the unconnected end of the expander cabinet ribbon cable through the nearest of the two cable ports in the RFI shield panel, and through the two corresponding ports in the shield panel of the CPU cabinet.

- Bring the cable up the inner side of the CPU cabinet to the cable rack at the top of the cabinet. If necessary, move the expander cabinet closer to the CPU cabinet to adapt to the cable length.
- Reinstall the CPU's RFI shield panel on the side of the cabinet by reversing the order of the steps for the RFI shield panel removal (step 3.e of the previous section).

CAUTION
Use care when inserting the projecting legs of the shield panel over the lower front and back of the cabinet frame. Careless insertion may damage the RFI gasket springs on the shield panel.

i. To join the CPU and expander cabinets:

- Carefully move the expander cabinet until its side just meets the side of the CPU cabinet (Figure E–7).

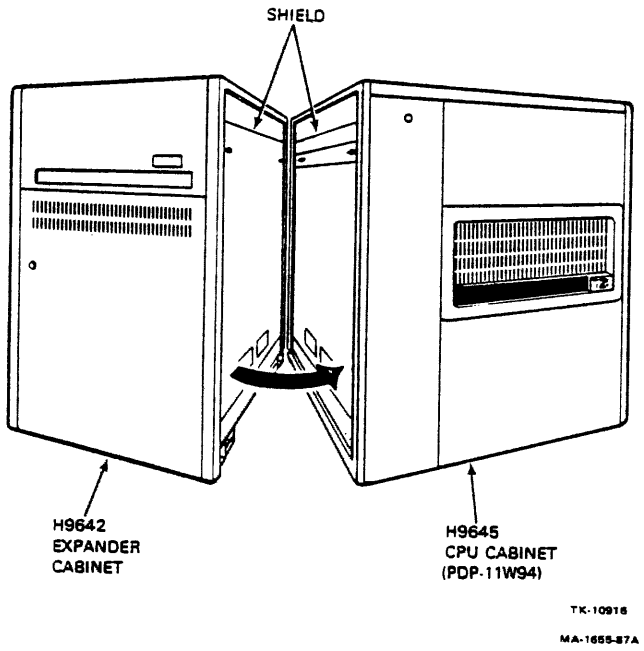


Figure E–7 Joining the CPU Cabinet and the H9642 Expander Cabinet

CAUTION
Ensure that the cable does not bunch up between cabinets. Damage to the cable can occur.

- Raise the expander panel on the side of the expander cabinet approximately 2.54 centimeters (1 inch).
- Hold the cabinets together and push the expander panel down slightly until its key slots just begin to engage the upper key buttons at the front and rear of both cabinets.

- From inside the expander cabinet, ensure that the lips on both cable port flanges are inserted into the port holes and that the six screw holes on each cable port flange are aligned with the screw holes in the RFI shield panel.

  NOTE
  Maneuver the expander cabinet or adjust its leveler feet until you get correct alignment of the cable port flanges for both ports of both cabinets.

- Secure each cable port flange to its RFI shield panel with six 8/32 × 1/4 inch screws.

j. Push down firmly on the expander panel to securely lock the cabinets together.

k. Bolt the cabinets together at the front using the front interconnecting bar provided (Figure E–8).

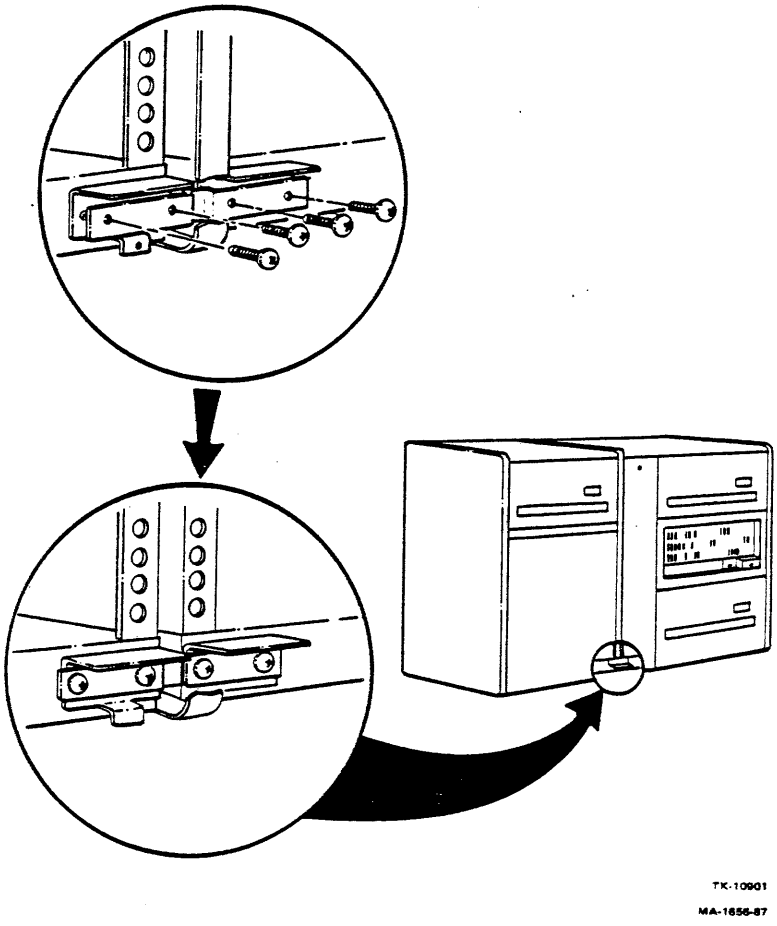


Figure E–8 Front Interconnecting Bar

1. Bolt the cabinets together at the back using the rear interconnecting bar provided (Figure E–9).

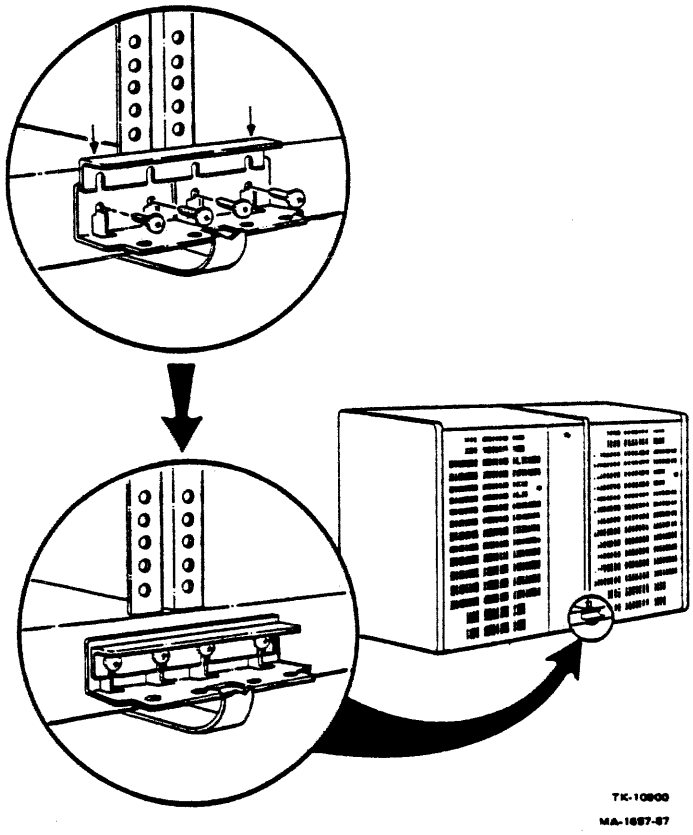


Figure E–9 Rear Interconnecting Bar

F
CPU Instruction Timing

F.1 Introduction

The execution time for an instruction depends on:

- The type of instruction executed.
- The mode of addressing used.
- The type of memory being referenced.

The total execution time is the sum of the base instruction fetch/execute time pl us the operand(s) address calculation/fetch time.

You can use the tables in this section to calculate the length of an instruction in terms of microcycles (MC). Tables Table F–1 through Table F–8 list the standard and floating point instructions, their op code listing, and execution times (MC). The "Execution MC" column specifies the number of microcycles required to fetch/execute the base instruction. The R/W column specifies the number of read microcycles (R) and write microcycles (W) in the Execution MC column. Any remaining microcycles are non-I/O (NIO).

If the instruction involves the calculation/fetch of one or more operands, a reference to a separate table (a source or destination table) is made in the last column. The column is usually labeled "Table" or "Dest Table". The tables referenced are Table F–9, Source Address Times: All Double Operand, Table F–10, Destination Address: Read-Only Single Operand through Table F–15, Destination Address Times: JSR, and Table F–16, Floating Source 1-7 through Table F–20, Integer Destination Modes 1-7. They are located at the end of this appendix. The source/destination tables specify the number of microcycles the source/ destination calculation/fetch requires, and how many of these are read or write microcycles. As before, any remaining microcycles are NIO.

The numbers contained in the tables are based on the assumptions that:

- A memory read must last a minimum of four CLK periods.
- A memory write must last a minimum of eight CLK periods.
- An NIO lasts four CLK periods (no DMA).

Any wait states caused by slower memory or a DMA transfer must be added to the total instruction time. If wait states are required, the first wait state of a nonstretched read or NIO cycle will last four clock periods and can continue in increments of two clock periods. Further wait states for stretched cycles occur in increments of two clock periods.

Floating-point instruction execution times are given as a range. The actual execution time will vary depending on the type of data being operated on.

The following are examples of how to use the tables.

Example 1

How long does a MOV R0,@ 2044 instruction last?

1. From Table F–2, Double Operand Instructions, the execution time for the MOV base instruction is 1 MC, or 4 CLK periods. This consists of one read and no write microcycles (R/W column). Depending on the type of memory in the system, the microcycle may be stretched. If so, the microcycle lasts at least 8 CLK periods and may be stretched thereafter in increments of 2 CLK periods.
2. To find the operand calculation/fetch time for the source operand (R0), refer to Table F–9, Source Address Times: All Double Operand. As shown in Table F–9, a mode 0 register 0 calculate/fetch takes 0 MC. Note that the operand is already available to the DCJ11 (in the register file).
3. To find the operand calculation/fetch time for the destination operand (the contents of memory location 2044), see Table F–12, Destination Address Times: Write-Only. Table F–12 specifies that a mode 3 register 7 calculate/fetch requires three microcycles (that is, one read microcycle and one write microcycle). Note that the remaining microcycle is an NIO microcycle.

   The type of memory in the system must be taken into account. If the read cycle is stretched, the stretched cycle lasts at least 8 CLK periods and may be stretched thereafter in increments of 2 CLK periods. The write microcycle lasts at least 8 CLK periods and may be stretched in increments of 2 CLK periods.
4. For a determination of the minimum time required, total up the microcycles. In this example, it is 1 + 0 + 3, or 4 MC (16 CLK periods if no microcycle stretching occurs).

Example 2

The source and destination tables for floating point instructions show a negative number in the microcycle column for certain mode 2 register 7 operations. For example, to determine how long a CLRD 2000 instruction lasts, you can follow steps 1 through 3:

1. As specified in Table F–8, Floating-Point Instructions, the base instruction time for the CLRD instruction is 14 MC.
2. From Table F–17, Floating Destination Modes 1-7, the calculation/fetch time for the operand (a mode 2 register 7 reference) is shown as (-1) under Double Precision. This means that you subtract 1 MC from the base instruction time. However you add 1 MC for the memory write operation. There are no memory read cycles.
3. Total the microcycles:

   14 - 1 + 1 = 14 MC minimum.

   NOTE
   This example assumes no cycle stretching.

Table F–1 shows the single operand instructions.

Table F–1 Single Operand Instructions

Mnemonic	Instruction	Op Code Listing	Timing			
			Execution MC	R/W	Source Table	Dest. Table
CLR(B)	Clear	0050DD	1	1/0	-	A-12
COM(B)	Complement (1's)	0051DD	1	1/0	-	A-13
INC(B)	Increment	0052DD	1	1/0	-	A-13
DEC(B)	Decrement	0053DD	1	1/0	-	A-13
NEG(B)	Negate (2's complement)	0054DD	1	1/0	-	A-13
TST(B)	Test	0057DD	1	1/0	-	A-13
Rotate and Shift						
ROR(B)	Rotate right	0060DD	1	1/0	-	A-13
ROL(B)	Rotate left	0061DD	1	1/0	-	A-13
ASR(B)	Arithmetic shift right	0062DD	1	1/0	-	A-13
SWAB	Swap bytes	0003DD	1	1/0	-	A-13
Multiple Precision						
ADC(B)	Add carry	0055DD	1	1/0	-	A-13
SBC(B)	Subtract carry	0056DD	1	1/0	-	A-13
SXT	Sign extend	0067DD	1	1/0	-	A-12
Multiprocessing						
TSTSET	Test and set (low bit interlocked)	0072DD	5	1/1	-	A-13
WRTLCK	Write interlocked	0073DD	4	1/1	-	A-13

Table F–2 shows the double operand instructions.

Table F–2 Double Operand Instructions

Mnemonic	Instruction	Op Code Listing	Timing			
			Execution MC	R/W	Source Table	Dest. Table
MOV(B)	Move	01SSDD	1	I/O	A-9	A-13
CMP(B)	Compare	02SSDD	1	I/O	A-9	A-13
ADD	Add	06SSDD	1	I/O	A-9	A-13
SUB	Subtract	16SSDD	1	I/O	A-9	A-13
Logical						
BIT(B)	Bit test (AND)	03SSDD	1	I/O	A-9	A-11
BIC(B)	Bit clear	04SSDD	1	I/O	A-9	A-13
BIS(B)	Bit set (OR)	05SSDD	1	I/O	A-9	A-13
Register						
MUL	Multiply	0704SS	22 (Notes 5, 11)	I/O	-	A-10
DIV	Divide	071RSS	34 (Notes 6, 7, 12)	I/O	-	A-10
ASH	Shift automatically	072RSS	4	I/O	-	A-10
ASHC	Arithmetic shift combined	073RSS	5 (Note 13)	I/O	-	A-10
XOR	Exclusive (OR)	074RDD	1	I/O	-	A-10

Table F–3 shows the branch instructions.

Table F–3 Branch Instructions

Mnemonic	Instruction	Branch Op Code Listing	Timing			
			Branch Not Taken MC	Branch Taken R/W	MC	R/W
BR	Branch (unconditional)	000400	2	1/0	4	2/0
BNE	Br if not equal (to 0)	001000	2	1/0	4	2/0
BEQ	Br if equal (to 0)	001400	2	1/0	4	2/0
BPL	Br if plus	100000	2	1/0	4	2/0
BMI	Br if minus	100400	2	1/0	4	2/0
BVC	Br if overflow is clear	102000	2	1/0	4	2/0
BVS	Br if overflow is set	102400	2	1/0	4	2/0
BCC	Br if carry is clear	103000	2	1/0	4	2/0
BCS	Br if carry is set	103400	2	1/0	4	2/0
Signed Conditional Branches						
BGE	Br if greater or equal (to 0)	020000	2	1/0	4	2/0
BLT	Br if less than (0)	002400	2	1/0	4	2/0
BGT	Br if greater than (0)	003000	2	1/0	4	2/0
BLE	Br if less or equal (to 0)	003400	2	1/0	4	2/0
Unsigned Conditional Branches						
BHI	Br if higher	101000	2	1/0	4	2/0
BLOS	Br if lower or same	101400	2	1/0	4	2/0
BHIS	Br if higher or same	103000	2	1/0	4	2/0
BLO	Br if lower	103400	2	1/0	4	2/0
SOB	Subtract 1 and branch (if not equal to 0)	077RNN	3	1/0	5	2/0

Table F–4 shows the jump and subroutine.

Table F–4 Jump and Subroutine

Mnemonic	Instruction	Op Code Listing	Timing		
			Execution MC	R/W	Dest. Table
JMP	Jump	0001DD	-	-	A-15
JSR	Jump to subroutine	004RDD	-	-	A-15 (Note 4)
RTS	Return from subroutine	00020R	5	3/0	- (Note 14)
MARK	Stack cleanup	0064NN	10	3/0	

Table F–5 shows the trap and interrupt instructions.

Table F–5 Trap and Interrupt Instructions

Mnemonic	Instruction	Op Code Listing	Timing	
			Execution MC	R/W
EMT	Emulator trap	104000-104377	20	4/2
TRAP	Trap	104400-104777	20	4/2
BPT	Breakpoint trap	000003	20	4/2
IOT	Input/output trap	000004	20	4/2
RTI	Return from interrupt	000002	9	4/0
RTT	Return from interrupt	000006	9	4/0

Table F–6 shows the condition code operators.

Table F–6 Condition Code Operators

			Timing	
Mnemonic	**Instruction**	**Op Code Listing**	**Execution MC**	**R/W**
CLC	Clear C	000241	3	1/0
CLV	Clear V	000242	3	1/0
CLZ	Clear Z	000244	3	1/0
CLN	Clear N	000250	3	1/0
CCC	Clear all CC bits	000257	3	1/0
SEC	Set C	000261	3	1/0
SEV	Set V	000262	3	1/0
SEZ	Set Z	000264	3	1/0
SEN	Set N	000270	3	1/0
SCC	Set all C bits	000277	3	1/0

Table F–7 shows the miscellaneous instructions.

Table F–7 Miscellaneous Instructions

Mnemonic	Instruction	Op Code Listing	Timing		
			Execution MC	R/W	Dest. Table
HALT	Halt	000000	-		-
WAIT	Wait for interrupt	000001	-		-
RESET	Reset external bus	000005	-		-
NOP	(No operation)	000240	3	1/0	-
SPL	Set priority level to N		7	1/0	-
MFPI	Move from previous instr space	00023N	5	1/1	A-10
MTPI	Move to previous instr space	0056DD	3	2/0	A-12
MFPD	Move from previous data space	1065SS	5	1/1	A-10
MTPD	Move to previous data space	1066DD	3	2/0	A-12
MTPS	Move byte to PSW PS	1064SS	8	1/0	A-10
MFPS	Move byte from PSW PS	1067DD	1	1/0	A-12
MFPT	Move from processor	000007	2	1/0	-
CSM	Call to supervisor mode	0070DD	28	3/3	A-10

Table F–8 shows the floating-point instructions.

Table F–8 Floating-Point Instructions

			Timing			
Mnemonic	Instruction	Op Code Listing	Min	Execution MC Non-Mode 0 Typical	Max	Table
ABSD	Make absolute	1706 fdst	23		24	A-18
ABSF	Make absolute	1706 fdst	19		20	A-18
ADDD	Add	172 (AC) fsvc	41	48	119	A-16
ADDF	Add	172 (AC) fsvc	31	35	102	A-16
CFCC	Copy Floating Condition Codes	170000	5		5	-
CLRD	Clear	1704 fdst	14		14	A-17
CLRF	Clear	1704 fdst	12		12	A-17
CMPD	Compare	173 (AC + 4)	24		25	A-17
CMPF	Compare	173 (AC + 4)	18		19	A-16
DIVD	Divide	174 (AC + 4)	160		167	A-16
DIVF	Divide	174 (AC + 4)	59		63	A-16
LDCDF	Ld & C from D to F	177 (AC + 4)	24		26	A-16
LDCFD	Ld & C from F to D	177 (AC + 4)	20		21	A-16
LDCID	Ld & C Integer to D	177 (AC) src	31		42	A-19
LDCIF	Ld & C Integer to F	177 (AC) src	26		36	A-19
LDCLD	Ld & C Long Integer to D	177 (AC) src	31		42	A-19
LDCLF	Ld & C Long Integer to F	177 (AC) src	26		44	A-19
LDD	Load	172 (AC + 4)	16		17	A-16
LDEXP	Load Exponent	176 (AC + 4)	17		18	A-19
LDF	Load	172 (AC + 4)	12		13	A-19
LDFPS	Load FPP Program Status	1701 src	6		6	A-19
MODD	Multiply and Separate	171 (AC + 4)	202	217	268	A-16

Table F–8 (Cont.) Floating-Point Instructions

Mnemonic	Instruction	Op Code Listing	Timing			
			Min	Execution MC Non-Mode 0 Typical	Max	Table
MODF	Integer and Fraction	171 (AC + 4)	82	94	115	A-16
MULD	Multiply	171 (AC) fsrc	165		173	A-16
MULF	Multiply	171 (AC) fsrc	56		61	A-16
NEGD	Negate	1707 fdst	22		23	A-18
NEGE	Negate	1707 fdst	18		19	A-18
SETD	Set Floating Double Mode	170011	6		6	-
SETF	Set Floating Mode	170001	6		6	-
SETI	Set Integer Mode	170002	6		6	-
SETL	Set Long Integer Mode	170012	6		6	-
STCDF	St & C from D to F	176 (AC) fdst	17		20	A-17
STCDI	St & C from D to Integer	176 (AC) fdst	26		38	A-20
STCDL	St & C from D to Long Integer	176 (AC) fdst	26		54	A-20
STCFD	St & C from F to D	176 (AC) fdst	19		20	A-17
STCFI	St & C from F to Integer	175 (AC + 4)	23		35	A-20
STCFL	St & C from F to Long Integer	175 (AC + 4)	23		51	A-20
STD	Store	174 (AC) fdst	12		12	A-17
STEXP	Store Exponent	175 (AC) dst	16		16	A-20
STF	Store	174 (AC) fdst	8		8	A-17
STFPD	Store FPP Program Status	1702 dst	9		9	A-20
STST	Store FPP Status	1703 dst	7		7	A-20
SUBD	Subtract	173 (AC) fsrc	47	55	122	A-16
SUBF	Subtract	173 (AC) fsrc	37	41	104	A-16
TSTD	Test	1705 fdst	11		12	A-16
TSTF	Test	1705 fdst	9		10	A-16

Table F–9 shows the source address times: all double operand.

Table F–9 Source Address Times: All Double Operand

Source Mode	Source Register	Microcode Cycles	Read Memory Cycles
0	0-7	0	0
1	0-7	2	1
2	0-6	2	1
2	7	1	1
3	0-6	4	2
3	7	3	2
4	0-6	3	1
4	7	6	2 (Note 1)
5	0-6	5	2
5	7	8	3 (Note 1)
6	0-7	4	2
7	0-7	6	3

Table F–10 shows the destination address: read-only single operand.

Table F–10 Destination Address: Read-Only Single Operand

Destination Mode	Destination Register	Microcode Cycles	Read Memory Cycles
0	0-7	0	0
1	0-7	2	1
2	0-6	2	1
2	7	1	1
3	0-6	4	2
3	7	3	2
4	0-6	3	
4	7	7	2 (Note 2)
5	0-6	5	2
5	7	9	3 (Note 3)
6	0-7	4	2
7	0-7	6	3

Table F–11 shows the destination address times: read-only double operand.

Table F–11 Destination Address Times: Read-Only Double Operand

Destination Mode	Destination Register	Microcode Cycles	Read Memory Cycles
0	0-7	0	0
1	0-7	3	1
2	0-6	3	1
2	7	2	1
3	0-6	5	2
3	7	3	2
4	0-6	4	1
4	7	8	2 (Note 2)
5	0-6	6	2
5	7	10	3 (Note 3)
6	0-7	5	2
7	0-7	7	3

Table F–12 shows the destination address times: write-only.

Table F–12 Destination Address Times: Write-Only

Destination Mode	Destination Register	Microcode Cycles	Memory Cycles Read	Memory Cycles Write
0	0-6	0	0	0
0	7	5	1	0
1	0-6	2	0	1
1	7	6	1	1
2	0-6	2	0	1
2	7	6	1	1
3	0-6	4	1	1
3	7	3	1	1
4	0-6	3	0	1
4	7	7	1	1
5	0-6	5	1	1
5	7	9	2	1
6	0-7	4	1	1
7	0-7	6	2	1

Table F–13 shows the destination address times: read modify write.

Table F–13 Destination Address Times: Read Modify Write

Destination Mode	Destination Register	Microcode Cycles	Memory Read Cycles	Write
0	0-6	0	0	0
0	7	5	1	0
1	0-6	3	1	
1	7	7	2	1
2	0-6	3	1	1
2	7	7	2	1
3	0-6	5	2	1
3	7	4	2	1
4	0-6	4	1	1
4	7	8	2	1 (Note 2)
5	0-6	6	2	1
5	7	10	3	1 (Note 3)
6	0-7	5	2	1
7	0-7	7	3	1

Table F–14 shows the destination address times: JMP.

Table F–14 Destination Address Times: JMP

Destination Mode	Destination Register	Microcode Cycles	Memory Read Cycles	Write
1	0-7	4	2	0
2	0-7	6	2	0
3	0-7	5	3	0
4	0-7	5	2	0
5	0-7	6	3	0
6	0-6	6	3	0
6	7	5	3	0
7	0-7	7	4	0

Table F–15 shows the destination address times: JSR.

Table F–15 Destination Address Times: JSR

Destination Mode	Destination Register	Microcode Cycles	Memory Read	Cycles Write
1	0-7	9	2	1
2	0-7	10	2	1
3	0-6	10	3	1
3	7	9	3	1
4	0-7	10	2	1
5	0-7	11	3	1
6	0-6	10	3	1
6	7	9	3	1
7	0-7	12	4	1

Table F–16 shows the floating source 1-7.

Table F–16 Floating Source 1-7

Microcode Mode	Memory Register	Memory Cycles	Read	Write
Single Precision				
1	0-7	3	2	0
2	0-6	3	2	0
2	7	1	1	0
3	0-6	4	3	0
3	7	3	3	0
4	0-7	4	2	0
5	0-7	5	3	0
6	0-7	4	3	0
7	0-7	6	4	0
Double Precision				
1	0-7	5	4	0
2	0-6	5	4	0
2	7	0 (Note 15)	1	0
3	0-6	6	5	0
3	7	5	5	0
4	0-7	6	4	0
5	0-7	7	5	0

Table F–16 (Cont.) Floating Source 1-7

Double Precision				
6	0-7	6	5	0
7	0-7	8	6	0

Table F–17 shows the floating destination modes 1-7.

Table F–17 Floating Destination Modes 1-7

Microcode Mode	Memory Register	Memory Cycles	Read	Write
Single Precision				
1	0-7	3	0	2
2	0-6	3	0	2
2	7	1	0	1
3	0-6	4	1	2
3	7	3	1	2
4	0-7	4	0	2
5	0-7	5	1	2
6	0-7	4	1	2
7	0-7	6	2	2
Double Precision				
1	0-7	5	0	4
2	0-6	5	0	4
2	7	(-1) (Note 15)	0	1
3	0-6	6	1	4
3	7	5	1	4
4	0-7	6	0	4
5	0-7	7	1	4
6	0-7	6	1	4
7	0-7	8	2	4

Table F–18 shows the floating read-modify-write modes 1-7.

Table F–18 Floating Read-Modify-Write Modes 1-7

Microcode Mode	Memory Register	Memory Cycles	Read	Write
Single Precision				
1	0-7	5	2	2
2	0-6	5	2	2
2	7	1 (Note 15)	1	1
3	0-6	6	3	2
3	7	5	3	2
4	0-7	6	2	2
5	0-7	7	3	2
6	0-7	6	3	2
7	0-7	8	4	2
Double Precision				
1	0-7	9	4	4
2	0-6	9	4	4
2	7	(-2) (Note 15)	1	1
3	0-6	10	5	4
3	7	9	5	4
4	0-7	10	4	4
5	0-7	11	5	4
6	0-7	10	5	4
7	0-7	12	6	4

Table F–19 shows the integer source modes 1-7.

Table F–19 Integer Source Modes 1-7

Microcode Mode	Memory Register	Memory Cycles	Read	Write
Integer				
1	0-7	2	1	0
2	0-6	2	1	0
2	7	0 (Note 15)	1	0
3	0-6	3	2	0
3	7	2	2	0
4	0-7	3	1	0

Table F–19 (Cont.) Integer Source Modes 1-7

Microcode Mode	Memory Register	Memory Cycles	Read	Write
Integer				
5	0-7	4	2	0
6	0-7	3	2	0
7	0-7	5	3	0
Long Integer				
1	0-7	4	2	0
2	0-6	4	2	0
2	7	0 (Note 15)	1	0
3	0-6	5	3	0
3	7	4	3	0
4	0-7	5	2	0
5	0-7	6	3	0
6	0-7	5	3	0
7	0-7	7	4	0

Table F–20 shows the integer destination modes 1-7.

Table F–20 Integer Destination Modes 1-7

Microcode Mode	Memory Register	Memory Cycles	Read	Write
Integer				
1	0-7	2	0	1
2	0-6	2	0	1
2	7	2	0	1
3	0-6	3	1	1
3	7	2	1	1
4	0-7	3	0	1
5	0-7	4	1	1
6	0-7	3	1	1
7	0-7	5	2	1
Long Integer				
1	0-7	4	0	2
2	0-6	4	0	2

Table F–20 (Cont.) Integer Destination Modes 1-7

Long Integer				
2	7	2	0	1
3	0-6	5	1	2
3	7	4	1	2
4	0-7	5	0	2
5	0-7	6	1	2
6	0-7	5	1	2
7	0-7	7	2	2

F.2 Source and Destination Table Notes

1. Subtract 2 MC and 1 read if both source and destination modes autodecrement PC, or if write-only or read-modify-write mode 07 or 17 is used.
2. Read-only and read-modify-write destination mode 47 references actually perform 3 READ operations. For bookkeeping purposes, one of the reads is accounted for in the execute, fetch timing.
3. READ-ONLY and READ-MODIFY-WRITE destination mode 57 references actually perform 4 READ operations. For bookkeeping purposes, one of the READs is accounted for in the EXECUTE, FETCHING TIMING.
4. Subtract 1 MC if the link register is PC.
5. Add 1 MC if the source operand is negative.
6. Subtract 1 MC if the source mode is not 0.
   a. Add 1 MC if the quotient is even.
   b. Add 2 MC if overflow occurs.
   c. Add 5 MC and 1 read if the PC is used as a destination register, but only if source mode 47 or 57 is not used.
7. Add 1 MC per shift.
8. Add 1 MC if source operand <15:6> is not 0.
9. Subtract 1 MC if one shift only.
10. Add 4 MC and 1 read if the PC is used as a destination register, but only if source mode 47 or 57 is not used.
11. Divide by zero executes in 5 MC (see Note 6).
12. Timing for no shift. Add 1 MC if a left shift. (Notes 8, 9, 11 apply.) Add 2 MC for a right shift. (Notes 8, 10, 11 apply.)
13. Add 1 MC if a register other than R7 is used.
14. Mode 27 references only access single-word operands. The execution time listed has been compensated in order to computer the total execution time accurately.

G
Floating-Point Instruction Timing

The FPJ11 is a coprocessor operating in parallel with the DCJ-11 chip set. The calculation of floating-point instruction times for DCJ-11 systems (using the FPJ11 option) must take this parallel processing into account.

Operation	Definition
FPJ11 cycle	Two clock periods (110 ns at 18 MHz).
DCJ-11 nonstretched cycle	Two FPJ11 cycles (220 ns at 18 MHz).
DCJ-11 read cycle	DCJ-11 nonstretched cycle if cache hit. Dependent on read access time of system if cache miss. The minimum is two DCJ-11 nonstretched cycles, after which the DCJ-11 stretches in half-cycle increments until MCONT is asserted.
DCJ-11 write cycle	Dependent on write access time of system (two DCJ-11 cycles + half cycles until MCONT).
Instruction Decode	A decode/prefetch cycle followed by a MOV microinstruction that allows the FPJ11 to assert DMR prior to the start of the next microinstruction (INPR for REG mode). This time equals two nonstretched cycles if the prefetch is a cache hit; otherwise nonstretched plus one read cycle.
Address Calculation Time	DCJ-11 time required to calculate the address of the operand. This time is dependent on the addressing mode of the instruction, the frequency of the system clock, and whether any indirect data required is present in the cache (see Table G–1).
Argument Transfer Time	DCJ-11 time required to load or store floating-point operands. This time is one nonstretched cycle (address relocation µcycle) plus one read cycle per 16-bit word read from memory for load class instructions, or one nonstretched plus one write cycle per 16-bit word to memory for store class instructions.
INPR (FEATEMP,TEMP)	DCJ-11 support code microinstruction execute for all FPJ11 instructions. Moves the PC of the previous FPJ11 instruction to a TEMP register in case that instruction resulted in a floating-point exception. If the FPJ11 is still executing the previous instruction when the DCJ-11 reaches its INPR microinstruction, the FPJ11 asserts STALL causing the DCJ-11 INPR µcycle to stretch. The DCJ-11 then waits for the FPJ11 to deassert STALL, signaling the system interface to assert MCONT before executing the next microinstruction (OUTR).

Operation	Definition
WAIT	DCJ-11 time waiting for the completion by the FPJ11 of the previous FP instruction. For load class or REG mode instructions, the time from when the DCJ-11 INPR cycle stretches at the trailing edge of male until the FPJ11 deasserts STALL. This time equals zero if a stall was not required or if the FPJ11 deasserted the stall signal after the INPR cycle began but prior to the trailing edge of male. Although the wait time for the latter case is zero, RESYNC time is required. For store class instructions the wait time equals the time between the assertion of SCTL (that is, when the system interface is ready to execute the first write cycle of an FP store) and the assertion of FPA-RDY (data ready) by the FPJ11.
RESYNC	For load class and REG mode instructions the time required to continue a stretched INPR. This is the time for the system interface to recognize the deassertion of STALL and assert MCONT, plus the time required for the DCJ-11 to synchronize MCONT and advance to the next microinstruction. Store class instructions normally do not have RSYNC time since the DCJ-11 is waiting in a stretched write cycle and the continuation time is part write cycle. However, if the FPJ11 is executing a previous MODF/D or DIVD, the FPJ11 will assert STALL in order to stretch a non-I/O cycle prior to the first bus write. This allows the system interface to service DMA, thus limiting the worst case DMA latency when waiting for FPJ11 output. In this case, a wait and RESYNC time associated with the stretched non-I/O cycle is added to the effective execution time of the store class instruction.
OUTR (PC,FEATEMP), TESTPLA FPE	Last DCJ-11 support microinstruction unless there is an FPE from the previous FP instruction. Saves address of PC in FEATEMP.
PRDC SYNC	Time required by FPJ11 to decode FP instruction and begin execution after receiving PRDC. This time equals two or three FPJ11 cycles depending upon synchronization. PRDC SYNC is not added to FPJ11 instruction execution times when the FPJ11 is executing a previous FP instruction at the assertion of PDRC.
Floating-Point Execution Time	Time required by FPJ11 to complete an FP instruction once it has received all arguments. For store class instructions, floating-point execution time includes the time from the start of the instruction until the FPJ11 asserts FPA-RDY, indicating the first 16-bit word is available for output (see Table G–2).
Effective Execution Time	Total DCJ-11 time required to execute an FP instruction.
Load class	Instruction Decode + Address Calculation + Argument Transfer + INPR + WAIT + RSYNC + OUTR
REG mode	Instruction Decode + INPR + WAIT + RSYNC + OUTR
Store class	Instruction Decode + Address Calculation + INPR + Argument Transfer + WAIT + OUTR

Table G–1 shows address calculation times.

Table G–1 Address Calculation Times

Mode	Load Class	Store Class
0	0	0
1	3	3
2	3	2
3	3 + RD[1]	2 + RD
4	4	4
5	3 + RD	3 + RD
6	3 + RDI[2]	2 + RDI
7	3 + RDI + RD	3 + RDI + RD
27	2	2
37	2 + RDI	1 + RDI
67	3 + RDI	2 + RDI
77	4 + RDI + RD	4 + RDI + RD

[1]RD = DCJ-11 Read Cycle

[2]RDI = DCJ-11 Istream Request

Table G–2 shows floating-point instruction times.

Table G–2 FPJ11 Instruction Times

Instruction	Min Cycles	Typ Cycles	Max Cycles	Stretch Cycles[1]	18 MHz[2] Typ(μs)
ADDF/SUBF	7	9	19	5	1.0
ADDD/SUBD	7	9	30	5	1.0
MULF	15	15	16	11	1.7
MULD	26	26	27	22	2.9
DIVF	17	24	30	25	2.7
DIVD	33	48	62	57	5.4
MODF	28	34	43	15	3.7
MODD	39	45	71	26	5.0
CMPF/D	3	4	6	2	0.4
LDF/D	3	3	3	0	0.3
LDEXP	2	3	2	0	0.2
LDCIF/D	10	10	10	3	1.1
LDCLF/D	10	10	10	3	1.1
LDCFD	4	4	4	1	0.4
LDCDF	4	4	8	1	0.4
STF/D	3	3	3	0	0.3
STCFI	8	10	13	1	1.1
STCFL	8	12	16	1	1.3
STCFD	4	4	4	0	0.4
STCDF	6	6	6	1	0.7
STEXP	5	5	5	0	0.6
TSTF/D, LDFPS STFPS, CFCC, SET	3	3	3	0	0.3
ABSF/D, NEGF/D	4	4	5	0	0.4

[1]Stretch cycles indicate the number of cycles out of max cycles that a data dependent stretch of one additional cycle could occur with probability less than 1 percent for each additional cycle.

[2]18 MHz = 111 ns Cycle

Load class instructions require input data and deposit results to the destination FP accumulator. REG mode instructions are FP accumulator to FP accumulator.

Execution of a Load class FP instruction by the FPJ11 occurs in parallel with DCJ-11 operation and can be overlapped as shown in the following flow.

DCJ-11	FPJ11
Load class instruction is prefetched. This occurs during previous instruction execution	
Instruction Decode Prefetch next instruction	PRDC SYNC
Address Calculation	
Argument Transfer	FPJ11 loads operands
INPR	FPJ11 execution starts
WAIT if any	
RSYNC if any	
OUTR	
Decode next instruction	
	FPJ11 only stalls if next instruction is FP and REG mode. The FPJ11 can overlap the loading of operands for subsequent load class instructions.
	FPJ11 execution unit done

Store class instructions can be overlapped by the DCJ-11 as the FPJ11 will complete a previously started load class or REG mode instruction and then continue to the store instruction. Execution of the store class instruction must be completed before the result can be stored in memory, thus eliminating further parallel processing for store class FP instructions, see the following flow.

DCJ-11	FPJ11
Store class instruction is prefetched. This occurs during previous instruction execution	
Instruction Decode Prefetch next instruction	PRDC SYNC
Address Calculation	FPJ11 starts execution
INPR Argument Transfer	FPJ11 places operands in output buffer and sets FPA_RDY
DCJ-11 waits during first write if FPA-RDY not asserted	
DCJ-11 completes argument transfer	
OUTR	
Decode next instruction	

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   _____

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