PDP-11/45, 11/70
HARDWARE INTRODUCTION
COURSE DRAWINGS

EY-D3Ø54-HO-ØØ2

SECTION I
ASYNCHRONOUS LINE INTERFACE

FIELD MAINTENANCE PRINT SET

TABLE OF CONTENTS

UNIT VARIATIONS COVERED BY THIS PRINT SET
DL11-W
DL11-WA
DL11-WB
DL11-WC

DL11-W
Field Maintenance Print Set

Digital Equipment Corporation

PRINT SET ORDER NO.
MPØØ1Ø6

REVISIONS		
REV.	A	B
CHG. NO.	DL11W-1	DL11-W-2
DATE	NOV-76	8-77

USED ON OPTION/MODEL

SHEET I OF 1

DRN. D. Head	DATE 26-MAR-76	digital
CHK'D D. Head	DATE 26-MAR-76	TITLE: FIELD MAINTENANCE PRINT SET DL11-W
PROJ. ENG. R.E. Hatt	DATE 29-MAR 1976	SIZE B · CODE TC · NUMBER DL11-W-1 · REV. B
FIELD SERV.	DATE 14-April 1976	DIST.

DRB 124

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

PARTS LIST

MADE BY	D. HEALY	CHECKED	D. HEALY	SECTION	1
DATE	25 MAR 76	DATE	25 MAR 76		
ENG	R.E. BRATT	PROD	K. MACDONALD	ISSUED SECT.	1
DATE	1 APR 76	DATE	7-APR-76		

ITEM NO	DWG NO./PART NO.	DESCRIPTION	QUANTITY/VARIATION DL11-W	DL11-WA	DL11-WB	DL11-WC
1	D-CS-M7856-Ø=1	SLU/RTC OPTION	1	1	1	1
2	D-1A-7008360-1-0	CABLE ASSY (KL8-E)	-	1	-	-
3	D-UA-BCØ5C-25-0	CABLE MODEM BCØ5C	-	-	1	-
4	D-UA-BC03L-10-0	CABLE ASSY	-	-	-	1
5	2376ØA9 *	BOOTSTRAP ROM	1	1	-	1
6	9906228 *	BOX ROM	1	1	-	1
7	D-CS-H315-0-1	MODEM TEST CONNECTOR (SEE NOTE 3.)	-	-	1	1

* 1. THE ROM AND ROM BOX WILL BE ADDED AT FA+T.

2. THE ROM AND ROM BOX ARE TO BE SHIPPED ONLY IF AN LT33 OPTION IS SHIPPED WITH A UNIBUS 11 SYSTEM.

3. ONE H315 PER PDP-11 SYS. OR ONE PER DL-11/WB OR WC LOOSE PIECE/ADD ON.

TITLE	ASSY NO.	SIZE	CODE	NUMBER	REV	ECO NO
SERIAL LINE/LINE CLOCK DL11-W	NONE	A	PL	DL11-W-Ø	D	DT11W MK005
	SHEET 1 OF 1	DIST				

NK

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

PARTS LIST

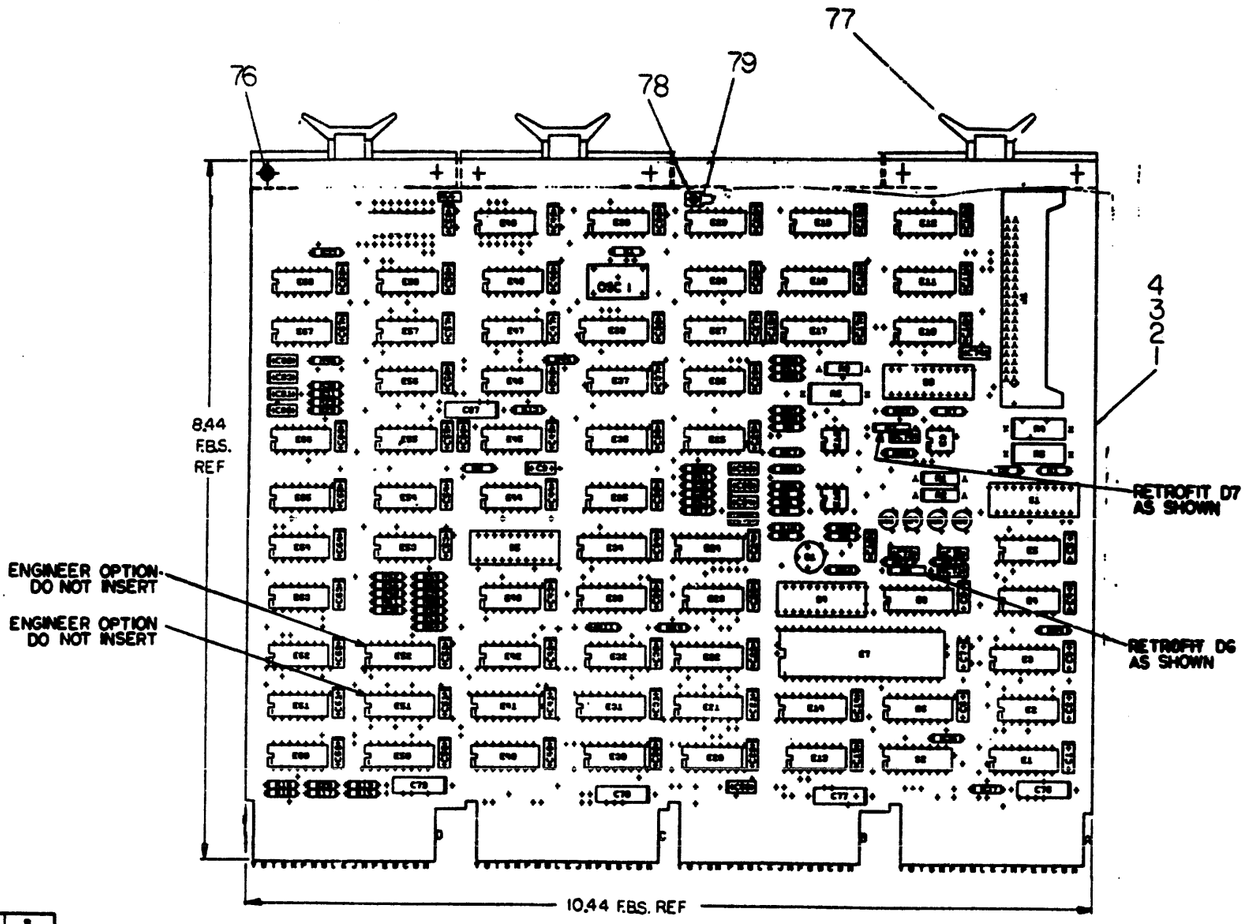
MADE BY D. HEALY	CHECKED D. HEALY	SECTION 1
DATE 25 MAR 76	DATE 25 MAR 76	
ENG RB Pratt	PROD K W. MacDonald	ISSUED SECT. 1
DATE 1-APR-76	DATE 7 APR 76	

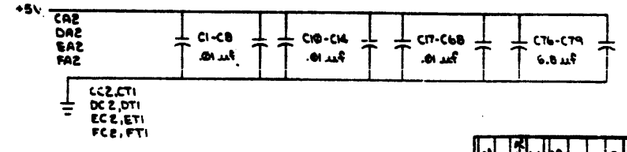
ITEM NO.	DWG NO. / PART NO.	DESCRIPTION	QUANTITY/VARIATION DL11-W	DL11-WA	DL11-WB	DL11-WC
1	D-CS-M7856-Ø-1	SLU/RTC OPTION	1	1	1	1
2	D-IA-7008360-1-0	CABLE ASSY (KL8-E)	-	1	-	-
3	D-UA-BCØ5C-25-0	CABLE MODEM BCØ5C	-	-	1	-
4	D-UA-BC03L-10-0	CABLE ASSY	-	-	-	1

TITLE: SERIAL LINE/LINE CLOCK DL11-W	ASSY NO. NONE	SIZE A	CODE PL	NUMBER DL11-W-Ø	REV. A
	SHEET 1 OF 1	DIST.			ECO NO. DL11W 00001

DEC FORM DEC 16-(325) 1031-N870
DRA 110

NOTES:





IC 384	1	8
IC 8837	8	16
IC 514A	1	8
IC 7423	8	16
IC 74157	8	16
IC 74153	8	16
IC 7493	10	5
IC 7492	10	5
IC 74151	8	16
IC 74175	8	16
IC UART	1	3
IC 8097	8	16
IC 8641	8	16
IC TYPE	GND	+5V

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

REF		DESCRIPTION	PART NO.	ITEM NO.
REF		X-Y COORDINATE HOLE LOCATION	K-CO-M7856-0-4	1
REF		ASSY/DRILLING HOLE LAYOUT	D-AH-M7856-0-5	2
REF		MODULE ECO HISTORY	D-MH-M7856-0-0	3
1		ETCHED CIRCUIT BOARD	5011484	4
67	C1 THRU C8,C10 THRU C15, C17 THRU C68,C86	CAPACITOR, .01uf, 100V, 20%	1001810-01	5
7	C9,C80 THRU C74	CAPACITOR, 470pf, 100V, 5%	1000024	6
1	C75	CAPACITOR, 330pf, 100V, 5%	1000023	7
6	C80 THRU C85	CAPACITOR, 82pf, 100V, 5%	1000015	8
1	C86	CAPACITOR, 150pf, 100V, 5%	1000019	9
1	C87	CAPACITOR, 2.2uf, 20V, 10%	1002027	10
4	C76,C77,C78,C79	CAPACITOR, 6.8uf, 35V, 10%	1005306	11
1	C16	CAPACITOR, 5000pf, 100V, 20%	1001765	12
3	D1,D2,D3	DIODE, IN4908R	1105796	13
1	D4	DIODE, ZENER IN4742	1109502	14
2	D6,D7	DIODE, CURRENT LIMITER MCL1301	1105616	15
1	D8	DIODE, D884	1106114	16
4	S1,S3,S4,S5	SWITCH, 10 POSITION	1211164-08	17
1	S2	SWITCH, 8 POSITION	1211164-04	18
				19
				20
1	J1	CONNECTOR, 40 PIN	1209841	21
1	R83	RESISTOR, 330, 1/4W, 5%	1300295	22
3	R1,R2,R3	RESISTOR, 100 OHM, 1/2W, 5%	1300268	23
3	R4,R5,R6	RESISTOR, 560 OHM, 1W, 5%	1303648	24
2	R7,R8	RESISTOR, 68K, 1/4W, 5%	1301327	25
1	R9	RESISTOR, 33 OHM, 1/4W, 5%	1300197	26
1	R10	RESISTOR, 120K, 1/4W, 5%	1300539	27
1	R12	RESISTOR,68Ω, 1/4W, 5%	1301424	28
1	R25	RESISTOR, 68 OHM, 1/4W, 5%	1300219	29
2	R13,R14	RESISTOR, 100 OHM, 1/4W, 5%	1300229	30
4	R15,R16,R17,R18	RESISTOR, 180 OHM, 1/4W, 5%	1301322	31
4	R19,R20,R21,R22	RESISTOR, 390 OHM, 1/4W, 5%	1300389	32
1	R23	RESISTOR, 7.5K, 1/4W, 5%	1301422	33
2	R27, R26	RESISTOR, 150 OHM, 1/4W, 5%	1360250	34
6	R28 THRU R33	RESISTOR, 270 OHM, 1/4W, 5%	1301972	35
27	R35,R36,R37,R39 THRU R62	RESISTOR, 10K, 1/4W, 5%	1300479	36
3	R11,R64,R38,	RESISTOR, 1K, 1/4W, 5%	1300385	37
1	R34	RESISTOR, 220 OHM, 1/4W, 5%	1300271	38
1	Q1	TRANSISTOR, DEC 8531B	1509338	39
2	Q3,Q4	TRANSISTOR, A05	1510705	40
2	Q2,Q5	TRANSISTOR, A55	1510706	41
2	E9,E16	OPTICALLY COUPLED ISOLATOR	1510727-1	42
1	OSC 1	OSCILLATOR 50688 MHZ	1811680-02	43
1	E15	I.C. DEC 4N26	911998	44
3	E1,E8,E14	I.C. DEC 8641	1911579	45
6	E2,E13,E20,E60,E61,E49	I.C. DEC 8881	1909705	46
1	E3	I.C. DEC 8097	1911527	47
3	E4,E44,E64	I.C. DEC 7408	1910159	48
7	E5,E35,E37,E55,E57,E63,E68	I.C. DEC 7474	1905547	49
1	E7	I.C. DEC UART(1808)	1910450-01	50
1	E8	I.C. DEC 74175	1910651	51
1	E10	I.C. DEC 1489L	1910323	52
1	E11	I.C. DEC 1488L	1910322	53
2	E17,E18	I.C. DEC 74151	1909936	54

QTY | REF. DESIGNATION | DESCRIPTION | PART NO. | ITEM NO.

PARTS LIST

ETCH BOARD REV. D

FIRST USED ON OPTION MODEL

SEMICONDUCTOR CONVERSION CHART

DEC NO.	EIA NO.	DEC NO.	EIA NO.

REV.	REVISIONS	CHANGE NO.	BY	DATE
D	ONE	M7856-0000	B. PRATT	8-3-76
E	ONE	M7856-0002	B. PRATT	8-10-76

DRN. B. PRATT 8-10-76
CHKD. R. Stewart 8-10-76
ENG. R. Stewart 8-10-76
PROJ. ENG. N/A
MFGR. N/A

NEXT HIGHER ASSY

digital

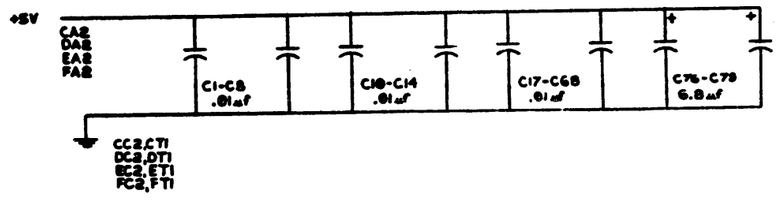
TITLE SLU/RTI OPTION

SIZE D | CODE | NUMBER SM7856-0-1 | REV. E

SCALE | SHEET 1 OF 9 | DIST.

DCS M7856-0-1

NOTES:



IC TYPE	GND	+5V
IC 8641	8	16
IC 344	1	8
IC 88-7	8	16
IC 514A	1	8
IC 74123	8	16
IC 74157	8	16
IC 74153	8	16
IC 7493	10	5
IC 7492	10	5
IC 74151	8	16
IC 74175	8	16
IC UART	1	3
IC 8097	8	16

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

QTY	REF. DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.

FIRST USED ON OPTION MODEL

PARTS LIST

ETCH BOARD REV. E

DEC NO.	EIA NO.	DEC NO.	EIA NO.

SEMICONDUCTOR CONVERSION CHART

REV.	CHANGE NO.	REVISIONS	BY	DATE
H	M7856-4	ADD TO	R. MARRINGTON	11-APR-80
J	M7856-4		R. CRAWN	

DRD D Dunphy 2/23/79
CHK'D. [illegible] DATE 3-7-79
ENG. [illegible] DATE
PROJ. ENG. [illegible] DATE
PROJ. [illegible] DATE

NEXT HIGHER ASSY

SCALE

SHEET 1 OF 8

TITLE: SLU/RTC OPTION

SIZE D | CODE CS | NUMBER M7856-0-1 | REV. J

EST.

M7856-0-1 CS D J

DL-1 RCVR INTR RQST H

+5V R45 10K

DL-4 BBD 6 H
RCSR CLR H
7474 E37

DL-4 B INIT L
DL-4 BBD0 H
DL-1 RCSR ENB (1) L
7474 E35
7408 E44

DL-1 RCVR BUSY(1) H
7408 E44
DL-4 SEL 2 L

7474 E37
7402 E58
DL-4 B INIT H

74197 E47
LD CLR CLKB CLK1
R3(0) R2(0) R1(0) R0(0)

+5V -12V
CLR R DONE
STB STATUS
STB RD
R CLK
SERIAL IN
XD7 XD6 XD5 XD4 XD3 XD2 XD1 XD0
LD XD
XCLK
SERIAL OUT
CLR LOC NBA PAR MP EP FE
U ART E7

DL-4 BBD 7 H
DL-4 BBD 6 H
DL-4 BBD 5 H
DL-4 BBD 4 H
DL-4 BBD 3 H
DL-4 BBD 2 H
DL-4 BBD 1 H
DL-4 BBD 0 H
DL-4 LD X DEL L

R DONE
RD7 DL-1 RD8TH
RD6 DL-1 RD86 H
RD5 DL-1 RD85 H
RD4 DL-1 RD84 H
RD3 DL-1 RD83 H
RD2 DL-1 RD82 H
RD1 DL-1 RD81 H
RD0 DL-1 RD80 H
CR ERR
FR ERR
P ERR
EOC
X RDY

8097 E3
7408 E4
DL-1 RCVR DONE H

DL-3 RCVR SEL H
DL-3 MASTER H
7408 E46
7408 E44
7459 E44

DL-1 RCVR INTR ENB (1) H

7474 E5
7408 E4

DL-1 CR ERR H
DL-1 FR ERR H
DL-1 P ERR H
DL-1 XMIT RDY H
DL-1 ERROR H
8097 E3
384 E48

+5V R47 10K
7474 E39
R32 270
R33 270
C84 82PF
C85 82PF
7414 E48
7414 E45

XMIT INTR ENB0'L
7408 E36

7474 E5

DL-1 XMIT INTR RQST H

DL-6 XMIT CLK H
DL-6 RCVR CLK H
DL-5 TTL SERIAL DATA IN
DL-5 SERIAL OUT H
FR ERR H
RCVR DONE H

74157 E38
A0 B0 A1 B1 A2 B2 A3 B3 S0 STB
C1 C2 C3

7837 E25
8881 E49
TB-1 BOOT SW L
(FASTON TAB)

74175 E8
D3 D2 D1 D0
R3(0) R2(0) R1(0) R0(0)
CLK CLR

DL-4 BBD 6 H
DL-4 BBD 0 H
DL-4 BBD 2 H
XMIT INTR ENB (1) L
DL-1 MAINT (1) H
DL-1 MAINT (1) L
SW-1
DL-4 XCSR CLR H
DL-4 B INIT L

DL-1 XMIT INTR ENB (1) H

7408 E46
DL-1 SERIAL OUT L
DL-1 BREAK (1) H
R46 10K

DL-3 MASTER H
DL-3 XMIT SEL H
7408 E46
DL-4 LD X DEL L

SPARE LOGIC
384 E48
1488L E11
1489L E10
7414 E44
7837 E41
7402 E36

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
SLU/RTC OPTION (DL-1)	D	CS	M7856-0-1	J
SCALE	SHEET 2 OF 8	DIST.		

DEC FORM NO. DRD 128

MK 1

+5V
R39 10K
DL-4 BBD 06 H
DL-2 LTC BIT 06 H
7474 E48
DL-4 BM SYN DEL L
DL-4 LTC IN L
7402 E58
DL-4 B INIT L
DL-2 LTC BIT 07 H
7474 E57
D8 D666
BUS LTC L
CDI
R43 330
7414 E46
C85 .01μF
C87 2.2μF
DL-4 BBD TH
7404 E44
DL-4 BSYN H L
7410 E52
7400 E67
7402 E58
BUS SSYN L
EJ1
BUS MR L
DM2
BUS B66 IN H
DM2
BUS B66 OUT H
FT2
BUS SACK L
ESI
+5V
MASTER CLEAR H
DL-4 B INIT H
RTC MASTER L
FDI
BUS BUSY L
DE2
BUS BR6 L
ENGR OPTION - DO NOT INSERT
DP2 BUS BG5 IN H
DR2 BUS BG5 OUT H
DM2 BUS BG7 IN H
DL2 BUS BG7 OUT H

*NOTE: PARTITION THESE COMPONENTS WITH THOSE ON SHT 5

7474 E55
R36 270
C82 82 PF
7414 E66
R31 270
C83 82 PF
7414 E44
8881 E68
DE2 BUS BR6 L
7400 E65
+5
R18 180
DM2 BUS B66 OUT H
+5V
R17 180
BUS B66 IN H
8837 E59
7400 E68
7400 E54
FT2 BUS SACK L
DL-4 B INIT H
7402 E59
7400 E54
7402 E42
+5V
R40 10K
7474 E63
FDI BUS BUSY L
BUS BUSY L FDI
BUS SSYN L EJI
8837 E58
DL-2 B BUS BUSY H
DL-2 B BUS SSYN H
7402 E53
7400 E64
7400 E64
7402 E42
DL-2 RTC MASTER L
7404 E56
8881 E28
PMI BUS INTR L
MASTER CLEAR H

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE: SLU/RTC OPTION (DL-2)		SIZE: D	CODE: CS	NUMBER: M7856-Ø-1
SCALE: —	SHEET 3 OF 8	DIST.		REV: J

mk1

BUS SACK L — FT2 — E52 pin 7
BUS BG4 OUT H — DT2 — E52 pin 6
BUS BG4 IN H — DS2 — E52 pin 5
BUS NPR L — FJ1 — E52 pin 4
BUS SSYN L — EJ1 — E52 pin 2
E52 pin 8 — GND
E52 pin 16 — +5V
E52 pin 9 — DNL
E52 pin 10 — FDI
E52 pin 11 — MASTER L
E52 pin 12 — SACK H
E52 pin 13 — DL-4 B INIT H
E52 pin 14 — MASTER H
E52 pin 15 — (no connection)
E52 pin 9 — BUS BR4 L
E52 pin 10 — BUS BUSY L
E52 pin 11 — MASTER L
E52 pin 12 — SACK H
E52 pin 13 — DL-4 B INIT H
E52 pin 14 — MASTER H
E52 pin 15 — (no connection)
E52 pin 16 — +5V
ENGR OPTION DO NOT INSERT

*NOTE: PARTITION THESE COMPONENTS WITH THOSE NOTED ON SHT. 4

DL-1 XMIT INIT H
RQST H
DL-1 RCVR INTR RQST H
E64 / E48
7404 E54
7408 E45
7474 E55
R28 270
R29 270
C28 .02µF
C31 .02µF
7416 E66
7416 E46
7404 E46
8881 E61
+5V
R96 1KΩ
DT2 — BUS BG4 OUT H
BUS BG4 IN H — DS2
+5V
R95 180
R19 340
8837 E58
8837 E58
7408 E65
7408 E64
FT2 — BUS SACK L
DL-4 B INIT H
7402 E62
8881 E61
7402 E53
7408 E54
+5V
R98 10KΩ
7474 E53
FDI — BUS BUSY L
DL-2 BBUS BUSY H
BBUS SSYN H
7402 E53
7408 E44
7408 E64
7402 E52
8881 E2
S2-4* — CT2 — BUS DO9 L
S2-7* — CM2 — BUS DO7 L
S2-8* — CL2 — BUS DO8 L
+5V
R97 10KΩ
S2-5* — DL-2 RTC MASTER L
8881 E22
R96 10KΩ
+5V
8881 E22
CV2 — BUS DO6 L
MASTER L
7404 E36
DL-3 MASTER H
8881 E13
PMI — BUS INTR L
8881 E15
S2-3* — CP2 — BUS DO5 L
8881 E13
S2-6* — CM2 — BUS DO4 L
8881 E15
CV2 — BUS DO3 L
SACK H
7408 E67
7474 E68
DL-3 RCVR SEL H
DL-3 XMIT SEL H
7408 E67

* VECTOR ADDRESS SWITCHES - ON=1 OFF=0

REVISIONS		
CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV.
SLU/RTC OPTION (DL-3)	D	CS	M7856-0-1	J
SCALE	SHEET 4 OF 8	DIST.		

DEC FORM NO. DRD 130

MK 1

BUS INIT L → 8837 E41 → 7404 E56 → DL-4 B INIT L, DL-4 B INIT H

BUS MSYN L → 8837 C34 → R15 CC, C68 470 pF → 8881 E49

DL-4 SMSYN DBL L, +5V R64 1K, DL-7 SSYN EN L → 7402 E23 → R14 1K, R16 100, C69 470 pF → 7414 E45 → DL-4 SSYN L

8881 E29 → BUS SSYN L

DL-7 LD XBUF H → C66 150 pF → 7423 E24 → DL-4 LDXCSL L; +5V R41 10K

DL-7 RBUF→BUS H → 7423 E24 → DL-4 SEL 2 L; R43 10K

DL-7 XCSR CLK ENBL L → 7402 E23 → DL-4 XCSR CLK H

DL-7 XCSR CLK ENBL → 7402 E23 → DL-4 XCSR CLK H

DL-1 BREAK (0) H, DL-1 RDS8 H, DL-1 MAINT (0) H, DL-1 RDS2 H → T4157 E22 (2:1 MUX) → DL-7 E22 S0 H, DL-7 E22 STB L

DL-1 RDS6 H, DL-1 XMIT INTR ENB (1) H, DL-1 RCVR INTR ENB (1) H, DL-2 LTC BIT 06 H, DL-1 RDS7 H, DL-1 XMIT READY H, DL-1 RCVR DONE H, DL-2 LTC BIT 07 H → T4153 E21 (4:1 MUX) → DL-7 E21 S1 H, DL-7 E21 S0 H

DL-1 RDS1 H → BUS DS1 L (CH2) → DL-4 BSD 1 H
DL-1 RDS3 H → BUS DS3 L (CT2) → DL-4 BSD 3 H
DL-1 RDS4 H → BUS DS4 L (CH2) → DL-4 BSD 4 H
DL-1 RDS5 H → BUS DS5 L (CP2) → DL-4 BSD 5 H
DL-7 E4 EN L → B641 E14

DL-1 RDS6 H → BUS DS6 L (CH2) → DL-4 BSD 6 H
DL-1 RDS2 H → BUS DS2 L (CU2) → DL-4 BSD 2 H
DL-1 RDS6 H → BUS DS6 L (CV2) → DL-4 BSD 6 H
DL-1 RDS7 H → BUS DS7 L (CW2) → DL-4 BSD 7 H
DL-7 E6 EN L → B641 E6

DL-7 E23 EN L → 7402 E23 → 8881 E29 ← DL-1 RCVR BUSY (1) H → BUS DI1 L (CH1)

DL-1 P ERR H → BUS DI2 L (CH2) → DL-4 BSD 1 H
DL-1 FR ERR H → BUS DI3 L (CP2) → DL-4 BSD 3 H
DL-1 OR ERR H → BUS DI4 L (CE2) → DL-4 BSD 4 H
DL-1 ERROR H → BUS DI5 L (CD2) → DL-4 BSD 5 H
DL-7 E8 ERR L → S4-7 → R44 10K, +5V → B641 E1

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
SLU/RTC OPTION (DL-4)	D	CS	M7856-0-1	J
SCALE	SHEET 5 OF 8	DIST.		

DCS M7856-0-1 J

NOTE:
1. SWITCHES ARE SHOWN IN ACTIVE MODE.
2. D7, D6 ARE MCL1361 1 MA CONSTANT CURRENT DIODES.

DL-1 RCR ENB (I)L

DL-1 MAINT (I)L

SERIAL OUT L

DL-5 SERIAL OUT H

DL-5 TTL SERIAL DATA IN

DATA TERMINAL READY

RQST TO SEND

+12/E11 PIN 14

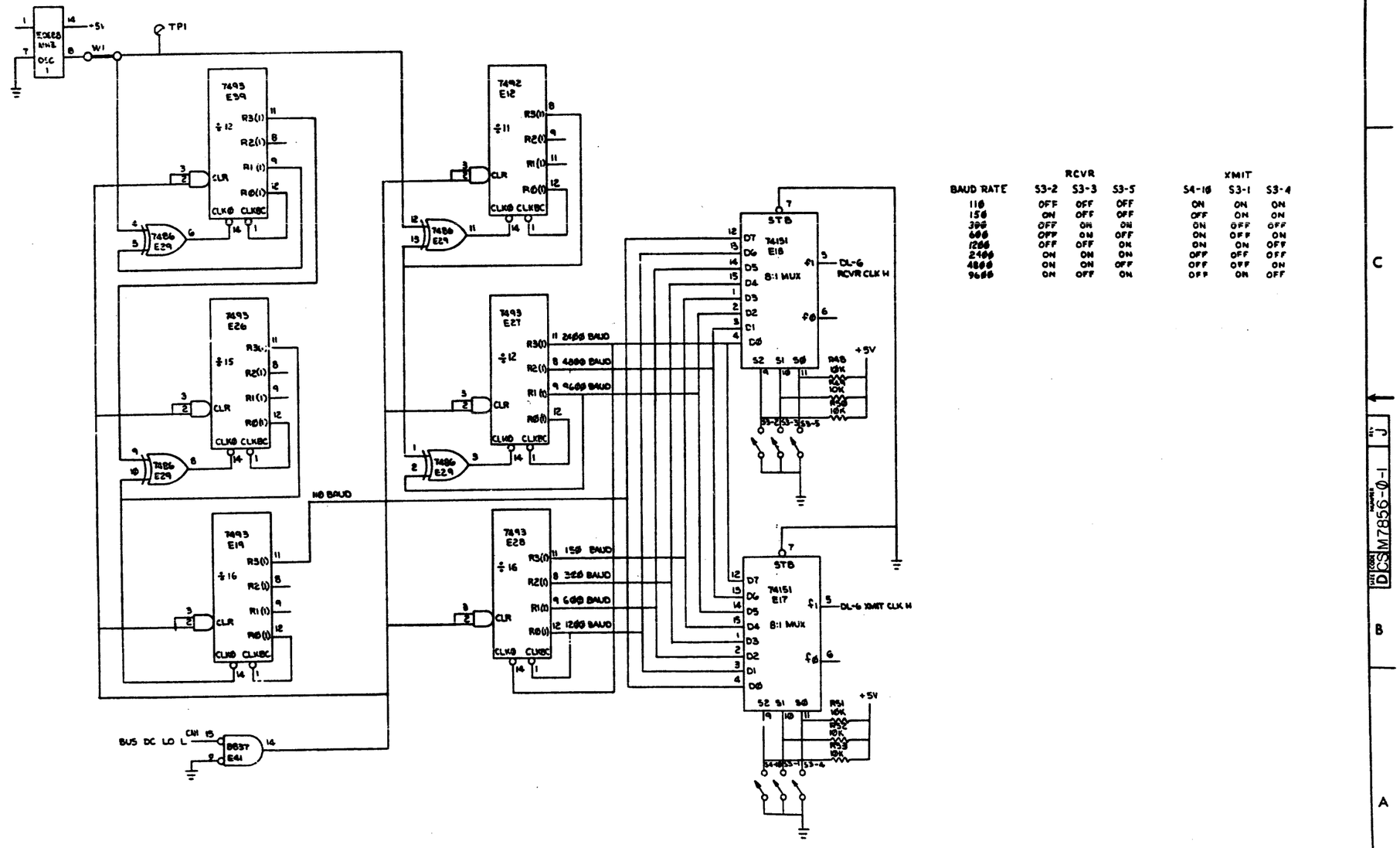
-12/E11 PIN 1

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SLU/RTC OPTION (DL-5)	SIZE/CODE D CS	NUMBER M7856-0-1 REV. J
SCALE	SHEET 6 OF 8	DIST.	

DCS M7856-0-1 J

MK 1

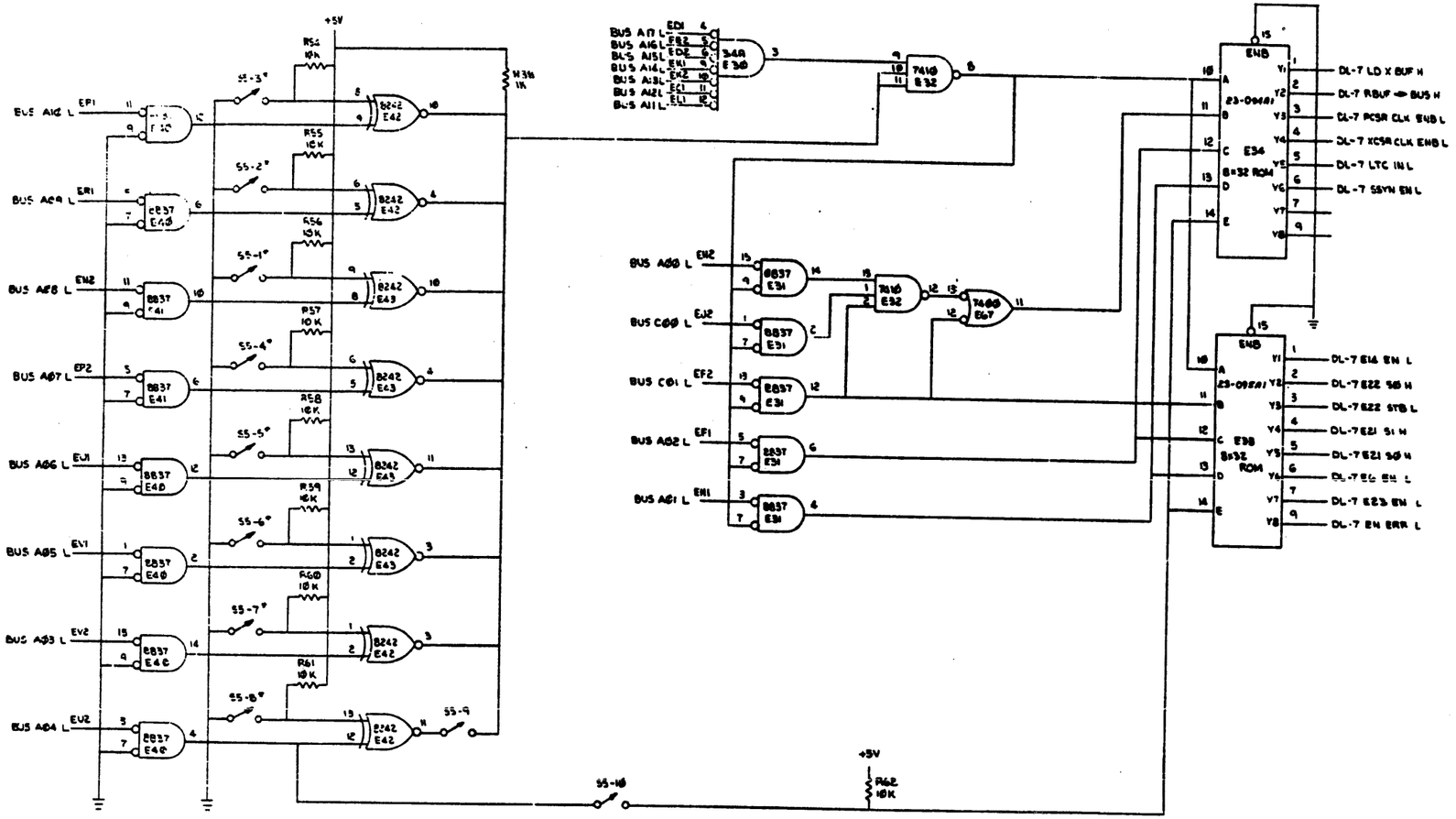


BAUD RATE	RCVR S3-2	RCVR S3-3	RCVR S3-5	XMIT S4-1@	XMIT S3-1	XMIT S3-4
110	OFF	OFF	OFF	ON	ON	ON
150	ON	OFF	OFF	OFF	ON	ON
300	OFF	ON	ON	ON	OFF	OFF
600	OFF	ON	OFF	ON	OFF	ON
1200	OFF	OFF	ON	ON	ON	OFF
2400	ON	ON	ON	OFF	OFF	OFF
4800	ON	ON	OFF	OFF	OFF	ON
9600	ON	OFF	ON	OFF	ON	OFF

REVISIONS		
CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV.
SLU/RTC OPTION (DL-6)	D	CS	M7856-Ø-1	J
SCALE	SHEET 7 OF 8	DIST.		

mk 1



*ADDRESS SELECTION SWITCHES - OFF=1 ON=0

REVISIONS		
CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV.
SLU/RTC OPTION (DL-7)	D	CS	M7856-0-1	J
SCALE	SHEET 8 OF 8	DIST		

DEC FORM NO. DRD 120

DCS M7856-0-1

REV.	NUMBER	SIZE	CODE	
	M7856-0-9	K	CS	2

(FOR 23094AI-A07 & 23095AI-A07)

DESCRIPTION	DWG./PART NO.	ITEM NO.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

ANGLES ±0° 30'	CLASS OF ACCURACY (CHECK ONE)	NOMINAL DIMENSION RANGE INCHES					
		OVER 0 TO 0.2	OVER 0.2 TO 1.2	OVER 1.2 TO 4.0	OVER 4.0 TO 12.0	OVER 12.0 TO 40.0	OVER 40.0 TO 80.0
SURFACE QUALITY IN ✓ MICROINCHES	MEDIUM ☐	±.004	±.008	±.012	±.016	±.024	±.04
	PREFERRED ☐	±.012	±.016	±.025	±.04	±.063	±0.1

QUANTITY & VARIATION

THIRD ANGLE PROJECTION

REMOVE BURRS AND BREAK SHARP CORNERS

DO NOT SCALE DWG

MATERIAL —

FINISH —

DRN. —

CHK'D —

ENG. —

PROJ. ENG. —

PROD. —

NEXT HIGHER ASSY. D-CS-M7856-0-1

SCALE —

SHEET 1 OF 3

FIRST USED ON DL11-W

digital

TITLE ROM LISTING

SIZE	CODE	NUMBER	REV.
K	CS	M7856-0-9	

DIST.

REVISIONS

REV.	CHANGE NO.	DATE

DEC PART NUMB: 23094A1-A07
ORIGINATOR: BOB PRATT
DATE OF ORIGIN: 2/28/75

DECIMAL LOC	OCTAL LOC	BINARY DATA	OCTAL DATA
0	00	00111100	074
1	01	00111100	074
2	02	00111100	074
3	03	00111100	074
4	04	00111100	074
5	05	00111100	074
6	06	00111100	074
7	07	00111100	074
8	10	00111100	074
9	11	00111100	074
10	12	00111100	074
11	13	00111100	074
12	14	00001100	014
13	15	00111100	074
14	16	00011100	034
15	17	00111100	074
16	20	00011000	030
17	21	00111100	074
18	22	00011100	034
19	23	00111100	074
20	24	00010100	024
21	25	00111100	074
22	26	00011100	034
23	27	00111100	074
24	30	00011100	034
25	31	00111100	074
26	32	00011110	036
27	33	00111100	074
28	34	00011101	035
29	35	00111100	074
30	36	00011100	034
31	37	00111100	074

DEC PART NUMB: 23-095A1-A07
ORIGINATOR: BOB PRATT
DATE OF ORIGIN: 2/28/75

DECIMAL LOC	OCTAL LOC	BINARY DATA	OCTAL DATA
0	00	11111111	377
1	01	11111111	377
2	02	11111111	377
3	03	11111111	377
4	04	11111111	377
5	05	11111111	377
6	06	11111111	377
7	07	11111111	377
8	10	11111111	377
9	11	11111111	377
10	12	11111111	377
11	13	11111111	377
12	14	11011111	337
13	15	11111111	377
14	16	11111111	377
15	17	11111111	377
16	20	10001111	217
17	21	11111111	377
18	22	11111111	377
19	23	11111111	377
20	24	11010001	321
21	25	11111111	377
22	26	11111111	377
23	27	11111111	377
24	30	01000010	102
25	31	11111111	377
26	32	11111111	377
27	33	11111111	377
28	34	11111111	377
29	35	11111111	377
30	36	11111111	377
31	37	11111111	377

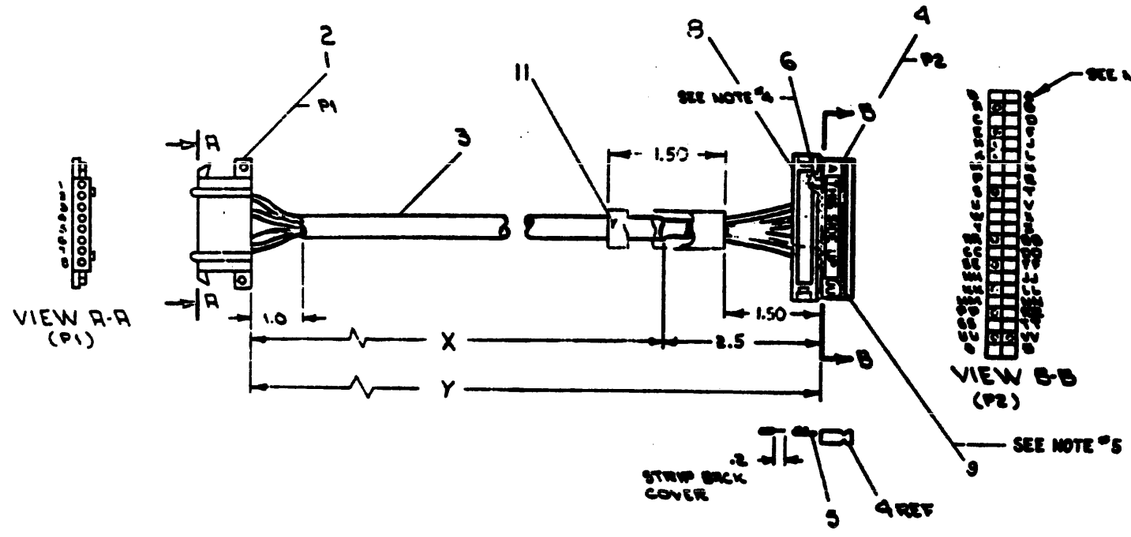
WIRE TABLE

ITEM NO.	DESCRIPTION AWG	DESCRIPTION COLOR	PAIR NO.	FROM CONNECTION	FROM WITH	TO CONNECTION*1	TO WITH
3	22	BLK	1	P1-2	2	P2-KK	5
3	22	WHT	1	P1-3	2	P2-S	
3,7		SHIELD	1	SEE NOTE #2	—	P2-R(NOTE #3)	
3		BLK	2	P1-4	2	P2-EE	
3		WHT	2	P1-5	2	P2-RR	
3,7		SHIELD	2	SEE NOTE #2	—	P2-UU(NOTE #3)	
3		BLK	3	P1-6	2	P2-PP	
3		GRN	3	P1-7	2	P2-K	
3,7	1	SHIELD	3	SEE NOTE #2	—	P2-VV(NOTE #3)	1
6	22	BLK	—	P2-L	3	P2-H	8

LEGEND

VARIATION	LENGTH X	LENGTH Y
7008360-0	45 IN ±10	27 IN ±10
7008360-1	45 IN ±10	48 IN ±10
7008360-9	SPEC'D SUM OF 27 IN ± 2 IN	

NOTES:
1. # ASTERISKS INDICATE CAVITIES NOT USED OR DESIGNATED BY LETTERS.
2. DRAIN WIRES TO BE CUT BACK TO OUTER INSULATION ON P1 END OF CABLE ONLY. SHIELDS TO BE CUT BACK TO OUTER INSULATION ON BOTH ENDS OF CABLES.
3. STRAIN WIRES ON P2 END OF CABLE TO BE EACH ENCLOSED WITH ITEM#7 (TUBING) FROM END OF CABLE JACKET TO POINT WHERE THEY ENTER P2 CONNECTOR.
4. ITEM#6(WIRE) TO BE APPROXIMATELY ONE(1) INCH LONG.
5. PLACE ITEM#9("THIS SIDE UP" STICKER) ON LETTERED SIDE OF ITEM#4(BERG HOUSING) AS SHOWN.



ITEM	QTY.	DESCRIPTION	PART NO.
11	1	LABEL, CABLE IDENT	3616073
10	A/R	TUBING, SHRINK	9107252-00
9	1	LABEL, THIS SIDE UP	3611567
8	1	STRAIN RELIEF	1211166
7	A/R	TUB. THINWALL, NAT	9107267-11
6	A/R	WIRE, #22 AWG STRD TEF BLK	9107550-00
5	11	SOCKET, CRIMP# 47216	1810009-01
4	1	HOUSING, BERG #65043-015	3103118-15
3	A/R	CABLE, BELDEN #8777-8PR SHLD	9107725-0
2	6	CONTACT MATE-N-LOCK (FEMALE)	1209379-03
1	1	CONN. MATE-N-LOCK (FEMALE)	1209340-00

PARTS LIST

REVISIONS			
DWR	CHANGE NO	REV	
C. LABE	000	B	
E. CLARK			
2 W	7008360-0000	C	
E. CLARK	11-23-70		
B. REGAN			
E. CLARK	2/8/71	D	
REGAN			
A. LEMIRE	3/8/74		
M.S. LEMIRE	2-11-74	E	
M. MAHAN			
M. MAHAN	2-28-74	F	
7008360-0000			
E. HARRINGTON	5-8-74	G	
7008360-ML000			
E. HARRINGTON	5-8-74	H	

FIRST USED ON OPTION / MODEL: PDP-8E

NEXT HIGHER ASSY: A ML-KL8-E-0

SEE PARTS LIST

DRAWN		DATE 11-23-70
CHECKED		DATE 4-6-71
ENGR		DATE 4-6-71
MFG		DATE 4-6-71
QUAL		DATE 4-6-71

EQUIPMENT CORPORATION

TITLE: CABLE ASSEMBLY (KL8E)

SIZE/CODE: D | NUMBER: IA 7008360-0-0 | REV: J

SCALE: NONE | SHEET: OF | DWG:

WIRE TABLE

ITEM NO.	DESCRIPTION AWG	DESCRIPTION COLOR	FROM CONNECTION	FROM WITH	TO CONNECTION	TO WITH
1	26	BLU/WHT	P1-1 *	12	J1-W	7
		WHT/BLU	P1-2	8	J1-F	
		ORN/WHT	P1-3	1	J1-J	
		WHT/ORN	P1-4		J1-V	
		GRN/WHT	P1-5	1	J1-T	
		WHT/GRN	P1-6	8	J1-Z	
		GRN/WHT	P1-7 **	12	J1-UU	
		WHT.BRN	P1-8	8	J1-BB	
		SLA/WHT	P1-9	1	J1-Y	
		WHT.SLA	P1-10		J1-W	
		BLU/RED	P1-11		J1-FF	
		RED/BLU	P1-12		J1-JJ	
		ORN/RED	P1-13		J1-D	
		SLA/RED	P1-14		J1-LL	
1	26	SLA/GRN	P1-15		J1-N	7

ITEM NO.	DESCRIPTION AWG	DESCRIPTION COLOR	FROM CONNECTION	FROM WITH	TO CONNECTION	TO WITH
1	26	RED/BRN	P1-16	8	J1-NN	7
		SLA	P1-17		J1-R	
		RED/SLA	P1-18		J1-U	
		BLU/BLK	P1-19		J1-P	
		BLK/BLU	P1-20		J1-DD	
		ORN/BLK	P1-21		J1-MM	
		BLK/ORN	P1-22		J1-X	
		GRN/BLK	P1-23		J1-RR	
		BRN/RED	P1-24		J1-C	
		RED/ORN	P1-25	3	J1-C	
		SHIELD	P1-1 *	12	J1-A	
1		SHIELD	P1-7 **	12	J1-B	7
3		BLK	P1-1 *	12	P1-7 **	12
2	26	RED	J1-E	7	J1-M	7

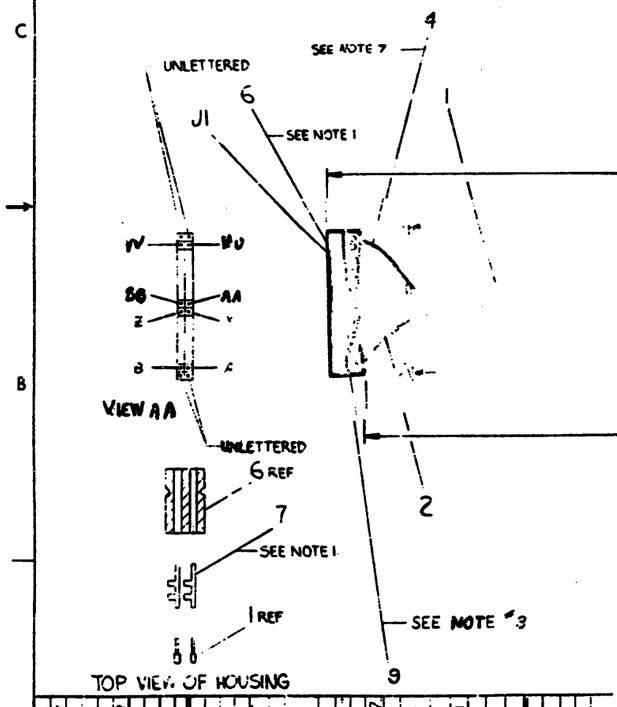
NB
* DENOTES THREE WIRES ARE SOLDERED INTO THE P1-1 SOLDER CUP
** DENOTES THREE WIRES ARE SOLDERED INTO THE P1-7 SOLDER CUP

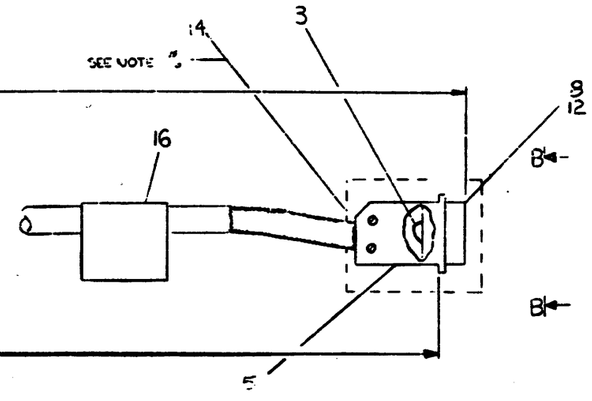
LEGEND

NUMBER	VARIATION DIM X	VARIATION DIM Y (PRECUT)
BCØ5C-25	25"±3"	25"1.8"
BCØ5C-5Ø	5Ø"±2%	5Ø"1.8"
BCØ5C-Ø9	9"±3"	9"1.8"
BCØ5C-1F	18"±1	19.8"
BCØ5C-2F	3Ø"±1"	31.8"

NOTES:

1. MANUFACTURING SHOULD USE MACHINE CRIMPER TOOL FOR CRIMPING PINS (ITEM #7) MUST BE HT68 FROM BERG ELECT
2. ONLY DEC PART "12109I8-15 MAY BE USED AS J1.
3. PLACE ITEM #9 ("THIS SIDE UP" STICKER) ON LETTERED SIDE OF ITEM #6 (BERG HOUSING) AS SHOWN.
4. ~~USE ITEM #12 (9107256-00) HEAT SHRINK TUBING TO PREVENT SHORTING OF P1 AND THE SOLDER CUPS~~
5. USE ITEM #12 (9107256-00) HEAT SHRINK TUBING TO PREVENT SHORTING SOLDER CUPS TO PREVENT SHORTING.
6. DUE TO ± TOLERANCES WITH DIFFERENT VENDORS THE HOOD (ITEM #5) MAY VARY IN OUTSIDE DIAMETER CAUSING POTENTIAL STRAIN RELIEF GRIPPING PROBLEM SHOULD THIS CONDITION BE PRESENT USE ITEM #4 (9107834) AT JUNCTION OF CABLE AND HOOD
7. PLACE ITEM #4 (9107834) OVER SHIELD WIRE J1-A, J1-B, P1-1, P1-7





ITEM NO.	QTY	DESCRIPTION	PART NO
1	1	LABEL, CABLE IDENTIFICATION	3G1G073-00
15	1	HOOD	12104935Ø
14	A/R	TAPE, DOUBLE SIDED	9007834
13	1	MALE SCREW	12104I3-51
12	2	PIN CONTACT	1211241
11	2	~~TIE WRAPS~~	~~9007031~~
10	1	~~NAME LABEL~~	~~9009532~~
9	1	LABEL, THIS SIDE UP	3611567
8	23	PIN 24-2Ø AWG	1210493-43
7	23	SOCKET, #HT-68	1210089-5
6	1	HOUSING, #2Ø383 BERG	12109I8-15
5	1	SHELL AND INSERT MALE	1210493-31
4	A/R	TUBING, #22 AWG TEF BLK	9107256-ØØ
3	A/R	WIRE, #26 AWG STRD TEF BLK	9107636-ØØ
2	A/R	WIRE, #26 AWG STRD TEF RED	9107636-22
1	A/R	CABLE, 25 CONDUCTOR #26 AWG	9107736

FIRST USED ON OPTION/MODEL: DN11

PARTS LIST

UNLESS OTHERWISE SPECIFIED IN VERSION IN INCHES
TOLERANCES
DECIMALS: XXX .005, XX .02, X .1
ANGLES: ±0° 30'
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓
MATERIAL —
FINISH —

DRN S Roberts DATE 11/11/11
CHK T Cook DATE 11/21/11
ENG DATE
PROJ. ENG. DATE
PROD DATE
NEXT HIGHER ASSY —

EQUIPMENT CORPORATION

TITLE: CABLE, MODEM BCØ5C

SIZE D | CODE UA | NUMBER BCØ5C-Ø-Ø | REV

SCALE NONE
SHEET 1 OF 1

REVISIONS	DIR	ECN NO.	DESCRIPTION	DATE	APPROVED
REV					
A		BCØ5C-00001	ORIGINAL RELEASE	10-20-99	A. REGAN
B		BCØ5C-00002	ADDED ITEM 12	10-29-99	A. REGAN
C		BCØ5C-00003	ADDED ITEM 11	1-14-00	J. SMITH
D		BCØ5C-00004	ADDED ITEM 10	2-22-00	J. SMITH
E		BCØ5C-00005	ADDED ITEM 9	4-7-00	J. SMITH
F		BCØ5C-00006	ADDED ITEM 8	5-22-00	J. SMITH
G		BCØ5C-MK007	ADDED ITEM 7	MAR 19	R. HARRINGTON
H		BCØ5C-MK008	ADDED ITEM 6	6-15-21	R. HARRINGTON
J		BCØ5C-MK009	ADDED ITEM 4	1-14-22	J. FIELD

WIRE TABLE

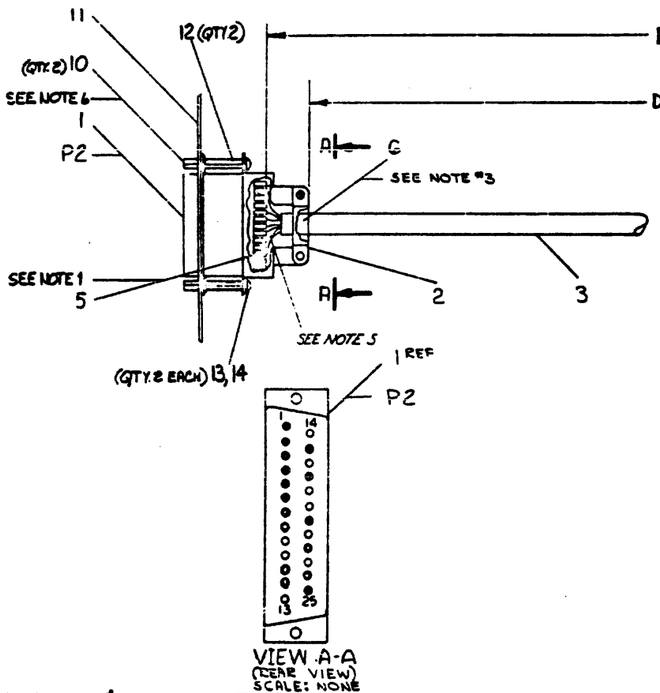
ITEM NO	DESCRIPTION AWG	COLOR	FROM CONNECTION	FROM WITH	TO CONNECTION	TO WITH
3	22	BLK	P1-VV	7	P2-7	SOLDER
↓	↓	GRN/WHT	P1-C	↓	P2-25	↓
		GRN/BLK	P1-JJ		P2-12	
		ORN/BLK	P1-FF		P2-11	
		RED	P1-DD		P2-20	
		GRN	P1-BB		P2-8	
		YELLOW/WHT	P1-Z		P2-6	
		ORN	P1-X		P2-22	
		BLU	P1-V		P2-4	
		WHT	P1-T		P2-5	
		BLU/BLK	P1-R		P2-17	
		BLK/WHT	P1-N		P2-15	
		RED/WHT	P1-L		P2-24	
		WHT/BLK	P1-J		P2-3	
↓		RED/BLK	P1-F	↓	P2-2	SOLDER
8	↓	BLK	P1-E	7	P1-M	7
8	22	BLK	P2-1	SOLDER	P2-7	SOLDER

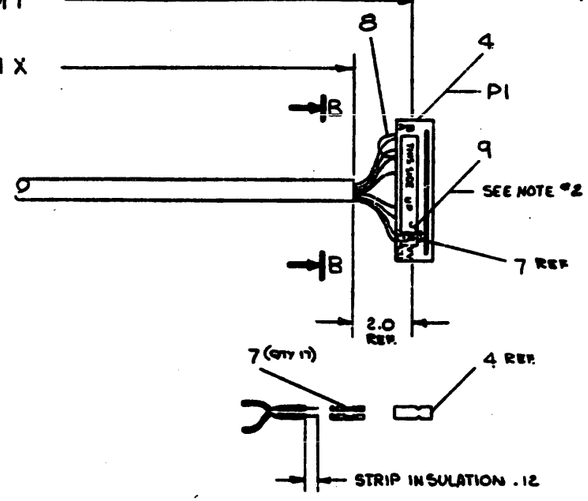
LEGEND

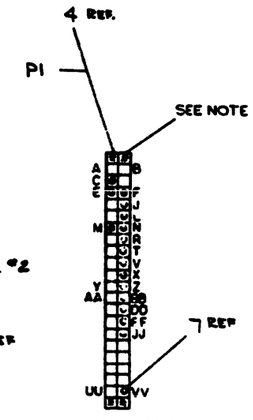
NUMBER	VARIATION DIM "X"	DIM "Y" PRECUT
BCØ3L-10	10FT ± 2IN	10FT, 5IN
BCØ3L-5	5FT ± 2IN	5FT, 5IN
BCØ3L-1K	1FT 9IN ± 1IN	2FT
BCØ3L-Ø1	1FT ±1IN	1FT, 3IN

NOTES

1. EACH SOLDERED CONN ON P2 SHALL BE INSULATED WITH A .25 PIECE OF SHRINK TUBING (ITEM #5)
2. PLACE ITEM #9 (THIS SIDE UP STICKER) ON LETTERED SIDE OF ITEM #4 (CONN HOUSING) AS SHOWN.
3. FOR STRAIN RELIEF WRAP 2 TURNS OF TAPE (ITEM #6) AROUND CABLE (ITEM #3) AS SHOWN.
4. PINS MARKED * IN VIEW B-B ARE NOT USEABLE
5. WIRES COMING FROM CENTER OF PLUG CONN SHOULD BE SIZE 26. ALL OTHERS SHOULD BE CONFINED INTO HOOD OF CONN SO THAT THEY'RE NOT BUNCHED.
6. PLACE LOCKWASHER (SUPPLIED WITH ITEM #10) BETWEEN SPACER AND CONNECTOR FLANGE. DISCARD NUT (QTY 2) SUPPLIED WITH ITEM #10.







2	WASHER, LOCK #4	9006688	14
2	SCR, PHL PAN HD #4-40 X .25	9008301-1	13
2	SPACER, THREADED, HEX	9008833	12
1	PLATE, CONN. MTG.	B-MD-7111776-00	11
2	SCREW LOCK ASSY	9008951-00	10
1	LABEL (THIS SIDE UP)	3611567	9
3IN	WIRE, STRANDED #22 AWG IPVC (BLK)	9107350-00	8
17	SOCKET, CRIMP	1210089-07	7
A/R	TAPE, DOUBLE SIDED .50 W.D.	9007834	6
16	TUBING, HEAT SHRINK .12	9107253-09	5
1	CONN, 44 POS, HSG.	1210918-15	4
A/R	CABLE, 15 COND, 22 AWG.	9107672-00	3
1	HOOD, CONN.	1212516-00	2
1	CONNECTOR, PLUG, FILTERED	1214031-00	1

RELEASED	CHANGE NO.	REV
ENG	1-01-00002	A
B. SAMPSON 4-25		
B. SAMPSON 10-3-75	1-01-00003	B
M.E. LEVANDOWSKI	1-01-00004	C
R. SAMPSON	1-01-00005	D
T. ORR	1-01-00006	E
T. ORR	BC03L-MK0007	F

DESCRIPTION: FILTERED CABLE ASSY BC03L
DWG PART NO: BC03L-Ø Ø
ITEM NO.
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
ANGLES ±0° 30'
SURFACE QUALITY IN MICROINCHES
CLASS OF ACCURACY (CHECK ONE)
NOMINAL SIZE RANGE INCHES: OVER 0 TO .12; OVER .12 TO .40; OVER .40 TO 1.2; OVER 1.2 TO 4.0; OVER 4.0 TO 12.0; OVER 12.0 TO 40.0; OVER 40.0 TO 120
MEDIUM: ±.005 ±.008 ±.012 ±.016 ±.024 ±.04
PREFERRED: ±.012 ±.010 ±.020 ±.04 ±.060 ±0.1
QUANTITY & VARIATION
THIRD ANGLE PROJECTION
REMOVE BURRS AND BREAK SHARP CORNERS
DO NOT SCALE DWG
MATERIAL SEE PARTS LIST
FINISH
DRN
CHK
ENG
PROJ
PROD
NEXT HIGHER ASSY
FIRST USED ON
SIZE D | CODE UA | NUMBER BC03L-Ø Ø | REV F
SCALE 1/1
SHEET 1 OF 1
DIST.

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

ENGINEERING SPECIFICATION

DATE 2-28-77

TITLE DL11-W Installation Procedure

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	ECO CHANGE	00002	B. CRAMM	8-77	B. Pratt	8-77

ENG	APPD	SIZE	CODE	NUMBER	REV
Bob Pratt	B. Pratt	A	SP	DL11-W-2	A

DEC 16-13821-1078-N971
DRA 107

ENGINEERING SPECIFICATION — CONTINUATION SHEET

TITLE DL11-W Installation Procedure

DL11-W Installation Procedure

Installation of the M7856 module consists of the following preparations:

1) Switch selection of the address mode and register addresses.

2) Switch selection of vector address.

3) Switch selection of data format.

4) Switch selection of receiver and transmitter baud rates.

5) Switch selection of operation mode for the current loops.

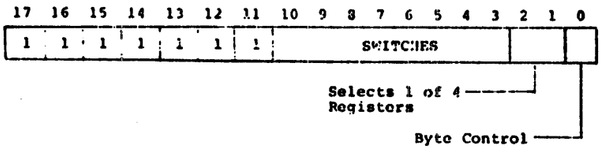
6) Additional switch selections for compatability.

7) Installation of G9000 in systems where +15V is not available.

NOTE: The notation used to indicate a particular switch is as follows: SX-Y where X denotes the particular switch pack and Y denotes the individual switch in the pack. The switch pack is labeled on the P. C. board with an SX(ie S2) and the individual switches are labeled on the switch pack as are the on-off positions.

A. Register Address Assignments:

The DL11-W can respond to addresses with the following format:



The DL11-W can be operated in one of three different address selection modes. Normally, a DL11-W used as console terminal control would operate in the first mode, whereas additional DL11-W's would be operated in the second mode. The third mode is not normally used, but is included here for completeness.

SIZE	CODE	NUMBER	REV
A	SP	DL11-W-2	A

DEC FORM NO DEC 16 (1381) 1022 N370
DRA 108

ENGINEERING SPECIFICATION — CONTINUATION SHEET

TITLE DL11-W Installation Procedure

Mode 1: Both the serial line unit and the real-time clock sections can be addressed. Due to common address selection logic, operation in this mode requires that the serial line unit addresses be restricted to 77756X. The line clock address is 777546.

Mode 2: Only the serial line unit section can be addressed. Address selection ranges from 74000 to 777777. Line clock is disabled and does not respond to address 777546.

Mode 3: Only the line clock section can be addressed at 777546. The serial line unit section does not respond to any address.

ADDRESS AND MODE SELECTION

Address Bit	A10	A09	A08	A07	A06	A05	A04	A03	N/A	N/A
Switch	S5-3	S5-2	S5-1	S5-4	S5-5	S5-6	S5-8	S5-7	S5-9	S5-10
Mode 1	Off	Off	Off	On	Off	Off	Off	On	Off	On
Mode 2*	Off	Off	Off	On	Off	Off	Off	On	On	Off
Mode 3	Off	Off	Off	On	Off	Off	On	On	On	On

*Address 77756X selected for serial line interface. Other addresses may be selected using SWITCH-OFF = 1 and SWITCH-ON = 0.

Note: Remove R63 from DL11-W's operated in Mode 2 to allow proper operation of a line frequency clock or DL11-W operated in Mode 1 or Mode 3.

Address assignments for serial lines are normally made in the ranges from 77650X to 77667X and from 77561X to 77617X.

B. Vector Address Assignments:

The line clock, if enabled, has a fixed vector address of 100 and cannot be changed. The serial line assignments are to floating vectors produced in the form XX0 (Receiver) and XX4 (Transmitter) where XX ranges from 00 to 77.

For a DL11-W used as the console device, the vector is 060/064. Additional DL11-W's vector addresses are floating.

SIZE	CODE	NUMBER	REV
A	SP	DL11-W-2	A

DEC FORM NO DEC 16 (1381) 1022 N370
DRA 108

ENGINEERING SPECIFICATION — CONTINUATION SHEET

TITLE DL11-W Installation Procedure

V8	V7	V6	V5	V4	V3	V2	V1	V0
						0/1	0	0

Switch Selectable for Serial Line

Vector Bit	V8	V7	V6	V5	V4	V3
Switch	S2-8	S2-7	S2-5	S2-3	S2-6	S2-4
060/064	Off	Off	Off	On	On	Off

On = 1, Off = 0

C. Selection of Data Format:

1. Data Bits

Switches S4-3 and S4-4 control the number of data bits in the serial character as follows:

S4-4	S4-3	# of Data Bits
On	On	5
On	Off	6
Off	On	7
Off	Off	8

2. Parity

Parity is controlled by switches S4-2 and S4-6 as follows:

S4-2	S4-6	Parity
Off	Off	Off
On	Off	Off
Off	On	Even
On	On	Odd

3. Stop Bits

Switch S4-5 controls the number of stop bits selected in the serial character as follows:

SIZE	CODE	NUMBER	REV
A	SP	DL11-W-2	A

DEC FORM NO DEC 16 (1381) 1022 N370
DRA 108

S4-5	# of Stop Bits
On	1
Off	2 (or 1.5 if 5 data bits are selected)

D. Baud Rate Selection:

Receiver and Transmitter baud rates are independent, so any combination may be selected.

Baud Rate Switch Selections

Baud Rate	Receiver			Transmitter		
	S3-2	S3-3	S3-5	S4-10	S3-1	S3-4
110	Off	Off	Off	On	On	On
150	On	Off	Off	Off	On	On
300	Off	On	On	On	Off	Off
600	Off	On	Off	On	Off	On
1200	Off	Off	On	On	On	Off
2400	On	On	On	Off	Off	Off
4800	On	On	Off	Off	Off	On
9600	On	Off	On	Off	On	Off

E. Current Loop Operation Mode:

Normally, current loops should be in active mode, unless interfaced to another active loop, such as to another DL11.

Active - Passive Mode Selection

Transmitter	S1-1	S1-2	S1-3	S1-6	S1-7
Active	On	On	Off	Off	On
Passive	Off	Off	On	On	Off
Receiver	S3-6	S3-7	S3-8	S3-9	S3-10
Active	On	Off	On	Off	On
Passive	Off	On	Off	On	Off
Reader Enable	S1-4	S1-5	S1-8	S1-9	S1-10
Active	On	Off	On	Off	On
Passive	Off	On	Off	On	Off

F. Compatability Selection:

Switches S4-1 and S4-7 allow the DL11-W to be configured to replace DL11-A, B, C, and D options in most applications.

DL11-W Compatability Switches

Selectable	Switch	Description
Break Bit	S4-1	Enabled in the ON position. Should be disabled (switch OFF) if replacing a DL11-A, or DL11-B should be enabled (switch ON) if replacing a DL11-C or DL11-D.
Error Bits	S4-7	Error bit reporting is enabled in the ON position. Should be disabled if replacing DL11-A or DL11-B, and should be enabled if replacing DL11-C or DL11-D.

Note: Both EIA level and current loop signals are available at the berg connector on the module. No selection is necessary. The proper cable will pick up the correct signals.

G. G8000 Installation:

For DL11-W EIA operation, a positive voltage is required between 9 and 15 volts to operate the EIA drivers. For PDP-11/20 and PDP-11/15 systems with the H720 power supply, a G8000 module must be installed to provide this voltage. Using a filter network, this module converts the full-wave rectified "+8V" signal to a positive DC voltage.

1. Install G8000 into slot A02 or DD11-A.
2. Wire A03V2 to A02V2.
3. Wire A02N2 to CXXU1 where XX is the slot location of the M7856.

H. DL11-W Systems with +15V Available Using DD11-A

There is a special situation of using a DD11-A to mount a DL11-W in systems with +15V available. These systems have +15V available, and it appears at pin A03V2 of the DD11-A when using power harness such as 7009177, 7008855, or 7008909. In this situation, no G8000 is necessary, and +15V can be wired directly from A03V2 to CXXU1, where XX is the slot number of the DL11.

I. When using the DL11-W in an 11/05 processor pin CXXU1 has +15V available on it so no G8000 or no jumpers are required.

J. INSTALLATION

The DL11-W module plugs into an SPC slot. A wire must be installed to pick up the LTC L signal from the power supply and apply it to the line frequency input of the DL11-W.

When installed, the LTC L input to the DL11-W is located on pin CD1. Connect a length of 30 AWG wire from pin CD1 on the backplane to the pin on the backplane, as designated in Table 1-1, for each application.

Table 1-1 LTC L Connection

PDP Computer	Processor	Pin Number
11/04	KD11-D (4 slot)	C02D1,C03D1,C04D1
11/04	KD11-D (9 slot)	C02D1,C03D1,C04D1,C05D1, C06D1,C07D1,C08D1, or C09D1
11/05	KA11-A w/8K memory	C01D1,C02D1,C03D1,C04D1, or F08V2
11/05	KD11-A w/16K memory	C01D1 or F08V2
11/20	KA11	A13P2 or B12R1
11/34	KD11-E	C03D1,C04D1,C05D1,C06D1, C07D1,C08D1, or C09D1
11/35	KD11-A	F03R1 or C09D1
11/40	KD11-A	F03R1 or C09D1
11/45	KB11-A	C26D1,C27D1, or C28D1
11/55	KB11-D	C26D1,C27D1, or C28D1
11/70	KB11-B	C40D1,C41D1,C42D1,C43D1, or C44D1
11/70	KB11-C	C40D1, C41D1,C42D1,C43D1, or C44D1
DD11-B Peripheral Mounting Panel		C01D1,C02D1,C03D1, or C04D1
DD11-D Peripheral Mounting Panel		C01D1,C02D1,C03D1,C04D1,
DD11-A Peripheral Mounting Panel		C05D1,C06D1,C07D1,C08D1,C09D1 A03P2

NOTE: A wire connection is not necessary for backplane pin numbers ending in D1. LTC L is already connected to the line frequency input of the DL11-W.

K. Installation

The DL11-W module plugs into an SPC slot. A wire must be installed to pick up the DCLOL signal from the power supply and apply it to the DCLO input of the DL11-W.

When installed, the DCLOL input to the DL11-W is located on pin CN1. Connect a length of 30 AWG wire from pin CN1 on the backplane to the pin on the backplane, as designated in Table 1-2 for each application.

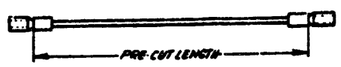
Table 1-2 DCLOL Connection

PDP Computer	Processor	Pin Number
11/04*	KD11-D (4 slot)	C03N1, C04N1
11/04*	KD11-D (9 slot)	C03N1 thru C09N1
11/05*	KA11-A w/8K Memory	C01N1, C02N1, C03N1, C04N1
11/05*	KD11-A w/16K Memory	C01N1
11/20	KA11	B11F2, B14F2, A13S2, A08S2, A03S2, B04D2, F06B2
11/34*	KD11-E	C03N1 thru C09N1
11/35	KD11-A	C09F2
11/40	KD11-A	C09F2
11/45*	KB11-A	C26N1, C26N1, C28N1
11/55*	KB11-D	C26N1, C26N1, C28N1
11/70*	KB11-B	C40N1, C41N1, C42N1, C43N1, C44N1
11/70*	KB11-C	C40N1, C41N1, C42N1, C43N1, C44N1
DD11-B Peripheral Mounting Panel		C01N1 thru C04N1
DD11-D Peripheral Mounting Panel		C01N1 thru C09N1
DD11-A Peripheral Mounting Panel		B01F2, B04F2, A03S2

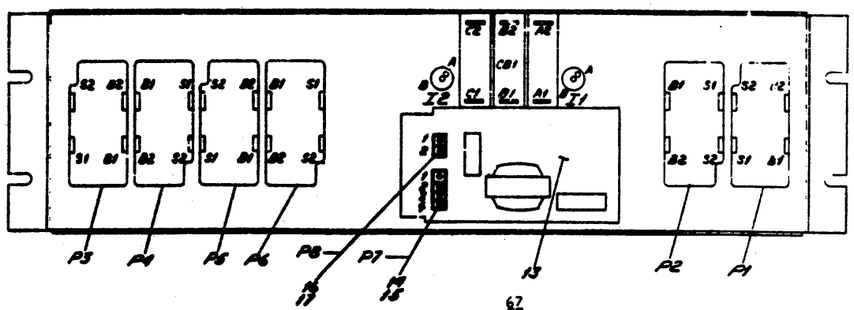
*NOTE: A wire connection is not necessary for backplane pin numbers ending in N1 DCLOL. Is already connected to the input of the DL11-W.

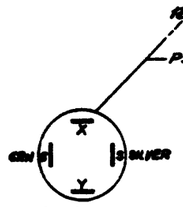
SECTION II
POWER SYSTEM ENGINEERING DRAWINGS

LEGEND			
DWG. NO.	VARIATION VACUUM	PHASES	AMPS OUT
861-A	120	2	32
861-B	240	1	16
861-C	120	1	24
861-F	120	1	12

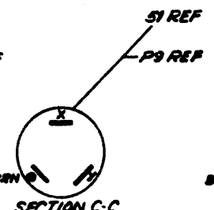


DETAIL 'A'
SCALE: NONE

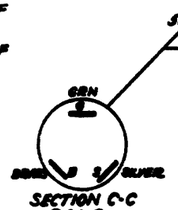




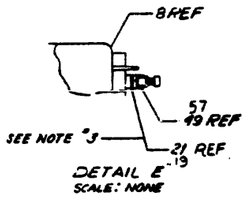
SECTION C-C
861-A
SCALE: NONE



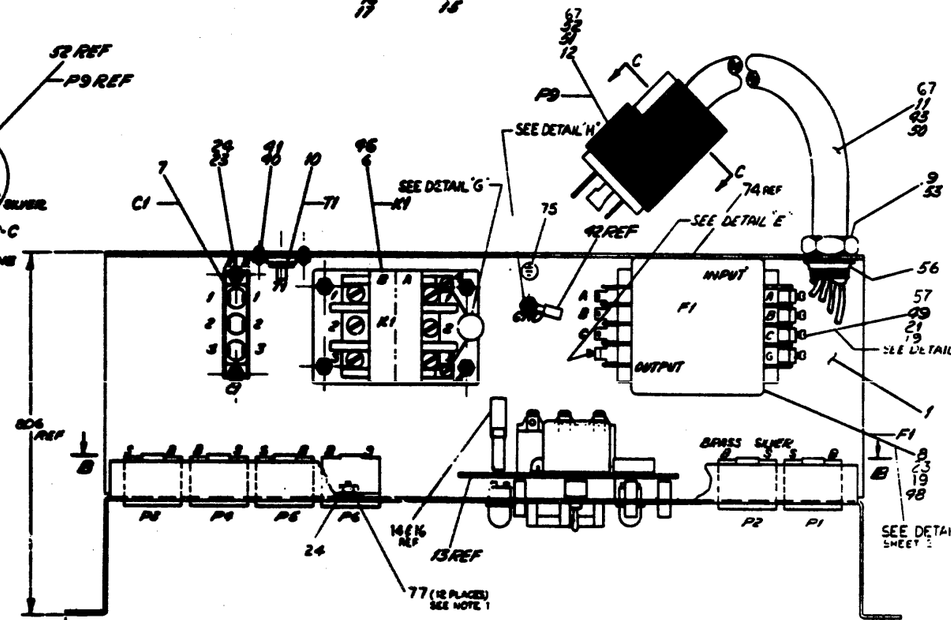
SECTION C-C
861-B
SCALE: NONE

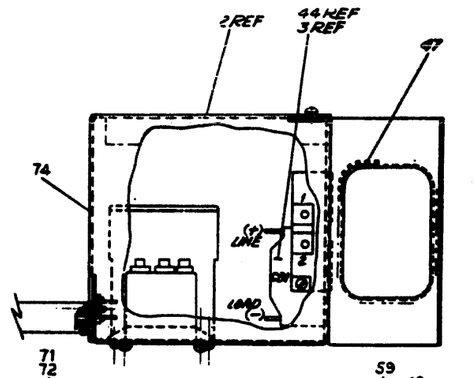


SECTION C-C
861-C
SCALE: NONE



DETAIL 'E'
SCALE: NONE





DETAIL 'G'
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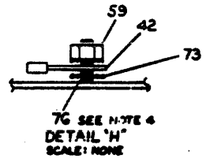
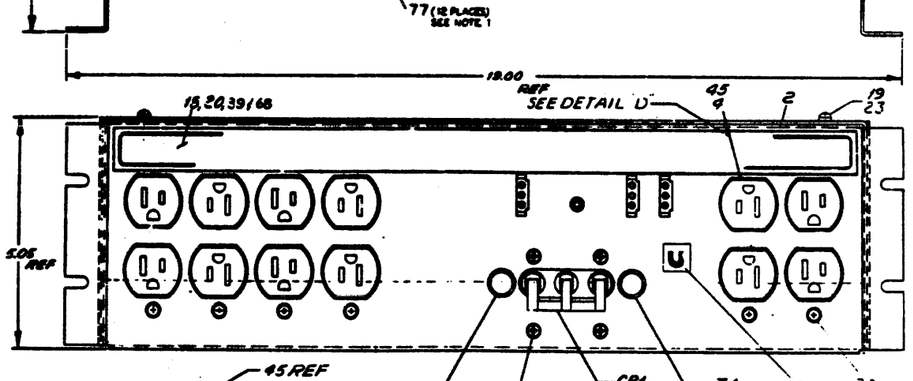


DETAIL 'H'
SCALE: NONE



DETAIL 'D'
ARRANGEMENT FOR
861-B

QTY.	DESCRIPTION	PART NO
1	CHASSIS, 861 P.C.	B-CD-861-0
1	COVER, 861 P.C.	D-AD-861-0
1	CIRCUIT BREAKER, 20 AMP 1 POLE	1811-32
1	FILTER 3 POLE 6 WIRE	1711187
1	CONTACTOR 115 V	KP11947-0
2	LAMP, PORRO 115 V	4005357
6	RECEPTACLE 15A, 115 VAC	1205351
1	CAPACITOR	4000039
1	THERMOSTAT	KP11158
1	STRAIN RELIEF (GRN)	1211198-01
1	FILTER 3 POLE 6 WIRE	1711187
1	FUSE RKB, 1.5/250V 20A	1811065
1	POWER CORD 18FT. 12/6	1700026
1	PC BOARD ASSY	003-340206-0-1
3	PIN, FEMALE	1209379-01
3	HOUSING, 6 PIN FEMALE	1210821-9
1	HOUSING, 7 PIN MALE	1210822-2
2	PIN, MALE	1209377-01
1	NAME PLATE, 861 A	003-361121-1-66
18	SCREW, PH PAN HD #6-32 X 3/8 LG	9006021-1
6	LOCKWASHER, #6 INT TOOTH	9006433
6	NUT, KEP #6-32	9006560
4	SCREW, PH PAN HD #8-32 X 1/4 LG	9006057-1
4	NUT, KEP #8-32	9006563
4	WIRE, #18 AWG 1 PVC (RED)	9107370-22
4	WIRE, #18 AWG 1 PVC (BLK)	9107370-00
1	WIRE, #18 AWG 1 PVC (WHT)	9107370-99
1	WIRE, #18 AWG 1 PVC (GRN)	9107360-99
1	WIRE, #18 AWG 1 PVC (BLU)	9107360-00
1	WIRE, #18 AWG 1 PVC (RED)	9107360-22
1	WIRE, #18 AWG 1 PVC (ORG)	9107360-54
1	NAME PLATE, 861-F	003-361218-04
4	CONN, SOLDERLESS DUAL 1000 SERIES	9007965
29	CONN, SOLDERLESS (BLU)	9007919
1	CONN, SOLDERLESS (RED)	9007917
1	WIRE, #18 AWG 1 PVC (GRN)	9107360-99
1	WIRE, #18 AWG 1 PVC (BLK)	9107370-00
1	WIRE, #18 AWG 1 PVC (WHT)	9107370-99
1	WIRE, #18 AWG 1 PVC (RED)	9107370-22
4	NUT, KEP #8-32	9006563
4	SCREW, PH PAN HD #8-32 X 1/4 LG	9006057-1
4	NUT, KEP #6-32	9006560
18	SCREW, PH PAN HD #6-32 X 3/8 LG	9006021-1
6	LOCKWASHER, #6 INT TOOTH	9006633
1	NAME PLATE, 861 A	003-361121-1-66
2	PIN, MALE	1209377-01
1	HOUSING, 7 PIN MALE	1210822-2
3	PIN, FEMALE	1209379-01
3	HOUSING, 6 PIN FEMALE	1210821-9
1	PC BOARD ASSY	003-340206-0-1
1	FUSE RKB, 1.5/250V 20A	1811065
A/R	POWER CORD 18FT. 12/6	1700026
1	THERMOSTAT	KP11158
1	STRAIN RELIEF (GRN)	1211198-01
1	FILTER 3 POLE 6 WIRE	1711187
1	CAPACITOR	4000039
1	CONTACTOR 115 V	KP11947-0
2	LAMP, PORRO 115 V	4005357
6	RECEPTACLE 15A, 115 VAC	1205351
1	CIRCUIT BREAKER, 20 AMP 1 POLE	1811-32
1	COVER, 861 P.C.	D-AD-861-0
1	CHASSIS, 861 P.C.	B-CD-861-0
QTY.	DESCRIPTION	PART NO

861 P.C.

SEE PARTS LIST

B-CD-861-0

B UA 861-0-0 F

EQUIPMENT CORPORATION

POWER CONTROL, 861

NOTES:
1. DOTTED LINES INDICATED WINDINGS OMITTED IN E AND F VERSIONS.
2.

VERSION	TB1 JUMPERS	CB1
A	2→6, 4→8	20 A
B	4→6	15
E	2→6, 4→8	--
F	4→6	5

3. NUMBERS IN ( ) INDICATE XFORMER LEAD NUMBERS ON E&F VERSION.
4. ~~6 CKTS TERMINATE CONNECTORS.~~
5. ~~FAST-ON CONNECTIONS.~~

QTY	REF. DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

FIRST USED ON OPTION MODEL: H742Ø

SEMICONDUCTOR CONVERSION CHART

DEC NO.	EIA NO.	DEC NO.	EIA NO.

DRN		DATE 1-17-73
CHK		DATE 2-27-73
ENGR		DATE 3/1/73
PROJ ENGR		DATE 3/1/73
PROD		DATE 3/5/73

NEXT HIGHER ASSY

SCALE

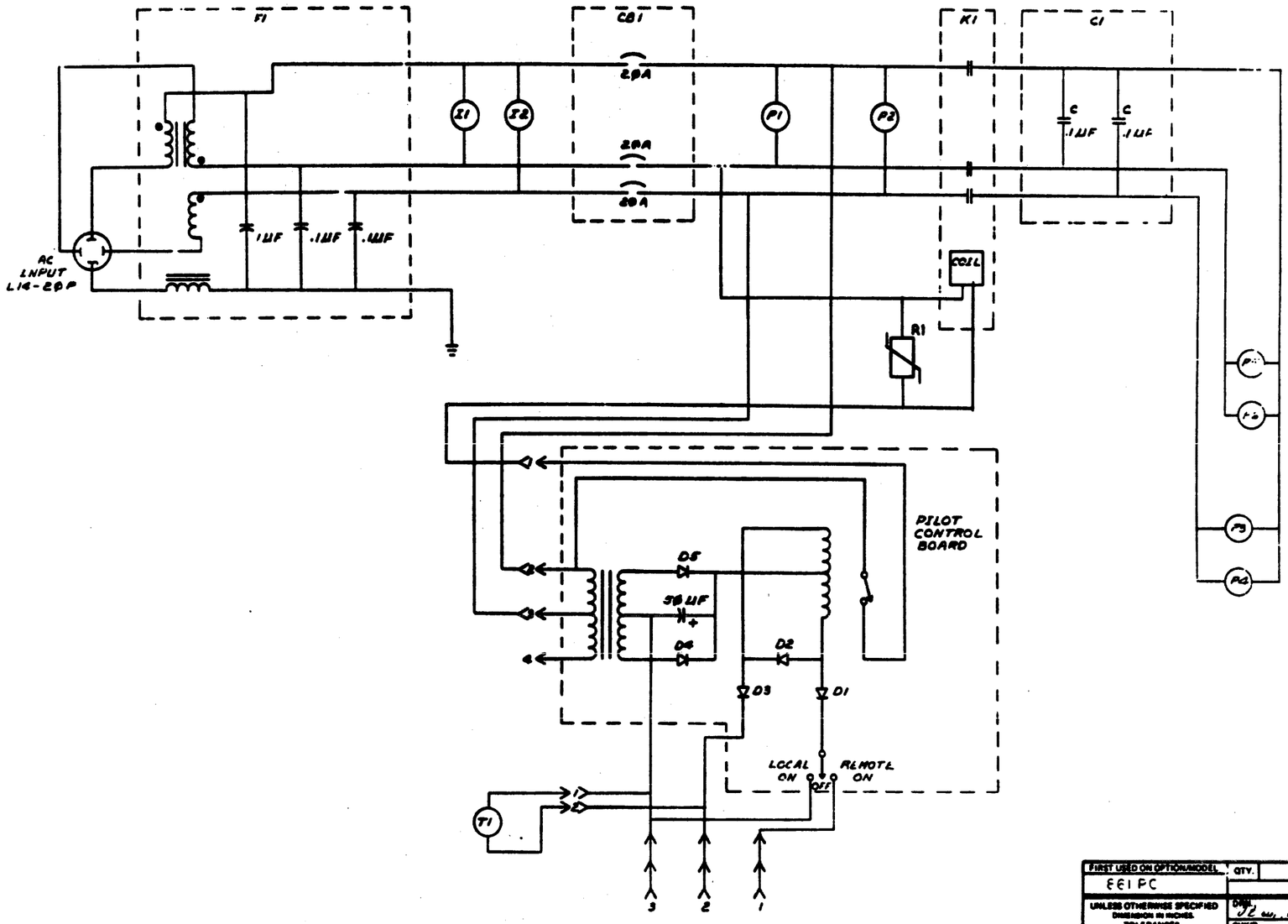
SHEET 1 OF 1

digital

TITLE: WIRING DIAGRAM

SIZE D | CODE CS | NUMBER H742Ø-Ø-1 | REV A

DWG.



FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO	ITEM NO.
661 PC		PARTS LIST		

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES
DECIMALS: XXX ± .005; XX ± .02; X ± .1
ANGLES: ± 1° 30'
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓
MATERIAL —
FINISH —

DRN. [illegible] DATE 9-11-72
CHK'D [illegible] DATE 10-6-72
ENG. [illegible] DATE
PROJ. ENG. [illegible] DATE
APPD. [illegible] DATE

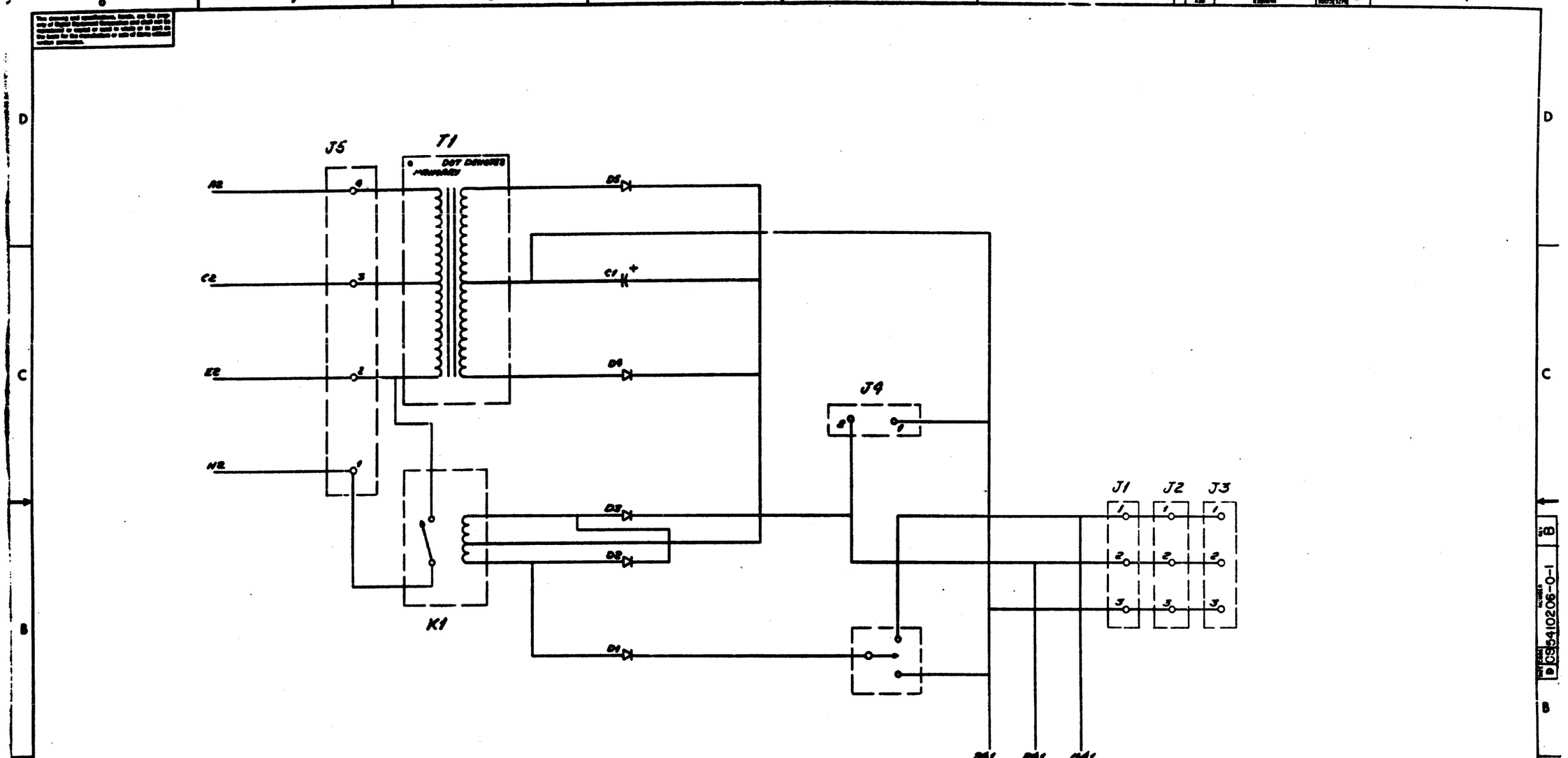
NEXT HIGHER ASSY. B-DD-561-C
SCALE —
SHEET 1 OF 1

DIGITAL EQUIPMENT CORPORATION
MAYNARD MASSACHUSETTS

TITLE
CIRCUIT
SCHEMATIC
(661-A P.C.)

SIZE D | CODE CS | NUMBER 861-A-1 | REV. B
DIST.

REVISIONS				
DIR	CHANGE NO.	REV.		
[illegible]	191-00006	A	[illegible]	[illegible]
[illegible]	191-00009	B	[illegible]	[illegible]



FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
861 P.C.		PARTS LIST		

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES
DECIMALS: XXX ± .005, XX ± .02, X ± .1 — ANGLES: ±0° 30'
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓
MATERIAL —
FINISH —

DRN.	DATE 9-25-70	digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS
CHK'D.	DATE 7-11-71	
ENG.	DATE 9-15-71	
PROJ. ENG.	DATE 9-16-71	
PROD.	DATE 9-21-71	

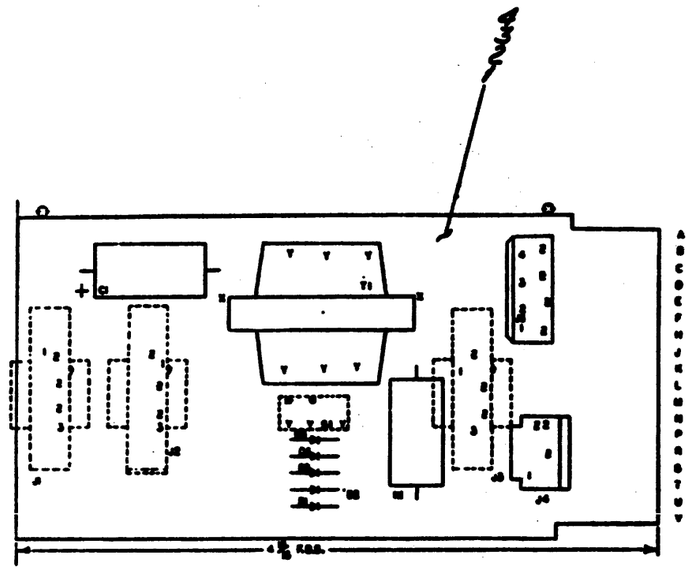
NEXT HIGHER ASSY. —

TITLE: PILOT CONTROL

SIZE D | CODE IDENT NO. CS | NUMBER DCS 5410206-0-1 | REV. B

SCALE NONE | SHEET 2 OF 2 | DIST.

NOTES:



QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.
		PACKAGING INSTRUCTION	A-PI-3700143-0-0	15
1	S1	SWITCH, 3-POS.	12-11190	14
1	K1	RELAY, REED	12-11179	13
1	T1	PC TRANSFORMER	16-11173	12
9	FOR USE ON J5	PIN, PC MALE MATE-N-LOCK	1210833	11
1	J9	SOCKET, 2 PIN MATE-N-LOCK	1210832-02	10
11	FOR USE ON J1-J4	PIN, PC FEMALE MATE-N-LOCK	1209956	9
1	J5	PLUG, 9 PIN MATE-N-LOCK	1209351-01	8
3	J1, J2, J3	SOCKET, 7 PIN MATE-N-LOCK	1209350-03	7
5	D1-D5	DIODE IN 4004	1105796	6
1	C1	CAP, 5.0 μF, 50V 6% MYLAR	1100380	5
REF		MODULE ECO HISTORY	D-WG-5910206-0-6	4
REF		ASSY DRILLING HOLE LAYOUT	D-WG-5910206-0-5	3
REF		X-Y COORDINATE HOLE LOCN.	K-CO-5410206-0-4	2
1		ETC CKT BOARD	5010205	1

PARTS LIST

PRINT USED ON OPTION MODEL: 861 PC.

ETCH BOARD REV: B

DEC NO.	EIA NO.	DEC NO.	EIA NO.

SEMICONDUCTOR CONVERSION CHART

IC TYPE	GND	+5V

GND AND 5V ARE NORMALLY PIN 7 AND 14 RESPECTIVELY UNLESS OTHERWISE NOTED ABOVE

IC PIN LOCATIONS

DRWN	A. LOYA	DATE 8-25-72
CHKD	F. Vasco	DATE 9-19-72
ENGR	R. Hamlin	DATE 9-19-72
PROJ ENGR	R. Hamlin	DATE 9-19-72
MFG ENGR	Wayne	DATE 9-19-72
NEXT HIGHER ASSY		

DIGITAL EQUIPMENT CORPORATION

TITLE: PILOT CONTROL

SIZE: D | CODE: CS | NUMBER: 5410206-0-1 | REV: B

SCALE: 2/1 | SHEET 1 OF 2 | DIST.

B 5410206-0-1 B

15

WIRE TABLE 861-A

ITEM NO.	DESCRIPTION COLOR	AWG	FROM CONN	FROM POINT	FROM WITH	TO CONN	TO POINT	TO WITH	REMARKS SEE DETAIL "A"
29	BLK	14	P1-B2		37	K1-A3		37	12.0
~~35~~	~~BLK~~	~~18~~	~~P1-B1~~		~~36~~	~~K1-A5~~		~~36~~	~~12.0~~
28	WHT	14	P1-S1		37	P2-S1		37	4.0
28	WHT	14	P1-S2		37	K1-A2		37	12.0
32	WHT	18	P2-S2		36	P7-2		15	10.0
31	RED	18	P2-B2		36	P7-3		15	10.0
27	RED	14	P2-B1		37	K1-A1		37	12.0
28	WHT	14	P3-S1		37	P4-S2		37	6.0
28	WHT	14	P3-S2		37	C1-A3		37	6.0
27	RED	14	P3-B1		37	C1-A1		37	6.0
27	RED	14	P3-B2		37	P4-B1		37	4.0
28	WHT	14	P4-S1		37	P5-S2		37	4.0
28	WHT	14	P5-S1		37	P6-S2		37	6.0
29	BLK	14	P5-B1		37	C1-A2		37	6.0
29	BLK	14	P5-B2		37	P6-B1		37	4.0
29	BLK	14	K1-B3		37	C1-B2		37	4.0
28	WHT	14	K1-B2		37	C1-B3	C	37	4.0
27	RED	14	K1-B1		37	C1-B1		37	4.0
5	BLK	14	Z1-A		—	CB1-B1	LINE+	38	—
5	BLK	14	Z1-B		—	CB1-A1	LINE+	38	—
5	BLK	14	Z2-A		—	CB1-B1	LINE+	38	—
5	BLK	14	Z2-B		—	CB1-C1	LINE+	38	—
29	BLK	14	F1-C	OUTPUT	37	CB1-A1	LINE+	37	6.0
28	WHT	14	F1-B	OUTPUT	37	CB1-B1	LINE+	37	6.0
27	RED	14	F1-A	OUTPUT	37	CB1-C1	LINE+	37	6.0
27	RED	14	K1-A1		37	CB1-C2	LOAD−	37	6.0
28	WHT	14	K1-A2		37	CB1-B2	LOAD−	37	6.0
29	BLK	14	K1-A3		37	CB1-A2	LOAD−	37	6.0
60	GRN	12	F1-G	OUTPUT	49	GND		65	6.0
~~34~~	~~BRN~~	~~18~~	[illegible]		~~36~~	[illegible]		[illegible]	~~10.0~~
35	ORN	18	P8-1		17	T1		36	10.0
35	ORN	18	P8-2		17	T1		36	10.0
11	BLK	12	P9-Y		—	F1-C	INPUT	49	
11	RED	12	P9-X		—	F1-A	INPUT	49	
11	WHT	12	P9-S		—	F1-B	INPUT	49	
11	GRN	12	P9-G		—	F1-G	INPUT	49	
[illegible]			~~S1~~			~~T5-1~~			
[illegible]			~~S2~~			~~T5-2~~			
~~34~~	~~BRN~~	~~18~~	~~T5-2~~			~~K1-4~~		~~36~~	~~3.0~~
~~34~~	~~BRN~~	~~18~~	~~T5-1~~						~~6.0~~
33	BLK	18	P1-B1		36	K1-5		37	12.0
~~34~~	~~BRN~~	~~18~~	[illegible]						~~3.0~~
34	BRN	18	P7-1		36	K1-4		37	10.0
71	—	—	R1-1	—	—	K1-4	—	—	—
71	—	—	R1-2	—	—	K1-5	—	—	—

WIRE TABLE 861-B

ITEM NO.	DESCRIPTION COLOR	AWG	FROM CONN	FROM POINT	FROM WITH	TO CONN	TO POINT	TO WITH	REMARKS SEE DETAIL A
29	BLK	14	P1-B2		37	K1-A3		37	12.0
29	BLK	14	P1-B1		37	P2-B2		37	[illegible]
28	WHT	14	P1-S1		37	P2-S1		37	4.0
28	WHT	14	P1-S2		37	K1-A2		37	12.0
32	WHT	18	P2-S2		36	P7-2		15	10.0
28	WHT	14	P3-S1		37	P4-S2		37	6.0
28	WHT	14	P3-S2		37	C1-A3		37	6.0
29	BLK	14	P3-B2		37	P4-B1		37	4.0
28	WHT	14	P4-S1		37	P5-S2		37	4.0
28	WHT	14	P5-S1		37	P6-S2		37	6.0
29	BLK	14	P5-B1		37	C1-A2		37	6.0
29	BLK	14	P5-B2		37	P6-B1		37	4.0
29	BLK	14	K1-B3		37	C1-B2		37	4.0
28	WHT	14	K1-B2		37	C1-B3	C	37	4.0
5	BLK	14	Z1-A		—	CB1-B1	LINE+	38	—
5	BLK	14	Z1-B		—	CB1-A1	LINE+	38	—
5	BLK	14	Z2-A		—	CB1-B1	LINE+	38	—
5	BLK	14	Z2-B		—	CB1-C1	LINE+	38	—
29	BLK	14	F1-C	OUTPUT	37	CB1-A1	LINE+	37	6.0
28	WHT	14	F1-B	OUTPUT	37	CB1-C1	LINE+	37	6.0
28	WHT	14	K1-A2		37	CB1-C2	LOAD−	37	6.0
29	BLK	14	K1-A3		37	CB1-A2	LOAD−	37	6.0
60	GRN	12	F1-G	OUTPUT	49	GND		65	6.0
[illegible]									~~10.0~~
35	ORN	18	P8-1		17	T1		36	10.0
35	ORN	18	P8-2		17	T1		36	10.0
[illegible]						~~P7-4~~		~~15~~	~~10.0~~
[illegible]									~~10.0~~
43	GRN	14	P9-G		—	F1-G	INPUT	49	—
43	BLK	14	P9-Y		—	F1-C	INPUT	49	—
43	WHT	14	P9-X		—	F1-B	INPUT	49	—
29	BLK	14	P4-B2		37	P6-B2		37	6.0
[illegible]									
[illegible]									
[illegible]								~~36~~	~~3.0~~
[illegible]									~~6.0~~
33	BLK	18	P7-4		15	K1-5		37	10.0
33	BLK	18				P2-B1		36	10.0
[illegible]									~~3.0~~
34	BRN	16	P7-1		15	K1-4		37	10.0
72	—	—	R1-1	—	—	K1-4	—	—	—
72	—	—	R1-2	—	—	K1-5	—	—	—

WIRE TABLE 861-C, 861-F

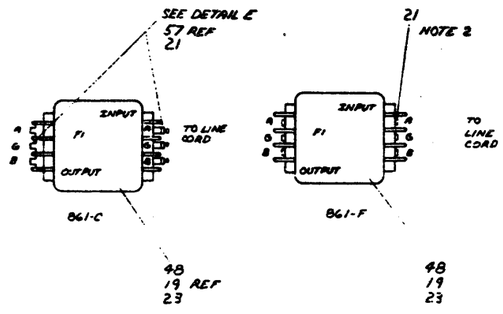
ITEM NO.	DESCRIPTION COLOR	AWG	FROM CONN	FROM POINT	FROM WITH	TO CONN	TO POINT	TO WITH	REMARKS SEE DETAIL A
29	BLK	14	P1-B2		37	K1-A3		37	12.0
~~33~~	~~BLK~~	~~18~~	~~P1-B1~~		~~36~~	[illegible]		~~36~~	~~12.0~~
54	WHT	10	P1-S1		65	P2-S1		65	4.0
54	WHT	[illegible]	P1-S2		65	K1-A2		65	12.0
32	WHT	18	P2-S2		36	P7-2		15	10.0
31	RED	18	P2-B2		36	P7-3		15	10.0
27	RED	14	P2-B1		37	K1-A1		37	12.0
54	WHT	10	P3-S1		65	P4-S2		65	6.0
54	WHT	10	P3-S2		65	C1-A3		65	6.0
27	RED	14	P3-B1		37	C1-A1		37	6.0
27	RED	14	P3-B2		37	P4-B1		37	4.0
54	WHT	10	P4-S1		65	P5-S2		65	4.0
54	WHT	10	P5-S1		65	P6-S2		65	6.0
29	BLK	14	P5-B1		37	C1-A2		37	6.0
29	BLK	14	P5-B2		37	P6-B1		37	4.0
29	BLK	14	K1-B3		37	C1-B2		37	4.0
54	WHT	10	K1-B2		65	C1-B3	C	65	4.0
27	RED	14	K1-B1		37	C1-B1		37	4.0
5	BLK	14	Z1-A		—	CB1-A1	LINE+	38	—
5	BLK	14	Z1-B		—	CB1-B1	LINE+	38	—
5	BLK	14	Z2-A		—	CB1-A1	LINE -	38	—
5	BLK	14	Z2-B		—	CB1-C1	LINE+	38	—
29	BLK	14	F1-B	OUTPUT	37	CB1-B1	LINE+	37	6.0
54	WHT	10	F1-A	OUTPUT	65	CB1-A1	LINE+	65	6.0
27	RED	14	F1-B	OUTPUT	37	CB1-C1	LINE+	37	6.0
27	RED	14	K1-A1		37	CB1-C2	LOAD−	37	6.0
54	WHT	10	K1-A2		65	CB1-A2	LOAD−	65	6.0
29	BLK	14	K1-A3		37	CB1-B2	LOAD−	37	6.0
60	GRN	12	F1-G	OUTPUT	57	GND		42	6.0
35	ORN	18	P8-1		17	T1		36	10.0
35	ORN	18	P8-2		17	T1		36	10.0
~~34~~	~~BRN~~	~~18~~	~~K1-A4~~		~~36~~	~~P7-1~~		15	10.0
50	GRN	12	P9-G		—	F1-G	INPUT	49	
50	BLK	12	P9-B		—	F1-B	INPUT	49	
50	WHT	12	P9-S		—	F1-A	INPUT	49	
[illegible]			~~S1~~			~~T5-1~~			
[illegible]			~~S2~~			~~T5-2~~			
~~34~~	~~BRN~~	~~18~~	~~T5-2~~		—	~~K1-4~~	—	36	3.0
~~36~~	~~BRN~~	~~18~~	~~T5-1~~						6.0
33	BLK	18	C1-B1		36	K1-5		37	12.0
~~34~~	~~BRN~~	~~18~~	[illegible]						~~3.0~~
34	BRN	18	P7-1		15	K1-4		[illegible]	10.0
71	—	—	R1-1	—	—	K1-4	—	—	—
71	—	—	R1-2	—	—	K1-5	—	—	—

NOTES:

1. ITEM 77 #6 EXT TOOTH WASHER MUST BE BETWEEN CHASSIS AND MOUNTING TAB OF RECEPTACLE P1-P6).
2. REMOVE FASTON TABS FOR 861F.
3. LOCKWASHER (ITEM 19 OR 21) MUST BE PLACED BETWEEN FILTER(ITEM 8) AND TERM CLAMP (ITEM 49)
4. REMOVE PAINT MASK AROUND 10-32 GROUND STUD AND COAT EXPOSED SURFACE WITH CONDUCTIVE GREASE, (ITEM 76) PLACE EXTERNAL TOOTH LOCKWASHER (ITEM 73) ON STUD FIRST, THEN CRIMP LUG (ITEM 42, AND KEP NUT (ITEM 53) LAST. SEE DETAIL "H".

WIRE TABLE 861-F

ITEM NO	DESCRIPTION COLOR	AWG	CONN	FROM POINT	FROM WITH	CONN	TO POINT	TO WITH	REMARKS SEE DETAIL A
29	BLK	14	P1-B2		37	K1-A3		37	12.0
28	WHT	14	P1-S1		37	P2-S1		37	4.0
28	WHT	14	P1-S2		37	K1-A2		37	12.0
32	WHT	18	P2-S2		36	P7-2		15	10.0
31	RED	18	P2-B2		36	P7-3		15	10.0
27	RED	14	P2-B1		37	K1-A1		57	10.0
28	WHT	14	P3-S1		37	P4-S2		37	6.0
28	WHT	14	P3-S2		37	C1-A3		37	6.0
27	RED	14	P3-B1		37	C1-A1		37	6.0
27	RED	14	P3-B2		37	P4-B1		37	4.0
28	WHT	14	P4-S1		37	P5-S2		37	4.0
28	WHT	14	P5-S1		37	P6-S2		37	6.0
29	BLK	14	P5-B1		37	C1-A2		37	6.0
29	BLK	14	P5-B2		37	P6-B1		37	4.0
29	BLK	14	K1-B3		37	C1-B2		37	4.0
28	WHT	14	K1-B2		37	C1-	C	37	4.0
27	RED	14	K1-B1		37	C1-B1		37	4.0
29	BLK	14	F1-B	OUTPUT	70	CB1-B1	LINE+	37	6.0
28	WHT	14	F1-A	OUTPUT	70	CB1-A1	LINE+	38	6.0
27	RED	14	F1-B	OUTPUT	70	CB1-C1	LINE+	37	6.0
5	BLK	18	Z1-A		—	CB1-A1	LINE+	38	—
5	BLK	18	Z1-B		—	CB1-B1	LINE+	38	—
5	BLK	18	Z2-A		—	CB1-A1	LINE+	36	—
5	BLK	18	Z2-B		—	CB1-C1	LINE+	38	—
27	RED	14	K1-A1		37	CB1-C2	LOAD−	37	6.0
28	WHT	14	K1-A2		37	CB1-A2	LOAD−	37	6.0
29	BLK	14	K1-A3		37	CB1-B2	LOAD−	37	6.0
60	GRN	12	F1-G	OUTPUT	42	GND		42	6.0
35	ORN	18	P8-1		17	T1		36	10.0
35	ORN	18	P8-2		17	T1		36	10.0
67	GRN	16	P9		—	F1-G	INPUT	—	SEE
67	BLK	16	P9		—	F1-B	INPUT	70	NOTE
67	WHT	16	P9		—	F1-A	INPUT	70	5
[illegible]									
[illegible]									
~~34~~	[illegible]								~~3.0~~
34	BRN	18	P7-1		15	K1-4		37	10.0
[illegible]									~~6.0~~
33	BLK	18	P1-B1		36	K1-5		37	12.0
71	—	—	R1-1	—	—	K1-4	—	—	—
71	—	—	R1-2	—	—	K1-5	—	—	—



DETAIL F
SCALE: NONE

DESCRIPTION | DWG./PART NO. | ITEM NO.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

QUANTITY & VARIATION

THIRD ANGLE PROJECTION

REMOVE BURRS AND BREAK SHARP CORNERS

DO NOT SCALE DWG

DRN C SCHMINT 9-12-72
CHK'D J KALAGHN 10-6-72
ENG. R BURTON 10-6-72
PROJ. ENG. ALLEN 10-6-72
PROD. P FAZIO 10-6-72

FIRST USED ON 861-PC

TITLE POWER CONTROL 861

NEXT HIGHER ASSY.

SCALE

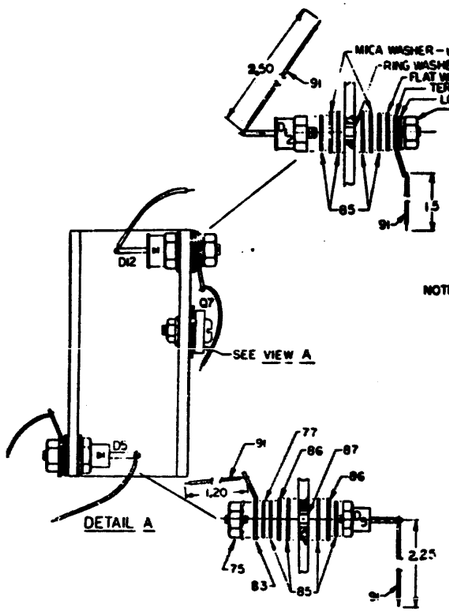
SHEET 2 OF 2

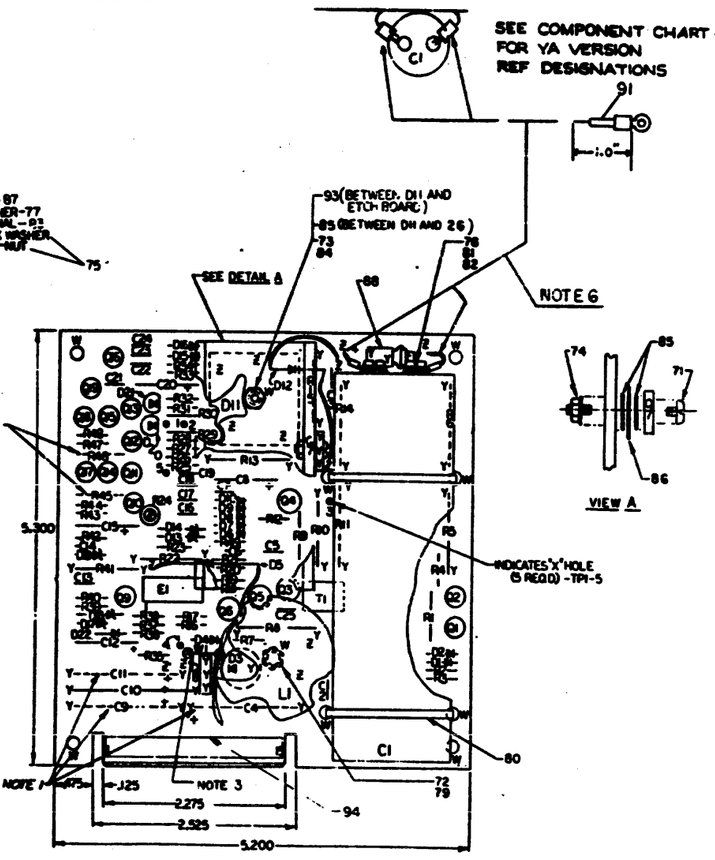
SIZE E
CODE UA
NUMBER 861-0-0
REV

16

NOTES:

1. R45, R46, C4, C9, & C11 ARE NOT USED ON BASIC MODEL BUT ARE RESERVED FOR PLANNED FUTURE MODULE VARIATIONS.
2. ~~*~~ TOTAL +15V AND +8V CURRENT NOT TO EXCEED 4.0 AMPERES.
3. W1 (TEST JUMPER) MAYBE TEMPORARILY REMOVED WHILE TROUBLE-SHOOTING TO DETERMINE IF LOSS OF 15V IS DUE TO CROW-BAR CIRCUITRY. BUT MUST BE IN THE BOARD FOR NORMAL OPERATION.
4. ~~NON-PRINTED PARTS SUPPLIED WITH D12.~~
4. YA VERSION DOES NOT CONTAIN +15VDC REG.
5. A) FOR STANDARD VERSION USE SHEETS 1, 2, 3, & 4 OF THIS DWG.
   B) FOR YA VERSION USE SHEETS 1, 2, & 3 OF THIS DWG.
6. WIRES MUST NOT EXTEND BEYOND THE DIMENSIONS OF THE BOARD.





REF	REF				
REF	REF		X-Y COORDINATE HOLE LOCATION	K-CO-5411086-0-4	1
REF	REF		ASSY/DRILLING HOLE LAYOUT	D-AH-5411086-0-5	2
REF	REF		MODULE ECO HISTORY	B-HH-5411086-0-8	3
-	1		ETCHED CIRCUIT BOARD	5011085	4
0	1	C2	CAPACITOR 56PF 100V 5%	1000812	5
4	4	C16,C17,C18,C21	CAPACITOR 330PF 100V 5%	1000823	6
3	5	C3,C13 C19,C22,C23	CAPACITOR .01uf 100V 20%	1001810-01	7
1	3	C6,C12,C15	CAPACITOR 2.2uf 35V 10%	1002431	8
2	2	C8,C25	CAPACITOR 18PF 100V 5%	1002808	9
1	1	C20	CAPACITOR 1.5uf 35V 10	1003725	10
4	4	C5,C7,C14,C24	CAPACITOR .22uf 50V -20% +80%	1010274-01	11
0	1	C10	CAPACITOR 500uf 25V -10% +75%	1010509-01	12
1	1	C1	CAPACITOR 8400uf 50V -10% +75%	1010851	13
1	2	D2,D19	DIODE IN748A	1100122	14
0	1	D5	DIODE IN2976B	1100134	15
0	1	D3	DIODE MPI833B	1103341	16
7	8	D1,D6,D7,D8,D9,D15,D16,D22	DIODE D672	1105275	17
1	2	D18,D17	DIODE IN4744	1105648	18
0	1	D4	DIODE IN4004	1105796	19
0	1	D12	DIODE IN3893	1109440	20
0	1	D16	DIODE IN967A	1110089	21
2	2	D20,D21	DIODE MV5054-1 (LIGHT EMITTING)	1110324	22
1	1	D11	DIODE BRIDGE 200V 2A	1110714	23
2	2	D13,D14	DIODE 1TTZ429	1110925	24
0	1	F1	FUSE PICO 5A	1205747	25
0	1		HEAT SINK	1211986	26
0	1	R23	RESISTOR 47 1 4W 5%	1300202	27
0	2	R7,R46	RESISTOR 100 1 4W 5%	1300229	28
0	1	R41	RESISTOR 100 1W 5%	1300232	29
1	3	R4,R12,R49	RESISTOR 220 1 4W 5%	1300271	30
0	1	R14	RESISTOR 220 2W 10	1300278	31
0	1	R11	RESISTOR 680 2W 5%	1300348	32
2	2	R10,R28	RESISTOR 1K 1 4W 5%	1300365	33
0	1	R1	RESISTOR 1 5K 1 2W 5%	1300394	34
0	1	R18	RESISTOR 2 2K 1W 10%	1300420	35
1	1	R15	RESISTOR 3.3K 1W 10%	1300437	36
0	1	R3	RESISTOR 3.3K 1/4W 5%	1300439	37
2	2	R43,R47	RESISTOR 10K 1 4W 5%	1300479	39
0	1	R37	RESISTOR 10 1 4W 5%	1301317	39
2	3	R2,R44,R48	RESISTOR 750 1 4W 5%	1301401	40
0	1	R39	RESISTOR 680 1/4W 5%	1301424	41
0	1	R16	RESISTOR 22K 1 4W 5%	1301808	42
1	1	R13	RESISTOR 1K 2W 5%	1301952	43
0	1	R9	RESISTOR 27 1 2W 5%	1302253	44
2	2	R19,R21	RESISTOR 30K 1/4W 5%	1302394	45
0	1	R36	RESISTOR 511 1/4W 1%	1302411	46
0	1	R38	RESISTOR 909 1/4W 1%	1302805	47
1	1	R25	RESISTOR 3 16K 1/4W 1%	1303045	48
1	1	R8	RESISTOR 470 2W 5%	1303062	49
1	2	R17,R29	RESISTOR 1K 1 4W 1%	1303114	50
1	1	R31	RESISTOR 2.61K 1 4W 1%	1303303	51
0	1	R42	RESISTOR 10K 1 4W 1%	1303312	52
2	2	R33,R34	RESISTOR 5 11K 1/4W 1%	1304854	53
1	1	R30	RESISTOR 9 09K 1/4W 1%	1304855	54
YA	QTY	REF. DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

COMPONENT CHART - YA VERSION		
3	C19, C22, C23	7
1	C8	8
1	D19	14
7	D6, D7, D8, D9, D15, D16, D22	17
1	D10	18
1	R49	30
2	R44, R48	40
1	R28	50
4	Q5, Q8, Q10, Q19	63
4	Q11, Q12, Q13, Q16	66
QTY	REF. DESIGNATION	ITEM

IC TYPE	GND	+5V
GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE NOTED ABOVE		
IC PIN LOCATIONS		

REVISIONS					
REV.	CHANGE NO.	CHK.			
J	5411086-00005	E. LOVA			
H	5411086-00003	V. BOREN			
F	5411086-00002	V. BOREN			
D	5411086-00001	V. BOREN			
C	ORIGINAL				

SEMICONDUCTOR CONVERSION CHART			
DEC NO.	EIA NO.	DEC NO.	EIA NO.

FIRST USED ON OPTION MODEL

ETCH BOARD REV.

DRN.		DATE 10-9-74
CHK'D.		DATE
ENG.		DATE
PROJ. ENG.		DATE
PROD.		DATE
NEXT HIGHER ASSY		
SCALE		
SHEET	1 OF 4	

digital

TITLE: PWR. LINE MONITOR/15V REG.

SIZE	CODE	NUMBER	REV.
D	CS	5411086-0-1	J

DIST.

NOTES:

1	1	R20	RESISTOR 3.48K 1/4W 1%	1305114	55
1	1	R26	RESISTOR 5.62K 1/4W 1%	1305128	56
1	1	R27	RESISTOR 4.99K 1/4W 1%	1305324	57
0	1	R28	RESISTOR 24.9K 1/4W 1%	1305485	58
0	1	R24	RESISTOR 200 20% 02PR	1302150-10	59
1	1	R32	RESISTOR 10 2K 1/4W 1%	1309412	60
0	2	R5,R6	RESISTOR .2 5W 5% WW	1309884	61
0	1	Q7	TRANSISTOR MJE3055	1510555	62
4	6	Q2,Q3,Q5,Q8,Q18,Q19	TRANSISTOR MPSA05	1510705	63
0	2	Q4,Q9	TRANSISTOR MPS A55	1510706	64
0	1	Q6	TRANSISTOR 2N 4441	1505867	65
4	5	Q1,Q11,Q12,Q13,Q16	TRANSISTOR 2N 4258	1509142	66
4	4	Q14,Q15,Q17,Q10	TRANSISTOR 2N 5433	1511686	67
0	1	L1	INDUCTOR, 500 uh	1611866	68
1	1	T1	TRANSFORMER	1612026	69
0	1	E1	I.C. DEC 723	1910415	70
0	1		SCREW, PHM #4-40 X 7/16 LG.	9006012-1	71
0	1		SCREW, PHM #6-32 X 1/4 LG	9006020-1	72
0	1		SCREW, PHM #6-32 X 7/16 LG	9006027-1	73
0	1		KEP NUT #4-40	9006557	74
0	2		KEP NUT #10-32	9006565	75
2	2		WASHER, ITTLKWR #10	9006835	76
0	2		WASHER, FLAT	9006688	77
0	2	(W1)	SPLIT LUG	9006751	78
0	1		SPACER, 1/4AF X 1/2	9006844	79
4	4		CABLE TIE	9007880	80
2	2		TERMINAL	9007930	81
2	2		SCREW, PHM #10-32 X 1/4 LG.	9008007-1	82
0	2		TERMINAL	9008150	83
0	1		KEP NUT #6-32	9008185	84
0	A/R		COMPOUND, THERMAL JOINT	9008268	85
0	5		WASHER, MICA	9008424	86
0	2		WASHER, RING	9008440	87
0	1		FUSE HOLDER	9009141	88
1	1	R22	RESISTOR, 390, 2W 10%	130/880	89
0	1	W1	JUMPER	9009185	90
2	12		WIRE #18 STRANDED BLK	9107980-0-0	91
REF	REF		MODULE TEST PROCEDURE	A-SP-1145-TA-2	92
1	1		WASHER, RING	9006713	93
1	1		.010 INCH SHIM	7413721-0-0	94
REF	REF		ENG. SPEC-AND TEST PROC.	A-SP-5411086-0-3	95

YA	QTY	REF DESIGNATION	DESCRIPTION	PART NO	ITEM NO

FIRST USED ON OPTION MODEL

PARTS LIST

ETCH BOARD REV D

IC TYPE	GND	+ 5V
GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE		

IC PIN LOCATIONS

CHG	CHANGE NO	REV
	REVISIONS	

DEC NO	EIA NO	DEC NO	EIA NO

SEMICONDUCTOR CONVERSION CHART

DRN [illegible] DATE 1/7
CHK D DATE 1/7
ENG. [illegible] DATE 1/14/74
PROJ ENG. [illegible] DATE 1/14/74
PROD [illegible] DATE 1/14/74
NEXT HIGHER ASSY

digital EQUIPMENT CORPORATION

TITLE PWR. LINE MONITOR/15V REG.

SIZE CODE DCS NUMBER 5411086-0-1 REV. J

SCALE —

SHEET 2 OF 4

DIST

DCS 5411086-0-1 J

+25 TO +45 VDC

R8 47Ω 2W

C25 18pf

R21 30K

Q3 MPS A05

R20 1K

R18 1K

Q5 MPS A05

R19 30K

C6 18pf

C5 .22uf 50V

T1

C8 2.2uf 35V

R13 1K 2W

TP3

R25 3.99K 1%

R26 5.62K 1%

TP5

R27 4.99K 1%

D15 D672

R34 5.11K 1%

R33 5.11K 1%

AC-2

D16 D672

AC-1

20V TO 33V RMS AC INPUT

C24 .22uf 50V

C25 1.5uf 35V

TP1

R32 18.2K 1%

Q16 2N4250

Q13 2N4250

Q12 2N4250

Q11 2N4250

C21 330pf

C18 330pf

C17 330pf

C16 330pf

R31 2.61K 1%

TP2

R30 5.89K 1%

R25 3.16K 1%

ACOK

D20 MV5054-1

C21 MV5054

DCOK

D14 ITT4429 5.1V

D13 ITT4429 5.1V

C22 .01uf 100V

C23 .01uf 100V

R28 1K 1%

C19 .01uf 100V

RETURN

+25 TO +45VDC

TO 20V TO 33V RMS AC INPUT

AC-1 15

AC-2 14

D11

L1 BEAD 50Ω

R15 3.3K 1W

R22 390Ω 2W

D19 3.3V IN748A

C14 .22uF 50V

6 LINE CLK L

D22 D672

D8 D672

D9 D672

D6 D672

D7 D672

C7 .22uf 50V

D10 IN6746 15V

R48 75Ω

Q19 MPS A05

5 -18V TO -15V (TEST POINT)

R49 22Ω

R47 10K

R43 10K

(ENG OPTION SEE NOTE 1)

R46 1/2W

Q15 2N5433

Q18 2N5433

3 AC LO 1

8 AC LO 2

4 LO GND

R44 75Ω

Q13 MPS A05

Q17 2N5433

Q14 2N5433

1 DC LO 2

2 DC LO 1

R45 1/2W

(SEE NOTE 1 (ENG. OPTION)

POWER FAIL CIRCUIT

REVISIONS		
CHK	CHANGE NO	REV.

TITLE PWR. LINE MONITOR/15V REG.

SIZE D CODE DCS NUMBER 5411086-0-1

SCALE — SHEET 3 OF 4 DIST.

+25 TO +45 VDC

F1

25 - 45 VDC

C3 .01μf

R14 220 2W, 10%

D12 IN5806

L1 560μH

Q7 MJE 3055

R9 27 1/2W

Q4 MPS A53

R13 220

R10 2.2K 1W, 10%

R11 680 2W

TP4

+15V

4.28V

D4 IN4004

R35 20.9K 1%

D3 MR1038

D5 IN2970B 6.8V

R41 100 1W

9 10 +15VDC ± 5% @ 4A MAX (SEE NOTE 2)

7 +8VDC ± 10% @ 1A MAX (SEE NOTE 2)

W1 (SEE NOTE 3)

C10 500μf 25V | C4 50μf 50V | C9 50μf 50V | C11 50μf 50V

SEE NOTE *1

D17 IN4794 15V ± 1% C12 2.2μf 35V

1/2 723C E1 — REF

R36 511 1%

R24 249 4.28V

R39 999 1%

C15 2.2μf 35V

R17 1K 1%

R16 22K 1%

1/2 723C E1 — COMP

R23 47

Q6 MPS A65

R7 100

D1 D672

C2 56pf

R2 75Ω

D2 IN748A 3.9V

R3 3.3K

Q1 2N4250

R1 1.5K 1/2W

R42 10K 1%

R38 680

R37 10

Q9 MPS A55

Q8 2N4441

C13 .01μf

R40 100

D18 IN963A 18V

Q2 MPS A05

R4 220

R6 .2 5W

R5 .2 5W

11 GND
12 GND
13 GND

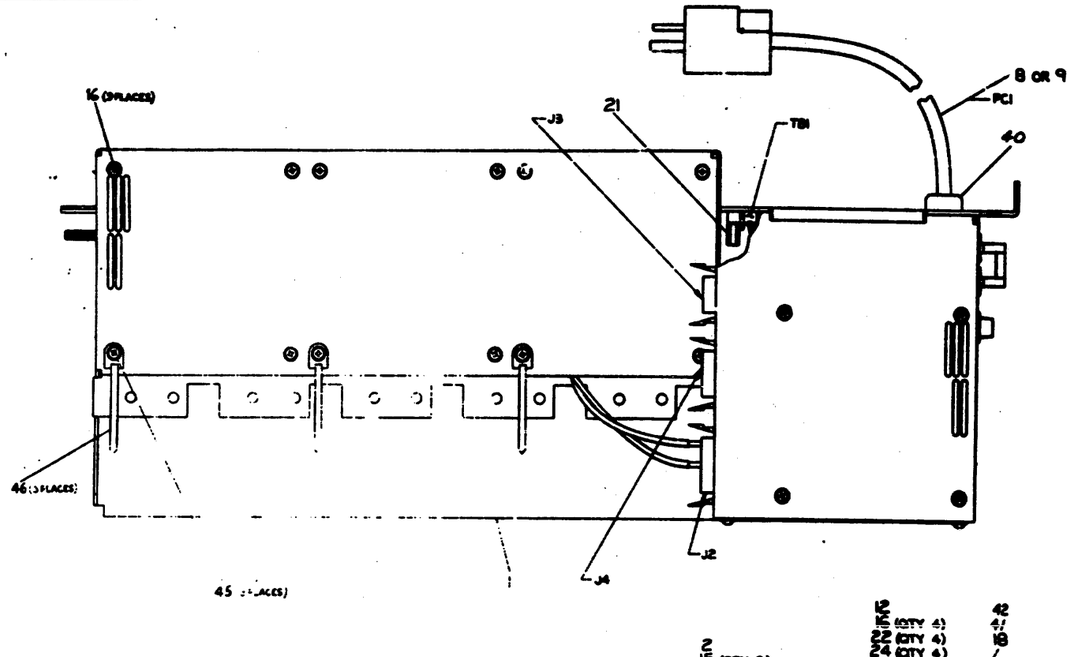
RETURN

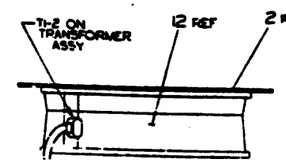
15V REGULATOR
(SEE NOTE *4)

REVISIONS		
CHK	CHANGE NO.	REV.

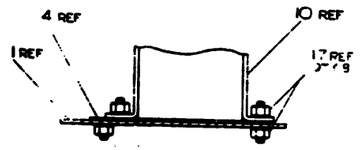
TITLE	PWR. LINE MONITOR/15V REG.	SIZE/CODE	NUMBER
		D	CS 5411086-0-1
SCALE —H—	SHEET 4 OF 4	DIST.	

5411086-0-1





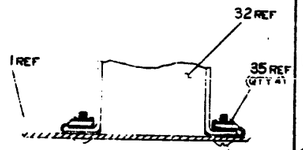
SECTION D-D
SCALE: NONE



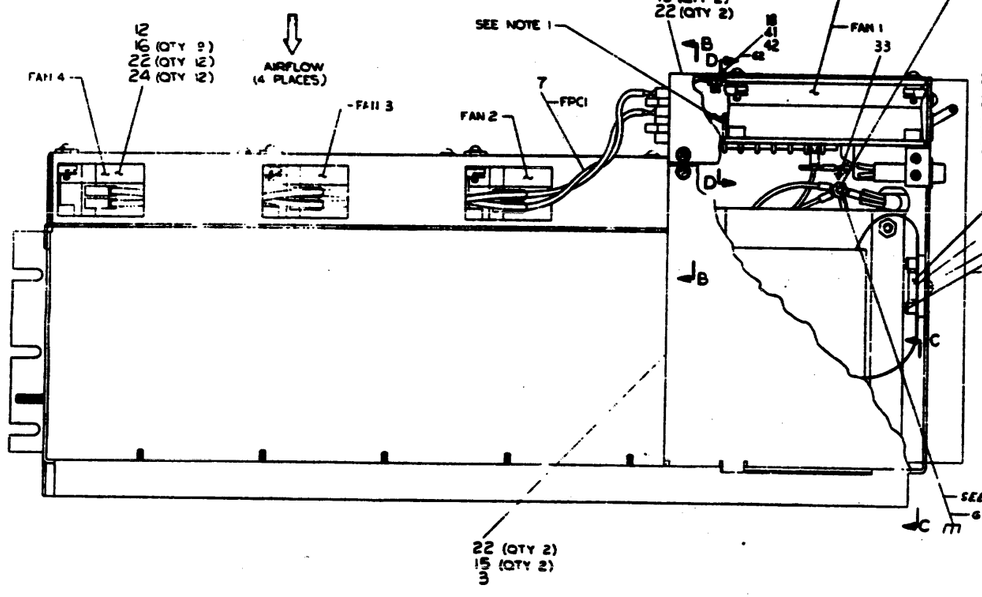
SECTION C-C
SCALE: NONE
SEE NOTE 6

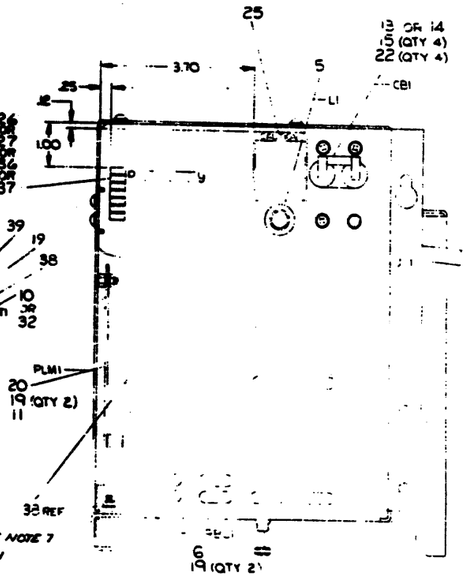
NOTES.

1. AFTER TERMINAL BLOCK (PART OF TRANSFORMER ASSEMBLY) IS MOUNTED TO CHASSIS, CAPACITOR AND VARISTOR SHOULD BE BENT FORWARD TO ALLOW CLEARANCE FOR COVER.
2. REV. D AND EARLIER TRANSFORMERS DO NOT HAVE THIS WIRE. H7420 E+F ONLY
3. FILLER PANELS (D-IA-7413605-0-0) MAY BE USED IN UNFILLED REGULATOR SLOTS (REF).
4. CABLE TIE MOUNTS TO BE MOUNTED AFTER TRANSFORMER ASSEMBLY IS INSTALLED.
5. H7420 A+B ONLY.
6. H7420 E+F ONLY.
7. REMOVE PAINT MASK, APPLY CONDUCTIVE GREASE ITEM 42, PLACE ITEM 41 8-32 EXT TOOTH WASHER AS REF TO CHASSIS BEFORE INSTALLING REMAINING HARDWARE. DO THIS AT G1 AND G2.



SECTION C-C
SCALE: NONE
SEE NOTE 5





FOR PARTS LIST REFER TO A-PL-H7420-0-0

H7420

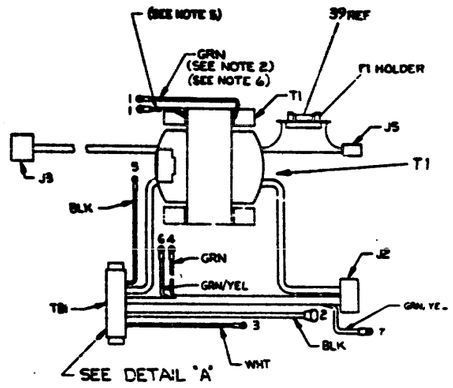
POWER SUPPLY

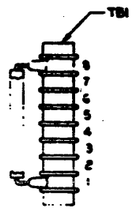
WIRE TABLE

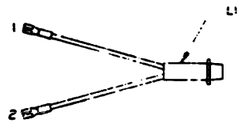
ITEM NO	DESCRIPTION AWG	COLOR	FROM CONNECTION	TO CONNECTION	REMARKS
10	⟷	⟷	T1-J5	RBC1-P5	
1	14	GRN	T1-1	6/	SEE NOTE 2 & 7
	⟷	BLK	T1-2	FAN1-1 & 2	
	14	WHT	T1-3	CB1-1	
4	14	GRN	T1-4	6/	SEE NOTE 7
10	14	BLK	T1-5	CB1-2	
5	22	BLK	L1-1	TB1-5	
6	22	BLK	L1-2	TB1-7	
7	18	RED	FPC1-J6	FAN 4-1	
1	1	WHT	FPC1-J7	FAN 4-2	
		RED	FPC1-J8	FAN 3-1	
		WHT	FPC1-J9	FAN 3-2	
		RED	FPC1-J10	FAN 2-1	
		WHT	FPC1-J11	FAN 2-2	
8	8	RED	FPC1-1	J2-3	
7	18	WHT	FPC1-2	J2-1	
8/9	14	BLK	PCI-1	CB1-4	
8/9	14	GRN	PCI-2	/	SEE NOTE 7
8/9	14	WHT	PCI-3	CB1-3	
11	⟷	⟷	PLMI	REF	
10	14	GRN/YEL	T1-6	/	SEE NOTE 7
10	14	GRN/YEL	T1-7	J2	SEE NOTE 7

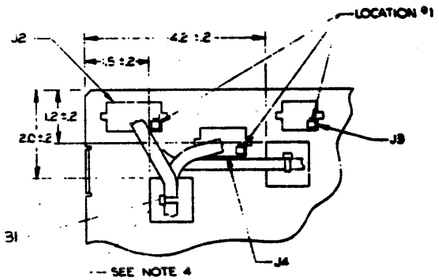
JUMPER TABLE

ITEM NO	DESCRIPTION AWG	COLOR	FROM CONNECTION	WITH	TO CONNECTION	WITH	FREQUT LENGTH	VARIATION
23	14	BLK	TB1-2	ITEM 28	TB1-6	ITEM 28	3.0	H7420E(A
24	14	BLK	TB1-4	ITEM 28	TB1-8	ITEM 28	3.0	
25	14	BLK	TB1-4	ITEM 28	TB1-6	ITEM 28	3.0	H7420F(B

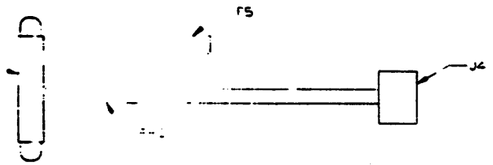


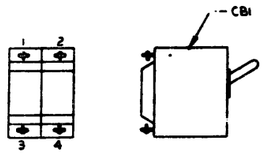


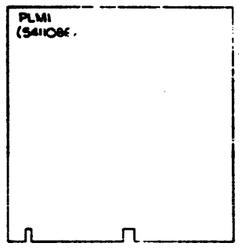


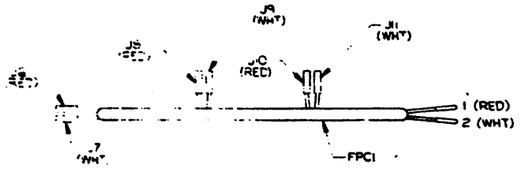


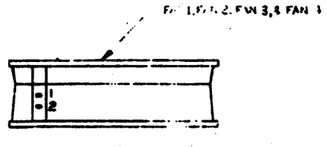
SECTION E-E
SCALE: NONE

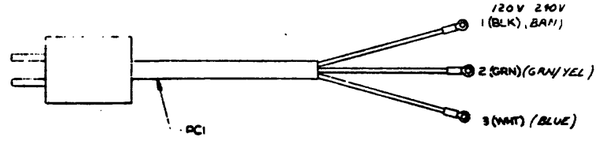




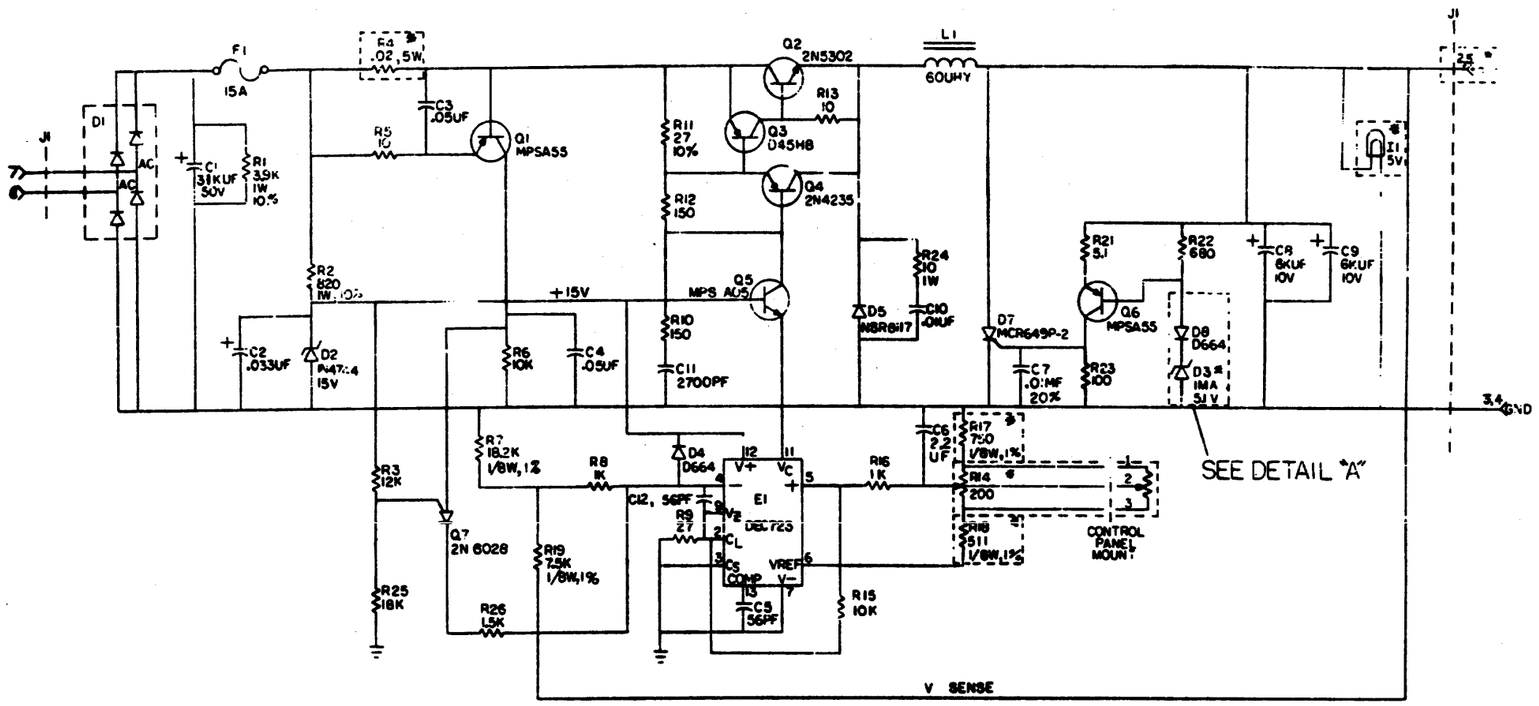


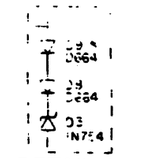






H7420 POWER SUPPLY





[*] FOR YA VARIATION COMPONENT VALUES ARE AS FOLLOWS:
R4 - .06 5W
R14 - 1K 10 TURN
R17 - 300 1/8W 1%
R18 - 150 1/4W 5%
D3 - IN754
I1 - 15V
J1-2,5 - +2.0-8.0V

D9 - D664 ADDED FOR YA VARIATION ONLY

UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W, 5%

QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

ETCH BOARD REV F H

IN964A	SAME	MPSA55	
D664	IN3605	2N5302	
MCR649P-2		D45H5	
1175A	SAME	MPSA05	
IN4744	SAME		
NSR8117			
2N6028			
DEC NO.	EIA NO.	DEC NO.	EIA NO.

SEMICONDUCTOR CONVERSION CHART

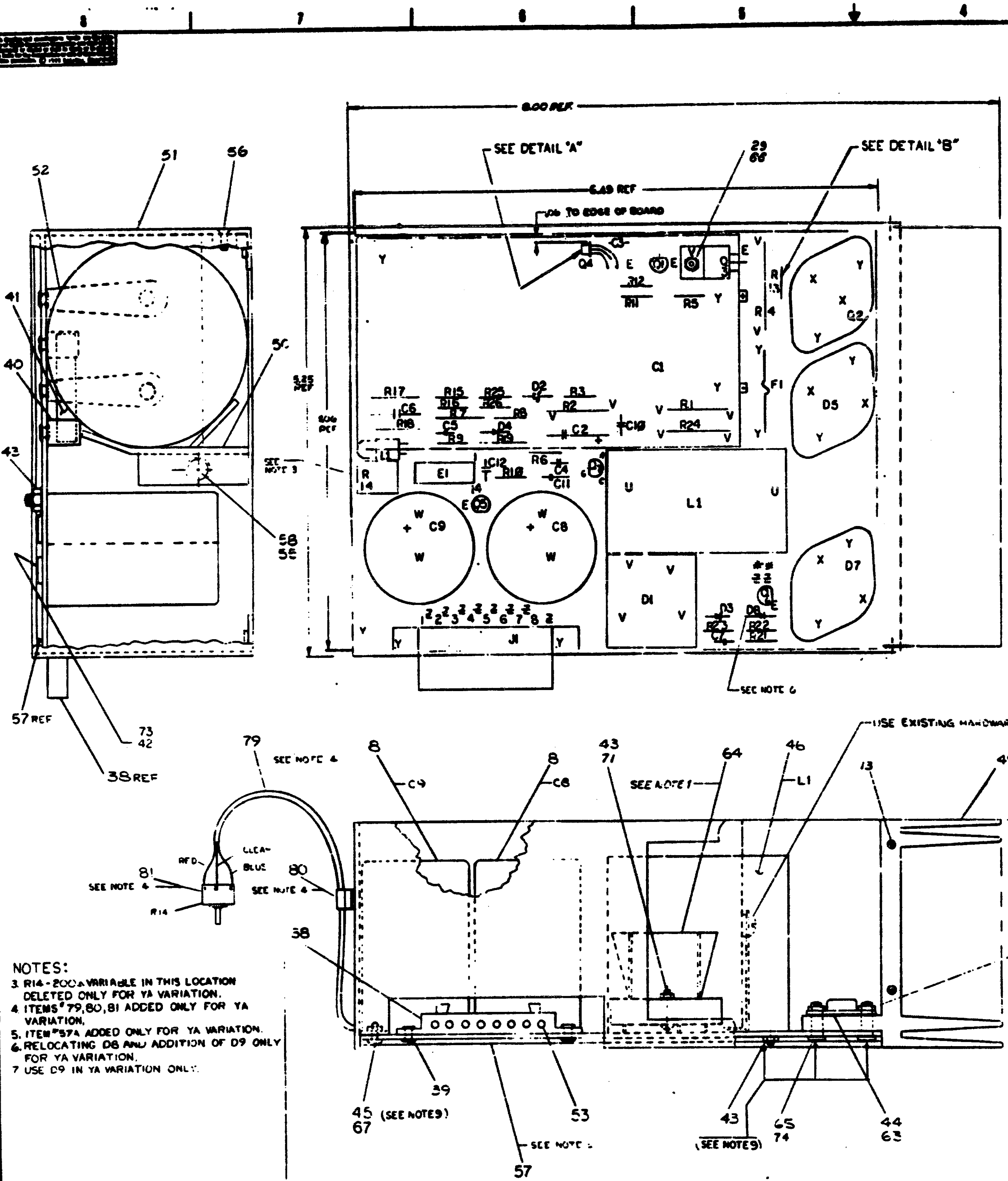
DRWN A.BARON 7-15-74
CHK'D A.BARON 7-15-74
ENG'R R.WOLF 7-15-74
PROJ'T R.WOLF 7-15-74
MFG'R G.POTTER 7-15-74
NEXT HIGHER ASSY
SCALE
SHEET 1 OF 1

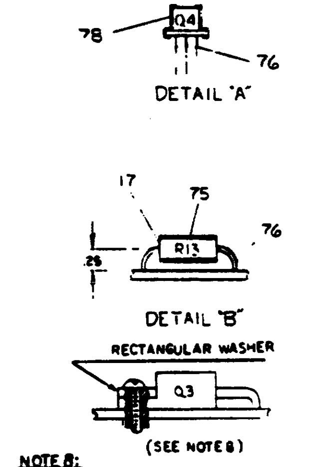
EQUIPMENT CORPORATION

TITLE: 5V REGULATOR

SIZE D | CAGE CODE DCS | NUMBER H744-0-1 | REV V

DIST.





NOTES:

1. APPLY ITEM #63 (COMPOUND) BETWEEN TRANSISTOR (Q2), DIODES (D5, D7) AND ITEM #44 (WASHER) ALSO BETWEEN ITEM #44 (WASHER) AND HEAT SINK (ITEM #49). ALSO APPLY ITEM #63 (COMPOUND) BETWEEN ITEM #9 (DIODE BRIDGE) AND ITEM #64 (HEAT SINK BRIDGE).
2. SECURE Q4 TO CKT BOARD WITH PERMABOND 101 CONTACT CEMENT - THEN CONNECT LEADS AS SHOWN.

QTY	QTY	REF DESIGNATION	DESIGNATION	PART NO.	ITEM NO.
1	1	R22	RES 680 1/4W 5%	1301424	69
1	1		PACKING INSTRUCTIONS	API-3700074-0-0	70
1	1		SCR, PHL PAN HD #6-32 x 5/8 LG	9006025-1	71
1	0	I1	15 VOLT LAMP	1209169	72
4	4		LOCKWASHER #10 INT	9006638	73
A/R	A/R		PERMABOND 101 CEMENT	9009157	74
A/R	A/R		TEF TUBING	9107302-11	75
A/R	A/R		TEF TUBING	9107278-11	76
1	1	Q4	TRANSISTOR 2N4235	1508555	77
A/R	A/R		SHRINK SLEEVING	9107252-09	78
1	0	2 IN	WIRE, MICRODOT	1700014	79
1	0		CLAMP, CABLE	9007079	80
1	0	R14	POT, 10 TURN, 1KΩ	1309532-04	81
1	0	R17	RES, 300Ω 1/4W 5%	1301425	82
1	0	R16	RES, 150Ω 1/4W 5%	1300250	83
1	0	R4	RES, 06Ω 5W 3%	1310876-02	84
1	0	D3	DIODE ZENER 1N754	1109991	85
6	6		FLAT WASHER #4	9006655	86

744-YA	744-00	REF DESIGNATION	DESCRIPTION	PART NO.	
0	1	I1	5 VOLT LAMP	12-09219-1	68
2	2		L WASHER #4	9006632	67
7	7		NUT KEPS #4-40	9006657	66
6	6		SCR PHL PAN HD #4-40 x 3/16 LG	9008033-1	65
1	1		[illegible]	1210907	64
A/R	A/R		COMPOUND THERMAL JOINT	9006268	63
1	1	R26	RESISTOR 1.8K 1/4 W 5%	[illegible]	62
1	1	R19	RESISTOR 7.5K 1/8 W 1%	1305322	61
1	1	R3	RESISTOR 12K 1/4W 5%	1300488	60
1	1	Q7	TRANSISTOR, UNIJUNCTION [illegible]	1510877	59
1	1		SCR. PHL PAN HD #6-32 X 1/4 LG	9006020-1	58
~~2~~	~~2~~		~~COVER~~	~~C-MD-[illegible]~~	57
1	1		SCR. PHL FLT HD #6-32 x 3/16 LG	9008020-2	56
1	1		WASHER, LOCK #6	9006[illegible]33	55
			~~SCR PHL FLT HD [illegible]~~	~~[illegible]~~	54
8	8		CONTACT FEMALE	1209496	53
2	2		STRAP, CAPACITOR	C-MD-5309759-0	52
1	1		BRACKET, REGULATOR	D-IA-5309756-0	51
1	1		HOLDER, CAPACITOR 2.5	C-IA-12398 -0	50
1	1		HEAT SINK REGULATOR	D-PS-1210737-0	49
2	2	C8, C12	CAP 56 PF	1000012	48
1	1	R24	RESISTOR 10 1W	1300171	47
1	1	L1	REACTOR 60 μHY MM-[illegible]	1610850	46
2	2		SCR, PHL PAN HD #4-40 1/4 LG	9008031-1	45
3	3		WASHER, INSULATOR	9006721	44
3	3		NUT, KEPS #6-32	9008195	43
4	4		SCR #10-32 X [illegible] SLOTTED PAN HD	9009668-[illegible]	42
1	1	F1	FUSE 15 AMP	9007226	41
2	2		FUSE CLIP	9007203	40
6	6		EYELET [illegible]-4-5	9001000	39
1	1	J1	MATE N [illegible] CONN, 6 PIN	1209340	38
1	1	E1	INTEGRATED CIRCUIT DEC 723C	1910418	37
1	1	Q5	TRANSISTOR A05	1510705	36
1	1	Q3	TRANSISTOR D45H8	1510708-1	35
2	2	Q1, Q6	TRANSISTOR MPSA55 MOT	1510706	34
1	1	Q2	TRANSISTOR 2N5302	1510196	33
0	1	R14	RES VARIABLE 200	[illegible]	32
1	1	R21	RES 5.1 1/4W 5%	1309422	31
1	1	R23	RES 100 1/4W 5%	1300229	30
1	1		SCR, [illegible] #4 40 X 1/4	9006011-1	29
1	1	R11	RES 27 1/4W 10%	1301420	28
0	1	R17	RES 750 1/8W, 1%	1302955	27
1	1	R9	RES 27 1/4W 5%	1301522	26
1	1	R7	RES 16.2K 1/8W, 1%	[illegible]	25
2	2	R8, R16	RES 1K 1/4W 5%	1300365	24
0	1	R18	RES 511 1/8W 1%	1302411	23
1	1	R15	RES 18K 1/4W 5%	1302465	22
2	2	R6, R15	RES 10K 1/4W 5%	1300474	21
0	1	R4	RES .02 5W 3%	1310876	20
1	1	R2	RES 820 1W 10%	1300356	19
1	1	R1	RES 3.9K 1W 10%	1302927	18
2	2	R5, R13	RES 10 1/4W 5%	1301317	17
2	2	R12 R10	RES 150 1/4W 5%	1300250	16
0	1	D3	DIODE ZENER 1 MA. 5.1V	1110925	15
1	1	D7	SCR MCR 649P-2	1109465	14
4	4		SCR, FFH #4 X 5/16 LG [illegible]	9009142	13
1	1	D5	DIODE PWR [illegible]	1110715	12
3	2	D4 D8 D9*	DIODE P[illegible] D664	1100114	11
1	1	D2	DIODE ZENER 1N4744	110[illegible]648	10
1	1	D1	DIODE BRIDGE	1110714	9
2	2	C8, C9	CAP 6K μF 10V	1010704	8
1	1	C1	CAP 31K μF 30V	[illegible]10458	7
2	2	C4, C3	CAP .05μF 25V	1001774	6
1	1	C2	CAP .033 μF [illegible]	1000050	5
1	1	C11	CAP 2700PF 100V 5% DM	1001637	4
2	2	C7, C10	CAP .01 μF 100V 20% DISC	1001610	3
1	1	C6	CAP [illegible]	1002627	2
1	1		ETCHED CIRCUIT BOARD	5009725	1
			ASSY/DRILLING HOLE LAYOUT	D-AH-H744-0-5	
			X-Y COORDINATE HOLE LOCATION	[illegible]-H744-0-4	REF
			MODULE ECO HISTORY	D-MH-H744-0-6	REF
			CIRCUIT SCHEMATIC	D-CS-H744-0-1	REF

PARTS LIST

* SEE NOTE 7

NOTE 8:

(1) Q3 SCREW HEAD SHOULD BE ON TOP OF FLAT RECTANGULAR WASHER AS SHOWN. APPLY 6 INCH LBS. OF TORQUE WHEN SECURING Q3 TO CKT. BOARD BEFORE SOLDERING.

NOTE 9: TORQUE APPLICATION

(1) APPLY 12 INCH LBS. OF TORQUE TO ALL #4 HARDWARE EXCEPT Q3.
(2) APPLY 16 INCH LBS. OF TORQUE TO ALL #6 AND #10 HARDWARE.
(3) ALL HARDWARE TO BE TORQUED BEFORE SOLDERING.

NOTES:

3. R14 - 200Ω VARIABLE IN THIS LOCATION DELETED ONLY FOR YA VARIATION.
4. ITEMS #79, 80, 81 ADDED ONLY FOR YA VARIATION.
5. ITEM #57A ADDED ONLY FOR YA VARIATION.
6. RELOCATING D8 AND ADDITION OF D9 ONLY FOR YA VARIATION.
7. USE D9 IN YA VARIATION ONLY.

MA 723C	7	12

FIRST USED ON OPTINCO
D-UA-H742A-0-0

ETCH BOARD REV H

DEC NO.	EIA NO.
3664	1N3606
1N4744	

[redacted] EQUIPMENT CORPORATION

TITLE: 5V REGULATOR

E [illegible]H744-0-0 J

D-UA-H744-0-0

SECTION III
KB11-C/D BLOCK DIAGRAMS

ALU
PCA (DAPF,H)
PCB (DAPF,H)
PCA(T2)[36]
0 NO CLOCK
1 LOAD
PCB(T2)[50-49]
0 NO CLOCK 2 SF7:LOAD
1 LOAD 3 DF7:LOAD
SHFR (DAPF,H,J)
SHF (T2) [48-47]
0 SWAP BYTES
1 PCB
2 NO SHIFT
3 RIGHT SHIFT
ALU (DAPF, DAPH)
B A
ALU(T9)[17-15]
0 NOT A
1 B
2 A PLUS b
3 A PLUS 1
4 NOT USED
5 A PLUS A
6 A AND B
7 INSTRUCTION DEPENDENT
BMX (T1) [21-20]
0 KOMX
1 K1MX
2 SR
3 SR
BMX (DAPB,C,D)
AMX (DAPB,C,A)
AMX(T1)[23-22]
0 DR
1 PCB
2 SR
3 SR
KOMX (DAPD)
K1MX (DAPE)
KMX (T1) [19-18]
KOMX
0 1
1 2
2 SOURCE CONST.
3 DEST. CONST.
K1MX
START VECTOR
TRAP VECTOR
BOB & MARK OFFSET
BXX OFFSET
SRCCON
DSTCON
TV
SV
SS (16 REGISTERS) (GRAD,E,F,H)
SD (16 REGISTERS) (GRAD,E,F,H)
SHFR
SRMX (GRAD,E,F,H)
DRMX (GRAD,E,F,H)
SR (GRAD,F,H)
DR (GRAD,E,F,H)
SC (GRAJ)
SRX (T2) [61-60]
0 SHFR
1 SS
2 SF7:SHFR, -SF7:SS
3 NOT USED
SRK (T2) [57]
0 NO CLOCK
1 LOAD
PAD (T14) [43-40]
SS SD SS SD
0 SF SF 4 SFV1 SFV1 0
1 SF DF 5 DF DF 1
2 S S 6 0 0 2
3 NOT USED 7 6 6 3
PWE (T14) [45-44]
0 DON'T WRITE
1 CONDITIONAL WRITE
3 NOT USED
DRX (T2) [59-58]
0 SHFR
1 SD
2 DF7:SHFR, -DF7:SD
3 CLR DR
DRK (T2) [56-55]
0 NO CLOCK
1 SHIFT RIGHT
2 SHIFT LEFT
3 LOAD
SHC (T1) [34-33]
0 NO COUNT
1 COUNT
2 LOAD DR<5:0>
3 LOAD 17₈
BAX (T1) [38-37]
0 DR
1 PCB
2 SR
3 FP EALU (MAINT)
SAMX (DAPB, C,D)
VIRTUAL ADDRESS
FROM FPP ACOMX
DATA FROM SEMI-COND MEMORY
TO/FROM UNIBUS
INT BUS
UNIBUS
BRMX (PDRA)
BRX (T2) [62]
0 SHFR
1 BUS (UNIBUS, FAST BUS, OR INTERNAL BUS)
BUS BUFFER REGISTER (PDR,J)
(T3)
SHFR
FROM FPP UADR/ CPU UADR
MULTIPLEXER DISPLAY (PDRF)
TO CONSOLE DATA LIGHTS
BRK (T2) [63]
0 NO CLOCK
1 LOAD
BR (DAPA)
BRA (PDRB)
IR (IRCA)
AFIR (RACJ)
IRK(T2)[44]
0 NOCLOCK
1 LOAD
LR
BR
DATA TO SEMI-COND MEMORY
LR (PDRB)
PS (IRCH/PDRB)
PIRQ (PDRD)
SL (PDRC)
PB (PDRC)
SL/PB
PIRQ
PS
DMX (PDRE)
IBB (T1) [36-35]
0 NO COMMAND
1 READ SW
2 LOAD PS
3 READ PS
FROM SWITCH REGISTER (PDRH)
INTERNAL BUS
DATA FROM FPP DOMX
DATA TO KT11-CD REGISTERS AND FPP FDR
DATA FROM KT11-CDREGISTERS

SYMBOL DEFINITION
FUNCTION NAME
DATA BUS OUT
XXXX
(YYYY)
DATA BUS IN
CIRCUIT SCHEMATIC LOCATION
ROM BUFFER SIGNAL NAME
TIME PULSE / STATE
ROM OUTPUT NUMBER
ZZZ (T1)[NN]
CONTROLLING SIGNAL

REVISIONS			
DWG	CHANGE NO	REV	
20	11/55-00001	A	V. BOMEN 12/16

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	FIND NO.
11/45		PARTS LIST		

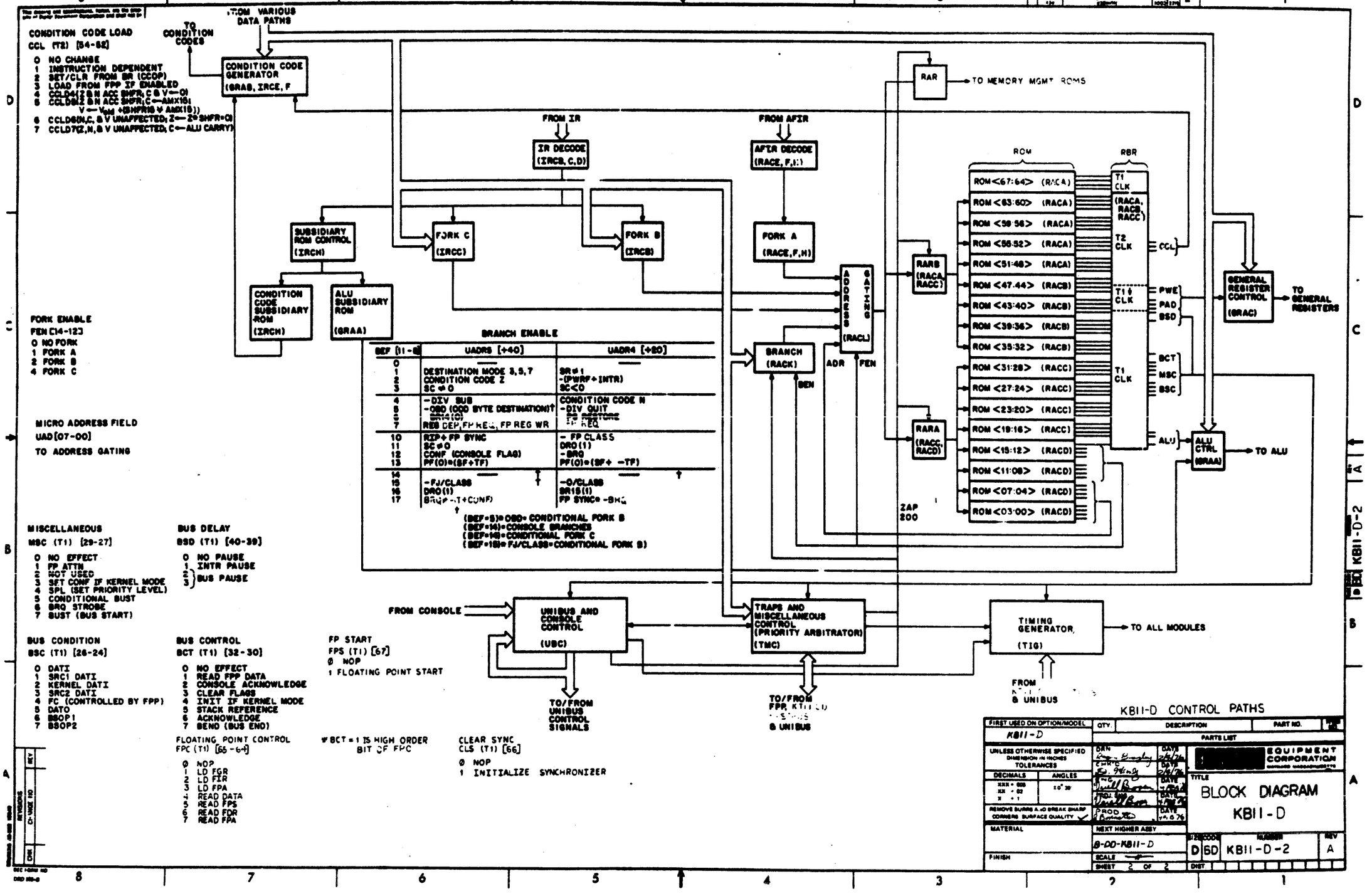
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES
DECIMALS .XXX ± .005 .XX ± .02 X ± .1
ANGLES ±0° 30'
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓
MATERIAL
FINISH

DRAWN A. Bradley 12-16-72
CHK'D
ENGR
PROJ.
NEXT HIGHER ASSY. B-DD-KB11-D
SCALE
SHEET 1 OF 2

EQUIPMENT CORPORATION

TITLE BLOCK DIAGRAM KB11-D

SIZE D | DWG NO BD KB11-C-2 | REV A


CONDITION CODE LOAD
CCL (T2) [54-52]
0 NO CHANGE
1 INSTRUCTION DEPENDENT
2 SET/CLR FROM BR (CCOP)
3 LOAD FROM FPP IF ENABLED
4 CCLD4(Z & N ACC SHFR; C & V←0)
5 CCLD5(Z & N ACC SHFR; C←AMX16)
V←V_old ÷(SHFR16 ∀ AMX16))
6 CCLD6(N,C, & V UNAFFECTED; Z←Z• SHFR•0)
7 CCLD7(Z,N,& V UNAFFECTED; C←ALU CARRY)
TO CONDITION CODES
FROM VARIOUS DATA PATHS
CONDITION CODE GENERATOR (GRAB, IRCE, F
FROM IR
IR DECODE (IRCB, C, D)
FROM AFIR
AFIR DECODE (RACE, F, H)
RAR
TO MEMORY MGMT ROMS
ROM
RBR
SUBSIDIARY ROM CONTROL (IRCH)
FORK C (IRCC)
FORK B (IRCB)
FORK A (RACE, F, H)
CONDITION CODE SUBSIDIARY ROM (IRCH)
ALU SUBSIDIARY ROM (GRAA)
ADDRESS GATING (RACL)
RARB (RACA, RACC)
RARA (RACC, RACD)
ROM<67:64> (RACA)
ROM<63:60> (RACA)
ROM<59:56> (RACA)
ROM<55:52> (RACA)
ROM<51:48> (RACA)
ROM<47:44> (RACB)
ROM<43:40> (RACB)
ROM<39:36> (RACB)
ROM<35:32> (RACB)
ROM<31:28> (RACC)
ROM<27:24> (RACC)
ROM<23:20> (RACC)
ROM<19:16> (RACC)
ROM<15:12> (RACD)
ROM<11:08> (RACD)
ROM<07:04> (RACD)
ROM<03:00> (RACD)
T1 CLK
(RACA, RACB, RACC)
T2 CLK
CCL
T1 Φ CLK
PWE
PAD
BSD
BCT
MSC
BSC
T1 CLK
ALU
ALU CTRL (GRAA)
TO ALU
GENERAL REGISTER CONTROL (GRAC)
TO GENERAL REGISTERS
ZAP 200
BRANCH ENABLE
BEF [11-8]
UADR8 [+40]
UADR4 [+80]
0
1 DESTINATION MODE 3,5,7 / CONDITION CODE Z / SC ≠ 0
2
3
4 -DIV SUB / -ODD (ODD BYTE DESTINATION)† / CONDITION CODE N
5 / -DIV QUIT
6
7 REG DEF, FP REG, FP REG WR
10 RIP+FP SYNC / - FP CLASS
11 SC ≠ 0 / DRO(1)
12 CONF (CONSOLE FLAG) / -BRQ
13 PF(0)•(BF+ -TF) / PF(0)•(BF+ -TF)
14
15 -FJ/CLASS / -O/CLASS
16 DRO(1) / BR15(1)
17 BRQ•(-T+CONF) / FP SYNC• -BRQ
† (BEF=5)•ODD• CONDITIONAL FORK B
(BEF=14)•CONSOLE BRANCHES
(BEF=16)•CONDITIONAL FORK C
(BEF=15)• FJ/CLASS•CONDITIONAL FORK B)
BRANCH (RACK)
BEN
ADR
FEN
FORK ENABLE
FEN [14-12]
0 NO FORK
1 FORK A
2 FORK B
4 FORK C
MICRO ADDRESS FIELD
UAD[07-00]
TO ADDRESS GATING
MISCELLANEOUS
MSC (T1) [29-27]
0 NO EFFECT
1 FP ATTN
2 NOT USED
3 SET CONF IF KERNEL MODE
4 SPL (SET PRIORITY LEVEL)
5 CONDITIONAL BUST
6 BRQ STROBE
7 BUST (BUS START)
BUS DELAY
BSD (T1) [40-39]
0 NO PAUSE
1 INTR PAUSE
2 } BUS PAUSE
3 }
BUS CONDITION
BSC (T1) [26-24]
0 DATI
1 SRC1 DATI
2 KERNEL DATI
3 SRC2 DATI
4 FC (CONTROLLED BY FPP)
5 DATO
6 BSOP1
7 BSOP2
BUS CONTROL
BCT (T1) [32-30]
0 NO EFFECT
1 READ FPP DATA
2 CONSOLE ACKNOWLEDGE
3 CLEAR FLAGS
4 INIT IF KERNEL MODE
5 STACK REFERENCE
6 ACKNOWLEDGE
7 BEND (BUS END)
FLOATING POINT CONTROL
FPC (T1) [55-64]
0 NOP
1 LD FGR
2 LD FIR
3 LD FPA
4 READ DATA
5 READ FPS
6 READ FDR
7 READ FPA
FP START
FPS (T1) [67]
0 NOP
1 FLOATING POINT START
BCT = 1 IS HIGH ORDER BIT OF FPC
CLEAR SYNC
CLS (T1) [66]
0 NOP
1 INITIALIZE SYNCHRONIZER
FROM CONSOLE
UNIBUS AND CONSOLE CONTROL (UBC)
TRAPS AND MISCELLANEOUS CONTROL (PRIORITY ARBITRATOR) (TMC)
TIMING GENERATOR (TIG)
TO ALL MODULES
TO/FROM UNIBUS CONTROL SIGNALS
TO/FROM FPP, KT11-D
& UNIBUS
FROM
& UNIBUS
KB11-D CONTROL PATHS
FIRST USED ON OPTION/MODEL
KB11-D
QTY.
DESCRIPTION
PART NO.
PARTS LIST
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES TOLERANCES
DECIMALS
ANGLES
REMOVE BURRS & BREAK SHARP CORNERS SURFACE QUALITY
MATERIAL
FINISH
DRN
DATE
ENGR
PROJ
PROD
EQUIPMENT CORPORATION
TITLE
BLOCK DIAGRAM
KB11-D
NEXT HIGHER ASSY
B-00-KB11-D
SCALE
SHEET 2 OF 2
SIZE CODE
D 60
NUMBER
KB11-D-2
REV
A
DIST
REVISIONS
KB11-D-2

CONDITION CODE LOAD
CCL (T2) [54-52]

0 NO CHANGE
1 INSTRUCTION DEPENDENT
2 SET/CLR FROM BR (CCOP)
3 LOAD FROM FPP IF ENABLED
4 CCLD4(Z & N ACC SHFR; C & V←0)
5 CCLD5(Z & N ACC SHFR; C←AMX15;
V ← V_{old} +(SHFR15 ∨ AMX(15))
6 CCLD6(N,C, & V UNAFFECTED; Z← Z• SHFR=0)
7 CCLD7(Z,N, & V UNAFFECTED; C← ALU CARRY)

FORK ENABLE
FEN [14-12]
0 NO FORK
1 FORK A
2 FORK B
4 FORK C

MICRO ADDRESS FIELD
UAD[07-00]
TO ADDRESS GATING

MISCELLANEOUS
MSC (T1) [29-27]

0 NO EFFECT
1 FP ATTN
2 NOT USED
3 SET CONF IF KERNEL MODE
4 SPL (SET PRIORITY LEVEL)
5 CONDITIONAL BUST
6 BRQ STROBE
7 BUST (BUS START)

BUS CONDITION
BSC (T1) [26-24]

0 DATI
1 SRC1 DATI
2 KERNEL DATI
3 SRC2 DATI
4 FC (CONTROLLED BY FPP)
5 DATO
6 BSOP1
7 BSOP2

BUS DELAY
BSD (T1) [40-39]

0 NO PAUSE
1 INTR PAUSE
2, 3 BUS PAUSE

BUS CONTROL
BCT (T1) [32-30]

0 NO EFFECT
* 1 READ FPP DATA
2 CONSOLE ACKNOWLEDGE
3 CLEAR FLAGS
4 INIT IF KERNEL MODE
5 STACK REFERENCE
6 ACKNOWLEDGE
7 BEND (BUS END)

FLOATING POINT CONTROL
FPC (T1) [64-65]

0 NOP
1 LD FGR
2 LD FIR
3 LD FPA
4 READ DATA
5 READ FPS
6 READ FDR
7 READ FPA

* BCT = 1 IS HIGH ORDER OF FPC

FP START
FPS (T1) [67]
0 NOP
1 FLOATING POINT START

CLEAR SYNC
CLS (T1) [66]
0 NOP
1 INITIALIZE SYNCHRONIZER

BRANCH ENABLE

BEF [11-8]	UADR5 [+40]	UADR4 [+20]
0	GND	GND
1	DESTINATION MODE 3,5,7	SR = 1
2	CONDITION CODE Z	-(PWRF+INTR)
3	SC = 0	SC<0
4	-DIV SUB	CONDITION CODE N
5	-OBD (ODD BYTE DESTINATION)†	-DIV QUIT
6	BR14(0)	RESTORE
7	RACK BE 7 5 H	RACK FP REQ H
10	RIP+FP SYNC	FRMB FP CLASS L
11	SC = 0	DRO(1)
12	CONF (CONSOLE FLAG)	-BRQ
13	PF(0)•(SF+TF)	PF(0)•(SF+ -TF)
14	—— †	-O/CLASS
15	-FJ/CLASS	SR15(1)
16	DRO(1)	TMCB BRQ•(T+CONF)L
17	RACK RIP+FP SYNC L • TMCB BRQ•(T+CONF)L	

† (BEF=5)•OBD=CONDITIONAL FORK B
(BEF=14)•CONSOLE BRANCHES
(BEF=14)•CONDITIONAL FORK C
(BEF=15)•FJ/CLASS•CONDITIONAL FORK B)

FROM VARIOUS DATA PATHS
TO CONDITION CODES
CONDITION CODE GENERATOR (GRAB, IRCE, F)
FROM IR
IR DECODE (IRCB, C, D)
FROM AFIR
AFIR DECODE (RACE, F, H)
RAR → TO MEMORY MGMT
SUBSIDIARY ROM CONTROL (IRCH)
FORK C (IRCC)
FORK B (IRCB)
FORK A (RACE, F, H)
CONDITION CODE SUBSIDIARY ROM (IRCH)
ALU SUBSIDIARY ROM (GRAA)
ADDRESS GATING (RACL)
RARB (RACA, RACC)
RARA (RACC, RACD)
BRANCH (RACK)
ADR
FEN
BEN
ZAP 200
ROM
RBR
ROM <67:64> (RACA)
ROM <63:60> (RACA)
ROM <59:56> (RACA)
ROM <55:52> (RACA)
ROM <51:48> (RACA)
ROM <47:44> (RACB)
ROM <43:40> (RACB)
ROM <39:36> (RACB)
ROM <35:32> (RACB)
ROM <31:28> (RACC)
ROM <27:24> (RACC)
ROM <23:20> (RACC)
ROM <19:16> (RACC)
ROM <15:12> (RACD)
ROM <11:08> (RACD)
ROM <07:04> (RACD)
ROM <03:00> (RACD)
T1 CLK
(RACA, RACB, RACC)
T2 CLK
T1↓ CLK
T1 CLK
CCL
PWE
PAD
BSD
BCT
MSC
BSC
ALU
ALU CTRL (GRAA)
TO ALU
GENERAL REGISTER CONTROL (GRAC)
TO GENERAL REGISTERS
FROM CONSOLE
UNIBUS AND CONSOLE CONTROL (UBC)
TRAPS AND MISCELLANEOUS CONTROL (PRIORITY ARBITRATOR) (TMC)
TIMING GENERATOR (TIG)
TO ALL MODULES
TO/FROM UNIBUS CONTROL SIGNALS
TO/FROM FPP, MEMORY MGMT. INTERNAL DATA BUS & UNIBUS
FROM MEMORY MGMT. & UNIBUS

Figure 1-1 Block Diagram

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	FROM NO.
KB11-C		PARTS LIST		

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES TOLERANCES
DECIMALS: XXX = .005, .XX = .02, X = 1 — ANGLES: ±0° 30'
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓

DRN D HAMEL DATE 9/6/75
CHK DATE 3/20/76
ENG DATE 3/21/76
PROJ ENG DATE 3/24/76
PROD DATE 3/24/76

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: BLOCK DIAGRAM KB11-C

MATERIAL
FINISH
NEXT HIGHER ASSY: B-DD-KB11-
SCALE
SHEET 1 OF 1
SIZE D CODE BD NUMBER KB11-C-3 REV
DIST

ALU
PCA (DAPF,H)
PCA(T2)[38]
0 NO CLOCK
1 LOAD
PCB (DAPF,H)
PCB(T2)[30-49]
0 NO CLOCK 2 SF7: LOAD
1 LOAD 3 DF7: LOAD
CLA
PCB
SHFR (DAPF,H,J)
SHF (T2) [48-47]
0 SWAP BYTES
1 PCB
2 NO SHIFT
3 RIGHT SHIFT
ALU (DAPF, DAPH)
B A
ALUXT0 [17-15]
0 NOT A
1 B
2 A
3 A PLUS B
4 NOT USED
5 A PLUS A
6 A MINUS B
7 INSTRUCTION DEPENDENT
AMX(T1)[23-22]
0 DR
1 PC
2 SR
3 SR
BMX (T1) [21-20]
0 KOMX
1 K1MX
2 SR
3 SR
BMX (DAPB,C,D)
AMX (DAPB,C,D)
KOMX (DAPD)
K1MX (DAPE)
SRCCON
DSTCON
TV
SV
KOMX (T1) [19-16]
KOMX K1MX
0 1 START VECTOR
1 2 TRAP VECTOR
2 SOURCE CONST. SOB & MARK OFFSET
3 DEST. CONST. BXX OFFSET
GS (16 REGISTERS) (GRAD,E,F,H)
GD (16 REGISTERS) (GRAD,E,F,H)
PAD (T1&) [43-41]
PWE (T1&) [45-44]
0 GS GD GS GD
1 SF SF SF+1 SF+1
2 DF DF DF DF
3 S S 0 0
4 NOT USED 5 5 6 6
0 CON'T WRITE
1 CONDITIONAL WRITE
2 NOT USED
SRX (T2) [61-60]
0 SHFR
1 GS
2 SF7:SHFR, -SF7:GS
3 NOT USED
SRX (T2) [37]
0 NO CLOCK
1 LOAD
SRMX (GRAD,E,F,H)
DRMX (GRAD,E,F,H)
SR (GRAD,F,H)
DR (GRAD,E,F,H)
SHFR
DRX (T2) [39-38]
0 SHFR
1 GD
2 DF7:SHFR; -DF7:GD
3 CLR DR
DRX (T2) [36-35]
0 NO CLOCK
1 SHIFT RIGHT
2 SHIFT LEFT
3 LOAD
SC (GRAJ)
SHC (T1) [34-33]
0 NO COUNT
1 COUNT
2 LOAD DR<5:0>
3 LOAD 17₈
BAX (T1)[38-37]
0 DR
1 PCB
2 SR
3 FP EALU (MAINT)
BAX (DAPB, C,D)
VIRTUAL ADDRESS
MEMORY MGMT (SAP,SSR, SCC)
UNIBUS ADDRESS
CACHE ADDRESS
DATA FROM CACHE MEMORY
DATA TO/FROM UNIBUS (INCL. CACHE & UNIBUS MAP REGISTERS)
TO CONSOLE DATA LIGHTS
DATA TO CACHE MEMORY
FROM FPP EALU
SHFR
CACHE
INT DATA BUS
UNIBUS
BUS BUFFER REGISTER (PDRJ)
BRMX (PDRA)
BRX (T2) [62]
0 SHFR
1 BUS (DETERMINED BY ADDRESS)
(T3)
SHFR
FROM FPP UADR/ CPU UADR
DISP MULTIPLEXER (PDRF)
BRX (T2) [63]
0 NO CLOCK
1 LOAD
BR (DAPA)
BRA (PDRB)
IR (IRCA)
A.IR (RACJ)
IRX(T2)[44]
0 NOCLOCK
1 LOAD
LR
BR
LR (PDRB)
PS (IRCH,PDRD)
PIRQ (PDRD)
SL (PDRC)
PB (PDRC)
SL/PB
PIRQ
PS
DMX (PDRE)
IBS (T1) [36-35]
0 NO COMMAND
1 READ SW
2 LOAD PS
3 READ PS
INTERNAL DATA BUS
DATA FROM FPP
DATA TO MEMORY MGMT. REGISTER, AND FPP DATA
DATA FROM MEMORY MGMT., SWITCH, CPU ERROR, AND SYSTEM SIZE & ID REGISTERS.

FIRST USED ON OPTION/MODEL	QTY	DESCRIPTION	PART NO	ITEM NO
KB11-C		PARTS LIST		

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES
TOLERANCES
DECIMALS: XXX ± .005, XX ± .02, X ± .1
ANGLES: ± 0° 30'
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓
MATERIAL
FINISH

DRN PJ Lynch DATE 1/15
CHK DATE
ENG DATE 11/15/75
PROJ ENG DATE 12/1/75
PROD DATE 12/19/75

digital EQUIPMENT CORPORATION

TITLE
BLOCK DIAGRAM
KB11-C

NEXT HIGHER ASSY
B-DD-KB11-C

SIZE D | CODE BD | NUMBER KB11- -2 | REV

SCALE
SHEET 1 OF 1 | DIST

REV	REVISIONS	CHANGE NO

SECTION IV
KB11-C FLOW DIAGRAMS

NOTE:
1. t_p BUS PAUSE = t_8 FOR UNIBUS CYCLES, t_5 FOR CACHE CYCLES

FET.00
FET.00 (217)
FET.01 (351)
FET.02 (352)
FET.03 (354)
FET.04 (1C4)
FET.05 (12C)
FET.06 (378)

START FETCH NEXT INSTR. CLEAR INSTR. REG
t_1 BA←PCB; BC←DATI
t_2 SWFR←SR-SR
t_4 BUST; CLEAR FLAGS
t_6 IR←SWFR

DEFINE(240) BRQ → BRK.00 (244)

-BRQ

FET.10 (264)
FET.11 (262)
FET.12 (333)
FET.13 (334)

GET INSTR & STEP PC BEYOND
t_1 BA←PCB; BC←DATI
t_2 <SWFR←PCB+2>
t_3 BRQ STROBE
t_4 BUS PAUSE
t_5 PCA←PCB+2
t_6 IR←BUS, BR←BUS, PCB←PCA
t_7 PBA←BA
(348)

IRD.00
IRD.01 (346)
DECODE THIS INSTR & STEP PCB BEYOND (EBMD SPEC'S DST FIELD, GEN REGS
t_1 BA←PCB; BC←DATI
t_2 SWFR←ACB
t_3 CONDITIONAL BUST F/RA←BR
t_5 PCB←PCB+2
t_6 -SFT: SRA←GBC(SF)
SFT: SR←SWFR
-DFT: DA←GDC(DF)
DFT: DR←SWFR

FEN1 (377)

A-FORK

BIN*SM128
S/3.00 (321) SM1
S/3.01 (322) SM28
FETCH SRC & STEP REGISTER UP
t_1 BA←SR; BC←SRC1 DATI
t_2 SWFR←SR+SRCCON
t_3 BUST
t_5 PCA←SR+SRCCON GR(SF)←SWFR
t_6 SFT: PCB←PCA
(327)

S/3.10 (327)
GET SEC'D ARGMN'S DST REG
t_1 BA←SR; BC←SRC1 DATI
t_2 SWFR←PCB
t_3 BRQ STROBE
t_4 BUS PAUSE
t_6 BA←BUS
-DFT: DA←GDC(DF)
DFT: DR←SWFR

C-FORK 4
S/3.20 2 (317)
FEN4 BENM(317)
-SM357 SM357

BIN*SM48
S/65.00 (330)
STEP REGISTER, DOWN
t_1 <BA←PCB>
t_2 SWFR←SR-SRCCON
t_3 BEND
t_5 PCA←SR-SRCCON GR(SF)←SWFR
t_6 SR←SWFR SFT: PCB←PCA
(325)

S/65.10 (325)
FETCH SRC
t_1 BA←SR; BC←SRC1 DATI
t_2 <SWFR←PCB>
t_3 BUST; GR(SF)
(327)

MTP
MTR00 (345)
READ IN SR (SPL IN OP CODE); POP TOP OF STACK
t_1 <BA←PCB>
t_2 SWFR←SAV2
t_3 BEND
t_4 GR(SF)←SWFR
(151)

MTR10 (151)
CORRECT DR IN CASE DEST. FIELD G; GET TOP OF STACK
t_1 BA←SR; BC←SRC2 DATI
t_2 SWFR←PCB
t_4 BUST
t_6 -DFT: DA←GDC(DF)
DFT: DR←SWFR
(196)

S/48.48 2

BXX*BCOK
BXX.00 (206)-BCO(BNE, BEQ, BPL, BMI, BVC, BCC)
BXX.01 (326)-BCO(BMI, BLOS, BVS, BCS)
BXX.02 (326)-BCO(BR, BNE, BLT, BLE)
BXX.03 (206)-BCO(BNE, BEQ, BPL, BMI, BVC, BCC)
BXX.04 (326)-BCO(BMI, BLOS, BVS, BCS)
BXX.05 (326)-BCO(BGE, BGT, BLT, BLE)

SUCC'SSFUL BRANCH, FIX PC
t_1 <BA←PCB>
t_2 <SWFR←PCB+BXX DISP>
t_3 BEND; BRQ STROBE
t_4 PCA←PCB+BXX DISP
t_5 PCB←PCA
(217)

FET.00 1

BXX*-BCOK *-BRQ
FET.N 1 (321) BPL, BMI, BVC, BCC
FET.12 1 (322) BNE, BGE, BGT
FET.13 1 (324) BCC, BLT, BLE, BMI, BLOS, BVS, BCS

A-FORK 2
FET.01 1 (331) BPL, BMI, BVC, BCC
FET.02 1 (332) BNE, BGE, BGT
FET.03 1 (334) BCC, BLT, BLE, BMI, BLOS, BVS, BCS

INSTRUCTION FETCH

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
11/70		PARTS LIST		

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES
DECIMALS: XXX ± .005; XX ± .02; X ± .1
ANGLES: ±0° 20'
REMOVE BURRS AND BREAK SHARP CORNERS. SURFACE QUALITY ✓
MATERIAL: --
FINISH: --

DRN [illegible] DATE
CHK [illegible] DATE
ENG [illegible] DATE
PROJ. ENG. [illegible] DATE
PM [illegible] DATE 11/6/74

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE: KB11-C FLOW DIAGRAMS (FLOWS 1)
NEXT HIGHER ASSY: B-DD-KB11-B
SIZE/CODE: D FD
NUMBER: KB11-C-1
REV:
SCALE: --
SHEET 2 OF 15
DIST:

REVISIONS: REV | CHANGE NO | CHK

DEC FORM NO
DRD 388-B

DIGITAL EQUIPMENT CORP.

A-FORK

BIN#SM67

SM7.0B (0A6)
SET INDEX WORD; FIX UP SR, & DR TO POINT BEYOND INDEX WORD IF SP? OR DF?
t, BA←PCB; BC←DATI
t₂ SHFR←PCB+2
t₃ BUS PAUSE
t₄ BRQ←BUS
-SP?: SC←GSC[SP]
SP: SR←SHFR,
-DF?: DC←GDF[DF]
DF: DR←SHFR

SM7.1B (0B9)
DO INDEXING; FIX UP PC TO POINT BEYOND INDEX WORD
t, <BA←PCB>
t₂ SHFR←SR+BR
t₃ SR←SHFR,
PCB←PCA
(101)

SM7.2B (101)
FETCH SRC; NO SL CHECK
t, BA←SR; BC←SRC1 DATI
t₂ <SHFR←PCB>
t₃ BUST; GRC[0]
(102)

SM7.3B (102)
GET SRC
t, BA←SR; BC←SRC1 DATI
t₂ <SHFR←PCB>
t₃ BRQ STROBE
t₄ BUS PAUSE
t₅ BR←BUS
FEN4 BEN/(KSJ) -SM3S7
C-FORK 4

S/S.2B
S/S.3B (0A7)
SRC ADDRS TO SR (INDIRECT)
t, <BA←PCB>
t₂ SHFR←BA,
t₃ SR←SHFR
(102)

S/S.3B (1A8)
FETCH SRC OPERAND; NO SL CHECK
t, BA←SR; BC←SRC2 DATI
t₂ <SHFR←PCB>
t₃ BUST; GRC[0]
(104)

S/S.4B (104)
S/S.4B (104)
GET SRC OPERAND
t, BA←SR; BC←SRC2 DATI
t₂ <SHFR←PCB>
t₃ BRQ STROBE
t₄ BUS PAUSE
t₅ BR←BUS
FEN4 (377)
C-FORK 4

F/CLASS
FOP.0B (101)
MOVE GR TO BR
START FPU
=: <BA←PCB>
t₂ SHFR←DR
t₃ BEND
t₄ FP START
BR←SHFR
(314)

FOP.1B (314)
LD GRC0F3 TO FPU
t₃ FDR←BR
t₄ <BA←PCB>
<SHFR←BR>
FEN4 (377)
C-FORK 4

RTI+RTT
RTI0B (0A6) RTI
RTT0B (0A6) RTT
GET STACK POINTER (SP)
t, <BA←PCB>
t₂ SHFR←BR>
t₃ BEND
t₄ SR←GSC[6]
(178)

RTI.1B (178)
FETCH TOP OF STACK (NEW PC)
t, BA←SR; BC←DATI
t₂ <SHFR←BR>
t₃ BUST; GRC[6]
(216)

RTI.2B (216)
STEP STACK POINTER (POP); ADRS OF NEXT WORD TO BR, GET NEW PC
t, BA←SR; BC←DATI
t₂ SHFR←SR+2
t₃ BUS PAUSE
t₄ GRC[6]←SHFR
t₅ BR←BUS
DR←SHFR,
(213)

RTI.3B (213)
FETCH TOP OF STACK (NEW PS)
t, BA←DR; BC←DATI
t₂ <SHFR←PCB>
t₃ BUST; GRC[7]
t₄ PCB←PCA
(214)

RTI.4B (214)
STEP STACK POINTER; GET NEW PS
t, BA←DR; BC←DATI
t₂ SHFR←DR+2
t₃ BUS PAUSE
t₄ GRC[6]←SHFR
t₅ BR←BUS
(215)

RTI.5B (215)
NEW PS TO PS
t, <BA←DR>
t₂ <SHFR←PCB?>
t₃ PSB←BR
(178)

RTI.6B (178)
CLOCK BREAKS
t, <BA←DR>
t₂ <SHFR←PCB?>
t₃ BRQ STROBE
t₄ CONS ACKN
(217)
FETCH
J

RTS
RTS.0B (0A6)
DST FIELD REG TO PC, GET STACK POINTER (SP)
t, <BA←PCB>
t₂ <SHFR←DR>
t₃ BEND
t₄ PCB←DR
t₅ SC←GSC[6]
PCB←PCA
(220)

RTS.1B (220)
FETCH TOP OF STACK AND STEP SP
t, BA←SR; BC←DATI
t₂ SHFR←SR+2
t₃ BUST
t₄ GRC[6]←SHFR
(224)

RTS.2B (224)
GET TOP OF STACK TO BR
t, BA←SR; BC←DATI
t₂ <SHFR←PCB>
t₃ BUS PAUSE
t₄ BR←BUS
(375)
(375)

RTS.3B
BR (TOP OF STACK) TO DST FIELD REG;
t, <BA←SR>
t₂ SHFR←BR
t₃ BRQ STROBE
t₄ PCB←BR
GRC[DF]←SHFR
t₅ DF?: PCB←PCA
(217)
FETCH
J

SOB
SOB.0B (0A7)
COLD PC TO BR & PC-OFFSET TO AC
t, <BA←PCB>
t₂ SHFR←PCB
t₃ BEND
BRQ STROBE
t₄ PCB←PCB-SOB OFFSET
t₅ BR←SHFR
PCB←PCA
BENWH (242)
SA=1

SA=1
SOB.1B (242)
FALL THRU SOB COLD PC TO PC
t, <BA←SR>
t₂ <SHFR←BR>
t₃ BRQ STROBE
t₄ PCB←BR
t₅ PCB←PCA
(262)

SOB.2B (262)
DECREMENT SRC FIELD REG (LOOP COUNT) & START NEXT INSTR FETCH
t, BA←PCB; BC←DATI
t₂ SHFR←SR-1
t₃ BUST
t₄ GRC[SR]←SHFR
BENR (240)
BRQ
BRK.9B
(240)
-BRQ
FET.1B
1
(266)

MARK
MARK.0B (0A7)
PC+OFFSET TO DR & RS TO SP
t, <BA←PCB>
t₂ SHFR←PCB+MARK OFFSET
t₃ BEND
t₄ SA←GSC[5]
DR←SHFR
(358)

MRK.1B (358)
RS TO PC; DR POINTS TO TOP OF STACK
t, BA←DR; BC←DATI
t₂ <SHFR←SR>
t₃ BUST
t₄ PCB←SR
t₅ PCB←PCA
(236)
(235)

MRK.2B (235)
GET TOP OF STACK, STEP SP
t, BA←DR; BC←DATI
t₂ SHFR←DR+2
t₃ BRQ STROBE
t₄ BUS PAUSE
t₅ GRC[6]←SHFR
t₆ BR←BUS
(234)
(239)

MRK.3B (234)
START FETCH NEXT INSTR & TOP OF STACK TO RS
t, BA←PCB; BC←DATI
t₂ SHFR←BR
t₃ BUST
t₄ GRC[RS]←SHFR
BENIB (240)
BRQ
BRK.9B
(240)
-BRQ
FET.1B
1
(266)

A-FORK 9

CONTROL; FLOATING; INDEXED SOURCE

PART USED ON OPTION/MODEL	QTY	DESCRIPTION	PART NO.	ITEM NO.
11/70		PARTS LIST		

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES
TOLERANCES
DECIMALS: XXX ± .005, XX ± .02, X ± .1
ANGLES: ± 0 30'
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓
MATERIAL
FINISH

DRN — DATE
CHK'D — DATE
ENG — DATE 4-9-75
PROJ. ENG. — DATE 4-9-75
PROD — DATE 12-5-75

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: KB11-C FLOW DIAGRAMS (FLOWS 2)

NEXT HIGHER ASSY: B-DD-KB11-B

SIZE	CODE	NUMBER	REV.
D	FD	KB11-C-1	

SCALE
SHEET 3 OF 15
DIST

REV	REVISIONS	CHANGE NO	CHK

DEC HDW NO 030 000-0

KB11-C-1

DIGITAL EQUIP. CORP.

A-FORK

RESET (RESET)

RCC.00 (RCC) (9-5)
GET RB TO DR
c1 <BA←PCB>
c2 <SMFR←BR>
c3 BEMD
c4 DR←GDCB>

RES.10 (RES) (557)
INIT IP IN KERNEL MODE
c1 <BA←PCB>
c2 <SMFR←DR>
c3 START INIT
IF AS 14 (9)

RCS.20 (RCS) (529)
WAIT FOR INIT DONE
SHOW PC AND RB
c1 BA←PCB
c2 SMFR←DR
c3 DMO STROBE
c4 CASL ACRN
RIP BEMD (334)

-RIP
FET.68 1 (334)

HALT

HLT.00 (HLT) (9-8)
GET RB AND PS | PC TO SR
c1 <BA←PCB>
c2 SMFR←PCB
c3 BEMD
c4 BR←PS
DR←GD[CB]
SR←SMFR

HLT.10 (HLT) (516)
SET CONSOLE FLAG IF KERNEL MODE OTHERWISE TRAP
c1 <BA←PCB>
c2 <SMFR←BR>
c3 CONF←1 IF PSW14

BEMD 06 (186)
BRK(1) TRAP2 15 (184)
BRK(0)
FET.04 1 (164)

CCOP

CCP.00 (CCP) (529)
CONDITION CODE OPERATE INSTR
c1 <BA←PCB>
c2 <SMFR←BR>
c3 DMO STROBE
BEMD
c4 CC←IR
CLEAR OR CLR SEL BIT(4)
(217)
FET.00 1

OP 2
OP 7
IOT
TRAP 08 15 (842)
TRAP 01 15 (819)
RESD.01 15 (817)

WAIT

WAT.00 (WAI) (9-11)
READ RB AND SHOW IT
SHOW PC IN ADRS LIGHTS
c1 BA←PCB
c2 SMFR←DR
c3 BEMD
c4 DR←GDCB>
BEMD (WAI)
BRQ
-BRQ
WAT.10 WAIT.W (264) (233)
NO BREAK REQUESTS
c1 BA←PCB
c2 SMFR←DR
c3 DMO STROBE
(WAI)

WAT.20 (249)
BREAK REQUEST; GET VECTOR AND SET HALT & S
c1 <BA←PSB>
c2 SMFR←'V'
INTR ANSWR
DR←SMFR
BA←BVR
BEMD 22 (125)
CONF COM.01 15 (167)
-CONF

WAT.30 (183)
SET UP INSTR CYCLE
NO CONFIRM
c1 <BA←PCB>
c2 <SMFR←BA>
(PWRF+INTRF) BEMD (830)
(PWRF+INTRF)
BRKN 15 (850)

OP 2
RESD.02 15 (9-12)

SPL
SPL.00 (SPL) (9-12)
SET PRIORITY LEVEL
c1 <BA←PCB>
c2 <SMFR←BA>
c3 BEMD
c4 BR|PS[7:5]←BR[3:0]
IF KERN MODE
(SPL)

SPL.10 (SPL) (961)
START FETCH OF NEXT INSTR
c1 BA←PCB; BCO←BAT1
c2 <SMFR←PCB>
c3 BUST
CLR FLAGS
(SPL)
FET.10 1

RSVD + EMT + TRAP
RESD.00 15 (9-8)

F(CLASS#-(FP PRESENT)
A-FORK 5
RESD.08 15 (808)

A-FORK

(JMP+JSR)DMP
RCLOG 15 (BOB)

NEG.B DMP
NEG.78 (784)
COMPLEMENT DST FIELD (B)
c1 <BA←PCB>
c2 SMFR←ALUB
(A=DR, B=1)
c3 BEMD
c4 SR←SMFR
(218)
NEG.90 (218)
INCREMENT AND SHIFT DST
c1 <BA←SR>
c2 SMFR←SR+1
c3 DMO STROBE
c4 RCA←SR+1
-I(CLASS: GR(DST)←SMFR
CCLDB
DF7! RCB←RCA
(817)
RFT.08 1

ASH # DMP
RSH 10 7 (882)

ASHC # DMP
REC.10 7 (853)

MFP # DMP
MFPRR 11 (894)

E(CLASS # -[DF7+BRQ]*DMP
EIC.00
EIC.00 (EIC) (828)
SRC MODE & DST MODE & FETCH SRC OF THIS AND FETCH NEXT INSTR
c1 BA←PCB: SRC-PTR
c2 SMFR←ALU(A=DA, B=SA)
c3 DMO STROBE
c4 DMA PAUSE
c5 -I(CLASS: GR(OP)←SMFR
c6 CCLDB
IRR-BUS | BA-BUS
RCB←RCA
(879)
IRQ.00 1

E(CLASS # [DF7+BRQ]*DMP
EIC.90
EIC.90 (EIC) (826)
SOURCE & DST MODE & FETCH EXECUTE OF THIS INSTR (NEW PC)
c1 BA←PCB
c2 SMFR←ALU(A=DA, B=SA)
c3 DMO
BRQ STROBE
c5 RCA←ALU
-I(CLASS: GR(OP)←SMFR
c6 CCLDB
DF7! RCB←RCA
(817)
FET.90 1

MUL # DMP
MUL.00 (MUL) (8-10)
SETUP SHIFT COUNTER
c1 <BA←PCB>
c2 <SMFR←DA>
c3 BEMD
SC←17
(MUL)
MUL.10 8

DIV # DMP
DVS.00 (DVS) (861)
DIVISOR TO BR
c1 <BA←PCB>
c2 SMFR←DR
c3 BEMD
c4 BR←SMFR
(861)
DIV.00 9

F(CLASS:=SWAB+CLR.B+COM.B+INC.B+DEC.B+NEG.B+ADC.B+SBC.B+ASR.B+ASL.B+ROR.B+ROL.B+SXT.B+BIS.B+ADD+SUB+SXT+MOV.B+XOR
I(CLASS:=TST.B+CMP.B+BIT.B+MUL+DIV+MFP
E(CLASS:=[F(CLASS=-NEG.B]+MOV+TST.B+CMP.B+BIT.B

A-FORK 5

EXECUTE NO MEM REF

FIRST USED ON ORDER/PROTO	QTY	DESCRIPTION	PART NO.	ITEM NO
11/70		PARTS LIST		

UNLESS OTHERWISE SPECIFIED
DIMENSIONS IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINISH SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL —
FINISH —

		DATE
DRN		
CHK'D	K. Clark	7-9-73
ENG		
ENG		7-9-73
MFG		7-9-73
QA		7-9-73

DIGITAL EQUIPMENT CORPORATION
MAYNARD MASSACHUSETTS

TITLE
KB11-C
FLOW DIAGRAMS
(FLOWS 3)

SIZE/CODE	NUMBER	REV
D FD	KB11-C-1	

NEXT ASSY	USED ON
8-DD-KB11-B	

SCALE —
SHEET 4 OF 15
DIST

REVISIONS: REV | CHANGE NO | DWN

DEC 1-0000 ND
DRO 1002A

KB11-C-1
FD

C-FORK

DMØ* - F/CLASS * -DF7 * SRØ(Ø)

DMØ* - F/CLASS * -DF7 * SRØ(1)

DØØ.Ø1 (202)
ODD BYTE SRC, RIGHT JUSTIFY
t_4 <BA ← DR>
t_5 SHFR ← SWAP(DR)
t_6 SRC STROBE
t_7 BR ← SHFR
(205)

DMØ* - F/CLASS * DF7 * SRØ(E)

DØ7.ØE (202)
MODIFYING THE PC
t_4 <BA ← DR>
t_5 SHFR ← BR
t_6 BR ← SHFR
(Ø3Ø)

DMØ* - F/CLASS * DF7 * SRØ(1)

DØ7.Ø6 (202)
MODIFYING THE PC- ODD BYTE
t_4 <BA ← DR>
t_5 SHFR ← SWAP(BR)
t_6 BR ← SHFR
(Ø3Ø)

DMØ* F/CLASS

FOR 2Ø (211)
GET CC AND SEE IF FP SYNC = 1
t_5 <BA ← ACONX>
t_6 <SHFR ← DR>
READ FPS
t_6 BR ← BUS

FOR 6Ø BENTY (?, 3)

DØØ.ØØ (2ØC)
DST MODE Ø BUT SRC MODE NOT FINISH) EXECUTE THIS & REVIEW NEXT
t_4 BA ← ACB; DC ← DATI
t_5 SHFR ← ALU $
(A = DR, B = BR)
t_6 BUST
t_8 -3/CLASS: GR[DF] ← SHFR
t_6 CCLD $
BENIE (Ø1Ø)

BRQ

BRK.9Ø (2Ø4)
Ø

-BRQ

FET.1Ø (264)
1

EXC.9Ø (2Ø2)
Ø

FOP.3Ø (133)
GET CC'S AND WAIT FOR FP
READ FPS
BRQ STROBE
t_6 BR ← BUS

BENTY (173)

-(BRQ + SYNC)

BRQ

SYNC* - BRQ

FOR 5C (173)
TELL FPU TO EXECUTE
FP START
<BA ← ACONX>
<SHFR ← BR>
t_4 CC ← BR ; EN FPP

BENTY (333)

FOP.6Ø (153)
CC TO SERVICE SET BACK PC
READ FPA
t_6 BR ← BUS

(245)

FSV.9Ø (2Ø) (245)

FP REG WR

~FP REG WR

FET.26 (373)

FOP 5Ø (333)
GET FP DATA
t_3 BRQ STROBE
t_4 <BA ← ACONX>
FP READ DATA
t_5 <SHFR ← BR>
t_6 BR ← BUS
(365)

FET ØB (365)
WRITE GR AND START FETCH
BA ← PCB
BC ← DATI
SHFR ← BR
GR[DF] ← SHFR
BUST

BE·1128 (24Ø)

BRK.7Ø (24Ø)
BRQ

-BRQ

FET.1Ø (26Ø)

DMØ = IR(5-3) = Ø + FCLASS * IR(11-6) = Ø

DESTINATION MODE Ø

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
11/7Ø		PARTS LIST		

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES TOLERANCES
DECIMALS .XXX ± .ØØØ .XX ± .Ø2 .X ± .1 ANGLES ± Ø° 3Ø'
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓
MATERIAL //
FINISH //

DSN [redacted] DATE 12-9-75
CHK'D [redacted] DATE 7/8/76
ENG [redacted] DATE 12-9-75
PROJ [redacted] DATE 12-9-75
PROG [redacted] DATE 12/9/75

NEXT HIGHER ASSY. B-DD-KB11-B
SCALE //
SHEET 5 OF 15

EQUIPMENT CORPORATION [redacted]

TITLE KB11-C FLOW DIAGRAMS (FLOWS 4)

SIZE D CODE FD NUMBER KB11-C-1 REV.

DIST

REVISIONS	REV.	CHANGE NO	CHK

KB11-C-1

DIGITAL EQUIP. CORP.

A-FORK

DAC ← DM12

DI8.00 (DI8.01) (DI8.02) (DI8.03) (111)

DESTINATION ADDR IN DR
SRC OPERAND IN BR & SA ;
CHECK STACK LIM.

t₁ BA←DR ; BC←BSOP1
t₂ SHFR←BR
t₃ BUST ; GR[DF]
t₄ BR←SHFR

BENIS (118)

DM12 ← SAS(1)

DI8.00 (111)

DST ADDR IN DR, SRC
OPERAND IN BR & SA
CHECK STACK LIMIT

t₁ BA←DR ; BC←BSOP1
t₂ SHFR←BR
t₃ BUST ; GR[DF]
t₄ SA←SHFR

BENIS(118)

DM12 ← SAS(1)

DI8.00 (111)

DST ADDR IN DR ; RESULT
INTO DST SRC
CHECK STACK LIMIT

t₁ BA←DR ; BC←BSOP1
t₂ SHFR←SWAP(BR)
t₃ BUST ; GR[DF]
t₄ SA←SHFR

BENIS(118)

DM8 ← SAS(1)

DI8.00 (111)

FETCH DST OPERAND ADDR
SRC OPERAND IN GR & SA

t₁ BA←DR ; BC←DATI
t₂ SHFR←BR
t₃ BUST ; GR[DF]
t₄ GR←SHFR

(221)

DM8 ← SAS(1)

DI8.00 (111)

FETCH DST OPERAND ADDR
RESULT ADDR'S SRC TO SA

t₁ BA←DR ; BC←DATI
t₂ SHFR←SWAP(BR)
t₃ BUST ; GR[DF]
t₄ SR←SHFR

(221)

DAC ← DM12

DI8.00 (111)

FETCH DST OPERAND ADDR
SRC IN SA

t₁ BA←DR ; BC←DATI
t₂ <SHFR ← SA>
t₃ BUST ; GR[DF]

(221)

DI8.10 (221)

SET DST OPERAND ADDR
STORE DST ADDR REGISTER

t₁ BA←DR ; BC←DATI
t₂ SHFR←DR+DSTCON
t₃ BUS PAUSE
t₄ PCA←DR+DSTCON
GR[DF]←SHFR
BR←BUS
DF7: PCB←PCA

(233)

DI8.20 (312)

FETCH NEXT INSTR
SET CONDITION CODES

t₁ BA←PCB ; BC←DATI
t₂ SHFR←BA
t₃ BUST ; GR[DF]
t₄ CCLD

BENIS (249)

BRQ → BRK.RQ 12 (244)

- BRQ → FET.10 1 (264)

O/CLASS

DI8.60 (155)

STEP DST FIELD REG ;
OUTPUT SRC TO DST(DATO)

t₁ BA←DR ; BC←BSOP1
t₂ SHFR←DR+DSTCON
t₃ BRQ STROBE
t₄ BUS PAUSE
t₅ PCA←DR+DSTCON
GR[DF]←SHFR
t₆ DF7: PCB←PCA

(316)

-FJ/CLASS = -O/CLASS

DI8.16 (175)

FINISH DATIP OR DATI ;
STEP DST FIELD REG

t₁ BA←DR ; BC←BSOP1
t₂ SHFR←DR+DSTCON
t₃ BUS PAUSE
t₄ BRQ STROBE
t₅ PCA←DR+DSTCON
GR[DF]←SHFR
t₆ BR←BUS
DF7: PCB←PCA

BENGS (137) PEN 2

DR8(1) → DI8.30

DR8(0) → B-FORK 7

DI8.36 (137)

ODD BYTE DST, RIGHT JUSTIFY

t₁ <BA←DR>
t₂ SHFR←SWAP(BR)
t₃ BR←SHFR

PENB (371)

B-FORK 7

FJ / CLASS

DI8.70 (135)

STEP DST FIELD REGISTER

t₁ <BA←DR>
t₂ SHFR←DR+DSTCON
t₃ BEND
BRQ STROBE
t₄ PCA←DR+DSTCON
GR[DF]←SHFR
t₅ DF7: PCB←PCA

PENE (137)

B-FORK 7

BIN:=MOV.B+CMP.B+BIT.B+BIS.B+BIC.B+ADD+SUB

DAC:=[I/CLASS+A/CLASS]#[C-BIN+SNGL]+[MOV+SNGL]+ASH+ABSMC+JMP+JSR

O/CLASS:=MOV+MTP

F/CLASS:=IR<15:12>(17)

J/CLASS:=JMP+JSR

FJ/CLASS:=F/CLASS+J/CLASS

BSOP1:=[I/CLASS:DATI]+[CP/CLASS:DATIP]+[CO/CLASS:DATO]

BSOP2:=[DATO]+[BYTE INSTRUCTION:DATOB]

DESTINATION MODES 1-3

FIRST USED ON OPTION/MODEL	QTY	DESCRIPTION	PART NO.	ITEM NO.
11/70		PARTS LIST		

UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL —
FINISH —

	NAME	DATE
DRN		7-72
CHKD		10-72
ENGR		1-2-73
MGR		1-2-73
QA		1/19/73

NEXT HIGHER ASSY B-DD-KB11-B

SCALE —
SHEET 6 OF 15

DIGITAL EQUIPMENT CORPORATION

TITLE KB11-C FLOW DIAGRAMS (FLOWS 5)

DRAWING NUMBER DFD KB11-C-1 REV

SHEET

REVISIONS REV | CHANGE NO | DATE

DEC 10990 100 0004

KB11-C-1 DFD B 2

DIGITAL EQUIP. CORP.

AFORK

C-FORK

DM45*SRB(0)

D46.0B (115)
STEP DST FIELD REGISTER
t, <BA←DR>
t2 SNFRA←DR-DSTCON
t3 PCA←DR-DSTCON
GRCDF3←SNFR
t4 DRE←SNFR
DF7: PCB←PCA

BENBK(182)

-DM357

DM357

D47.3B (181)
DATIA DATI, DATO DST SRC OPERAND TO SR; CHECK STACK LIMIT
t, BA←DR; BC←BSOP1
t2 SNFR←SR
t3 BUST; GRCDF3
t4 SR←SNFR

D47.2B (161)
FETCH DST OPERAND ADRS; SRC OPERAND TO SR
t, BA←DR; BC←DATI
t2 SNFR←SR
t3 BUST; GRCDF3
t4 SR←SNFR
(231)

D/B/6 6

BENIS(157) PEN2

DM96*SRB(1)

D45.9B (114)
STEP DST FIELD REGISTER; ODD BYTE SOURCE
t, <BA←DR>
t2 SNFRA←DR-DSTCON
t3 BRQ STROBE
t4 PCA←DR-DSTCON
GRCDF3←SNFR
t5 DRE←SNFR
DF7: PCB←PCA

BENBI(130)

-DM357

D48.3B (131)
DATIB DATI, DATO DST; RIGHT JUSTIFY SRC TO SR; CHECK STACK LIMIT
t, BA+DR; BC←BSOP1
t2 SNFRA←SWAP(BA)
t3 BUST; GRCDF3
t4 SR←SNFR

BENIS(170) PEN2

-FJ/CLASS

D/B/6 6 (177)

FJ/CLASS

B-FORK 7

DM357

D47.3B (171)
FETCH DST OPERAND ADRS; RIGHT JUSTIFY SRC TO SR
t, BA←DR; BC←DATI
t2 SNFR←SWAP(BA)
t3 BUST; GRCDF3
t4 SR←SNFR
(231)

D/B/.1B

D48.1B (231)
GET DST OPERAND ADRS
t, BA←DR; BC←DATI
t2 <SNFR←BR>
t3 BUS PAUSE
t4 BR←BUS
(288)

D/B/.2B

D48.2B (288)
DST OPERAND ADRS TO DR
t, <BA←DR>
t2 SNFR←BR
t3 BRQ STROBE
t4 DRE←SNFR
(311)

D48.5B (311)
DATIA DATI, DATO DST SRC OPERAND TO BR
t, BA←DR; BC←BSOP1
t2 SNFR←SR
t3 BUST; GRCDB3
t4 BRE←SNFR

BENIS(157) PEN2

DAC*DM45

D45.6B (004) DM6
(005) DM5
STEP DST FIELD REGISTER
t, <BA←PCA>
t2 SNFRA←DR-DSTCON
t3 BEND
t4 PCA←DR-DSTCON
GRCDF3←SNFR
t5 DRE←SNFR
DFT: PCA←P.A

BEN0I(182)

DM357

D/B/.6B

D48.6B (162)
FETCH DST OPERAND ADRS
t, BA←DR; BC←DATI
t2 <SNFR←PCB>
t3 BUST; GR.CDF3
(231)

-DM357

DM357

D/B/.1B

DM96*SRB(0)

D47.8B (117)
FETCH INDEX WORD; SRC TO SR
t, BA←PCB; BC←DATI
t2 SNFR←BA
t3 BUST; GRCDB3
t4 SR←SNFR

(286)

DM67*SRB(1)

D47.9B (116)
FETCH INDEX WORD; RIGHT JUSTIFY SRC TO SR
t, BA+PCB; BC←DATI
t2 SNFR←SWAP(BA)
t3 BUST; GRCDB3
t4 SR←SNFR

(225)

DAC*DM67

D47.6B (006) DM6
D47.6I (007) DM7

GET INDEX WORD; ADJUST DST IF DST=PC

t, BA←PCB; BC←DATI
t2 SNFR←PCB+2
t3 BUS PAUSE
t4 ACA←PCB+2
t5 BR←BUS
- DFT: DRE←GRCDF3
DFT: DR←SNFR

(251)

D47.1B (251)

DO INDEXING, STEP PC;

t, <BA←PCB>
t2 SNFR←BR+DR
t3 BRQ STROBE
t4 DR←SNFR
PCB←PCA

BEN0I(182)

-DM357

DM357

D/B/.6B 6 (162)

D/B/.3B (122)
DATIA DATI, DATO LST SRC OPERAND TO BR; CHECK STACK LIMIT
t, BA←DR; BC←BSOP1
t2 SNFR←SR
t3 BUST; GRCDF3
t4 BRE←SNFR

BENIS(157) PEN2

-O/CLASS*-FJ/CLASS

D/B/.6B

D/B/.6B (177)
FINISH DATIA, DATI DST
t, BA←DR; BC←BSOP
t2 <SNFR←BR>
t3 BUS PAUSE
t4 BRQ STROBE
t5 BR←BUS

(137)

D/B/.3B 5

DEQ(1)

BENIS(157) PEN2

DSKIP(1)

B-FORK 7

O/CLASS

D/B/.9B

D48.9B (157)
FINISH DSTB DST; LOAD CCLS
t, BA←DR; BC←BSOP
t2 SNFR←BR
t3 BRQ STROBE
t4 BUS PAUSE
t5 CCLOE

(231)

FETCH 1

FJ/CLASS

B-FORK 7

DESTINATION MODES 4-7

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
11/70		PARTS LIST		

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES
DECIMALS .XXX ± .005, .XX ± .02, .X ± .1; ANGLES ±0° 30'
REMOVE BURRS AND BREAK SHARP CORNERS. SURFACE QUALITY ✓
MATERIAL —
FINISH —

		DATE
D&M	-	-'70
CHIEF		12/1/70
ENG		12/1/70
MFG CONTROL		12/1/70
PROJ		12/1/70

NEXT HIGHER ASSY: B-DD-KB11-B
SCALE —
SHEET 7 OF 15

EQUIPMENT CORPORATION — MAYNARD, MASSACHUSETTS

TITLE: KB11-C
FLOW DIAGRAMS
(FLOWS 6)

SIZE D | CODE DFD | NUMBER KB11-C-1 | REV.
DIST.

KB11-C-1

REVISIONS: REV | CHANGE NO | DWN

B-FORK

ASH

ASH.0B (168)
SHIFT COUNT TO DR;
c, <BA← DR>
c₂ SHFR←BA
c₃ ABS←SHFR
(BEN)

ASH.1B (158)
LOAD STEP COUNTER WITH SHIFT COUNT
c, <BA←PCB>
c₂ <SHFR←SR>
c₃ BEND
SCD←DR

ASH.2B (168)
STEP SC; SET COND CODES & SEE IF NO SHIFT
c, <BA←DR>
c₂ SHFR←SR
c₃ ARO STROBE
SCD←SCSI
c₄ CCLDA
CSIGN ACC SHFR; C←V←0

BENCS(217)

SC>0 → ASH.4B (157) (166)
SHIFT LEFT (ZERO INSERTION) CC'S NEFT CURRENT
c, <BA←PCB>
c₂ SHFR←SHL(SR)
c₃ ARO STROBE SCD←SCSI
c₄ GRCSF)←SHFR
c₅ SBA←SHFR
CCLDS
CSIGN ACC SHFR; C←MSB XOR MSB-1
V←1 IF SHIFT IS 1 MORE THAN COUNT

BENCS(182) SC≠0

SC=0 → FET.06 1 (126)

SC<0 → ASH.3B (127)
SHIFT RIGHT SIGN EXTENDED; CC'S NEFT CURRENT
c, <BA←PCB>
c₂ SHFR←SHR(SR)
c₃ ARO STROBE SCD←SCSI
c₄ GRCSF)←SHFR
c₅ SBA←SHFR
CCLDS

BENCS(127) SC≠0

SC=0 → FET.07 1 (137)

SC=0 → REFSB 1 (217)

ASHC

ASC.0B (164)
SHIFT COUNT TO DR
c, <BA←DR>
c₂ SHFR←BA
c₃ ABS←SHFR
(BEN)

ASC.1B (154)
LOAD STEP COUNTER, READ AD-DRESS OPERAND TO DR
c, <BA←PCB>
c₂ <SHFR←SR>
c₃ BEND
SCD←DR
c₄ DR←DR OR SHFR(17)

ASC.2B (164)
STEP SC; SET COND CODES & SEE IF NO SHIFT
c, <BA←DR>
c₂ SHFR←SR
c₃ ARO STROBE SCD←SCSI
c₄ BBA←SHFR SCLD 0
CSIGN ACC SHFR; C←V←0

BENCS(207)

SC<0 → ASC.4B (157)
SHIFT RIGHT; SR→ AR; DR←10; SET COND CODES ON AR
c, <BA←DR>
c₂ SHFR←SHR(SR)
c₃ ARO STROBE SCD←SCSI
c₄ GRCSF)←SHFR
c₅ SBA←SHFR DBA←RESULT(DR) C.ALUB INSERTED CCLDB
CSIGN ACC SHFR; C←DARB V←0

BENCS(207) SC≠0

SC=0 → ASC.5B (157)
SHIFT DONE; SAVE AD DRESS, SET COND CODES ON LO; START FETCH NEXT INSTR.
c, BA←PCB; BC←DATI
c₂ SHFR←DR
c₃ BUST
c₄ GRCSF,13←SHFR
c₅ CCLDS
CALC EV MM; E←E OLD IF SHFR=0

BENI2(208)

SC>0 → ASC.3B (247) (176)
SHIFT LEFT; SR→AR; DR←10; SET COND CODES ON AR
c, <BA←DR>
c₂ SHFR←ALUS(0←SR,0←)
CSHL(SR)←DR(15)
c₃ ARO STROBE SCD←SCSI
c₄ GRCSF)←SHFR
c₅ SBA←SHFR DR←LEFT(DR) (0 INSERTED) CCLDS
CSIGN ACC SHFR; C←MUX(15); V←10LLA+(SIGN CHANGES)

BENCS(176) SC≠0

SC=0 → ASC.6B (227) (136)
SHIFT DONE; SAVE AD DRESS, SET COND CODES ON LO; START FETCH NEXT INSTR.
c, BA←PCB; BC←DATI
c₂ SHFR←DR
c₃ BUST
c₄ GRCSF,13←SHFR
c₅ CCLDS
CALC EV MM; E←E OLD IF SHFR=0

BENI2(248)

F/CLASS

FPP 7B (226)
DST ADDR TO BE ENABLE FP ATTN
c, <BA←DR>
c₂ SHFR←DR
c₃ BEND
c₄ BBA←SHFR FP ATTN

BEN(T:307)

-(SYNC+BRQ) → FSV-6B /3 (327)

BRQ → FSV-7B /3 (347)

SYNC←BRQ → FSV-9B /3 (367)

B-FORK

-BEQ → FET.1B 1 (260)

BEQ → BRK.9B 1B (240)

ASH & ASC

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	FIND NO.
11/70		PARTS LIST		

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES
DECIMALS XXX ± .010, XX ± .02, X ± .1; ANGLES ±
REMOVE BURRS AND BREAK SHARP CORNERS. SURFACE QUALITY ✓
MATERIAL
FINISH

DRWN — DATE 1-20
CHKD — DATE 11-30-72
ENGR — DATE 12-25
PROJ MGR — DATE 12-25
QA — DATE 11/9/72

NEXT HIGHER ASSY: B-DD-KB11-B
SCALE
SHEET 5 OF 15

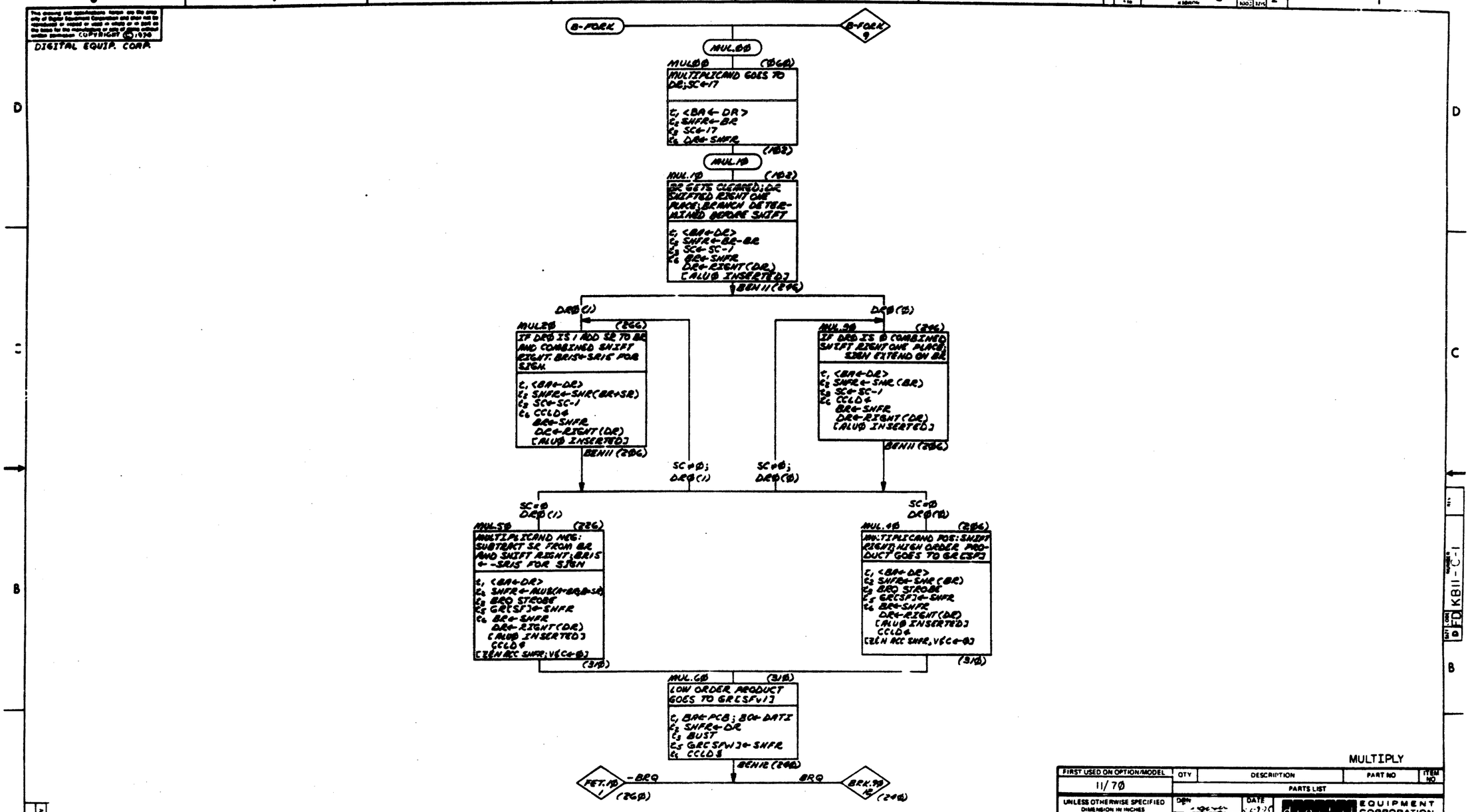
EQUIPMENT CORPORATION

TITLE: KB11-C FLOW DIAGRAMS (FLOWS 7)

SIZE D | CODE FD | NUMBER KB11-C-1 | REV.

DIST.

REVISIONS	REV	CHANGE NO	CHK



MULTIPLY

FIRST USED ON OPTION/MODEL	QTY	DESCRIPTION	PART NO	ITEM NO
11/70	PARTS LIST			

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES TOLERANCES
DECIMALS XXX ± .005, XX ± .02, X ± .1 ANGLES ± 0° 30'
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓
MATERIAL —
FINISH —

DRN — DATE 12/20/74
CHK — DATE 12/24/74
ENG — DATE 12-27-74
PROJ ENG — DATE 12-27-74
SUPV — DATE 12/19/75

NEXT HIGHER ASSY: B-DD-KB11-B
SCALE —
SHEET 9 OF 15

digital EQUIPMENT CORPORATION

TITLE: KB11-C FLOW DIAGRAMS (FLOWS 8)

SIZE D | CODE FD | NUMBER KB11-C-1 | REV

DIST

REVISIONS: REV | CHANGE NO | CHK

DRAWING 42-332 1968-0

DEC FORM NO DRD 1B8-0

KB11-C-1

DIGITAL EQUIP. CORP.

B-FORK

B-FORK (11)

LIKDB

DIKDB (186)
DIVISOR GOES TO SR, LOAD CONDITION CODE TO SEE IF IT IS ZERO; HIGH ORDER DIVIDEND GOES TO DR
t1 <BA←DR>
t2 SHFR←BR
t3 SR←SHFR
DR←GDCSF)
CCLD$
[NEW ARC SHFR; V(C←0)]
(254)

DIV.1B (254)
BRANCH ON DIVISOR 0; LOAD CONDITION CODE TO TEST THE SIGN OF DIVIDEND
t1 <BA←SR>
t2 SHFR←DR
t4 CCLD$
[NEW ARC SHFR; V(C←0)]

BEN02 (282)

0 — DVZ.0B (272)
DIVISOR IS ZERO, ABORT DIVIDE; SET C AND V BIT; GO FETCH NEXT INSTRUCTION
t1 <BA←DR>
t2 <SHFR←SR>
t3 BRQ STROBE
t4 CCLD$
(164)
→ FETCH 1

-0 — DIV 2B (282)
DIVISOR IS NON ZERO; BRANCH ON DIVIDEND NEG; SR HAS DIVISOR; DR HAS HIGH ORDER DIVIDEND
t1 <BA←DR>
t2 <SHFR←SR>

BEN04 (241)

N — DVN.0B (254)
DIVIDEND IS NEGATIVE, GOT TO MAKE IT POSITIVE. GET LOW ORDER DIVIDEND IN SR; BR HAS DIVISOR SAVED
t1 <BA←DR>
t2 <SHFR←SR>
t3 CLEAR DR
t4 SR←GSCSF.V1]
(188)

DVN.1B (188)
FIND TWO'S COMPLEMENT OF LOW ORDER AND WRITE IT BACK; DR IS 0
t1 <BA←DR>
t2 SHFR←DR-SR
t4 GRCSF.V1]←SHFR
(185)

DVN.2B (185)
TEST IF THERE WAS A CARRY OUT OF THE LOW ORDER DIVIDEND; PUT IT IN DR
t1 <BA←DR>
t2 SHFR←DR-SR
t4 DR←LEFT(DR)
[ALU CARRY INSERTED]
(186)
→ DVN.3B

-N — DVR.0B

DVN.3B (186)
MAKE DR 0 IF THERE WAS A CARRY OR A -1 IF NOT; GET THE HIGH ORDER DIVIDEND TO SR
t1 <BA←DR>
t2 SHFR←DR-1
t4 SR←GSCSF]
DR←SHFR
(185)

DVN.4B (185)
FIND TWO'S COMPLEMENT OF HIGH ORDER DIVIDEND IF THERE WAS A CARRY FROM LOW ORDER, ELSE ONE'S COMPLEMENT WRITE IT BACK; LOAD COND CODES
t1 <BA←DR>
t2 SHFR←DR-SR
t3 GRCSF]←SHFR
t4 DR←SHFR
CCLD$
[NEW ARC SHFR; V(C←0)]
(184)

DVN.5B (184)
SR GETS DIVISOR; BRANCH ON SIGN OF DIVIDEND
t1 <BA←DR>
t2 SHFR←BR
t4 SR←SHFR

BEN00 (248)

N — DVE.1B (248)
THE TWO'S COMPLEMENT OF A NEGATIVE NUMBER IS STILL NEGATIVE; MUST BE MOST NEG. NO. ABORT DIVIDE; SET V & C BITS
t1 <BA←DR>
t2 <SHFR←BR>
t4 CCLD$
(195)
→ DVE.2B 9

-N — DVN.6B (248)
HIGH ORDER DIVIDEND GOES TO BR; SR HAS DIVISOR
t1 <BA←DR>
t2 SHFR←DR
t4 BA←SHFR
(187)

DVN.7B (187)
DR GETS LOW ORDER DIVIDEND; SC GETS THE COUNT; SET N TO SHOW DIVIDEND WAS NEG
t1 <BA←DR>
t2 SHFR←DR
t3 SC←17
t4 DR←GDCSF.V13
CCLD$
[NEW ARC SHFR; V(C←0)]
(197)
→ DIV.3B 9

DVR.0B
-N
DVR.0B (241)
DIVIDEND IS POSITIVE; BR GETS THE HIGH ORDER DIVIDEND; SR HAS DIVISOR
t1 <BA←SR>
t2 SHFR←DR
t4 BR←SHFR
(183)

DVR.1B (183)
DR GETS THE LOW ORDER DIVIDEND; SC GETS THE COUNT
t1 <BA←SR>
t2 <SHFR←DR>
t3 SC←17
t4 DR←GD [SFV1]
(187)

DIV.3B
DIV.3B (197)
START FIRST DIVISION; SHIFT BR LEFT INSERT DR15; SET 2 BIT
t1 <BA←DR>
t2 SHFR←ALU$(A←BR,B←)
t4 BR←SHFR
CCLD$
[N←N, C, V ← 2←1]

BEN16 (346)

SR15 (0) — DIV.4B (346)
DIVISOR POSITIVE DO A SUBTRACTION TO FIND BIT 15 OF QUOTIENT
t1 <BA←DR>
t2 SHFR←BR-SR
t3 SC←SC-1
t4 BR←SHFR
DR←LEFT(DR)
[ALU CARRY INSERTED]
CCLD6
[Z←ZCLD*SHFR=0]
(213)

SR15 (1) — DIV.5B (346)
DIVISOR IS NEGATIVE, DO AN ADDITION TO FIND BIT 15 OF QUOTIENT
t1 <BA←DR>
t2 SHFR←BR+SR
t3 SC←SC-1
t4 BR←SHFR
DR←LEFT(DR)
[ALU CARRY INSERTED]
CCLD6
[Z←ZCLD*SHFR=0]
(310)

DIVC.0B (313)
CONTINUE DIVIDE IF QUOTIENT WILL BE POS. BUT ALLOW FOR MOST NEG NO. IF QUOT IS TO BE NEG.
t1 <BA←DR>
t2 <SHFR←BR>

BEN05 (195)

DIV QUIT — DVE.2B
DVE.2B (195)
DIVISION OVERFLOW, RESULTS WON'T FIT IN 16 BITS, V BIT IS SET; GO FETCH NEXT INSTR.
t1 <BA←SR>
t2 SHFR←DR
t3 BRQ STROBE
t4 CCLD7
[C←ALU CARRY]
(164)
→ FETCH 1

-DIV QUIT — DIV.7B (195)
FINISH DIVISION; SHIFT BR LEFT INSERT DR15; DR IS FORMING QUOTIENT BR AS REMAINDER
t1 <BA←DR>
t2 SHFR←ALU$(A←BR,B←)
t4 BR←SHFR

BEN04 (328)

DIV SUB — DIV.8B (328)
SIGNS OF DIVISOR & PART. REMAINDER ARE SAME SUBTRACT; DR IS -SIGN OF REMAINDER
t1 <BA←DR>
t2 SHFR←BR-SR
t3 SC←SC-1
t4 BR←SHFR
DR←LEFT(DR)
CALU CARRY INSERTED]

-DIV SUB — DIV.9B (328)
SIGNS OF DIVISOR & PARTIAL REMAINDER ARE DIFFERENT ADD; DR IS -SIGN OF REMAINDER
t1 <BA←DR>
t2 SHFR←BR+SR
t3 SC←SC-1
t4 BR←SHFR
DR←LEFT(DR)
CALU CARRY INSERTED]

BEN03 (185) — SC≠0
BEN03 (185) — SC=0

SC=0
DVC.0B (185)

DIVIDE

FIRST USED ON OPTION/MODEL	QTY	DESCRIPTION	PART NO.	ITEM NO.
11/70	PARTS LIST			

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES
TOLERANCES
DECIMALS: XXX ± .005, XX ± .02, X ± .1
ANGLES: ± 0° 30'
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓
MATERIAL —
FINISH —

DRN. — DATE 2-9-73
CHK'D [illegible] DATE 12/4/74
ENG. [illegible] DATE 12-9-75
PROJ. MGR. [illegible] DATE 12-9-75
APVD [illegible] DATE 12/9/75

NEXT HIGHER ASSY: B-DD-KB11-B
SCALE —
SHEET 10 OF 15

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS 01754

TITLE: KB11-C FLOW DIAGRAMS (FLOWS 9)

SIZE D | CODE FD | NUMBER KB11-C-1 | REV

DIST

KB11-C-1

REVISIONS: REV | CHANGE NO | CHK

DEC FORM NO 1060 B
DEC MS-0

DIGITAL EQUIP. CORP.

DVC.00

DVC.00 (125)
DIVIDE COMPLEMENTS MAGNITUDE REMAINDER INTO QUOTIENT MAY BE MODIFIED LATER
t1 <BA→DR>
t2 SHFR←BR
t3 GREG SF,13→SHFR

BRNG (216)

DR0(1) * SR15(0)
DVC.20 (256)
LAST DIVISION WENT, MAGNITUDE OF REMAINDER CORRECT; DO ONE'S COMPLEMENT IN CASE DIVIDEND STARTED NEG.
t1 <BA→DR>
t2 SHFR←-BR
t3 BA←SHFR

BRNG (256)

-N

DVC.70 (256)
DIVIDEND STARTED POS. DON'T CHANGE REMAINDER INSERT 1 STORE QUOTIENT IN [SF] RECORD IT'S COND. CODES
t1 <BR→DR>
t2 SHFR←DR
t3 BRO STROBE
t4 GREG SF,14→SHFR
t5 CCL 04
SKIP NOT SHFR; V/C←0]

(166)

RET.00 1

N

DVC.50 (270)
DIVIDEND STARTED NEG. FIND TWO'S COMPLEMENT OF REMAINDER & WRITE IT AWAY
t1 <BA→DR>
t2 SHFR←BR+1
t3 GREG SF,14→SHFR

(361)

DR0(0) * SR15(0)
DVC.30 (216)
LAST DIVISION DIDN'T GO CORRECT OTHERWISE BY ADDING DIVISOR & WRITE IT AWAY
t1 <BA→DR>
t2 SHFR←BR+SR
t3 GREG SF,13→SHFR
t4 BR←SHFR

(256)

DR0(1) * SR15(1)
DVC.40 (236)
LAST DIVISION DIDN'T GO AND ABSOLUTE VALUE OF MAG. DIVISOR TO BE ADDED & WRITE IT AWAY
t1 <BA→DR>
t2 SHFR←BA-SR
t3 GREG SF,13→SHFR
t4 BR←SHFR

(276)

DR0(1) * SR15(1)
DVC.40 (276)
LAST DIVISION WENT BUT DIVISOR IS NEG.; MAGNITUDE OF REMAINDER CORRECT; DO ONE COMPLEMENT IN CASE DIVIDEND STARTED NEG.
t1 <BA→DR>
t2 SHFR←-BR
t3 BA←SHFR

BRNG (351)

-N

DVC.80 (351)
DIVIDEND AND DIVISOR HAD DIFFERENT SIGNS; FIND ONE'S COMPLEMENT OF QUOTIENT
t1 <BA→DR>
t2 SHFR←-DR
t3 DR←SHFR
SR←GREG SF]
CCL04
[INT NOT SHFR; V/C←0]

(286)

DVC.90 (286)
FORM TWO'S COMPLEMENT OF QUOTIENT & WRITE IT AWAY; RECORD IT'S COND. CODES
t1 <BA→DR>
t2 SHFR←DR+1
t3 BRO STROBE
t4 GREG SF]←SHFR
t5 CCL04
[INT NOT SHFR; V/C←0]

BRNG (144)

-N

DVC.00 (144)
TEST FOR QUOTIENT BEING THE MOST NEGATIVE NUMBER
t1 <BA→DR>
t2 <SHFR←SR>

BRNG (358)

-N

DVD.12 (358)
QUOTIENT CAME OUT TO BE POSITIVE AFTER TWO'S COMPLEMENT; SET V BIT TO INDICATE OVERFLOW
t1 <BA→DR>
t2 <SHFR←SR>
t3 CCL05

(195)

DVC.00 9

N

RET.00 1

(166)

N

DVC.60 (371)
DIVIDEND STARTED NEG. FIND TWO'S COMPLEMENT OF REMAINDER & WRITE IT AWAY
t1 <BA→DR>
t2 SHFR←BR+1
t3 GREG SF,14→SHFR

(378)

DVC.70

RET.00 1

(378)

DIVIDE

FIRST USED ON OPTION/MODEL	QTY	DESCRIPTION	PART NO.	ITEM NO.
11/70		PARTS LIST		

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES TOLERANCES
DECIMALS: XXX ± .005, XX ± .02, X ± .1 — ANGLES: ±0° 30'
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓
MATERIAL —
FINISH —

DRN. [redacted] DATE 7-71
CHK'D [redacted] DATE 7-71
ENG. [redacted] DATE 10-71
PROJ. [redacted] DATE 11-71
APPD. [redacted] DATE 11/15/71

NEXT HIGHER ASSY. B-DD-KB11-B
SCALE —
SHEET 11 OF 15

[redacted] EQUIPMENT CORPORATION
MAYNARD MASSACHUSETTS

TITLE KB11-C
FLOW DIAGRAMS (FLOWS 10)

SIZE D | CODE FD | NUMBER KB11-C-1 | REV.
DIST

REV	DESCRIPTION	CHANGE NO
	REVISIONS	

KB11-C

B-FORK

P/CLASS←-C(ASRB+RORB)←DR0(1)+NEG.BJ

NEG. B (067)
NEG.00 — COMPLEMENT DST OPERAND
t1 <BA←DR>
t2 SHFR←$ALU(A=BR, B=1)
t4 BR←SHFR
(271)

NEG. 1@ (271)
AND THEN INCREMENT, SET CC'S, SEE IF DST IS ODD BYTE
t1 <BA←DR>
t2 SHFR←BA+1
t4 CCLD $
BA←SHFR
BEN@S (123)

DRQ(1)

DR@(@)
NEG.2@ (163)
EVEN BYTE OR WORD-OUTPUT RESULTS; CHECK STACK LIMIT
t1 BA←DR; BC←BSOP2
t2 <SHFR←BR>
t3 BUST; GO CDF]
(132)

CASRB+RORB]←DR@(1) (064)
SHR.00 — SHIFT OR ROTATE RIGHT ODD BYTE; SET CC'S
t1 <BA←DR>
t2 SHFR←$ALU(A=BR, B=1)
t4 CCLD $
BR←SHFR
(123)

SHR.1@ (122)
ODD BYTE-HI. ORDER BYTE POSITIONED & OUTPUT CHECK STACK LIMIT
t1 BA←DR; BC←BSOP2
t2 SHFR←SWAP(BR)
t3 BUST; GO CDF]
t4 BR←SHFR
(132)

EXEC. (132)
EXEC.00 — DO THE OPERATION; START BUS OPERATION
t1 BA←DR; BC←BSOP2
t2 SHFR←$ALU(A=BR, B=SR)
t3 BUST; GO CD7]
t4 CCLD $
BR←SHFR
(132)

EXEC.1@ (132)
FINISH BUS OPERATION
t1 BA←DR; BC←BSOP2
t2 <SHFR←BR>
t3 BRQ STROBE
t4 BUS PAUSE
(217)

FET.00 /1

TST. (033)
TST.00 — NO MORE BUS OPS: SET CC'S & START FETCH NEXT INSTR
t1 BA←PCB; BC←DATI
t2 SHFR←$ALU(A=BR, B=SR)
t3 BUST; GO CDF]
t4 CCLD $
BENIE (246)

-BRQ → FET.1@ /1 (064)

BRQ → BRK.96 /2 (246)

JMP (035)
JMP.00 — LOAD NEW PC FROM DST ADRS
t1 <BA←DR>
t2 <SHFR←PCB>
t3 BEND
BRQ STROBE
t4 PCA←DR
t5 PCB←PCA
(217)

FET.00 /1

JSR (034)
JSR.00 — SAVE DST ADRS IN PC(GET MODIFIED SRC FIELD REG TO SR
t1 <BA←DR>
t2 SHFR←PCB
t3 BEND
t5 PCA←DR
t6 -SFT: SR←GS C5F]
SET: SR←SHFR
(201)

JSR.1@ (201)
GET SP AND PUT SRC FIELD REG IN BA FOR PUSHING OLD CONTENTS ON STACK
t1 <BA←PCB>
t2 SHFR←SR
t3 BRQ STROBE
t4 DR←GD C6]
BA←SHFR
(274)

JSR.2@ (274)
STEP SP BACK FOR PUSH
t1 <BA←DR>
t2 SHFR←DR-2
t5 GR C6]←SHFR
t6 DR←SHFR
(275)

JSR.3@ (275)
WRITE OLD SRC FIELD REG ON STACK, CHECK STACK LIMIT
t1 BA←DR; BC←DATO
t2 <SHFR←BR>
t3 BUST; STACK REF
(@32)

JSR.4@ (@32)
FINISH PUSH; OLD PC GOES TO SRC FIELD REG AND DST ADRS TO PC
t1 BA←DR; BC←DATO
t2 SHFR←PCB
t4 BUS PAUSE
t3 BRQ STROBE
t5 GR C5F]←SHFR
t6 PCB←PCA
(217)

FET.00 /1

MFP (066)
MFP.00 — PREVIOUS MODE DATA IN BA; GET CURRENT MODE SP; SET CC'S.
t1 <BA←DR>
t2 SHFR←BR
t4 CCLD $
SR←GS C6]
(203)

MFP.1@ (256)
STEP STACK POINTER BACK FOR PUSH
t1 <BA←DR>
t2 SHFR←SR-2
t3 BEND
t5 GR C6]←SHFR
t6 DR←SHFR
(228)

SYC.00 /3

MFP.00

MFP. (046)
MFP.80 — PREVIOUS MODE DATA IN GR'S; IF R6 USE PREV MODE SP; R@-R5 SET DETERMINED BY REG. SET BIT (PS11)
t1 <BA←PCB>
t2 SHFR←PCB
t3 BEND
t5 -I/CLASS: GR C0F]←SHFR
t6 -DF7: DR←GD C0F]
DF7: DR←SHFR
(304)

MFP.9@ (304)
PUT DATA IN BR & SET CC'S; GET CURRENT MODE SP
t1 <BA←DR>
t2 SHFR←DR
t4 CCLD $
BR←SHFR
SR←GS C6]
(250)

EXECUTE-MEM REF

FIRST USED ON OPTION/MODEL	QTY	DESCRIPTION	PART NO.	ITEM NO.
11/70		PARTS LIST		

DIMENSIONAL TOLERANCE
DIMENSIONS ARE MILLIMETERS / INCHES UNLESS OTHERWISE SPECIFIED
MILLIMETERS: X.XX ±0.10; X.X ±0.5; X ±2%
INCHES: .XXX ±.005; .XX ±.02; .X ±.1; AA 32
THIRD ANGLE PROJECTION
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓
MATERIAL —
FINISH —

DRN. — DATE 12-9-75
CHK'D — DATE 12/9/75
ENG — DATE 12-9-75
PROJ. ENG. — DATE 12-9-75
PROJ — DATE 12/10/75
NEXT HIGHER ASSY. B-DD-KB11-B
SCALE NONE
SHEET 12 OF 15

digital

TITLE KB11-C FLOW DIAGRAMS (FLOWS 11)

SIZE D | CODE FD | NUMBER KB11-C-1 | REV.
DIST

REVISIONS: REV. | CHANGE NO. | DWG

DFD KB11-C-1

ZAR.00 (200)
ABORTED OPERATION OR ARRIVE ON SEQUENCE
c1 <BA←PCB>
c2 <SNFR←DR>
c3 BEND
BRQ STROBE

BRK.98 (352)
BRQ TO BE SERVICED; END LAST OPERATION
c1 <BA←PCB>
c2 <SNFR←DR>
c3 BEND
(352)

RSD.BB (300)
RSD.B1 (317)
RSD.B2 (303)
DR GETS VECTOR ADDR; PS TO BR
c1 <BA←PCB>
c2 SNFR←TV
c3 BEND
c4 DR←SNFR
BR←PS
(305)
RSD.B8 (315)
LEFT SHIFT VECTOR ADDR TO CORRECT ADDR; STORE IN DR
c1 <BA←DR>
c2 SNFR←SHL(DR)
c4 DR←SNFR
(354)

TRP.BB (313)
TRP.B1 (314)
TRP.B2 (124)
VECTOR ADRS IN DR; PS IN BR
c1 <BA←PCB>
c2 SNFR←TV
c3 BEND
c4 DR←SNFR
BR←PS
(354)
TRP.B8 (354)
PCA GETS OLD PS; FETCH NEW PC FROM VECTOR
c1 BA←DR; BC←KERN DATI
c2 <SNFR←BR>
c4 BUST; GR[6]
c5 PCA←BR
(355)
SVC.BB 18

PS RESTORE
ZAR.10 (376)
ABORT CAME FROM SERVICE ROUTINE; FIX UP PC & PS; PCB GETS OLD PS; DR HAS ABORTED ADDR
c1 <BA←DR>
c2 <SNFR←PCB>
c4 PCB←PCA
(315)
ZAR.20 (315)
RESTORE OLD PC; BR GETS OLD PS
c1 <BA←DR>
c2 SNFR←PCB
c3 PCA←SR
c4 BR←SNFR
PCB←PCA
(362)
(362)
ZAR.30
RESTORE OLD PS
c1 <BA←DR>
c2 <SNFR←PCB>
c5 PS←BR
(352)
BRK.BB 18

BEN06 (358)
-PS RESTORE
BRK.BB
BRK.01 (358)
WAIT FOR INTR. IF BUS REQ ACTIVE; GET VECTOR
c1 <BA←PCB>
c2 SNFR←PCB
c3 INTR PAUSE
c4 BR←BUS
SR←SNFR
BEN12 (136)
-CONF
CONF
CON.BB 18 (176)
BRK.18
BRK.10 (136)
BRK.11 (258)
INTR VECTOR TO DR; SR HOLDS PC
c1 <BA←PCB>
c2 SNFR←BR
c4 DR←SNFR
BEN18 (186)

POWER UP
[PF(1)]
PUP.00 (100)
START VECTOR ADRS TO DR
c1 <BA←PCB>
c2 SNFR←SV
c3 ACKN
c4 DR←SNFR
(356)
(352)
PUP.10 (154)
FETCH NEW PC FROM SV
c1 BA←DR; BC←DATI
c2 <SNFR←SV>
c4 BUST; GR[6]
(154)
(154)
PUP.20
GET NEW PC & STEP TO NEXT WORD OF VECTOR
c1 BA←DR; BC←DATI
c2 SNFR←DR+2
c4 BUS PAUSE
c6 SR←SNFR
BR←BUS
(340)

PUP.30 (340)
FETCH NEW PS; PC IN BR GOES TO PCB
c1 BA←SR; BC←DATI
c2 <SNFR←BR>
c3 BUST; GR[6]
c5 PCA←BR
c4 PCB←PCA
(341)
PUP.40 (341)
GET NEW PS FROM SV+2
c1 BA←SR; BC←DATI
c2 <SNFR←PCB>
c4 BUS PAUSE
c6 BR←BUS
(815)
RTI.BB 2

INTERNAL TRAPS EXCEPT RED STACK ERRORS
[PF(0)&TF#-SF]
BRK.BB
BRK.00 (148)
GET TRAP VECTOR ADRS TO DR & PROCESSOR STATUS (PS) TO BR
c1 <BA←PCB>
c2 SNFR←TV
c4 BR←PS
DR←SNFR
(158)

INTERRUPTS, PASSIVE RELEASE/CONSOLE CONTINUE
[PF(0)&-TF&-SF]
BRK.80 (158)
GET PROCESSOR STATUS TO BR; DR HAS INTERRUPT VECTOR
c1 <BA←PCB>
c2 <SNFR←DR>
c3 ACKN
c4 BR←PS
BEN02 (152)
(PWRF+INTRF)
-(PWRF+INTRF)
BRK.30 (158)
FETCH NEW PC FROM VECTOR; PCA GETS OLD PS; ADDR MAPPED TO KERNEL SPACE
c1 BA←DR; BC←KERN DATI
c2 <SNFR←BR>
c3 BUST; GR[6]
ACKN
c5 PCA←BR
(355)
SVC.80 13
RTI.BB 2 (178)

RED STACK ERRORS
[PF(0)&SF]
SER.00 (168)
EMERGENCY STACK LOCS & R6 WILL HAVE OLD PC & OLD PS AFTER SERVICE
c1 <BA←PCB>
c2 SNFR←2
c4 SR←SNFR
(344)
SER.10 (344)
STACK POINTER SET TO 4 FOR EMERGENCY STACK PUSHES
c1 <BA←PCB>
c2 SNFR←SR+2
c4 GR[6]←SNFR
(168)
BRK.BB 15

BREAK CONDITIONS

FIRST USED ON OPTION/MODEL	QTY	DESCRIPTION	PART NO.	ITEM NO.
11/70		PARTS LIST		

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES TOLERANCES
DECIMALS XXX = .005 XX = .02 X = .1 ANGLES ±0° 30
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓
MATERIAL
FINISH

		DATE
DRN		
CHK	T. Cook	12-9-75
ENG	Milton A. Bruno	12-9-75
PROJ. ENGR	Milton A. Bruno	12-9-75
PROG	Lee Taylor	12/9/75

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE KB11-C
FLOW DIAGRAMS
(FLOWS 12)

NEXT HIGHER ASSY. B-DD-KB11-B
SIZE D CODE FD NUMBER KB11-C-1 REV
SCALE
SHEET 13 OF 15 DIST

REVISIONS | REV | CHK | CHANGE NO

DEC FORM NO DRD 100-B

KB11-C-1 REV B

SVC.00 (355)
GET NEW PC TO BR; STEP DR FOR VECTOR +2 FETCH; PCB HAS OLD PS
c, BA←DR; BC←KERN DATA
c, SHFR←DATA
c, BUS PAUSE
c, BR←BUS DR←SHFR

(365) (365)
SVC.10
FETCH NEW PS FROM VECTOR +2; ADDR MAPPED TO KERNEL SPACE; SP GETS OLD PC; PCB GETS OLD PS
c, BA←DR; BC←KERN DATA
c, SHFR←PCB
c, BUST; GRC03
c, SP←SHFR PCB←PCB

(367) (367)
SVC.20
GET NEW PS TO BR; DR GETS OLD PS; PCA, PCB GET NEW PC
c, BA←DR; BC←KERN DATA
c, SHFR←PCB
c, BUS PAUSE
c, PCA←BR
c, BR←BUS DR←SHFR PCB←PCA

(368) (368)
SVC.30
PS GETS NEW PS; LOAD PREV MODE FROM CURRENT MODE; PCA & BR GET OLD PS; SP HAS OLD PC
c, <BA←DR>; BC←KERN DATA
c, SHFR←DR
c, PS←BR; GRC03
c, PCA←DR
c, BR←SHFR

(371) (371)
SVC.40
DR GETS NEW CURRENT MODE STACK POINTER; PCB HAS NEW PC; BR HAS OLD PS
c, <BA←DR>
c, (SHFR←PC-2)
c, DR←GD[0]

(377) (377)
SVC.50
STEP SP FOR PUSH; DR GETS SP-2; BR HAS OLD PS
c, <BA←DR>
c, SHFR←DR-2
c, GRC03←SHFR
c, DR←SHFR

(385) (385)
SVC.60
PUSH OLD PS ONTO CURRENT MODE STACK; CHECK FOR STACK LIMIT; STEP SP FOR NEXT PUSH
c, BA←DR; BC←DATO
c, SHFR←DR-2
c, BUST
c, GRC03←SHFR

(BW)
SVC.70 13

SVC.70
SVC.70 (364)
FINISH PUSH; BR GETS OLD PC; DR GETS SP
c, BA←DR; PC←DATO
c, SHFR←SP
c, BUS PAUSE
c, DR←GD[C]
BR←SHFR

(388) (388)
SVC.80
SVC.80 (822)
DO PUSH ONTO STACK; CHECK FOR STACK LIMIT; IF INTR OR TRAP SERVICE: BR HAS OLD PC; PCB HAS NEW PC
c, BA←DR; BC←DATO
c, <SHFR←PCB>
c, BUST; GRC03

(390) (390)
SVC.90
SVC.90 (368)
FINISH PUSH; STROBE BREAK REQUESTS
c, BA←DR; BC←DATO
c, <SHFR←BR>
c, GBD STROBE
c, BUS PAUSE

(BW)
FSV.00
1

FSV.00
FSV.00 (327)
WAIT FOR FP OR INTERRUPT
<BA←PCB>
<SHFR←DR>
BRQ STROBE

-(SYNC+BRQ) BEN:? (327) BRQ

FSV.20
SYNC+BRQ
FSV.20 (367)
START BUSOP
BA←DR BC←FC
FP READ DATA
BUST; GD C03
BR←BUS

BEN:0 (348)

FPCLASS

FSV.30 (348)
DO BUSOP AND ENTER WAIT LOOP
BA←DR BC←PC
BUS PAUSE
FP ATTN
BR←BUS

(225)
FSV.40 (226)
WAIT FOR FPU TO MODIFY DATA
<BA←SCRMX>
<SHFR←BR>

BEN:0 (225)
-SYNC
FSV.50 (265)
START NEXT CYCLE
BA←DR BC←FC
FP READ DATA
BUST GD C03
BR←BUS

(368)

~FPCLASS

FSV.12 (302)
FINISH BUSOP ENABLE FP ATTN
BA←DR
BC←FC
SHFR←DR+2
BUS PAUSE
FP ATTN
BR←BUS
DR←SHFR

BEN:? (367); FP REQ

-FP REQ
FSV.20 (367)
GET FPCS IF NEEDED
READ FPS
BRQ STROBE
BR←BUS

(237)
FET.27 (237)
START NEXT FETCH
BA←PCB BC←DATI
SHFR←SP-SR
BUST; CLR FLAGS
IR←SHFR
CC←FCC IF ENABLE

BEN:2 (242)
BRQ
BRK.91 (240)
-BRQ
FET.10 (266)

BRQ
FSV.70 (367)
READ BACK OLD GR
READ FDR
<BA←PCB>
BR←BUS

(150)
FSV.80 (150)
READ BACK OLD PC
READ FPA
GRC0?←SHFR
SHFR←BR
BR←BUS

(245)
FSV.90 (245)
RESTORE PCB
PCA←BR
PCB←PCA
<SHFR←BR>

(352)
BRK.00 (352)

SERVICE SEQUENCE

FIRST USED ON OPTION/MODEL	QTY	DESCRIPTION	PART NO.	ITEM NO.
11/70		PARTS LIST		

UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS .XXX ± .005, .XX ± .02, .X ± .1
ANGLES ± 10' 30"
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓
MATERIAL
FINISH

	NAME	DATE
DRN		1-70
CHK		1-70
ENG		2-4-75
ASSEMBLY		2-4-75
PROJ		7/71

NEXT HIGHER ASSY B-DD-KB11-B

DIGITAL EQUIPMENT CORPORATION

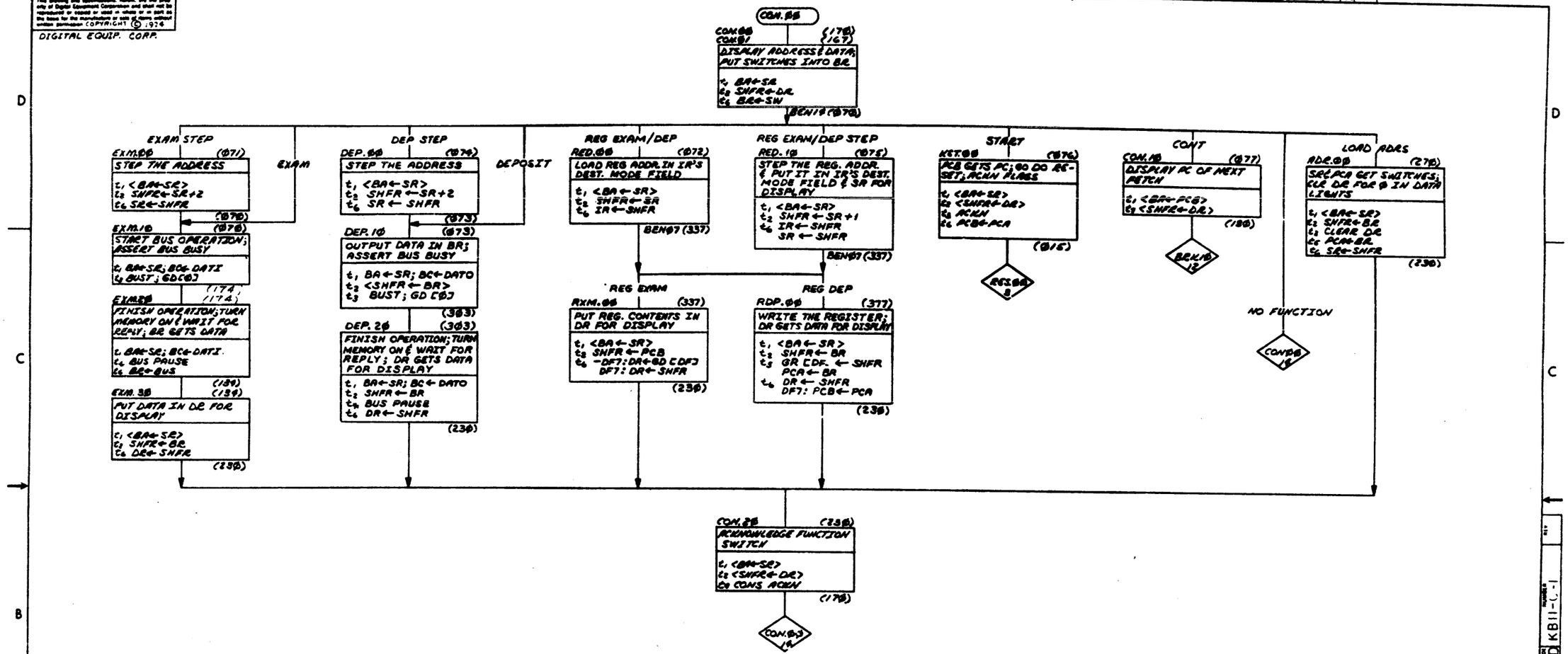
TITLE KB11-C
FLOW DIAGRAMS
(FLOWS 13)

SIZE D CODE FD NUMBER KB11-C-1 REV.
SCALE
SHEET 14 OF 15

REVISIONS	REV	CHANGE NO	CHK

DEC 1 0RIG NO
FSD 103-B

KB11-C-1
FD



CONSOLE

FIRST USED ON OPTION/MODEL	QTY	DESCRIPTION	PART NO.	ITEM NO.
11/70		PARTS LIST		

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES TOLERANCES
DECIMALS: XXX ± .005, XX ± .02, X ± .1 — ANGLES: ±0° 30
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓
MATERIAL —
FINISH —

		DATE
DRN.		9-75
CHK.		12/6/75
ENG.		12-9-75
PROJ. MGR.		12-9-75
PROD.		12/9/75

NEXT HIGHER ASSY: B DD-KB11-B
SCALE —
SHEET 15 OF 15

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

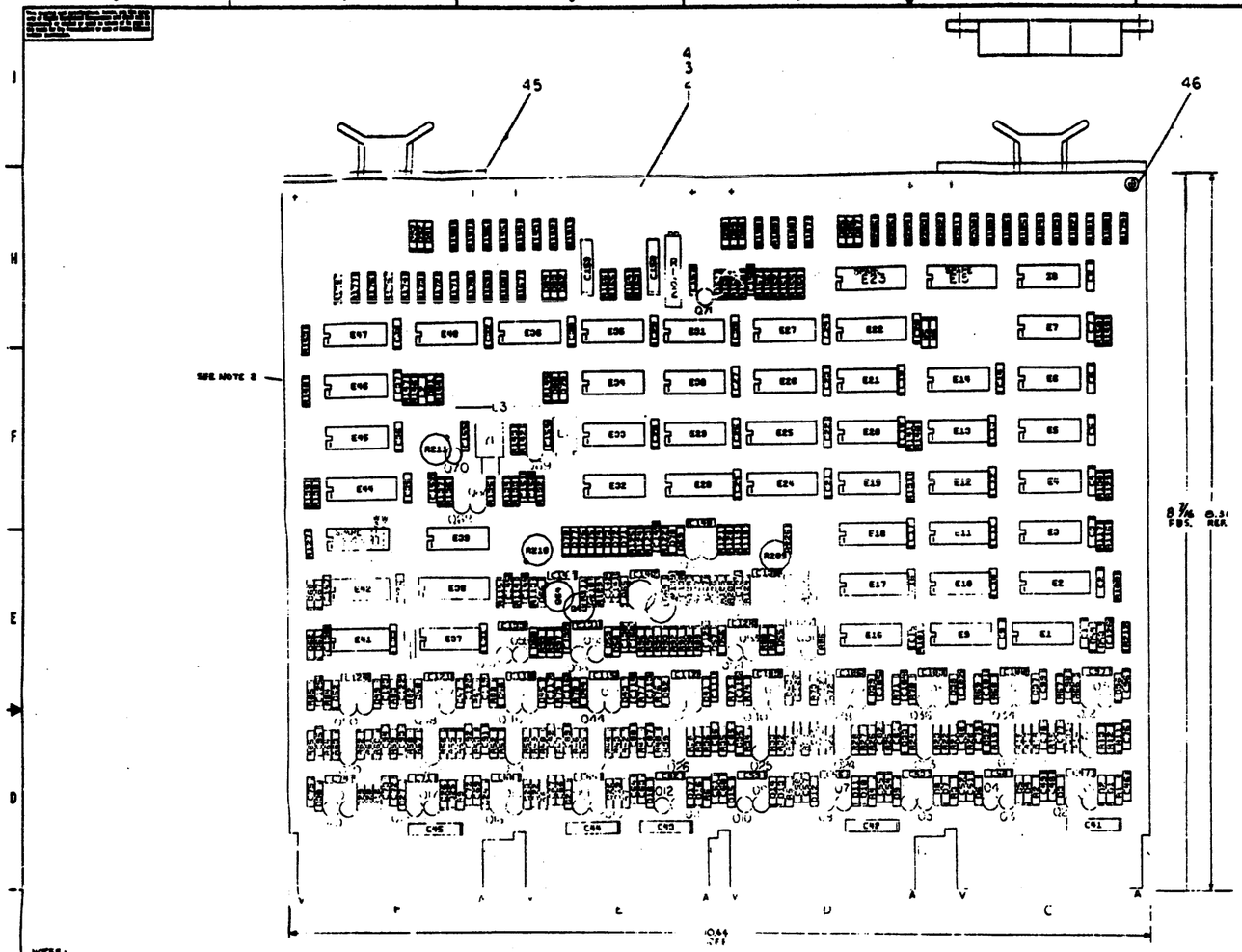
TITLE: KB11-C FLOW DIAGRAMS (FLOWS 14)

SIZE	CODE	NUMBER	REV
D	FD	KB11-C-1	

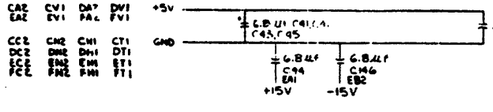
DIST

DRAWING 40-533 19640 — REVISIONS: REV | CHANGE NO | CHK
DEC FORM NO DRD 103-B

SECTION V
KB11-D TIMING LOGIC



NOTES:
1. UNLESS OTHERWISE NOTED: RESISTANCE IS IN Ω, CAPACITANCE IS IN PICOFARADS. CMPS WITHOUT VALUE NOTED ARE .22 MFD 50V. DIODES ARE TYPE FD777 & ALL NPN TRANSISTORS ARE DEC 3009 B# PNP TRANSISTORS ARE DEC 2.58.
2. BOND L1 TO ETCHED BOARD



QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM NO
2	R209, R210	POT. 2K V2 W	19-09150-07	51
1	R211	POT. 100 1/2 W	19-09150-05	50
1	R186	RES. 120 1/4 W 5%	19-00247	49
1	R212	RES 33 1/4 W 5%	1500197-00	48
2	W8, W8	JUMPER UNINSULATED	9009185	47
6		EYELET #664-7	9006732	46
4		HANDLE FLIP-CHIP MAGENTA	1008337-06	45
1	Y1	CRYSTAL 33.333 MHZ	1810694-1	44
1	L2	INDUCTOR .47uh NYTRONICS WEE-WEE -047	1610999	43
1	L1	INDUCTOR .22 uh VARIABLE NYTRONICS WEE VL .22	1611000	42
1	L3	INDUCTOR RFCS 33 uh	1601759	41

QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM NO
35	Q1, Q3, Q5, Q7, Q9, Q11, Q13, Q15, Q17, Q19, Q21, *MPU Q23, Q25 THRU Q40, Q51, Q54, Q56, Q58, Q60, Q63, Q65, Q66, Q69, Q70	TRANSISTOR DEC 42.58	1508321	40
36	Q2, Q4, Q6, Q8, Q10, Q12, Q14, Q16, Q18, Q20, Q26 THRU Q50, Q52, Q53, Q57, Q60, Q61, Q62, Q64, Q67, Q68, Q71, Q55	TRANSISTOR DEC 3009 B	1503100	39
1	E38	IC DEC 74S140	1910546	38
8	E12, E17, E18, E22, E24, E25, E28, E46	IC. DEC 74S112	1910545	37
8	E5, E6, E19, E20, E23, E26, E27	IC. DEC 74S74	1910544	36
4	E11, E12, E13, E20	IC DEC 74S69	1910543	35
1	E32	IC DEC 74S64	1910542	34
4	E1, E9, E14, E16, E37, E41	IC. DEC 74	1910541	33
2	E40, E44	IC DEC	1910539	32
3	E3, E36, E47	IC DEC 74S11	1910537	31
5	E4, E7, E21, E30, E45	I.C DEC 74S04	1910536	30
4	E10, E31, E34, E42	IC. DEC 74S00	1910532	29
1	R162	POT 1K 3MW K&R	1409145-07	28
9	R117, R130, R154, R140, R147, R150, R151, R143, R166	RES 680 1/4W 5%	1301424	27
1	R142	RES 750 1/4W 5%	1301401	26
13	R66, R68, R70, R72, R74, R76, R78, R80, R82, R84 R118, R119, R120	RES. 1.2K 1/4W 5%	1301320	25
26	R54, R55, R56, R57, R58, R28, R30, R43, R45, R38, R41, R44, R47, R50, R53 R54, R55, R56, R57, R58, R60, R64 R118, R119, R132, R148	RES. 10 1/4W 5%	1301311	24
5	R61, R71, R72, R21, R32	RES. 15K 1/4 5%	1300496	23
17	R5, R8, R10, R40, R46, R52 R58, R64, R67, R69, R71 R73, R75, R101, R113	RES. 4.7K 1/4 5%	1300447	22
12	R1, R10, R11, R22, R79, R81, R83, R105, R86, R103	RES. 3K 1/4 5%	1300456	21
6	R12, R24, R27, R60, R31, R143	RES. 1.5K 1/4 5%	1300391	20
76	R36, R37, R42, R43, R48, R49, R54, R55, R60, R61, R87 THRU R94, R95 THRU R102, R122, R123, R124, R125, R104, R105, R138, R139, R148, R149, R167 THRU R209	RES. 1K 1/4 5%	1300365	19
12	R2, R20, R44, R46, R48, R49, R54, R55, R60, R61, R87 THRU R94, R95 THRU R102, R122, R123, R124, R125, R104, R105, R138, R139, R148, R149, R167 THRU R209	RES. 330 1/4W 5%	1300295	18
1	R146	RES. 220 1/4W 5%	1300271	17
8	R9, R14, R17, R31, R42, R45, R65, R67	RES. 150 1/4W 5%	1300250	16
11	R3, R4, R13, R24, R27, R34, R39, R45, R51, R57, R63, R121	RES. 100 1/4W 5%	1300229	15
2	R133, R137	RES. 68 1/4W 5%	1300219	14
7	R97, R88, R97, R134, R135, R144, R98	RES. 47 1/4W 5%	1300202	13
52	D1, D3, D4, D7, D9, D10, D12, D13, D14, D16, D18, D19, D21, D22, D24, D25, D27, D28, D30, D31 THRU D56, D63, D64, D57, D58, D61, D62, D64, D65, D67, D68, D67, D71	DIODE FD777	1103041	12
39	D2, D5, D8, D11, D14, D17, D20, D23, D26, D29, D32, D35, D39, D60, D63, D66, D72 THRU D113	DIODE D662	1100113	11
96	C41 THRU C43, C49, C60, C62, C104, C105, C106, C108, C109, C111, C115, C117, C118, C120, C121, C123, C124, C126, C127 THRU C149, C151, C152	CAP .22 MF 50V MONO.	1010274-1	10
8	C41 THRU C45, C144, C58, C59	CAP 6.8 MF 35V 10% S.TANT	1008306	9
42	C1 THRU C39, C150 C155, C156,	CAP .01 MF 100V 80% DISC	1001610	8
1	C154	CAP 100 PF 100V 5% DM.	1000816	7
1	C157	CAP 47 PF 100V 5% DM	1000711	6
10	C98, C101, C104, C107, C110, C113, C116, C119, C122, C125	CAP 33PF 100V 5% DM	1000609	5
1		ETCHED CIRCUIT BOARD	5009799	4
REF		MODULE ECO HISTORY	B-MN-M8109-06	3
REF		ASSY/DRILL HOLE LAYOUT	D-AA-M8109-0-0	2
1		X-Y COORDINATE HOLE LOCATION	X-CO-M8109-0-0	1

PARTS LIST

DEC 745112	0	15
IC TYPE	GND	+5V

IC PIN LOCATIONS

JUMPER	AWG	FEET	TO PT
W8	30	1	

JUMPER LIST

ETCH BOARD REV F

DEC 4158	NONE
DEC 3009 B	2N3646
DEC FD777	1103041
DEC 662	1N649

DEC NO.	EIA NO.

SEMICONDUCTOR CONVERSION CHART

DIGITAL EQUIPMENT CORPORATION

TIMING GENERATOR

B-DD-KB11-D

M8109-0-0 T

+3VE
+5V
R152 330
R151
74S04 E21
+3VA
+3VE
+3VC
74S74 E27
TIGC TPBL
TIGC TI (1) L
SMCA MEM SYNC (B) L
CJ2
W9
W8
CU1
TIGA MEM SYNC H
TIGA STOP TI L
TIGA T1 MAT H
TIGA T2 MAT H
TIGA T3 MAT H
TIGA T4 MAT H
TIGA T5 MAT H
TIG TPH MAT H
PHKA STOP TI L
CT2
R149 330
R150 681
74S04 E7
TIGA T4 (0) H
TIGA T5 (0) H
74S40 E13
+3VE
+3VF
+3VA
+3VC
+3VF
CBZ
R140 1K
R138 1K
R135 1K
R161 1K
R159 1K
TMKA SEL SYS 1 L
CC1
+5V
TIGA UBSD@ H
74S11 E3
TMCC ABORT H
CA1
74S04 E7
TIGA UBSD@@ H
TIGA UBSD@1 H
T1 SYNC 74S19 E27
TIGC TPB L
TIGA TI (1) L
TIGA ROM INITA L
TIGC TPB H
TIGC TPB L
T1 74S74 E19
T1A 74S74 E19
T2 74S112 E18
T2A 74S112 E17
S0 74S112 E44
S1 74S112 E44
T3 74S112 E17
T4 74S112 E24
T5 74S112 E29
T5A 74S112 E24
TIGA T5 (1) L
TIGA TI SYNC (1) H
R137 150Ω
TIGA TI (1) L
TIGA T4 (1) H
74S04 E45
TIGA T5 (Ø) H
TIGA T2 (Ø) H
TIGA T1A (Ø) H
74S11 E34
TIGA ROM INITA L
INIT SYNC 74S74 E26
TIGC TPB L
+3VK
UBCA PAUSE H
CK1
UNI DLY 74S74 E56
TMCF FAST L
CB1
+3VM
+3VM
R154 150
CONT 74S74 E9
TIGA CONT H
TIGA ROM INIT B L
+3VF
74S04 E21
74S112 E22
+3VM
TIGB CONT L
TIGA TI (1) B L
T2 (B) H
TIGA CONT (1) L
TMCF FAST L
TIGA ROM40 W
74S40 E12
RACB EXT WRB H
RACB UBSD@@ H
TIGA UBSD@1 L
R116 300
R117 680
+5V
TIGA UBSD@@ H
TIGA SNG CY (1) H
TIGA TI (1) H
+3VF
74S65 E20
TIGA STOP TI L
R141 330
R140 68Ø
+5V
UBCE ROM INIT H
EJ1
74S40 E14
TIGA ROM INITB L
74S40 E14
TIGA ROM INITA L
74S20 E10
TIGA TI (1) B L
+3VD
74S04 E21
TIGA TI (1) H
74S04 E7
+3VM
74S04 E7
+3VN
TIGB ROM+ UPB (1) H
TIGC TPB H
R136 150
+3VN
TIGC TPB L
+3VN
74S74 E5
+3VM
UBCA SSYN RESTART H
CQ1
74S74 E6
CK2
UBCA INTR RESTART H
R131 150
+5V
PHKA STOP T3 L
DH2
R130 330
R129 680
+5V
74S04 E4
+3VN
TIGA TI (1) H
TIGC TPB H
TIGA CONT H
74S86 E2
R126 150
+3VN
TIGA T2A (1) H
TIGA CONT (1) L
RACB DIS BUST L
SS-B ENABLE T3 DLY H
74S65 E11
TIGA STOP T3 L
+3VA
TIGA TI (1) H
TIGC TPB H
S1-B DLY 74S40 E18
+3VA
R125 W2 W3 W4
TIGA S0 (1) H
TIGA S1 (1) H
+3VN
TIGA S0 (1) H
TIGA S1 (1) H
74S11 E47
TIGB SINGLE CY L
TIGC TPB H
TIGA CONT H
74S112 E25
+3VP
TIGA UBSD@1 L
RACB UBSD@1 H
CJ1
74S04 E4
74S04 E4
TIGA UBSD@1 H
RACB UBSD@@ H
CL1
74S04 E4
74S04 E4
TIGA UBSD@@ H
CM1
RAL S ROM40 BL
74S04 E4
TIGA ROM 40 H

TIMING GENERATOR CONTROL — SLOT 15

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
11/45		PARTS LIST		

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES
DECIMALS .XXX ± .005 .XX ± .02 .X ± .1 ANGLES ±0°30'
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓
MATERIAL
FINISH

Dsgn [redacted] DATE 4/25/71
Chkd DATE 4/26/71
Engr DATE 4/27/71
Mfg DATE 4-30-71
Prod DATE 5-11-71
NEXT HIGHER ASSY. B-DD-KB11-Ø
SCALE
SHEET 2 OF 5

EQUIPMENT CORPORATION [redacted] MASSACHUSETTS

TITLE TIMING GENERATOR (TIGA)

SIZE D | CODE | NUMBER CS M8109-Ø-1 | REV. T

REVISIONS: REV | CHANGE NO | LINK

DEC 30HH NO DRD 00-0

MAINDEC-11-DTIGA-B-1

SOURCE SYNCHRONIZER

PHASE SPLITTER/BUFFER

CRYSTAL CLOCK

R/C CLOCK (MAINTENANCE)

MAINT. SWITCHES: REF. TO XMAA BOARD		
S4	SINGLE TIME STEPPER	
S3	Ø = CRYSTAL TIMING SOURCE 1 = RC TIMING SOURCE	
S1	S2	MODE CONTROL
Ø	Ø	NO EFFECT
Ø	1	SINGLE ROM CYCLE
1	Ø	UPB STOP
1	1	SINGLE PULSE (USE SWØ)

TIMING SOURCE CONTROL — SLOT 15

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
11/45		PARTS LIST		

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES
TOLERANCES
DECIMALS .XXX ± .005 .XX ± .02 X ± .1
ANGLES ± 0° 30'
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓
MATERIAL —
FINISH —

DRN. S.W. Roberts DATE 8/28/71
CHKD. E. Hart DATE 9/6/72
ENG. E. Hart DATE 11/6/72
PROJ. ENG. D. Ward DATE 9-20-72
PROD. [illegible] DATE 11-21-72

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE: TIMING GENERATOR (TIGB)

NEXT HIGHER ASSY. B-DD-KB11-Ø

SIZE D | CODE CS | NUMBER M8109-Ø-1 | REV T

SCALE — SHEET 3 OF 5 DIST.

REVISIONS

NOTES:
1. ALL NPN TRANSISTORS ARE DEC 3009B, ALL PNP TRANSISTORS ARE DEC 4258, ALL DIODES ARE TYPE FD 777, ALL CAPACITORS ARE 22MF 20V MONOLYTHIC UNLESS OTHERWISE INDICATED.

T16C TP8 H
T16C TF H
T16C TFR H
T16B CLOCK H
T16C TP8 L
T16C TF L
T16C TFR L
T16B CLOCK L
T16A T1A(1)H
T16A T1A(0)L
T16C T1 H
T16C T1B H
T16C T1R H
T16C T1BR H
T16C T1 L
T16C T1B L
T16C T1R L
T16C T1BR L
T16A T2A(1)H
T16A T2A(0)L
T16C T2 H
T16C T2B H
T16C T2R H
T16C T2BR H
T16C T2 L
T16C T2B L
T16C T2R L
T16C T2BR L

SLOT 15

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
11/45		PARTS LIST		

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES
DECIMALS: .XXX ± .005, .XX ± .02, .X ± .1; ANGLES: ±0° 30'
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓
MATERIAL —
FINISH —

		DATE
DRAWN	R. Davis	2-25-72
ENGR		DATE
ENGR		DATE
ENGR MGR		DATE
QUAL ASSUR		DATE

EQUIPMENT CORPORATION

TITLE: TIMING GENERATOR (TIGC)

NEXT HIGHER ASSY: B-DD-K811-Ø
SCALE —
SHEET 4 OF 6

SIZE/CODE: DCS | NUMBER: M8109-Ø-1 | REV: T
DIST.

REVISIONS		
REV	CHANGE NO	CHK

DEC FORM NO DEV NO-0

M8109-Ø-1

T16B CLOCK H
T16B CLOCK L
T16A T3 (1) H
T16A T3 (1) L
T16A T4 (1) H
T16A T4 (1) L
T16A T8A (1) H
T16A T8A (1) L
T16D T3 H
T16D T3B H
T16D T3E H
T16D T3EB H
T16D T4 H
T16D T4B H
T16D T4E H
T16D T4EB H
T16D T5 H
T16D T5B H
T16D T5E H
T16D T5EB H
T16D T3 L
T16D T3B L
T16D T3E L
T16D T3EB L
T16D T4 L
T16D T4B L
T16D T4E L
T16D T4EB L
T16D T5 L
T16D T5B L
T16D T5E L
T16D T5EB L
-V3A
+V2
-V3B
+V4
-V1A
+V3
+V5
-15V
+15V
+8V
-V1A
C147
D67
D61
+V4
D68
D62
C134
D66
D64
D65
C126
C15E2
C15F2
C15E1
C15F1
C15B2
C15A2
C15B1
C15A1
FI5E2
FI5F2
FI5E1
FI5F1
FI5B2
FI5A2
FI5B1
FI5A1
C15I2
C15H2
C15I1
C15H1
NOTE:
1. ALL NPN TRANSISTORS ARE DEC 3009B, ALL PNP TRANSISTORS ARE DEC 4259, ALL DIODES ARE TYPE FDH77 ALL CAPACITORS ARE .02 MFD MONLYTHIC UNLESS OTHERWISE INDICATED.

SLOT 15

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.
11/45		PARTS LIST	

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES TOLERANCES
DECIMALS .XXX ± .005 .XX ± .02 .X ± .1 ANGLES ±0°30'
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓
MATERIAL
FINISH

DRAWN DATE 4-1-76
CHECKED DATE 4-7-76
ENGR DATE 4-7-76
MFG DATE 4-7-76
QUAL DATE 4-21-76

NEXT HIGHER ASSY. B-DD-KB11-Ø

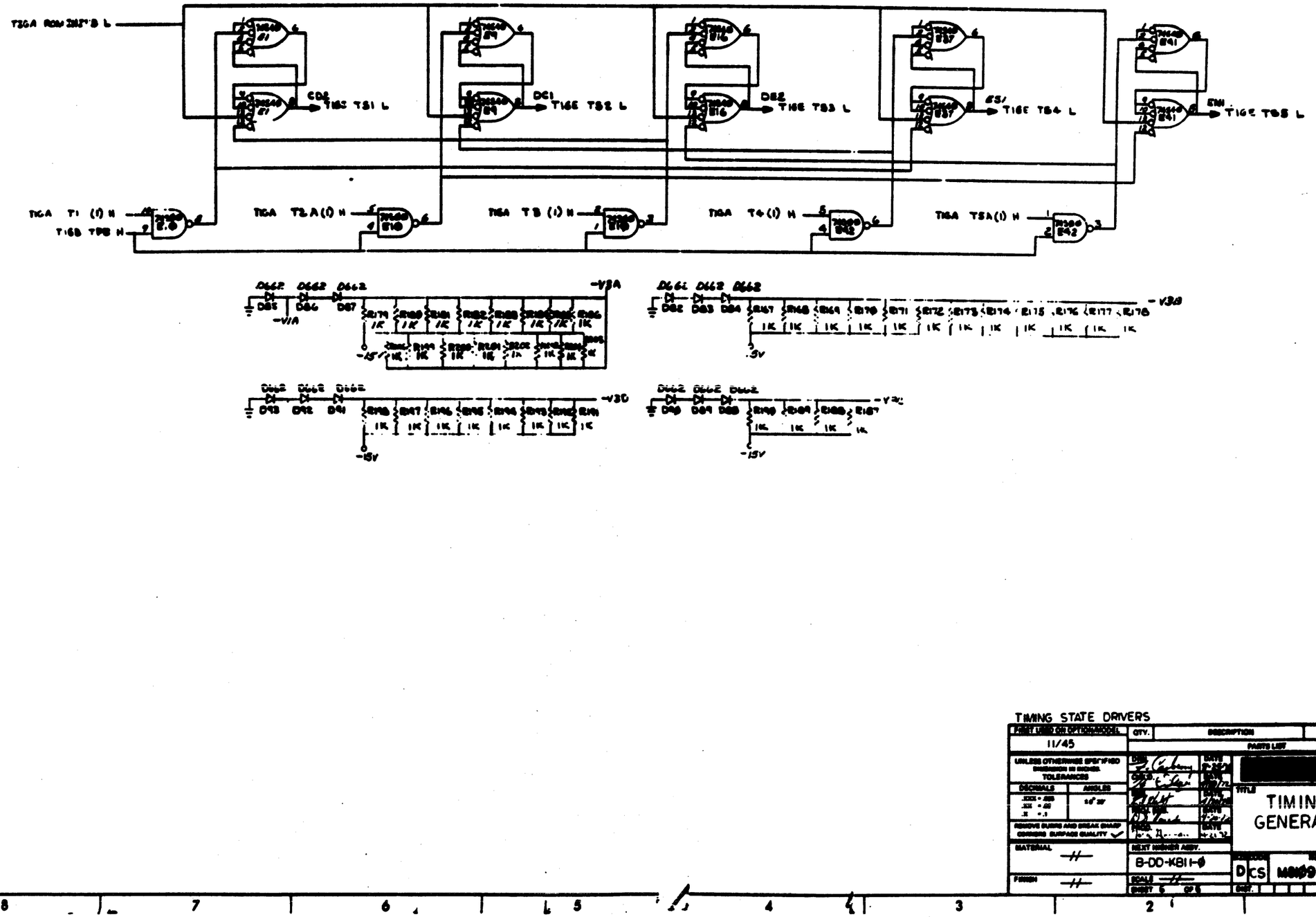
EQUIPMENT CORPORATION

TITLE
TIMING GENERATOR
(T16D)

DRAWING NUMBER DCS M8109-0-1 REV. F

SCALE
SHEET 5 OF 8

REV	CHANGE NO.	ORIG



TIMING STATE DRIVERS

SLOT 15

FIRST USED ON OPTION MODEL	11/45		
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES TOLERANCES	DECIMALS .XXXX ± .0005 .XXX ± .002 .X ± .1	ANGLES ±0° 30'	
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓			
MATERIAL	—		
FINISH	—		

QTY.	DESCRIPTION	PART NO.	REV
PARTS LIST			

DRN		DATE
CHK		
ENGR		
PROJ		
MFG		DATE
NEXT HIGHER ASSY.	8-00-KB11-0	
SCALE	—	
SHEET 5 OF 5		

EQUIPMENT CORPORATION

TITLE

TIMING GENERATOR

(T16E)

DWG NO. D CS M8009-0-1 REV. B

NEXT ASSY

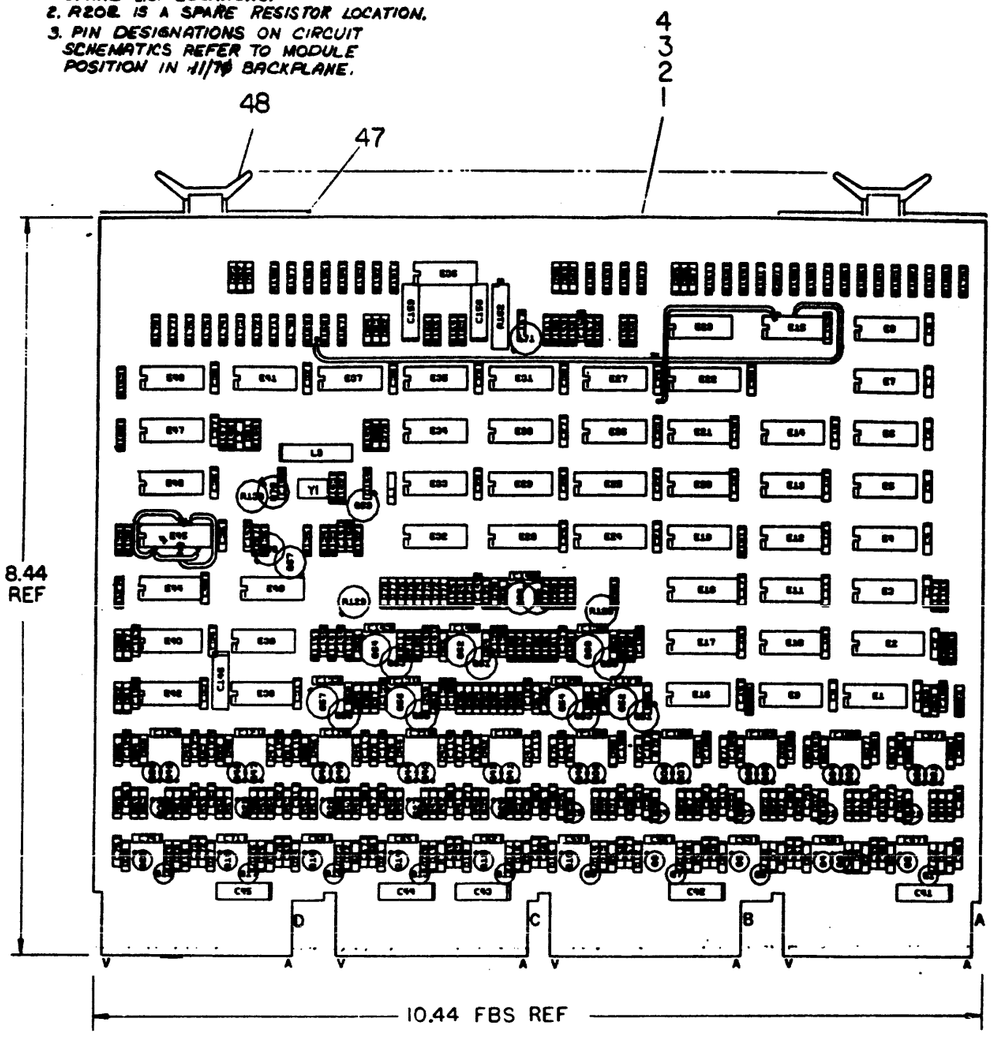
REVISIONS

REV	CHANGE NO	CHK

SECTION VII
KB11-C TIMING LOGIC

NOTES:

1. E3, E27, E36, E40, E44, AND E49 ARE SPARE I.C. LOCATIONS.
2. R208 IS A SPARE RESISTOR LOCATION.
3. PIN DESIGNATIONS ON CIRCUIT SCHEMATICS REFER TO MODULE POSITION IN 11/70 BACKPLANE.



PIN NOMENCLATURE

MODULE PIN	BACKPLANE PIN
A	C
B	D
C	E
D	F

REF				
REF		X Y COORDINATE HOLE LOCATION	K-CO-M8139-0-4	1
REF		ASSY/DRILLING HOLE LAYOUT	D-AH-M8139-0-5	2
REF		MODULE ECO HISTORY	B-MH-M8139-0-0	3
1		ETCHED CIRCUIT BOARD	5011344	4
44	C1 THRU C40. C150,C153, C155,C156	CAP, .01uf, 100V	1001818-01	5
6	C41,C42,C43,C44,C45,C146, C158,C159	CAP, 6.8uf, 35V, 10%	1005300	6
98	C48 THRU C97,C99,C100,C102 C103,C105,C106,C108,C109, C111,C114,C115,C117,C118, C120,C121,C123,C124,C126 THRU C145,C147,C148,C149, C151,C152,C160,C112	CAP, .22uf, 50V, 80-20%	1010274-01	7
18	C98,C101,C104,C107,C110, C113,C116,C119,C122,C125	CAP, 33pf, 100V 5%	1000609	8
1	C157	CAP, 47pf, 100V, 5%	1000611	9
1	C154	CAP, 100pf, 100V 5%	1000618	10
52	D1,D3,D4,DC,D7,D9,D10,D12, D13,D15,D16,D18,D19,D21, D22,D24,D25,D27,D28,D30 THRU D50,D57,D58,D61,D62, D64,D65,D67,D68,D69,D70,D53,D54	DIODE DEC 777	1103841	11
39	D2,D5,D8,D11,D14,D17,D20, D23,D26,D29,D53,D56,D59, D60,D63,D66,D71 THRU D93	DIODE D662	1100113	12
17	R6 THRU R10,R40,R46,R52, R58,R64,R67,R71,R73,R75, R99,R113,R69	RESISTOR, 4.7K, 1/4W, 5%	1300447	13
6	R11,R16,R21,R26,R31,R143	RESISTOR, 1.5K, 1/4W, 5%	1300391	14
5	R12,R17,R22,R27,R32	RESISTOR, 15K, 1/4W, 5%	1300498	15
28	R13,R15,R18,R20,R23 R25, R28,R30,R33,R35,R38,R41 R47,R50,R53,R56,R59,R62, R65,R102,R104,R114,R115, R132,R150,R44	RESISTOR, 10 OHM, 1/4W, 5%	1301317	16
11	R14,R19,R24,R29,R34,R39, R45,R51,R57,R63,R121	RESISTOR, 100 OHM, 1/4W, 5%	1300229	17
76	R36,R37,R42,R43,R48,R49, R54,R55,R60,R61,R69 THRU R96,R101,R105 THRU R112, R123,R124,R126,R130,R139, R140,R141,R148 THRU R153, R167 THRU R200, R122,R20	RESISTOR, 1K, 1/4W, 5%	1300365	18
13	R66,R68,R70,R72,R76,R74, R78,R80,R82,R84,R118,R119, R120	RESISTOR, 1.2K, 1/4W, 5%	1301329	19
12	R77,R79,R81,R83,R85,R86, R103,R1 THRU R5	RESISTOR, 3K, 1/4W, 5%	1300432	20
7	R87,R88,R97,R98,R134,R135, R144	RESISTOR, 47 OHM, 1/4W, 5%	1300282	21
8	R100,R125,R127,R131,R154, R155	RESISTOR, 150 OHM, 1/4W, 5%	1300258	22
8	R116,R146,R158,R159,R160, R161,R164,R165	RESISTOR, 330 OHM, 1/4W, 5%	1300295	23
5	R117,R147,R157,R163,R166	RESISTOR, 680 OHM, 1/4W, 5%	1301424	24
2	R128,R129	RESISTOR, 2K, 1/2W, 10%, POT	1309150-07	25
1	R138	RESISTOR, 100 OHM, 1/2W, 10%, POT	1309150-05	26
2	R133,R137	RESISTOR, 68 OHM, 1/4W, 5%	1300219	27
1	R142	RESISTOR, 750 OHM, 1/4W, 5%	1301481	28
1	R145	RESISTOR, 220 OHM, 1/4W, 5%	1300271	29
1	R162	RESISTOR, 1K, 3/4W, POT	1309143-07	30
35	Q1,Q3,Q5,Q7,Q9,Q11,Q13, Q17,Q19,Q21 THRU Q25,Q31 THRU Q40,Q51,Q54,Q56,Q58, Q59,Q63,Q65,Q66,Q69,Q70 Q15	TRANSISTOR DEC 4258	1905321	31
QTY	REF DESIGNATION	DESCRIPTION	PART NO	ITEM NO

PARTS LIST

IC DEC 749112	8	16
IC TYPE	GND	+ 5V

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

CA2, DA2, EA2, FA2
CV1, DV1, EV1, FV1
CC2, DC2, EC2, FC2
CH1, DH1, EN1, FH1
CN2, DN2, EN2, FN2
CT1, DT1, ET1, FT1

+5V
C1 THRU C40 & C153 .01 uf
C41, C42, C43 & C45 6.8 uf
GND
C44 6.8 uf EA1 +15V
C46 6.8 uf EB2 -15V

FIRST USED ON OPTION MODEL: 11/70

ETCH BOARD REV: B

SEMICONDUCTOR CONVERSION CHART

DEC NO.	EIA NO.	DEC NO.	EIA NO.

REV	REVISIONS	CHANGE NO.	DATE	APPROVED
B		M8139-00001	4-15-71	A. HELENIUS

DRN. F. Lindeman 12/9/70
CH'D. D. Kappelman 12-9-70
ENG. Allen Nelson 12-15-70
PROJ. ENG. Allen Nelson 1-15-71
PROD. F. Taylor 1/15/71
NEXT HIGHER ASSY B-00-KB11-0
SCALE #
SHEET 1 OF 2

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE: TIMING GENERATOR

SIZE D | CODE CS | NUMBER M8139-0-1 | REV. B

DCS M8139-0-1

NOTES:

QTY	REF DESIGNATION	DESCRIPTION	PART NO	ITEM NO
36	Q2,04,06,08,010,012,014, 016,018,020,026 THRU 030, 041 THRU 050,052,053,055, 057,060,061,062,064,067, 068,071	TRANSISTOR DEC 30098	1503188	32
1	L1	INDUCTOR .22 UH	1811000	33
1	L2	INDUCTOR .47 UH	1810998	34
1	L3	INDUCTOR 33 MH	1881759	35
6	E1,E9,E14,E16,E36,E42	IC 74S40	1910541	36
8	E2,E17,E18,E22,E24,E25,E28 E45	IC DEC 74S112	1910545	37
5	E4,E7,E21,E40,E30	IC 74S04	1910534	38
7	E5,E8,E19,E26,E29,E33,E8..	IC 74S74	1910544	39
5	E10,E15,E31,E37,E43	IC 74S00	1910532	40
2	E11,E12	IC 74S65	1910543	41
4	E20,E23,E32,E13	IC 74S64	1910542	42
2	E34,E48	IC 74S11	1910537	43
2	E35,E39	IC 74S140	1910548	44
2	E41,E47	IC 74S20	1910539	45
1	Y1	CRYSTAL 33.333 MHZ	1810694-01	46
8		EYELET	9006732	47
4		HANDLE FLIP CHIP MAGENTA	9008337-06	48
A/R		TAPE,2 SIDED	9007834	49
12"		WIRE,#30 AWG BUSS(RETROFIT)	9105740-55	50
A/R		PERMA-BOND	9009157	51
1	R136	RESISTOR 120 OHM 1/4W 5%	1300247	52
1	R203	RESISTOR 33 OHM 1/4W 5%	1300197	53

IC TYPE	GND	+5V
GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE		

IC PIN LOCATIONS

FIRST USED ON OPTION MODEL: 11/70

PARTS LIST

ETCH BOARD REV: B

REV	CHANGE NO.	DEC NO.	EIA NO.

REVISIONS

SEMICONDUCTOR CONVERSION CHART

	NAME	DATE
DRN	L Lieberman	12/9/74
CHK-B		12/9/74
ENG		1-13-75
PROJ ENG		1-13-75
PROD		1/13/75

NEXT HIGHER ASSY: B-DD-KB11-0

SCALE: FF

SHEET 2 OF 7

DIST

digital EQUIPMENT CORPORATION

TITLE: TIMING GENERATOR

SIZE D | CODE CS | NUMBER M8139-0-1 | REV. B

DCS M8139-0-1 B

TMCF CACHE ADRS H
CA1
TMCC ABORT H
TIGA MEM SYNC IN H
TIGB SNGLE CY L
TIGC TPB H
R153 150Ω
TIGA CONT (1) H
+3VB
CL2
TIGA SNGCY H
TIGA STOP T1 L
+3VE
TIGC TPB L
TIGC TPB H
R153 1K
AV2
TIGA T1 MAT H
R138 1K
FT2
TIGA T2 MAT H
TIGA T5 (0) H
TIGA T2 (0) H
TIGA T4A (0) H
R200 1K
CB2
TIGA T3 MAT H
+3VA
R148 1K
FD1
TIGA T4 MAT H
R186 1K
FK1
TIGA T5 MAT H
R139 1K
FU1
TIGA TAH MAT H
R187 150Ω
TIGA ROM INIT A L
TIGA T6 (1) H
TIGA T6 L
UBCE ROM INIT H
EJ1
+3VD
TIGA ROM INIT B L
+3VF
+3VH
TIGA CONT (1) H
TIGB CONT L
TIGA T1 (1) L
+3VJ
TIGA S1 (0) H
TIGA PAUSE H
TIGB ROM+UPB (1) H
TIGA T2 (0) H
CB2
SCCD INTO REG (1) L
CM2
UBCA UNIBUS ADRS H
CB1
UBCB TIG RESTART H
TIGC TPB L
R131 150Ω
+5V
CM2
SAAN NOT CACHE ADRS H
TIGA S0 (0) H
CA1
RACB ROM 40 L
CC1
UBCD EXT BRQ H
FL2
RACB UBSDBB H
+5V
RN6 330Ω
R117 680Ω
+3VD
UBCE ROM INIT H
EJ1
TIGC TPB L
R154 150Ω
+3VK
DH2
SSAC INH PSEUDO T3 L
TIGC TPB H
TIGA PAUSE H
TIGA S0 (1) H
FC1
TIGA PSEUDO T3 H
TIGA T5 (1) L
CU1
TIGA MEM SYNC H
CCBC MEM SYNC H
CM2
TIGA MEM SYNC (1) H
TIGA T1 (1) H
TIGA MEM SYNC (0) H
TIGA ROM INIT A L
RACA UBAR H
CU1
CP1
TIGA CLK BBA H
TIGC TPB L
+3VD
+3VF
TIGA T3 (1) H
R100 150Ω
+3VF
+3VN
DA1
TIGA CLK BR H
+3VJ
CM1
RACB ROM 40 L
TMCF CACHE ADRS H
CB1
TIGA T3A (1) H
TIGA PAUSE H

TIMING CONTROL SLOT 13

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE TIMING GENERATOR (TIGA)
SIZE D CODE CS NUMBER M8139-Ø-1 REV B
SCALE — SHEET 3 OF 7 DIST

DCS M8139-Ø-1 REV B

XMAA S3 L — FJ1 — +5V R146 330Ω — R147 680Ω

TIGB RC EN (Ø) H
TIGB MS EN (Ø) H
TIGB XTAL L
TIGB XTAL EN (Ø) H
TIGB RC H
TIGB RC L
TIGB XTAL H

74S04 E30 — 74S00 E34 — 74S11 E34 — 74S04 E30 — 74S04 E30

74S74 E29 — 74S74 E28 — 74S74 E29 — 74S74 E28 — 74S00 E33 — 74S74 E38

+3VJ — 74S04 E30 — +3VK — 74S04 E21

TIGB XTAL H — TIGB XTAL L — TIGB RC H — TIGB RC L

74S64 E32 — TIGB SOURCE CLOCK L

SOURCE SYNCHRONIZER

XMAA S2 L — FV2 — +5V R164 330Ω — R163 680Ω — C158 .33µf

XMAA S1 L — FB1 — +5V R165 330Ω — R166 680Ω — C189 .33µf

74S00 E37 — 74S00 E37 — 74S00 E37 — 74S20 E41 — 74S20 E41

SCCF CONT H — DN1 — XMAA S4 L (MAINT STEPPER) — FU2 — PDRC PB CMP H — FB1 — SCCF SINGLE CYCLE H — SCCF HALT H

+5V R156 330 — R157 680

74S04 E30 — 74S04 E30 — 74S00 E31 — 74S00 E31 — 74S08 E31 — TIGB CONT L

+3VK — 74S74 E26 — TIGB ROM + UPB (1) H — TIGC TP8 L — TIGA T5 (1) L

ROM V UPB CYCLE

TIGA T4 (1) H — UBCF CNSL ACT (Ø) H — TIGA PAUSE H — 74S20 E47 — TIGB SINGLE CY L

TIGA T1 (1) H — PDRC PB CMP H — FE1 — 74S11 E48 — FU2 — TIGB PB SYNCH H

R132 10Ω — +5V

R134 47 — D79 D662 — D80 D662 — XTAL — R135 47 — R138 100Ω 1/2W POT — R133 68 — TIGB XTAL H

Q69 DEC 4258 — L3 53 µH — Q70 DEC 4258 — R136 120 — Q67 DEC 30098

C151 .22µf 50V — C152 .22µf 50V — C154 100pF — L1 .22 µH — R142 750 — R145 680 — R143 1.8K — C153 .01µf — L2 .47µH — R137 68 — R144 47 — Q68 DEC 30098 — C150 .01µf — D81 D662

CRYSTAL CLOCK

+5V R158 10Ω — C155 .01µf

Q71 DEC 30098 — R162 1K, 3/4W — C157 47 PF — R161 330Ω — C156 .01µf

74S04 E21 — +3VE

74S00 E31 — 74S140 E35 — 74S00 E36 — TIGB RC H

R/C CLOCK (MAINTENANCE)

+15V — C138 .22µf — R120 1.2K — R121 100Ω — Q63 DEC 4258 — +V2 — Q66 DEC 4258 — C198 .22µf — +V5 — D64 DEC 777 — C130 .22µf — D56 D662 — Q61 30098 — D69 DEC 777 — D70 DEC 777 — C148 .22µf — R122 1K — C149 .22µf

R128 2K, 1/2W — R129 2K, 1/2W — +15V — C142 .22µf

R105 1K — R106 1K — R107 1K — R108 1K — R152 1K — R101 1K — R111 1K — R110 1K — R109 1K

+5V — Q53 30098 — C128 .22µf — D65 DEC777 — Q54 DEC 4258 — -V3A — C129 .22µf — D57 DEC 777 — D70 D662 — D71 D662 — D76 D662 — D59 D662 — Q62 30098 — Q55 30098 — C131 .22µf — Q56 DEC 4258 — TIGB CLOCK L — -V3A — -V1A — D58 DEC 777 — C130 .22µf — C132 .22µf — TIGB CLOCK H

R117 1K — R118 1K — R119 1K — R120 1K — R121 1K — R122 1K — R123 1K — R124 1K — -15V

C160 .22µf

PHASE SPLITTER/BUFFER

+5V — R125 150Ω — +V5 — D71 D662 — +V4 — D72 D662 — +V3 — D73 D662 — +V2 — D74 D662 — +V1 — D75 D662 — C141 .22µf

MAINT. BOARD SWITCH POSITION

S3 S1 S4 S2 — Ø ⟷ 1

MAINT. SWITCHES: REF. TO XMAA BOARD		
S4	SINGLE TIME STEPPER	
S3	Ø = CRYSTAL TIMING SOURCE 1 = RC TIMING SOURCE	
S1	S2	MODE CONTROL
Ø	Ø	NO EFFECT
Ø	1	SINGLE ROM CYCLE
1	Ø	UPB STOP
1	1	SINGLE PULSE (USE SW4)

TIMING SOURCE CONTROL — SLOT 13

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
11/70		PARTS LIST		

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES
DECIMALS: .XXX = .005, .XX = .02, .X = .1 — ANGLES: ±0° 30'
REMOVE BURRS AND BREAK SHARP CORNERS. SURFACE QUALITY ✓
MATERIAL — FINISH

DRN		DATE 10/1/74
CHKD		DATE 10/1/74
ENG		DATE 10/1/74
PROJ. ENG.		DATE 11/4/74
PROD.		DATE 11/5/75

NEXT HIGHER ASSY: B-DD-KB11-Ø
SCALE —
SHEET 4 OF 7

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: TIMING GENERATOR (TIGB)

SIZE	CODE	NUMBER	REV
D	CS	M8139-Ø-1	B

DIST

REVISIONS: REV | CHANGE NO | DWR

DEC-11-DRM-NO
DRD.MS-0

NOTES:

+5V R104 1Ø C137 .22µf
R88 47 Q60 DEC 30098 D63 D662 TIGC TPB H
Q59 DEC 4258 R103 3K -V3D -15V C136 .22µf

+5V R102 1Ø C135 .22µf
TIGB CLK H R87 47 Q52 DEC 30098 D62 D662 DM2 TIGC TF H
Q51 DEC 4258 R86 3K -V3C -15V C127 .22µf DM1 TIGC TFR H

+5V +15V R114 1Ø C144 .22µf R113 4.7K Q64 DEC 30098 D66 D662 TIGC TPB L
TIGB CLK L R97 47 Q63 DEC 4258 -V3D C143 .22µf

+5V +15V R116 1Ø C145 .22µf R99 4.7K Q57 DEC 30098 ER2 D68 D662 TIGC TF L
R98 47 Q58 DEC 4258 -V3C C133 .22µf ER1 TIGC TFR L

-V3A +V5 +15V +5V
Q25 DEC 4258 R34 1ØØ C85 .22µf C84 .22µf R35 1Ø C64 .22µf
Q39 DEC 4258 R33 1Ø D15 DEC 777 R32 1.8K Q10 DEC 30098 DT2 TIGC T1 H
D39 D22 777 +V2 DS2 TIGC T1B H
D14 D662 Q9 DEC 4258
TIGA T1A (1) H R75 4.7K D35 DEC 777 C89 .22µf C90 .22µf D18 DEC 777 R29 3K -V3A
R74 1.2K Q34 DEC 4258 C59 .22µf DT1 TIGC T1R H
C110 .33µf R31 1.8K C58 .22µf -15V DS1 TIGC T1BR H
-15V

+5V +V4 +15V +5V
Q26 DEC 30098 R39 1ØØ C87 .22µf C86 .22µf R41 1Ø C63 .22µf
Q41 DEC 30098 D41 DEC 777 R38 1K D8 DEC 777 Q12 DEC 30098 ED2 TIGC T1 L
+V3 C111 .22µf D17 D662 EB2 TIGC T1B L
D46 DEC 777 Q11 DEC 4258 R6 4.7K -V3B C62 .22µf EE1 TIGC T1R L
C61 .22µf -15V ED1 TIGC T1BR L
+15V Q42 DEC 30098 R77 3K R76 1.2K E36 1K +15V
TIGA T1A (1) L C113 .33µf -V3B C112 .22µf D42 DEC 777 R40 4.7K -15V

-V3A +V5 +15V +5V
Q24 DEC 4258 C83 .22µf C82 .22µf R23Ø 1Ø C57 .22µf
R29 1ØØ D12 DEC 777 R27 1K Q8 DEC 30098 DK2 TIGC T2 H
R28 1Ø Q37 DEC 4258 D39 DEC 777 +V2 D11 D662 DL2 TIGC T2B H
+15V +5V R24 3K -V3A
R73 4.7K D34 DEC 777 C106 .22µf C56 .22µf DK1 TIGC T2R H
R72 1.2K C107 .33µf Q38 DEC 4258 C105 .22µf D10 DEC 777 DL1 TIGC T2BR H
TIGA T2A (1) H R26 1.5K C55 .22µf -15V -15V

+5V +V4 +15V +5V
Q27 DEC 30098 C89 .22µf C88 .22µf R47 1Ø C66 .22µf
R45 1ØØ R44 1Ø D21 DEC 777 R43 1K Q14 DEC 30098 EM2 TIGC T2 L
Q43 DEC 30098 D43 DEC 777 +V3 D20 D662 EA2 TIGC T2B L
C114 .22µf D19 DEC 777 Q13 DEC 4258 -V3B
+15V R7 4.7K C65 .22µf EM1 TIGC T2R L
R79 3K C64 .22µf EA1 TIGC T2BR L
R78 1.2K Q44 DEC 30098 -15V
TIGA T2A (1) L C116 .33µf D45 DEC 777 -V3B C115 .22µf R42 1K +15V
R46 4.7K -15V

SLOT 13

FIRST USED ON (PRODUCT)ION/MODEL	QTY.	DESCRIPTION	PART NO	ITEM NO
11/70		PARTS LIST		

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES TOLERANCES
DECIMALS: XXX ± .005, XX ± .02, X ± .1 — ANGLES: ±0° 30'
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓
MATERIAL —
FINISH —

DRN	J Sudman	DATE 10/1/70
CHK'D	T Pierson	DATE 10/1/70
ENG	Wm Holmes	DATE 10/27/70
ENG MGR	Wm Holmes	DATE 11/5/70
PROD	R Taylor	DATE 11/15/70

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE: TIMING GENERATOR (TIGC)

NEXT HIGHER ASSY: B-DD-K811-Ø
SCALE —
SHEET 5 OF 7

SIZE	CODE	NUMBER	REV
D	CS	M8139-Ø-1	B

DIST

REVISIONS: ZONE | CHANGE NO | REV

T16B CLOCK H
TIGA T3 (1) H
T16D T3 H
T16D T3B H
T16D T3E H
T16D T3BE H
TIGA T4 (1) H
T16D T4 H
T16D T4B H
T16D T4E H
T16D T4BE H
TIGA T5A (1) H
T16D T5 H
T16D T5B H
T16D T5E H
T16D T5BE H

T16B CLOCK L
TIGA T3 (1) L
T16D T3 L
T16D T3B L
T16D T3E L
T16D T3BE L
TIGA T4 (1) L
T16D T4 L
T16D T4B L
T16D T4E L
T16D T4BE L
TIGA T5A (1) L
T16D T5 L
T16D T5B L
T16D T5E L
T16D T5BE L

SLOT 13

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO	ITEM NO
11/70		PARTS LIST		

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES TOLERANCES
DECIMALS XXX = ±.005 XX = ±.02 X = ±.1 ANGLES ±0° 30'
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓
MATERIAL —
FINISH —

DRN	J Lindsay	DATE 10/1/74
CHKD	J Ferguson	DATE 10/1/74
ENG	Dallas Hohman	DATE 11/5/74
PROJ ENGR	Dallas Hohman	DATE 11/5/74
PROD	J Taylor	DATE 11/15/74

digital EQUIPMENT CORPORATION

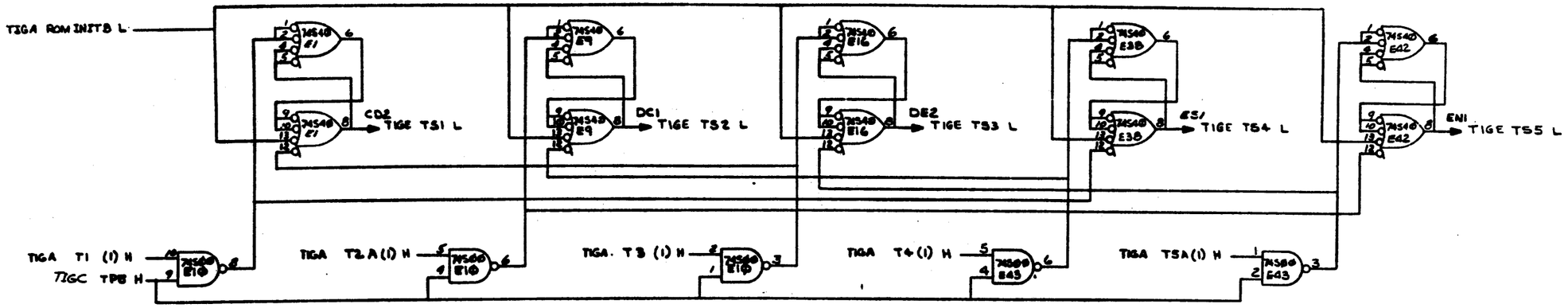
TITLE
TIMING GENERATOR
(TIGD)

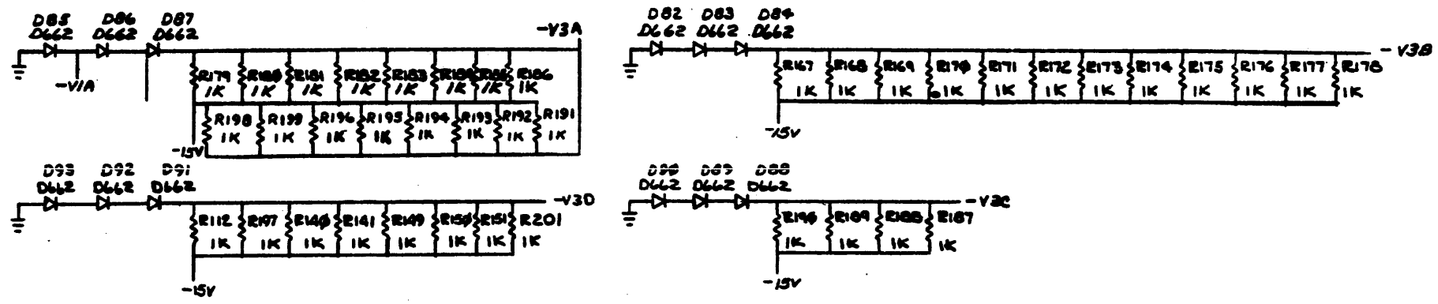
NEXT HIGHER ASSY: B-DD-KB11-Ø
SCALE —
SHEET 6 OF 7

SIZE	CODE	NUMBER	REV
D	CS	M8139-Ø-1	B

DIST

REVISIONS		
CHK	CHANGE NO	REV





TIMING STATE DRIVERS — SLOT 13

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
11/70		PARTS LIST		

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES
DECIMALS: .XXX = .005, .XX = .02, .X = .1 — ANGLES: ±0° 30'
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓
MATERIAL —
FINISH —

	DATE
DRAWN F. Christian	10/70
CHKD.	11/70
ENGR.	11/75
MAINT. ENGR.	11/75
PROD. J. Taylor	11/11/75

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE: TIMING GENERATOR (TIGE)

NEXT HIGHER ASSY.: B-DD-KB11-Ø
SCALE —
SHEET 7 OF 7

SIZE	CODE	NUMBER	REV
D	CS	M 8139-Ø-1	B

DIST.

REVISIONS: REV | CHANGE NO | CHK