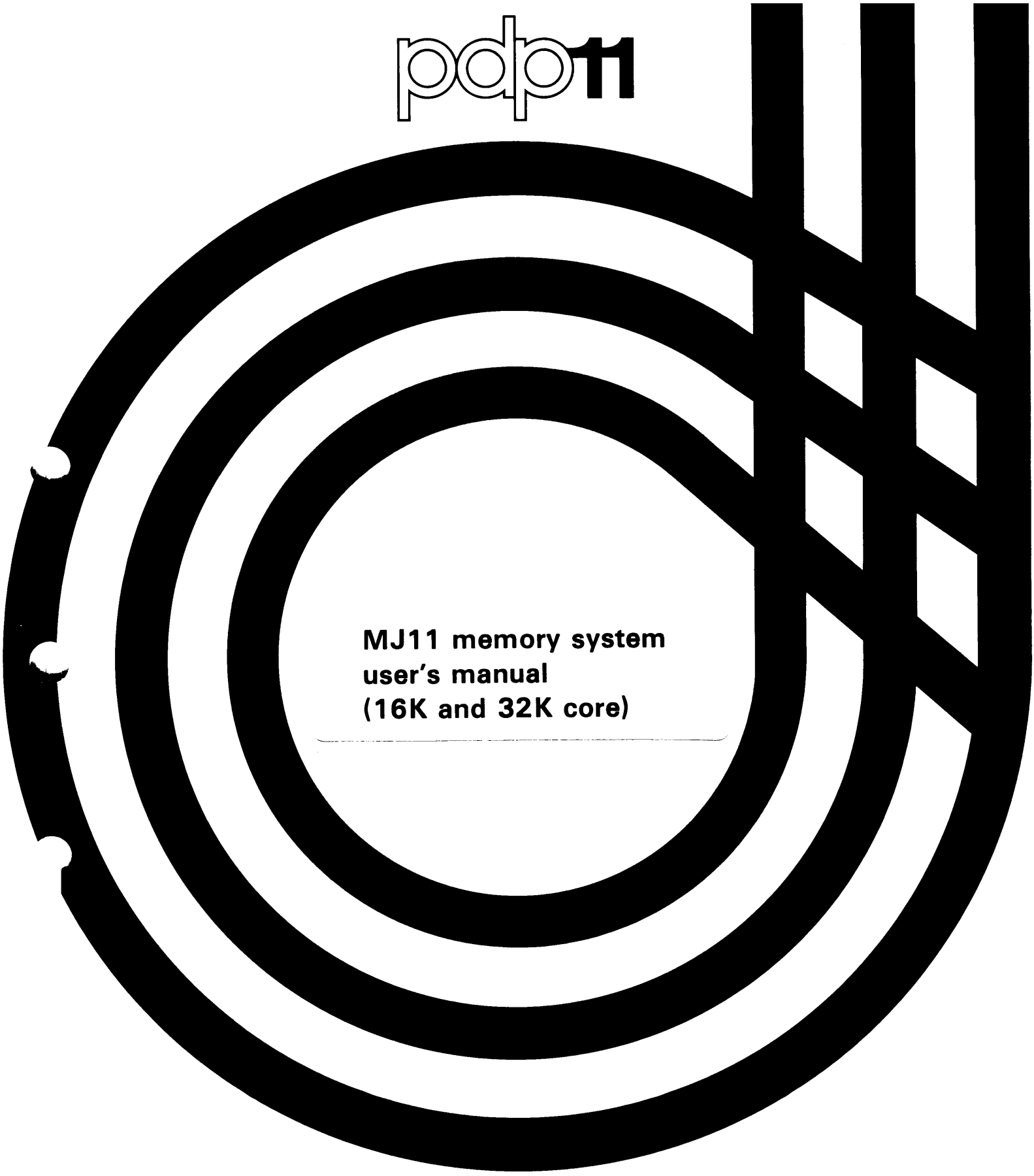

MJ11 memory system user's manual (16K and 32K core)

digital

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MJ11 memory system user's manual (16K and 32K core)

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CHAPTER 1
INTRODUCTION

1.1 INTRODUCTION
This manual provides the user with a general description of the core memory.

A complete set of engineering logic drawings is shipped with each core memory system. The drawings are bound in a separate volume entitled *MJ11 Memory System Engineering drawings*. The drawings reflect the latest print revisions and correspond to the specific memory shipped to the user.

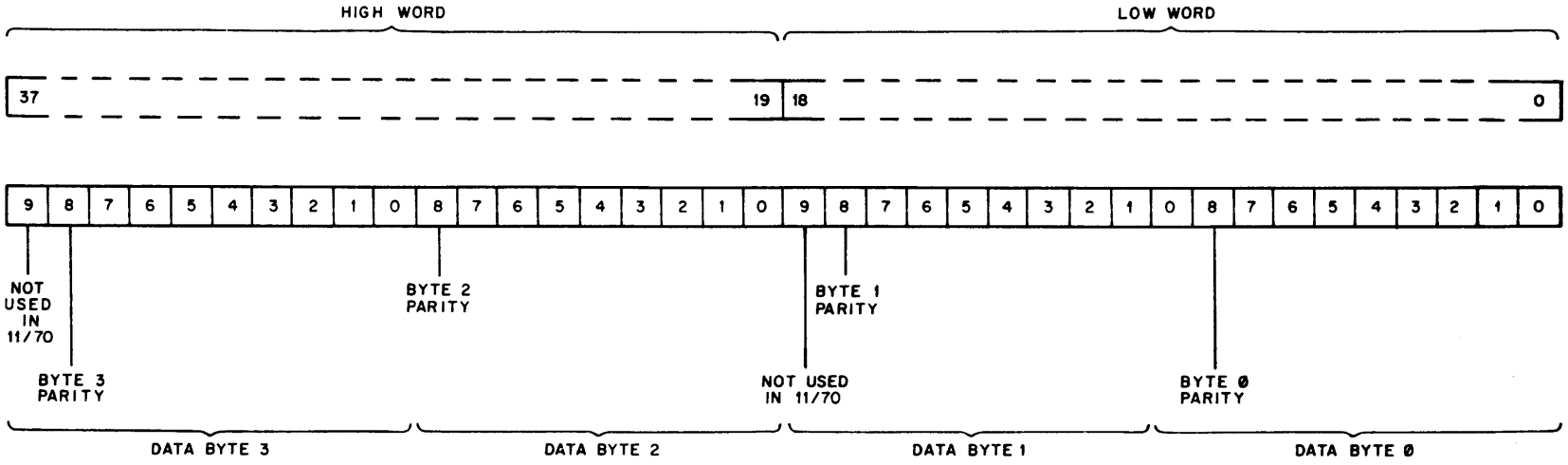
1.2 GENERAL DESCRIPTION
The MJ11 memory is a read/write, random access, coincident current, magnetic core memory. It is organized in a 3D, 3-wire planar configuration. During an MJ11 cycle, 36 bits of data (two PDP-11 words) are transferred in the format illustrated in Figure 1-1. A maximum of eight MJ11 memory boxes can be used in an 11/70 system. The eight boxes allow a maximum of 1920K words of 32K stacks, or 1024K words of 16K stacks (16K and 32K stacks can also be used together in the same system.)

1.2.1 Functional Description
Transfer of data to and from the MJ11 memory is via the Main Memory Bus. The Main Memory Bus is controlled by a single bus master that initiates all data transfers on the bus. (In the case of PDP-11/70, the bus master is the Cache.)

The bus master determines which word in memory will be accessed by placing the address of the word on the Main Memory Bus address lines. The bus master also determines the operation (read or write) to be performed. When a word is read from memory, all four bytes of the word are read; however, on a write the bus master can indicate which bytes of the word are to be written.

1.2.1.1 Memory Operations – The MJ11 memory is capable of performing three types of memory operations, as determined by Main Memory Bus operation bits MAIN C0, C1.

C1	C0	Type of Memory Cycle
0	0	Read
0	1	Not used
1	0	Write
1	1	Exchange



NOTES:

BIT 9 of DATA BYTES 3 and 1 are implemented on the MAIN MEMORY BUS but are not used in the PDP-11/70.

BIT 8 of each DATA BYTE is the byte parity bit in PDP-11/70 applications.

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Figure 1-1 36-Bit Data Transfer (2 Words)

The read operation is equivalent to a DATI on the Unibus; the write operation is equivalent to a DATO. However, the exchange operation is not equivalent to a Unibus DATIP, as indicated below.

Read – When the Main Memory Bus master reads data stored in the MJ11 memory, it performs a Read operation. Magnetic cores are a destructive-read data storage medium, i.e., as data is read from magnetic cores, the data stored in the cores is destroyed. After the data stored in the magnetic cores is destructively read, the cores are remagnetized so that they contain the original data. When a read operation is performed, the MJ11 reads the information from the selected core location and stores it in a memory data register. The MJ11 then gates the information onto the Main Memory Bus data lines to the bus master and also rewrites the information into core.

Write – When the Main Memory Bus master writes data into the MJ11 memory, it performs a write operation. The write operation is performed only on selected bytes within the addressed word. During the write operation, the data bytes to be written are loaded into a memory data register. Next, the selected bytes of the addressed memory location are cleared (destructively read) to all zeros. The data in the memory data register is then written into memory. During the write operation, the unselected bytes are read/restored just as in a read operation.

Exchange – The exchange operation allows the bus master to exchange data with the MJ11 memory. Like a write operation, the exchange operation is performed on selected bytes within the addressed word. Although only the selected bytes are written into core, all four bytes at the addressed location are transmitted to the bus master. During an exchange operation, the data bytes from the bus master are temporarily latched in the memory, as the cores at the selected memory location are destructively read. The data read from the cores is transmitted to the bus master, while the data which has been temporarily latched is written into core. During the exchange operation, unselected bytes are read/restored just as in a read operation.

The exchange operation can be seen as a combination of the read and write operations. Note that the exchange operation differs from a DATIP in that the new data must be provided by the bus master prior to receipt of the read data.

1.2.1.2 Specifications – Table 1-1 lists the specifications for the MJ11 memory.

1.2.1.3 MJ11 Options – Various configurations of the MJ11 Memory are available. Table 1-2 lists these options.

1.3 3D, 3-WIRE CORE MEMORY FUNDAMENTALS

Data stored in ferrite cores by magnetizing the iron compound in the cores. A core which has been magnetized so that the ferromagnetic domains align, as shown in Figure 1-2a, can be said to store a logic 1. Magnetization in the opposite direction (Figure 1-2b) would then represent a logic 0. The magnetic state of the core can be switched from a logic 1 to a logic 0 and vice versa by a magnetic field induced by current flowing in a wire threaded through the core (Figure 1-3). Due to the hysteresis effect inherent in all ferromagnetic materials, the current must be large enough to produce sufficient magnetic field intensity to switch the core. Once switched, the core remains in its new state.

In a 3-wire, planar core memory configuration, 3 wires are threaded through each core. The combined magnetic field induced by currents flowing through two of these wires (X and Y windings) is used to change the magnetic state of the core. The third wire (Sense/Inhibit winding) will be discussed later. The configuration used is shown in Figure 1-4.

Table 1-1 MJ11 Memory Specifications

	MJ11-A	MJ11-B
Type:	Magnetic core, read/write, coincident current, random access	
Organization:	Planar, 3D, 3wire	Folded, 3D, 3 wire
Capacity:	MAX. – 2 million bytes MIN. – 64K bytes Increments – 64K bytes	MAX. – 4 million bytes MIN. – 128K bytes Increments – 128K bytes
Cycle Types:	Read, Write, Exchange	Read, Write, Exchange
Access Time:	600-800 ns 750 ns typical	650-900 ns 810 ns typical
Cycle Time:	850-1150 ns 1080 ns typical	980-1320 ns 1260 typical
X-Y Current Margins:	±6% @ 0° C, ±7% @ 25° C, ±6% @ 50° C	
Voltage Requirements:	+5 V ± 5% (< 0.2 V ripple) +20 V ± 5% (< 5% ripple) -5 V ± 5% (< 5% ripple)	
Power Requirements:		
Memory Control and Timing:	M8148 7W	M8147 7W
Memory Transceiver Module:	M8149 5W	M8149 5W
Drive Module:	G235 35W	G236 35W
Stack Module:	H217C 40W	H224C 40W
Sense/Inhibit Module:	G114 40W	G116 40W
Environment:		
Ambient Temperature:	0° C to 50° C (32° F to 122° F)	
Relative Humidity:	0 – 90% (noncondensing)	

Table 1-2 MJ11 Memory Options

Designation	Description
MJ11-AA	Mounting Box, memory control and two 16K stack module sets providing 32K 18-bit words. For 115 Vac.
MJ11-AB	Same as MJ11-AA, but for 230 Vac.
MJ11-AC	Cabinet with power control, mounting box (memory frame), memory control with eight 16K stack module sets providing 128K 18-bit words. For 115 Vac, 3 phase.
MJ11-AD	Same as MJ11-AC, but for 230 Vac, 3 phase
MJ11-AE	Two 16K stack module sets
MJ11-AG	MJ11-AA plus three MJ11-AE
MJ11-AH	MJ11-AB plus three MJ11-AE
MJ11-AM	One 16K stack module set (spares inventory).
MJ11-AY	MJ11-AA without cables
MJ11-AZ	MJ11-AB without cables
MJ11-BA	Power control, memory control, and two 32K stack module sets providing 64K 18-bit words. (Space for three MJ11-BE or -AE) For 115 Vac.
MJ11-BB	Same as MJ11-BA, but for 230 Vac.
MJ11-BC	Cabinet with MJ11-BA and three MJ11-BE. For 115 Vac.
MJ11-BD	Same as MJ11-BC, but for 230 Vac.
MJ11-BE	64K 18-bit memory expansion (2 MJ11-BM)
MJ11-BG	MJ11-BA and three MJ11-BE. For 115 Vac.
MJ11-BH	Same as MJ11-BG, but for 230 Vac.
MJ11-BM	32K 18-bit memory modules (no cabinet)
MJ11-BY	MJ11-BA without cables
MJ11-BZ	MJ11-BB without cables

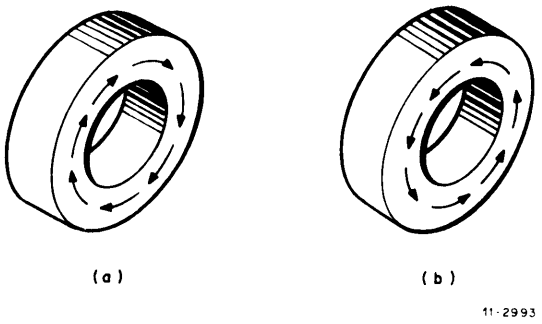

Figure 1-2 Magnetic States of Ferrite Core

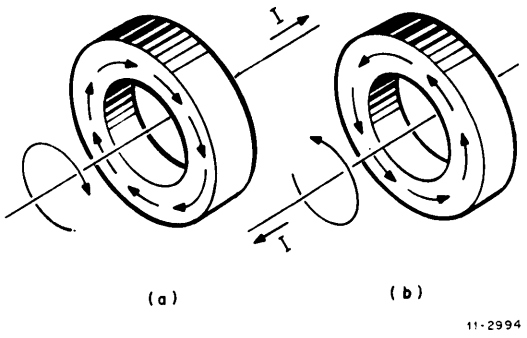

Figure 1-3 Switching Magnetic State of Ferrite Core

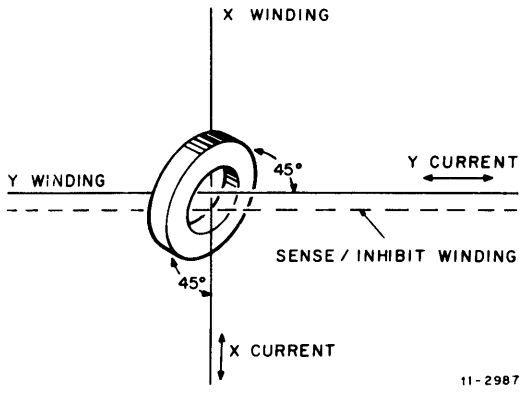

Figure 1-4 Configuration of Core Windings

The core is oriented at a 45 degree angle with respect to the X and Y windings. The current flowing through the X winding (X current) cannot by itself induce a magnetic field of sufficient intensity to change the state of the ferrite core. The same is true of current flowing through the Y winding (Y current). However, if the two currents are flowing at the same time, their combined magnetic fields can change the state of the core, as illustrated in Figure 1-5. Note that the directions of current flow must be such that their magnetic fields tend to combine rather than cancel each other out. This means that the X and Y currents required to change a core from state 1 to 0 must be opposite in direction from the currents required to change the core from state 0 to 1. (If the direction of only one of the currents was reversed, their magnetic field would tend to cancel.)

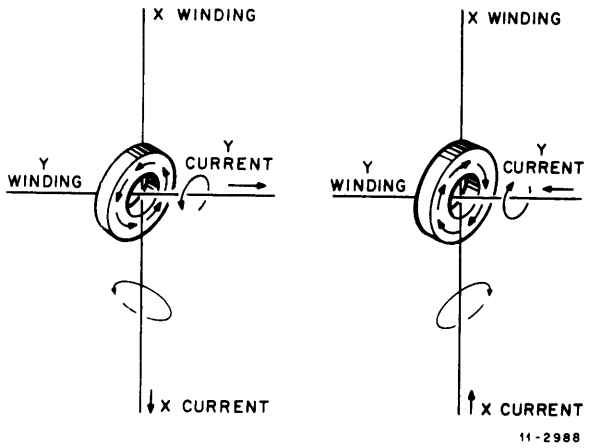

Figure 1-5 Switching Core State with Two Current Windings

1.3.1 Reading and Writing a Core

The Sense/Inhibit winding mentioned previously is threaded through a core in parallel with the Y current winding. The Sense/Inhibit winding allows a selected core to be read and written.

1.3.1.1 Reading a Core - In order to read a core, X and Y currents are switched through a core in the direction that will switch the core from the 1 magnetic state to the 0 state. This change in magnetic field induces a voltage (induced EMF) in the Sense/Inhibit winding, which is detected and amplified by a sense amplifier. This in turn sets a corresponding data register bit. If the core was originally in the 0 magnetic state, it will not "switch", but will remain in the 0 state. Consequently, no voltage is induced in the Sense/Inhibit winding, and the corresponding data register bit is not set.

Note that as a result of being read, the core will be in the 0 magnetic state. The data that was stored in the core has been destroyed - this is termed "destructive read". Therefore, it is necessary to restore the core to its original magnetic state. This is done by rewriting the data just read (and currently stored in the data register) back into the core. Restoring data into the core is done in a manner similar to writing data into a core.

1.3.1.2 Writing a Core - In order to write data into a core, the core is initially switched to the 0 state by performing a destructive read. If a 1 is to be written into the core, X and Y currents are switched through the core in the direction that will switch the core from the 0 magnetic state to the 1 magnetic state. (This requires that the direction of X and Y current flow be opposite to that of a read).

If a 0 is to be written into core, the X and Y currents are switched on as above but, in addition, inhibit current is switched through the Sense/Inhibit winding. The magnetic field induced by the inhibit current is opposite in polarity to the field induced by the X and Y currents; this causes the magnetic fields to cancel out so that the resulting field is not sufficient to switch the core to the 1 magnetic state. The core will thus remain in the 0 magnetic state.

1.3.2 Stack Organization – Each core in a memory represents one bit of one word. The cores in a memory are grouped to form stacks. The MJ11-A memory operates with stacks organized into 16,384 18-bit words (for H217C); thus, each stack contains 16,384 × 18 = 294,912 ferrite cores. The MJ11-B memory operates with stacks organized into 32,768 18-bit words; thus, each stack contains 32,768 × 18 = 589,824 ferrite cores.

The stack is laid out as a planar array of cores, organized into 18 mats (for H217C), each MJ11-A mat containing 16,384 cores; each MJ11-B mat containing 32,768 cores. All the cores in a mat store data corresponding to the same bit position in all 16K or 32K words.

The 16,384 cores in a mat of the MJ11-A are arranged in a 128 × 128 array. There are 128 X current windings (X00–X127) and 128 Y current windings (Y00–Y127) threaded through the cores in each mat. These windings form an X-Y coordinate matrix, as illustrated in Figure 1-6. The X and Y current windings on all the mats are connected in series; this means, for example, that if current is flowing in winding X35 in mat 0, the same current is flowing in winding X35 on the 17 other mats.

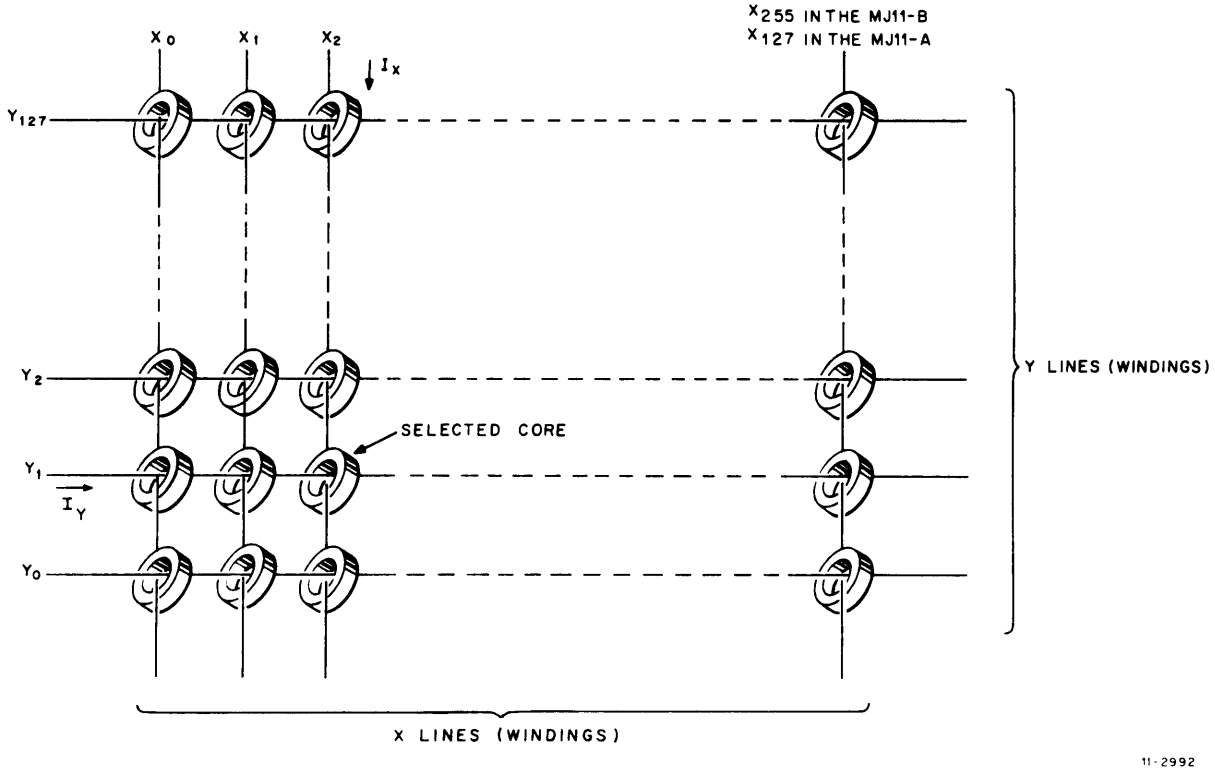

Figure 1-6 Core Configuration in an MJ11 Stack

The 32,768 cores in a mat of the MJ11-B are arranged similarly, except there are 256 X current windings (X00–X255 and 128 Y current windings (Y00–Y127) to form a 256 × 128 array (Figure 1-6).

As described earlier, both X and Y current are required to read or write data in a core. As a result of address decoding, current will be switched through one of the X windings and one of the Y windings. One core in each mat will lie at the intersection of these two current windings; this is the selected core within the mat. The set of 18 cores (one in each mat) that is selected by coincidence of X and Y current corresponds to the 18-bit word being addressed in the stack.

Sense/Inhibit Winding – It is worth re-emphasizing that the X and Y windings enable the function of selection of cores, while the Sense/Inhibit winding implements the function of reading and writing.

There are 18 Sense/Inhibit windings threaded through the cores that comprise the stack; one winding for each mat (bit position). Each Sense/Inhibit winding is threaded through all the cores of a single corresponding mat. During a read cycle, it senses whether the selected core within the mat has been switched from the 1 state to the 0 state. During a write cycle, it inhibits the selected core within the mat from switching from the 0 state to the 1 state if the bit position to which the mat corresponds is to be written with a 0.

1.3.3 Word Selection

As described in the previous paragraphs, the 16K stacks used in the MJ11 memory require that one of 128 X windings and one of 128 Y windings be energized to select a word. In the 32K stacks of the MJ11-B memory, one of 256 X windings and one of the 128 Y windings are energized to select a word. In a 3D memory organization, this selection is accomplished by means of decoding and matrices (Figure 1-7).

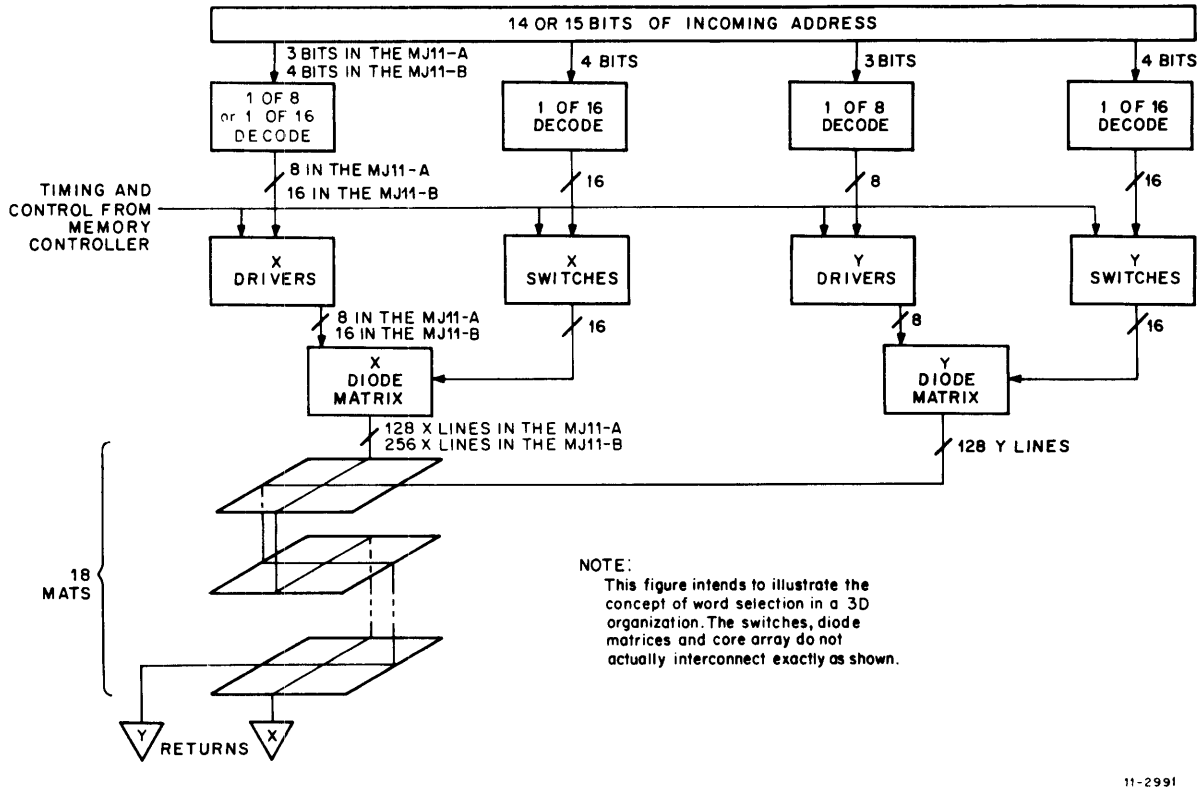

Figure 1-7 Word Selection Using 3D Organization

In the MJ11-A, 14 bits of the incoming address are decoded as follows:

3 bits select one of 8 X drivers
4 bits select one of 16 X switches
3 bits select one of 8 Y drivers
4 bits select one of 16 Y switches

In the MJ11-B, 15 bits of the incoming address are decoded as follows:

4 bits select 1 of 16 X drivers
4 bits select 1 of 16 X switches
3 bits select 1 of 8 Y drivers
4 bits select 1 of 16 Y switches

In the MJ11 the X drivers and switches operate in conjunction with an X diode matrix to select one X current winding. Likewise, the Y drivers and switches operate in conjunction with a Y diode matrix to select one Y current winding. When timing and control signals from the memory controller energize the selected drivers and switches, the flow of current through the selected X and Y current windings is enabled.

1.4 MEMORY SYSTEM ORGANIZATION

Figure 1-8 shows the relationship of the Main Memory Bus master to the MJ11 Memory Controllers. An MJ11 Memory Controller consists of an M8148 (for 16K) or M8147 (for 32K or 16K) Memory Control and Timing module, and an M8149 Memory Transceiver Card module. Up to eight memory controllers can be daisy-chained on the Main Memory Bus. Each memory controller contains switches which determine the lowest memory address to which the controller will respond. The total response range of a memory controller depends on the number of stack module sets located in the same memory frame as the memory controller and on whether interleaving is utilized.

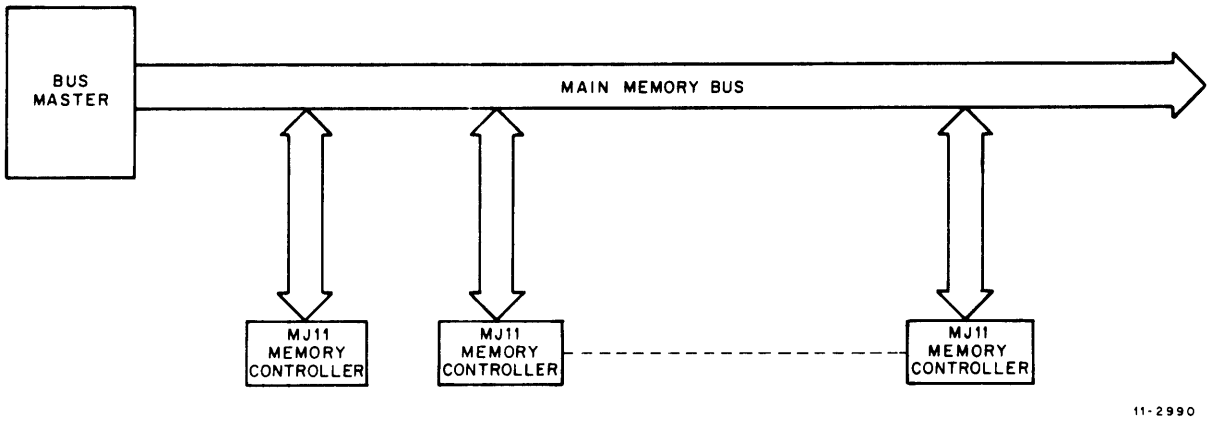

Figure 1-8 Relationship of Bus Master to Memory Controllers

Figure 1-9 is a simplified block diagram of an MJ11 memory. Note that the memory controller interfaces the Main Memory Bus to an internal bus to which all the memory stack module sets within the memory frame connect. The Main Memory Bus address and control lines connect to the M8147 (or M8148) Memory Control and Timing module, while the Main Memory Bus data lines connect to the M8149 Memory Transceiver Card. The control and timing module processes the Main Memory Bus address and control lines, determines which of the memory stacks are being accessed, decodes the type of operation to be performed, and generates the timing and control signals to perform the desired operation. The M8149 Memory Transceiver Card, controlled by the timing and control module, latches data from the bus master and gates data to and from the memory stacks, via the internal bus.

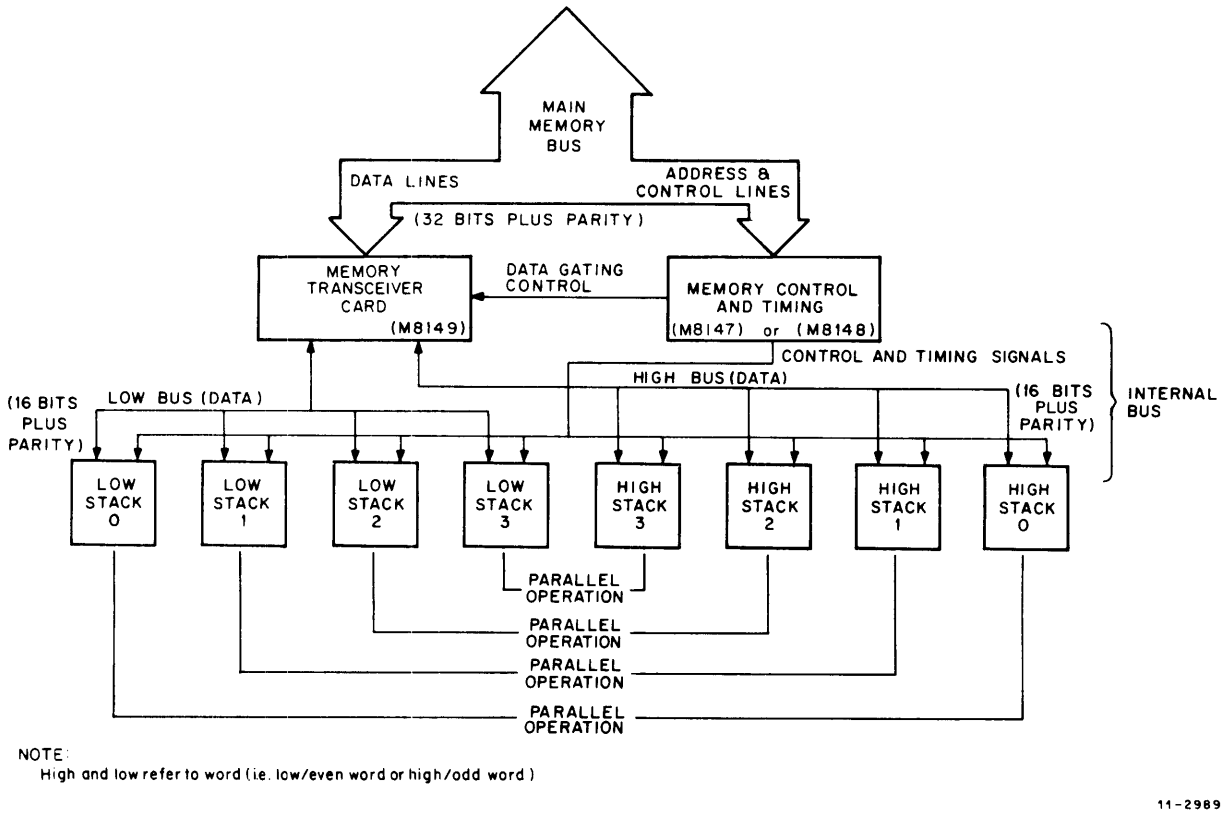

Figure 1-9 MJ11 Simplified Block Diagram

The internal bus interfaces the memory controller (i.e., the M8147 or M8148 Memory Control and Timing module and the M8149 Memory Transceiver Card module) to the stack module sets in which the memory data is stored. The Internal bus consists of bidirectional data lines and unidirectional control lines. The data lines comprise two groups: the Low Bus data lines and the High Bus data lines. The Low Bus data lines connect the stack module sets that store the low word (bytes 0 and 1) of the 36-bit double word, to the Memory Transceiver Card Module. The High Bus data lines connect the stack module sets that store the high word (bytes 2 and 3) of the 36-bit double word to the memory transceiver card module.

The control signals from the memory control and timing module enable operation of selected stack module sets; control the read, write and inhibit currents in the selected stack module sets; and determine which bytes of a 36-bit double word will be operated on and what that operation will be. The internal bus control signals are generated by the timing control signal generator in the M8147 or (M8148) module.

Each 16K stack module set consists of three modules:

	16K	32K
X-Y Driver Module	G235	G236
Sense/Inhibit Module	G114	G116
16K Stack Module	H217-C	H224-C

These are described briefly in Paragraph 1.4.1.

1.4.1 Module Descriptions

This paragraph provides a brief description of the modules used in the MJ11 memory. Paragraphs 1.4.1.1 and 1.4.1.2 describe the modules that make up the memory controller. Paragraphs 1.4.1.3 through 1.4.1.8 describe the three modules that make up a stack module set.

1.4.1.1 M8147 (or M8148) Memory Control and Timing Module - The M8147 (or M8148) module interfaces the address and control lines of the Main Memory Bus to the MJ11 memory. The M8148 is used for 16K stack modules; the M8147 is used for 32K stack modules. (The M8147 can also be used with 16K stack modules.) The memory control and timing module contains address recognition logic, address latches, stack selection logic, a read timing generator, write timing generator, timing control signal generator, power monitor logic, and maintenance circuits.

Address Recognition Logic - The address recognition logic processes the incoming Main Memory Bus address to determine whether the address falls within the response range of the memory controller. If the address is within its response range, the module will initiate a memory cycle when it receives MAIN START on the Main Memory Bus. When the address is outside the response range, the bus master is addressing some other memory controller, or perhaps nonexistent memory.

Memory Address Latches - If the Main Memory Bus Address is in the memory controller's response range, address (and control) bits are loaded into the memory address latch. The information loaded into the memory address latch indicates which operation is to be performed and the core locations to be operated on. Once this information is latched, the memory cycle can be executed without active participation by the bus master, and without tying up the Main Memory Bus. While the memory cycle is being executed, the bus master can attend to other tasks, such as initiating memory cycles by other memory controllers.

Stack Selection Logic - As a result of address processing, the memory control and timing module enables operation of the stack module sets that are being referenced by a particular memory cycle.

Read Timing Generator - The read timing generator produces the basic timing waveforms used to generate the signals that control the read cycle operation of the selected stack module sets.

Write Timing Generator - The write timing generator produces the basic waveforms utilized to generate the signals that control the write cycle operation of the selected stack module sets.

Timing Control Signal Generator – The timing control signal generator generates the timing and control signals that turn on the read, write, and inhibit currents in the stack module sets. Only stack module sets enabled by the stack selection logic will respond to these control signals. The timing control signal generator also generates timing and control signals used for interfacing on the main memory bus.

All of the timing and control signals generated by the timing control signal generator are developed from the basic timing waveforms produced by the read timing generator and the write timing generator.

Power Monitor and Initialize – The power monitor and initialize logic is activated when MAIN DC LOW is asserted on Main Memory Bus. This condition indicates that further memory operations are to be discontinued. A 3 μs approximate delay is provided to allow the memory to complete the current memory cycle; the current sources are then inhibited to ensure nonvolatility during a power outage.

Maintenance Circuits – The maintenance circuits allow memory functions to be tested under program control. The circuits test the memory parity logic and allow the memory current sources and sense amplifier strobe pulses to be margined.

1.4.1.2 Memory Transceiver Card (M8149) – The memory transceiver card interfaces the data lines of the Main Memory Bus to the data lines of the internal bus of the MJ11 memory. Four cable connectors are mounted on the M8149 module. One pair of connectors connect the Main Memory Bus data lines to the MJ11 memory; the other pair carry the Main Memory Bus out to the next memory controller in the daisy chain (or connect to type H873 Main Memory Bus terminators). The memory transceiver card contains data receivers, an input data latch, output data gating, and data drivers.

Data Receivers – The data receivers receive the signals on the Main Memory Bus data lines.

Input Data Latch – The input data latch latches the data received on the Main Memory Bus at the beginning of every memory cycle.

Output Data Gating – The output data gating logic gates read data from the internal bus of MJ11 memory to be driven onto the Main Memory Bus. The data is gated out only during a fixed interval within the read memory cycle; this prevents the Main Memory Bus data lines from being occupied unnecessarily by the memory.

Data Drivers – The data drivers drive data being read from the MJ11 memory to the bus master.

1.4.1.3 H217 C Stack Module – The H217C Stack module contains the ferrite 16K core array, X diode matrix, Y diode matrix, sense/inhibit terminations, stack charge circuit, and a thermistor.

Ferrite Core Array – The ferrite core array is a planar array containing 18 mats. Each mat is an array of 128 × 128 equals 16K cores.

X Diode Matrix – The X diode matrix is used in conjunction with the X current drivers and switches on the G235 module to route current through one of the 128 X windings threaded through the cores in each mat of the stack.

Y Diode Matrix – The Y diode matrix is used in conjunction with the Y current drivers and switches on the G235 module to route current through one of the 128 Y windings threaded through the cores in each mat of the stack. The cores which lie at the intersection of energized X and Y windings comprise the word being addressed in the stack.

Sense/Inhibit Terminations – The sense/inhibit terminations terminate the sense/inhibit lines in order to minimize transmission line reflections.

Stack Charge Circuit – The stack charge circuit is used to bias the X and Y drive lines to near ground potential during read time, and to near +20 V during write time. The purpose of this is to backbias the diodes on the X-Y matrix to prevent loss of drive currents due to charging capacitance through unselected diodes.

Thermistor – The thermistor provides temperature compensation for the bias source generator on the G235 X-Y Driver Module.

1.4.1.4 H224-C Stack Module – The H224-C Stack module contains the ferrite 32K core array, X diode matrix. Y diode matrix, sense/inhibit terminations, stack charge circuit, and a thermistor.

Ferrite Core Array – The ferrite core array is a planar array containing 18 mats. Each mat is an array of 256 × 128 = 16K cores.

X Diode Matrix – The X diode matrix is used in conjunction with the X current drivers and switches on the G236 module to route current through one of the 256 X windings threaded through the cores in each mat of the stack.

Y Diode Matrix – The Y diode matrix is used in conjunction with the Y current drivers and switches on the G236 module to route current through one of the 128 Y windings threaded through the cores in each mat of the stack. The cores which lie at the intersection of energized X and Y windings comprise the word being addressed in the stack.

Sense/Inhibit Terminations – The sense/inhibit terminations terminate the sense/inhibit lines in order to minimize transmission line reflections.

Stack Charge Circuit – The stack charge circuit is used to bias the X and Y drive lines to near ground potential during read time, and to near +20 V during write time. The purpose of this is to backbias the diodes on the X-Y matrix to prevent loss of drive currents due to charging capacitance through unselected diodes.

Thermistor – The thermistor provides temperature compensation for the bias source generator on the G236 X-Y Driver module.

1.4.1.5 G114 Sense/Inhibit Module – The G114 Sense/Inhibit module interfaces a 16K stack module set to the data lines of the internal bus of the memory. The module contains bus receivers and drivers, a data register, inhibit drivers, sense amplifiers, and a threshold circuit.

Bus Receivers and Drivers – The data lines of the memory internal bus are received by type 8640 receivers and applied to the data input of the data register. This register is clocked under control of the M8417 (or M8148) Control and Timing module.

The bus drivers gate read data from the data register onto the memory internal bus.

Sense Amplifiers – During a destructive read of cores selected by an incoming address, the sense amplifiers pick up the voltages induced on the sense/inhibit lines when a core is switched from a 1 to a 0. These signals are detected and amplified by the sense amplifiers, whose outputs direct set the corresponding bits of the data register.

Threshold Circuit – The threshold circuit provides a reference threshold voltage to the sense amplifiers. In a read operation, if the threshold voltage (17 mV) is exceeded during sense strobe time, the sense amplifier produces an output.

Inhibit Drivers - When switched on, the inhibit drivers drive current through the sense/inhibit lines. There are 18 inhibit drivers, one corresponding to each mat in the stack (i.e., one per bit). Inhibit current is driven through a mat during the write portion of a memory cycle to inhibit the selected core within the mat from being written a logic 1.

Data Register - The data register is an 18-bit flip-flop register used to temporarily store data during read and write operations.

During a read operation:

a. The register is initially cleared.

b. Register bits corresponding to logic 1s sensed by the sense amplifiers are set.

c. The data in the register is written (restored) into core.

d. The data in the register is gated to the Main Memory Bus via the internal bus.

During a write operation:

a. The register is initially cleared.

b. The register bytes not to be written are loaded with data read from core.

c. The remaining register bytes are loaded with the data to be written.

d. The data in the register is written into core.

During an exchange operation:

a. The register is initially cleared.

b. Register bits corresponding to logic 1s sensed by the sense amplifiers are set.

c. The data in the register is gated to the Main Memory Bus via the internal bus.

d. The register is loaded with the data to be written.

e. The data in the register is written into core.

1.4.1.6 G116 Sense/Inhibit Module - The G116 Sense/Inhibit module interfaces a 32K stack module set to the data lines of the internal bus of the memory. The module contains transceivers, a data register, inhibit drivers, sense amplifiers, and a threshold circuit.

Transceivers - The 8641 transceivers are used to interface data between the M8149 Memory Transceiver module and the data input of the data register in the G116. The data register is clocked from timing signals of the control and timing module.

Sense Amplifiers - During a destructive read of cores selected by an incoming address, the sense amplifiers pick up the voltages induced on the sense/inhibit lines when a core is switched from a 1 to a 0. These signals are detected and amplified by the sense amplifiers, whose outputs direct set the corresponding bit of the data register.

Threshold Circuit – The threshold circuit provides a reference threshold voltage to the sense amplifiers. In a read operation, if the threshold voltage (17 mV) is exceeded during sense strobe time, the sense amplifier produces an output.

Inhibit Drivers – When switched on, the inhibit drivers drive current through the sense/inhibit lines. There are 18 inhibit drivers, one corresponding to each mat in the stack (i.e., one per bit). Inhibit current is driven through a mat during the write portion of a memory cycle to inhibit the selected core within the mat from being written as a logic 1.

Data Register – The data register is an 18-bit flip-flop register used to temporarily store data during read and write operations.

1.4.1.7 G235 X-Y Driver Module – The G235 Driver module contains the address decoders, X and Y current switches and drivers, sense strobe control, bias source generator, and current sources.

Address Decoders – The address decoders decode 14 bits of the incoming address. Seven of the 14 address bits are used for X address selection and seven are used for Y address selection. Four of the seven X bits select an X current switch and three select an X driver. The same situation occurs for the Y switches and drivers. The address bits not sent to the G235 module are used in the memory control and timing module. The selected X and Y drivers and switches ultimately specify one core out of 16,384 in each mat in the stack.

Current Switches and Drivers – The switches and drivers, in conjunction with the X and Y diode matrices, direct the flow of current through the magnetic cores to ensure the proper polarity for the desired function. This action is necessary because the currents for a write operation are opposite in polarity to the currents required for a read operation. There are separate switches and drivers for the read and write circuits in the selection matrix.

Sense Strobe Control – The sense strobe control is a one-shot multivibrator whose duration can be controlled by an external voltage input. The sense strobe control determines when the sense amplifiers are examined.

NOTE

A factory adjustment is made by cutting certain jumpers to determine the optimum position for the sense strobe to occur. Sophisticated test equipment is used in making this factory adjustment and changing the jumper configuration will result in less than optimum memory performance.

Bias Source Generator – The bias source generator is a dc, temperature-compensated, bias current used to control the amplitude of the current from the X and Y current generators and inhibit current sources.

Current Sources – X and Y current generators provide the current necessary to change the state of the magnetic cores. The rise time and amplitude of the output-current waveform have been selected to provide optimum switching of the core states and maximum signal-to-noise ratio for a wide range of temperatures.

1.4.1.8 G236 X-Y Driver Module – The G236 X-Y Driver module contains the address decoders, X and Y current switches and drivers, sense strobe control, bias source generator, and current sources.

Address Decoders – The address decoders decode 15 bits of the incoming address. Eight of the 15 address bits are used for X address selection and seven are used for Y address selection. Four of the eight X bits select an X current switch and four select an X driver. Four of the seven Y bits select Y current switch and three select Y driver. The address bits not sent to the G236 module are used in the memory control and timing module. The selected X and Y drivers and switches ultimately specify one core out of 32,768 in each mat in the stack.

Current Switches and Drivers – The switches and drivers, in conjunction with the X and Y diode matrices, direct the flow of current through the magnetic cores to ensure the proper polarity for the desired function. This action is necessary because the currents for a write operation are opposite in polarity to the currents required for a read operation. There are separate switches and drivers for the read and write circuits in the selection matrix.

Sense Strobe Control – The sense strobe control is a one-shot multivibrator whose duration can be controlled by an external voltage input. The sense strobe control determines when the sense amplifiers are examined.

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A factory adjustment is made by cutting certain jumpers to determine the optimum position for the sense strobe to occur. Sophisticated test equipment is used in making this factory adjustment and changing the jumper configuration will result in less than optimum memory performance.

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Current Sources – X and Y current generators provide the current necessary to change the state of the magnetic cores. The rise time and amplitude of the output-current waveform have been selected to provide optimum switching of the core states and maximum signal-to-noise ratio for a wide range of temperatures.

CHAPTER 2
INSTALLATION

2.1 SCOPE

This chapter describes the unpacking, installation, and certification procedures pertaining to the MJ11 memory. Paragraph 2.2 describes the procedure for physical installation of an MJ11 memory cabinet. Paragraph 2.3 describes the procedure for installing a memory frame within an existing cabinet. Paragraph 2.4 describes procedures and guidelines required to expand memory capacity within an existing memory frame.

NOTE

The memory configuration rules presented in Paragraph 2.4 apply to any installation in which memory capacity is altered. In PDP-11/70 systems, the System Size register must be reconfigured (Paragraph 2.7) whenever memory capacity is altered.

2.2 MEMORY CABINET INSTALLATION

Before unpacking the equipment, check the shipment against the packing list provided. Check that the correct number of packages have been delivered and that each package contains all the items listed on the accompanying packing slip. Also, check that all items on the accessories list in the Customer Acceptance Procedures have been included in the shipment. Unpack and install the cabinet as follows:

1. Remove outer shipping container.
2. Remove the polyethylene cover from the cabinets.
3. Remove the tape or plastic shipping pins from the cabinet access door.
4. Remove the two bolts securing the cabinet to the shipping pallet.
5. Remove the side panel from the cabinet with which the memory cabinet will abut.

NOTE

In PDP-11/70 systems, a memory cabinet is added to the right of the existing memory cabinet. TU16 tape drives, if present, must be moved to provide space for the memory cabinet being added to the system.

6. Raise the leveling feet so that they are above the level of the roll-around casters.

7. Use wood blocks and planks to form a ramp from the skid to the floor and carefully roll the cabinet onto the floor.

8. Roll the system to the proper location for installation.

9. With the cabinet in position, install H952-GA filler strips between the memory cabinet and the adjacent cabinet. Remove four bolts each from the front and rear filler strips. Butt the cabinets and the filler strips in place and rebolt through both cabinets and the filler strips (Drawing C-UA-H952-G-0). Do not tighten the bolts securely at this time.

10. Lower the leveling feet so that the cabinet is not resting on the roll-around casters but is supported on the leveling feet.

11. Tighten the bolts that secure the memory cabinet to the adjacent cabinet. Ensure that all leveling feet are firmly on the floor.

12. Install ground strapping to ensure that all cabinets are at a common earth ground.

13. Remove the two shipping brackets securing each memory frame to the cabinet. The shipping brackets are located at the front of the memory frame. Save the shipping hardware for possible re-use.

14. Plug the memory cabinet power controller into an appropriate 3-phase, 5-wire ac outlet. The 861-E power controller (220 Vac) is not supplied with a power cord and connector. A power cord and connector meeting local legal requirements must be installed. Refer to the *861-A,B,C,D,E Power Controller Maintenance Manual* for this procedure. The 861-D power receptacle and plug are illustrated in Figure 2-1.

15. Connect a power control cable from the memory cabinet power controller to power controllers in adjacent cabinets.

16. Configure the switches on the M8147 (or M8148) modules (Paragraph 2.4).

17. Route and connect the Main Memory bus cables (Paragraph 2.5).

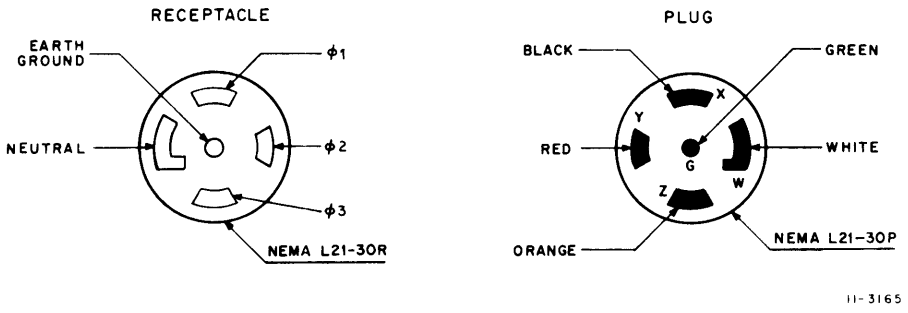


Figure 2-1 861-D Power Connectors

2.3 MEMORY FRAME INSTALLATION

An MJ11 memory frame is shipped in a protective box (Figure 2-2). Remove the memory frame from the box and visually inspect for damage. Save the shipping cartons and packaging materials in case it becomes necessary to return the memory frame for service. The slide mounts are attached to the memory frame, but the mounting screws are packed in a bag placed in the shipping container.

2.3.1 Slide Mounting

The fixed slides must be mounted equidistant from and parallel to the floor at the proper cabinet frame hole number (Figure 2-3). The front of the fixed slide has an integral bracket and is mounted in the cabinet with four screws that are secured with captive (Tinnerman) nuts. The rear of the fixed slide is attached to a separate L-shaped bracket with two screws and nuts. The bracket is attached to the cabinet with two screws that are secured with captive nuts.

Lift the memory frame and slide it carefully into the fixed guides until the slide release engages. Unlock the slide release and push the memory frame fully into the cabinet. Extend the memory frame enough to allow access to the front mounting screws. Slightly loosen the front and rear slide mounting screws and slide the memory frame back and forth. This allows the slides to assume a position that results in minimum binding. Retighten the mounting screws.

2.3.2 Cable Retractor

The cable retractor rod (DIGITAL Part No. 12-12173-00) prevents the Main Memory Bus cables from tangling when memory frames are extended from the cabinet. Install the cable retractor rod at the holes indicated in Figure 2-3.

2.3.3 AC Power Connection

Plug the memory frame power cord into one of the switched outlets of the cabinet power controller.

NOTE

The load at the power controller outlets must be distributed among the three phases. No other device should be plugged into a power controller phase circuit loaded by two memory frames. In PDP-11/70 installations, refer to Drawing E-AR-11/70-0-1 for exact connections.

2.4 MEMORY CONFIGURATION

Whenever memory capacity is expanded the following guidelines must be adhered to:

a. Before installing memory controller modules (M8147 or M8148 and M8149), ensure that the switches on the M8147 (or M8148) module are configured properly.

2. Lower addresses must be implemented in memory frames electrically closest to the bus master.

3. All interleaved memory frames must be closer to the bus master than noninterleaved memory frames.

4. When memory frames are interleaved, the memory frames must be physically and electrically adjacent, with the memory frame containing "even" addresses closer to the bus master.

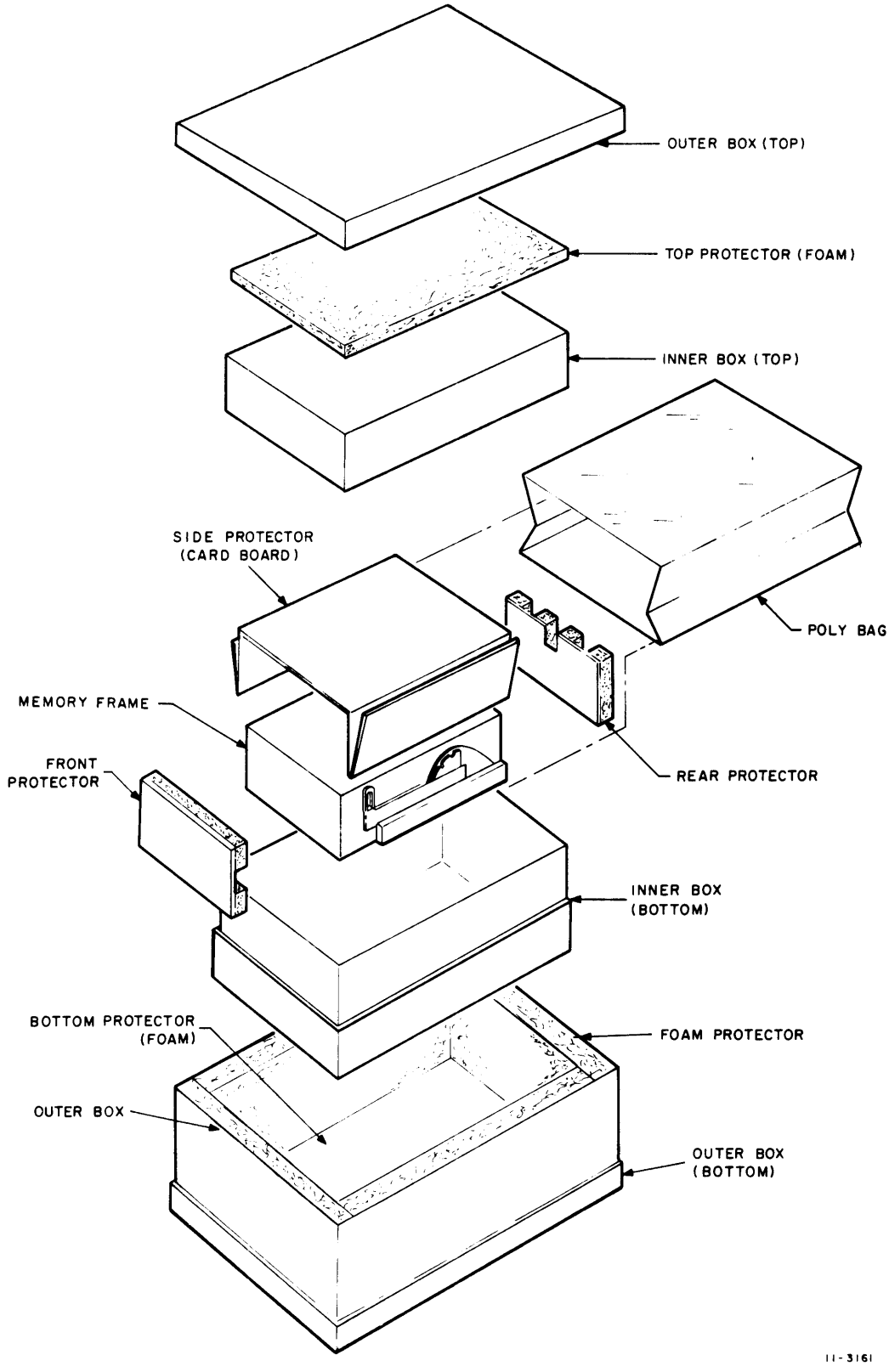


Figure 2-2 Memory Frame Packaging

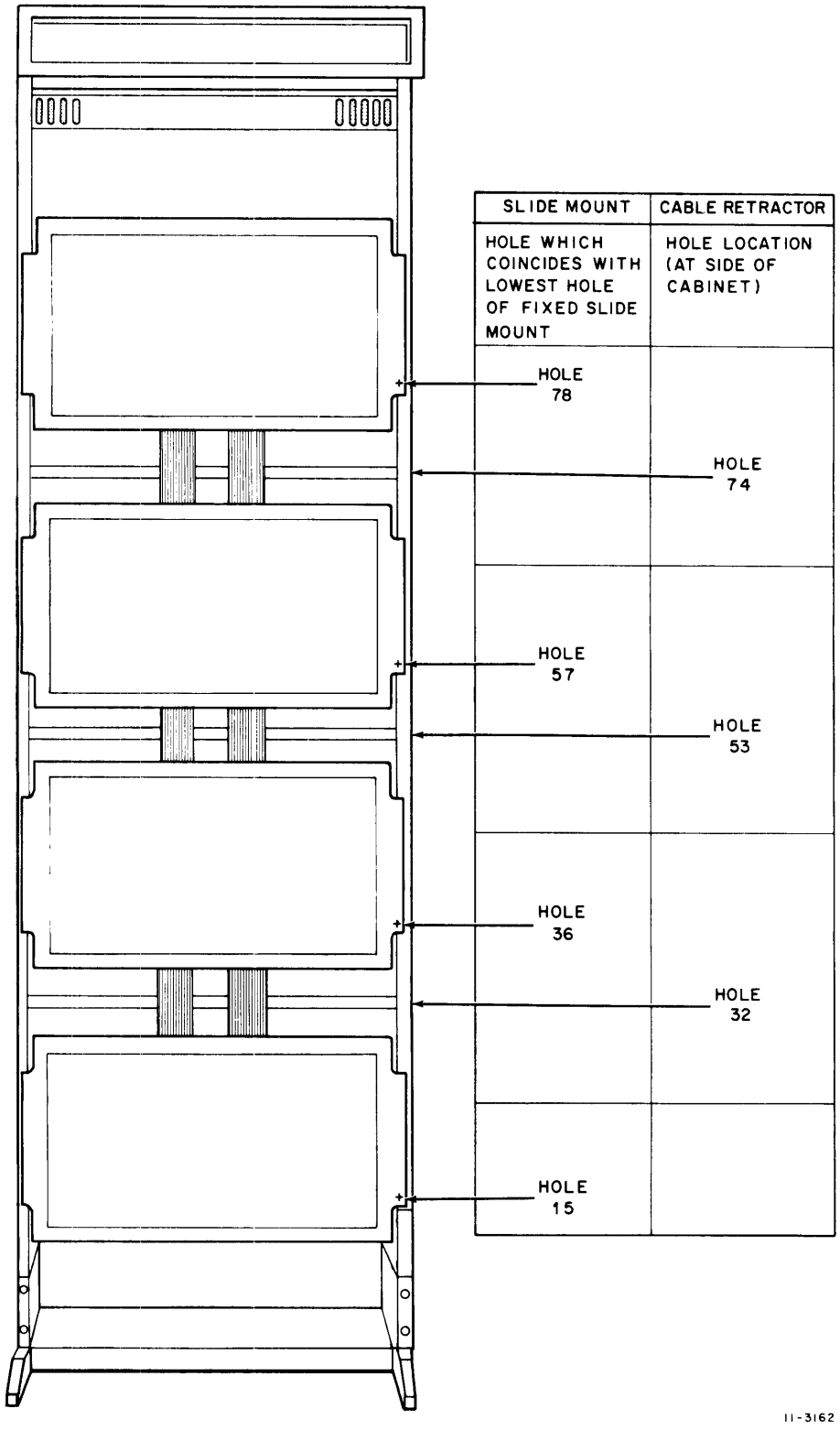


Figure 2-3 Memory Frame and Cable Retractor Mounting

5. Care should be taken that modules are installed in their designated slots, as indicated in the module utilization diagram (Figure 2-4).

NOTE

In the MJ11-A, stack 0 consists of two 16K word stacks: one 16K stack for the low word stack 0, and one 16K stack for the high word stack 0; likewise for stack 1, stack 2, and stack 3.

In the MJ11-B, stack 0 consists of two 32K word stacks: one 32K stack for the low word stack 0, and one 32K stack for the high word stack 0; likewise for stack 1, stack 2, and stack 3.

6. When memory capacity is increased within a memory frame, stack module set pairs are installed at the left- and right-hand side of the backplane, working toward the center. Thus the stack 3 (high and low word) modules are the last module sets added to a memory frame.

2.4.1 Adding 32K Stacks for System Up-Date

When 16K module sets are replaced with 32K module sets, two wires must be added to the MJ11 backplane (7010497) for each pair of 32K module sets installed. The additional wire to each set of the pair connects pin EJ1 of the G116 sense/inhibit module to EJ2 of the G236 driver module.

NOTE

Because the MJ11 provides parallel operation, installation of new module sets (of different stack size) must be done in pairs (i.e., changing the 16K low word stack 0 to 32K also requires changing the 16K high word stack 0 to 32K).

Once these wires are installed, the backplane modification is complete and 16K or 32K module sets may be used in these locations. (Note, contoller modification is explained below.) Recently manufactured MJ11 backplanes include an ECO (7010497 - 00004), which provides this modification.

The M8148 Timing and Control module must be replaced with the M8147 when replacing 16K module sets with 32K module sets. The M8147 Timing and Control module can handle 16K or 32K module sets.

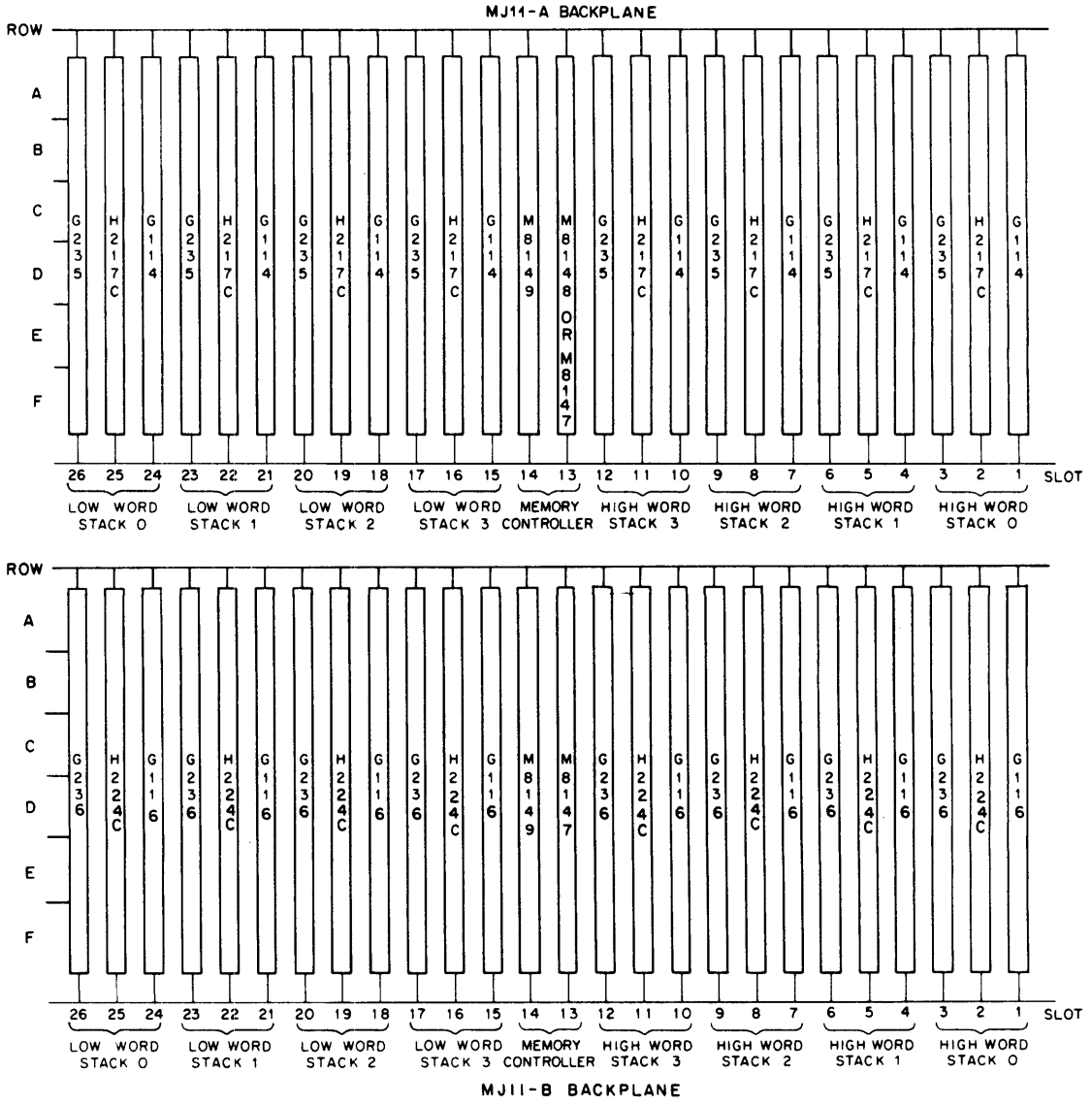
When 32K and 16K stacks (module set pairs) are mixed on the MJ11 backplane, the 16K stacks must occupy lower stack locations than the 32K stacks (i.e., for one 16K stack pair and one 32K stack pair, the 16K stacks must comprise stack 0 and the 32K stack pair must comprise stack 1). A configuration error will cause an LED to light on the M8147 module preventing any memory access.

2.4.2 Starting Address Switch Configuration

Switches S1-1 through S1-7, S2-1, and S2-2 on the M8147 (or M8148) module (Drawing MCTB) must be configured to represent the starting address of the memory controller. This is done by setting in the switches the binary number, which represents the total number of 16K blocks of 36-bit double words controlled by memory controllers having lower starting addresses.

A closed switch (set to ON) represents a logic 0. Switch S1-1 represents the LSB, and switch S2-2 the MSB.

The steps required to determine the starting address switch settings are shown in Figure 2-5 in flowchart form. Refer to Paragraph 2.4.4 for an example of switch configuration.



NOTE:

1. This figure illustrates a view as seen from the pin side (in a maintenance position with the power supply below the modules).
2. Stack 0 consists of two 16K word stacks (MJ11-A) or two 32K word stack (MJ11-B). Likewise for stack 1, stack 2, & stack 3.

11-4510

Figure 2-4 Module Utilization

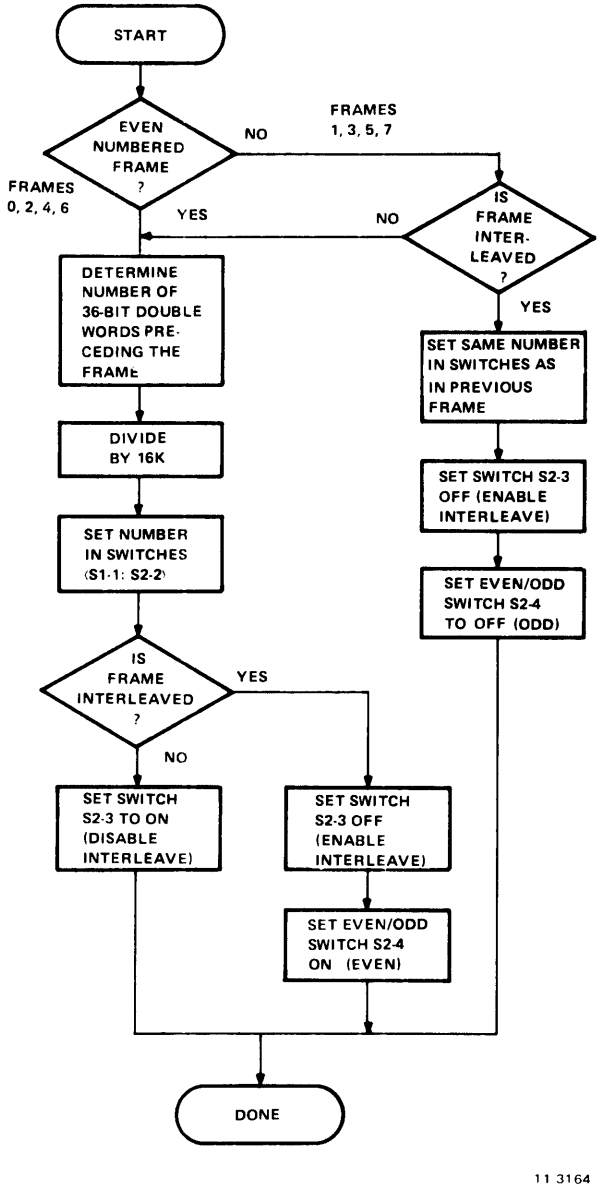


Figure 2-5 Procedure for Configuring M8147 (or M8148) Switches

2.4.3 Interleaving Switch Configuration

In an MJ11 Memory System, any two adjacent memory frames containing equal amounts of memory can be interleaved. Figure 2-6 illustrates stack interleaving variations in four examples with minimum memory. If interleaving is desired, switch S2-3 on the M8147 (or M8148) modules (Drawing MCTB) in both memory frames must be open (OFF). By convention, the memory controller located closer (electrically) to the bus master is required to respond to "even" addresses. Switch S2-4 in this controller must be open (OFF); switch S2-4 in the memory controller, which is further from the bus master, should be closed (ON).

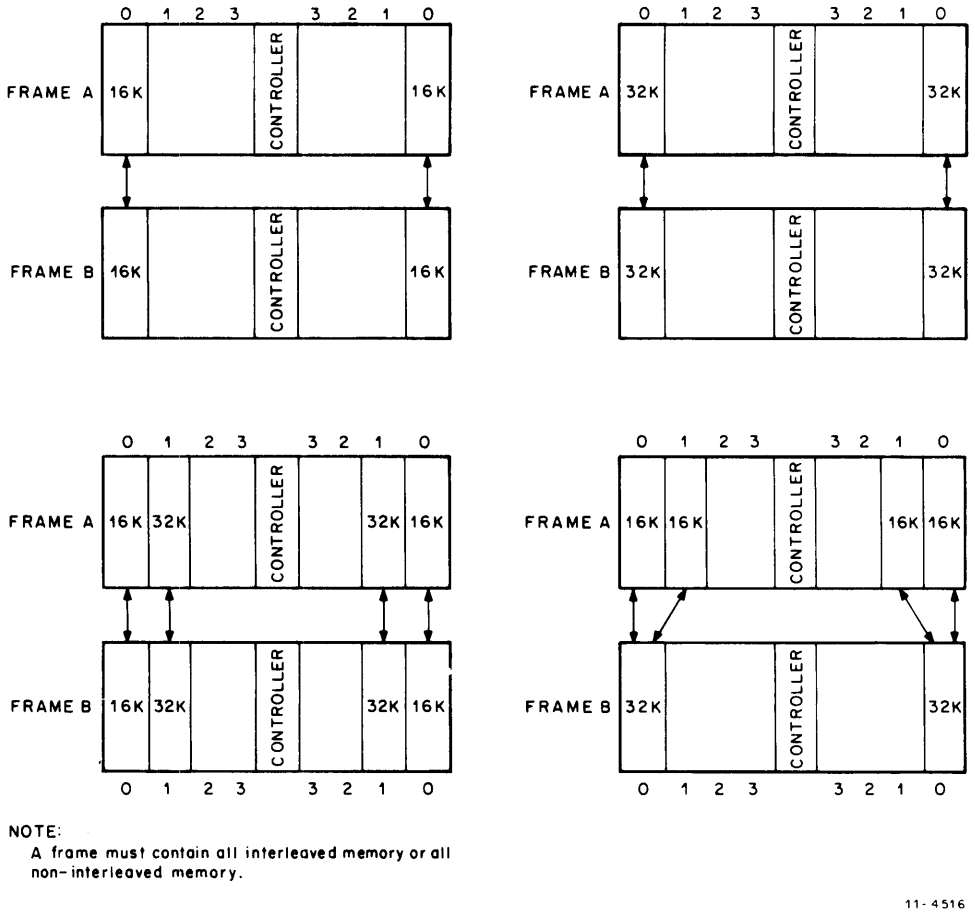


Figure 2-6 Examples of Stack Interleaving (with minimum number of stacks)

2.4.4 Switch Configuration Example

In a memory system consisting of three MJ11-A memory frames, assume that the first two frames (0 and 1) contain 128K of 18 bit words (i.e., 64K 36-bit double words), each, and that memory frame 2 contains 32K 18-bit words (i.e., 16K 36-bit double words). If memory frames 0 and 1 are interleaved, the memory frames are configured as follows:

Memory Frame 0 – Since no words precede this frame, 0÷16K = 0 is set into switches S1-1:S2-2 (i.e., all 9 switches are set to ON). Switch S2-3 is set for interleaved operation (OFF) and Switch S2-4 is set for even addresses (OFF).

Memory Frame 1 – Since this frame and frame 0 are interleaved, the starting address switches are configured as in memory frame 0. Switch S2-3 is set for interleaved operation (OFF) and switch S2-4 is set for odd addresses (ON).

Memory Frame 2 – Since frames 0 and 1 contain a total of 128K 36-bit double words, 128K÷16K = 8_{10} = 10_8 = 000001000_2 is set into switches S1-2:S2-2 (i.e., S1-4 is set to OFF while the remaining switches are set ON). Switch S2-3 is set to ON to disable interleaving. With interleaving disabled, the state of switch S2-4 is irrelevant.

2.5 MAIN MEMORY BUS CABLING

1. Remove the M8147 (or M8148) and M8149 modules comprising the last memory controller on the Main Memory Bus.
2. Remove the H873 bus terminator from J2 and J4 on each module.
3. Install the address cable assembly 7010824-1 in connectors J2 and J4 of the M8147 (or M8148) module.
4. Install the data cable assembly 7010824-0 in connectors J2 and J4 of the M8149 module.
5. Replace the modules in their proper backplane slots.
6. Route the Main Memory Bus cables as shown in Figures 2-7 and 2-8. Ensure that the cables do not obstruct the air vents at the rear of the memory frame. Connect the cables to J1 and J3 on the M8147 (or M8148) and M8149 modules, of the memory frame being installed.
7. Insert the Main Memory Bus terminators in connectors J2 and J4 of the M8147 (or M8148) and M8149 modules that are last on the Main Memory Bus.
8. Install the modules in their proper backplane slots.
9. Secure the bus cables by tightening the cable clamps.

2.6 VOLTAGE CHECKS

After installation has been completed, check regulator voltage outputs in all the memory frames (Paragraph 7.3.2 in the *MJ11 Memory System Maintenance Manual*). Perform voltage adjustments (Paragrah 7.4.3) if necessary.

2.7 MEMORY EXPANSION IN THE PDP-11/70

Prior to installation verification, the PDP-11/70 System Size register must be reconfigured to represent the new memory size. Refer to Drawing D-CS-M8140-0-1, sheet SCCN in the PDP-11/70 Engineering Drawings, and to the *PDP-11/70 Installation and Maintenance Manual* for the procedure.

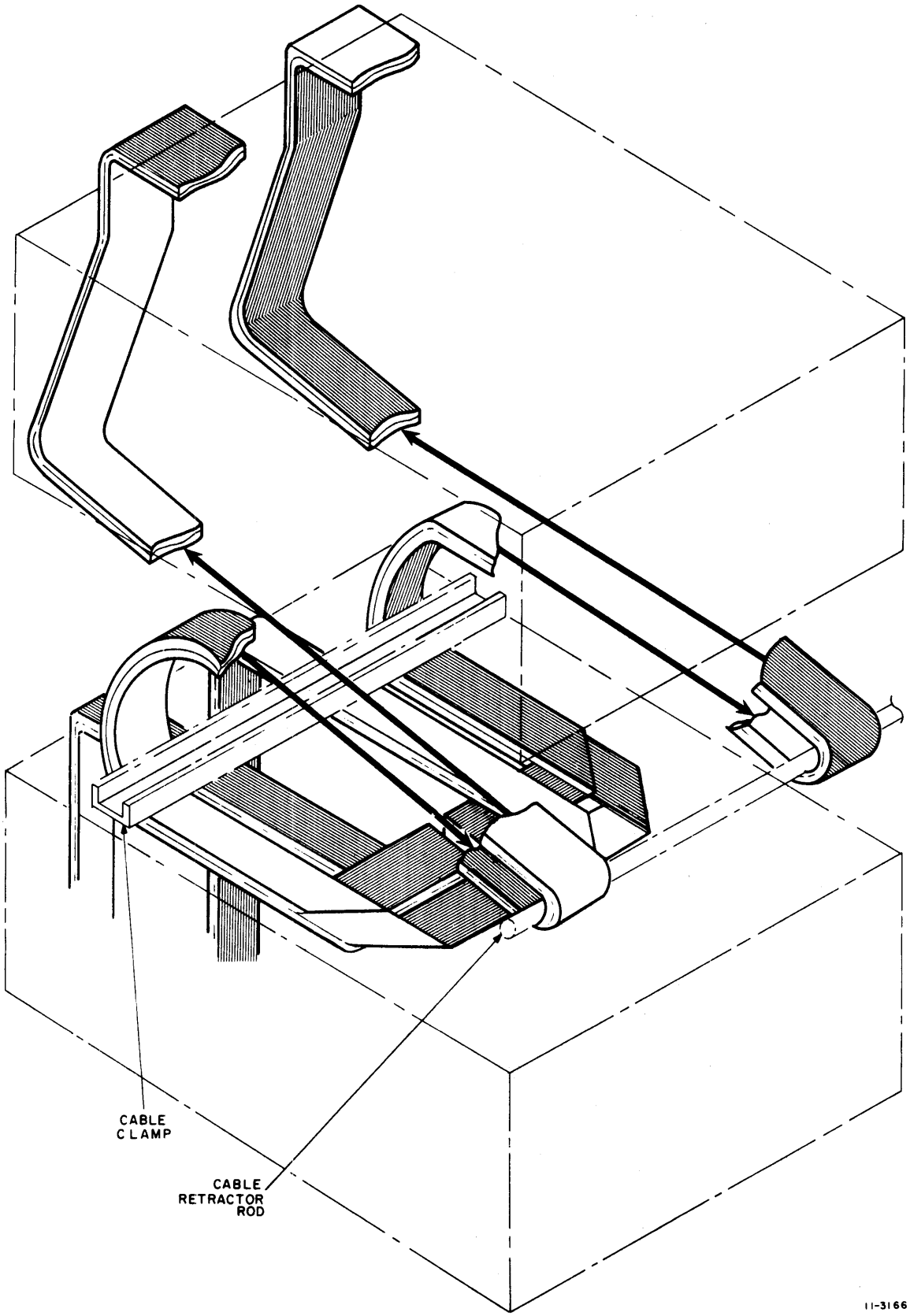


Figure 2-7 Typical Cable Routing

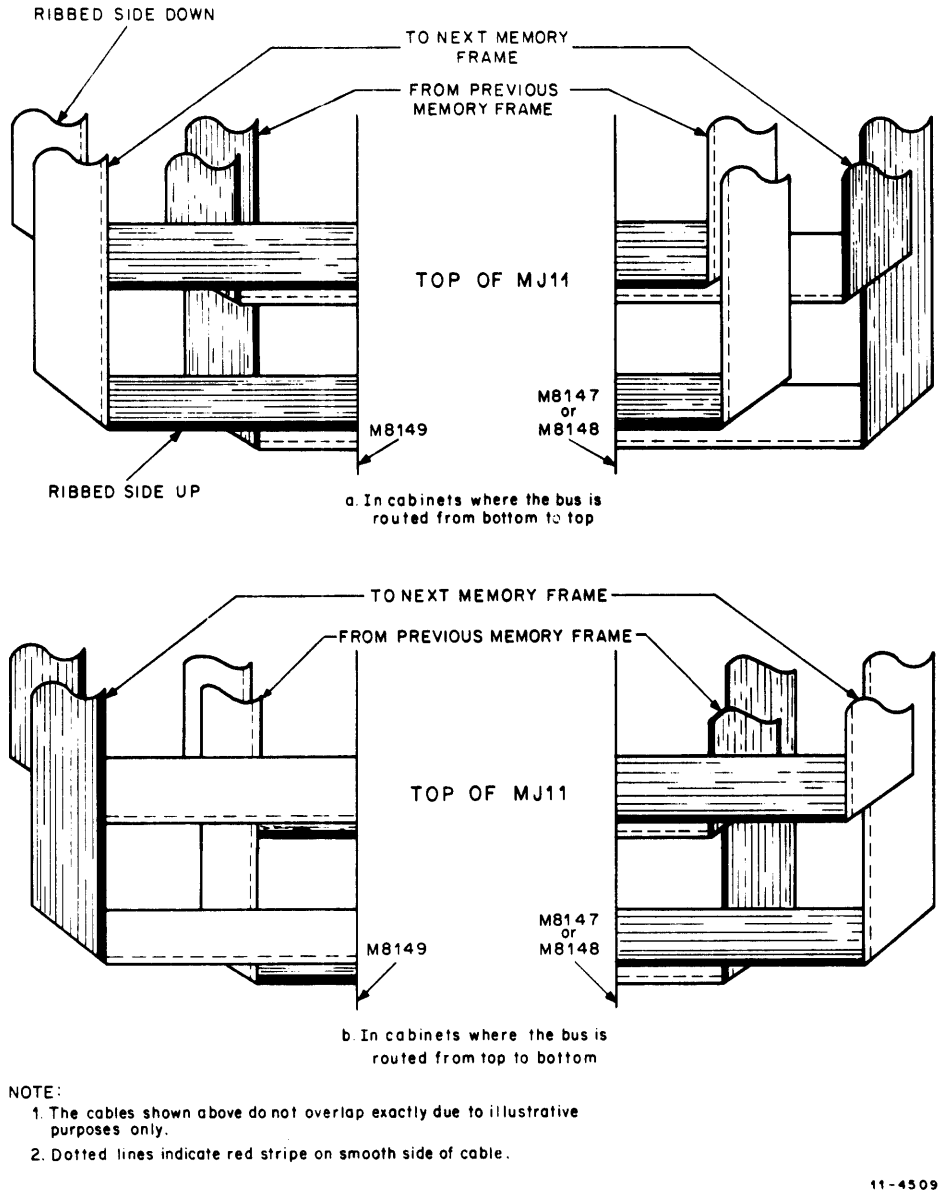


Figure 2-8 Main Memory Bus Cable Routing

2.8 INSTALLATION CERTIFICATION

Run the memory diagnostic to ensure that the equipment operates correctly and that the installation has been performed properly. Running the diagnostic also ensures that correct parity is present in all memory locations prior to turning the system over to the customer. Consult the documentation supplied with the diagnostic for loading, control, and printout interpretation information.

Reader's Comments

MJ11 Memory System
User's Manual
(16K and 32K Core)

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