

PDP-11/70 HARDWARE
STUDENT HANDOUTS

PDP-11/70 PROCESSOR MAINTENANCE
COURSE OUTLINE

DAY 1

- I. Introduction
- II. PDP-11/70 System Description
 - A. System Components
 - B. Physical Configuration
 - C. PDP-11/70 Addressing Space
- III. KB11-B Block Diagram
 - A. Data Paths Block Diagram
 - B. Control Block Diagram
- IV. KB11-B Timing
 - A. Basic Timing
 - B. Pause Timing

References: KB11-B Processor Manual Sec. I Ch. 1, Sec. II pp 1-1 to 1-6, pp 2-1 to 2-3, Ch. 4.

Reading Assignment: KB11-B Processor Manual Sec. I Ch. 1, Sec. II, Ch.4.

DAY 2

V. Control ROM

- A. RAR and RBR Timing
- B. Address Calculation
 - 1. Fork
 - 2. Branch

VI. Flow Diagram Concepts

- A. Symbology
- B. Correlation to ROM Map and Block Diagram

VII. Control Console

- A. Flows
- B. Logic

VIII. Load Address Operation

References: KB11-B Processor Manual Sec. II Para. 1.2 to 1.2.3,
Para. 1.4 to 1.4.8, Sec. III Para. 2.1 to 2.5.2.

Reading Assignment: KB11-B Processor Manual Sec. II Para. 1.2.1,
1.4 to 1.4.4.

DAY 3

- IX. Register Deposit/Deposit Step Operation
 - A. General Register Selection
- X. Register Examine/Examine Step Operation
- XI. Examine and Examine Step Operation
 - A. Unibus Data Transfers
- XII. Deposit and Deposit Step Operation
- XIII. Start Operation
- XIV. Troubleshooting Laboratory

References: KB11-B Processor Manual Sec. II Para. 2.1.4, Ch. 5,
Sec. III, Para 2.5 to 2.12

Reading Assignment: KB11-B Processor Manual Sec. II Ch. 5, Sec. III
Para. 2.7.3.

DAY 4.

XV. Condition Code Instructions

- A. Flows
- B. Logic

XVI. Branch Instructions

- A. Flows
- B. Logic

XVII. Single Operand Instructions

- A. No Memory Reference
- B. Destination Operand Acquisition

XVIII. Troubleshooting Laboratory

References: KB11-B Processor Manual Sec. II, Para.1.4.6.1 to 1.5.8.

Reading Assignment: KB-11-B Processor Manual Sec. II Para.1.4.6.1 to 1.5.8.

DAY 5

XIX. Double Operand Instructions

XX. Register Instructions

A. ASH

B. ASHC

XXI. Troubleshooting Laboratory

References: KB11-B Processor Manual Sec. II Para. 1.2.5.7, 2.1.5 to 2.1.8.

Reading Assignment: KB11-B Processor Manual Sec. II Para. 2.1.5 to 2.1.8.

DAY 6

XXII. Register Instructions (continued)

A. MUL

B. DIV

XXIII. Trap and Subroutine Operations

A. JMP and JSR

B. RTS

C. TRAP

D. RTI and RTT

E. PSW Logic

References: KB11-B Processor Manual Sec. II Para. 1.2.5.8, 1.2.5.9.,
3.9 to 3.9.10.

Reading Assignment: KB11-B Processor Manual Sec. II Para. 1.2.5.8.,
1.2.5.9, 3.9 to 3.9.10.

DAY 7

XXIV. BRQ Operations

- A. Service Flows
- B. Interrupts and Traps
- C. Power Up and Power Down

XXV. Troubleshooting Laboratory

References: KB11-B Processor Manual Sec. II Ch. 6.

Reading Assignment: KB11-B Processor Manual Sec. II Ch. 6.

DAY 8

- XXVI. Cache Concepts
- XXVII. Block Diagram
 - A. Address Logic
 - B. Data Logic
- XXVIII. Program Example
- XXIX. Cache Logic
 - A. Timing
 - B. Power Up - Initialization
 - C. Request Arbitrator
 - D. Cache Registers
- XXX. Troubleshooting Laboratory

References: KB11-B Processor Manual Sec. VI Ch. 1, 2, Para. 4.3 to 4.8.8.

Reading Assignment: KB11-B Processor Manual Sec. VI Ch. 1, Para. 2.1 to 2.2.3.6, 4.3 to 4.5.

DAY 9

XXXI. Cache Operations

- A. Read Hit
 - 1. Processor
 - 2. Unibus Map
- B. Processor Bust - Bend Cycle
- C. Read Miss
 - 1. Processor
 - 2. Unibus Map
- D. Write
 - 1. Processor
 - 2. Unibus Map
- E. Register Read and Write

XXXII. Troubleshooting Laboratory

References: KB11-B Processor Manual Sec. VI Para. 3.8 to 3.8.8.

Reading Assignment: KB11-B Processor Manual Sec. VI Para. 3.8 to 3.8.8

DAY 10

XXXIII. Memory Management

- A. Relocation
- B. Protection
- C. Multiple Modes
- D. Statistical Information

XXXIV. Memory Management Timing

XXXV. ROM Control

References: KB11-B Processor Manual Sec. IV Ch. 1, Para 2.1,
2.2, 3.1, 3.2; Ch. 6.

Reading Assignment: KB11-B Processor Manual Sec. IV Ch. 1., 6.

DAY 11

- XXXVI. Memory Management Relocation Logic
 - A. Selection of K, S, U Space
 - B. Selection of I, D Space
 - C. Generation of Physical Address
- XXXVII. Memory Management Protection Logic
 - A. Selection of a PDR
 - B. Memory Management Trap Logic
 - C. Memory Management Abort Logic
- XXXVIII. Troubleshooting Laboratory

References: KB11-B Processor Manual Sec. IV Ch. 3,4,5,8.

Reading Assignment: KB11-B Processor Manual Sec. IV Ch. 3,4,5,8.

DAY 12

XXXIX. Memory Management Internal Register Logic

A. PDR A and W Bit Operation

XXXX. MTP, MFP Instruction Execution

XXXXI. Unibus Map

A. Block Diagram

B. Operation

XXXXII. Troubleshooting Laboratory

References: KB11-B Processor Manual Sec. IV Ch. 7, 9, Sec. V Ch. 1.

Reading Assignment: KB11-B Processor Manual Sec. IV Ch. 7, 9, Sec. V, Ch. 1.

DAY 13

XXXXIII. Unibus Map Logic

- A. Cache/Unibus Transactions
- B. Register Operations

XXXXIV. Troubleshooting Laboratory

References: KB11-B Processor Manual Sec. V Ch. 2,3.

Reading Assignment: KB11-B Processor Manual Sec. V Ch. 2,3.

Day 14

XXXXV. MJ11 Core Memory

- A. 3 Wire Memory Operation
- B. MJ11 Operations
 - 1. Read
 - 2. Write
 - 3. Exchange
- C. MJ11 Configuration
 - 1. Block Diagram
 - 2. Memory Controller
 - 3. Internal Bus
 - 4. Stack Module Set
- D. Main Memory Bus
 - 1. Description
 - 2. Bus Protocol
- E. Memory Timing Control Signals

XXXXVI.. Troubleshooting Laboratory

References: MJ11 Memory System Maintenance Manual: Ch. 1, 2,
Para. 3.1 to 3.5.

Reading Assignment: MJ11 Memory System Maintenance Manual: Ch. 1,
Para. 3.1 to 3.5.

DAY 15

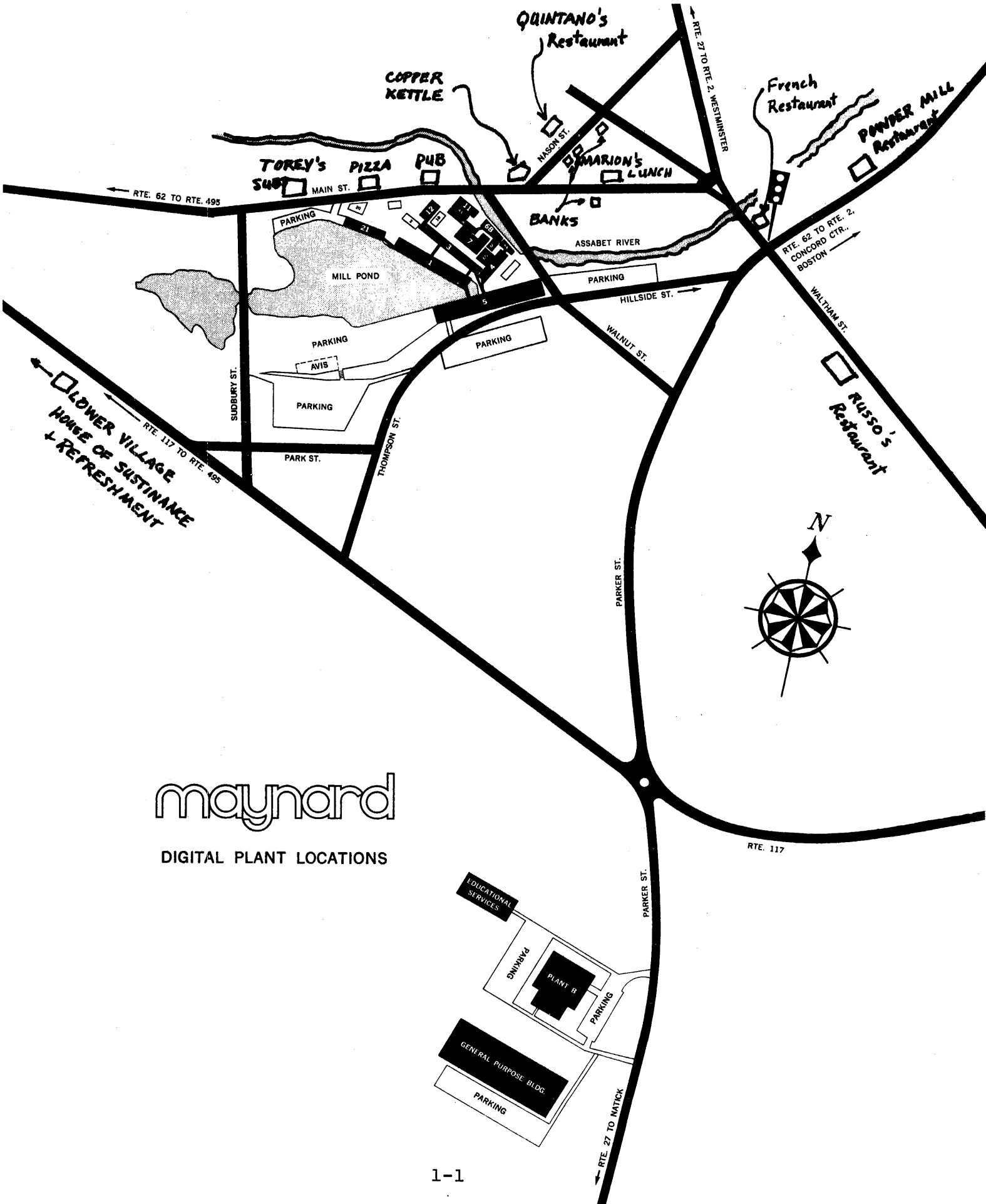
XXXXVII. MJ11 Stack Module Set

- A. Organization
- B. Logic Operation
- C. Example

XXXXVIII. Troubleshooting Laboratory

References: MJ11 Memory System Maintenance Manual: Ch. 4.

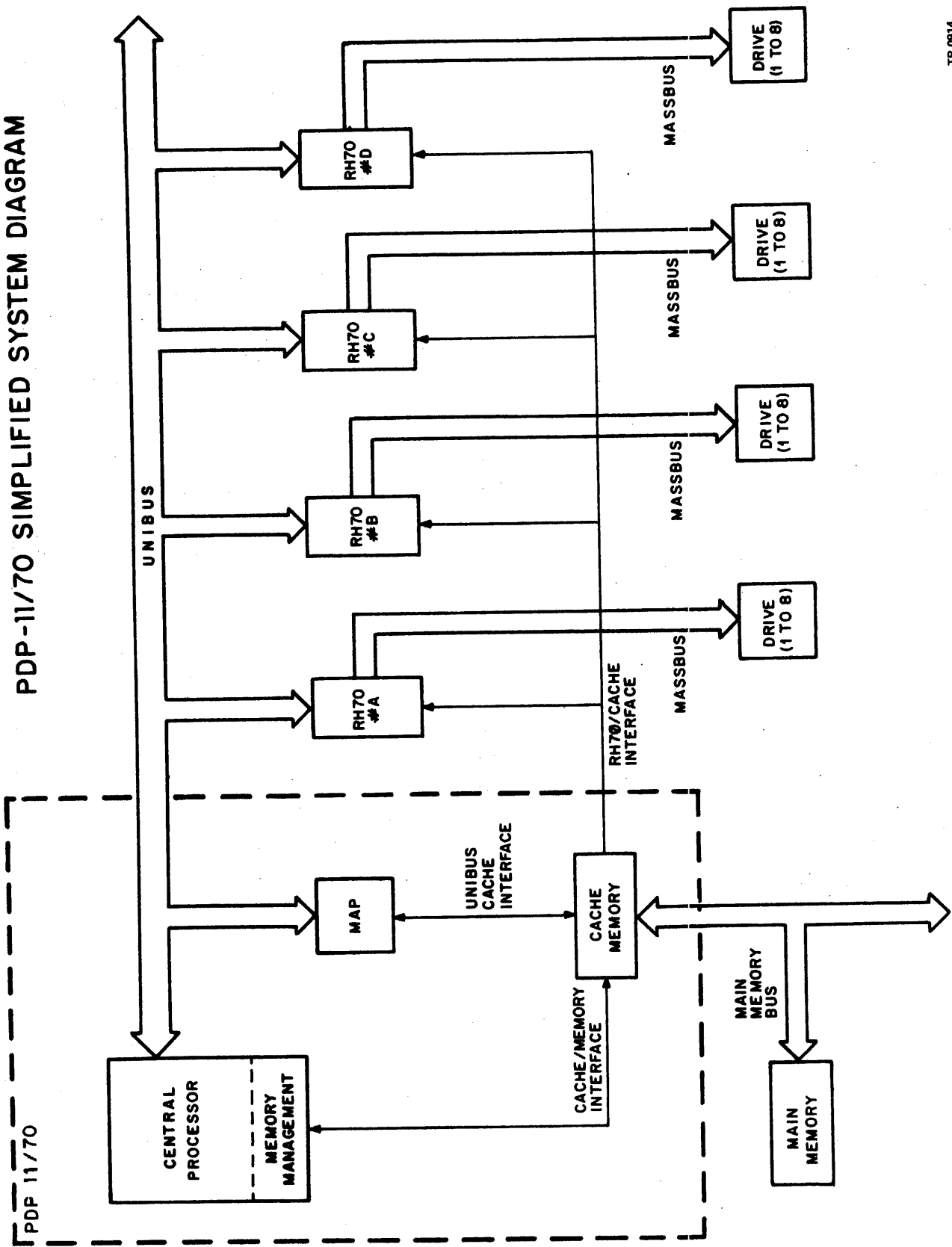
Reading Assignment: MJ11 Memory System Maintenance Manual: Ch. 4.



maynard

DIGITAL PLANT LOCATIONS

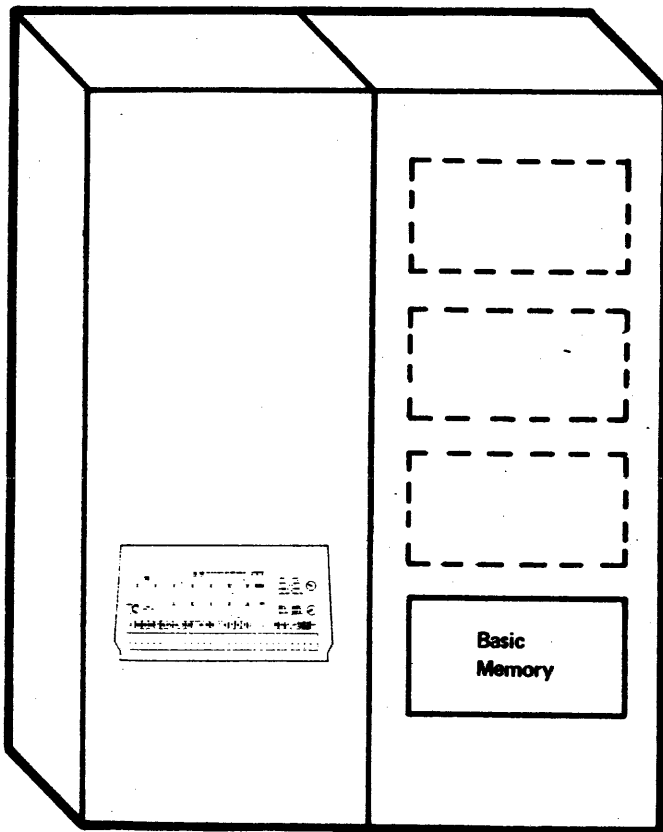
PDP-11/70 SIMPLIFIED SYSTEM DIAGRAM



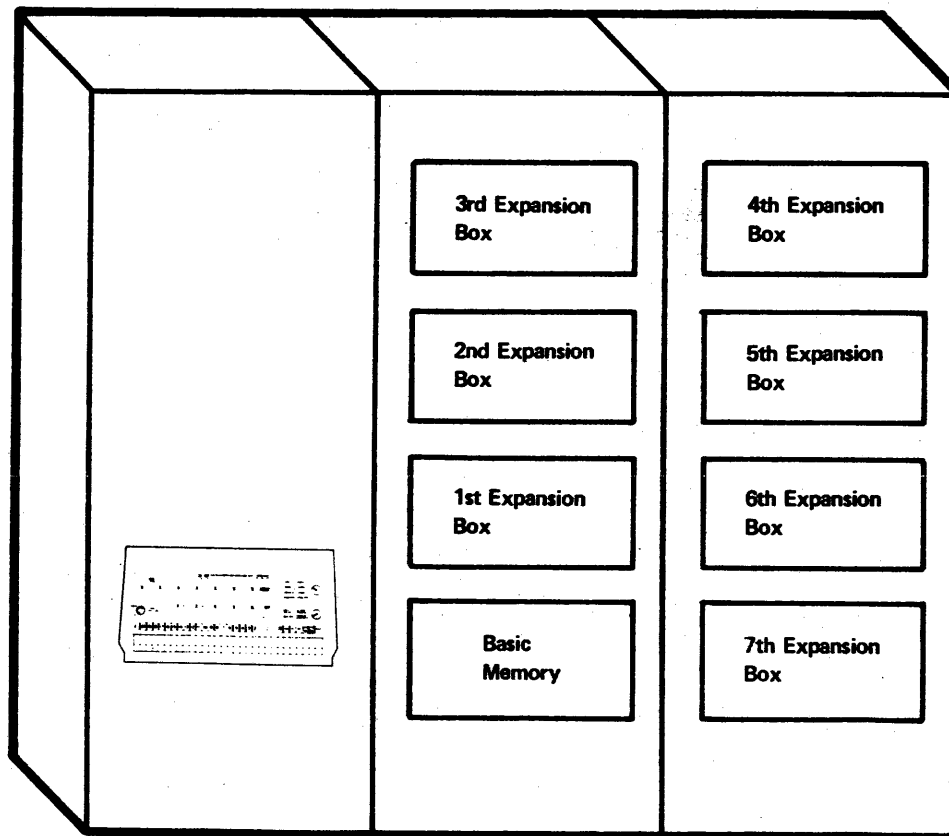
TR-0914

PDP-11/70 MJ11 MEMORY OPTIONS

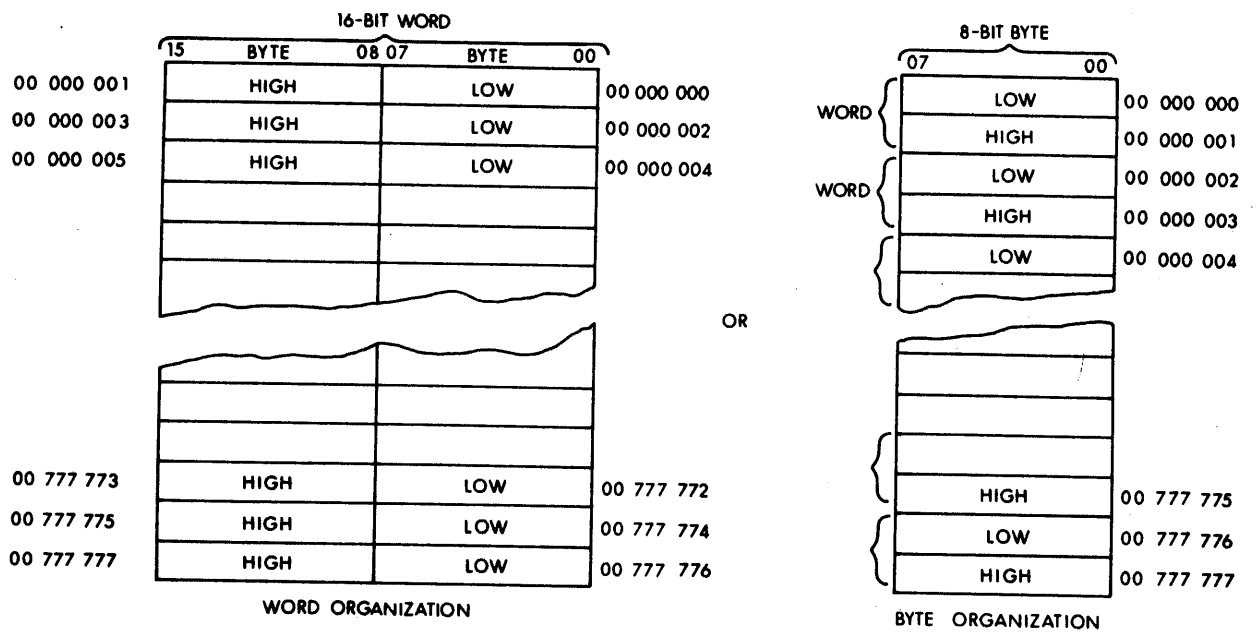
1-3



Minimum Configuration
 CPU Cabinet with CPU
 1 Memory Cabinet
 1 Memory Box with
 Controller and Transceiver
 64K words



Maximum Configuration
 CPU Cabinet with CPU
 2 Memory Cabinets
 8 Memory Boxes with Controller
 and Transceiver in each box
 1024K words



11-3195

Figure 1-5 Word and Byte Addresses

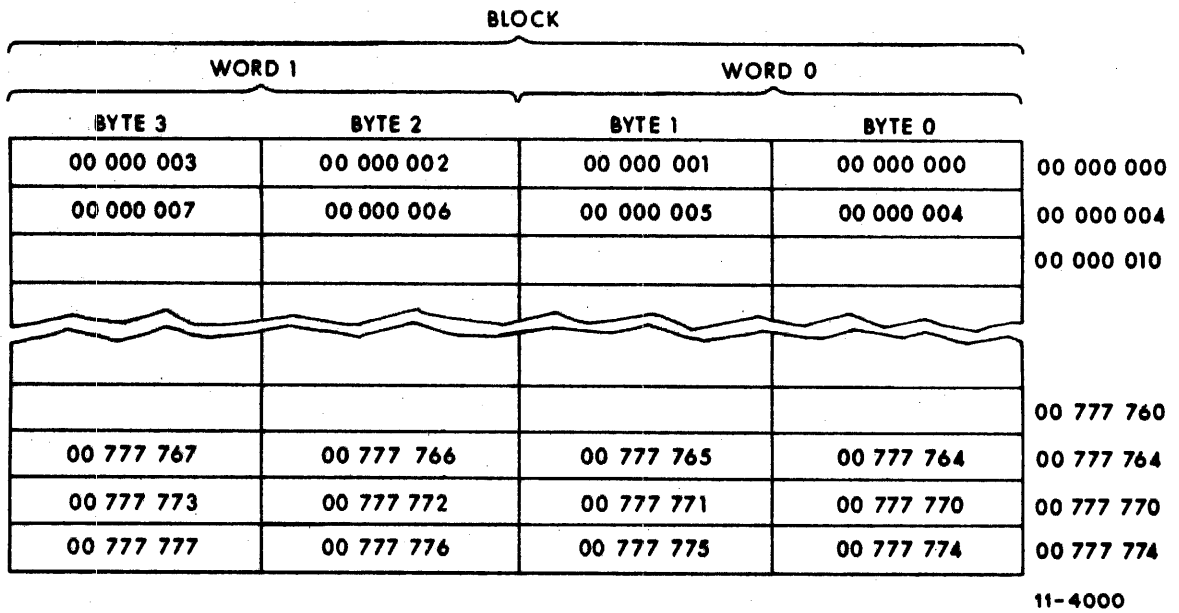
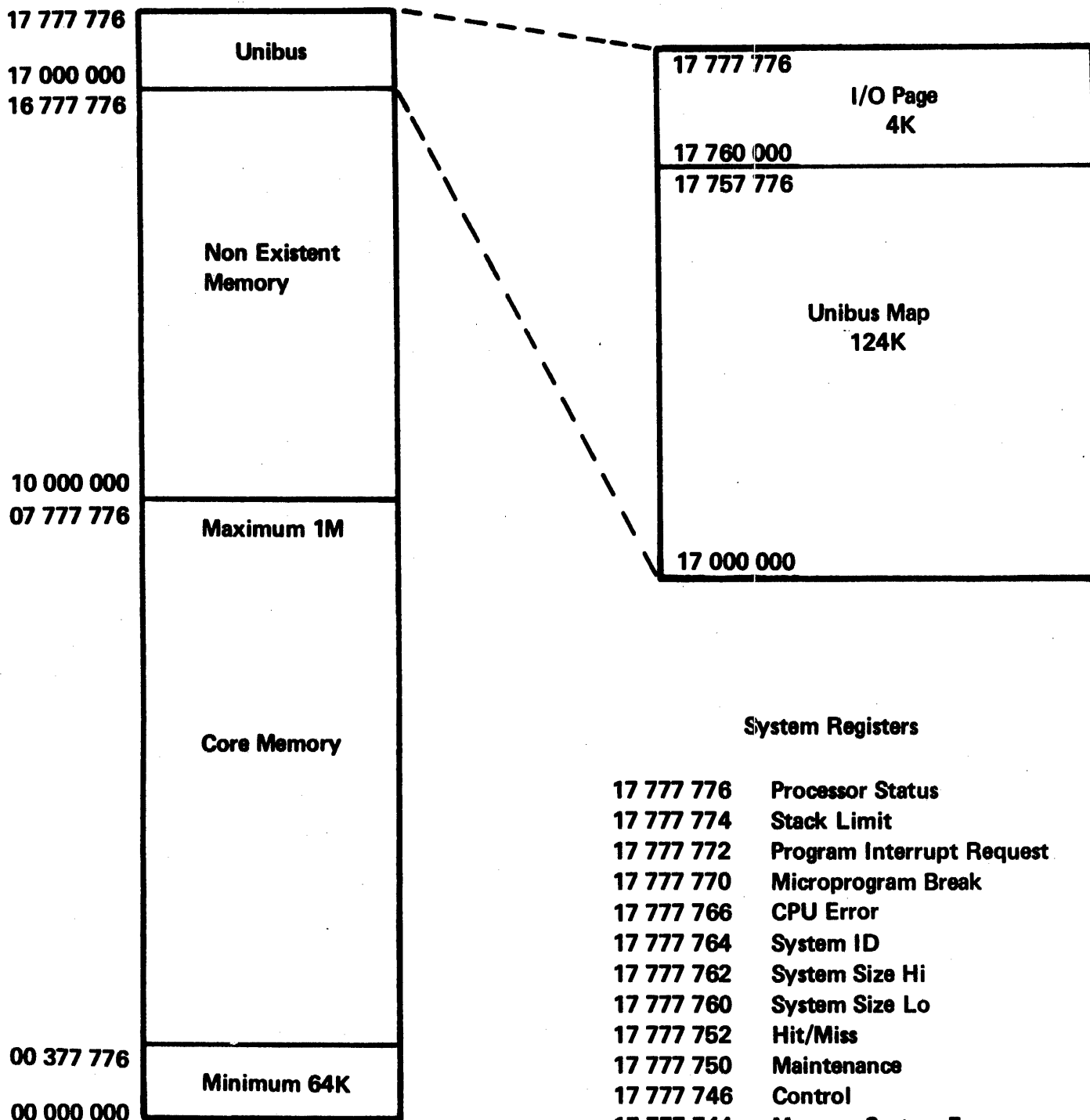
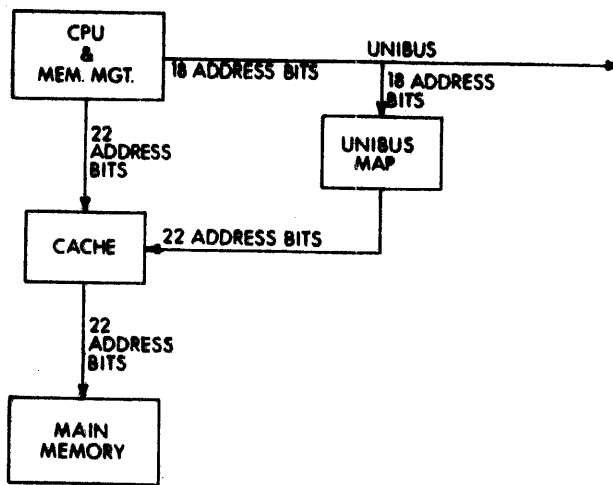


Figure 1-6 Main Memory Addresses

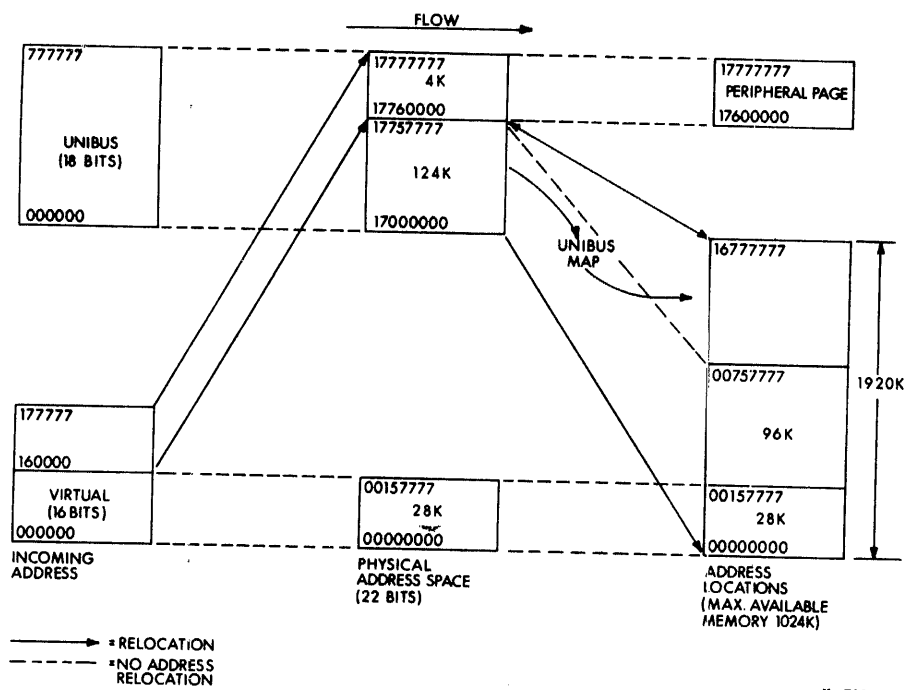
PDP-11/70 SYSTEM ADDRESS





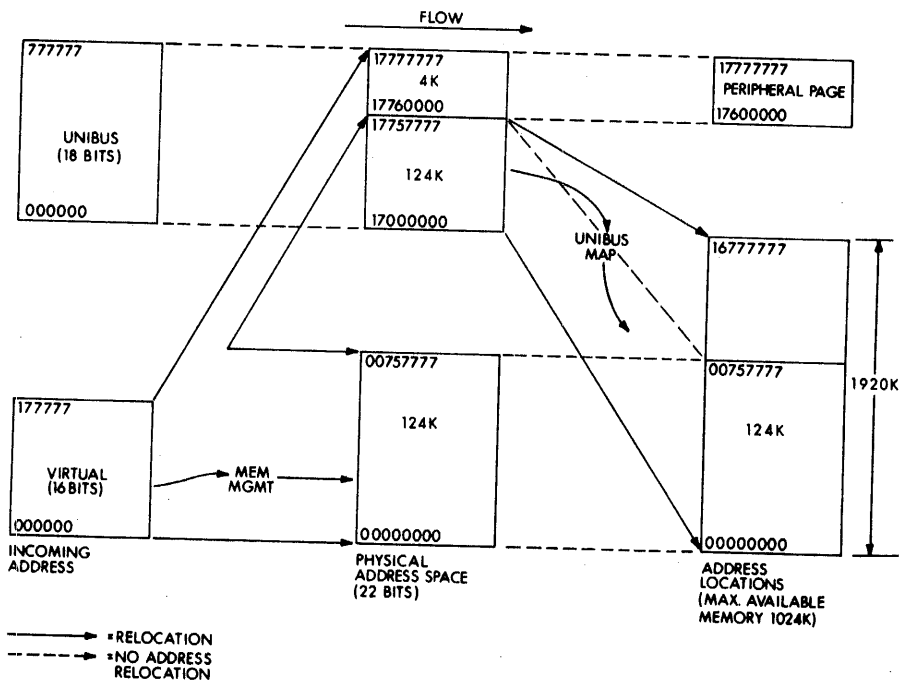
11-4001

Figure 1-7 Address Paths



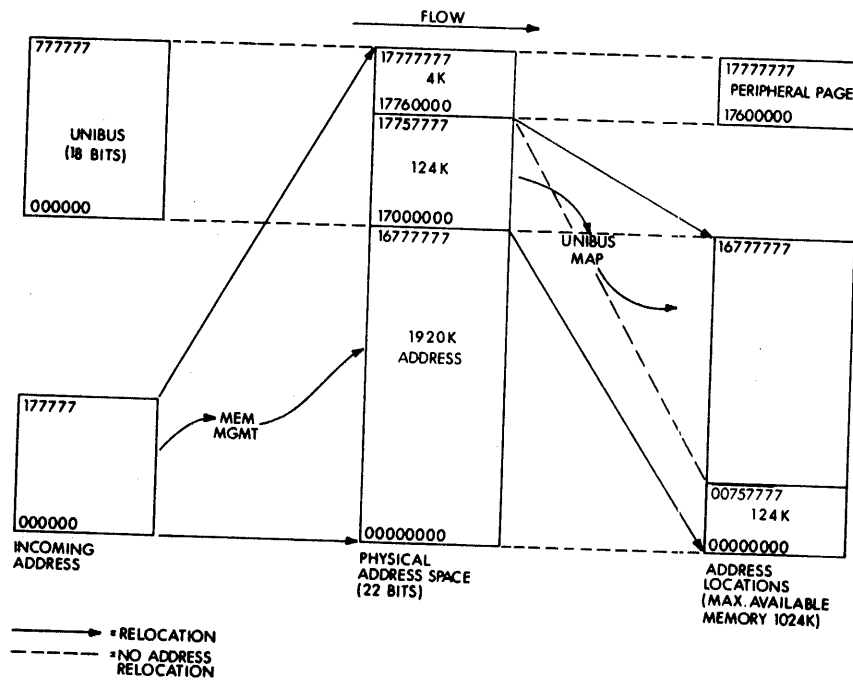
11-3196

Figure 1-9 16-Bit Mapping



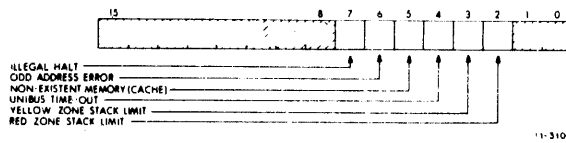
11-3197

Figure 1-10 18-Bit Mapping



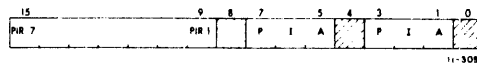
11-3198

Figure 1-11 22-Bit Mapping



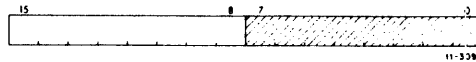
(TMCD) 17 777 766

Figure 3-1 CPU Error Register



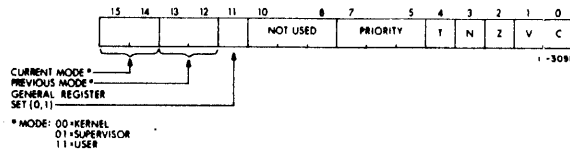
(PDRD) 17 777 772

Figure 3-2 Program Interrupt Register



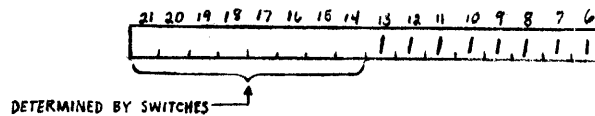
(PDRD) 17 777 774

Figure 3-3 Stack Limit Register



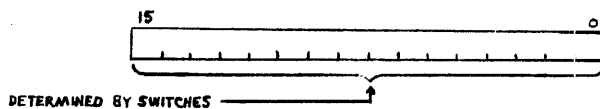
(IRCH, PDRD)
17 777 776

Figure 3-4 Processor Status Word



Lower Size Register

(SCCN) 17 777 760



System ID Register

(SCCN) 17 777 764

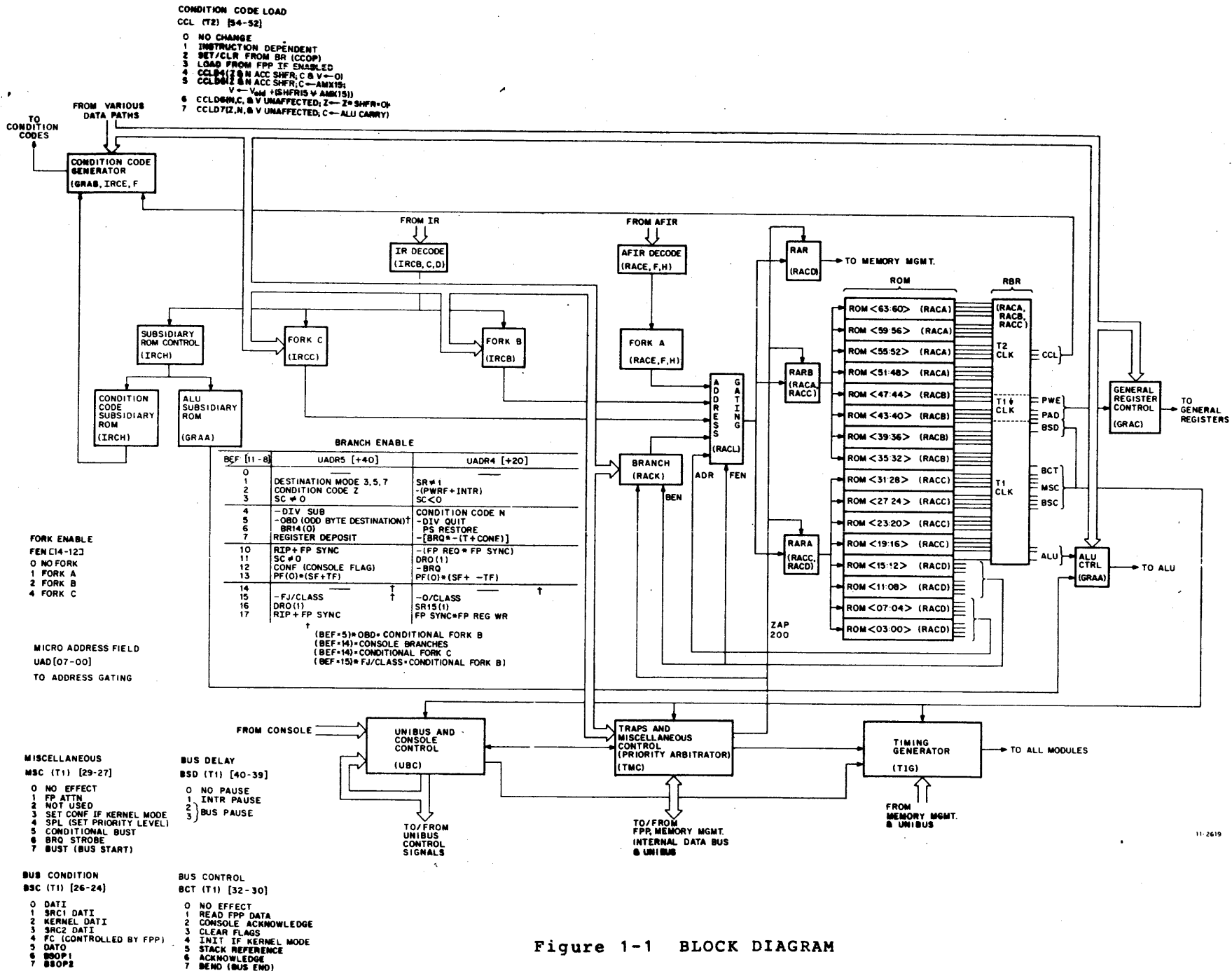
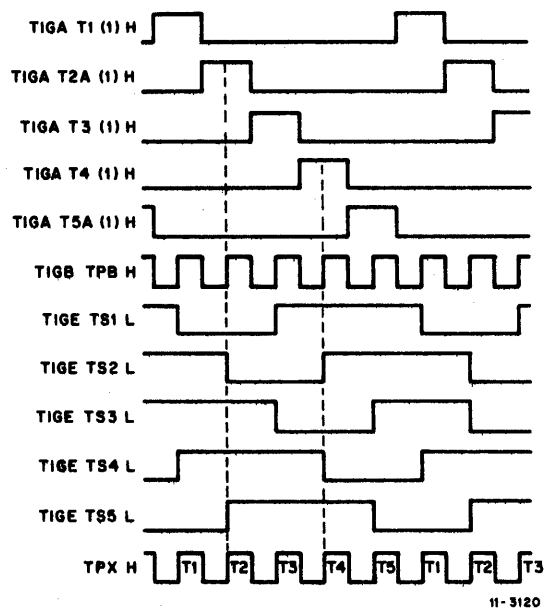


Figure 1-1 BLOCK DIAGRAM



11-3120

Figure 4-6 Time States

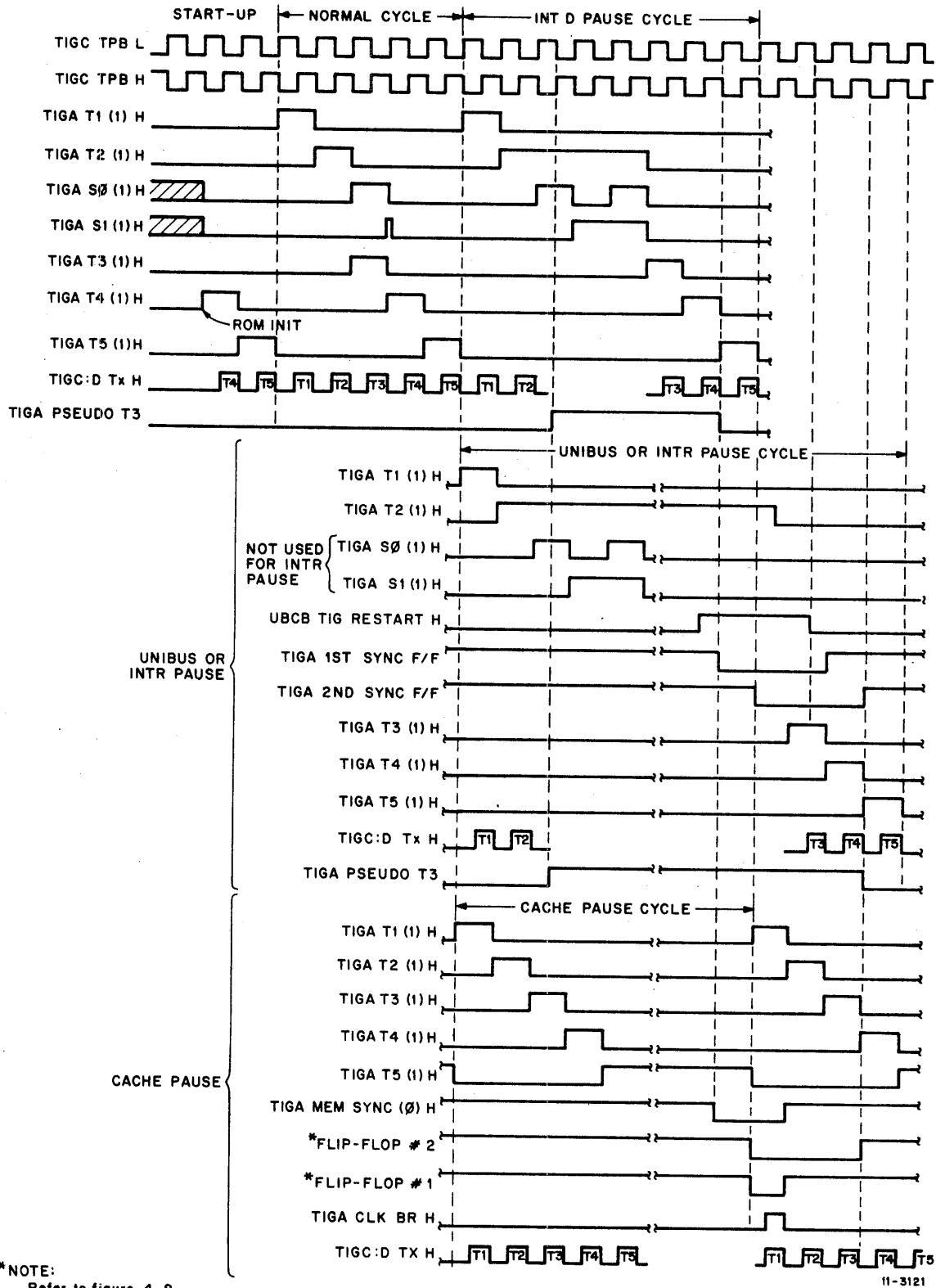
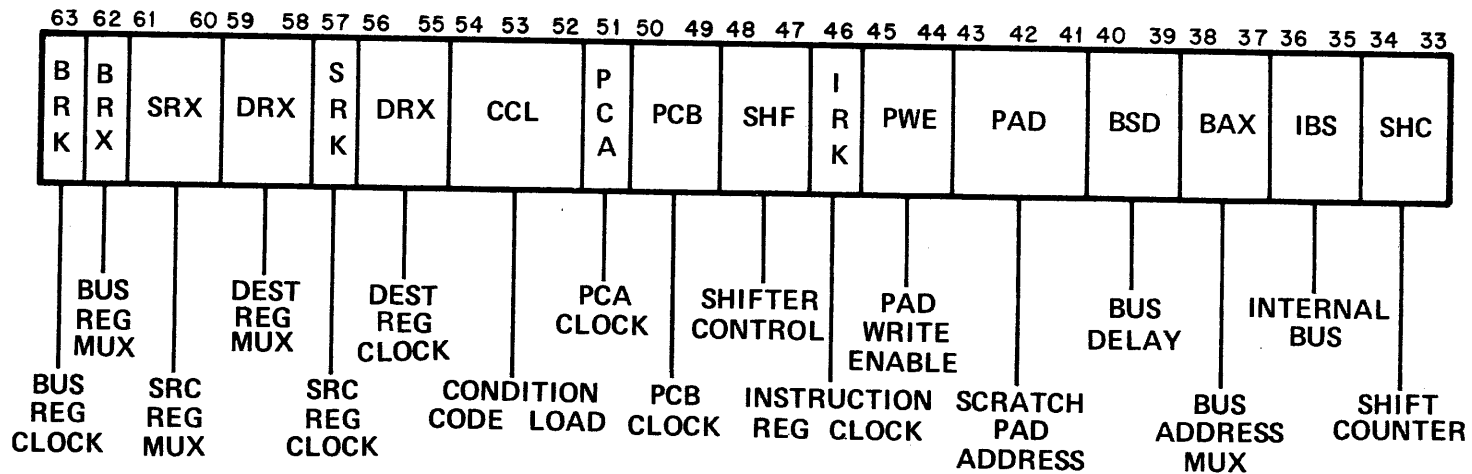
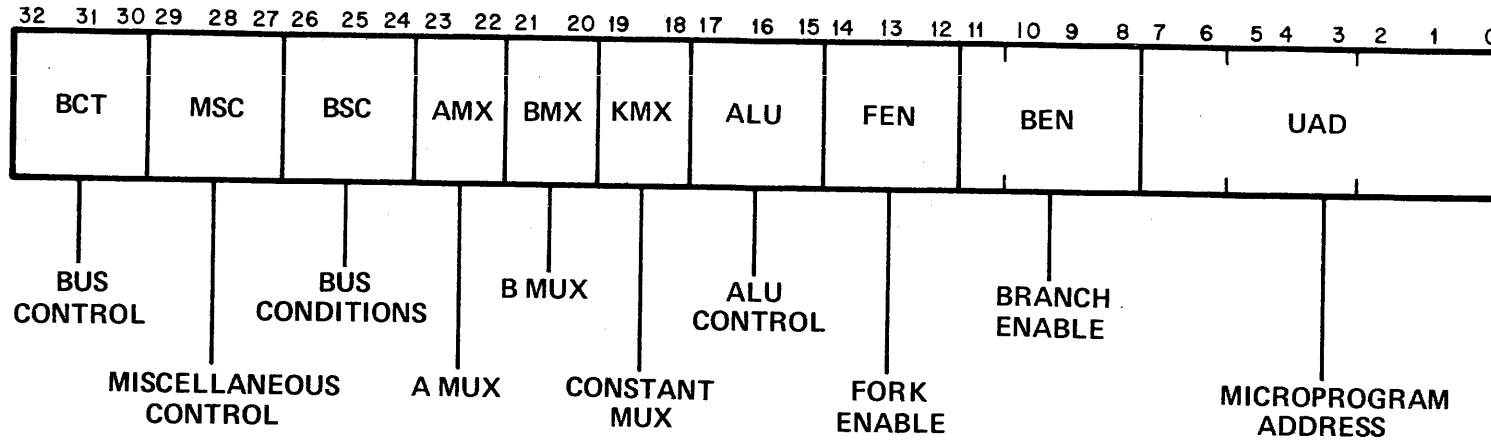


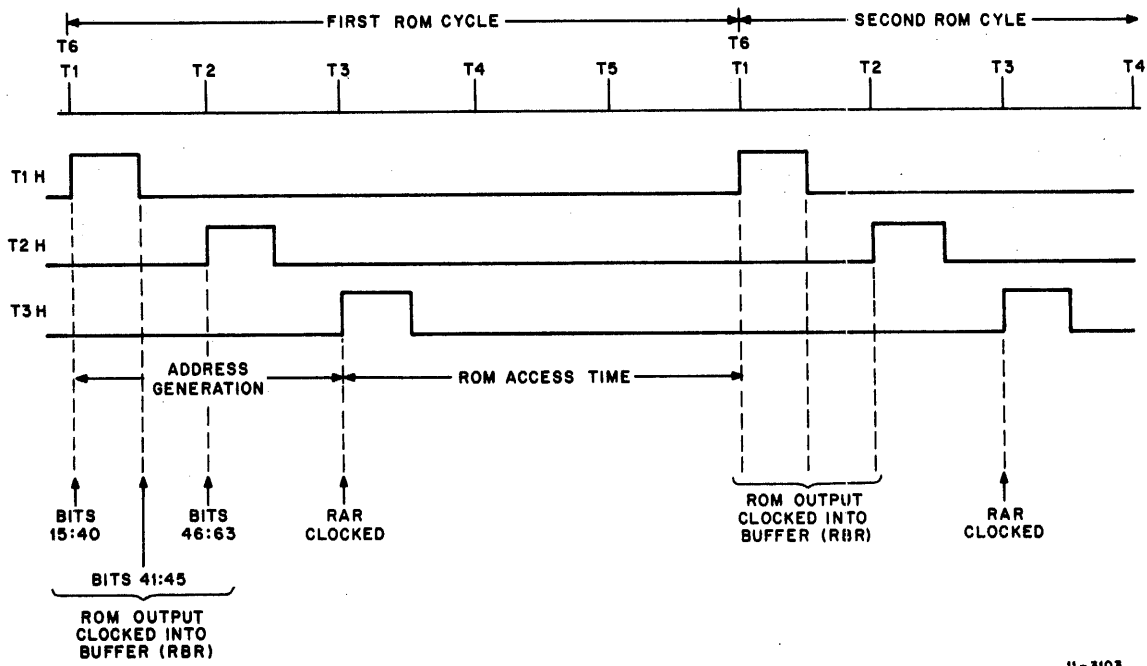
Figure 4-7 Timing Generator & Pauses

**Table 4-1
Ring Counter Stop and Pause Conditions**

STOP IN T2		
Internal Bus Pause	Stop:	SAPN NOT CACHE ADRS H TIGA PAUSE H (UBSD = 2 or 3) TIGA S0 (0) H or TIGA S1 (0) H
	Restart:	S0 and S1 count to 3 (90 ns).
Unibus Pause CPU Control Registers	Stop:	Same as Internal Bus Pause
	Restart:	Same as Internal Bus AND UBCB TIG RESTART H (BUS SSYN)
Interrupt Pause	Stop:	UBSD = 1 (INTR Pause) UBCD EXT BRQ H
	Restart:	UBCB TIG RESTART H (Passive Release or BUS INTR)
Single ROM Cycle	Stop:	TIGB ROM+UPB (1) H
	Restart:	CONTINUE or MAINTENANCE (XMAA S4) switches
STOP IN T5		
Cache Pause	Stop:	TMCF CACHE ADRS H TIGA PAUSE H (UBSD = 2 or 3) No Aborts (not TMCC ABORT H)
	Restart:	TIGA MEMSYNC (1) H
Single Bus Cycle	Stop:	TIGB SINGLE CY L TIGA PAUSE H
	Restart:	CONTINUE or MAINTENANCE (XMAA S4) switches

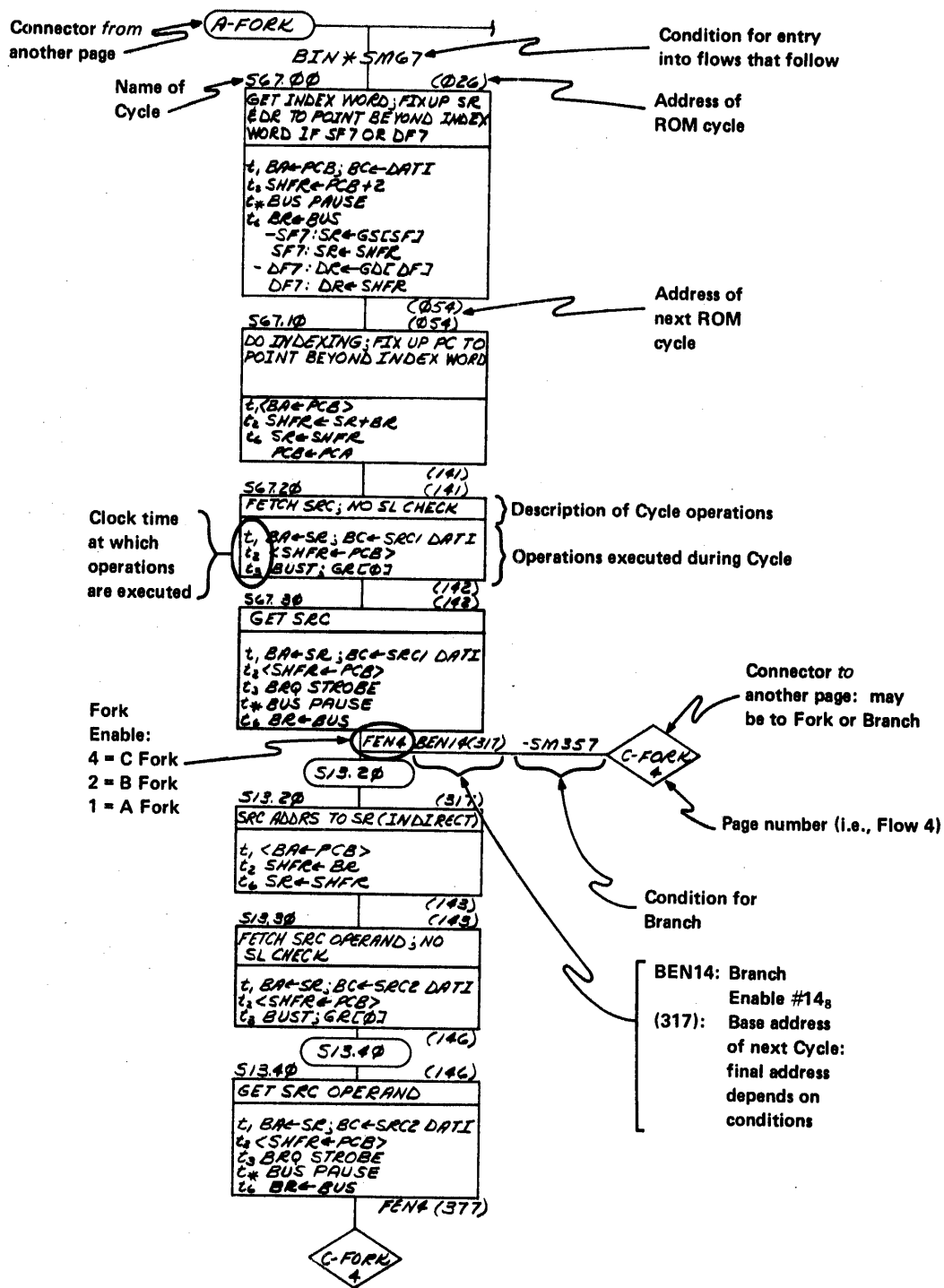
MICROPROGRAM WORD FIELDS





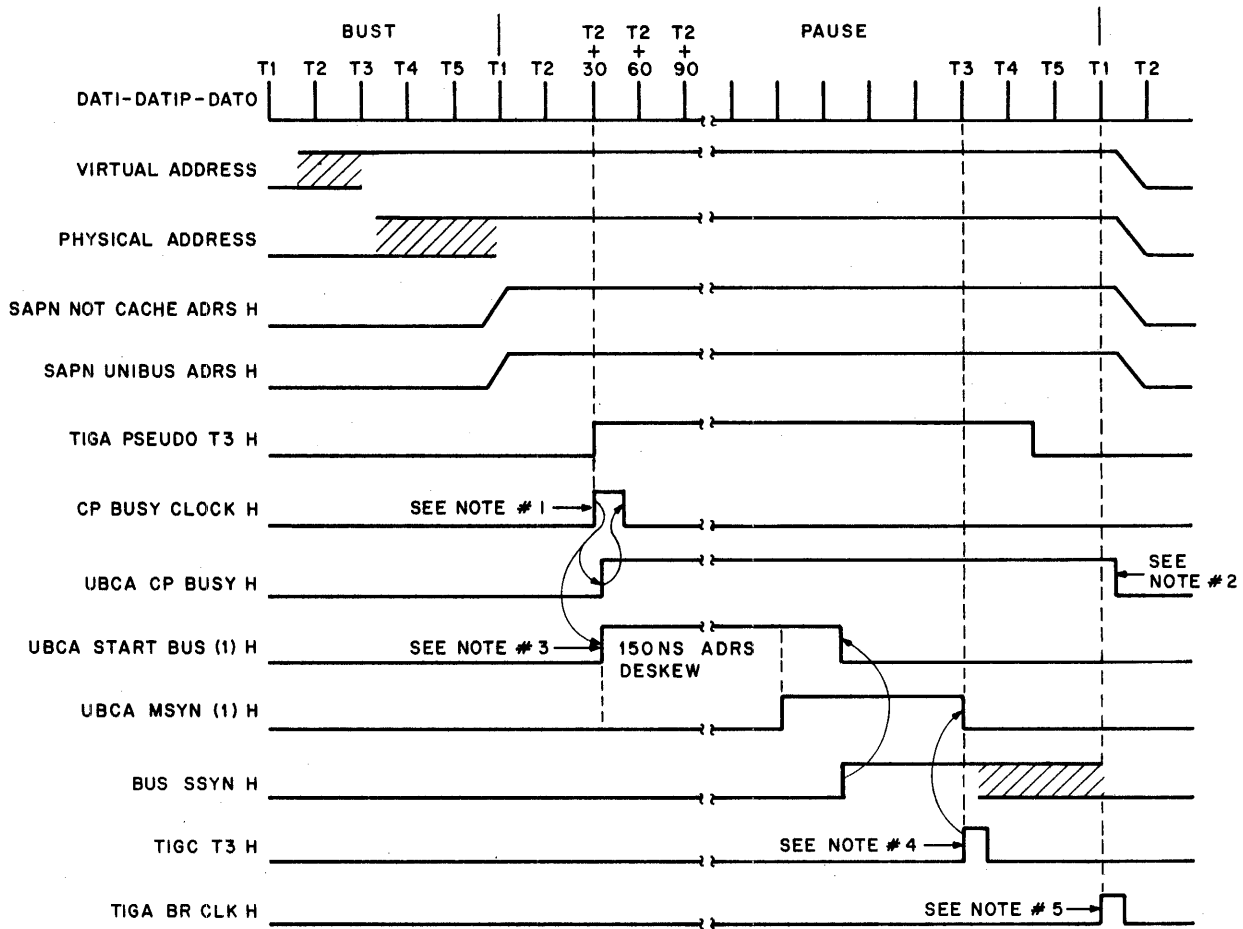
11-3103

Figure 1-4 ROM Timing



11-3135

Figure 1-3 Flow Chart Symbols (P/O Flows 2)

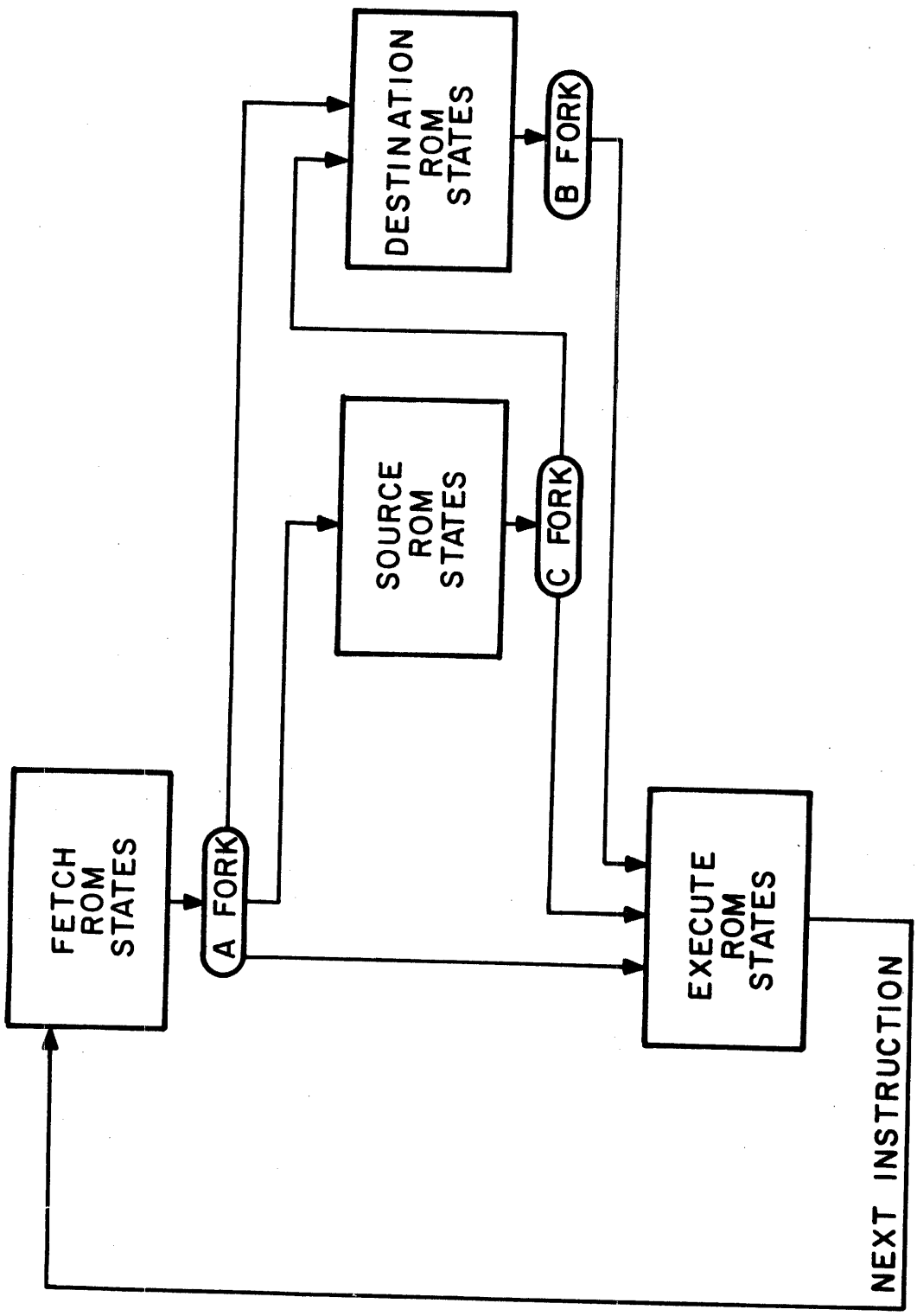


NOTES:

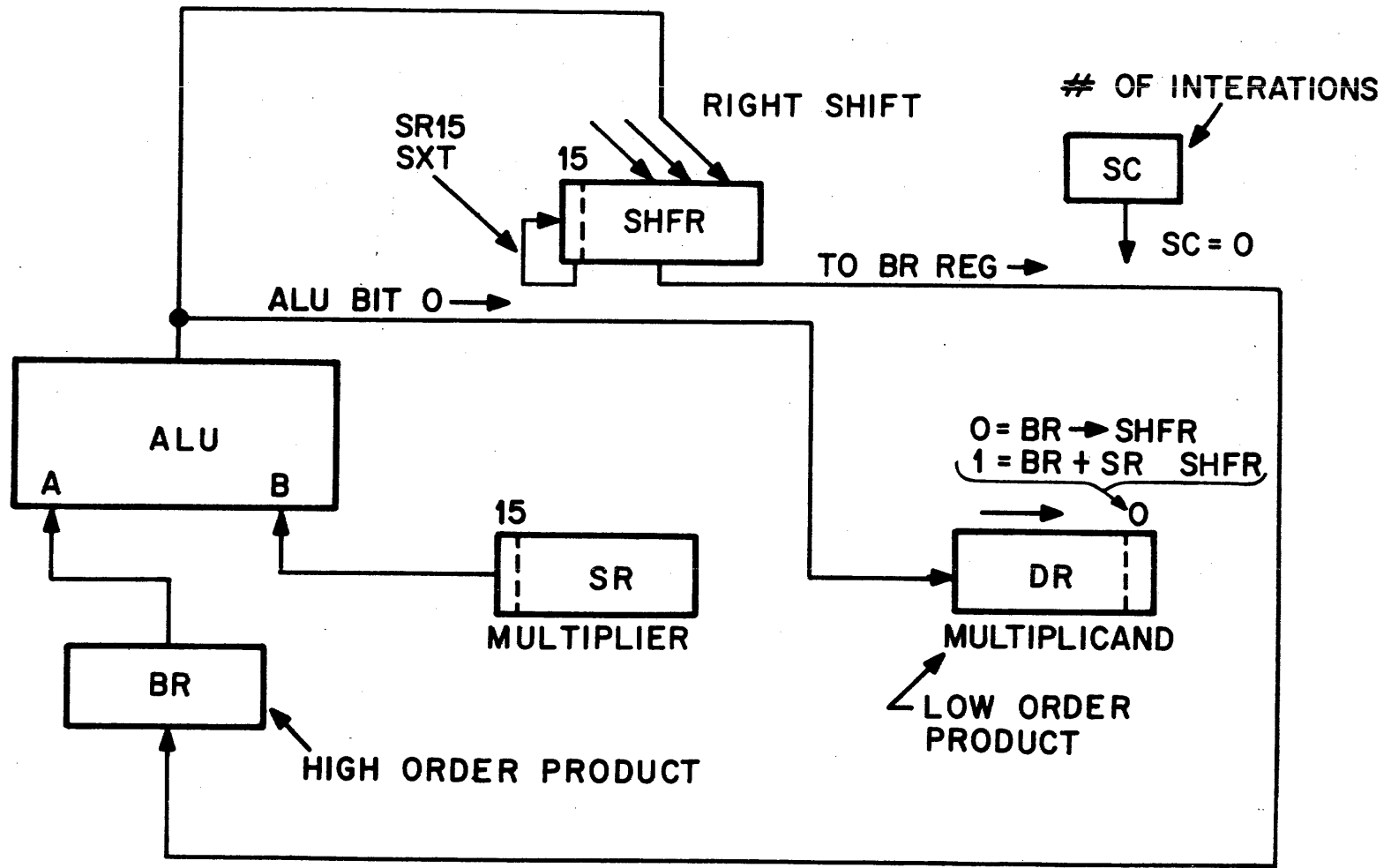
1. Set CP BUSY if $-(NPR + NPG + SACK + DSACK + ABORT + BBUSY)$.
2. CP BUSY is not cleared if DATIP cycle. It is cleared on DATO portion of DATIP/DATO.
3. Used to start DATO address deskew on DATIP/DATO operation.
4. 75 ns data deskew is obtained by 2 stage synchronizer on TIGA. Unibus data is loaded into PDRH buffer register at T3.
5. Address & control are deskewed from T3 to T1. PDRH buffer register loaded to BR at T1.

11-3124

Figure 5-2 Unibus Data Transfers



11/70 ROM PATHS



MULTIPLY DATA PATH

POSITIVE MULTIPLICAND, POSITIVE MULTIPLIER

MUL %0, 2

R0 = 005
R2 = 003

3
3

UADR	NEXT UADR	SC	SR	ALU	SHFR	BR	DR	
		7	00 000 011	0	0	0	00 000 101	
MUL.10	MUL.20	6	00 000 011	0	0	0	00 000 010	
MUL.20	MUL.30	5	00 000 011	00 000 011	00 000 001	00 000 001	10 000 001	
MUL.30	MUL.20	4	00 000 011	00 000 001	00 000 000	00 000 000	11 000 000	
MUL.20	MUL.30	3	00 000 011	00 000 011	00 000 001	00 000 001	11 100 000	
MUL.30	MUL.30	2	00 000 011	00 000 001	00 000 000	00 000 000	11 110 000	
MUL.30	MUL.30	1	00 000 011	00 000 000	00 000 000	00 000 000	01 111 000	
MUL.30	MUL.30	0	00 000 011	0 ← 0	0 ← 0	0 ← 0	00 111 100	
MUL.30	MUL.40	-	00 000 011	0 ← 0	0 ← 0	0 ← 0	00 011 110	
MUL.40	MUL.60	-	00 000 011	0 ← 0	0 ← 0	0 ← 0	00 001 111	STORE BR → R
MUL.60	FET.	-	00 000 011	00 001 111	00 001 111	0 ← 0	00 001 111	STORE DR → Rv1

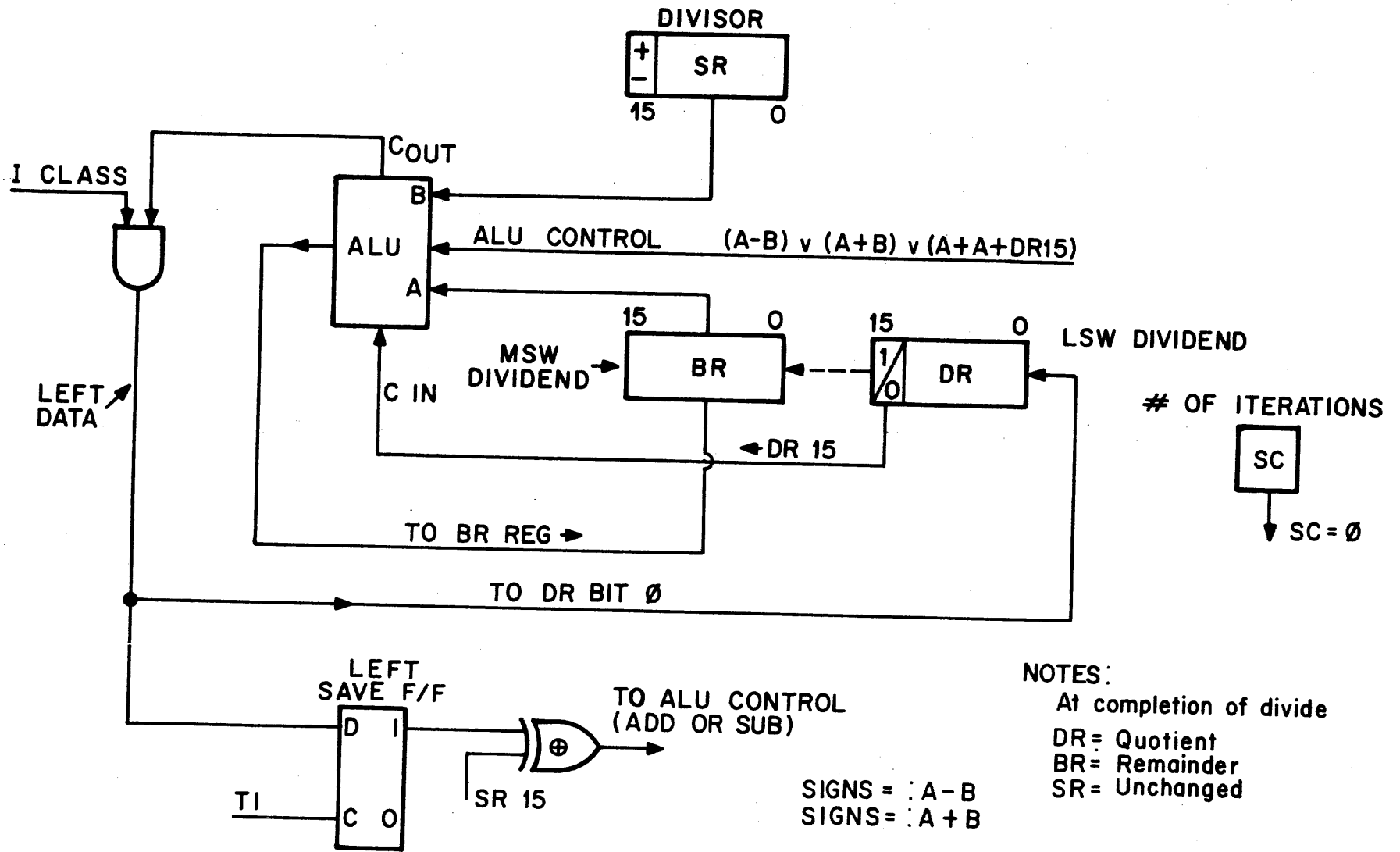
NEGATIVE MULTIPLICAND, NEGATIVE MULTIPLIER

MUL %0, 2

R2 = 375 (-3)	-3
R0 = 376 (-2)	<u>-2</u>
	+6

6-3

	UADR	NEXT UADR	SC	SR	ALU	SHFR	BR	DR	
			7	11 111 101				11 111 110	
MUL.10	MUL.30		6	11 111 101	0	0	0	01 111 111	
MUL.30	MUL.20		5	11 111 101	0	0	0	00 111 111	
MUL.20	MUL.20		4	11 111 101	11 111 101	11 111 110	11 111 110	10 011 111	
MUL.20	MUL.20		3	11 111 101	11 111 011	11 111 101	11 111 101	11 001 111	
MUL.20	MUL.20		2	11 111 101	11 111 010	11 111 101	01 111 101	01 100 111	
MUL.20	MUL.20		1	11 111 101	11 111 010	11 111 101	11 111 101	00 110 011	
MUL.20	MUL.20		0	11 111 101	11 111 010	11 111 101	11 111 101	00 011 001	
MUL.20	MUL.50		-	11 111 101	11 111 010	11 111 101	11 111 101	00 001 100	
MUL.50	MUL.60		-	11 111 101	00 000 000	00 000 000	00 000 000	00 000 110	STORE BR
MUL.60	FET.00		-	11 111 101	00 000 110	00 000 110	00 000 000	00 000 110	STORE DR



DIVIDE BLOCK DIAGRAM

-2 | -7

DIV. R2, R1

SR | BR, DR

R1 = 76
R2 = 77
R3 = 71

ICLASS
DAC
BSOPI

2000/DIV R2, R1

FET. 00

t1 BA ← PCB
BC ← DATI
t2 SHFR ← SR-SR
t3 BUST
CLEAR FLAGS
t6 IR ← SHFR

BA = 2000
BC0 & BC1 = 0
SHFR = 00
START BUS CYCLE
TMCC-CLRS E41&E37 F/F's
IR = 00

-BRQ

FET. 10

t1 BA ← PCB
BC ← DATI
t2 <SHFR ← PCB+2>
t3 BRQ STROBE
BUS PAUSE
t5 PCA ← PCB+2
t6 IR ← BUS
BR ← BUS
PCB ← PCA
1RD. 00

BA = 2000
BC0 & BC1 = 0
SHFR = 2002

PCA = 2002
IR = DIV R2, R1
BR = DIV R2, R1
PCB = 2002

t1 BA ← PCB
BC ← DATI
t2 SHFR ← PCB
t3 CONDITIONAL BUST
t5 PCA ← PCB+2
t6 -SF7: SR ← GS (SF)
SR ← R2
-DF: DR ← GD (DF)
DR ← R1

BA = 2002
BC0 & BC1 = 0
SHFR = 2002
START BUS CYCLE
PCA = 2004

SR = 77

DR = 76

DIV * DM0

DVS. 00

t1 <BA ← PCB>
 t2 SHFR ← DR
 t3 BEND
 t6 BR ← SHFR

BA = 2002
 SHFR = 76
 BUS CYCLE END
 BR = 76 DIVISOR

DIV. 00

t1 BA ← DR
 BC ← BSOPI
 t2 SHFR ← BR
 t6 SR ← SHFR
 DR ← GD(SF)
 DR ← R2
 CCLD4
 N=1, Z=0, V&C=0

BA = 76
 BC = DATA
 SHFR = 76 DIVISOR
 SR = 76
 DR = 77 HI ORDER DIVIDEND

DIV. 10

t1 <BA ← SR>
 t2 SHFR ← DR
 t6 CCLD4
 N=1, Z=0, V&C=0

BA = 76
 SHFR = 76

'
 -Z
 '

DIV. 20

t1 <BA ← DR>
 t2 <SHFR ← SR>

BA = 77
 SHFR = 76

'
 N
 '

DVN. 00

t1 <BA ← DR>
 t2 <SHFR ← SR>
 t3 CLEAR DR
 t6 SR ← GS(SFV1)
 SR ← R3

BA = 77
 SHFR = 76
 DR = 00
 SR = 71

DVN. 10

t1 <BA ← DR>
 t2 SHFR ← DR-SR

BA = 00
 DR = 000000
 SR² = 000111
 SHFR = 000111

t5 GR(SFV1) ← SHFR
R3 ← SHFR

R3 = 07

DVN.20

t1 <BA ← DR>
t2 SHFR ← DR-SR

BA = 00
DR = 000000
SR² = 000111
SHFR = 000111
DR = 00

t6 DR ← LEFT (DR)

DVN. 30

t1 <BA ← DR>
t2 SHFR ← DR-1

BA = 00
DR = 000000
-1 = 111111
SHFR = 111111 COUT15 = 0

t6 SR ← GS(SF)
SR ← R2
DR ← SHFR

SR = 77 HI ORDER DIVIDEND
DR = 77

DVN.40

t1 <BA ← DR>
t2 SHFR ← DR-SR

BA = 77
DR = 111111
SR² = 000001
SHFR = 000000

t5 GR(SF) ← SHFR
R2 ← SHFR
t6 DR ← SHFR
CCLD4

R2 = 00
DR = 00

N=0, Z=1, V&C = 0

DVN.50

t1 <BA ← DR>
t2 SHFR ← BR
t6 SR ← SHFR

BA = 00
SHFR = 76 DIVISOR
SR = 76

-N

DVN.60

t1 <BA ← DR>
t2 SHFR ← DR
t6 BR ← SHFR

BA = 00
SHFR = 00
BR = 00

DVN. 70 (9)

t1 <BA ← DR>
t2 SHFR ← DR
t3 SC ← 05
t6 DR ← GD (SFV1)
DR ← R3
CCLD4

BA = 00
SHFR = 77
SC = 05
DR = 07 LOW ORDER DIVIDEND

N=1, Z=0, V&C=0

DIV.30

t1 <BA ← DR>
t2 SHFR ← ALU\$ BR+BR+DR15

BA = 07
BR = 000000
BR = 000000
DR15 = 0
SHFR = 000000
BR=00

t6 BR ← SHFR
CCLD\$

N=1, C,V&2=1

SR15(1)

DIV.50

t1 <BA ← DR>
t2 SHFR ← BR+SR

BA = 07
BR = 000000
SR = 111110
SHFR = 111110 COUT15 = 0

t3 SC ← SC-1
t6 BR ← SHFR
DR ← LEFT (DR)
(ALU CARRY INSERTED)
CCLD6

SC=04
BR = 76
DR = 001110

N=0, Z=0, C=1 & V=1

DIV.60

t1 <BA ← DR>
t2 SHFR ← BR

BA = 16
SHFR = 76

-DIV QUIT Z=1 ^ SR15(1)

DIV.70

t1 <BA ← DR>
t2 SHFR ← ALU\$

BA = 16
BR = 111110
BR = 111110
DR15 = 0
SHFR = 111100

t6 BR ← SHFR

BR = 74

DIV SUB

COUT15 = ∅ SR15(1) FROM DIV.50

DIV.8∅

t1 <BA ← DR>
t2 SHFR ← BR-SR

BA = 001110
BR = 111100
SR² = 000010
SHFR = 111110

t3 SC ← SC-1
t6 BR ← SHFR
DR ← LEFT (DR)

SC = ∅3

COUT15 = ∅
BR = 76
DR = 011100

DIV.7∅

t1 <BA ← DR>
t2 SHFR ← ALU\$

BA = 34
BR = 111110
BR = 111110
DR15 = 0
SHFR = 111100
BR = 74

t6 BR ← SHFR

DIV SUB

COUT15=∅ / SR15(1)

DIV.8∅

t1 <BA ← DR>
t2 SHFR ← BR-SR

BA = 34
BR = 111100
SR² = 000010
SHFR = 111110

t3 SC ← SC-1
t6 BR ← SHFR
DR ← LEFT (DR)

SC = ∅2 COUT15 = ∅
BR = 76
DR = 111000

DIV.70

t1 <BA ← DR>
t2 SHFR ← ALU\$

BA = 70
BR = 111110
BR = 111110
DR15 = 1
SHFR = 111101

t6 BR SHFR

BR = 75

DIV SUB

COUT15=~~0~~ SR15(1)

DIV. 8~~0~~

t1 <BA ← DR>
t2 SHFR ← BR-SR

BA = 70
BR = 111101
SR² = 000010
SHFR = 111111 COUT15=~~0~~
SC=~~0~~1
BR = 111111
DR = 110000

t3 SC ← SC-1
t6 BR ← SHFR
DR ← LEFT(DR)

DIV. 7~~0~~

t1 <BA ← DR>
t2 SHFR ← ALU\$

BA = 110000
BR = 111111
BR = 111111
DR15 = 1
SHFR = 111111
BR = 77

t6 BR ← SHFR

DIV SUB

DIV. 8~~0~~

t1 <BA ← DR>
t2 SHFR ← BR-SR

BA = 110000
BR = 111111
SR² = 000010
SHFR = 000001 COUT15=1
SC=~~0~~~~0~~
BR = 000001
DR = 100001

t3 SC ← SC-1
t6 BR ← SHFR
DR ← LEFT(DR)

DIV. 70

t1 <BA ← DR>
t2 SHFR ← ALU\$

BA = 41
BR = 000001
BR = 000001
DR15 = 1
SHFR = 000011
BR = 03

t6 BR ← SHFR

-DIV SUB

DIV. 9~~0~~

t1 <BA ← DR>

BA = 41

t2 SHFR ← BR+SR

BR = 000011
SR = 111110
SHFR = 000001

t3 SC ← SC-1

SC = 77

t6 BR ← SHFR

BR = 000001 000010

DR ← LEFT (DR)

DR = 000011

DVC. 00

t1 < BA ← DR >

BA = 03

t2 SHFR ← BR

SHFR = 01 000010

t5 GR(SFV1) ← SHFR

R3 = 01

R3 ← SHFR

DR(1) * SR15 (1)

DVC. 40

t1 < BA ← DR >

BA = 03

t2 SHFR ← -BR

SHFR = 111110

t6 BR ← SHFR

BR = 111110

N

DVC. 60

t1 < BA ← DR >

BA = 03

t2 SHFR ← BR+1

BR = 111110

SHFR = 111111

t5 GR(SFV1) ← SHFR

R3 = 77

R3 ← SHFR

DVC. 70

t1 < BA ← DR >

BA = 03

t2 SHFR ← DR

SHFR = 03

t3 BRQ STROBE

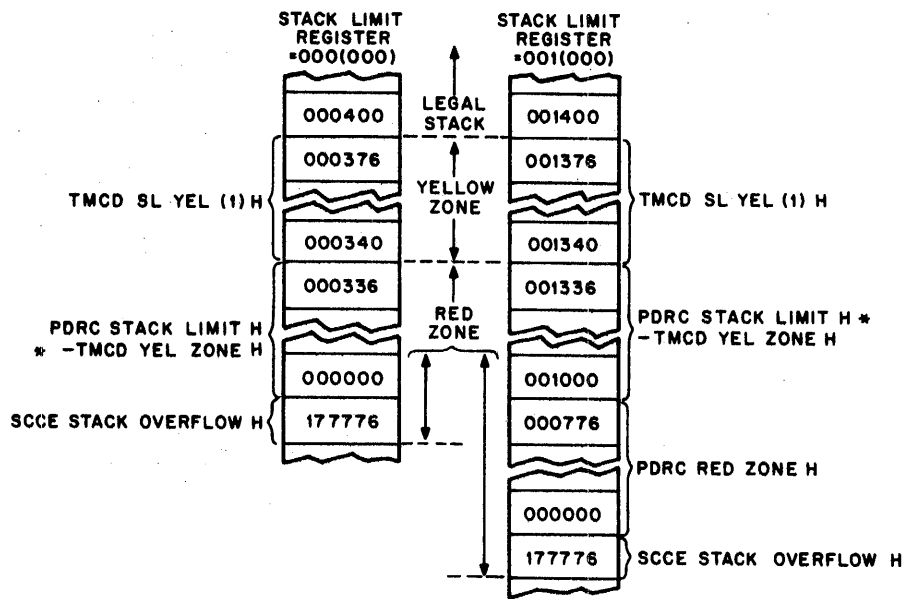
t5 GR(SF) ← SHFR

R2 = 03

R2 ← SHFR

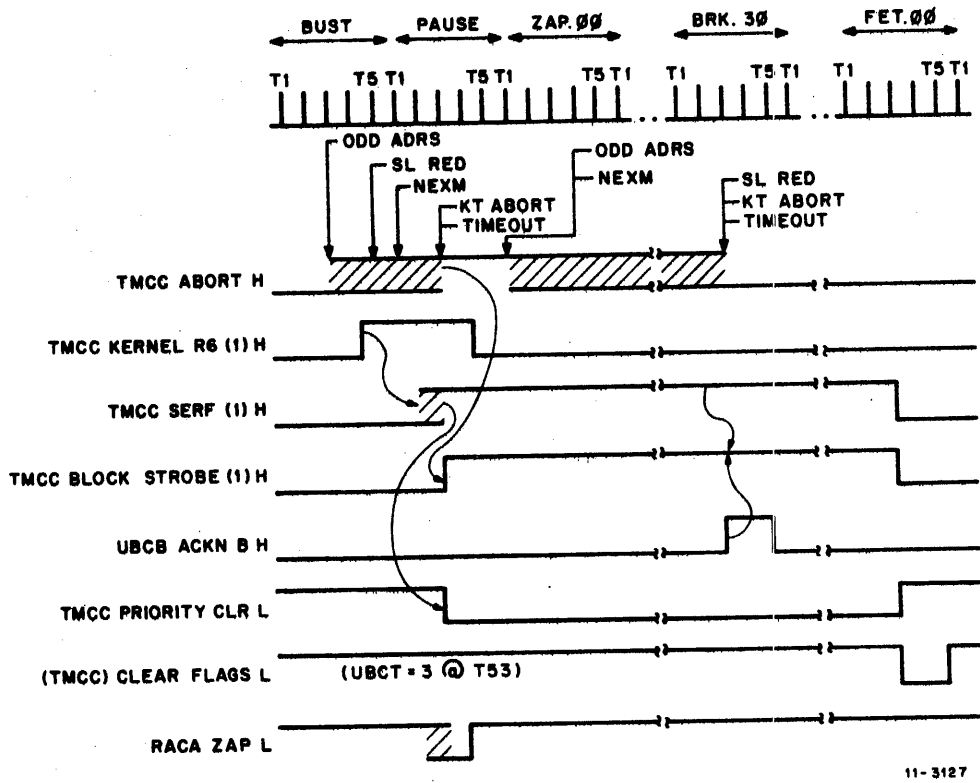
t6 CCLD4

N=0, Z=0, V&C=0



11-3125

Figure 6-1 Examples of Stack Limit



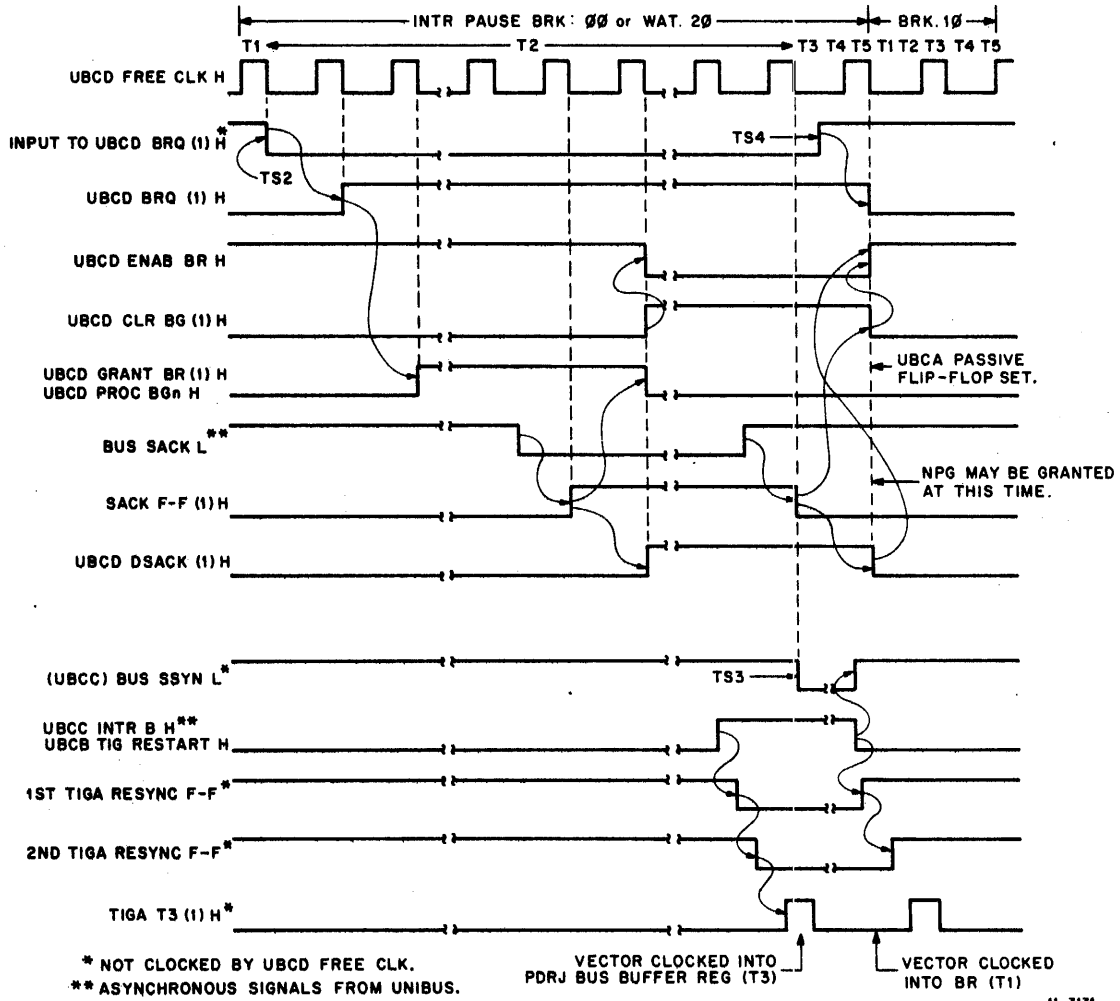
11-3127

Figure 6-3 Stack Error Aborts

Table 6-2
Processor Service in Order of Priority

Order	Condition	Input	Output*	Result*
1	console flag	UBCF STOP L	TMCA CONF (1) H	do console control function
2	cache parity	CCBJ PARITY TRAP H	TMCB PART L	trap (114)
3	memory management traps	SSRD MEM MGMT TRAP L	TMCB SEGT L TMCA HONOR SEGT H	trap (250)
4	warning stack violation	TMCD SL YEL	TMCA HONOR SLY H	trap (4)
5	power fail	UBCE PDNF (1) H	TMCA HONOR PWR F L	trap (24)
6	floating-point exception trap CP LEV 7	FRHH FP EXC TRAP L	TMCA HONOR FPTRAP L	trap (224)
7	priority interrupt request PIRQ7	PDRD PIR15 (1) H	TMCA HONOR PIR7 L	trap (240)
8	bus request, level 7 interrupt CP LEV 6	BUS BR7 L	TMCA HONOR BR7 L	interrupt
9	priority interrupt request PIRQ6	PDRD PIR14 (1) H	TMCA HONOR PIR6 L	trap (240)
10	bus request, level 6 interrupt CP LEV 5	BUS BR6 L	TMCA HONOR BR6 L	interrupt
11	priority interrupt request PIRQ5	PDRD PIR13 (1) H	TMCA HONOR PIR5 L	trap (240)
12	bus request, level 5 interrupt CP LEV 4	BUS BR5 L	TMCA HONOR BR5 L	interrupt
13	priority interrupt request PIRQ4	PDRD PIR12 (1) H	TMCA HONOR PIR4 L	trap (240)
14	bus request, level 4 interrupt CP LEV 3	BUS BR4 L	TMCB HONOR BR4 L	interrupt
15	priority interrupt request PIRQ3 CP LEV 2	PDRD PIR11 (1) H	TMCB HONOR PIR3 L	trap (240)
16	priority request PIRQ2 CP LEV 1	PDRD PIR10 (1) H	TMCB HONOR PIR2 L	trap (240)
17	priority request PIRQ1	PDRD PIR09 (1) H	TMCB HONOR PIR1 L	trap (240)
18	T bit set and not RTT	PDRD PS04 (1) H and - (IRCD RTT L)	TMCB HONOR T L	trap (14)

* Only if no higher priority request has been received.



11-3131

Figure 6-9 INTR Sequence

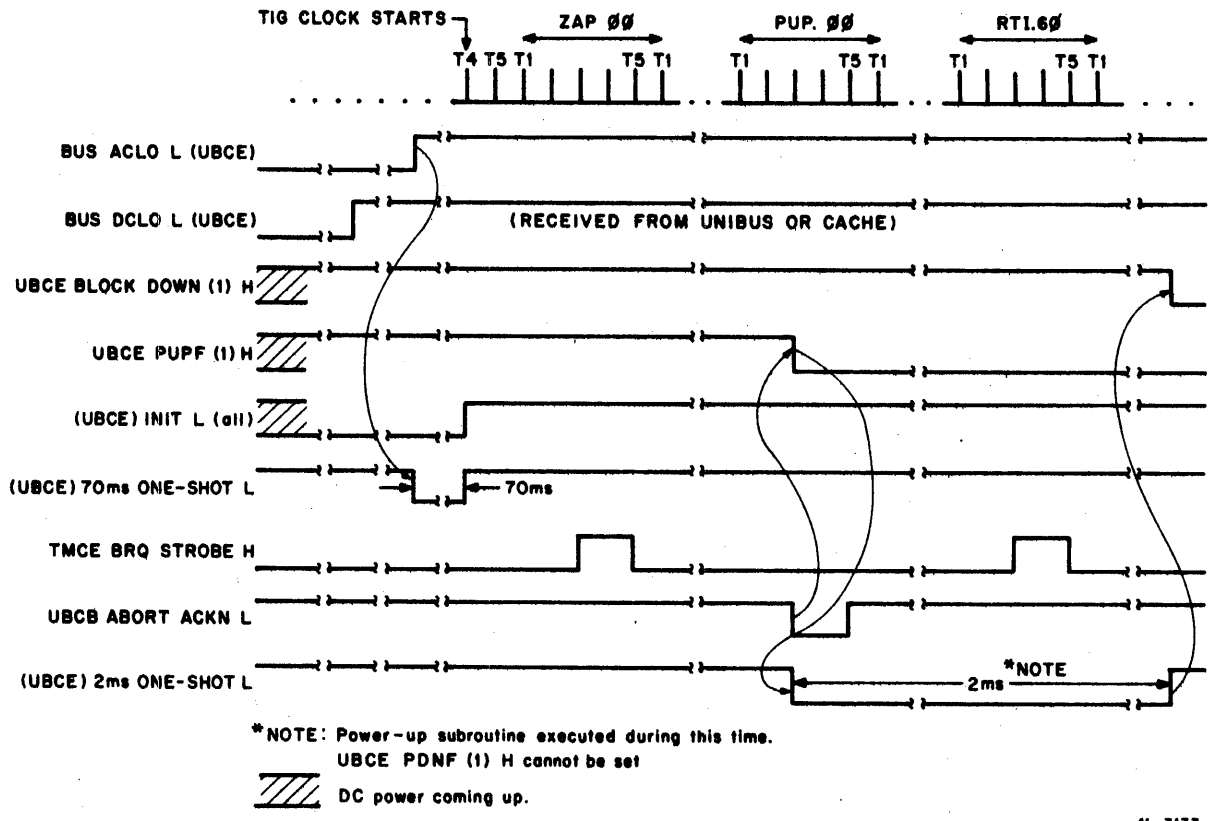
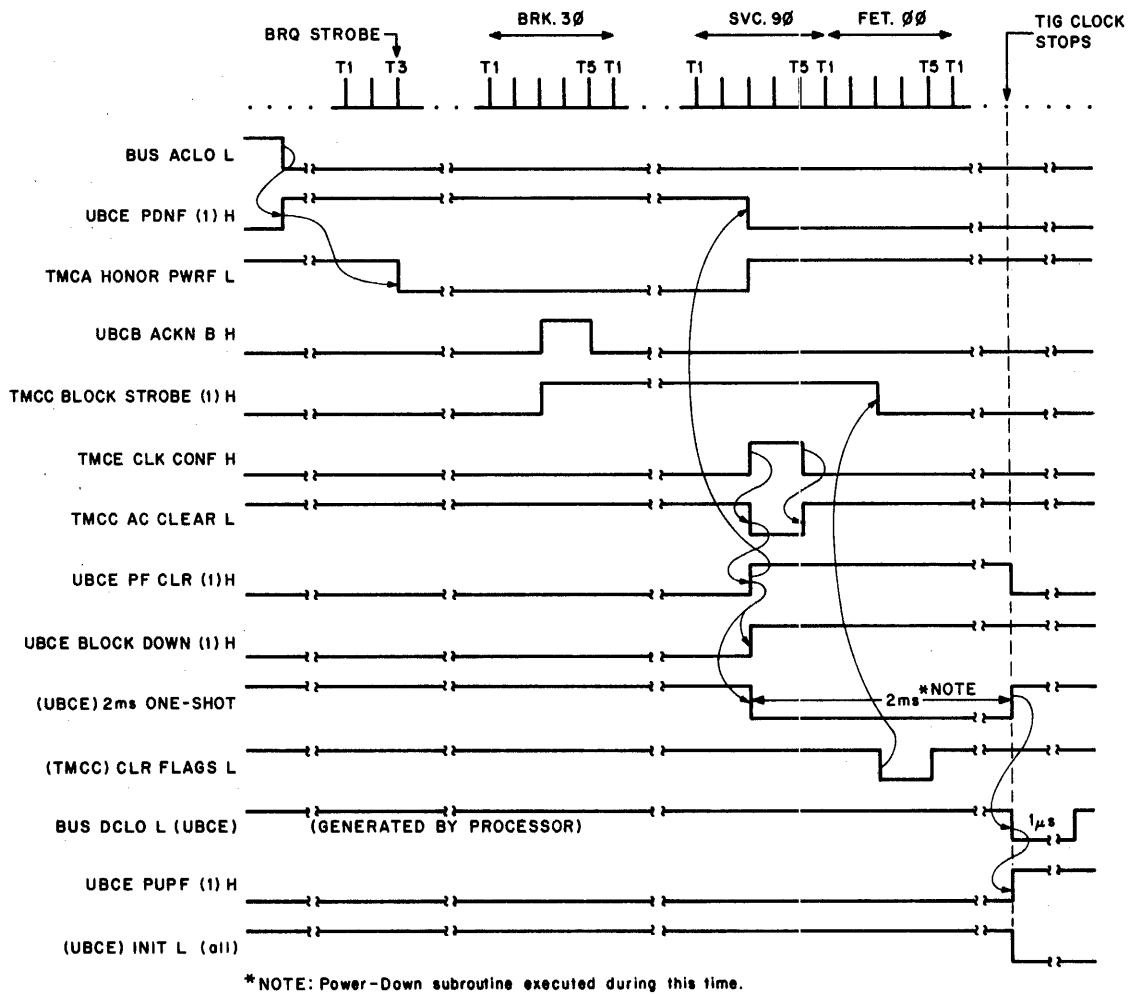


Figure 6-11 Power-Up

11-3133



11-3132

Figure 6-10 Power-Down

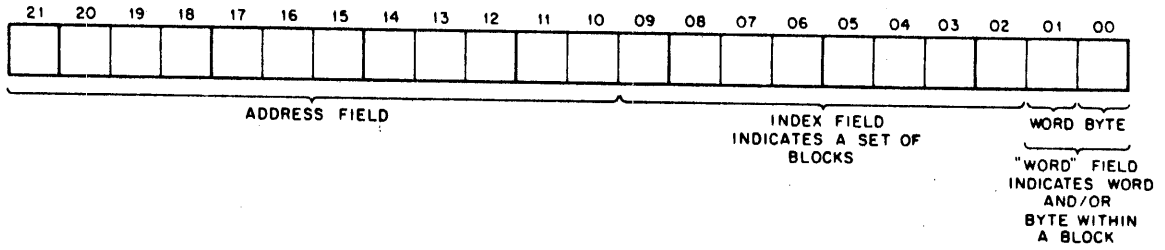


Figure 2-1 22-Bit Byte Address Breakdown (2 Words per Block, 256 Sets of Blocks)

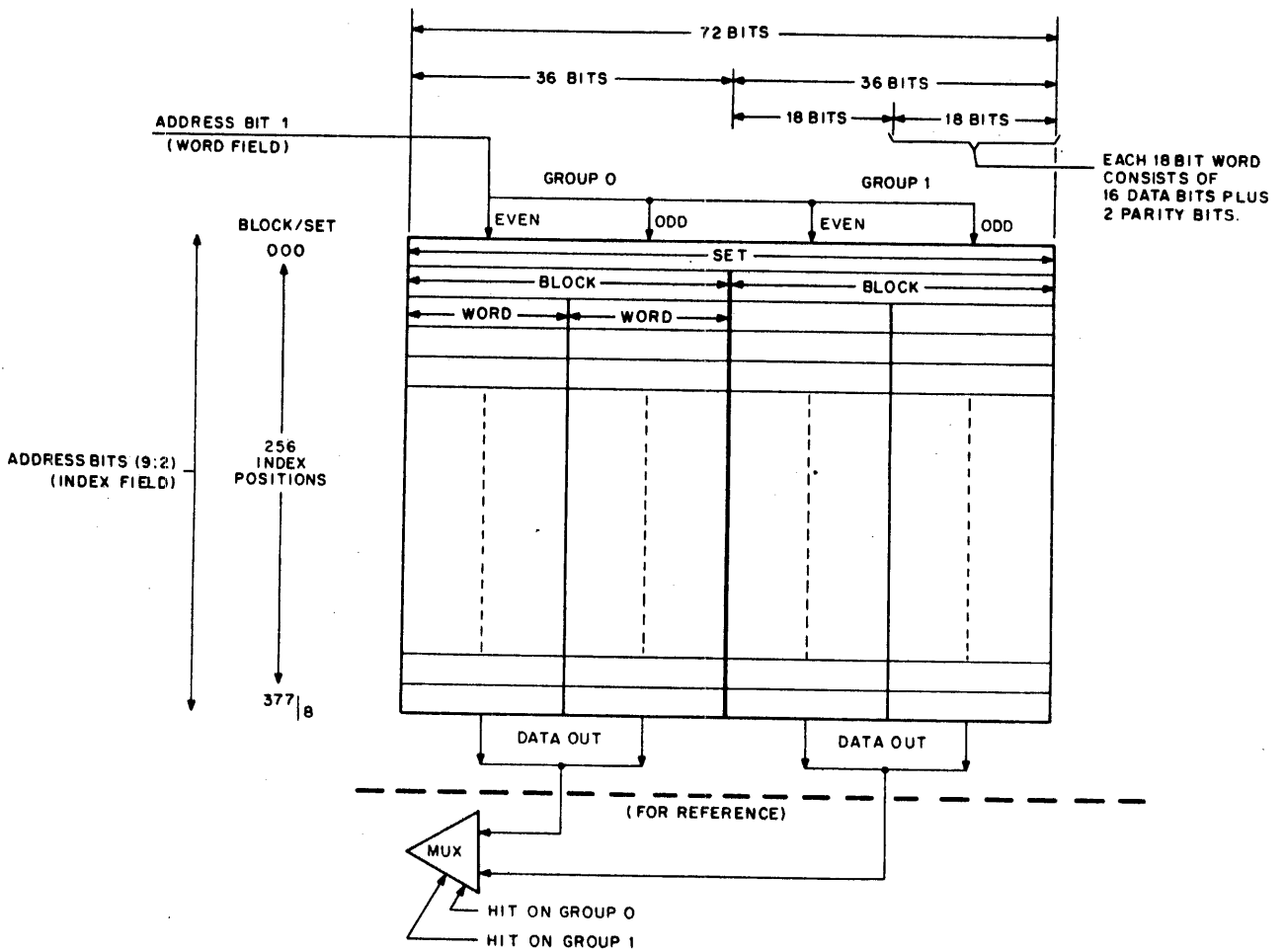
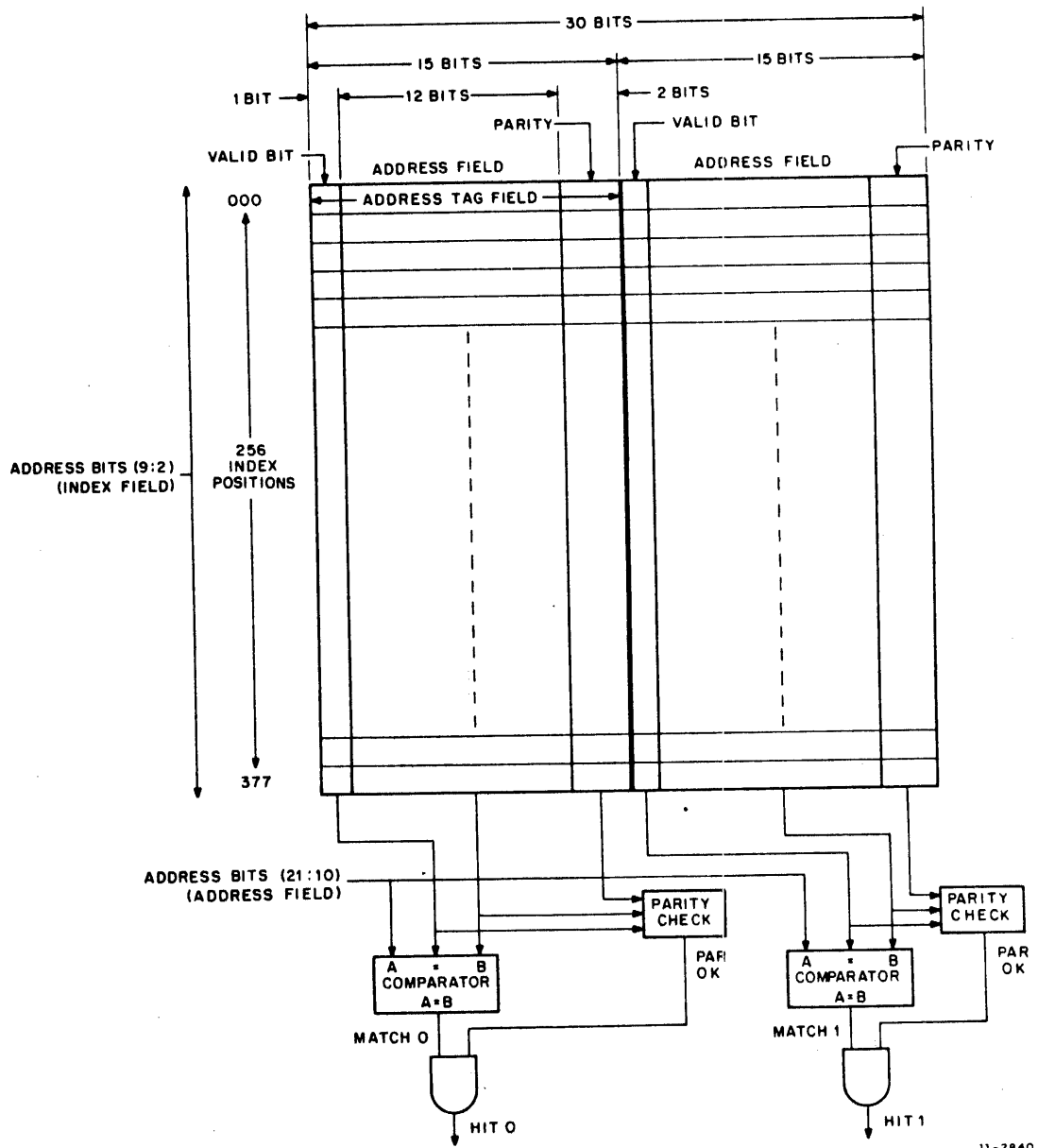
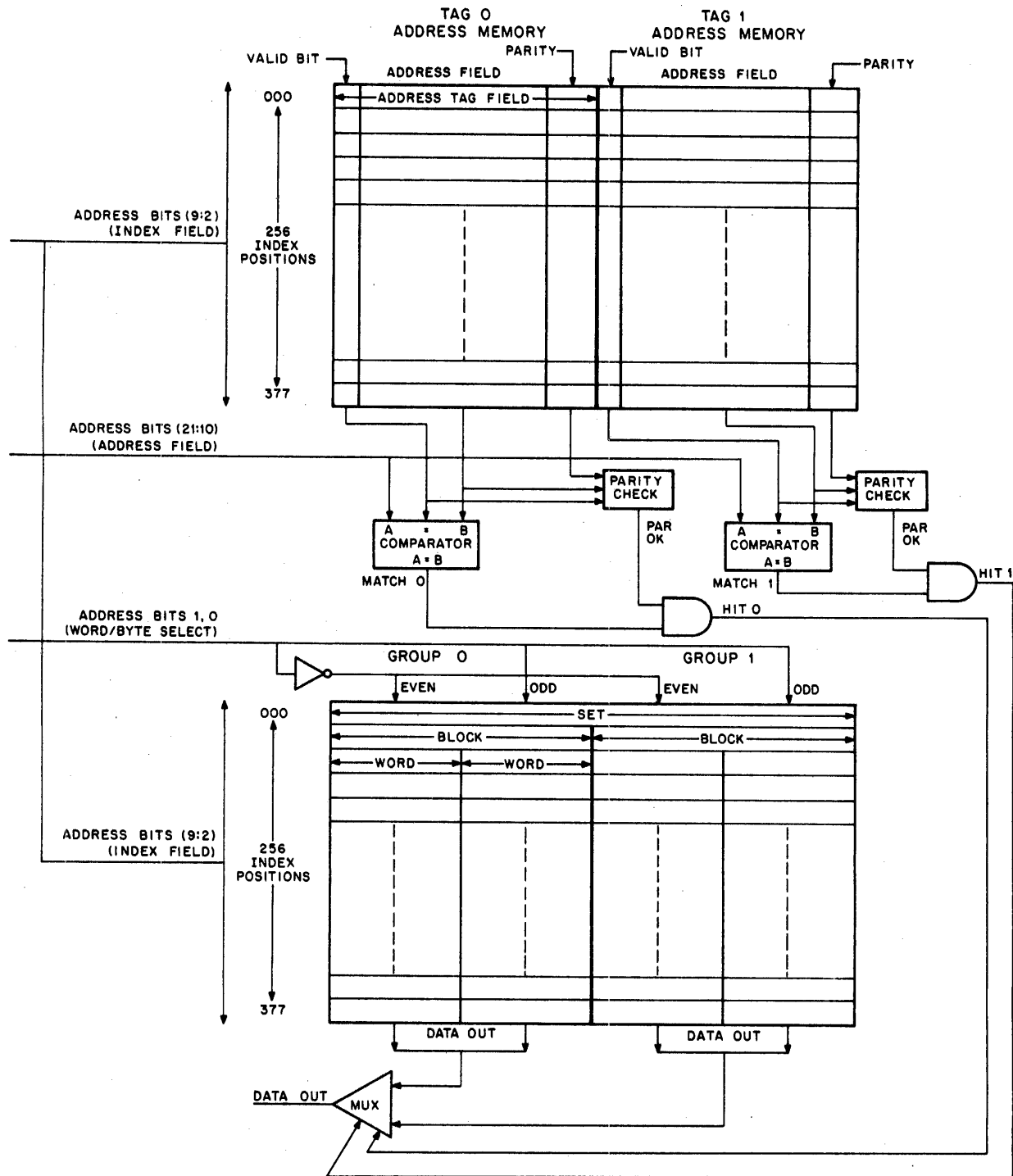


Figure 2-2 Fast Data Memory Organization



11-2840

Figure 2-3 Address Memory Organization



11-2953

Figure 2-4 PDP-11/70 Cache Simplified Data Path Diagram

PDP 11/70 CACHE MEMORY

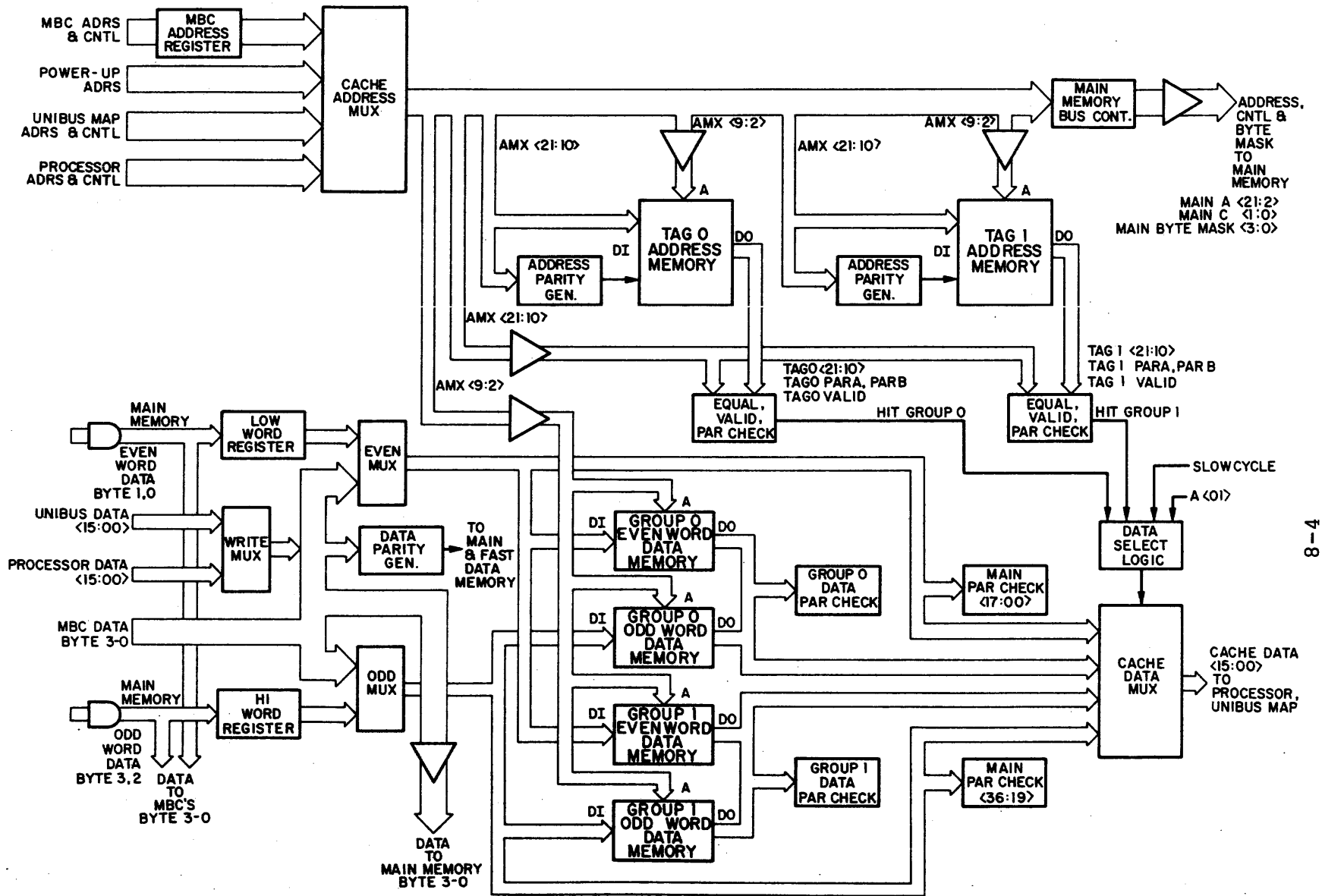


Table 2-1
Example Program
(all numbers in octal notation)

Address Loaded	Machine Code	Index Field	Address Field	Mnemonics	Remarks
001000	013737	[200]	[0000]	MOV @#5000@#3000	This program moves the INC instruction at address 5000 to address 3000, then jumps to address 3000, performs the INC instruction, and HALTS
001002	005000				
001004	003000				
001006	000137				
001010	003000				
001012	177776	[202]		JMP @#3000	
003000	DONT CARE	[200]	[0001]	HALT	
003002	001012				
003004	000000				
005000	005237	[200]	[0002]	INC @ #	

Table 2-2
Summary of Cache Operations Example

Processor			Random Bit (Assumed)	Hit / Miss	Fast Data Memory						Address Memory		Remarks
REF	PC	Operation			GROUP 0			GROUP 1			TAG 0	TAG 1	
					Block	Contents		Block	Contents		Address Memory	Address Memory	
				Low Word	High Word		Low Word	High Word	Address Field Loaded	Address Field Loaded			
1	1000	Fetch (1000) = 013737	0	Read Miss	200	(1000) = 013737	(1002) = 005000			0000		Fetch MOV instruction	
	1002	Fetch (1002) = 005000	1	Hit on	200		↑			↑ Hit		Fetch source address	
	1004	Fetch (5000) = 005237	0	Read Miss	200	(5000) = 005237	(5002) = xxxxxx			0002		Fetch contents at source address	
4	1004	Fetch (1004) = 003000	1	Read Miss	201		(1004) = 003000	(1006) = 000137		0000		Fetch destination address	
5	1006	Write 005237 into 3000	0	Write Miss								MOV contents of source to destination address	
6	1006	Fetch (1006) = 000137	1	Hit on	201		↑			↑ Hit		Fetch JMP instruction	
7	1010	Fetch (1010) = 003000	0	Read Miss	202	(1010) = 003000	(1012) = 177776			0000		Fetch destination address	
8	3000	Fetch (3000) = 005237	1	Read Miss	200		(3000) = 005237	(3002) = 001012			0001	JUMP; Fetch INC instruction	
9	3002	Fetch (3002) = 001012	0	Hit on	200			↑		↑ Hit		Fetch destination address	
10	3004	Fetch (001012) = 177776	1	Hit on	202			↑		↑ Hit		Fetch contents of destination address (DATIP)	
11	3004	Write 177777 into 001012	0	Hit on	202	(1010) = unaltered	(1012) = 177777			↑ Hit		INC and restore (DATO)	
12	3004	Fetch (3004) = 000000	1	Read Miss	201		(3004) = 000000	(3006) = xxxxxx				Fetch and execute HALT instruction	

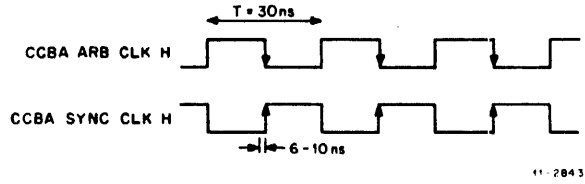


Figure 4-1 Cache Clock Waveforms

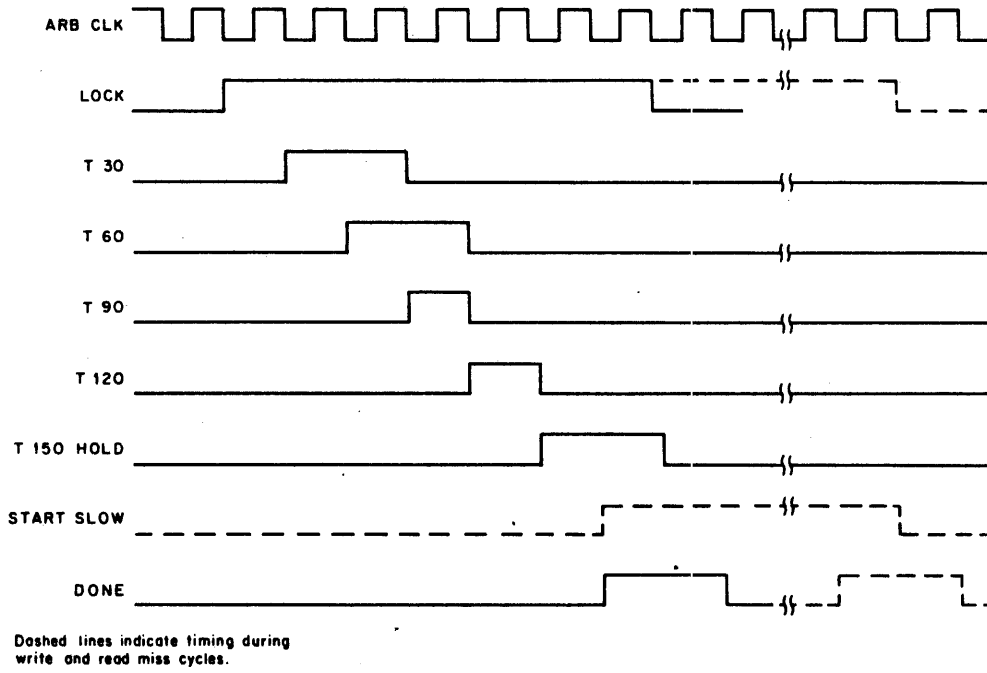


Figure 4-2 Cache Timing Sequence

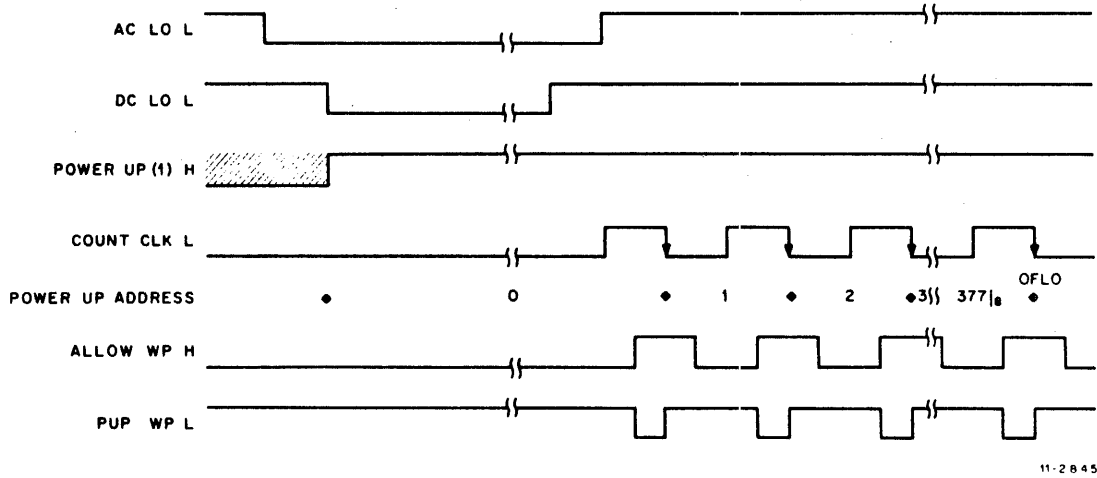


Figure 4-3 Power-Up Sequence Timing Diagram

Table 4-2
Cache Registers

Register	Address	Access
Low Error Address	17 777 740	Read only
High Error Address	17 777 742	Read only
Memory System Error	17 777 744	Read/selective clear
Control	17 777 746	Read/write
Maintenance	17 777 750	Read/write
Hit/Miss	17 777 752	Read only

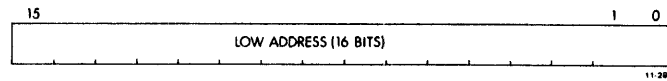


Figure 4-8 Low Error Address Register

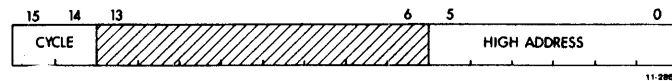


Figure 4-9 High Error Address Register

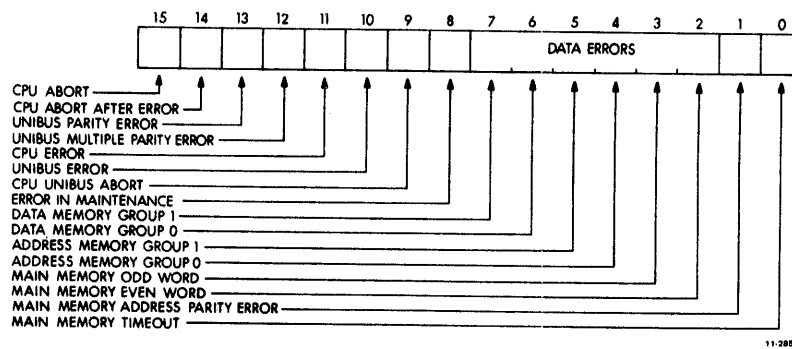


Figure 4-10 Memory System Error Register

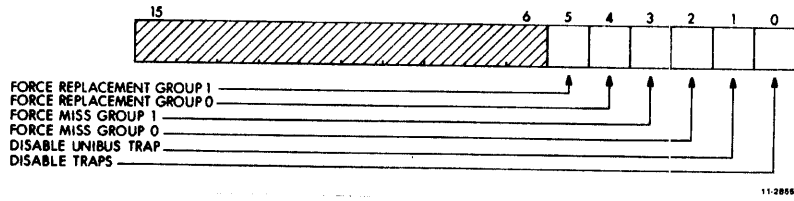


Figure 4-11 Control Register

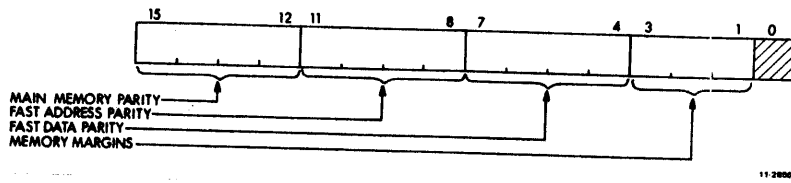


Figure 4-12 Maintenance Register

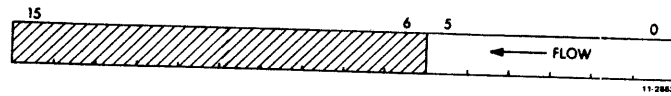
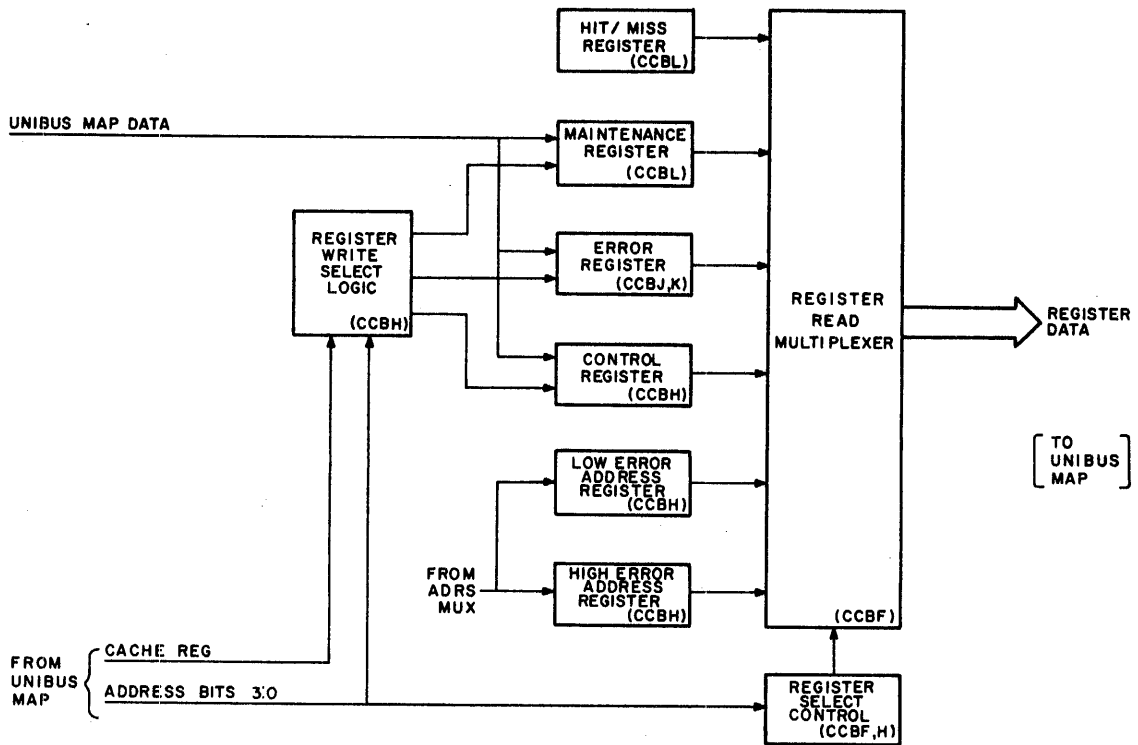


Figure 4-13 Hit/Miss Register



11-2850

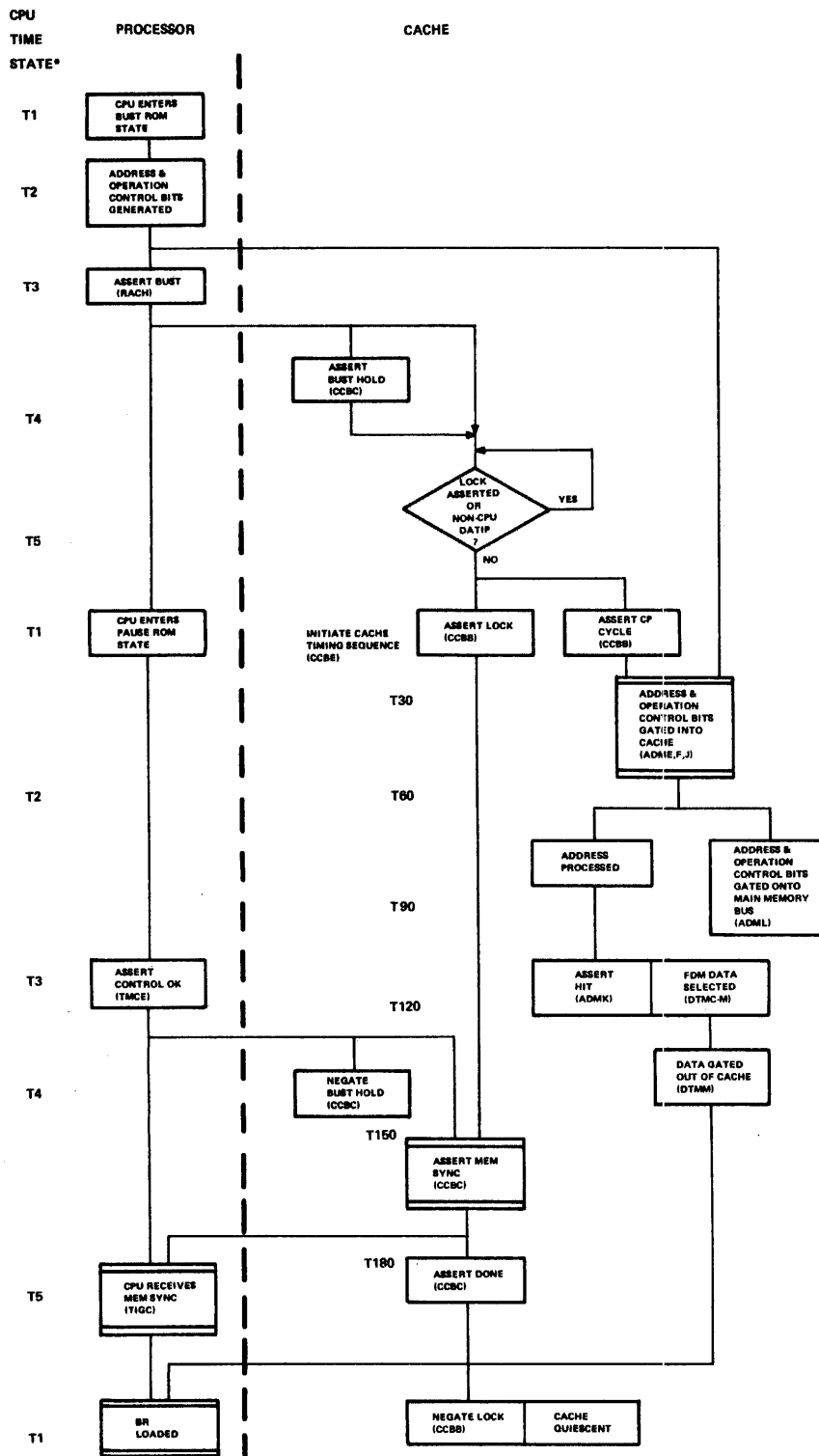
Figure 4-14 Register Logic Block Diagram

CACHE OPERATION ON HIT AND MISS

9-1

		What Happens In:	
		CACHE	MAIN MEMORY
Processor or Unibus Map	READ	HIT	No Change
		MISS	Update
	WRITE	HIT	Update
		MISS	No Change
RH-70 Massbus Controller	READ	HIT	No Change
		MISS	No Change
	WRITE	HIT	Invalidate
		MISS	No Change

TR-1021



*The processor time states are intended as a frame of reference only for events which occur in the processor.

11-2830

Figure 3-8 Processor Read Hit

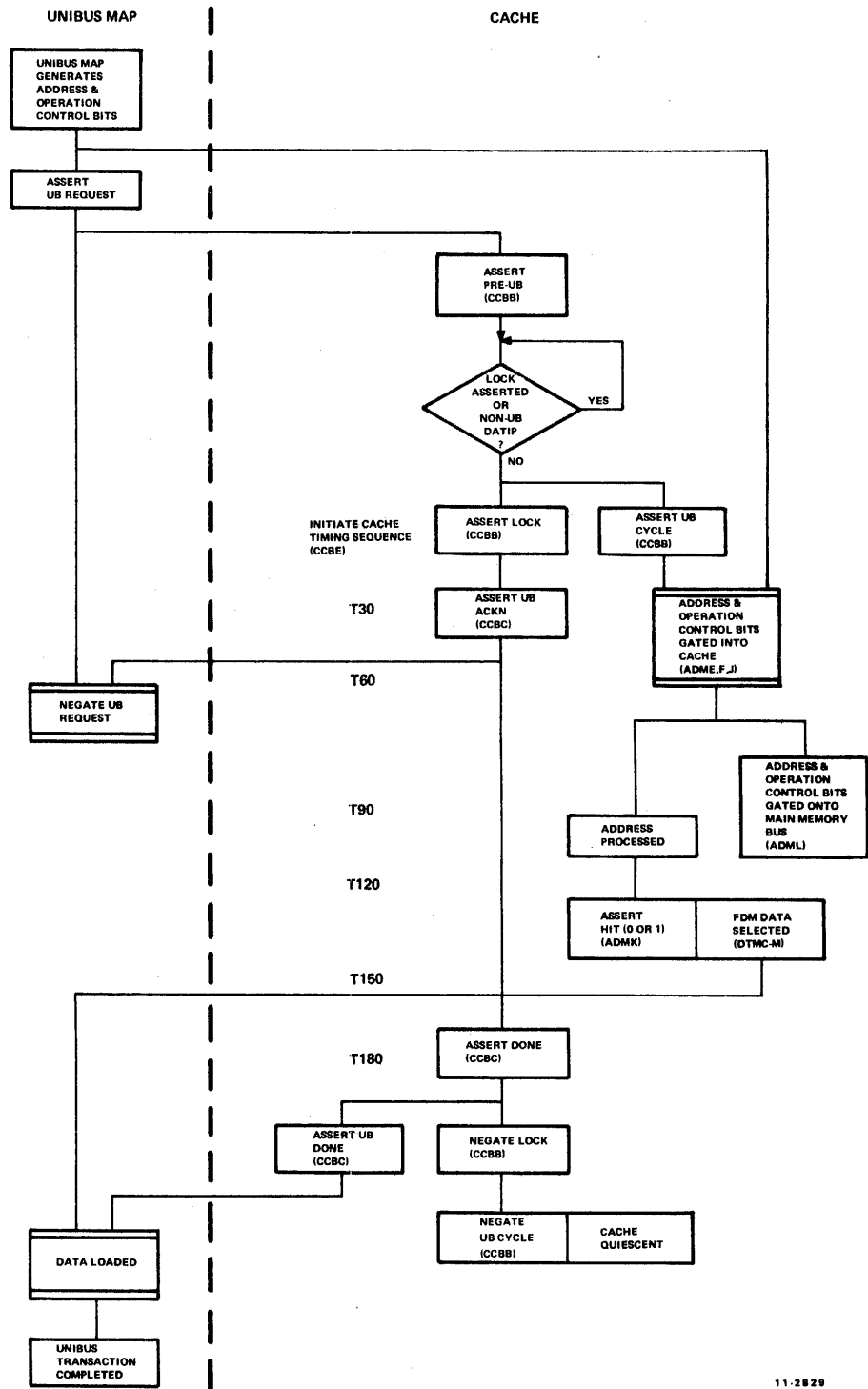


Figure 3-12 Unibus Map Read Hit

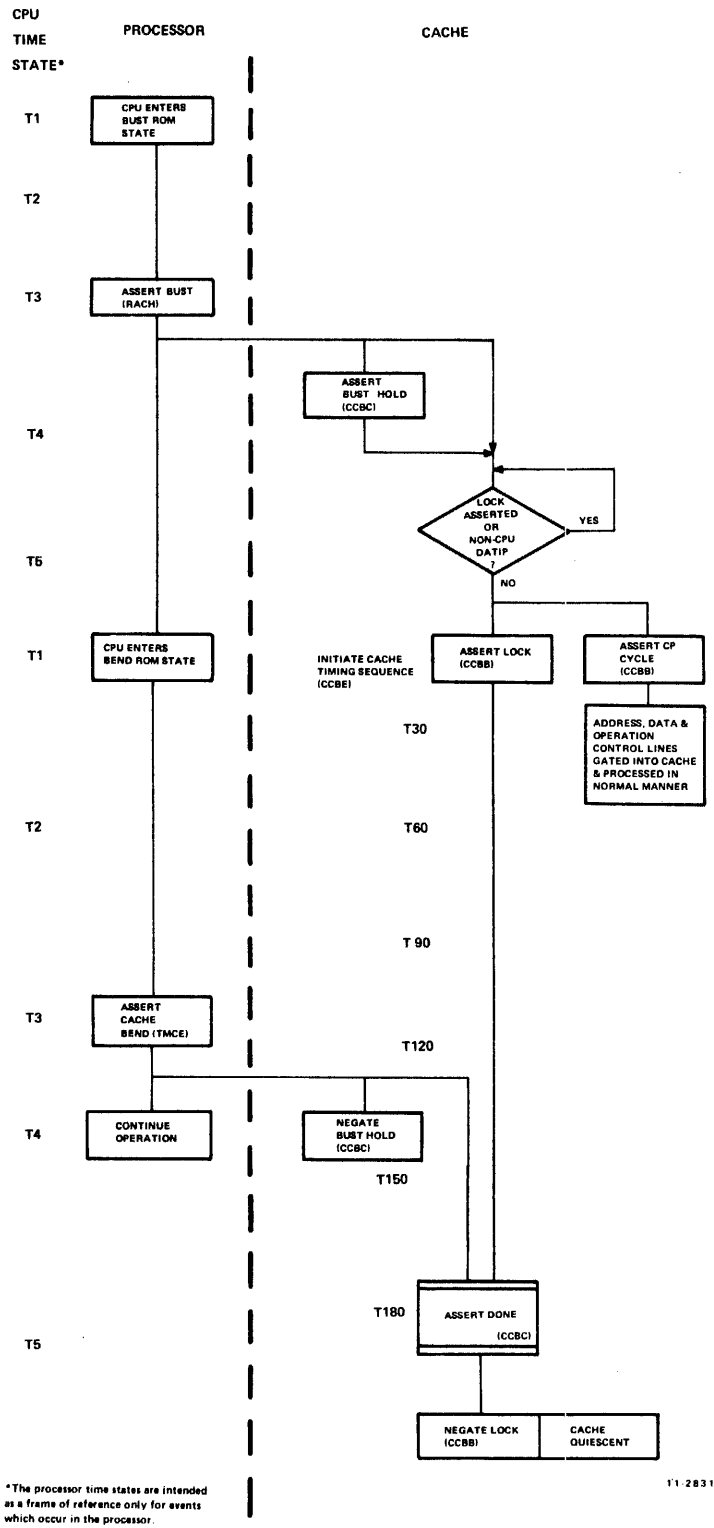
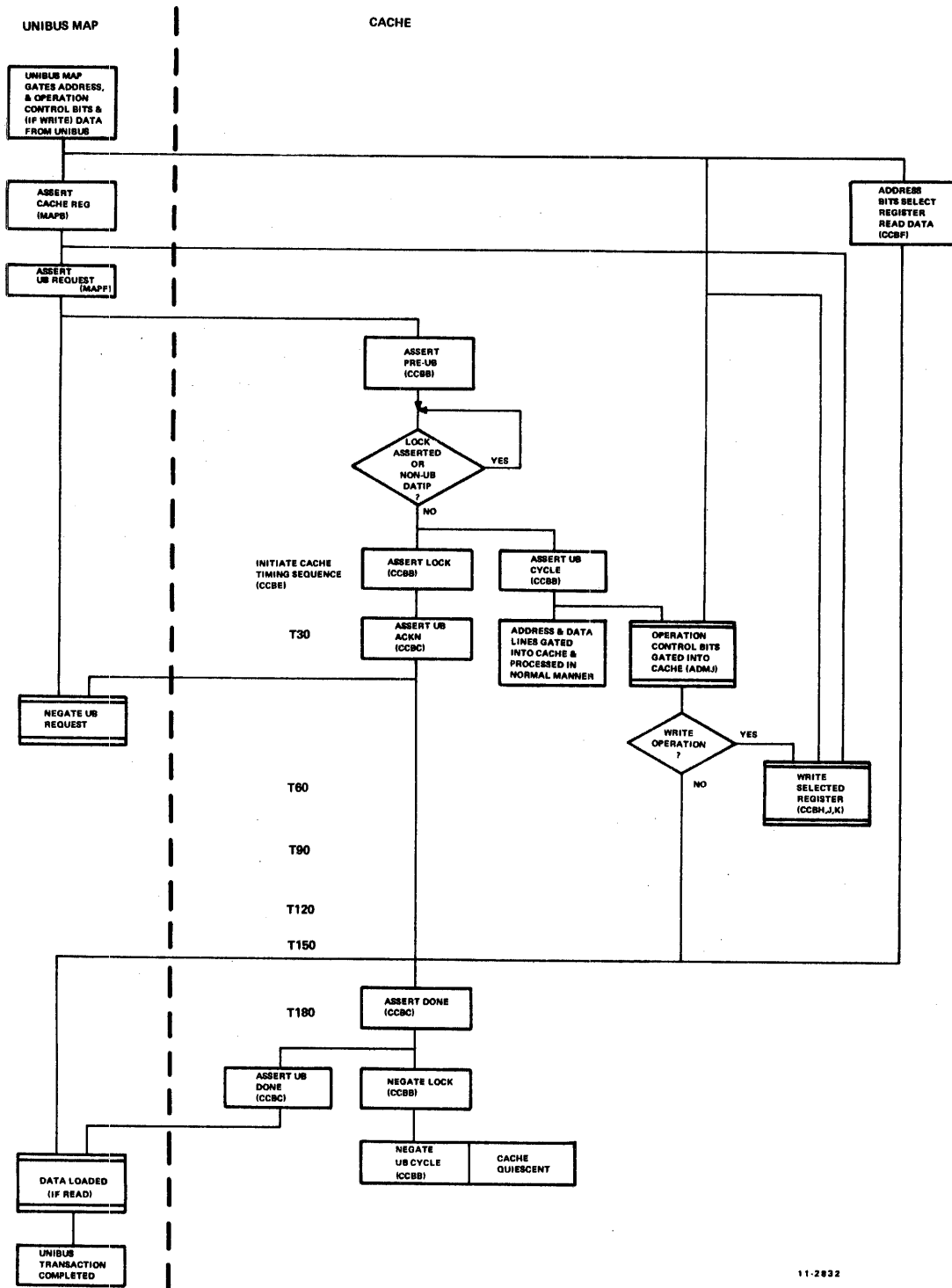
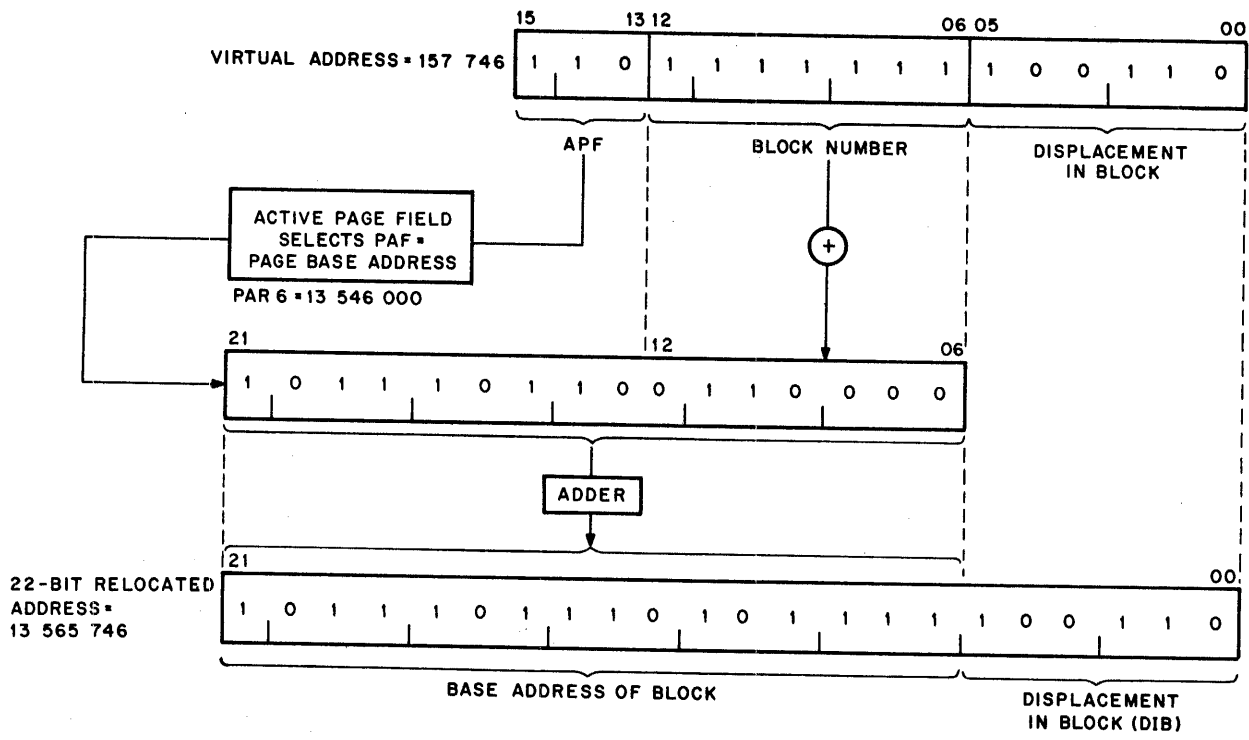


Figure 3-11 Processor Bust-Bend Cycle



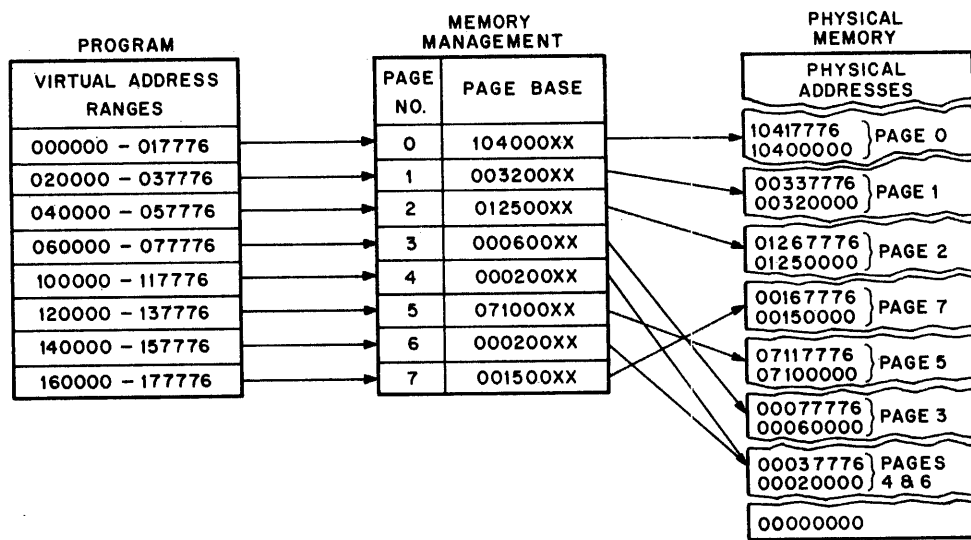
11-2832

Figure 3-15 Register Read and Write



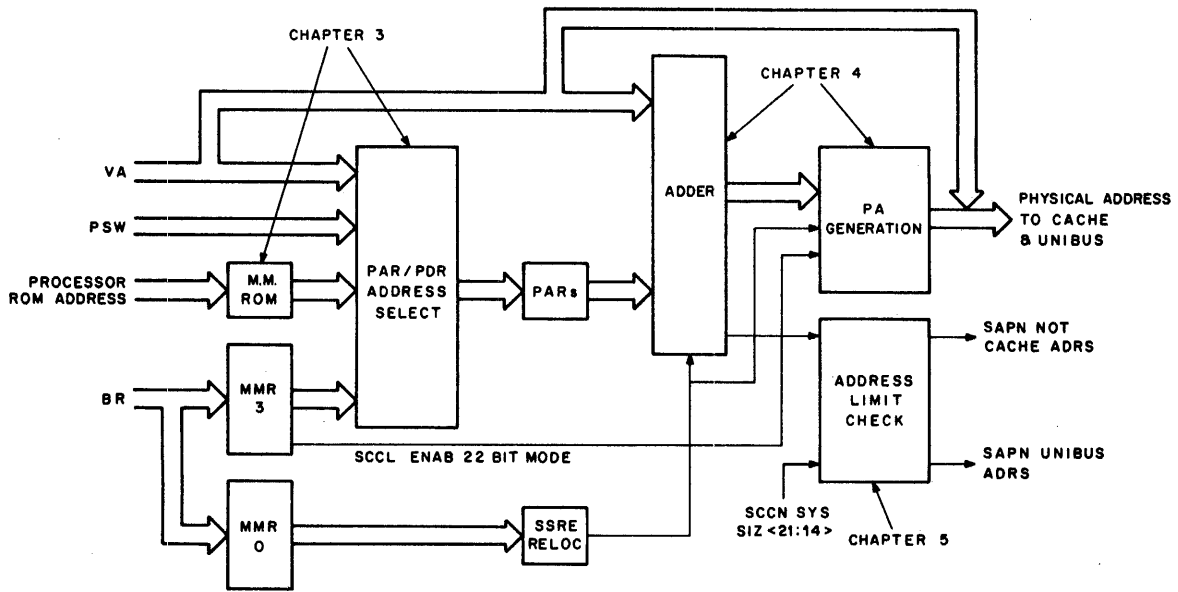
11-4082

Figure 1-2 Construction of PA



11-4016

Figure 1-3 Relocation



H-4009

Figure 2-4 MM Relocation Function

PDP-11/70 MEMORY MANAGEMENT FAMILIARIZATION LAB

1. Set up the appropriate PAR's to complete each of the following steps.
 - a. Map all virtual page zero addresses to the entire upper 4K section of memory in your processor for Kernel, User and Super modes. (do not map into the device register address range).
 - b. Use I Space control at this time.
2. What is the memory size of the processor you are working on _____K.
3. What value did you deposit into the Kernel, User, and Super PAR's? _____8.
4. What value did you deposit into the Kernel, User, and Super PDR's? _____8.
5. Enable the memory management relocation logic for 18 bit mapping.
 - a. How was this done? _____

6. Load address with zero in the switch register.
 - a. Which function or functions has the memory management performed during Load Address? Explain:

6. b. Select Kernel I with the address select switch, depress the Examine key.

(1) What address is displayed _____8

(2) Is this the virtual or physical address?

c. Select Program Physical display. What address is displayed? _____8

Explain: _____

7. Repeat steps 6, 6b, and 6c using the User I and Super I controls.

a. Notice the mode control lights change on the console (top center) as the new mode is entered and operated on.

8. Repeat step 6. This time load address with the value 1000g.

a. Explain what happens this time.

9. Repeat step 6 again. This time load address with 21,000g.

a. Explain what happens now. _____

10. Turn the memory management relocation logic off. Look up the address of the TTY or LA30, printer data buffer; what is it? _____8.

For the PDP-11/70 this address must be prefixed by a 17g.

a. If you deposit the ASCII code of a valid character into this address, the character will print one time.

(1) Try this operation.

11. Enable the memory management logic again. The virtual address of the buffer is 177566. Load this address. Select Kernel I and deposit the character.

a. What happens, and why? _____

b. Which PAR and PDR must be set up?

(1) PAR = _____8

(2) PDR = _____8

c. Do what has to be done to make it work with Memory Management on.

d. There are actually several PAR values which will cause the printer data buffer address to be output from memory management. When using 18 bit mapping an address is defined as a Unibus address if bits _____ are all 1's. If this is true, the bits 21:18 are forced to 1's, even though they might have contained some other value after relocation. In a sense, Unibus addressing may be relocated twice; once to the upper 4K of the 18 bit addressing space, and once to the upper 4K of the 22 bit addressing space. To verify this, load Kernel I PAR7 with the constant required to relocate Kernel I address 177566g to physical address 00777566g.

Kernel I PAR7 = _____

Deposit the code for an ASCII character in that address. Note that the character is printed. Select PROG PHY, and note the 22 bit address displayed.

22 bit address = _____

12. Twenty two bit mapping is enabled by setting bit 4 of memory management register 3. (Refer to the KB11B Processor Manual, Section IV, Figure 9-6) For memory addresses in the range 0-124K, there is no difference between 18 bit mapping and 22 bit mapping. Valid addresses above 124K were relocated to the 4K device addresses under 18 bit mapping. Under 22 bit mapping, addresses up to 1920K are treated as memory addresses. The 128K addresses with address bits 21:18 equal to all 1's are treated as Unibus addresses. The upper 4K

12. of these are the device addresses, the remaining 124K address the Unibus Map. After relocation; the address is determined to be a Unibus address, the leading 1's are stripped off and bits 17:00 are used as the 18 bit Unibus address.
- Enable 22 bit mapping.
 - Repeat step 6 again. Is the operation different from the previous execution of step 6? _____
 - Repeat step 11. Is the printer data buffer addressed? _____. The value loaded into PAR7 in step 1101 causes the memory management output to be a non-Unibus address. Change it so that the buffer register will be addressed.
13. To use D-Space memory management register three must be set up to specify the mode.
- Enable Kernel D-Space. Repeat step 6.
 - Explain what happens and why? _____

 - Correct the problem, and see that Kernel D-Space works.
14. Analyze the following simple program. Deposit it into the specified location. Do what is needed to make it work with the memory management enabled.

```

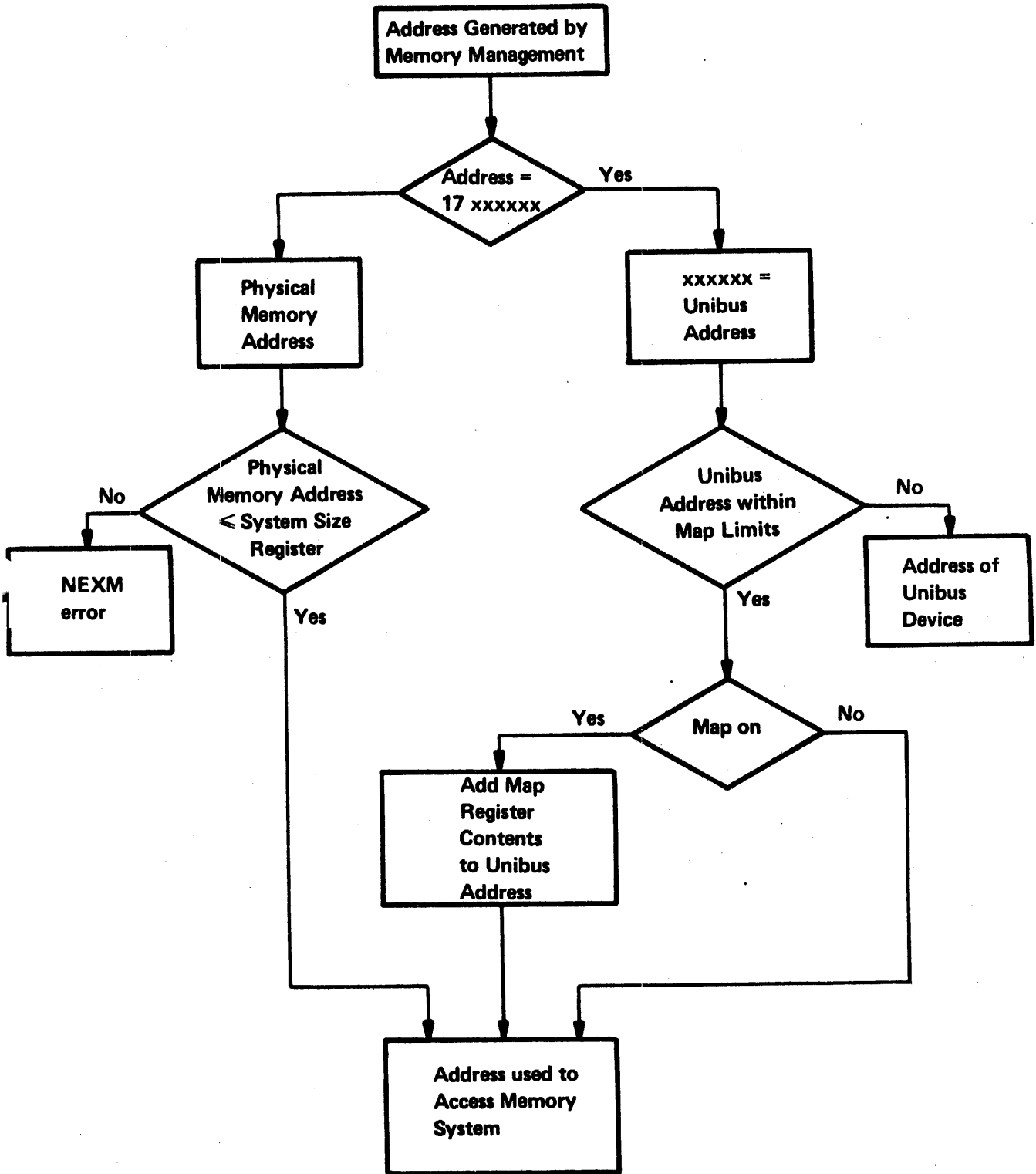
20000g    MOV#1,@#777572
          2    000001
          4    177572
          6    BR

```

ANSWERS TO QUESTIONS

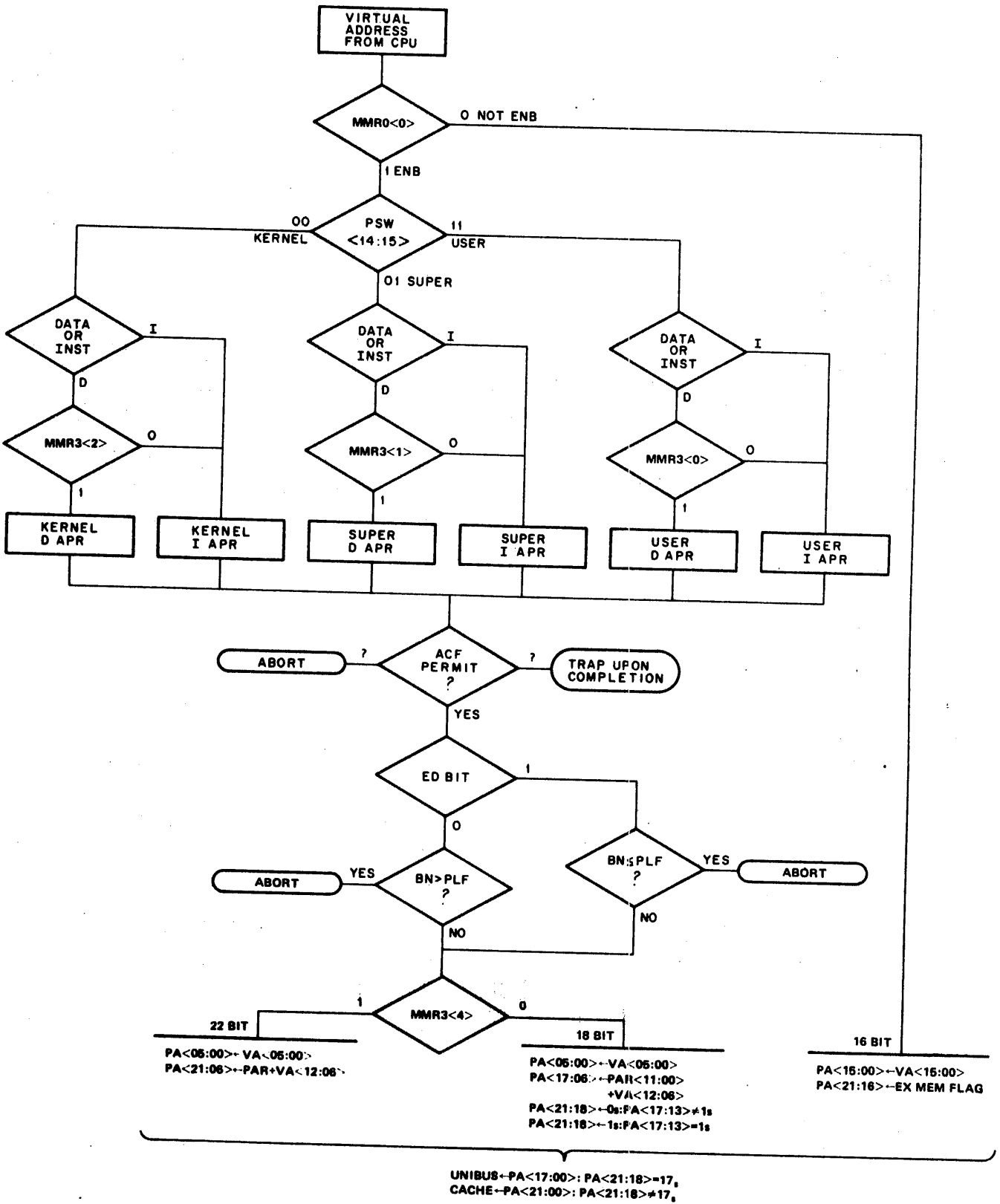
<u>STEP NUMBER</u>	<u>ANSWERS</u>
3	Core Range PAR's 32K- 1600g 40K- 2200g 48K- 2600g 56K- 3200g 64K 3600g
4	PDR's = 077406g
5	Deposit a one into SR0 bit 0
6a	None; KT11-C only deals with address from the BAMX.
6b(1)	Zero
6b(2)	Virtual
6c	PAR+0: This is the physical address after the PAR0 and the virtual addresses were added.
8a	The virtual address is 1000. This address is mapped to the specified physical ad- dress range.
9a	Memory Management abort. The virtual address is in page two. Page two hardware is not set up.
10	777566g
11a	Memory Management abort. Vir- tual page 7 is referenced and the hardware is not set up.
11b	Kernel PAR7 and PDR7.
11b(1)	PAR = 177600g.
11b(2)	PDR = 077406g.
11d	17:13 Kernel I PAR7 = 007600g 22 bit address = 17777566
12b	No
12c	No
13	Memory Management abort. The Kernel D PAR and PDR are not set up correctly.

PDP 11/70 Address Handling Format



TR-1022

PDP-11/70 MEMORY MANAGEMENT FLOW CHART



PDP-11/70 MEMORY MANAGEMENT

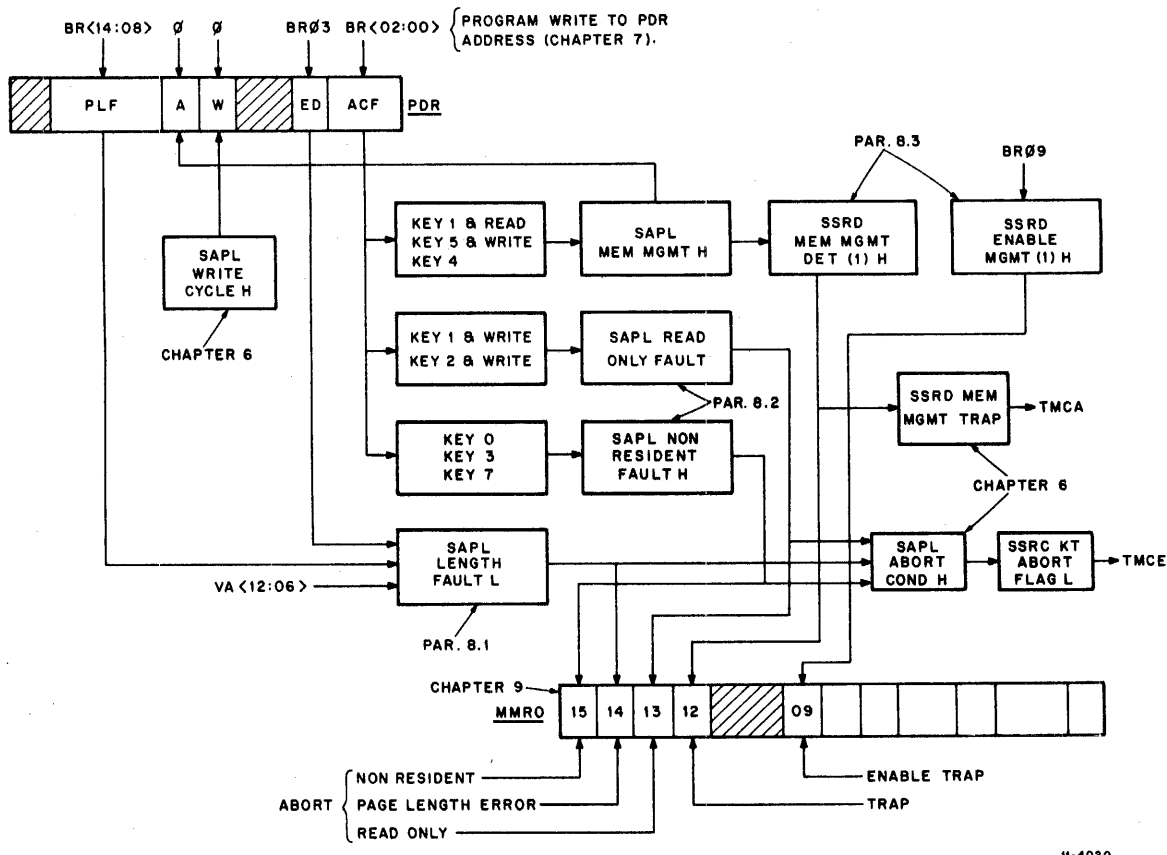
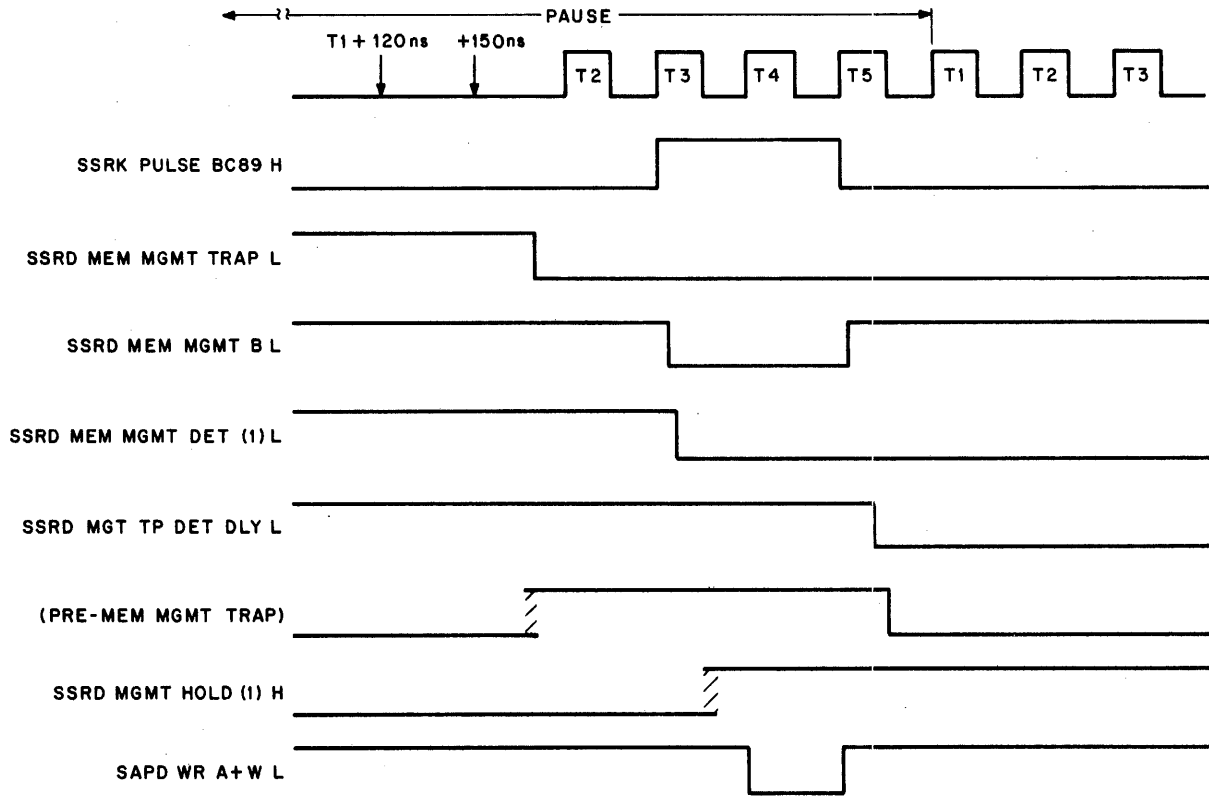


Figure 8-1 Traps and Aborts

11-4020



11-4022

Figure 8-2 Trap Timing

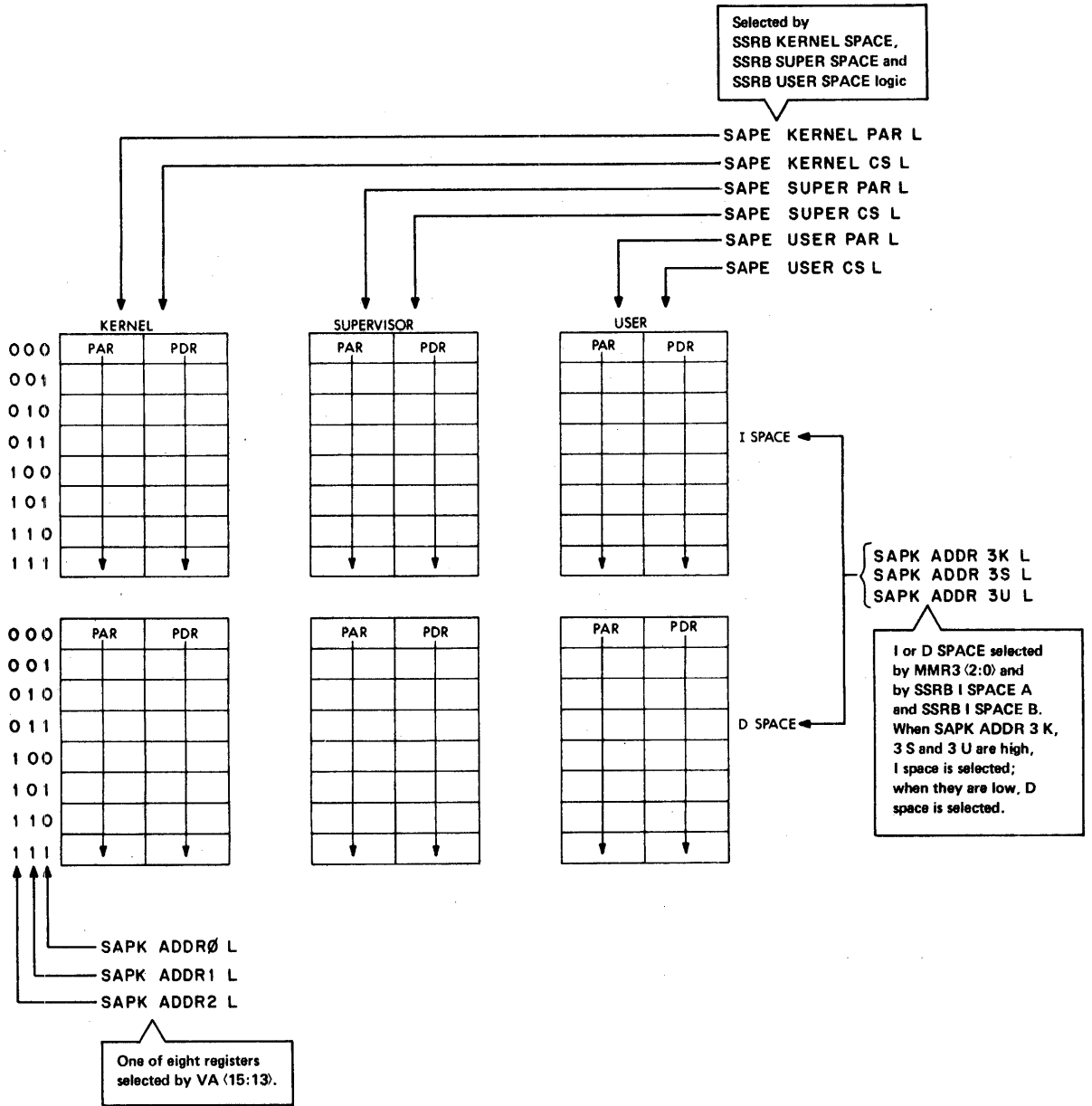
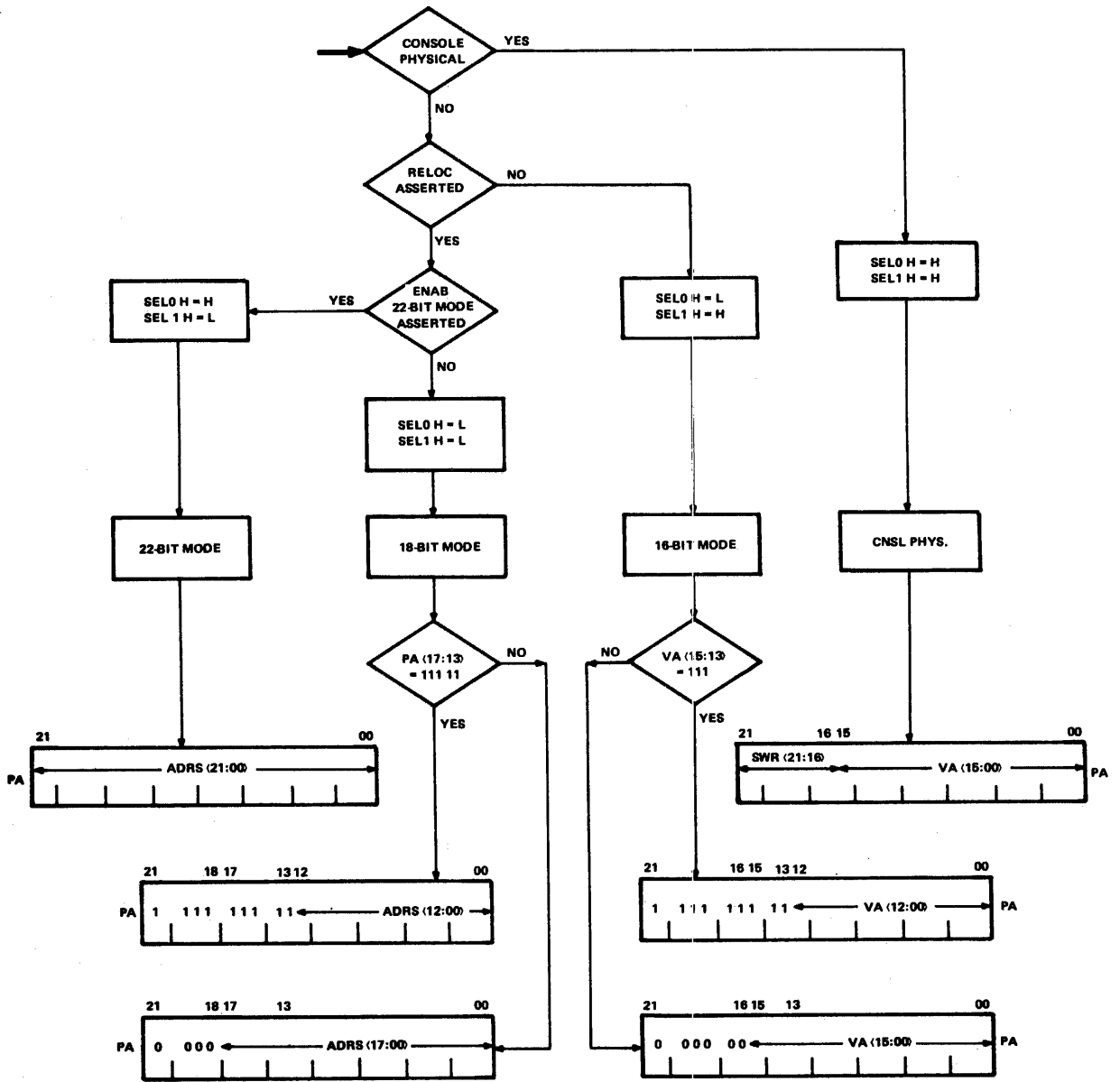
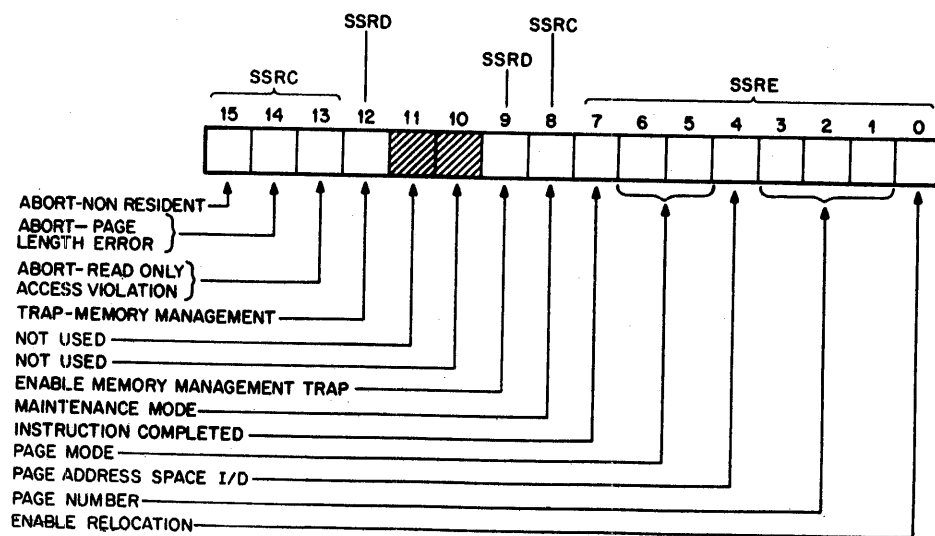


Figure 3-1 Addressing of PAR/PDR



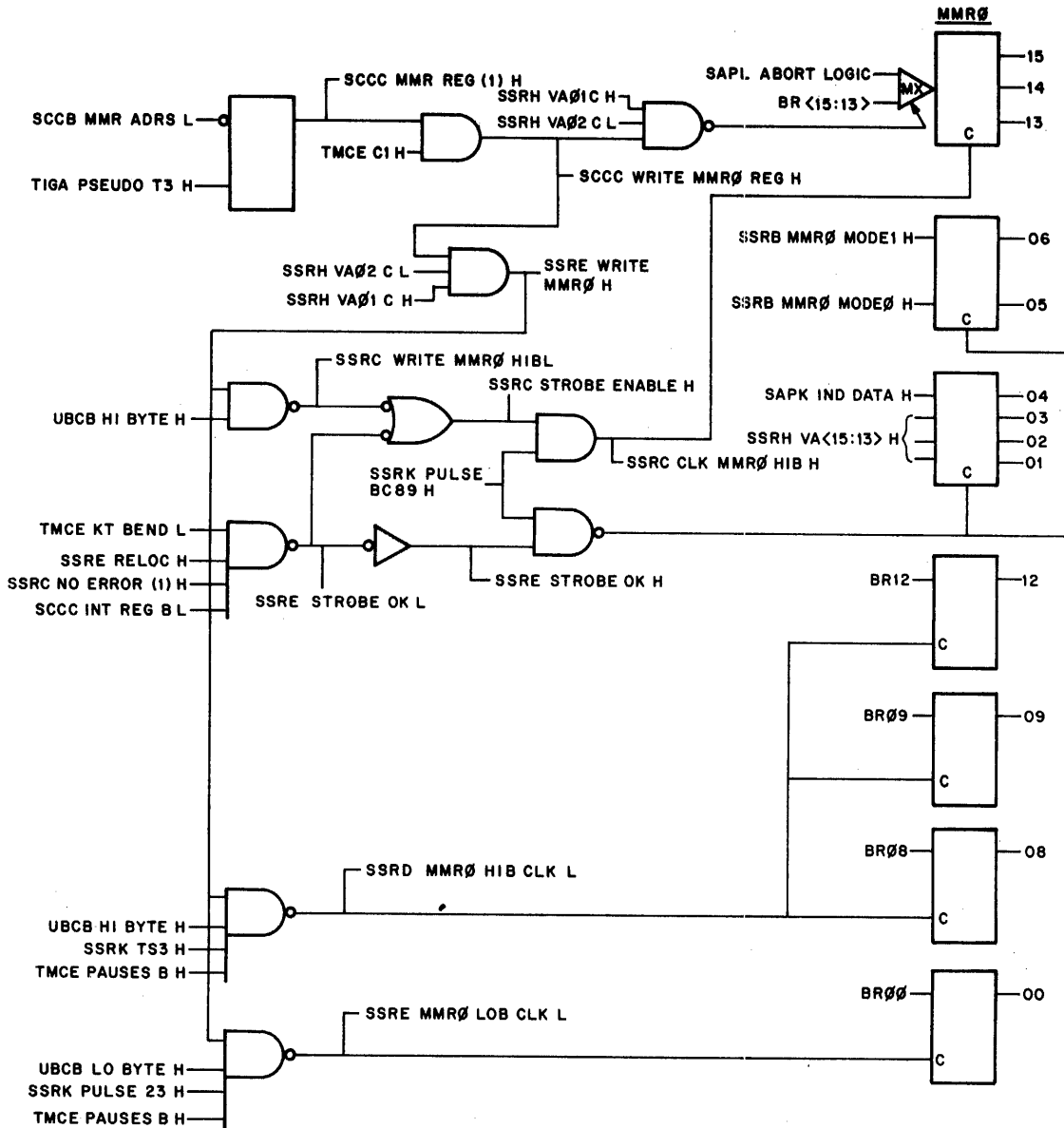
11-4011

Figure 4-10 Generation of Physical Address



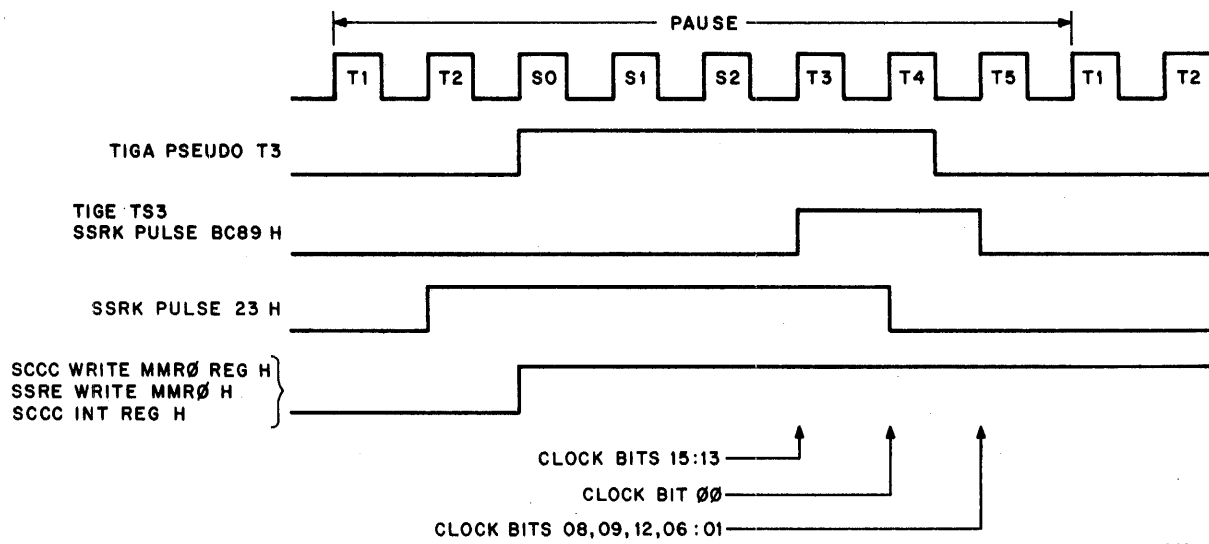
11-4046

Figure 9-1 MMR0



11-4014

Figure 9-2 Clocking of MMR0



11-4021

Figure 9-3 MMR0 Write Timing

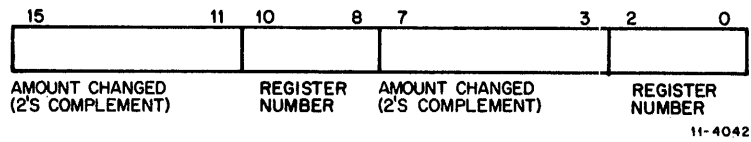


Figure 9-4 MMR1

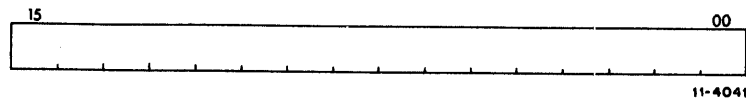


Figure 9-5 MMR2

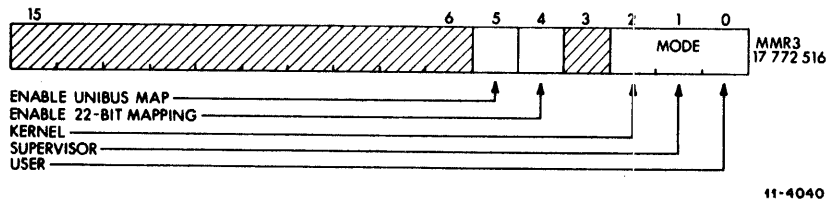
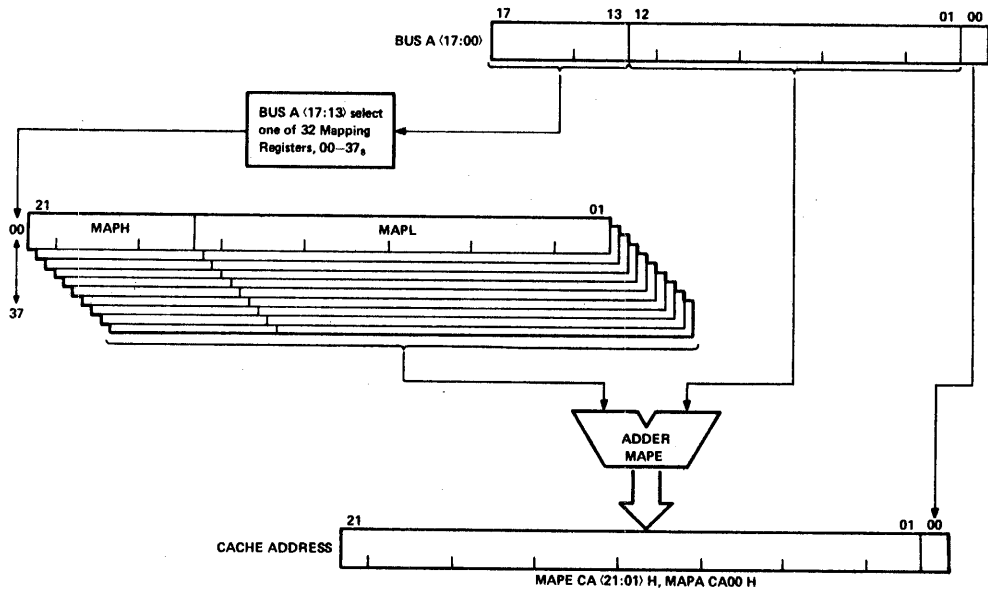


Figure 9-6 MMR3



11-4029

Figure 1-1 Construction of the PA

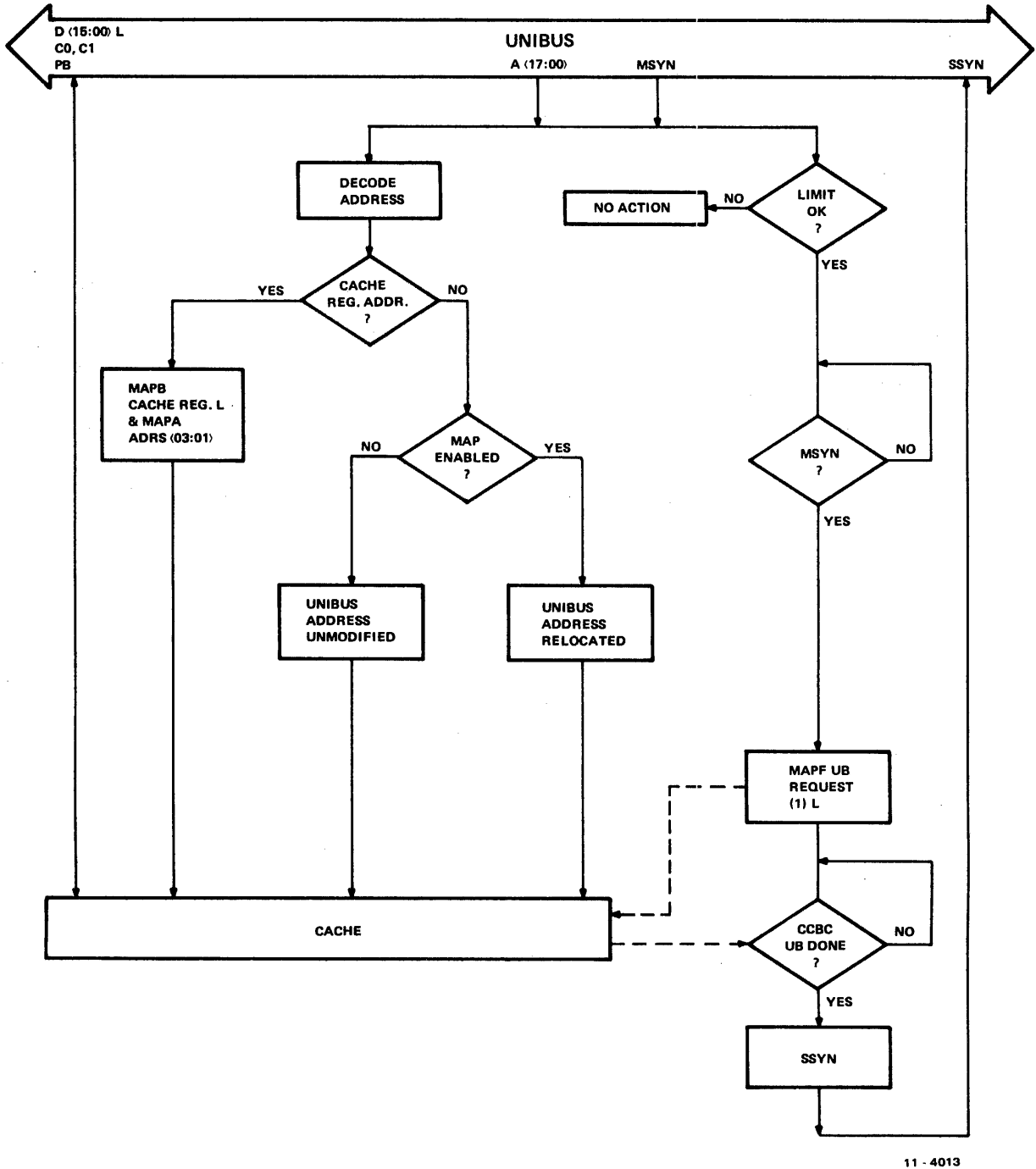
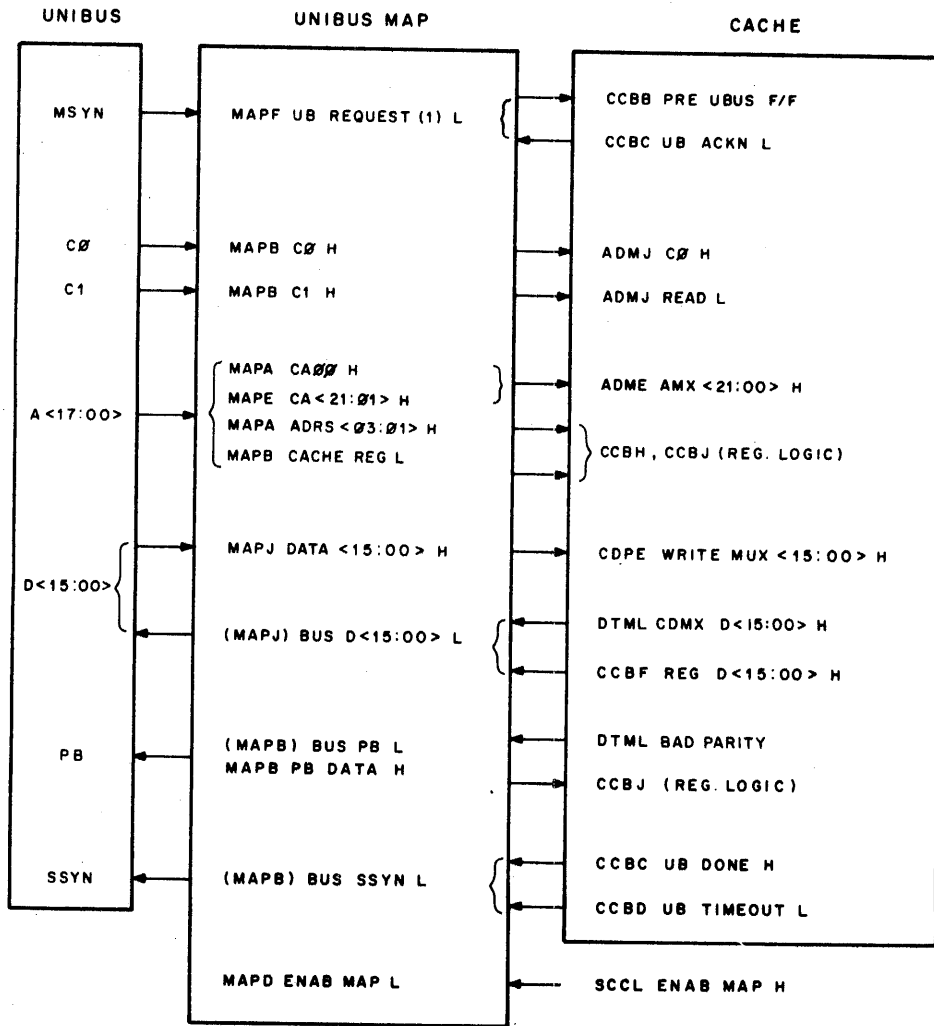
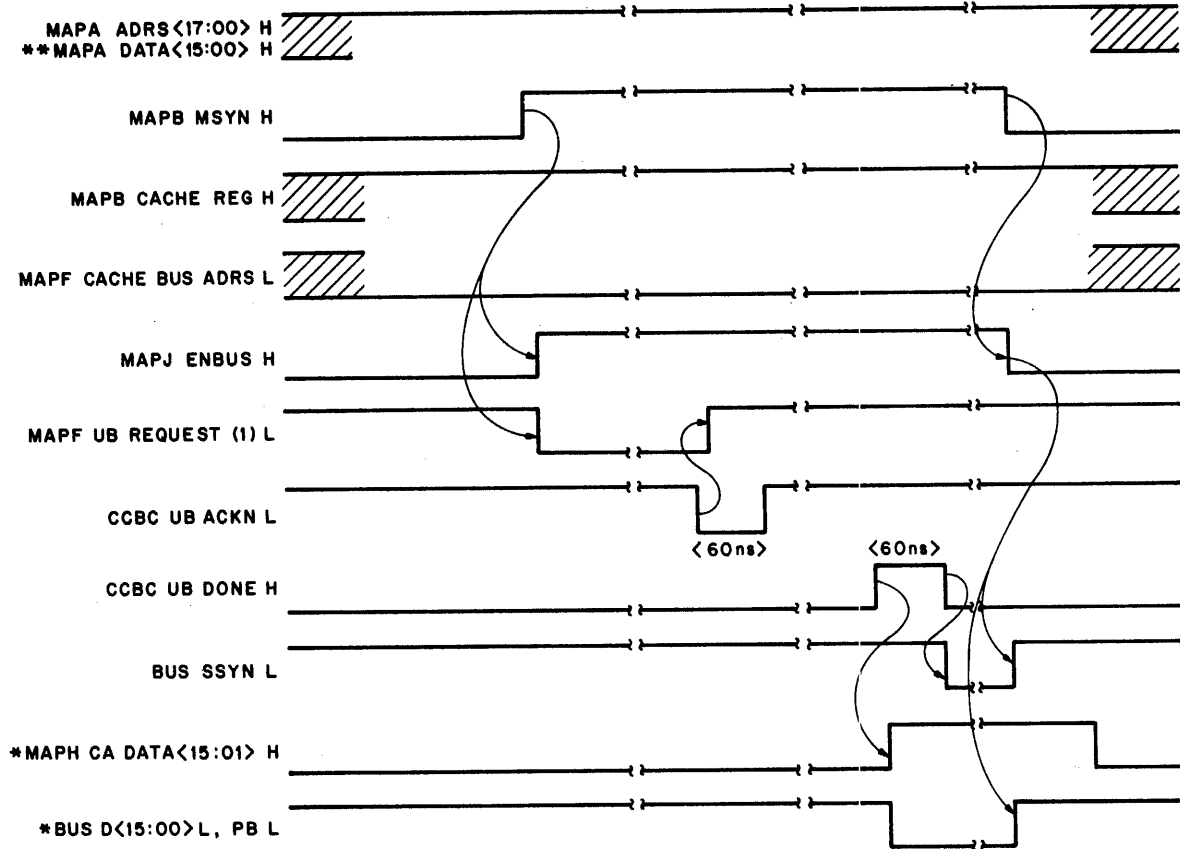


Figure 2-1 Unibus Map Flowchart



11-4052

Figure 2-3 Unibus Map Interface



*NOTE: DATI or DATIP only.
 **NOTE: DATO or DATOB only.

11-4025

Figure 2-4 Cache/Unibus Transactions

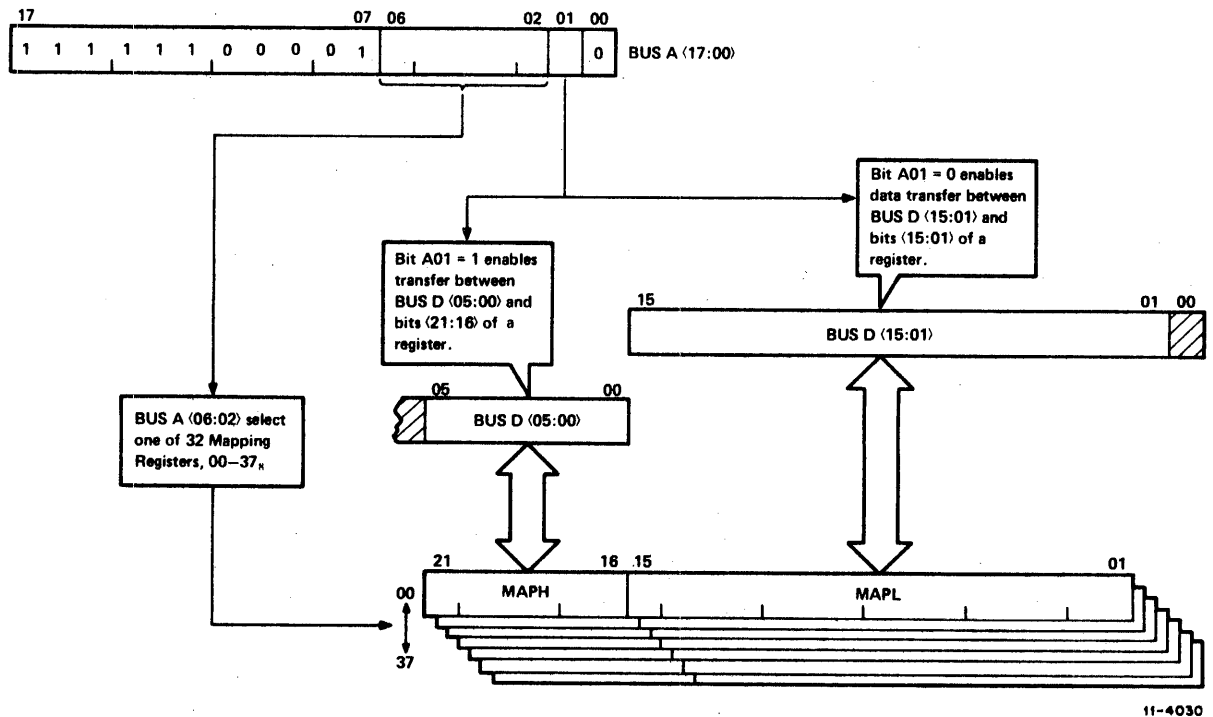


Figure 3-1 Addressing of UB Map Register

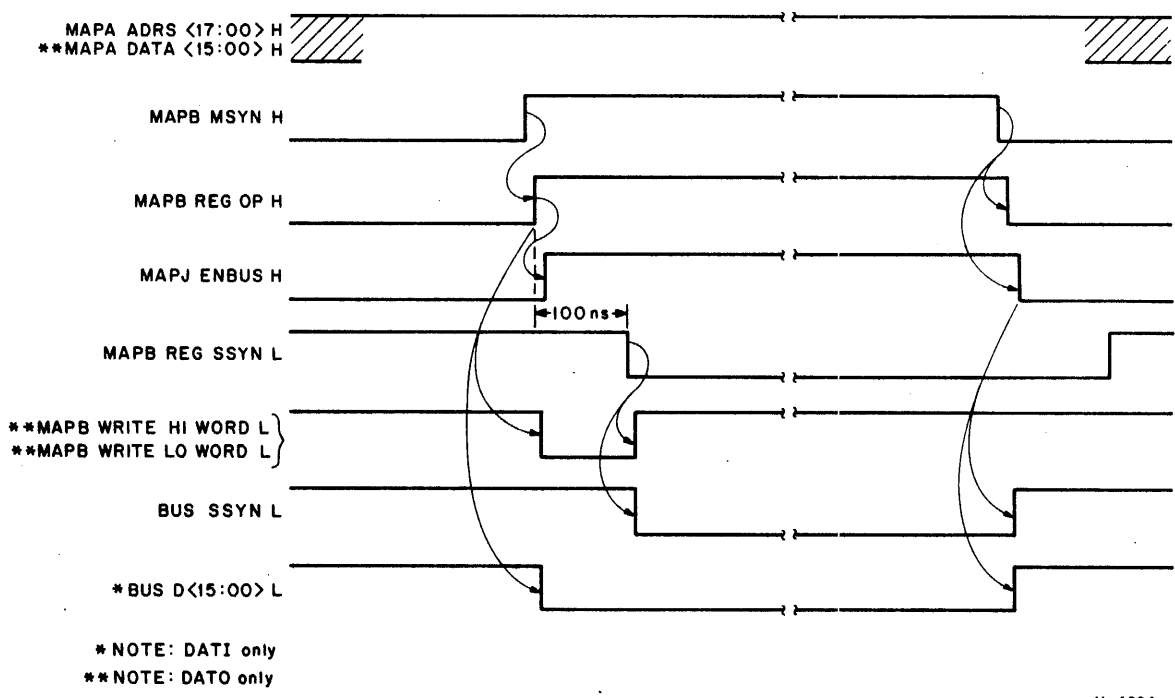
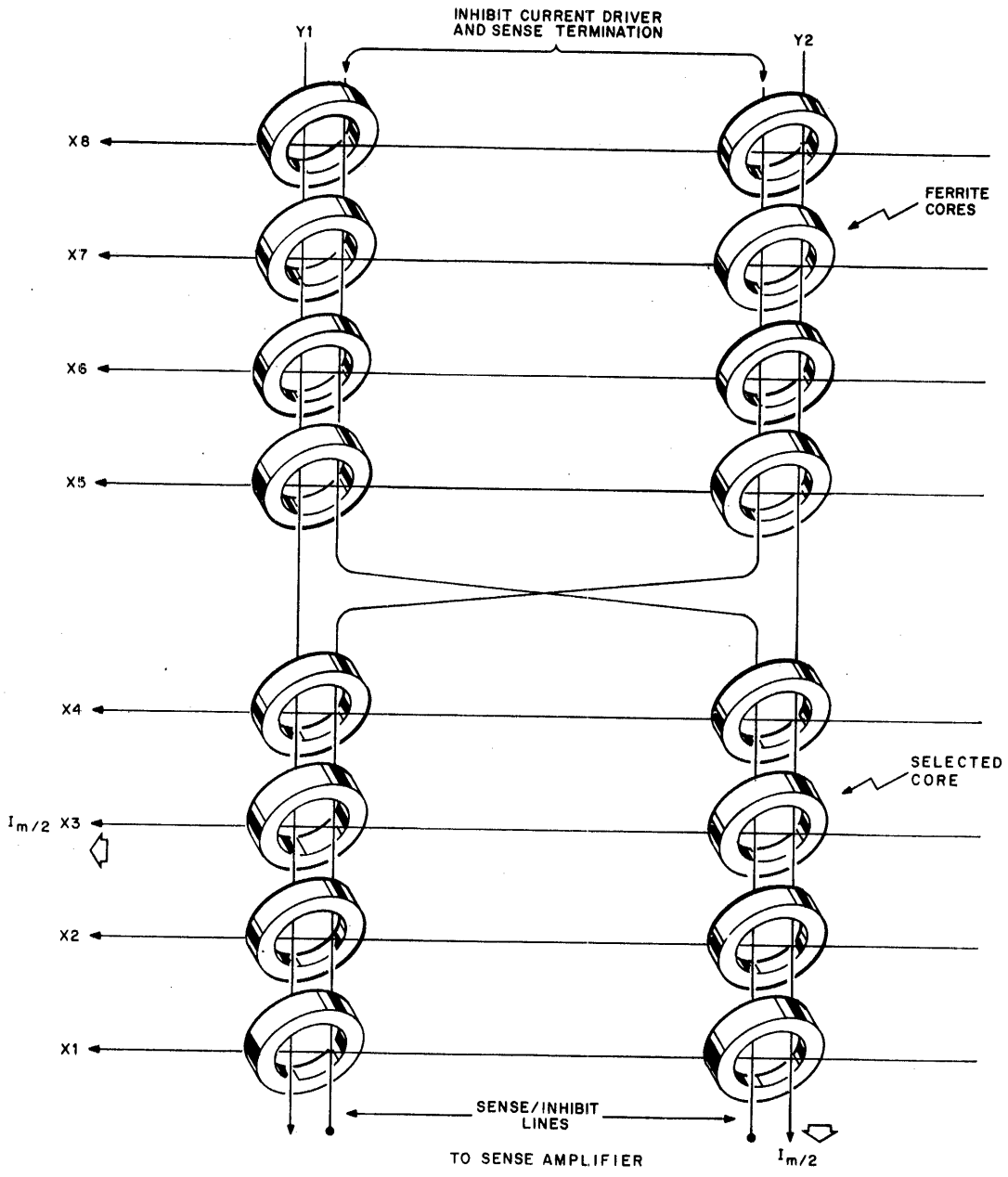


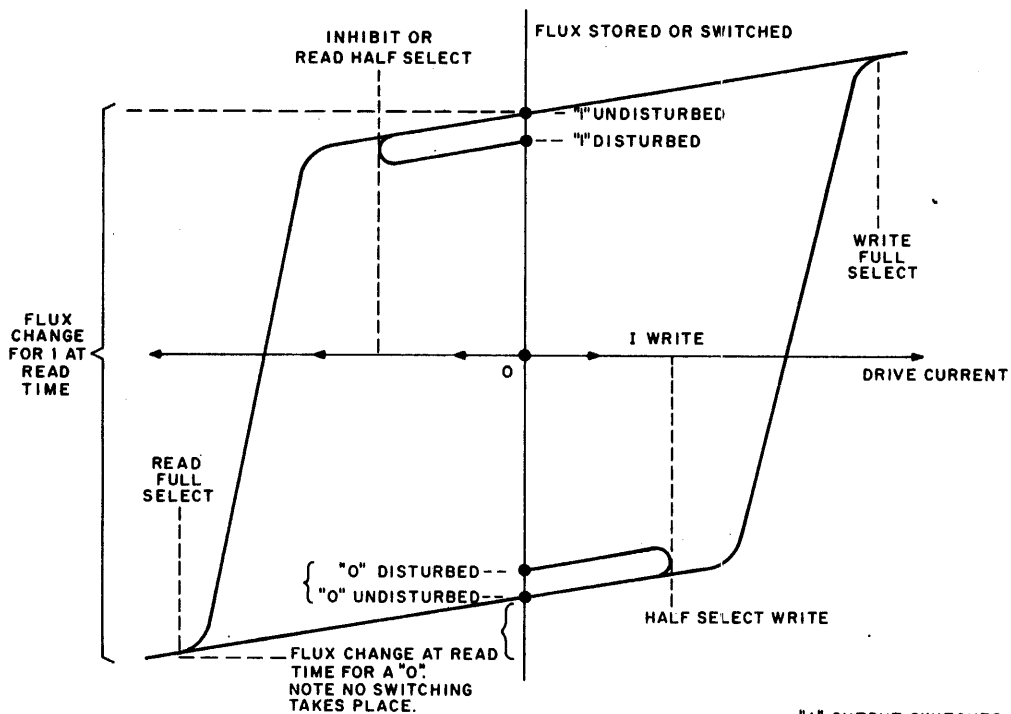
Figure 3-2 UB Map Register Read/Write



11-1790

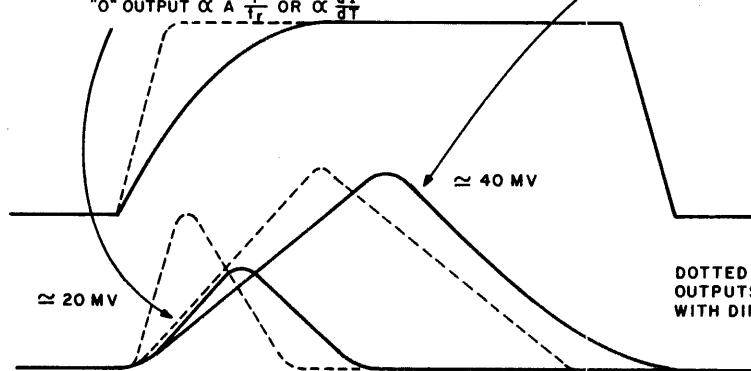
Figure 4-1 Three-Wire Memory Configuration

HYSTERESIS LOOP FOR CORE



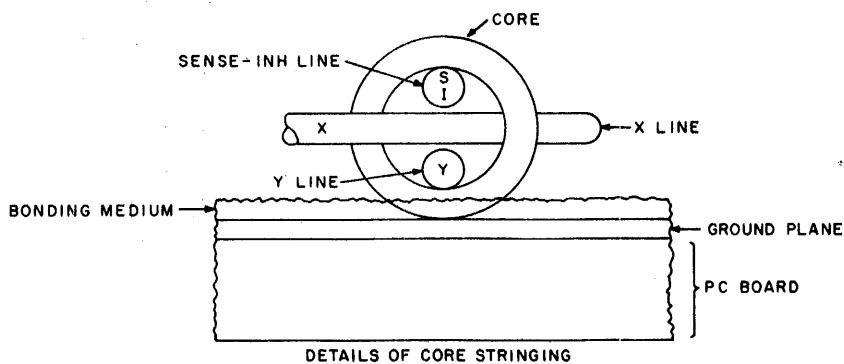
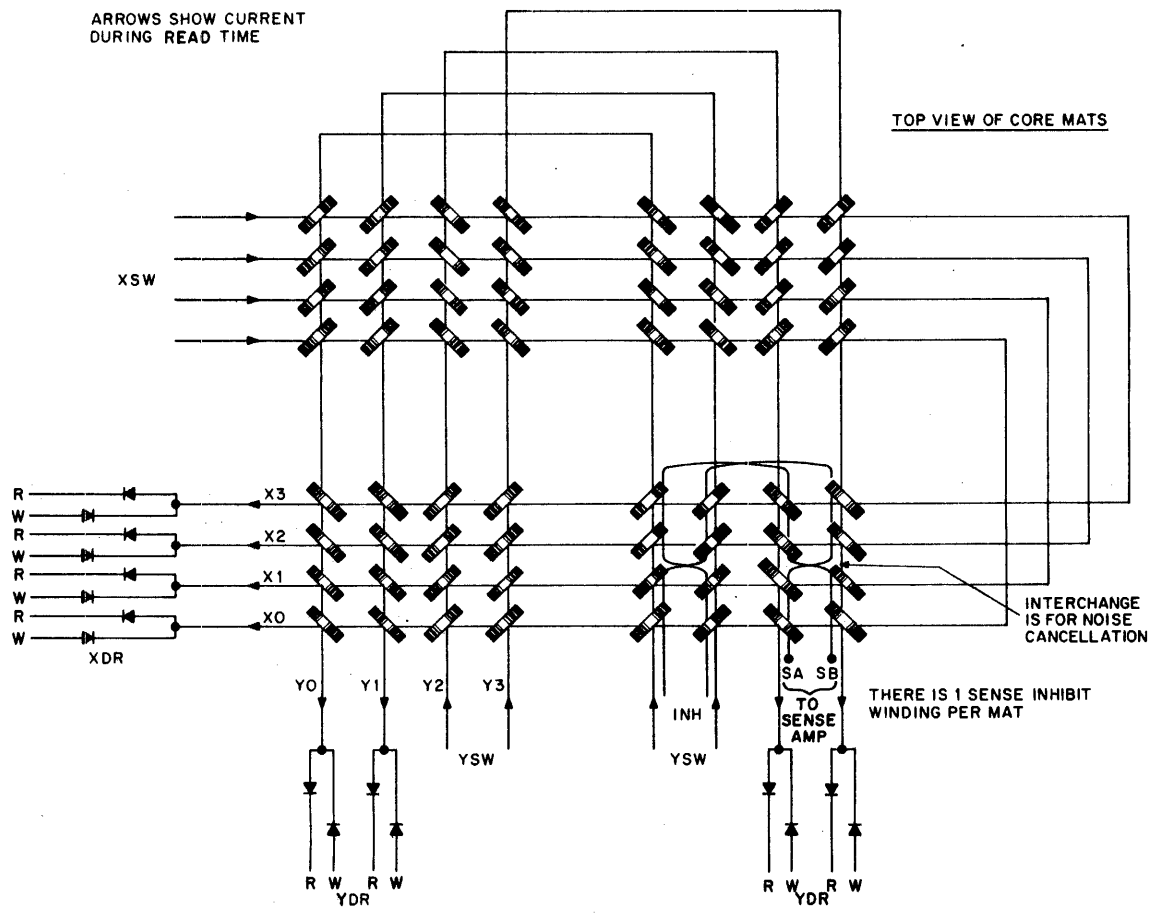
"0" OUTPUT COMES DURING I RISE TIME AND IS A FUNCTION OF IT AND CURRENT AMPLITUDE.
 "0" OUTPUT $\propto \frac{1}{T_r}$ OR $\propto \frac{dI}{dt}$

"1" OUTPUT SWITCHES AT THE CORE TIME CONSTANT AND IS PRIMARILY DEPENDENT ON CURRENT AMPLITUDE. IT WILL SWITCH FASTER AND GROW AS RISE TIME IS DECREASED.



11-00868

Figure 4-2 Hysteresis Loop for Core



11-1791

Figure 4-3 Three-Wire, 3D Memory - Four Mats of a 16-Word by 4-Bit Memory

MJ11 MEMORY OPTIONS

MJ11-AE: 32K words

MJ11-AA: Memory Box with Controller and Transceiver, 32K words, 110 V.

AB: Memory Box with Controller and Transceiver, 32K words, 220 V.

MJ11-AG: Memory Box with Controller and Transceiver, 128K words, 110 V.

AH: Memory Box with Controller and Transceiver, 128K words, 220 V.

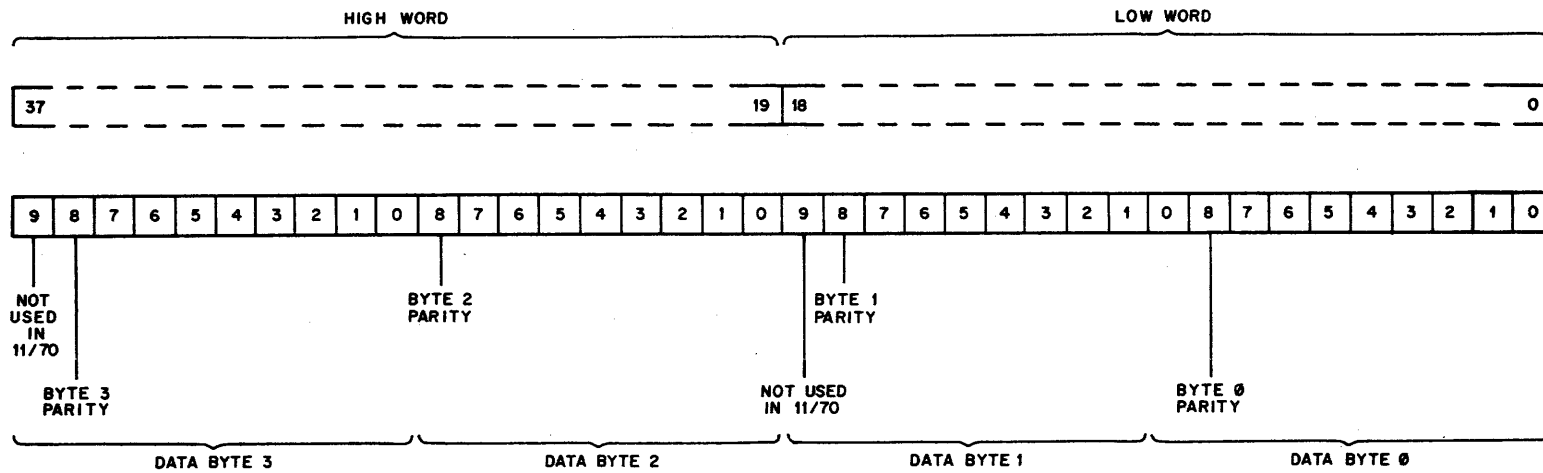
MJ11-AC: Memory Cabinet and one Memory Box with Controller and Transceiver, 128K words, 110 V.

AD: Memory Cabinet and one Memory Box with Controller and Transceiver, 128K words, 220 V.

Maintenance Spares (not for expansion purposes)

MJ11-AM: 16K words

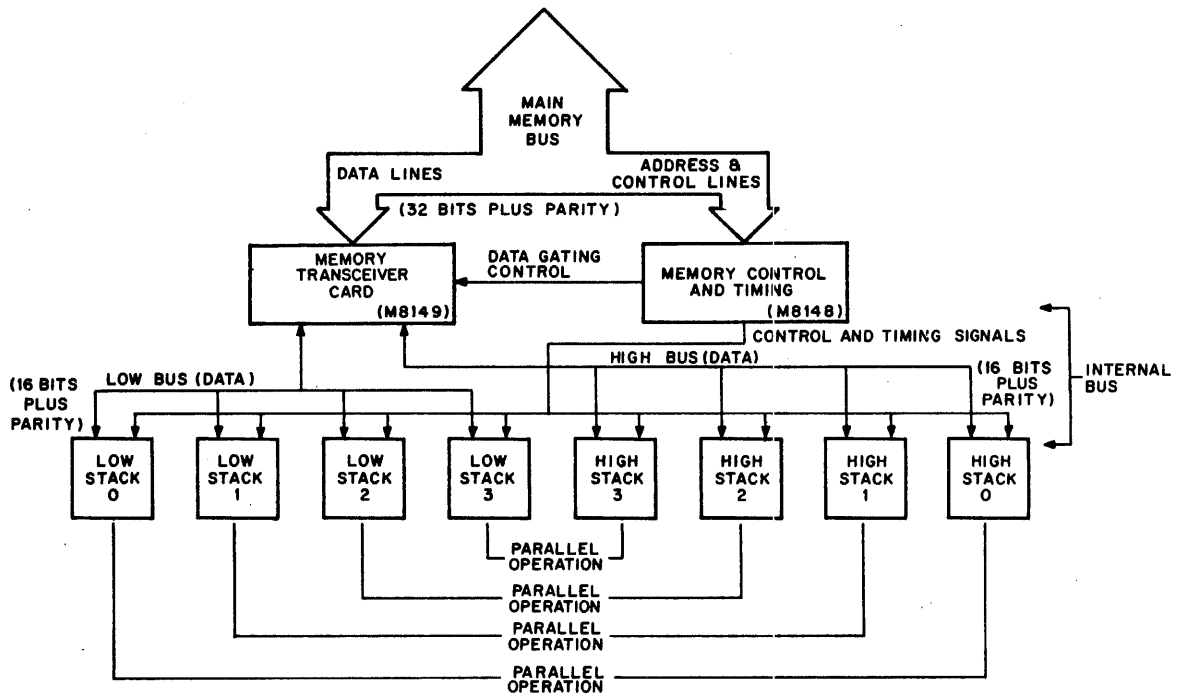
TR-0916

**NOTES:**

BIT 9 of DATA BYTES 3 and 1 are implemented on the MAIN MEMORY BUS but are not used in the PDP-11/70.

BIT 8 of each DATA BYTE is the byte parity bit in PDP-11/70 applications.

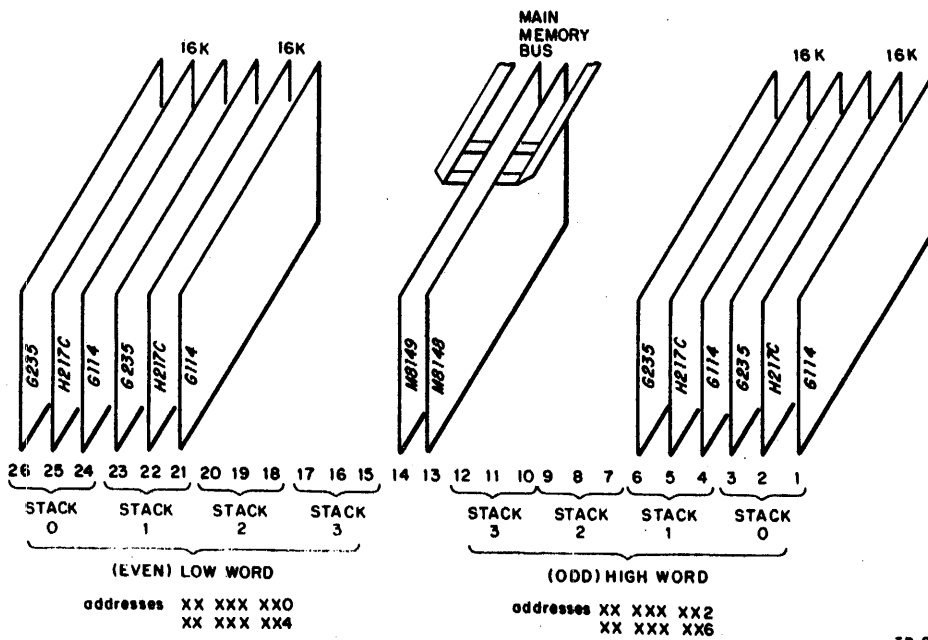
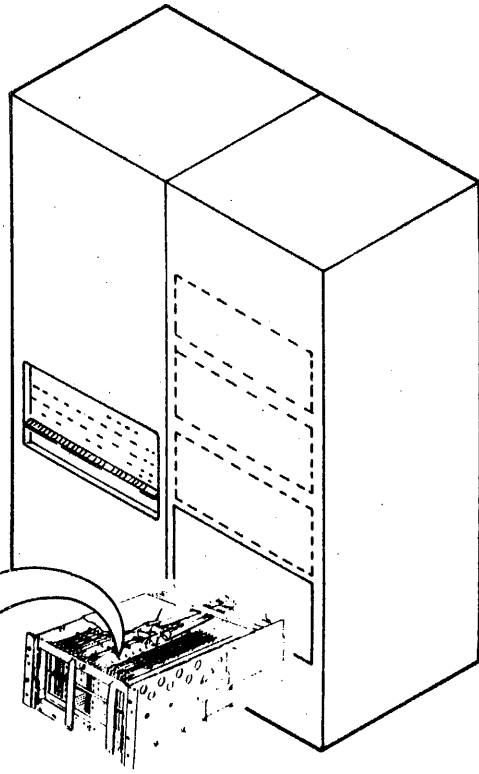
Figure 1-1 Data Word Organization



11-2989

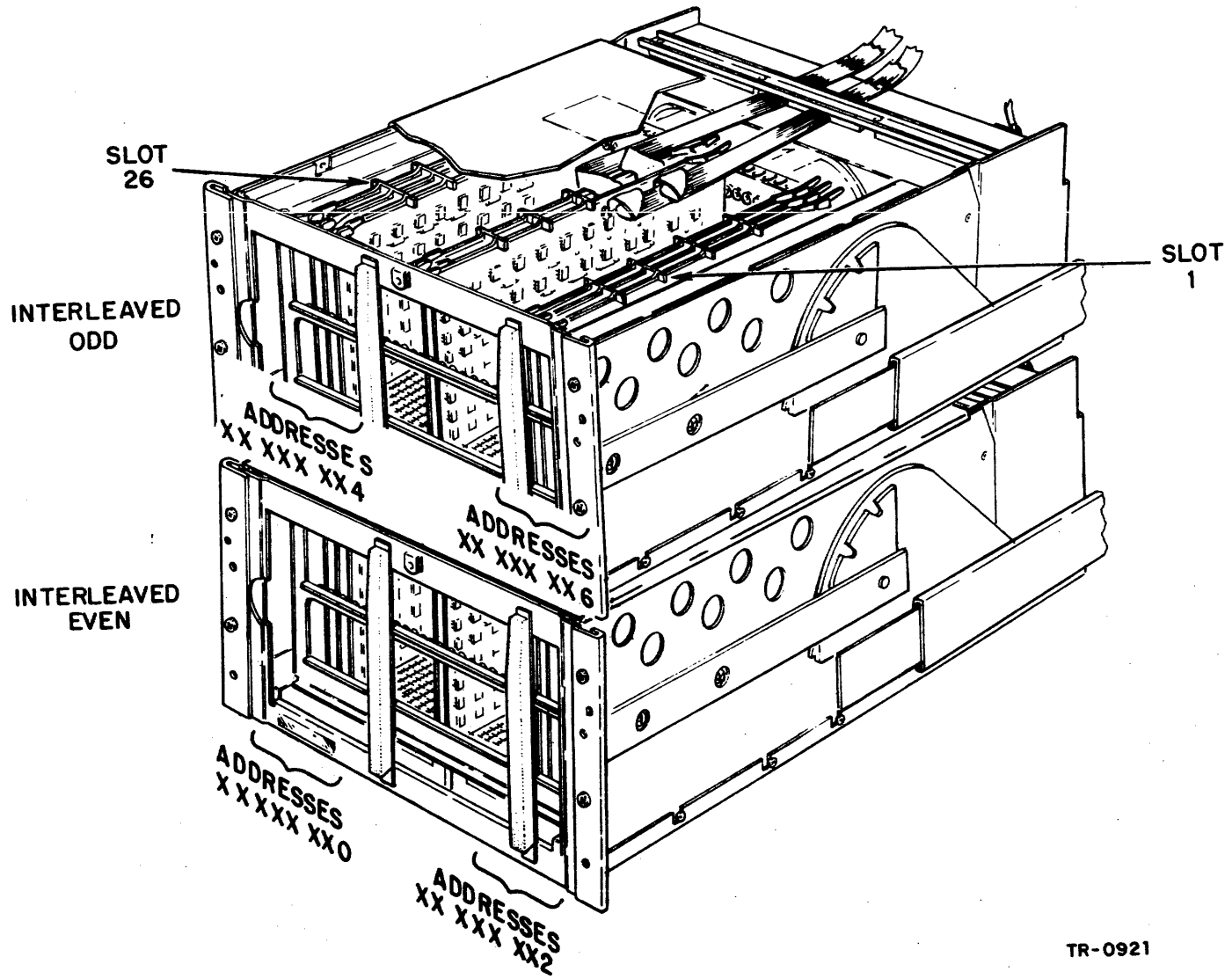
Figure 1-9 MJ11 Simplified Block Diagram

MJ-II MEMORY
 MINIMUM CONFIGURATION 64K WORDS



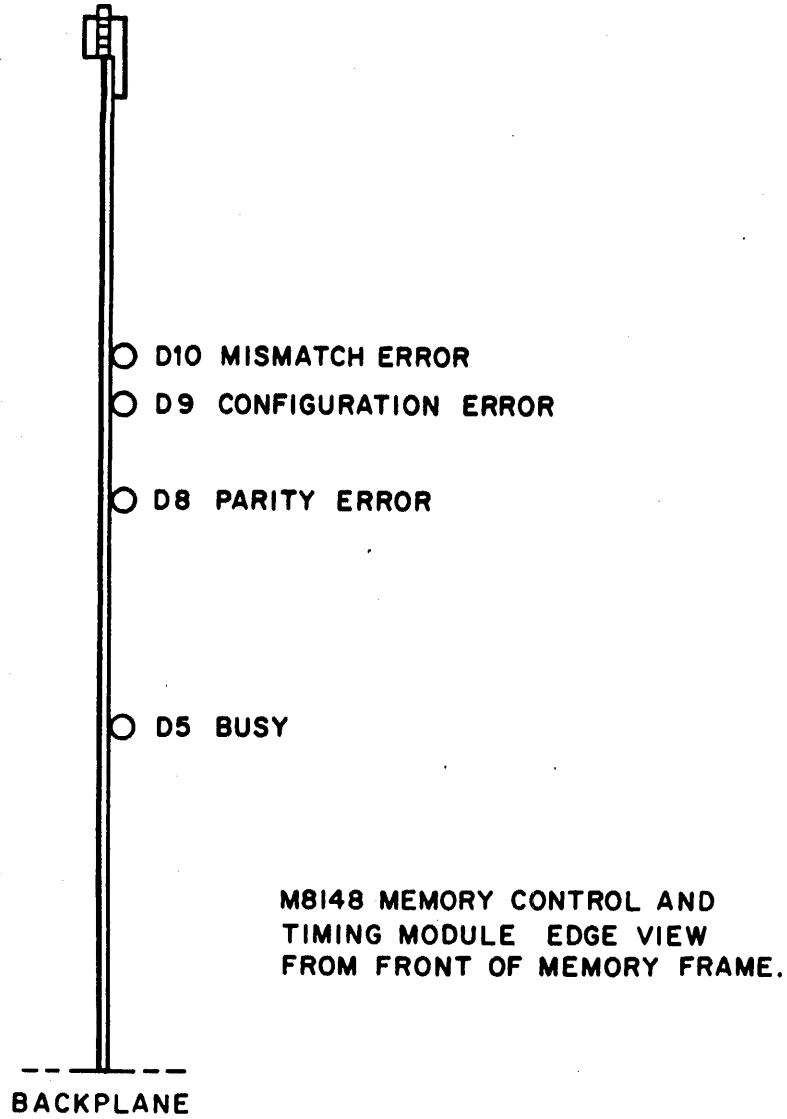
TR-0920

MJ-11 INTERLEAVED MEMORY



TR-0921

TOP OF MODULE



11-2972

Figure 3-3 Location of Memory Controller Status LED Indicators

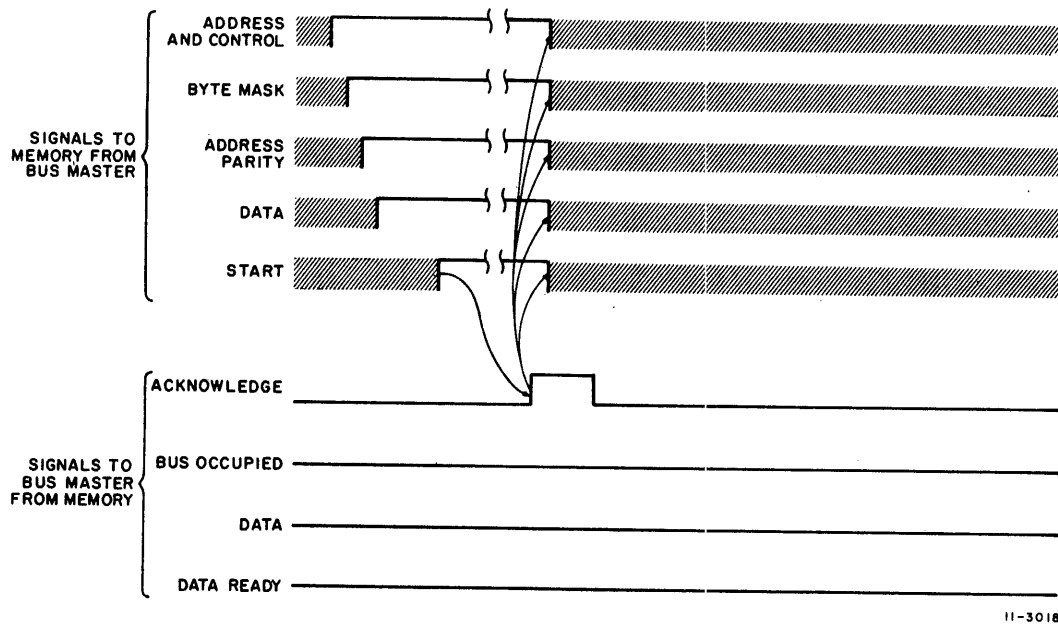


Figure 2-2 Write Operation - Main Memory Bus Protocol

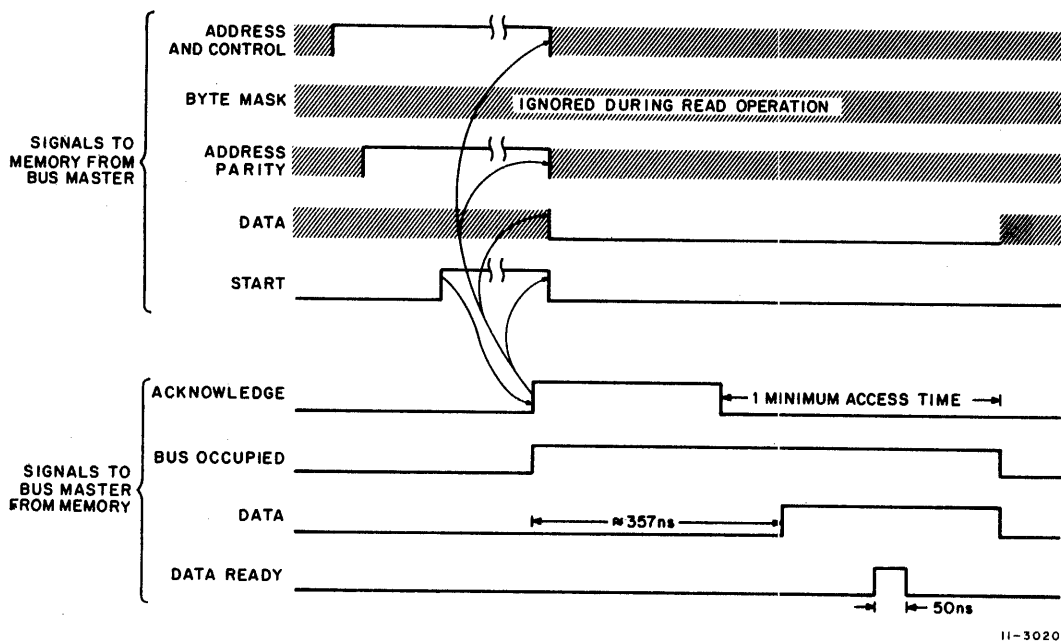
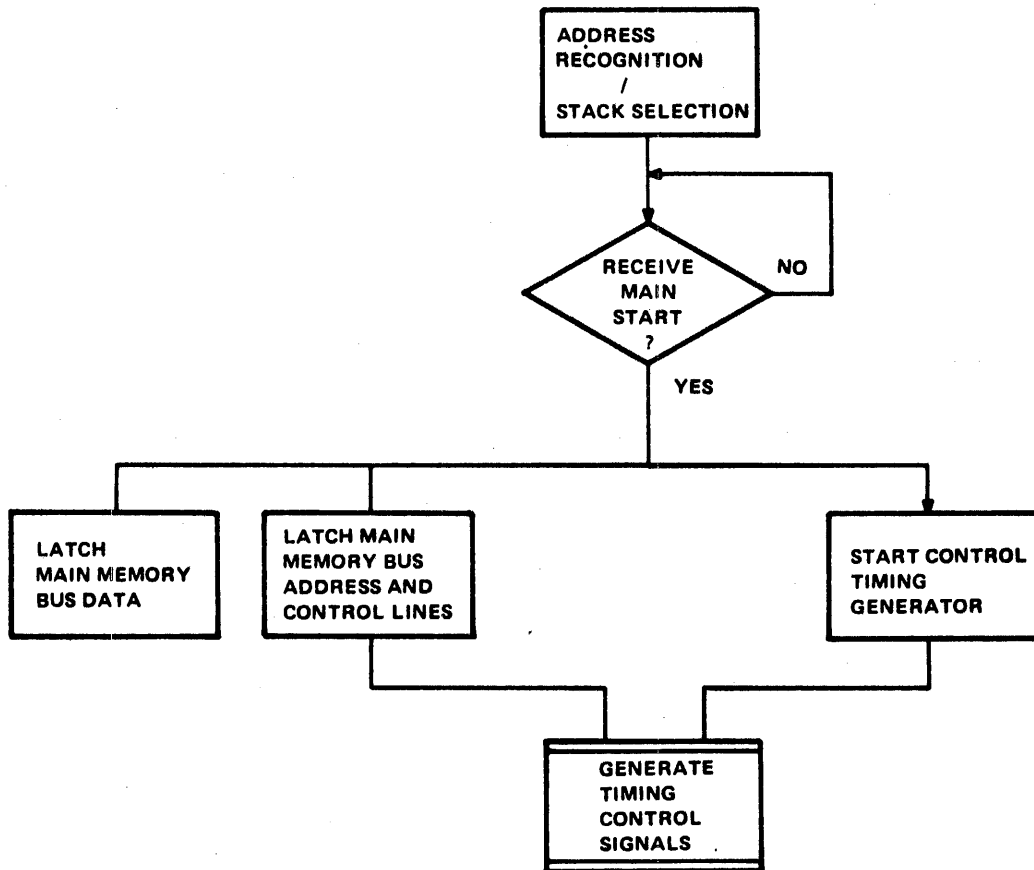
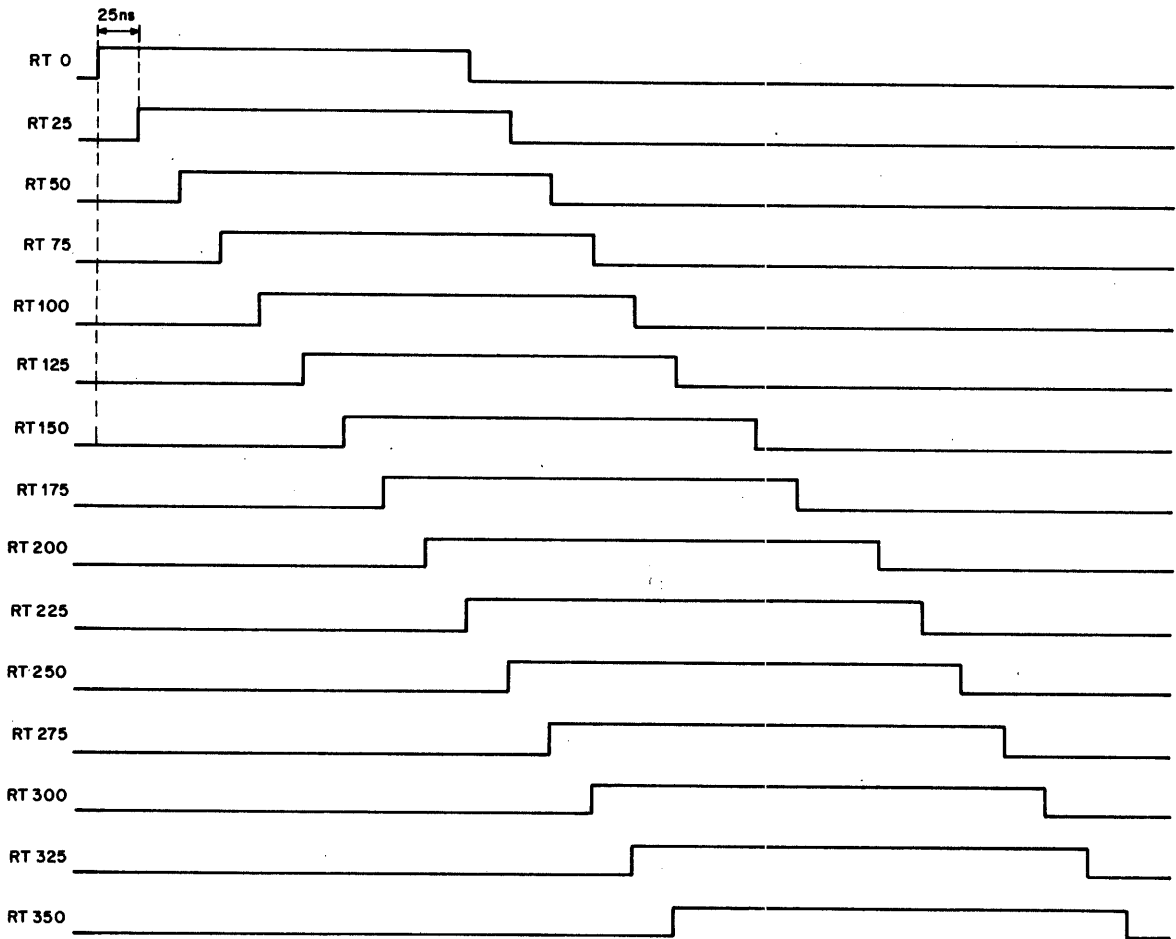


Figure 2-3 Read Operation - Main Memory Bus Protocol



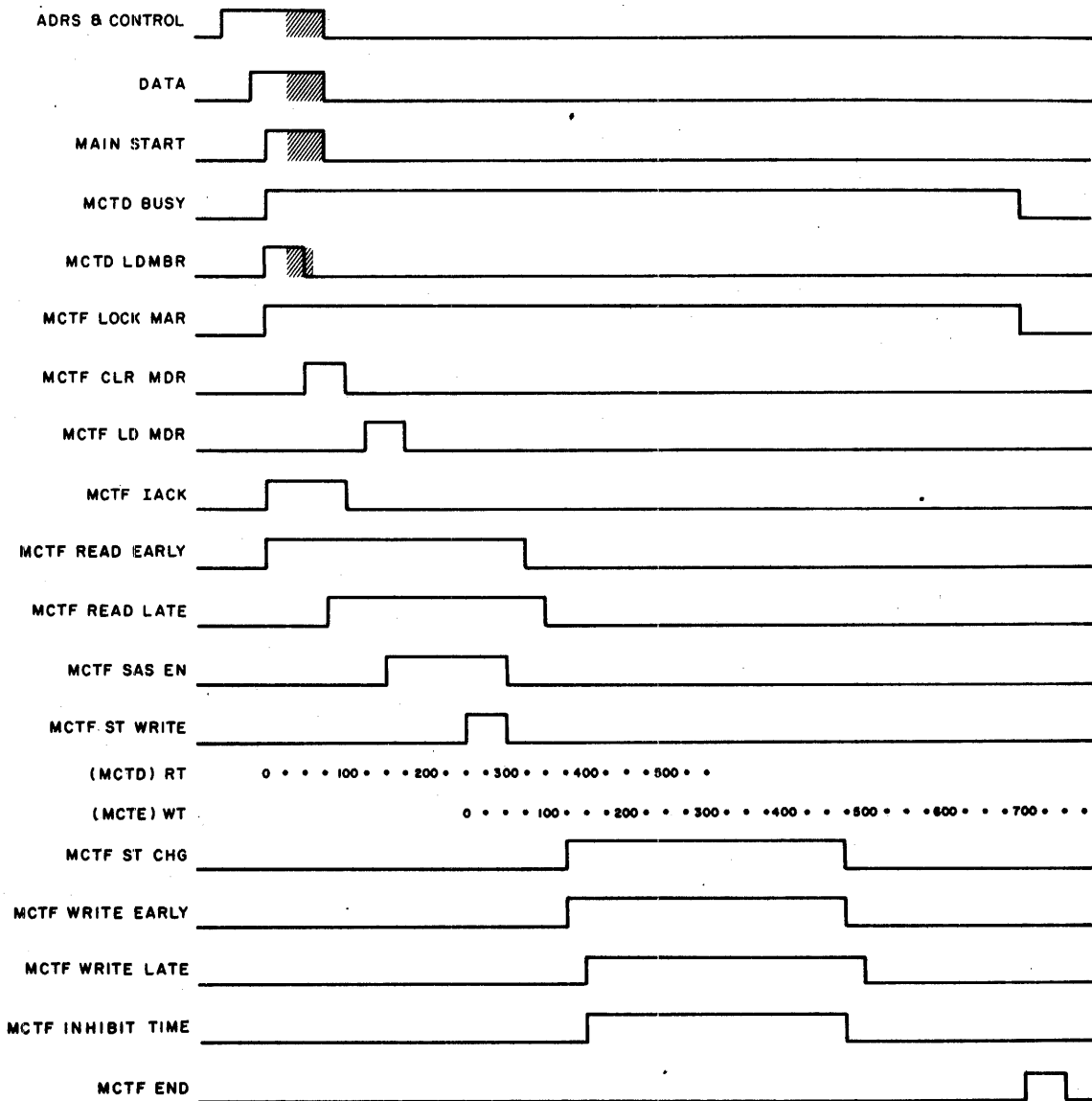
11-2996

Figure 3-1 Memory Controller Operation -- Simplified Flowchart



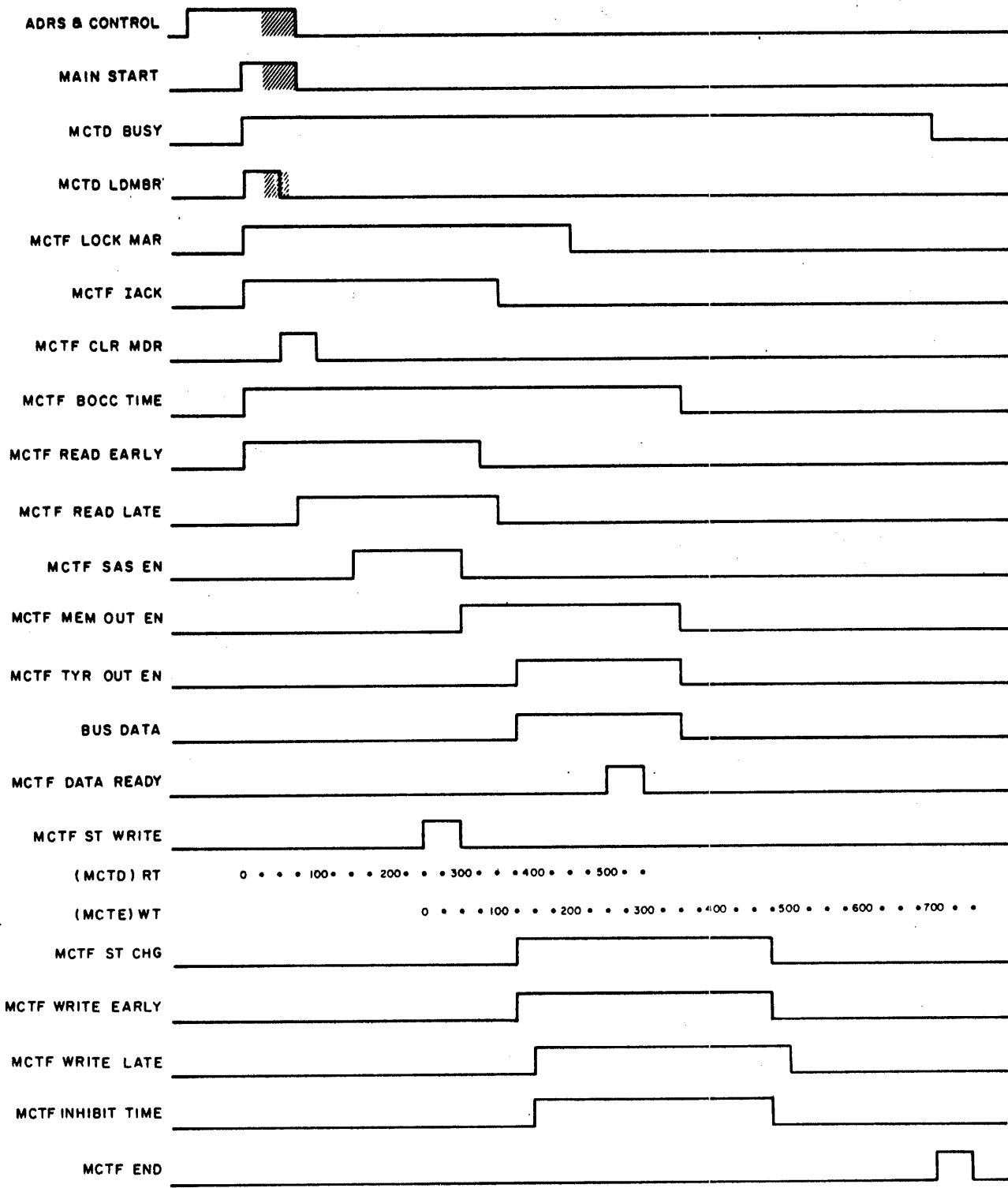
11-2971

Figure 3-5 Buffered Outputs of Read Timing Delay Line



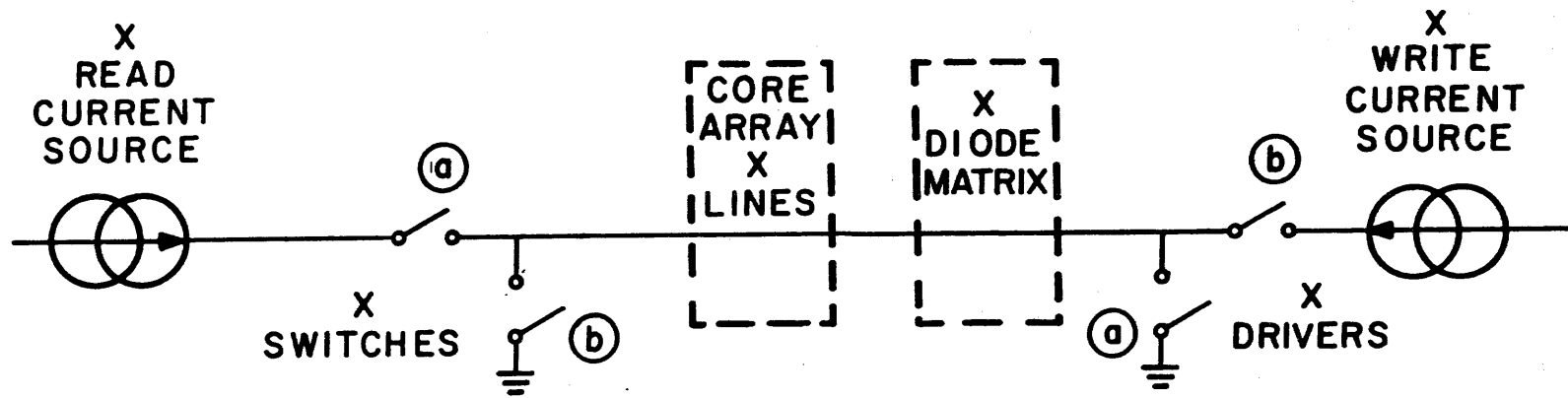
11-2989

Figure 3-6 Write Operation Timing Control Signals



11-2970

Figure 3-7 Read Operation Timing Control Signals

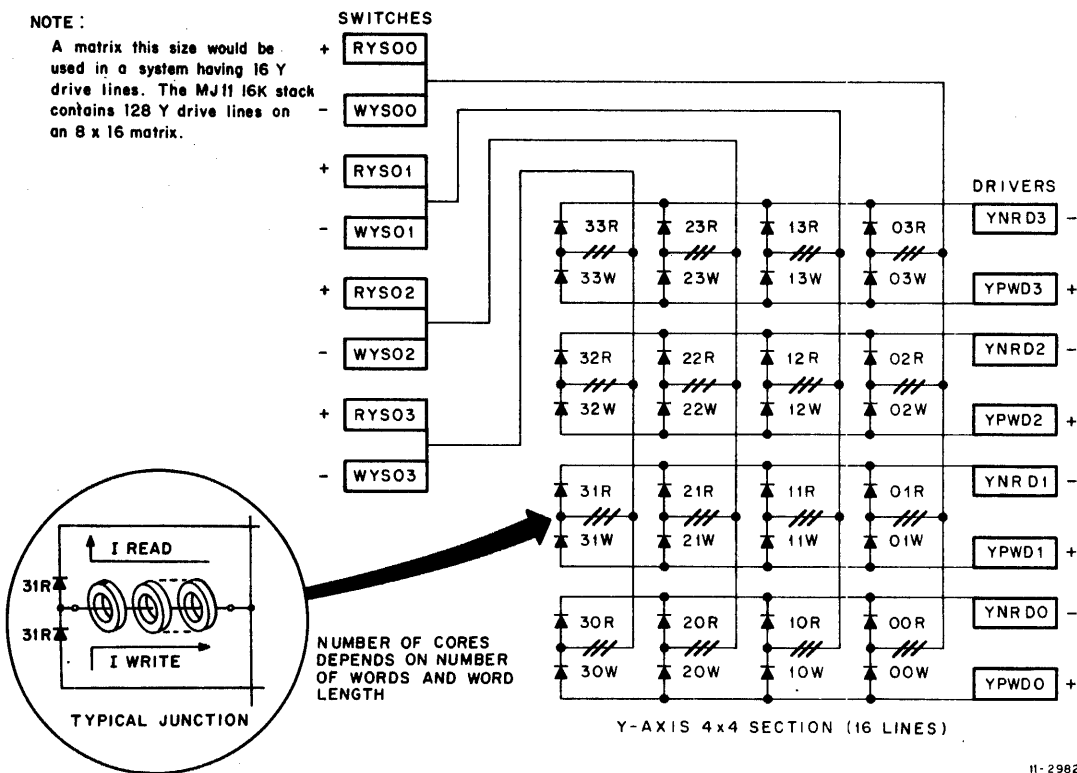


11-2979

Figure 4-4 Operation of Drivers and Switches

NOTE :

A matrix this size would be used in a system having 16 Y drive lines. The MJ11 16K stack contains 128 Y drive lines on an 8 x 16 matrix.



11-2982

Figure 4-5 Simplified Y Line Selection Stack Diode Matrix

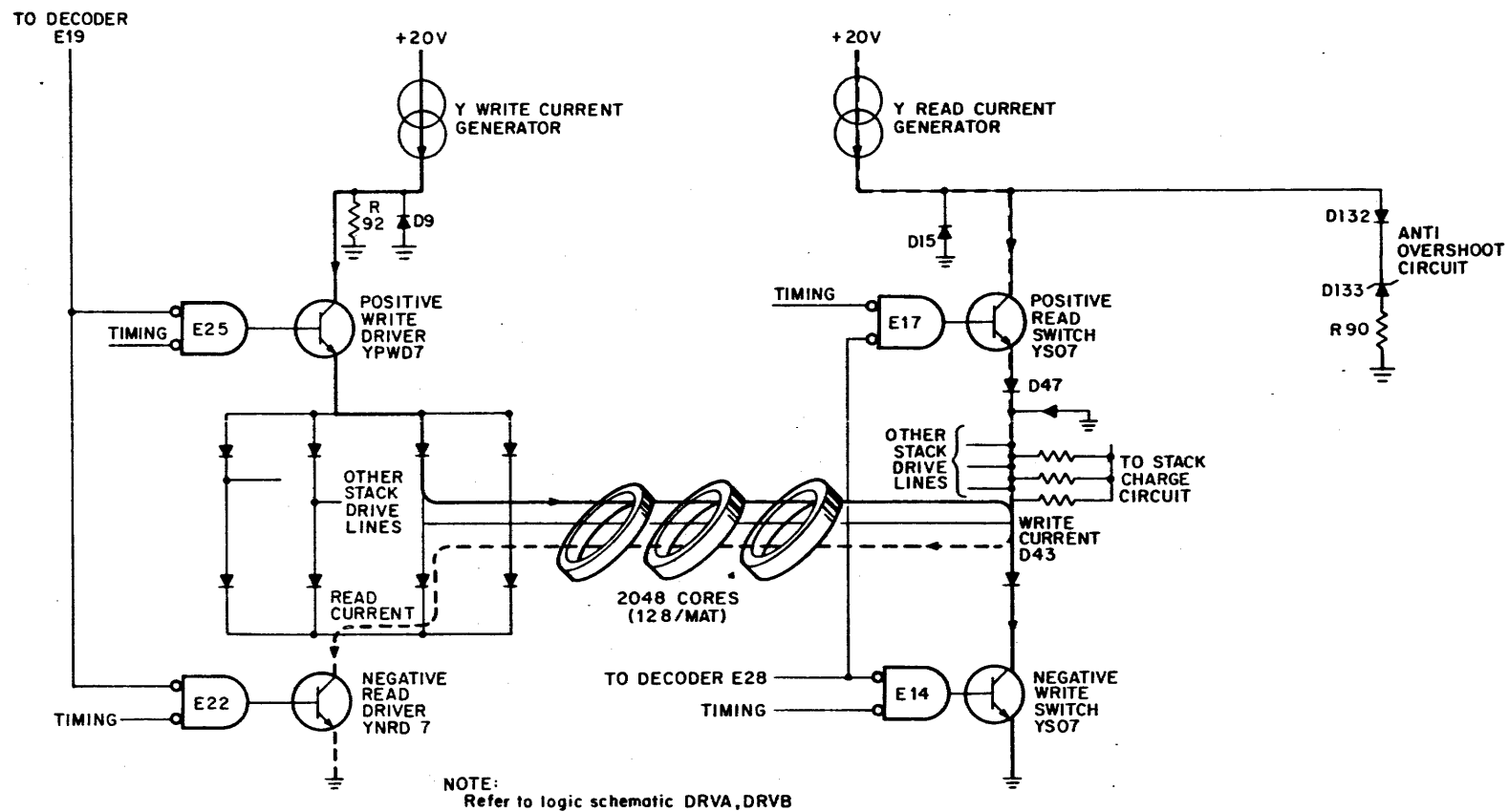
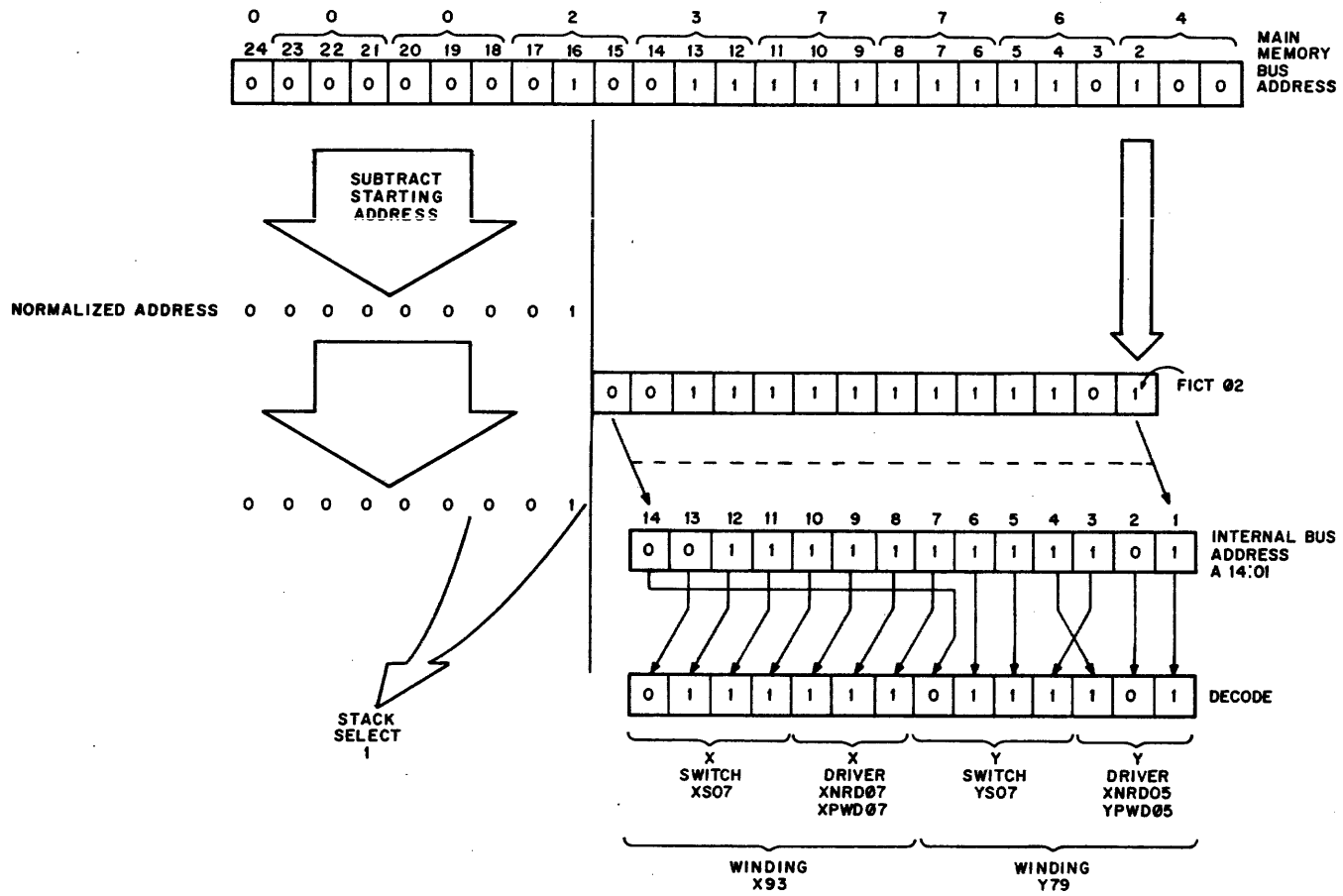


Figure 4-6 Typical Y Line Read/Write Switches and Drivers

11-1784



11-2980

Figure 4-7 Example of Address Decoding (Non-interleaved)

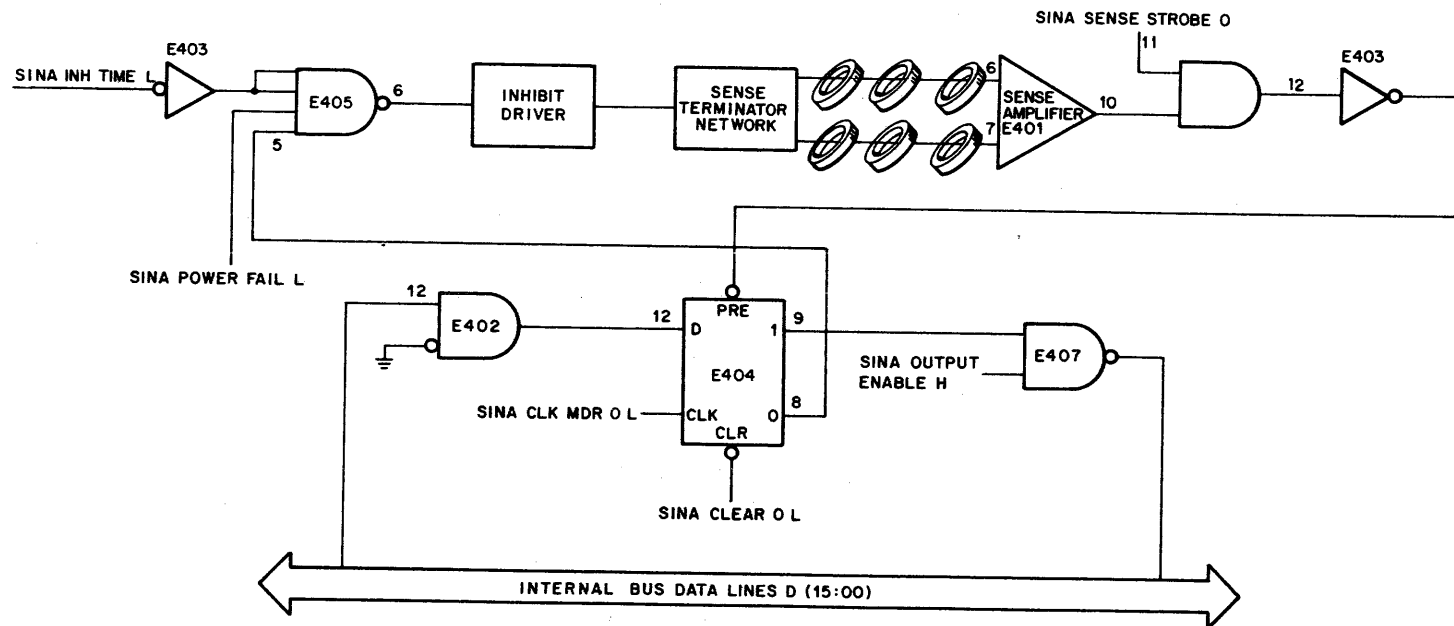


Figure 4-8 Interconnection of Internal Bus, Data Register, Sense Amplifier and Inhibit Driver

11-2981

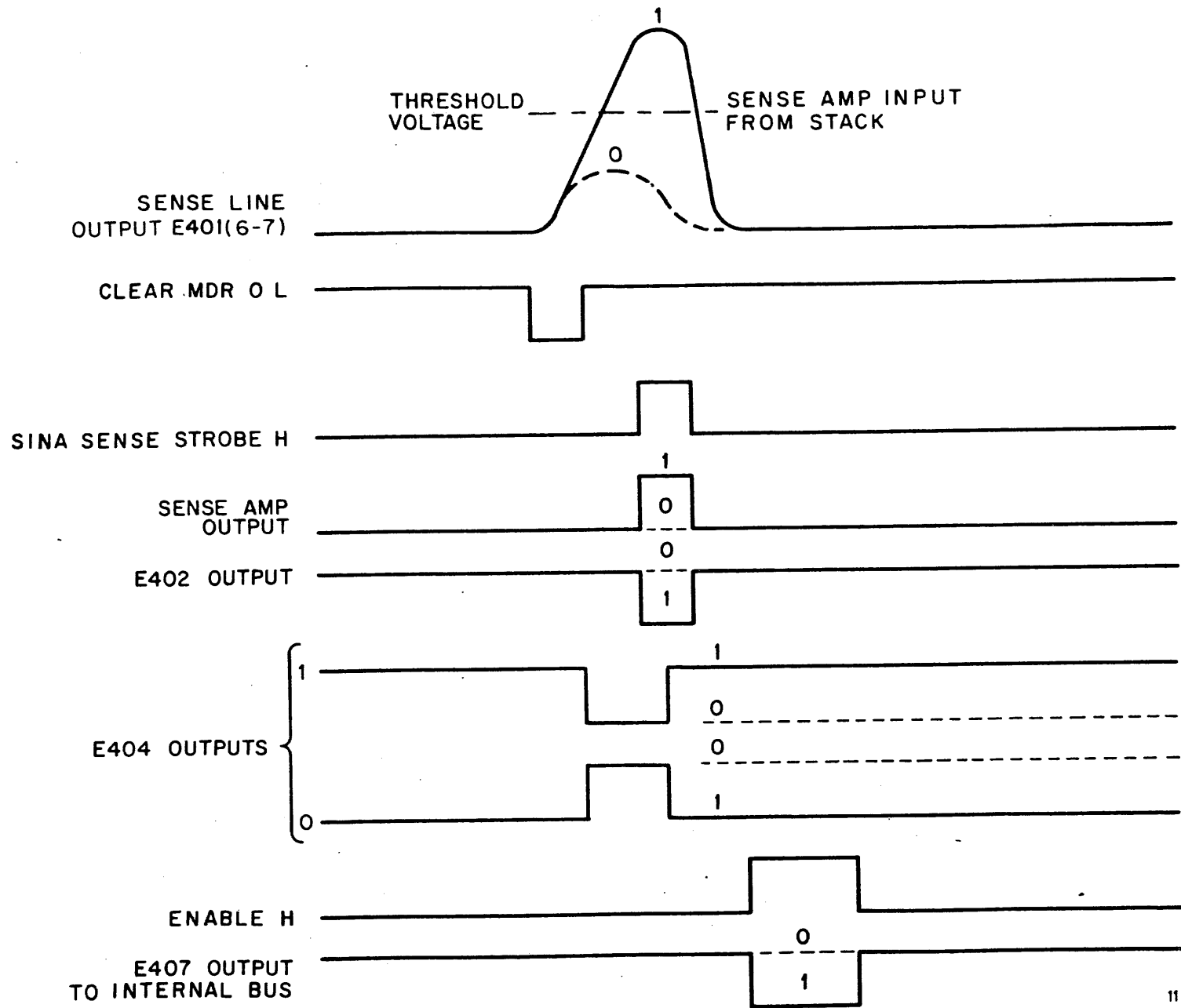
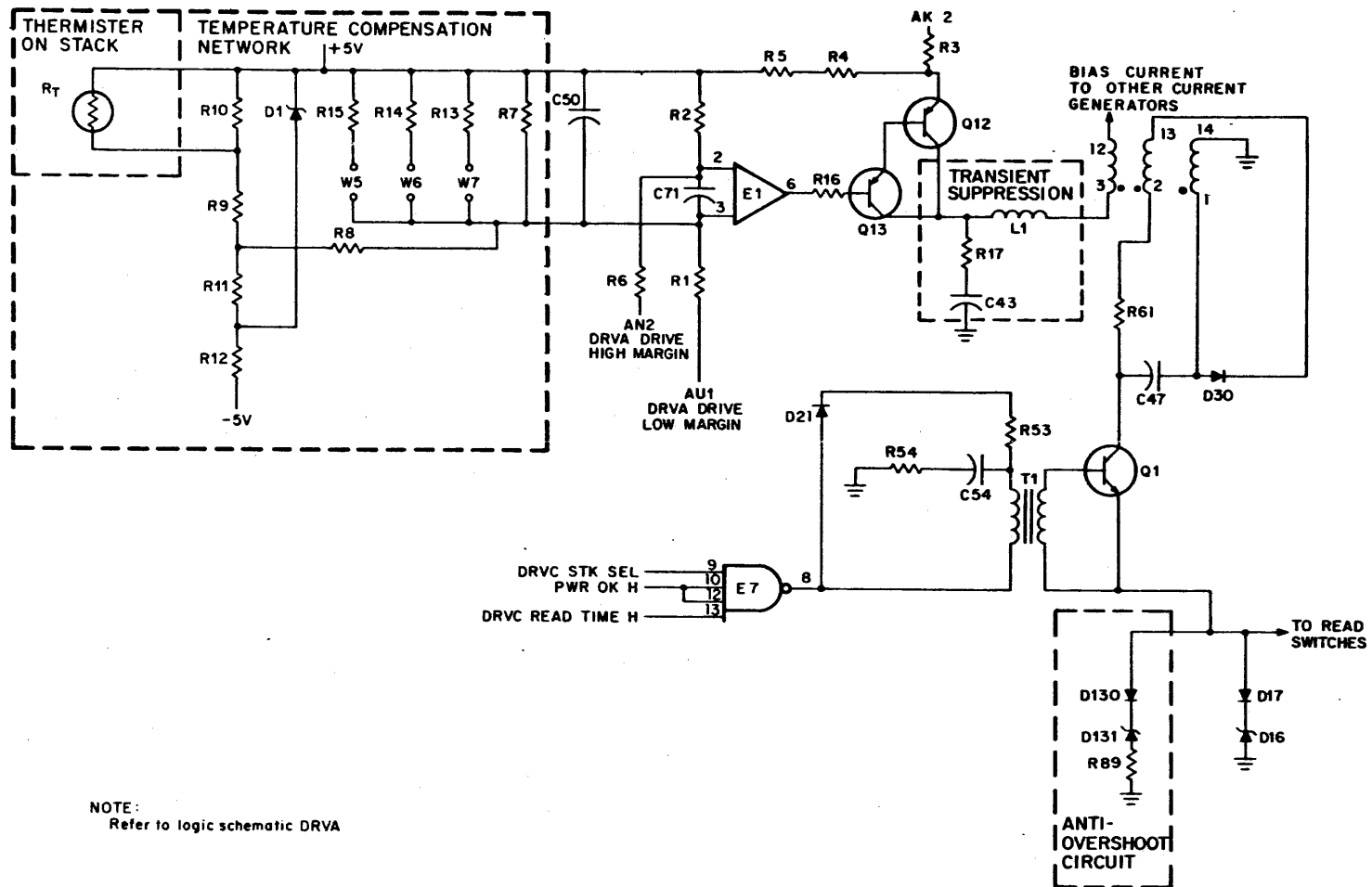


Figure 4-9 Sense Operation Timing Diagram



11-1787

Figure 4-10 Bias Current Supply and Read X Current Generator

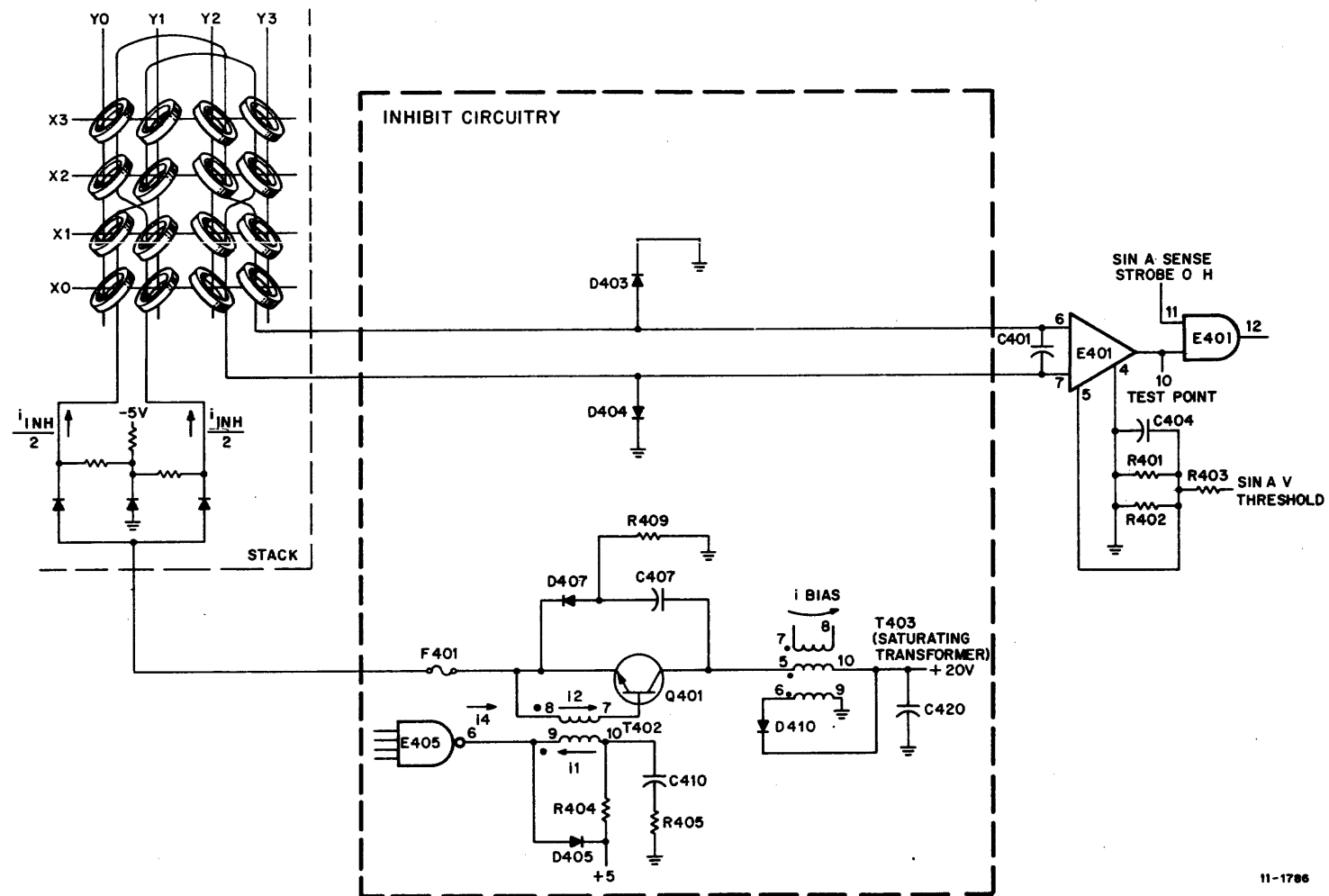
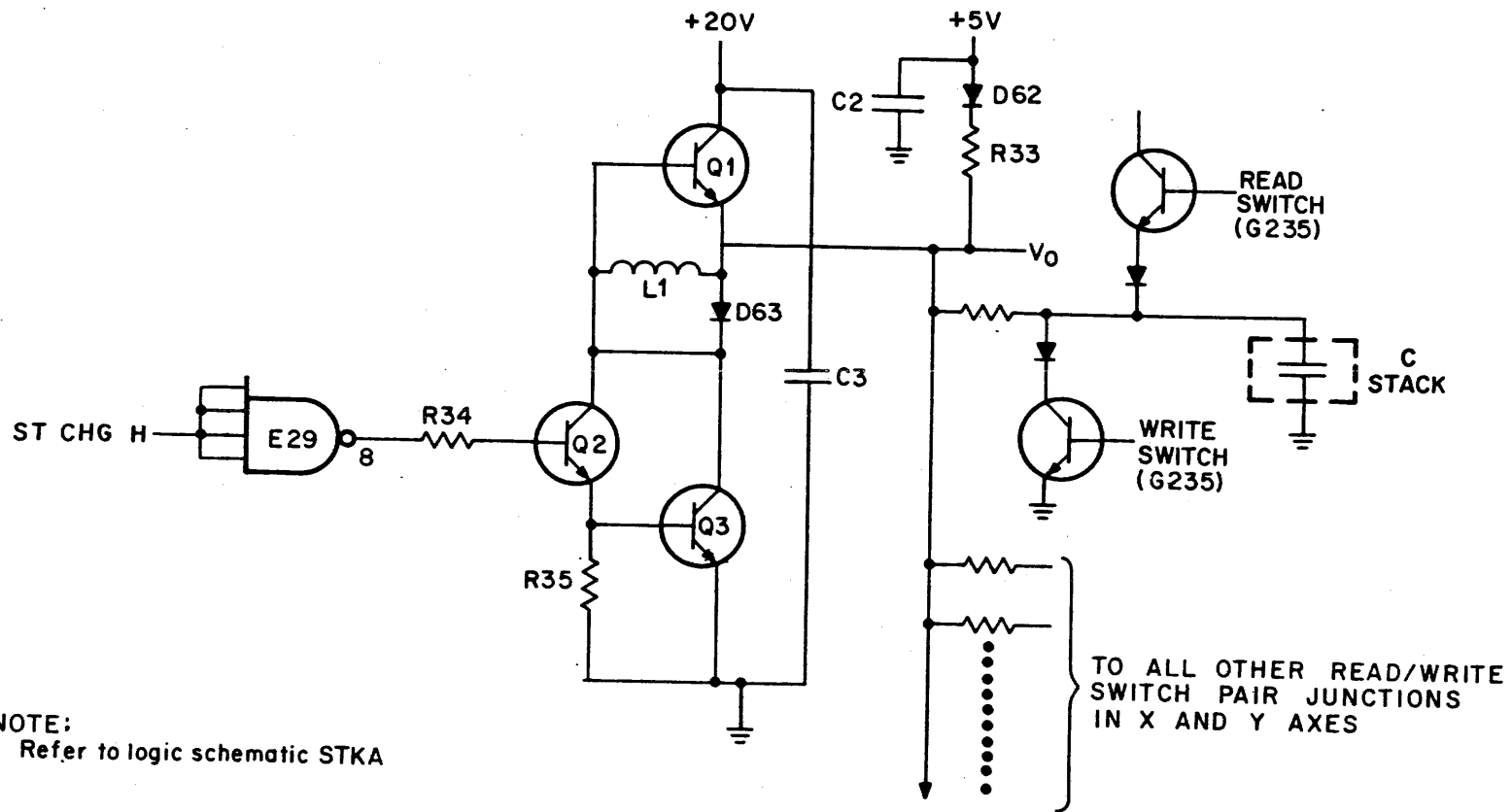


Figure 4-11 Sense Amplifier and Inhibit Driver

11-1786



NOTE:
Refer to logic schematic STKA

11-2984

Figure 4-13 Stack Charge Circuits

