digital INTEROFFICE MEMORANDUM

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DEPT: DECsystem-1Ø Engineering

SUBJ: KL1Ø PROJECT TECHNOLOGY GOALS

CONFIDENTIAL

PROJECT GOALS

On the 27th of October, 1971, the DECsystem-1Ø Product Line proposed a Phase I study to determine an Engineering Specification, Software Specification, Marketing and business plan for the KL1Ø. At that time the KL1Ø performance was that of the KA1Ø and the factory cost estimate of the following configuration was estimated at $36.5K.

Processor
PDP11/Ø5
VTØ5
32K of Memory
(2) 16ØØ bpi, 45 ips mag tapes
3ØØ lpm line printer
3ØØ cpm card reader
1Ø mega word discs

The cost of an equivalent KA1Ø was $135K, therefore the KL1Ø was proposed to have a cost/performance factor normalized to KA1Ø of 3.69. As the study progressed and more detailed estimates were made, we discovered a number of cost items had been left out such as $5.ØK worth of assembly, processor checkout and system integration. We also watched the size of the present monitor grow and realized that a system with 32K of memory was not viable. We therefore placed 64K on the system. With the

advent of 8K and 16K sense memories, the addition did not escalate the cost of the system very much. Finally the cost of 16 asynchronous lines was added in so that the basic KL1Ø would be capable of timesharing. The price of the system was then estimated at $51.2K.

In addition, the cost of an equivalent KA1Ø system was reduced to $1ØØK with the advent of the MF1Ø memory. The combination of the increase of the KL1Ø cost and reduction of the KA1Ø equivalent system cost reduced the cost performance ratio to 1.95 from 3.69. To bring that ratio back up to our goal, the performance goals of the KL1Ø had to be raised to 1.89 that of the KA1Ø. In order to hedge against further erosion of this cost/performance ratio over the development period, we increased the ratio from 3.69 to 5.

PERFORMANCE

In order to really get a handle on exactly which technology to use in order to accomplish our goals, we investigated three circuit families: 74ØØ T^2L, T^2LS and ECL. We did not have the set of scripts or a simulator to run them on, so up to this point we have based our permormance on a Gibson mix. This does not measure true system performance, but is the best we have available at this point. The results for T^2LS and ECL are summarized in Table I.

TABLE I

INST	INST%	KL1Ø T^2LS		KL1Ø ECL	
		EXEC TIME	PRODUCT	EXEL TIME	PRODUCT
ADD/SUB	33	1.9Ø	62.7	1.9Ø	62.7
MUL	Ø.6	4.34	2.6	2.51	1.5
DIV	Ø.2	8.28	1.7	4.6Ø	.9
JRST	6.5	.95	6.2	.95	6.2
CAML	4.Ø	1.99	8.Ø	1.9Ø	7.6
MOVE	17.5	5.7	99.8	5.7Ø	99.8
LSH	4.6	1.39	6.4	.95	4.4
AND	1.7	1.9Ø	3.2	1.9Ø	3.2
INDEXING	19.Ø	.Ø6	1.1	Ø.3	.6
FAD	7.3	3.17	23.1	1.9Ø	13.9
FMP	4.Ø	3.9Ø	15.6	2.27	9.1
FDV	1.6	6.94	11.1	3.9Ø	6.2
AVER INST X	1ØØ.Ø		241.5		216.1

Although not shown in the table, the KA1Ø had an average instruction time of 4.38 μ sec, and the KL1Ø with 74ØØ T^2L was 2.82 μ sec. A summary of performance ratios normalized to KA1Ø would then be as follows:

	AVER. INST. TIME (μ sec)	PERF. RATIO
KA1Ø	4.38	1
KL1Ø 74ØØ	2.82	1.55
KL1Ø S	2.41	1.82
KL1Ø E	2.16	2.Ø3

(TABLE 2)

Assuming that any of the KL1Ø machines could be built for the $51.2K cost estimate so that a 2 to 1 cost improvement over the KA1Ø with MF1Ø memory could be realized, the 5 to 1 performance/cost ratio could not be obtained. ECL came closest with 4.Ø6 to 1, followed by T^2LS with 3.64 to 1.

We then went back over the Gibson mix figures and recognized that the short instructions were memory limited. By using an IC memory buffer to reduce access time to 3Ø ns 95% of the time, we came up with a new set of average instruction times and performance ratios.

TABLE 3

	AVER. INST. TIME (μ sec)	PERF. RATIO
KA1Ø	4.38	1
KL1Ø 74ØØ	2.12	2.Ø7
KL1ØS	1.25	3.5Ø
KL1ØE	Ø.69	6.39

The conclusion of this study was that with cache memory, either T^2LS or ECL would meet our requirements. The almost 2 to 1 performance of ECL over T^2LS intrigued us though, so we investigated the cost of both types of machines.

COST

The first thing we did was to interview all IC vendors at length in order to determine component costs for the future. The results are summarized in TABLE 4.

TABLE 4 (Component Cost)

	1972	1973	1974	1975
SIMPLE GATES				
T^2L	.43	.42	.29	.24
ECL	.56	.43	.33	.28
FF'S				
T^2L	1.Ø1	.87	.57	.43
ECL	1.77	1.15	.89	.72
MSI (ALU)				
T^2L	1Ø.ØØ	5.75	4.68	3.73
ECL	6.15	4.7Ø	3.84	3.16

ECL competes reasonably well in the simple gates, has an edge in MSI but loses big on FF's, because only a dual version is available. Motorola has promised a hex or quint version if we desire it. costing figures assume its availability. A later section on risks states the implication of being wrong in this area.

The next level of cost we studied was the hex board which is summarized in table 5.

TABLE 5

HEX BOARD COST

	T^2LS	ECL
Multilayer Board	61.ØØ	76.86
Filter capacitor	7.84	7.84
Terminators	4.8Ø	6.6Ø
IC's	59.12	61.44
Rework	8.ØØ	8.ØØ
Test	4.ØØ	4.ØØ
TOTAL	144.76	164.74
COST PER IC	1.81	2.Ø5
		+13.2%

The cost of ECL is 13.2% higher than T^2LS at the board level because of an additional board layer for the -2 volt termination requirement, resistor terminators and higher IC cost.

We then investigated total processor and system cost. This is summerized in Table 6.

TABLE 6

		KL1ØS	KL1ØE	
15	Processor boards	216Ø	246Ø	
1	Paging boards	3Ø6	346	
2	RAM boards	768	96Ø	
	Packaging, cooling & wiring	2345	2345	
	CPU power	675	776	
	I/O power	5ØØ	5ØØ	
	11/Ø5 -12K of memory	2ØØØ	2ØØØ	
	VTØ5	7ØØ	7ØØ	
	Checkout	2ØØØ	2ØØØ	
	TOTAL BASIC PROCESSOR	11,454	12,Ø87	+5.5%
2	Channels	975	975	
2	Mag tapes (16ØØ bpi,45 ips)	7ØØØ	7ØØØ	
	Card reader (3ØØ cpm)	12ØØ	12ØØ	
	Line printer (3ØØ lpm)	7ØØØ	7ØØØ	
	Disc (1Ø mega words)	5ØØØ	5ØØØ	
	TTY MUX (16 lines)	31ØØ	31ØØ	
	Memory(64K) + cache	11Ø71	11438	
	System integration	3ØØØ	3ØØØ	
	TOTAL BASIC SYSTEM	49,8ØØ	5Ø,8ØØ	+2%

The ECL machine was more expensive at the processor level by 5.5% and at the system level by 2%.

COST/PERFORMANCE

A summary of basic system cost figures for KA1Ø and KL1Ø is as follows:

TABLE 7

	CACHE ($K)	NO CACHE ($K)
KA1Ø		1ØØ.Ø
KL1ØS	49.8	46.6
KL1ØE	5Ø.8	47.3

A summary of cost/performance ratios normalized to KA1Ø and based on Table 2, Table 3 and Table 7 is as follows:

TABLE 8

	CACHE	NO CACHE
KA1Ø		1
KL1ØS	7.Ø2	3.9Ø
KL1ØE	12.5	4.29

It is clear that a T^2LS KL1Ø will meet the goals set down one year ago by some margin, but it is also clear that an ECL KL1Ø is a bigger winner. We also feel though that ECL exhibits a moderate risk and increase in startup cost as outlined in appendices 1 & 2.

The performance margin between the machines is so great that I feel it to be a bigger risk with respect to the present competion or competition to be if we don't go for the ECL machine. Another consideration is that no matter what we decide for the KL1Ø, ECL is apparently closing quickly with T^2L and warrents watching closely.

APPENDIX I

TRAINING	TTL	ECL
1. Incomming Inspection 2 people (2 days at 3 locations)	Ø	Ø.5K
2. Module test		
Total labor cost including training and debugging of initial modules on XOR.	25.9K	27.5K
3. Production checkout		
3Ø people for 2 weeks on KL1Ø processor course.	28.8K	28.8K
4. Field Service		
75 people for 5 weeks on KL1Ø system course	18Ø.ØK	18Ø.ØK
5. XOR follow on labor failure analysis etc. for one year.	19.ØK	19.ØK
SUB TOTAL	253.7K	255.8K
DEVELOPMENT		
1. Incoming Inspection Teredyne-development labor.	Ø	5.ØK
2. XOR development	Ø	1Ø.6K
3. 5 layer board and backpanel		
In house development cost if we were to use 5 layers.	Ø	1ØØ.ØK
SUB TOTAL	Ø	115.6K

APPENDIX I (Contd.)

CAPITAL EQUIPMENT

	TTL	ECL
1. Incomming Inspection (3 locations)		
All hardware and programs needed to test 25 new devices on Teredyne tester.	Ø	95.3K
2. Module Test		
2 XOR testers, 2 KL1Ø's and 2 bus simulators	91.9K	95.6K
3. Basic checkout (2 wk)		
1Ø station ACT-11 line and 4 bus simulators	11Ø.ØK	11Ø.ØK
4. System Integration (4 wk)		
2Ø station ACT line and 1Ø bus simulators	23Ø.ØK	23Ø.ØK
SUB TOTAL	431.9K	53Ø.9K
TOTAL START UP COSTS	686.ØK	9Ø2.ØK
DIFFERENCE		216.ØK

APPENDIX II

RISKS

1. 5 layer multilayer board - The 11/45 uses a 4 layer hex board consisting of +5 volt and ground on the inner layers and 2 outer signal layers.

   The KL1Ø requires either a 5 layer hex consisting of -5, -2 volts and ground inner layers with 2 outer signal layers or could utilize a 4 layer board with bus strips for the additional voltage.

   Joe St. Amour estimates the development of the 5th layer to be $5ØK. This has been included in the startup costs for ECL.

   There was some concern that the 5th layer would make the board too thick for the Sylvania block. This has been investigated thoroughly and the conclusion is that the 5 layers can readily be manufactured to within 65 mils, 1Ø mils more than the 11/45 board and 5 mils within the block specification.

2. Multilayer PC back panel - The 11/45 uses a 2 layer back panel for voltage and ground.

   The KL1Ø was originally proposed with a 5 layer backpanel with the same layer assignments as the multilayer hex.

   This arrangement has changed to 2 voltage layers and a ground in order to make servicing and ECO's easier.

Joe St. Armour estimates $5ØK for this effort. This also has been factored into the startup costs.

3. IC availability and delivery is close to zero risk. At least one vendor has all the types we require. (See Appendix IV). Second sourcing will be available on all devices by 4/73.
4. One of the keys to the cost/performance of the machine is the cache design. Our best estimate of the risk this represents is a possible 2 months slippage on a 24 month project.
5. Motorola has committed to deliver the hex flop 3/73. In order to eliminate the associated risk, the KL1Ø design will be based on the available quad flop if the hex flop development slips.
6. The biggest risk of this or any project which uses large boards is the time required to perform PC layout. Redac must be in place by February 1973 in order for the project to succeed.

KL10 CIRCUIT FAMILIES

The purpose of this memo is to summarize the relative performance of Schottky T.T.L. and the 10 000 ECL family of devices, which are the two logic families suitable for use in the KL10 to achieve the desired performance.

1. BASIC PERFORMANCE

1.1 Gate Propagation Delay

The basic family of 74S devices is about a factor of two slower than ECL as shown below.

	74S	ECL 10K
Gates	7 ns	4.0 ns
Flip Flops (Dual D) (Clock to output)	11 ns	6.6 ns
74151 (8 line mux. address-output)	19.5 ns	8.6 ns

2.0 LINE DRIVING CAPABILITY

74S gates are not capable of driving transmission lines, but 10K gates can drive 50 ohm lines resistively terminated.

To minimize reflections 74S lines must be terminated by a clamp diode biased to clamp any negative going signal transient at ground.

Gates such as the 74S14Ø power driver require a clamp diode biased to turn on at about +5 volts as ringing may cause overshoot above 5.5 volts which is an illegal condition for TTL. The overshoot occurs with above about 52 ohms, and the duration of the overshoot is equal to twice the signal line propagation delay.

Because of the poor drive capability it is necessary to wait for twice the delay of signal line to ensure that the line has been charged to a voltage above the minimum gate input threshold when making a positive transition.

The performance when driving a line of 12" length and impedance of 7ØΩ is shown below:

			12" (Line)	
74S	7.Øns	Biased Diode	2.1ns	11.2ns
1ØK	4.Øns	Resistor	2.1ns	6.1ns

The total delay is considered to be the time required for all points on the line to be above the minimum input threshold of a receiving gate.

3. POWER DISSIPATION

The dissipation of the two families for a 5Ø% duty cycle with 1ØK assumed driving a 68Ω line terminated to -2 volts is shown below, at 1MHz and at 16MHz, which is the clock frequency of the KL1Ø with Schottky logic. The 74S dissipation also increases with operating frequency.

	FREQUENCY	POWER (per gate)	OUTPUT STAGE DISSIPATION	TERMINATOR DISSIPATION	TOTAL DISSIPATION
74S	1MHz	35mW	---	---	35mW
1ØK	1MHz	26mW	11mW	9mW	46mW
74S	16MHz	46mW	---	---	46mW
1ØK	16MHz	26mW	11mW	9mW	46mW

4.Ø NOISE IMMUNITY

The DC noise immunity is a measure of how much interference may occur at a gate input without spurious operation.

Coupled interference (crosstalk) from one signal line to another is also dependent on the amplitude and transition of the signal causing the interference. A comparative measure of noise immunity may then be made by defining a figure of merit for a logic family as

$$F = \frac{\text{Noise Immunity} \times \text{Transition time}}{\text{Signal swing}}$$

The comparison for 74S and 1ØK is shown below. Larger values of F mean better performance.

	D.C. Noise Immunity		Max. Signal Swing	Min. Transition Time	F
74S	3ØØmV	'0' state	3.8V	1.5ns	.117
	7ØØmV	'1' state	3.8V	1.5ns	.273
1ØK	125mV	1&0 states	Ø.95V	1.5ns	.145

ECL noise immunity is dependent upon supply voltage and temperature difference between the driving and receiving gate.

For a voltage difference of 136mV which is 5.2V± 2% + 32mV I.R. drop i distribution and a temperature difference of 11°C (2Ø°F) which is based on an ambient temperature ranging from 15½° C to 35½°C at the inlet, F = Ø.128 for 1ØK.

5.Ø SUPPLY CURRENT VARIATION

The variation of supply current in a 74S gate function varies by a ratio of about 2:1 depending on whether the gate is in a '0' or '1' state.

A current spike also occurs during switching of the output stage due to overlap switching effects of the totem pole output and charging currents to the output load capacitance.

These transients require good decoupling and make the use of multilayer boards with low inductance power and ground planes mandatory.

1ØK ECL uses two supply voltages. -5.2 volts supplies the differential input amplifier and voltage reference source. The current drawn by these stages is very constant regardless of which logic state the gate is in and decoupling is much less critical than for the +5 volt supply for 74S.

The 1ØK gates use a terminating supply of -2volts and this supply experiences current fluctuations of about 5:1 between '0' and '1' state for a 68Ω terminating resistor, hence the -2 volt supply requires careful distribution, so a 4 layer multilayer board is required as it is for the 74S family.

APPENDIX IV

PRODUCT AVAILABILITY

Bill Walton
9/6/72

		MOT	SIG	TI	NATIONAL
1Ø1Ø1	QUAD OR/NOR	*	1Ø/72	11/72	11/72
1Ø1Ø2	QUAD NOR	*	11/72	1Ø/72	*
1Ø1Ø4	QUAD AND	12/72	6/73	1Ø/72	n.p.
1Ø1Ø5	triple 2-3-2 OR/NOR	*	*	11/72	*
1Ø1Ø6	triple 4-3-3 NOR	*	*	11/72	*
1Ø1Ø7	triple XOR	*	*	11/72	*
1Ø1Ø9	dual 4-5 OR/NOR	*	*	12/72	*
1Ø11Ø	dual 3 input 3 output OR	*	*	1Ø/72	*
1Ø111	dual 3 input 3 output NOR	*	*	1Ø/72	*
1Ø117	dual 2 wide OR-AND-invert	*	*	11/72	*
1Ø118	dual 2 wide OR-AND	*	*	11/72	*
1Ø119	4 wide OR-AND	*	*	11/72	*
1Ø121	4 wide OR-AND-invert	*	*	11/72	*
1Ø124	QUAD TTL to MECL translator	*	*	2/73	12/72
1Ø125	QUAD MECL to TTL translator	*	*	2/73	12/72
1Ø131	dual D flip flop	*	*	2/73	12/72
1Ø141	4 bit Universal Shift Register	*	2/73	4/73	n.p.
1Ø144+	256 bit RAM +	4/73	3/73	7/73	n.p.
1Ø16Ø	12 bit Parity Generator	*	11/72	9/72	12/72
1Ø161	Binary to 1 of 8 decoder	*	*	9/72	n.p.
1Ø174	Dual 4-1 Multiplexer	*	1Ø/72	4/73	1/73
1Ø179	Look ahead carry block	*	3/73	1/73	n.p.
1Ø181	4 bit ALU	*	3/73	4/73	n.p.

* - Available in production quantities now.

n.p. - No development plans at this time.

All dates are months that production quantities will be available.

+ Fairchild is now delivering a pin compatible device which we can use until other vendors are available.

KL1Ø BLOCK DIAGRAM

A. Kotok
9/6/72