

KL10 Field Maintenance Print Set Supplement

KL10 BLOCK DIAGRAMS

The block diagrams in this manual are selected from the *KL10 Technical Descriptions*. These drawings are not under ECO control. They are intended to be used as a supplement to the *KL10 Field Maintenance Print Set*.

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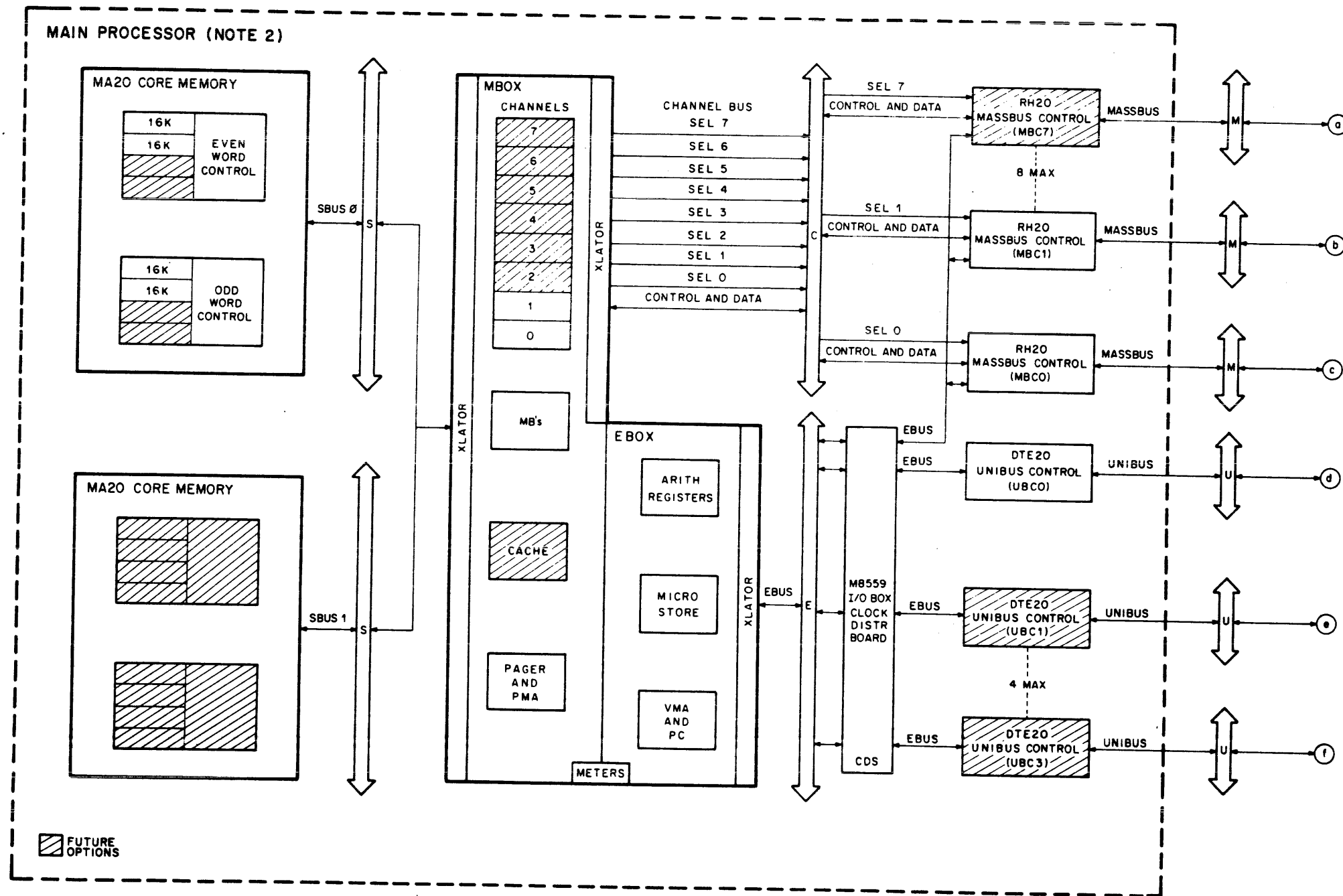
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DECSYSTEM-20	MASSBUS	TYPESET-11
		UNIBUS

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Figure 1 DECSYSTEM-20 Block Diagram - Typical (Sheet 1 of 2)

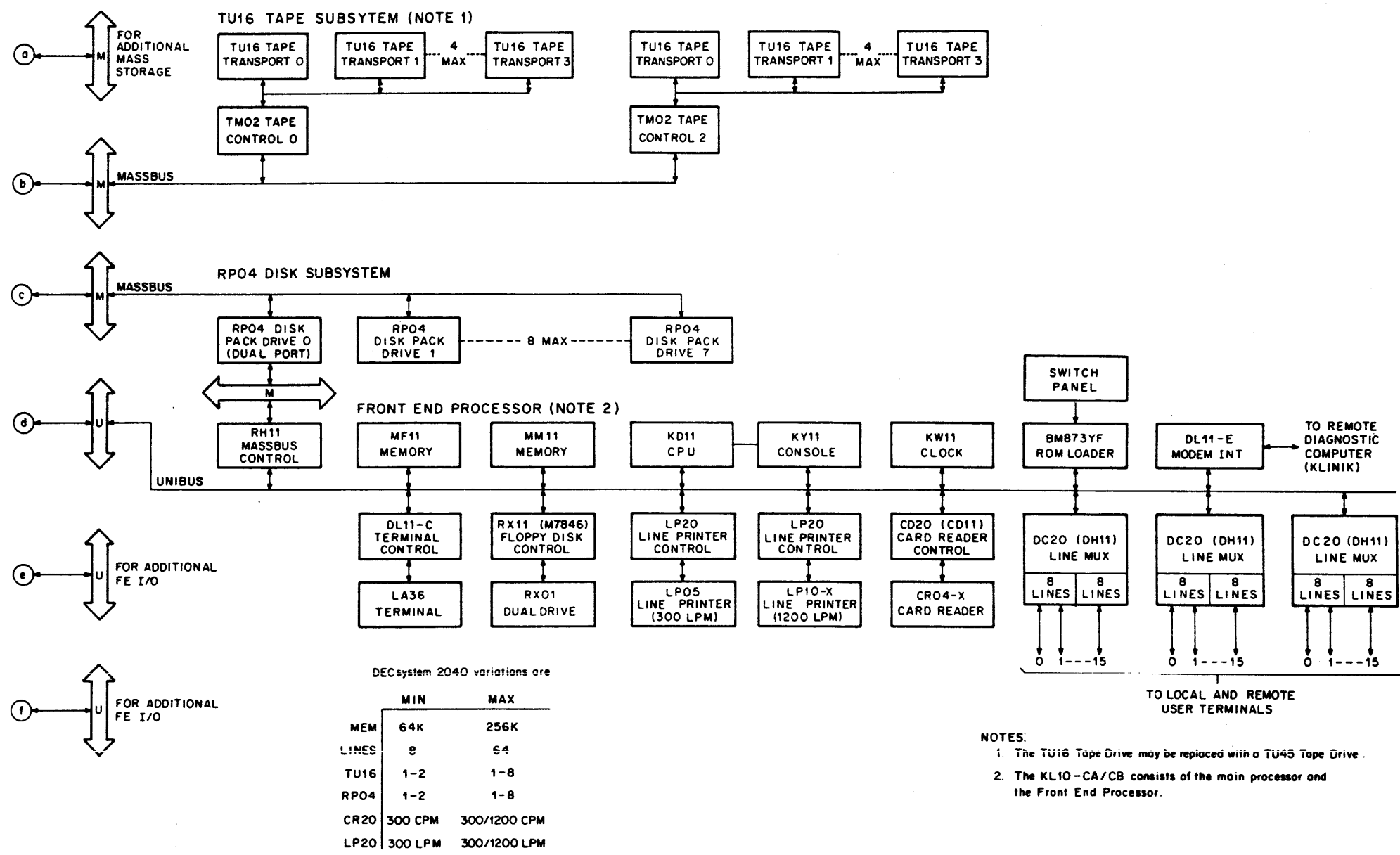
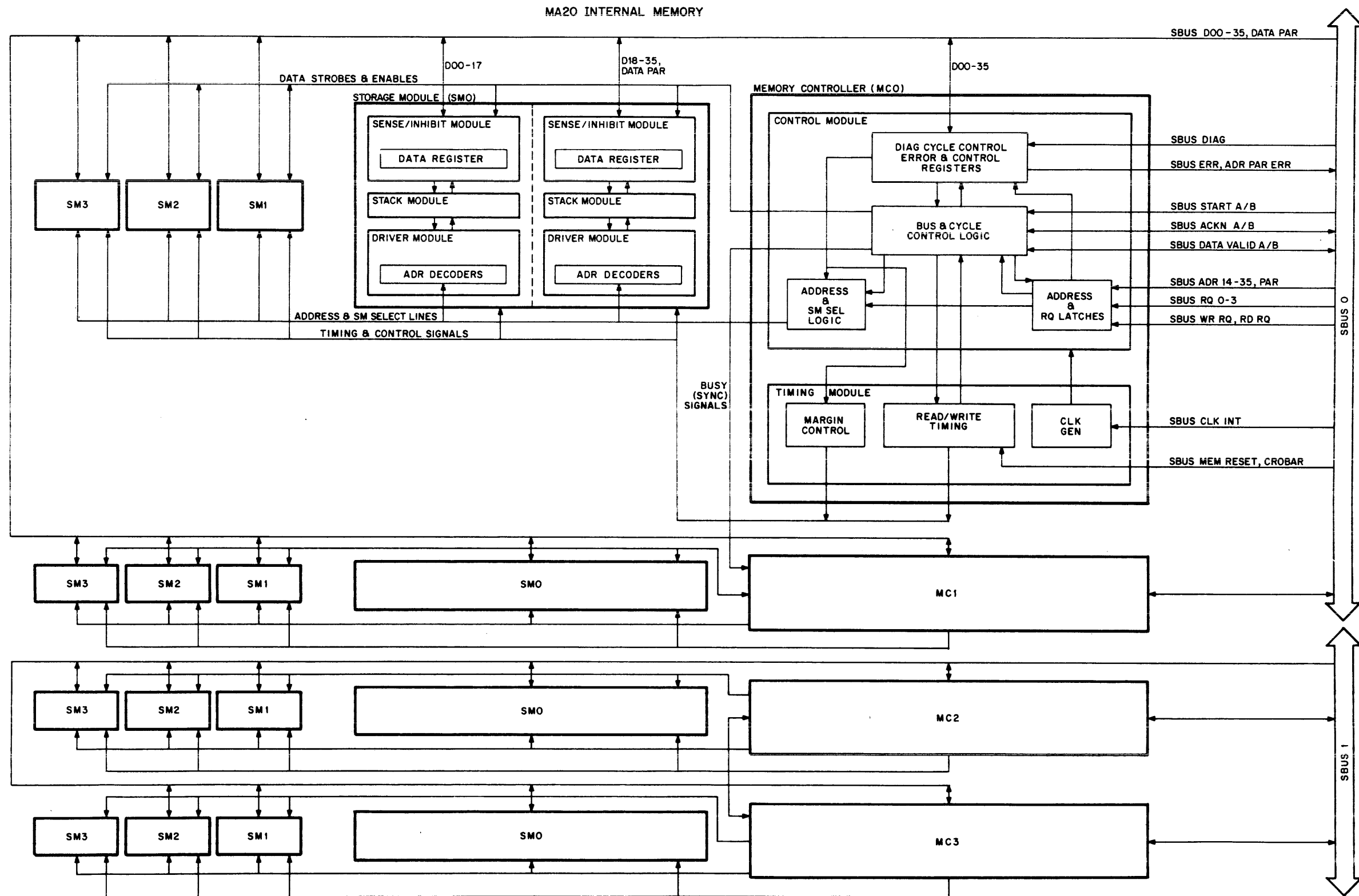
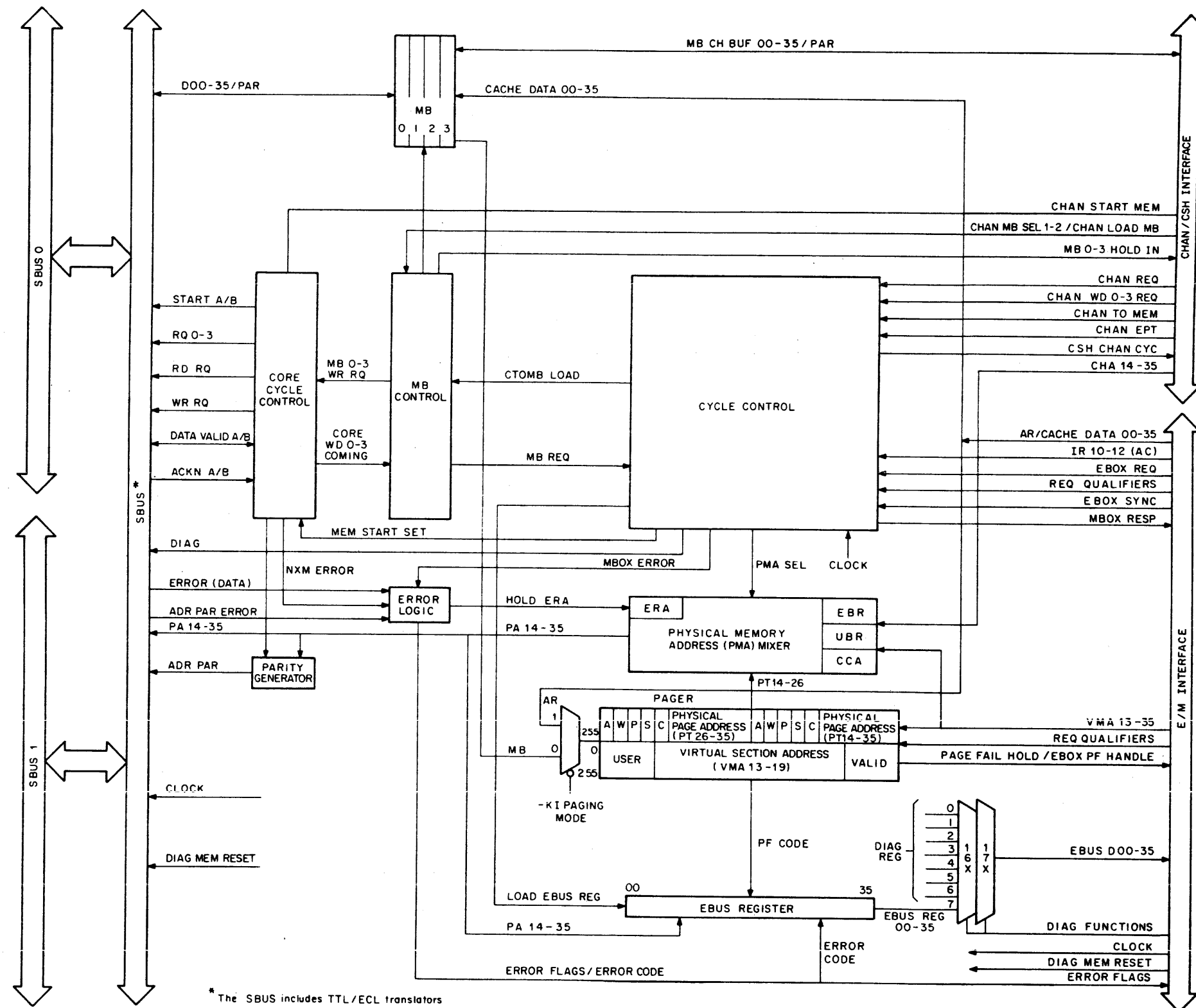


Figure 1 DECSYSTEM-20 Block Diagram - Typical (Sheet 2 of 2)



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Figure 2 Main Processor Subsystem Block Diagram (Sheet 1 of 4)



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Figure 2 Main Processor Subsystem Block Diagram (Sheet 2 of 4)

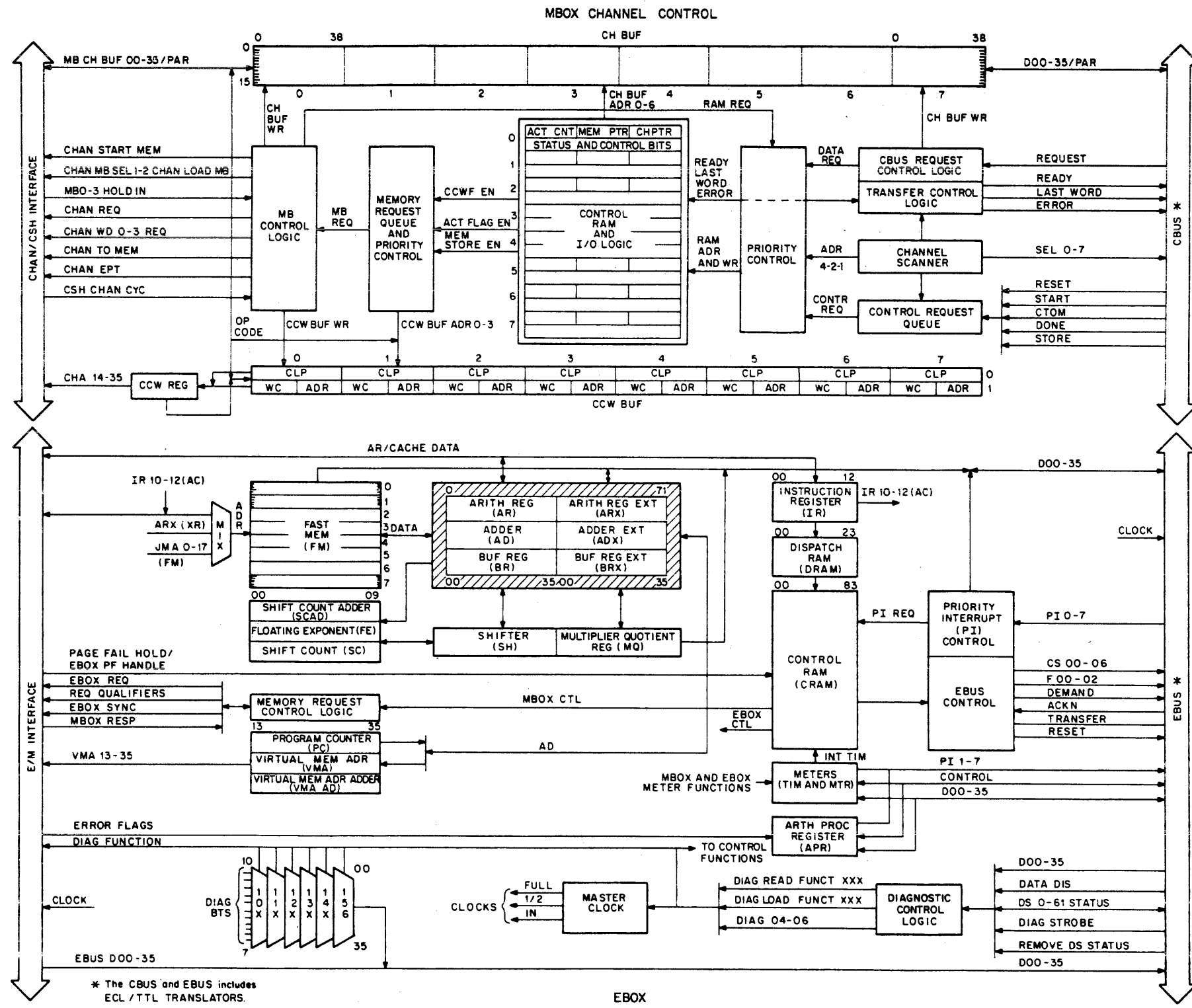


Figure 2 Main Processor Subsystem Block Diagram (Sheet 3 of 4)

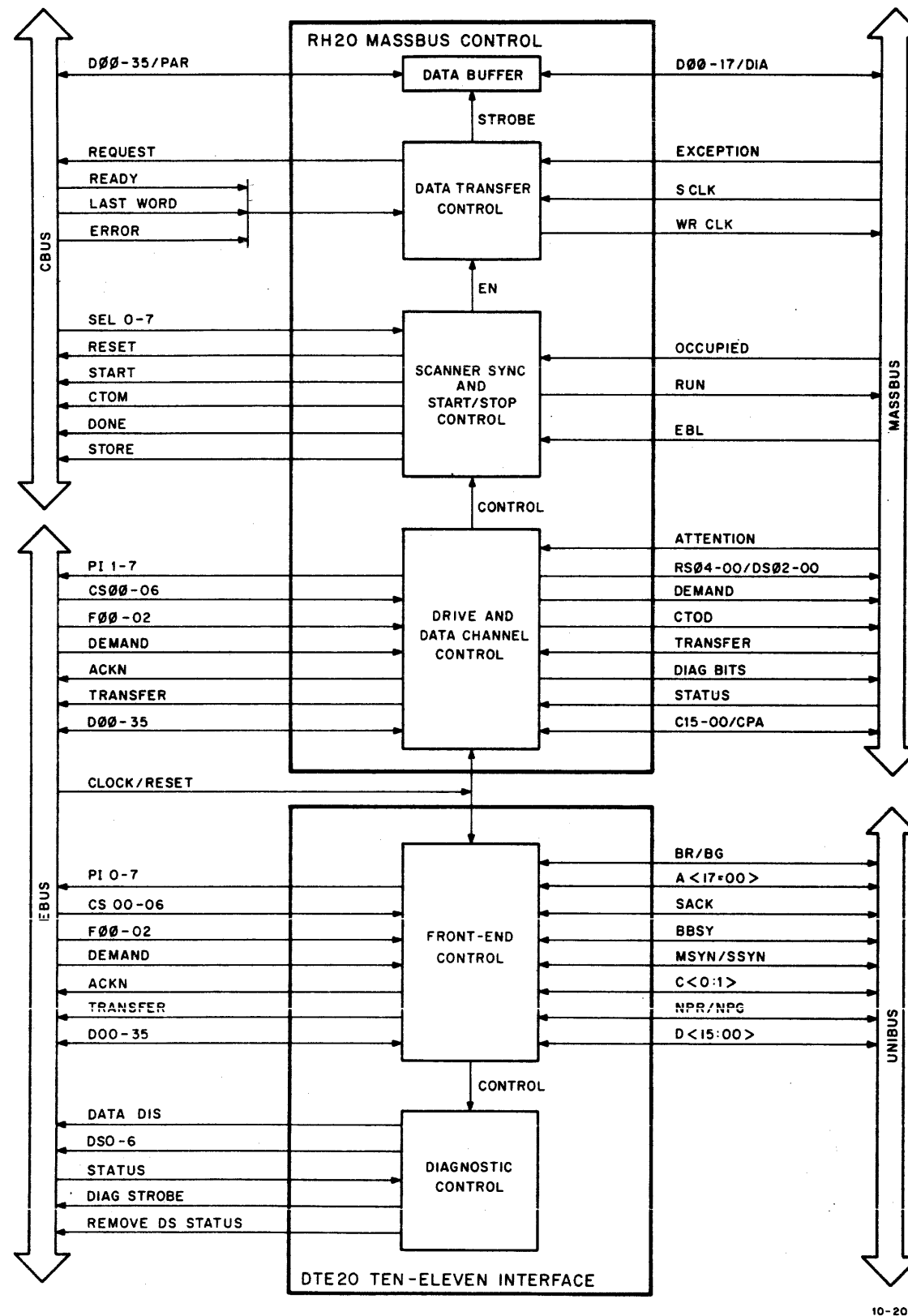


Figure 2 Main Processor Subsystem Block Diagram (Sheet 4 of 4)

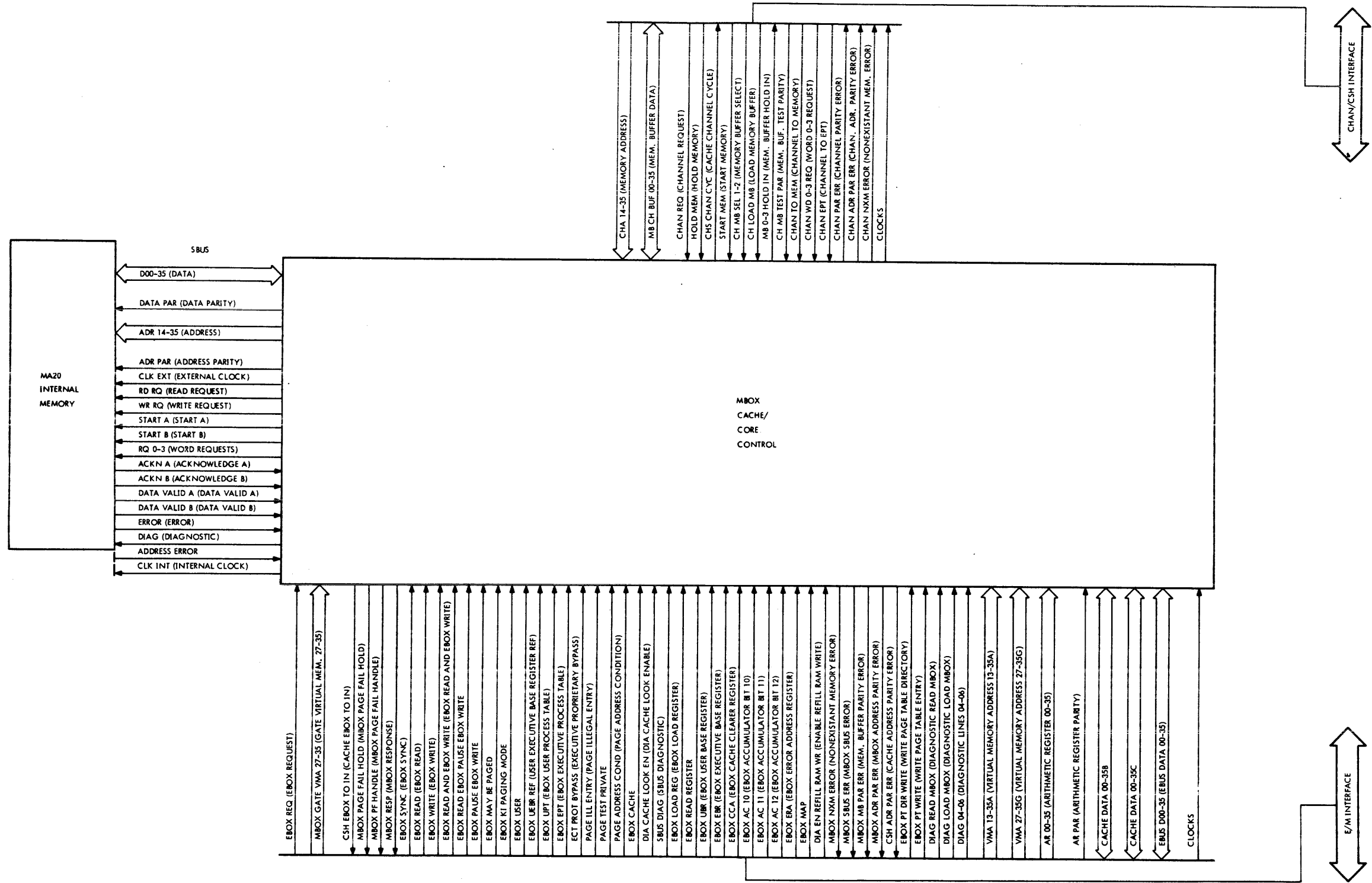
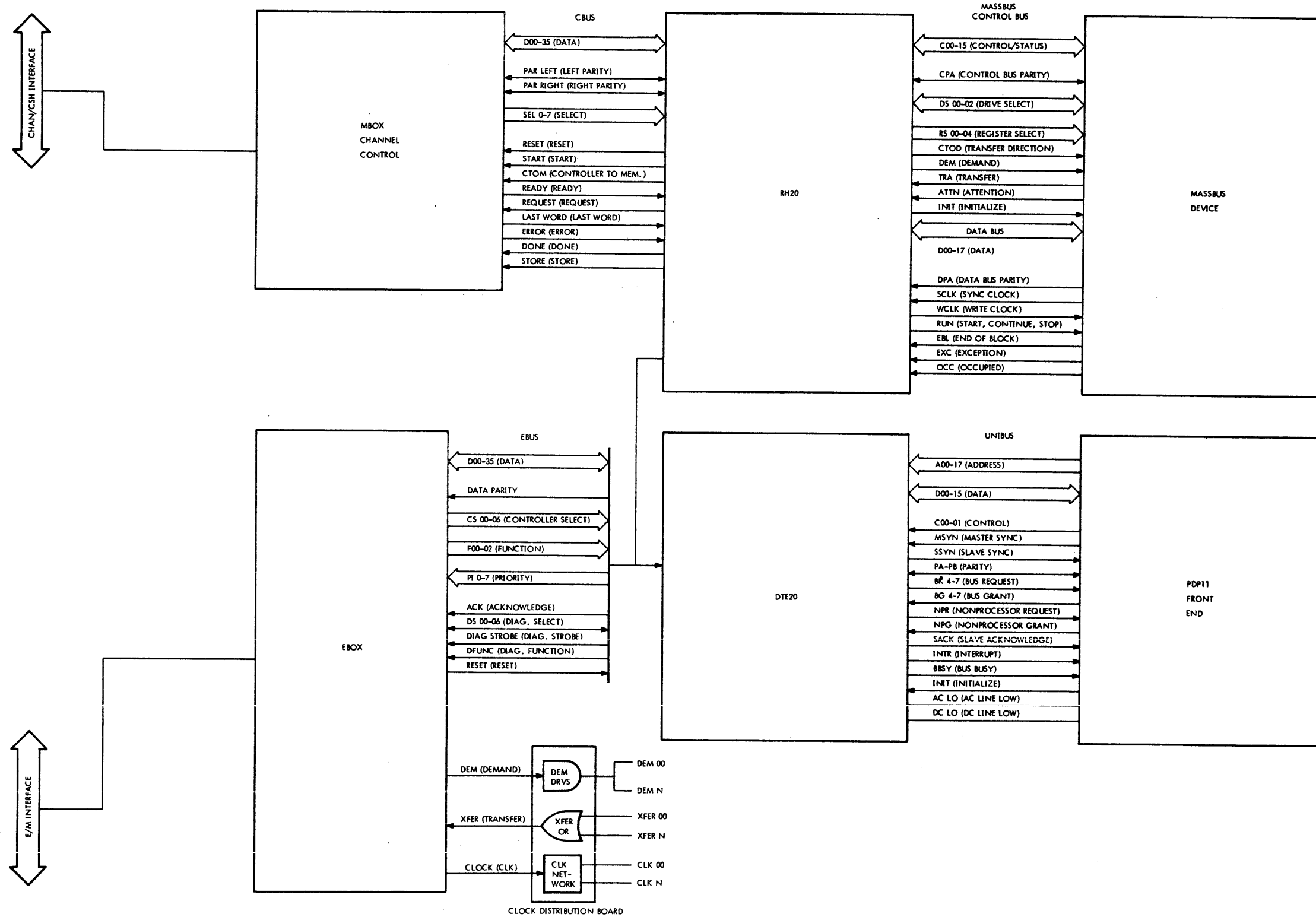
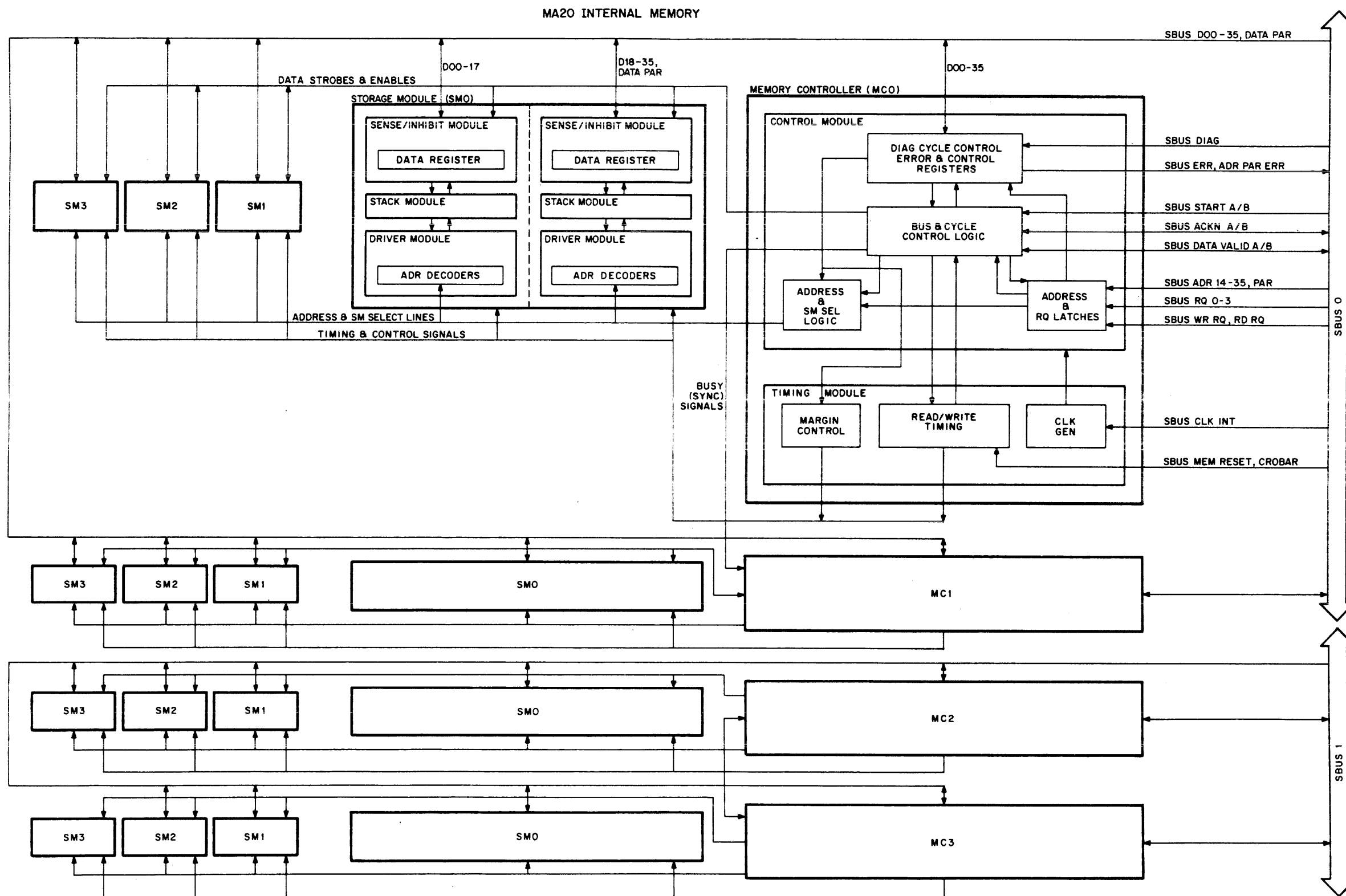


Figure 3 Composite Interface Drawing (Sheet 1 of 2)



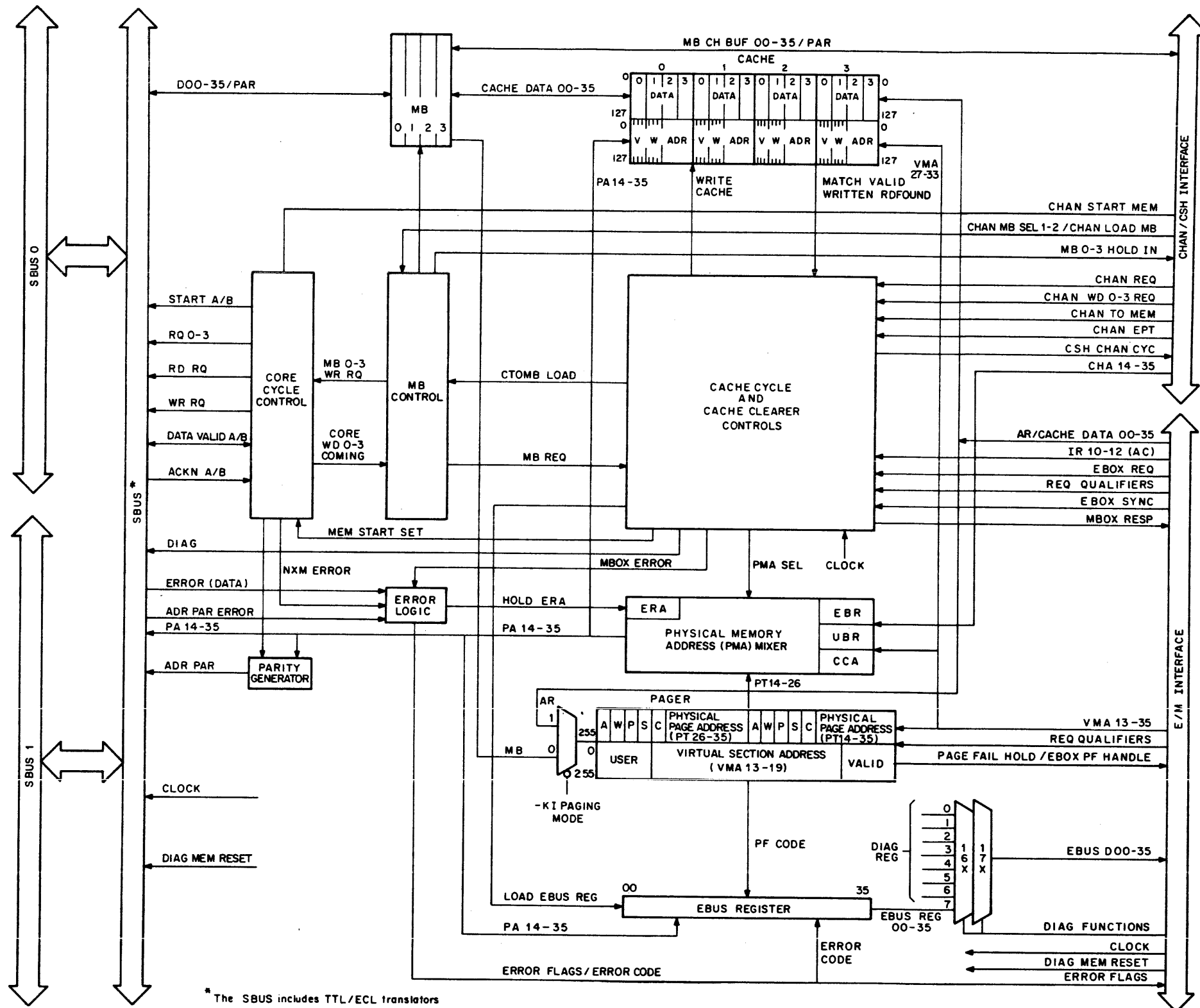
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Figure 3 Composite Interface Drawing (Sheet 2 of 2)



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Figure 4 Front End Channel Functional Block Diagram (Sheet 1 of 6)



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Figure 4 Front End Channel Functional Block Diagram (Sheet 2 of 6)

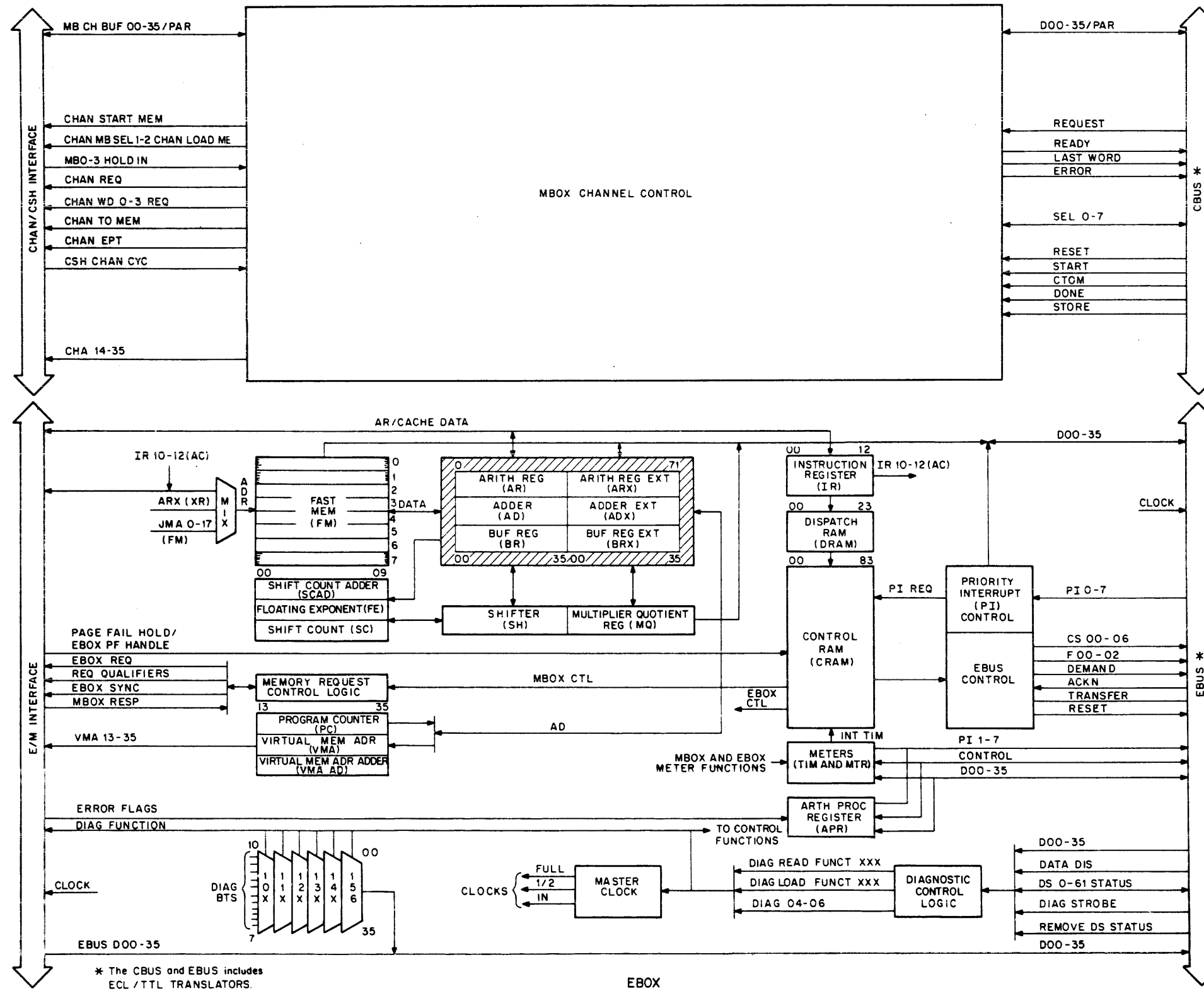
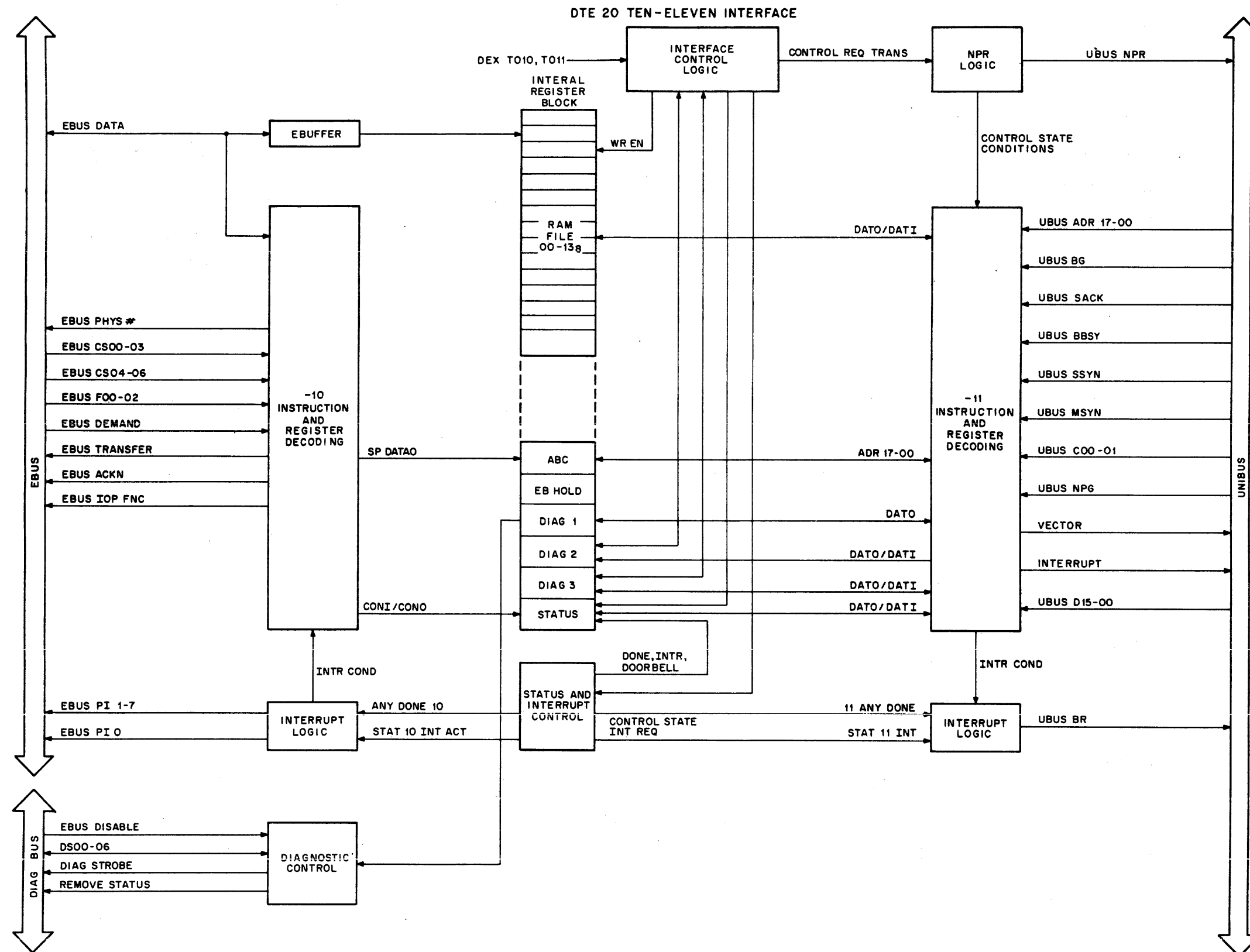


Figure 4 Front End Channel Functional Block Diagram (Sheet 3 of 6)



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Figure 4 Front End Channel Functional Block Diagram (Sheet 4 of 6)

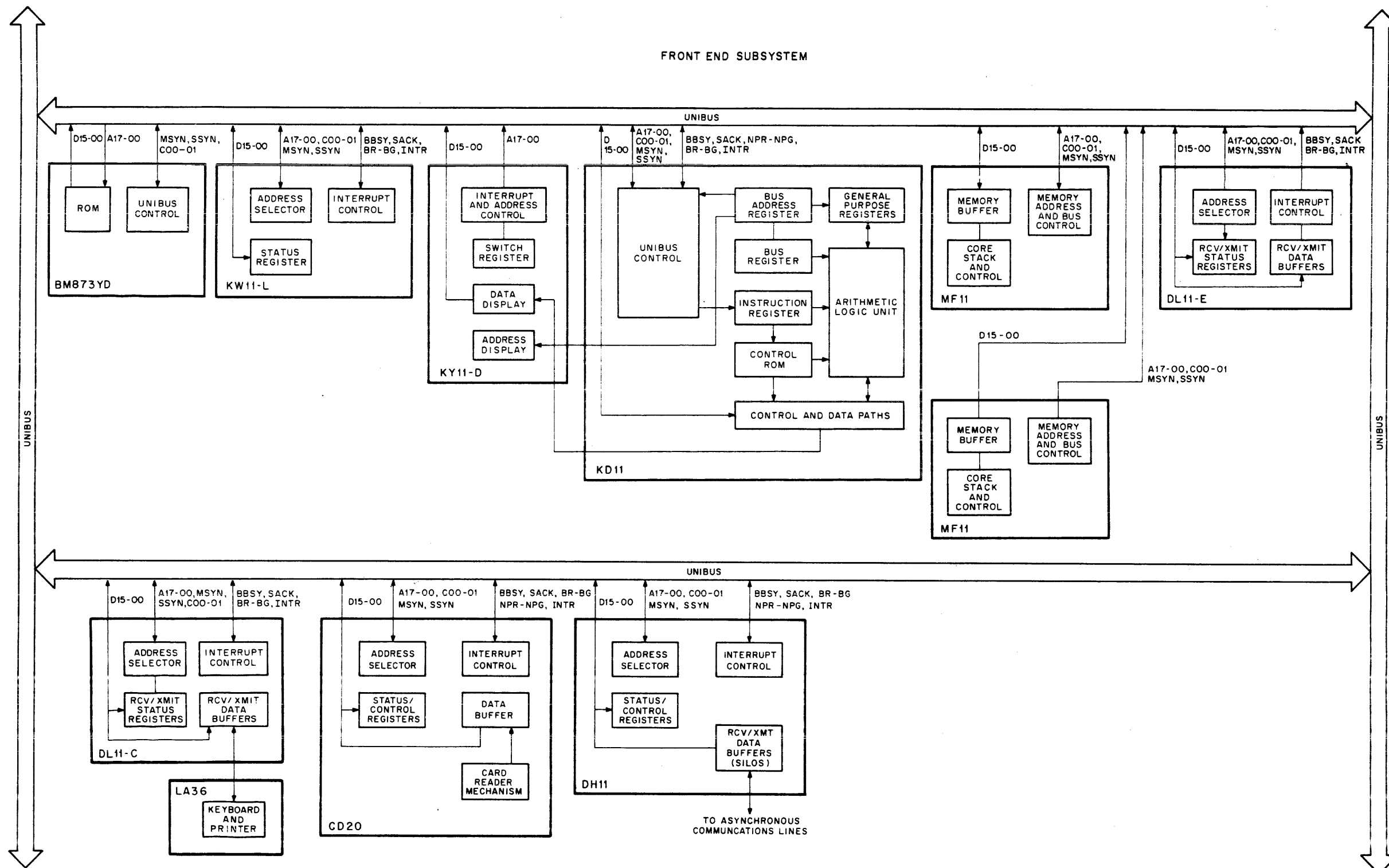
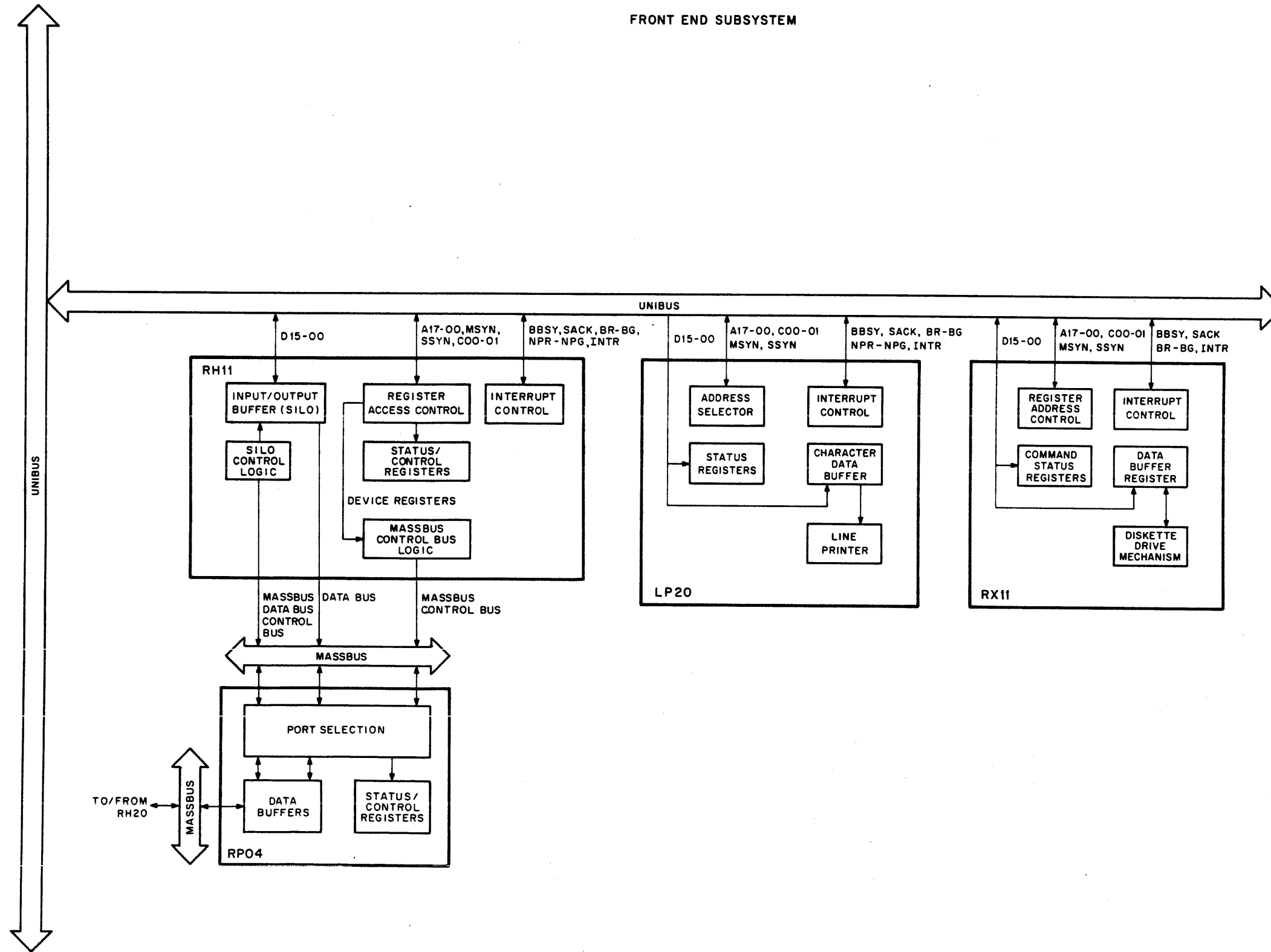


Figure 4 Front End Channel Functional Block Diagram (Sheet 5 of 6)

FRONT END SUBSYSTEM



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Figure 4 Front End Channel Functional Block Diagram (Sheet 6 of 6)

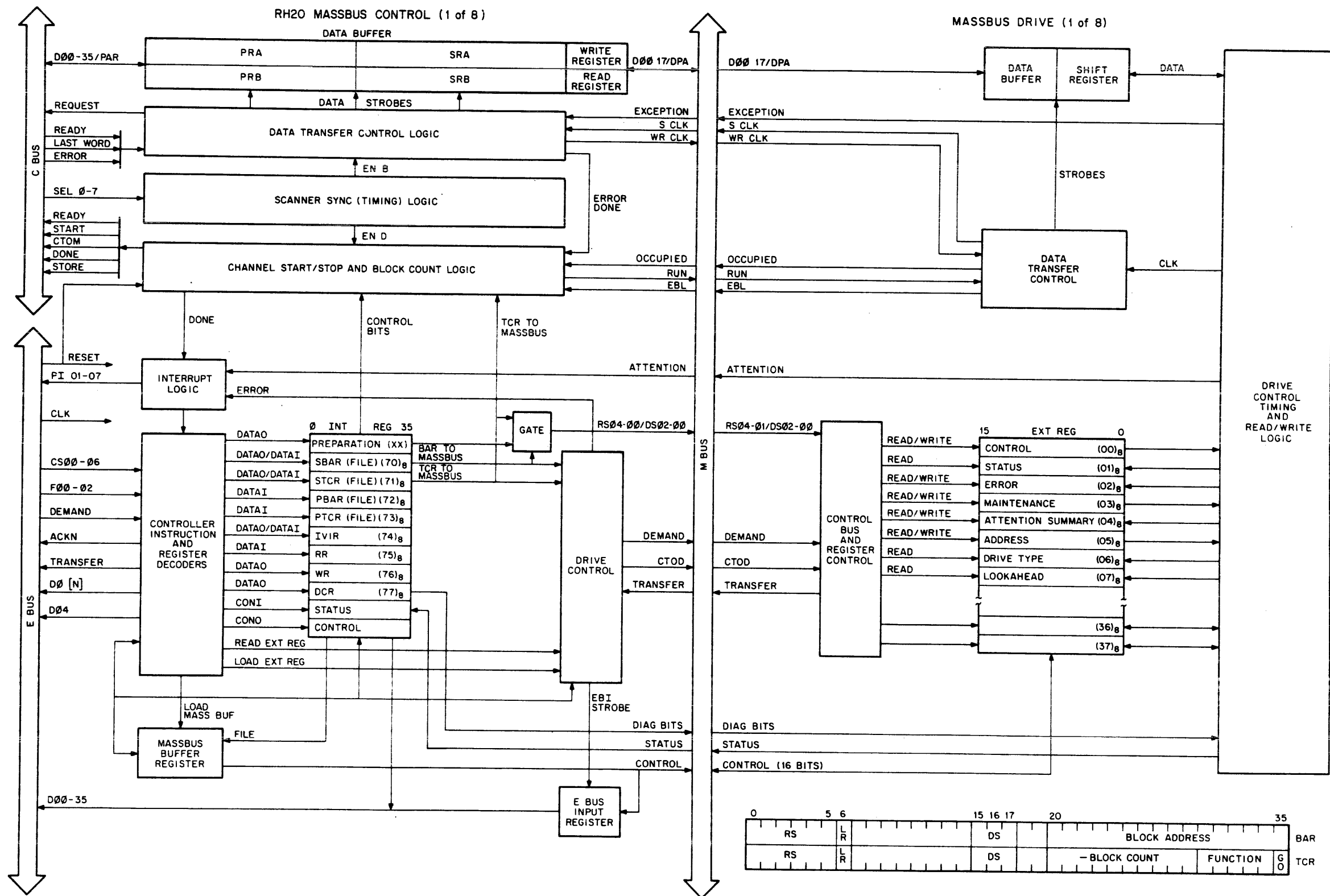
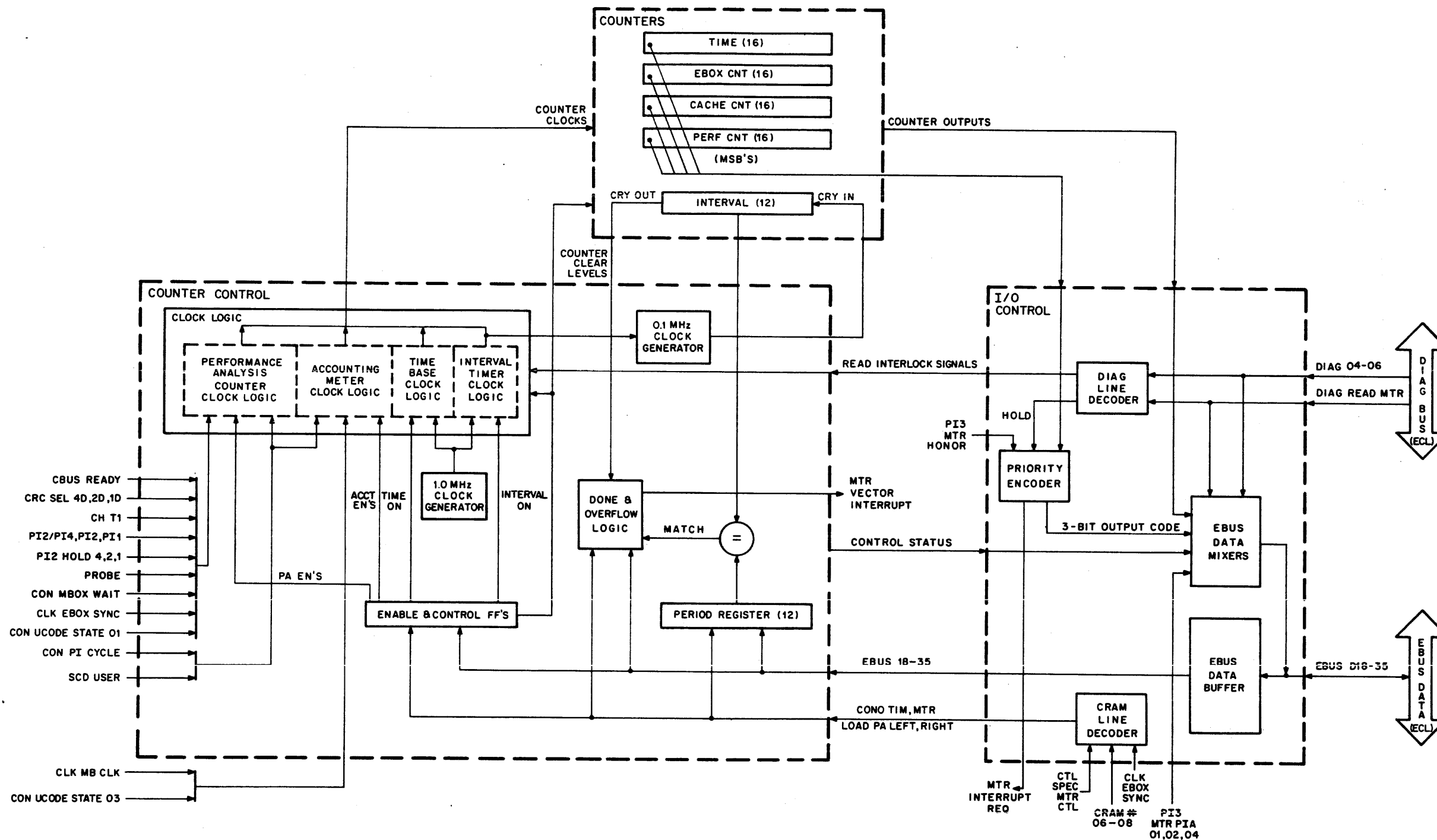


Figure 5 RH20/Massbus Drive Functional Block Diagram



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Figure 6 Meter Board Block Diagram

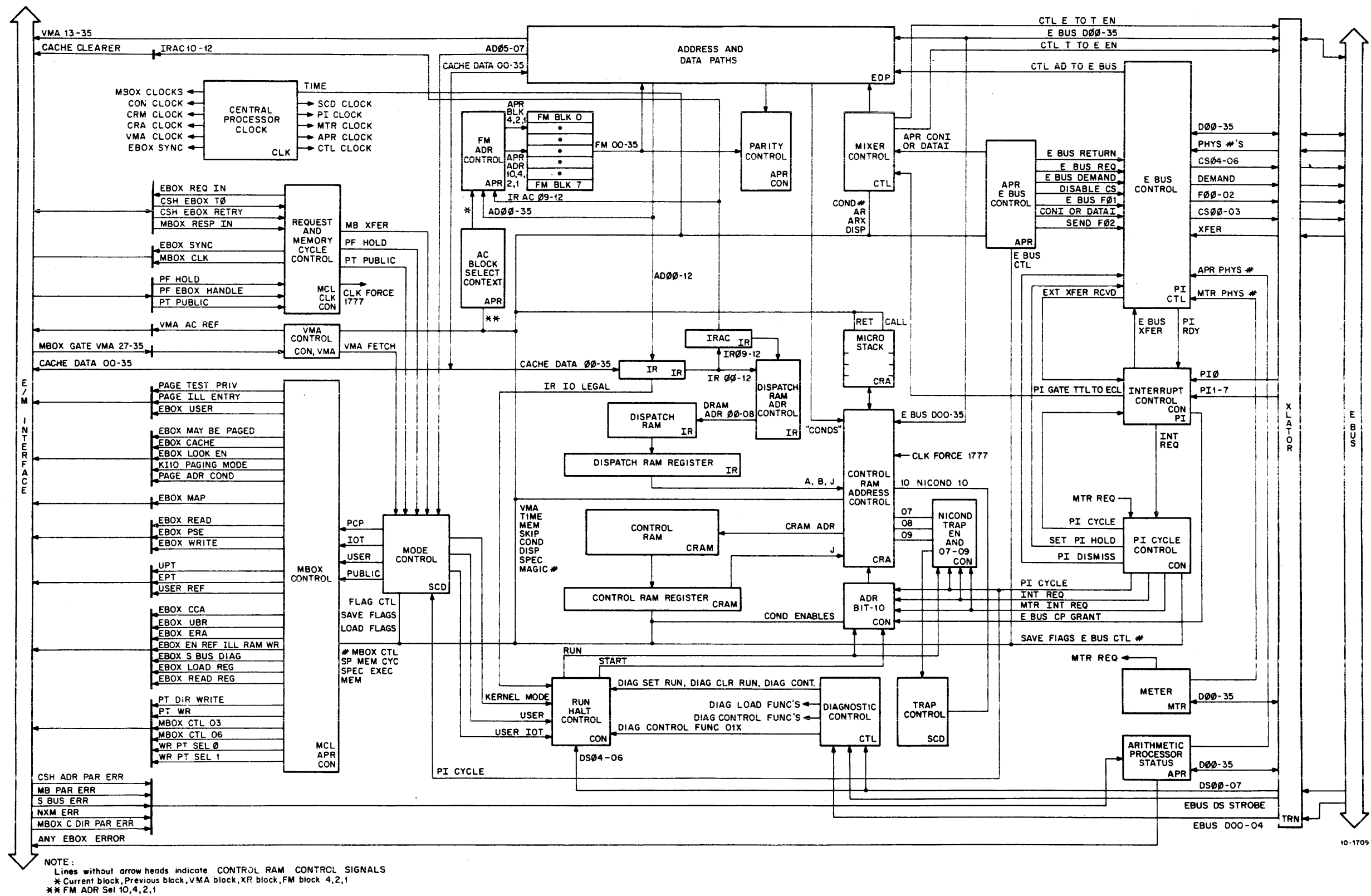
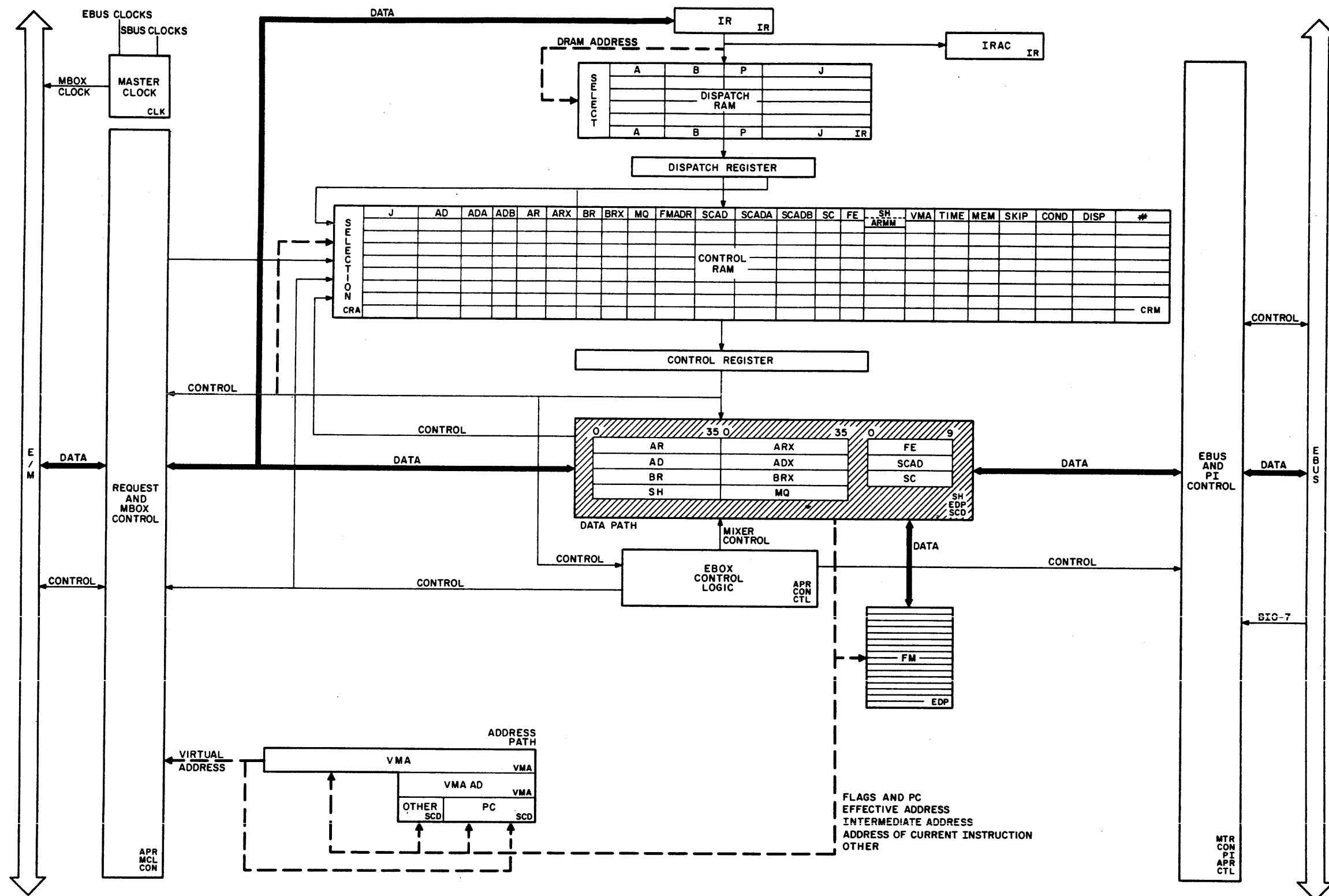


Figure 7 EBox Functional Block Diagram



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Figure 8 EBox RAM Structures Interface and Controls Block Diagram

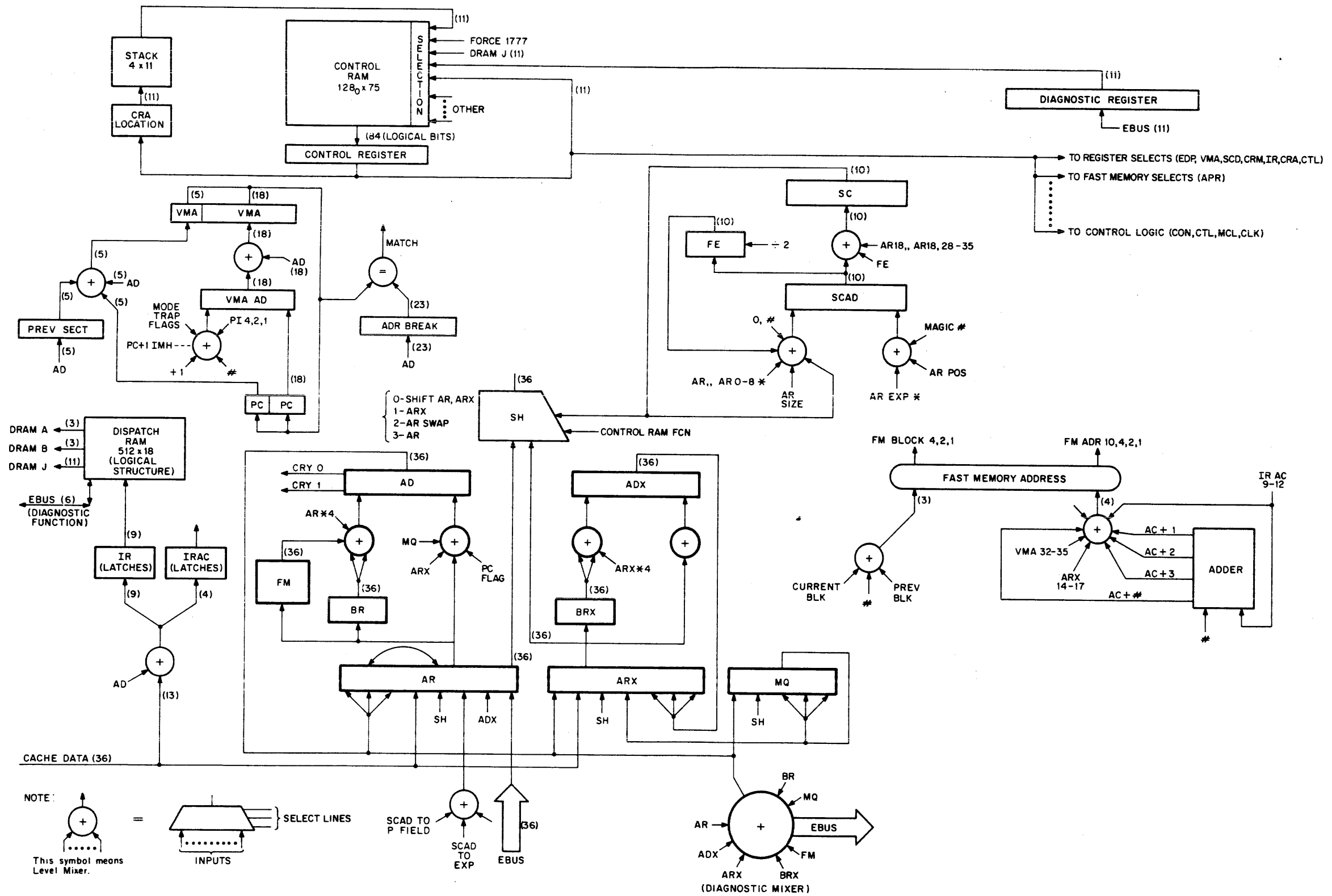


Figure 9 Register Interconnection Diagram

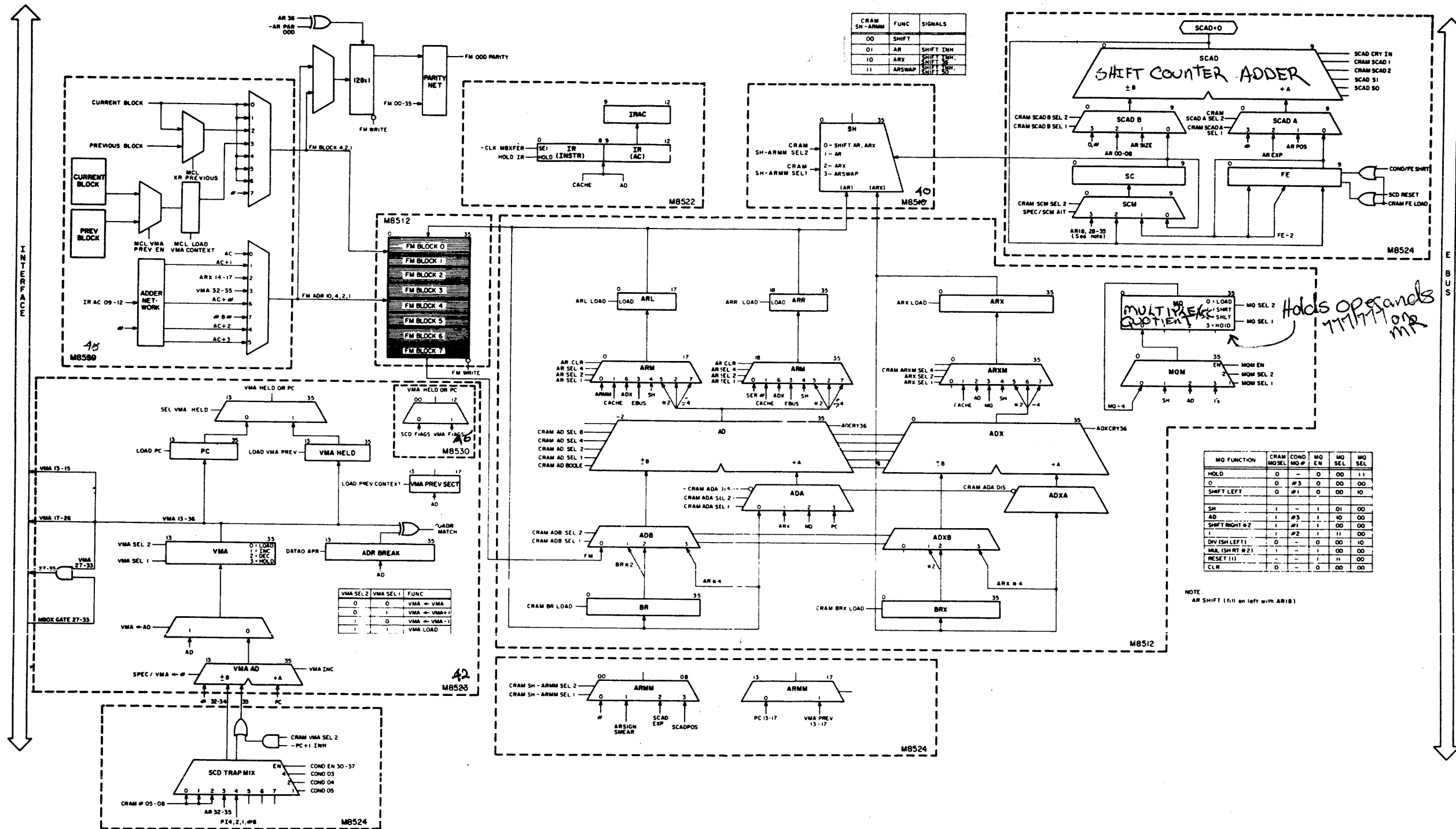


Figure 10 EBox Data and Address Paths

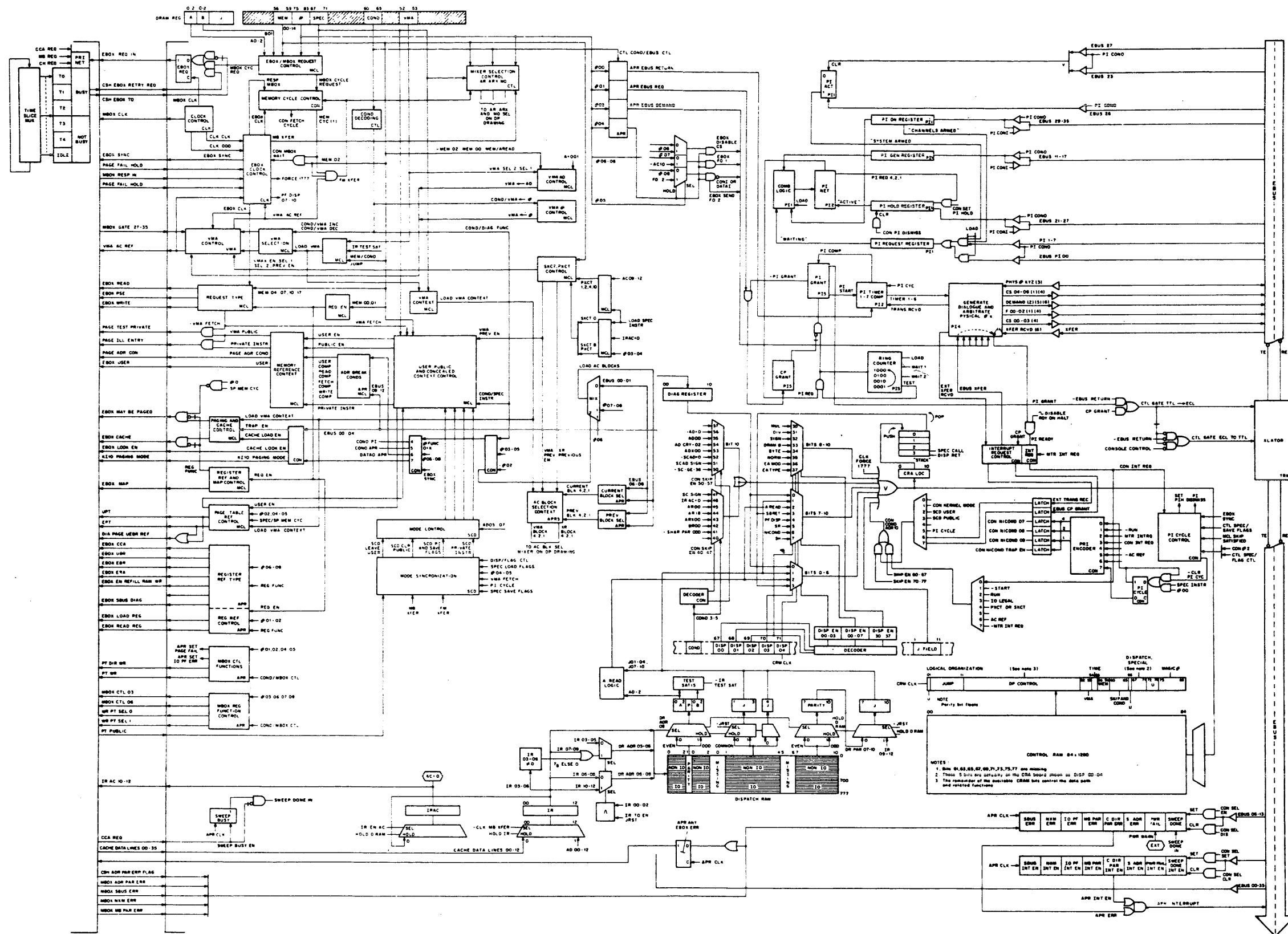


Figure 11 EBox, MBox, and EBus Control Diagram

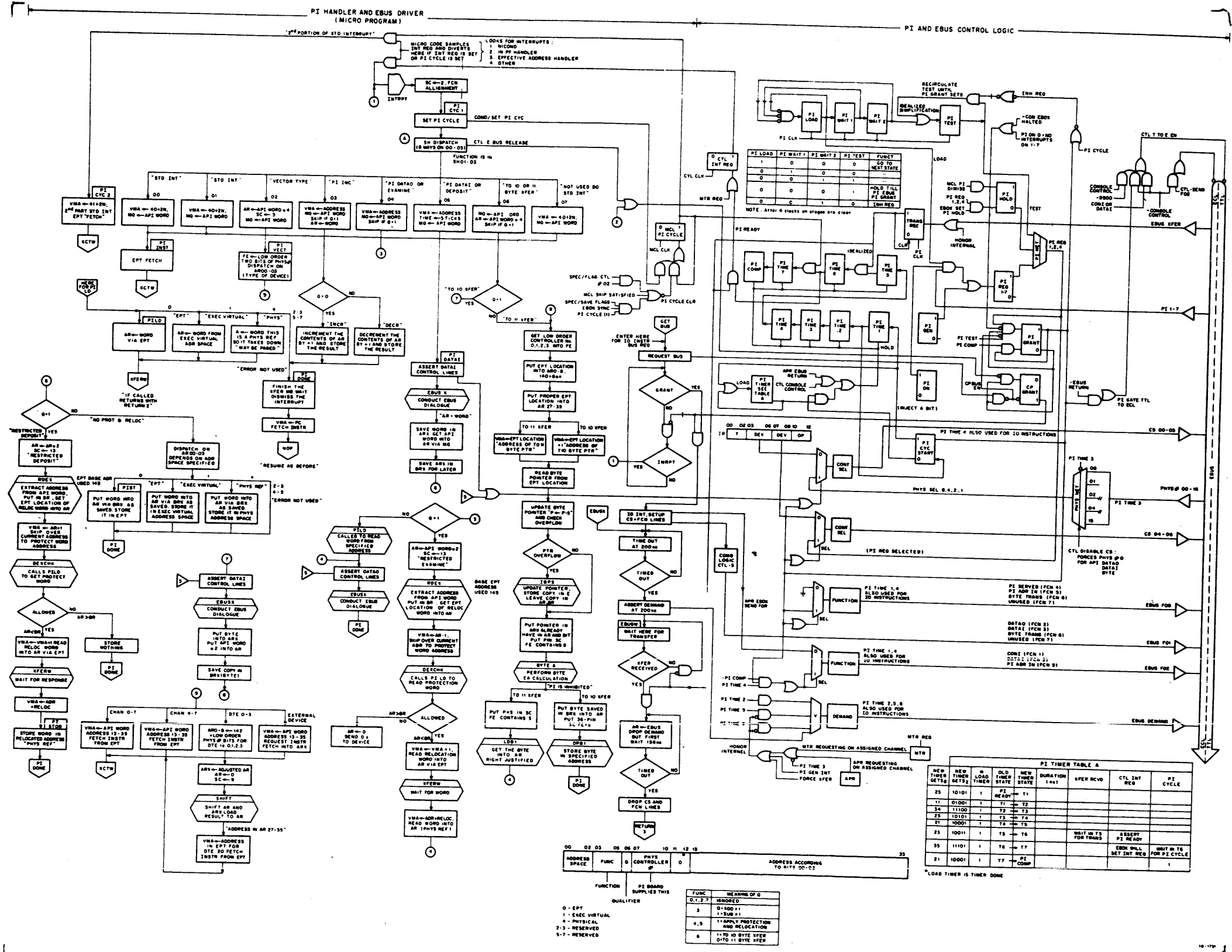


Figure 12 EBus Control, Hybrid Flow Diagram

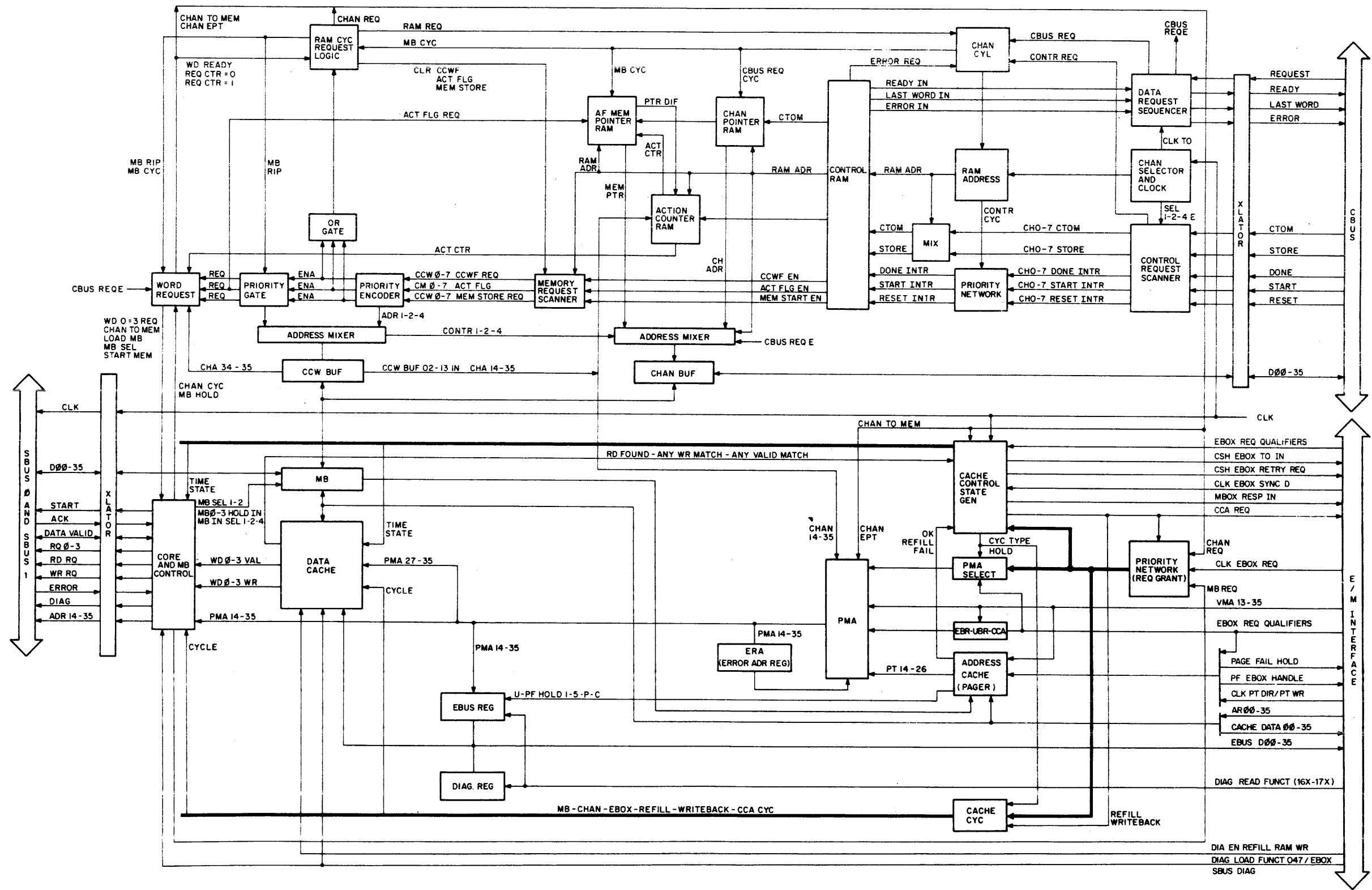
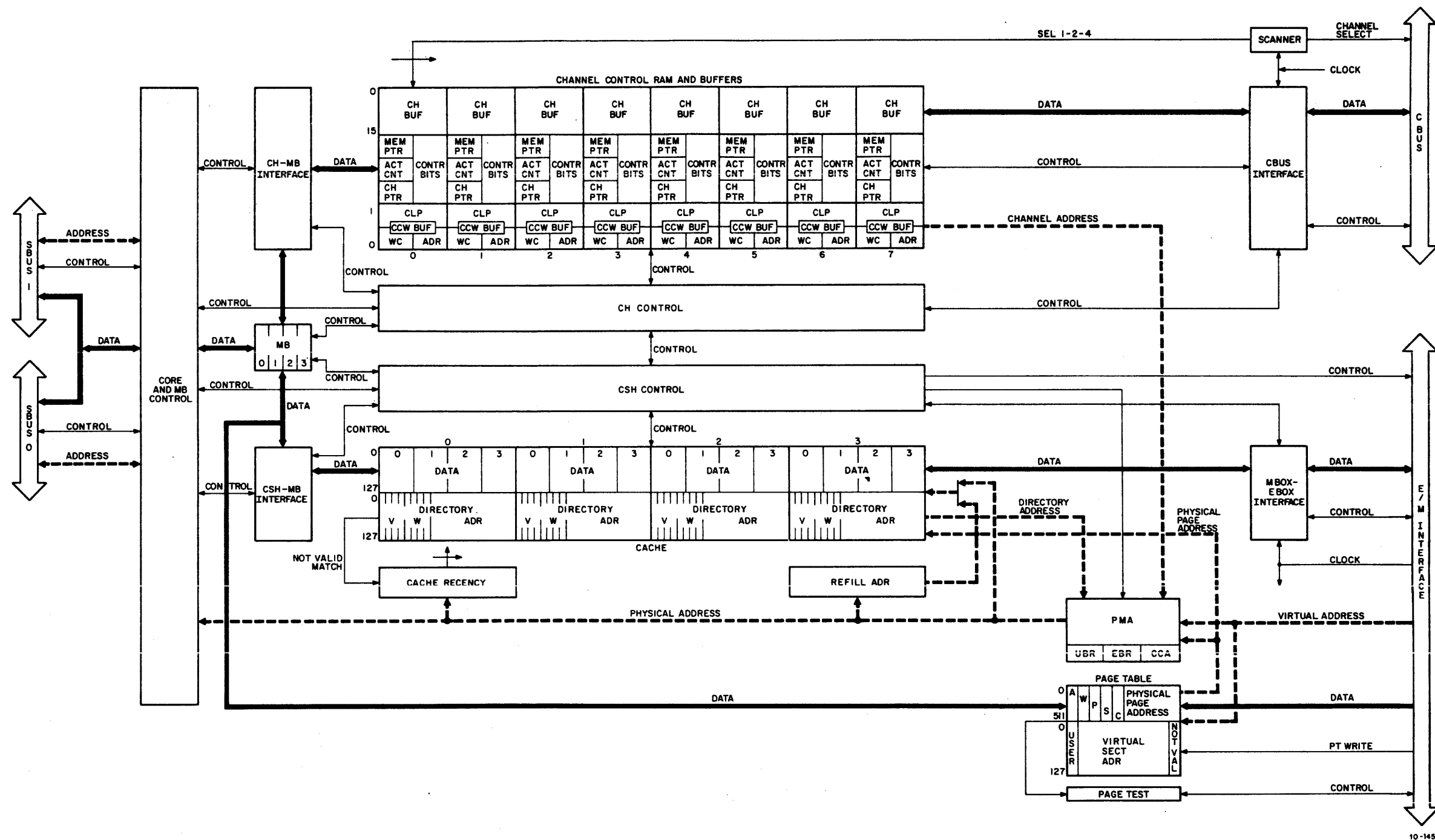


Figure 13 MBox Overall Block Diagram



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Figure 14 MBox RAM Structures Interfaces and Controls Block Diagram

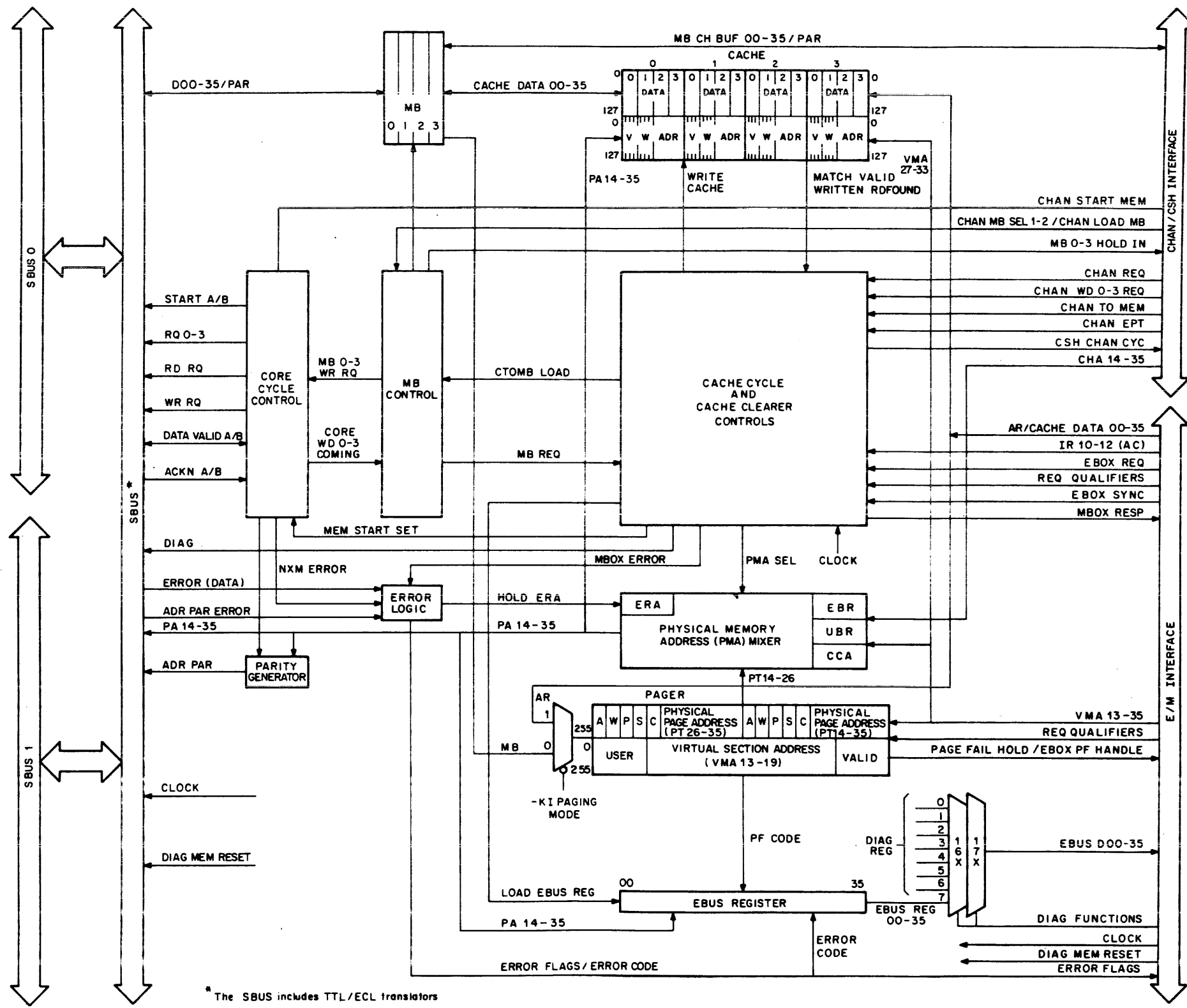
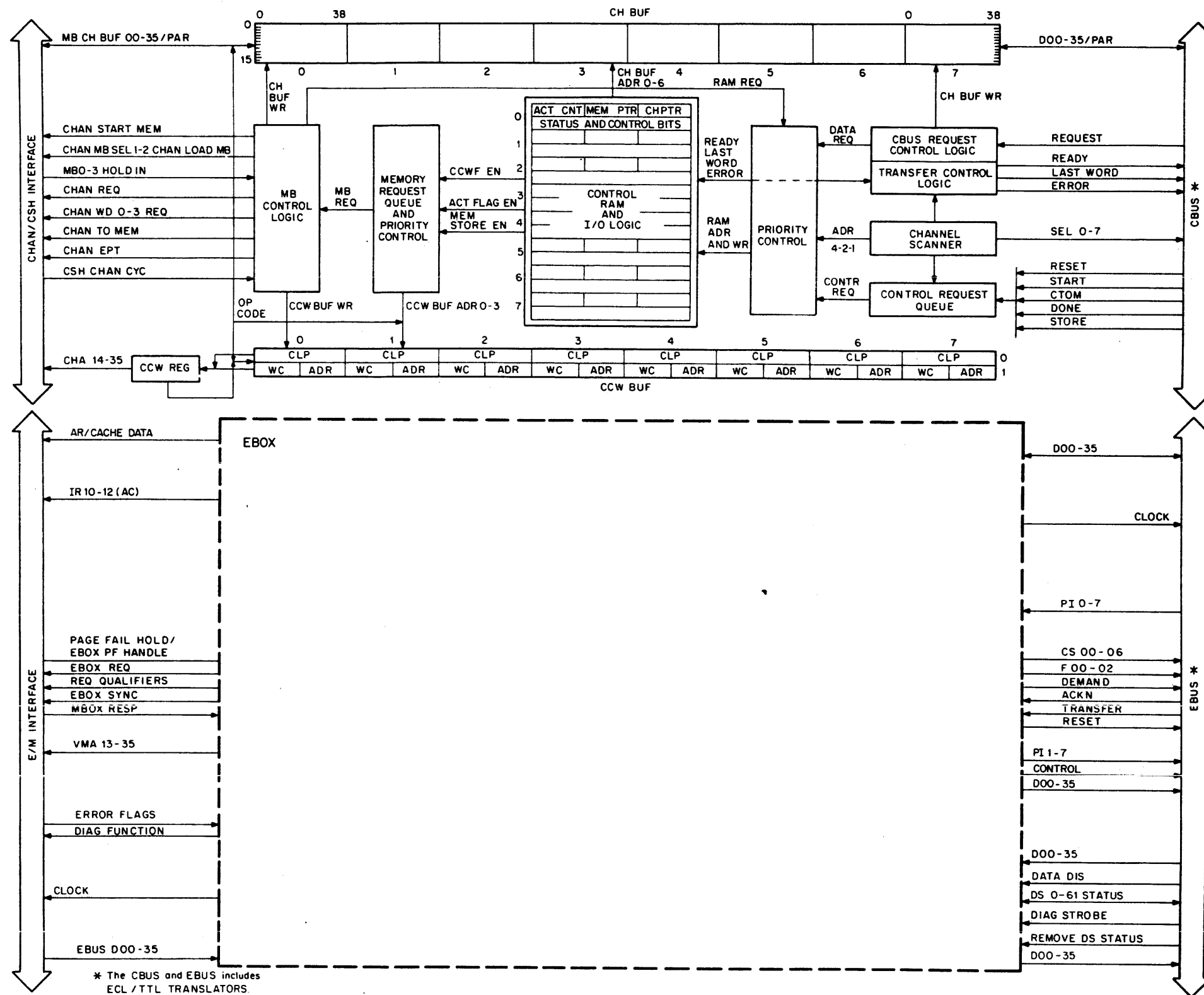


Figure 15 MBox Functional Block Diagram (Sheet 1 of 2)



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Figure 15 MBox Functional Block Diagram (Sheet 2 of 2)

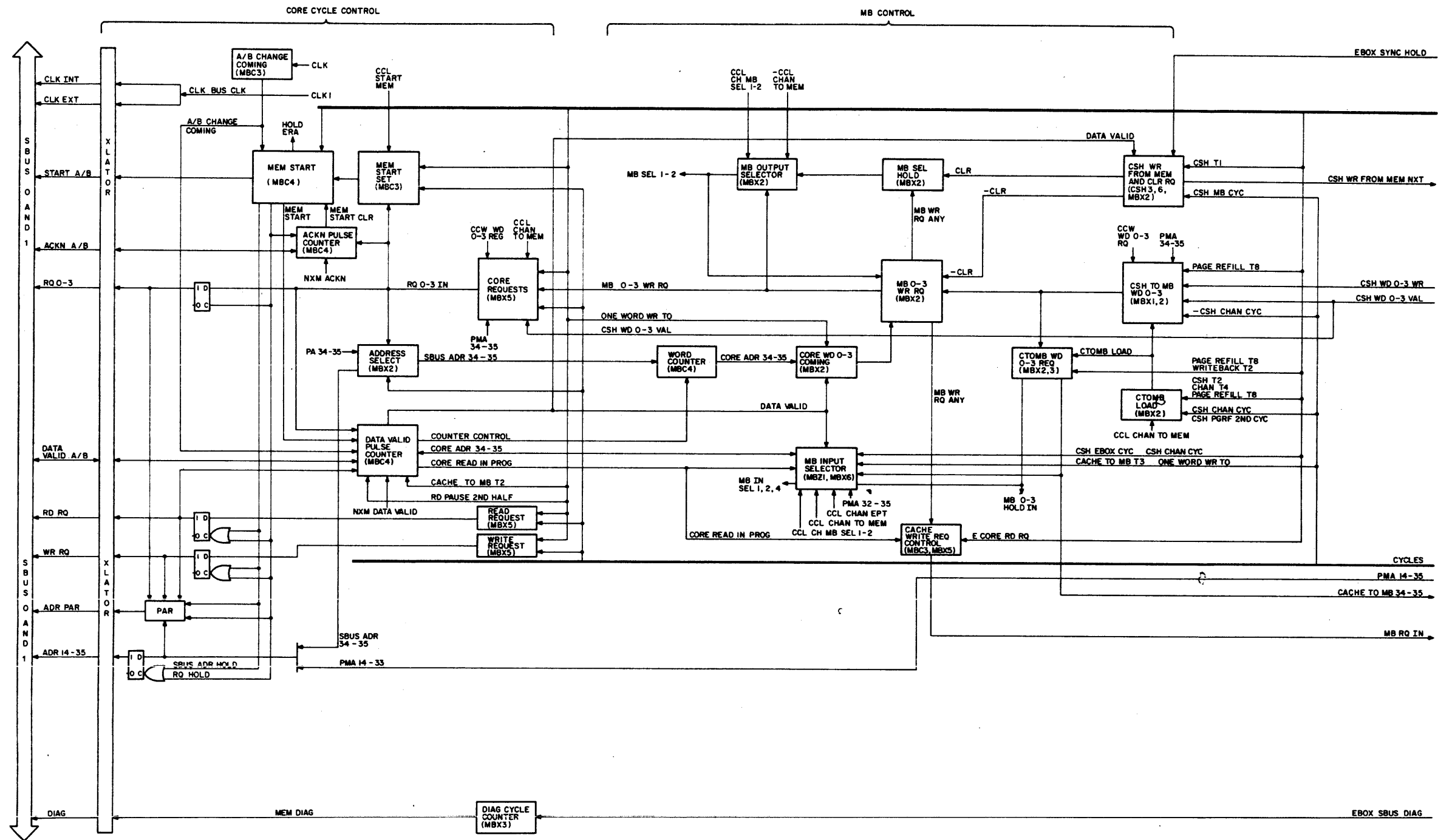


Figure 17 MBox Control Logic Block Diagram (Sheet 1 of 2)

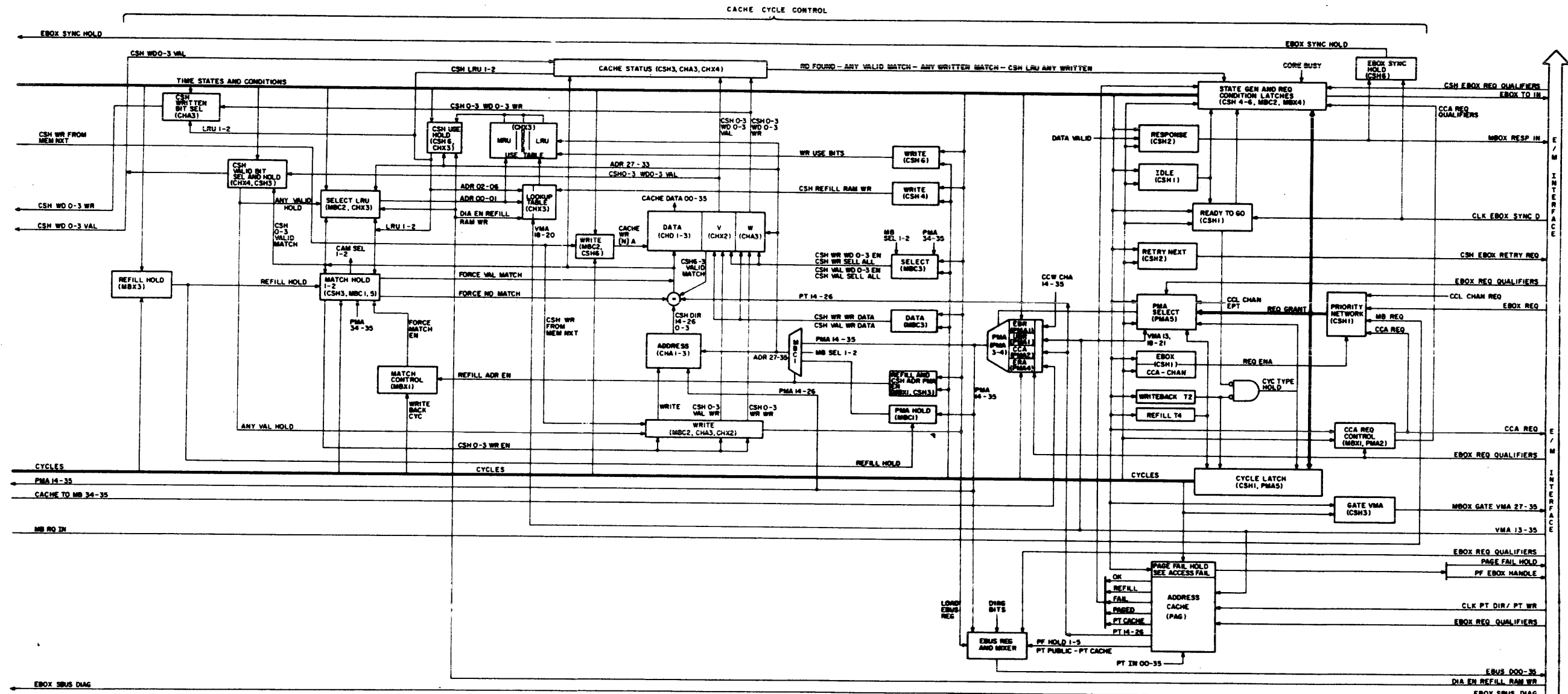
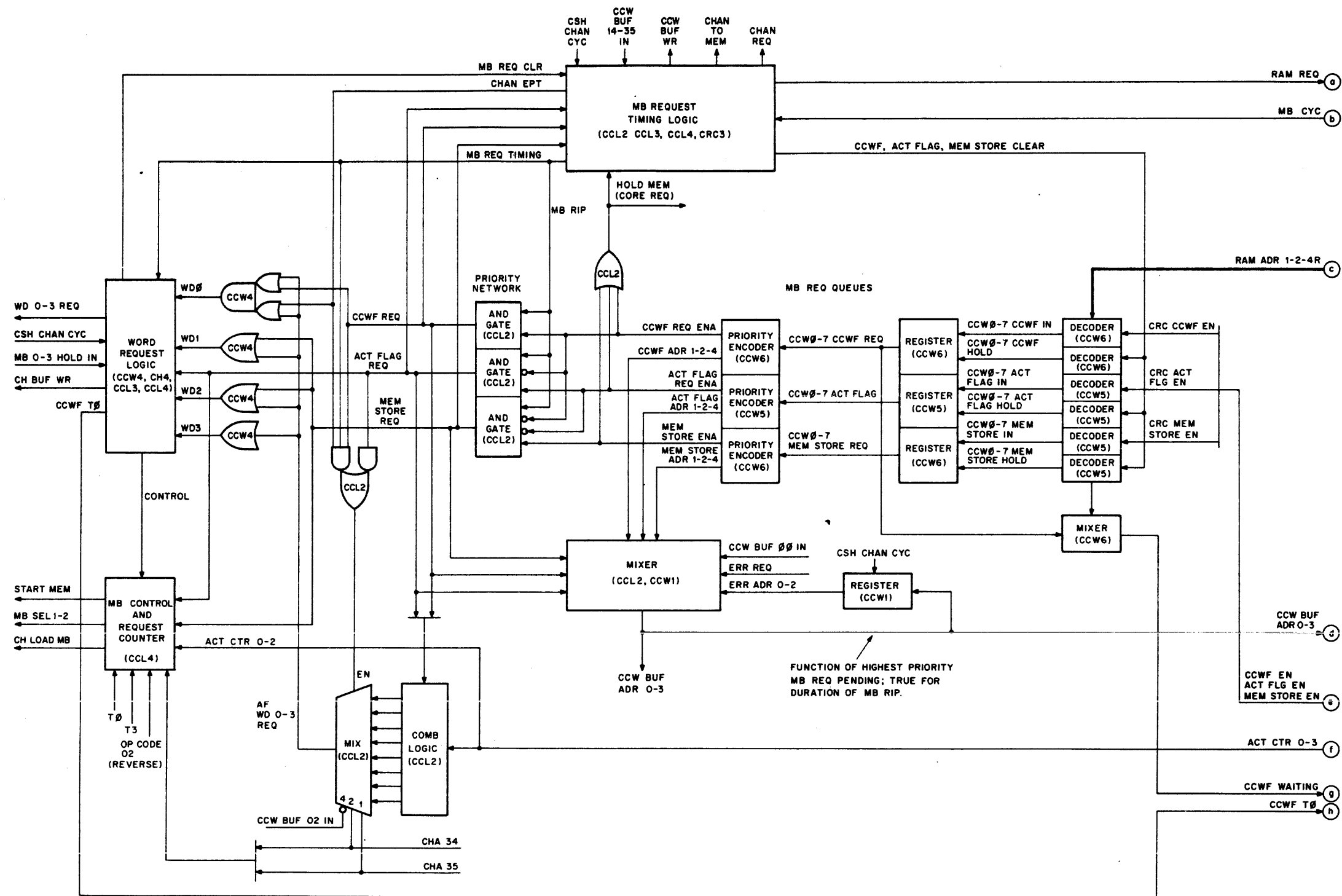


Figure 17 MBox Control Logic Block Diagram (Sheet 2 of 2)



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Figure 18 MBox Channel Control Logic Block Diagram (Sheet 1 of 3)

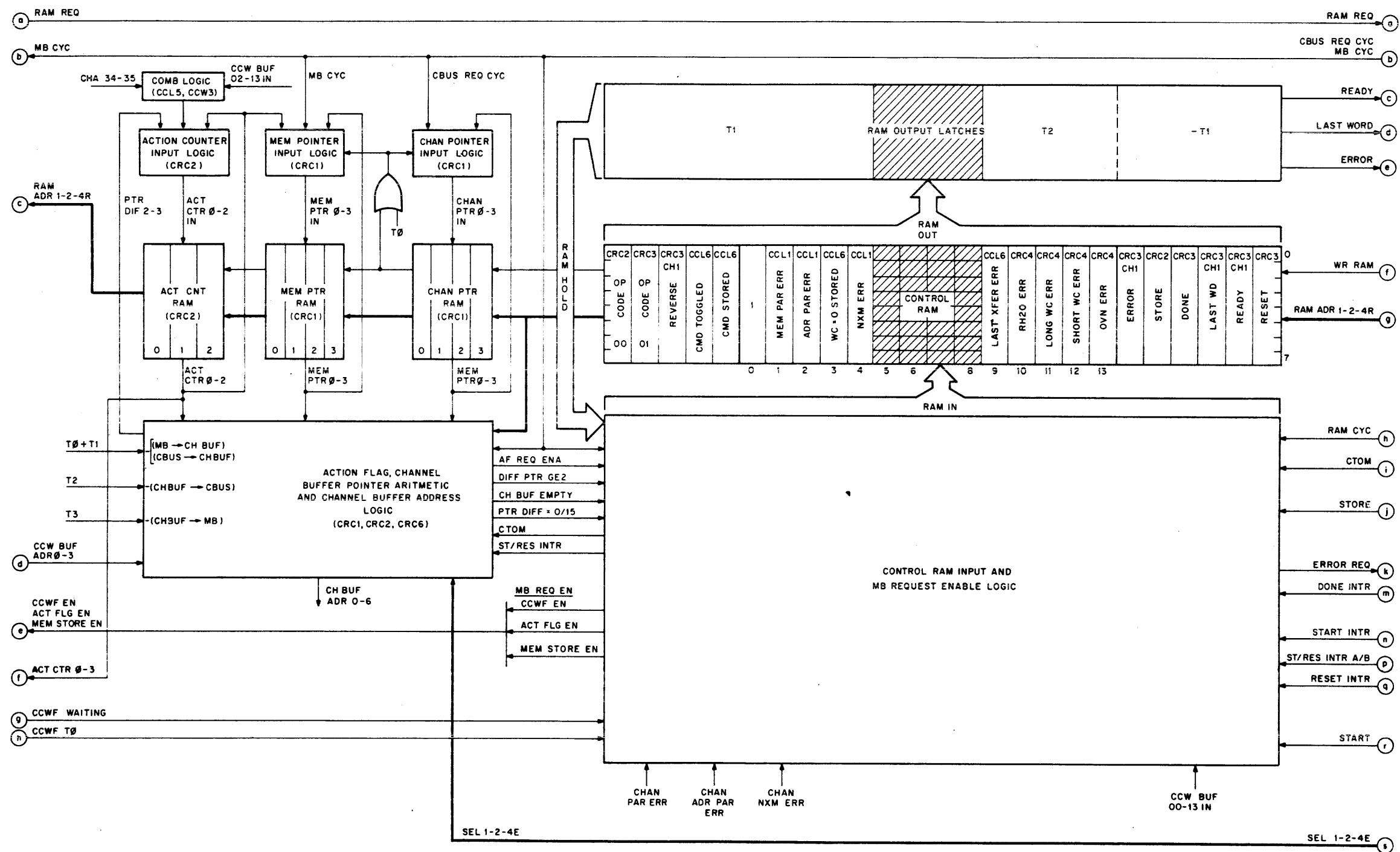
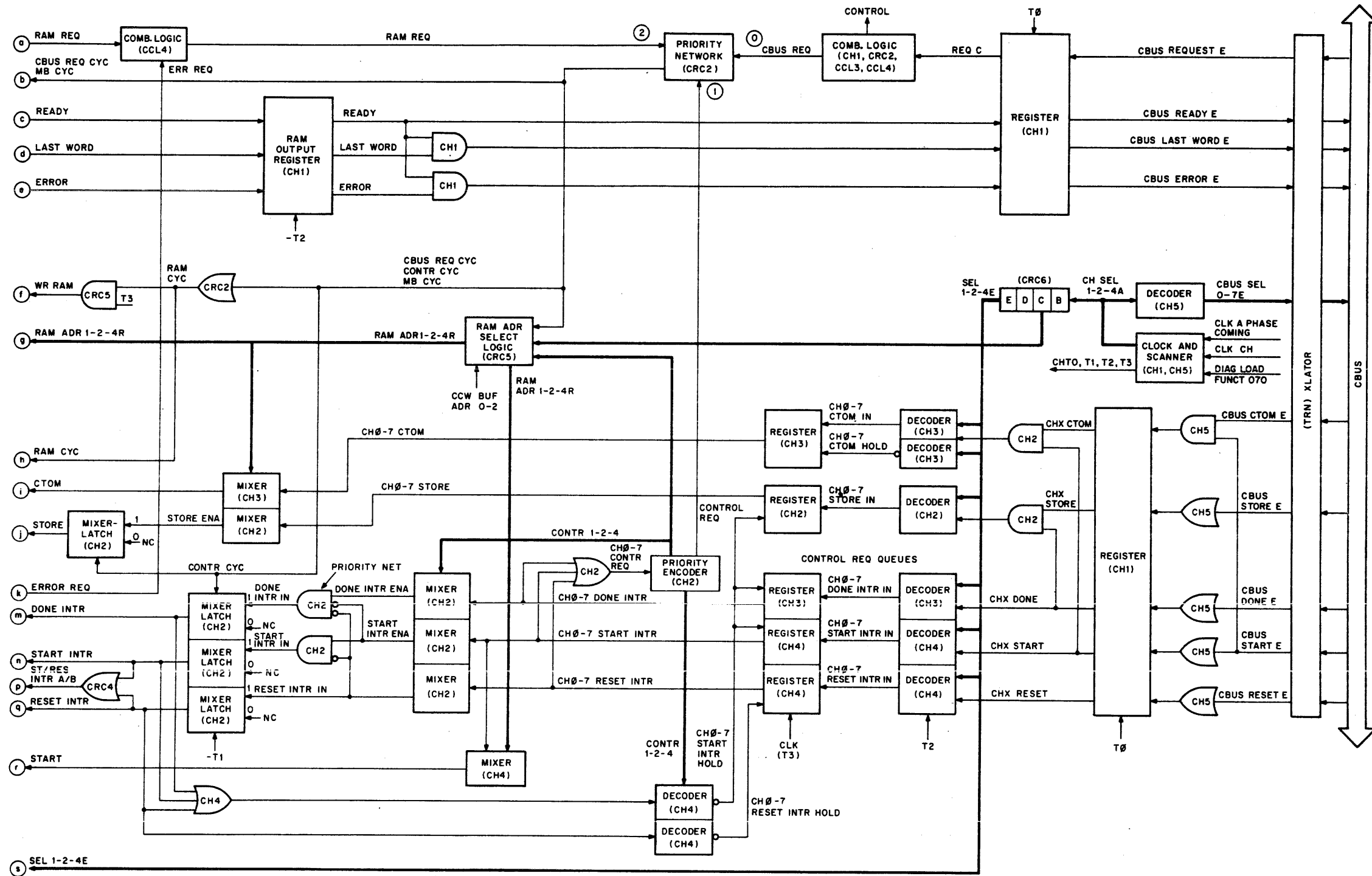


Figure 18 MBox Channel Control Logic Block Diagram (Sheet 2 of 3)



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Figure 18 MBox Channel Control Logic Block Diagram (Sheet 3 of 3)

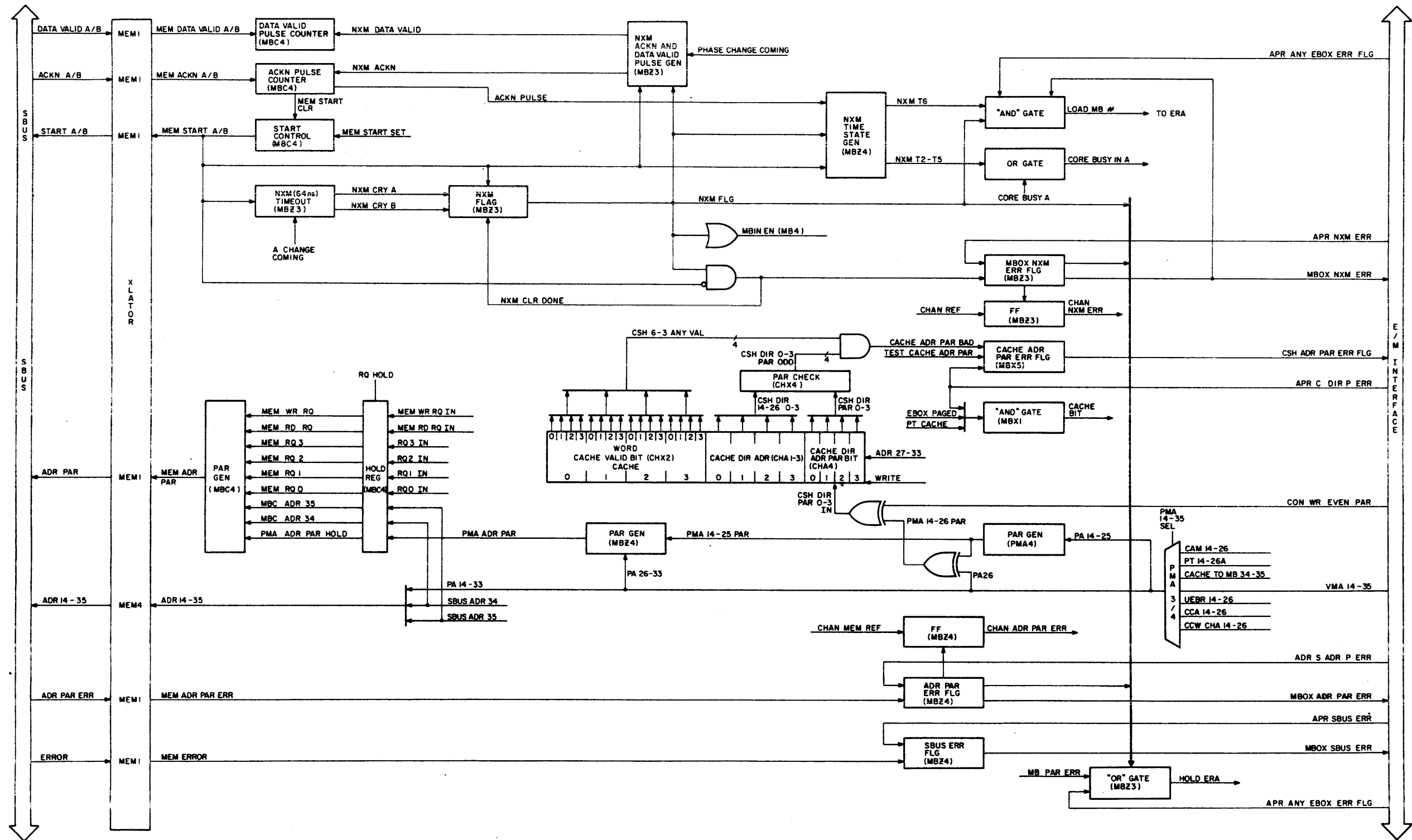
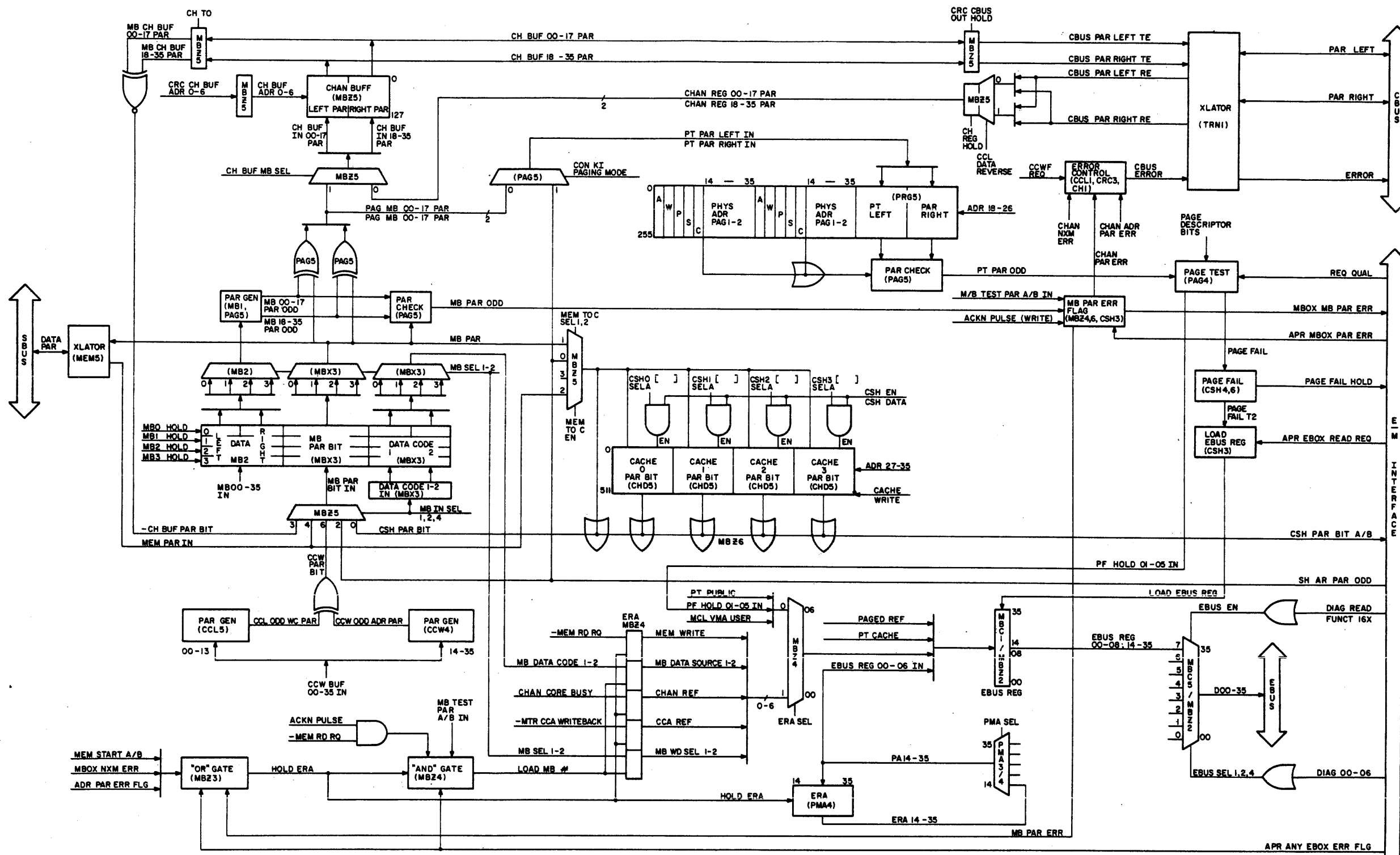


Figure 19 MBox Address Parity, NXM and SBus Error, Path Diagram



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Figure 20 MBox Data and Page Table, Path Diagram

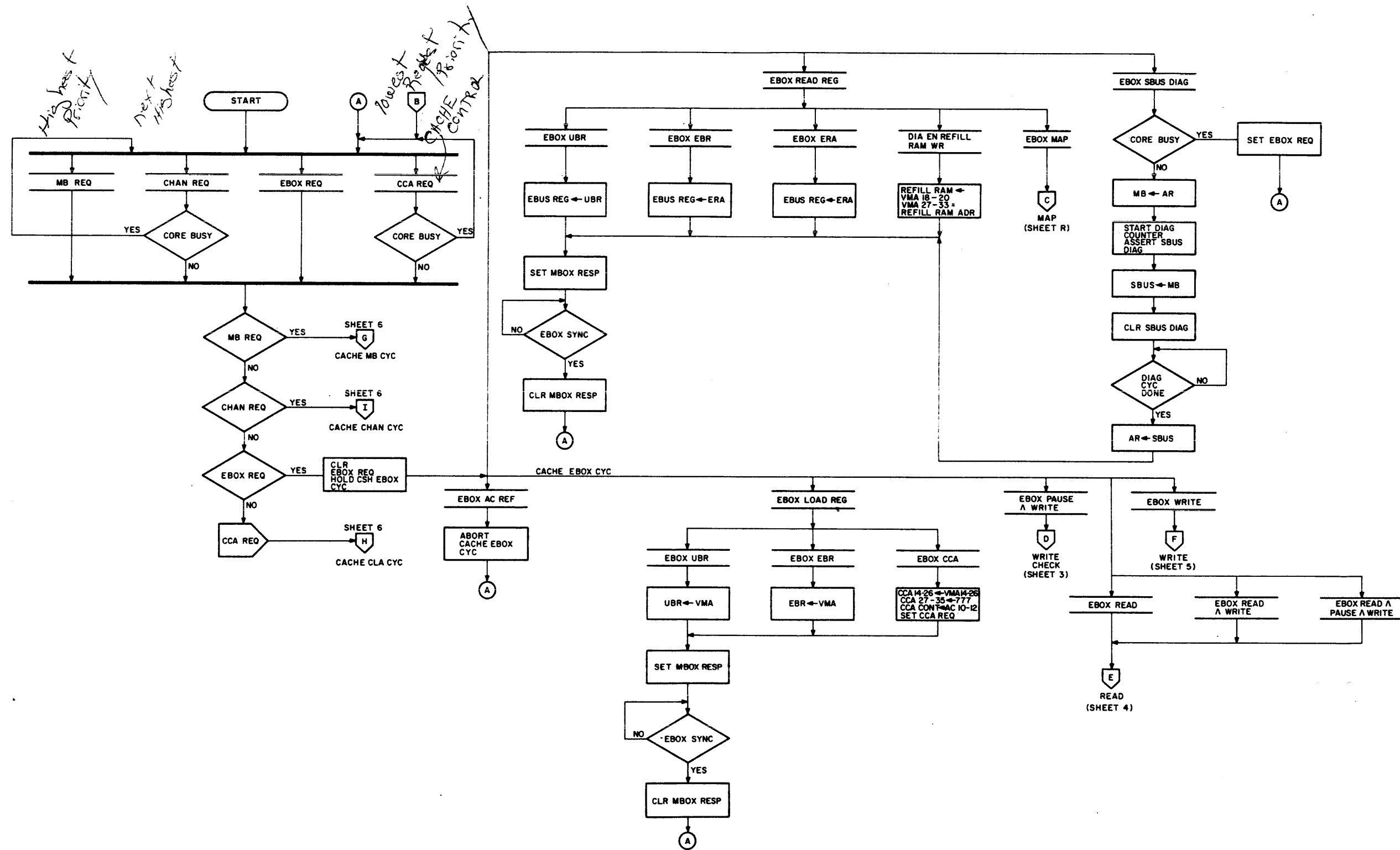
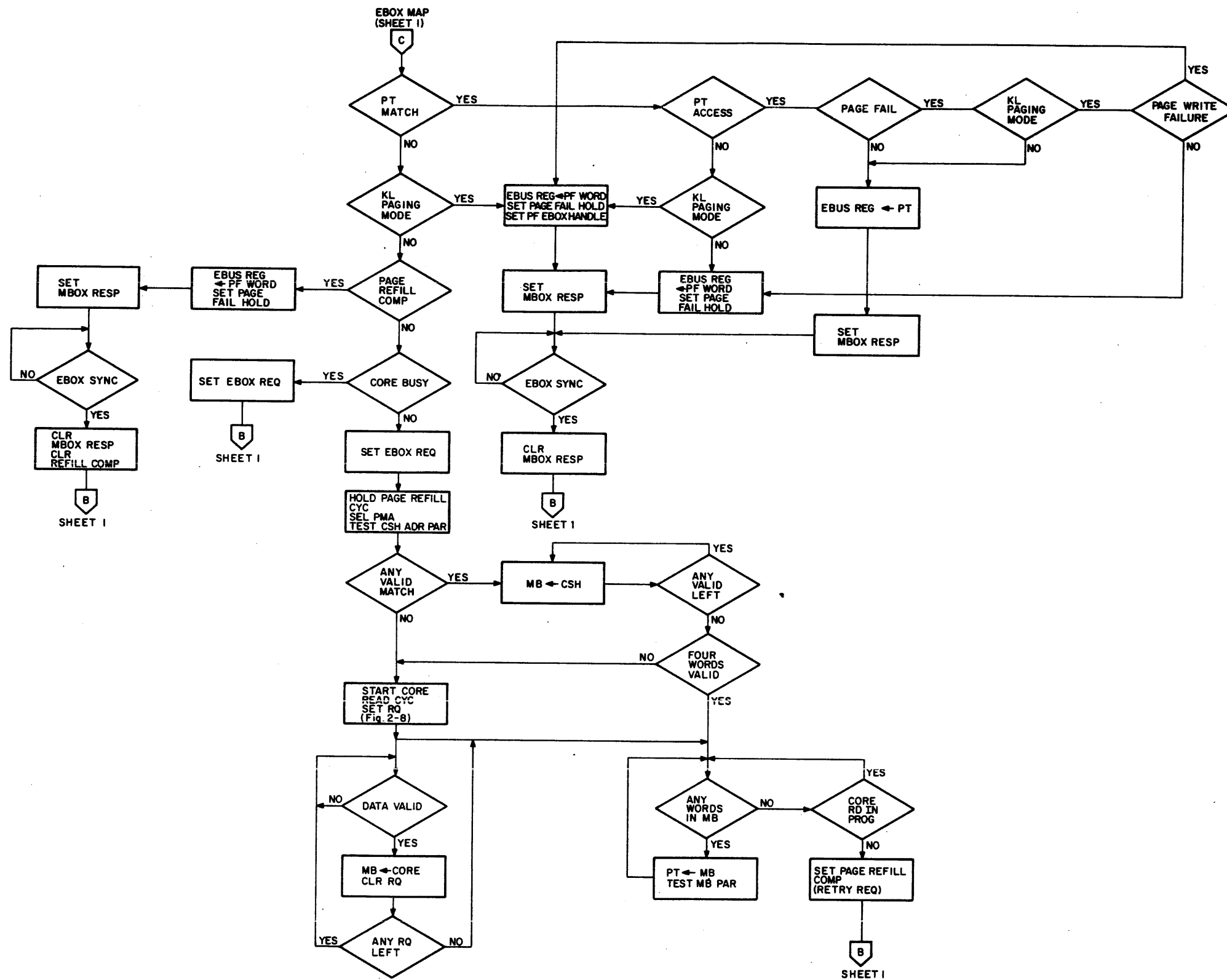
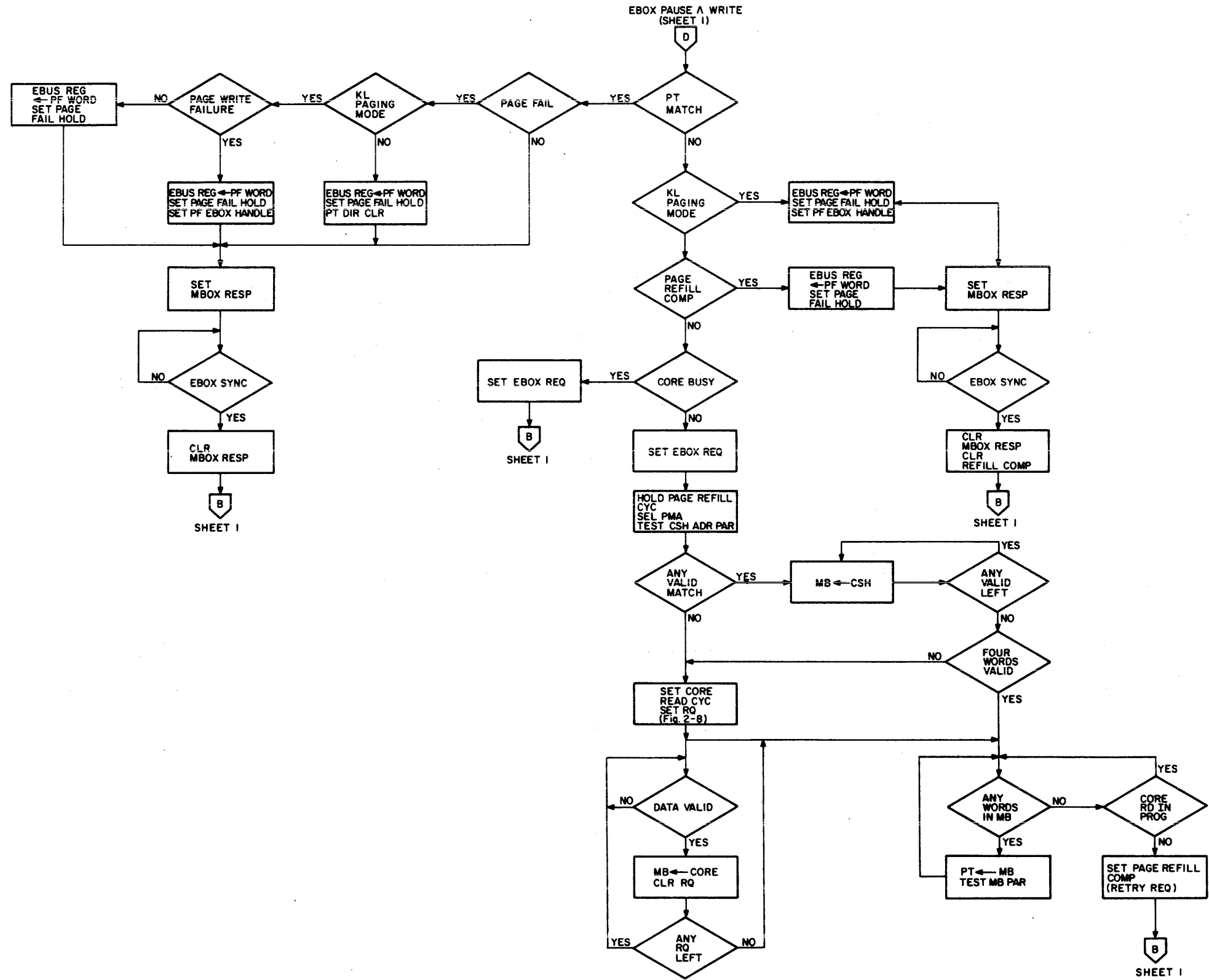


Figure 21 MBox Cache Cycle Control Functional Flow Diagram (Sheet 1 of 6)



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Figure 21 MBox Cache Cycle Control Functional Flow Diagram (Sheet 2 of 6)



10-1478

Figure 21 MBox Cache Cycle Control Functional Flow Diagram (Sheet 3 of 6)

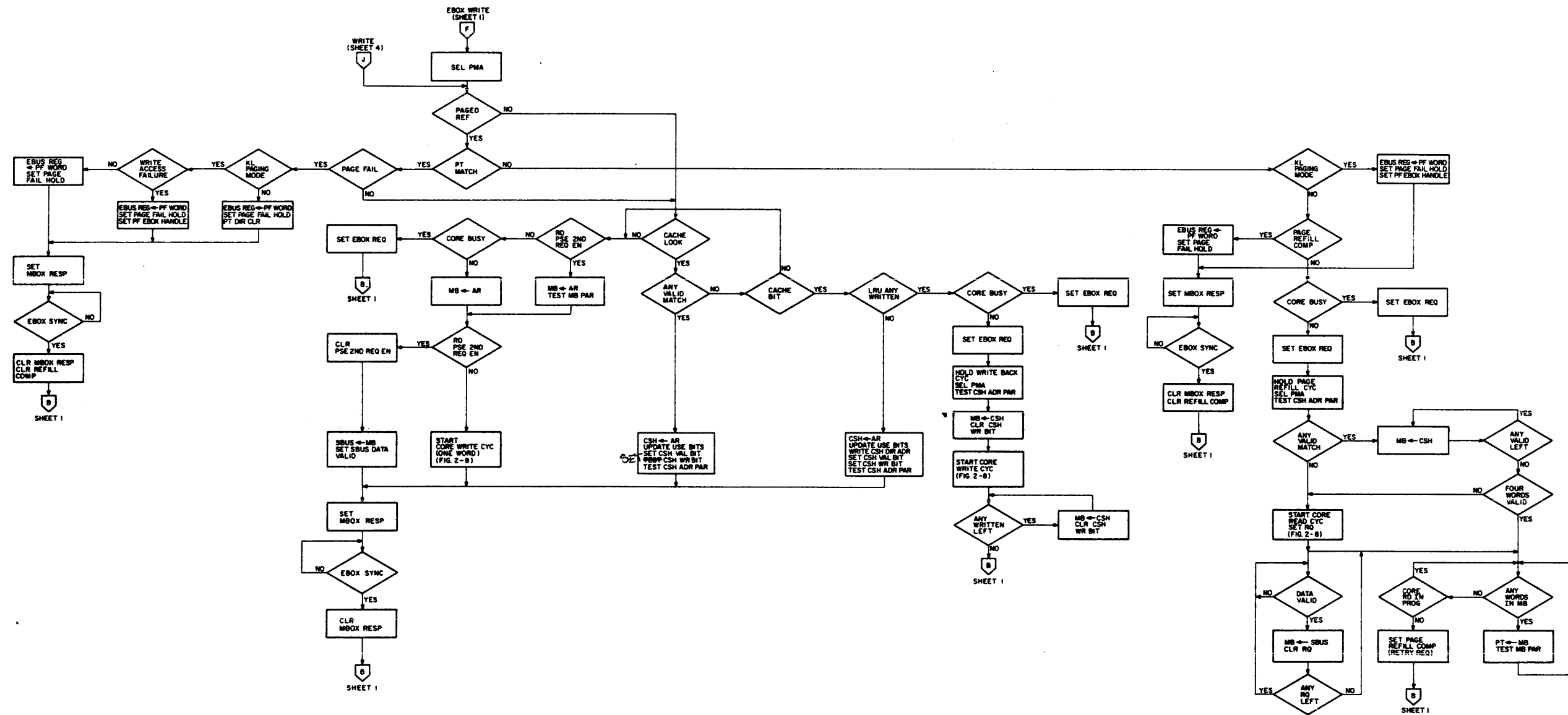
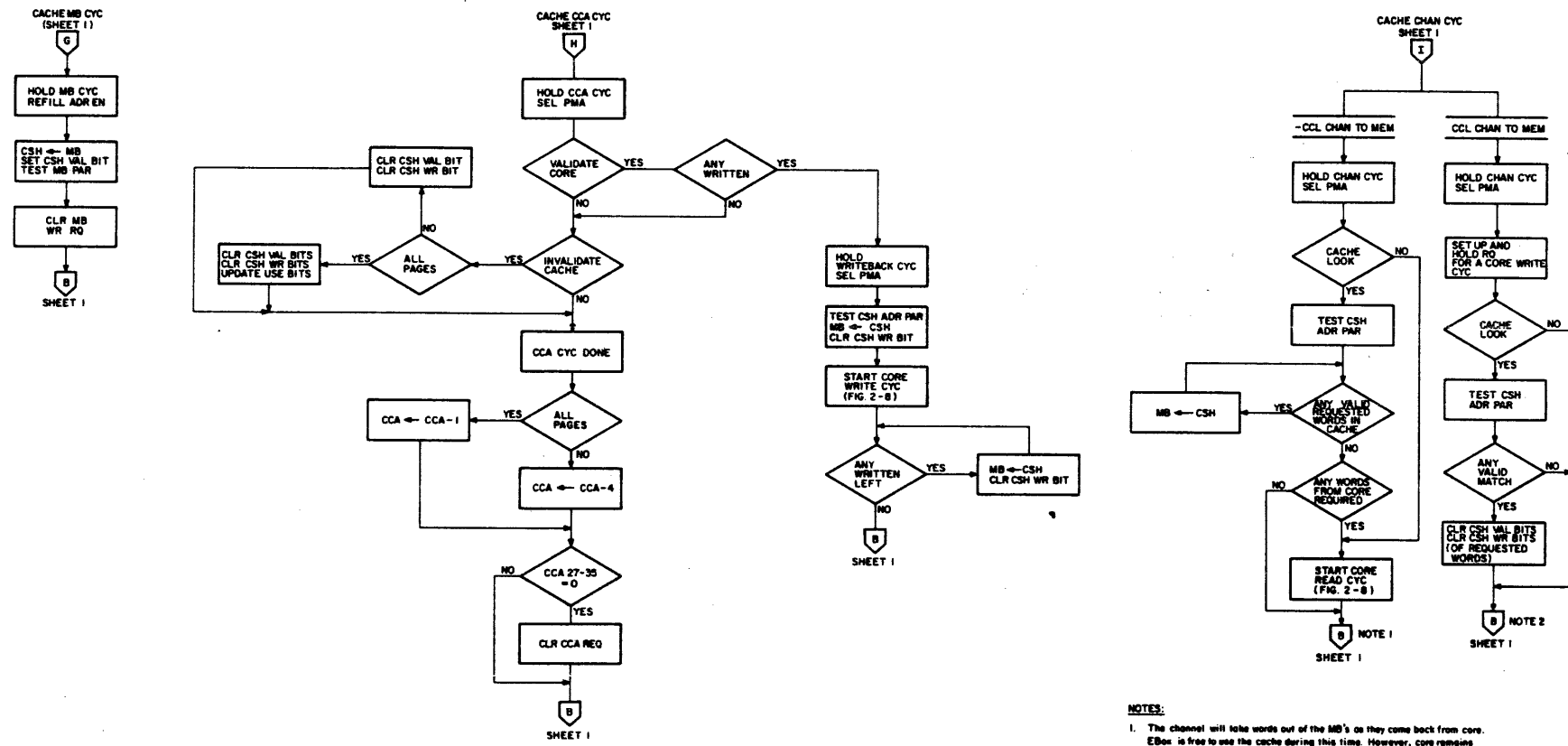


Figure 21 MBox Cache Cycle Control Functional Flow Diagram (Sheet 5 of 6)



NOTES:

1. The channel will take words out of the MB's as they come back from core. EBox is free to use the cache during this time. However, core remains busy and prevents the EBox from getting a core cycle.
2. The channel takes control at this point. The channel loads a word into the MB's and starts a core write cycle. The channel then loads any remaining words into the MB's. EBox is free to use the cache during this time. However, Core remains busy and prevents the EBox from getting a core cycle.

10-1481

Figure 21 MBox Cache Cycle Control Functional Flow Diagram (Sheet 6 of 6)

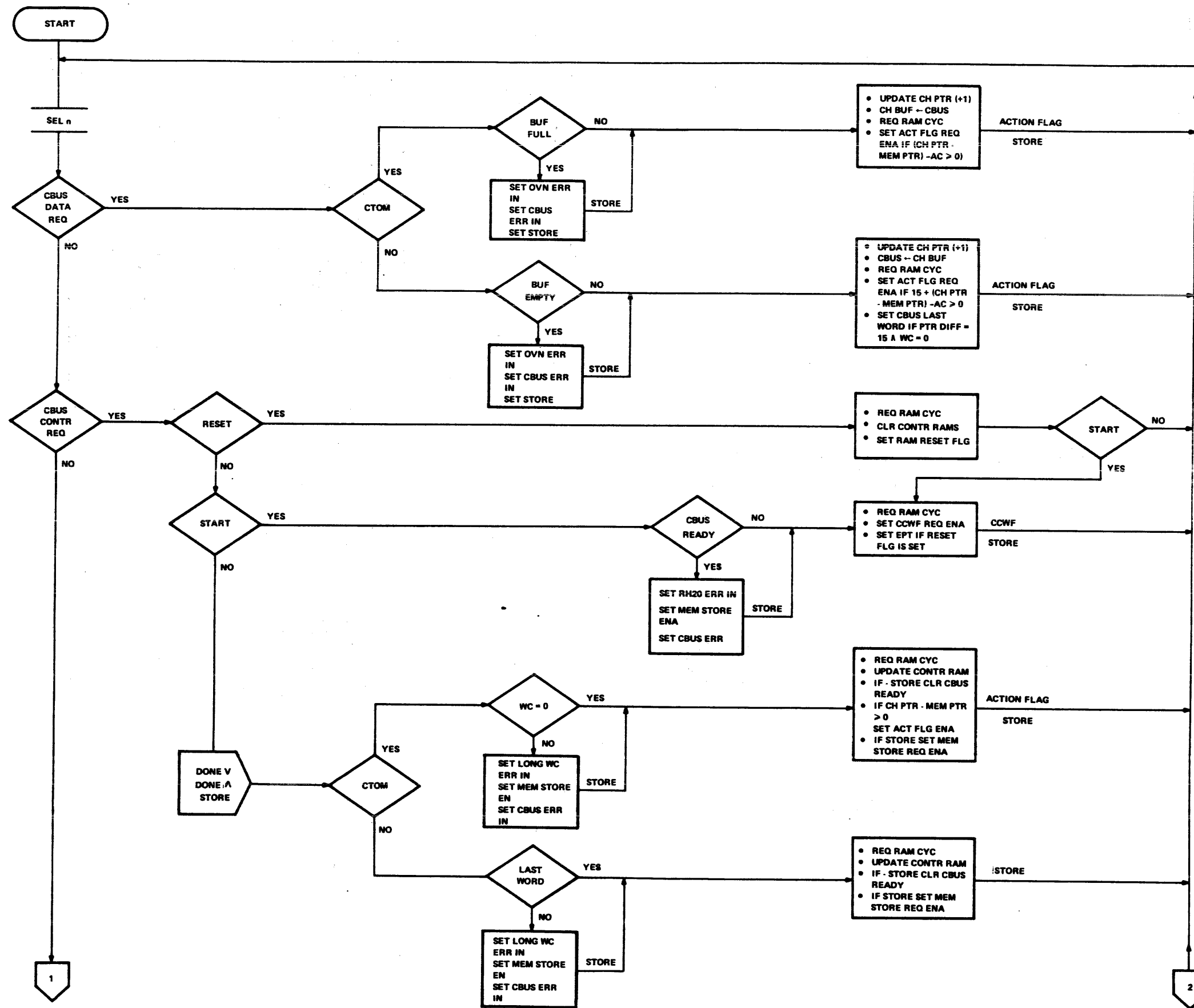
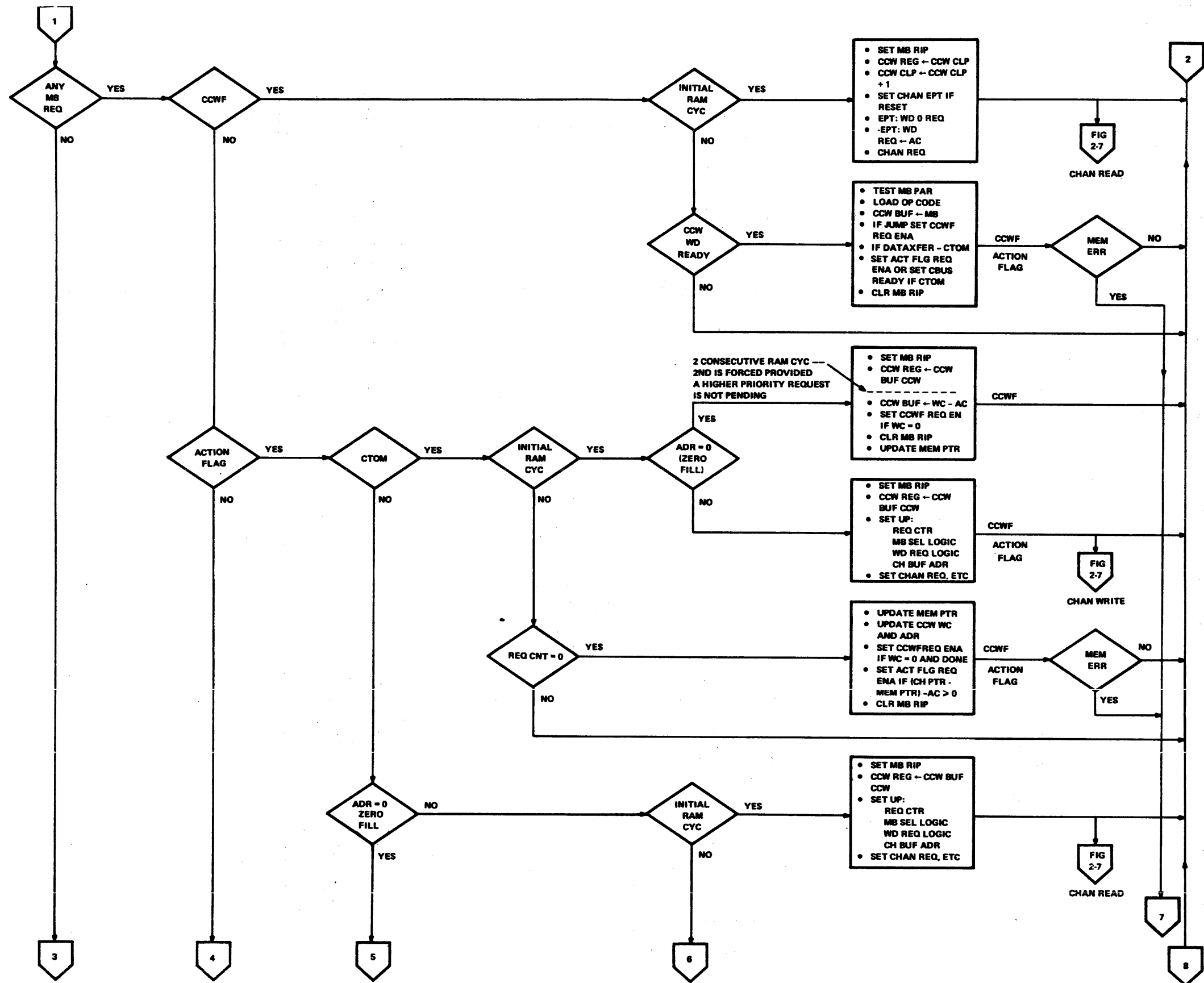
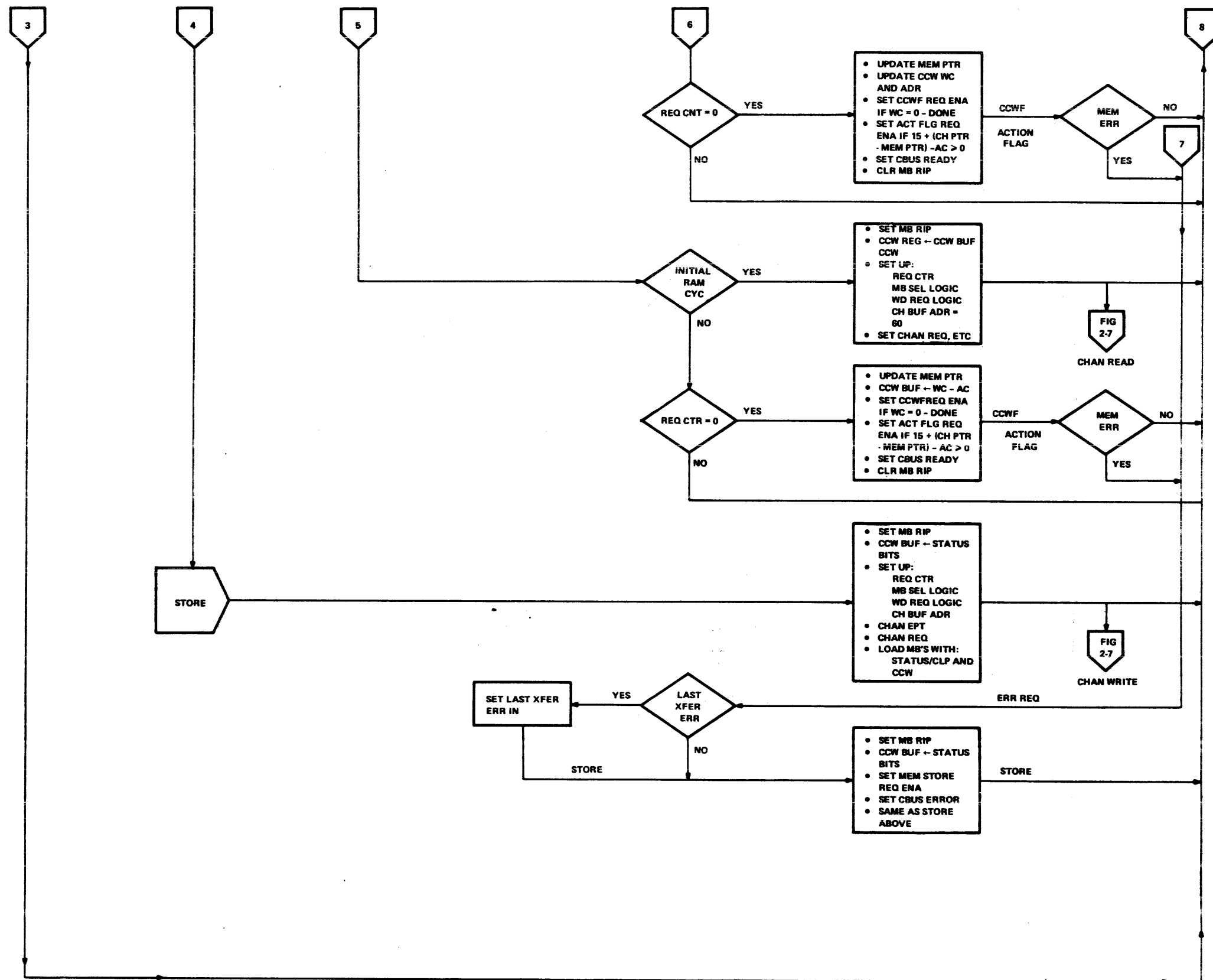


Figure 22 MBox Channel RAM Cycle Control Functional Flow Diagram (Sheet 1 of 3)



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Figure 22 MBox Channel RAM Cycle Control Functional Flow Diagram (Sheet 2 of 3)



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Figure 22 MBox Channel RAM Cycle Control Functional Flow Diagram (Sheet 3 of 3)

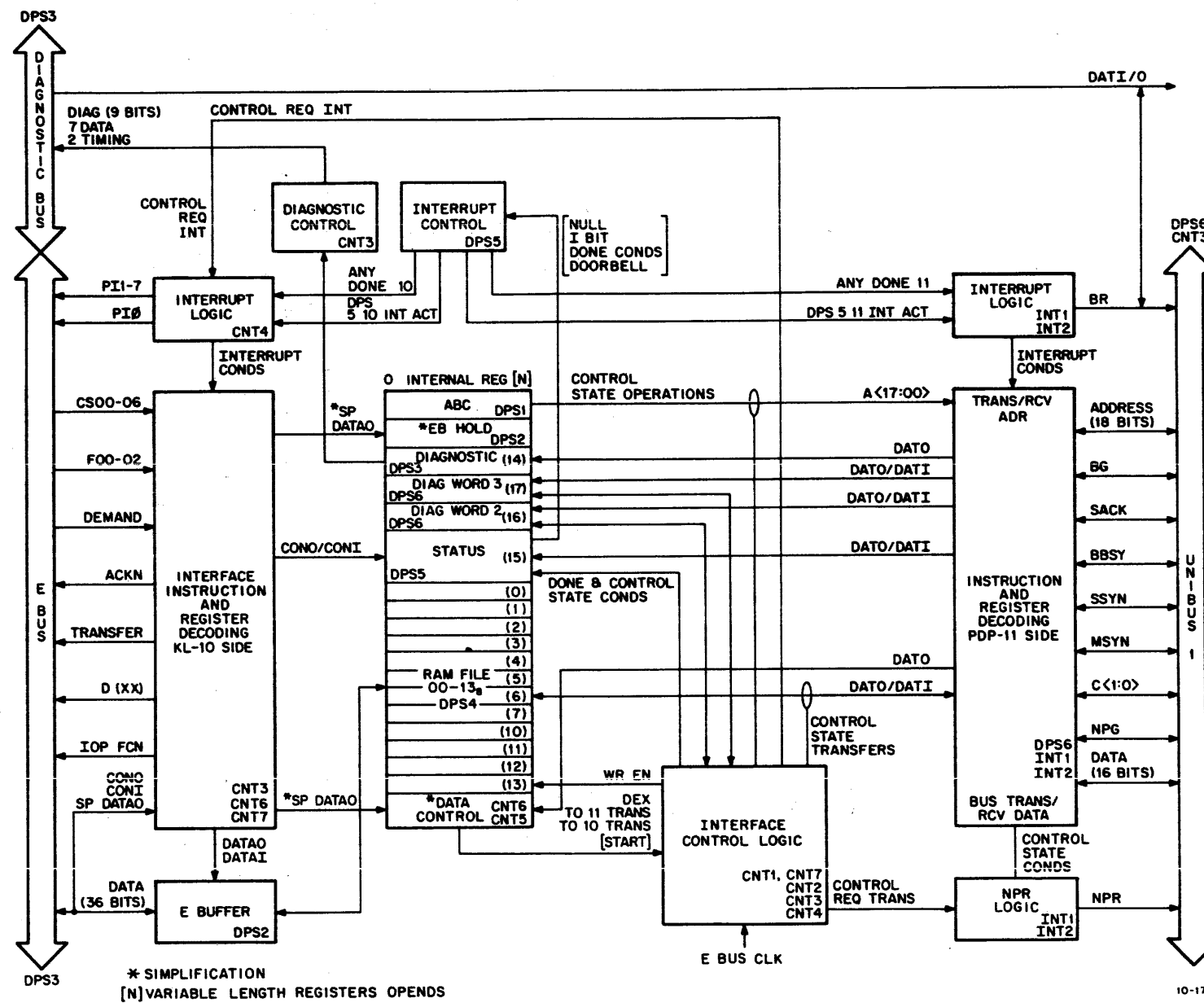
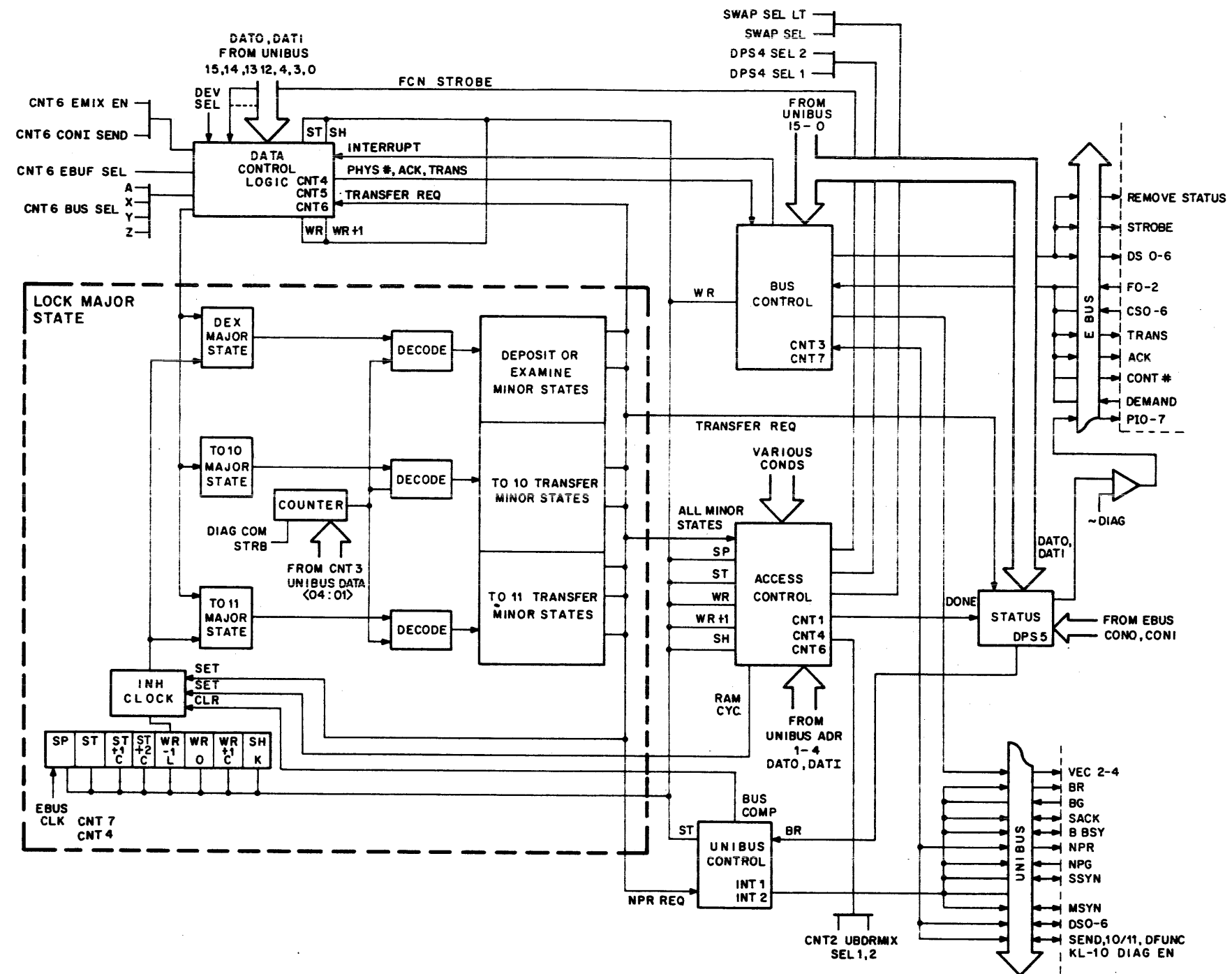


Figure 23 DTE Simplified Functional Block Diagram



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Figure 24 DTE Simplified Control Block Diagram

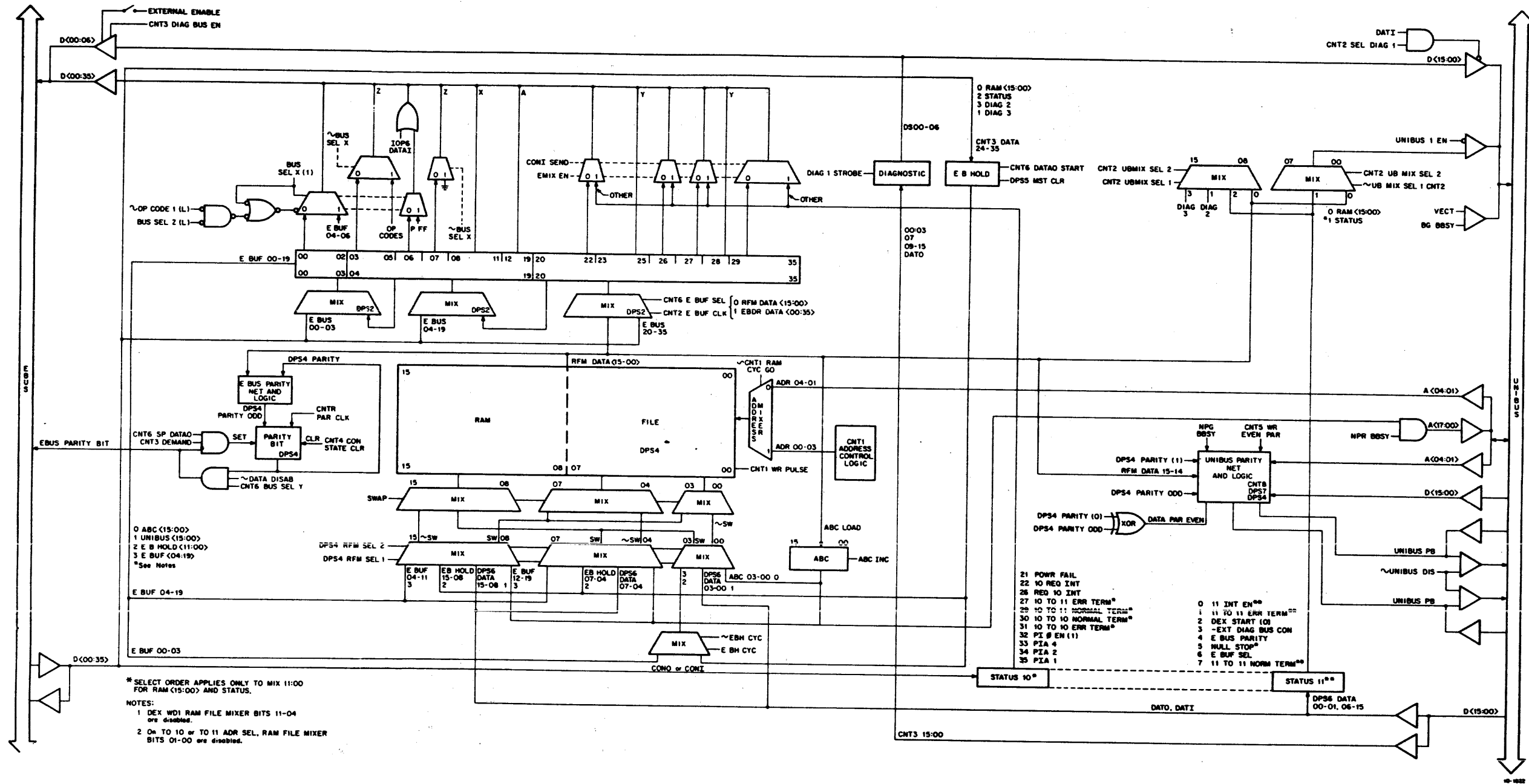


Figure 25 DTE20 Address and Data Paths Block Diagram

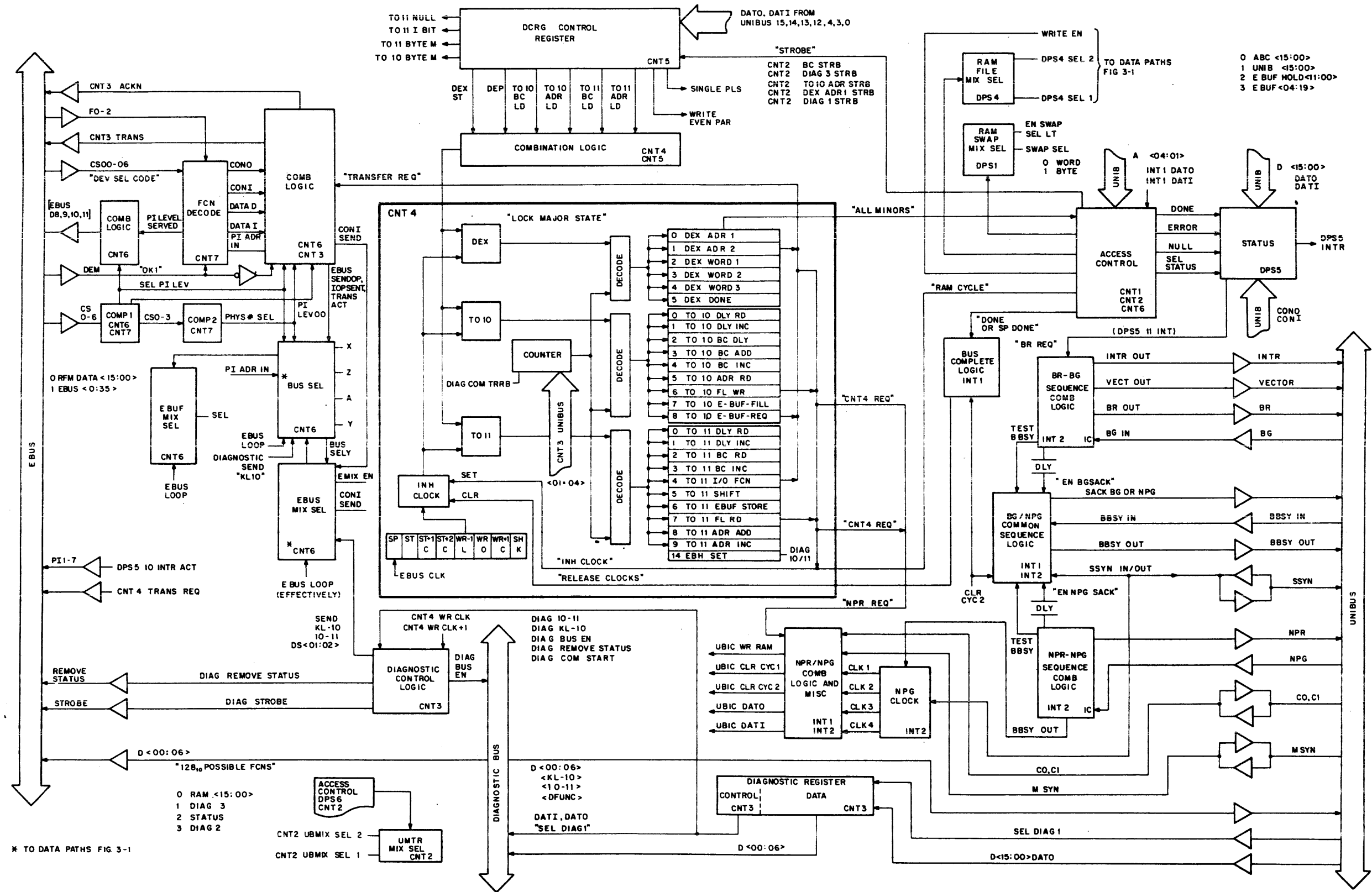
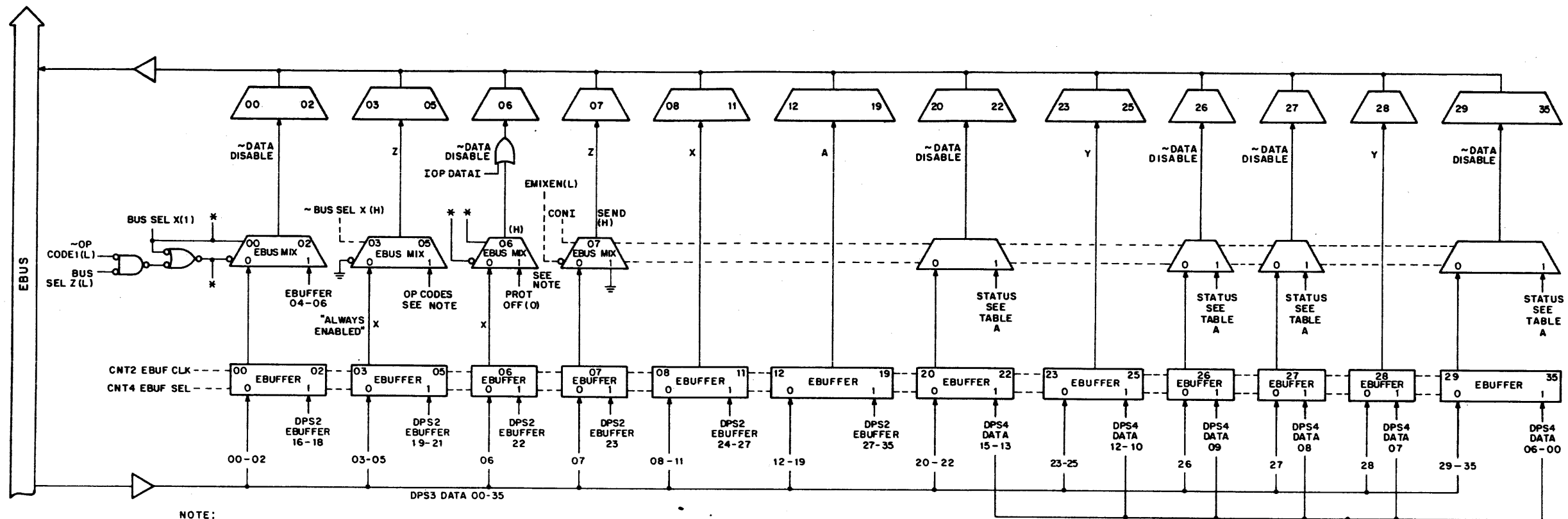


Figure 26 DTE20 Detailed Control Block Diagram



NOTE:

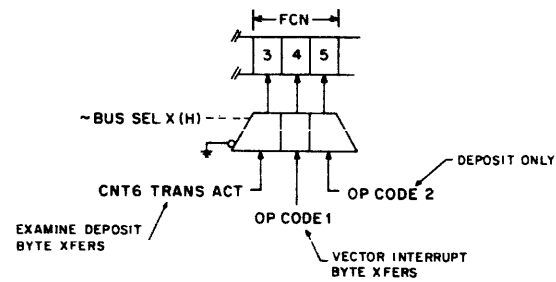


TABLE A	
E BUS MIXER	TYPE OF STATUS
20	~EXT DIAG BUS EN
21	INT1 PWR FAIL
22	DPS5 10 REQ INT
26	DPS5 REQ 10 INT
27	DPS5 10 TO11 ERR TERM
29	DPS5 10 TO11 NORM TERM
30	DPS5 10 TO10 ERR TERM
31	DPS5 10 TO10 NORM TERM
32	DPS3 P10 EN
33	DPS3 PIA 4 (1)
34	DPS3 PIA 2 (1)
35	DPS3 PIA 1 (1)

BUS SELECTS	WAYS OF GETTING THE SELECT
Z	1.) CNT6 EBUS SEND OP 2.) BUS SEL X
X	1.) CNT4 EBUS LOOP 2.) CNT6 DIAG SEND 3.) CNT6 IOP SENT (1) ^ [CNT7 DATA1 ^ CNT4 DEX (1)]
Y	1.) BUS SEL X 2.) BUS SEL A 3.) CNT6 TO10 DATA CYC = CNT4 TO10 TRANS (1) ^ CNT6 IOP SENT
Z	1.) ~CNT6 OP CODE 2.) BUS SEL X
DATA DISABLE	1.) ~EXT DIAG BUS CON EBUS DATA DISABLE

CNT6 E BUFFER SELECT	
0	E BUFFER 00-19 ← E BUFFER 16-35 ← E BUFFER 20-35 ← RAM DATA 15-00
1	E BUFFER 00-35 ← EBUS 00-35

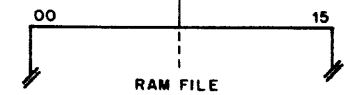


Figure 27 DTE20 EBus and EBuffer Mixers

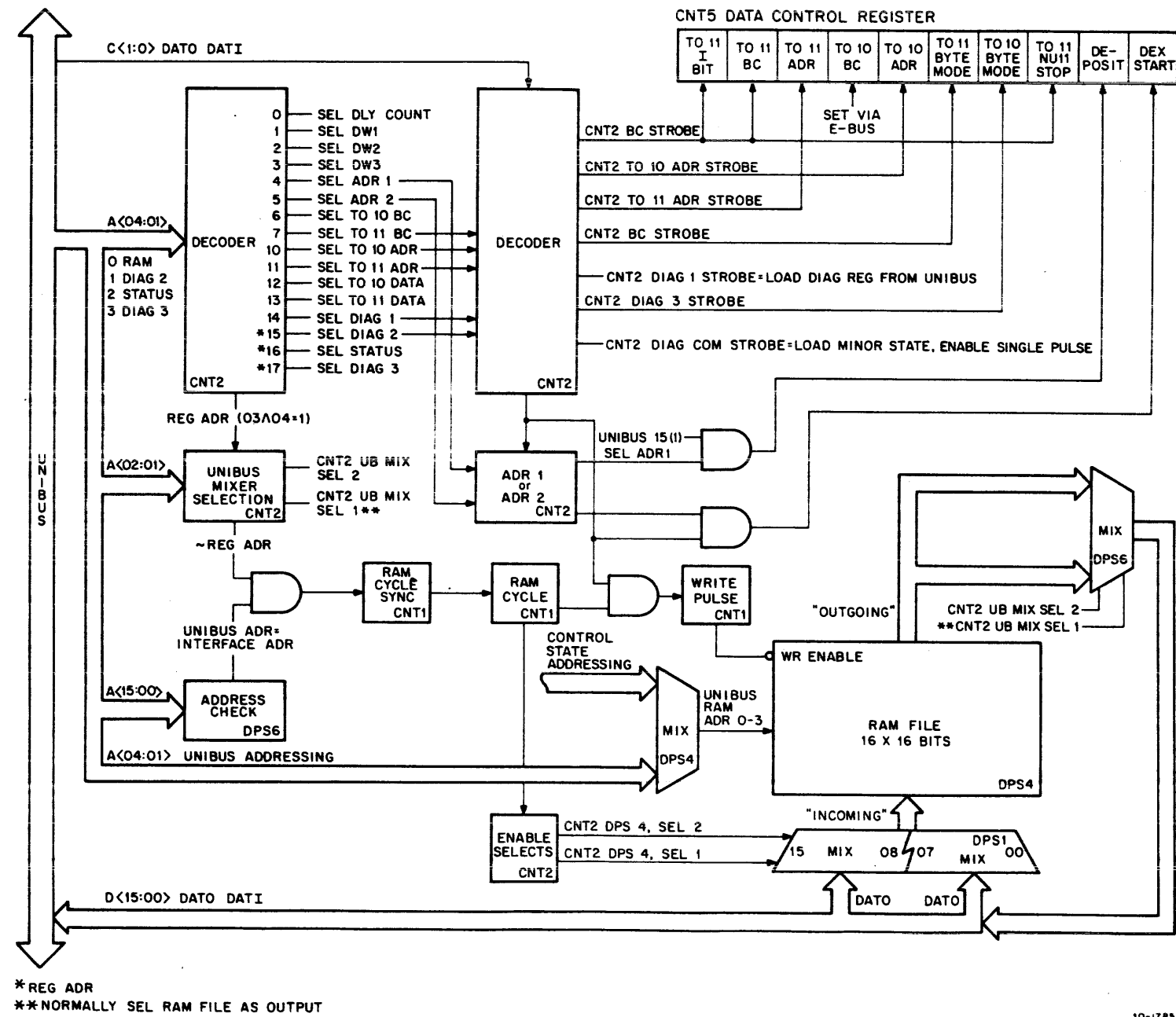
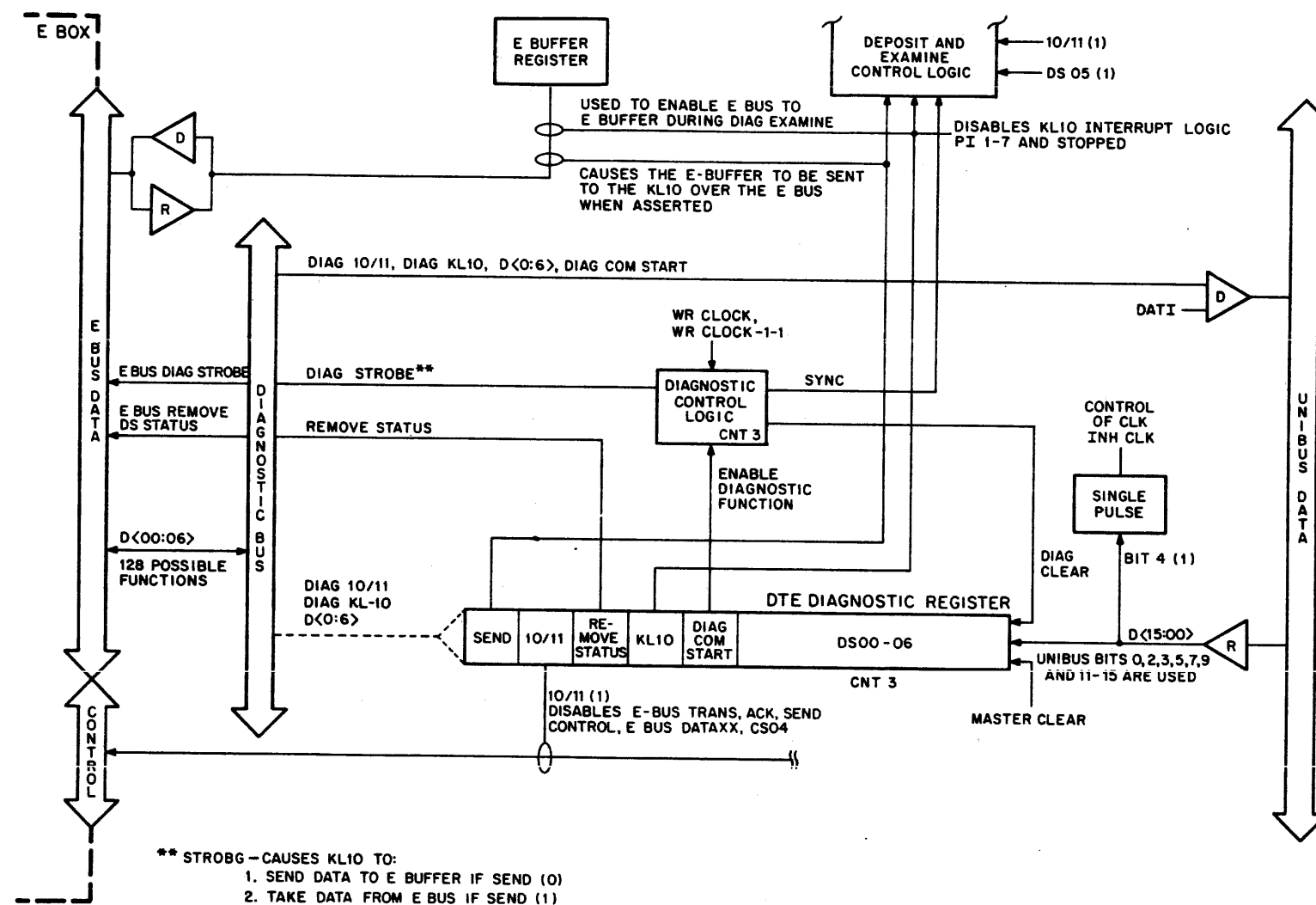


Figure 28 DTE20 Interface Address and Access Control Simplified



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Figure 29 DTE20 Simplified Diagnostic Functional Diagram

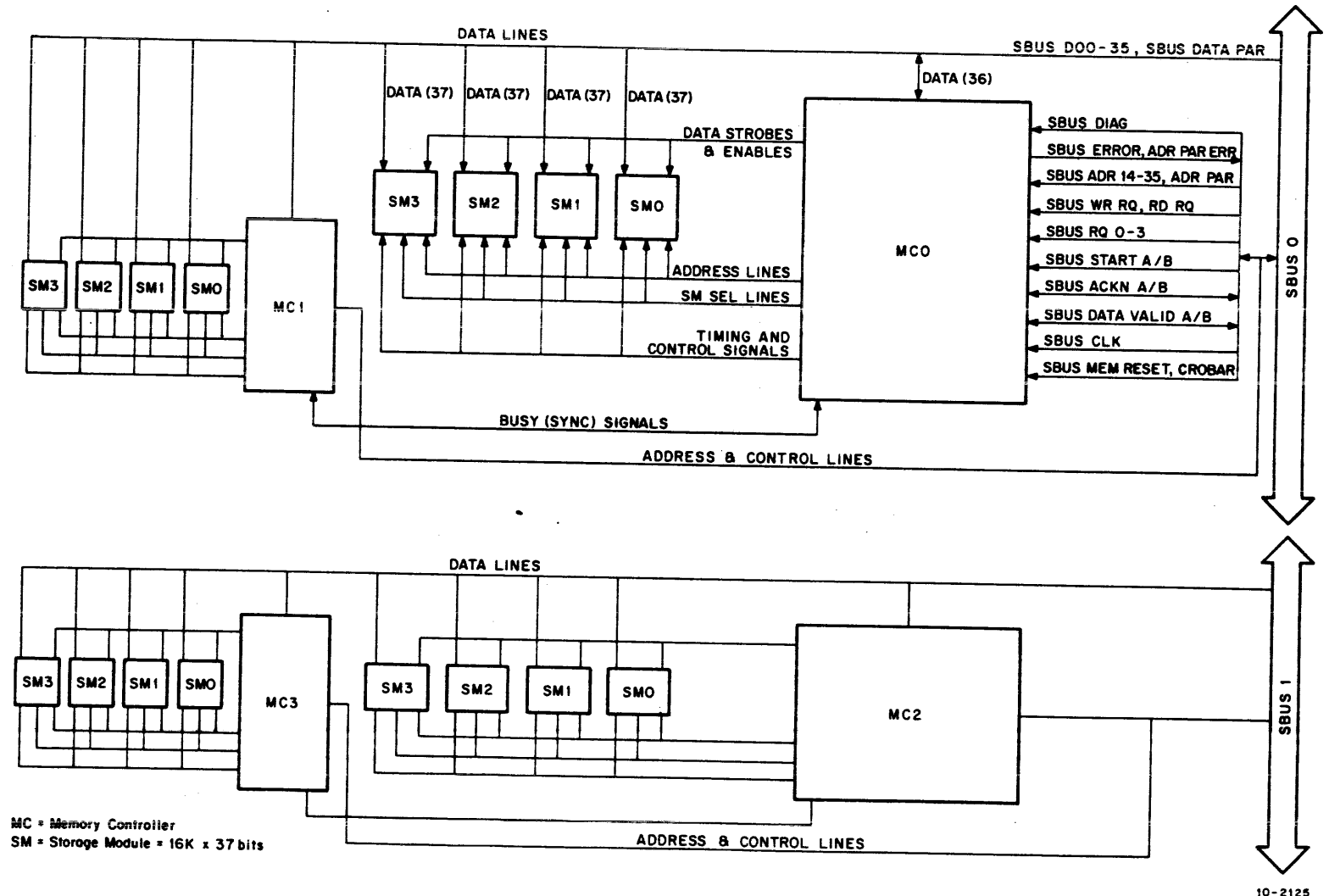
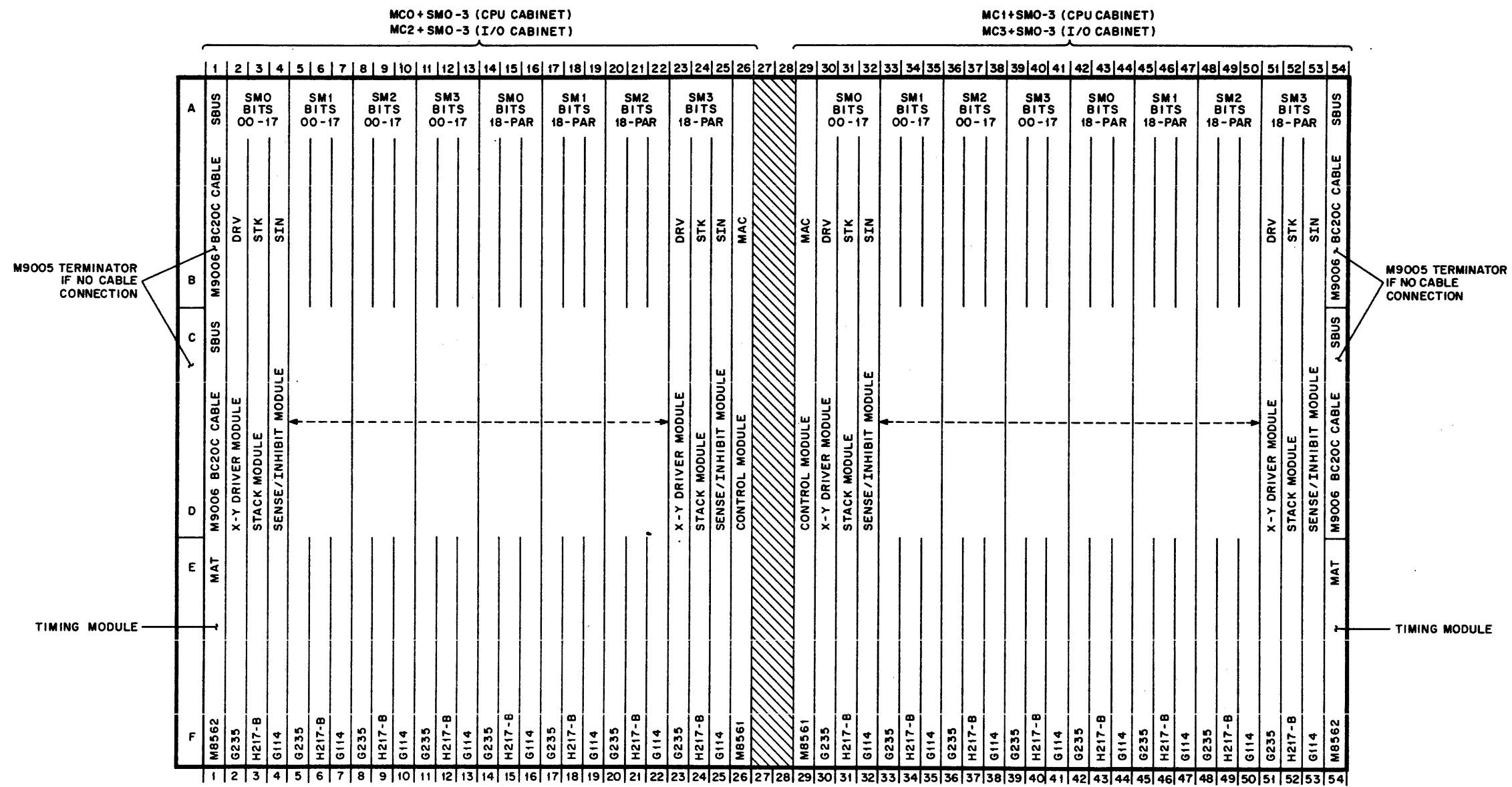


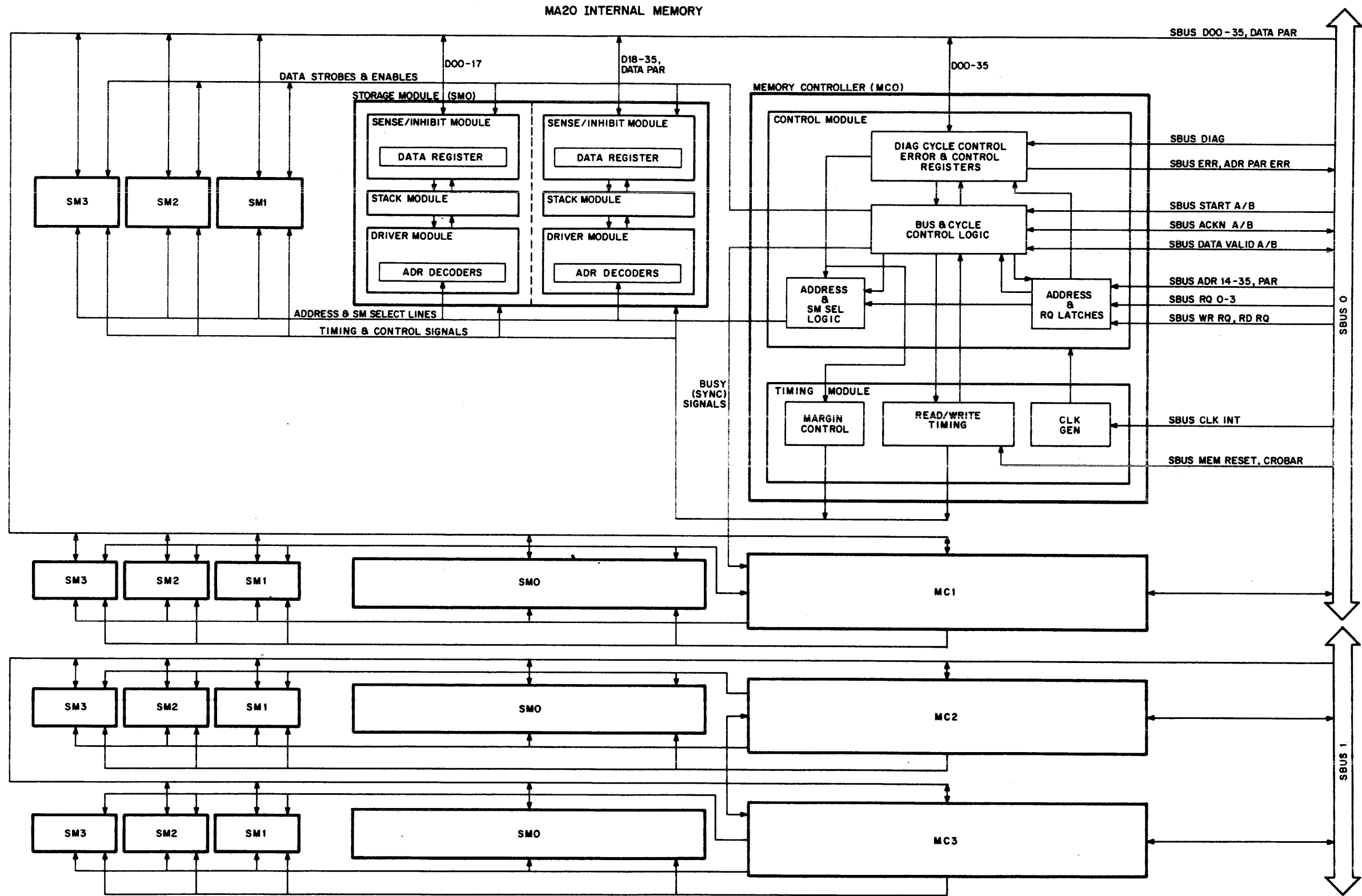
Figure 30 MA20 Internal Memory



NOTES:
 1. Viewed from wire side
 2. MU same for CPU and I/O cabinets

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Figure 31 MA20 Module Utilization



10-2127

Figure 32 MA20 Functional Block Diagram

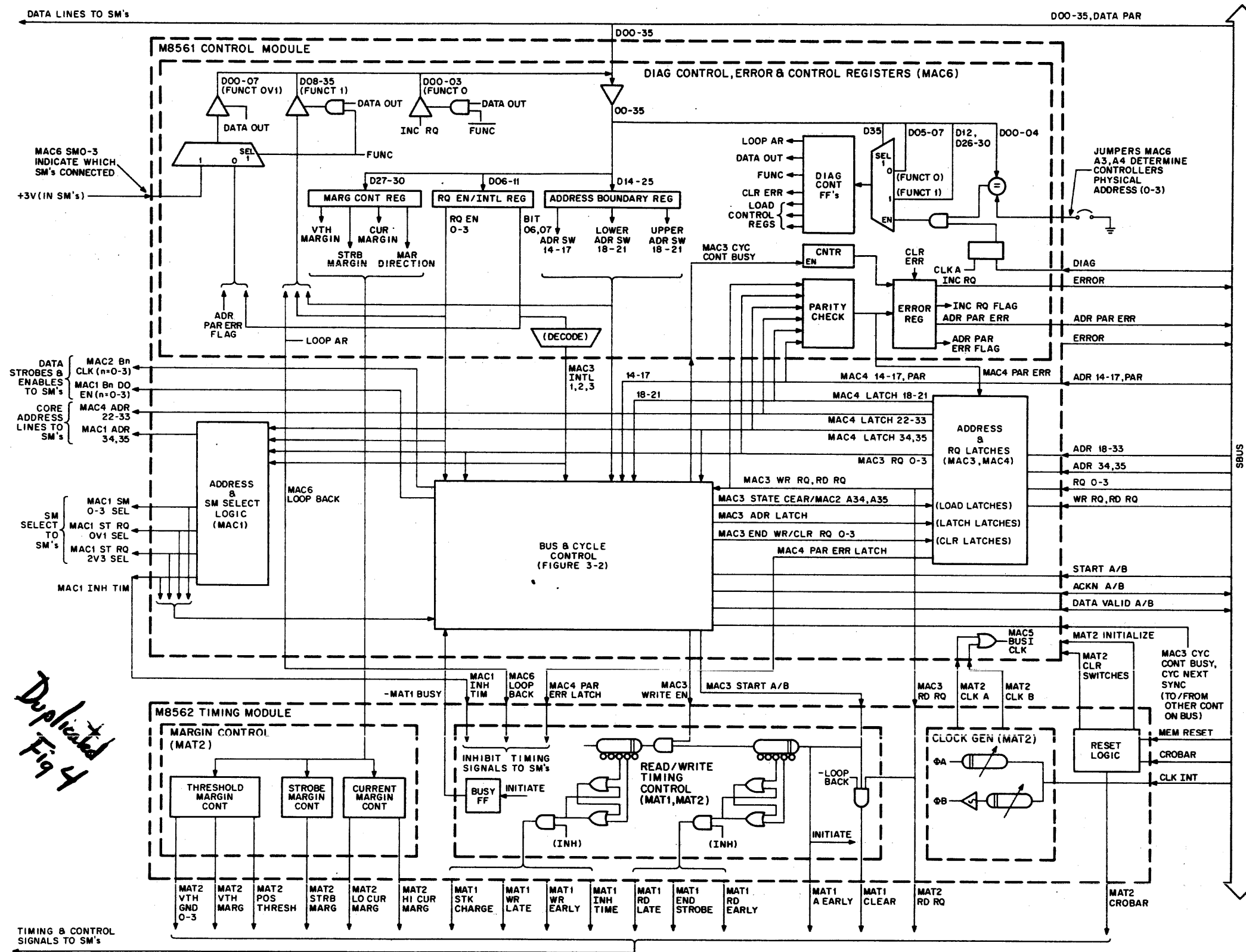
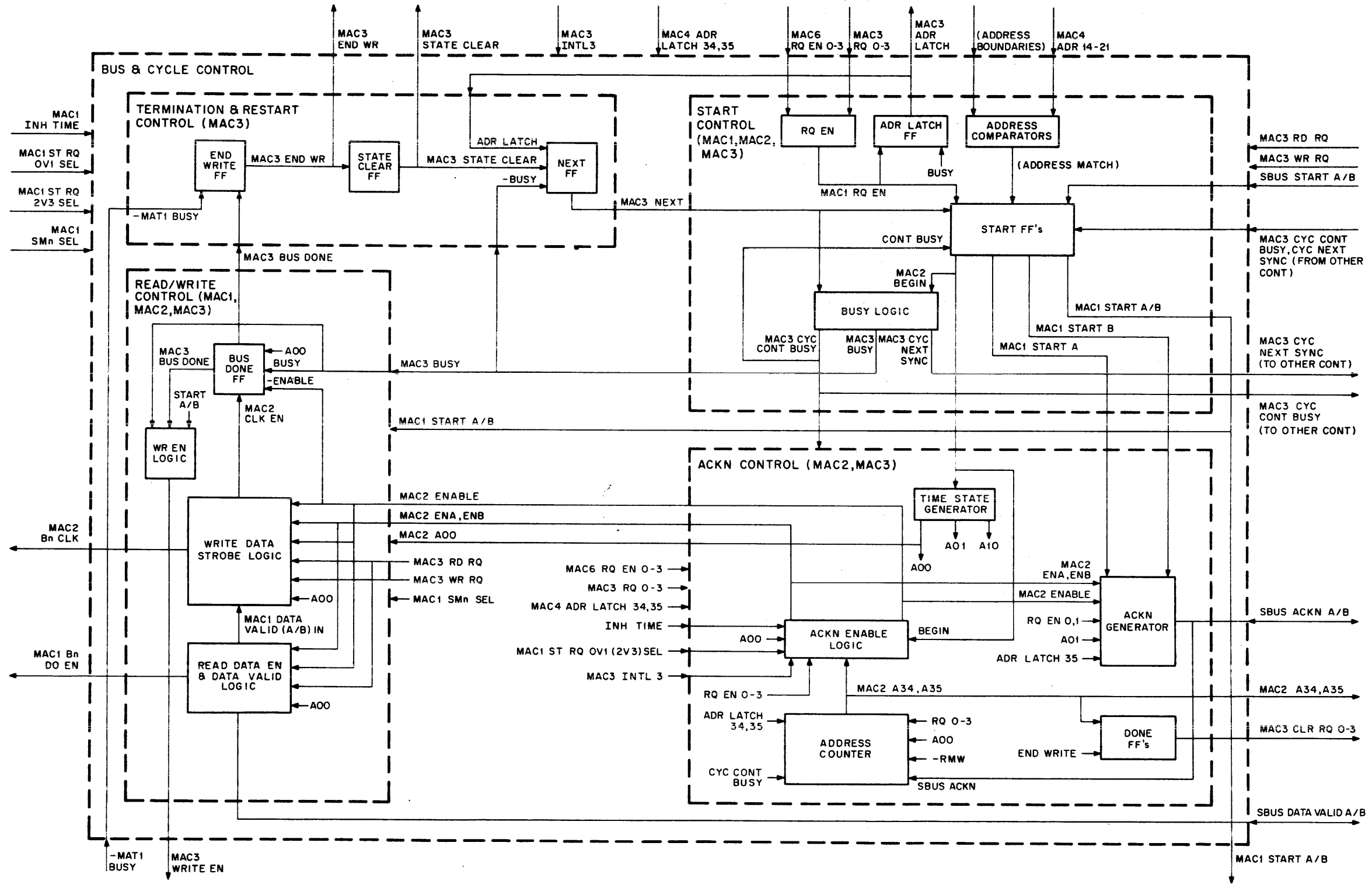
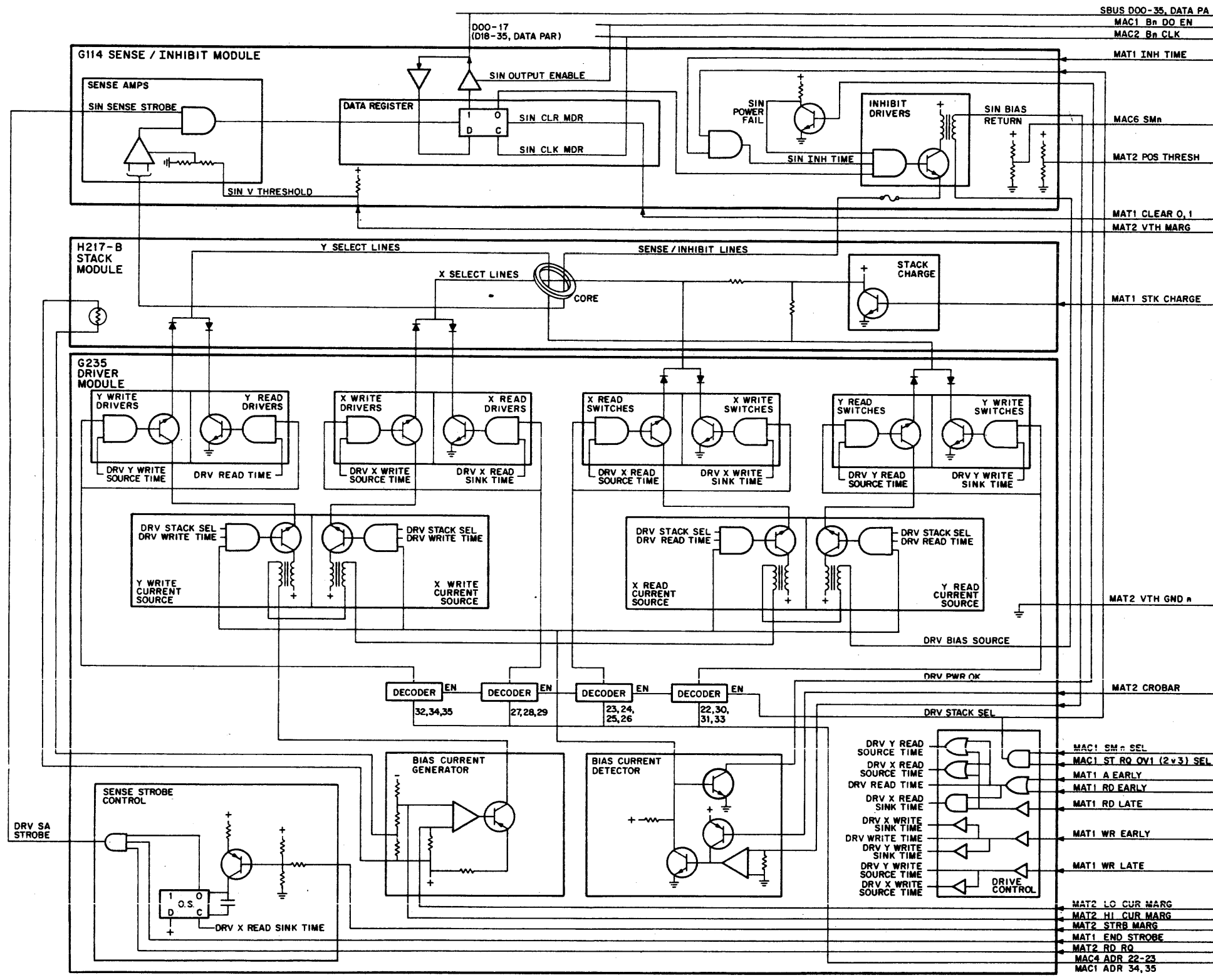


Figure 33 MA20 Controller Detailed Block Diagram



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Figure 34 MA20 Bus and Cycle Control



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Figure 35 MA20 Storage Module Detailed Block Diagram

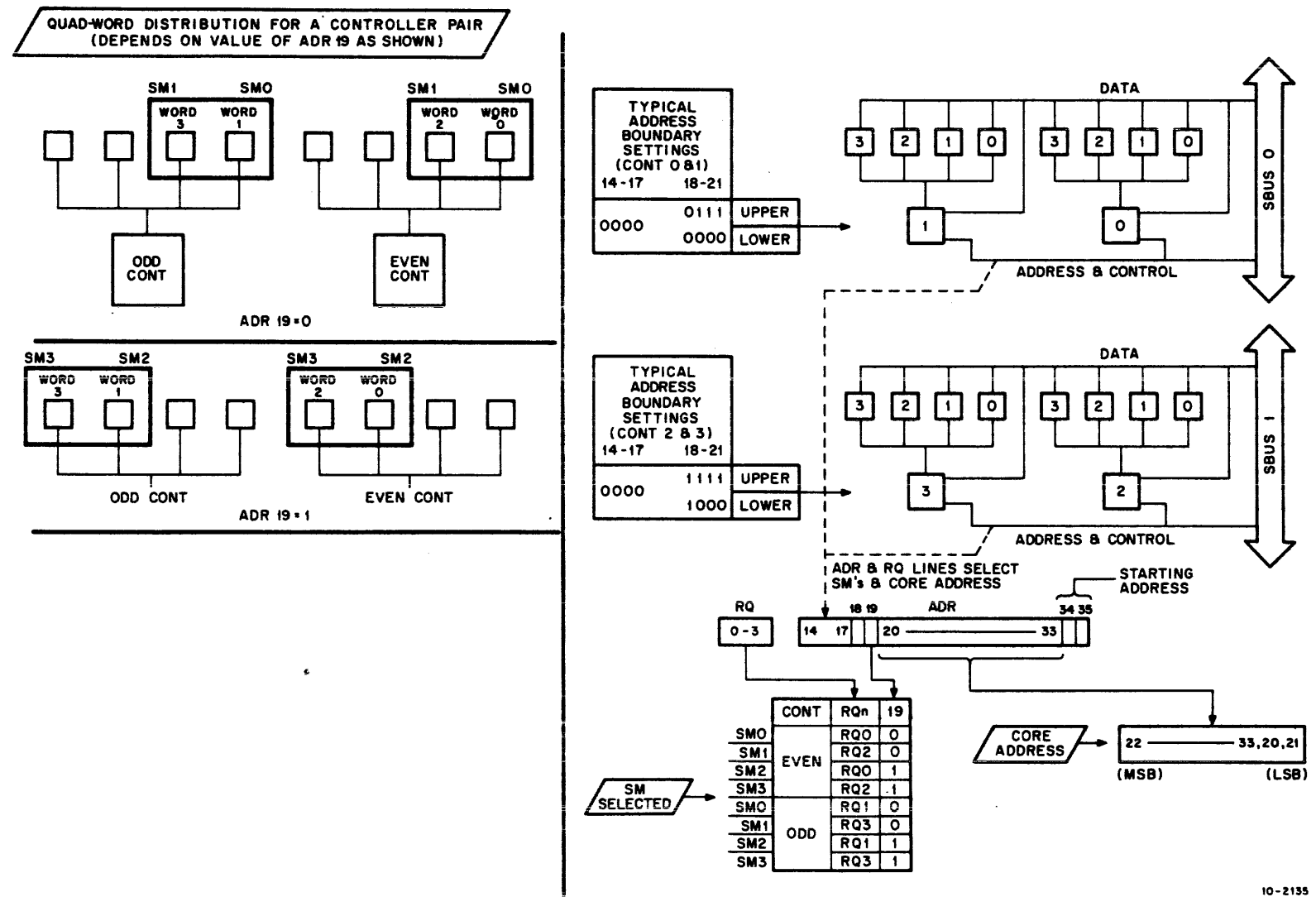


Figure 36 MA20 Memory Selection 4-Way Interleave Mode

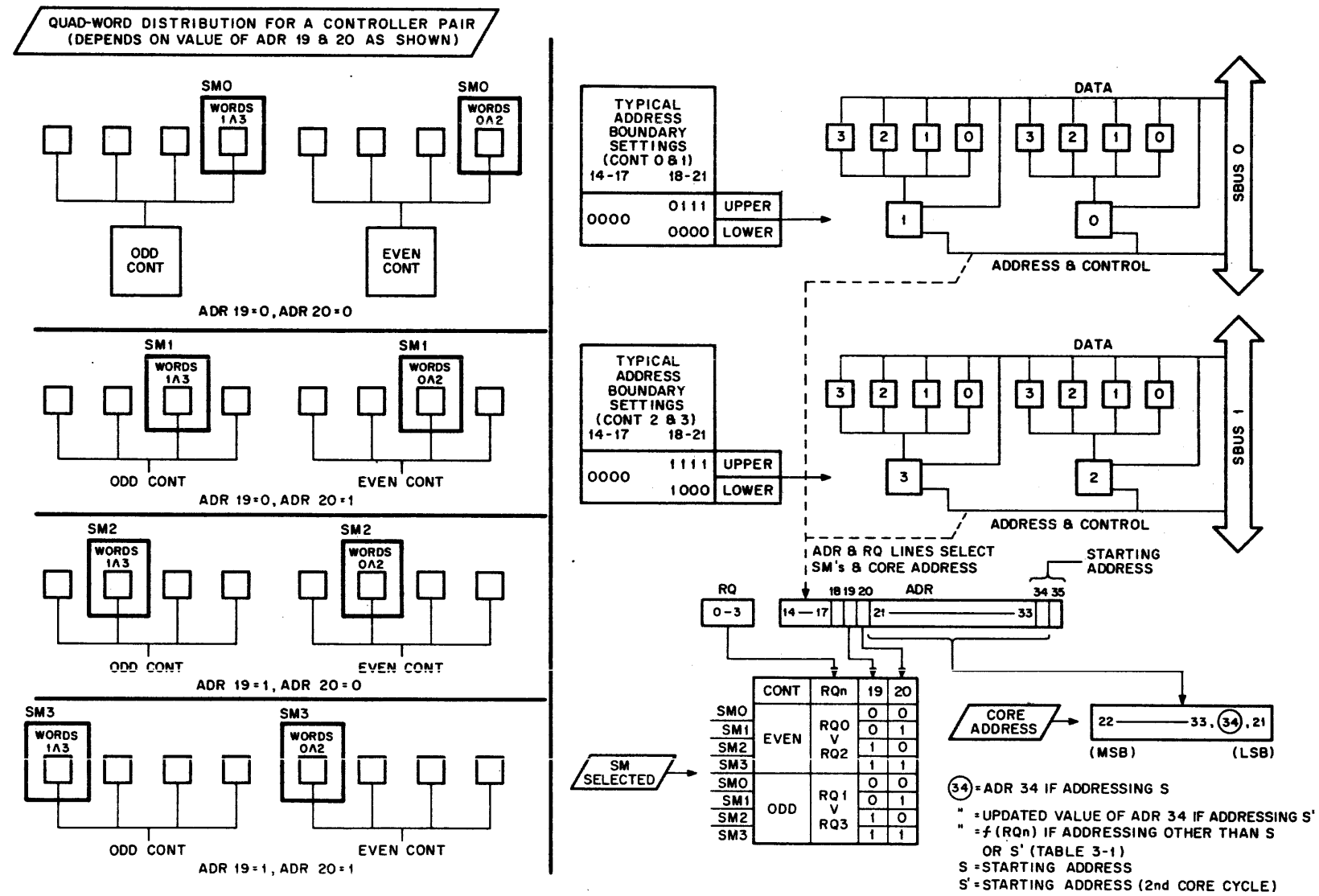


Figure 37 MA20 Memory Selection 2-Way Interleave Mode

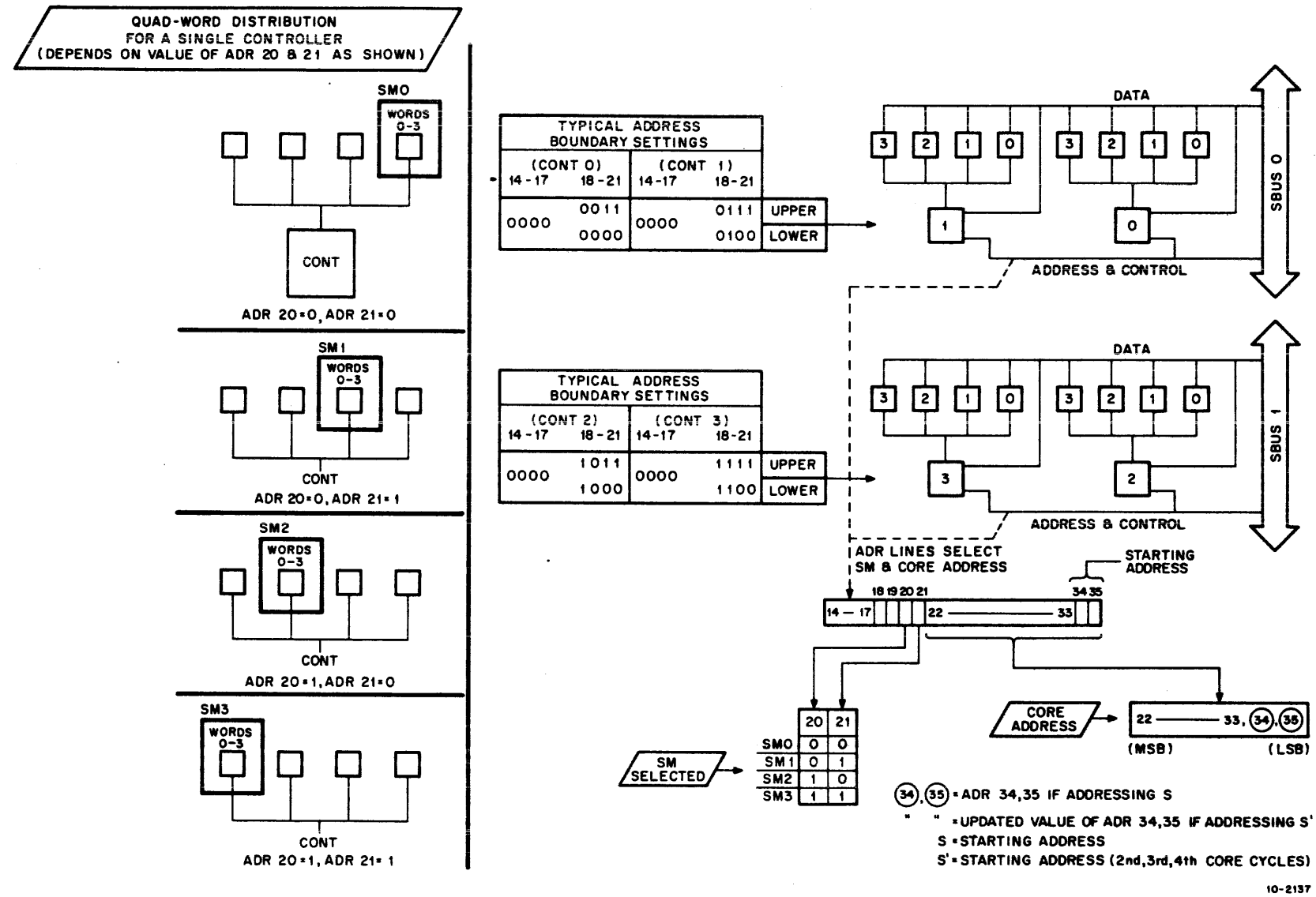
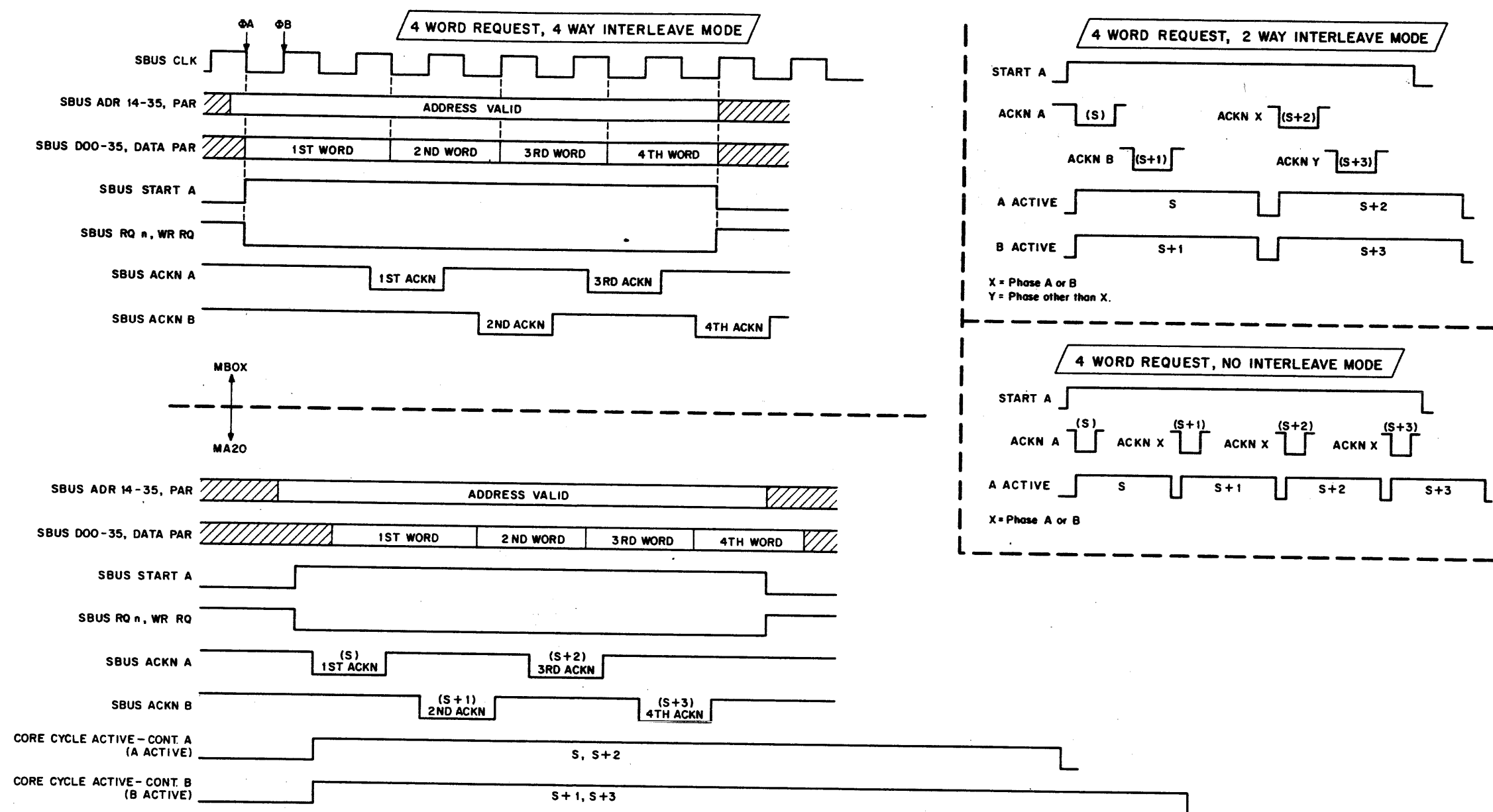


Figure 38 MA20 Memory Selection Non-Interleave Mode



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Figure 39 MA20 SBus Write Timing Diagram

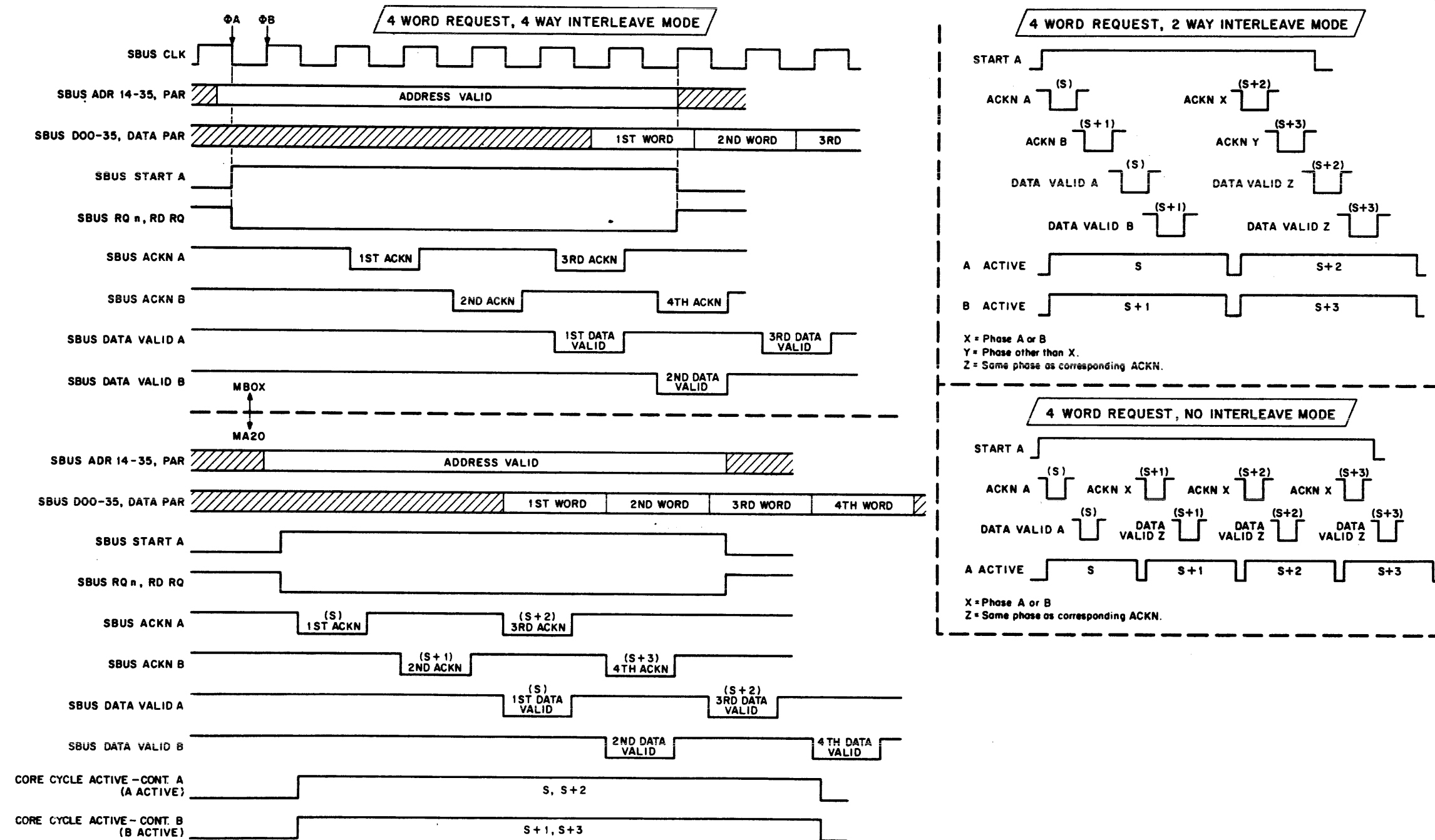
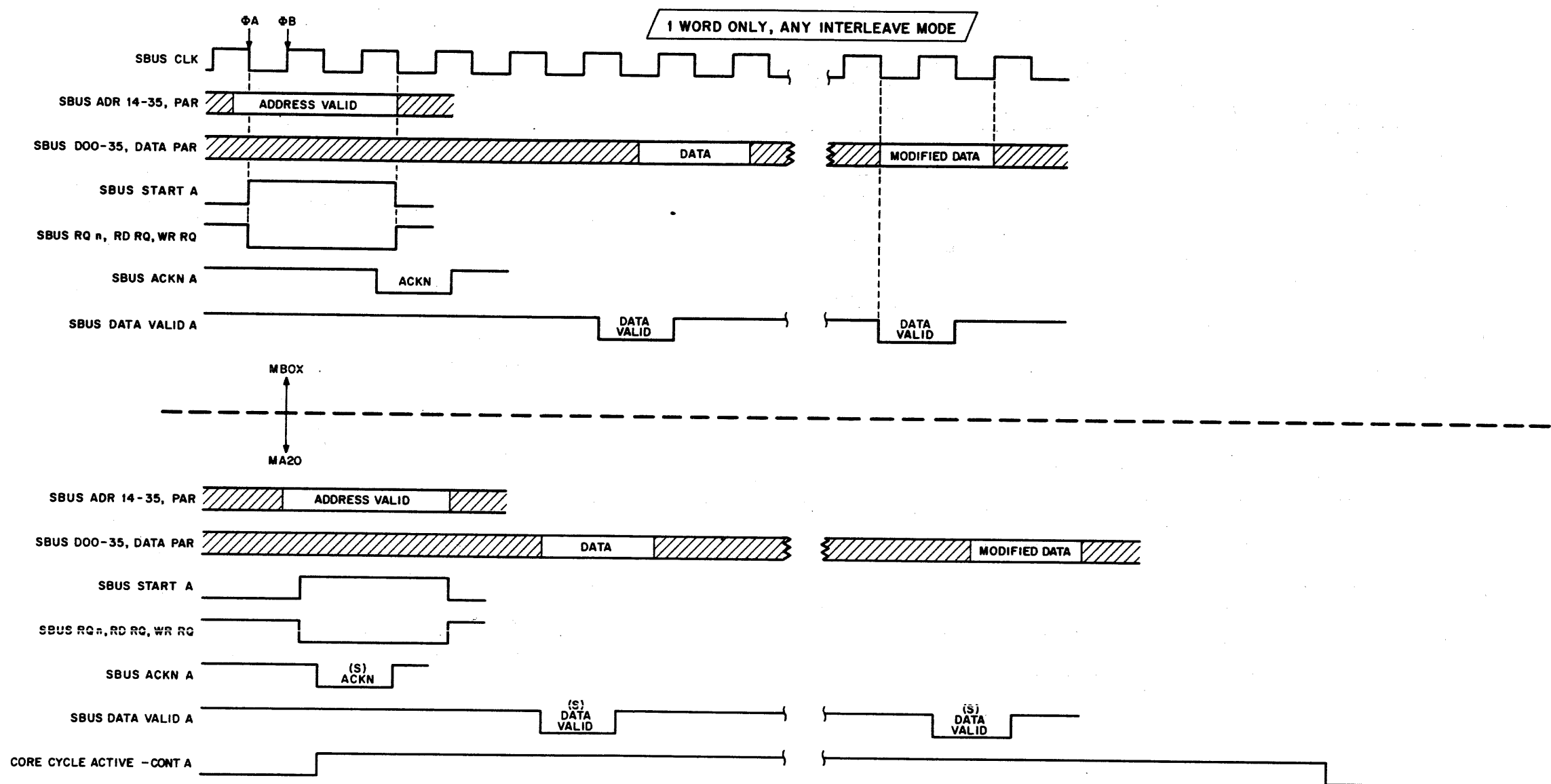


Figure 40 MA20 SBus Read Timing Diagram



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Figure 41 MA20 SBus RMW Timing Diagram

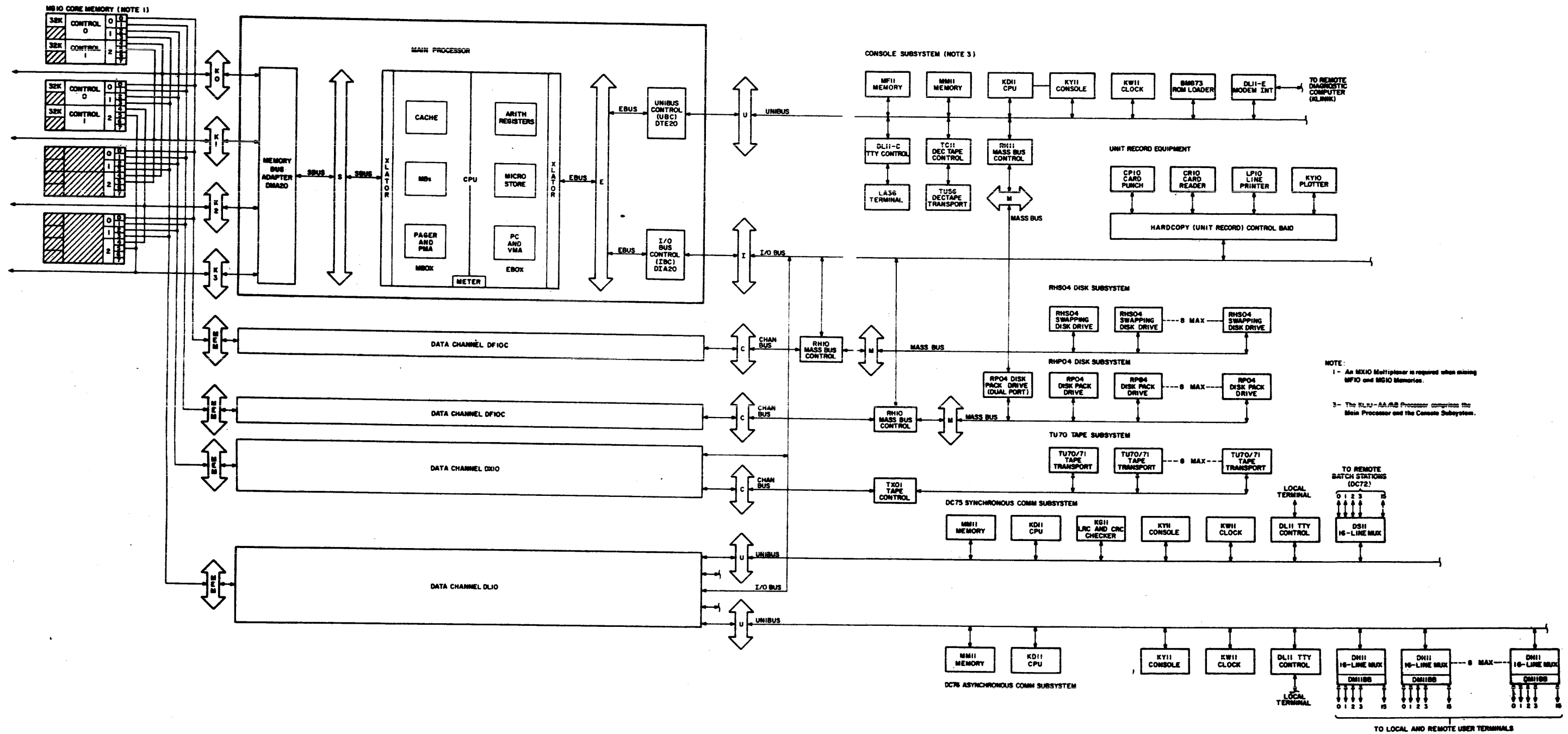
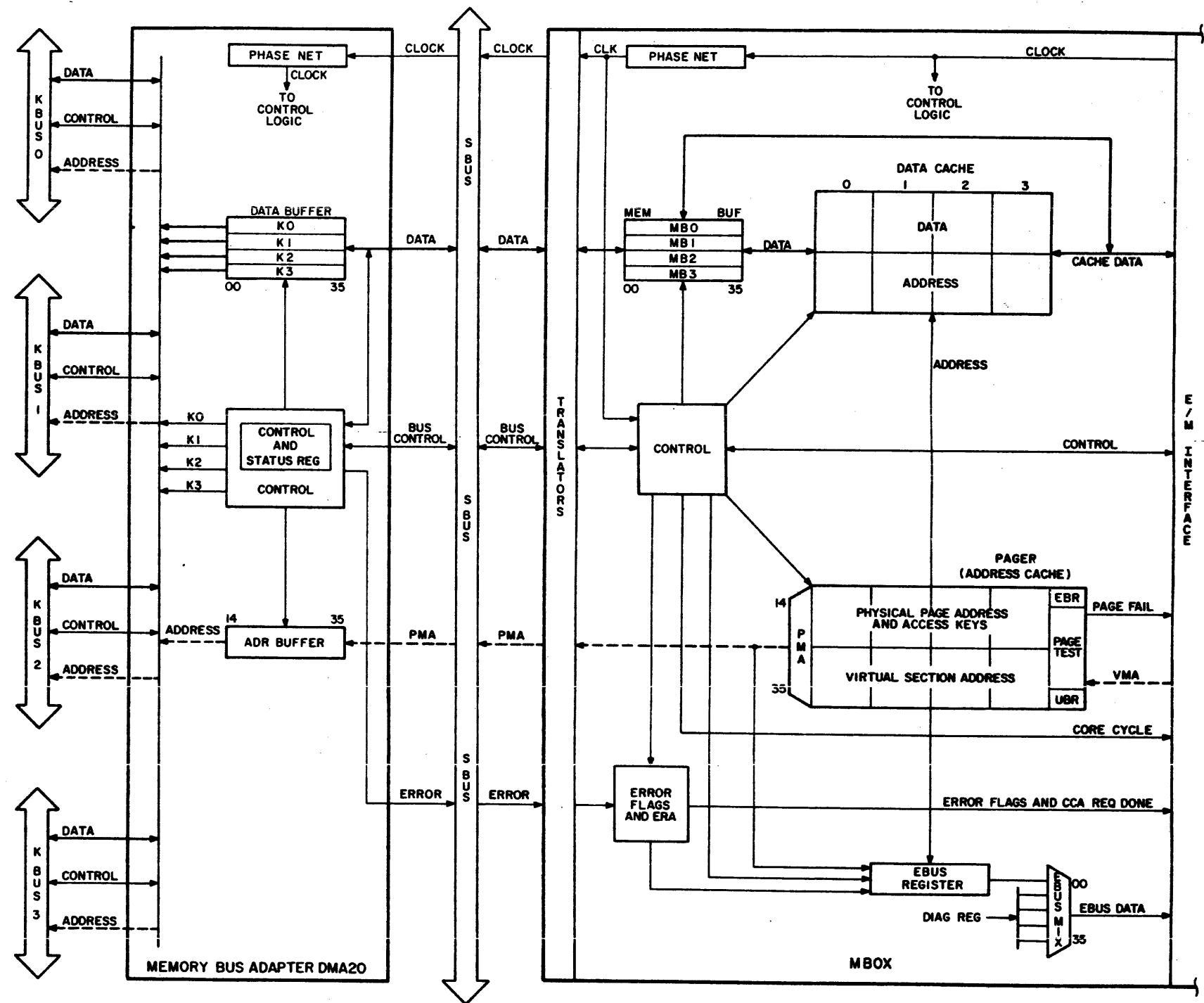


Figure 42 DECsystem-1080 Block Diagram (Typical)



10-1920-A

Figure 43 Main Processor Subsystem Block Diagram (Sheet 1 of 2)

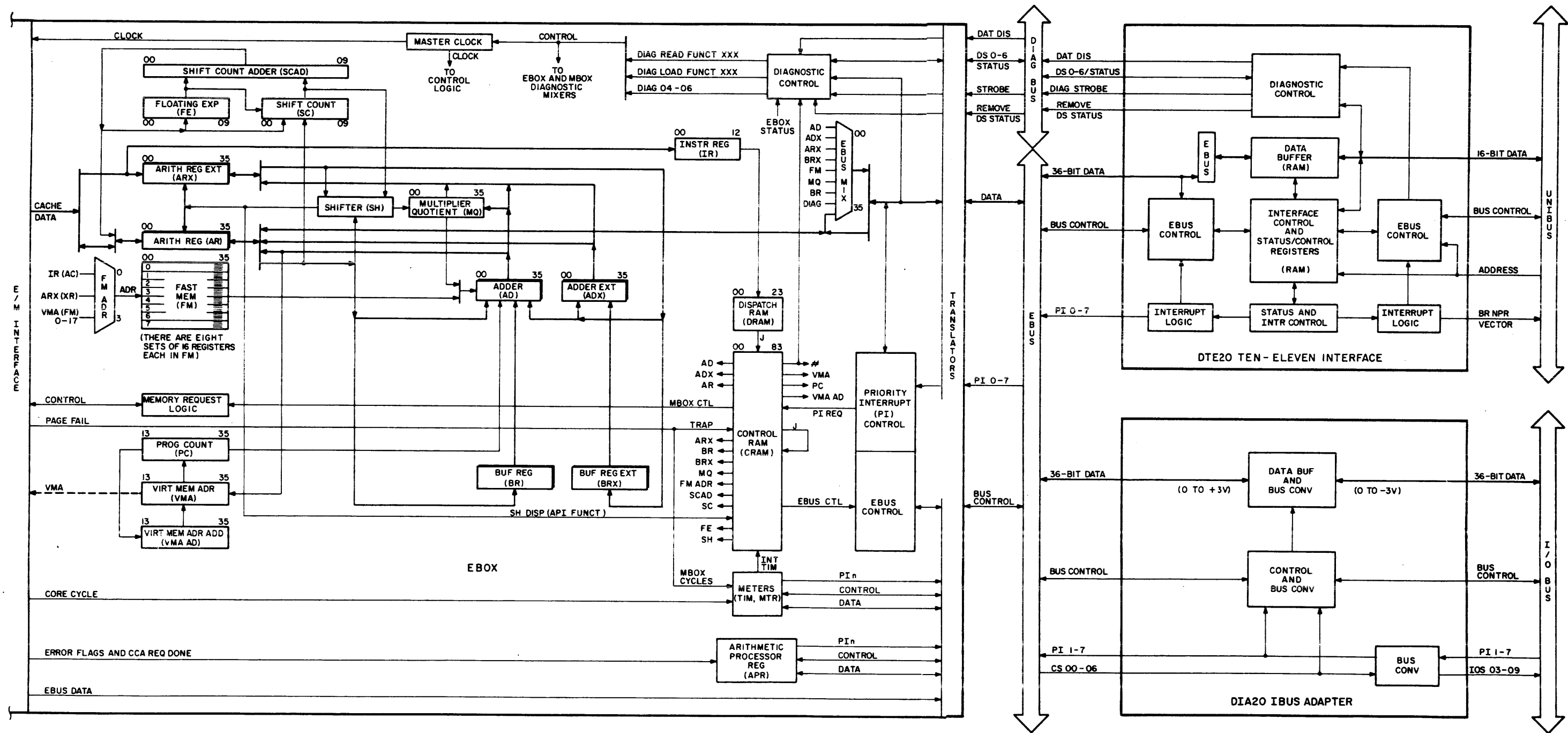


Figure 43 Main Processor Subsystem Block Diagram (Sheet 2 of 2)

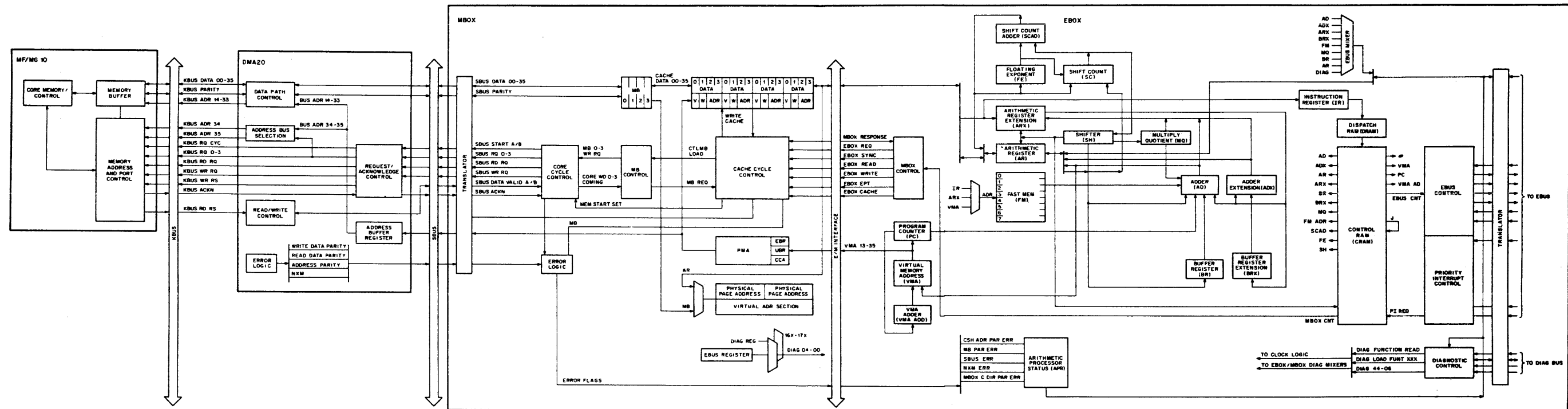
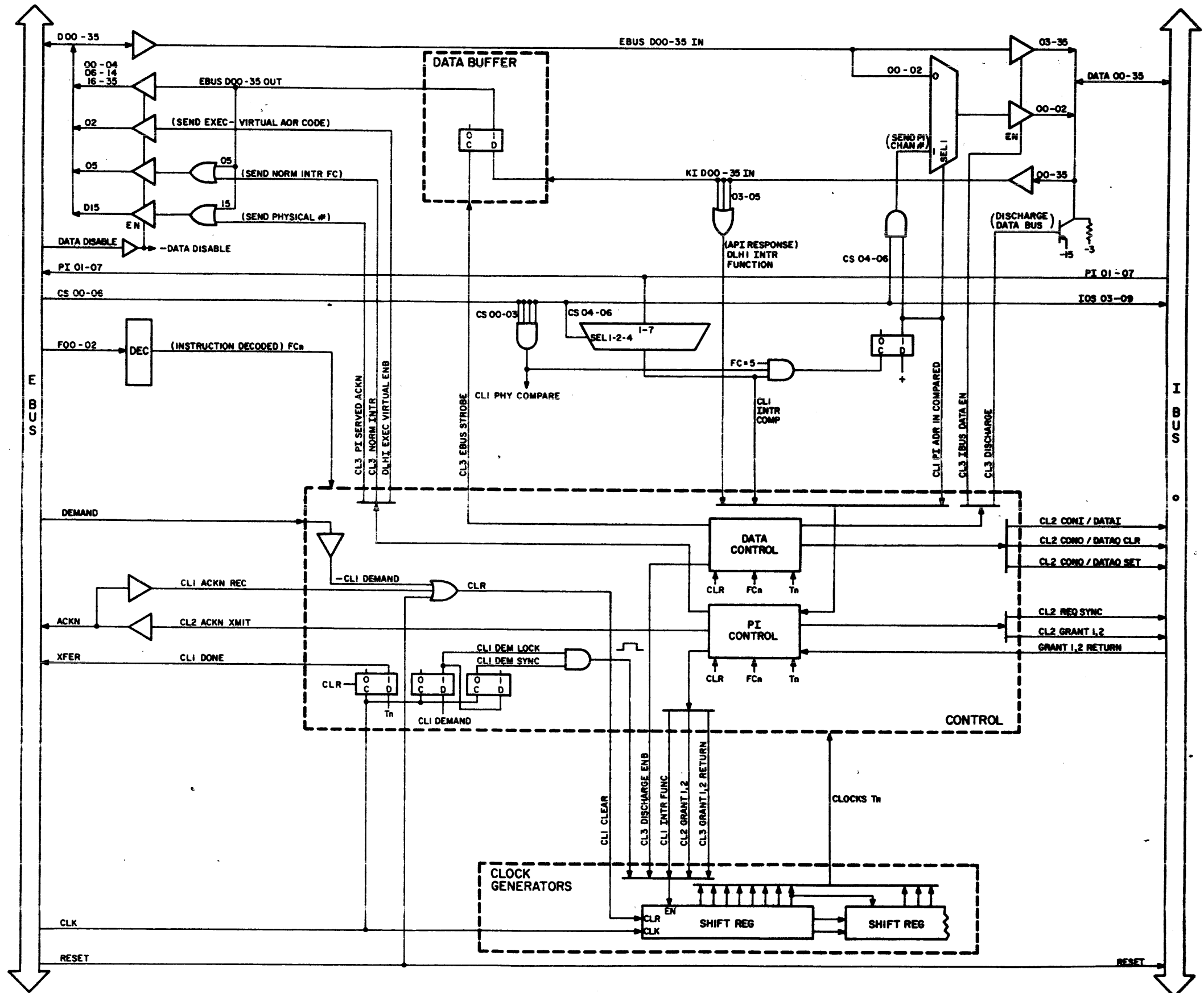


Figure 44 Detail Channel Interface Block Diagram



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Figure 45 DIA20 Detailed Block Diagram

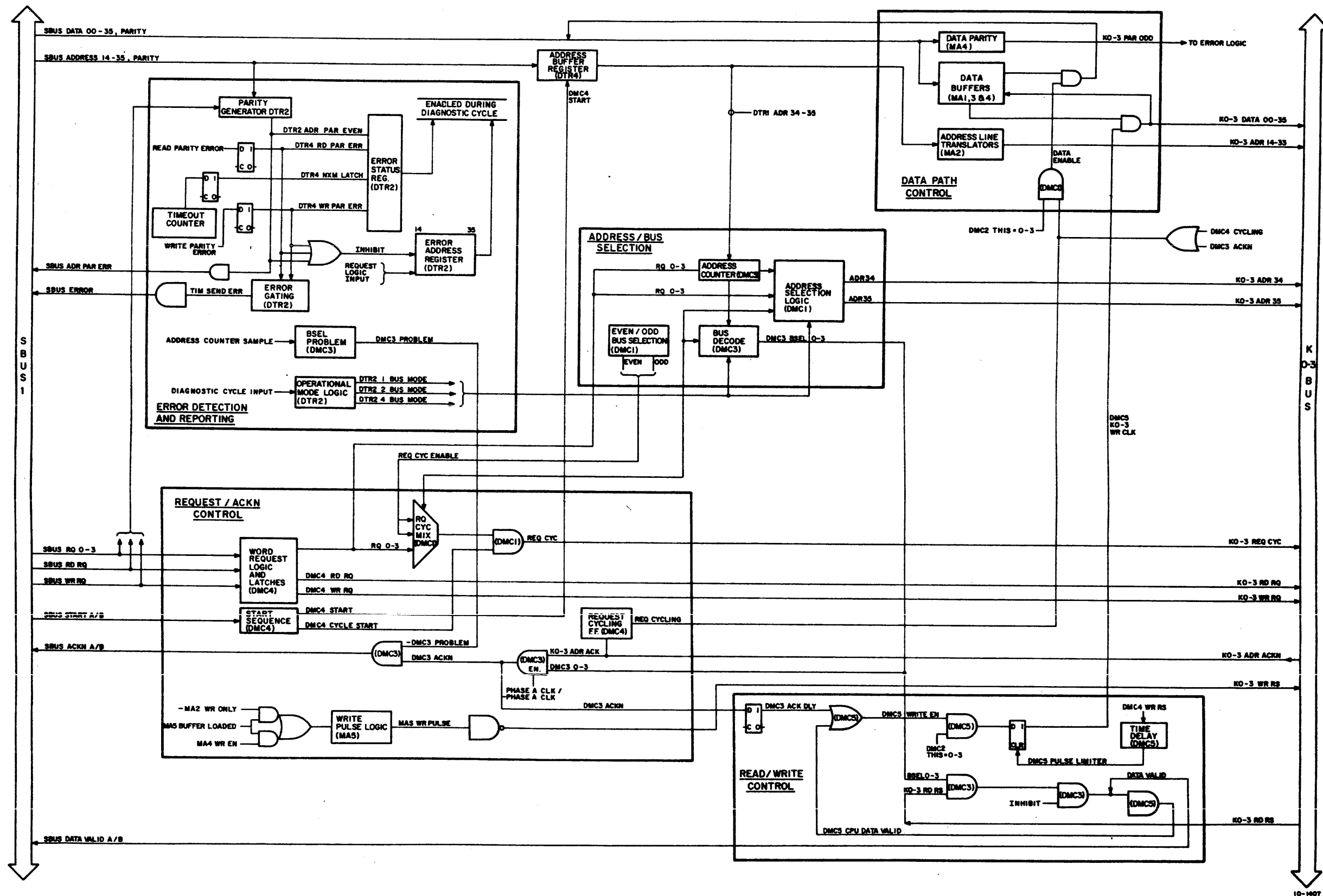


Figure 46 DMA20 Functional Block Diagram

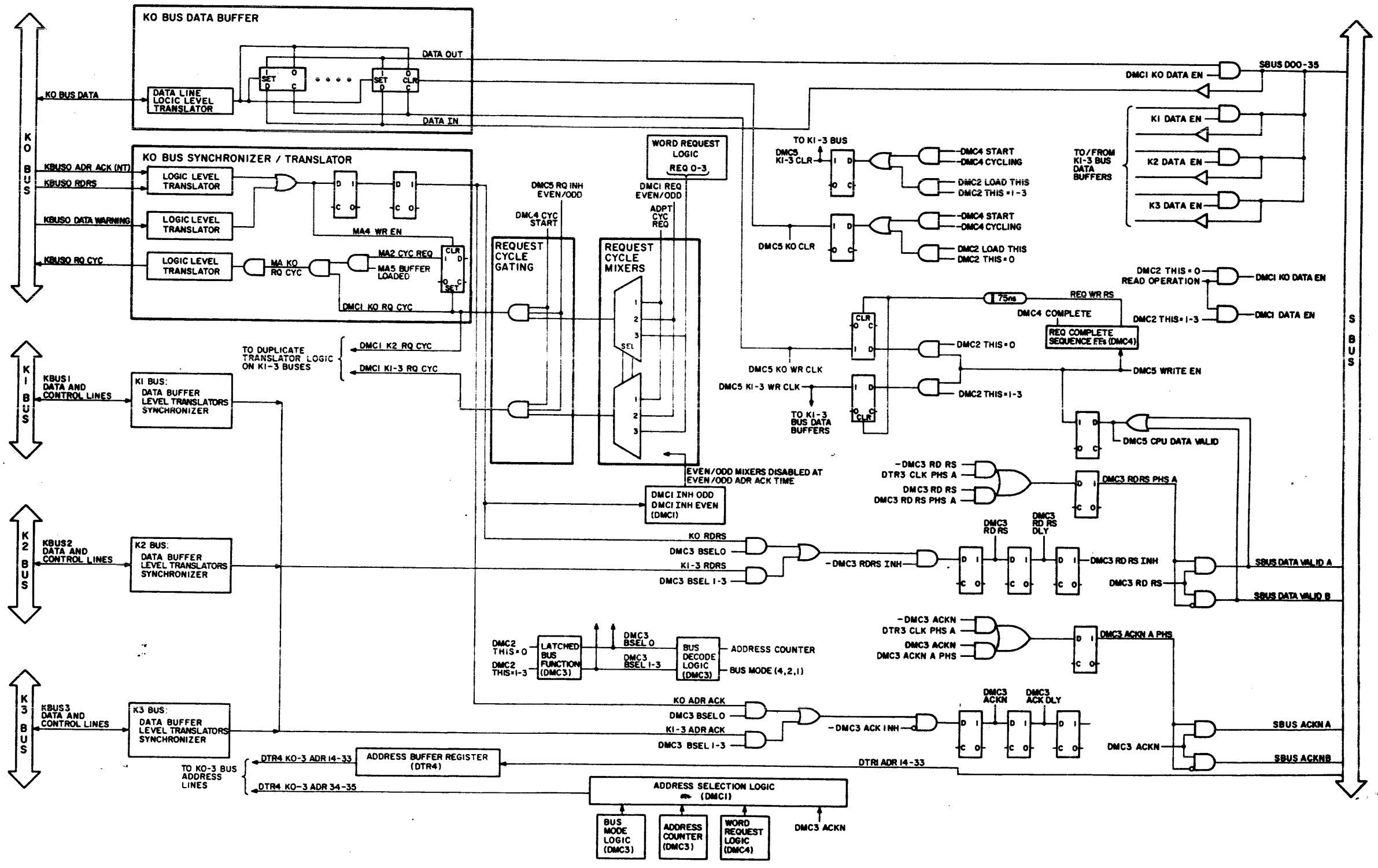


Figure 47 DMA20 Detailed Logic Block Diagram

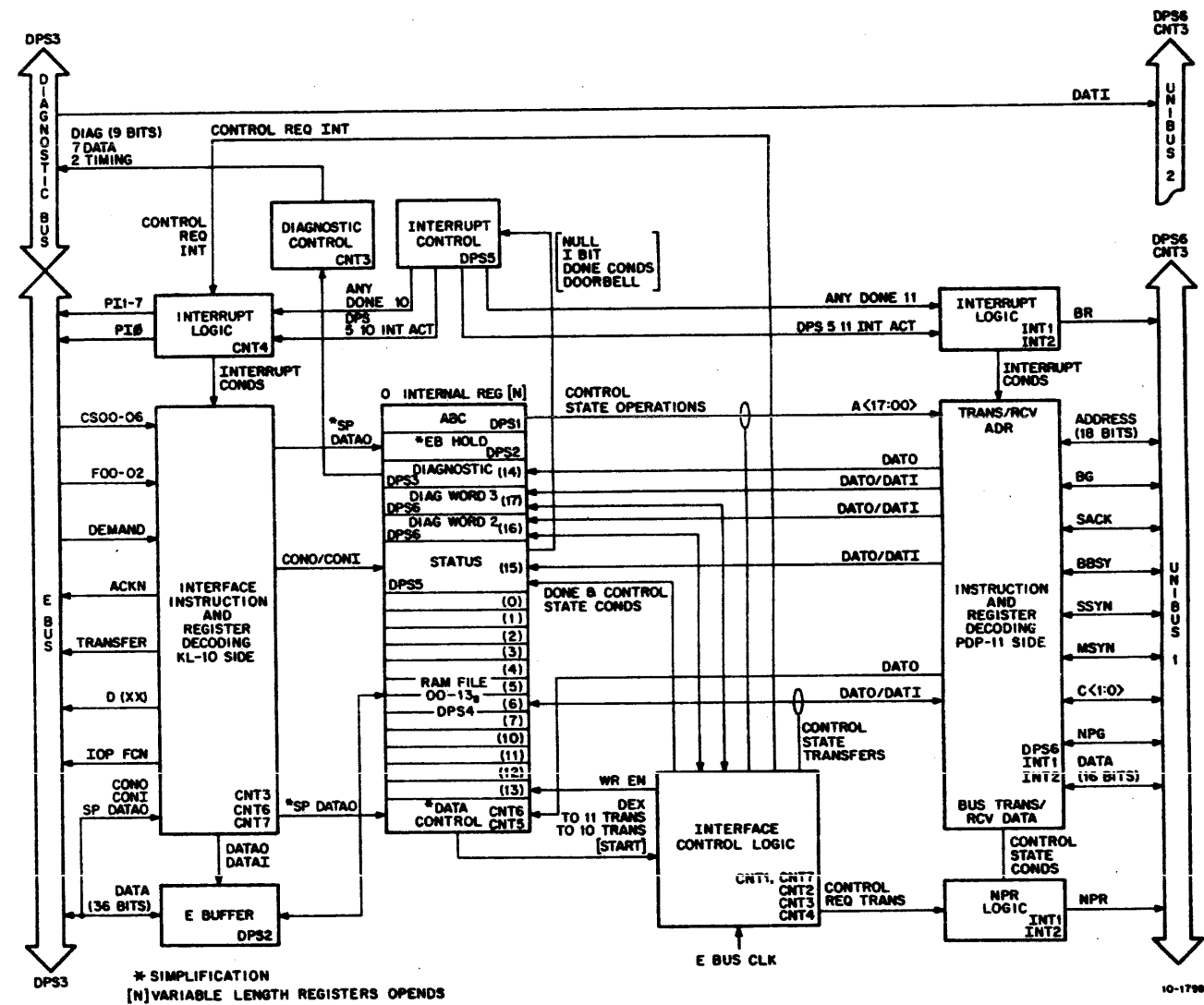
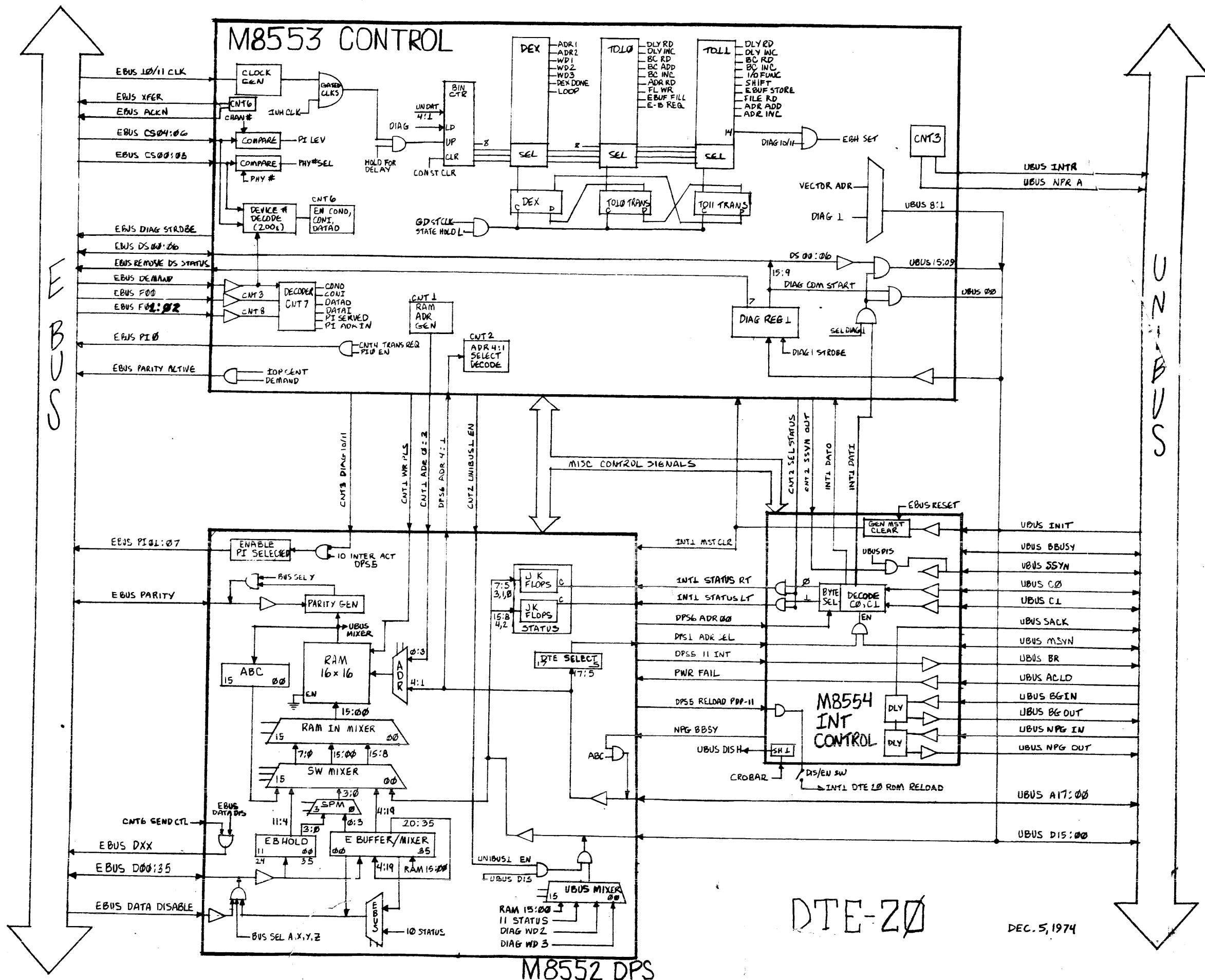


Figure 48 DTE20 Functional Block Diagram (Simplified)



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FIGURE 49 DTE