Table 1-2 (Cont)
Alphabetical Index

Subject	Drawing Number	Type Code	Page
Byte Instruction Flow	KA10-0-BYTF	D-FD	42
Cable Set	7005607-0-0	D-AD	154
Console Switch Connections	KA10-0-ICSC1	D-IC	169
Console Switch Connections	KA10-0-ICSC2	D-IC	170
DC Power Wiring	KA10-0-1	D-IC	155
Divide Subroutine and Fixed Divide	KA10-0-DIVF	D-FD	43
Double Floating Negate	KA10-0-FSDN	D-FD	49
Drawing Index List	KA10-0-3	D-DI	27
Execute and Store Cycle	KA10-0-ESC	D-FD	44
Execution Cycle	KA10-0-E	D-BS	82
Executive Control	KA10-0-EX	D-BS	83
Extended Instruction Set	KE10-0	A-ML	31
External Component List	KA10-0-CP	A-CP	163
Fast Memory	KM10-0	A-ML	33
Fast Memory	KA10-0-FM	D-BS	89
Fast Memory Address	KA10-0-FMA	D-BS	90
Fast Memory Flow	KA10-0-MCFM	D-FD	53
Fetch Cycle Flow	KA10-0-FC	D-FD	46
Fetch Cycle Levels	KA10-0-F2	D-BS	85
Fetch Cycle Time Pulse	KA10-0-F1	D-BS	84
Fixed Divide and Subroutine	KA10-0-DSDV	D-BS	81
Fixed Point Divide and Subroutine	KA10-0-DIVF	D-FD	43
Floating Add Instruction	KA10-0-FA	D-BS	86
Floating ADD, SUB, UFA Flow	KA10-0-FAF	D-FD	45
Floating Divide	KA10-0-FDV	D-BS	87
Floating Divide	KA10-0-FDVF	D-FD	47
Floating Exponent Calculation	KA10-0-FPFM	D-BS	91
Floating Exponent Calculation Subroutine	KA10-0-FPMC	D-FD	48
Floating Exponent Register and Control	KA10-0-FE	D-BS	88

Table 1-2 (Cont)
Alphabetical Index

Subject	Drawing Number	Type Code	Page
Floating Multiply and Multiply Subroutine	KA10-0-FPMC	D-FD	48
Floating Scale and DBL Floating Negate	KA10-0-FSDN	D-FD	49
Half Word Transfer	KA10-0-HWT	D-BS	92
Indicator and Console SW Connections	KA10-0-ICSC1	D-IC	169
Indicator and Console SW Connections	KA10-0-ICSC2	D-IC	170
I/O Bus Control and I/O Selection	KA10-0-IOBC	D-BS	96
I/O Bus Inputs	KA10-0-IOBI	D-BS	97
I/O Bus (0-17)	KA10-0-IOB1	D-BS	94
I/O Bus (18-35)	KA10-0-IOB2	D-BS	95
In-Out Transfer Control	KA10-0-IOT	D-BS	98
In-Out Transfer Control Flow	KA10-0-IOTF	D-FD	51
Instruction and Address Cycles	KA10-0-IAC	D-FD	50
Instruction and Address Cycles	KA10-0-IA	D-BS	93
Instruction Register	KA10-0-IR	D-BS	99
Instruction Register Decoding	KA10-0-IR1	D-BS	100
Instruction Register Decoding	KA10-0-IR2	D-BS	101
Instruction Register Decoding	KA10-0-IR3	D-BS	102
Inter-Bay Cables	KA10-0-IBC1	D-CL	169
Inter-Bay Cables	KA10-0-IBC2	D-CL	170
JFFO Flow	KA10-0-SMF	D-FD	59
JFFO Instruction Control	KA10-0-JFFO	D-BS	103
KA10 Assembly	KA10-A-0	D-UA	194
KA10 Assembly Parts List	KA10-A-0	A-PL	197
KA10 Register Interconnections	KA10-0-REG	D-FD	55
Key and Switches Controls	KA10-0-KEY1	D-BS	104
Key and Switches Controls	KA10-0-KEY2	D-BS	105
Key and Switches Controls	KA10-0-KEY3	D-BS	106
Key Operations Flow Diagram	KA10-0-KO	D-FD	52
Level and Pulse Terminations Bay 1 and 2	KA10-0-TERM	D-CL	173

Table 1-2 (Cont)
Alphabetical Index

Subject	Drawing Number	Type Code	Page
Master Clear and Power Clear	KA10-0-MR	D-BS	117
Memory Address Control	KA10-0-MA1	D-BS	107
Memory Address Register	KA10-0-MA2	D-BS	108
Memory Address Interface	KA10-0-MAI	D-BS	109
Memory Bus Data Interface	KA10-0-MBDI	D-BS	110
Memory Control	KA10-0-MC1	D-BS	111
Memory Control	KA10-0-MC2	D-BS	112
Memory Control and Fast Memory Flow	KA10-0-MCFM	D-FD	53
Memory Indicator	KA10-0-MI	D-BS	113
Module Utilization Panels 1A-1D	KA10-0-1A1D	D-MU	141
Module Utilization Panels 1E-1J	KA10-0-1E1J	D-MU	142
Module Utilization Panels 1K-1N	KA10-0-1K1N	D-MU	143
Module Utilization Panels 1P-1T	KA10-0-1P1T	D-MU	144
Module Utilization Panels 2A-2D	KA10-0-2A2D	D-MU	145
Module Utilization Panels 2E-2J	KA10-0-2E2J	D-MU	146
Module Utilization Panels 2K-2N	KA10-0-2K2N	D-MU	147
Module Utilization Panels 2P-2T	KA10-0-2P2T	D-MU	148
Module Utilization Panels 3A-3D	KA10-0-3A3D	D-MU	149
Module Utilization Panels 3E-3F	KA10-0-3E3F	D-MU	150
Module Count	KA10-0-MC	A-PL	151
Multiplier Quotient (MQ 0-17)	KA10-0-MQ2	D-BS	115
Multiplier Quotient (MQ 18-35)	KA10-0-MQ3	D-BS	116
Multiplier Quotient	KA10-0-MQ1	D-BS	114
Multiply	KA10-0-BTMP	D-BS	77
Multiply Flow	KA10-0-SMF	D-FD	59
Normalize Return and NR Long	KA10-0-NRNL	D-BS	118
Normalize Return Subroutine	KA10-0-NRF	D-FD	54
Paper Tape Punch Control	KA10-0-PTP1	D-BS	126
Paper Tape Punch Control	KA10-0-PTP2	D-BS	127
Paper Tape Reader Control	KA10-0-PTR1	D-BS	128

Table 1-2 (Cont)
Alphabetical Index

Subject	Drawing Number	Type Code	Page
Paper Tape Reader Control	KA10-0-PTR2	D-BS	129
Paper Tape Reader Control	KA10-0-PTR3	D-BS	130
Parity Buffer Register	KA10-0-PB	D-BS	119
Parity Network	KA10-0-PN	D-BS	124
PI Control	KA10-0-PI1	D-BS	122
Power Clear	KA10-0-MR	D-BS	117
Priority Interrupt PIH, PIR, PIO	KA10-0-PI2	D-BS	123
Program Counter Control	KA10-0-PC1	D-BS	120
Program Counter Register	KA10-0-PC2	D-BS	121
Protect Register	KA10-0-PR	D-BS	125
Pulse and Level Terminations Bay 1 and 2	KA10-0-TERM	D-CL	171
Readin Function Isolated Flow	KA10-0-RIMF	D-FD	56
Register Interconnections	KA10-0-REG	D-FD	55
Relocate Register	KA10-0-RL	D-BS	131
Shift Connections	KA10-0-ARMQ	D-FD	73
Shift Count Register	KA10-0-SC	D-BS	134
Shift Count Adder	KA10-0-SCAD	D-BS	135
Shift Counter Control	KA10-0-SCC1	D-BS	136
Shift Counter Control	KA10-0-SCC2	D-BS	137
Shift and Count Subroutine and Shift Instruction	KA10-0-SCSR	D-BS	138
Shift Count Subroutine and BLT Flow	KA10-0-SCBT	D-FD	58
Shift Count Action Flow	KA10-0-SCAF	D-FD	57
Shift and MUL and JFFO Flow	KA10-0-SMF	D-FD	59
Store Cycle	KA10-0-ESC	D-FD	44
Store Cycle Time Pulses	KA10-0-S1	D-BS	132
Store Cycle Levels	KA10-0-S2	D-BS	133
Switch Controls	KA10-0-KEY1	D-BS	104
Switch Controls	KA10-0-KEY2	D-BS	105
Switch Controls	KA10-0-KEY3	D-BS	106
Teletype Control	KA10-0-TTY1	D-BS	139

Table 1-2 (Cont)
Alphabetical Index

Subject	Drawing Number	Type Code	Page
Teletype Control	KA10-0-TTY2	D-BS	140
TTY Socket Wiring	KA10-0-GW	A-WL	168
Time Sharing Option	KT10-0	A-ML	36
Twisted Pair List KA10 Bay 1	KA10-0-TWP1	A-WL	174
Twisted Pair List KA10 Bay 2	KA10-0-TWP2	A-WL	183
Wire List KA10	KA10-0-4	K-WL	162

Table 1-3
KA10 Signal Glossary

Signal Name	Source Drawing	Description
AD0-35	AD3	Adder. Performs arithmetic and logical operations using AR and BR register contents as inputs.
AD0-7=0	AD2	Level. True when bits AD0 through 7 contain all zeroes.
AD 1 AR INP	AD3	Level. Used to generate AD CRY1 on AD2.
AD 1 BR INP	AD3	Level. Used to generate AD CRY1 on AD2.
AD9-35=0	AD2	Level. True when bits AD9 through 35 all contain zeroes.
AD10-35=0	AD2	Level. True when bits AD10 through 35 all contain zeroes.
AD AR NEGATE (FT9)	AD2	Level. Setup for two's complement of AR contents. Produces AD AR-EN (FT9) and AD CRY 36 (FT9).
AD AR+ EN	AD1	When set, gates ARn (1) to ADn.
AD AR+ EN (FT9)	AD2	Level. Prevents FT9 from clearing AD AR+ EN.
AD AR- EN	AD1	When set, gates ARn (0) to ADn.
AD AR- EN (FT9)	AD2	Level. Allows FT9 pulse to set AD AR- EN.
AD BR± (FT9)	AD2	Level. Produces AD BR+ EN (FT9) and AD BR- EN (FT9). Used to form arithmetic -1 at AD inputs.
AD BR+ EN	AD1	When set, gates BRn (1) to ADn.
AD BR+ ONLY EN (ET0)	AD2	Level. Enables ET0 pulse to clear AD AR+ EN, AD AR- EN, AD CRY 36, and to set AD BR+ EN.
AD BR- EN	AD1	When set, gates BRn (0) to ADn.
AD BR- EN (FT9)	AD2	Level. Enables FT9 pulse to set AD BR- EN.
AD COND	AD2	Level. Provides sign/overflow compensation for arithmetic compare instructions (CAMX and CAIX).
AD CRY 0	AD2	Level. Indicates carry out of bit AD0.
AD CRY 1	AD2	Level. Indicates carry out of bit AD1.
AD CRY 36	AD1	When set, produces carry into AD35. Used for incrementing or for two's complement subtraction.
AD CRY 36 (FT9)	AD2	Level. Enables FT9 pulse to set AD CRY 36.
AD CRY ALLOW	AD2	Level. Completes the carry logic through AD bits 5, 14, 23, 32 (B138's). When false, speeds up carry de-propagation, important to multiply instructions.

Table 1-3 (Cont)
KA10 Signal Glossary

Signal Name	Source Drawing	Description
AD CRY INS	AD1	When set, produces carry into summing network of all adder bits turning the adder into an "EQUIVALENCE" gate for the normal inputs.
AD CRY INS (FT9)	AD2	Level. Enables FT9 pulse to set AD CRY INS.
AD = 0	AD2	Level. True when all adder bits are zero.
AD MD+	AD2	Level. Enables SCT3 pulse (and others) to set AD BR+ EN during multiply or divide subroutine, as determined by operands.
AD MD-	AD2	Level. Enables SCT3 pulse (and others) to set AD BR- EN and AD CRY 36 during multiply or divide subroutine, as determined by operands.
AD MINUS BR (FT9)	AD2	Level. Produces AD BR- EN (FT9) and AD CRY 36 (FT9). Setup for subtraction of BR contents from AR contents.
AD+1 BOTH (FT9)	AD2	Level. Produces AD CRY 36 (FT9) and permits FT9 pulse to set AD+1 LH.
AD+1 LH	AD1	When set, causes a "one" input to AD17.
AD-1 LH	AD1	When used in conjunction with AD BR+ EN and AD BR- EN, causes a "zero" input to AD17.
AF2	IA	Address cycle memory subroutine flip-flop. Also causes AT3 to deliver indexed address to AR from AD.
AR0-35	AR1	Arithmetic register. Used for holding arithmetic operand. Communicates with memory bus, in-out bus, and fast memory.
AR0 = BR0	ARC3	Level. True for equal signs of AR and BR operands. Used during floating point exponent calculation. (FMP or FDV).
AR0 = SCAD0	ARC3	Level. True for equal signs of AR and SCAD (shift counter adder). Used during floating point exponent calculation. (FMP or FDV).
AR0 SHLT INP	ARMQ	Level. Provides left shift inputs to AR0 as shown on SCAF diagram.
AR35 SHLT INP	ARMQ	Level. Provides left shift inputs to AR35 as shown on SCAF diagram.
AR CRY 0 FLAG	ARF	Stores condition of AD CRY 0 resulting from certain arithmetic operations.
AR CRY 1 FLAG	ARF	Stores condition of AD CRY 1 resulting from certain arithmetic operations.

Table 1-3 (Cont)
KA10 Signal Glossary

Signal Name	Source Drawing	Description
AR DCK	ARF	Divide check flag. Set when fractional dividend not smaller than divisor.
AR FOV	ARF	Floating point overflow flag. Set for various error conditions by floating point instructions. Interrupt possible.
AR FXU	ARF	Floating point exponent underflow. Set by normalize return subroutine if result exponent is too negative to represent.
AR OV COND	ARF	True when overflow occurs during an additive process. An inequality (XOR) of AD CRY 0 and AD CRY 1. Used to set AR OV FLAG.
AR OV FLAG	ARF	Arithmetic overflow flag. Set by any arithmetic overflow condition. Interrupt possible.
AR SWAP	ARC1	Pulse. Causes the two 18-bit halves of AR contents to be exchanged.
AR0 XOR AR1	ARF	Level. Used to set AR OV FLAG during an arithmetic left shift.
ARF CRY STB	ARF	Pulse. Causes AD CRY 0 and AD CRY 1 to be stored in AR CRY0 FLAG and AR CRY1 FLAG; and stores AR OV COND in AR OV FLAG.
AS COND	AS	Level. True when contents of console address switches equal the absolute core memory address. Used for address stop or break (MC2) and memory indicator loading (MI).
AS = FMA	AS	Level. True when contents of address switches equals output of FMA address selector.
AS = RLA	AS	Level. True when contents of address switches equals the memory bus memory address. (RLA is obsolete)
BIO CPA SEL	MR	Level. True when IR 3-9 contain 000. Processor device address.
BIO PI SEL	MR	Level. True when IR 3-9 contain 004. Priority interrupt device address.
BIO PTP SEL	MR	Level. True when IR 3-9 contain 100. Paper tape punch device address.
BIO PTR SEL	MR	Level. True when IR 3-9 contain 104. Paper tape reader device address.

Table 1-3 (Cont)
KA10 Signal Glossary

Signal Name	Source Drawing	Description
BIO TTY SEL	MR	Level. True when IR 3-9 contain 120. Console teletype device address.
BLT FI	BTMP	Subroutine flop for block transfer. Used when storing word in destination location.
BR0-35	BR2	Buffer register. Holds arithmetic operand.
BYF4	BYTE	Subroutine flop for restoring incremented pointer in byte instructions. Also enables MQ to shift left (MQ1) to generate mask.
BYF5	BYTE	Control flop for byte instructions. When zero causes "first part" activities (incrementation and/or size mask generation); when one causes "second part" activities (operand fetch and loading or depositing). BYF5 (0) produces PC+1 INH.
BYF6	BYTE	Byte increment status (BIS) flag. Set by ILDB and IDPB in "first part" and cleared in "second part". Prevents double incrementation if instruction is interrupted between parts as may happen. BYF6 is the "Byte Interrupt" stored by JSR, JSP, PUSHJ and restored by JRSTF.
BYTE PTR INC	BYTE	Level. Allows ET0 pulse to start "first part" at BYT1 for those conditions and instructions which require byte pointer incrementation.
BYTE PTR NOT INC	BYTE	Level. Causes bypassing of the incrementation sequence for those instructions which load or deposit but do not want to change the pointer at this time. Allows ET0 to pulse BYT6.
CPA ADR BREAK	CPA	Set by an address break condition. Interrupt possible.
CPA AR OV EN	CPA	When set, enables AR OV FLAG to processor interrupt decoder.
CPA CLK EN	CPA	When set, enables power frequency clock to processor interrupt decoder.
CPA CLK FLAG	CPA	Set by CPA PWR CLK once each cycle of line current. Interrupt possible.
CPA FOV EN	CPA	When set, enables AR FOV to processor interrupt decoder.
CPA MEM PROT FLAG	CPA	Set by MC ILLEG ADR when a memory reference in user mode uses a relative address larger than the protection constant. Interrupt possible.

Table 1-3 (Cont)
KA10 Signal Glossary

Signal Name	Source Drawing	Description
CPA NON EX MEM	CPA	Level. Set by MC NON EX MEM when no core module responds. Interrupt possible.
CPA PAR ENB	CPA	Level. Enables CPA PAR ERR to processor interrupt decoder.
CPA PAR ERR	CPA	Set by MC PAR ERR when even parity is detected in a word read from core memory.
CPA PDL OV	CPA	Push down list pointer overflow. Set if left half of pointer goes to zero when incremented or decremented by the pushdown instructions.
CPA PIA 33-35	CPA	Processor interrupt bus address storage flops. Non-zero to allow interrupt.
CPA PWR CLR	CPA	Pulse. One pulse per cycle of line current.
CPA PWR FAIL	CPA	Sets if two consecutive CPA PWR CLK pulses are missed. Interrupt possible.
DB BYTE DEP	DBLB	Level. Common to DPB and IDPB to condition "second part" operations such as shifting AR and MQ to the left.
DIV LOW ZERO COND	DSDV	Level. During the negation of two word dividends (floating or fractional) this indicates that second word is zero.
DSFI	DSDV	Divide subroutine flop. Enables left shift of AR and MQ at SCT3 with connections as shown on SCAF diagram. Permits AD MD+ and AD MD- to be controlled by BR0 and AD0.
DSF7	DSDV	Flip-flop used to store the original sign of the dividend in a divide instruction. (Divide subroutine requires a positive dividend.)
DSF7 XOR BR0	DSDV	Level. True when dividend and divisor are of opposite sign. Used at end of divide to correct the quotient sign.
E LONG	E	Level. Enabled by those instructions which use a long execution cycle (ET0, ET1, ET2). Permits ET0 DEL to pulse ET1.
E LONG V ST INH	E	Level. Prevents ET0 DEL from pulsing ST1.
E UUOF	E	Set by UUO instruction. Causes the following IT0 to set MA35.

Table 1-3 (Cont)
KA10 Signal Glossary

Signal Name	Source Drawing	Description
E XCTF	E	Set by UUO, XCT, or KEY RDI DONE pulse to prevent the following IT0 from disturbing the MA, which points to the instruction to be executed.
EF0 LONG	E	Level. Causes a long delay to occur between FT9 and ET0 to allow for additive processes (AD XX EN set and carry propagation times).
EVEN 0-8	PN	Level. True when PB bits 0-8 contain even parity.
EVEN 0-26	PN	Level. True when PB bits 0-26 contain even parity.
EVEN 9-17	PN	Level. True when PB bits 9-17 contain even parity.
EVEN 18-26	PN	Level. True when PB bits 18-26 contain even parity.
EVEN 27-35	PN	Level. True when PB bits 27-35 contain even parity.
EX ALLOW IOTS	EX	Level. Indicates that machine is in executive mode or privileged user mode. Used on IR UUO.
EX ILL OP	EX	Set by UUO's which trap to absolute locations 40 or 60. Suppresses relocation by producing EX TRAP COND. Cleared by an IOT BLK executed from a PI location if UUO interrupted between halves. (Prevents unwanted memory reference by an unrelocated user PC.) Normal clear is by subroutine jump instruction in 41 or 61.
EX IOT USER	EX	Set by executive mode JRSTF only. Allows user program to use all instructions, does not affect relocation, however.
EX MODE SYNC	EX	When set, causes entry into user mode at subsequent IT0 (MR CLR).
EX PI SYNC	EX	Set by PI CYC (1). Prevents relocation of PI trap address (40+2n) by producing EX TRAP COND.
EX REL A, B	EX	True when in user mode and not referencing an AC, UUO or PI trap location, or performing an examine or deposit. When true, causes address checking by the protection adder (PR) and use of relocated address (MAI).
EX TRAP COND	EX	Level. True when fetching an instruction from a PI trap location or a non-relocated UUO trap location. Prevents relocation by making EX REL A and EX REL B false. If fetched instruction is JSR, JSP, PUSHJ, will cause EX USER to clear (to exec. mode).

Table 1-3 (Cont)
KA10 Signal Glossary

Signal Name	Source Drawing	Description
EX USER	EX	When a one, machine is in user mode. Determines decoding of IR UUO, EX REL A, EX REL B (chiefly).
FAC INH	F2	Level. ("Fetch AC Inhibit") When true, causes (AC) fetch to be bypassed in fetch cycle.
FAC2	F2	Level. ("Fetch AC_2") When true causes fetch of (AC+1) to occur (FT5).
FAF1	FA	Shift subroutine flop set by floating add routine.
FCC ACLT	F2	Level. ("Fetch C (C (AC) Left)") When true causes the left half contents of fetched AC to be used as an operand address from which a word is fetched (FT7).
FCC ACRT	F2	Level. ("Fetch C (C (AC) Right)") When true causes the left half contents of fetched AC to be used as an operand address from which a word is fetched (FT7).
FCE	F2	Level. ("Fetch C(E)") When true causes the contents of the location addressed by MA to be fetched by MC RD RQ. (FT0).
FCE PSE	F2	Level. ("Fetch C(E); Pause") When true causes the contents of the location address by MA to be fetched by MC RD/WR RS. (FT1). This level is produced instead of FCE by those instructions which store a result in the location from which a memory operand was fetched, and which have a relatively short execution time. (e.g. FADM doesn't meet the latter requirement, SUBM meets both.)
FDF1	FDV	Memory subroutine flop set when floating divide fetches dividend exponent from memory.
FDF3	FDV	Flop set to store fact that dividend was unnormalized by one right shift. Used at end of floating divide to assure proper remainder exponent (which is related to dividend exponent).
FMA AC EN	FMA	Level. Makes FMA 32-35 a copy of IR 9-12. (Accumulator address).
FMA AC2 EN	FMA	Level. Makes FMA 32-35 equal to (IR 9-12) +1.
FMA MA EN	FMA	Level. Makes FMA 32-35 a copy of MA 32-35. Also inhibits FMA AC EN, FMA AC2 EN, and FMA XR EN. Produced when a core memory request is initiated to read out of a fast memory location (e.g. PC or E is 0-18).

Table 1-3 (Cont)
KA10 Signal Glossary

Signal Name	Source Drawing	Description
FMA XR EN	FMA	Level. Makes FMA 32-35 a copy of IR 14-17. (Index register address).
FMD 0-17	FMA	Level. Binary to 1 out of 16 decoder. One output selects a 36 bit fast memory location (FM).
FP EXP ADD	FPFM	Level. Used during exponent calculation to change SCAD inputs so that exponent magnitudes are added during FMPX and subtracted during FDVX instructions.
HWT 3 LET	HWT	Level. ("half-word transfer (3 Letter)") in direct mode which specify that "other half" is to be preserved. (e.g. HRL).
HWT ARLT CLR (ET0)	HWT	Level. True for half-word transfers which zero the left half. (e.g. HXRZX). The action occurs at ET0 because of this level.
HWT BR ± EN (FT9)	HWT	Level. Produces AD BR ± EN (FT9) for those half word instructions which set to ones the "other half" receiving word.
HWT DIR	HWT	Level. Direct or blank mode for half word instructions. (IR7 and 8 = 0).
HWT E TEST	HWT	Level. Used for HXXEX instructions to determine the four outcomes: 0 to left, 0 to right, 1's to left, 1's to right.
IF0	IA	Instruction fetch/indirect word fetch memory subroutine flop. Also used in address condition test (MC2).
IOB0-35	IOB1	In-out bus data lines
IOB BUS RESET A-D	IOBC	A 2 μs pulse that switches 20 mA additional clamped load to each bus data line (IOB0-35) to restore the zero state (-3V).
IOB CONO CLR	IOBC	Conditions out clear. A 400 ns pulse that may be used by a device to clear its command/status register.
IOB CONO SET	IOBC	Conditions out set. A 400 ns pulse used by devices to load command register from IOB0-35.
IOB DATAI	IOBC	A 2.5 μs pulse used to gate an input device data register to IOB0-35.
IOB DATAO CLR	IOBC	Data out clear. A 400 ns pulse used by output device to clear data register.

Table 1-3 (Cont)
KA10 Signal Glossary

Signal Name	Source Drawing	Description
IOB DATAO SET	IOBC	Data out set. A 400 ns pulse used by output device to load its data register from IOB0-35.
IOB DR SPLIT	IOBC	"Drum split." May be activated by a device attached to memory port to prevent processor from doing read-modify-write cycles. (See MC SPLIT CYC SYNC).
IOB PI 1-7	IOBC	Bus priority interrupt lines. Grounded by a device requesting service on that channel.
IOB RDI DATA	IOBC	Readin data flag. Activated by device during a key read in operation when a data word is ready.
IOB RDI PULSE	IOBC	Readin pulse. A 400 ns pulse issued to start the selected device for key readin operations.
IOB RESET	IOBC	General clear pulse going to all devices.
IOB STATUS	IOBC	A 2.5 μs pulse used to gate a device status register to IOB0-35. Called IOB CONI on IO bus.
IOS 3-9	IOBC	Device selection code. A buffered version of IR 3-9.
IOT BLK	IOT	Level. True for either BLKI OR BLKO op codes.
IOT CONSX	IOT	Level. True for either CONSO or CONSZ op codes.
IOT DATA XFER	IOT	A 2.5 μs pulse. Basic timing for placing information on IOB0-35.
IOT F1	IOT	Memory subroutine flop used by BLKI, BLKO when restoring incremented pointer.
IOT GO	IOT	Synchronizing flip-flop that is set at ET0 to request entry into IOTT0-5.
IOT OUT GOING	IOT	Level. True for either CONO or DATAO or second part of BLKO.
IR 0-17	IR	Instruction register. Holds OP, AC, I, X during execution.
IR 0XX	IR1	Level. Means op code in range 000 to 077.
IR 13X	IR2	Level. Indicates op code in range 130 to 137.
IR 26X E LONG	IR3	Level. True for those codes in this range requiring long execution cycle. Pushdowns, JSR, JSA, JRA.
IR AOJX	IR3	Level. True for Add one and jump, any mode.
IR AOSX	IR3	Level. True for Add one and skip, any mode.
IR AOXX	IR3	Level. True for AOJX or AOSX.

Table 1-3 (Cont)
KA10 Signal Glossary

Signal Name	Source Drawing	Description
IR AS	IR1	Level. True for add or subtract, any mode.
IR AS BOTH	IR3	Level. True for ADDB, SUBB. Used to provide fetch cycle levels (F2).
IR AS DIR	IR3	Level. True for ADD, SUB. Used to provide fetch cycle levels. (F2).
IR AS IMM	IR3	Level. True for ADDI, SUBI.
IR AS MEM	IR3	Level. True for ADDM, SUBM. Used to provide fetch cycle levels. (F2)
IR BOOLE 0-17	IR2	Levels. Decoding of the 16 Boolean instructions, any mode. (See BIF1.)
IR FDV NOT L	IR3	Level. True for FDV, FDVR, all modes except FDVL.
IR FP	IR2	Level. True for op codes 140-177 (Floating point) unless floating point trap switch is on (IR UUO, IR2 drawing),
IR IOT	IR2	Level. True when IOT op code in IR and IOT's are permissible (See IRUUO).
IR IOT A	IR1	Level. True when IR0-2 = 7 (IOT op code).
IR JRST	IR2	Level. True when JRST op code in IR and JRST is permissible. (See IRUUO)
IR JRST A	IR1	Level. True when 254 op code in IR (JRST op code).
IR JUMPS	IR3	Level. True for JUMPX, AOJX, SOJX op codes. Used to condition PC from MA transfer during these instructions (PC1).
IR LT EN	IR	When set, enables IR bits 0-12 to receive input from memory bus.
IR MD	IR2	Level. True for MUL, IMUL, DIV or IDIV op codes, any mode.
IR RDI SETUP	IR	Pulse. Issued by key readin operation to force IR to contain DATAI DEV, or BLKI DEV, depending on RDI PART 2 flop. "DEV" (IR3-9) determined by readin device switches on maintenance panel.
IR RT EN	IR	When set, enables IR bits 13-17 to receive input from memory bus.
IR TEST	IR1	Level. True when op code 600-677 in IR. Boolean test class of instructions.

Table 1-3 (Cont)
KA10 Signal Glossary

Signal Name	Source Drawing	Description
IR UUO	IR2	Level. Unimplemented User Operation True for op codes 000-127 and 130-177 if FP trap switch is on. Also true for IOT, HALT, JEN in non-privileged user mode. When true, inhibits IR IOT and IR JRST.
IT0-IT1	IA	Instruction cycle time pulses.
KEY ADR BRK	KEY1	Level. True when console ADR BREAK switch is on.
KEY ADR INST	KEY1	Level. True when console ADDRESS CONDITION INST FETCH switch is on.
KEY ADR RD	KEY1	Level. True when console ADDRESS CONDITION DATA FETCH switch is on.
KEY ADR STOP	KEY1	Level. True when console ADR STOP switch is on.
KEY ADR WR	KEY1	Level. True when console ADDRESS CONDITION WRITE switch is on.
KEY AS STROBE EN	KEY3	Level. True for those key operations which use data switch information.
KEY AT INH	KEY2	100 μs level. Produced by RESET with RUN (1). Holds IF0 cleared to stop instruction cycle, preventing data from being clobbered when clear pulse is issued.
KEY CONT SW	KEY1	Continue. Momentary level true when console CONT switch is held on.
KEY DEP NXT SW	KEY1	Deposit next. Momentary level, true when console DEPOSIT - NEXT switch is held on.
KEY DEP SW	KEY1	Deposit this. Momentary level, true when console DEPOSIT - THIS switch is held on.
KEY EX NXT	KEY1	Examine next. Momentary level, true when console EXAMINE - NEXT switch is held on.
KEY EXA SW	KEY1	Examine this. Momentary level, true when console EXAMINE - THIS switch is held on.
KEY EXE SW	KEY1	Execute. Momentary level, true when console XCT switch is held on.
KEY F1	KEY3	Memory subroutine flop used by examines and deposits. Also used in MI control to allow data to be displayed.
KEY FCN CLR	KEY1	Pulse. Clears key function storage register at termination of function execution.

Table 1-3 (Cont)
KA10 Signal Glossary

Signal Name	Source Drawing	Description
KEY FCN STROBE	KEY1	Pulse. Loads corresponding function register flop from momentary key level.
KEY IT0 EN	KEY3	Level. True when FT9 to be allowed to pulse IT0.
KEY MANUAL	KEY1	Level. Produced by key functions to initiate timing chain.
KEY MEM REF	KEY3	Level. True for those key functions (examines and deposits) which reference memory.
KEY MID INST STOP	KEY3	Level. True when a memory stop or shift counter stop has occured. Used to condition action of CONT key on RUN flip-flop.
KEY NEXT	KEY3	Level. True for examine next or deposit next. Causes key flow to increment MA.
KEY NXM STOP	KEY1	Level. Non-existent memory stop. True when console NXM STOP switch is on. Used in memory control (MC2).
KEY PAR STOP	KEY1	Level. Parity stop. True when console PAR STOP switch is on. Used in memory control (MC2).
KEY PI INH	KEY1	Level. True during key execute operation to prevent interrupts and PC incrementation at FT9. (PI1 and PC1).
KEY PROG STOP	KEY3	Level. True for HALT instruction, enables clearing of RUN flop.
KEY RDI DLY	KEY2	One-shot. Used to produce IOB RDI PULSE to start read in device. Delay permits device selection levels to settle down on bus.
KEY RDI DONE	KEY3	Read in done. Pulse sets up machine to execute the last word read in by setting RUN and E XCTF.
KEY RDI PART 2	KEY3	Determines how IR12 is affected by IR RDI SETUP pulse to cause either DATAI or BLKI op code.
KEY RDI SW	KEY1	Momentary level. True when console READ IN switch is held on.
KEY REPEAT BYPASS SW	KEY1	Level. True when maintenance panel REPEAT BY-PASS switch is on. Used when troubleshooting key time pulses. Allows KT0 to be retriggered by the repeat delay.
KEY REPEAT SW	KEY1	Level. True when console REPT switch is on. Inhibits KEY FCN CLR and allows KEY DONE to retrigger KT0 after the delay as controlled by maintenance panel speed knobs.

Table 1-3 (Cont)
KA10 Signal Glossary

Signal Name	Source Drawing	Description
KEY REPT DLY	KEY1	Variable delay controlled by speed knobs on maintenance panel. Used to retrigger KT0.
KEY REPT SYNC	KEY1	Set by KEY REPEAT operations, inhibits KEY FCN CLR.
KEY RESET SW	KEY1	Momentary level. True when console RESET switch is held on.
KEY RIM	KEY3	Remains set during readin operation. Allows entry to IT0 when IOB RDI DATA pulse occurs (for each data word). Also allows BLKI pointer overflow to set PI OV.
KEY RUN CLR	KEY3	Pulse. Clears RUN flop at time appropriate to operation (HALT, STOP switch, or SING INST switch).
KEY SING CYCLE	KEY1	Single cycle. True when console SING CYCLE switch is on. Causes memory stop after each reference.
KEY SING INST	KEY1	Single instruction. True when console SING INST switch is on. Used to clear RUN during instruction execution.
KEY SP CNTL-X	KEY1	Connections to coarse and fine speed controls on maintenance panel. (See KEY REPT DLY)
KEY STA SW	KEY1	Momentary level. True when console START switch is held on.
KEY STOP SW	KEY1	Momentary level. True when console STOP switch is held on.
KEY SYNC	KEY3	Set to allow ST9 to pulse KT1 for those key functions which operate when RUN is a one (EXA THIS, DEP THIS, EXE).
KEY SYNC RQ	KEY3	Set by certain key functions (see KEY SYNC) to enable FT9 to set KEY SYNC.
KNT1-3	KEY3	Pulse chain used by key next operations to increment MA.
KST1-2	KEY2	Pulse chain used by STOP and RESET functions.
KT0-KT4	KEY2	Key timing pulse chain.
LB BYTE LOAD	DBLB	Level. Produced for LDB, ILDB "second part" to cause fetching of operand, loading of byte.
M BUS 0-35	MBDI	Memory bus data lines, bi-directional. Connect to AR and IR. Called MBD0-35 on Memory Bus.
MA 18-35	MA2	Memory address register.

Table 1-3 (Cont)
KA10 Signal Glossary

Signal Name	Source Drawing	Description
MAIB MM 18-21,35	MAI	Bipolar module selection levels to bus. Four bits to address a module, may be 18-21 (normal) or 18-20, 35 (interleaved) as determined by switches on module. Called MADR18-22, 35 on memory bus.
MC ADR ACK	MC1	Local acknowledge pulse triggered by MAI CMC ADR ACK. Clears parity buffer and MC RQ flop to end nonexistent memory check.
MC ADR BREAK SET	MC2	Pulse to set CPA address break flop when conditions are met.
MC BUS WR RS	MC1	Pulse to core memory to enable write portion of cycle. Issued after data sent to module.
MC FM EN	MC1	Level. True when maintenance panel FM DISABLE switch is off. Causes all references to address 0-17 to go to fast memory. If false, causes core memory references to these addresses and prevents read-modify-write (pause) operations.
MC FM RD RQ	MC1	Pulse to initiate reading core locations 0-17 when in address or fetch cycles. (AC or AC2 fetch).
MC FM WR RQ	MC1	Pulse to initiate writing core locations 0-17 when in store cycle (AC or AC2 store).
MC IGNORE PARITY	MC2	Flop set by MAI IGN PAR PULSE to inhibit parity checking when reading from a 36 bit (no parity plane) core memory.
MC ILLEG ADR	MC2	Pulse. Happens if protection violation in user mode memory reference. Sets CPA MEM PROT FLAG and causes exit from memory subroutine with no reference to core memory.
MC NON EX MEM	MC2	Pulse occurs 100 μs after memory request if no response (ADR ACK). Sets CPA NON EX MEM flop and causes exit from the memory subroutine.
MC NXM RD	MC2	Pulse. Uses NON EX MEM pulse to simulate action of read restart.
MC NXM RST	MC2	Pulse. Uses NON EX MEM pulse to simulate action of address acknowledge.
MC PAR ERR	MC1	Parity error pulse. Occurs during read if 37 bits have even parity unless told to ignore parity. Sets CPA PAR ERR flop.

Table 1-3 (Cont)
KA10 Signal Glossary

Signal Name	Source Drawing	Description
MA 18-31 = 0	MAI	True when MA contains an address in range 0-17. Used to cause MC access to fast memory if one exists or to suppress relocation (EX REL A, B) if one doe not.
MA 29-35 SET	MAI	Pulses. Used to force reserved location addresses into a cleared MA. Used in PI, UUO Operations.
MA FM PICH (1)	MAI	Pulse. Sets address 40 + 2N into MA in response to interrupt on channel N.
MA TRAP OFFSET	MAI	Level. True when switch in bay 1 is on. Used to change references to non-relocated 40-61 to 140-161 as in a dual processor system.
MAI 18-35	MAI	Memory address interface. The address bits that go on the memory bus. May be copy of MA, RLA and MA, or FMA.
MAI CMC ADR ACK	MAI	Pulse. Core memory address acknowledge. Issued by addressed module at start of memory cycle.
MAI CMC RD RS	MAI	Pulse. Core memory read restart. Issued by core memory at same time data strobed onto bus to enter the AR.
MAI FMA SEL	MAI	Set when core locations 0-17 are to be addressed from FMA address selector. Makes MAI 18-31 = 0 and MAI 32-35 a copy of FMA 32-35.
MAI IGN PAR PULSE	MAI	Core memory ignore parity pulse. May be issued by memory at same time as ADR ACK to inhibit processor parity checking.
MAIB 21-35	MAI	Buffered MAI bits. Called MADR 21 to 35 on memory bus.
MAIB FMC SELECT	MAI	For bus compatibility with PDP-6. Pin T must be negative and pin V ground to allow memory modules to accept requests.
MAIB MC RD	MAI	Buffered read signal (level) to core memory. Called RD REQ on memory bus.
MAIB MC REQ CYC	MAI	Buffered request level to core memory. Used to start memory access. Inhibited during power up process. Called REQ CYC on memory bus.
MAIB MC WR	MAI	Buffered write signal (level) to core memory. Called WR REQ on memory bus.

Table 1-3 (Cont)
KA10 Signal Glossary

Signal Name	Source Drawing	Description
MC PAR STOP	MC2	Set by request pulse if console PAR STOP switch is on. Lengthens read timing to allow parity checking to take place between RD RS and MC RST0. Will enable MC STOP to set if error detected.
MC PARITY PULSE	MC1	Bidirectional pulse generated by a one in plane 36 of core memory during a read and sent to the parity buffer (PB) also generated by processor during a write at same time as MC WR RS, if necessary.
MC RD	MC2	Read command flop. Produces MAIB MC RD. Enables MBDI 0-35 to receive data from M BUS 0-35.
MC RD RQ PULSE	MC1	Pulse triggered from instruction flow to start a memory read operation. Sets MC RD.
MC RD RS	MC1	Local pulse produced by MAI CMC RD RS. Starts parity checking.
MC RD/WR RQ PULSE	MC1	Pulse triggered from instruction flow to start a read-pause operation. Sets both MC RD and MC WR.
MC RD/WR RS	MC1	Pulse triggered from instruction flow to restart a paused memory in the write cycle.
MC REQ CYC	MC2	Level. When true, causes a request to core memory.
MC RQ	MC2	Flop set by read, read-pause, or write requests. Causes a core memory or fast memory cycle to begin depending upon the contents of MA and MC FM EN.
MC RQ PULSE	MC1	Pulse common to all memory requests. Starts non-esistent memory timer, and address checking. Causes PI system to strobe requests from I/O bus.
MC SPLIT CYC EN	MC2	Level. True for those cases in which read-modify-write (pause) operations must be prevented.
MC SPLIT CYC SYNC	MC2	Flop set to prevent read-modify-write (pause) cycles. Enables MC RD/WR RQ pulse to trigger MC RD RQ pulse and MC RD/WR RS pulse to trigger MC WR RQ.
MC STOP	MC2	Flop set to inhibit normal exit from MC subroutine by any memory stop condition. Allows continue key to pulse MC RS T0.
MC STOP EN	MC2	Level. Allows MC STOP SET pulse to set MC STOP flop if doing single cycle or satisfied address stop condition.
MC SW COND	MC2	Level. True when ADDRESS CONDITION conditions are satisfied. Distinguishes between instruction fetch, data fetch, or write.

Table 1-3 (Cont)
KA10 Signal Glossary

Signal Name	Source Drawing	Description
MC WR	MC2	Write command flop. Produces MAIB MC WR and conditions actions occurring after ADR ACK is received.
MC WR RQ PULSE	MC1	Pulse triggered from instruction flow to start a write operation. Sets MC WR.
MC RST0-1	MC1	Final pulses of MC subroutine. Cause return to instruction flow depending on subroutine flop.
MI 0-35	MI	Memory indicator register. Displays data on console lights. Loaded by key functions (examine, deposit) or by program (DATAO PI).
MI PROG	MI	When set, prevents MI from automatically displaying contents of location addressed by console address switches. Preserves program display.
MI PROG DIS SW	MI	True when maintenance panel MI PROG DIS switch is on. Forces automatic display of location addressed by switches.
MIT0-1	MI	Pulses produced by references to a location addressed by the address switches. Will cause loading of MI from AR if MI PROG is zero. (So-called automatic display).
MPF1	BTMP	Fixed point multiply subroutine flop. Enables return to MPT2 from SCT4.
MPF2	BTMP	Multiply sign storage. Set if both operand signs negative. Used for fractional overflow test at MPT2.
MPT2-4	BTMP	Fixed point multiply execution time pulses.
MQ 0-35	MQ2	Multiplier-quotient register. Can be loaded from AD, and shifted left or right one place.
MQ 0 SHLT INP	ARMQ	Level. Provides input to MQ bit 0 for left shift operations shown on SCAF diagram.
MQ 0 SHRT INP	ARMQ	Level. Provides input to MQ bit 0 for right shift operations shown on SCAF diagram.
MQ 1 SHRT INP	ARMQ	Provides input to MQ bit 1 for right shift operations shown on SCAF diagram.
MQ 7 SHLT INP	ARMQ	Provides input to MQ bit 7 for left shift operations shown on SCAF diagram.
MQ 8 SHRT INP	ARMQ	Provides input to MQ bit 8 for right shift operations shown on SCAF diagram.

Table 1-3 (Cont)
KA10 Signal Glossary

Signal Name	Source Drawing	Description
MQ 9-35 = 0	MQ1	Level. True as stated. Used by normalize subroutine for making rounding and zero result decisions.
MQ 35 SHLT INP	ARMQ	Provides input to MQ bit 35 for left shift operations shown on SCAF diagram.
MR CLR, A, B	MR	"Master clear". (Mister Clear). Clears subroutine flops, SC, MQ, IR, sets adder enables for indexing, enables IR to memory bus, and generally prepares processor for fetching and executing the current instruction.
MR PWR CLR	MR	B-series clear pulses produced at a 500 kHz rate when powering up or down.
MR PWR CLR R	MR	R-series (400 ns) pulses at 500 kHz rate.
MR PWR CLR ENB	MR	A 5 second level occuring shortly after power turn-on and 100 ms after power turn-off. Enables 500 kHz pulse source for MR PWR CLR.
MR START, A, B	MR	A general system clear, more general than MR CLR. Resets peripheral devices as well as processor. Caused by PWR CLR, console RESET operation, and at start of readin operation.
MR START R	MR	R-series (400 ns) pulse produced by MR START.
MSF1	BTMP	Multiply subroutine-shift counter subroutine flop. Causes right shift of AR, MQ at SCT3 (ARC2, MQ1) and qualifies register connections (ARMQ). Also allows AD MD+ and AD MD- to be controlled by MQ 34 and 35.
MST0-1	BTMP	Multiply subroutine time pulses.
NLT0-4	NRNL	Pulses. "Normalize long time". Part of normalize return subroutine that determines exponent for second word in floating point long mode instructions.
NR ALL ZERO	NRNL	Level. True when floating point result is zero in both AR and MQ.
NR NORMAL	NRNL	Level. True when a floating result is normalized or if UFA op code in IR.
NR ROUND	NRNL	Level. True when data condition and op code specify rounding to take place. Permits NRT3 delayed to pulse NRT6.

Table 1-3 (Cont)
KA10 Signal Glossary

Signal Name	Source Drawing	Description
NR SH RT COND	NRNL	Level. True when a significant bit of result mantissa is in AR bit 8. Causes NRT10 to make one right shift.
NRF1	NRNL	Normalize return rounding control flop. Prevents rounding the same result more than once.
NRT0-7, 10, 99	NRNL	Normalize return subroutine pulses.
ODD 0-8	PN	True when PB bits 0-8 contain odd parity.
ODD 0-26	PN	True when PB bits 0-26 contain odd parity.
ODD 9-17	PN	True when PB bits 9-17 contain odd parity.
ODD 18-26	PN	True when PB bits 18-26 contain odd parity.
ODD 27-35	PN	True when PB bits 27-35 contain odd parity.
PB 0-35	PB	Parity buffer data bits. Loaded from memory bus. Drives parity computing network (PN).
PB PAR	PB	Parity buffer parity bit. May be set during a read. Is held clear during write to force PN to compute parity of ones in PB 0-35.
PC 18-35	PC2	Program counter register. Contents used to address memory to fetch instruction.
PC COND P	PC1	Level used by arithmetic compare or test (op 300-377) instructions. True when Equal, Not equal, or Always conditions are satisfied. Allows PC to be changed at ET0.
PC COND Q	PC1	Level used by arithmetic compare (op 300-317) instructions. True when Less than or Greater than conditions are met. Allows PC to increment at ET0.
PC COND R	PC1	Level used by arithmetic test (op 320-377) instructions. True when less than or greater than conditions are met. Allows PC to be changed at ET0.
PC SET (ET0)	PC1	Level. True to allow ET0 pulse to load PC from MA.
PC+1 (ET2)	PC1	Level. True to allow ET2 pulse to increment the PC.
PC+1 INH	PC1	Level. True to prevent FT9 pulse from incrementing PC.
PCLT+1	PC1	Pulse. Transfers increment network outputs to PC 18-26.
PCRT+1	PC1	Pulse. Transfers increment network outputs to PC 27-35.

Table 1-3 (Cont)
KA10 Signal Glossary

Signal Name	Source Drawing	Description
PI ACT	PI1	Priority interrupt system active. When zero, no interrupt requests will be recognized. When true, enables priority network at PI REQ 1 and PI OK 2.
PI CYC	PI1	Flop set during execution of PI location contents. Prevents interruption of instruction in that location, also inhibits PC incrementation. Sets EX PI SYNC to inhibit relocation.
PI DATA I/O	PI1	Level. DATAI or DATAO op code in IR. (Intent is second half of BLKI or BLKO).
PI ENC 32-34	PI1	Level. Octal to binary encoding of channel number whose PI REQ n is currently true. Used in MA control to generate address 40+2N or 40+2N+1.
PI HOLD	PI1	Level. When true allows PIHn flop to set for channel now being serviced. Allows PI OV and PI CYC to be cleared.
PI OV	PI1	Flop set during BLKI/BLKO instruction if left half of pointer overflows, but only during interrupt or key read in situations. Inhibits PI HOLD, PI RESTORE, causes IT0 to generate 40+2N+1 in MA.
PR REQ 1-7	PI2	Priority network "request granted" outputs. Only one can be true at a time (highest priority one, lowest number).
PI RESTORE	PI1	Level. When true allows the highest priority (lowest numbered) PI in progress flop (PIH) to be cleared.
PI RQ	PI1	Priority interrupt request. Alters instruction flow after IT0, BLTT3. Produced by any PI REQ n level but is inhibited by KEY PI INH (key execute) or PI CYC (1).
PIH 1-7	PI2	PI Hold register. (PI IN PROGRESS lights on console). PIHn (1) feeds back to priority network preventing PI REQ n through PI REQ 7 from being produced. Also clears PIRn.
PIO 1-7	PI2	PI On. Channel on/off switch or enable. PIOn must be a one to allow IOB PI RQn to be loaded into PIRn.
PIOK 2-7	PI2	Priority network functions. PIOKn must be true to allow PI REQ n to happen. PIOKn means there is nothing currently in progress or being requested for channels 1 through n-1.

Table 1-3 (Cont)
KA10 Signal Glossary

Signal Name	Source Drawing	Description
PIR 1-7	PI2	PI Request storage. Stores requests for enabled channels. PI bus strobed each core memory reference by MC RQ PULSE. Can also be set by CONO PI, to initiate interrupt from within program. Outputs go to priority network.
PN PAR EVEN	PN	Level. True for even parity in PB 0-35 and PB PAR. Used in MC subroutine (MC1).
PN PAR ODD	PN	Level. True for odd parity in PB 0-35 and PB PAR.
PR 18-25	PR	First protection register. Holds protection constant.
PRB 18-25	PR	Second protection register.
PRA ILL ADR	PR	Protection adder illegal address. True when MA 18-25 are greater than PR 18-25, or PRB 18-25 and memory protection is desired. Used in memory control (MC2).
RDI SEL 3-9	IR	Read in device selection switches. Located on maintenance panel.
RL 18-25	RL	First relocation register. Holds relocation constant.
RLA 18-25	RL	First relocation adder. Forms sum of MA 18-25 and RLA 18-25. Outputs may be used by MAI logic.
RLB 18-25	RL	Second relocation register.
RLC 18-25	RL	Second relocation adder, sum of MA 18-25 and RLB 18-25.
RUN	KEY3	Run flip-flop. When set, allows repetition of IT0-ST9 sequence. Clearing run causes a program to stop with ST9 of current instruction.
SAC = 0	S2	True when IR9-12 = 0000. Used by store cycle to inhibit storing result in AC zero for Self mode and skip instructions.
SAC INH	S2	Store AC inhibit. Prevents storage of AR in location addressed by FMA.
SAC2	S2	Store AC2. Causes store cycle to write MQ into location AC+1.
SAR ≠ BR	S2	Causes store cycle to write AR contents into (AC) and BR contents into (MA).
SC 0-8	SC	Shift counter register. Used to control shift count subroutine and for floating exponent calculation.

Table 1-3 (Cont)
KA10 Signal Glossary

Signal Name	Source Drawing	Description
SC 0-8 CLR or SET	SC	Outputs of shift counter incrementation network.
SC0 = AR0	SCC2	True when SC sign equals AR sign. Used by floating add to make AR contain operand with smaller exponent. (FAT3A).
SC DATA 0-8	SCAD	Outputs of a data multiplexer that supplies data to be arithmetically combined with SC by SCAD (shift count adder.)
SC FP SETUP	SCC2	Shift count pre-load for floating multiply (745_8) or divide (744_8).
SC MD SETUP	SCC2	Shift count pre-load for fixed point multiply or divide (735_8).
SC NEGATE SETUP	SCC1	Sets the SCAD controls to cause the negative of SC to appear at the SCAD outputs.
SC SBR (ET0)	SCSR	Level to allow ET0 to pulse SCT0 for certain instructions.
SC STOP	SCSR	When set, inhibits SCT1 pulse until continue key is set. Controlled by SC STOP.
SC STOP SW	SCSR	When maintenance panel switch is on, allows SCT0 to set SC STOP.
SC+1	SC	Pulse that transfers SC incrementing network outputs to SC during shift count subroutine.
SC+ EN	SCC1	Sets the SCAD controls to cause an addition of the SC and DATA.
SC- EN	SCC1	Sets the SCAD controls to cause the data to be subtracted from the SC. Result at SCAD outputs.
SCAD 0-8	SCAD	Shift counter adder. Performs arithmetic operations on SC contents and selected other data.
SCAD 200 EN	SCC1	When set, makes SC DATA equal 200_8.
SCAD 33 EN	SCC1	When set, makes SC DATA equal 033. (May be 032 if FDF3(1) during floating divide).
SCAD ALL DIS	SCC1	Sets the SCAD controls to cause SCAD outputs to be only a copy of SC.
SCAD AR 6-11 EN	SCC1	When set, makes SC DATA a copy of AR 6-11 contents. (Byte pointer size field).
SCAD BR EN	SCC1	When set, makes SC DATA a copy of BR0-8. (Floating point operand exponent).

Table 1-3 (Cont)
KA10 Signal Glossary

Signal Name	Source Drawing	Description
SCAD DATA 0	SCC1	When set, gates SC DATA true to SCAD B138's.
SCAD DATA 1	SCC1	When set, gates SC DATA false (complement) to SCAD B138's.
SCAD SC COMP	SCC1	When set, gates SCn(0) to SCADn. When cleared, gates SCN(1) to SCADn.
SCAD SC COMP SETUP	SCC1	Sets SCAD controls to make SCAD outputs the complement of SC contents.
SCAD SC+1 SETUP	SCC1	Sets SCAD controls to make SCAD output equal (SC) +1.
SCAD SC+BR SETUP	SCC1	Sets SCAD controls to make SCAD take sum of SC and BR 0-8.
SCAD SC-BR SETUP	SCC1	Sets SCAD controls to make SCAD take difference between SC and BR 0-8.
SCAD +1 EN	SCC1	When set, causes carry into SCAD 8.
SCE	S2	Store contents of E. Causes store cycle flow to write AR into (MA).
SCT0-4	SCSR	Shift count subroutine time pulses.
SF1	S1	Store cycle memory subroutine flop.
SF6	S1	Store cycle memory subroutine flop.
SF8	S1	Store cycle memory subroutine flop.
SR GO LEFT	SCSR	Level. True for shift-rotate instructions with positive effective address. Enables SCT3 to produce AR and MQ shift left pulses.
SR GO RIGHT	SCSR	Level. True for shift-rotate instructions with negative effective address. Enables SCT3 to produce AR and MQ shift right pulses.
SR OP	SCSR	Level. True for shift or rotate instructions.
SRT1	SCSR	Shift-rotate time pulse. Used to negate shift counter for left shifts and rotates.
ST INH	S2	Store inhibit. When true prevents ET0 or ET2 from pulsing ST1. Used by instructions which have special execution pulse chains.
ST0-9	S1	Store cycle pulses.

Pages 19 through 22 will accommodate supplemental data to be furnished at a later date.

MASTER DRAWING LIST

DWG. NO.	REV. LET.	NO. OF SHEETS	TITLE
D-UA-KA10-A-0		3	KA10 ASSEMBLY
A-PL-KA10-A-0		8	KA10 ASSEMBLY PARTS LIST
D-BS-KA10-0-AD1	A	1	ADDER CONTROL FLIP-FLOPS
D-BS-KA10-0-AD2	A	1	ADDER CONTROL
D-BS-KA10-0-AD3		1	ADDER LEFT HALF
D-BS-KA10-0-AD4		1	ADDER RIGHT HALF
D-BS-KA10-0-AR1		1	AR REGISTER
D-BS-KA10-0-AR2		1	AR REGISTER
D-BS-KA10-0-AR3		1	AR REGISTER
D-BS-KA10-0-AR4		1	AR REGISTER
D-BS-KA10-0-ARC1	B	1	AR CONTROL PULSE
D-BS-KA10-0-ARC2		1	AR CONTROL PULSE
D-BS-KA10-0-ARC3	A	1	AR CONTROL PULSE
D-BS-KA10-0-ARF		1	ARITHMETIC FLAGS
D-BS-KA10-0-ARI		1	AR INPUTS
D-BS-KA10-0-ARMQ		1	AR & MQ SHIFT CONNECTIONS
D-BS-KA10-0-AS		1	ADDRESS SWITCH COMPARATORS
D-BS-KA10-0-BR1		1	BR CONTROL
D-BS-KA10-0-BR2		1	BR REGISTER
D-BS-KA10-0-BTMP		1	BLOCK TRANSFER AND MULTIPLY

A-ML-KA10-A-0 KA10 Processor 60 Hz 115V (Sheet 1)

MASTER DRAWING LIST

DWG. NO.	REV. LET.	NO. OF SHEETS	TITLE
D-BS-KA10-0-BYTE		1	BYTE INSTRUCTION FIRST PART
D-BS-KA10-0-CPA		1	ARITHMETIC PROCESSOR STATUS REG
D-BS-KA10-0-DBLB		1	BYTE DEPOSIT AND LOAD
D-BS-KA10-0-DSDV	A	1	DIVIDE SUBROUTINE & FIXED DIVIDE
D-BS-KA10-0-E	A	1	EXECUTION CYCLE
D-BS-KA10-0-EX	A	1	EXECUTIVE CONTROL
D-BS-KA10-0-F1		1	FETCH CYCLE TIME PULSE
D-BS-KA10-0-F2		1	FETCH CYCLE LEVELS
D-BS-KA10-0-FA		1	FLOATING ADD INSTRUCTION
D-BS-KA10-0-FDV		1	FLOATING DIVIDE
D-BS-KA10-0-FE		1	FLOATING EXPONENT REGISTER & CONTROL
D-BS-KA10-0-FM		1	FAST MEMORY
D-BS-KA10-0-FMA	A	1	FAST MEMORY ADDRESS
D-BS-KA10-0-FPFM		1	FP EXP CALC FLOATING MULTIPLY
D-BS-KA10-0-HWT		1	HALF WORD TRANSFER
D-BS-KA10-0-IA		1	INSTRUCTION & ADDRESS CYCLES
D-BS-KA10-0-IOB1		1	I/O BUS (0-17)
D-BS-KA10-0-IOB2		1	I/O BUS (18-35)

A-ML-KA10-A-0 KA10 Processor 60 Hz 115V (Sheet 2)

MASTER DRAWING LIST

DWG. NO.	REV. LET.	NO. OF SHEETS	TITLE
D-BS-KA10-0- IOBC		1	I/O BUS CONTROL & I/O SELECTION
D-BS-KA10-0-IOBI	B	1	IOB INPUTS
D-BS-KA10-0-IOT	A	1	IN-OUT TRANSFER CONTROL
D-BS-KA10-0-IR		1	INSTRUCTION REGISTER
D-BS-KA10-0-IR1	A	1	IR DECODING
D-BS-KA10-0-IR2	A	1	IR DECODING
D-BS-KA10-0-IR3		1	IR DECODING
D-BS-KA10-0-JFF0	A	1	JFF0 INTRUCTION CONTROL
D-BS-KA10-0-KEY1		1	KEY & SWITCHES CONTROLS
D-BS-KA10-0-KEY2		1	KEY & SWITCHES CONTROLS
D-BS-KA10-0-KEY3		1	KEY & SWITCHES CONTROLS
D-BS-KA10-0-MA1	A	1	MA CONTROL
D-BS-KA10-0-MA2		1	MA REGISTER
D-BS-KA10-0-MAI	A	1	MEMORY ADDRESS INTERFACE
D-BS-KA10-0-MBDI		1	MEMORY BUS DATA INTERFACE
D-BS-KA10-0-MC1		1	MEMORY CONTROL
D-BS-KA10-0-MC2		1	MEMORY CONTROL
D-BS-KA10-0-MI		1	MEMORY INDICATOR
D-BS-KA10-0-MQ1	A	1	MQ CONTROL
D-BS-KA10-0-MQ2	A	1	MULTIPLIER QUOTIENT (MQ 0-17)

MASTER DRAWING LIST

DWG. NO.	REV. LET.	NO. OF SHEETS	TITLE
D-BS-KA10-0-MQ3	A	1	MULTIPLIER QUOTIENT (MQ18-35)
D-BS-KA10-0-MR		1	MASTER CLEAR & POWER CLEAR
D-BS-KA10-0-NRNL		1	NORMALIZE RETURN & NR LONG
D-BS-KA10-0-PB		1	PARITY BUFFER REGISTER
D-BS-KA10-0-PC1	A	1	PROGRAM COUNTER CONTROL
D-BS-KA10-0-PC2		1	PROGRAM COUNTER REGISTER
D-BS-KA10-0-PI1		1	PI CONTROL
D-BS-KA10-0-PI2		1	PRIORITY INTERRUPT PIH,PIR,PIO
D-BS-KA10-0-PN		1	PARITY NETWORK
D-BS-KA10-0-PR	A	1	PROTECT REGISTER
D-BS-KA10-0-PTP1		1	PAPER TAPE PUNCH CONTROL 1
D-BS-KA10-0-PTP2	A	1	PAPER TAPE PUNCH CONTROL 2
D-BS-KA10-0-PTR1	B	1	PAPER TAPE READER CONTROL
D-BS-KA10-0-PTR2		1	PAPER TAPE READER CONTROL
D-BS-KA10-0-PTR3		1	PAPER TAPE READER CONTROL
D-BS-KA10-0-RL	A	1	RELOCATE REGISTER
D-BS-KA10-0-S1	A	1	STORE CYCLE TIME PULSES
D-BS-KA10-0-S2	A	1	STORE CYCLE LEVELS

MASTER DRAWING LIST

DWG. NO.	REV. LET.	NO. OF SHEETS	TITLE
D-BS-KA10-0-SC		1	SHIFT COUNT REGISTER
D-BS-KA10-0-SCAD		1	SHIFT COUNT ADDER
D-BS-KA10-0-SCC1		1	SHIFT COUNTER CONTROL
D-BS-KA10-0-SCC2		1	SHIFT COUNTER CONTROL
D-BS-KA10-0-SCSR	A	1	SHIFT & COUNT SUBROUTINE SHIFT INST
D-BS-KA10-0-TTY1		1	TELETYPE CONTROL
D-BS-KA10-0-TTY2	C	1	TELETYPE CONTROL
D-FD-KA10-0-BIF1		1	BASIC INSTRUCTION FLOW
D-FD-KA10-0-BIF2		1	BASIC INSTRUCTION FLOW
D-FD-KA10-0-BIF3		1	BASIC INSTRUCTION FLOW
D-FD-KA10-0-BIOR		1	BASIC I-O REGISTERS
D-FD-KA10-0-BYTF		1	BYTE INSTRUCTION FLOW
D-FD-KA10-0-DIVF		1	FIXED POINT DIVIDE & SUBROUTINE
D-FD-KA10-0-ESC	A	1	EXECUTE AND STORE CYCLE
D-FD-KA10-0-FAF		1	FLOATING ADD, SUB, UFA FLOW
D-FD-KA10-0-FC		1	FETCH CYCLE FLOW

MASTER DRAWING LIST

DWG. NO.	REV. LET.	NO. OF SHEETS	TITLE
D-FD-KA10-0-FDVF		1	FLOATING DIVIDE
D-FD-KA10-0-FPMC		1	FP EXP CALCULATE SUBR FM & MPY SUBR
D-FD-KA10-0-FSDN		1	FLOATING SCALE & DBL FLOATING NEGATE
D-FD-KA10-0-IAC		1	INSTRUCTION & ADDRESS CYCLES
D-FD-KA10-0-KO	A	1	KEY OPERATIONS FLOW DIAGRAM
D-FD-KA10-0-MCFM	A	1	MEMORY CONTROL & FAST MEMORY FLOW
D-FD-KA10-0-NRF		1	NORMALIZE RETURN SUBROUTINE
D-FD-KA10-0-SCAF		1	SHIFT COUNT ACTION FLOW
D-FD-KA10-0-SMF	A	1	SHIFT & MUL & JFFO FLOW
D-FD-KA10-0-IOTF		1	IN-OUT TRANSFER CONTROL FLOW
D-FD-KA10-0-REG		1	KA10 REGISTER INTER-CONNECTIONS
D-FD-KA10-0-RIMF		1	READ-IN FUNCTION ISOLATED FLOW
D-FD-KA10-0-SCBT		1	SHIFT COUNT SUBROUTINE &BLT FLOW
D-IC-KA10-0-ICSC1	A	1	INDICATOR & CONSOLE SW CONNECTIONS
D-IC-KA10-0-ICSC2	A	1	INDICATOR & CONSOLE SW CONNECTIONS
D-CL-KA10-0-IBC1	A	1	INTER-BAY CABLES
D-CL-KA10-0-IBC2	A	1	INTER - BAY CABLES

MASTER DRAWING LIST

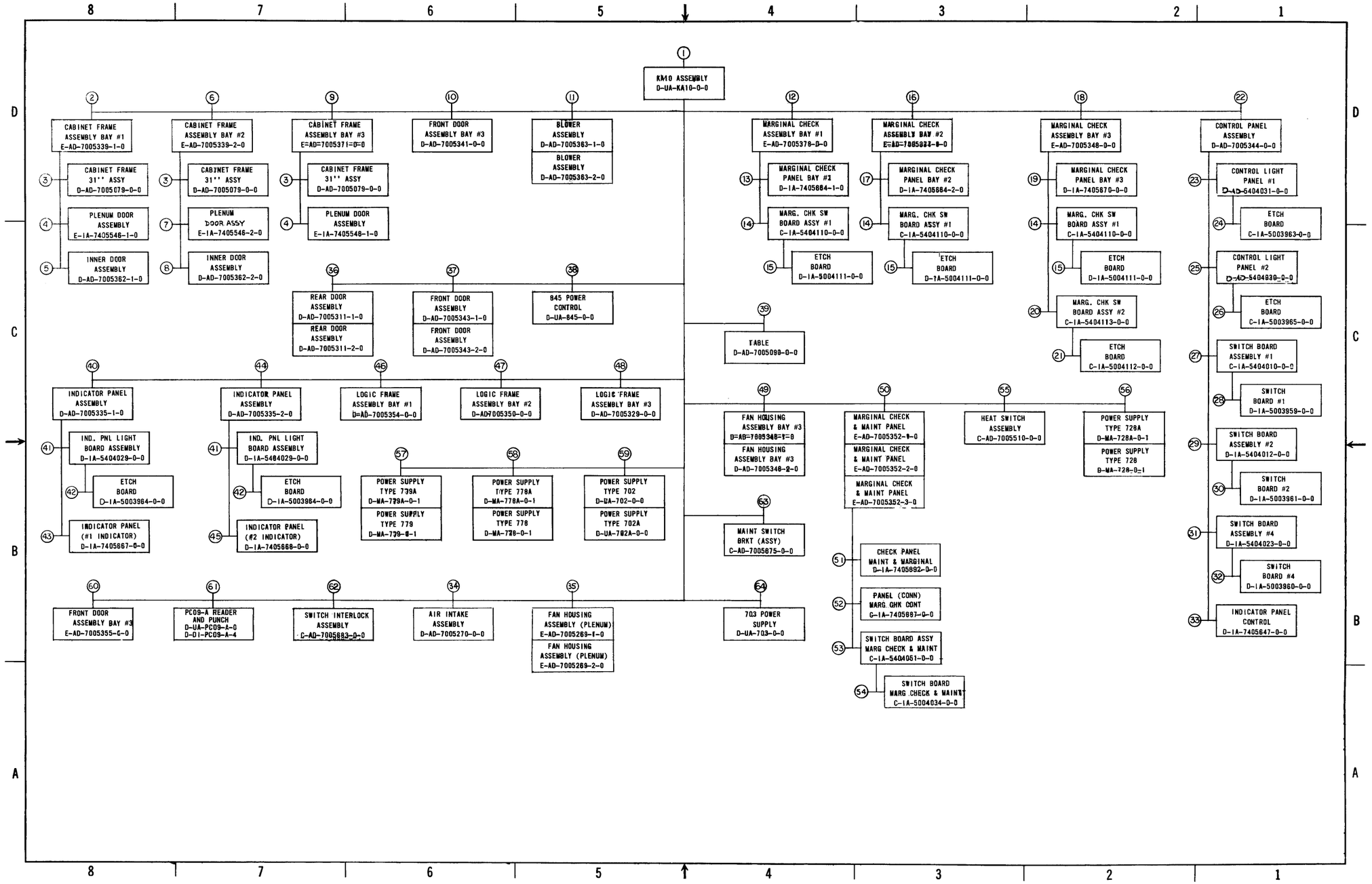
DWG. NO.	REV. LET.	NO. OF SHEETS	TITLE
D-MU-KA10-0-1A1D		1	MODULE UTILIZATION PANELS 1A-1D
D-MU-KA10-0-1E1J	A	1	MODULE UTILIZATION PANELS 1E-1J
D-MU-KA10-0-1K1N	A	1	MODULE UTILIZATION PANELS 1K-1N
D-MU-KA10-0-1P1T	A	1	MODULE UTILIZATION PANELS 1P-1T
D-MU-KA10-0-2A2D		1	MODULE UTILIZATION PANELS 2A-2D
D-MU-KA10-0-2E2J		1	MODULE UTILIZATION PANELS 2E-2J
D-MU-KA10-0-2K2N	C	1	MODULE UTILIZATION PANELS 2K-2N
D-MU-KA10-0-2P2T	A	1	MODULE UTILIZATION PANELS 2P-2T
D-MU-KA10-0-3A3D	A	1	MODULE UTILIZATION PANELS 3A-3D
D-MU-KA10-0-3E3F	B	1	MODULE UTILIZATION PANELS 3E-3F
A-PL-KA10-0-MC	A	6	MODULE COUNT
A-CP-KA10-0-CP	C	10	EXTERNAL COMPONENT LIST
D-CL-KA10-0-TERM	C	1	PULSE & LEVEL TERMINATIONS BAY 1 & 2
D-IC-KA10-0-1	F	3	DC POWER WIRING
D-IC-KA10-0-2	C	3	AC POWER WIRING
D-AD-7005607-0-0	B		CABLE SET
D-DI-KA10-0-3		4	DRAWING INDEX LIST
K-WL-KA10-0-4	F		WIRE LIST KA10
A-WL-KA10-0-GW		1	TTY SOCKET WIRING OF KA10
A-WL-KA10-0-TWP1	B	17	TWP LIST KA10 BAY 1

A-ML-KA10-A-0 KA10 Processor 60 Hz 115V (Sheet 7)

MASTER DRAWING LIST

DWG. NO.	REV. LET.	NO. OF SHEETS	TITLE
A-WL-KA10-0-TWP2	B	22	TWP LIST KA10 BAY 2
A-ML-KM10-0		1	FAST MEMORY
A-ML-KE10-0		1	EXTENDED INSTRUCTION SET
A-ML-KT10-0		1	TIME SHARING OPTION

A-ML-KA10-A-0 KA10 Processor 60 Hz 115V (Sheet 8)



D-DI-KA10-0-3 Drawing Index List KA10 (Sheet 1)

FIND NO.	MECHANICAL DESCRIPTION	PART NO.	DEPT USAGE PROD	CUST	F/C
1	KA10 ASSEMBLY	D-UA-KA10-0-0			
	KA10 ASSEMBLY (P.L.)	A-PL-KA10-0-0			
	END PANEL ASSEMBLY	E-IA-7405092-0-0			
	PANEL, BLANK FILLER	C-IA-7498083-0-0			
	BRACKET, SUPPORT	C-MD-7406336-0-0			
	CABLE MARG CHK RMTE CONTROL	C-UA-BC10B-15-C			
	CABLE MARG CHK RMTE CONTROL	C-UA-BC10B-3-0			
	SHORTING PLUG	B-IA-7005498-0-0			
	CABLE MARG CHK RMTE CONTROL	C-UA-BC10B-5-0			
	CABLE MARG CHK RMTE CONTROL	C-UA-BC10B-7-0			
	CABLE, POWER	C-IA-7005514-0-0			
	SLIDE BRACE	C-MD-7406268-3C			
	CHASSIS TRACK (LEFT)	D-SC-3404701-1-0			
	CHASSIS TRACK (RIGHT)	D-SC-3404701-2-0			
	STANDARD CHASSIS 7402037	B-5111			
	STANDARD CHASSIS 7402036	B-5111			
	STANDARD CHASSIS 7402038	B-5111			
	PROTECTION STRIP	D-01454			
	CABLE SET	D-AD-7005607-0-0			
	CTR CLIP 7403106	B-MD-01486			
	CABLE ASSEMBLY POWER CLOCK	C-AD-7005604-0-0			
	BRACKET, SHIPPING	B-IA-7406001-0-0			
	SUPPORT, CABLE DUCT	C-IA-7406406-0-0			
	CABLE, DUCT	C-MD-7406409-0-0			
2	CABINET FRAME ASSEMBLY BAY #1	E-AD-7005339-1-0			
	CAB FRAME ASSY BAY #1 (P.L.)	A-PL-7005339-0-0			
	SUPPORT-BLOWER VERTICAL #2	C-IA-7405701-1-0			
	FILLER PANEL-INTAKE	C-MD-7405641-1-0			
	SUPPORT-INNER DOOR-LOWER	D-IA-7405723-0-0			
	"E" FRAME	D-IA-7405688-0-0			
	BRACKET HINGE PIN	B-MD-7405680-0-0			
	AIR BAFFLE, "E" FRAME	D-MD-7405724-0-0			
	SUPPORT-INNER DOOR-UPPER	D-IA-7405591-1-0			
	PANEL BLANK, PLENUM DOOR	D-IA-7405699-0-0			
	PAD, SUPPORT LOGIC FRAME	B-IA-7405617-0-0			
	STRIKER PLATE	B-MD-7405643-0-0			
	SUPPORT-BLOWER VERTICAL #1	D-IA-7405703-0-0			
	STRIKER, LATCH PIN	C-MD-7405618-0-0			
	FILLER	C-MD-7405594-0-0			
	STRIP, SEAL CABINET(7403230)	D-MD-20406-1			
3	CABINET FRAME ASSY 31"	D-AD-7005079-0-0			
	CABINET FRAME ASSY 31" (P.L.)	A-PL-7005079-0-0			
	CABINET FRAME 31"	E-IA-7405091-0-0			
	TRIM STRIP, BOTTOM	D-MD-7405095-0-0			
	TRIM STRIP, TOP	C-MD-7405088-0-0			
	SCREEN FAN	C-MD-7405087-(-0			
4	PLENUM DOOR ASSY	E-IA-7405546-1-0			
	PLENUM DOOR LATCH SPRING	C-MD-20407-3			
	PLENUM DOOR LATCH PIN	C-MD-20407-4			
5	INNER DOOR ASSY	D-AD-7005382-1-0			
	INNER DOOR ASSY (P.L.)	A-PL-7005362-0-0			
	DOOR, INNER	D-IA-7405678-0-0			
	HINGE PIN, TOP	B-MD-20400-7			
	DOOR SPACER, BOTTOM	A-MD-7405312-0-0			
	HINGE PIN, BOTTOM	B-MD-20400-8			
	LATCH PIN, LOGIC DOOR	B-MD-7405598-0-0			
	DOOR COVER, FOAM	B-MD-7405777-0-0			
6	CABINET FRAME ASSEMBLY BAY #2	E-AD-7005339-2-0			
	CAB FRAME ASSY BAY #2 (P.L.)	A-PL-7005339-0-0			
	SUPPORT-BLOWER VERTICAL #2	C-IA-7405701-2-0			
	FILLER PANEL-INTAKE	C-MD-7405641-2-0			
	SUPPORT-INNER DOOR-LOWER	D-IA-7405723-0-0			
	"E" FRAME	D-IA-7405688-0-0			
	BRACKET, HINGE PIN	B-MD-7405680-0-0			
	AIR BAFFLE, "E" FRAME	D-MD-7405724-0-0			
	SUPPORT-INNER DOOR-UPPER	D-IA-7405591-2-0			
	PANEL BLANK, PLENUM DOOR	D-IA-7405699-0-0			
	PAD, SUPPORT LOGIC FRAME	B-IA-7405617-0-0			
	STRIKER PLATE	B-MD-7405643-0-0			
	SUPPORT, BLOWER VERTICAL #1	D-IA-7405703-0-0			
	STRIKER; LATCH PIN	C-MD-7405618-0-0			
	FILLER	C-MD-7405594-0-0			
	STRIP, SEAL CABINET(7403230)	D-MD-20406-1			
7	PLENUM DOOR ASSY	E-IA-7405546-2-0			
	PLENUM DOOR LATCH SPRING	C-MD-20407-3			
	PLENUM DOOR LATCH PIN	C-MD-20407-4			

FIND NO.	MECHANICAL DESCRIPTION	PART NO.	DEPT USAGE PROD	CUST	F/C
8	INNER DOOR ASSEMBLY	D-AD-7005362-2-0			
	INNER DOOR ASSEMBLY (P.L.)	A-PL-7005362-0-0			
	DOOR, INNER	D-IA-7405678-0-0			
	HINGE PIN, TOP	B-MD-20400-7			
	DOOR SPACER, BOTTOM	A-MD-7405312-0-0			
	HINGE PIN, BOTTOM	B-MD-20400-8			
	LATCH PIN, LOGIC DOOR	B-MD-7405598-0-0			
	DOOR COVER, FOAM	B-MD-7405777-0-0			
9	CABINET FRAME ASSEMBLY BAY #3	E-AD-7005371-0-0			
	CAB FRAME ASSY BAY #3 (P.L.)	A-PL-7005371-0-0			
	TRIM STRIP, SHORT	A-MD-7405675-0-0			
	TRIM STRIP, LONG	B-MD-7405674-0-0			
	STRIKER PLATE	B-MD-7405643-0-0			
	SPACER	B-MD-7405545-0-0			
	PIVOT POST	C-IA-7405544-0-0			
	LOWER DOOR SUPPORT	C-MD-7405440-0-0			
	TABLE SUPPORT	B-MD-5-0-1-17			
	HORIZONTAL SUPPORT	C-MD-7405160-0-0			
	VERTICAL PANEL BRACKET	C-MD-7405702-0-0			
	STOP DOOR	A-MD-7405700-0-0			
	VERTICAL SUPPORT	D-IA-7405721-0-0			
	SPACER CABINET	C-MD-7405343-0-0			
	FILLER	D-IA-7405347-0-0			
	CENTER CLIP	D-IA-7405344-0-0			
	PANEL BLANK, PLENUM DOOR	D-MD-7405699-0-0			
	TABLE SUPPORT BAR	C-IA-7405672-0-0			
	TABLE SUPPORT	B-MD-7405163-0-0			
	LATCH PLATE	A-MD-7405686-0-0			
	PLATE, STRIKER	C-MD-7405618-0-0			
10	FRONT DOOR ASSEMBLY BAY #3	D-AD-7005347-0-0			
	FRONT DOOR ASSY BAY #3 (P.L.)	A-PL-7005347-0-0			
	FRONT DOOR	D-IA-7405704-0-0			
	HINGE PIN, TOP	B-MD-20400-7			
	DOOR SPACER, BOTTOM	A-MD-7405312-0-0			
	HINGE PIN, BOTTOM	B-MD-20400-8			
	KICK PLATE	C-MD-7405677-0-0			
11	BLOWER ASSY	D-AD-7005363-1-0			
	BLOWER ASSY	D-AD-7005363-2-0			
	BLOWER ASSY (P.L.)	A-PL-7005363-0-0			
	BLOWER HOUSING	D-IA-7405728-0-0			
	COVER TOP, BLOWER	D-IA-7405774-0-0			
	FILTER, BLOWER	C-SC-3405433-0-0			
	COVER BOTTOM, BLOWER	D-IA-7405732-0-0			
	BAFFLE, BLOWER	D-IA-7405778-0-0			
	EXTENTION CORD, REWORK	B-IA-7405470-0-0			
	BLOWER EASTERN	D-SC-3405463-0-0			
12	MARGINAL CHECK ASSEMBLY BAY #1	E-AD-7005378-0-0			
	MARG CHK ASSY BAY #1 (P.L.)	A-PL-7005378-0-0			
	PLATE CONN	C-MD-7405662-0-0			
13	PANEL, MARGINAL CHECK, BAY #1	D-IA-7405664-1-0			
14	MARG CHECK SW BOARD ASSY #1	C-IA-5404110-0-0			
	ETCH BOARD	D-IA-5004111-0-0			
15	ETCH BOARD	D-IA-5004111-0-0			
	ETCH PATTERN	PC-5404110-0-1			
	FIRST PUNCH FLIP CHIP MODULE (BLANK)	D-MD-1402230-0-0			
16	MARGINAL CHECK ASSEMBLY BAY #2	E-AD-7005377-0-0			
	MARG CHK ASSY BAY #2 (P.L.)	A-PL-7005377-0-0			
	PLATE CONN	C-MD-7405662-0-0			
17	PANEL, MARGINAL CHECK, BAY #2	D-IA-7405664-2-0			
18	MARGINAL CHECK ASSEMBLY BAY #3	E-AD-7005348-0-0			
	MARG CHK ASSY BAY #3 (P.L.)	A-PL-7005348-0-0			
	PLATE LATCH LIMIT	A-MD-7405773-0-0			
	PANEL OUTLET	B-MD-7405671-0-0			
	CONN PLATE	C-MD-7405662-0-0			
	COVER, PROTECTION	B-MD-7405897-0-0			

FIND NO.	MECHANICAL DESCRIPTION	PART NO.	DEPT USAGE PROD	CUST	F/C
19	PANEL, MARGINAL CHECK, BAY #3	D-IA-7405670-0-0			
	SILK SCREEN	C-SS-7405775-0-0			
20	MARG CHECK SW BOARD ASSY #2	B-IA-5404113-0-0			
21	ETCH BOARD	D-IA-5004112-0-0			
	ETCH PATTERN	PC-5404113-0-1			
	FIRST PUNCH FLIP CHIP MOD, PLAIN	D-MD-1402230-(-0			
22	CONTROL PANEL ASSEMBLY	D-AD-7005344-0-0			
	CONTROL PANEL ASSY (P.L.)	A-PL-7005344-0-0			
	CASTING, REWORK	E-MD-7405676-0-0			
	GLASS SUPPORT	E-IA-7405638-0-0			
	RETAINER,, GLASS SUPPORT	B-MD-7405684-0-0			
	BRACKET, MTG CONSOLE	C-MD-7405673-1-0			
	BRACKET, MTG CONSOLE	C-MD-7405673-2-0			
23	CONTROL PANEL LIGHT BOARD ASSY #1	D-AD-5404031-0-0			
	18 PIN RECEPTACLE, REWORK	C-IA-5503954-0-0			
24	ETCH BOARD	C-IA-5003963-(-0			
	PRINTED CIRCUIT LAYOUT	PC-5404031			
	FIRST PUNCH FLIP CHIP MOD, BLANK	D-MD-1402230-0-0			
25	CONTROL PANEL LIGHT BOARD ASSY #2	D-AD-5404030-0-0			
	18 PIN RECEPTACLE, REWORK	C-IA-5503954-0-0			
26	ETCH BOARD	C-IA-5003965-0-0			
	PRINTED CIRCUIT LAYOUT	PC-5404030			
	FIRST PUNCH FLIP CHIP MOD, BLANK	D-MD-1402230-0-0			
27	SWITCH BOARD ASSEMBLY #1	C-IA-5404010-0-0			
	SPACER BAR	B-MD-7405656-1-0			
	18 PIN CONN, REWORK	B-MD-5503630-0-0			
	ROCKER SWITCH RS-50-FB-PC(CHALK BLU)	C-AD-5404331-1-0			
	ROCKER SWITCH RS-50-FB-PC(WEG WD GRN)	C-AD-5404331-3-0			
28	SWITCH BOARD #1	D-IA-5003959-0-0			
	ETCH PATTERN	PC-5003959-0-1			
	BOARD, GLASS EPOXY, BLANK	D-MD-1402671-0-0			
29	SWITCH BOARD #2 ASSEMBLY	D-IA-5404012-0-0			
	SPACER BAR	B-MD-7405656-2-0			
	SPACER BAR #2	B-MD-7405655-0-0			
	SWITCH ROCKER	C-AD-5404331-2-0			
	SWITCH ROCKER	C-AD-5404331-1-0			
	18 PIN CONN, REWORK	B-MD-5503630-0-0			
	SWITCH ROCKER	C-AD-5404413-1-0			
	SWITCH ROCKER	C-AD-5404413-3-0			
30	SWITCH BOARD #2	D-IA-5003961-0-0			
	ETCH PATTERN	PC-5003961			
	FIRST PUNCH FLIP CHIP, BLANK	D-MD-1402671-0-0			
31	SWITCH BOARD ASSEMBLY #4	D-IA-5404023-0-0			
	SWITCH ROCKER	C-AD-5404331-3-0			
	SWITCH ROCKER	C-AD-5404331-1-0			
	SPACER BAR	B-MD-7405833-0-0			
	18 PIN CONN, REWORK	B-MD-5503630-0-0			
	SWITCH ROCKER	C-AD-5404331-2-0			
32	SWITCH BOARD #4	D-IA-5003960-0-0			
	ETCH PATTERN	PC-5003960-0-1			
	BOARD, GLASS EPOXY (BLANK)	D-MD-1402671-0-0			
33	INDICATOR PANEL CONTROL	D-IA-7405647-0-0			
	SILK SCREEN (CHK BLU) STEP #4(FS)	D-SS-7405467-0-0			
	SILK SCREEN (GRN) STEP #3 (FS)	D-SS-7405466-0-0			
	SILK SCREEN (BLU) STEP #2 (FS)	D-SS-7405465-0-0			
	SILK SCREEN (GRY) STEP #1 (FS)	D-SS-7405464-0-0			
	SILK SCREEN (BLK) (RS)	D-SS-7405645-0-0			

FIND NO.	MECHANICAL DESCRIPTION	PART NO.	DEPT USAGE PROD	CUST	F/C
34	AIR INTAKE ASSEMBLY	D-AD-7005270-0-0			
	AIR INTAKE ASSY (P.L.)	A-PL-7005270-0-0			
	BEZEL REWORK, BOTTOM	D-MD-7405635-0-0			
	GRILL, BEZEL	B-MD-7405646-0-0			
	BEZEL REWORK, TOP	D-MD-7405636-0-0			
	HINGE, REWORK	C-MD-7405620-0-0			
	STRIKER PLATE	A-MD-7405640-0-0			
	GRILL RETAINER #1	C-MD-7406163-0-0			
	GRILL RETAINER #2	C-MD-7406164-0-0			
35	FAN HOUSING ASSEMBLY, PLENUM	E-AD-7005269-1-0			
	FAN HOUSING ASSEMBLY, PLENUM	E-AD-7005269-2-0			
	FAN HOUSING ASSY, PLENUM (P.L.)	A-PL-7005269-0-0			
	FAN HOUSING, PLENUM	D-MD-7405637-0-0			
	EXTENTION CORD,REWORK	B-IA-7405470-0-0			
	FAN SCREEN	C-MD-7404981-0-0			
	PROTECTION COVER, 4 TERM	B-MD-7404721-0-0			
36	REAR DOOR ASSEMBLY	D-AD-7005311-1-0			
	REAR DOOR ASSEMBLY	D-AD-7005311-2-0			
	REAR DOOR ASSY (P.L.)	A-PL-7005311-0-0			
	REAR DOOR	D-IA-7405624-0-0			
	HINGE PIN, TOP	B-MD-20400-7			
	DOOR SPACER, BOTTOM	A-MD-7405312-0-0			
	HINGE PIN, BOTTOM	B-MD-20400-8			
37	FRONT DOOR ASSEMBLY	D-AD-7005343-1-0			
	FRONT DOOR ASSEMBLY	A-AD-7005343-2-0			
	FRONT DOOR ASSY (P.L.)	A-PL-7005343-0-0			
	FRONT DOOR	D-IA-7405705-0-0			
	HINGE PIN, TOP	B-MD-20400-7			
	HINGE SLIDE REWORK	B-MD-7405955-0-0			
	DOOR SPACER, BOTTOM	A-MD-7405312-0-0			
	HINGE PIN, BOTTOM	B-MD-20400-8			
	BRACKET, MAGNET MTG	B-MD-7405710-0-0			
38	845 POWER CONTROL	D-UA-845-0-0			
	845 POWER CONTROL (P.L.)	A-PL-845-0-0			
39	TABLE	D-0A-7005090-0-0			
	TABLE (P.L.)	A-PL-7005090-0-0			
	TABLE TOP	D-IA-7405353-0-0			
	TABLE FRAME	D-IA-7405189-0-0			
40	INDICATOR PANEL ASSEMBLY	D-AD-7005335-1-0			
	INDICATOR PANEL ASSY (P.L.)	A-PL-7005335-0-0			
	BEZEL, INDICATOR-REWORK	D-MD-7405533-0-0			
	SUPPORT GLASS	D-IA-7405771-0-0			
	MOUNT, INDICATOR PANEL	B-MD-7405690-0-0			
41	INDICATOR PANEL LIGHT BOARD ASSY	D-AD-5404029-0-0			
	18 PIN RECEPTACLE	B-MD-5503954-0-0			
42	ETCH BOARD	D-IA-5003964-0-0			
	PRINTED CIRCUIT LAYOUT	PC-5404029			
	FIRST PUNCH FLIP CHIP MOD,BLANK	1402230-0-0			
43	INDICATOR PANEL (INDICATOR #1)	D-IA-7405667-0-0			
	SILK SCREEN (GRY) (FS)	D-SS-7405587-0-0			
	SILK SCREEN (BLK) (RS)	D-SS-7405598-0-0			
44	INDICATOR PANEL ASSEMBLY	D-AD-7005335-2-0			
	INDICATOR PANEL ASSY (P.L.)	A-PL-7005335-(-0			
	BEZEL INDICATOR-REWORK	D-MD-7405533-0-0			
	SUPPORT GLASS	D-IA-7405771-0-0			
	MOUNT, INDICATOR PANEL	B-MD-7405690-0-0			
45	INDICATOR PANEL (INDICATOR #2)	D-IA-7405663-0-0			
	SILK SCREEN (BLK) (RS)	D-SS-7405588-0-0			
	SILK SCREEN (GRY) (FS)	D-SS-7405589-0-0			

D-DI-KA10-0-3 Drawing Index List KA10 (Sheet 2)

FIND NO.	MECHANICAL DESCRIPTION	PART NO.	DEPT USAGE PROD	CUST	F/C
46	LOGIC FRAME ASSEMBLY BAY #1	D-AD-7005354-0-0			
	LOGIC FRAME ASSY BAY #1 (P.L.)	A-PL-7005354-0-0			
	LOGIC FRAME	D-IA-7405584-0-0			
	144 PIN CONNECTOR BLK	D-MD-100095			
	MTG BAR	D-IA-7405543-1-0			
	MTG BAR	D-IA-7405543-2-0			
	SCOTCHCAL (CLR BACKGND, WHT LTR)	A-SS-7406201-0-0			
47	LOGIC FRAME ASSEMBLY BAY #2	D-AD-7005350-0-0			
	LOGIC FRAME ASSY BAY #2 (P.L.)	A-PL-7005350-0-0			
	LOGIC FRAME	D-IA-7405584-C-0			
	144 PIN CONNECTOR BLK	D-MD-10095			
	MTG BAR	D-IA-7405543-1-0			
	MTG BAR	D-IA-7405543-2-0			
	SCOTCHCAL (CLR BACKGND, WHT LTR)	A-SS-7406200-0-0			
48	LOGIC FRAME ASSEMBLY BAY #3	D-AD-7005329-0-0			
	LOGIC FRAME ASSY BAY #3 (P.L.)	A-PL-7005329-0-0			
	LOGIC FRAME	D-IA-7405317-0-0			
	144 PIN CONNECTOR BLOCK	D-MD-100095			
	MTG BAR	D-MD-7405543-2-0			
	MTG BAR	D-MD-7405543-1-0			
	SCOTCHCAL (CLR BACKGND, WHT LTR)	A-SS-7406199-0-0			
49	FAN HOUSING ASSEMBLY BAY #3	D-AD-7005346-1-0			
	FAN HOUSING ASSEMBLY BAY #3	D-AD-7005346-2-0			
	FAN HOUSING ASSY BAY #3 (P.L.)	A-PL-7005346-0-0			
	FAN HOUSING, LOGIC DOOR	E-IA-7405661-0-0			
	MTG PLATE, FAN HOUSING	C-MD-7405663-0-0			
	SCREEN, FAN	C-MD-7404881-0-0			
	PROTECTION COVER	B-MD-5303134-0-0			
	BOTTOM PLATE, FAN HOUSING	C-IA-7405665-0-0			
50	MARG CHK & MAINT PANEL ASSEMBLY	E-AD-7005352-1-0			
	MARG CHK & MAINT PANEL ASSEMBLY.	E-AD-7005352-2-0			
	MARG CHK & MAINT PANEL ASSEMBLY	E-AD-7005352-3-0			
	MARG CHK & MAINT PNL ASSY (PL)	A-PL-7005352-0-0			
51	CHECK PANEL MAINT & MARGINAL	D-IA-7405692-0-0			
	SILK SCREEN (SEE NOTE #2)	C-SS-7405428-0-0			
52	PANEL (CONN) MARG CHECK CONT	C-IA-7405687-0-0			
	PANEL (CONN) MARG CHK CONT	B-SS-7405776-0-0			
53	SWITCH BOARD ASSY (MARG CHK & MAINT)	C-IA-5404051-0-0			
	18 PIN RECEPTACLE REWORK	B-MD-5503954-0-0			
	SPACER BAR	B-MD-7405509-0-0			
	ROCKER TO SW (PEACOCK BLU)	C-AD-5404424-2-0			
	ROCKER TO SW (CHK BLU)	C-AD-5404424-1-0			
54	SWITCH BOARD, MARG CHK & MAINT	C-IA-5004034-0-0			
	BOARD GLASS EPOXY, BLANK	D-MD-1402230-0-0			
55	HEAT SWITCH ASSEMBLY	C-AD-7005510-0-0			
	HEAT SWITCH ASSY (P.L.)	A-PL-7005510-0-0			
	RETAINER	C-MD-7406109-0-0			
	BRACKET, SIDE	B-IA-7406106-0-0			
	COVER	B-MD-7406107-0-0			
56	728 POWER SUPPLY	D-MA-729-0-1			
	729 POWER SUPPLY (P.L.)	A-PL-729-0-1			
	728A POWER SUPPLY	D-MA-728A-0-1			
	728A POWER SUPPLY (P.L.)	A-PL-728A-0-1			
57	779 POWER SUPPLY	D-MA-779-0-1			
	779 POWER SUPPLY (P.L.)	A-PL-779-0-1			
	779A POWER SUPPLY	D-MA-779A-0-1			
	779A POWER SUPPLY (P.L.)	A-PL-779A-0-1			
58	778 POWER SUPPLY	D-MA-778-0-1			
	778 POWER SUPPLY (P.L.)	A-PL-778-0-1			
	778A POWER SUPPLY	D-MA-778A-0-1			
	778A POWER SUPPLY (P.L.)	A-PL-778A-0-1			

FIND NO.	MECHANICAL DESCRIPTION	PART NO.	DEPT USAGE PROD	CUST	F/C
59	702A MARGINAL CHK POWER SUPPLY	D-UA-702A-0-0			
	702A MARG CHK POWER SUPPLY (P.L.)	A-PL-702A-0-0			
	702 MARGINAL CHK POWER SUPPLY	D-UA-702-0-0			
	702 MARG CHK POWER SUPPLY (P.L.)	A-PL-702-0-0			
60	FRONT DOOR ASSEMBLY BAY #3	E-AD-7005355-0-0			
	FRONT DOOR ASSY BAY #3 (P.L.)	A-PL-7005355-0-0			
	DOOR FRAME	E-IA-7405725-0-0			
	HINGE PIN, TOP	B-MD-20400-7			
	HINGE PIN, BOTTOM	B-MD-20400-8			
	SPACER, DOOR	B-MD-7405501-0-0			
61	PC09-A READER & PUNCH	D-UA-PC09-A-0			
	DWG INDEX	D-DI-PC09-A-4			
62	SWITCH INTERLOCK ASSEMBLY	C-MD-7005683-0-0			
	SWITCH INTERLOCK ASSY (PL)	A-PL-7005683-0-0			
	PLATE CONNECTOR	B-IA-7406415-0-0			
	~~PLATE STRIKER~~	~~B-MD-7406414-0-0~~			
	COVER	B-MD-7406413-0-0			
63	MAINT SWITCH BRKT (ASSY)	C-MD-7005675-0-0			
	MAINT SWITCH BRKT (ASSY) (PL)	A-PL-7005675-0-0			
	BRKT, MAINT SWITCH	C-MD-7406397-0-0			
	DECAL	A-DC-7406404-0-0			
64	703 POWER SUPPLY	D-UA-703-0-0			
	703 POWER SUPPLY (PL)	A-PL-703-0-0			
CONT	DECALS KA10	A-DC-7406473-0-0			
50	SWITCH REWORK	B-MD-7405875-0-0			
	PHENOLIC BOARD	C-MD-7406490-0-0			
	METER REWORK (HOBBS)(240V 50 HZ)	B-MD-7406249-1-0			
	METER REWORK (HOBBS)(115V 60 HZ)	B-MD-7406249-2-0			
	METER REWORK (HOBBS)(115V 50 HZ)	B-MD-7406249-3-0			

D-DI-KA10-0-3 Drawing Index List KA10 (Sheet 3)

FIND NO.	ELECTRICAL DESCRIPTION	PART NO.	DEPT USAGE PROD	CUST	F/C
	KA10 (60 HZ 115V)	A-ML-KA10-A			
	KA10 (50 HZ 115V)	A-ML-KA10-B			
	KA10 (50 HZ 220V)	A-ML-KA10-C			
	ADDER CONTROL FLIP-FLOP	D-BS-KA10-0-AD1			
	ADDER CONTROL	D-BS-KA10-0-AD2			
	ADDER LEFT HALF	D-BS-KA10-C-AD3			
	ADDER RIGHT HALF	D-BS-KA10-0-AD4			
	AR INPUTS	D-BS-KA10-0-ARI			
	AR REGISTER	D-BS-KA10-0-AR1			
	AR REGISTER	D-BS-KA10-0-AR2			
	AR REGISTER	D-BS-KA10-0-AR3			
	AR REGISTER	D-BS-KA10-0-AR4			
	AR CONTROL PULSE	D-BS-KA10-0-ARC1			
	AR CONTROL PULSE	D-BS-KA10-0-ARC2			
	AR CONTROL PULSE	D-BS-KA10-0-ARC3			
	ARITHMETIC FLAGS	D-BS-KA10-0-ARF			
	AR & MQ SHIFT CONNECTIONS	D-BS-KA10-0-ARMQ			
	ADDRESS SWITCH COMPARATORS	D-BS-KA10-0-AS			
	BR CONTROL	D-BS-KA10-0-BR1			
	BR REGISTER	D-BS-KA10-0-BR2			
	BLOCK TRANSFER AND MULTIPLY	D-BS-KA10-0-BTMP			
	BYTE INSTRUCTION FIRST PART	D-BS-KA10-0-BYTE			
	ARITHMETIC PROCESSOR STATUS REG	D-BS-KA10-0-CPA			
	BYTE DEPOSIT AND LOAD	D-BS-KA10-0-DBLB			
	DIVIDE SUBROUTINE & FIXED DIVIDE	D-BS-KA10-0-DSDV			
	EXECUTION CYCLE	D-BS-KA10-0-E			
	EXECUTIVE CONTROL	D-BS-KA10-0-EX			
	FETCH CYCLE TIME PULSE	D-BS-KA10-0-F1			
	FETCH CYCLE LEVELS	D-BS-KA10-0-F2			
	FLOATING ADD INSTRUCTIONS	D-BS-KA10-0-FA			
	FLOATING DIVIDE	D-BS-KA10-0-FDV			
	FLOATING EXPONENT REG & CONTROL	D-BS-KA10-0-FE			
	FAST MEMORY	D-BS-KA10-0-FM			
	FAST MEMORY ADDRESS	D-BS-KA10-0-FMA			
	FP EXP CALC FLOATING MULTIPLY	D-BS-KA10-0-FPFM			
	HALF WORD TRANSFER	D-BS-KA10-0-HWT			
	INSTRUCTION & ADDRESS CYCLES	D-BS-KA10-0-IA			
	I/O BUS (8- 17)	D-BS-KA10-0-IOB1			
	I/O BUS (18-35)	D-BS-KA10-0-IOB2			
	I/O BUS CONTROL & I/O SELECTION	D-BS-KA10-0-IOBC			
	IOB INPUTS	D-BS-KA10-0-IOBI			
	IN-OUT TRANSFER CONTROL	D-BS-KA10-0-IOT			
	INSTRUCTION REGISTER	D-BS-KA10-0-IR			
	IR DECODING	D-BS-KA10-0-IR1			
	IR DECODING	D-BS-KA10-0-IR2			
	IR DECODING	D-BS-KA10-0-IR3			
	KEY & SWITCHES CONTROLS	D-BS-KA10-0-KEY1			
	KEY & SWITCHES CONTROLS	D-BS-KA10-0-KEY2			
	KEY & SWITCHES CONTROLS	D-BS-KA10-0-KEY3			
	MA CONTROL	D-BS-KA10-0-MA1			
	MA REGISTER	D-BS-KA10-0-MA2			
	MEMORY ADDRESS INTERFACE	D-BS-KA10-0-MAI			
	MEMORY BUS DATA INTERFACE	D-BS-KA10-0-MBD1			
	MEMORY CONTROL	D-BS-KA10-0-MC1			
	MEMORY CONTROL	D-BS-KA10-0-MC2			
	MQ CONTROL	D-BS-KA10-0-MQ1			
	MULTIPLIER QUOTIENT (MQ8-17)	D-BS-KA10-0-MQ2			
	MULTIPLIER QUOTIENT (MQ18-35)	D-BS-KA10-0-MQ3			
	MASTER CLEAR & POWER CLEAR	D-BS-KA10-0-MR			
	NORMALIZE RETURN & NR LONG	D-BS-KA10-0-NRNL			
	PARITY BUFFER REGISTER	D-BS-KA10-0-PB			
	PROGRAM COUNTER CONTROL	D-BS-KA10-0-PC1			
	PROGRAM COUNTER REGISTER	D-BS-KA10-0-PC2			
	PI CONTROL	D-BS-KA10-0-PI1			
	PRIORITY INTERRUPT PIH, PIR, PIO	D-BS-KA10-0-PI2			
	PARITY NETWORK	D-BS-KA10-0-PN			
	PROTECT REGISTER	D-BS-KA10-0-PR			
	PAPER TAPE PUNCH CONTROL 1	D-BS-KA10-0-PTP1			
	PAPER TAPE PUNCH CONTROL 2	D-BS-KA10-0-PTP2			
	PAPER TAPE READER CONTROL	D-BS-KA10-0-PTR1			
	PAPER TAPE READER CONTROL	D-BS-KA10-0-PTR2			
	PAPER TAPE READER CONTROL	D-BS-KA10-0-PTR3			
	RELOCATE REGISTER	D-BS-KA10-0-RL			
	STORE CYCLE TIME PULSES	D-BS-KA10-0-S1			
	STORE CYCLE LEVELS	D-BS-KA10-0-S2			
	SHIFT COUNT REGISTER	D-BS-KA10-0-SC			
	SHIFT COUNT ADDER	D-BS-KA10-0-SCAD			
	SHIFT COUNTER CONTROL	D-BS-KA10-0-SCC1			
	SHIFT COUNTER CONTROL	D-BS-KA10-0-SCC2			
	SHIFT & CNT SUBROUTINE	D-BS-KA10-0-SCSR			
	TELETYPE CONTROL	D-BS-KA10-0-TTY1			
	TELETYPE CONTROL	D-BS-KA10-0-TTY2			
	BASIC INSTRUCTION FLOW	D-FD-KA10-0-BIF1			
	BASIC INSTRUCTION FLOW	D-FD-KA10-0-BIF2			
	BASIC INSTRUCTION FLOW	D-FD-KA10-0-BIF3			
	BASIC I/O REGISTERS	D-FD-KA10-0-BIOR			
	BYTE INSTRUCTION FLOW	D-FD-KA10-0-BYTF			
1	FIXED POINT DIVIDE & SUBROUTINE	D-FD-KA10-0-DIVF			
	EXECUTE & STORE CYCLE	D-FD-KA10-0-ESC			
	FLOATING ADD, SUB & UFA FLOW	D-FD-KA10-0-FAF			
	FETCH CYCLE FLOW	D-FD-KA10-0-FC			
	FLOATING DIVIDE	D-FD-KA10-0-FDVF			
	FP EXP CAL SUBR FN & MPY SUBR	D-FD-KA10-0-FPMC			
	INSTRUCTION & ADDRESS CYCLE	D-FD-KA10-0-IAC			
	KEY OPERATIONS FLOW DIAGRAM	D-FD-KA10-0-KO			
	MEMORY CONTROL & FAST MEM FLOWS	D-FD-KA10-0-MCFM			
	NORMALIZE RETURN SUBROUTINE	D-FD-KA10-0-NRF			
	PDP-10 REGISTER ORGANIZATION	D-FD-KA10-0-REG			
	SHIFT COUNT ACTION FLOW	D-FD-KA10-0-SCAF			
	SHIFT & MUL FLOW	D-FD-KA10-0-SMF			
	IN-OUT TRANSFER CONTROL FLOW	D-FD-KA10-0-IOTF			
	READ-IN FUNCTION ISOLATED FLOW	D-FD-KA10-0-RIMF			
	SHIFT CNT SUBROUTINE & BLT FLOW	D-FD-KA10-0-SCBT			
	INDICATOR & CONSOLE SW CONN	D-IC-KA10-0-ICSC1			
	INDICATOR & CONSOLE SW CONN	D-IC-KA10-0-ICSC2			
	INTER-BAY CABLES	D-IC-KA10-0-IBC1			
	INTER-BAY CABLES	D-IC-KA10-0-IBC2			
	MODULE UTILIZATION PNL 1A-1D	D-MU-KA10-0-1A1D			
	MODULE UTILIZATION PNL 1E-1J	D-MU-KA10-0-1E1J			
	MODULE UTILIZATION PNL 1K-1N	D-MU-KA10-0-1K1N			
	MODULE UTILIZATION PNL 1P-1T	D-MU-KA10-0-1P1T			
	MODULE UTILIZATION PNL 2A-2D	D-MU-KA10-0-2A2D			
	MODULE UTILIZATION PNL 2E-2J	D-MU-KA10-0-2E2J			
	MODULE UTILIZATION PNL 2K-2N	D-MU-KA10-0-2K2N			
	MODULE UTILIZATION PNL 2P-2T	D-MU-KA10-0-2P2T			
	MODULE UTILIZATION PNL 3A-3D	D-MU-KA10-0-3A3D			
	MODULE UTILIZATION PNL 3E-3F	D-MU-KA10-0-3E3F			
	PULSE & LEVEL TERMS BAY 1 & 2	D-IC-KA10-0-TERM			
	PDP-10 PROCESSOR LAYOUT	D-IC-KA10-0-PRL			
	DC POWER WIRING	D-IC-KA10-0-1			
	AC POWER WIRING	D-IC-KA10-0-2			
	MEMORY INDICATOR	D-BS-KA10-0-MI			
	FLOAT SCALE & DBL FLOAT NEG	D-FD-KA10-0-FSDN			
11	BLOWER ASSEMBLY	D-AD-7005363-0-0			
12	MARGINAL CHECK ASSY BAY #1	E-AD-7005378-0-0			
14	MARG CHK SW BOARD ASSEMBLY #1	C-IA-5404110-0-0			
	CIRCUIT SCHEMATIC	B-CS-5404110-0-1			
16	MARGINAL CHECK ASSEMBLY BAY #2	E-AD-7005377-0-0			
18	MARGINAL CHECK ASSEMBLY BAY #3	E-AD-7005348-0-0			
20	MARG CHK SW BOARD ASSEMBLY #2	C-IA-5404113-0-0			
	CIRCUIT SCHEMATIC	B-CS-5404113-0-1			
23	CONTROL LIGHT PANEL #1	D-AD-5404031-0-0			
	CIRCUIT SCHEMATIC	B-CS-5404031-0-1			
25	CONTROL LIGHT PANEL #2	D-AD-5404030-0-0			
	CIRCUIT SCHEMATIC	B-CS-5404030-0-1			
27	SWITCH BOARD ASSEMBLY #1	C-IA-5404010-0-0			
	CIRCUIT SCHEMATIC	B-CS-5404010-0-2			
29	SWITCH BOARD ASSEMBLY #2	D-IA-5404012-0-0			
	CIRCUIT SCHEMATIC	B-CS-5404012-0-1			
31	SWITCH BOARD ASSEMBLY #4	D-IA-5404023-0-0			
	CIRCUIT SCHEMATIC	B-CS-5404023-0-1			
35	FAN HOUSING ASSEMBLY, PLENUM	E-AD-7005269-0-0			
41	LIGHT BOARD ASSEMBLY	D-IA-5404029-0-0			
	CIRCUIT SCHEMATIC	B-CS-5404029-0-1			
46	LOGIC FRAME ASSY BAY #1	D-AD-7005354-0-0			
	WIRE LIST KA10	K-WL-KA10-0-4			
47	LOGIC FRAME ASSEMBLY BAY #2	D-AD-7005350-0-0			
	WIRE LIST KA10	K-WL-KA10-0-4			
48	LOGIC FRAME ASSEMBLY BAY #3	D-AD-7005329-0-0			
	WIRE LIST KA10	K-WL-KA10-0-4			
49	FAN HOUSING ASSEMBLY BAY #3	D-AD-7005346-0-0			
50	MARGINAL CHK & MAINT PANEL	E-AD-7005352-0-0			
53	SWITCH BOARD ASSEMBLY	C-IA-5404051-0-0			
	CIRCUIT SCHEMATIC	B-CS-5404051-0-3			
55	HEAT SWITCH ASSEMBLY	C-AD-7005510-0-0			
62	SWITCH INTERLOCK ASSEMBLY	C-AD-7005683-0-0			
1 CONT	MODULE COUNT	A-PL-KA10-0-MC			
	EXTERNAL COMPONENTS LIST	A-WL-KA10-0-GW			
	TWP LIST KA10 BAY 1	A-WL-KA10-0-TWP1			
	TWP LIST KA10 BAY 2	A-WL-KA10-0-TWP2			
	FAST MEMORY	A-ML-KM10-0-0			
	EXTENDED INSTRUCTION SET	A-ML-KE10-0-0			
	TIME SHARING OPTION	A-ML-KT10-0-0			

D-DI-KA10-0-3 Drawing Index List KA10 (Sheet 4)

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

ENGINEERING SPECIFICATION DATE 10/16/67

TITLE Removing and Reinstalling the KE10 Option: Byte and Floating Point

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE

A-ML-KE10-0 Extended Instruction Set (Sheet 1)

1. Removing the Option

   A. Before removing the KE10 Option, the computer should be thoroughly checked out, including the instructions in this option.

   B. 1. Procure 38 W990 Blank modules.
      2. Install a continuous jumper through lugs C-D-E-P-N on each of 32 W990's. (Unlabeled)
      3. Install a jumper through lugs C-F-N-S-V on one of the W990's and label it 1N23.
      4. Install a jumper through lugs C-F-L-R-V on one of the W990's and label it 1N14.
      5. Install a jumper through lugs C-D-E-K-N-P-U on three W990's and label them 1B03 and 1A07and 1B09.
      6. Install a jumper through lugs C-U on one W990 and label it 1L21.

   C. Remove the following modules:

Panel	Module Positions
1A	1, 2, 3, 4, 5, 6, 7, 9, 1Ø, 11, 12, 13, 14, 15, 16, 17, 2Ø, 22, 24
1B	2, 3, 4, 5, 6, 9, 1Ø, 11, 12, 14, 15, 18, 19, 21, 22, 23, 24, 25, 26, 27, 28, 33, 36, 39, 4Ø
1C	1, 2, 3, 5, 6, 7, 8, 1Ø, 11, 12, 23, 24, 3Ø, 34, 38
1D	1, 2, 3, 4, 5, 6, 7, 8, 9, 1Ø, 12, 13, 15, 16, 17, 18, 19, 2Ø, 22, 23, 24, 25, 26, 31, 32, 33, 35, 37, 38, 39
1E	1, 2, 3, 4, 6, 7, 8, 11, 12, 13, 14, 16, 17, 18, 19, 2Ø, 24, 25, 36
1F	18, 22, 23, 24, 29, 31, 35
1H	21
1J	4, 29, 38, 39
1K	3Ø
1L	21, 33, 39
1M	
1N	14, 23
1P	38
1R	
1S	25

A-ML-KE10-0 Extended Instruction Set (Sheet 2)

1. Removing the Option (continued)

C. Remove the following modules: (continued)

Panel	Module Positions
1T	
2E	6, 8, 10, 11, 12, 14, 16, 32, 37, 40

You should have removed 138 modules.

D. 1. Install the 32 unlabeled W990's in the following slots:

Panel	Module Positions
1A	2, 5, 10, 12, 14, 16
1B	5,14,21,24
1C	1, 5, 8
1D	2, 5, 8, 12, 16, 19, 22, 24, 25
1E	2, 4, 7, 11, 14, 18
1F	
1H	21
1J	4
1K	30
1L	
1M	
1N	
1P	
1R	
1S	25
1T	

2. Install the 6 labeled W990's in the appropriate slots.

E. Turn the machine on and run all diagnostics, remembering to disable the Byte and Floating Point tests.

2. Reinstalling the KE10 Option

A. Procure the following modules

B130	2	
B133	4	
B134	16	
B135	6	
B137	4	
B141	1	
B156	1	
B163	3	
B165	10	
B168	9	
B212	9	
B311	39	
B312	1	(Set to 280 ns Pin L to N)
B611	33	
Total	138	

B. Remove the 41 W990's specified in parts 1B3 through 1B6 and 1D above.

C. Referring to the appropriate UML's, install all modules listed in Part 1C above.

D. Make sure the F-P trap switch to the right of panel 1J is off (down).

E. Run all diagnostics, making sure to thoroughly test the byte and floating point instructions.

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

ENGINEERING SPECIFICATION

DATE 10-18-67

TITLE Removal and Re-Installation of KM-10 "Fast Registers"

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE

1. Removing KM-1Ø Option

   A. Before removing the KM-1Ø option, the computer should be thoroughly checked out, including using the fast ac's.

   B. Procure a W990 blank module and install a continuous jumper thru pins C-D-E-P-N.

   C. Remove the following modules:

      1J 26

      1T 31, 33

      2E 15, 19, 23

      2K-L 9, 10, 11, 12, 13, 15, 16, 17, 18, 20, 21, 22, 23

      2L 8

   D. Install the W990 in 1J26.

   E. Remove the 703 power supply on the door of BAY 2; also remove the 728 supply at the top of the BAY 2. Be sure to thoroughly tape all exposed wire ends. Do not remove the wires themselves.

   F. Procure and install a 31 1/2" x 11 1/4" blank panel (#7405689) in place of the 7Ø3, and an 8" plenum door blank (7402036) place of the 728.

   G. Turn off FM Enable switch on the maintenance panel.

   H. Run all diagnostic programs briefly to insure correct operation of the machine.

2. Re-Installing KM-1Ø Option

No.	Description	Quantity
728	Power Supply	1
703	Power Supply	1
B163	Module	3
B199	"	1
B250	"	12
B311	"	2
B611	"	2

B. Remove the blank panels from the bay 2 plenum door (described in 1F). Remove the W990 in 1J26.

C. Install the 2 power supplies in the bay 2 plenum door, and wire them using the existing taped-up wires, according to fig. 1, (attached).

D. On Line Checkout Procedure for the KM-1Ø.

NOTE: Do not install modules

1.0 Visually check the wiring run from the 703 Power Supply to the logic on Bay 2.

1.1 Check for correct size of wire.

A. 14 gauge for the +1.8 volt line and the -3 volt line.
B. 18 gauge for the sense line for both the +1.8 volt line and the -3 volt line.

1.2 Check for correct color of wire

A. Brown -3 volt line
B. Yellow +1.8 volt line

1.3 Check for correct location of wire on logic.

A. -3 volt line on pin U of 2L16
B. +1.8 volt line on pin V of 2L16

2.0 Visually inspect the 703 Power Supply for

A. 1-G811 (+1.8 volt regulator)
B. 1-G812 (-3.0 volt regulator)
C. 2-G805C (series regulator)

2.1 Visually inspect the 728 or 728A power supplies for

A. H series or latter on the 728 60 H_z P.S.
B. E series on the 728 A 50 H_z P.S.

Note the models 728 (H) or 728A (E) provide a 160,000 MFD capacitor on the +10 volt side.

3.0 Power Check. Turn on power.

3.1 Using a Triplett meter. place one probe on pin U of 1L16 and the other probe to ground. Observe a -3 volt reading.

3.2 Place one probe on pin V of 1L16 and the other probe to ground. Observe a+1.8 volt reading.

3.3 Adjustments for the voltages are made on the 703 Power Supply while observing voltage reading on the logic.

NOTE: Turn power down.

4.0 Insert the modules specified in 2A as follows:

1J26	B611
1T31, 33	B311
2E 15, 19, 23	B163
2K-L 9	B199
2K-L 10, 11, 12, 13, 15, 16, 17, 18, 20, 21, 22, 23	B250
2L 8	B611

4.1 Turn power on and again measure the voltages.

Pin U -3.0 volts 1L16
Pin V +1.8 volts 1L16

5.0 Dynamic Test

5.1 Deposit and examine all ones through fast memory.

5.2 Deposit and examine all zeroes through fast memory.

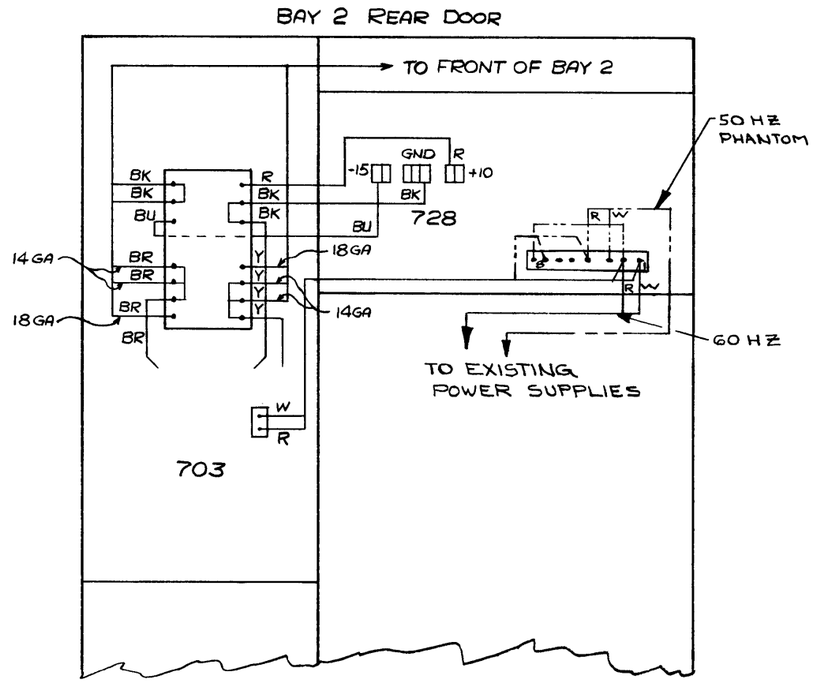
NOTE: The following programs shall be used while taking margins both at room temperature and elevated temperature.

A. Blt.
B. Program M
C. Address test high and low
D. Fast memory test = Maindec 10-D1FM-D

5.3 Margins

A. The +10 volt lines shall be margined at + - 7.5 volt.
B. The -15 volt lines shall be margined at + - 3.0 volts.
C. All margins shall be kept at the high end for five (5) minutes and at the low end for five (5) minutes.

FIG.1: AC & DC POWER WIRING FOR KM-10 POWER SUPPLIES



REFER TO DWG'S D-IC-KA10-0-2 SHT #3 & D-IC-KA10-0-1 SHT #3 FOR MASTER OF POWER WIRING.

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

ENGINEERING SPECIFICATION

DATE 12/21/67

TITLE Removing and Re-Installing the KT10 Option: "Time Sharing Option"

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE

I. **Removing the KT10 Option.**

A. Before removing the KT10 option the computer shall have been thoroughly tested, including the KT10 option

B. 1. Obtain two W990 Blank Modules.

2. Label one W990: "1S20". Connect a jumper from pin C to pin N of this module.

3. Label the other W990: "1S33". Connect a jumper from pin C, to pin F, and to pin R of this module.

C. Remove the following modules:

1P	21, 23
1S	20, 33
1T	14
2M	27 through 43 (17 modules)
2N	28, 30, 38, 40, 42

D. Install the two W990 modules in the appropriate slots.

E. Turn on the computer and run all diagnostic programs briefly. Remember to set console switches appropriately, to disable the user mode tests.

II. Re-Installing the KT10 Option.

A. Obtain the following modules:

B133:	1
B134:	1
B135:	1
B138:	17
B311:	2
S203:	5
Total	27

ENGINEERING SPECIFICATION digital CONTINUATION SHEET

TITLE Removing and Re-Installing the KT10
Option: **"Time Sharing Option"**

B: Remove the W990 modules in slots 1S20 and 1S33.

C: Insert the 27 modules specified above as follows:

B133	1P21
B134	1S33
B135	1P23
B138's	2M27-43 (17 modules)
B311's	1S20, 1T14
S203's	2N 28, 30, 38, 40, 42

D: Run Diagnostic Test "D" and block transfer test. Record margins of the B138's in panel 2M while running block transfer test.

INSTRUCTION	BOOLE	ADD SUBTRACT	FWT	HWT $-H^{LR}_{RL}(\overline{\ }_{I})$	HWT $H^{LR}_{RL}(\overline{\ }_{I})$	EXCH	UUO
INITIAL SWITCHES	BOOLE 2,10,13,16: E LONG BOOLE 0,3,10,17: FAC INH BOOLE Λ-(0,5,12,17)ΛXXX-: FCE BOOLE Λ-(0,5,12,17)ΛXXX$^{M}_{B}$: FCE PSE	EF0 LONG XXX-: FCE XXX$^{M}_{B}$: FCE PSE	MOV$^{M}_{N}$X: EF0 LONG MOVX$^{I}_{S}$: FAC INH MOVX-: FCE MOVXS: FCE PSE	E LONG HXXXSVHXX$\overset{0}{\underset{ES}{\Sigma}}$I: FAC INH HXXX-: FCE HXXXSVHXX-M: FCE PSE		FCE PSE	FAC INH PC+1 INH
INITIAL REGISTERS	AR; C(AC) or 0 BR; (0, E) or C(E) MA; E	AR; C(AC) BR; (0, E) or C(E) MA; E	AR; C(AC) or (0, E) or C(E) BR; (0, E) or C(E) MA; E	AR; C(AC) or (0, E) or C(E) BR; (0, E) or C(E) NOTE: IF HWT IS F (1 OPERAND), OPERAND IS IN AR. IF TWO OPERANDS, MEM IS IN BR, AC IS IN AR	AR; C(AC) BR; C(E) or (0, E)	AR; C(AC) BR; C(E)	MA; 0 AR; 0, E IR; INST
ET9	BOOLE 6,11,12,17: AD AR-EN SET BOOLE 1,6,7,10,16: AD BR+EN SET BOOLE 2,9,11,13,14,15: AD BR-EN SET BOOLE 6,11: AD CRY INS SET	AD AR+EN SET ADDX: AD BR+EN SET SUBX: AD BR-EN SET AD CRY 36 SET	MOV$^{N}_{M}$X: AD AR NEGATE	AD BR+EN SET HXXOXVHXXEX: AD BR± EN		AD BR+EN SET	
ET0	BOOLE 0,6,11,12,14: AR FM AD(J) BOOLE 1,9,13,16: AR FM AD(0) BOOLE 2,7,10,15,17: AR FM AD[1]	AR FM AD(J) ARF CRY STB	MOVSX: AR SWAP MOVNXV (MOVMX Λ AR0(1)): AR FM AD(J) ARF CRY STB	HLRXX: ARRT FM ARLT(J) HRLXX: ARLT FM ARRT (J) HXLOXV(HXLEX Λ HWT E TEST) VHXL-MVHXR-$\overline{\ }_{I}$: ARRT FM AD(J) HXROXV(HXREX Λ HWT E TEST) VHXR-MVHXL-$\overline{\ }_{I}$: ARLT FM AD(J) HXL≠XV(HXLEX Λ-HWT E TEST): ARRT CLR HXR≠XV(HXREX Λ-HWT E TEST): ARLT CLR	AR FM AD(J) BR FM AR(J) AD BR+ ONLY EN	AR FM AD(J) BR FM AR(J)	ARLT FM IR0-12[1] MA30 SET IR2(1) VIR3(1): EX ILL OP SET EXCTF SET EUUOF SET IR1XX: MA31 SET
ET1	AD CRY INS CLR AD AR-EN SET AD BR+EN CLR AD BR-EN CLR				HLRXX: ARRT FM ARLT(J) HRLXX: ARLT FM ARRT(J) HXRXX: ARLT FM AD(J) HXLXX: ARRT FM AD(J)		
ET2	AR FM AD(J)						
FINAL SWITCHES	XXXM: SAC INH	XXXM: SAC INH	MOVXM: SCE MOVXSΛ AC(0)VMOVXM: SAC INH	(HXXXSΛAC=0)VHXXXM: SAC INH HXX$\overset{0}{\underset{E}{\Sigma}}$M: SCE		SAR+BR	SCE SAC INH

BOOLE #	MNEMONIC
0	SET Z
1	AND
2	ANDCA
3	SETM
4	ANDCM
5	SETA
6	XOR
7	IOR
10	ANDCB
11	EQV
12	SETCA
13	ORCA
14	SETCM
15	ORCM
16	ORCB
17	SETO

NOTES:

1. UUO=(IR JRST A Λ-EX ALLOW IOTS Λ IR3(1))V(IR JRST A Λ-EX ALLOW IOTS Λ IR10(1)) V(IR IOT A Λ-EX ALLOW IOTS Λ EX PI SYNC(0))V(IR0(0)ΛIR1(0)ΛIR2(0))VIR 100-127 * OPEN IR 2(0) FROM TERM TO DISABLE FLOATING POINT HARDWARE
2. FLAGS: 0) AR OV FLAG
   1) AR CRY 0 FLAG
   2) AR CRY 1 FLAG
   3) AR FOV
   4) BYF G
   5) EX USER (SAVED)
   EX MODE SYNC (RESTORE)
   6) EX IOT USER (CANNOT BE TURNED ON IN USER MODE)
   7)
   8)
   9)
   10)
   11) AR FXU
   12) AR DCK
3. AR OV COND = (AD CRY 0(0) Λ AD CRY 1(1)) V (AD CRY 0(1) Λ AD CRY 1(0))
4. HWT E TEST = (IR3(0)ΛIR6(0)ΛAR0(1))V(IR3(1)ΛIR6(1)ΛAR0(1))V(IR3(0)Λ(IR6(1)ΛAR18(1))V(IR3(1)ΛIR6(0)ΛAR18(1))
5. ARF CRY STB Λ AR OV COND : AR OV FLAG SET
   Λ AD CRY 0(1) : AR CRY 0 FLAG SET
   Λ AD CRY 1(1) : AR CRY 1 FLAG SET

INSTRUCTION	JSR	JSP	JSA AC FM (E,PC+1) E FM C(AC) PC FM E+1	JRA AC FM C(C(ACLT)) PC FM E	JFCL	JRST	TEST	AOBJX
INITIAL SWITCHES	FAC INH E LONG	FAC INH	E LONG	FC C ACLT E LONG	FAC INH	FAC INH IR 10 (1) : E LONG	TDXX: FCE TSXX: FCE E LONG	EF∅ LONG
INITIAL REGISTERS	AR; ∅, E BR; ∅, E MA; E	MA; E	AR; C(AC) BR; (∅, E) MA; E	AR; AC SWAPPED BR; (∅, E) MQ; C(C(ACLT)) MA; C(ACLT)	MA; E	MA; E BR; LAST MEM REF (FLAGS LT HALF)	AR; C(AC) BR; (∅, E) C(E); MASK	AR; C(AC) MA; E
FT9			AD BR+EN	AD BR+EN			TXOX: AD BR+EN SET TXCX: AD AR+EN SET TX$^{Z}_{C}$X: AD BR-EN SET TXCX: AD CRY INS SET	AD AR+EN SET AD+1 BOTH
ET∅	PC FM MA(J) ARRT FM PC(J) ARLT FM FLAGS(J) BYF6 CLR	PC FM MA(J) ARRT FM PC(J) ARLT FM FLAGS(J) BYF6 CLR	ARRT FM PC(J); PC+1 BR FM AR(J); C(AC) PC FM MA(J); E	AR FM AD(J); (∅, E)	CONDITION Z; PC FM MA(J) IR 9(1) : AR OV CLR IR 10(1) : AR CRY ∅ CLR IR 11(1): AR CRY 1 CLR IR 12(1): AR FOV CLR	AR FM PC(J) PC FM MA(J) IR 12(1): EX MODE SYNC SET IR 11(1): ARF FLAGS FM BR(J) IR 9(1): PIOK CLEARS PIH IR 10(1): RUN CLR	T$^{S}_{L}$XX: AR SWAP	AR FM AD(J) (AOBJN ∧ AD∅(1)) : PC FM MA(J) (AOBJP ∧ AD∅(∅)) : PC FM MA(J)
ET1			ARLT FM ARRT(J); PC+1 ARRT FM PC(J); E	MA FM AR(J); E AR FM MQ(J); C(C(ACLT))		MA FM AR (J)	AD CRY INS CLR BR FM AR[∅] TX$^{C}_{C}$X: AR FM AD[1] TX$^{C}_{Z}$X: AR FM AD[∅] AD BR-EN CLR AD BR+EN SET AD AR+EN CLR	
ET2	PC+1; E+1		PC+1; E+1 AR SWAP	PC FM MA(J); E			T$^{S}_{L}$XX: AR SWAP TXXAV(TXXE ∧ AD=∅)V (TXXN ∧ AD≠∅): PC+1	
FINAL SWITCHES	SCE SAC INH		SAR+BR		SAC INH	SAC INH	TXNX: SAC INH	

NOTES:

1. CONDITION Z = (IR 9(1) ∧ AR OV(1)) V (IR 10(1) ∧ AR CRY ∅ FLAG (1)) V (IR 11(1) ∧ AR CRY 1 FLAG (1)) V (IR 12(1) ∧ AR FOV(1))
2. FLAGS: ∅) AR OV FLAG
   1) AR CRY ∅ FLAG
   2) AR CRY 1 FLAG
   3) AR FOV
   4) BYF6
   5) EX USER (SAVED)
      EX MODE SYNC (RESTORE)
   6) EX IOT USER (CANNOT BE TURNED ON IN USER MODE)
   7)
   8)
   9)
   10)
   11) AR FXU
   12) AR DCK

INSTRUCTION	SKIP AOSX SKIPX SOSX	JUMP AOJX JUMPX SOJX	CAM CAI	PUSH	PUSH J	POP	POPJ	XCT
INITIAL SWITCHES	EFØ LONG XOSX: FCE PSE SKIPX: FCE FAC INH	EFØ LONG	EFØ LONG CAMX: FCE	EFØ LONG FCE E LONG	EFØ LONG E LONG	EFØ LONG FC E ACEF E LONG		FAC INH PC+1, INH
INITIAL REGISTERS	AR; C(E)	AR; C(AC) MA; E	AR; C(AC) BR; (Ø, E) OR C(E)	AR; C(AC) BR; C(E) MA; E	AR; C(AC) BR; E MA; E MQ; Ø	AR; C (AC) BR; (Ø, E) MQ; (C(ACRT)) MA; C(ACRT)		MA; E
FT9	AD AR←EN SET AOXX: CRY 36 SOXX: AD BR←EN SET AD BR-EN SET		AD MINUS BR AD AR←EN SET	AD AR←EN SET AD CRY 36 SET AD+1 LH SET		AD AR←EN SET AD BR←EN AD-1 LH SET		
ETØ	AR FM AD(J) PC COND PV PC COND R: PC+1	AR FM AD(J) PC COND PV PC COND R: PC FM MA(J)	AR FM AD(J) PC COND PV PC COND Q: PC+1	AR FM AD(J) AD CRY Ø: CPA PDL OV SET	AR FM PC FLAGS(J) MQ FM AD(J) PC FM MA(J) AD CRY Ø: CPA PDL OV SET BYF 6 CLR	MQ FM AD(J) AR FM MQ(J) -AD CRY Ø: CPA PDL OV SET AD BR← ONLY EN		EXCTF SET
	XOXX ∧ { AR OV COND: AR OV FLAG SET ∨ AD CRY Ø(1): AR CRY Ø FLAG SET ∨ AD CRY 1(1): AR CRY 1 FLAG SET							
ET1				MA FM AR(J)	BR FM AR(J) AR FM MQ(J)	AR FM AD(J) BR FM AR(J)	MA FM AR(J) AR FM MQ(J)	
ET2					MA FM AR(J)	MA FM AR(J) AR FM MQ(J)	PC FM MA(J)	
FINAL SWITCHES	AC=Ø: SAC INH	JUMPX: SAC INH	SAC INH	SAR←BR	SAR←BR	SAR←BR		SAC INH

NOTES:

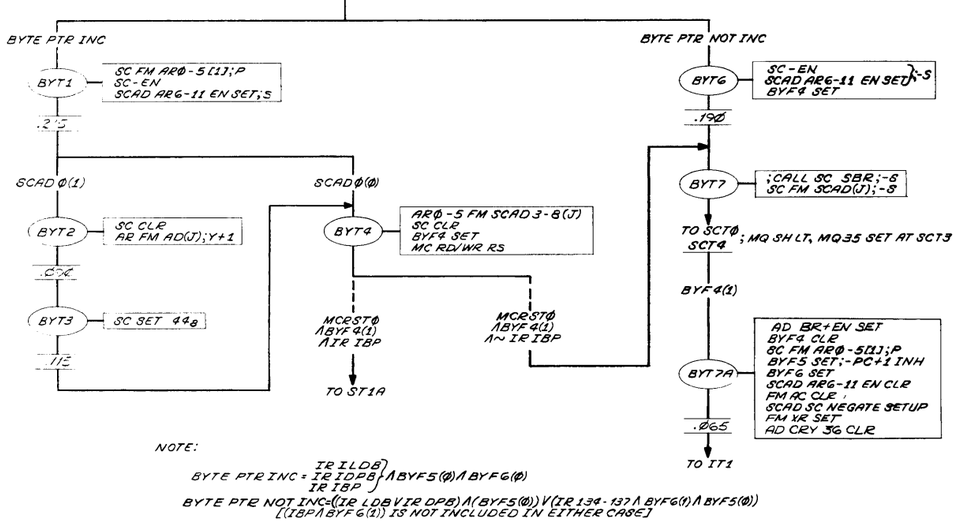
1. PC COND P = (IREG(Ø) ∧ AD = Ø ∧ IR7(1)) ∨ (IREG(1) ∧ IR7(Ø) ∧ IR8(Ø)) ∨ (IREG(1) ∧ − AD = Ø ∧ IR8(Ø))
   PC COND Q = (IREG(Ø) ∧ AD COND ∧ IR8(1)) ∨ (IREG(1) ∧ IR7(Ø) ∧ − AD COND) ∨ (IREG(1) ∧ − AD = Ø ∧ − AD COND)
   PC COND R = (IREG(Ø) ∧ IR8(1) ∧ AD Ø(1)) ∨ (IREG(1) ∧ IR7(Ø) ∧ AD Ø(Ø)) ∨ (IREG(1) ∧ − AD = Ø ∧ AD Ø(Ø))
2. AR OV COND = (AD CRY Ø(Ø) ∧ AD CRY 1(1)) ∨ (AD CRY Ø(1) ∧ AD CRY 1(Ø))
3. AD COND = (AD Ø(1) ∧ AD CRY Ø(1) ∧ AD CRY 1(1)) ∨ (AD Ø(1) ∧ AD CRY Ø(Ø) ∧ AD CRY 1(Ø)) ∨ (AD Ø(Ø) ∧ AD CRY Ø(1) ∧ AD CRY 1(Ø)) ∨ (AD Ø(Ø) ∧ AD CRY Ø(Ø) ∧ AD CRY 1(1))

D-FD-KA10-0-BIF3 Basic Instruction Flow

DEVICE NAME	ABBREV	DEV #	FUNCTION	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	DETAILED NOTES
PROCESSOR	CPA	000	CONO	CPA PDL OV CLR	IOB RESET	—	CPA ADR BREAK CLR	CPA MEM PROT FLAG CLR	CPA NON EX MEM CLR	CPA CLK EN CLR	CPA CLK EN SET	CPA CLK FLAG CLR	CPA FOV EN CLR	CPA FOV EN SET	AR FOV CLR	CPA AROV EN CLR	CPA AROV EN SET	AR OV CLR	CPA PIA 33	CPA PIA 34	CPA PIA 35	
			CONI	—	CPA PDL OV (1)	EX IOT USER (1)	CPA ADR BREAK (1)	CPA MEM PROT FLAG (1)	CPA NON-EX MEM (1)	—	CPA CLK EN (1)	CPA CLK FLAG (1)	—	CPA FOV EN (1)	AR FOV (1)	—	CPA AROV EN (1)	AR OV (1)	CPA PIA 33	CPA PIA 34	CPA PIA 35	
			DATAO LEFT HALF	PR0	PR1	PR2	PR3	PR4	PR5	PR6	PR7	—	—	—	—	—	—	—	—	—	—	NONE
			DATAO RIGHT HALF	RL18	RL19	RL20	RL21	RL22	RL23	RL24	RL25	—	—	—	—	—	—	—	—	—	—	
			DATAI LEFT / RIGHT	DS0 / DS18	DS1 / DS19	DS2 / DS20	DS3 / DS21	DS4 / DS22	DS5 / DS23	DS6 / DS24	DS7 / DS25	DS8 / DS26	DS9 / DS27	DS10 / DS28	DS11 / DS29	DS12 / DS30	DS13 / DS31	DS14 / DS32	DS15 / DS33	DS16 / DS34	DS17 / DS35	NONE
RELOCATE & HARDWARE BOOT	PI	001	CONO	CPA PWR FAIL CLR	CPA PAR ERR CLR	CPA PAR EN CLR	CPA PAR EN SET	—	PI RESET	PI0 FM IOB(1)	PI0(2) FM IOB(1)	PI0(0) FM IOB(1)	PI ACT CLR	PI ACT SET	PI 1 SELECT	PI 2 SELECT	PI 3 SELECT	PI 4 SELECT	PI 5 SELECT	PI 6 SELECT	PI 7 SELECT	
			CONI	CPA PWR FAIL (1)	CPA PAR ERR (1) MF 1/19	CPA PAR EN (1) 8/20	PIH 1 (1)	PIH 2 (1)	PIH 3 (1)	PIH 4 (1)	PIH 5 (1)	PIH 6 (1)	PIH 7 (1)	PI ACT (1)	PIO 1 (1)	PIO 2 (1)	PIO 3 (1)	PIO 4 (1)	PIO 5 (1)	PIO 6 (1)	PIO 7 (1)	
			DATAO LEFT / RIGHT	MI 0/18			MI 3/21	4/22	5/23	MF 6/24	7/25	8/26	MI 9/27	10/28	11/29	MI 12/30	13/31	14/32	MI 15/33	16/34	17/35	DATAO SET MI PROG
PAPER TAPE PUNCH	PTP	100	CONO	—	—	—	—	—	—	—	—	—	—	—	—	PTP BIN	PTP BUSY	PTP DONE	PTP PIA 33	PTP PIA 34	PTP PIA 35	
			CONI	—	—	—	—	—	—	—	—	—	—	—	PTP NO TAPE	PTP BIN (1)	PTP BUSY (1)	PTP DONE (1)	PTP PIA 33 (1)	PTP PIA 34 (1)	PTP PIA 35 (1)	
			DATAO	—	—	—	—	—	—	—	—	—	—	PTP HOLE 8	PTP HOLE 7	PTP HOLE 6	PTP HOLE 5	PTP HOLE 4	PTP HOLE 3	PTP HOLE 2	PTP HOLE 1	PTP DONE CLR PTP BUSY SET
PAPER TAPE READER	PTR	104	CONO	—	—	—	—	—	—	—	—	—	—	—	PTR EOT	PTR BIN	PTR BUSY	PTR DONE	PTR PIA 33	PTR PIA 34	PTR PIA 35	
			CONI	—	—	—	—	—	—	—	—	—	PTR TAPE FLAG (1)	—		PTR BIN (1)	PTR BUSY (1)	PTR DONE (1)	PTR PIA 33 (1)	PTR PIA 34 (1)	PTR PIA 35 (1)	
			DATAI LEFT / RIGHT	PTR0 / PTR18	PTR1 / PTR19	PTR2 / PTR20	PTR3 / PTR21	PTR4 / PTR22	PTR5 / PTR23	PTR6 / PTR24	PTR7 / PTR25	PTR8 / PTR26	PTR9 / PTR27	PTR10 / PTR28	PTR11 / PTR29	PTR12 / PTR30	PTR13 / PTR31	PTR14 / PTR32	PTR15 / PTR33	PTR16 / PTR34	PTR17 / PTR35	PTR DONE CLR PTR BUSY SET
TELETYPE	TTY	120	CONO	—	—	—	—	—	—	TTY TEST SET	TTI BUSY CLR	TTI FLAG CLR	TTO BUSY CLR	TTO DONE CLR	TTI BUSY SET	TTI FLAG SET	TTO BUSY SET	TTO DONE SET	TTY PIA 33	TTY PIA 34	TTY PIA 35	
			CONI	—	—	—	—	—	—	TTY TEST (1)	—	—	—	—	TTI BUSY (1)	TTI FLAG (1)	TTO BUSY (1)	TTO DONE (1)	TTY PIA 33 (1)	TTY PIA 34 (1)	TTY PIA 35 (1)	
			DATAO	—	—	—	—	—	—	—	—	—	—	TTO 0	TTO 1	TTO 2	TTO 3	TTO 4	TTO 5	TTO 6	TTO 7	TTO DONE CLR TTO BUSY SET TTI FLAG CLR
			DATAI	—	—	—	—	—	—	—	—	—	—	TTI 0	TTI 1	TTI 2	TTI 3	TTI 4	TTI 5	TTI 6	TTI 7	
PROGRAM COUNTER FLAGS SAVED BY JSP, ETC.				0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
				AR OV FLAG (1)	AR CRY 0 FLAG (1)	AR CRY 1 FLAG (1)	AR FOV (1)	BYF 6 (1)	EX USER (1)	CPA IOT USER (1)	—	—	—	—	AR FXU (1)	AR DCK (1)	*	*	*	*	*	

* THESE BITS NOT AVAILABLE FOR FLAGS SINCE THEY WILL CAUSE ADDRESS MODIFICATION WHEN INDIRECTED THRU

INSTRUCTION	BYTE (FIRST PART BYF5(Ø))		BYTE (SECOND PART BYF5(1)) XLDB	XDPB
INITIAL SWITCHES	FAC INH BYTE PTR INC: FCE PSE BYTE PTR NOT INC: FCE -IR IBP: PC+1 INH BYTE PTR INC V BYTE PTR NOT INC: ST INH		FAC INH FCE ST INH	FCE ST INH
INITIAL REGISTERS	AR; C(E); POINTER BR; C(E); POINTER IR 13-17; C(E 13-17); I, X OF POINTER		AR; C(E); DATA WORD BR; C(E); DATA WORD SC; P MQ; MASK	AR; C(AC); BYTE BR; C(E); DESTINATION WORD SC; P MQ; MASK
FT9	BYTE PTR INC: AD AR+ EN SET AD CRY 36 SET			
ETØ			SC FM SCAD(J); -P ; CALL SC SBR	SC FM SCAD(J); -P ; CALL SC SBR
FINAL SWITCHES	IBP: SAC INH			SAC INH SCE



NOTE:

BYTE PTR INC = { IR ILDB, IR IDPB, IR IBP } ∧ BYF5(Ø) ∧ BYF6(Ø)

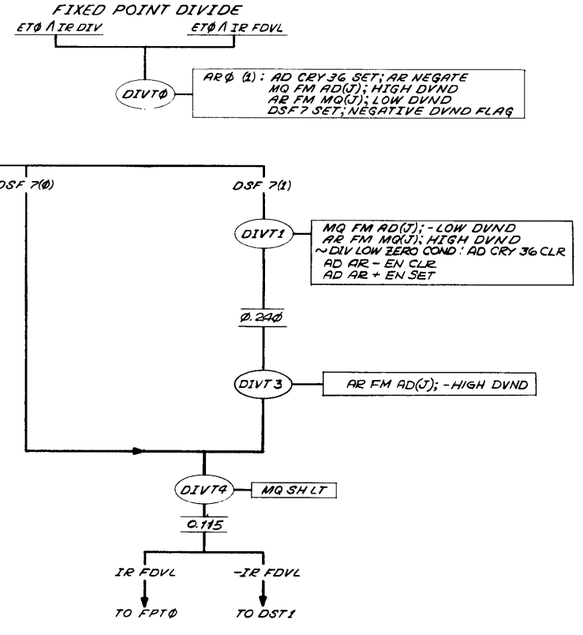
BYTE PTR NOT INC = [(IR LDB V IR DPB) ∧ (BYF5(Ø)) V (IR 134-137 ∧ BYF6(1) ∧ BYF5(Ø))] [(IBP ∧ BYF6(1)) IS NOT INCLUDED IN EITHER CASE]

BYTE LOAD = (IR ILDB V IR LDB) ∧ BYF5(1)

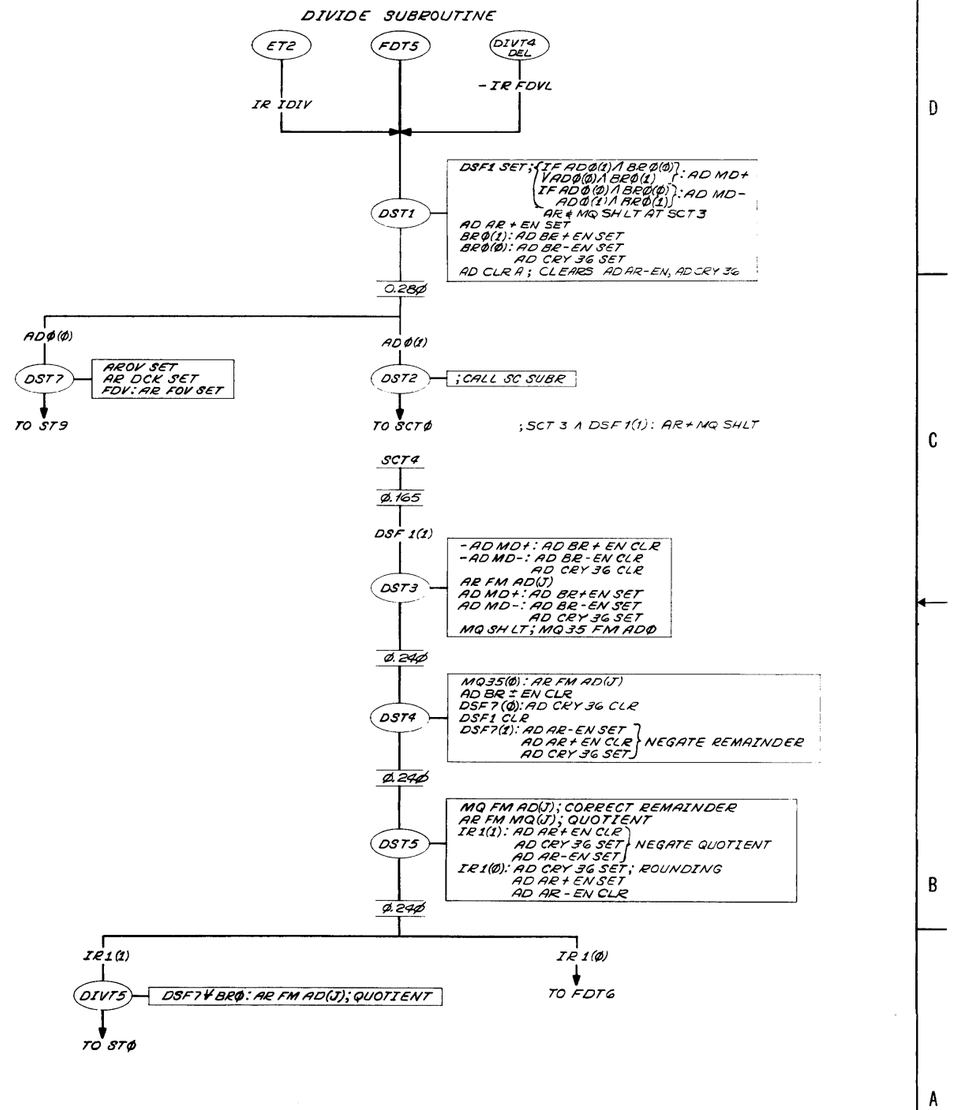
BYTE DEPOSIT = (IR IDPB V IR DPB) ∧ BYF5(1)

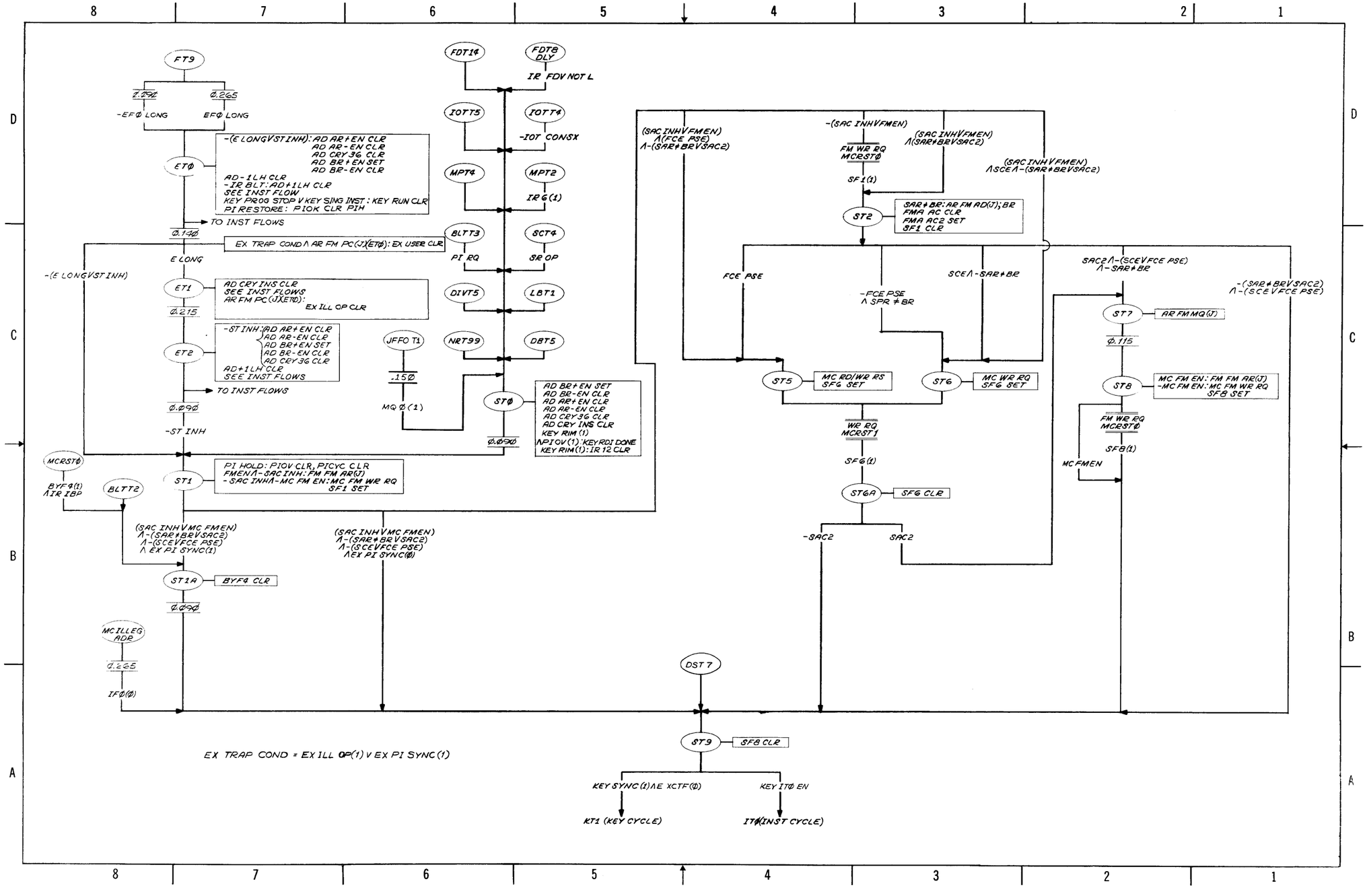
INSTRUCTION	IDIVX	DIVX
INITIAL SWITCHES	-IDIVI: FCE EFØ LONG E LONG ST INH	FAC2 -DIVI: FCE ST INH E LONG
INITIAL REGISTERS	AR; C(AC); DIVIDEND BR; Ø, E OR C(E); DIVISOR MQ; Ø	AR; C(AC); HIGH DIVIDEND BR; Ø, E OR C(E); DIVISOR MQ; C(AC2); LOW DIVIDEND
FT9	AD AR NEGATE	AD AR-EN SET
ETØ	ARØB(1): AR FM AD(J); -DVND DSF7 SET SC MD SETUP AD AR-EN CLR AD AR+EN SET AD CRY 36 CLR	SC MD SETUP (TO DIVT Ø)
ET1	MQ FM AD(J) AR CLR	
ET2	MQ SH LT (TO DST1)	(TO DIVT1 OR DIVT4)
FINAL SWITCHES	XDIVM: SAC INH XDIV(J/B): SAC2 XDIV(M/B): SCE	

FIXED POINT DIVIDE

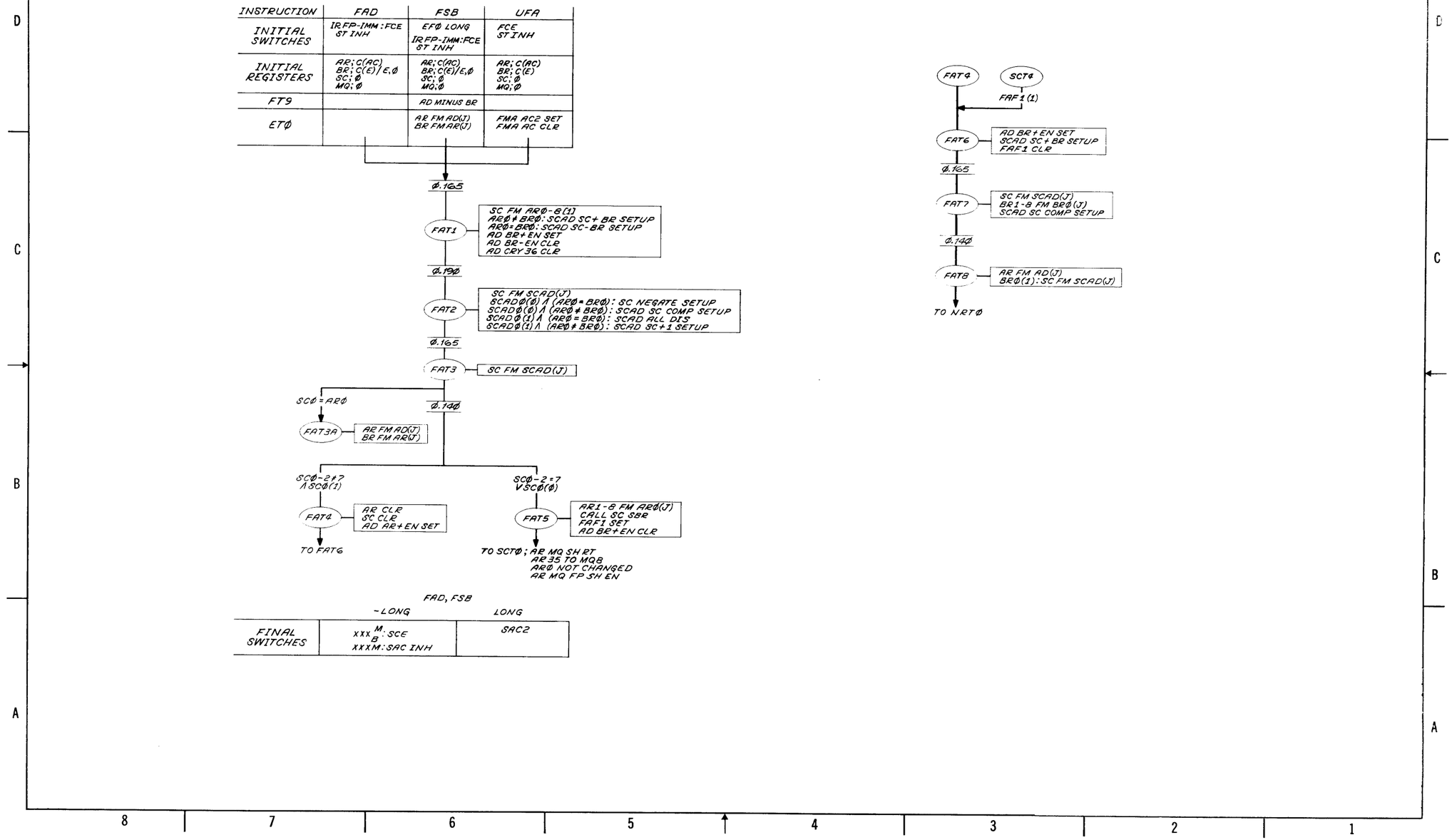


DIVIDE SUBROUTINE

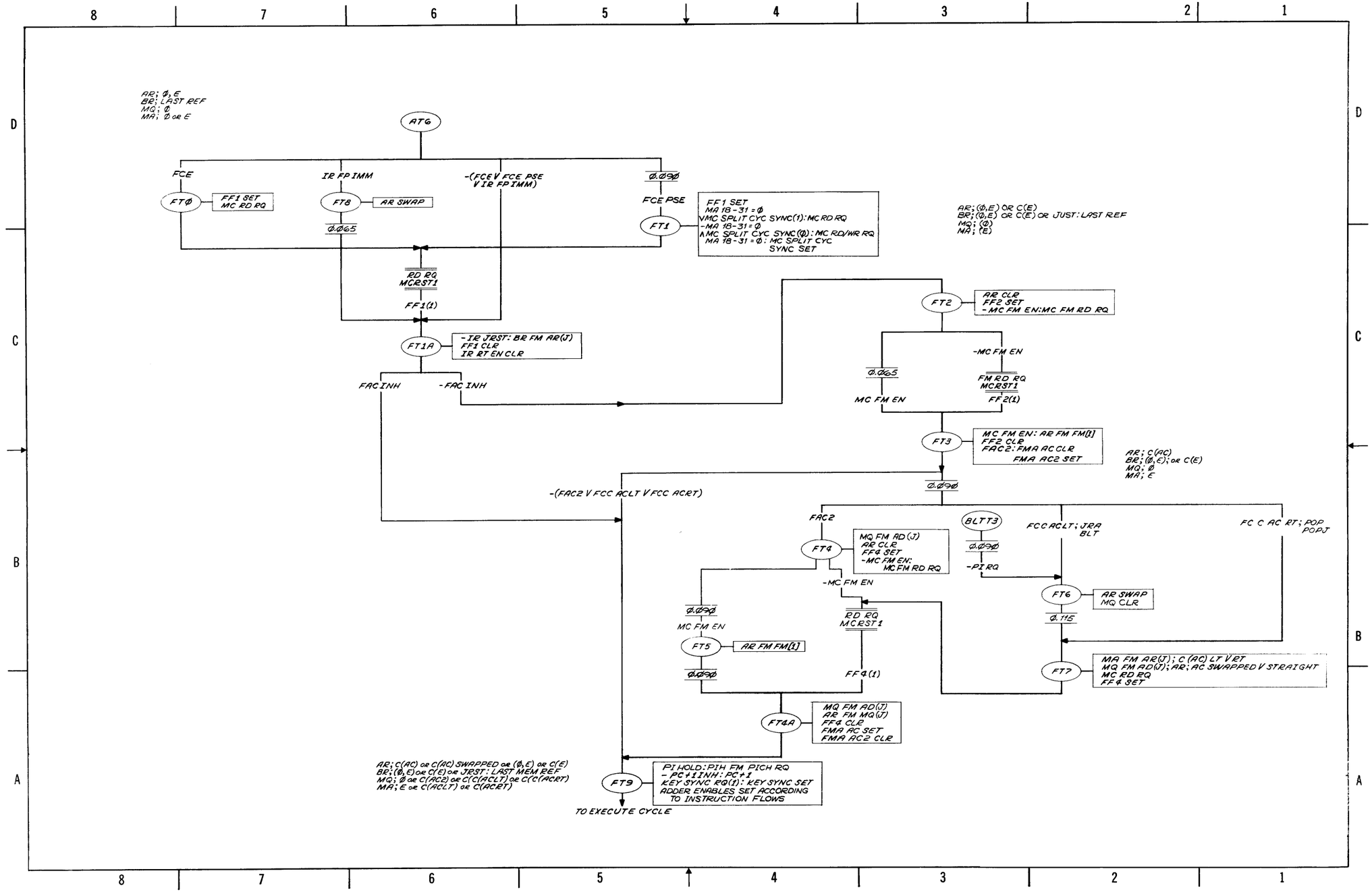




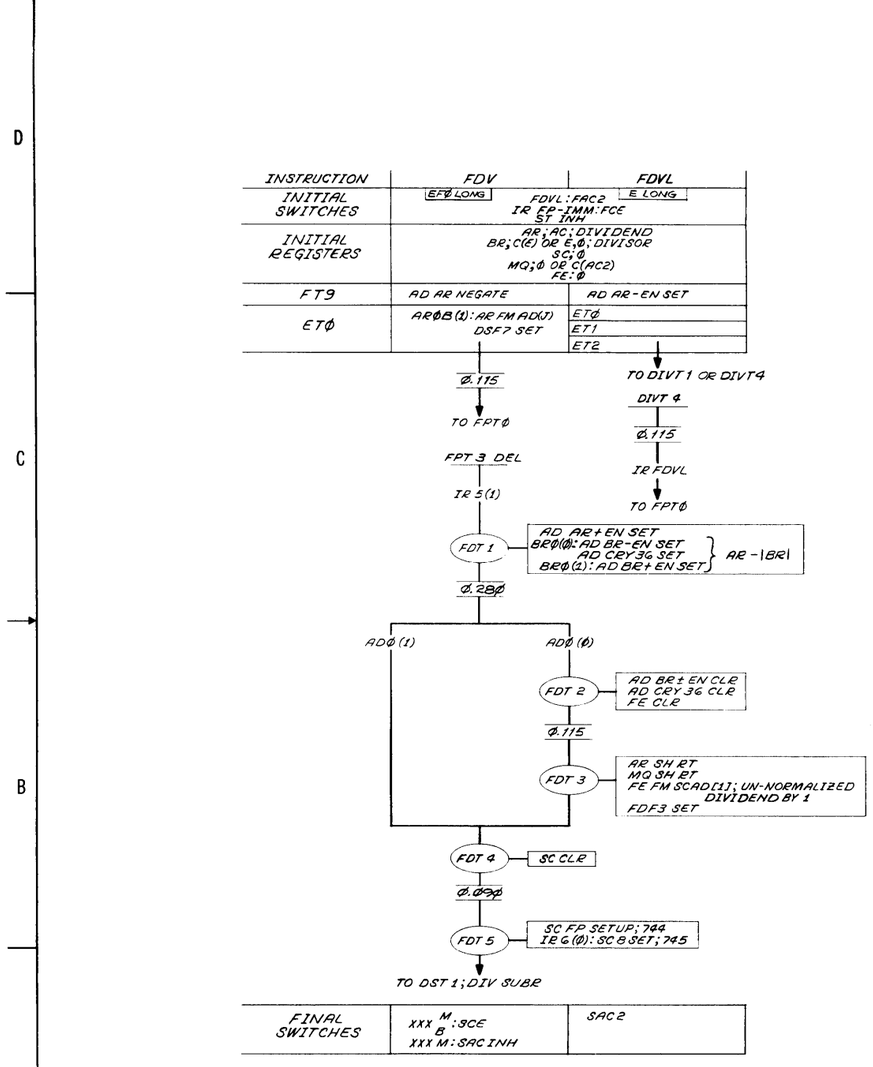
D-FD-KA10-0-ESC Execute and Store Cycles

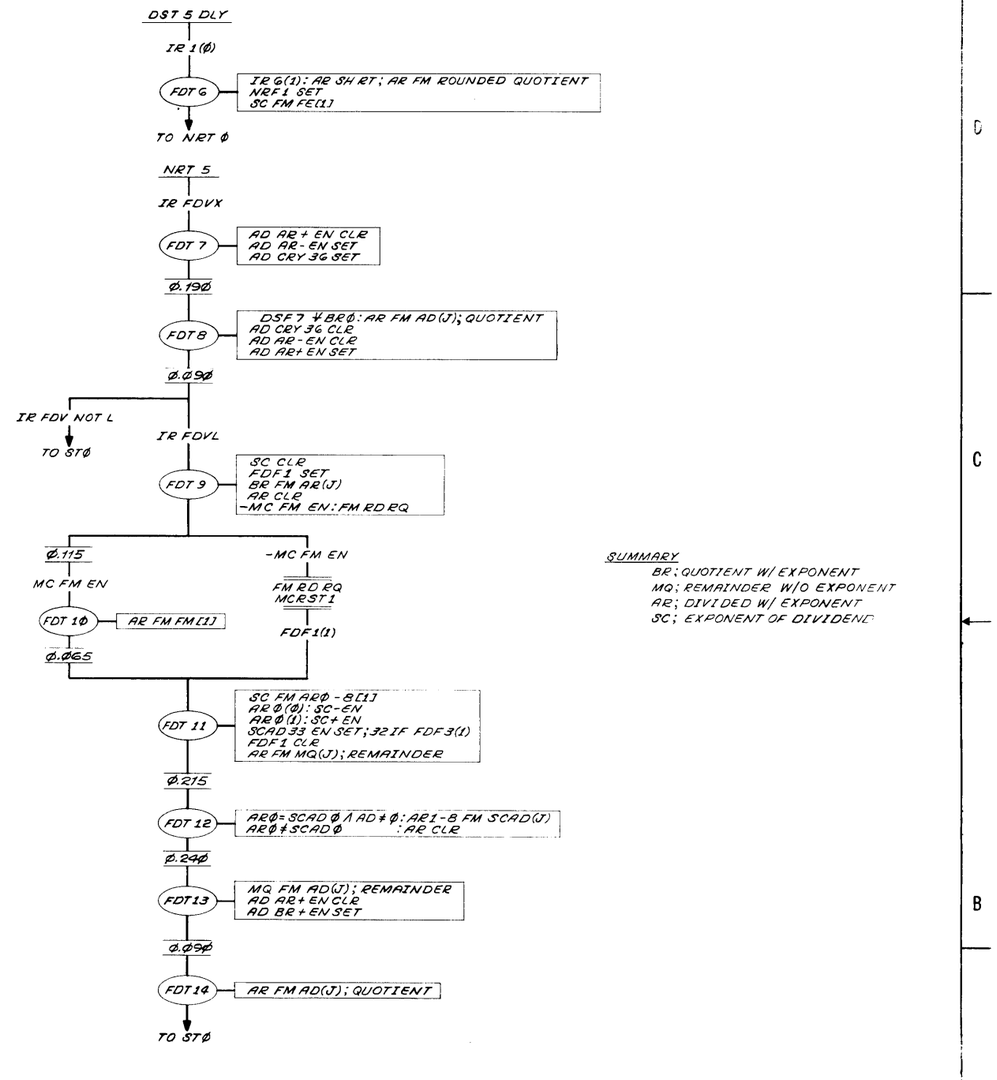


D-FD-KA10-0-FAF Floating Add, Sub and UFA Flow



D-FD-KA10-0-FC Fetch Cycle Flow





D-FD-KA10-0-FDVF Floating Divide

INSTRUCTION	FMP
INITIAL SWITCHES	-FP IMM : FCE ST INH
INITIAL REGISTERS	AR ; C(AC) BR ; C(E) or (E,Ø) SC ; Ø
FT9	
ETØ	

→ FPTØ

FINAL SWITCHES:	XXXM : SAC INH XXXM : SCE XXXL : SAC 2 XXXB : SCE

F.P. EXPONENT CALCULATE

ETØ → Ø.165 → IR FDV NOT L
DIVT4 → Ø.115 → IR FDVL
ETØ → FMP

→ FPTØ: SC FM ARØ-8[1]
ARØ(1): SCAD SC COMP SETUP

→ Ø.14Ø

→ FPT1: SC FM SCAD(J)
SCAD BR EN SET
-FP EXP ADD: SCAD DATA 1 EN
FP EXP ADD: SCAD DATA Ø EN
IR5(1): SCAD+1 EN SET

→ Ø.14Ø

→ FPT2: SC FM SCAD(J)
SCAD BR EN CLR
IR5(Ø): SC-EN
IR5(1): SC+EN
SCAD 2ØØ EN SET

→ Ø.14Ø

→ FPT3: BR1-8 FM BRØ(J)
AR1-8 FM ARØ(J)
SCAD SC+1 SETUP
FE FM SCAD[1]
IR5(Ø): SC CLR
IR5(1): SC FM SCAD(J)
AD AR-EN CLR
AD CRY 36 CLR

→ Ø.Ø65

IR5(Ø) → TO FMT 1
IR5(1) → TO FDT 1

NOTE : FP EXP ADD = IR5 + BRØ

FLT MPY

FROM FPT3 DEL IR5(Ø) → FMT1: SC FP SETUP; 745
AD BR+EN SET

FROM ETØ ∧ IR XMUL → Ø.Ø9Ø →

→ MSTØ: MQ FM AD(J)
BR FM AR(J)
ARØ(1) ∧ BRØ(1): MPF 2 SET

→ Ø.115

→ MST 1: MSF1 SET; AR MQ SH RT AT SCT3, IF MQ35(1) ∧ MQ34(Ø): AD MD +
IF MQ35(Ø) ∧ MQ34(1): AD MD -
AD BR+EN CLR
MQ35(1): AD BR-EN SET
AD CRY 36 SET
MQ35(Ø): AD BR-EN CLR
AD CRY 36 CLR
TO SC SUBR
AR CLR

→ TO SCTØ

SCT4: MSF1 CLR → Ø.165

MPF1(1) → TO MPT 2

IR FMP → FMT3: AR FM AD(J)
SC FM FE[1]
MQ35 CLR

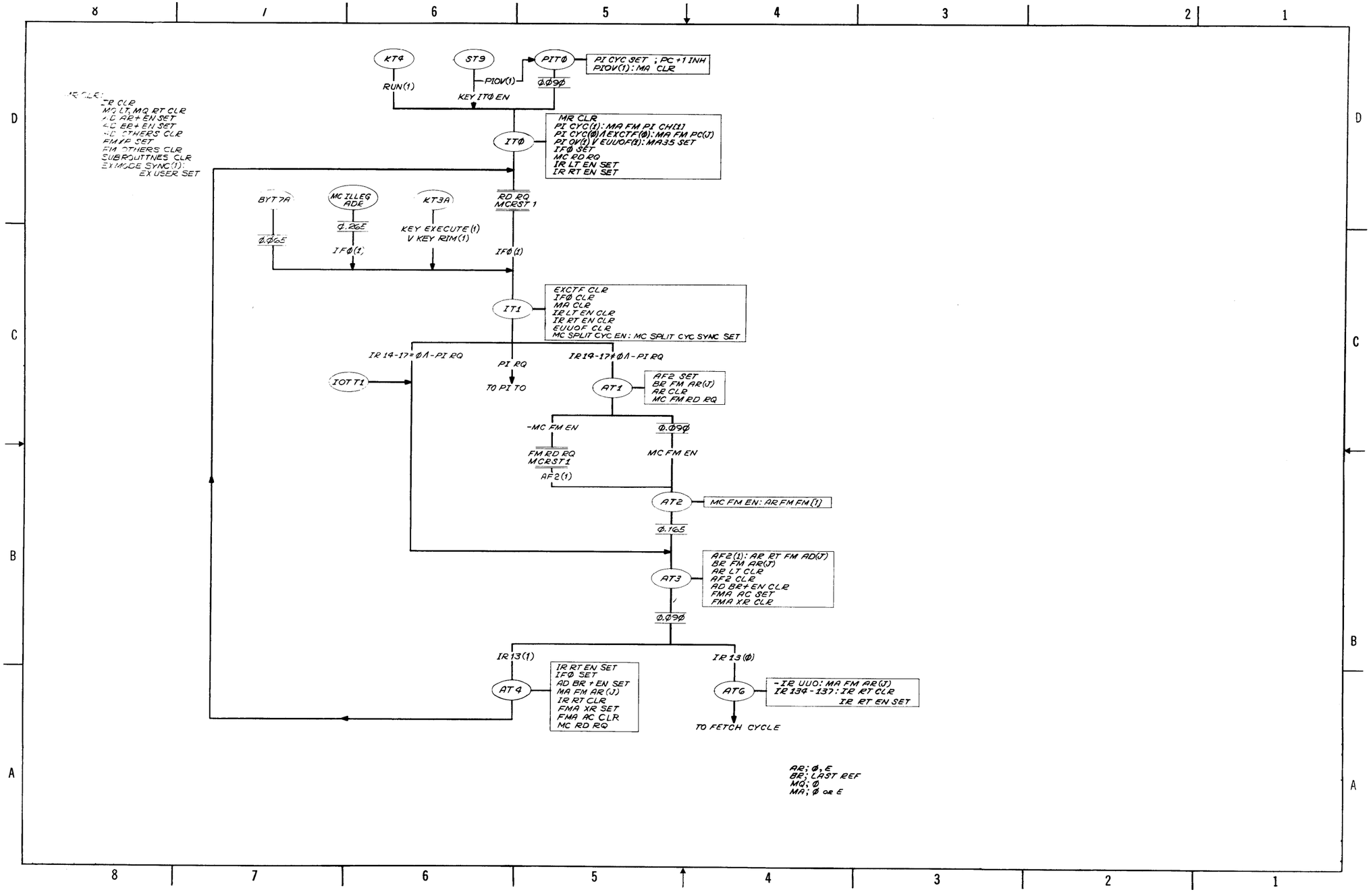
→ TO NRTØ

INSTRUCTION	FSC FLOATING SCALE (132)	DFN DOUBLE FLOATING NEGATE (131)
INITIAL SWITCHES	ST INH E LONG	E LONG FCE PSE EFØ LONG
INITIAL REGISTERS	BE; Ø, E AE; C(AC) SC; Ø	BR; C(E) AE; C(AC) SC; Ø
FT9		AD MINUS BE SCAD SC+BR SETUP
ETØ	SC FM BR(1); E BE FM AR(J) AEØ(Ø): SCAD SC+BR SETUP AEØ(1): SCAD SC-BE SETUP ;SC+1 EN INH,	SC FM SCAD(J) BR FM AR(J) AR FM AD(J) AD 9-35 # Ø; AD CRY 36 CLR SCAD ALL DTS
ET1	AR 1-8 FM AEØ(J)	AEØ-8 FM SCAD(J)
ET2	SC FM SCAD(J)	BR FM AR(J) AR FM AD(J)

TO NRTØ

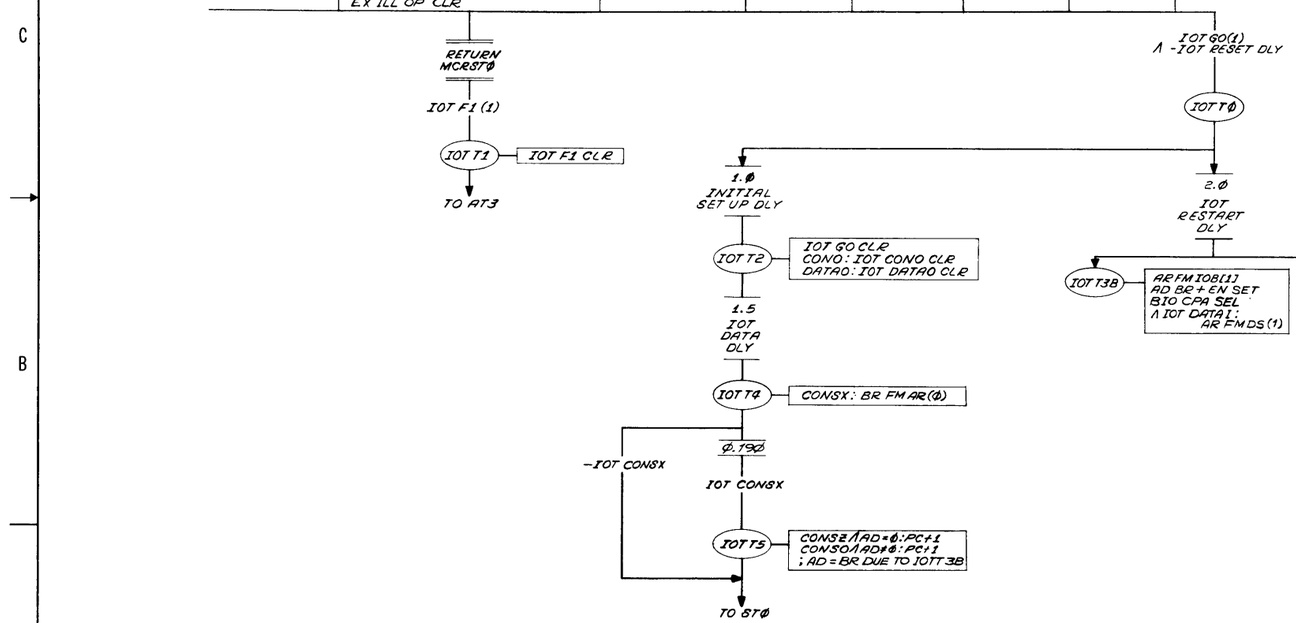
FINAL SWITCHES		SAR ≠ BR

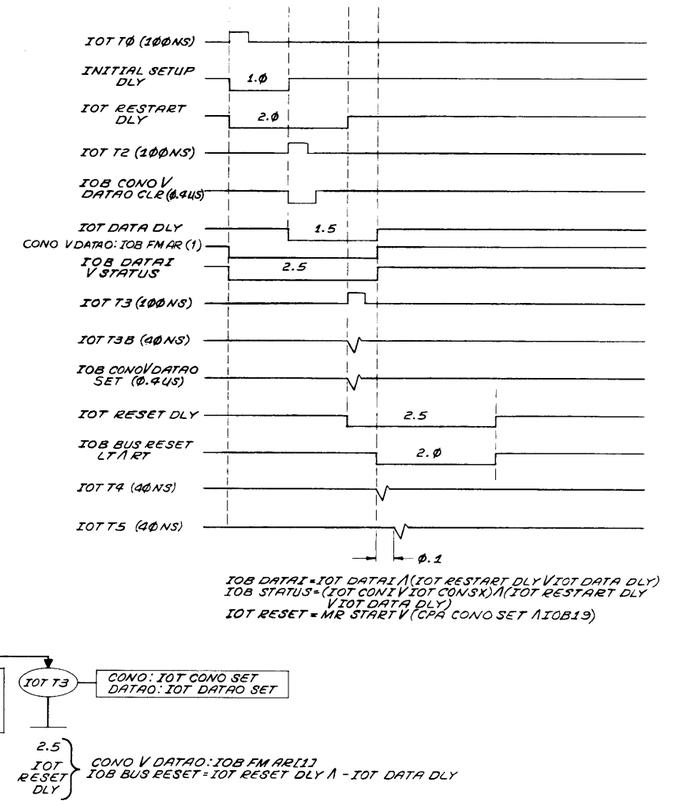
D-FD-KA10-0-FSDN Floating Scale and Double Floating Negate



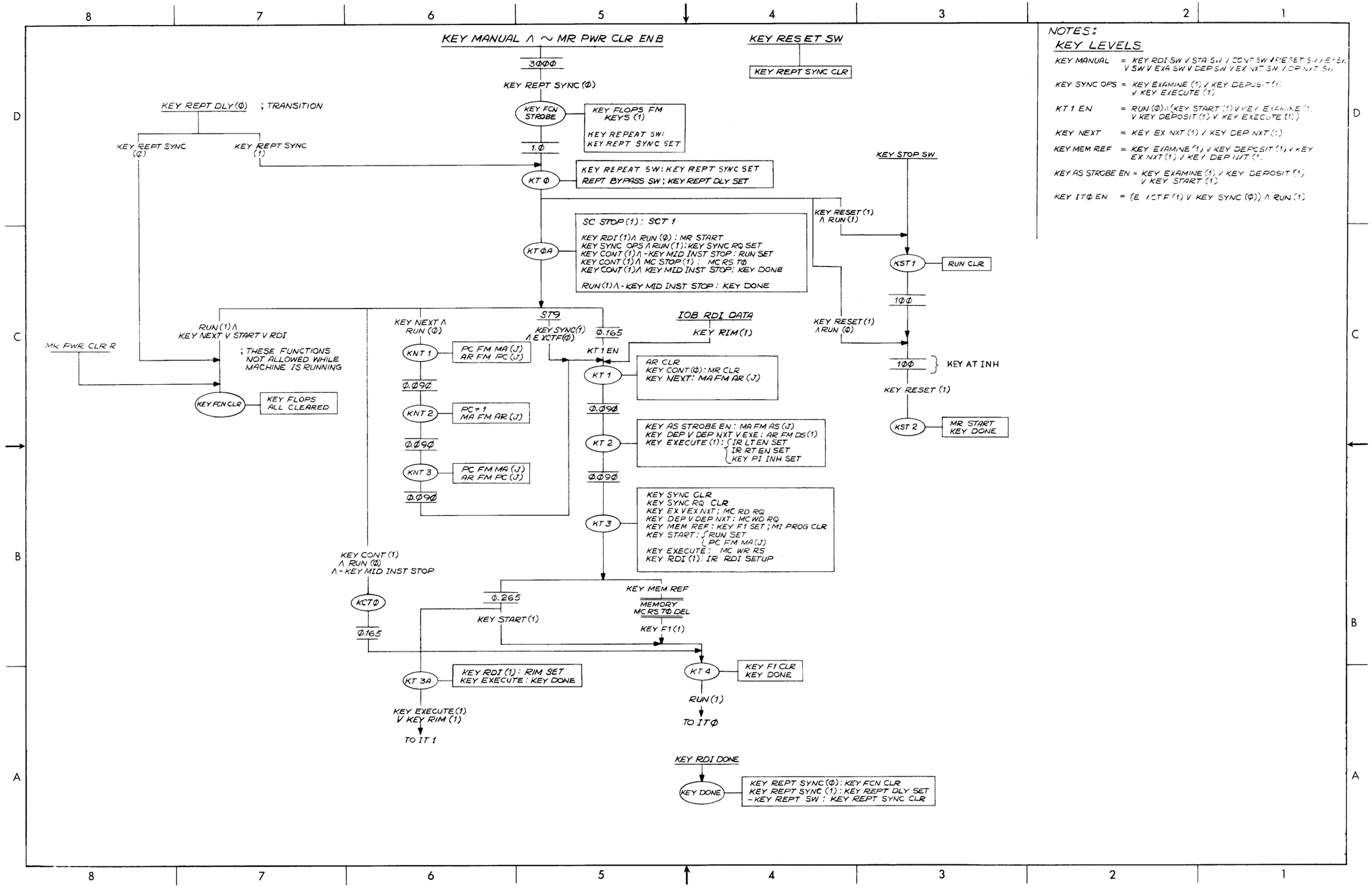
D-FD-KA10-0-IAC Instruction and Address Cycles

INSTRUCTION	BLKO/BLKI	CONO	CONI	CONSX	DATAO	DATAI
INITIAL SWITCHES	FAC INH FCE PSE EFØ LONG PC+1 INH ST INH	FAC INH ST INH	FAC INH ST INH	FAC INH ST INH	FAC INH FCE ST INH	FAC INH ST INH
INITIAL REGISTERS	AR;C(E);OLD POINTER	AR;Ø,E BR;Ø,E	BR;Ø,E	BR;Ø,E	AR;C(E)	
FINAL SWITCHES	SAC INH	SAC INH	SAC INH SCE	SAC INH	SAC INH	SAC INH SCE
FT9	AD+1 BOTH					
ETØ	AR FM AD(J); NEW POINTER AD CRY Ø(Ø) Λ PI CYC (Ø): PC+1 AD CRY Ø(1) APR OV EN: PI OV SET IOT F1 SET MC RD/WR RS IR 12 SET EX ILL OP CLR	ARLT FM ARRT(J) IOT GO SET	AR CLR IOT GO SET	AR CLR IOT GO SET	IOT GO SET	AR CLR IOT GO SET





D-FD-KA10-0-IOTF In-Out Transfer Control Flow



NOTES:

KEY LEVELS

KEY MANUAL = KEY RDI SW V STA SW V CONT SW V RESET SW V EXA SW V EXA SW V DEP SW V EX NXT SW V DP NXT SW

KEY SYNC OPS = KEY EXAMINE (1) V KEY DEPOSIT (1) V KEY EXECUTE (1)

KT 1 EN = RUN (Ø) ∧ (KEY START (1) V KEY EXAMINE (1) V KEY DEPOSIT (1) V KEY EXECUTE (1))

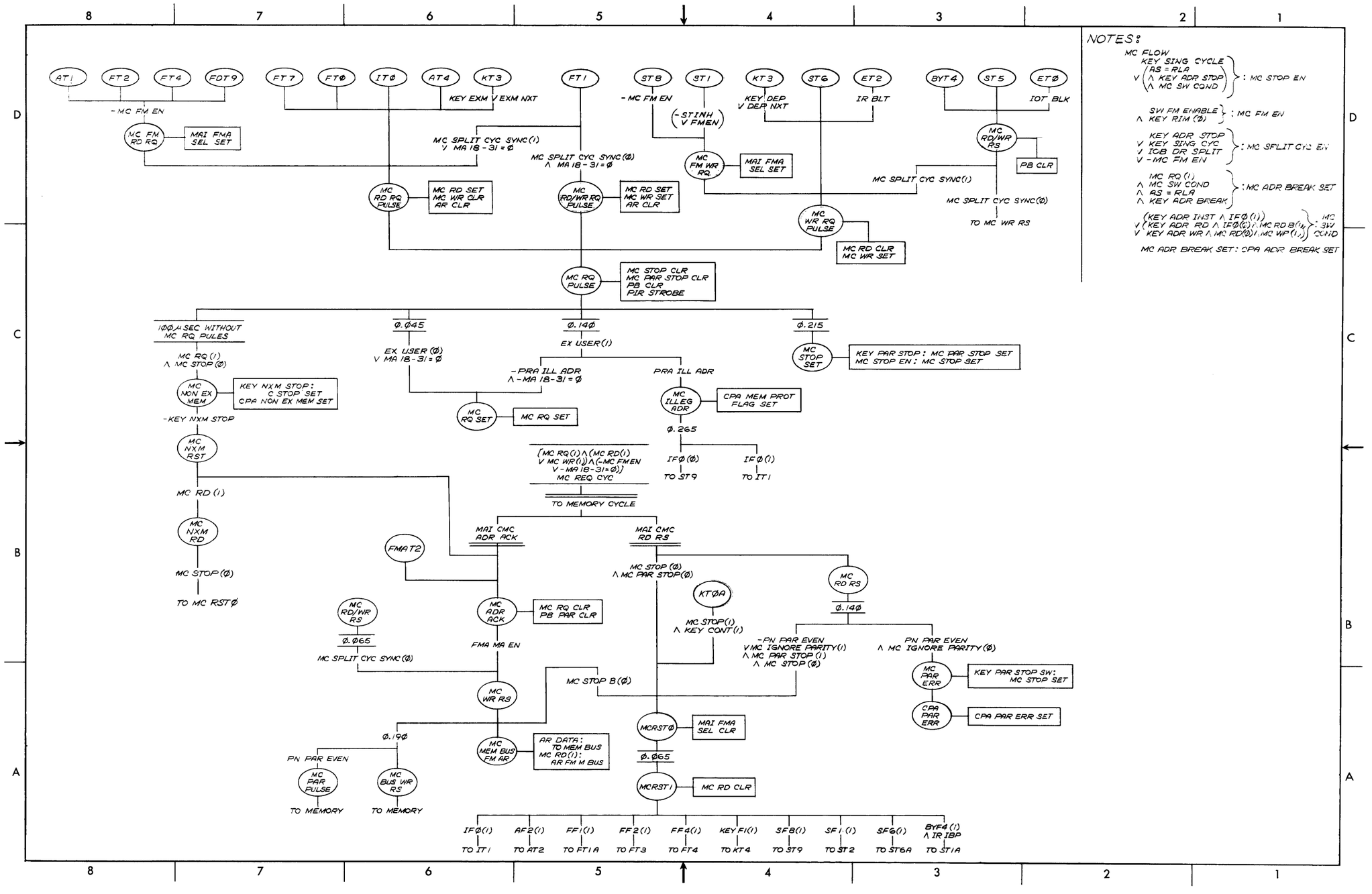
KEY NEXT = KEY EX NXT (1) V KEY DEP NXT (1)

KEY MEM REF = KEY EXAMINE (1) V KEY DEPOSIT (1) V KEY EX NXT (1) V KEY DEP NXT (1)

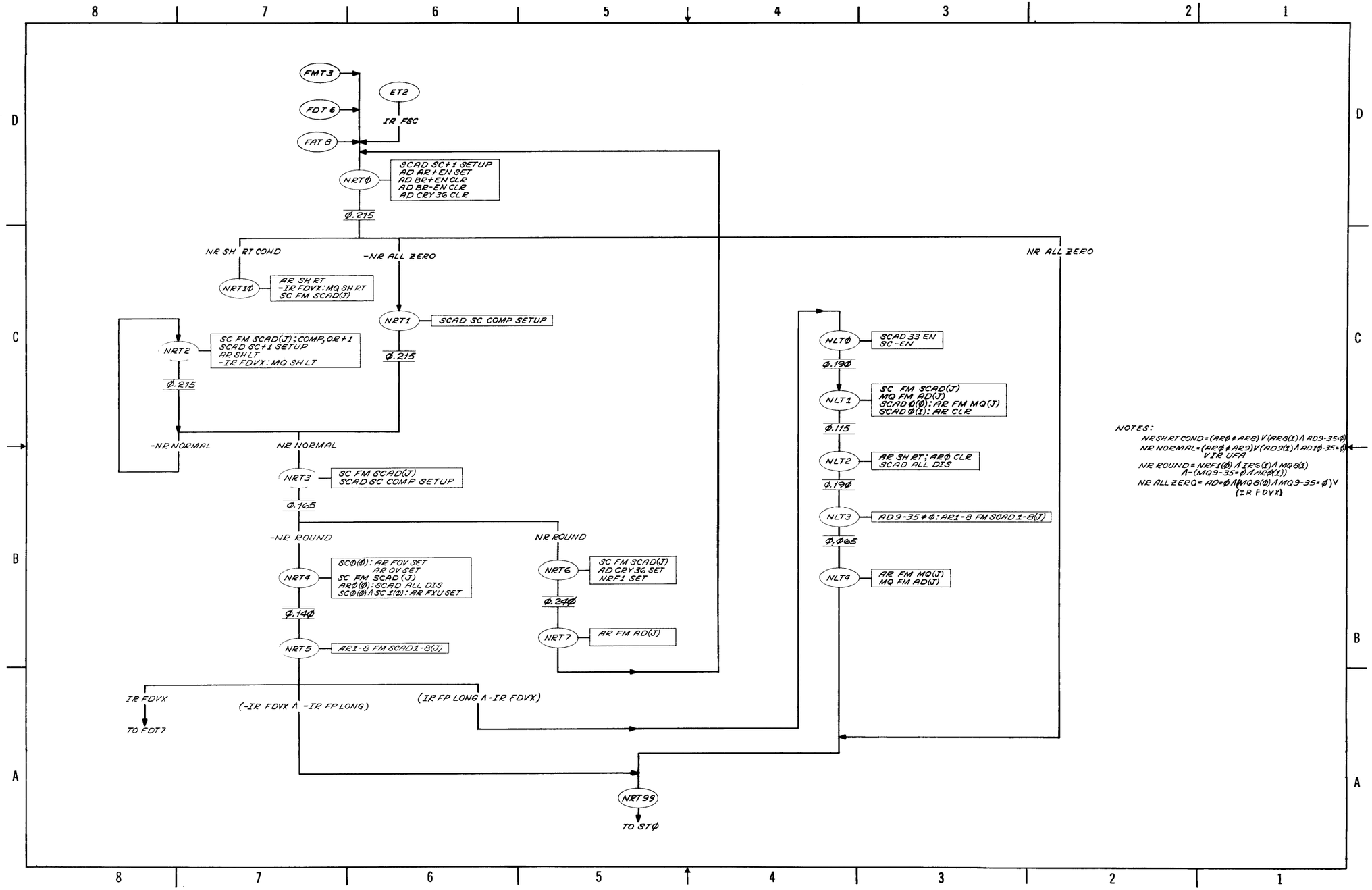
KEY AS STROBE EN = KEY EXAMINE (1) V KEY DEPOSIT (1) V KEY START (1)

KEY IT Ø EN = (E XCTF (1) V KEY SYNC (Ø)) ∧ RUN (1)

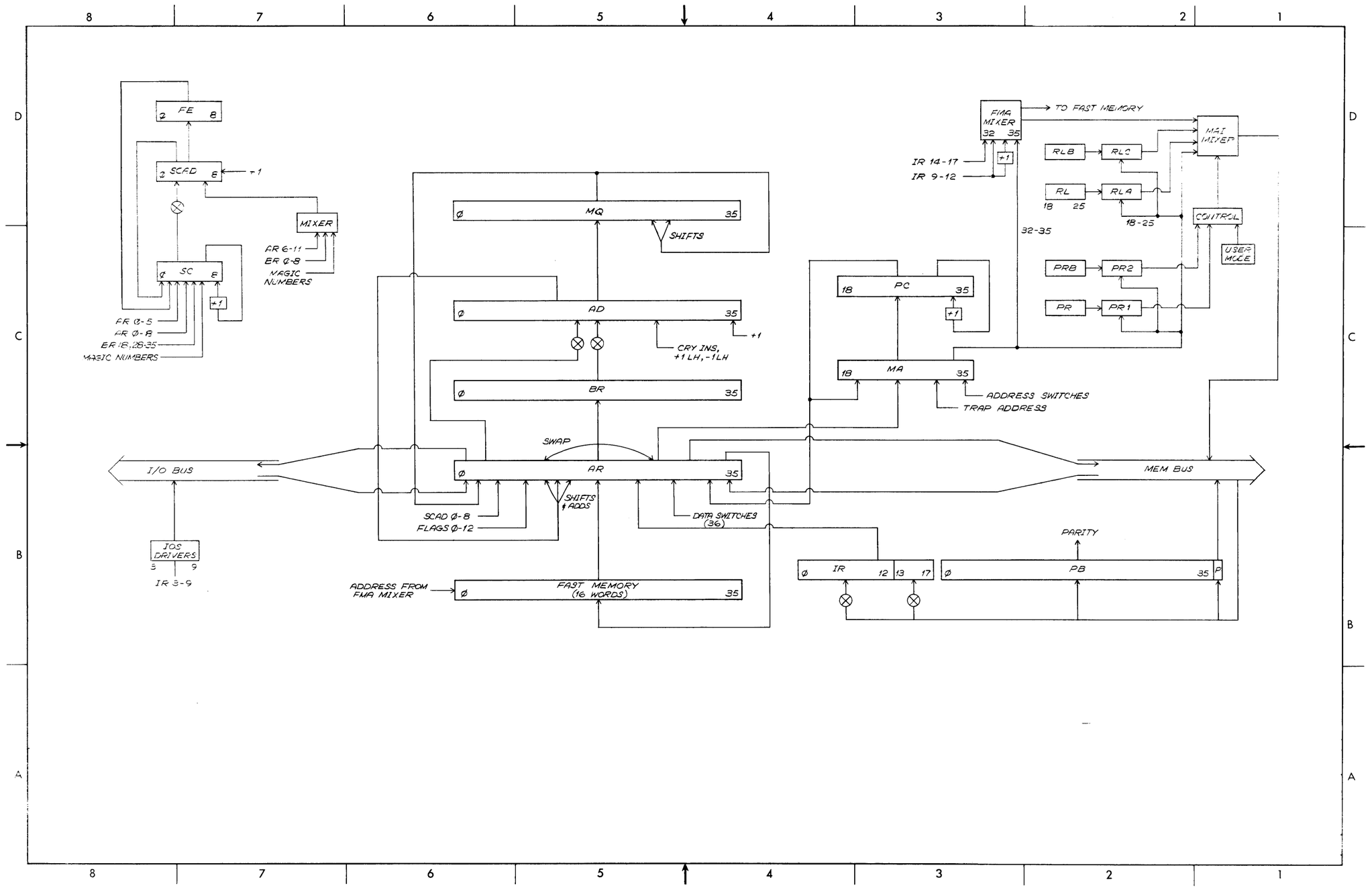
D-FD-KA10-0-KO Key Operations Flow Diagram



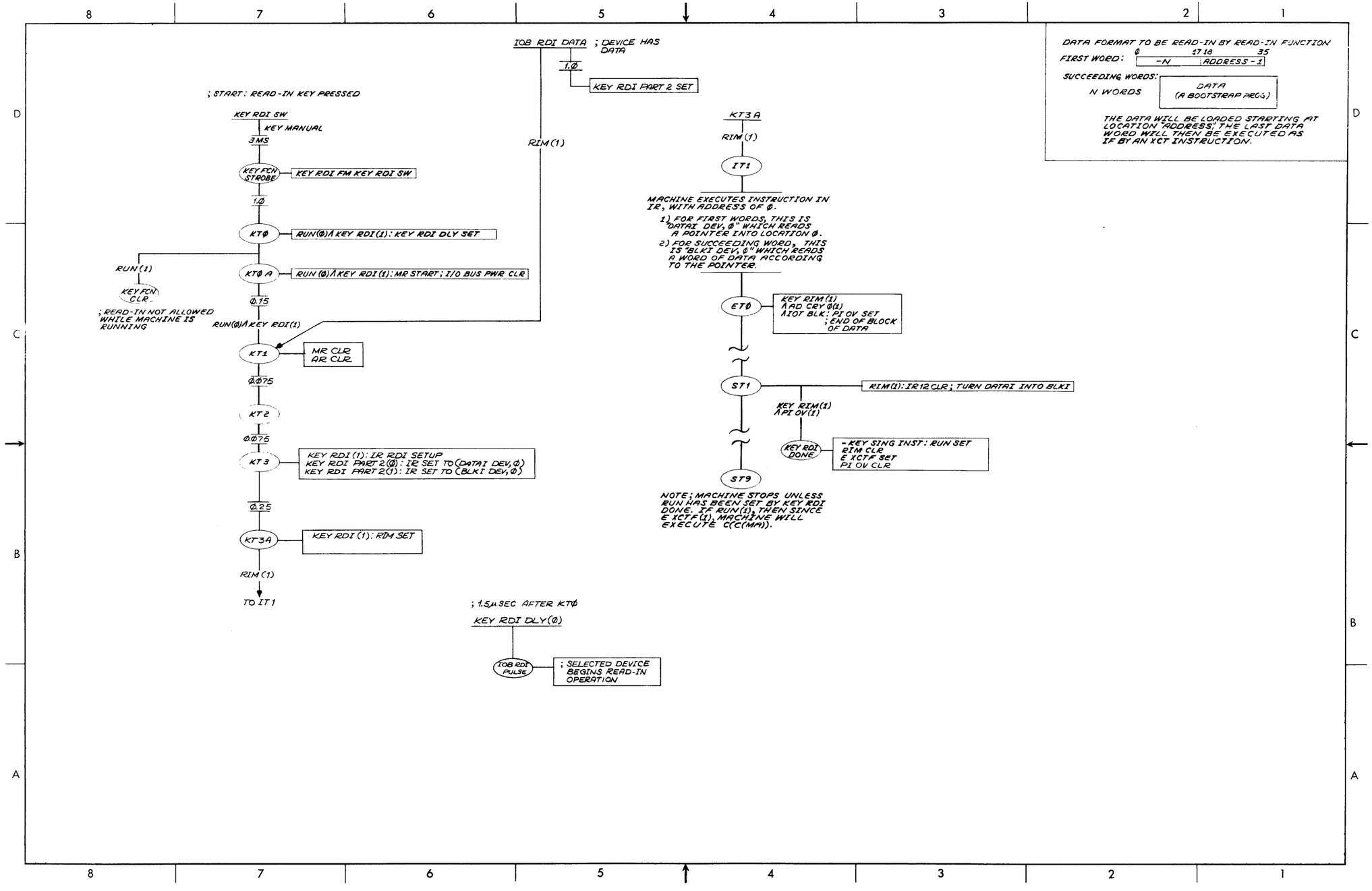
D-FD-KA10-0-MCFM Memory Control and Fast Memory Flow



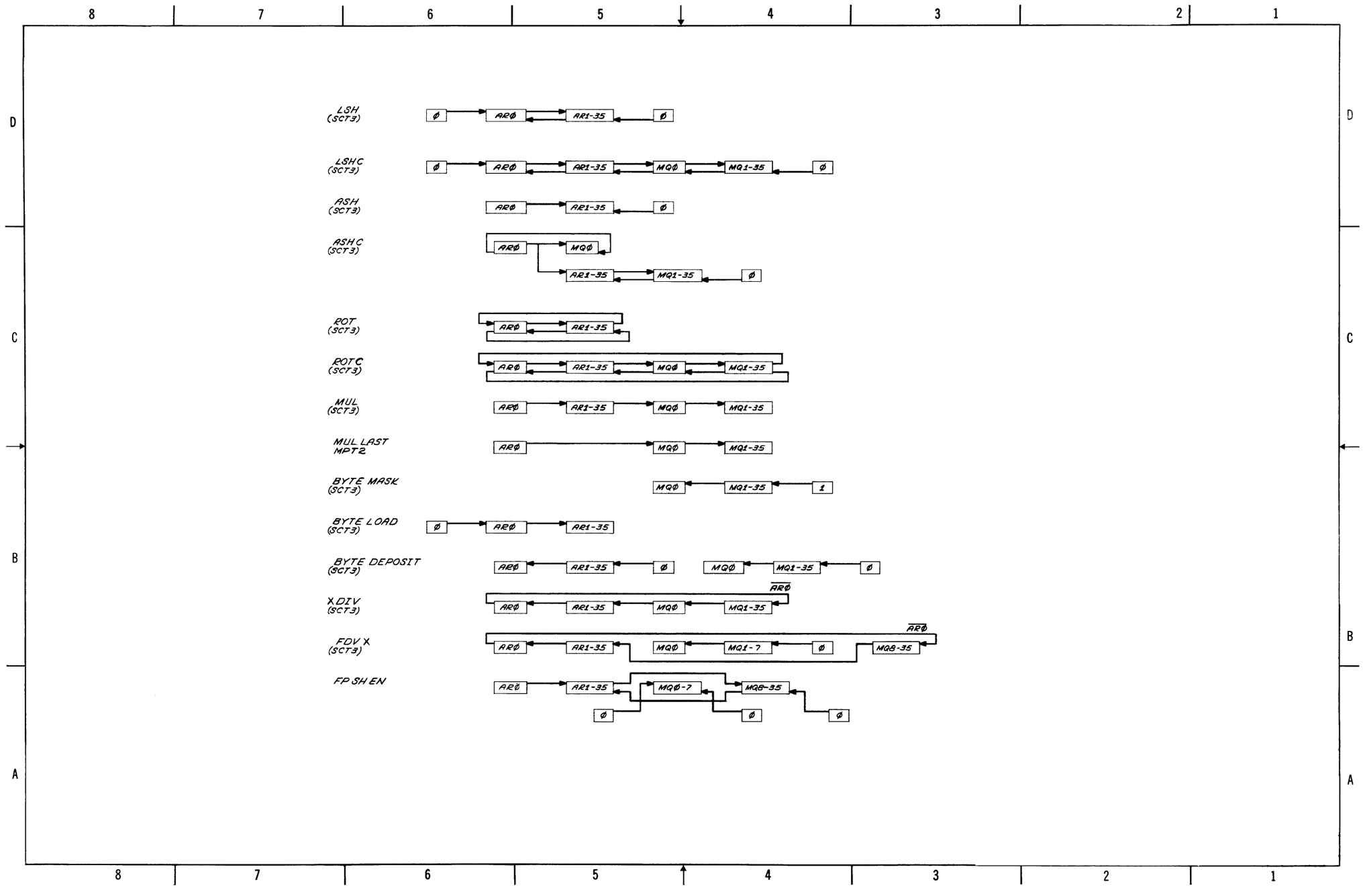
D-FD-KA10-0-NRF Normalize Return Subroutine



D-FD-KA10-0-REG KA10 Register Interconnections



D-FD-KA10-0-RIMF Read-in Function Isolated Flow



D-FD-KA10-0-SCAF Shift Count Action Flow

INSTRUCTION	BLT
INITIAL SWITCHES	PC+1 INH FC C ACLT ST INH E LONG
INITIAL REGISTERS	AR; TO, FROM BR; Ø, LAST MQ; DATA; C (FROM) MA; FROM PC; ADDRESS (BLT)
FT9	AD AR+EN SET AD+1 BOTH
ETØ	AR SWAP; FROM, TO
ET1	MA FM AR(J); TO
ET2	AR FM MQ(J); DATA MQ FM AD(J); (FROM+1, TO+1) AD+1 LH CLR MC WR RQ BLT F1 SET

RETURN
MCRST1 ∧ BLT F1(1)

BLT T1 — BLT F1 CLR, AR LT CLR, AR RT FM MQ(J), AD BR-EN SET, AD CRY 36 CLR

Ø.335

AD 17(Ø) → BLT T2 — PC+1 → TO ST1A

AD 17(1) → BLT T3 — AD BR-EN CLR, AR FM MQ(J); (FROM+1, TO+1)

Ø.Ø9Ø

-PIRQ → TO FT6

PI RQ → TO STØ

BYT 7, SRT 1, ETØ (SC SBR(ETØ))
DST 2
FAT 5, MST 1

SCTØ — SCAD SC+1 SETUP, AD AR+EN SET, AD AR-EN CLR, SC STOP SW: SC STOP SET

Ø.165

KTØ / SC STOP(1)

SC STOP(Ø) ∧ SCØ(1)

SC Ø(Ø) → SCT4 — MSF1 CLR, SC STOP CLR → RETURN

SCT1 — ; SC+1

AD BR+EN(Ø) ∧ AD BR-EN(Ø)

AD BR+EN(1) ∨ AD BR-EN(1)

SCT2

Ø.28Ø SEE NOTE 2

SCT3 — AR, MQ, SHIFT; AS CONTROLLED BY INST.
AD MD+: AD BR+EN SET
-AD MD+: AD BR+EN CLR
AD MD-: AD BR-EN SET
: AD CRY 36 SET
-AD MD-: AD BR-EN CLR
AD CRY 36 CLR

Ø.75Ø SEE NOTE 1

AD MD+ = (MSF1(1) ∧ MQ 34(Ø) ∧ MQ 35(1)) ∨ [DSF1(1) ∧ (ADØ(1) ∧ BRØ(Ø)) ∨ (ADØ(Ø) ∧ BRØ(1))]

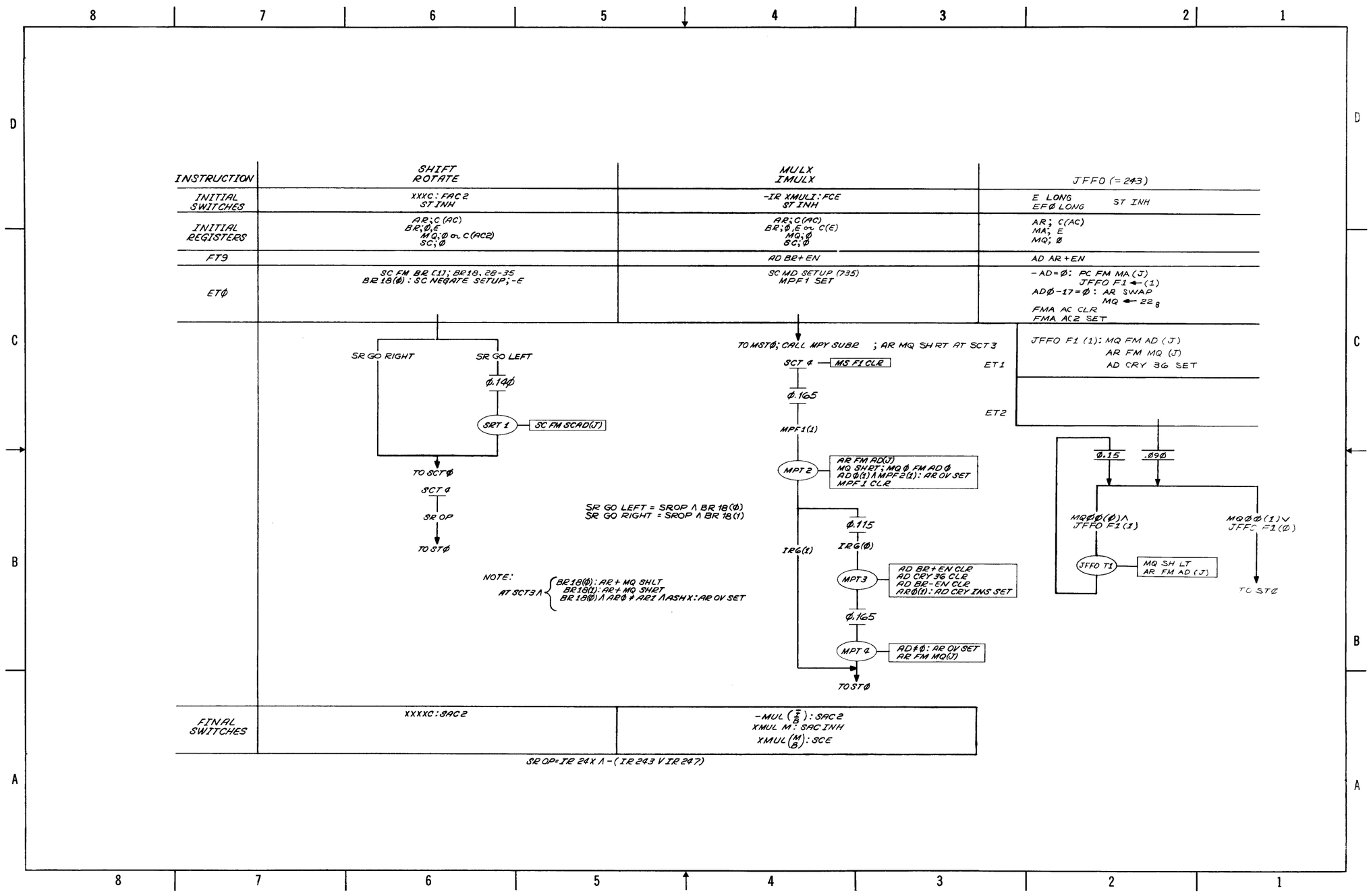
AD MD- = (MSF1(1) ∧ MQ 34(1) ∧ MQ 35(Ø)) ∨ [DSF1(1) ∧ (ADØ(Ø) ∧ BRØ(Ø)) ∨ (ADØ(1) ∧ BRØ(1))]

SUMMARY

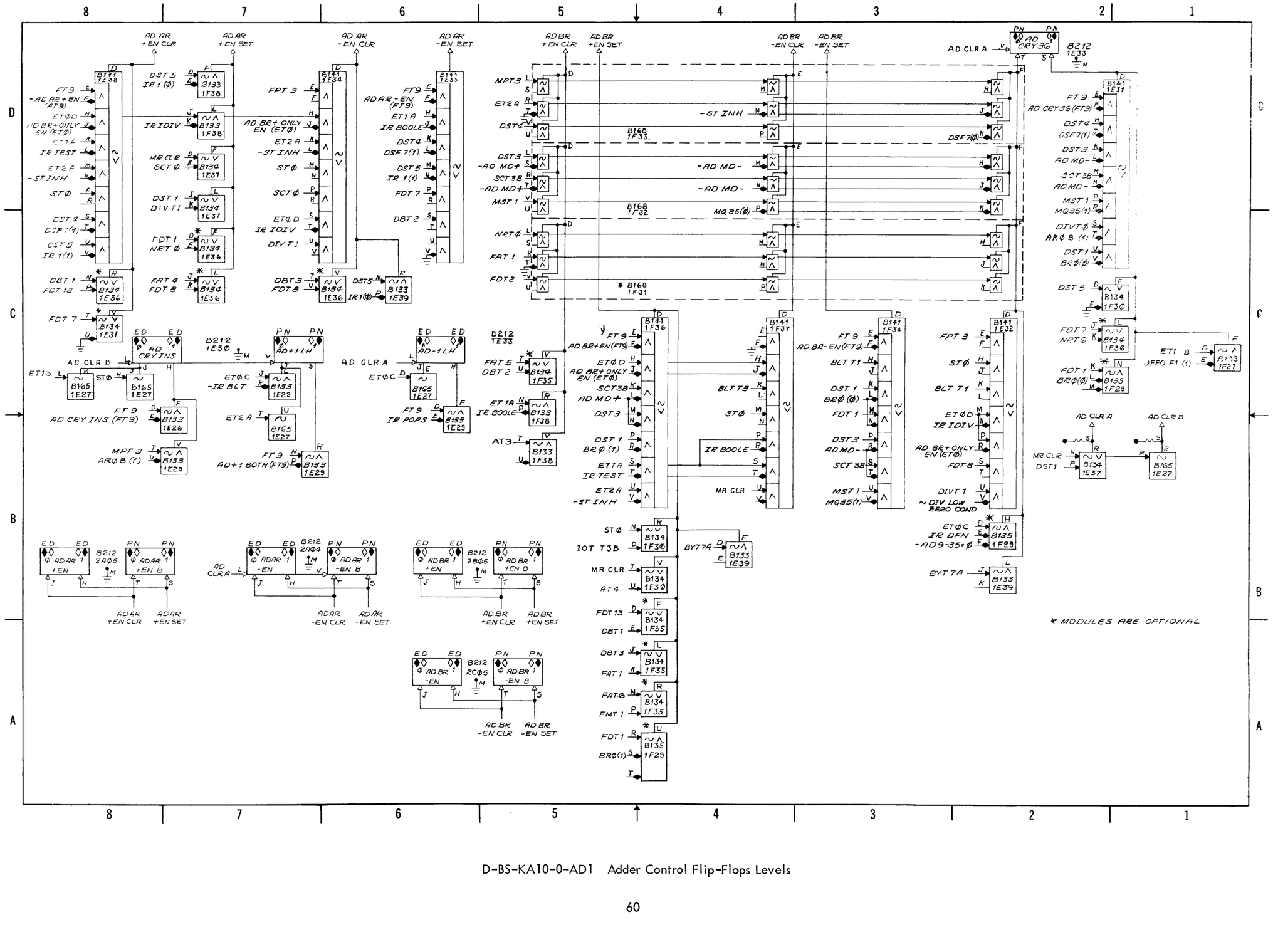
BR; (Ø, FINAL)
AR; (NEW FROM, TO)
MA; (OLD, TO)
MQ; (NEW FROM, TO)

NOTES:
1. THIS IS THE SHIFT TIME LOOP DELAY.
   THE DELAY IS ADJUSTED FOR 150 NS BETWEEN SCT3 WHILE DOING ROTATES.
   THIS DELAY MUST BE SETUP BEFORE SCT2 DELAY
2. THIS IS THE ADD TIME LOOP DELAY FOR MUL & DIV.
   THE DELAY IS ADJUSTED FOR 280 NS BETWEEN SCT2 PULSES.
   THIS DELAY IS SET AFTER THE SCT3 DELAY.

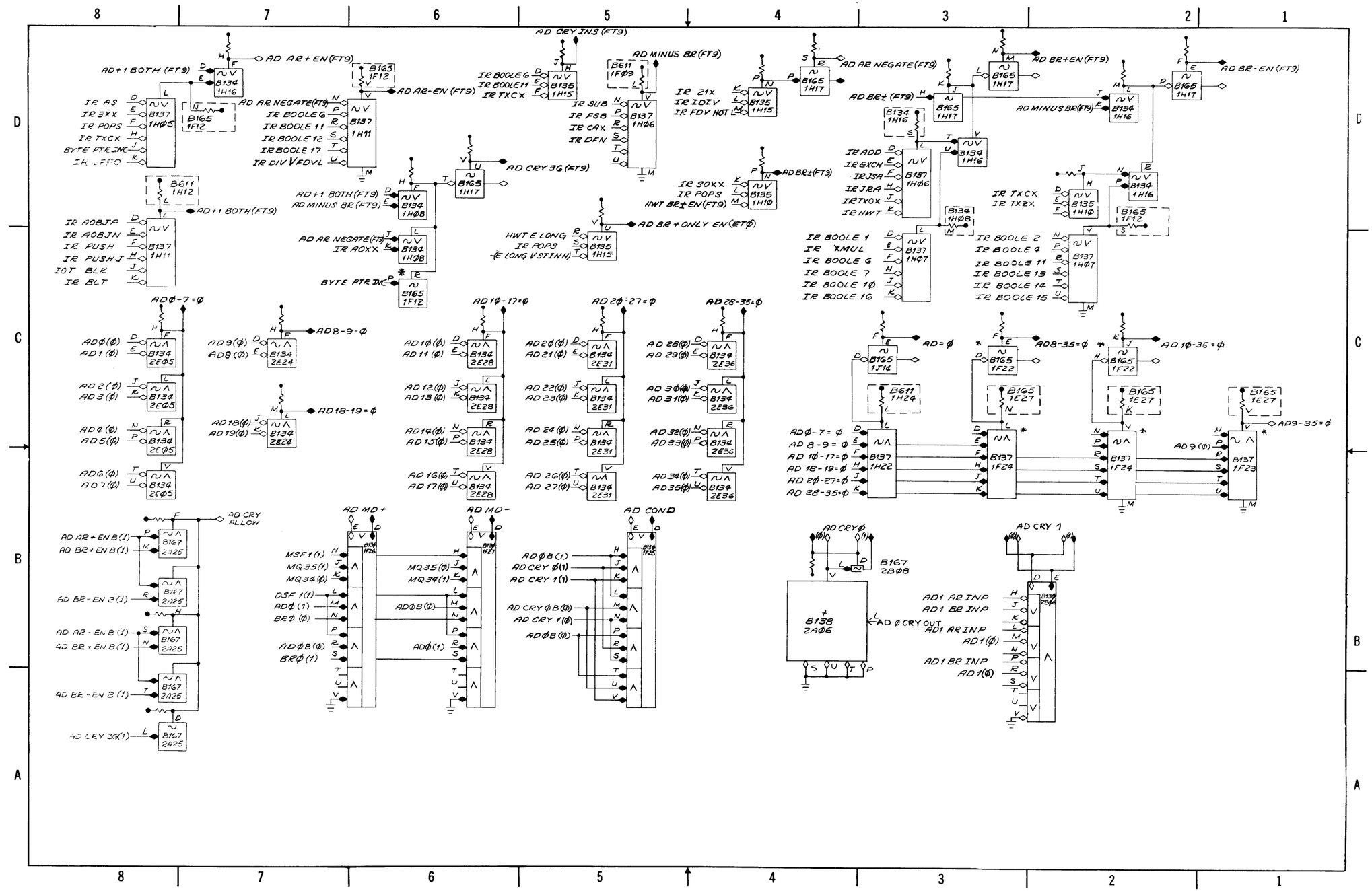
D-FD-KA10-0-SCBT Shift Count Subroutine and BLT Flow



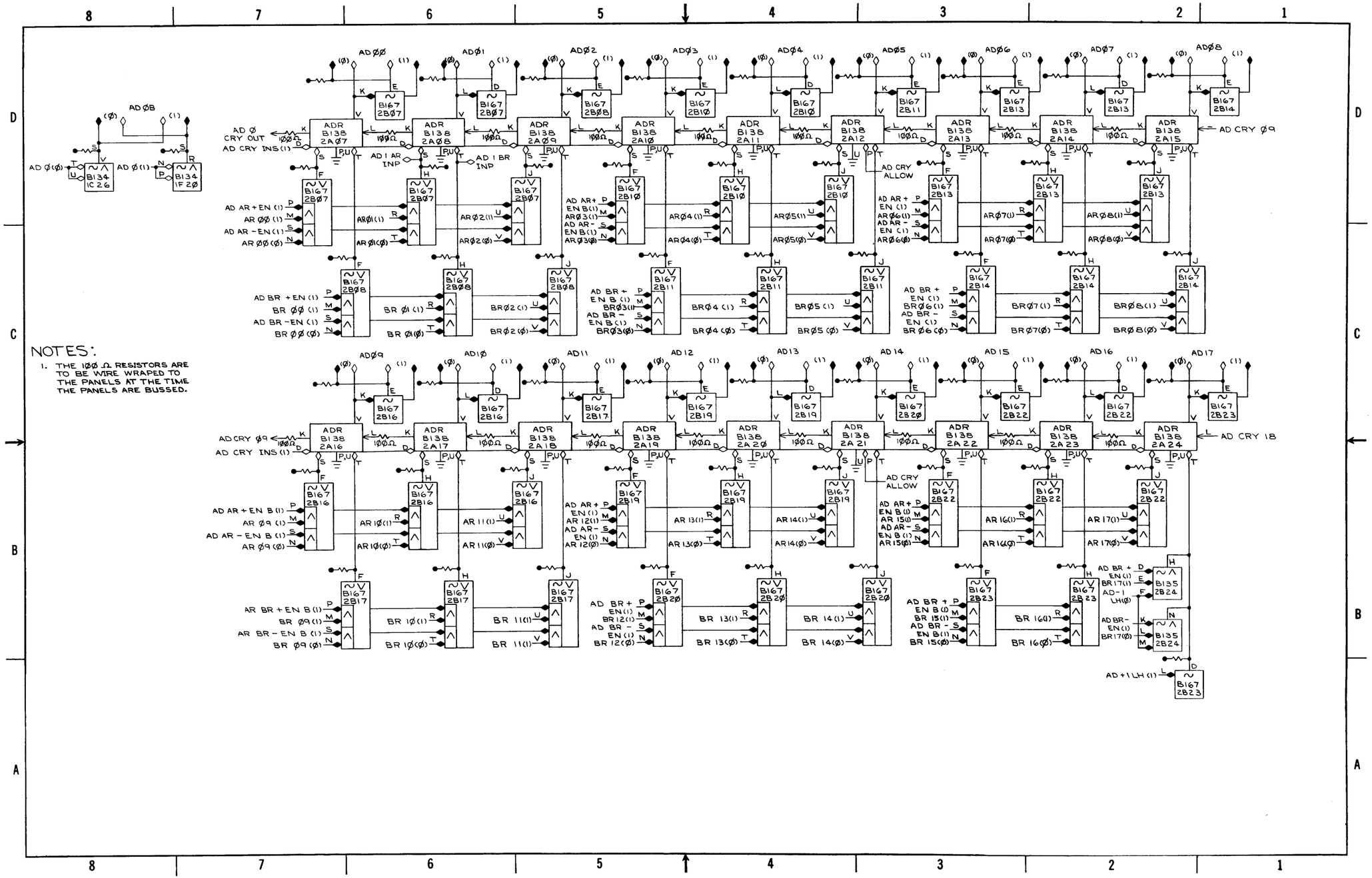
D-FD-KA10-0-SMF Shift and MUL and JFFO Flow



D-BS-KA10-0-AD1 Adder Control Flip-Flops Levels



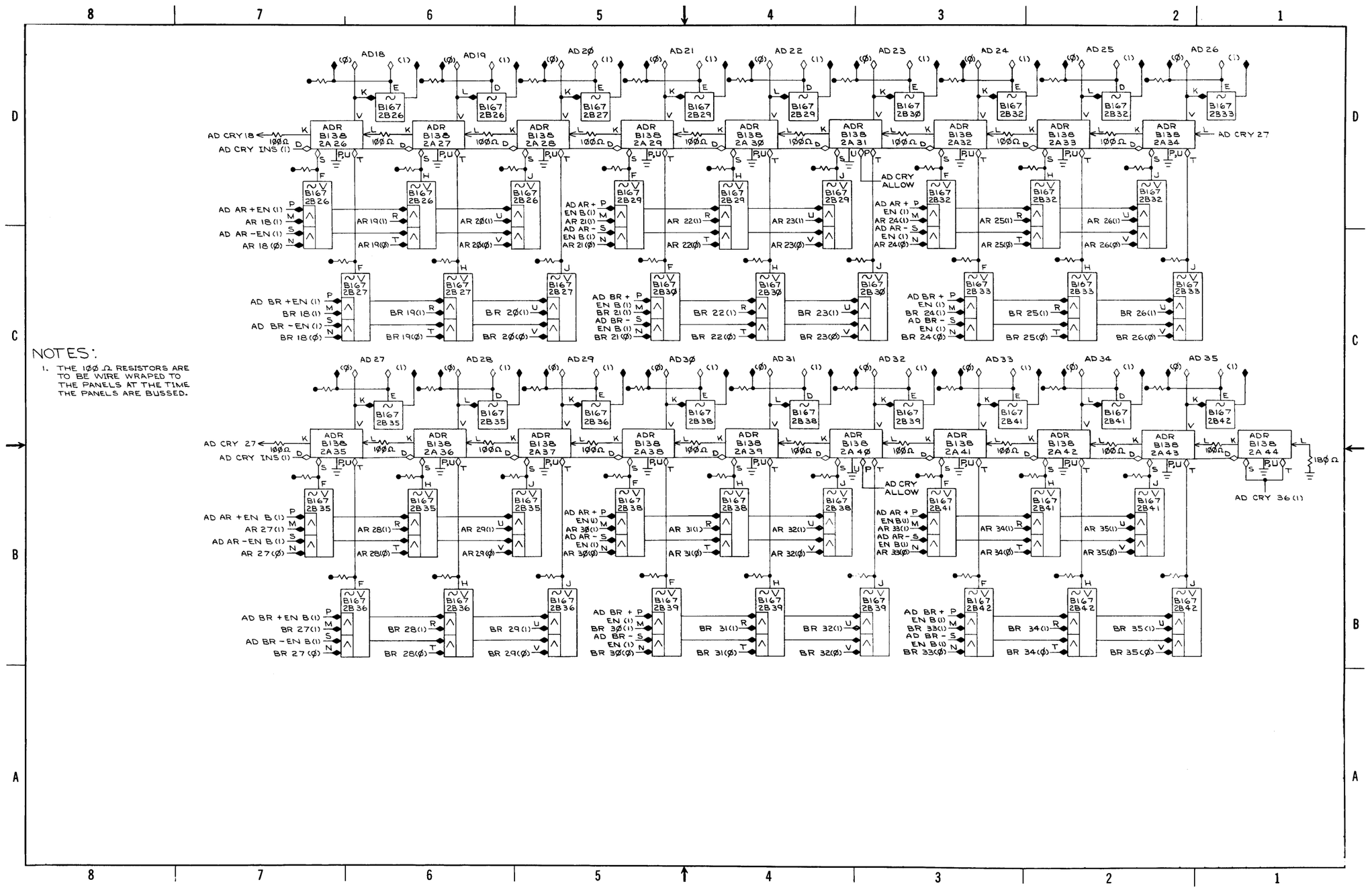
D-BS-KA10-0-AD2 Adder Control Levels



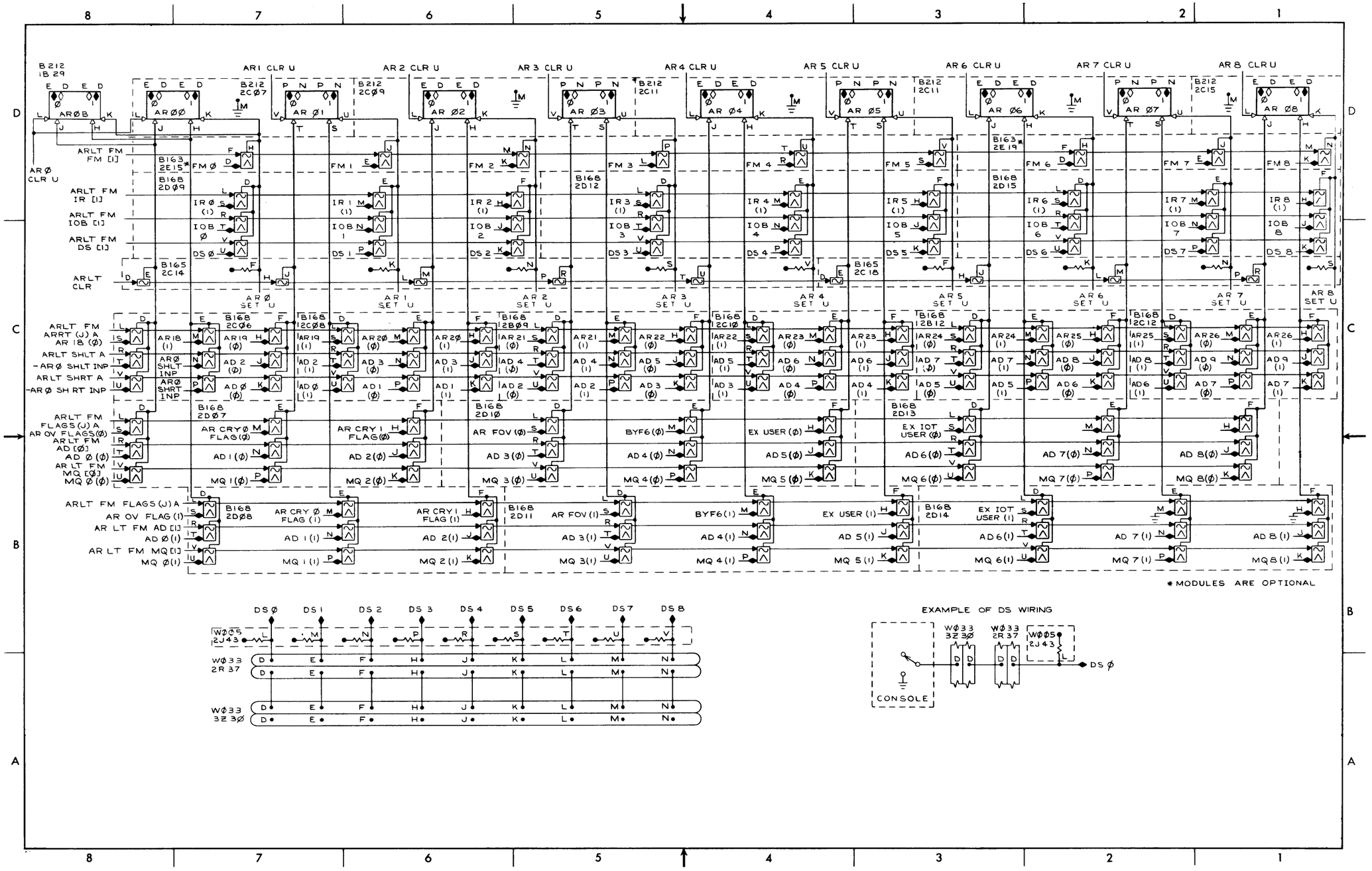
D-BS-KA10-0-AD3 Adder Left Half

NOTES:

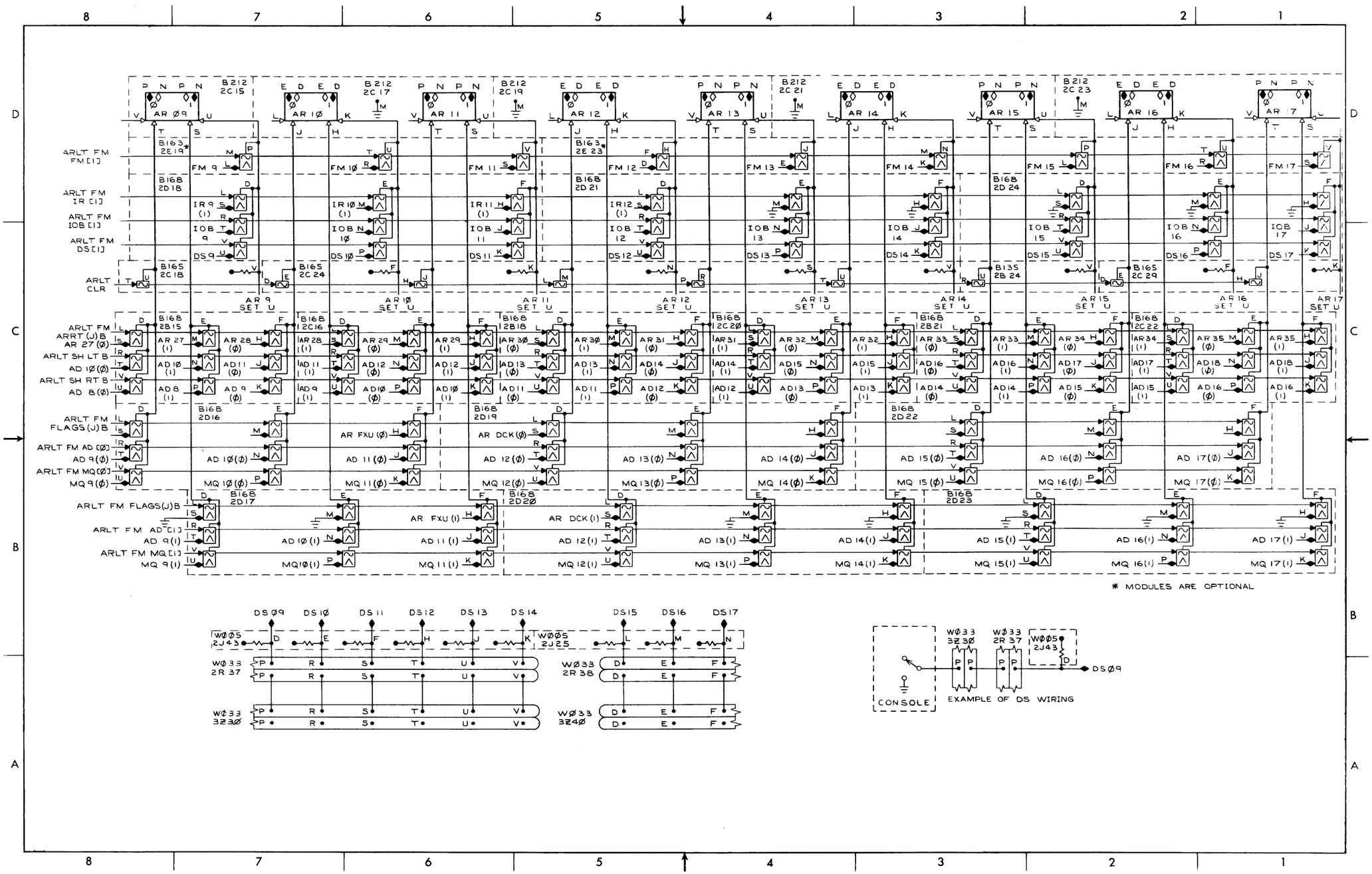
1. THE 100 Ω RESISTORS ARE TO BE WIRE WRAPED TO THE PANELS AT THE TIME THE PANELS ARE BUSSED.



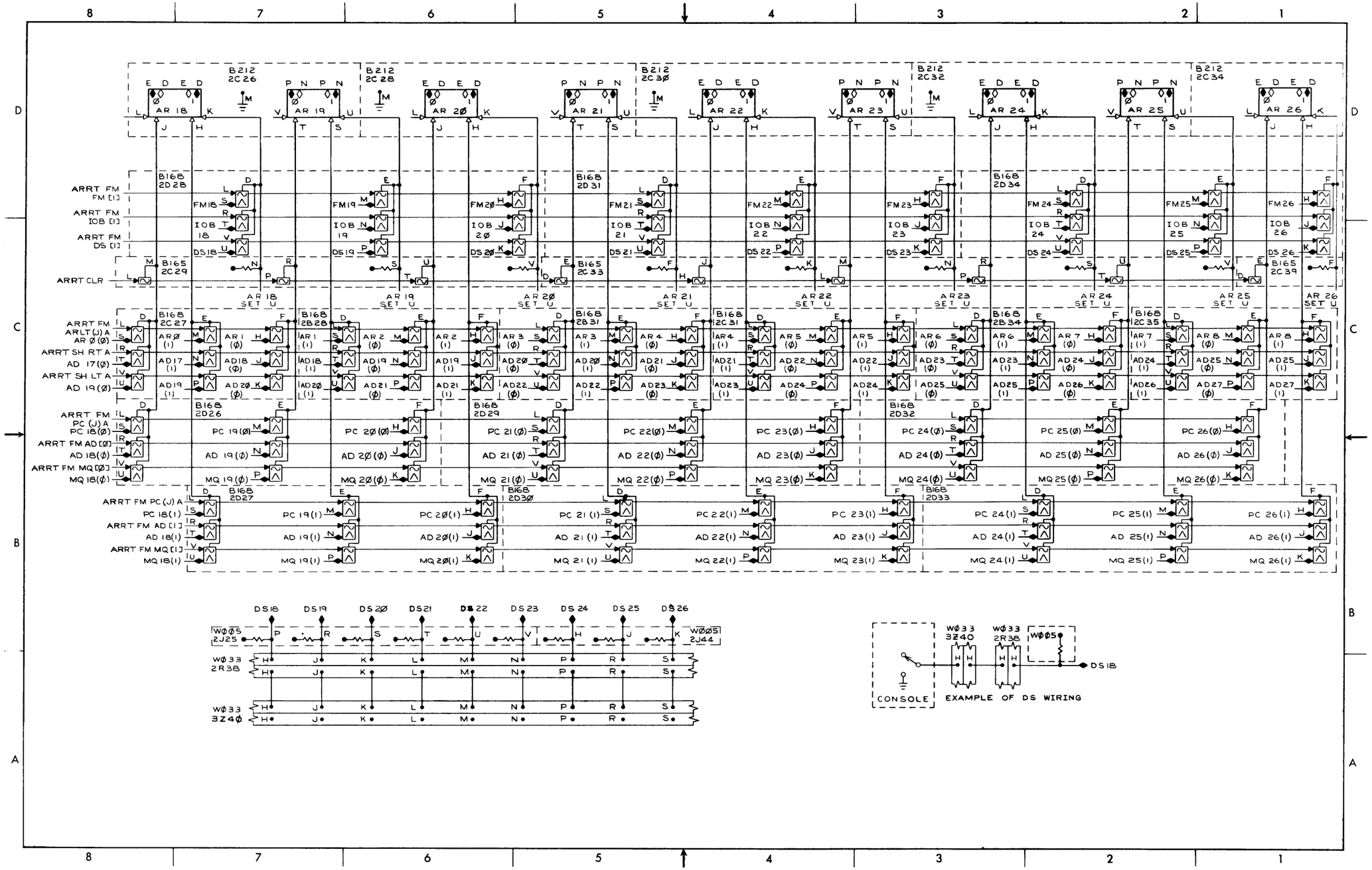
D-BS-KA10-0-AD4 Adder Right Half



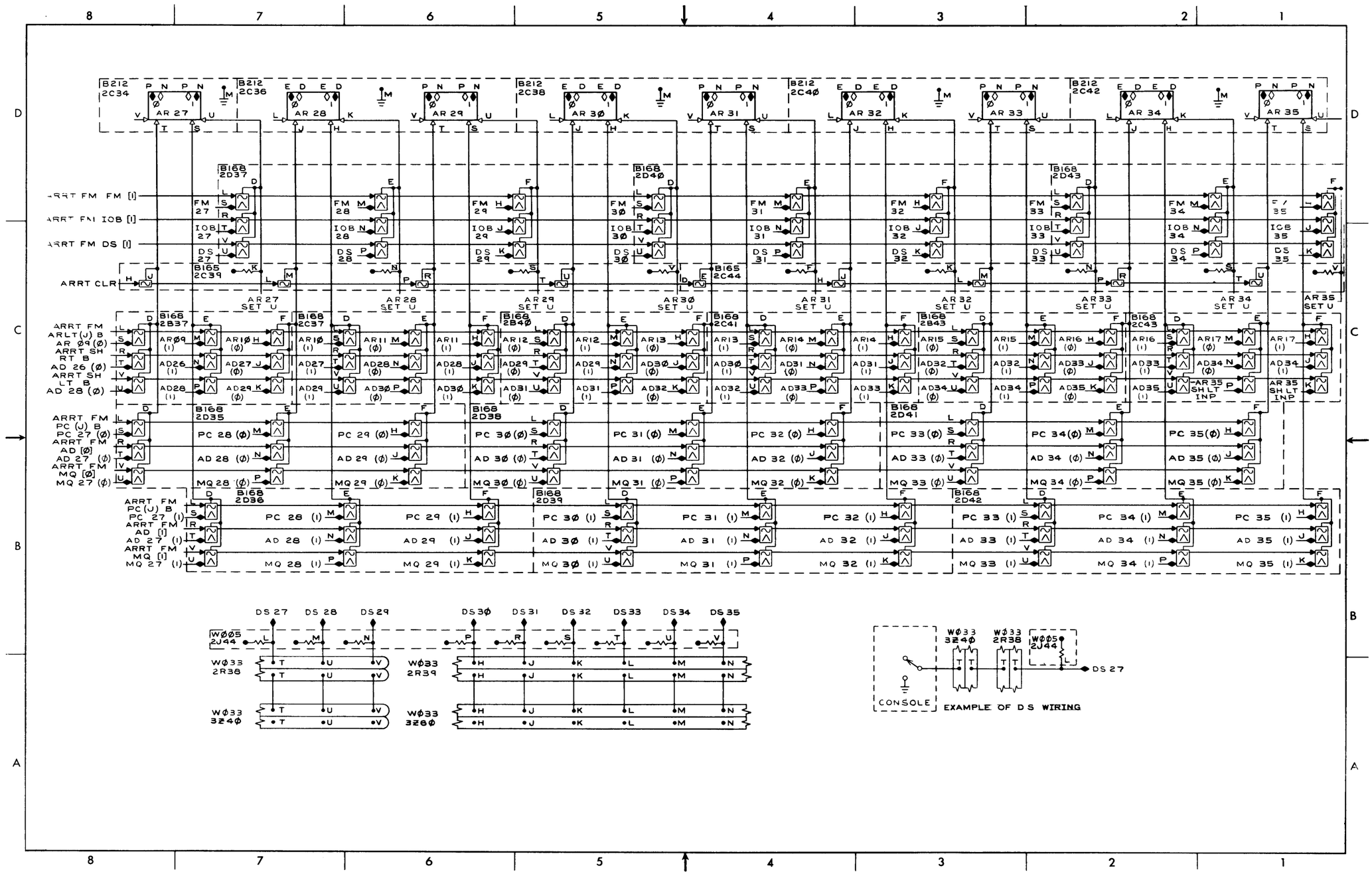
D-BS-KA10-0-AR1 AR Register



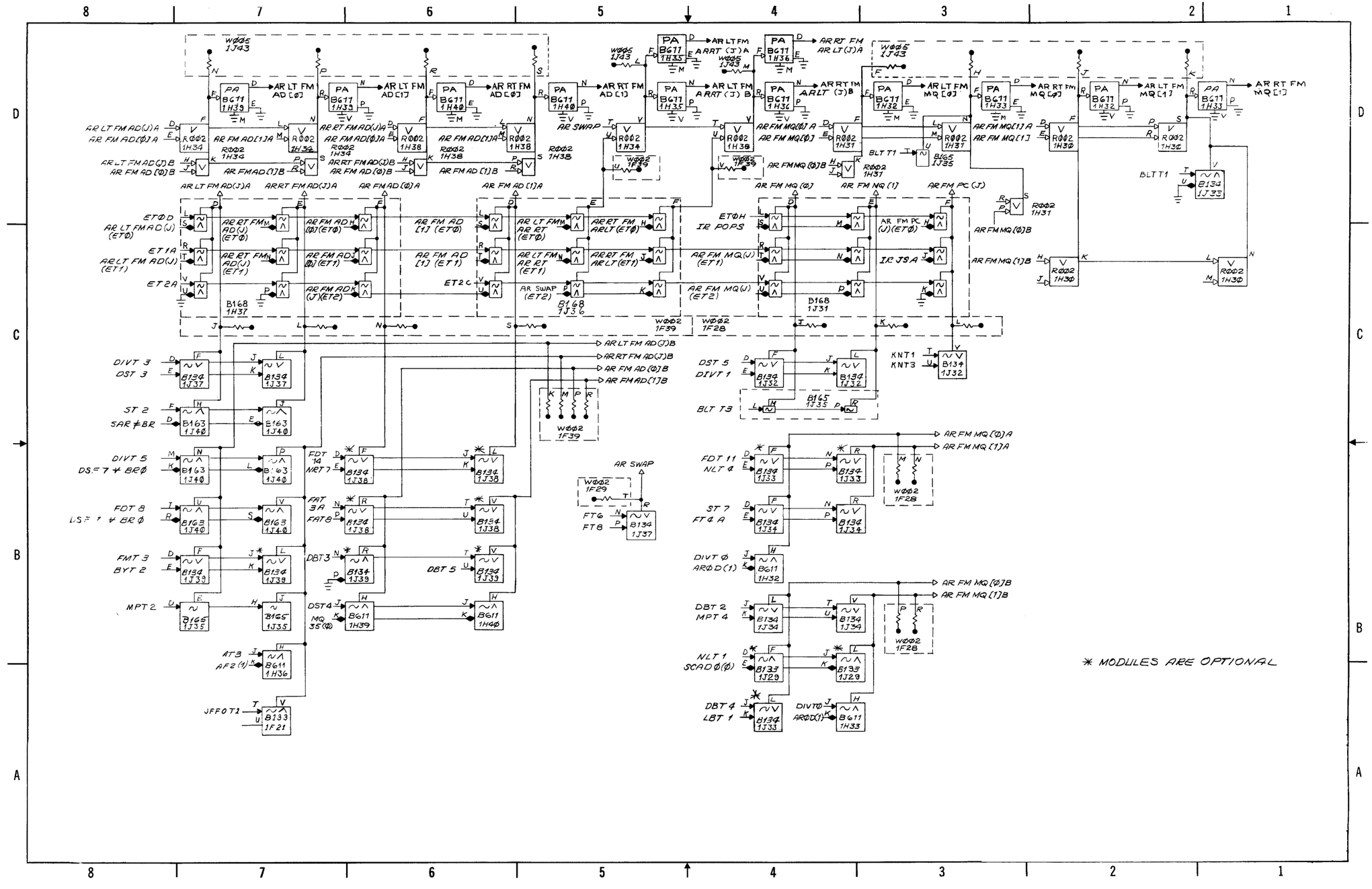
D-BS-KA10-0-AR2 AR Register



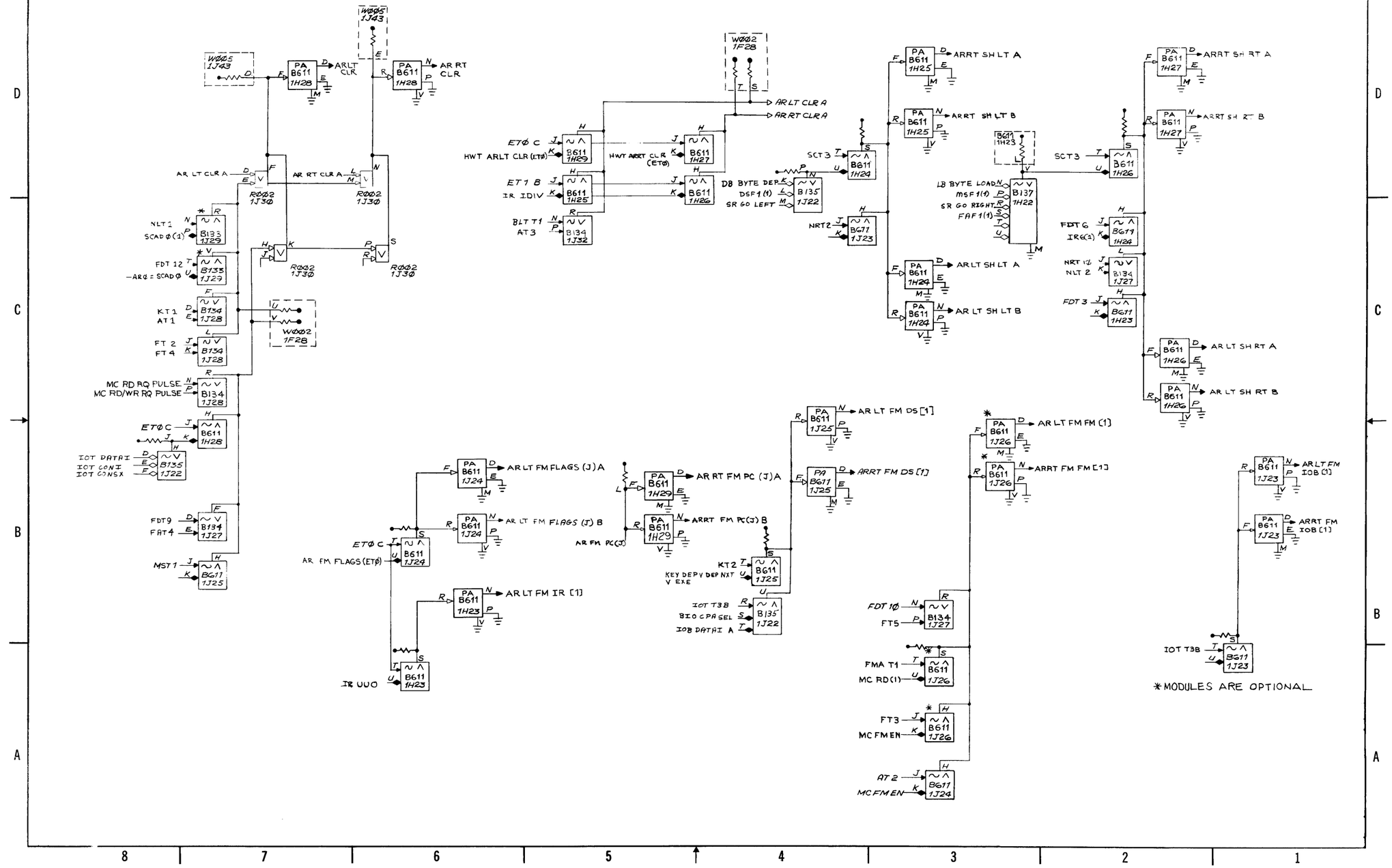
D-BS-KA10-0-AR3 AR Register



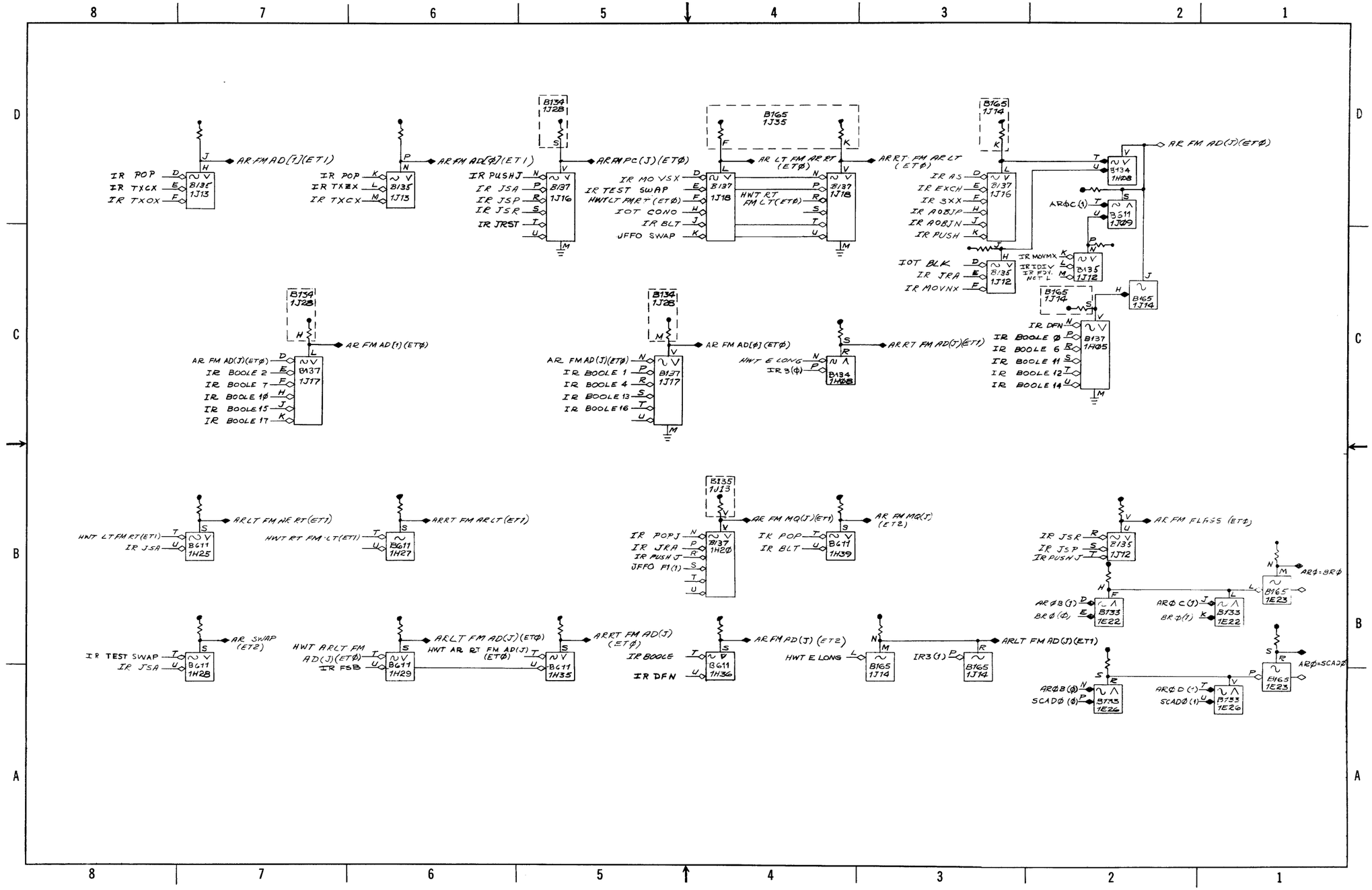
D-BS-KA10-0-AR4 AR Register



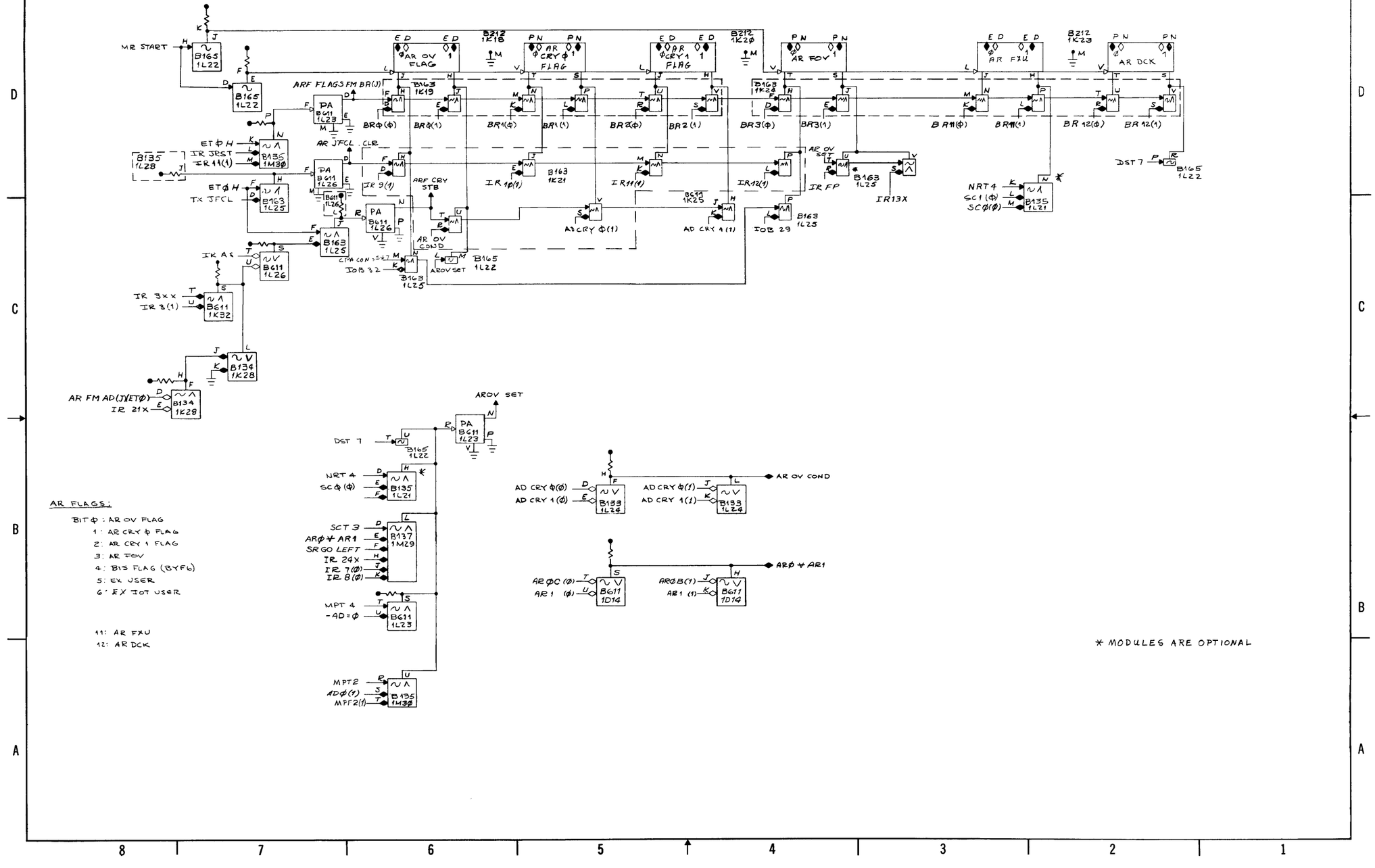
D-BS-KA10-0-ARC1 AR Control Pulses



D-BS-KA10-0-ARC2 AR Control Pulses



D-BS-KA10-0-ARC3 AR Control Levels



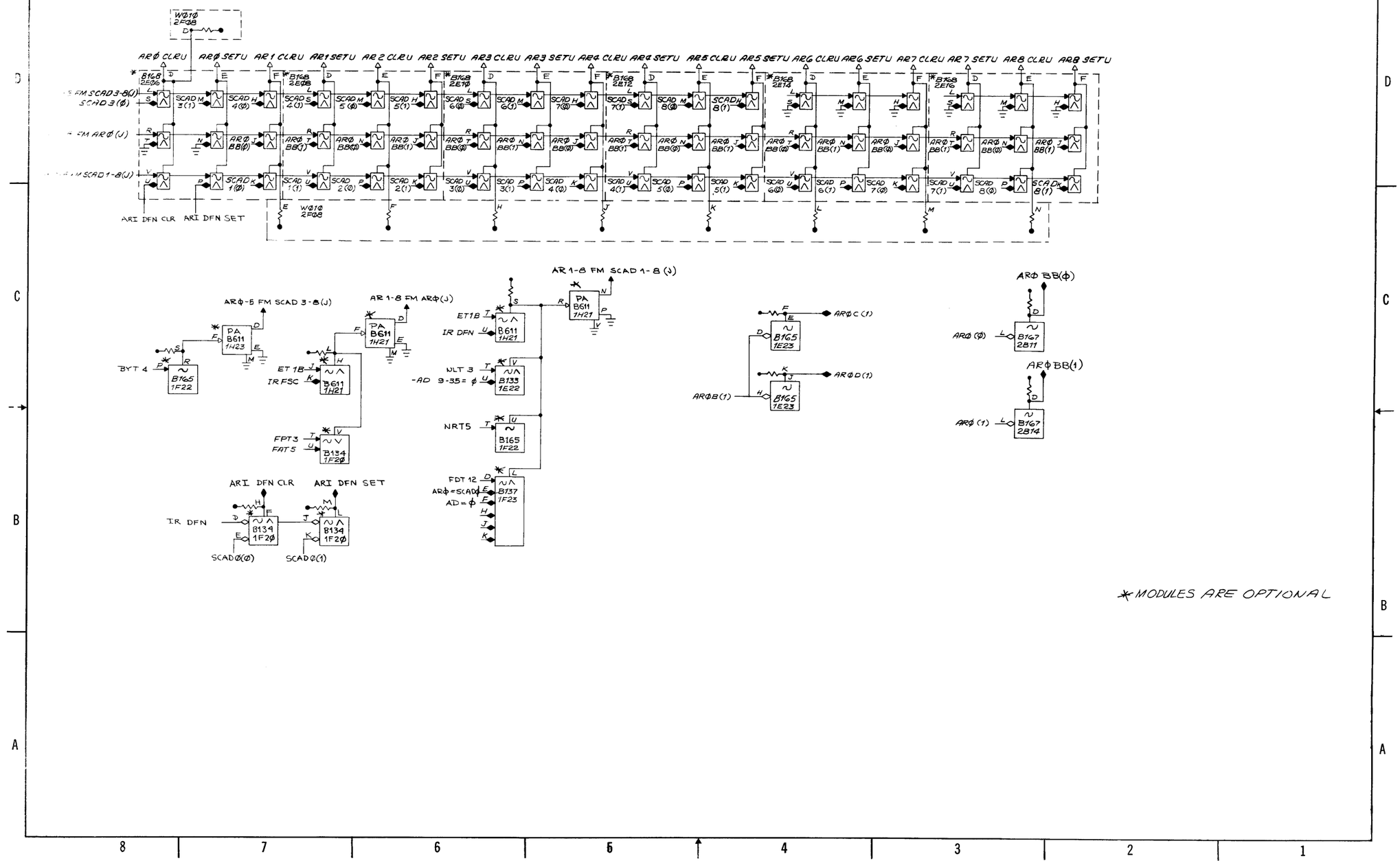
AR FLAGS:

BIT Φ : AR OV FLAG
1: AR CRY Φ FLAG
2: AR CRY 1 FLAG
3: AR FOV
4: BIS FLAG (BYFW)
5: EX USER
6: EX IOT USER

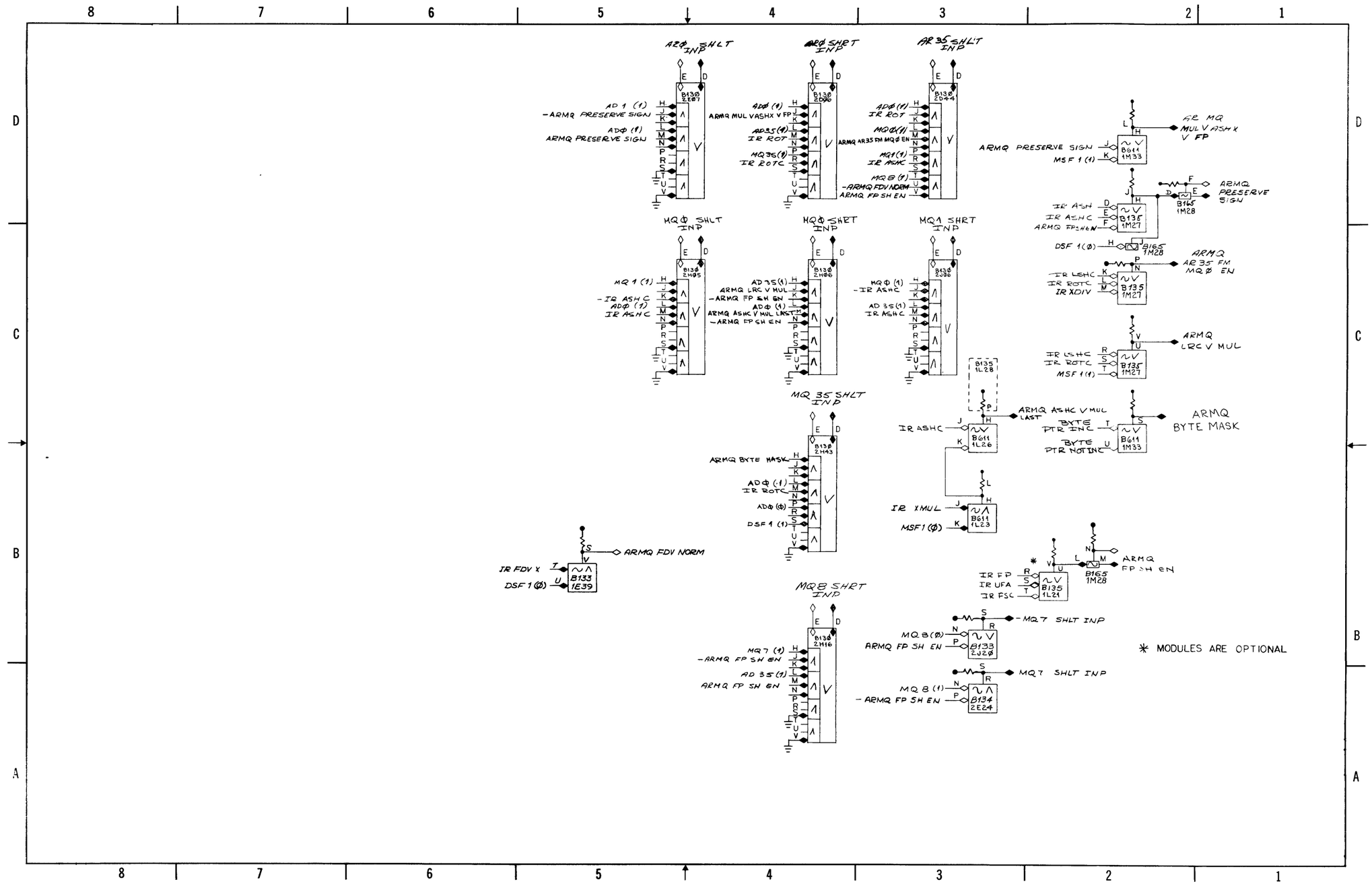
11: AR FXU
12: AR DCK

* MODULES ARE OPTIONAL

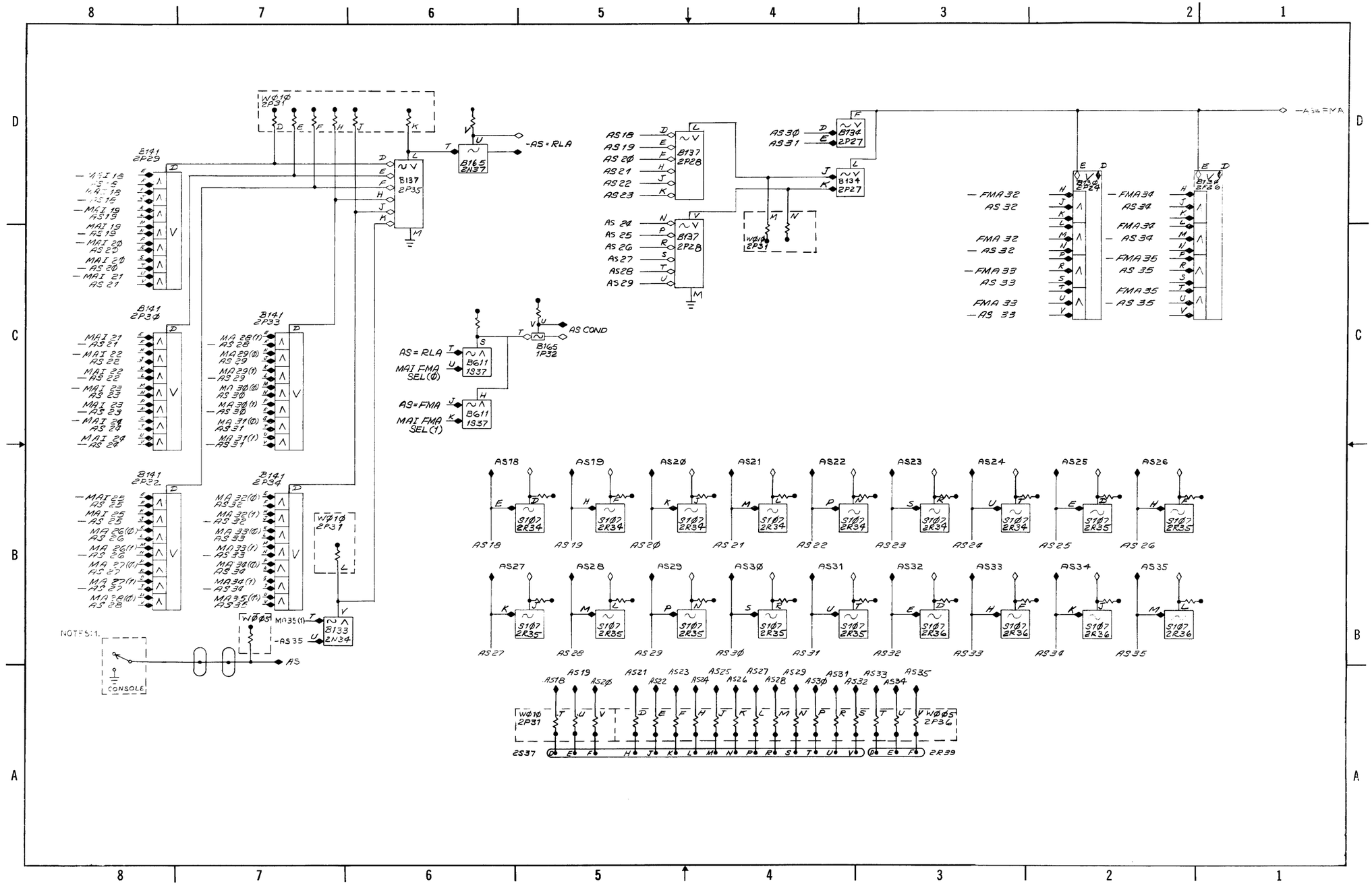
D-BS-KA10-0-ARF Arithmetic Flags



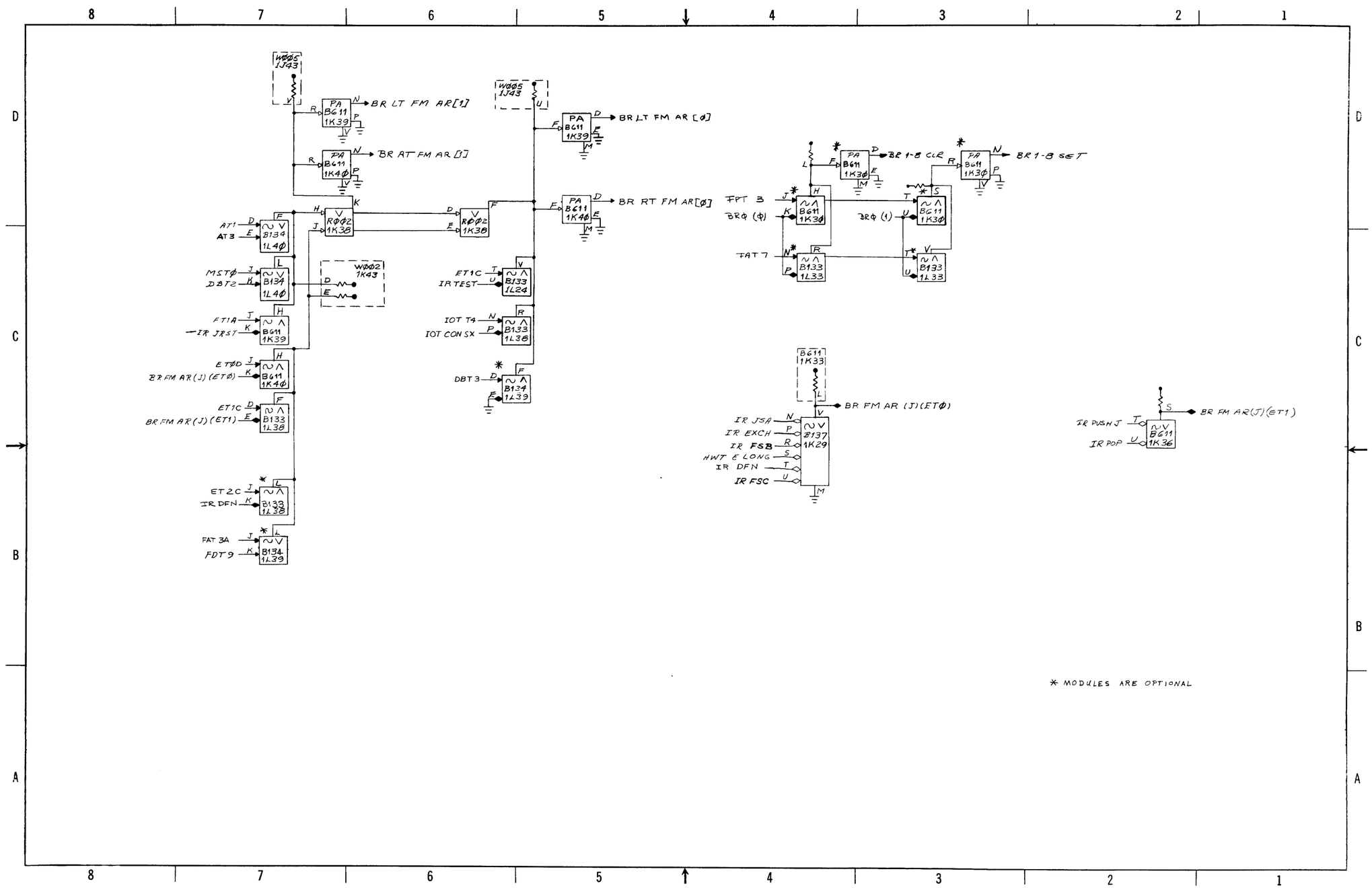
D-BS-KA10-0-ARI AR Inputs



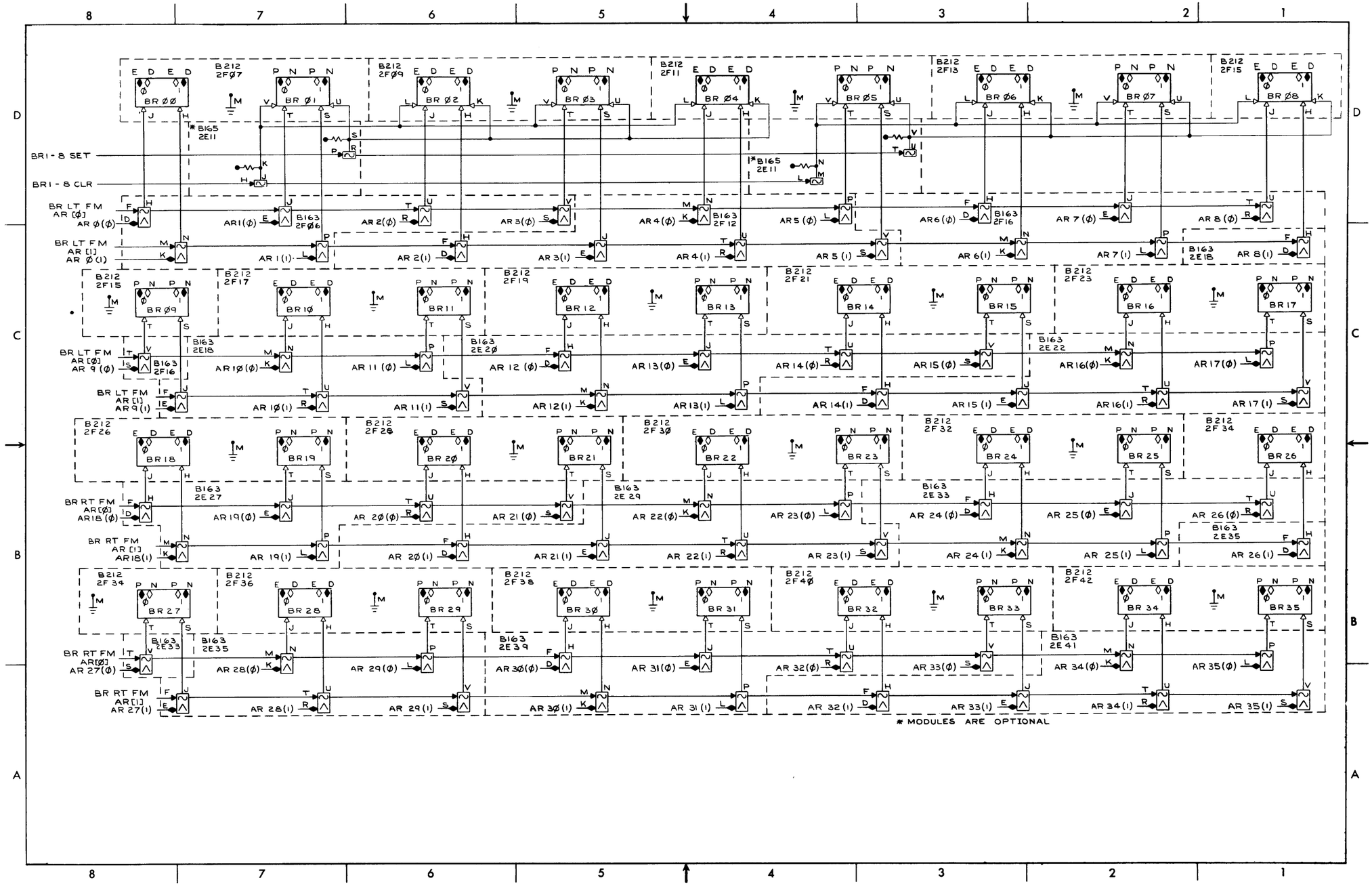
D-BS-KA10-0-ARMQ AR and MQ Shift Connections



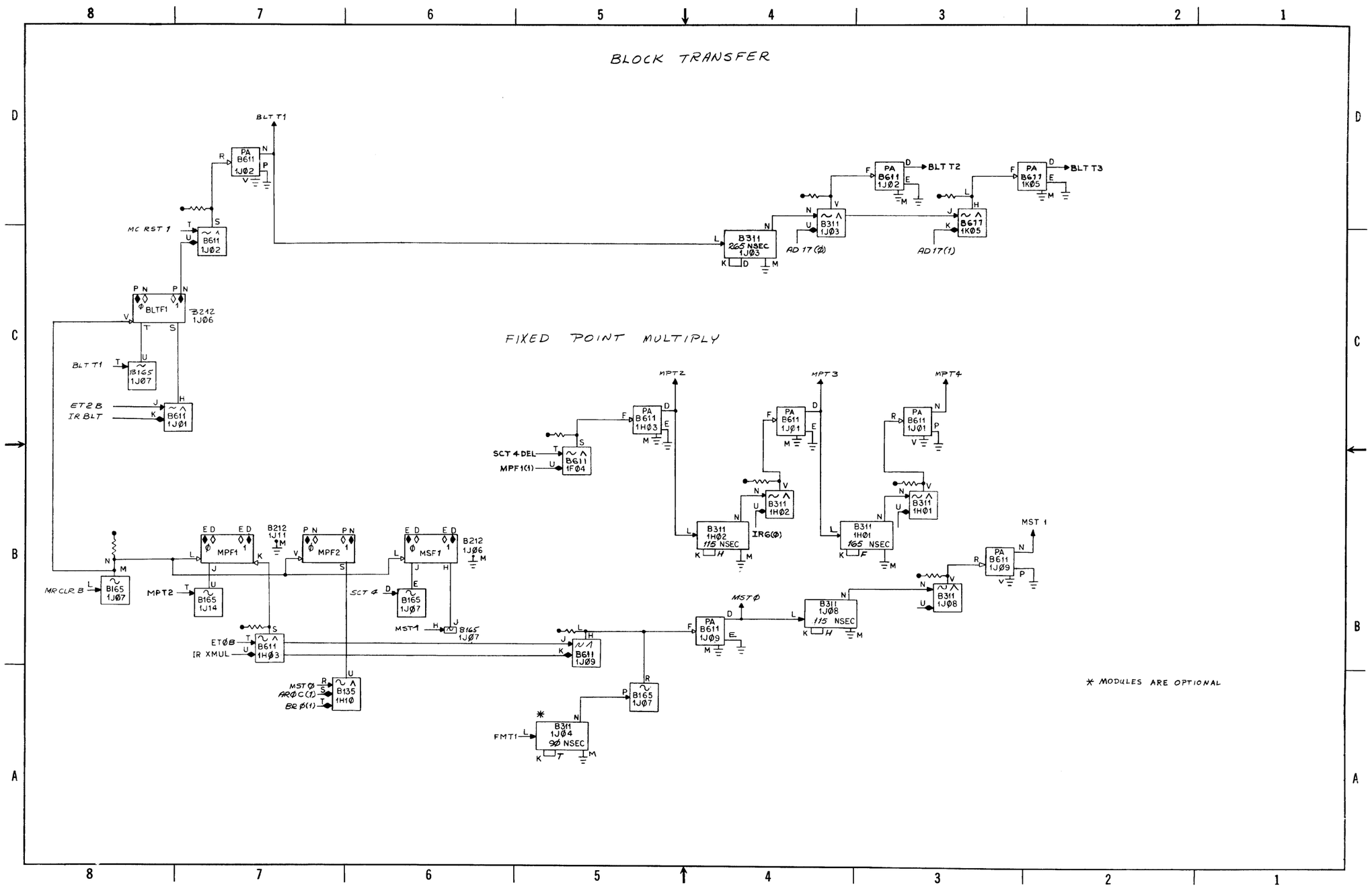
D-BS-KA10-0-AS Address Switch Comparators



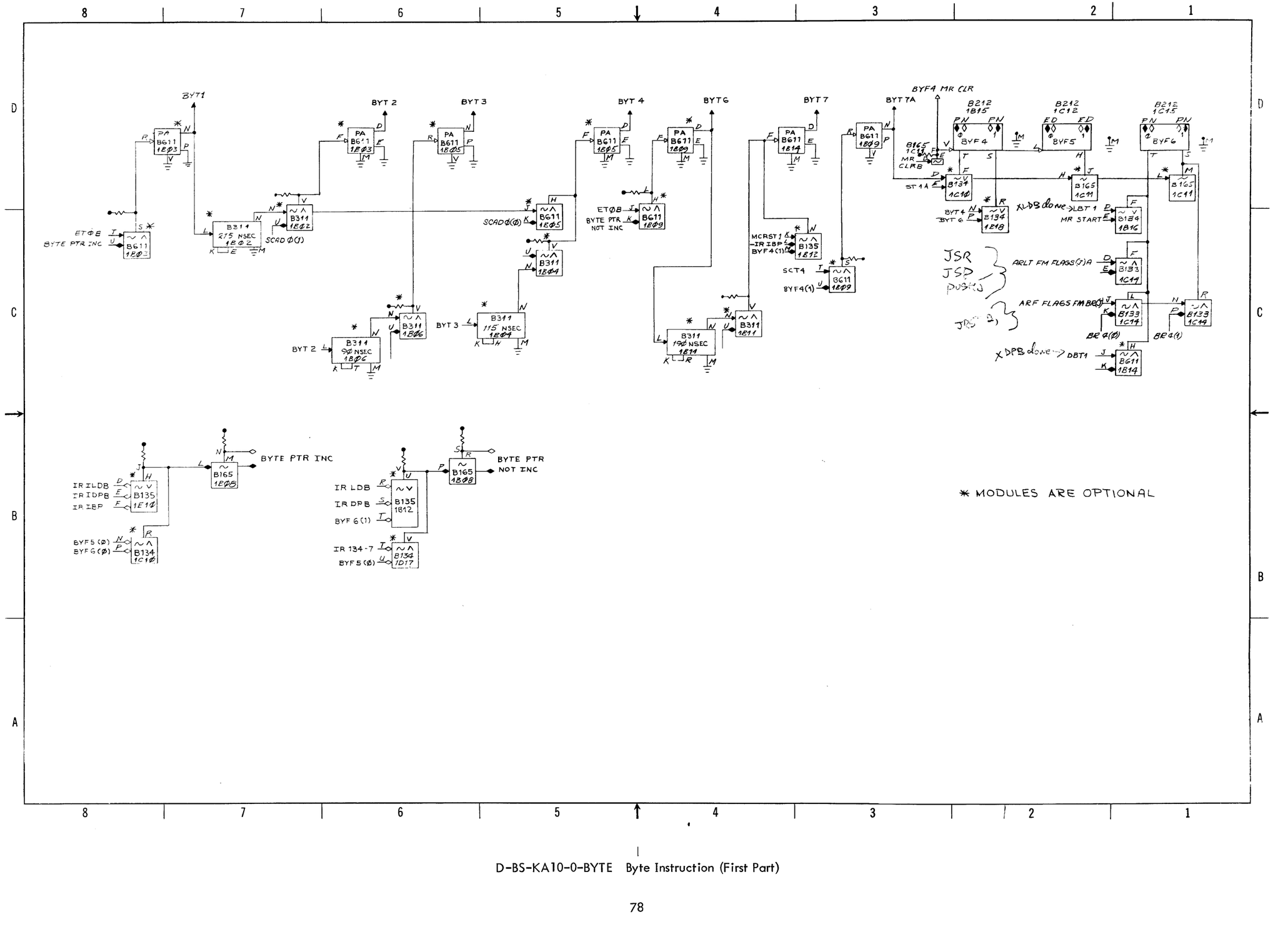
D-BS-KA10-0-BR1 BR Control



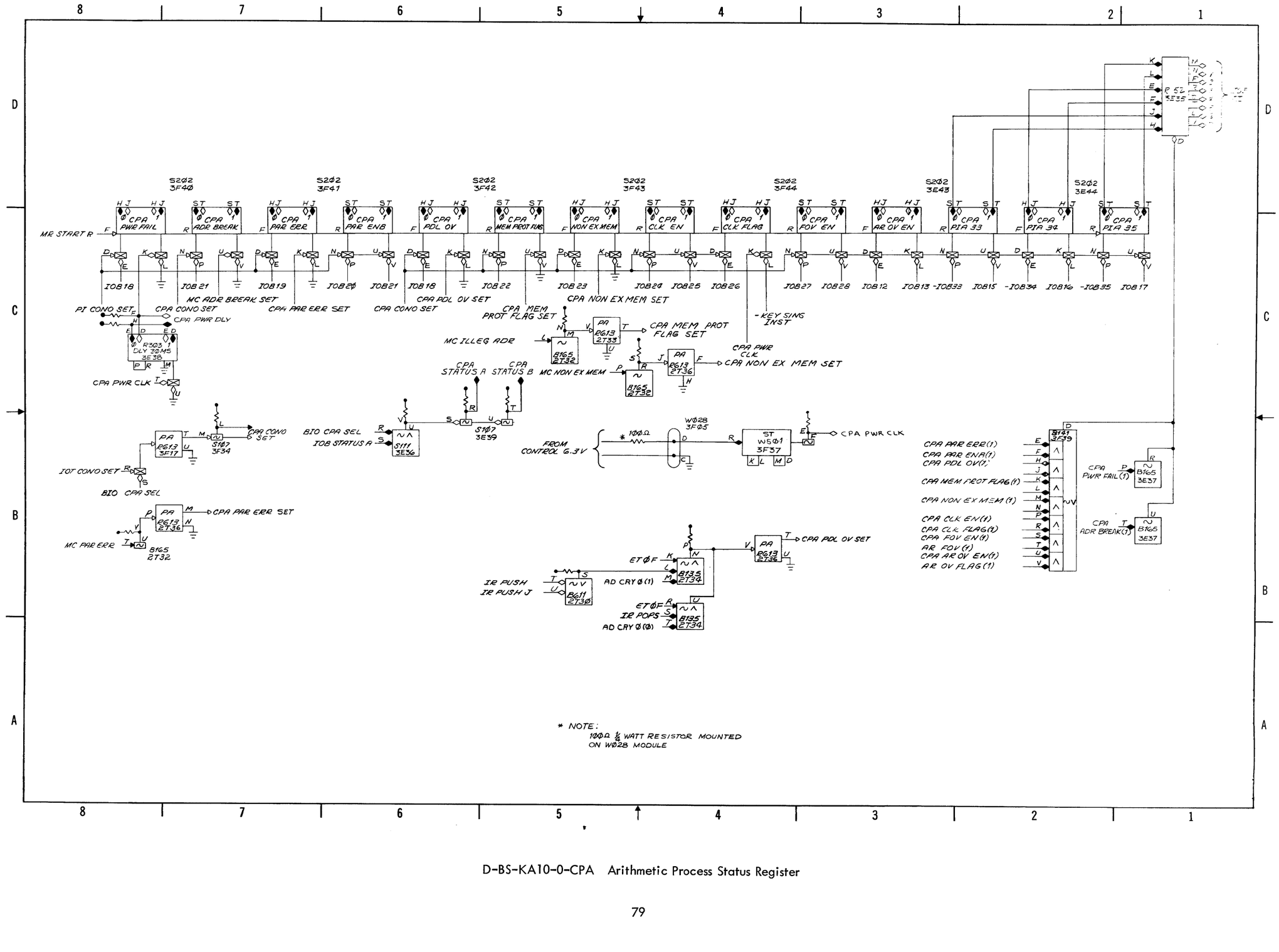
D-BS-KA10-0-BR2 BR Register



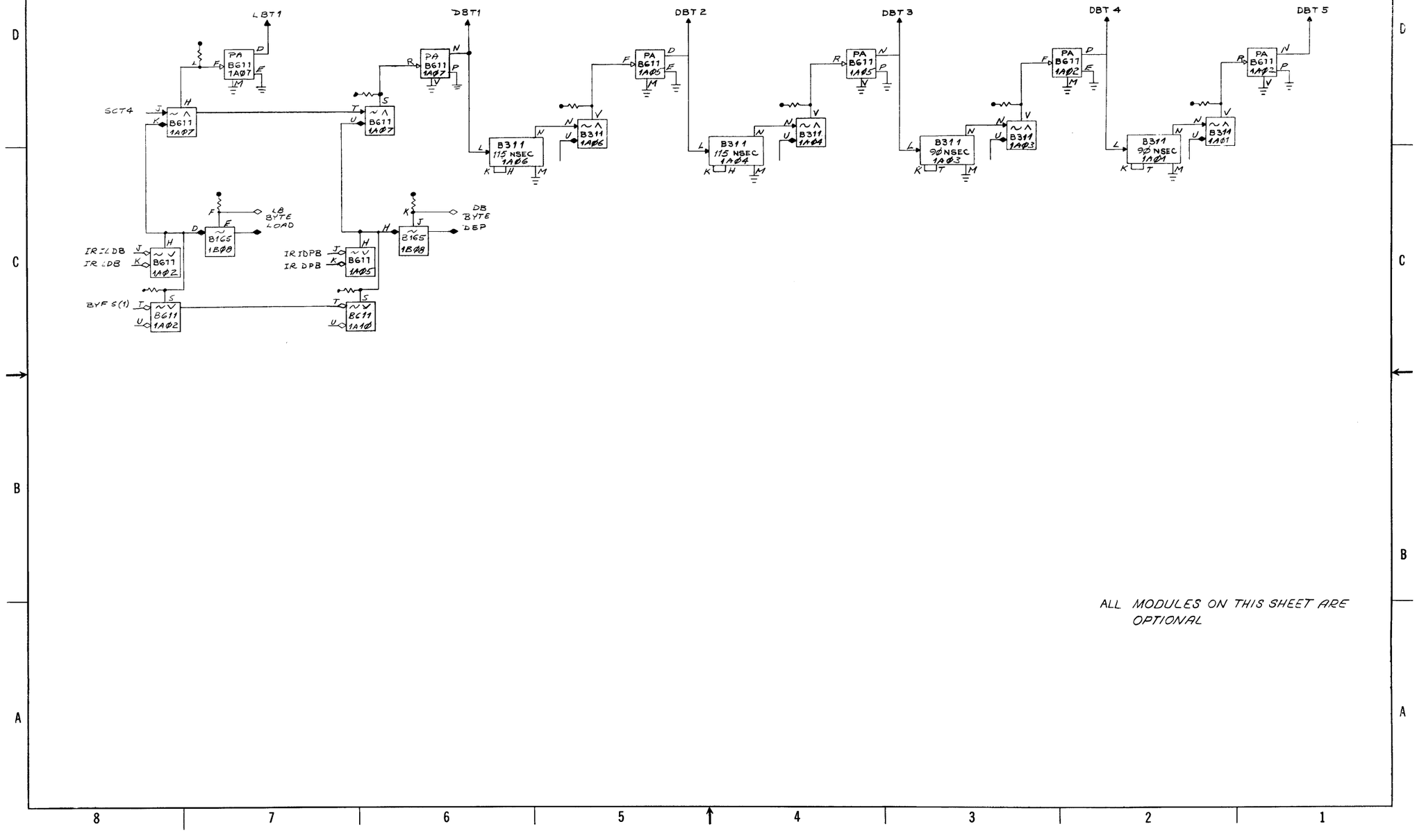
D-BS-KA10-0-BTMP Block Transfer and Multiply



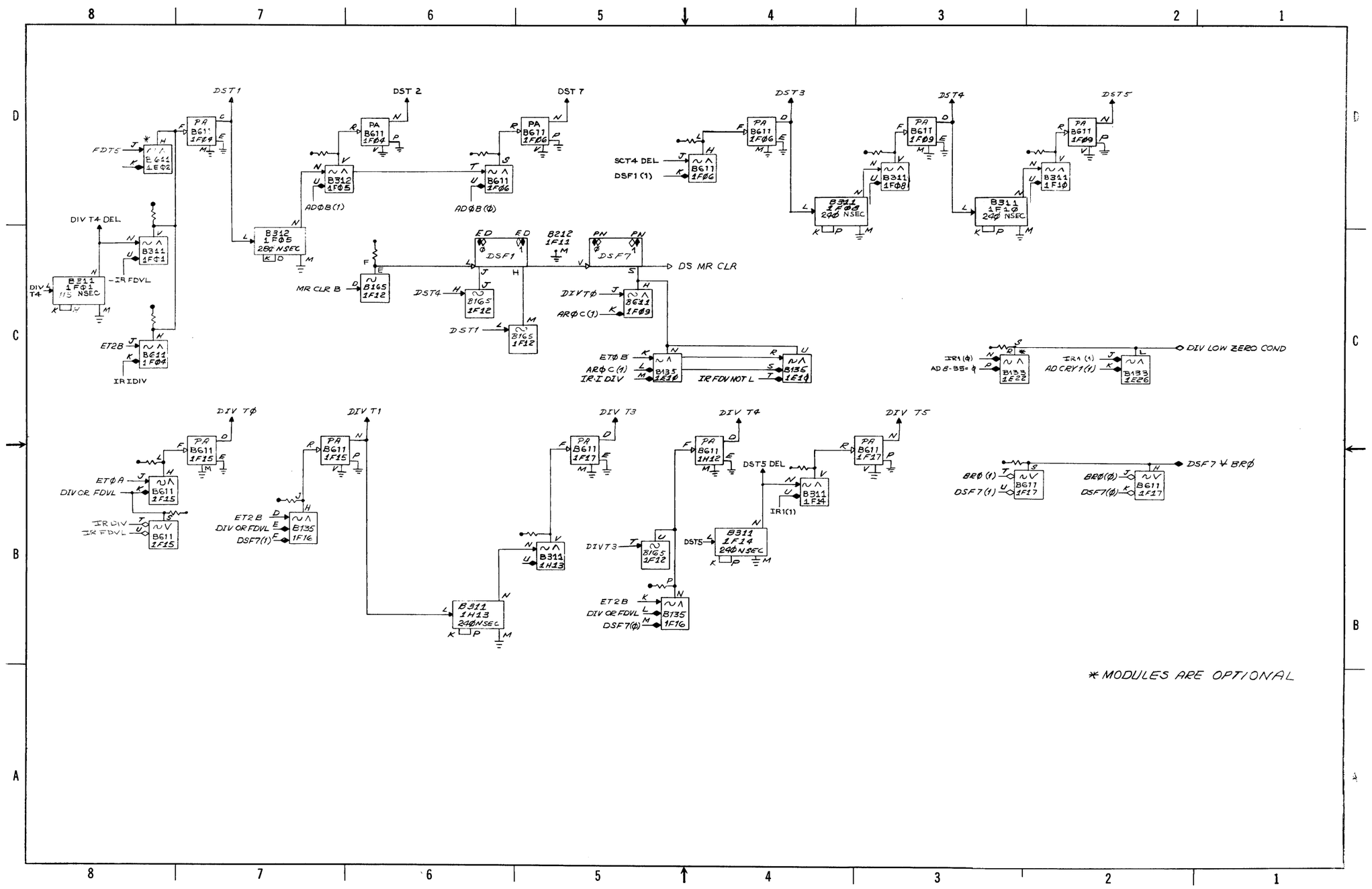
D-BS-KA10-0-BYTE Byte Instruction (First Part)



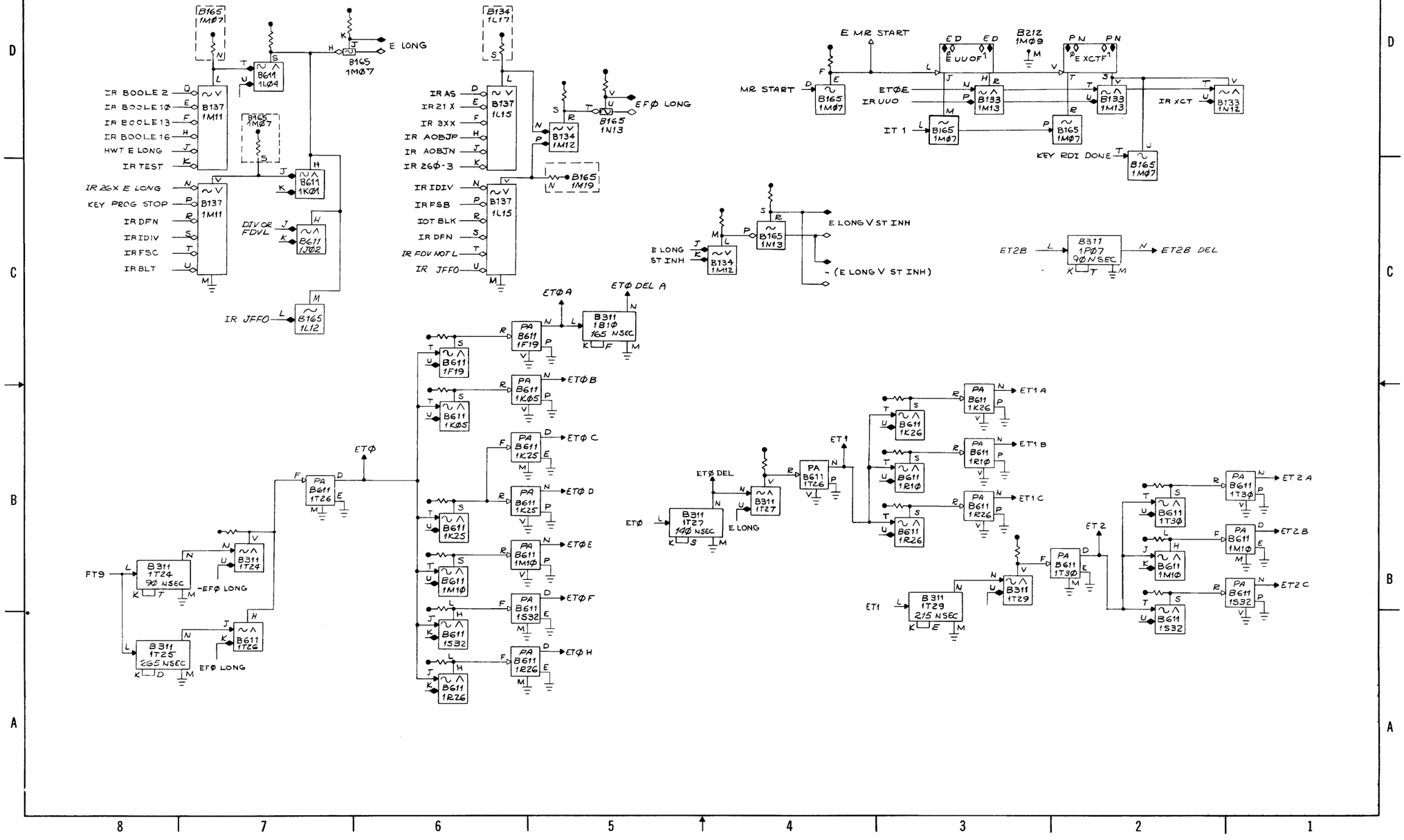
D-BS-KA10-0-CPA Arithmetic Process Status Register



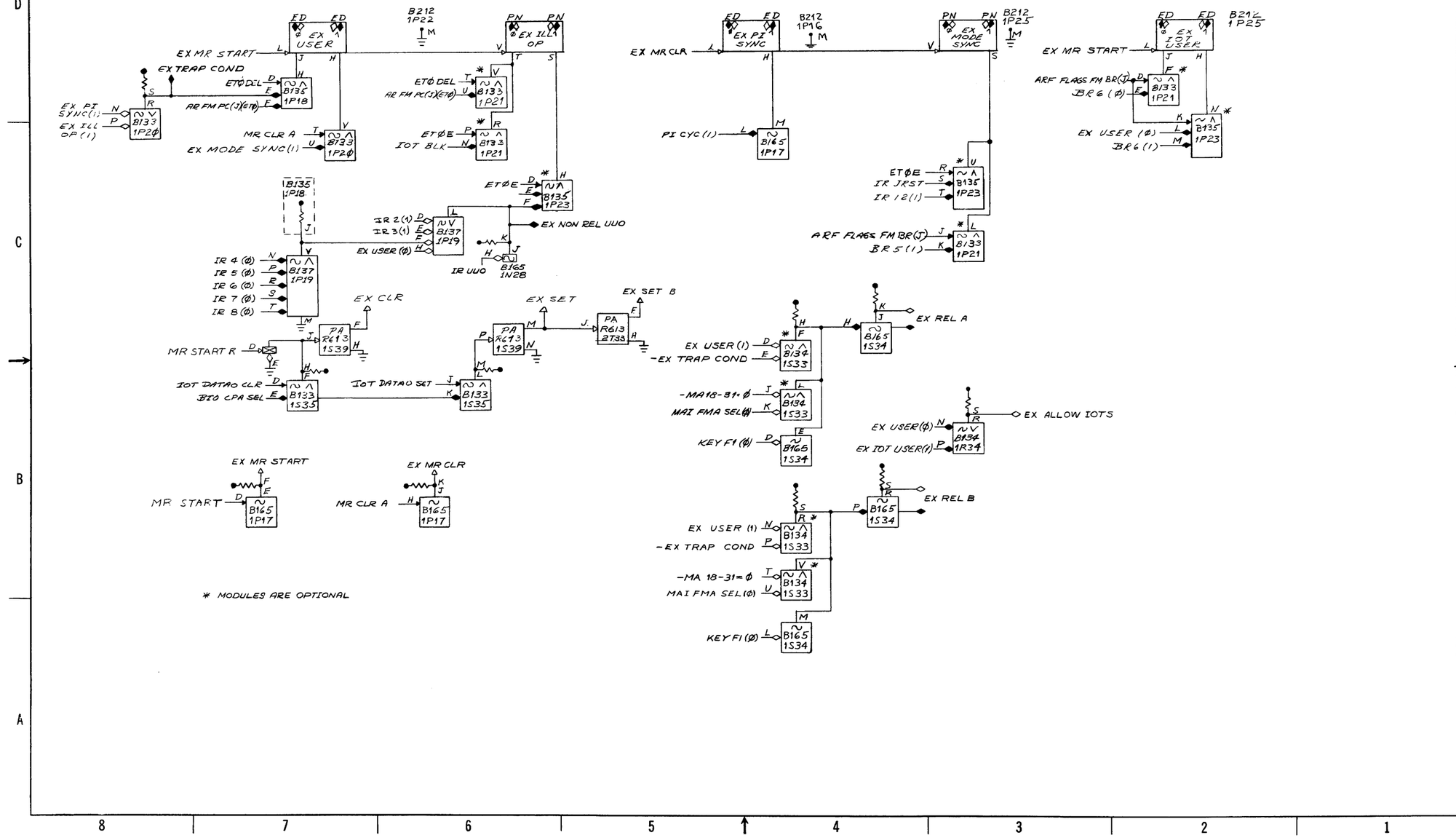
D-BS-KA10-0-DBLB Byte Instruction Deposit and Load (Second Part)

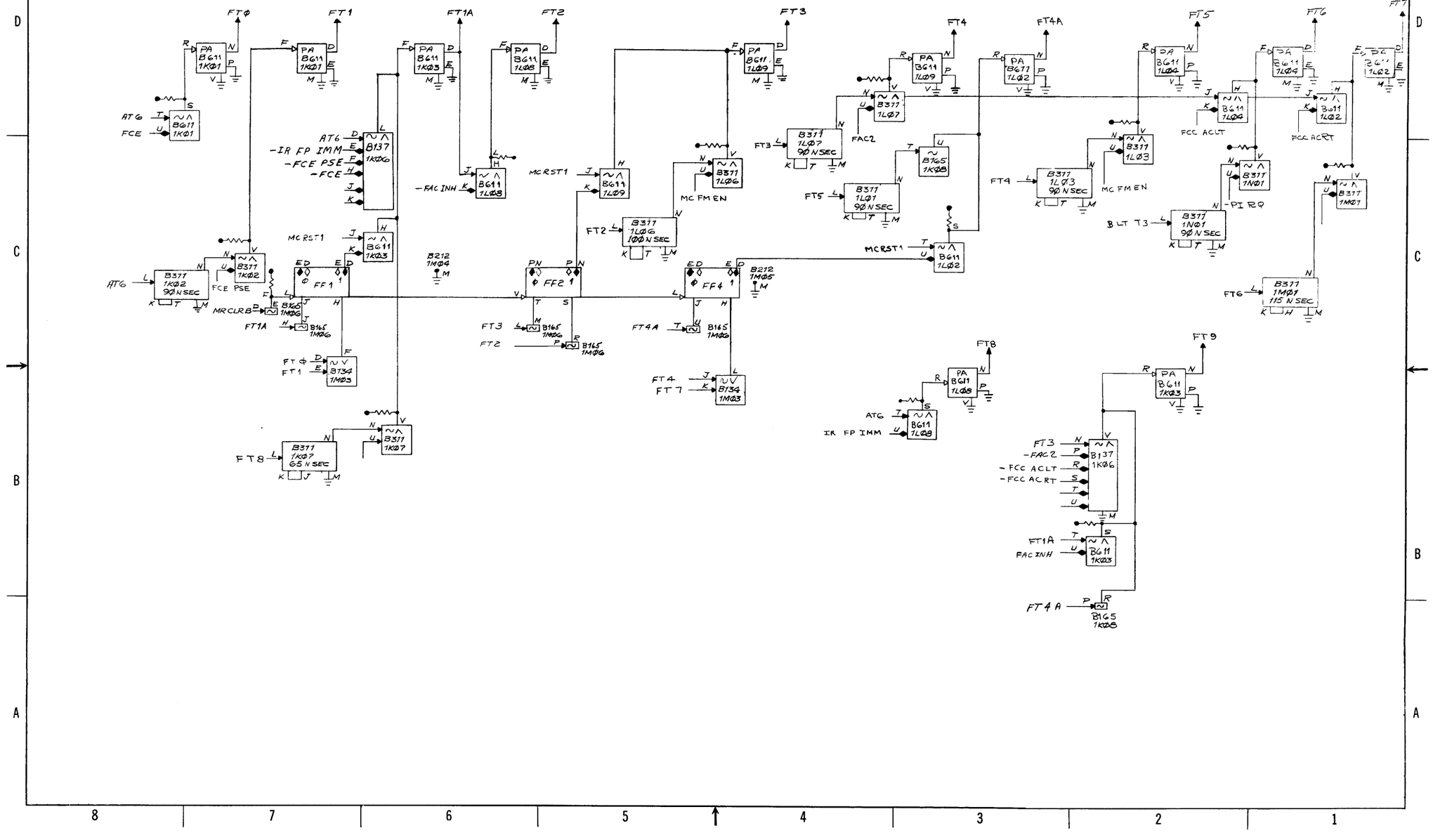


D-BS-KA10-0-DSDV Divide Subroutine and Fixed Divide

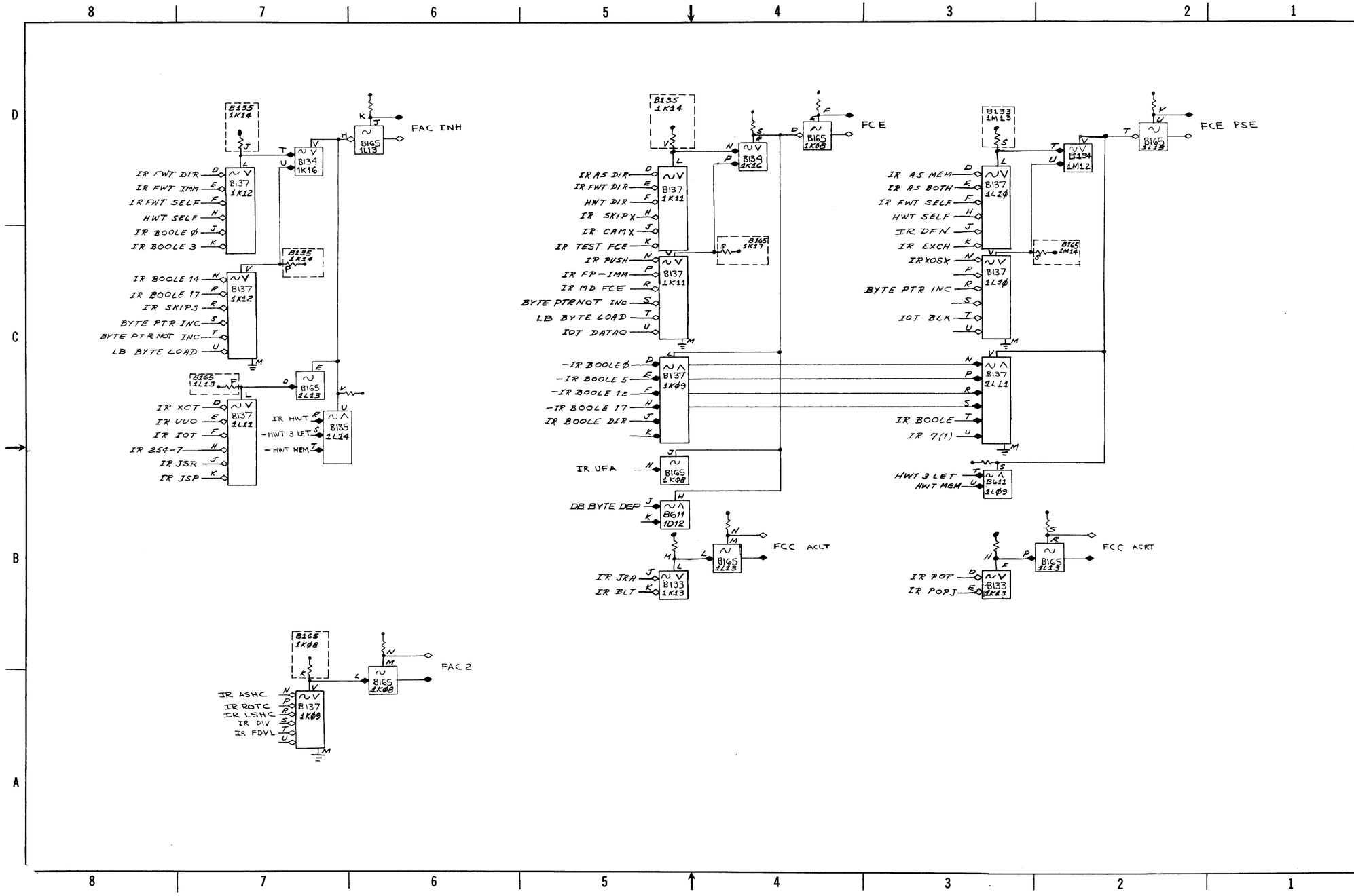


D-BS-KA10-0-E Execution Cycle

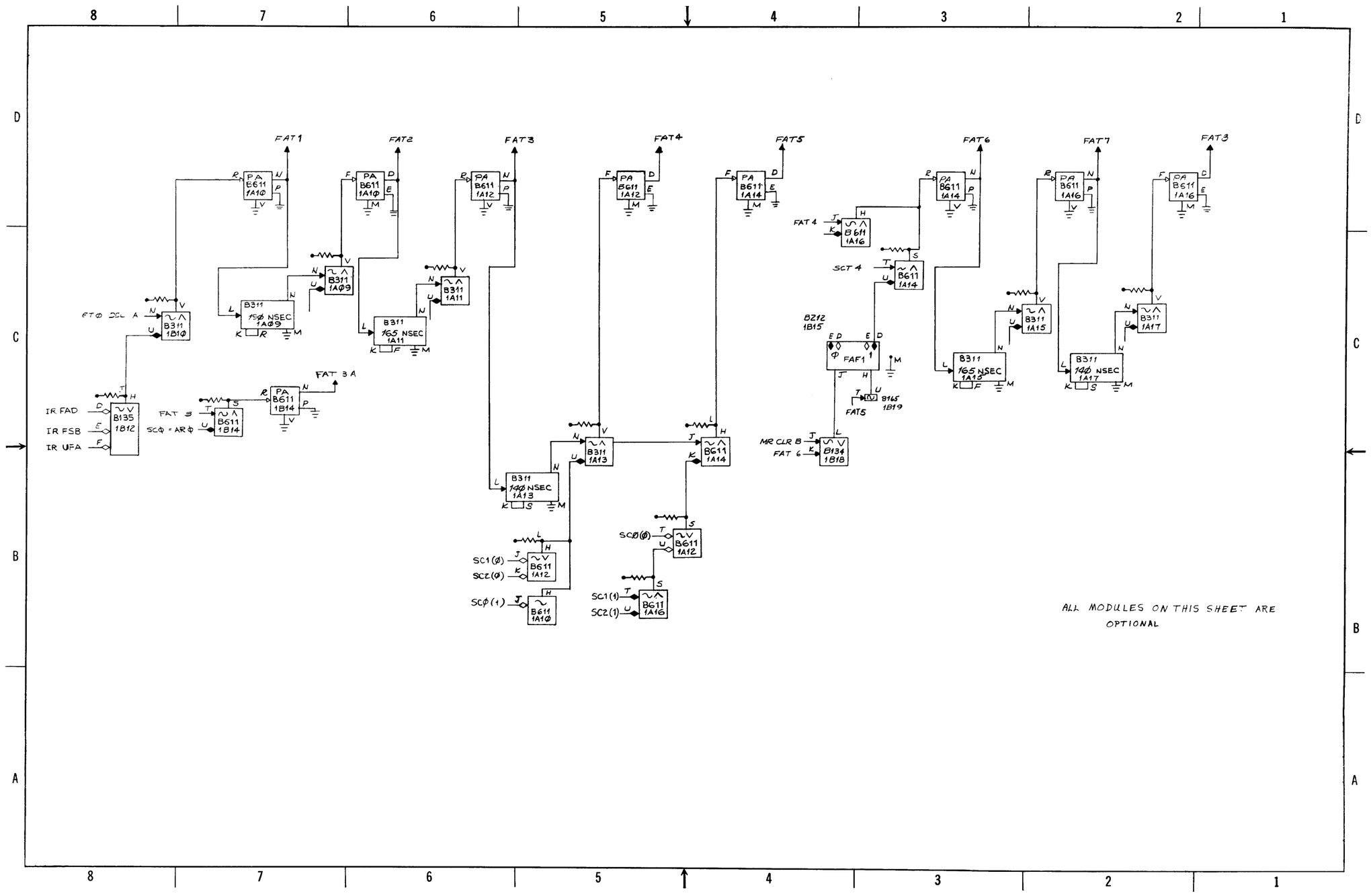

EX MR START
EX TRAP COND
EX PI SYNC (1)
EX ILL OP (1)
B135 1P18
B133 1P20
B133 1P21
B135 1P23
B137 1P19
B165 IN28
IR 2 (1)
IR 3 (1)
EX USER (Ø)
EX NON REL UUO
IR UUO
IR 4 (Ø)
IR 5 (Ø)
IR 6 (Ø)
IR 7 (Ø)
IR 8 (Ø)
EX CLR
EX SET
EX SET B
MR START R
IOT DATAO CLR
BIO CPA SEL
IOT DATAO SET
B133 1S35
B133 1S39
B133 2T33
EX MR CLR
PI CYC (1)
B165 1P17
EX MODE SYNC
ETØE
IR JRST
IR 12 (1)
ARF FLAGS FM BR(J)
BR 5 (1)
BR 6 (Ø)
EX USER (Ø)
BR 6 (1)
EX REL A
EX USER (1)
-EX TRAP COND
-MA 18-31=Ø
MAI FMA SEL(Ø)
KEY F1 (Ø)
B134 1S33
B165 1S34
EX ALLOW IOTS
EX IOT USER(1)
B134 1R34
EX REL B
MR START
MR CLR A
* MODULES ARE OPTIONAL

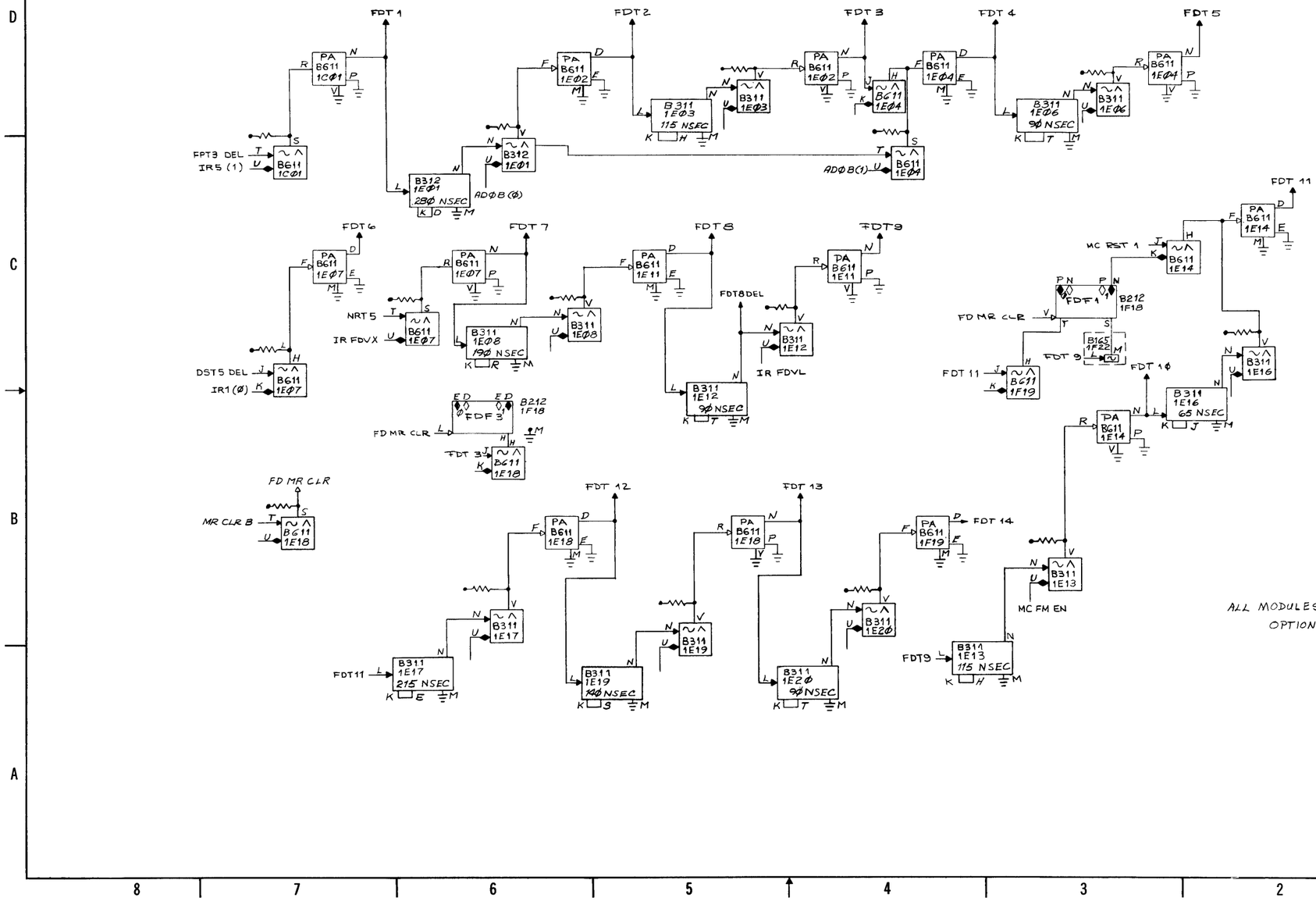


D-BS-KA10-0-F1 Fetch Cycle Time Pulses

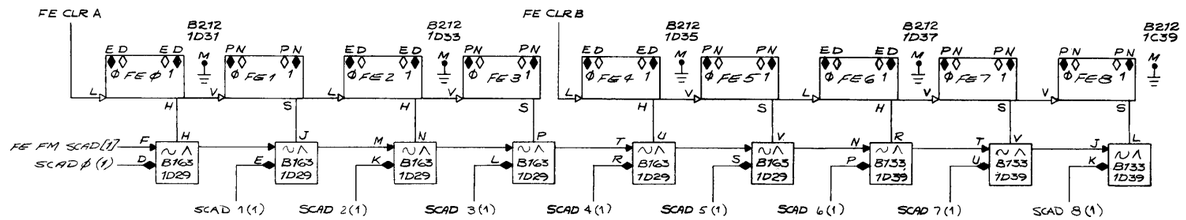


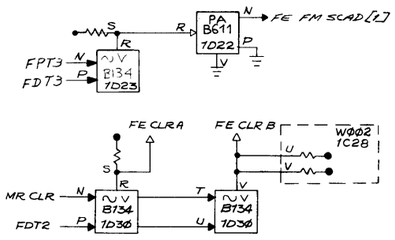
D-BS-KA10-0-F2 Fetch Cycle Levels


FAT 1
FAT 2
FAT 3
FAT 4
FAT 5
FAT 6
FAT 7
FAT 8
FAT 3 A
ET Φ DCL A
IR FAD
IR FSB
IR UFA
FAT 3
SC Φ + AR Φ
FAT 4
SCT 4
BZ12 1B15
FAF1
FAT5
MR CLR B
FAT 6
SC1(Φ)
SC2(Φ)
SCΦ(1)
SCΦ(Φ)
SC1(1)
SC2(1)
B611 1A1Φ
B311 1AΦ9
B311 150 NSEC 1AΦ9
B311 1A11
B311 165 NSEC 1A11
B611 1A12
B311 140 NSEC 1A13
B611 1A13
B611 1A14
B311 165 NSEC 1A15
B611 1A15
B611 1A16
B311 140 NSEC 1A17
B611 1A17
B311 1A17
B135 1B12
B611 1B14
B611 1A16
B611 1A14
B165 1B19
B134 1B18
B611 1A12
B611 1A1Φ
B611 1A16
ALL MODULES ON THIS SHEET ARE OPTIONAL

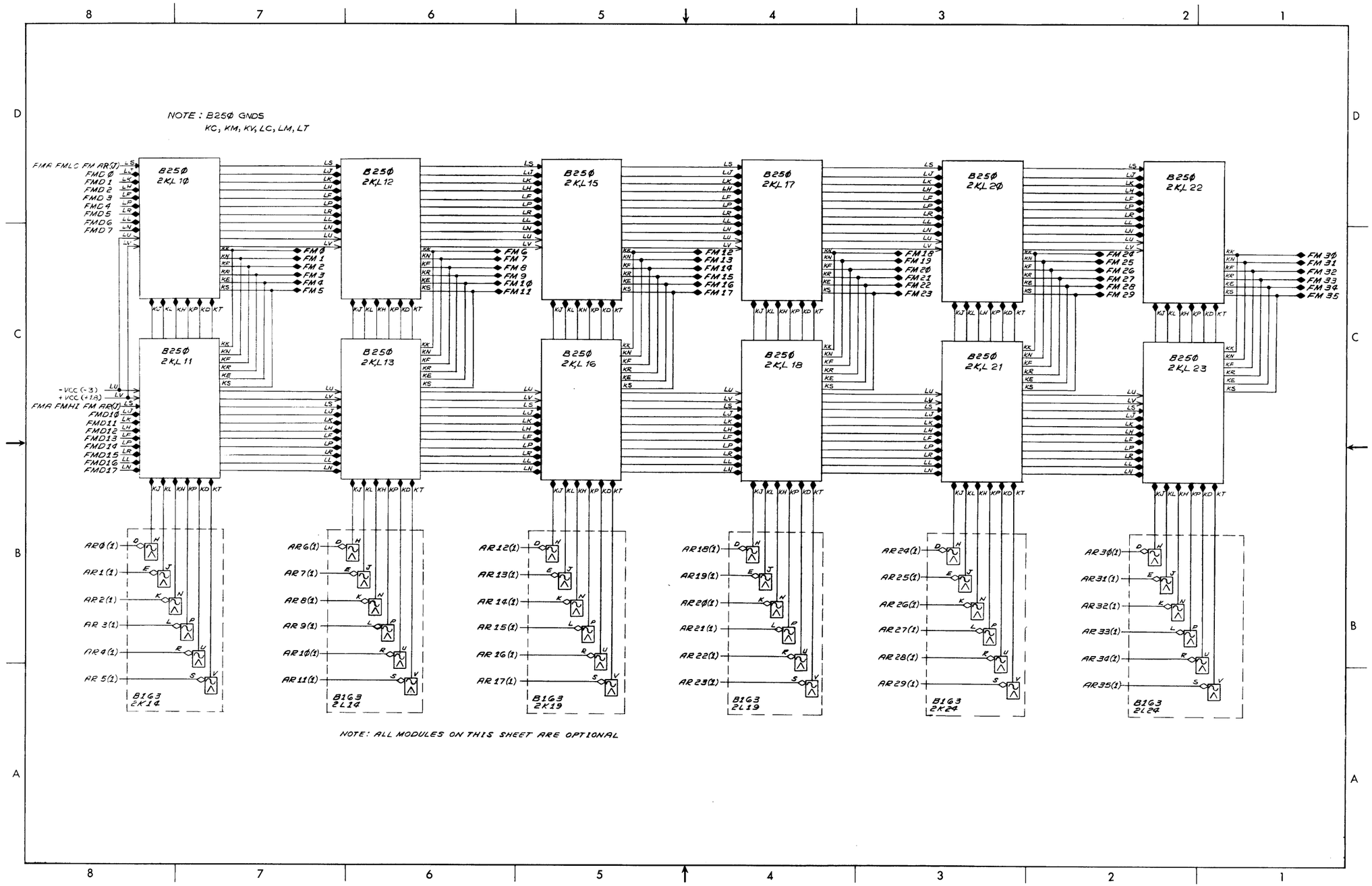


D-BS-KA10-0-FDV Floating Divide

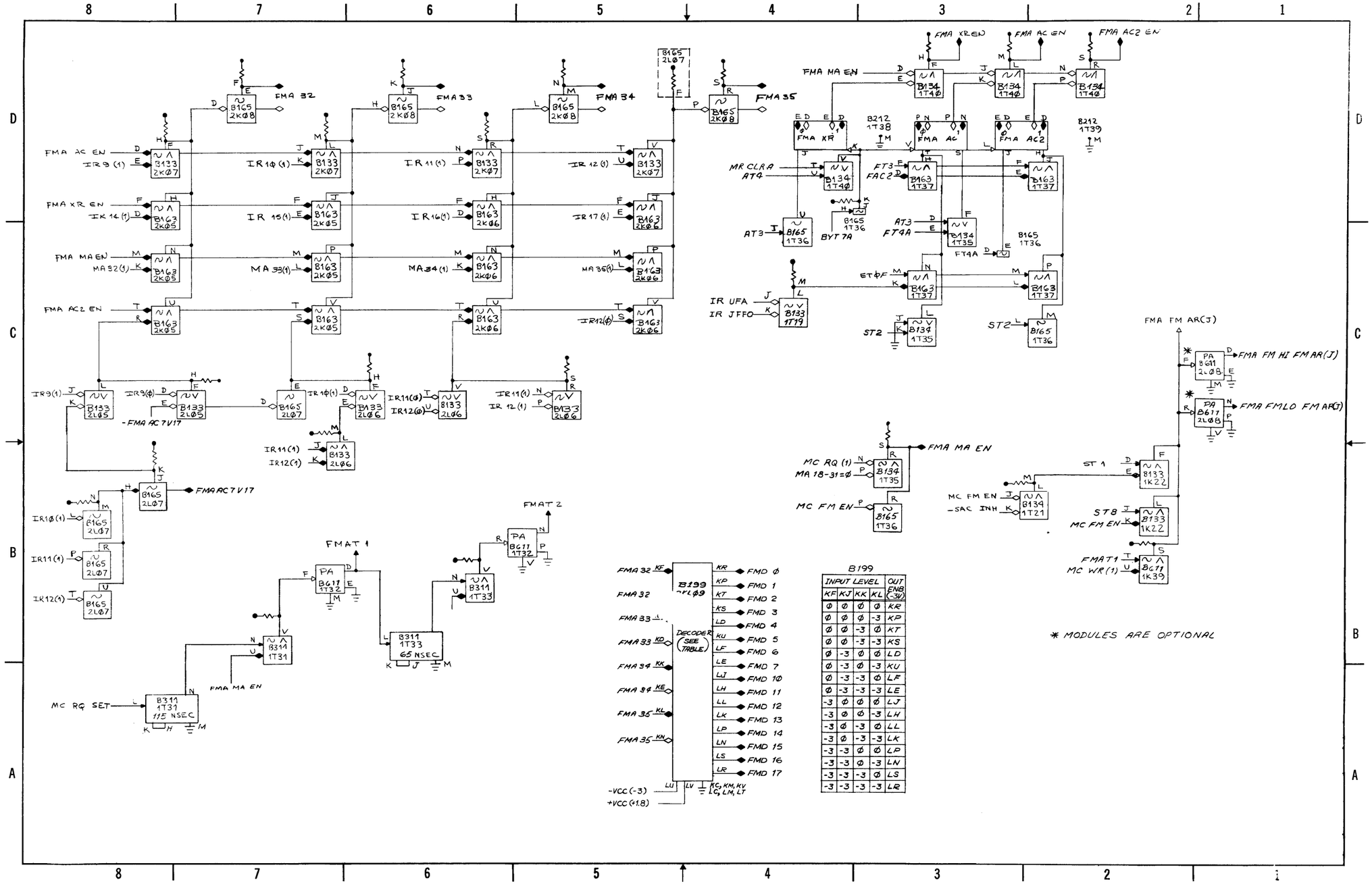




ALL MODULES ON THIS SHEET ARE OPTIONAL

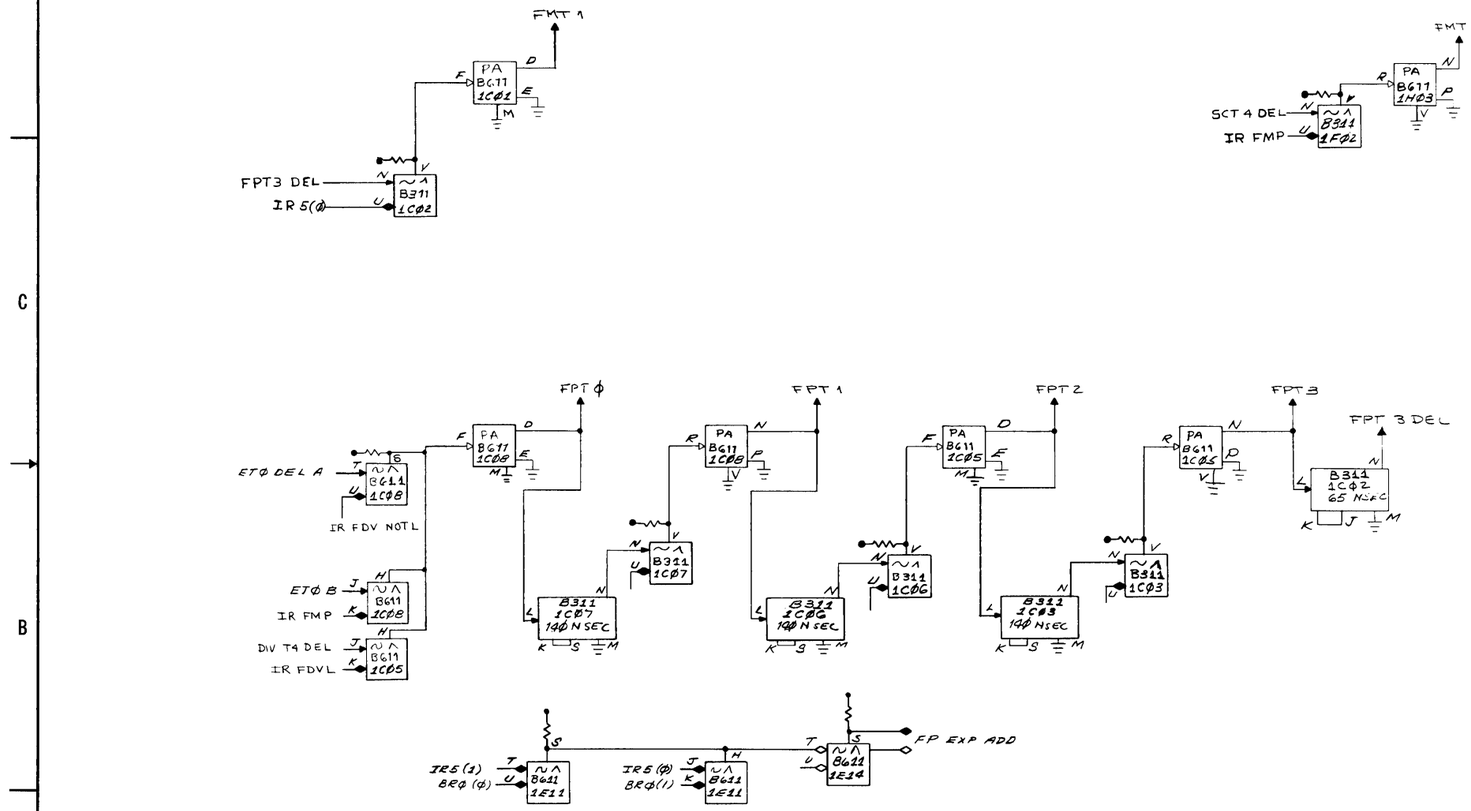


NOTE: ALL MODULES ON THIS SHEET ARE OPTIONAL

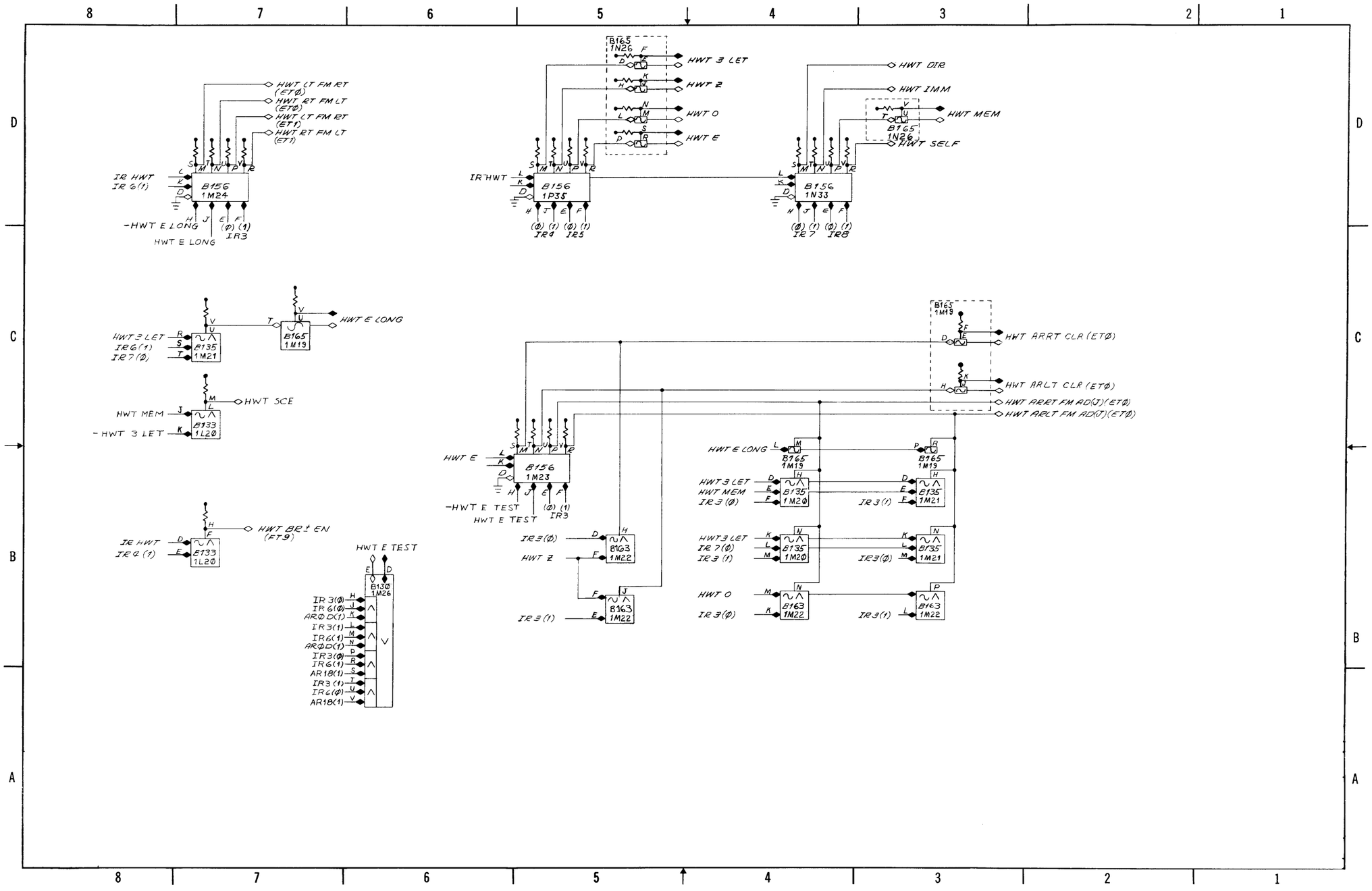


B199				
INPUT LEVEL				OUT ENB (-3V)
KF	KJ	KK	KL	
Ø	Ø	Ø	Ø	KR
Ø	Ø	Ø	-3	KP
Ø	Ø	-3	Ø	KT
Ø	Ø	-3	-3	KS
Ø	-3	Ø	Ø	LD
Ø	-3	Ø	-3	KU
Ø	-3	-3	Ø	LF
Ø	-3	-3	-3	LE
-3	Ø	Ø	Ø	LJ
-3	Ø	Ø	-3	LH
-3	Ø	-3	Ø	LL
-3	Ø	-3	-3	LK
-3	-3	Ø	Ø	LP
-3	-3	Ø	-3	LN
-3	-3	-3	Ø	LS
-3	-3	-3	-3	LR

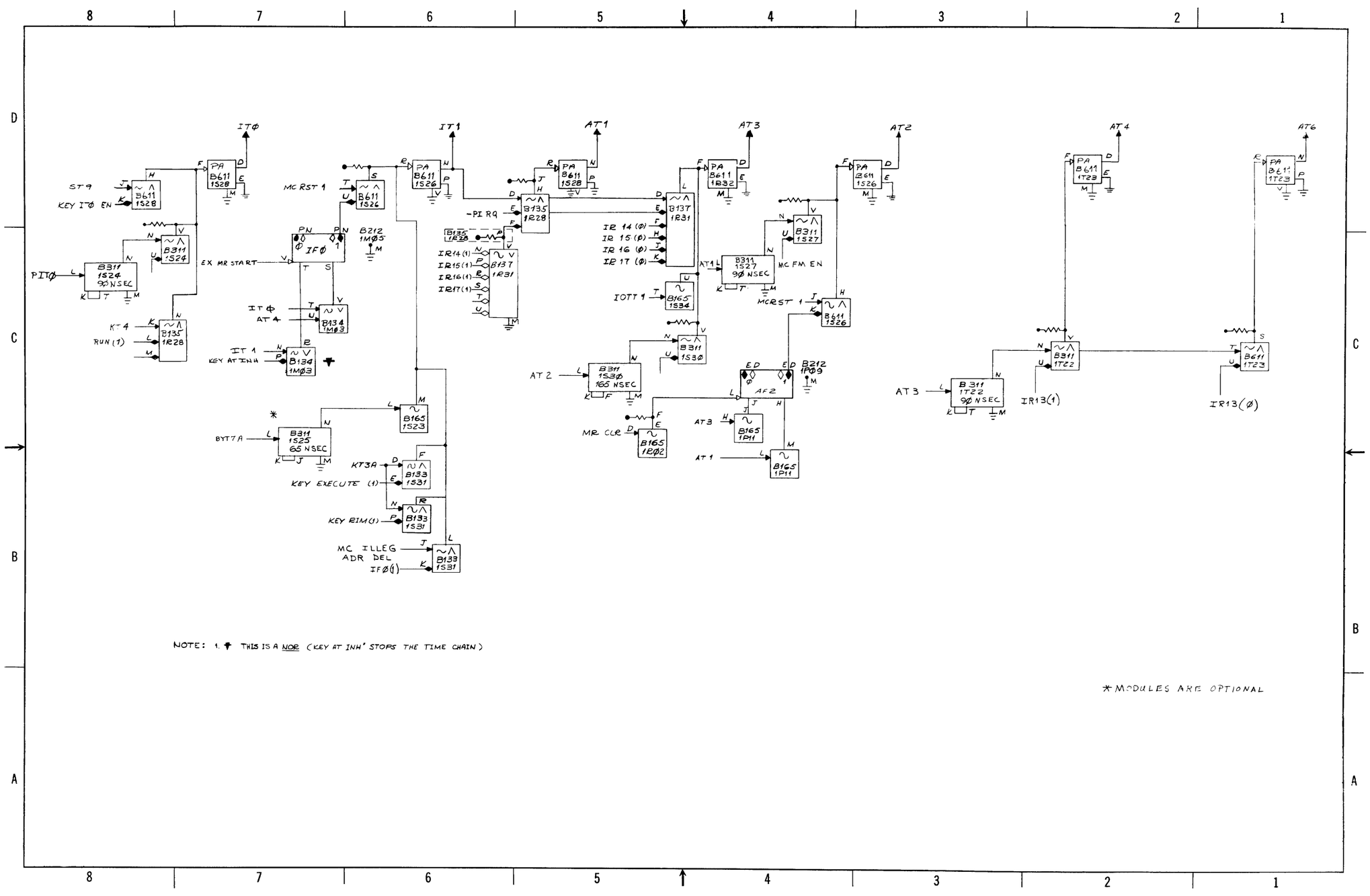
D-BS-KA10-0-FMA Fast Memory Address



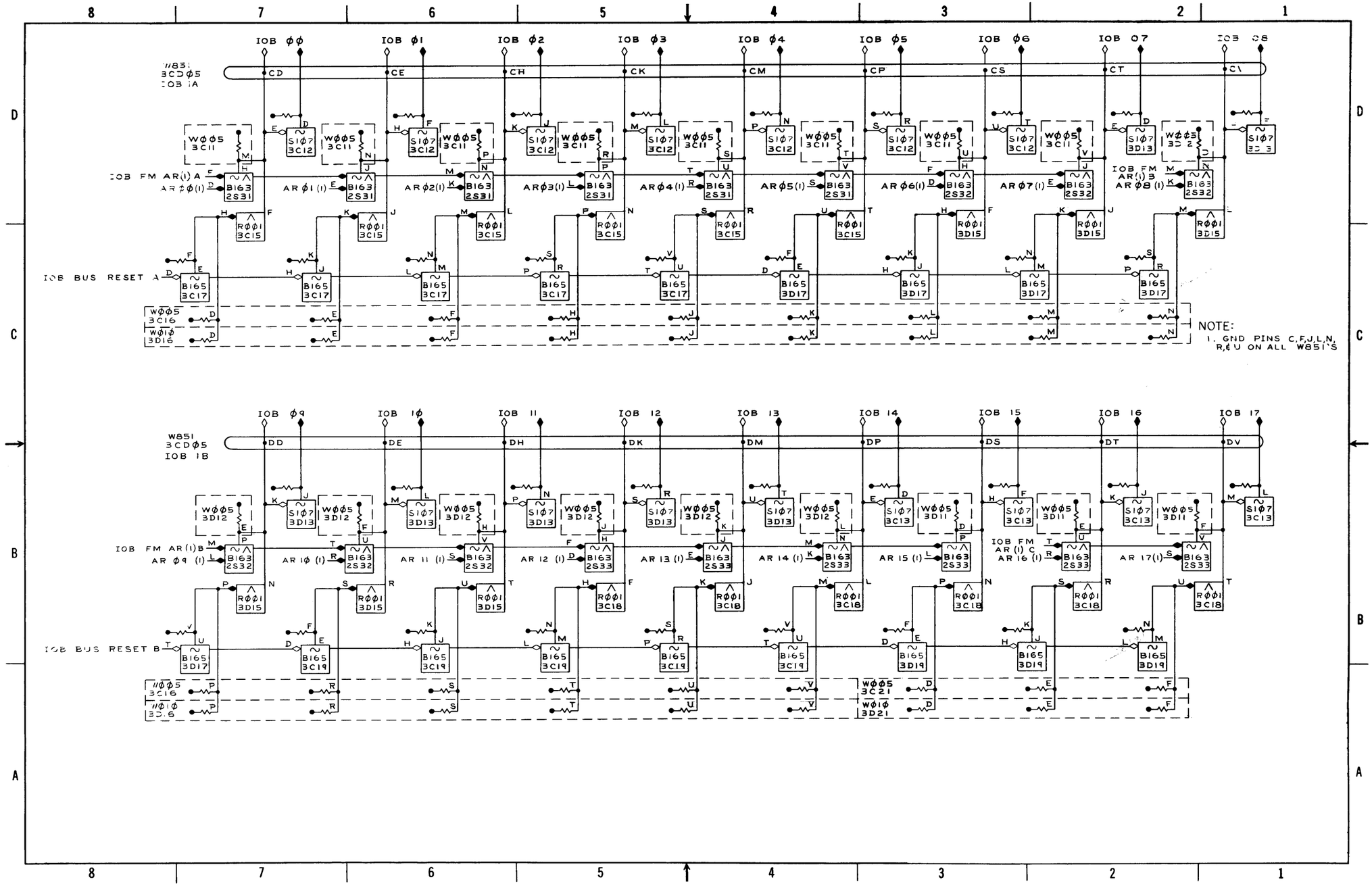
D-BS-KA10-0-FPFM EXP CALC Floating Multiply



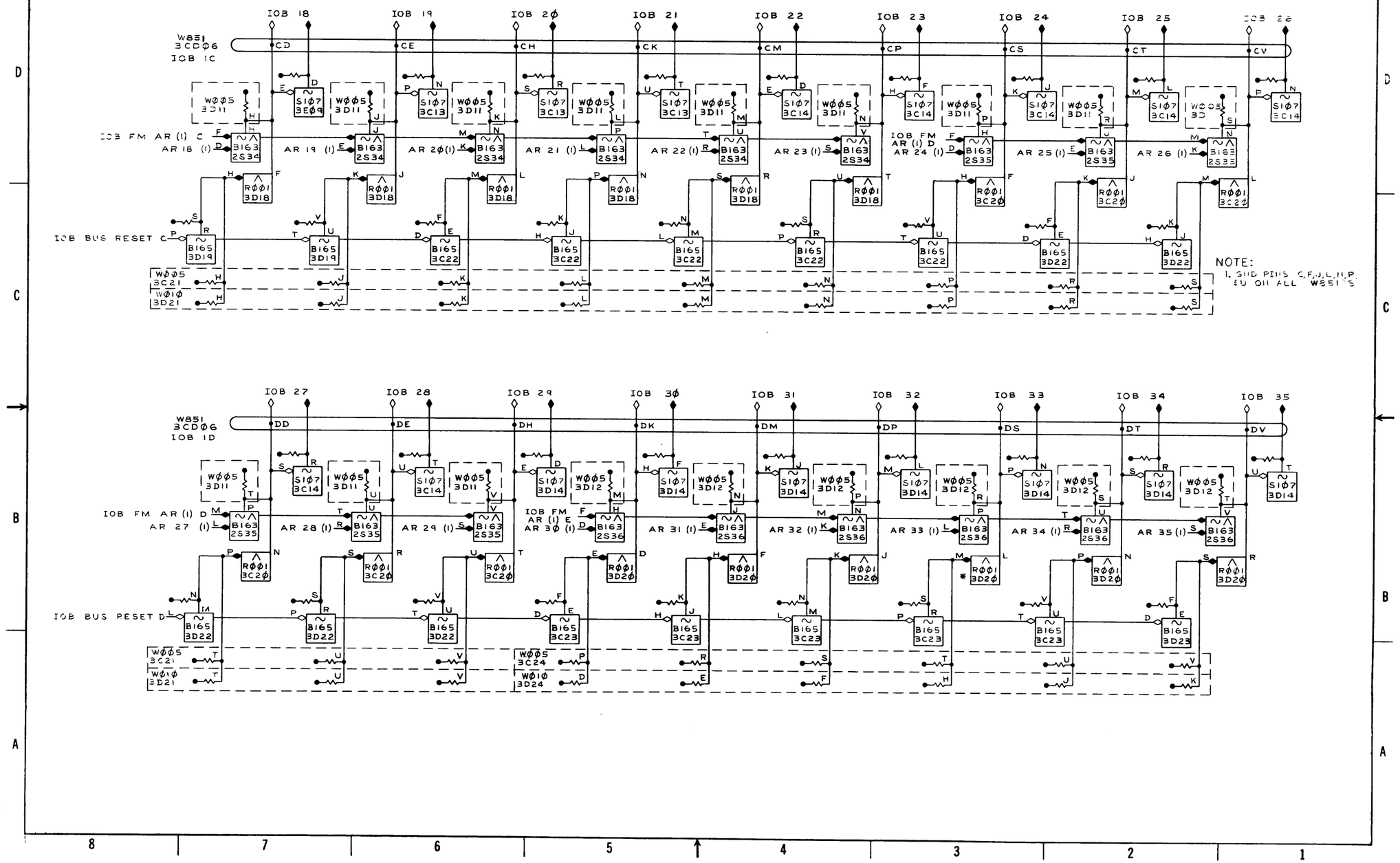
D-BS-KA10-0-HWT Half Word Transfer



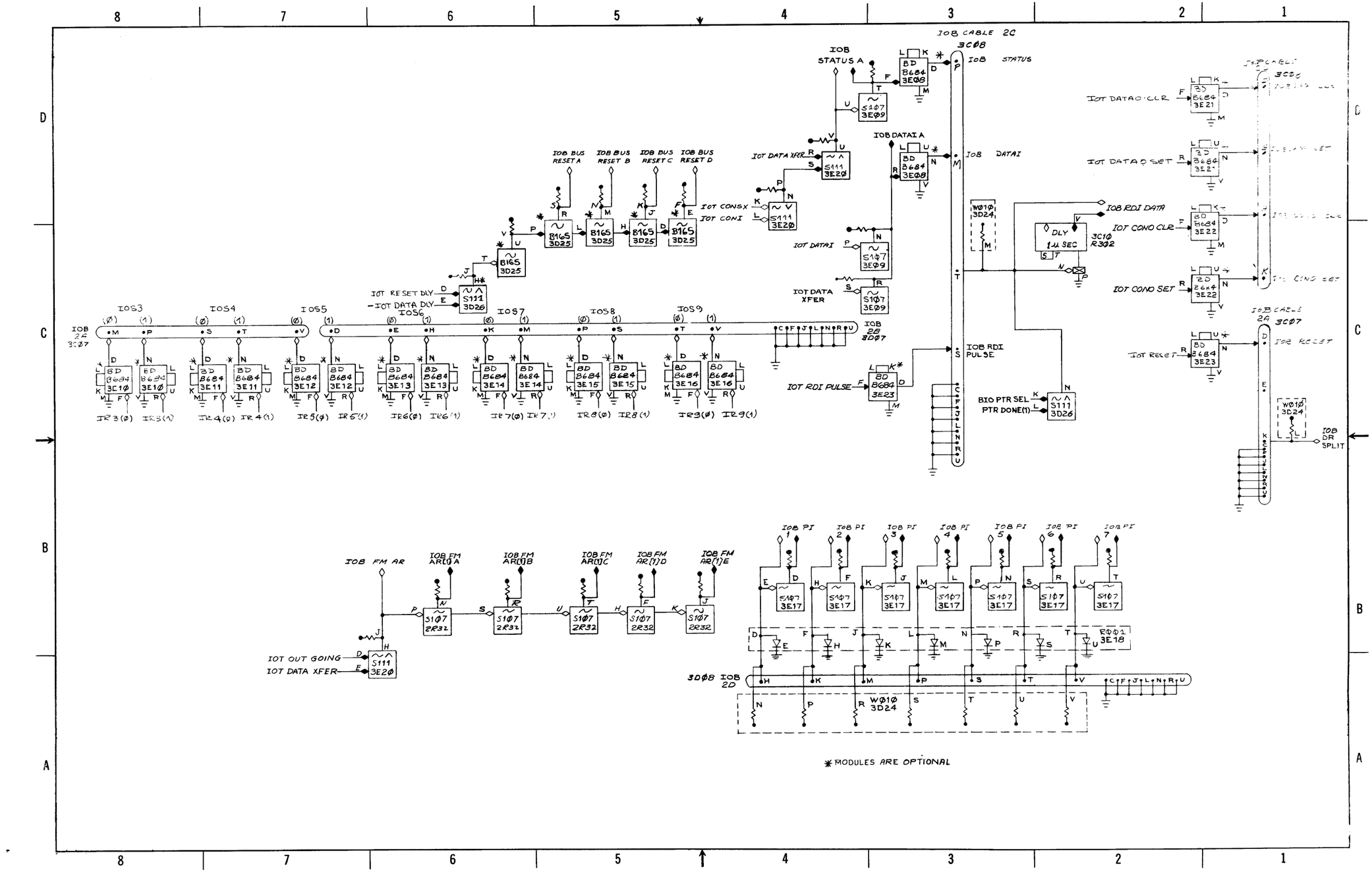
D-BS-KA10-0-IA Instruction and Address Cycles



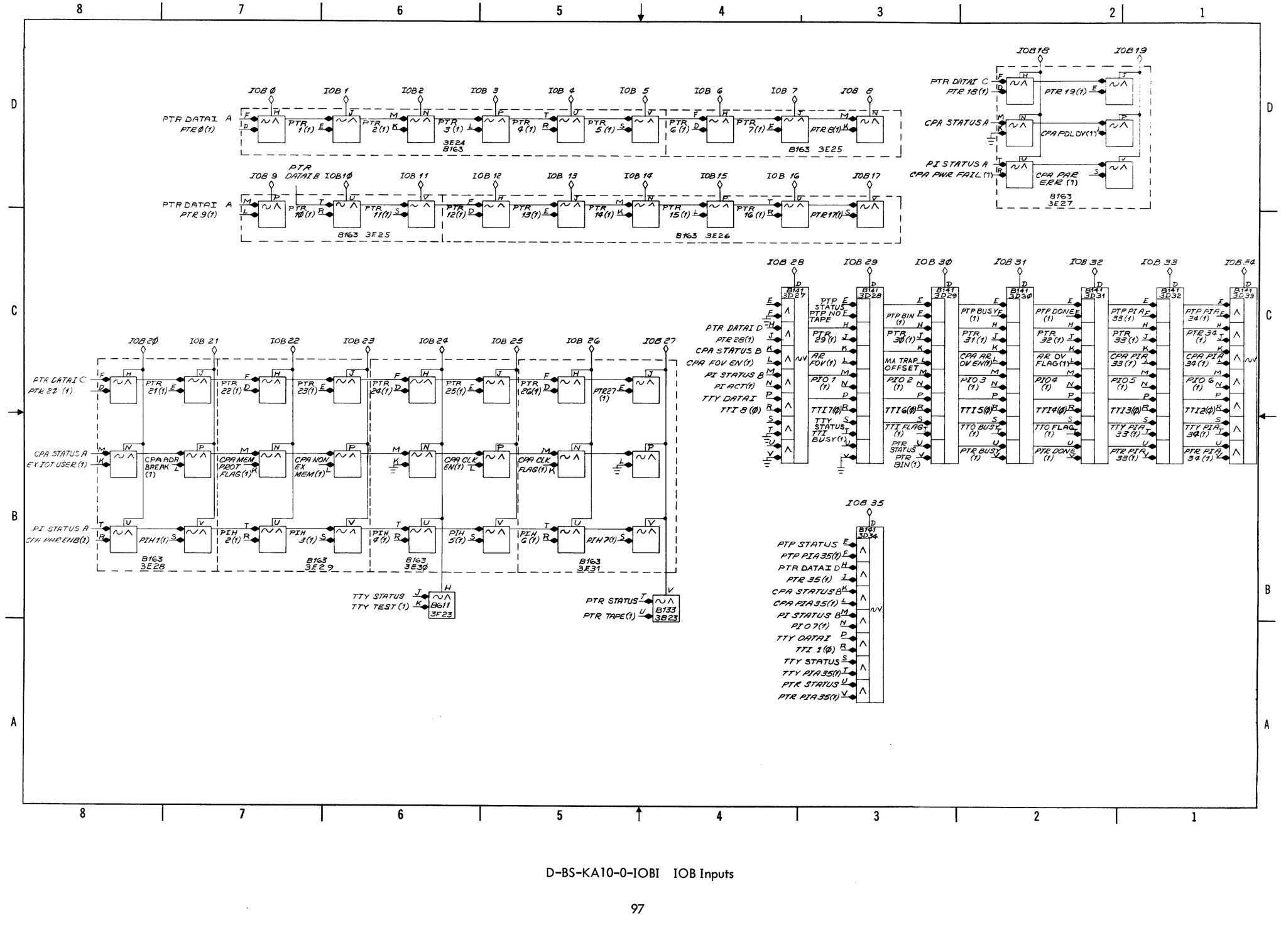
D-BS-KA10-0-IOB1 I/O Bus 0-17

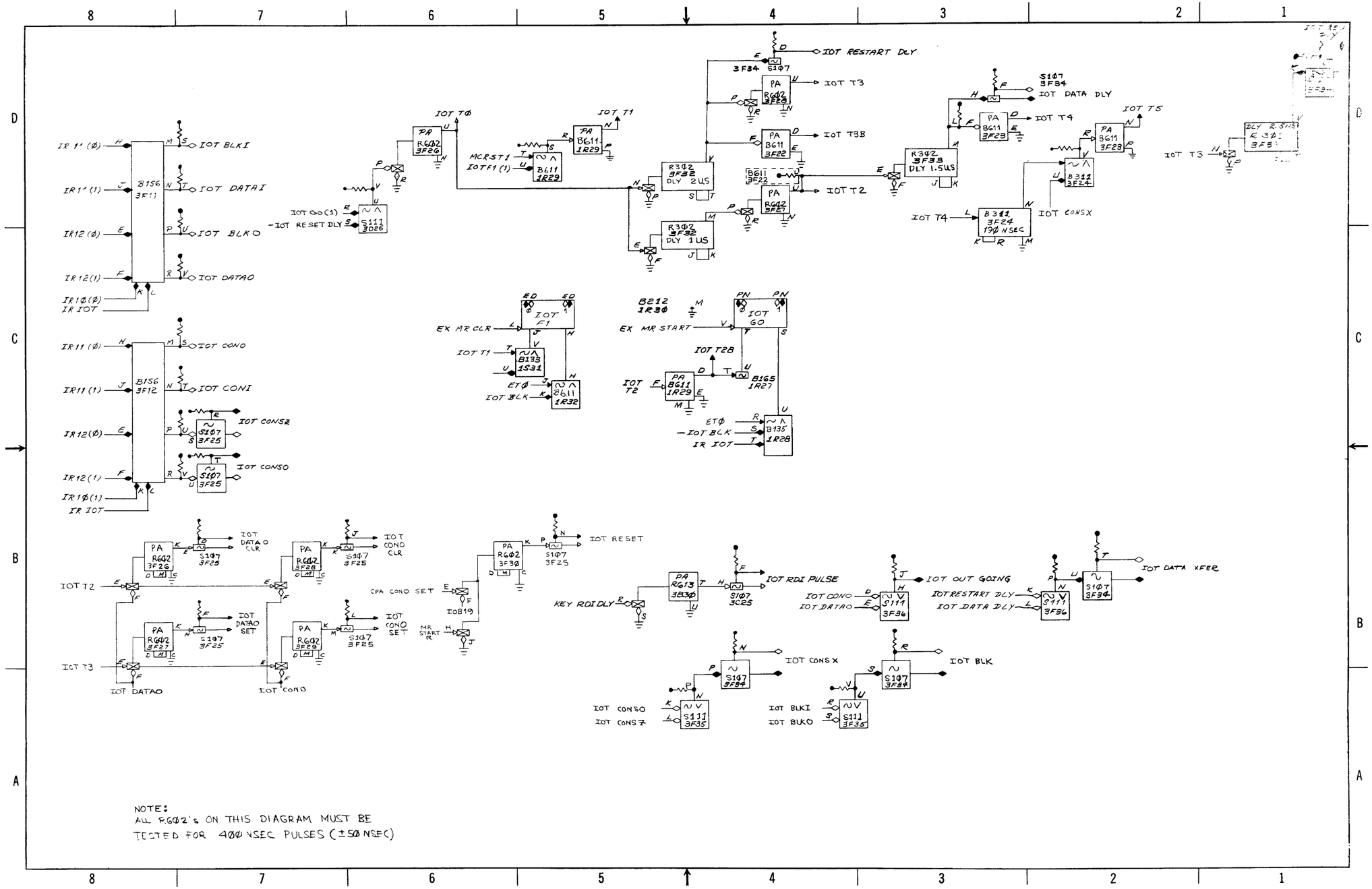


D-BS-KA10-0-IOB2 I/O Bus 18-35



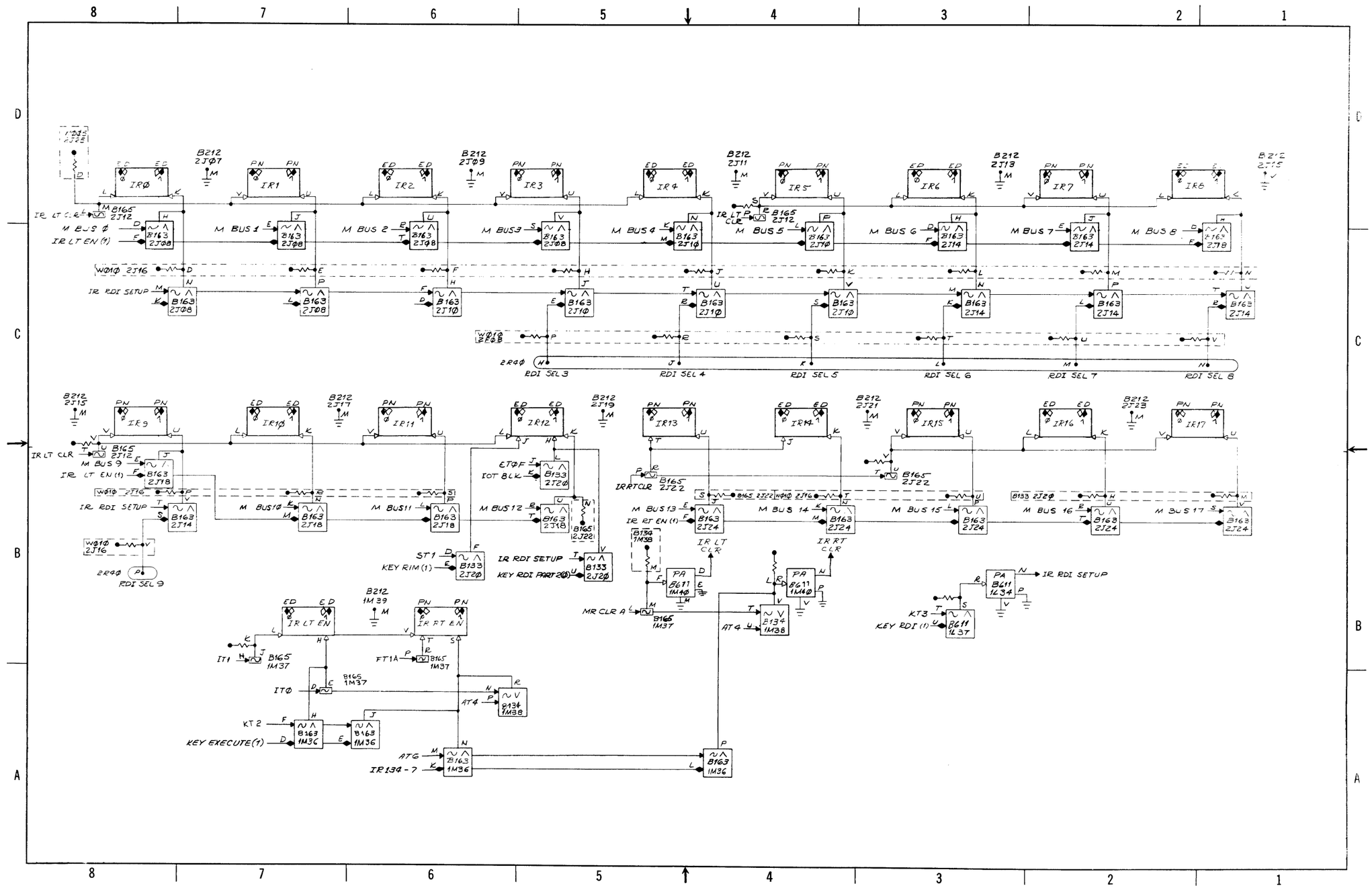
D-FD-KA10-0-IOBC I/O Bus Control and IO Selection


IOB Ø
IOB 1
IOB 2
IOB 3
IOB 4
IOB 5
IOB 6
IOB 7
IOB 8
PTR DATAI A
PTR Ø (1)
PTR 1 (1)
PTR 2 (1)
PTR 3 (1)
PTR 4 (1)
PTR 5 (1)
PTR 6 (1)
PTR 7 (1)
PTR 8 (1)
3E24 B163
B163 3E25
IOB 9
IOB 10
IOB 11
IOB 12
IOB 13
IOB 14
IOB 15
IOB 16
IOB 17
PTR DATAI B
PTR DATAI A
PTR 9 (1)
PTR 10 (1)
PTR 11 (1)
PTR 12 (1)
PTR 13 (1)
PTR 14 (1)
PTR 15 (1)
PTR 16 (1)
PTR 17 (1)
B163 3E25
B163 3E26
IOB 18
IOB 19
PTR DATAI C
PTR 18 (1)
PTR 19 (1)
CPA STATUS A
CPA PDL OV (1)
PI STATUS A
CPA PWR FAIL (1)
CPA PAR ERR (1)
B163 3E27
IOB 20
IOB 21
IOB 22
IOB 23
IOB 24
IOB 25
IOB 26
IOB 27
PTR DATAI C
PTR 20 (1)
PTR 21 (1)
PTR 22 (1)
PTR 23 (1)
PTR 24 (1)
PTR 25 (1)
PTR 26 (1)
PTR 27 (1)
CPA STATUS A
EX TOT USER (1)
CPA ADR BREAK (1)
CPA MEM PROT FLAG (1)
CPA NON EX MEM (1)
CPA CLK EN (1)
CPA CLK FLAG (1)
PI STATUS A
CPA PIR ENB (1)
PIH 1 (1)
PIH 2 (1)
PIH 3 (1)
PIH 4 (1)
PIH 5 (1)
PIH 6 (1)
PIH 7 (1)
B163 3E28
B163 3E29
B163 3E30
B163 3E31
TTY STATUS
TTY TEST (1)
B611 3F23
PTR STATUS
PTR TAPE (1)
B133 3B23
IOB 28
IOB 29
IOB 30
IOB 31
IOB 32
IOB 33
IOB 34
B141 3D27
B141 3D28
B141 3D29
B141 3D30
B141 3D31
B141 3D32
B141 3D33
PTR DATAI D
PTR 28 (1)
CPA STATUS B
CPA FOV EN (1)
PI STATUS B
PI ACT (1)
TTY DATAI
TTI 8 (Ø)
PTP STATUS
PTP NOT TAPE
PTR 29 (1)
AR FOV (1)
PIO 1 (1)
TTI 7 (Ø)
TTY STATUS
TTI BUSY (1)
PTP BIN (1)
PTR 30 (1)
MA TRAP OFFSET
PIO 2 (1)
TTI 6 (Ø)
TTI FLAG (1)
PTR STATUS
PTR BIN (1)
PTP BUSY (1)
PTR 31 (1)
CPA AR OV EN (1)
PIO 3 (1)
TTI 5 (Ø)
TTO BUSY (1)
PTR BUSY (1)
PTP DONE (1)
PTR 32 (1)
AR OV FLAG (1)
PIO 4 (1)
TTI 4 (Ø)
TTO FLAG (1)
PTR DONE (1)
PTP PIA 33 (1)
PTR 33 (1)
CPA PIA 33 (1)
PIO 5 (1)
TTI 3 (Ø)
TTY PIA 33 (1)
PTR PIA 33 (1)
PTP PIA 34 (1)
PTR 34 (1)
CPA PIA 34 (1)
PIO 6 (1)
TTI 2 (Ø)
TTY PIA 34 (1)
PTR PIA 34 (1)
IOB 35
B141 3D34
PTP STATUS
PTP PIA 35 (1)
PTR DATAI D
PTR 35 (1)
CPA STATUS B
CPA PIA 35 (1)
PI STATUS B
PI O 7 (1)
TTY DATAI
TTI 1 (Ø)
TTY STATUS
TTY PIA 35 (1)
PTR STATUS
PTR PIA 35 (1)

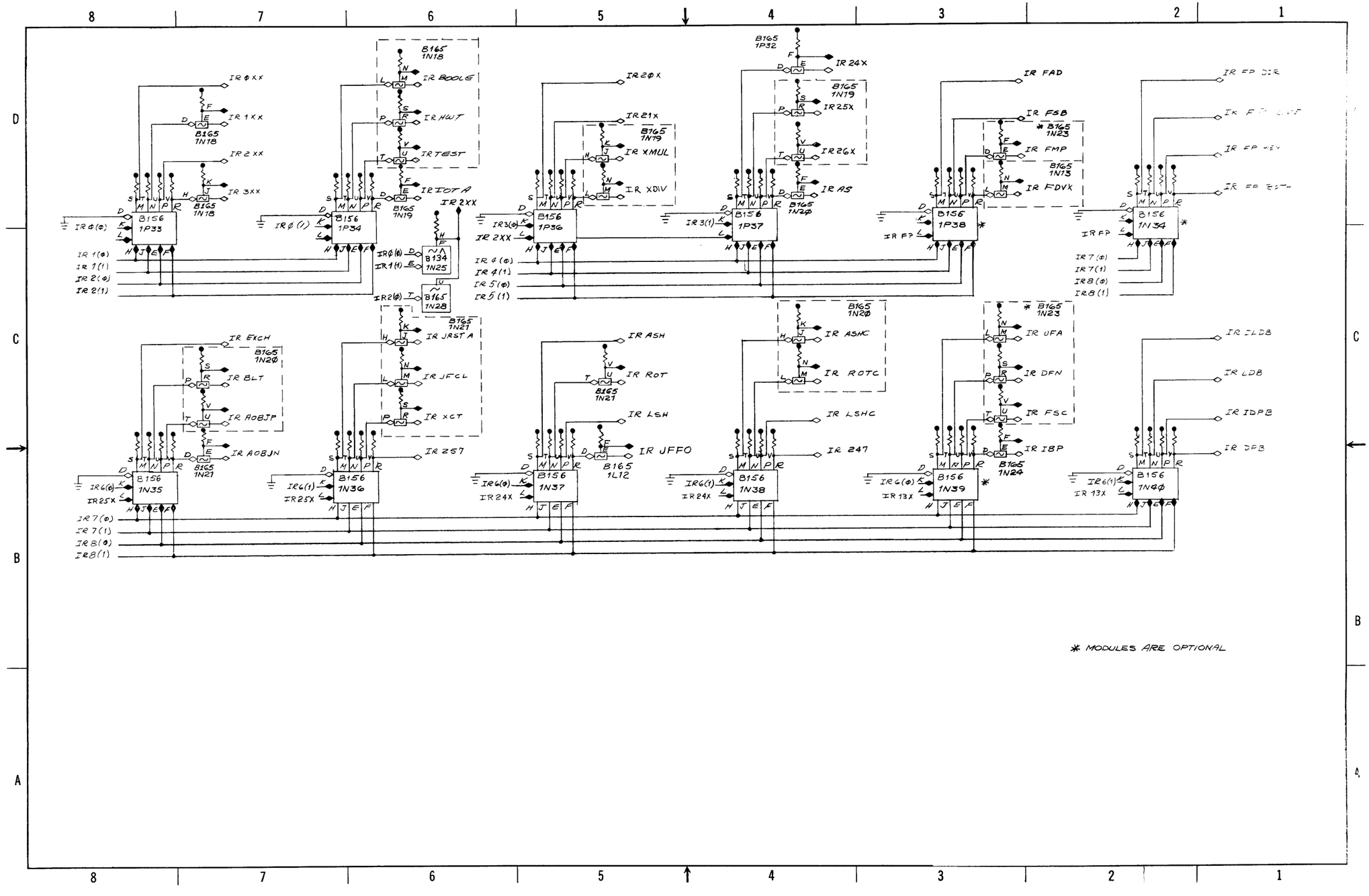


NOTE:
ALL RGØ2's ON THIS DIAGRAM MUST BE TESTED FOR 400 NSEC PULSES (±50 NSEC)

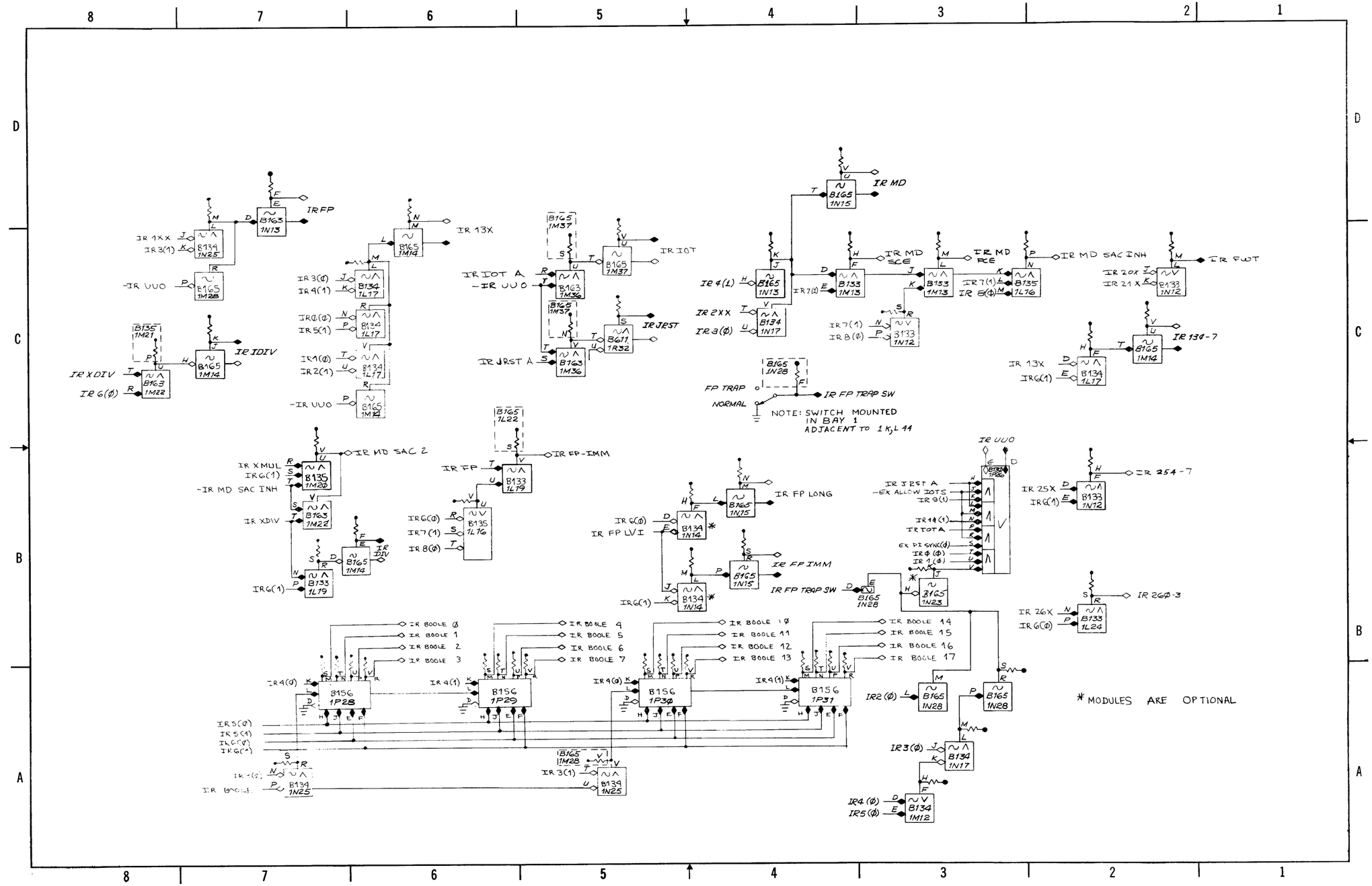
D-BS-KA10-0-IOT In-Out Transfer Control



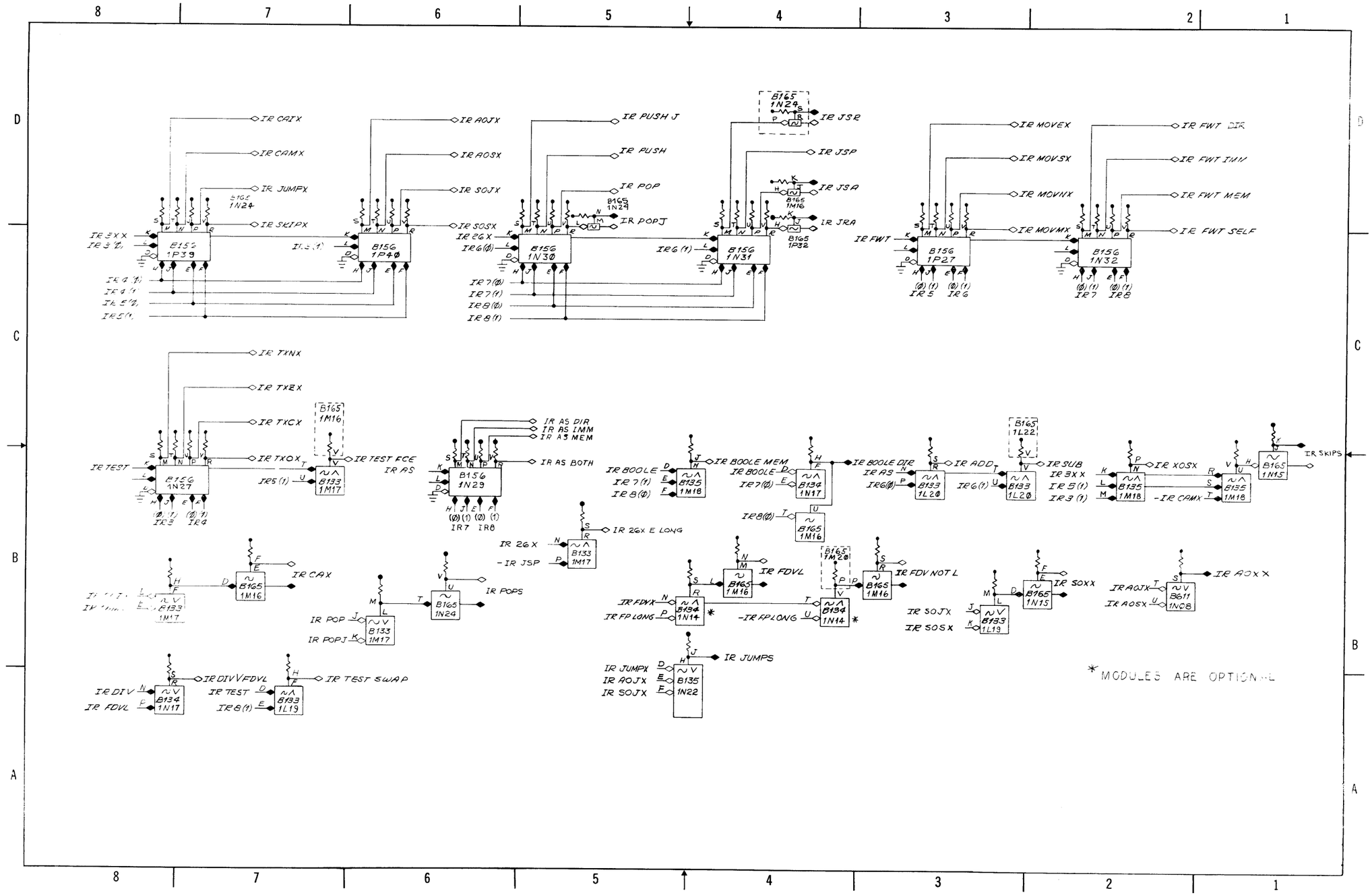
D-FD-KA10-0-IR Instruction Register



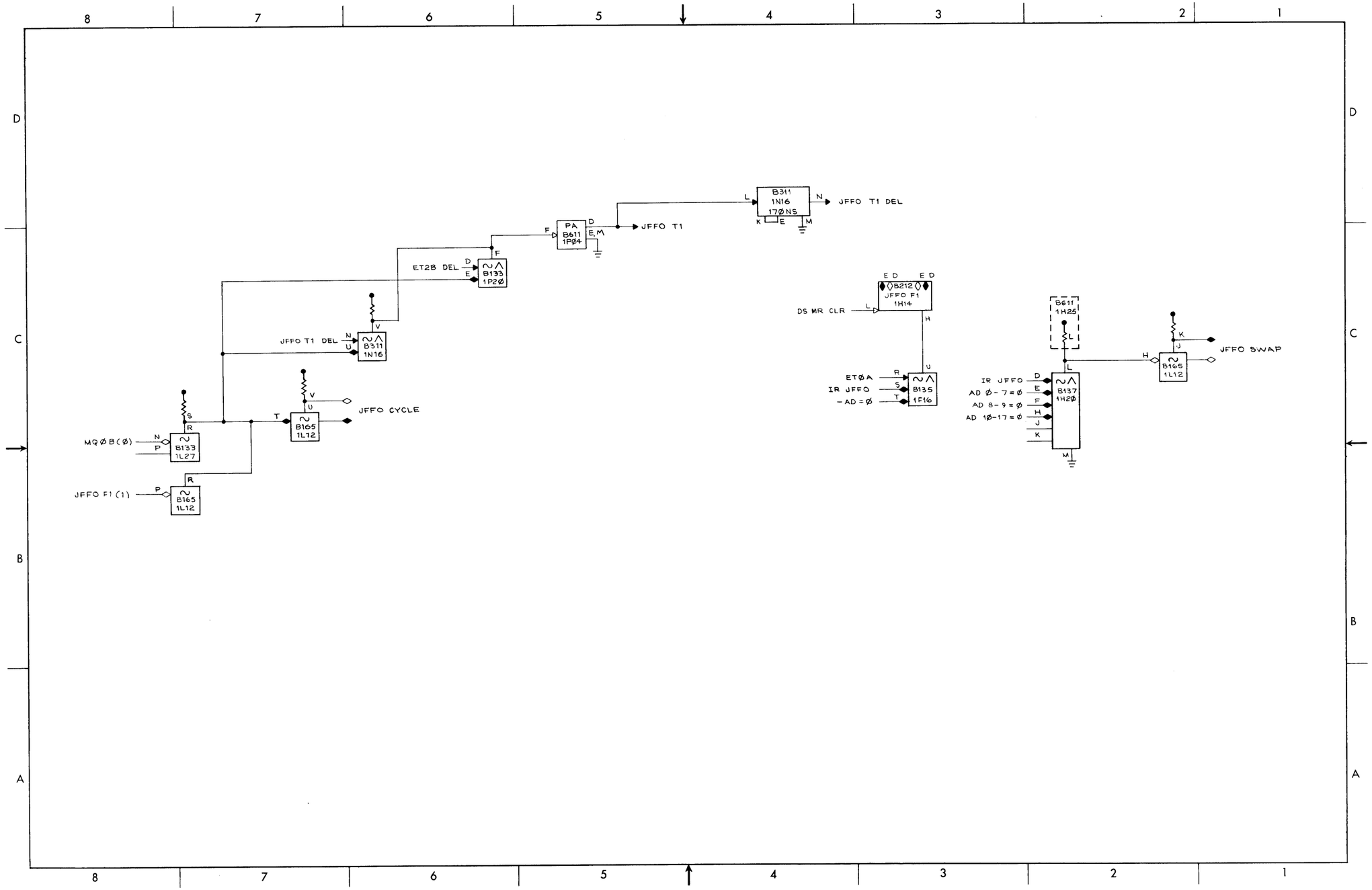
D-BS-KA10-0-IR1 IR Decoding



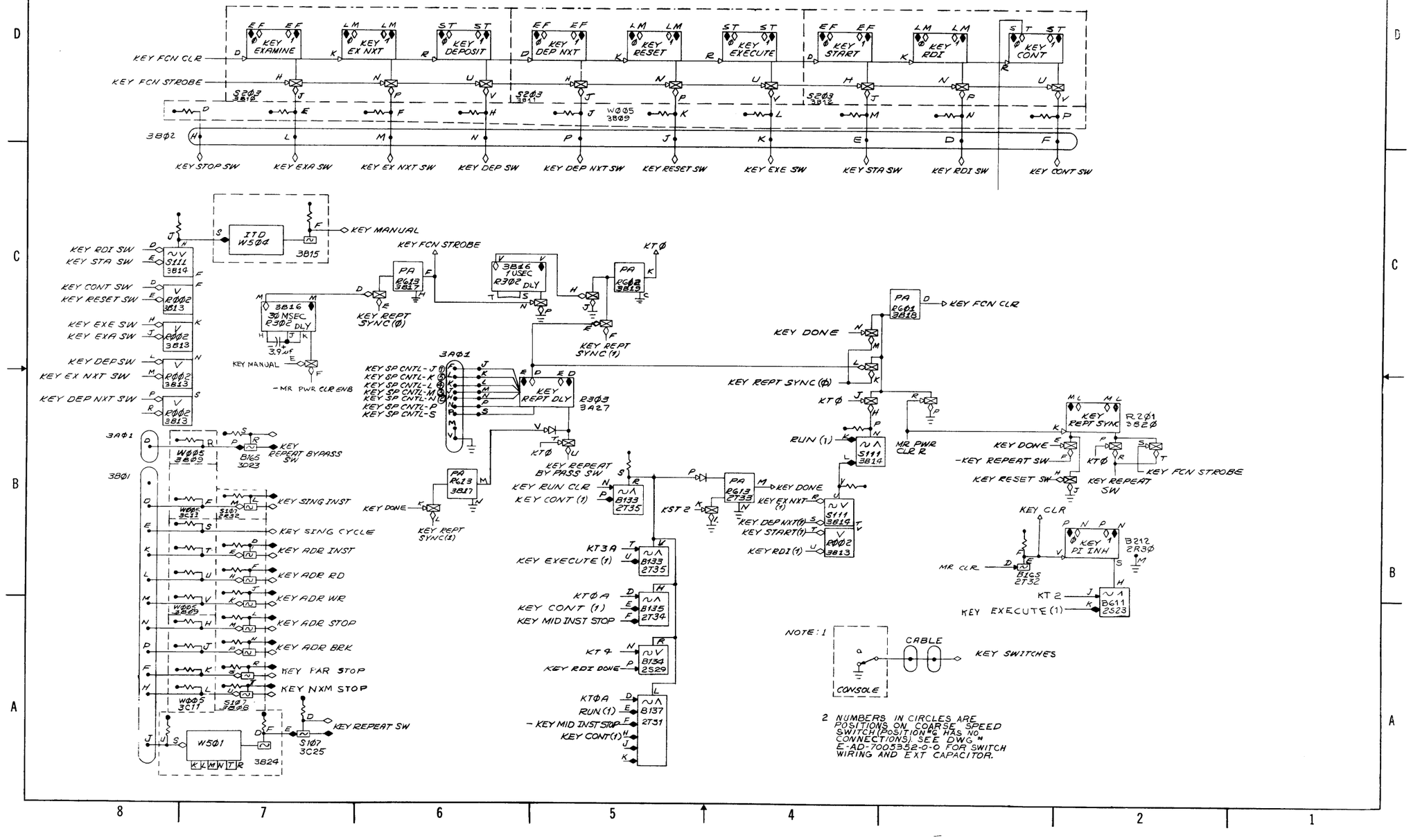
D-BS-KA10-0-IR2 IR Decoding



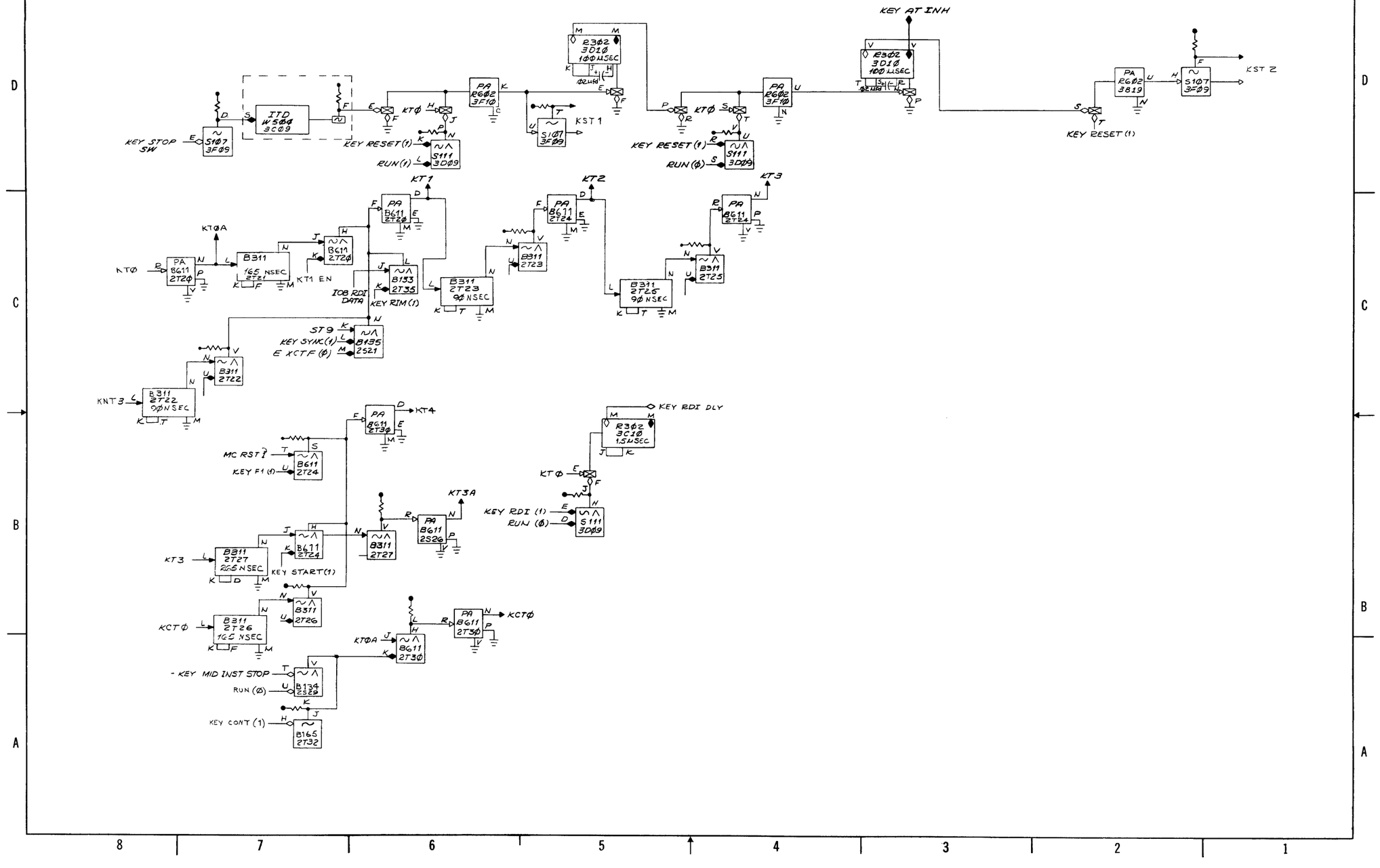
D-BS-KA10-0-IR3 IR Decoding



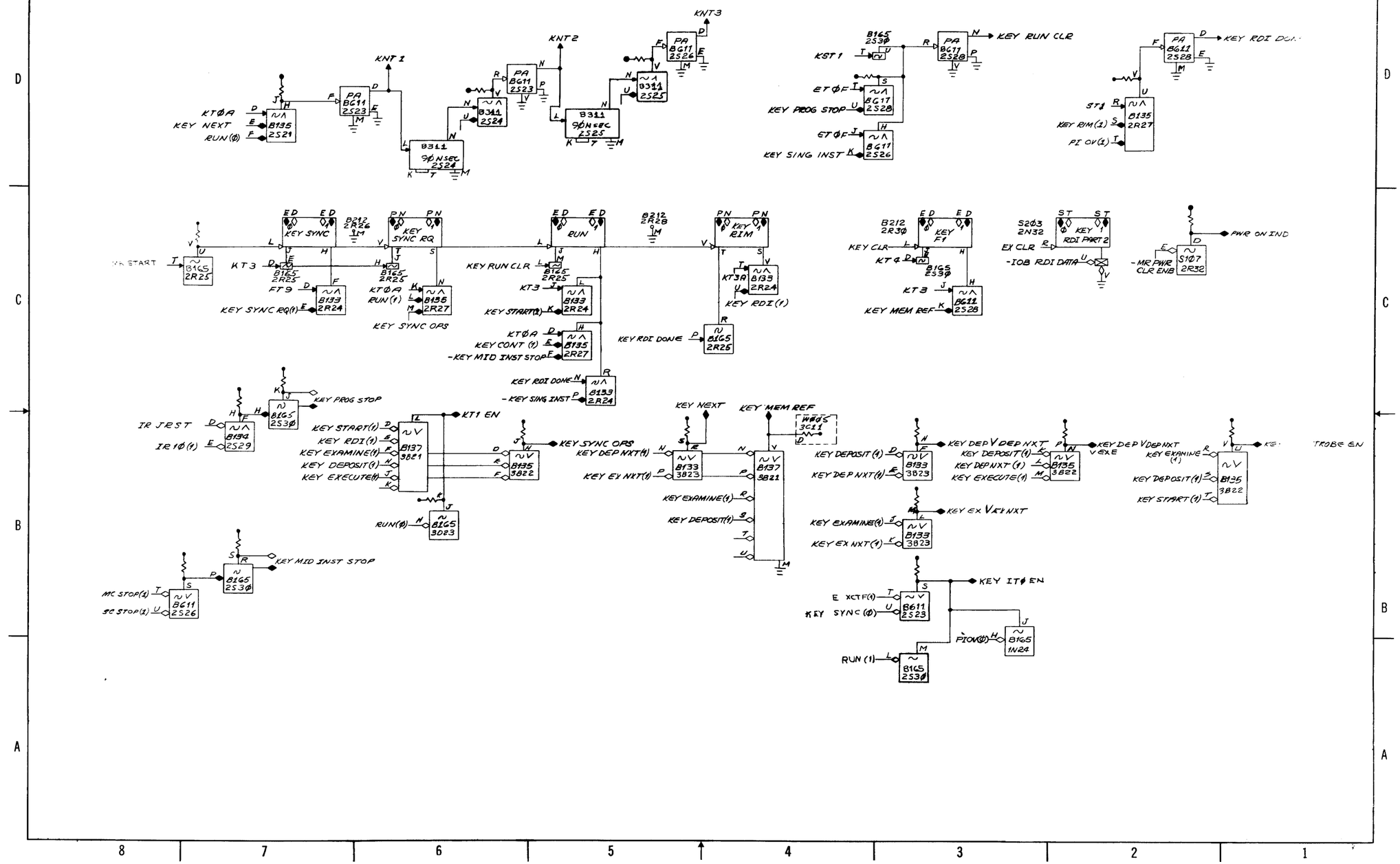
D-BS-KA10-0-JFFO JFFO Instruction Control



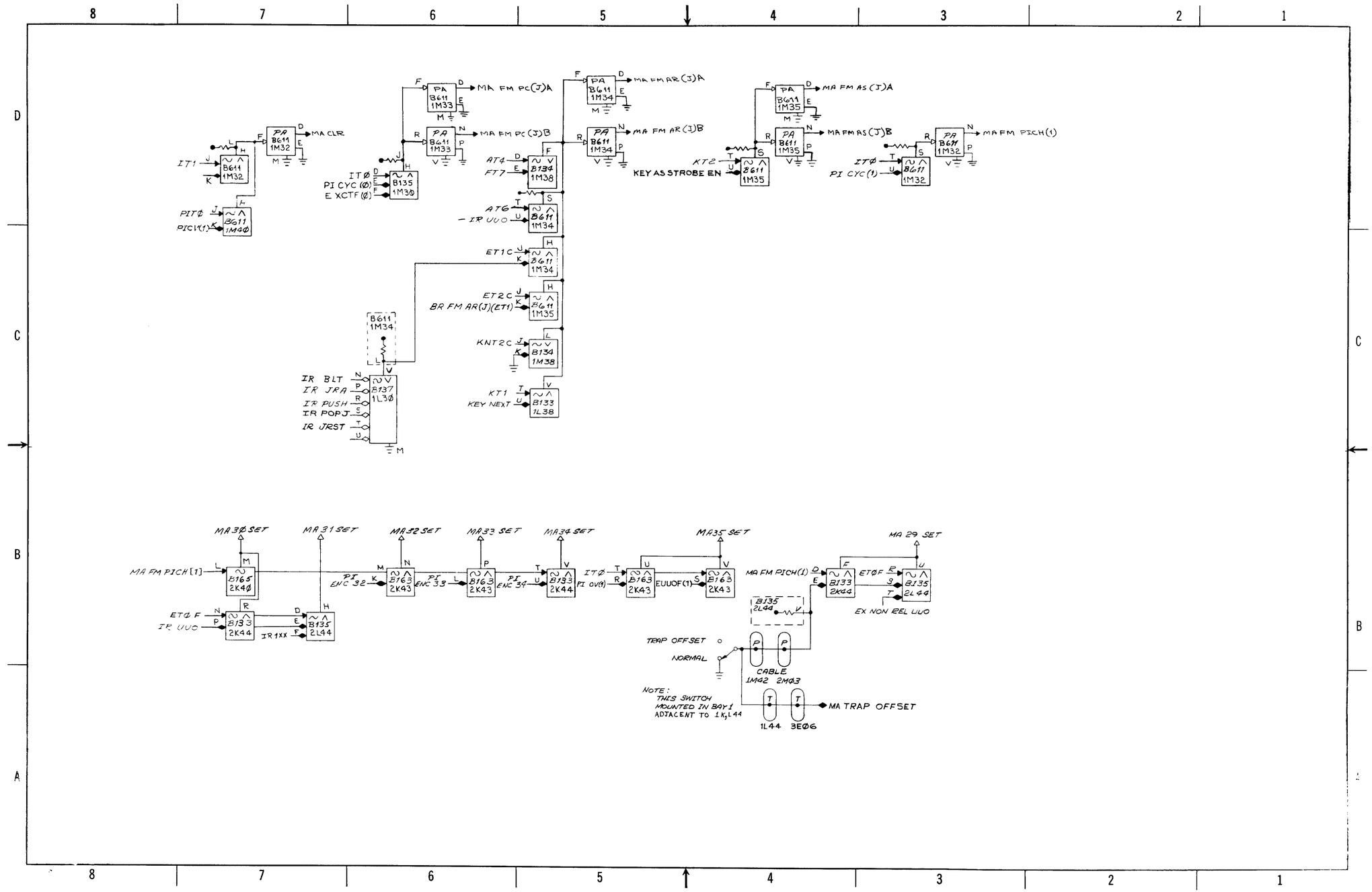
D-BS-KA10-0-KEY1 Key and Switches Controls

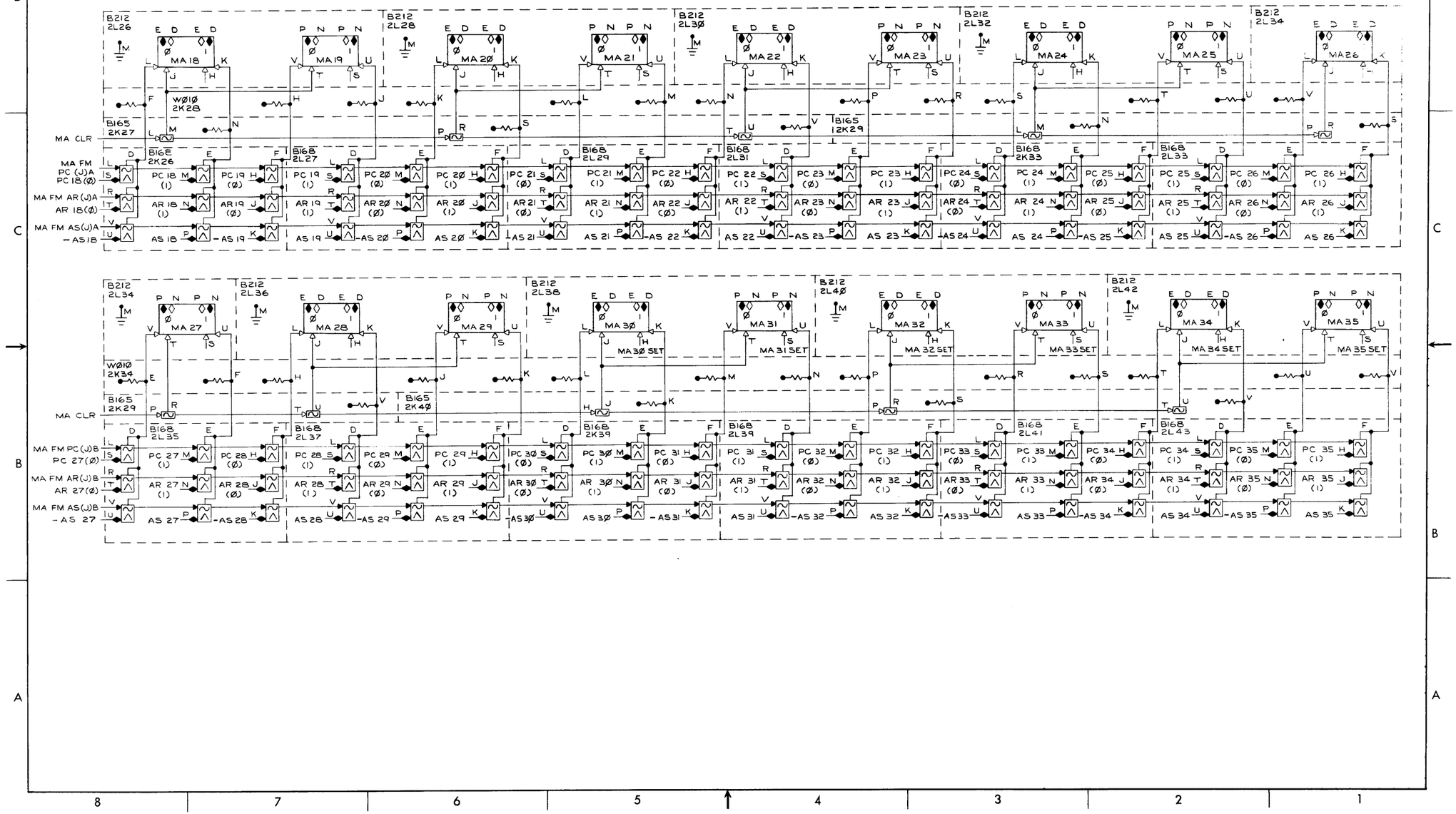


D-BS-KA10-0-KEY2 Keys and Switches Controls

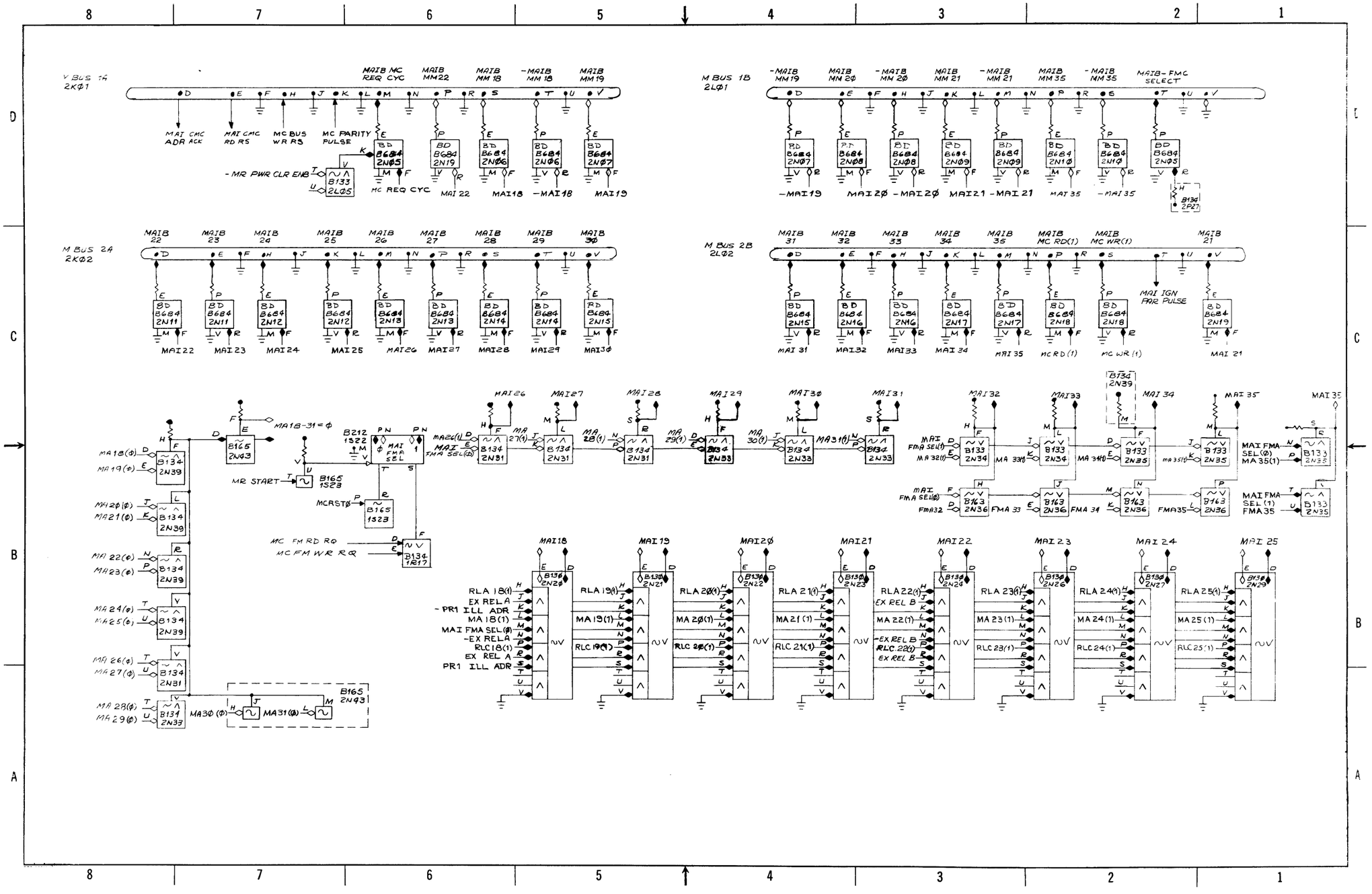


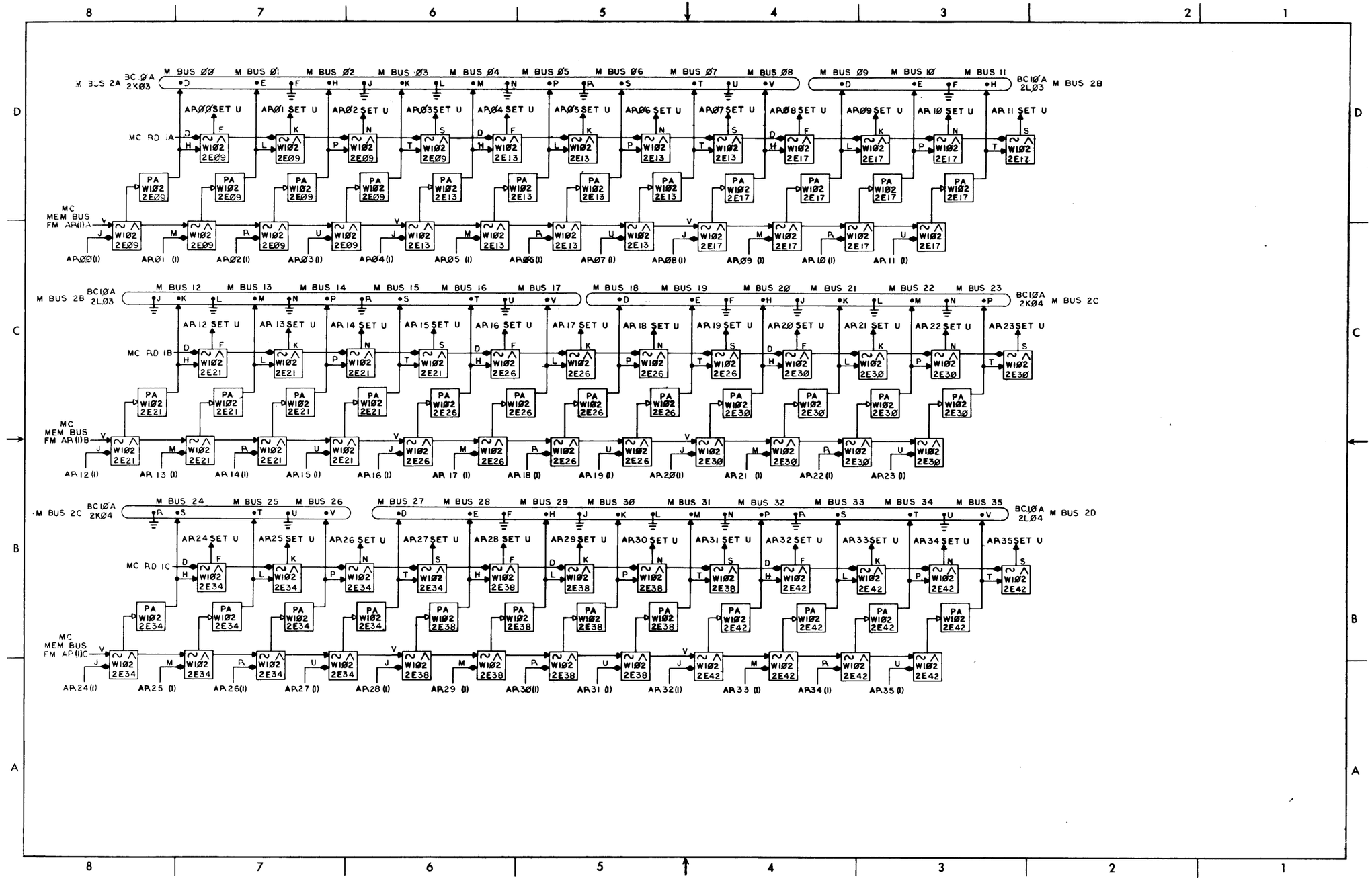
D-BS-KA10-0-KEY3 Keys and Switches Controls

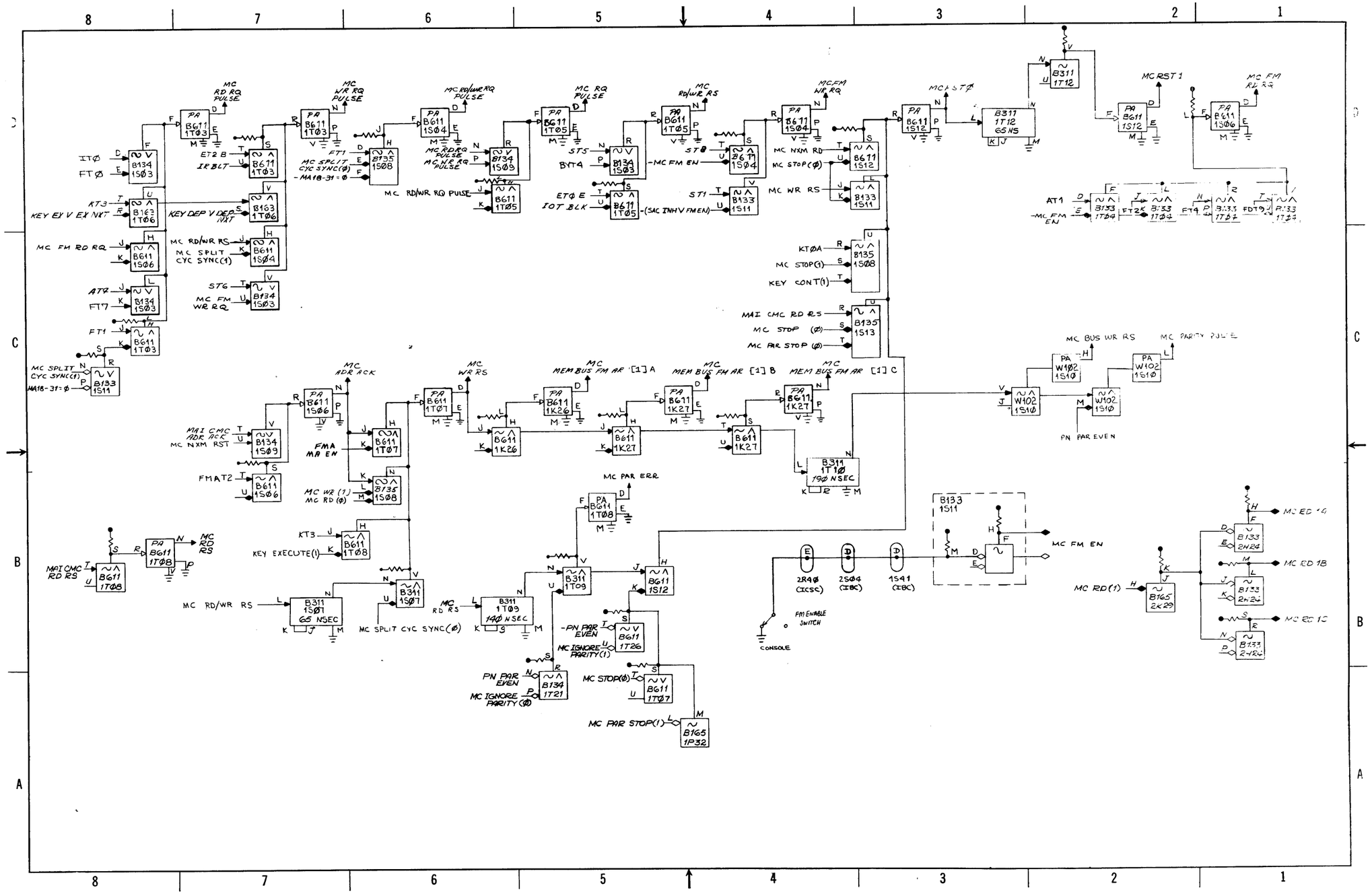

MA CLR
IT1
PIT∅
PICYC(1)
MA FM PC(J)A
MA FM PC(J)B
IT∅
PI CYC (∅)
E XCTF (∅)
AT4
FT7
AT6
– IR UUO
ET1C
ET2C
BR FM AR(J)(ET1)
KNT2C
KT1
KEY NEXT
IR BLT
IR JRA
IR PUSH
IR POPJ
IR JRST
MA FM AR(J)A
MA FM AR(J)B
KEY AS STROBE EN
XT2
MA FM AS(J)A
MA FM AS(J)B
IT∅
PI CYC(1)
MA FM PICH(1)
MA 30 SET
MA 31 SET
MA 32 SET
MA 33 SET
MA 34 SET
MA 35 SET
MA 29 SET
MA FM PICH[1]
PI ENC 32
PI ENC 33
PI ENC 34
IT∅
PI OV(1)
EUUOF(1)
ET∅ F
IR UUO
IR1XX
MA FM PICH(1)
ET∅F
EX NON EEL UUO
TRAP OFFSET
NORMAL
CABLE
1M42 2M03
NOTE:
TWIS SWITCH
MOUNTED IN BAY 1
ADJACENT TO 1K,L44
MA TRAP OFFSET
1L44 3E06

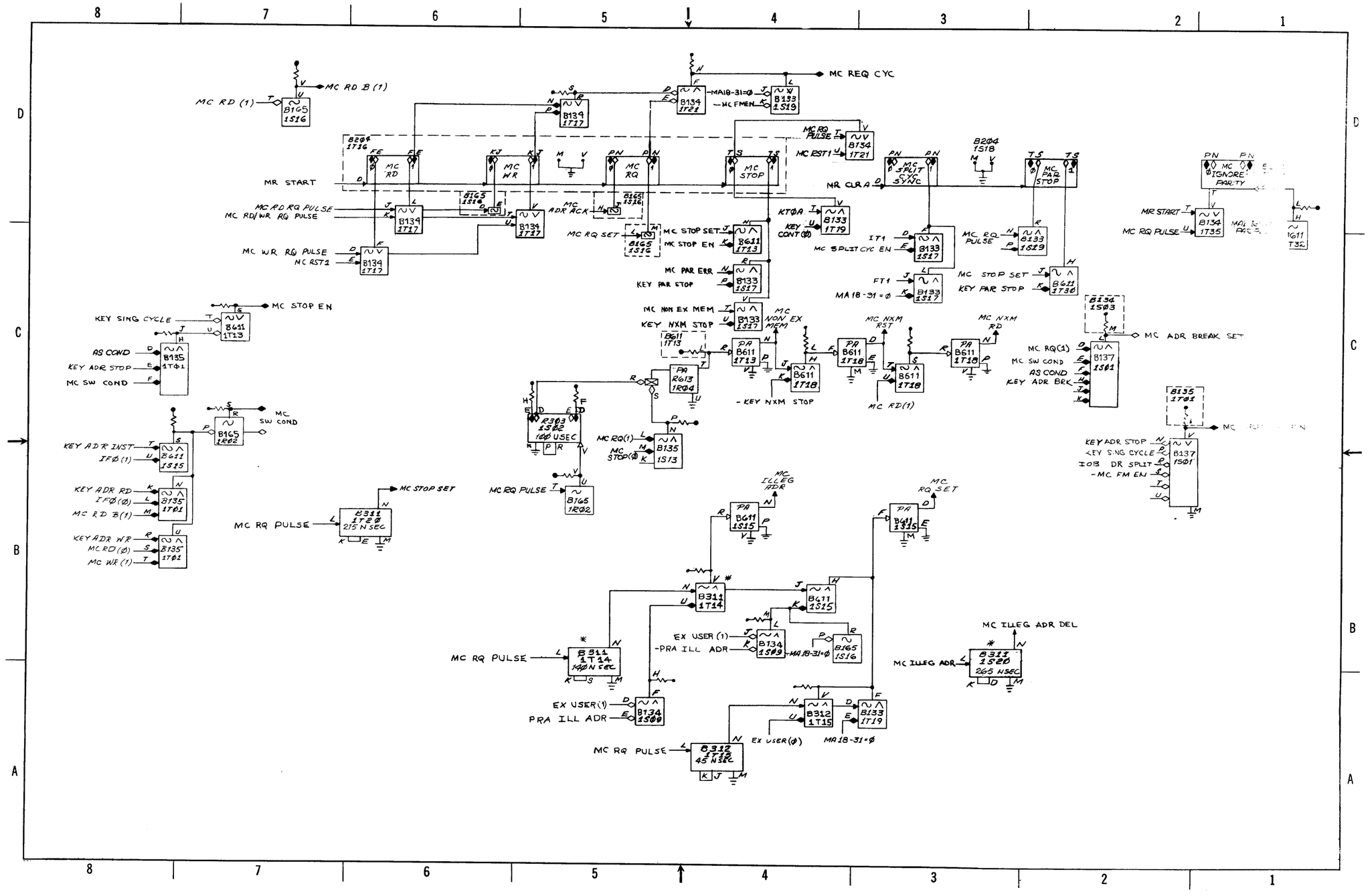


D-BS-KA10-0-MA2 MA Register

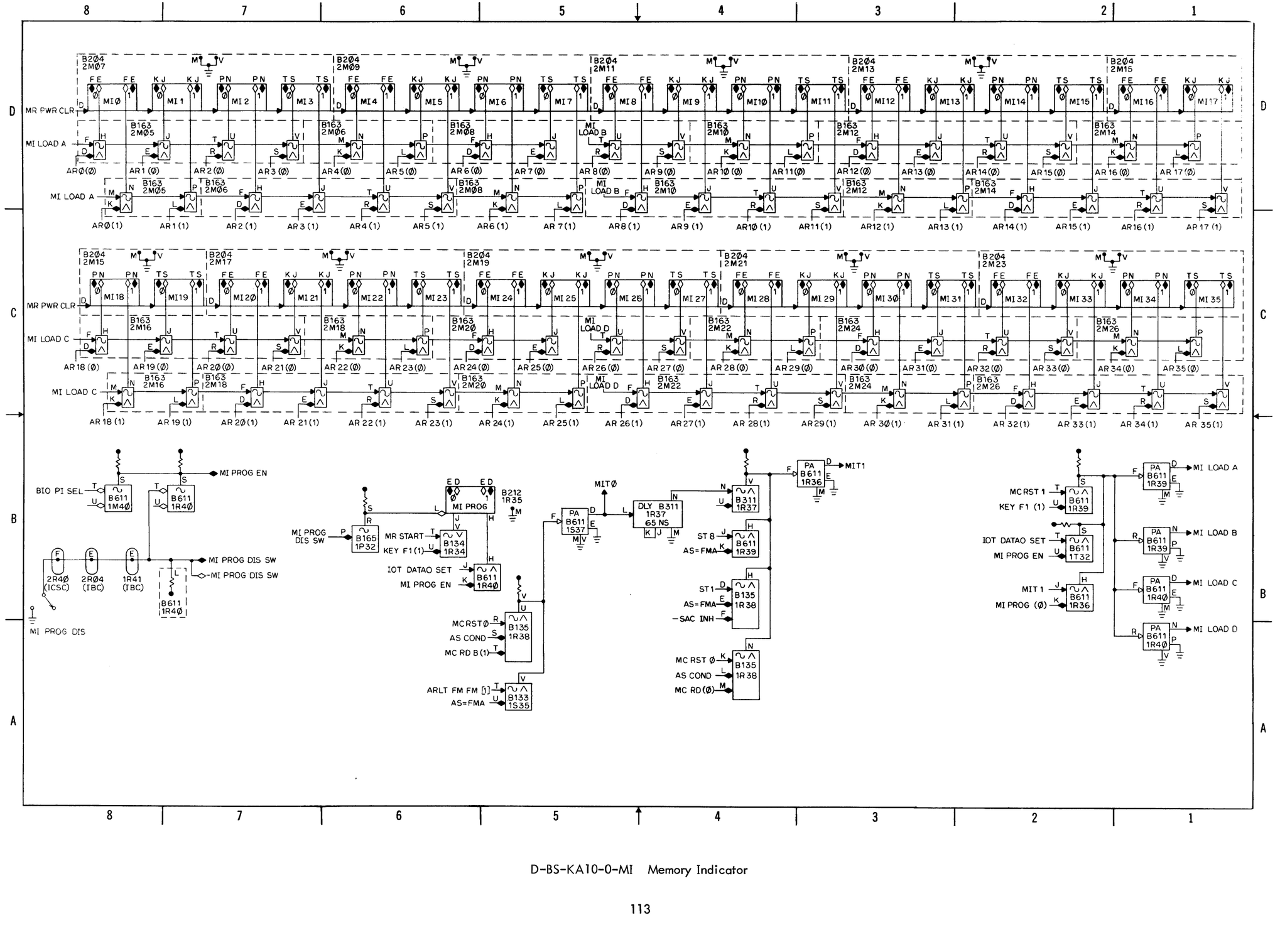

V BUS 1A 2KØ1
MAIB NC REQ CYC
MAIB MM22
MAIB MM 18
-MAIB MM 18
MAIB MM19
MAI CMC ADR ACK
MAI CMC RD RS
MC BUS WR RS
MC PARITY PULSE
-MR PWR CLR ENB
MC REQ CYC
MAI 22
MAI18
-MAI18
MAI19
M BUS 1B 2LØ1
-MAIB MM19
MAIB MM 20
-MAIB MM 20
MAIB MM 21
-MAIB MM 21
MAIB MM 35
-MAIB MM 35
MAIB-FMC SELECT
-MAI19
MAI2Ø
-MAI2Ø
MAI21
-MAI 21
MAI 35
-MAI 35
B134 2P27
M BUS 2A 2KØ2
MAIB 22
MAIB 23
MAIB 24
MAIB 25
MAIB 2G
MAIB 27
MAIB 28
MAIB 29
MAIB 3Ø
MAI22
MAI 23
MAI24
MAI 25
MAI26
MAI27
MAI28
MAI29
MAI3Ø
M BUS 2B 2LØ2
MAIB 31
MAIB 32
MAIB 33
MAIB 34
MAIB 35
MAIB MC RD(1)
MAIB MC WR(1)
MAIB 21
MAI IGN ERR PULSE
MAI 31
MAI32
MAI33
MAI 34
MAI 35
MC RD (1)
MC WR (1)
MAI 21
MA18-31=Ø
MA 18(Ø)
MA 19(Ø)
MA 2Ø(Ø)
MA 21(Ø)
MA 22(Ø)
MA 23(Ø)
MA 24(Ø)
MA 25(Ø)
MA 26(Ø)
MA 27(Ø)
MA 28(Ø)
MA 29(Ø)
MA 3Ø(Ø)
MA 31(Ø)
MR START
MCRSTØ
MC FM RD RQ
MC FM WR RQ
MAI FMA SEL(Ø)
MAI FMA SEL(1)
MA26(1)
MA 27(1)
MA 28(1)
MA 29(1)
MA 3Ø(1)
MA 31(1)
MA 32(1)
MA 33(1)
MA 34(1)
MA 35(1)
FMA32
FMA 33
FMA 34
FMA35
MAI18
MAI 19
MAI2Ø
MAI21
MAI22
MAI 23
MAI 24
MAI 25
RLA 18(1)
EX REL A
-PR1 ILL ADR
MA 18(1)
MAI FMA SEL(Ø)
-EX REL A
RLC 18(1)
EX REL A
PR1 ILL ADR
RLA 19(1)
MA 19(1)
RLC 19(1)
RLA 2Ø(1)
MA 2Ø(1)
RLC 2Ø(1)
RLA 21(1)
MA 21 (1)
RLC 21(1)
RLA 22(1)
EX REL B
MA 22(1)
-EX REL B
RLC 22(1)
EX REL B
RLA 23(1)
MA 23 (1)
RLC 23(1)
RLA 24(1)
MA 24 (1)
RLC 24(1)
RLA 25(1)
MA 25 (1)
RLC 25(1)

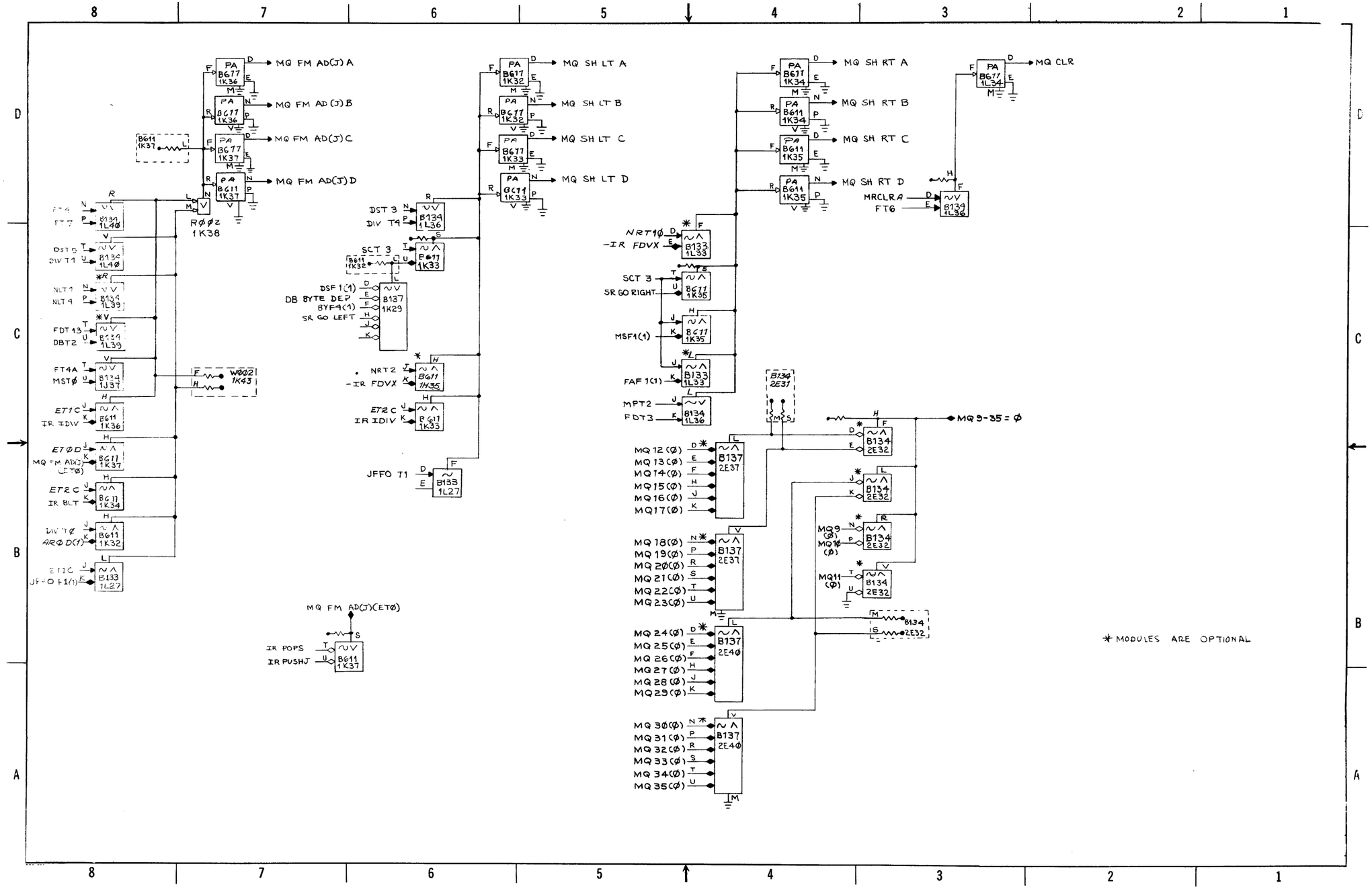

M BUS 2A
BC ØA 2KØ3
M BUS ØØ M BUS Ø1 M BUS Ø2 M BUS Ø3 M BUS Ø4 M BUS Ø5 M BUS Ø6 M BUS Ø7 M BUS Ø8 M BUS Ø9 M BUS IØ M BUS 11
BC IØA 2LØ3
M BUS 2B
ARØØ SET U ARØ1 SET U ARØ2 SET U ARØ3 SET U ARØ4 SET U ARØ5 SET U ARØ6 SET U ARØ7 SET U ARØ8 SET U ARØ9 SET U AR IØ SET U AR 11 SET U
MC RD IA
PA WIØ2 2EØ9
PA WIØ2 2E13
PA WIØ2 2E17
MC MEM BUS FM AR(I)A
WIØ2 2EØ9
WIØ2 2E13
WIØ2 2E17
ARØØ(I) ARØ1 (I) ARØ2(I) ARØ3 (I) APØ4(I) ARØ5 (I) ARØ6(I) ARØ7 (I) ARØ8(I) ARØ9 (I) AR IØ (I) AR 11 (I)
M BUS 2B
BC IØA 2LØ3
M BUS 12 M BUS 13 M BUS 14 M BUS 15 M BUS 16 M BUS 17 M BUS 18 M BUS 19 M BUS 2Ø M BUS 21 M BUS 22 M BUS 23
BC IØA 2KØ4
M BUS 2C
AR12 SET U AR13 SET U AR14 SET U AR15 SET U AR16 SET U AR17 SET U AR18 SET U AR19 SET U AR2Ø SET U AR21 SET U AR22 SET U AR23 SET U
MC RD IB
PA WIØ2 2E21
PA WIØ2 2E26
PA WIØ2 2E3Ø
MC MEM BUS FM AR(I)B
WIØ2 2E21
WIØ2 2E26
WIØ2 2E3Ø
AR12 (I) AR 13 (I) AR 14 (I) AR15 (I) AR16 (I) AR 17 (I) AR 18 (I) AR19 (I) AR2Ø(I) AR21 (I) AR22 (I) AR23 (I)
M BUS 2C
BC IØA 2KØ4
M BUS 24 M BUS 25 M BUS 26 M BUS 27 M BUS 28 M BUS 29 M BUS 3Ø M BUS 31 M BUS 32 M BUS 33 M BUS 34 M BUS 35
BC IØA 2LØ4
M BUS 2D
AR24 SET U AR25 SET U AR26 SET U AR27 SET U AR28 SET U AR29 SET U AR30 SET U AR31 SET U AR32 SET U AR33 SET U AR34 SET U AR35 SET U
MC RD IC
PA WIØ2 2E34
PA WIØ2 2E38
PA WIØ2 2E42
MC MEM BUS FM AR(I)C
WIØ2 2E34
WIØ2 2E38
WIØ2 2E42
AR24(I) AR25 (I) AR26(I) AR27 (I) AR28 (I) AR29 (I) AR3Ø(I) AR31 (I) AR32(I) AR33 (I) AR34 (I) AR35 (I)


MC RD RQ PULSE
MC WR RQ PULSE
MC RD/WR RQ PULSE
MC RQ PULSE
MC RD/WR RS
MC FM WR RQ
MC STØ
MC RST 1
MC FM RD RQ
IRBLT
ET2 B
FT1
MC SPLIT CYC SYNC(Ø)
-MA18-31=Ø
MC RD/WR RQ PULSE
MC RD/WR RQ PULSE
STS
BYT4
STØ
-MC FM EN
ETØ E
IOT BLK
ST1
-(SAC INH V FMEN)
MC NXM RD
MC STOP(Ø)
MC WR RS
KEY EX V EX NXT
KEY DEP V DEP NXT
MC FM RD RQ
MC RD/WR RS
MC SPLIT CYC SYNC(1)
STG
MC FM WR RQ
ATQ
FT7
FT1
MC SPLIT CYC SYNC(1)
-MA18-31=Ø
KTØA
MC STOP(1)
KEY CONT(1)
MAI CMC RD RS
MC STOP (Ø)
MC PAR STOP (Ø)
MC BUS WR RS
MC PARITY PULSE
PN PAR EVEN
AT1
-MC FM EN
FT2K
FT4
FDT9
MC ADR ACK
MC WR RS
MC MEM BUS FM AR [1] A
MC MEM BUS FM AR [1] B
MC MEM BUS FM AR [1] C
MAI CMC ADR ACK
MC NXM RST
FMA MA EN
FMAT2
MC WR (1)
MC RD (Ø)
MC PAR ERR
MAI CMC RD RS
MC RD RS
KT3
KEY EXECUTE(1)
MC RD/WR RS
MC SPLIT CYC SYNC(Ø)
MC RD RS
-PN PAR EVEN
MC IGNORE PARITY(1)
PN PAR EVEN
MC IGNORE PARITY(Ø)
MC STOP(Ø)
MC PAR STOP(1)
B133 1S11
2R9Ø (ICSC)
2S04 (IBC)
1S91 (IBC)
FM ENABLE SWITCH
CONSOLE
MC FM EN
MC RD(1)
MC ED 1A
MC ED 1B
MC ED 1C

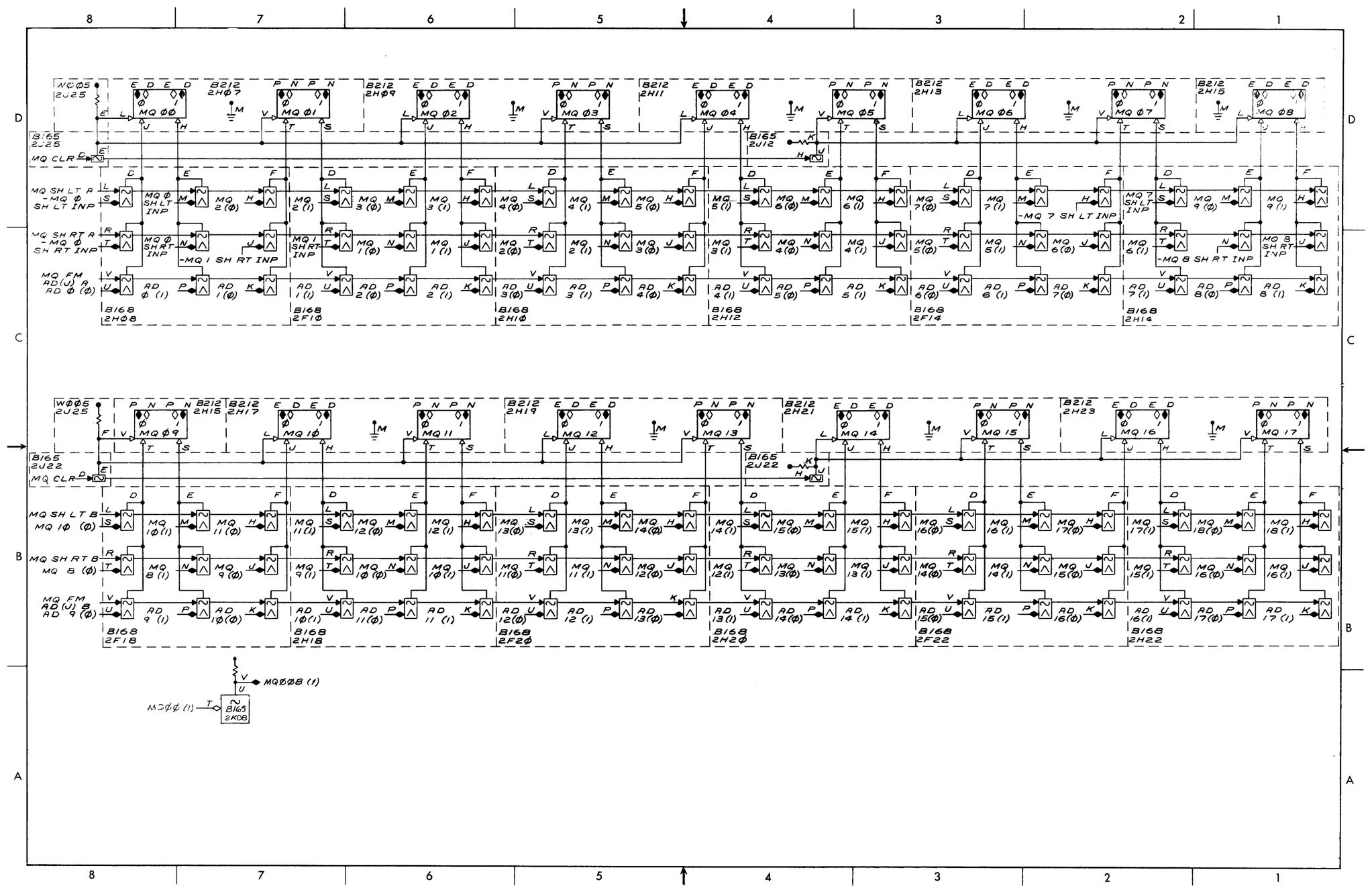


D-BS-KA10-0-MC2 Memory Control

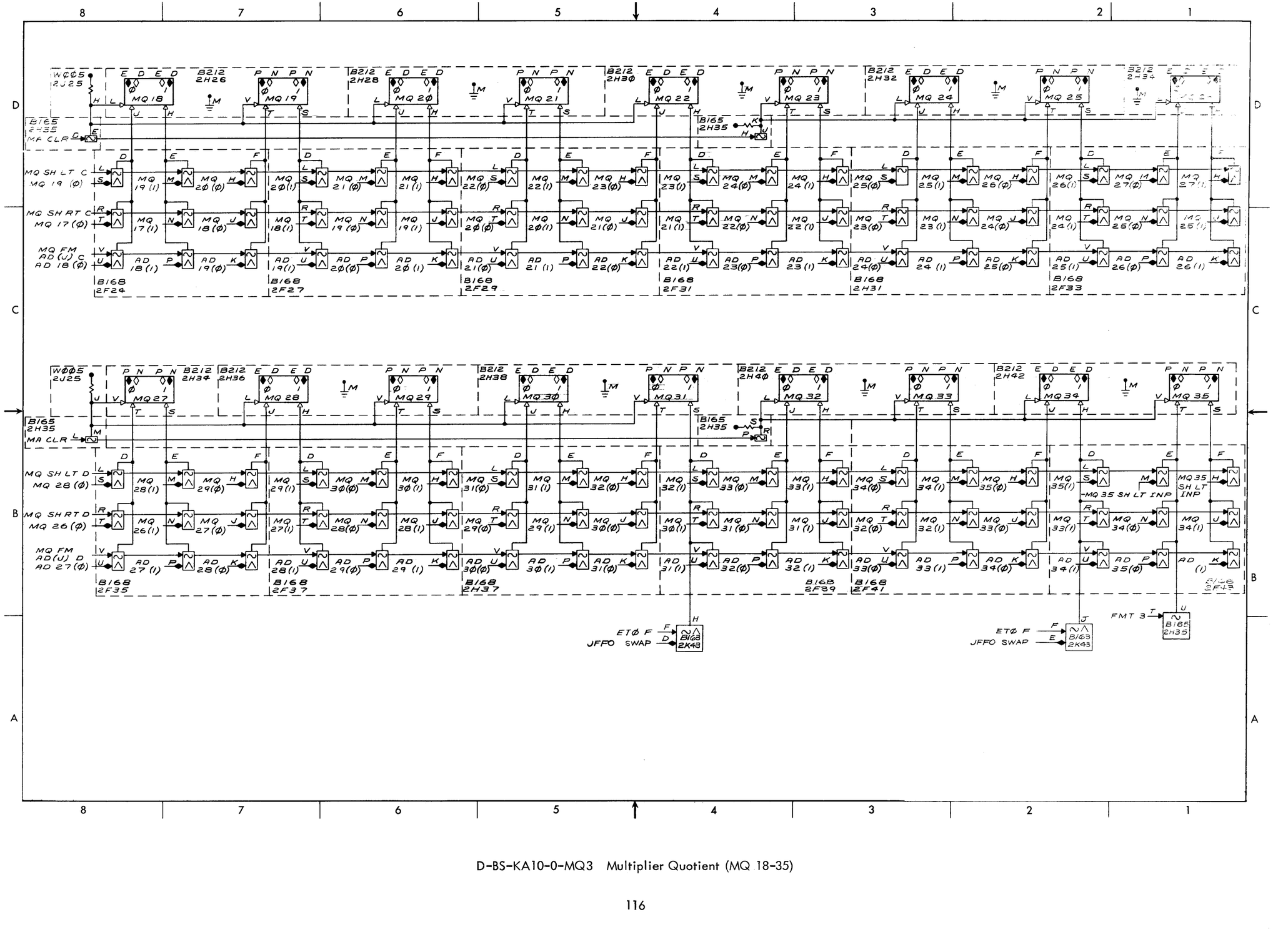

8
7
6
5
4
3
2
1
A
B
C
D
MR PWR CLR
MI LOAD A
MI LOAD B
MI LOAD C
MI LOAD D
MI PROG EN
MI PROG DIS SW
-MI PROG DIS SW
MI PROG DIS
BIO PI SEL
2RØ4 (ICSC)
2RØ4 (IBC)
1R41 (IBC)
MI PROG DIS SW
MI PROG
MR START
KEY F1(1)
IOT DATAO SET
MCRSTØ
AS COND
MC RD B(1)
ARLT FM FM [1]
AS=FMA
MITØ
DLY B311 1R37 65 NS
ST 8
ST 1
-SAC INH
MC RST Ø
MC RD(Ø)
MIT1
MC RST 1
MIT 1
MI PROG (Ø)



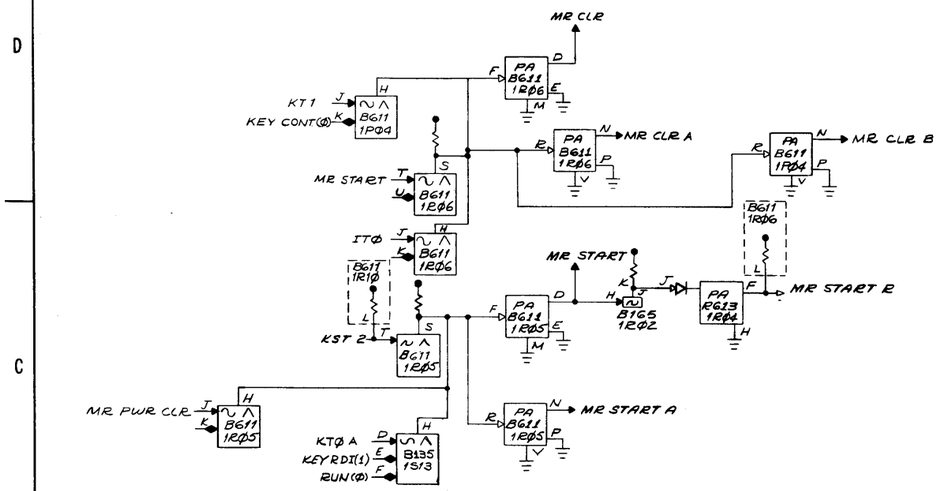
D-BS-KA10-0-MQ1 MQ Control

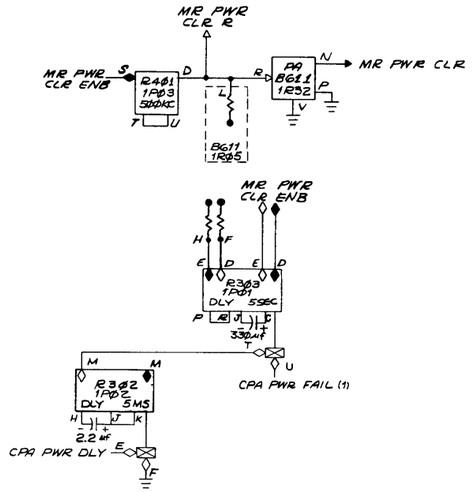


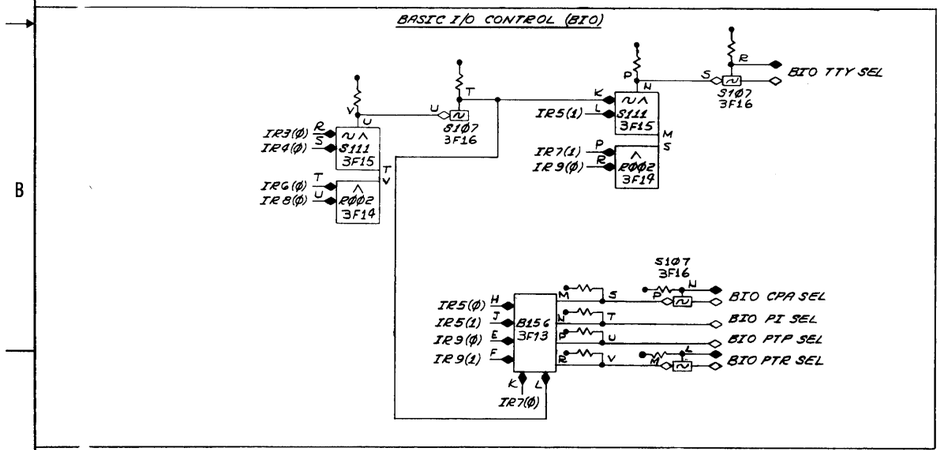
D-BS-KA10-0-MQ2 Multiplier Quotient (MQ 00-17)

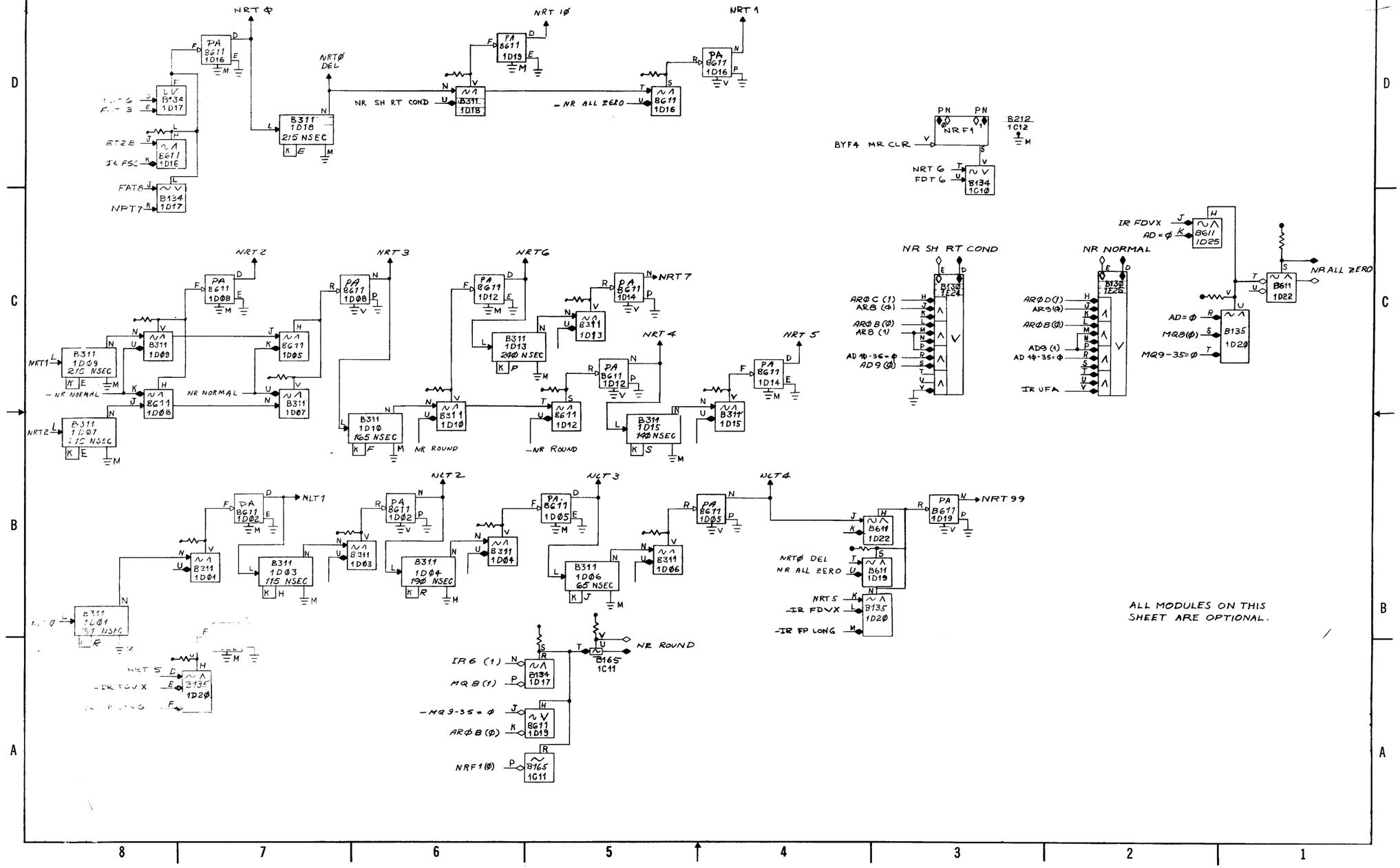


D-BS-KA10-0-MQ3 Multiplier Quotient (MQ 18-35)

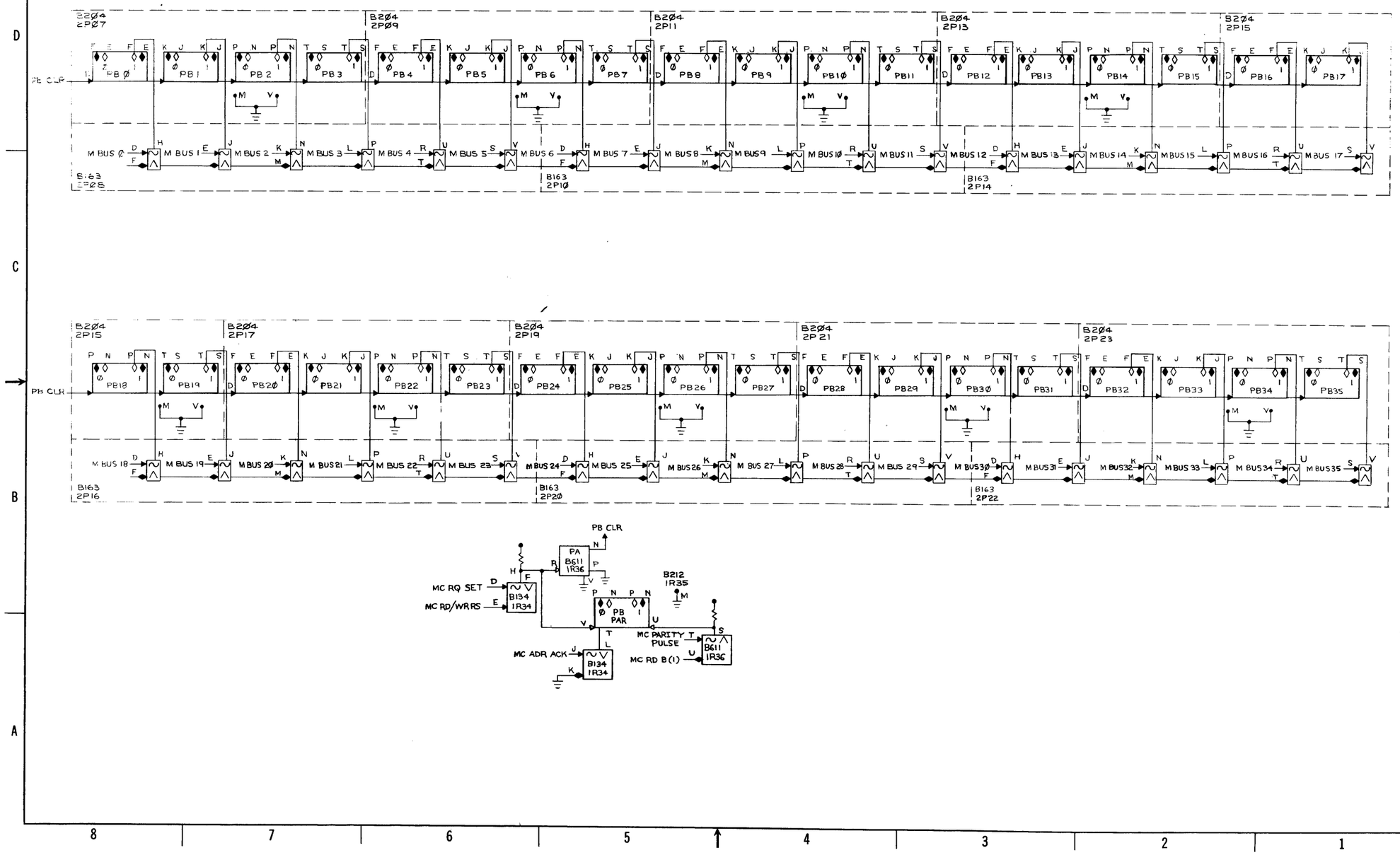

MR CLR
KT 1
KEY CONT(Ø)
BG11 1PØ4
PA BG11 1RØ6
MR CLR A
MR START
BG11 1RØ6
MR CLR B
PA BG11 1RØ4
ITØ
BG11 1RØ6
BG11 1RØ9
BG11 1RØ6
MR START
MR START B
BG11 1RØ5
PA BG11 1RØ5
B165 1RØ2
PA BG13 1RØ4
KST 2
BG11 1RØ5
MR PWR CLR
BG11 1RØ5
MR START A
KTØ A
KEYRDI(1)
RUN(Ø)
B135 1S13


MR PWR CLR R
MR PWR CLR ENB
R4Ø1 1PØ3 500KC
PA BG11 1RØ2
MR PWR CLR
BG11 1RØ5
MR PWR CLR ENB
R3Ø3 1PØ1 DLY 55SEC
330µF
CPA PWR FAIL (1)
R3Ø2 1PØ2 DLY 5MS
2.2 mF
CPA PWR DLY

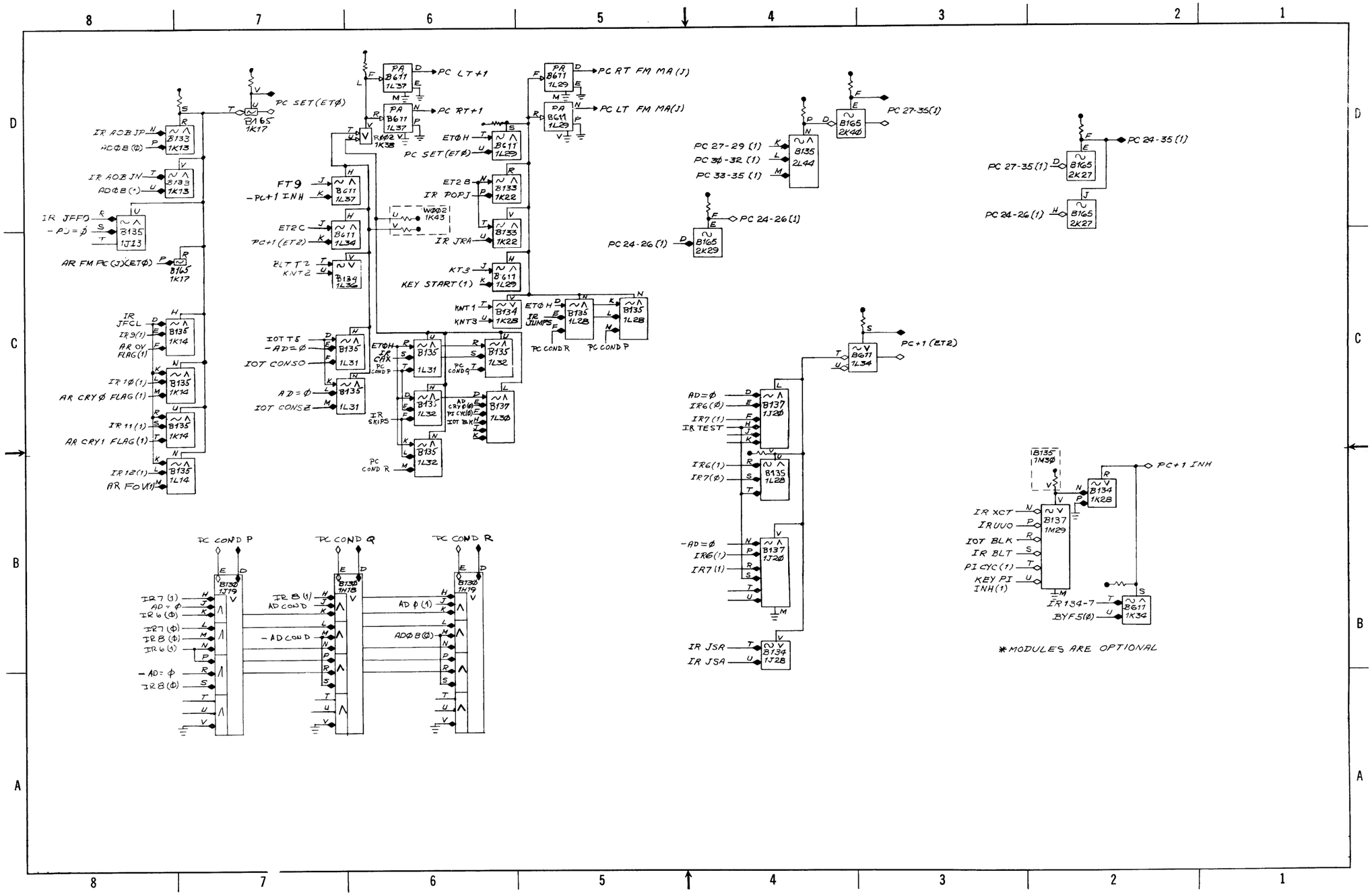

BASIC I/O CONTROL (BIO)
IR3(Ø)
IR4(Ø)
S111 3F15
S1Ø7 3F16
IR6(Ø)
IR8(Ø)
PØØ2 3F14
IR5(1)
IR7(1)
IR9(Ø)
PØØ2 3F19
BIO TTY SEL
IR5(Ø)
IR5(1)
IR9(Ø)
IR9(1)
IR7(Ø)
B156 3F13
BIO CPA SEL
BIO PI SEL
BIO PTP SEL
BIO PTR SEL



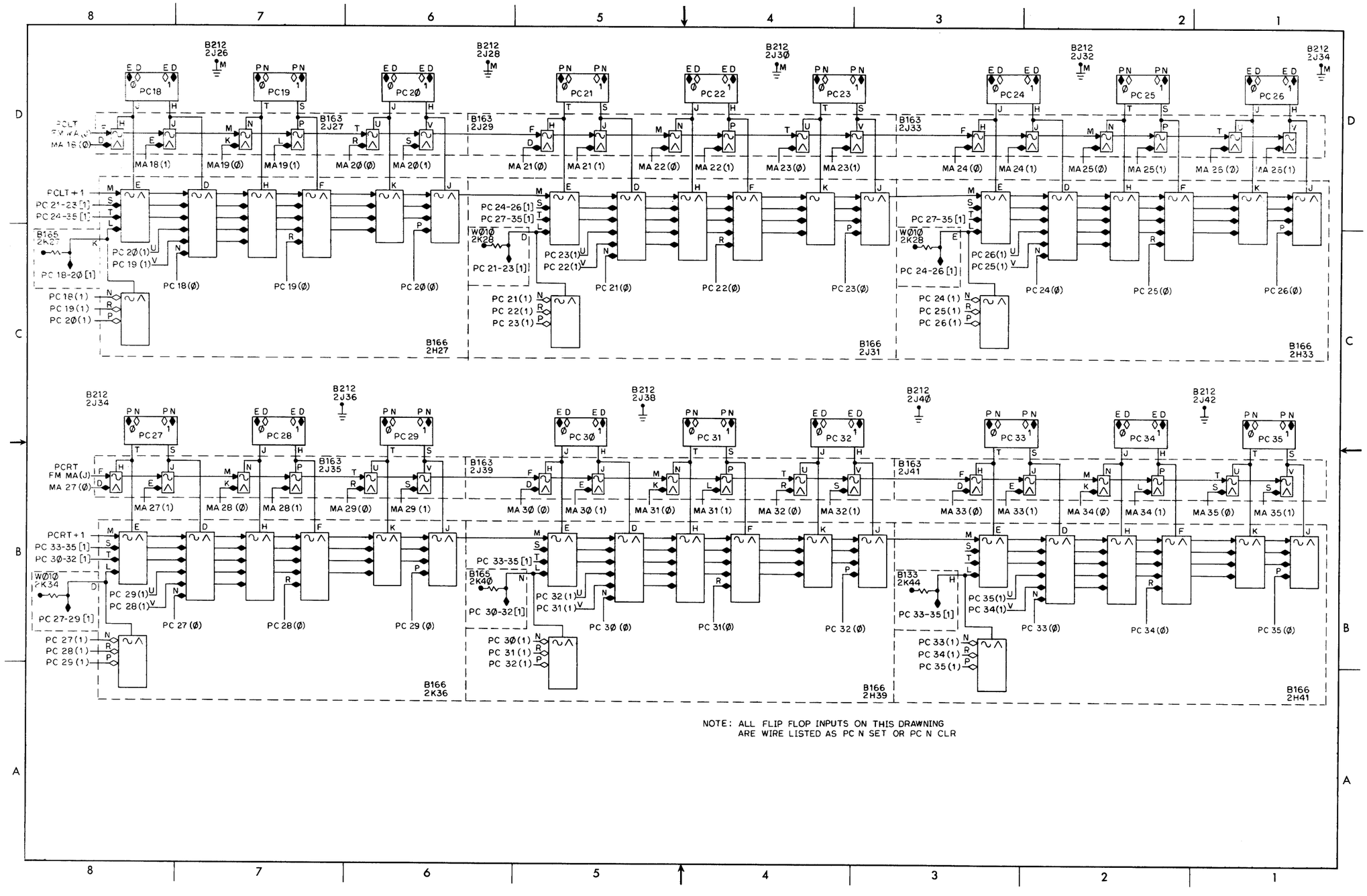
D-BS-KA10-0-NRNL Normalize Return and NR Long



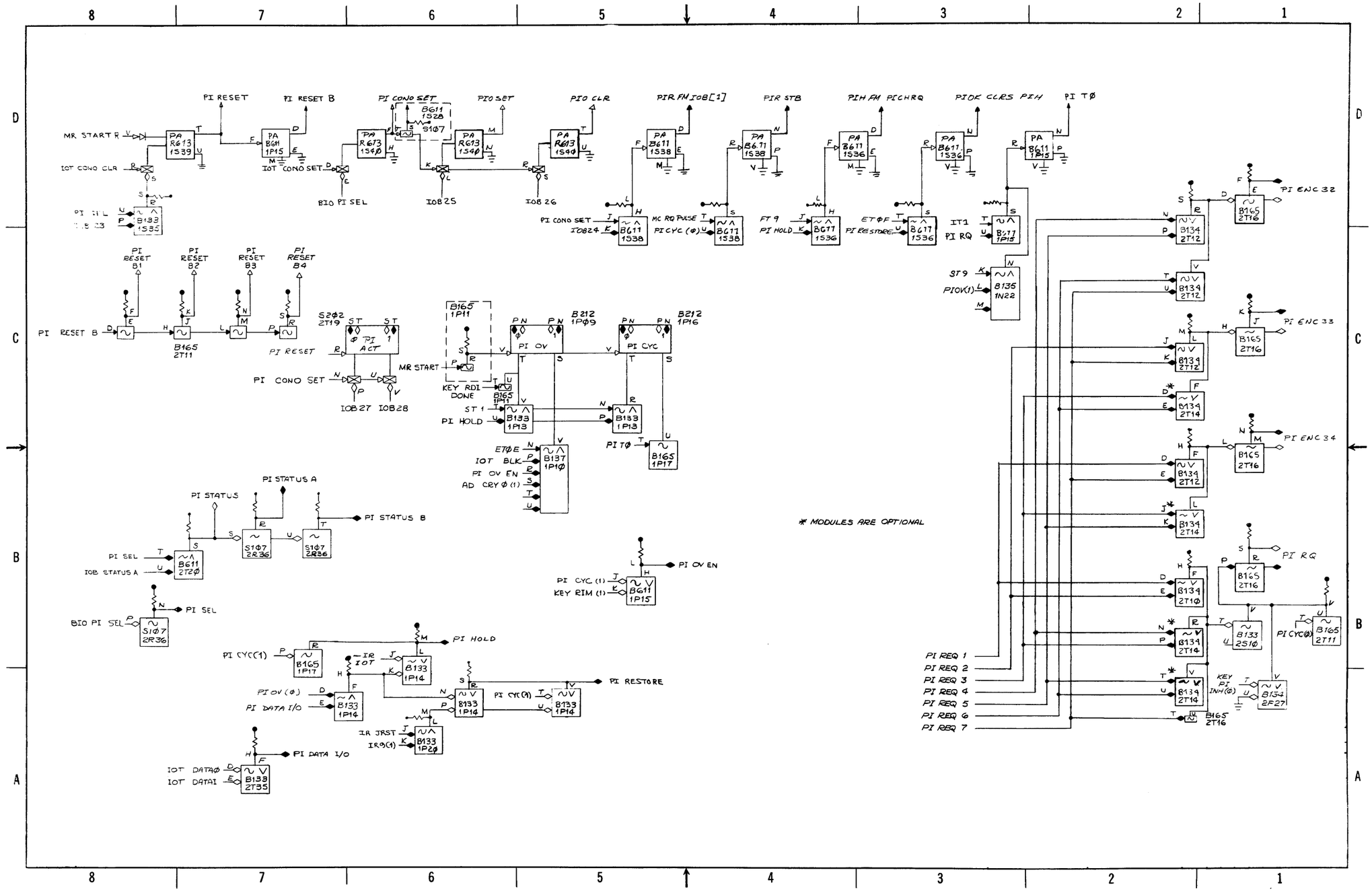
D-BS-KA10-0-PB Parity Buffer Register



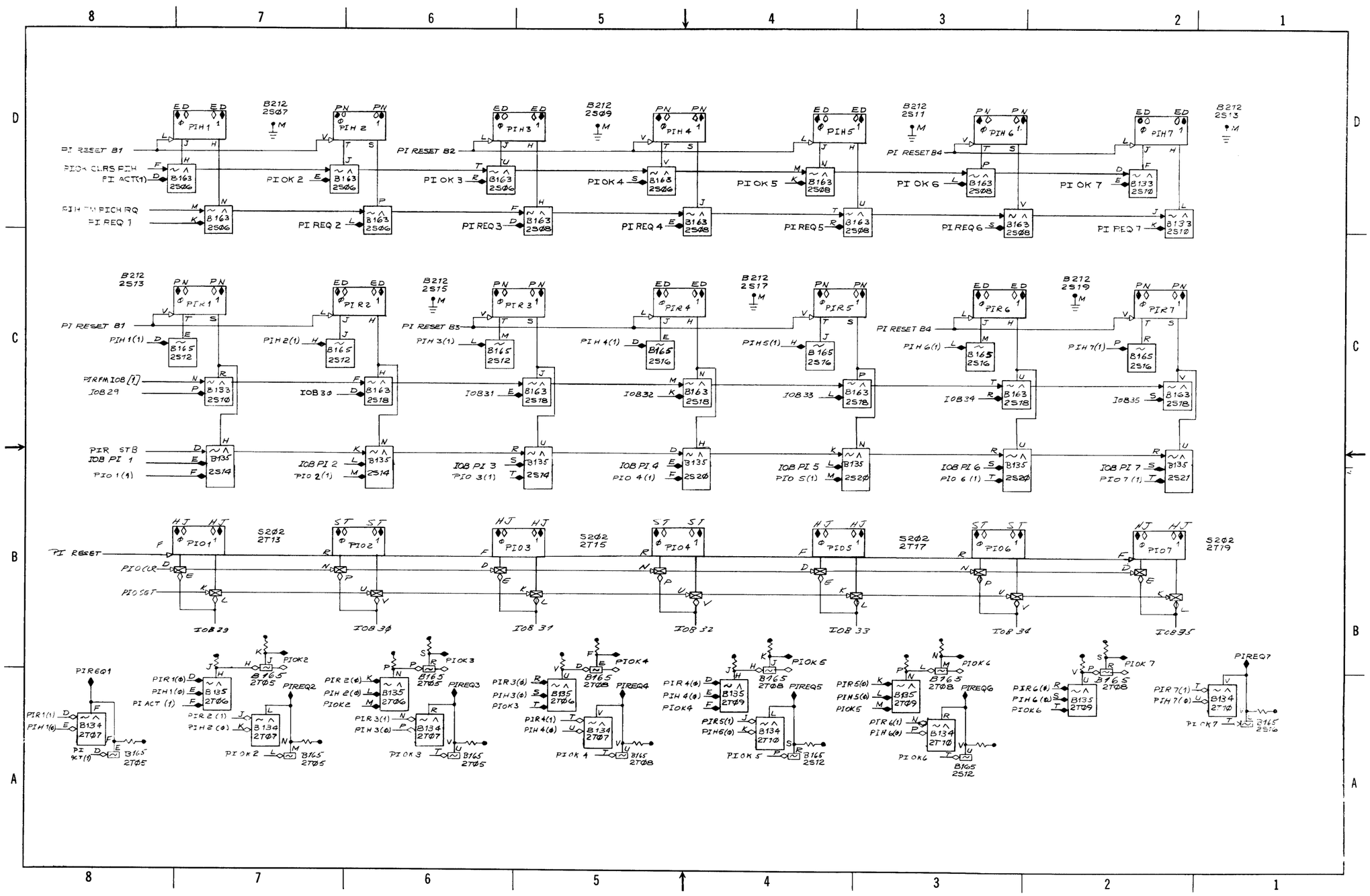
D-BS-KA10-0-PC1 Program Counter Control



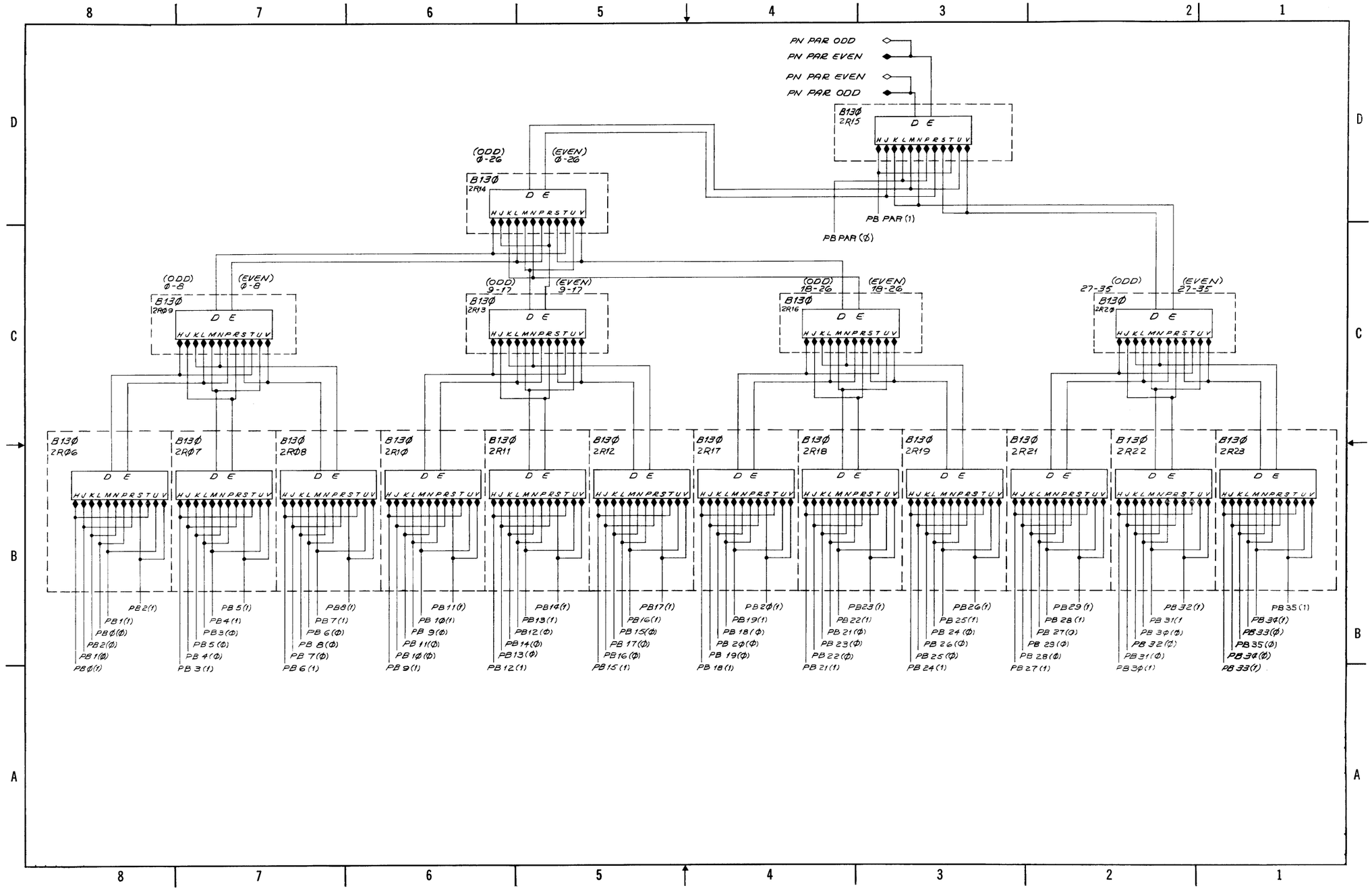
D-BS-KA10-0-PC2 Program Counter Register



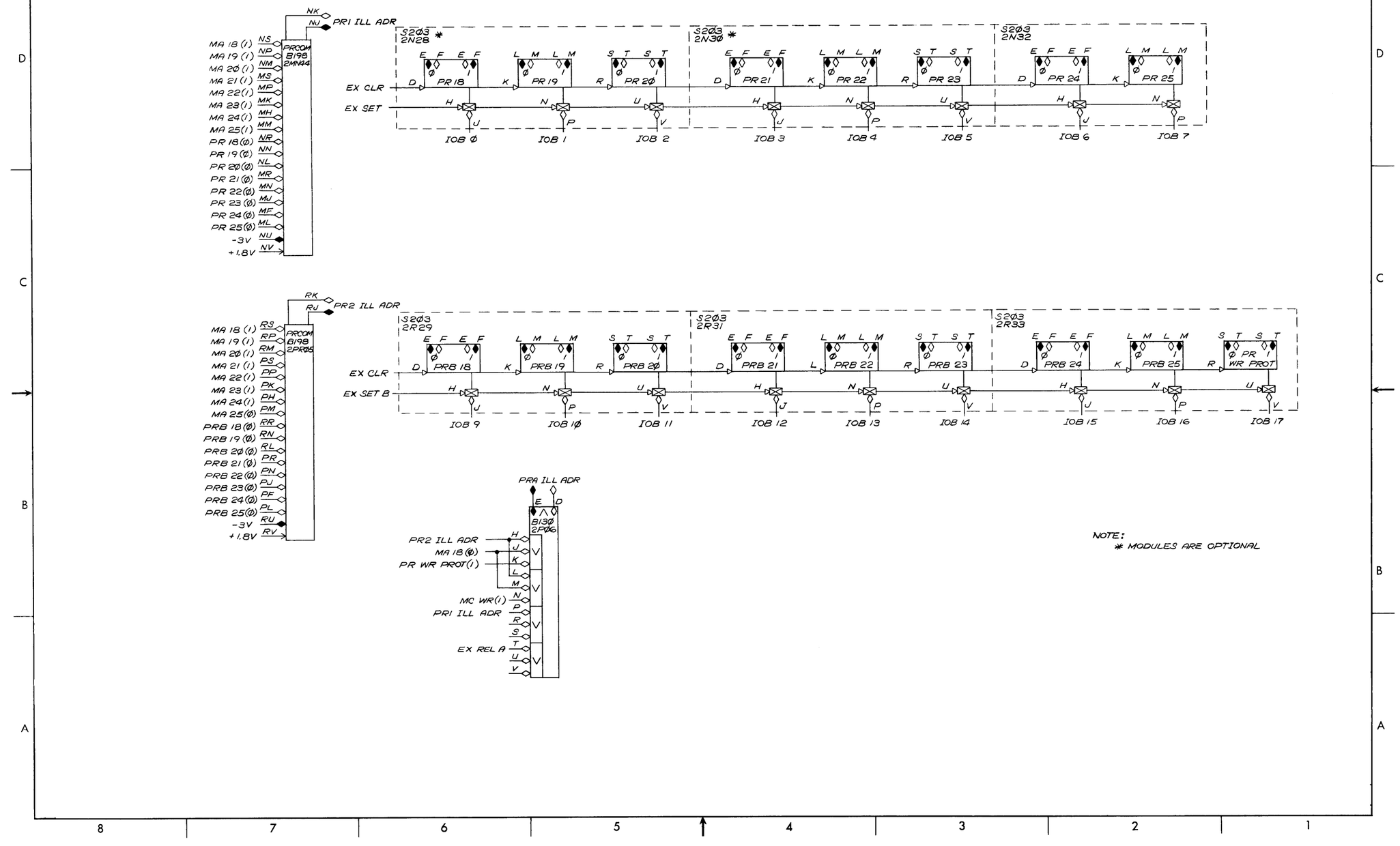
D-BS-KA10-0-PI1 PI Control

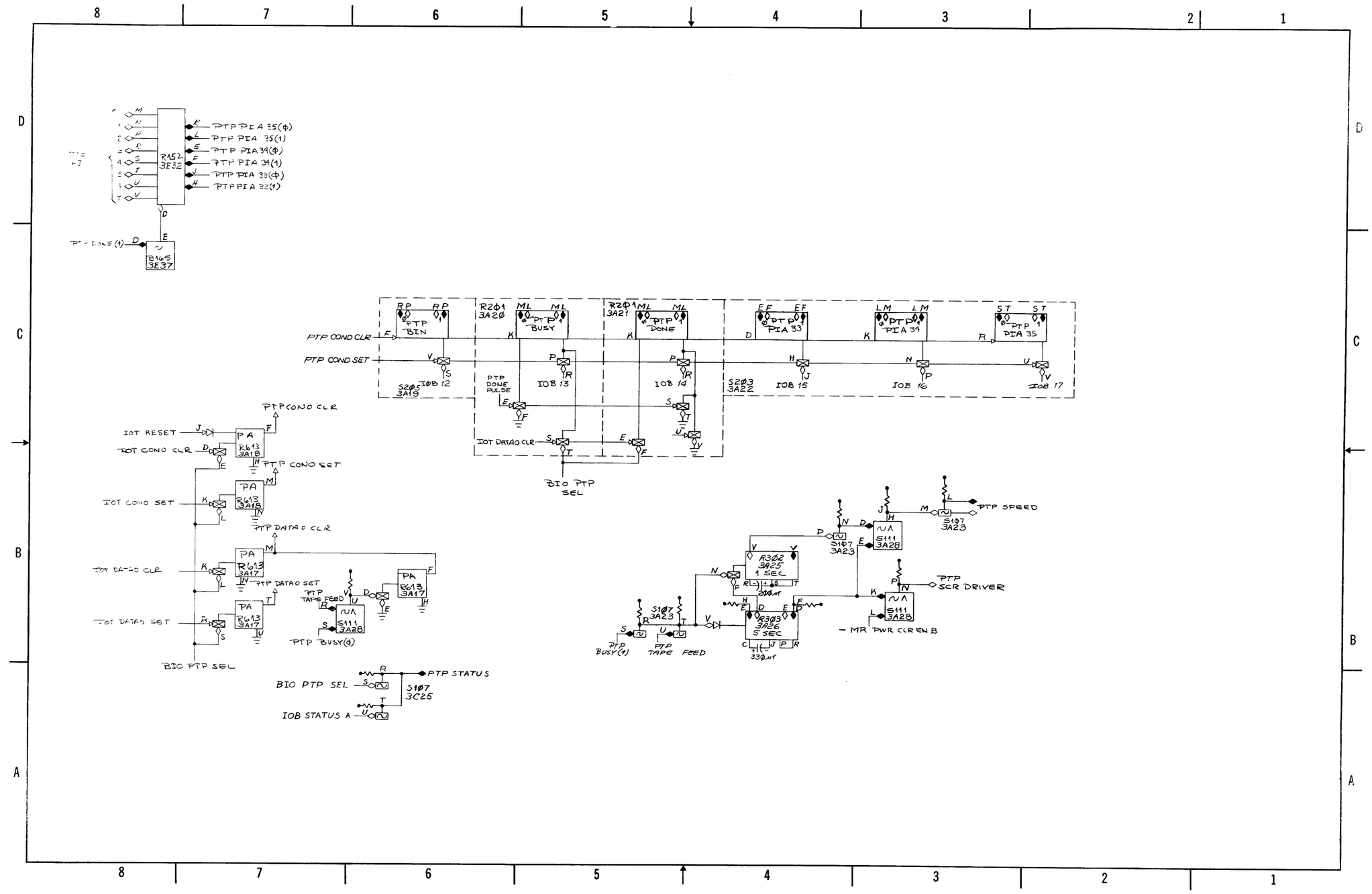


D-BS-KA10-0-P12 Priority Interrupt PIH, PIR, PIO

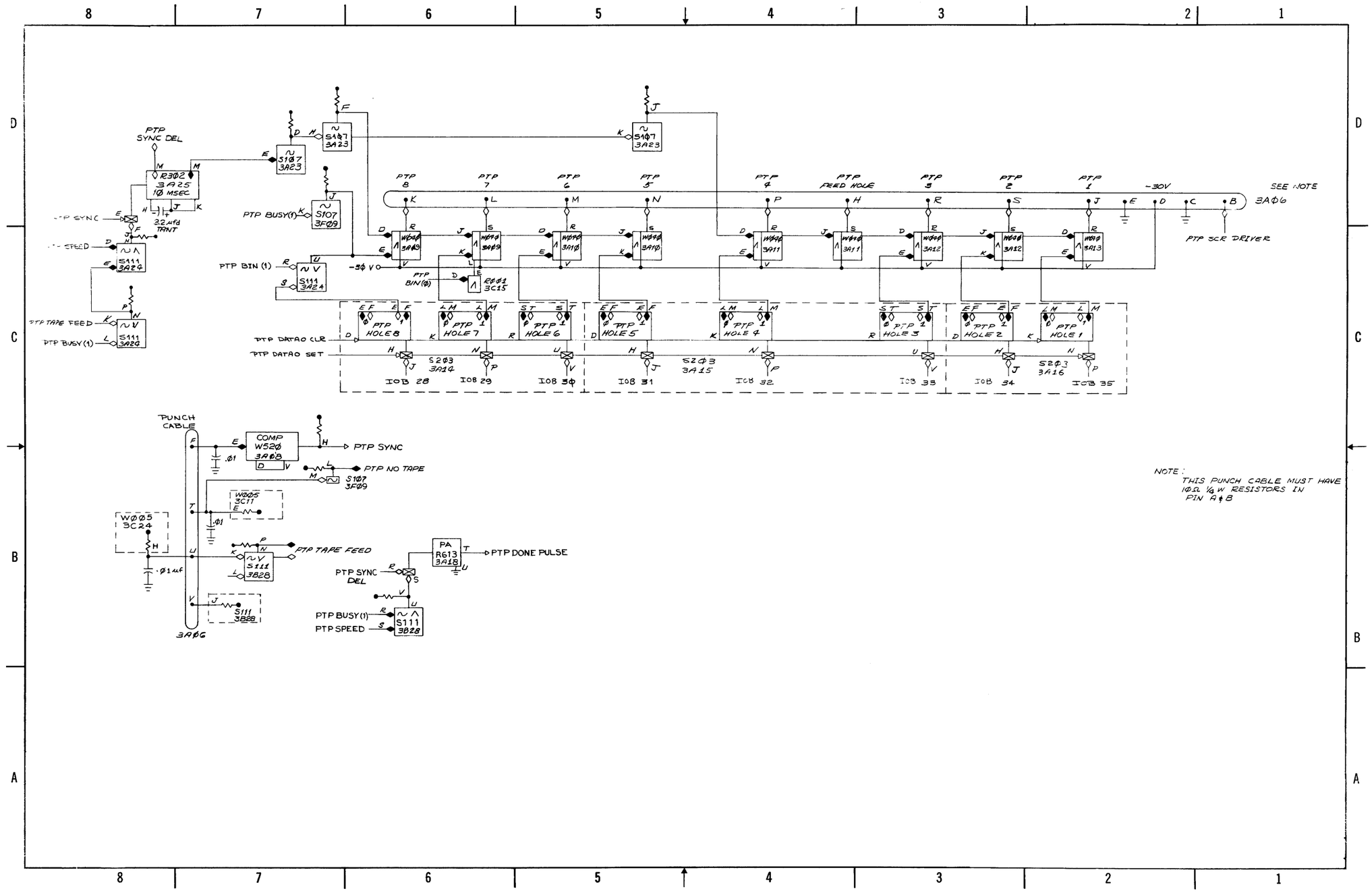


D-BS-KA10-0-PN Parity Network

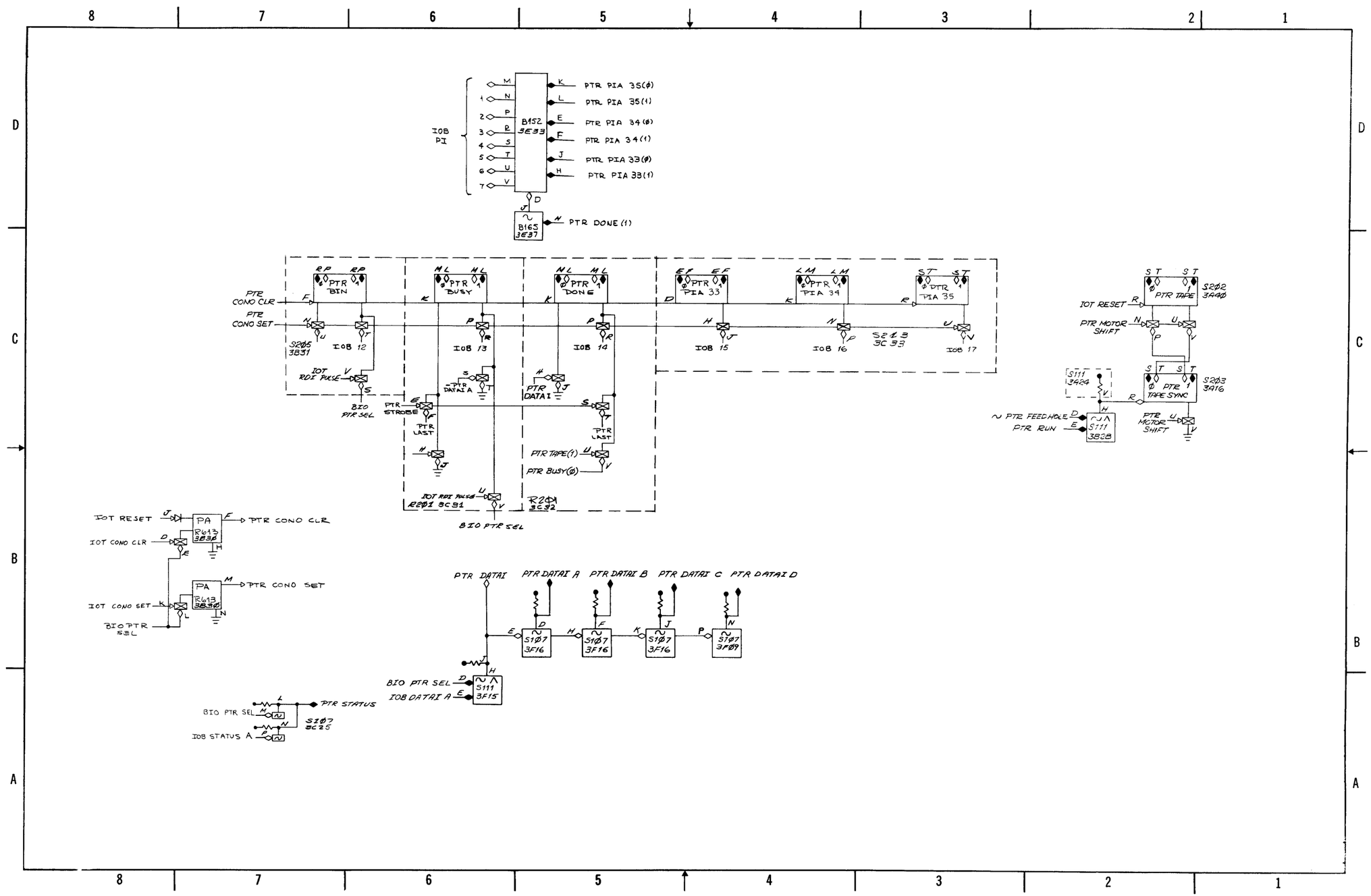

NK
NU
PR1 ILL ADR
MA 18 (1)
MA 19 (1)
MA 20 (1)
MA 21 (1)
MA 22 (1)
MA 23 (1)
MA 24 (1)
MA 25 (1)
PR 18 (Ø)
PR 19 (Ø)
PR 20 (Ø)
PR 21 (Ø)
PR 22 (Ø)
PR 23 (Ø)
PR 24 (Ø)
PR 25 (Ø)
-3V
+1.8V
PRCOM B198 2MN44
S2Ø3 2N28 *
S2Ø3 2N3Ø *
S2Ø3 2N32
EX CLR
EX SET
PR 18
PR 19
PR 20
PR 21
PR 22
PR 23
PR 24
PR 25
IOB Ø
IOB 1
IOB 2
IOB 3
IOB 4
IOB 5
IOB 6
IOB 7
RK
RJ
PR2 ILL ADR
PRCOM B198 2PR05
S2Ø3 2R29
S2Ø3 2R31
S2Ø3 2R33
EX SET B
PRB 18
PRB 19
PRB 20
PRB 21
PRB 22
PRB 23
PRB 24
PRB 25
PR WR PROT
IOB 9
IOB 1Ø
IOB 11
IOB 12
IOB 13
IOB 14
IOB 15
IOB 16
IOB 17
PRA ILL ADR
B13Ø 2PØ6
PR2 ILL ADR
MA 18 (Ø)
PR WR PROT (1)
MC WR (1)
PR1 ILL ADR
EX REL A
NOTE:
* MODULES ARE OPTIONAL



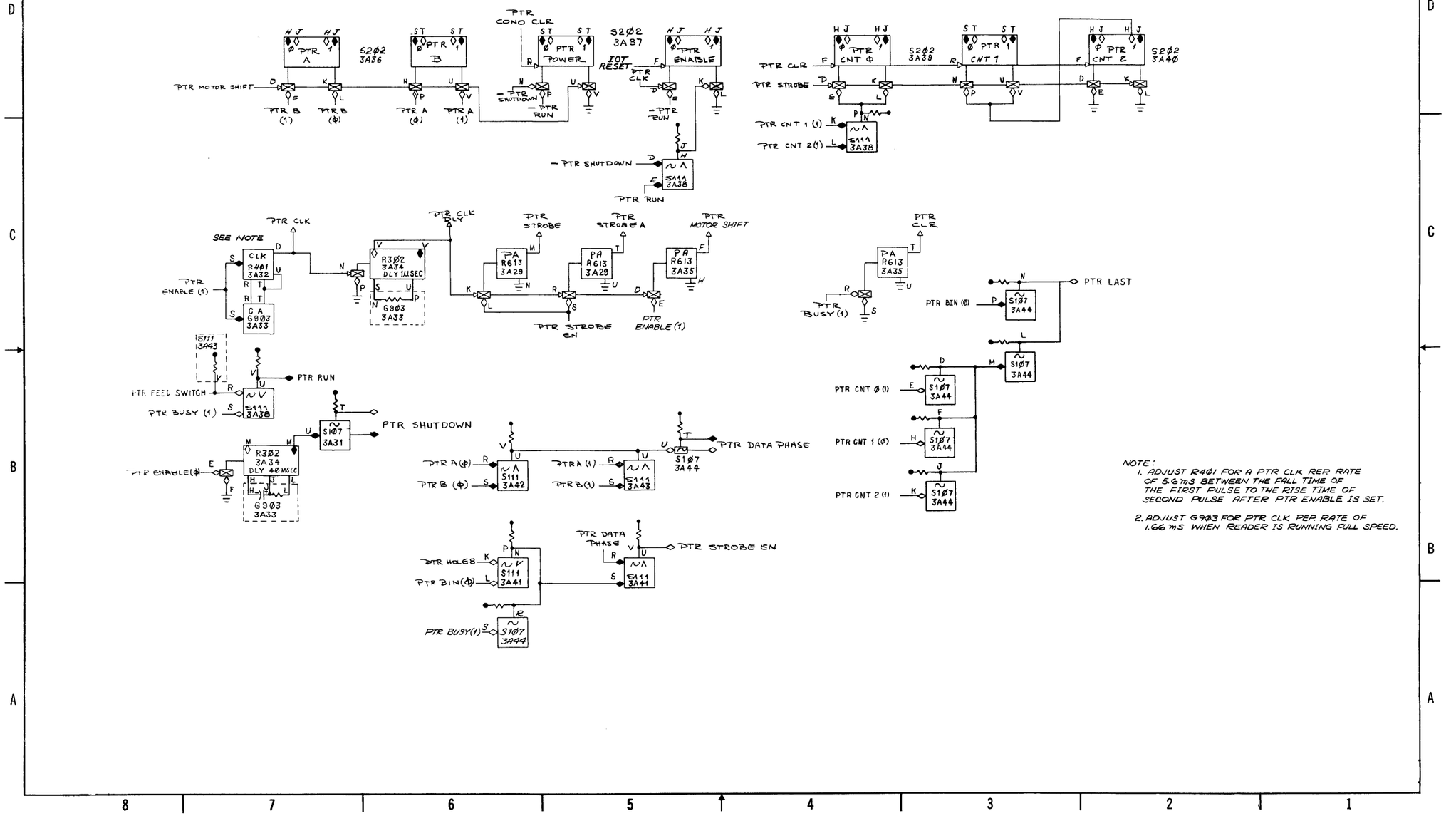
D-BS-KA10-0-PTP1 Paper Tape Punch Control 1



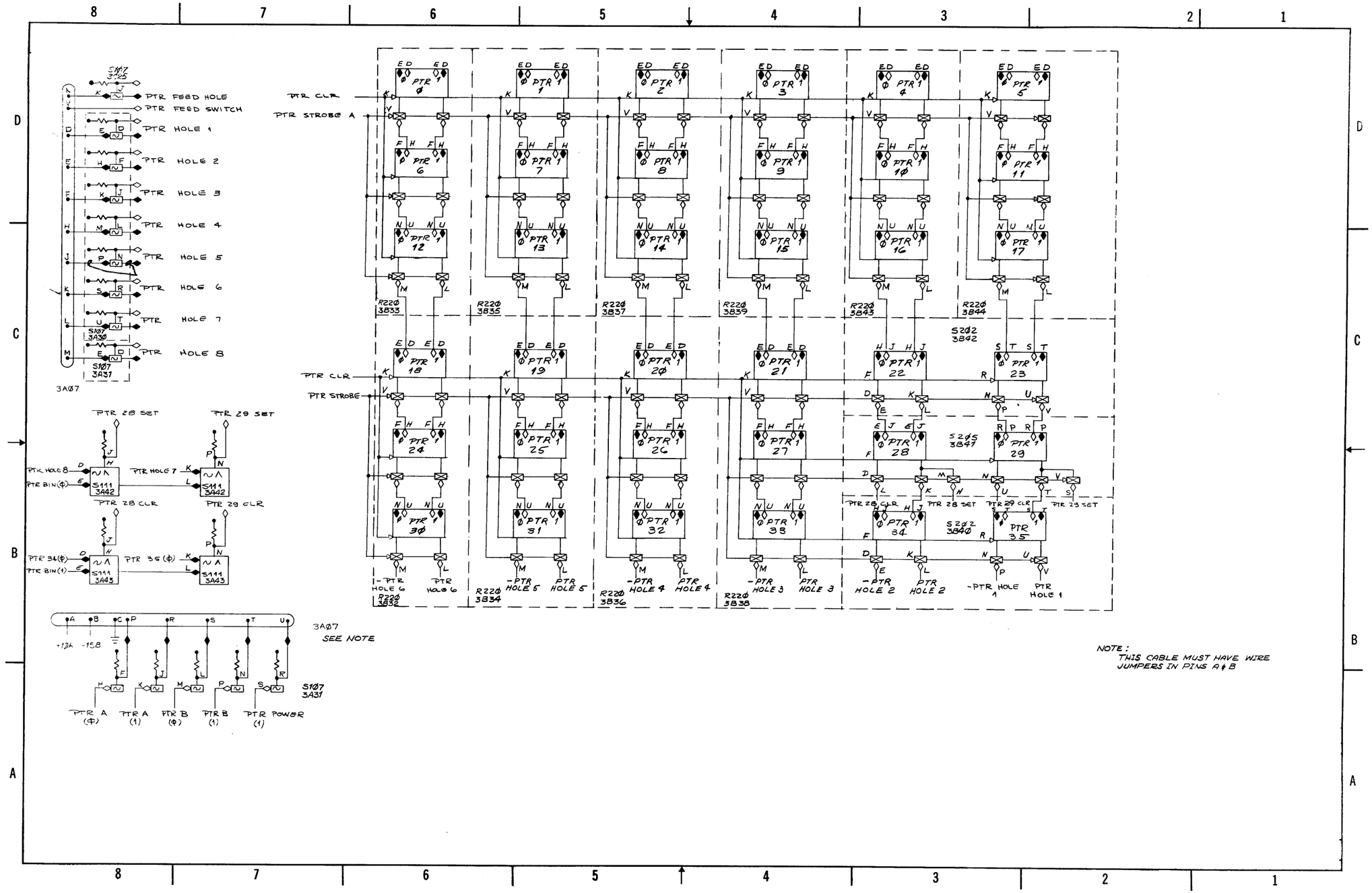
D-BS-KA10-0-PTP2 Paper Tape Punch Control 2



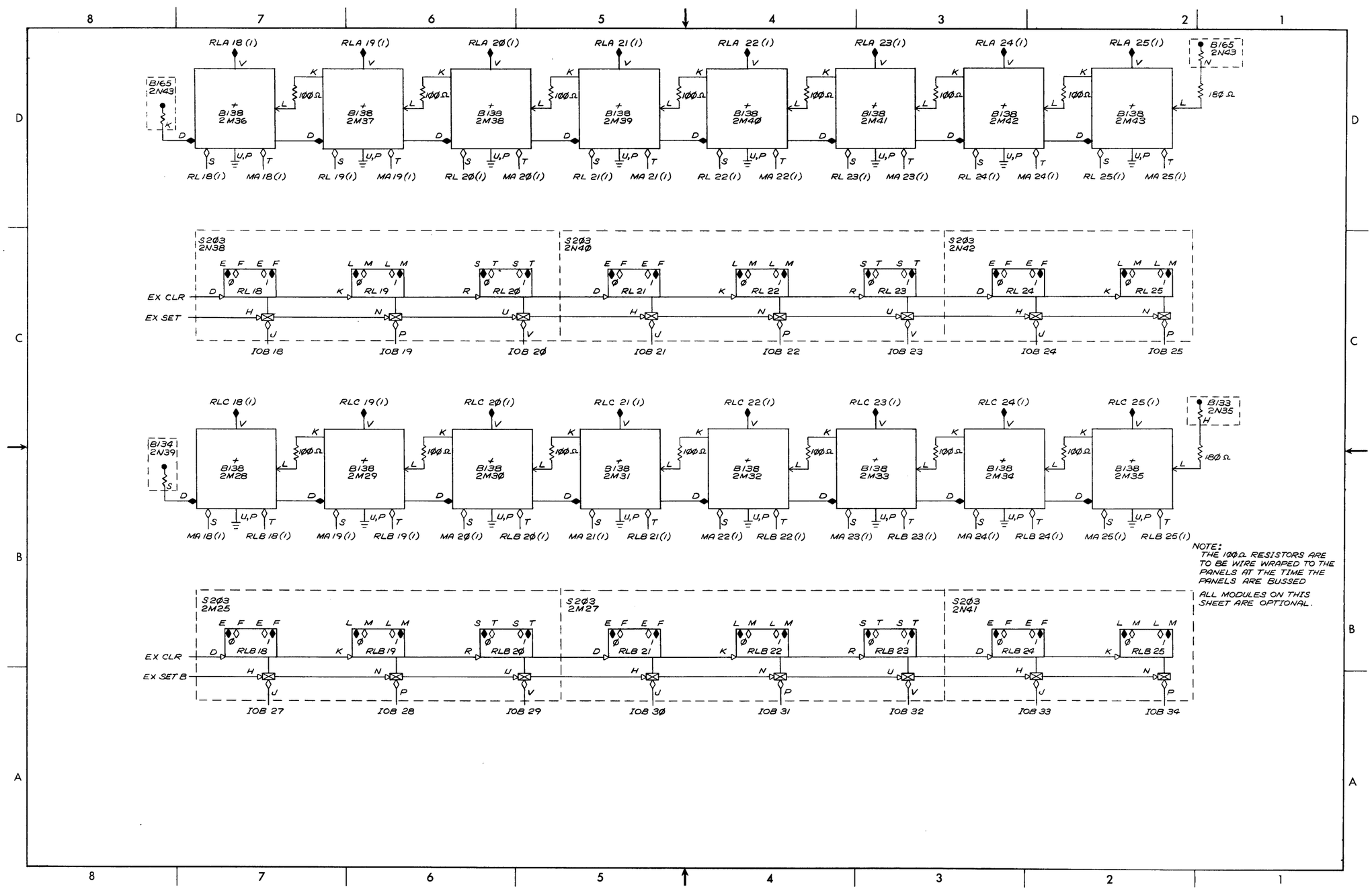
D-BS-KA10-0-PTR1 Paper Tape Reader Control



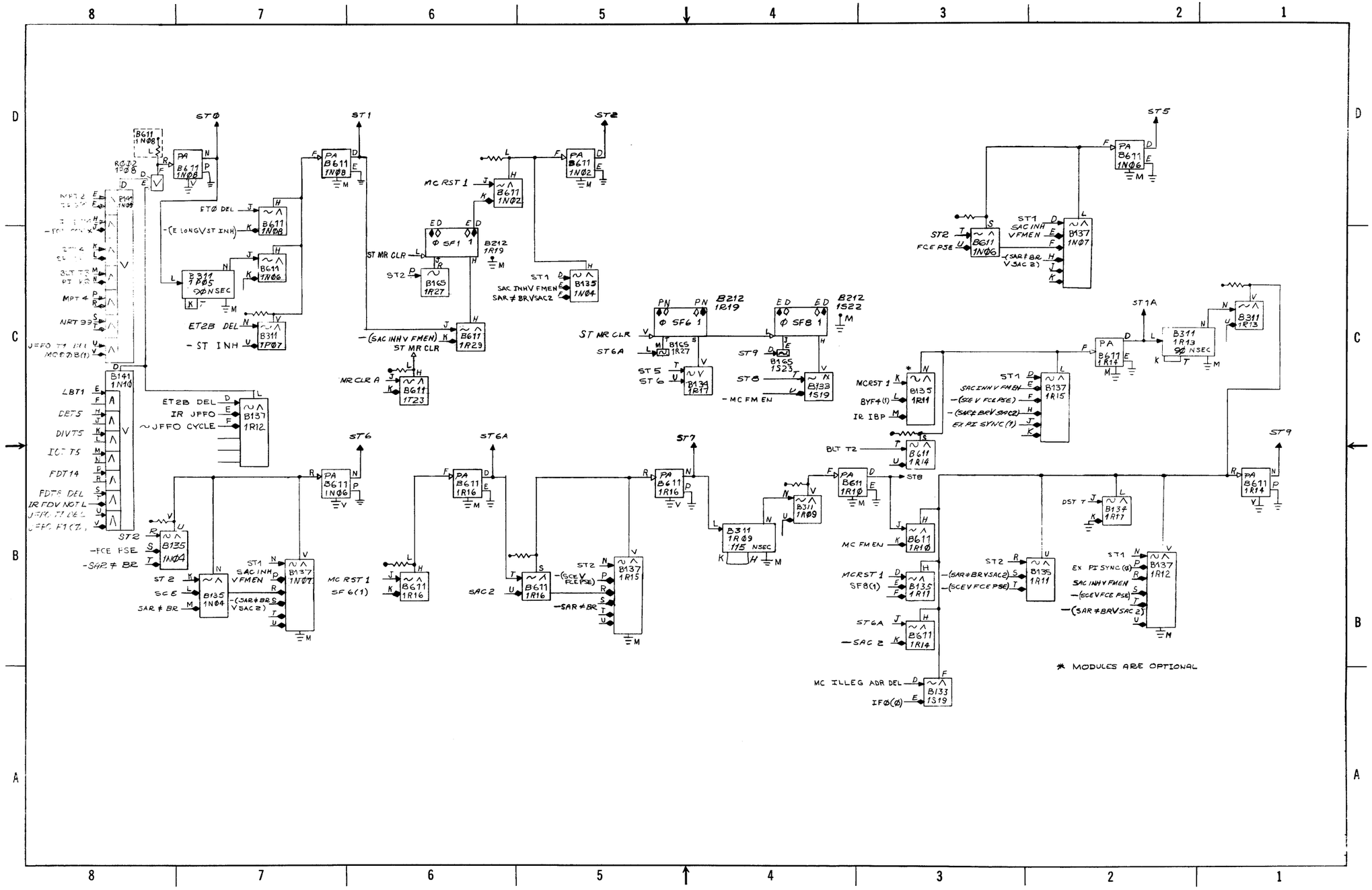
D-BS-KA10-0-PTR2 Paper Tape Reader Control



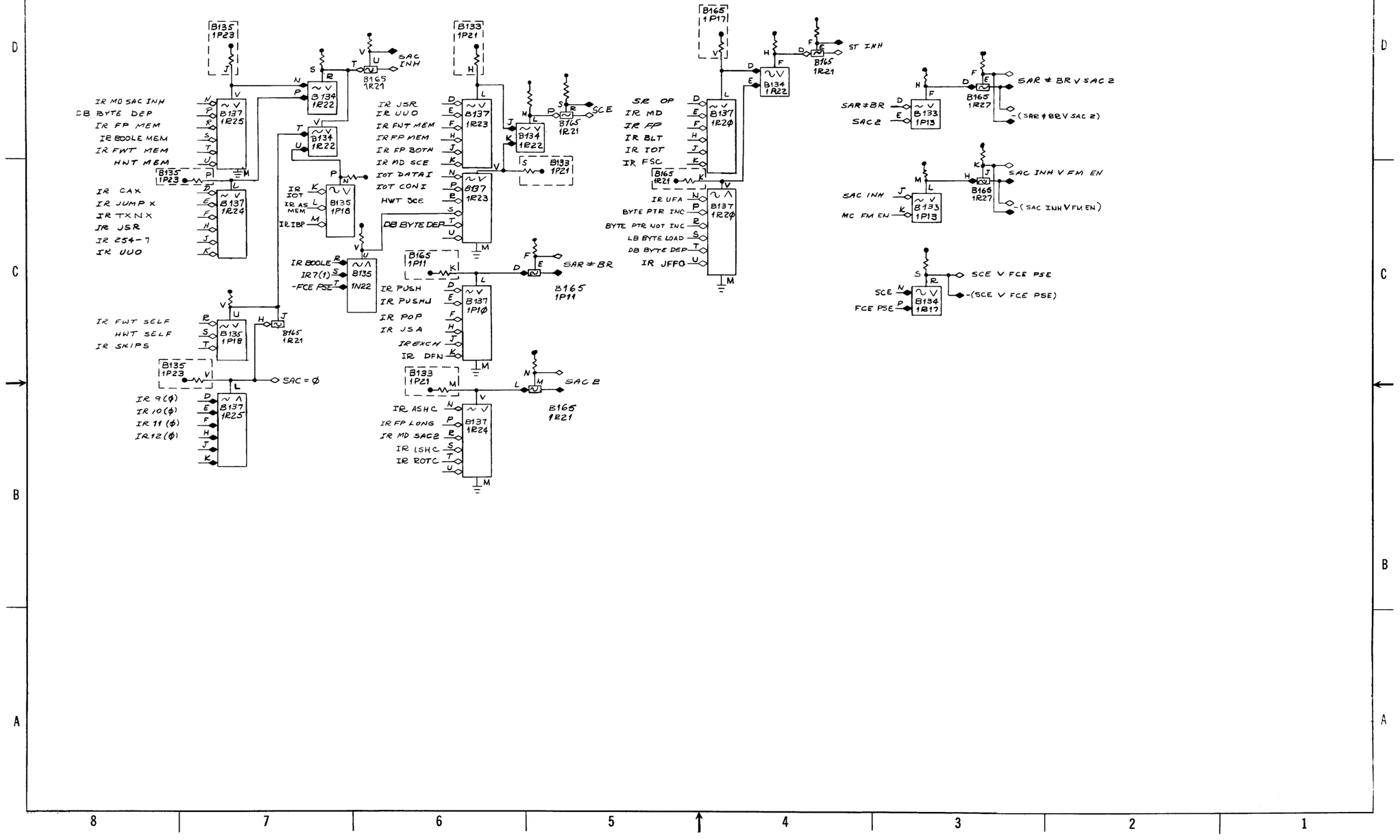
D-BS-KA10-0-PTR3 Paper Tape Reader Control



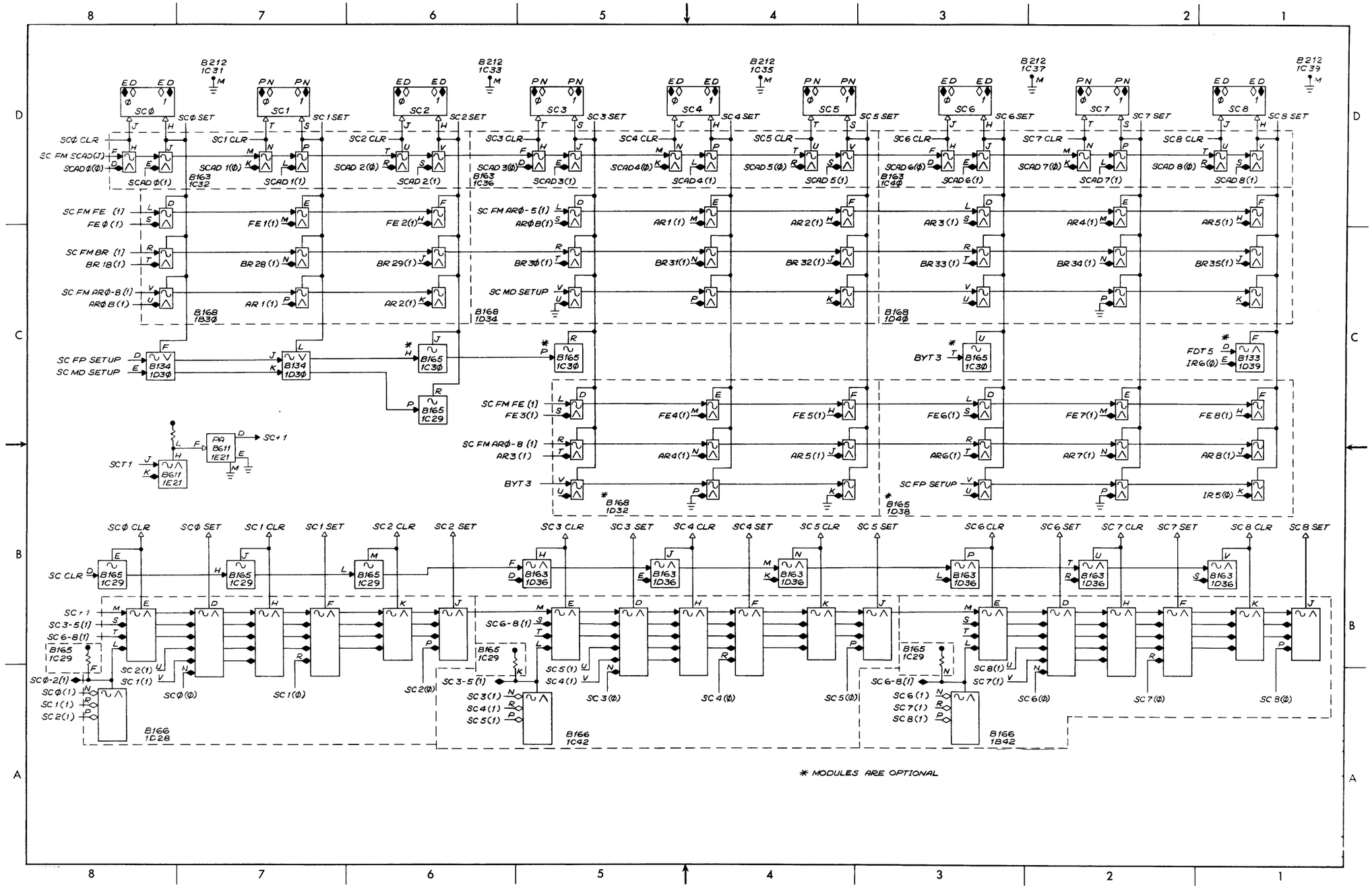
D-BS-KA10-0-RL Relocate Register



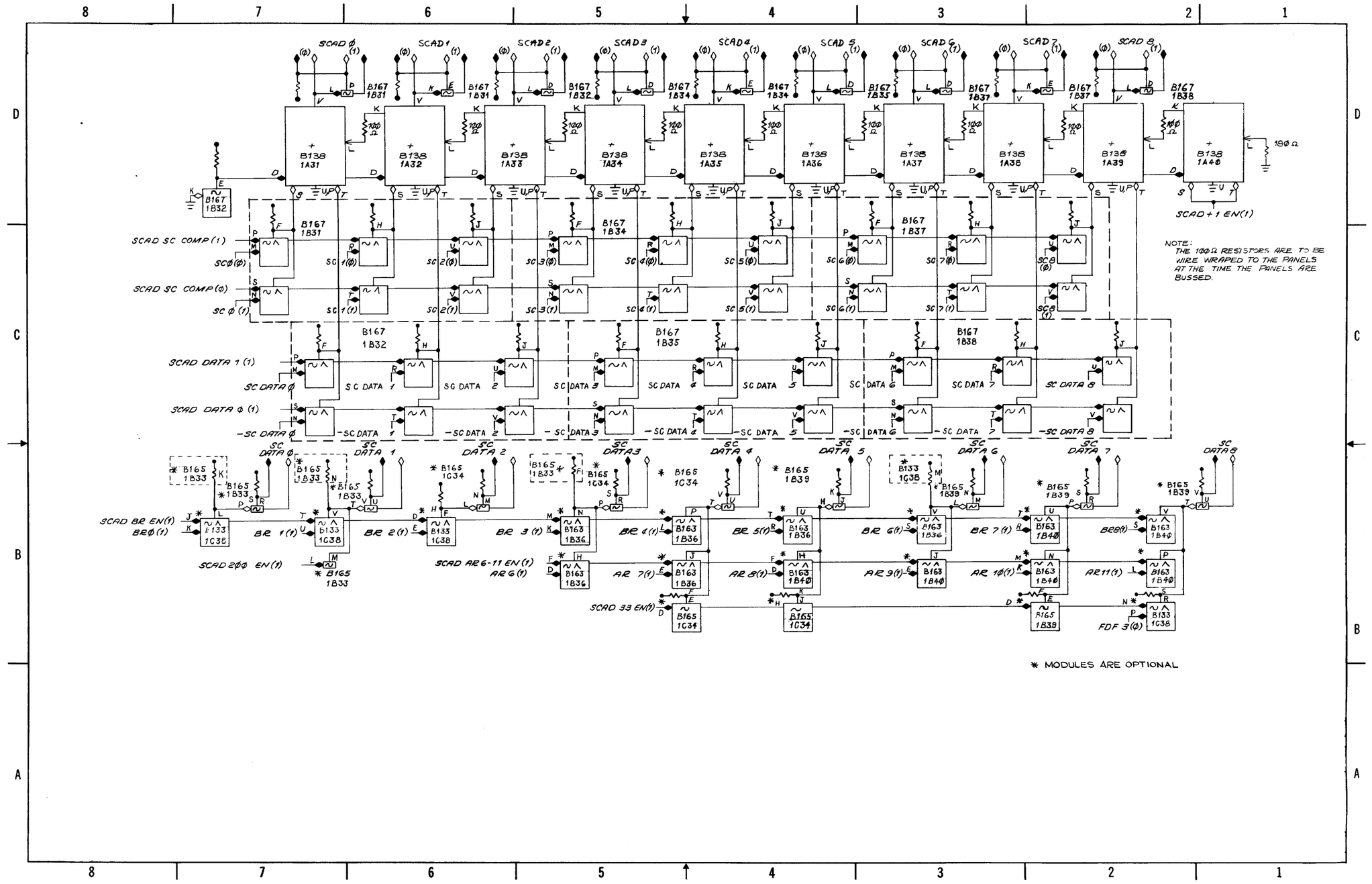
D-BS-KA10-0-S1 Store Cycle Time Pulses



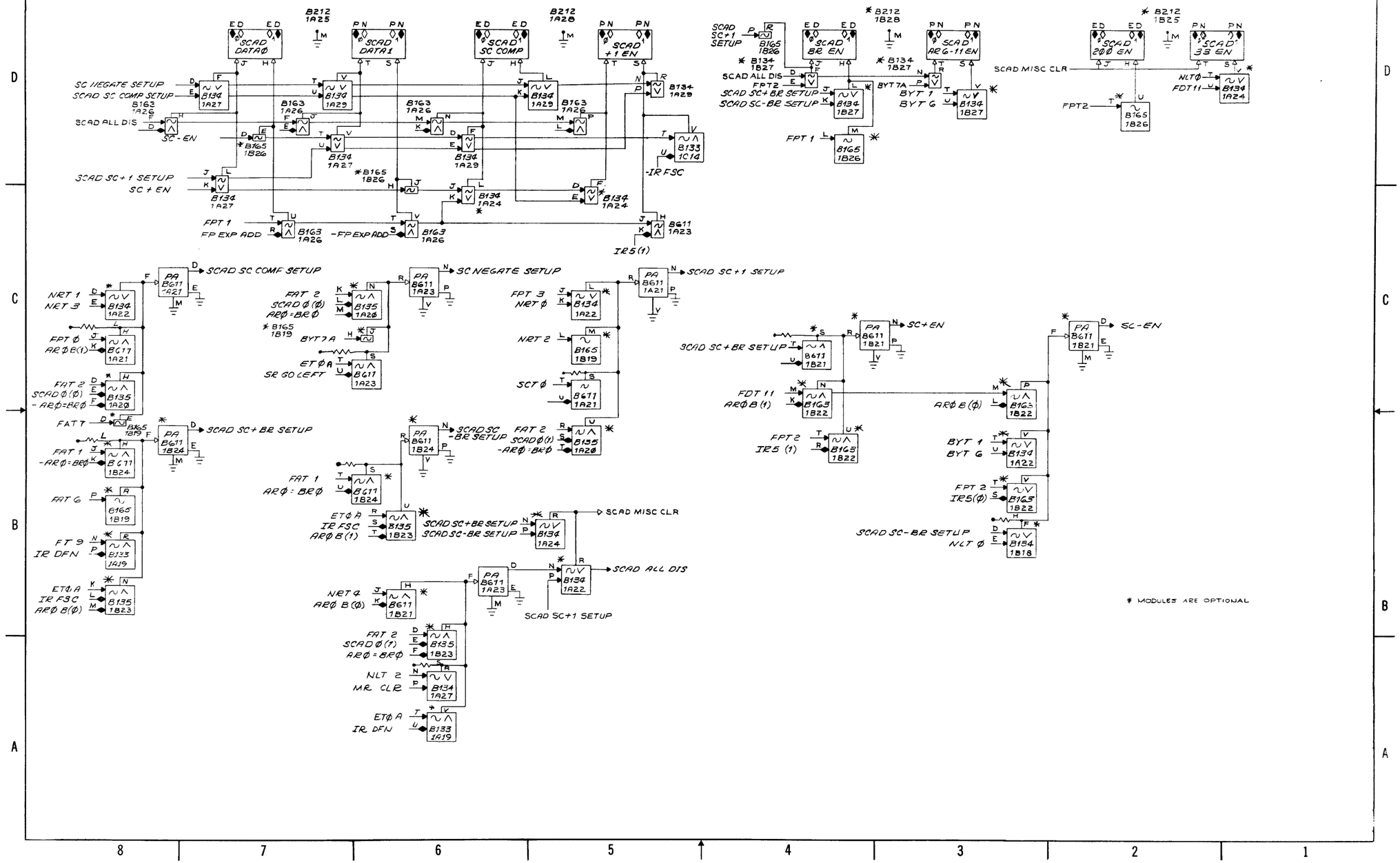
D-BS-KA10-0-S2 Store Cycle Levels



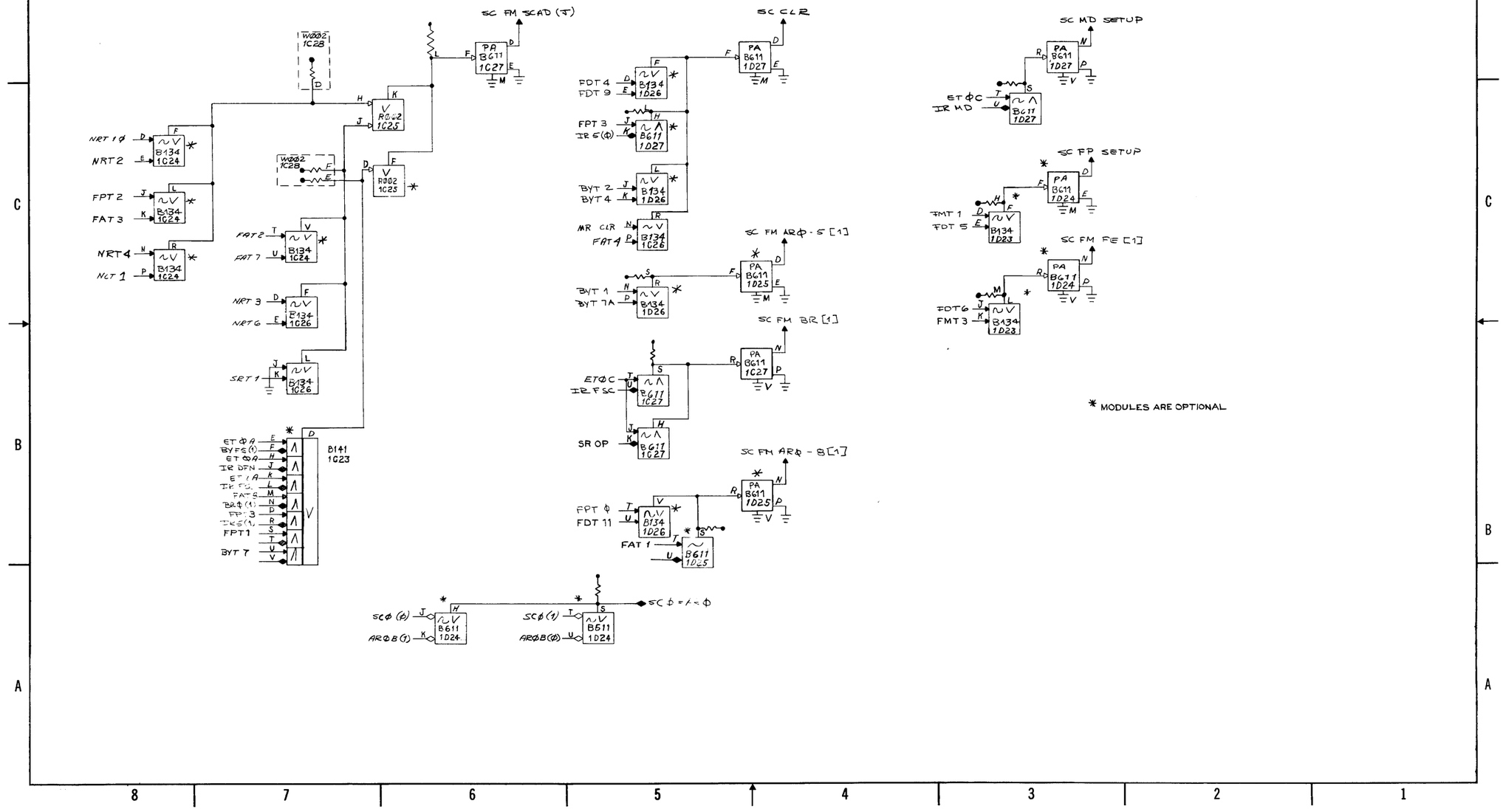
D-BS-KA10-0-SC Shift Count Register



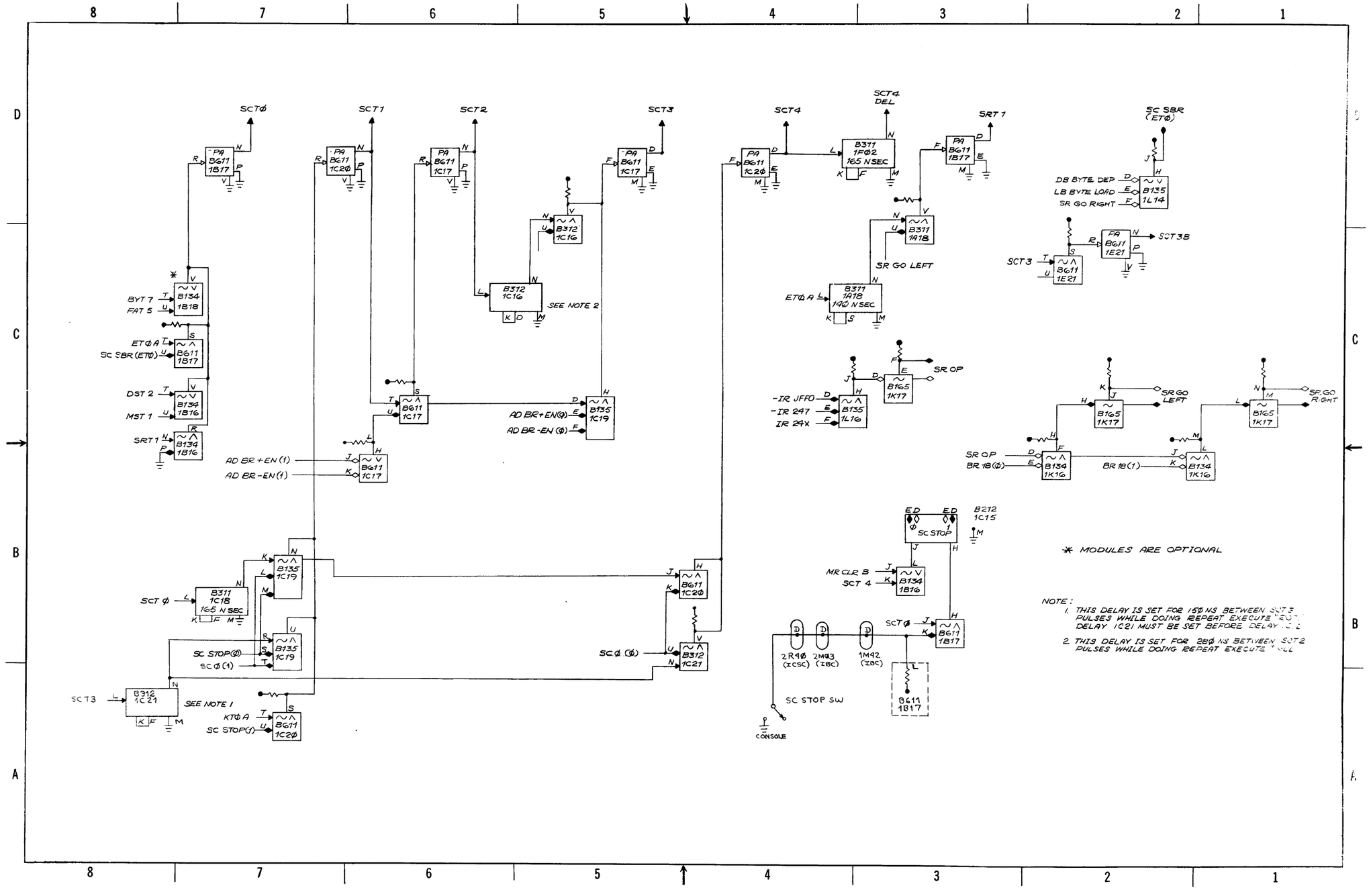
D-BS-KA10-0-SCAD Shift Count Adder



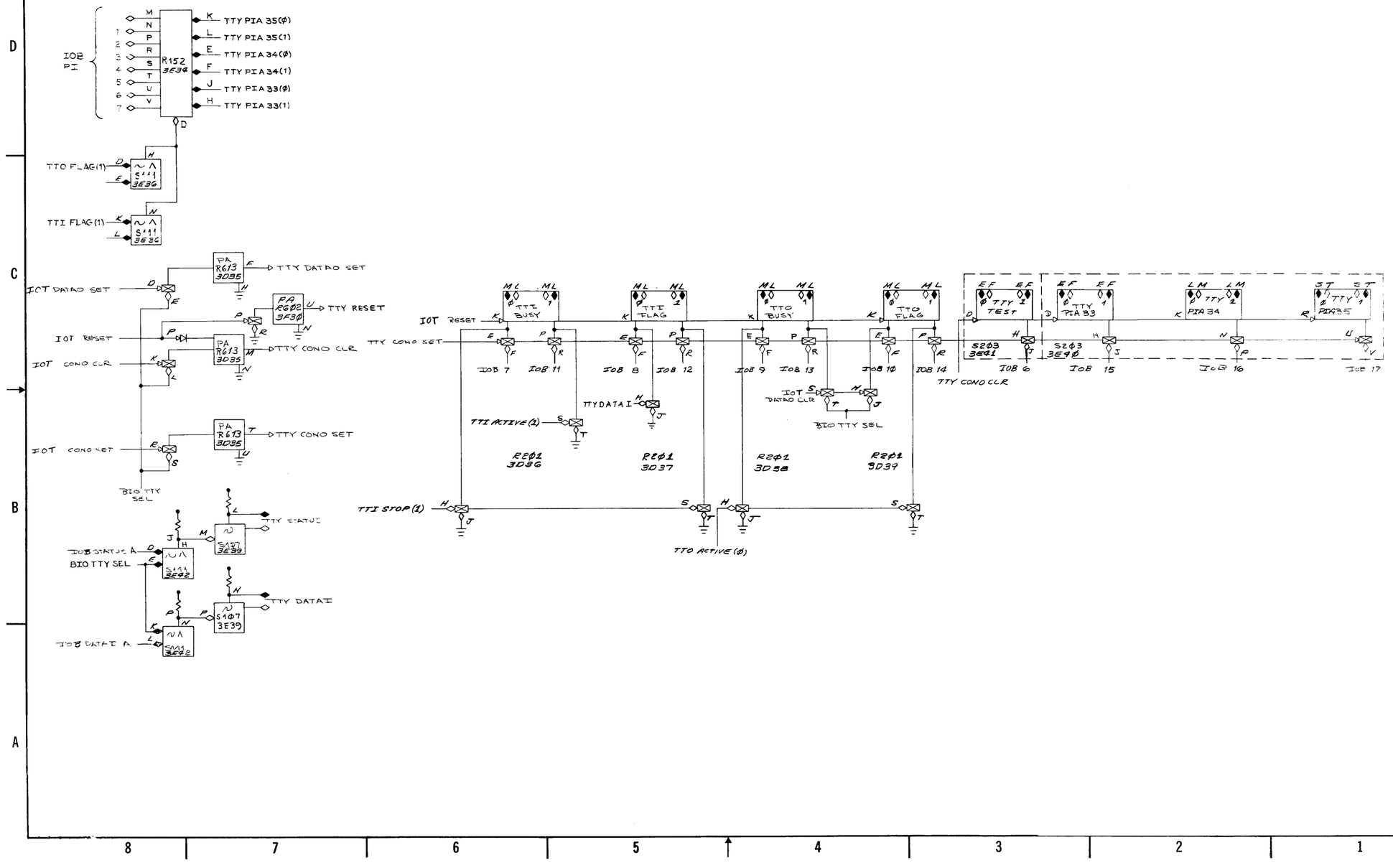
D-BS-KA10-0-SCC1 Shift Counter Control

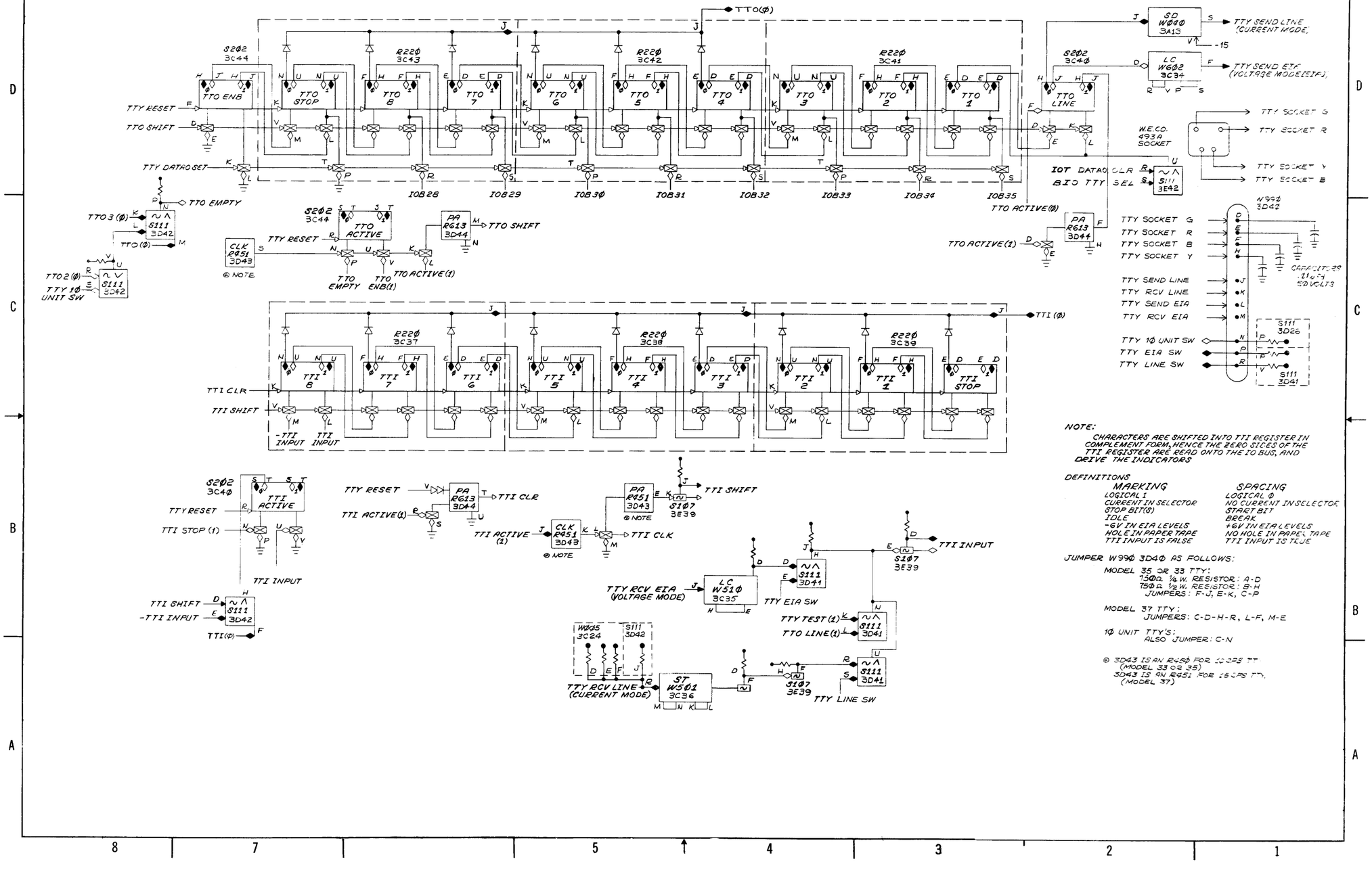


D-BS-KA10-0-SCC2 Shift Counter Control



D-BS-KA10-0-SCSR Shift and Cnt Subrtn and Shift Inst


IOB PI
R152 3E36
TTY PIA 35(0)
TTY PIA 35(1)
TTY PIA 34(0)
TTY PIA 34(1)
TTY PIA 33(0)
TTY PIA 33(1)
TTO FLAG(1)
TTI FLAG(1)
IOT DATAO SET
IOT RESET
IOT CONO CLR
IOT CONO SET
TTY DATAO SET
TTY RESET
TTY CONO CLR
TTY CONO SET
BIO TTY SEL
IOB STATUS A
TTY STATUS
IOB DATA I A
TTY DATA I
TTI BUSY
TTI FLAG
TTO BUSY
TTO FLAG
TTY TEST
TTY PIA 33
TTY PIA 34
TTY PIA 35
IOB 7
IOB 11
IOB 8
IOB 12
IOB 9
IOB 13
IOB 10
IOB 14
IOB 6
IOB 15
IOB 16
IOB 17
TTY CONO CLR
TTI ACTIVE(1)
TTYDATA I
IOT DATAO CLR
BIO TTY SEL
TTI STOP(1)
TTO ACTIVE(0)
R2Φ1 3D36
R2Φ1 3D37
R2Φ1 3D38
R2Φ1 3D39



NOTE:

CHARACTERS ARE SHIFTED INTO TTI REGISTER IN COMPLEMENT FORM, HENCE THE ZERO SIDES OF THE TTI REGISTER ARE READ ONTO THE IO BUS, AND DRIVE THE INDICATORS

DEFINITIONS

MARKING	SPACING
LOGICAL 1	LOGICAL Ø
CURRENT IN SELECTOR	NO CURRENT IN SELECTOR
STOP BIT(S)	START BIT
IDLE	BREAK
-6V IN EIA LEVELS	+6V IN EIA LEVELS
HOLE IN PAPER TAPE	NO HOLE IN PAPER TAPE
TTI INPUT IS FALSE	TTI INPUT IS TRUE

JUMPER W99Ø 3D4Ø AS FOLLOWS:

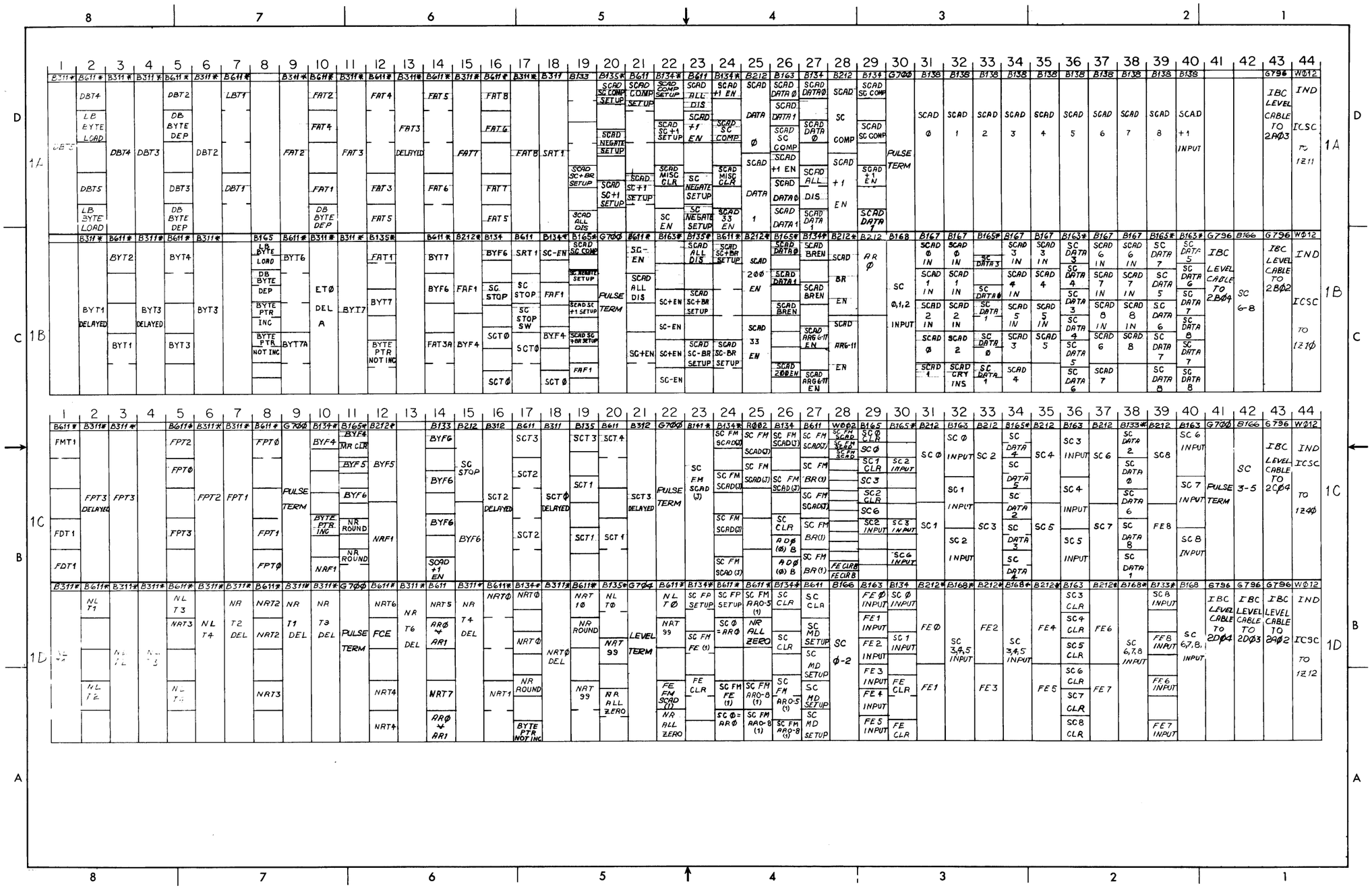
MODEL 35 OR 33 TTY:
- 75Ø Ω 1/4 W. RESISTOR: A-D
- 75Ø Ω 1/2 W. RESISTOR: B-H
- JUMPERS: F-J, E-K, C-P

MODEL 37 TTY:
- JUMPERS: C-D-H-R, L-F, M-E

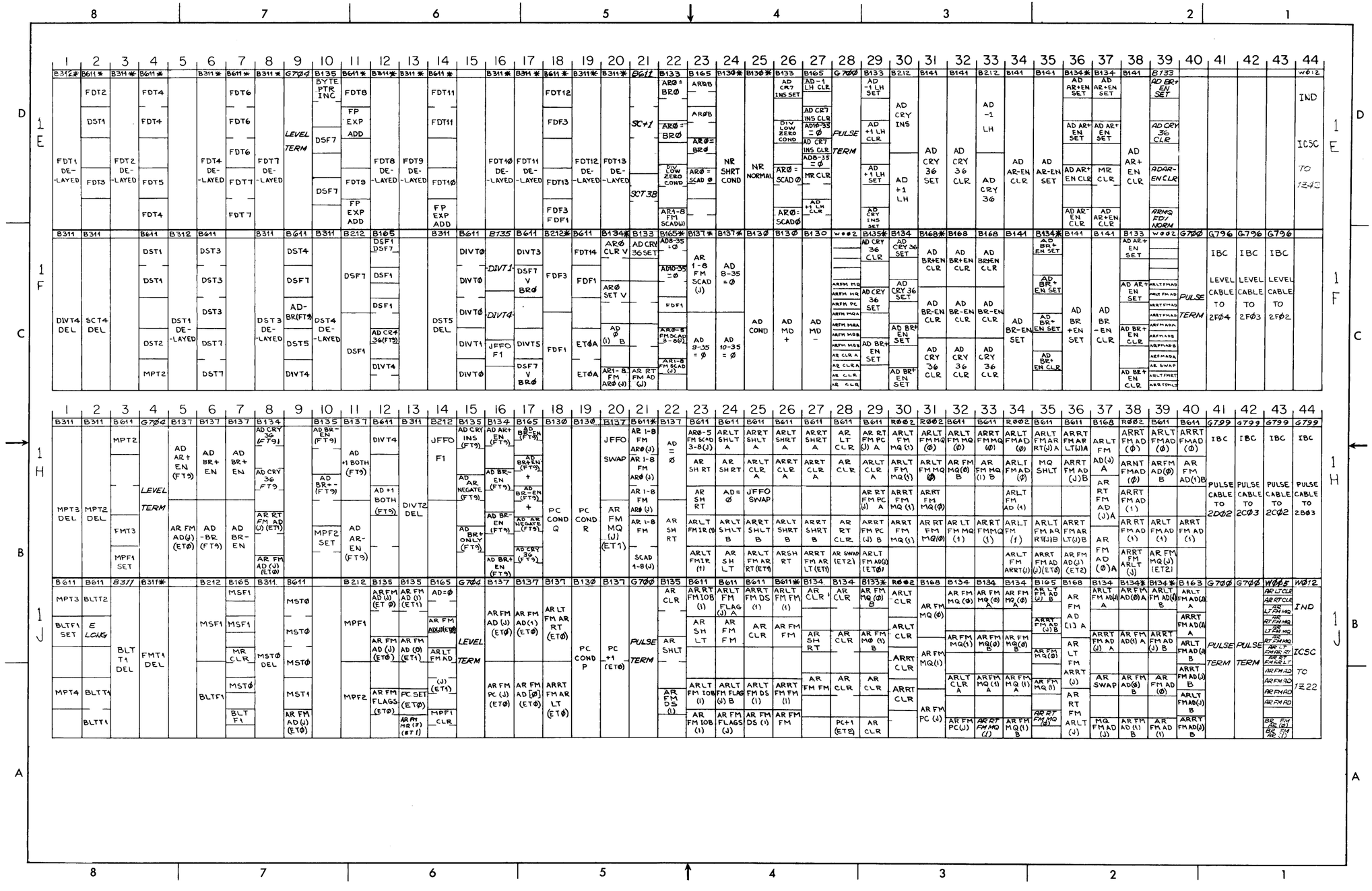
1Ø UNIT TTY'S:
- ALSO JUMPER: C-N

⊕ 3D43 IS AN R45Ø FOR 1Ø CPS TTY (MODEL 33 OR 35)
3D43 IS AN R451 FOR 15 CPS TTY (MODEL 37)

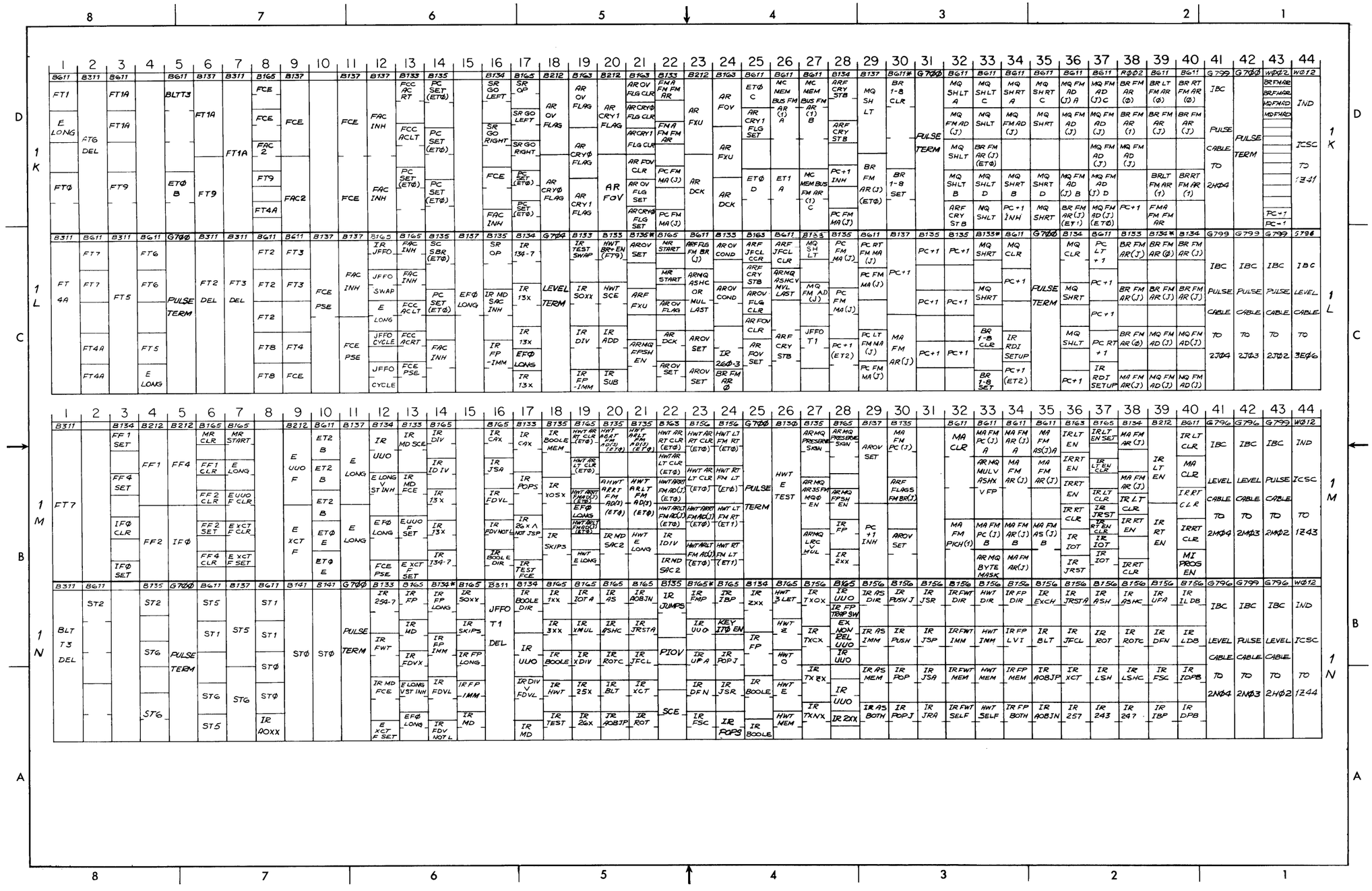
D-BS-KA10-0-TTY2 Teletype Control



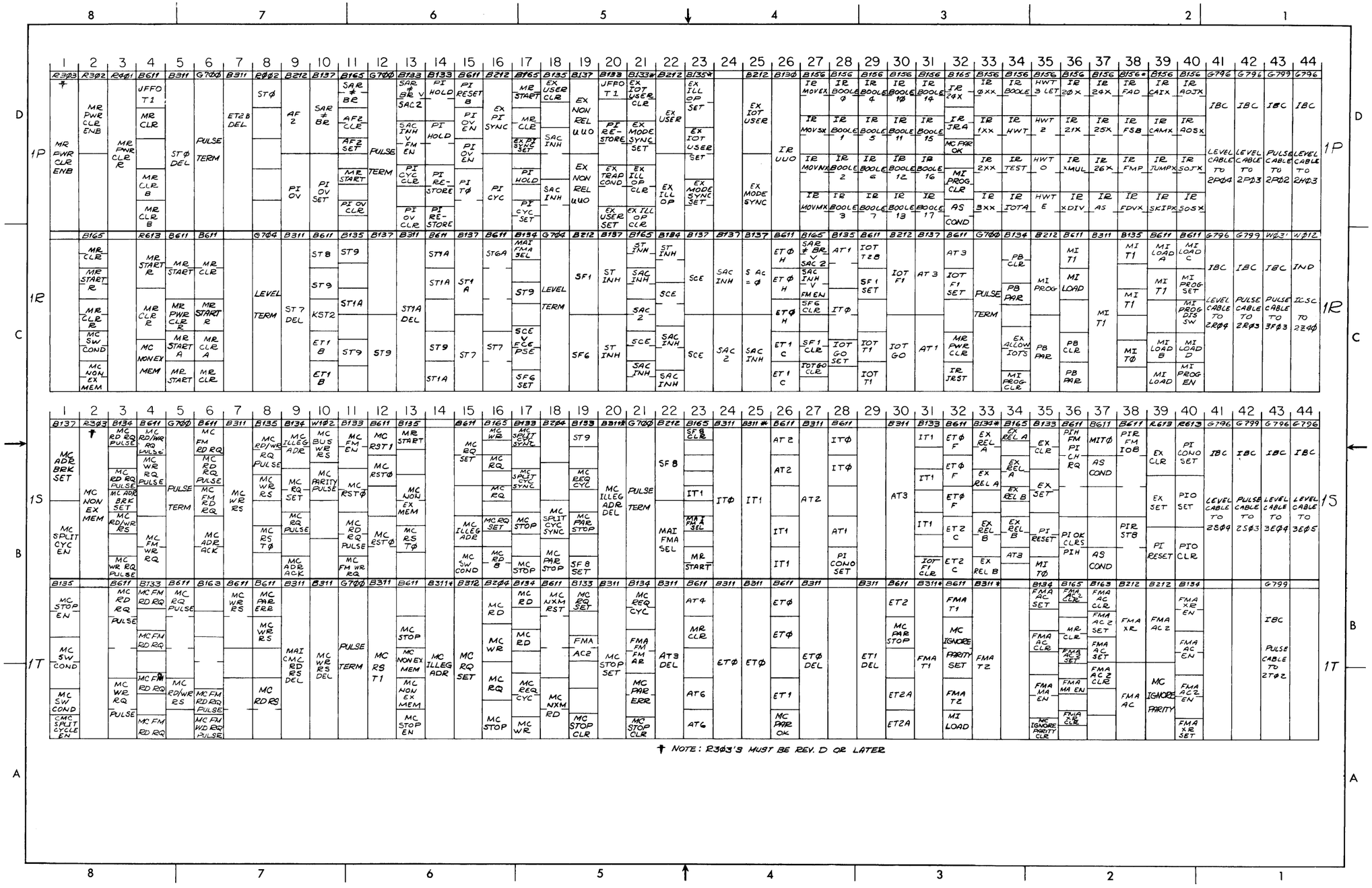
D-MU-KA10-0-IA1D Module Utilization PDP-10 (Panels 1A-1D)



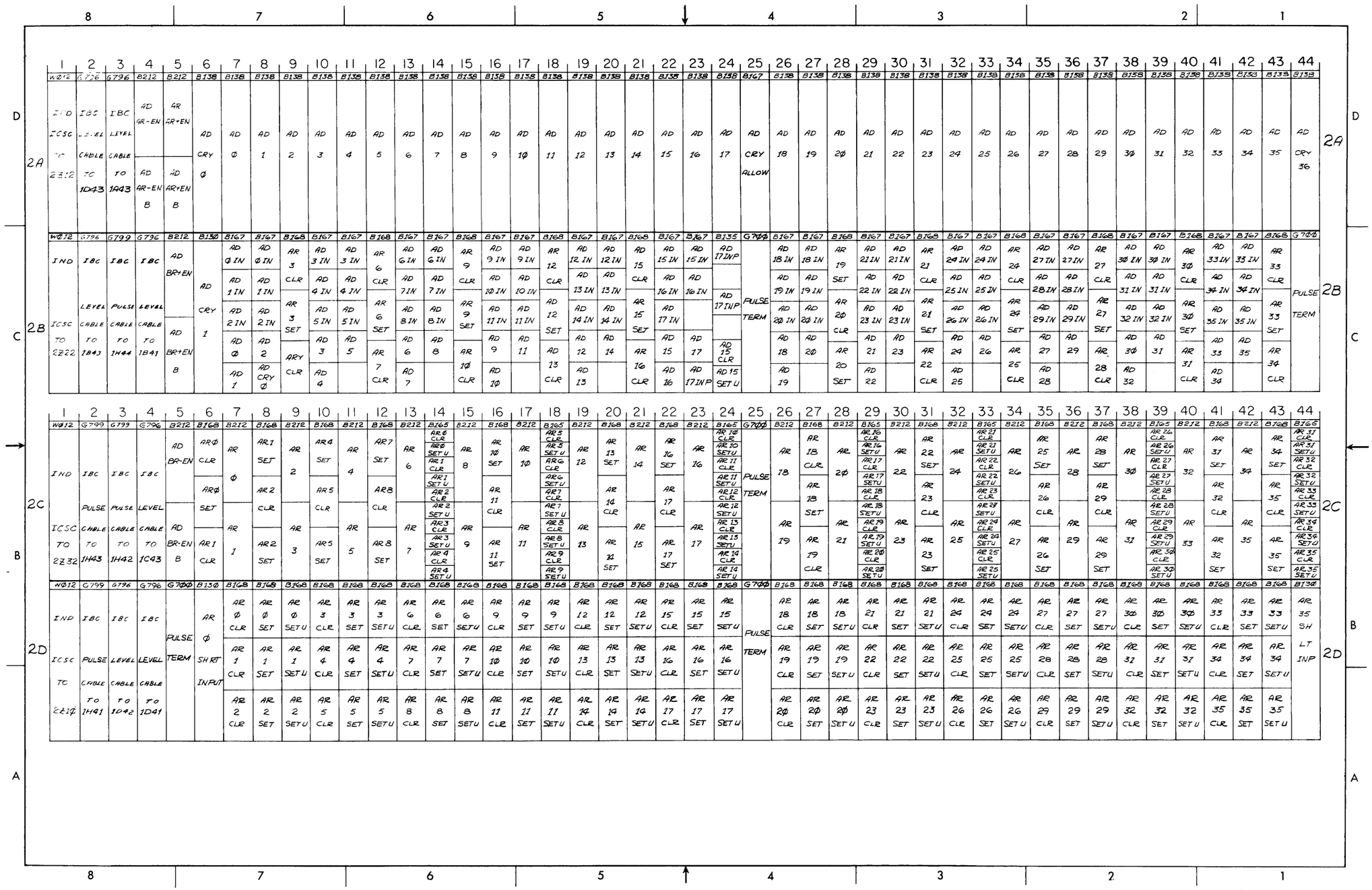
D-MU-KA10-0-1E1J Module Utilization PDP-10 (Panels 1E-1J)

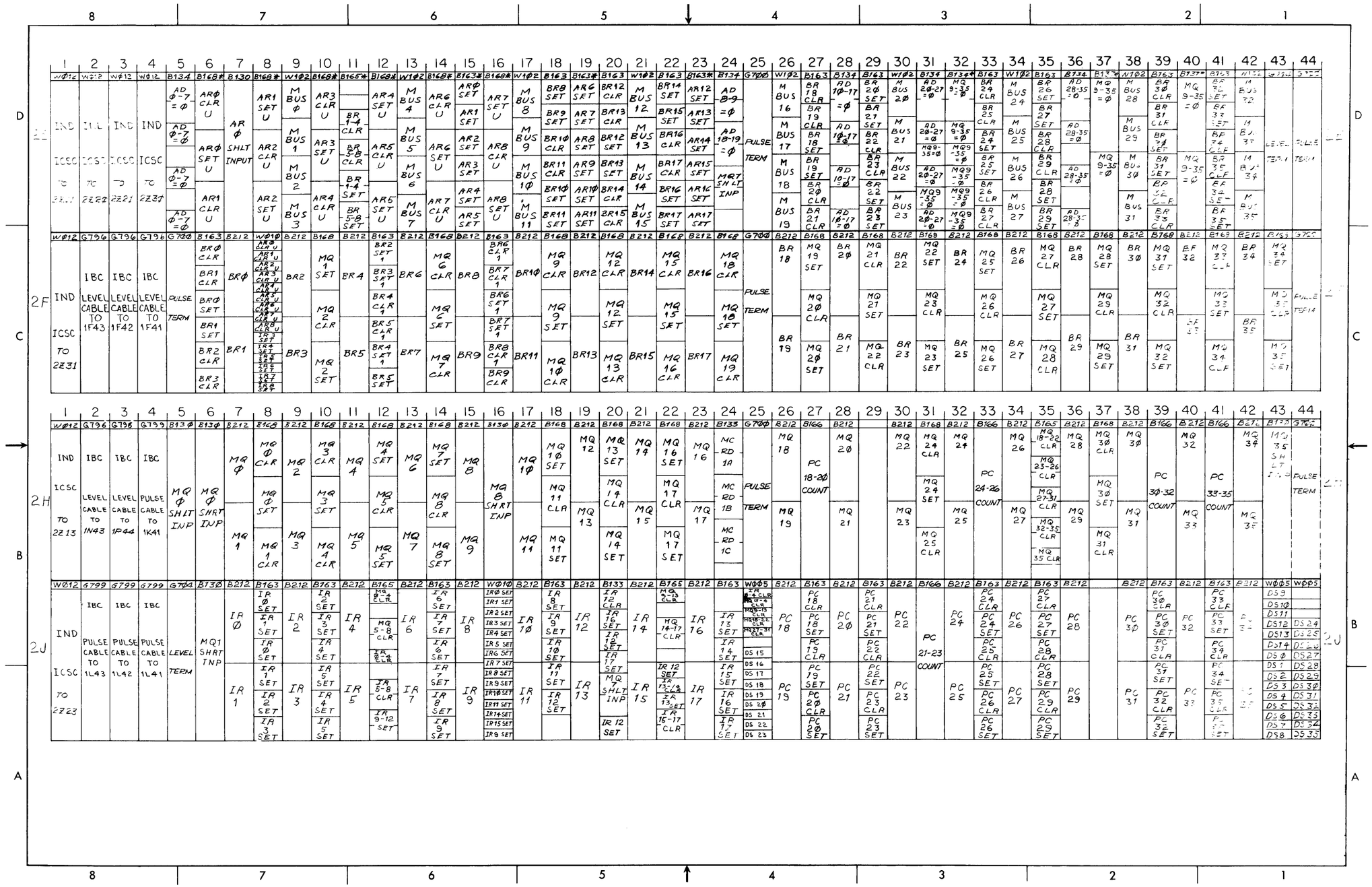


D-MU-KA10-0-1K1N Module Utilization PDP-10 (Panels 1K-1N)

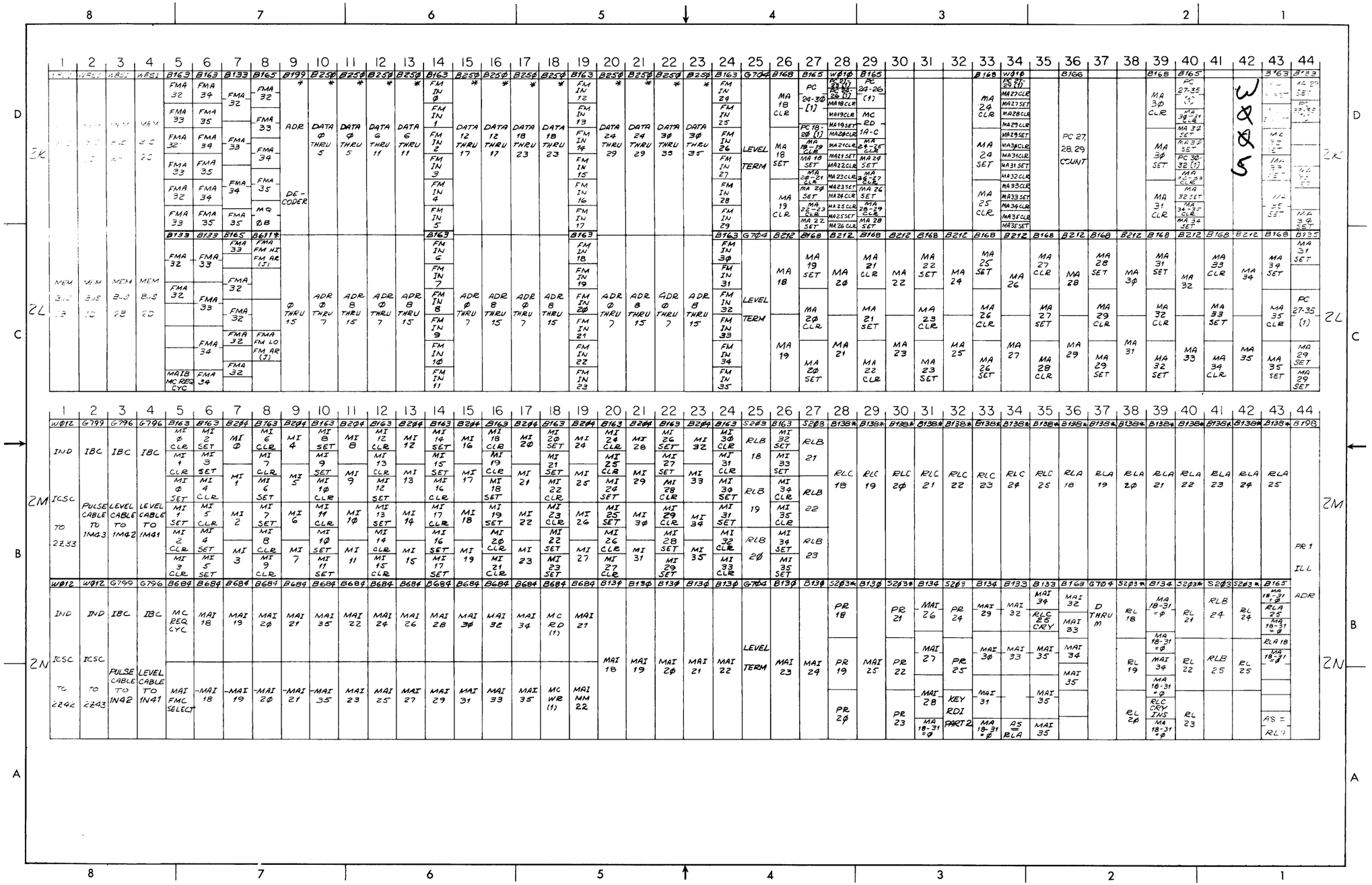


D-MU-KA10-0-1P1T Module Utilization PDP-10 (Panels 1P-1T)

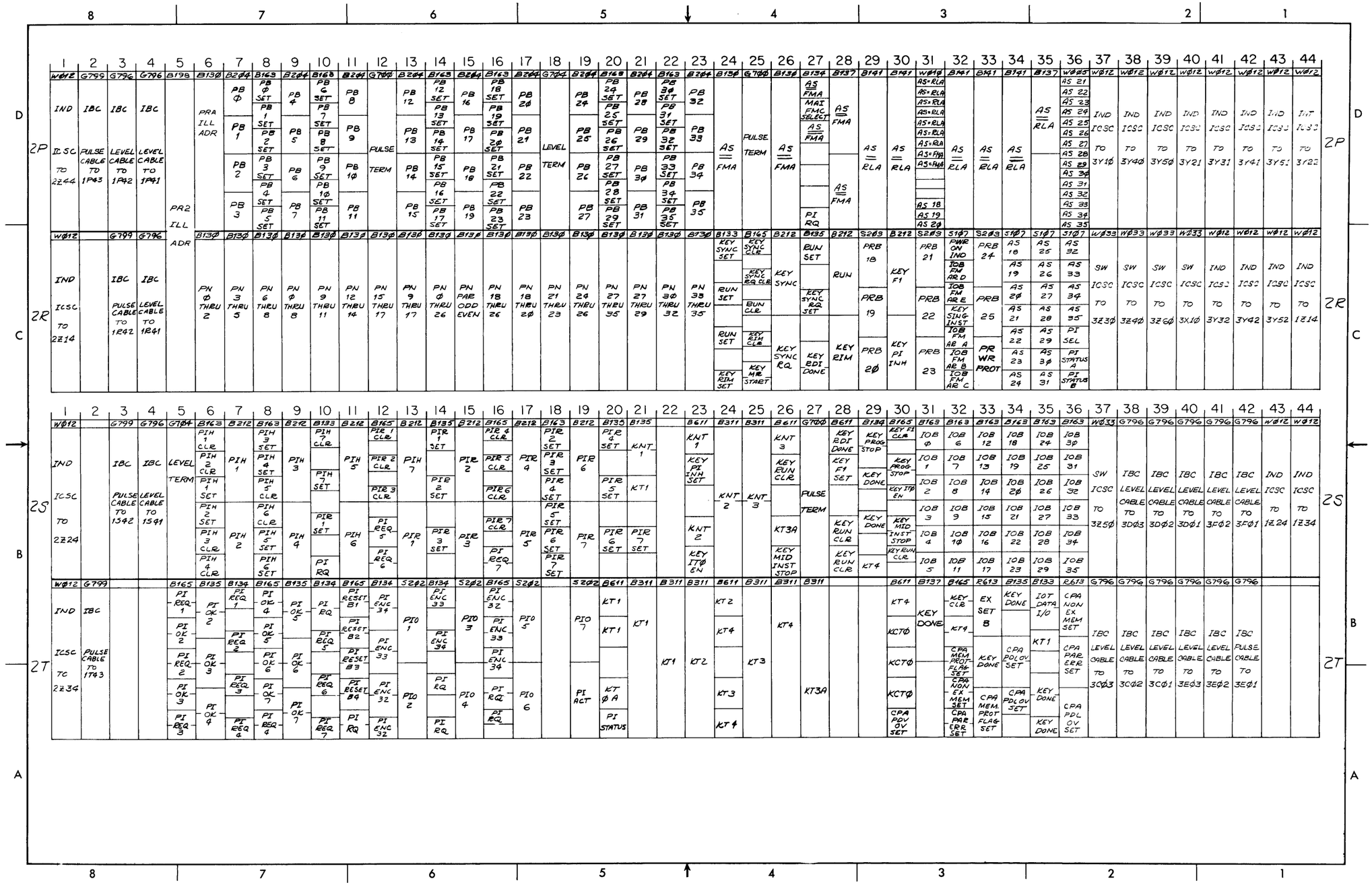

2A
2B
2C
2D
IND
IBC
PULSE
LEVEL
CABLE
ICSC
TO
PULSE
TERM
AD
AR
CRY
CLR
SET
SETU
INP
SH
LT



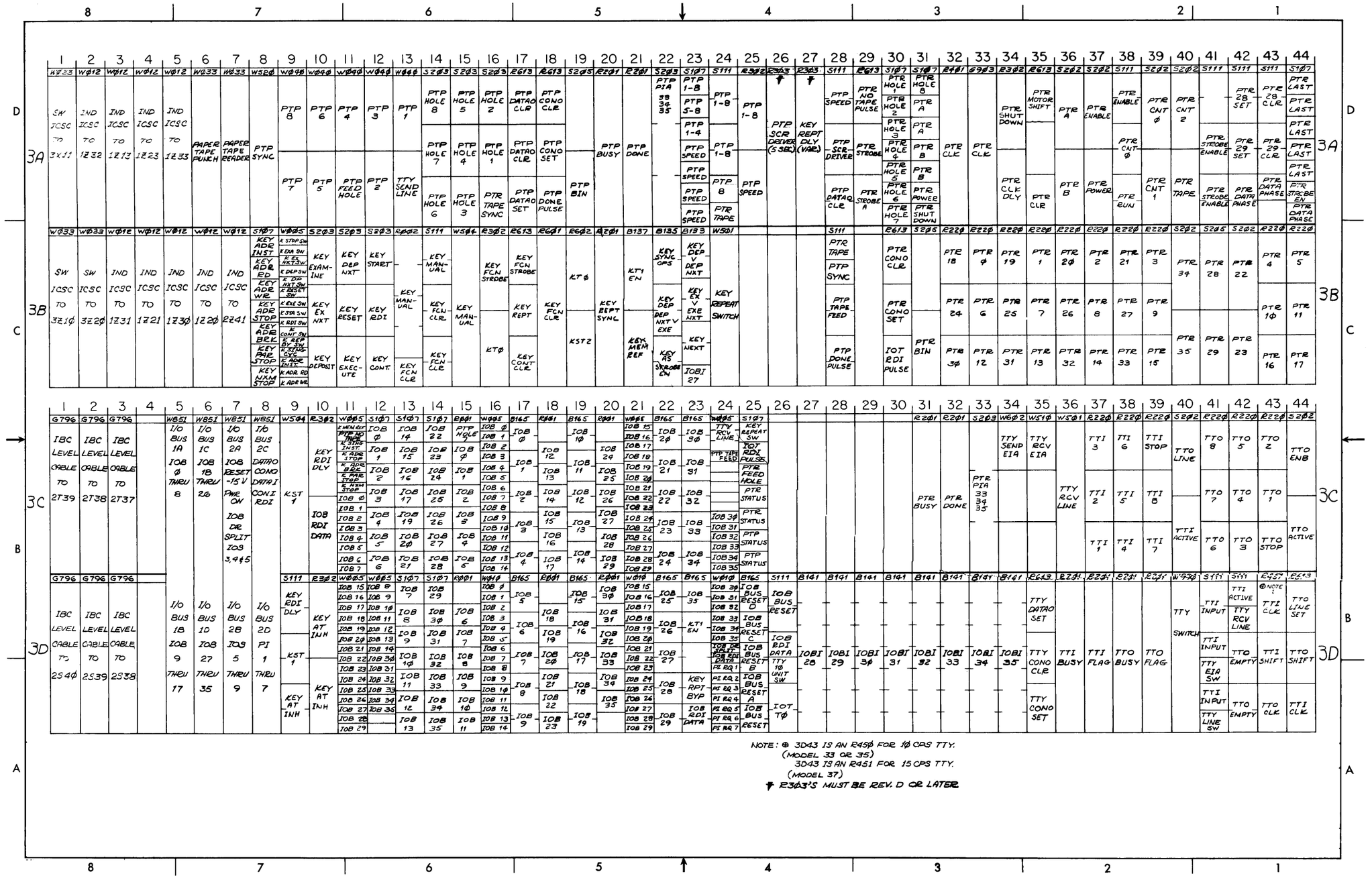
D-MU-KA10-0-2E2J Module Utilization PDP-10 (Panels 2E-2J)



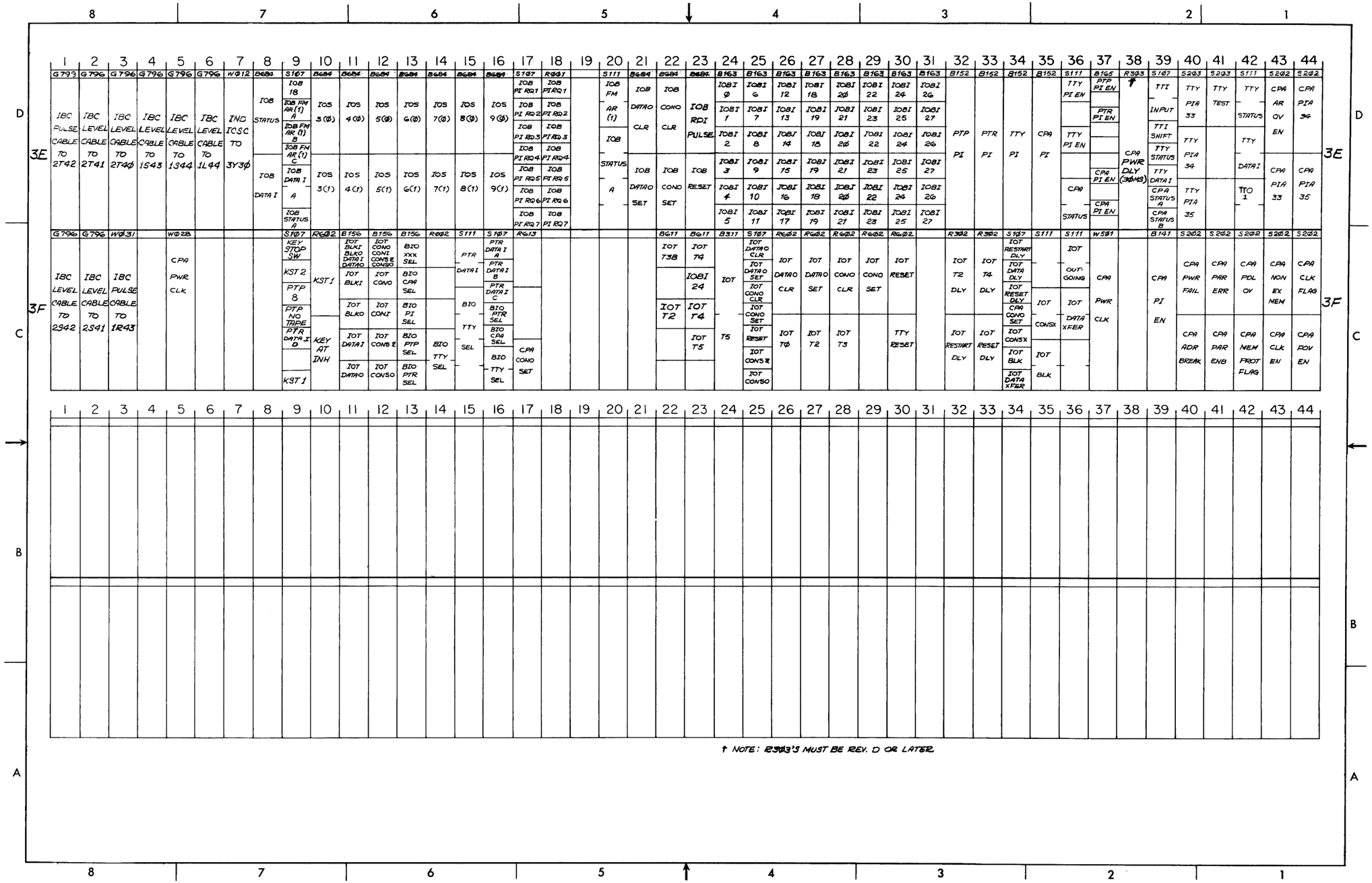
D-MU-KA10-0-2K2N Module Utilization PDP-10 (Panels 2K-2N)



D-MU-KA10-0-2P2T Module Utilization PDP-10 (Panels 2P-2T)



D-MU-KA10-0-3A3D Module Utilization PDP-10 (Panels 3A-3D)



D-MU-KA10-0-3E3F Module Utilization PDP-10 (Panels 3E-3F)

PARTS LIST		DIGITAL EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS			REVISIONS		
PART NO.	DRWG. NO.	NO. REQD.	DESCRIPTION ITEM — STOCK SIZE — CAT. NO. — MFG.	DEC. STOCK NO.	CHANGE NO.	DATE	ENG.
		48	3 BIT PARITY CIRCUIT	B130 2	A-29	5-20-68	RC
		45	DIODE GATE	B133 2			
		66	DIODE GATE	B134 2			
		45	DIODE GATE	B135 2			
		40	DIODE GATE	B137 2			
		64	ADDER	B138 2			
		25	DIODE GATE	B141 2			
		4	BINARY TO OCTAL DECODER	B152			
		31	HALF BINARY TO OCTAL DECODER	B156 2			
		89	DIODE GATE	B163 2			
		85	DIODE INVERTER	B165 2			
		9	COUNTING GATE	B166			
		31	ADDER GATE	B167			
		113	DIODE GATE	B168 2			
		2 1	PROTECTION COMPARATOR FM ADDRESS DECODER	B198 2 B199 2			
		20	FOUR FLIP FLOPS	B204			

A-PL-KA10-0-MC Module Count (Sheet 1)

PARTS LIST		DIGITAL EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS			REVISIONS		
PART NO.	DRWG. NO.	NO. REQD.	DESCRIPTION ITEM — STOCK SIZE — CAT. NO. — MFG.	DEC. STOCK NO.	CHANGE NO.	DATE	ENG.
		136	DUAL R-S FLIP FLOP	B212 2			
		12	FM MODULE	B250 2			
		91	TAPPED DELAY LINE	B311 2			
		5	VARIABLE DELAY LINE	B312 2			
		144	PULSE AMPLIFIER	B611 2			
		26	TWO BUS DRIVERS	B684			
		39	100Ω TERMINATOR	G700			
		15	2 MA LEVEL TERMINATOR	G704			
		1	CLOCK ACCELERATOR	G903			
		7	DIODE NETWORK	R001			
		10	DIODE CLUSTER	R002			
		9	2 MC FLIP FLOP	R201			
		16	3 BIT SHIFT REGISTER	R220			
		8	DELAY	R302			
		5	INTEGRATING ONE-SHOT	R303			
		2	CLOCK	R401			

A-PL-KA10-0-MC Module Count (Sheet 2)

PARTS LIST	DIGITAL EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS			REVISIONS		
PART NO.	DRWG. NO.	NO. REQD.	DESCRIPTION ITEM — STOCK SIZE — CAT. NO. — MFG.	DEC. STOCK NO.	CHANGE NO.	DATE	ENG.
		1	VARIABLE CLOCK	R450 [1]			
		1	PULSE AMPLIFIER	R601			
		7	PULSE AMPLIFIER	R602			
		14	PULSE AMPLIFIER	R613			
		22	INVERTER	S107			
		18	DIODE GATE	S111			
		19	DUAL FLIP FLOP	S202			
		22	TRIPLE FLIP FLOP	S203 [2]			
		3	DUAL FLIP FLOP	S205			
		4	CLAMP LOADS	W002			
		12	CLAMPED LOADS	W005			
		8	CLAMPED LOADS	W010			
		5	SOLENOID DRIVER	W040			
		10	PULSED BUS TRANSCIEVER	W102			
		3	SCHMITT TRIGGER	W501			
		2	INITIAL TRANSIENT DETECTOR	W504			

PARTS LIST	DIGITAL EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS			REVISIONS		
PART NO.	DRWG. NO.	NO. REQD.	DESCRIPTION ITEM — STOCK SIZE — CAT. NO. — MFG.	DEC. STOCK NO.	CHANGE NO.	DATE	ENG.
		1	PULSE LEVEL CONVERTER	W510			
		1	COMPARATOR	W520			
		1	BIPOLAR LEVEL AMPLIFIER	W602			
		1	SPLIT LUG BOARD	W990			
	NOTES:						
		1.	THE R450 IS USED WITH A MODEL 33 OR 35 TELETYPE				
			A R451 IS USED WITH A MODEL 37 TELETYPE				
		2.	THE MODULE COUNT INDICATED FOR THESE MODULES INCLUDE				
			THE MODULE COUNT FOR THE INTERNAL OPTIONS (KE10,KT10,KM10).				
			THE FOLLOWING IS A BREAK DOWN OF THE MODULES IN				
			THESE OPTIONS BUT THESE ARE NOT ADDITIONAL MODULES AS				
			THEY ARE ALREADY INCLUDED IN THE ABOVE MODULE COUNT.				
			KE10				
		2	3 BIT PARITY CIRCUIT	B130			

PARTS LIST	DIGITAL EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS				REVISIONS		
PART NO.	DRWG. NO.	NO. REQD.	DESCRIPTION ITEM — STOCK SIZE — CAT. NO. — MFG.	DEC. STOCK NO.	CHANGE NO.	DATE	ENG.
			KE10 CONT.				
		4	DIODE GATE	B133			
		16	DIODE GATE	B134			
		6	DIODE GATE	B135			
		4	DIODE GATE	B137			
		1	DIODE GATE	B141			
		1	HALF BINARY TO OCTAL DECODER	B156			
		3	DIODE GATE	B163			
		10	DIODE INVERTER	B165			
		9	DIODE GATE	B168			
		9	DUAL R-S FLIP FLOP	B212			
		39	TAPPED DELAY LINE	B311			
		1	VARIABLE DELAY LINE	B312			
		33	PULSE AMPLIFIER	B611			
			KT10				
		1 1	3 BIT PARITY CKT DIODE GATE	B130 B133			

PARTS LIST	DIGITAL EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS				REVISIONS		
PART NO.	DRWG. NO.	NO. REQD.	DESCRIPTION ITEM — STOCK SIZE — CAT. NO. — MFG.	DEC. STOCK NO.	CHANGE NO.	DATE	ENG.
		1	DIODE GATE	B134			
		1	DIODE GATE	B135			
		16	ADDER	B138			
		2 2	PROTECTION COMPARATOR TAPPED DELAY LINE	B198 B311			
		2 11	2MA LEVEL TERMINAOR TRIPLE FLIP FLOP	G704 S203			
			KM10				
		3	DIODE GATE	B163			
		1	FM ADDRESS DECODER	B199			
		12	FM MODULE	B250			
		2	TAPPED DELAY LINE	B311			
		2	PULSE AMPLIFIER	B611			

PARTS LIST ITEM NO.	MARK END	CONN. TYPE	TO	CONN. TYPE	MARK END	LENGTH	PART NO./DWG. NO.
1	2A01	W012	-	W250	2Z12	18 IN.	7005459-1
2	1C44	W012	-	W250	1Z40	29 IN.	7005459-2
2	2B01	W012	-	W250	2Z22	29 IN.	7005459-2
2	2P40	W012	-	W250	3Y21	29 IN.	7005459-2
2	2P44	W012	-	W250	3Y22	29 IN.	7005459-2
3	1E44	W012	-	W250	1Z42	30-1/2 IN	7005459-3
3	2D01	W012	-	W250	2Z10	30-1/2 IN	7005459-3
3	2P37	W012	-	W250	3Y10	30-1/2 IN.	7005459-3
4	2E01	W012	-	W250	2Z11	34 IN.	7005459-4
4	2H01	W012	-	W250	2Z13	34 IN.	7005459-4
5	2C01	W012	-	W250	2Z32	37 IN.	7005459-5
5	2P41	W012	-	W250	3Y31	37 IN.	7005459-5
5	2R41	W012	-	W250	3Y32	37 IN.	7005459-5
6	1A44	W012	-	W250	1Z11	39-1/2 IN	7005459-6
6	2E03	W012	-	W250	2Z21	39-1/2 IN	7005459-6
7	1B44	W012	-	W250	1Z10	42-1/2 IN	7005459-7
7	1D44	W012	-	W250	1Z12	42-1/2 IN	7005459-7
7	1K44	W012	-	W250	1Z41	42-1/2 IN	7005459-7
7	2E02	W012	-	W250	2Z20	42-1/2 IN	7005459-7
7	2R42	W012	-	W250	3Y42	42-1/2 IN	7005459-7
8	2J01	W012	-	W250	2Z23	44-1/2 IN	7005459-8
8	2P39	W012	-	W250	3Y40	44-1/2 IN	7005459-8
8	2P42	W012	-	W250	3Y41	44-1/2 IN	7005459-8
9	1M44	W012	-	W250	1Z43	47-1/2 IN	7005459-9
9	1N44	W012	-	W250	1Z44	47-1/2 IN	7005459-9
9	2E04	W012	-	W250	2Z30	47-1/2 IN	7005459-9
9	2F01	W012	-	W250	2Z31	47-1/2 IN	7005459-9
9	2P43	W012	-	W250	3Y51	47-1/2 IN	7005459-9
10	1J44	W012	-	W250	1Z22	49-1/2 IN	7005459-10
10	2P39	W012	-	W250	3Y50	49-1/2 IN	7005459-10
10	2R43	W012	-	W250	3Y52	49-1/2 IN	7005459-10
11	2R01	W012	-	W250	2Z14	52-1/2 IN	7005459-11
12	2M01	W012	-	W250	2Z33	56-1/2 IN	7005459-12
12	3E07	W012	-	W250	3Y30	56-1/2 IN	7005459-12
13	2S01	W012	-	W250	2Z24	63-1/2 IN	7005459-13
14	2N01	W012	-	W250	2Z42	68-1/2 IN	7005459-14
14	2N02	W012	-	W250	2Z43	68-1/2 IN	7005459-14
15	2T01	W012	-	W250	2Z34	71 IN.	7005459-15
15	2P01	W012	-	W250	2Z44	71 IN.	7005459-15
16	1R44	W012	-	W250	2Z40	77-1/2 IN	7005459-16
17	3B03	W012	-	W250	1Z31	142 IN.	7005459-17
17	3A02	W012	-	W250	1Z32	142 IN.	7005459-17
18	3B05	W012	-	W250	1Z30	144 IN.	7005459-18
18	3A05	W012	-	W250	1Z33	144 IN.	7005459-18
18	2S44	W012	-	W250	1Z34	144 IN.	7005459-18
19	3B04	W012	-	W250	1Z21	145-1/2 IN	7005459-19
20	3B06	W012	-	W250	1Z20	148 IN.	7005459-20
20	3A04	W012	-	W250	1Z23	148 IN.	7005459-20
21	2S43	W012	-	W250	1Z24	150-1/2 IN	7005459-21
22	3A03	W012	-	W250	1Z13	153-1/2 IN	7005459-22
23	2R44	W012	-	W250	1Z14	156-1/2 IN	7005459-23
23	3B07	W012	-	W250	2Z41	156-1/2 IN	7005459-23
24	1A43	G796	-	G796	2A03	10 IN.	7005469-3
24	1C43	G796	-	G796	2C04	10 IN.	7005469-3

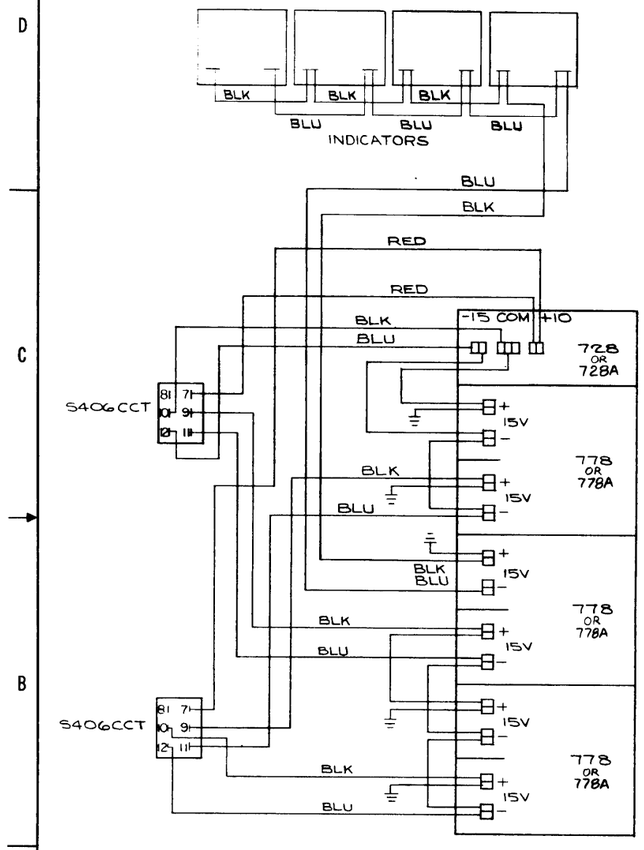
PARTS LIST	MARK	CONN.	TO	CONN.	MARK	LENGTH	PART NO. / DWG. NO.
24	1D41	G796	-	G796	2D04	10 IN.	7005469-3
24	1D42	G796	-	G796	2D03	10 IN.	7005469-3
24	1F42	G796	-	G796	2F03	10 IN.	7005469-3
24	1F43	G796	-	G796	2F02	10 IN.	7005469-3
24	1M42	G796	-	G796	2M03	10 IN.	7005469-3
24	1N41	G796	-	G796	2N04	10 IN.	7005469-3
24	1B43	G796	-	G796	2B02	10 IN.	7005469-3
24	1S41	G796	-	G796	2S04	10 IN.	7005469-3
24	1R42	G796	-	G796	2R03	10 IN.	7005469-3
24	1R41	G796	-	G796	2R04	10 IN.	7005469-3
24	1M41	G796	-	G796	2M04	10 IN.	7005469-3
25	1B41	G796	-	G796	2B04	12-1/2 IN.	7005469-4
25	1F41	G796	-	G796	2F04	12-1/2 IN.	7005469-4
25	1P41	G796	-	G796	2P04	12-1/2 IN.	7005469-4
25	1P42	G796	-	G796	2P03	12-1/2 IN.	7005469-4
26	1D43	G796	-	G796	2A02	20-1/2 IN.	7005469-5
27	1N43	G796	-	G796	2H02	29-1/2 IN.	7005469-6
28	1P44	G796	-	G796	2H03	35-1/2 IN.	7005469-7
29	3C01	G796	-	G796	2T39	47 IN.	7005469-8
29	3E03	G796	-	G796	2T40	47 IN.	7005469-8
29	3D01	G796	-	G796	2S40	47 IN.	7005469-8
30	3C02	G796	-	G796	2T38	49 IN.	7005469-9
30	3D03	G796	-	G796	2S38	49 IN.	7005469-9
30	3D02	G796	-	G796	2S39	49 IN.	7005469-9
30	3E02	G796	-	G796	2T41	49 IN.	7005469-9
30	3C03	G796	-	G796	2T37	49 IN.	7005469-9
31	3F01	G796	-	G796	2S42	56 IN.	7005469-10
31	3F02	G796	-	G796	2S41	56 IN.	7005469-10
32	3E04	G796	-	G796	1S43	92 IN.	7005469-11
32	3E05	G796	-	G796	1S44	92 IN.	7005469-11
33	3E06	G796	-	G796	1L44	111 IN.	7005469-12
34	1M43	G799	-	G799	2M02	12 IN.	7005463-1
34	1T43	G799	-	G799	2T02	12 IN.	7005463-1
34	1P43	G799	-	G799	2P02	12 IN.	7005463-1
34	1R42	G799	-	G799	2R03	12 IN.	7005463-1
34	1S42	G799	-	G799	2S03	12 IN.	7005463-1
34	1N42	G799	-	G799	2N03	12 IN.	7005463-1
35	1L43	G799	-	G799	2J02	11 IN.	7005463-11
34	1L42	G799	-	G799	2J03	12 IN.	7005463-1
37	1H41	G799	-	G799	2D02	23 IN.	7005463-4
36	1L41	G799	-	G799	2J04	13 IN.	7005463-10
36	1K41	G799	-	G799	2H04	13 IN.	7005463-10
39	1H42	G799	-	G799	2C03	26 IN.	7005463-6
39	1H44	G799	-	G799	2B03	26 IN.	7005463-6
40	1H43	G799	-	G799	2C02	28 IN.	7005463-7
41	2T42	G796	-	G796	3E01	56 IN.	7005469-10
42	1R43	W031	-	W031	3F03	92 IN.	7405552-6
43	3B01	W033	-	W033	3Z10	28 IN.	7405553-21
44	3B02	W033	-	W033	3Z20	30-1/2 IN.	7405553-22
45	2R37	W033	-	W033	3Z30	44 IN.	7405553-23
45	2R38	W033	-	W033	3Z40	44 IN.	7405553-23
46	2S37	W033	-	W033	3Z50	48-1/2 IN.	7405553-25
47	2R39	W033	-	W033	3Z60	53 IN.	7405553-24
48	2R40	W033	-	W033	3X10	38-1/2 IN.	7405553-26
45	3A01	W033	-	W033	3X11	44 IN.	7405553-23
* 45	3A06	W033	-	W033	PUNCH	44 IN.	7405553-23
* 45	3A07	W033	-	W033	READER	44 IN.	7405553-23

NOTES

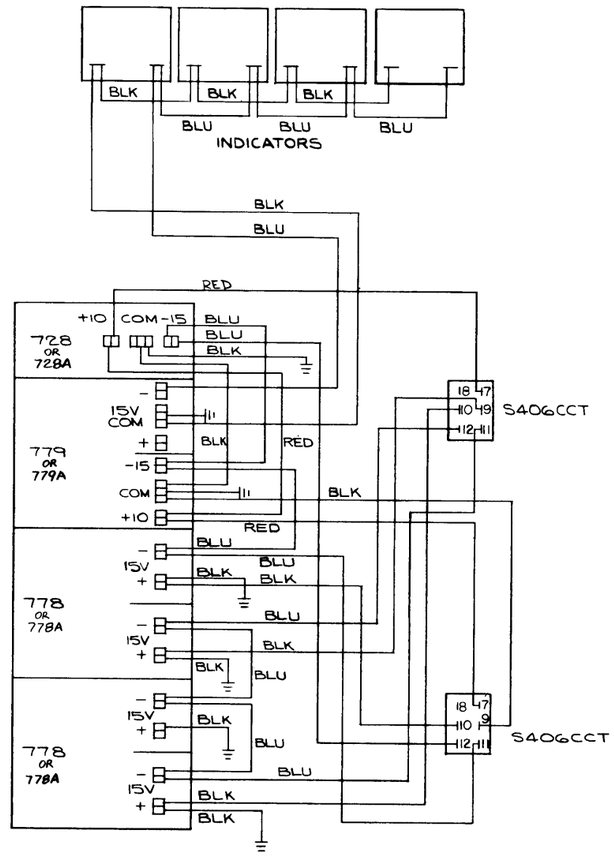
1. * WHEN INSTALLING THESE TWO CABLES, 3A06 TO THE PUNCH REQUIRES 10Ω ¼W PINS A,B. 3A07 TO THE READER REQUIRES JUMPERS PINS A,B.
2. ITEM #49 (B-DC-7406488-0-0) WILL BE PUT ON CABLES AT THE TIME OF ASSEMBLY.

D-AD-7006709-0-0 Cable Set

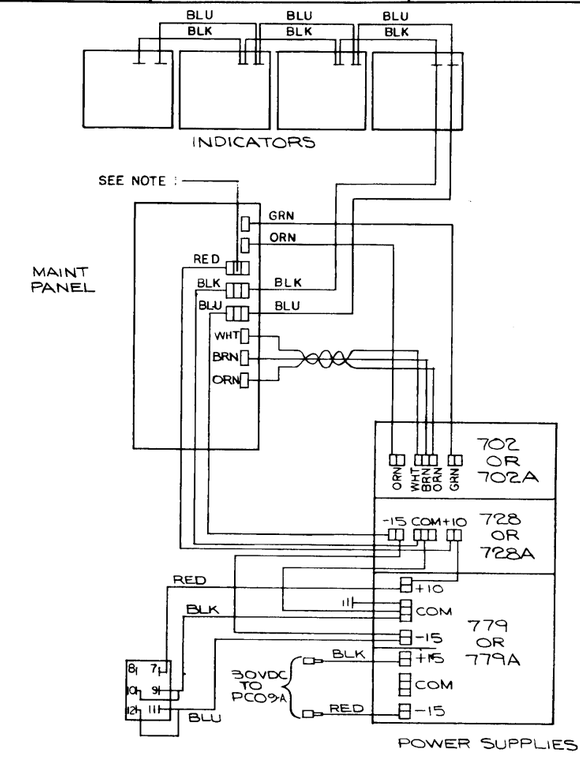
NOTE:
ALL WIRE TO BE #14 AWG STRANDED
UNLESS OTHER WISE SPECIFIED



BAY #1



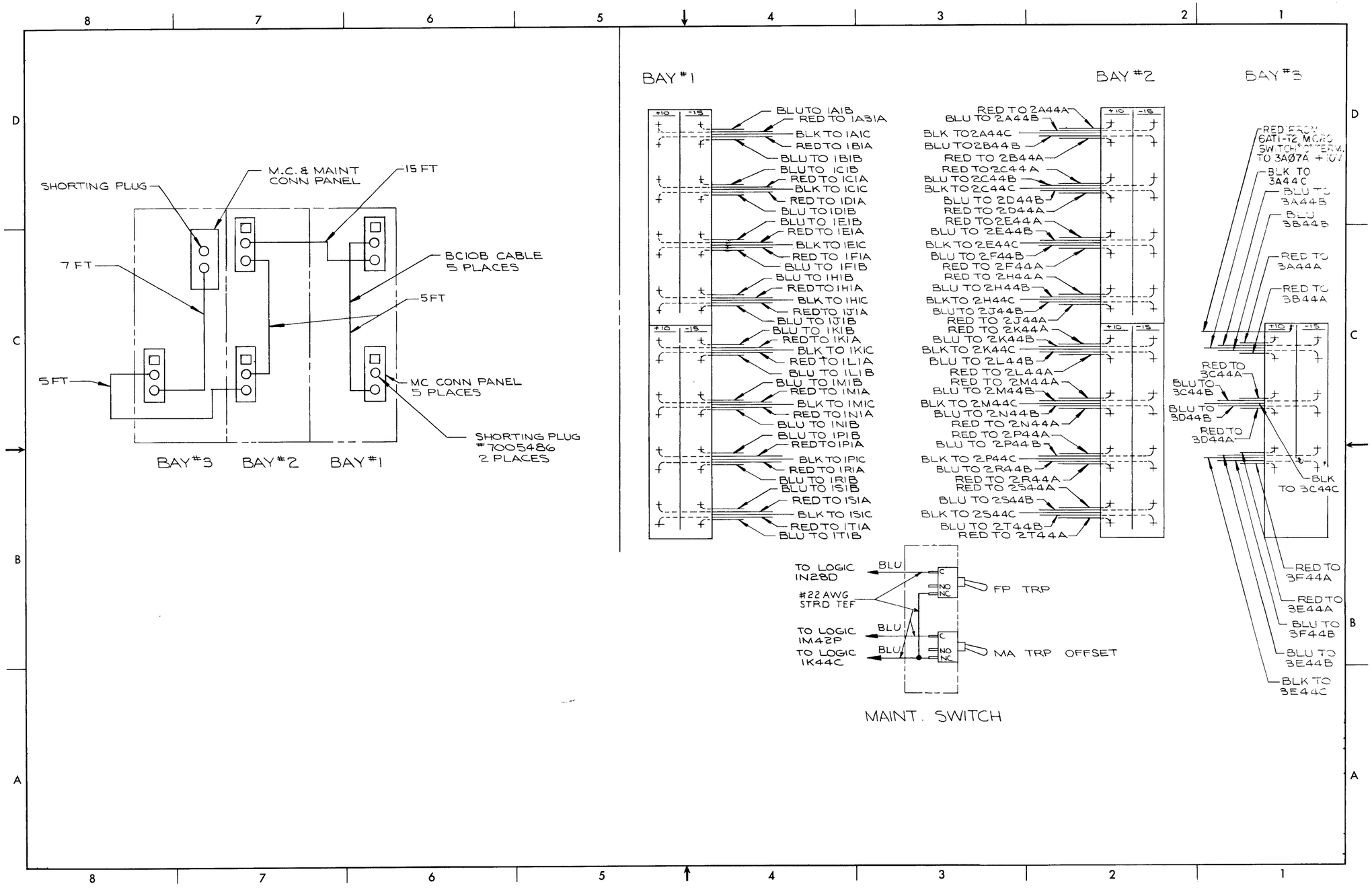
BAY #2



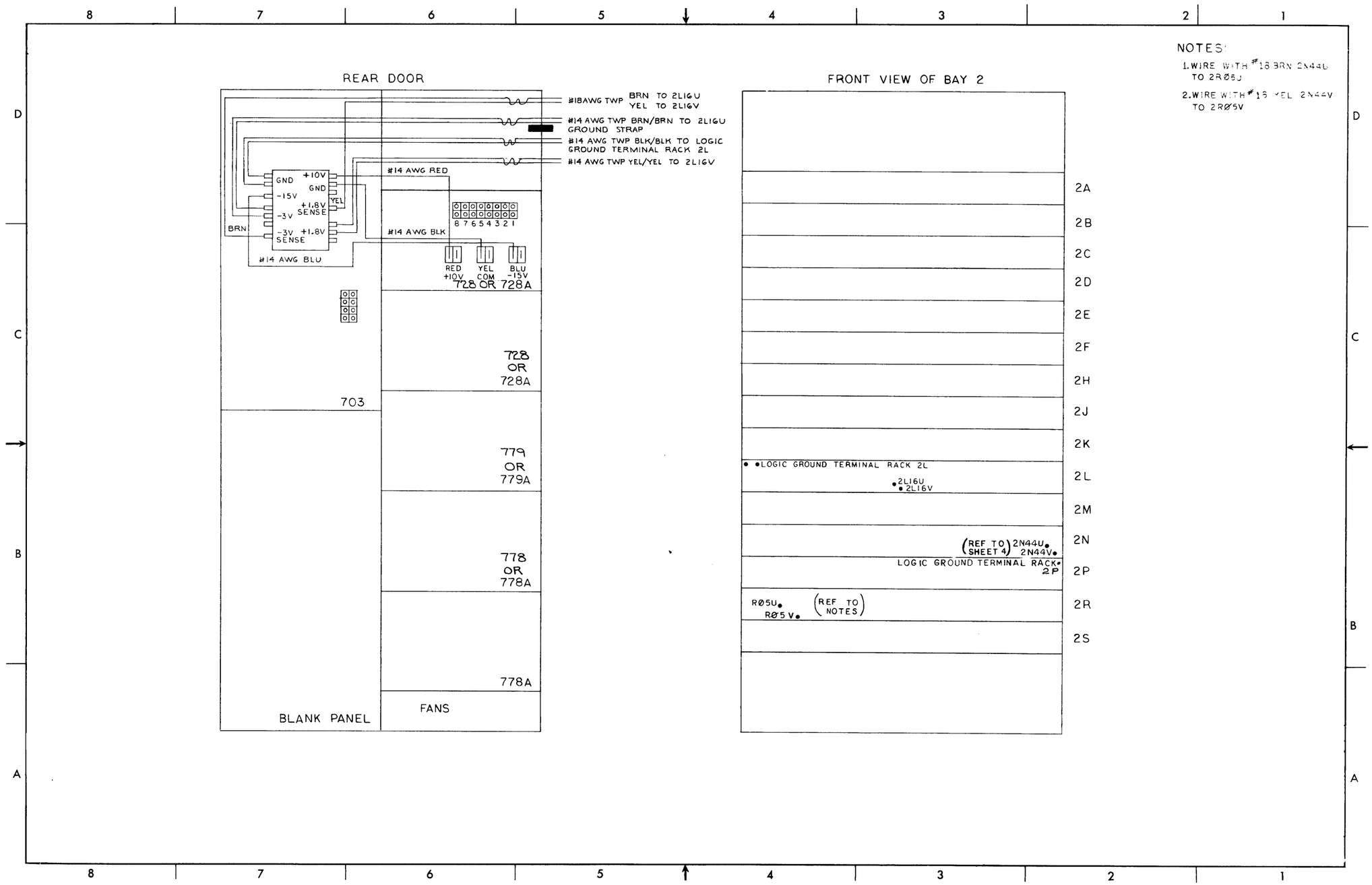
NOTES:
1. +10 VOLTS FOR PC09 LAMP IS WIRED FROM HERE.

BAY #3

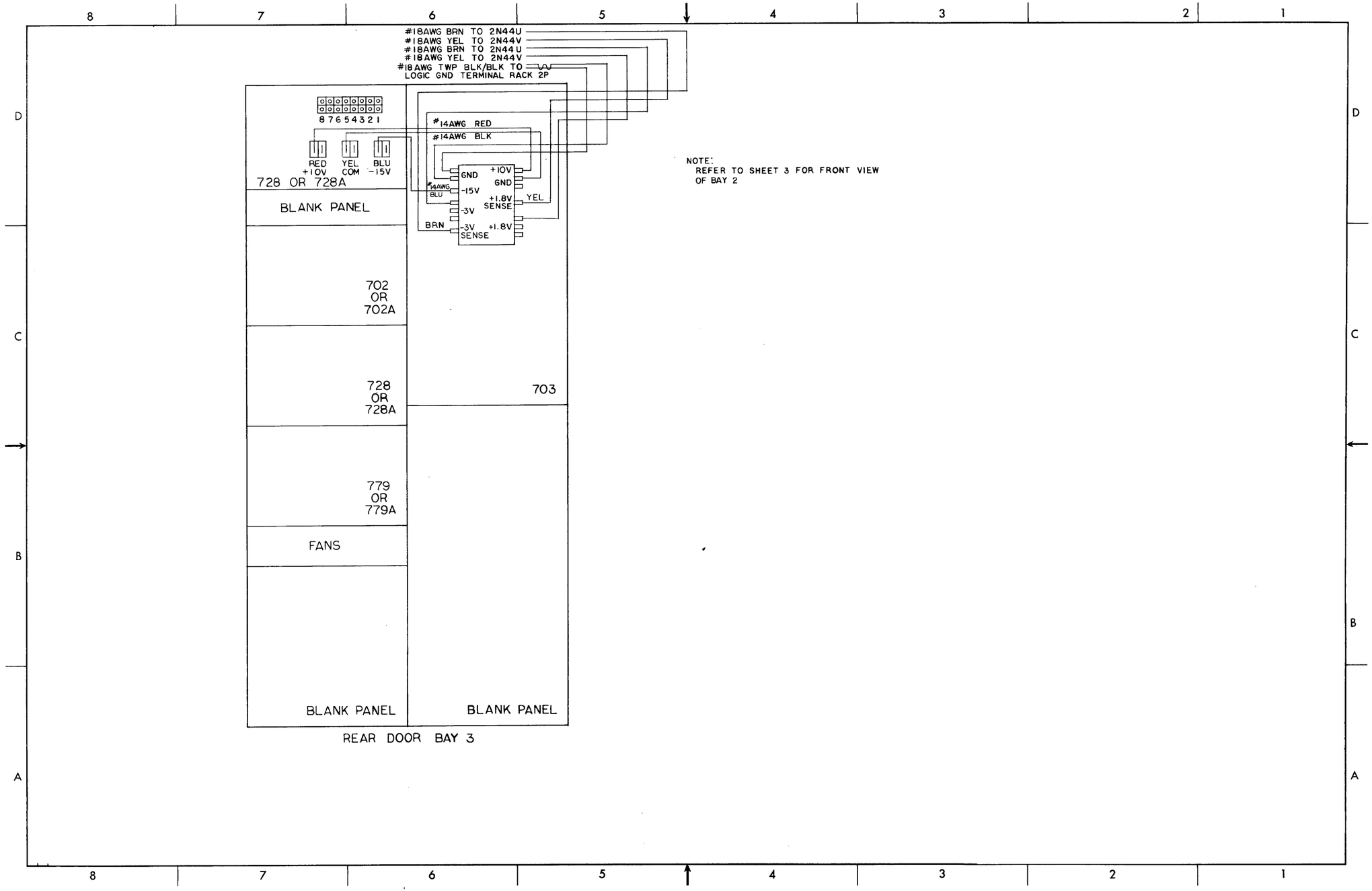
D-IC-KA10-0-1 DC Power Wiring (Sheet 1)



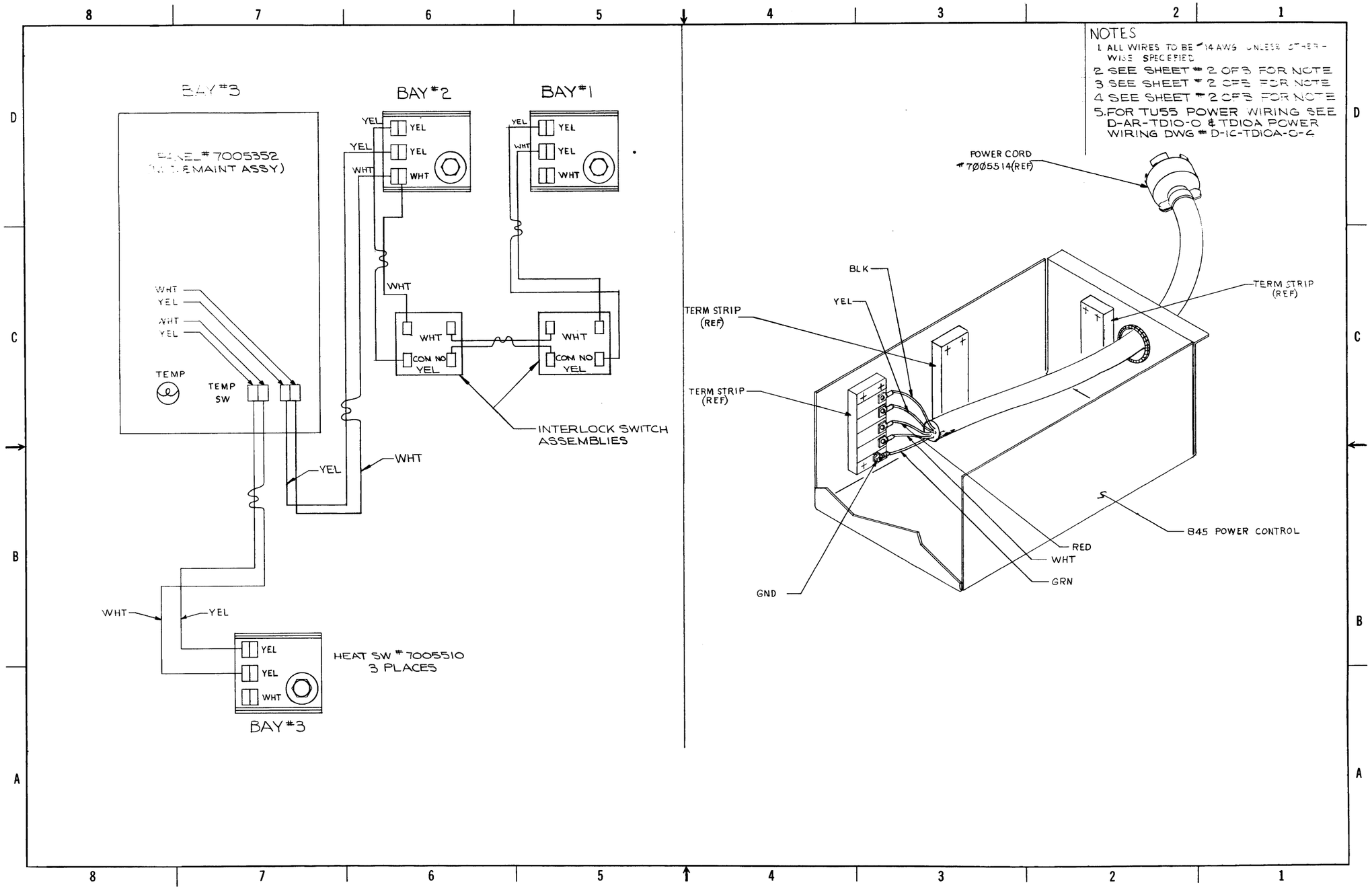
D-IC-KA10-0-1 DC Power Wiring (Sheet 2)



D-IC-KA10-0-1 DC Power Wiring (Sheet 3)



D-IC-KA10-0-1 DC Power Wiring (Sheet 4)

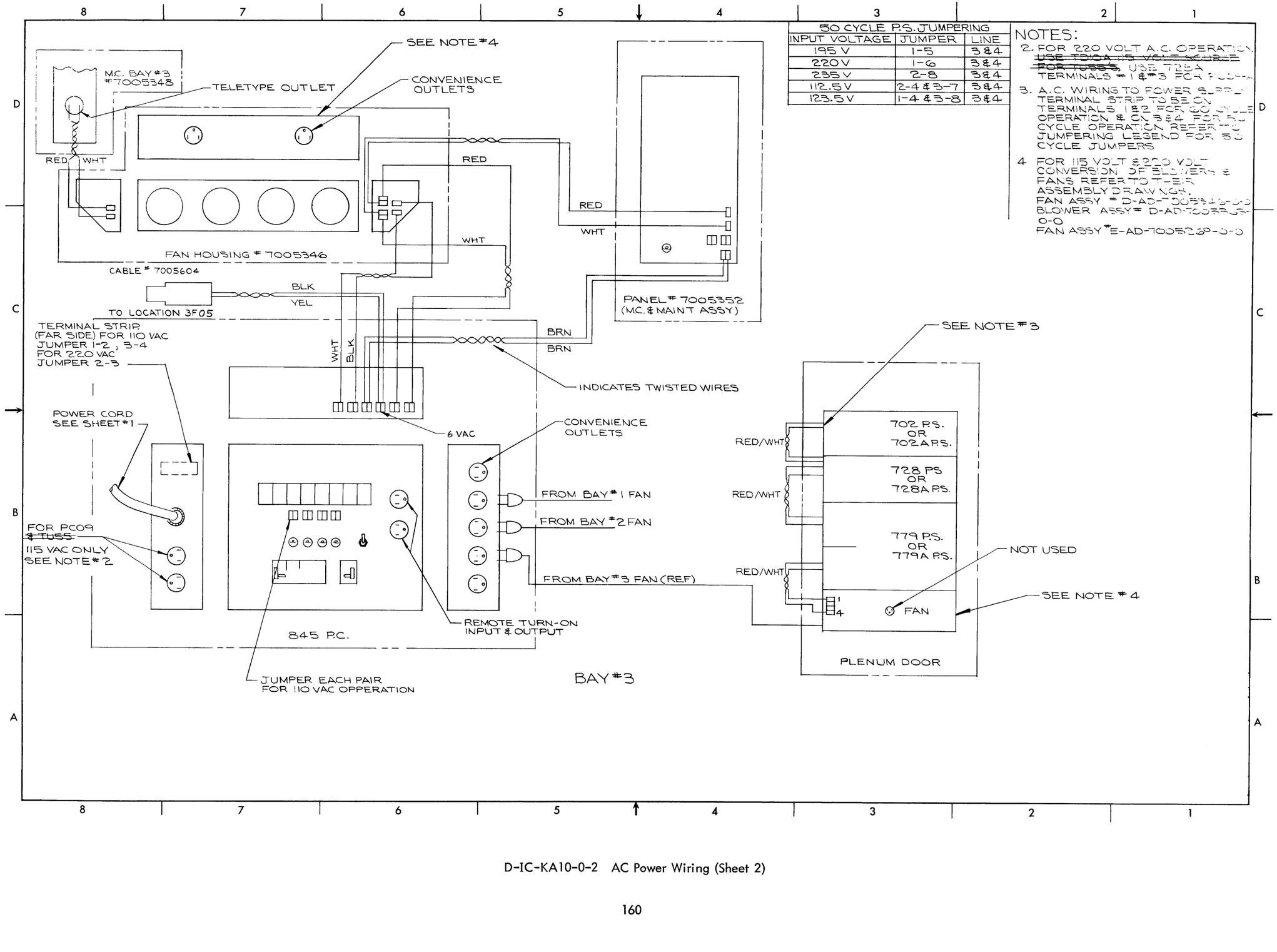


D-IC-KA10-0-2 AC Power Wiring (Sheet 1)

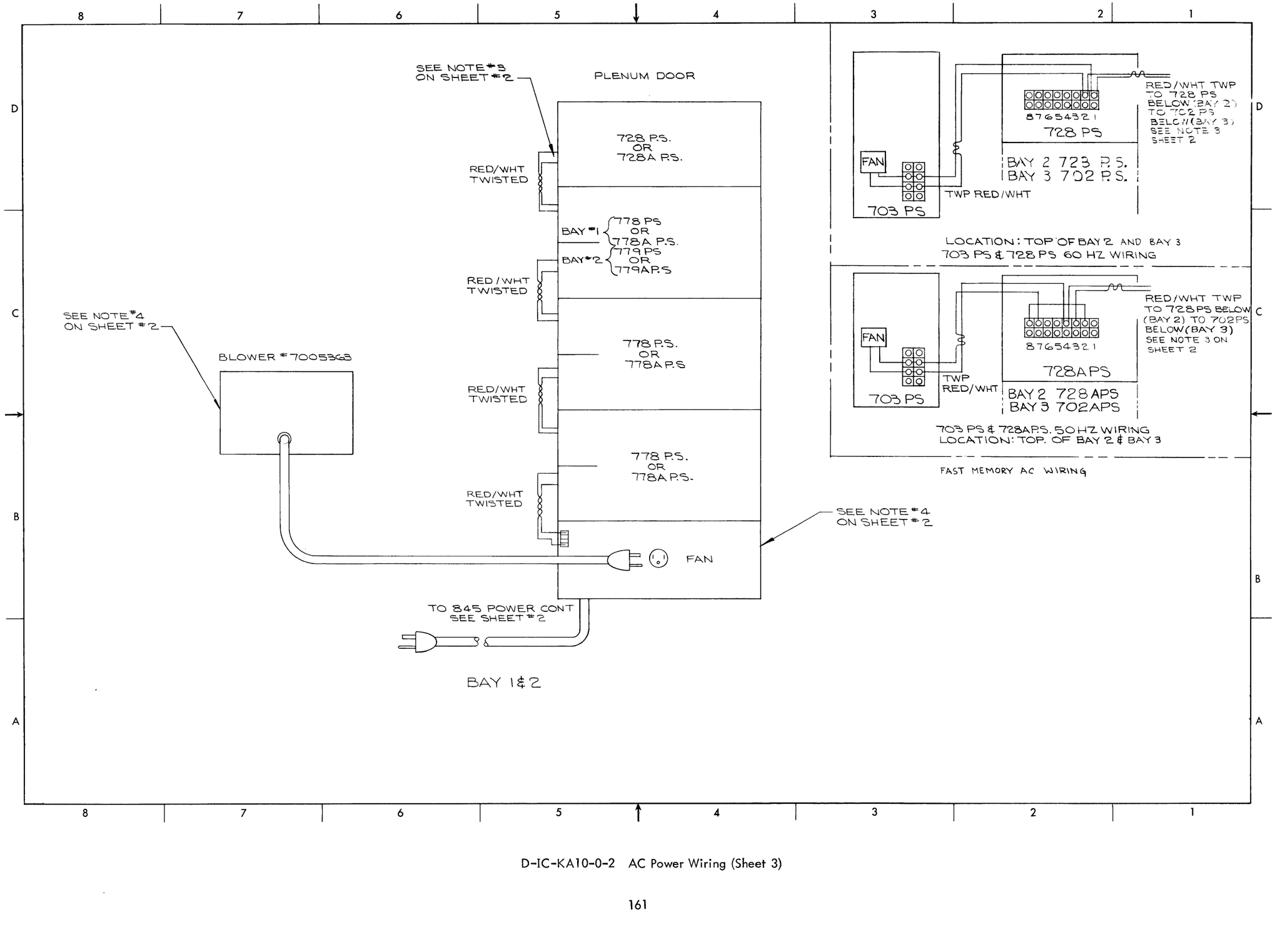
50 CYCLE P.S. JUMPERING		
INPUT VOLTAGE	JUMPER	LINE
195 V	1-5	3&4
220 V	1-6	3&4
235 V	2-8	3&4
112.5 V	2-4 & 3-7	3&4
123.5 V	1-4 & 3-8	3&4

NOTES:

2. FOR 220 VOLT A.C. OPERATION ~~USE TDCA 115 VOLT SOURCE FOR TUSS'S~~, USE TB1A TERMINALS #1 & #3 FOR POWER
3. A.C. WIRING TO POWER SUPPLY TERMINAL STRIP TO BE ON TERMINALS 1 & 2 FOR 60 CYCLE OPERATION & ON 3 & 4 FOR 50 CYCLE OPERATION. REFER TO JUMPERING LEGEND FOR 50 CYCLE JUMPERS
4. FOR 115 VOLT & 220 VOLT CONVERSION OF BLOWERS & FANS REFER TO THEIR ASSEMBLY DRAWINGS. FAN ASSY # D-AD-7005239-0-0 BLOWER ASSY # D-AD-7005238-0-0 FAN ASSY # E-AD-7005239-0-0



D-IC-KA10-0-2 AC Power Wiring (Sheet 2)



D-IC-KA10-0-2 AC Power Wiring (Sheet 3)

K-WL-KA10-0-4 Wire List KA10 (to be supplied)

COMPONENT NAME PART #	VALUE	POL.	FROM PIN	TO PIN	POL.
RES 74-4654	1500Ω ¼W5%		1A31R	1A31V	
			1A32R	1A32V	
			1A33R	1A33V	
			1A34R	1A34V	
			1A35R	1A35V	
			1A36R	1A36V	
			1A37R	1A37V	
			1A38R	1A38V	
			1A39R	1A39V	
			1A40R	1A40V	
			2 A06R	2A06V	
			2A07R	2A07V	
			2A08R	2A08V	
			2A09R	2A09V	
			2A10R	2A10V	
			2A11R	2A11V	
			2A12R	2A12V	
			2A13R	2A13V	
			2A14R	2A14V	
			2A15R	2A15V	
			2A16R	2A16V	
			2A17R	2A17V	
			2A18R	2A18V	
			2A19R	2A19V	
			2A20R	2A20V	
RES 74-4654	1500Ω 1/4W 5%		2A21R	2A21V	

A-CP-KA10-0-CP External Component List For KA10 (Sheet 1)

COMPONENT NAME PART #	VALUE	POL.	FROM PIN	TO PIN	POL.
RES 74-4654	1500Ω ¼W5%		2A22R	2A22V	
			2A23R	2A23V	
			2A24R	2A24V	
			2A26R	2A26V	
			2A27R	2A27V	
			2A28R	2A28V	
			2A29R	2A29V	
			2A30R	2A30V	
			2A31R	2A31V	
			2A32R	2A32V	
			2A33R	2A33V	
			2A34R	2A34V	
			2A35R	2A35V	
			2A36R	2A36V	
			2A37R	2A37V	
			2A38R	2A38V	
			2A39R	2A39V	
			2A40R	2A40V	
			2A41R	2A41V	
			2A42R	2A42V	
			2A43R	2A43V	
			2M36R	2M36V	
			2M37R	2M37V	
			2M38R	2M38V	
			2M39R	2M39V	
RES 74-4654	1500 Ω 1/4W5%		2M40R	2M40V	

A-CP-KA10-0-CP External Component List For KA10 (Sheet 2)

COMPONENT NAME PART#	VALUE	POL.	FROM PIN	TO PIN	POL.
RES.- 74-4654	1500Ω ¼W5%		2M41R	2M41V	
			2M42R	2M42V	
RES 74-4654	1500 Ω 1/4W5%		2M43R	2M43V	
RES	180Ω ¼W5%		2A44L	2A44C	
RES	180Ω 1/4W5%		2M35L	2N35H	
RES	180Ω 1/4W5%		2M43L	2N43N	
RES	180Ω 1/4W5%		1A40L	1A40C	

A-CP-KA10-0-CP External Component List For KA10 (Sheet 3)

COMPONENT NAME	VALUE	POL.	FROM PIN	TO PIN	POL.
RES.	100Ω 1% MF		1A32K	1A31L	
			1A33K	1A32L	
			1A34K	1A33L	
			1A35K	1A34L	
			1A36K	1A35L	
			1A37K	1A36L	
			1A38K	1A37L	
			1A39K	1A38L	
RES.	100 Ω 1%MF		1A40K	1A39L	
NOTE: These Res. are to be wire wraped to the panels at the time the panels are Bussed and before the panels are wired.					

A-CP-KA10-0-CP External Component List For KA10 (Sheet 4)

COMPONENT NAME	VALUE	POL.	FROM PIN	TO PIN	POL.
RES.	100Ω 1% MF		2A07K	2A06L	
			2A08K	2A07L	
			2A09K	2A08L	
			2A10K	2A09L	
			2A11K	2A10L	
			2A12K	2A11L	
			2A13K	2A12L	
			2A14K	2A13L	
			2A15K	2A14L	
			2A16K	2A15L	
			2A17K	2A16L	
			2A18K	2A17L	
			2A19K	2A18L	
			2A20K	2A19L	
			2A21K	2A20L	
			2A22K	2A21L	
			2A23K	2A22L	
			2A24K	2A23L	
			2A26K	2A24L	
			2A27K	2A26L	
			2A28K	2A27L	
			2A29K	2A28L	
			2A30K	2A29L	
RES.	100Ω1%MF		2A31K	2A30L	
NOTE: These Res. are to be wire wraped to the panels at the time the panels are Bussed and before the panels are wired.					

A-CP-KA10-0-CP External Component List For KA10 (Sheet 5)

COMPONENT NAME	VALUE	POL.	FROM PIN	TO PIN	POL.
RES.	100Ω 1% MF		2A32K	2A31L	
			2A33K	2A32L	
			2A34K	2A33L	
			2A35K	2A34L	
			2A36K	2A35L	
			2A37K	2A36L	
			2A38K	2A37L	
			2A39K	2A38L	
			2A40K	2A39L	
			2A41K	2A40L	
			2A42K	2A41L	
			2A43K	2A42L	
			2A44K	2A43L	
			2M29K	2M28L	
			2M30K	2M29L	
			2M31K	2M30L	
			2M32K	2M31L	
			2M33K	2M32L	
			2M34K	2M33L	
			2M35K	2M34L	
			2M37K	2M36L	
			2M38K	2M37L	
RES.	100Ω 1% MF		2M39K	2M38L	
NOTE: these Res. are to be wire wraped to the panels at the time the panels are Bussed and before the panels are wired.					

A-CP-KA10-0-CP External Component List For KA10 (Sheet 6)

COMPONENT NAME	VALUE	POL.	FROM PIN	TO PIN	POL.
RES.	100 Ω 1% MF		2M40K	2M39L	
↕	↕		2M41K	2M40L	
			2M42K	2M41L	
RES.	100 Ω 1% MF		2M43K	2M42L	

NOTE: These Res. are to be wire wraped to the panels at the time the panels are Bussed and before the panels are wired.

A-CP-KA10-0-CP External Component List For KA10 (Sheet 7)

COMPONENT NAME PART#	VALUE	POL.	FROM PIN	TO PIN	POL.
CAP.	3.9 uf @ 10V	-	3B16H	3B16J	+
Cap.	0.027uf@ 100V	-	3D10 H	3D10J	+
Cap.	0.027uf @ 100V	-	3D10R	3D10S	+
Cap. 74-5962	2.2uf @ 20V	-	1P02H	1P02J	+
Cap.	330 uf @ 15V	-	1P01J	1P01C	+
Cap.	180 uf @ 6V	-	3A25R	3A25S	+
Cap.	330 uf @ 15V	-	3A26J	3A26C	+
Cap. 74-5962	2.2 uf @ 20V	-	3A25H	3A25J	+

A-CP-KA10-0-CP External Component List For KA10 (Sheet 8)

COMPONENT NAME PARTS#	VALUE	POL.	FROM PIN	TO PIN	POL.
RES.-74-4644	100Ω ¼W5%		1K21F	1K18C	
Res -74-4644	100Ω ¼W5%		1R27T	1R27C	
Res -74-4644	100Ω ¼W5%		2J20T	2K21C	
Diode-74-4914	D664		2D06L	2D06C	
Diode 74 4914	D664		2H16M	2H16C	
Diode-74-4914	D664		2J20E	2J21C	
Res-74-4644	100Ω ¼W5%		2H41M	2H41C	
Res-74-4644	100Ω ¼W5%		2D14L	2D14C	
Res-74-4644	100Ω ¼W5%		2D33L	2D33C	
Cap-74-4657	.01ufd		3A06F	3A06C	
Cap	.01ufd		3A06T	3A07C	
Cap	.01ufd		3D40D	3D38C	
Cap	.01ufd		3D40E	3D39C	
Cap	.01ufd		3D40F	3D40C	
Cap-74-4657	.01ufd		3D40H	3D41C	
Res-74-4644	100Ω ¼W5%		1K21T	1K21C	
Res	100Ω ¼W5%		1C14J	1C14C	
Res	100Ω ¼W5%		1B27U	1C27C	
Res	100Ω ¼W5%		1S34T	1T34C	
Res	100Ω ¼W5%		1R37L	1S37C	
Res	100Ω ¼W5%		1R36J	1R36C	
Res 74 4644	100Ω ¼W5%		1L22L	1L22C	

A-CP-KA10-0-CP External Component List For KA10 (Sheet 9)

COMPONENT NAME PART#	VALUE	POL.	FROM PIN	TO PIN	POL.
RES 74-4644	100Ω 1/4W5%		2J12T	2J12C	
	100Ω 1/4W5%		2J22T	2K22C	
	100Ω 1/4W5%		2E13V	2F13C	
	100Ω 1/4W5%		2E26V	2F25C	
	100Ω 1/4W5%		2E38V	2F39C	
	100Ω 1/4W5%		1J22R	1J23M	
	100Ω 1/4W5%		3F03E	3F03C	
RES 74-4644	100Ω 1/4W5%		3F03H	3F03F	
CAP 74-4657	.01MF		3A06U	3B06C	

A-CP-KA10-0-CP External Component List For KA10 (Sheet 10)

SIGNAL NAME	FROM PIN	TO PIN	COLOR	REMARKS
TTY SOCKET B	3D40F	B of	WECO 493A	SOCKET
TTY SOCKET G	3D40D	G of	" "	"
TTY SOCKET R	3D40E	R of	" "	"
TTY SOCKET Y	3D40H	Y of	" "	"

A-WL-KA10-0-GW General Wiring Sheet for TTY Socket Wiring of KA10

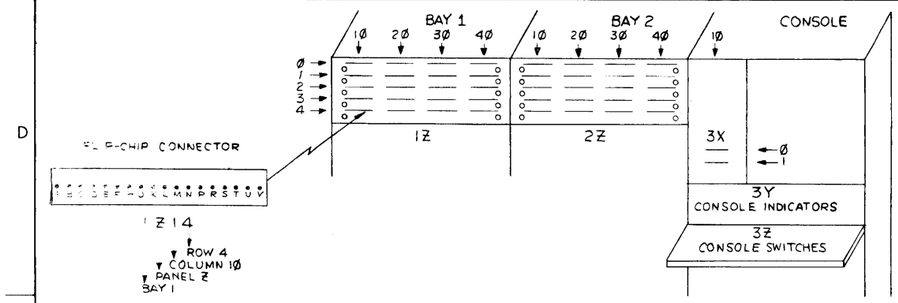
FROM	TO	D	E	F	H	J	K	L	M	N	P	R	S	T	U	V
G799 1H41	2D02 G799	ARRT FM AD (0)	ARRT FM MQ (0)	GND	ARRT FM AD (1)	GND	ARRT FM MQ (1)	GND	ARLT FM FM (1)	GND	AR0-5 FM SCAD 3-8(J)	GND	AR1-8 FM AR0 (J)	AR1-8 FM SCAD 1-8(J)	GND	ARRT FM PC (J) B
1H42	2C03	ARLT FM IOB (1)	ARRT FM IOB (1)	GND	ARLT FM AD (0)	GND	ARLT FM MQ (0)	GND	ARLT FM AD (1)	GND	ARLT FM MQ (1)	GND	ARLT FM FLAGS(J) A	ARRT FM PC (J) A	GND	ARLT FM FLAGS(J) B
1H43	2C02	ARRT SH RT A	ARRT SH RT B	GND	ARRT SH LT A	GND	ARRT SH LT B	GND	ARRT CLR	GND	ARRT FM FM (1)	GND	ARLT FM IR (1)	ARLT FM DS (1)	GND	ARRT FM DS (1)
1H44	2B03	ARLT CLR	ARLT FM ARRT (J) B	GND	ARLT SH LT B	GND	ARLT SH RT B	GND	ARLT FM ARRT (J) A	GND	ARLT SH LT A	GND	ARLT SH RT A	ARRT FM ARLT (J) A	GND	ARRT FM ARLT (J) B
1K41	2H04	MC MEM BUS FM AR(1) A	MC MEM BUS FM AR(1) B	GND	MC MEM BUS FM AR(1) C	GND	BR 1-8 CLR	GND	BR 1-8 SET	GND	BRLT FM AR(0)	GND	BRLT FM AR(1)	BRRT FM AR(0)	GND	BRRT FM AR (1)
1L41	2J04	MQ CLR	MQ SH LT A	GND	MQ SH LT B	GND	MQ SH RT A	GND	MQ SH RT B	GND	MQ FM AD(J) A	GND	MQ FM AD(J) B	MQ SH LT C	GND	MQ SH RT C
1L42	2J03	MQ SH LT D	MQ SH RT D	GND	MQ FM AD(J) C	GND	MQ FM AD(J) D	GND	FMT 3	GND	IR LT CLR	GND	IR RT CLR	IR RDI SETUP	GND	—
1L43	2J02	ET0F	ST 1	GND	PCLT FM MA (J)	GND	PCRT FM MA (J)	GND	PCLT +1	GND	PCRT +1	GND	MA FM PICH (1)	—	GND	—
1M43	2M02	MA CLR	MA FM PC(J) A	GND	MA FM PC(J) B	GND	MA FM AR(J) A	GND	MA FM AR(J) B	GND	MA FM AS(J) A	GND	MA FM AS(J) B	IT0	GND	MAI IGN PAR PULSE
1N42	2N03	KNT 2	KEY RDI DONE	GND	MR PWR CLR	GND	MI LOAD A	GND	MI LOAD B	GND	MI LOAD C	GND	MI LOAD D	KT2	GND	KT1
1P43	2P02	FT 9	MAI CMC RD RS	GND	EX CLR	GND	EX SET	GND	PB CLR	GND	PI RESET B	GND	KNT 1	KNT 3	GND	*IR UUO IND
1S42	2S03	MR START	ST 3	GND	PI OK CLRS PIH	GND	PIH FM PICH RQ	GND	PIR FM IOB (1)	GND	PIR STB	GND	PI RESET	PIO CLR	GND	PIO SET
1T43 G799	2T02 G799	KT4	MR CLR	GND	KT0A	GND	MC NON EX MEM	GND	MC ILLEG ADR	GND	MC PAR ERR	GND	MCRST 1	KT3	GND	—
3E01 G796	2T42 G796	KEY DONE	KT0	GND	KST 1	GND	KST 2	GND	PI CONO SET	GND	CPA MEM PROT FLAG SET	GND	CPA NON EX MEM SET	CPA PAR ERR SET	CPA PDL OV SET	GND
G796 1A43	G796 2A03	—	AR 1 (0)	AR 1 (1)	AR 2 (1)	AR 3 (1)	AR 4 (1)	AR 5 (1)	AR 6 (1)	AR 7 (1)	AR 8 (1)	AR 9 (1)	AR 10 (1)	AR 11 (1)	—	GND
1B41	2B04	AD CRY 36(1)	AD BR+ EN (0)	AD BR-EN (0)	—	—	—	—	—	AD 09 (1)	AD CLR A	AR 0 CLR U	AR 0 SET U	AR 0 CLR	AR 0 SET	GND
1B43	2B02	SCAD 1 (0)	SCAD 1 (1)	SCAD 2 (0)	SCAD 2 (1)	SCAD 3 (0)	SCAD 3 (1)	SCAD 4 (0)	SCAD 4 (1)	SCAD 5 (0)	SCAD 5 (1)	SCAD 6 (0)	SCAD 6 (1)	SCAD 7 (0)	SCAD 7 (1)	GND
1C43	2C04	SCAD 8 (0)	SCAD 8 (1)	AD CRY 0 (1)	AD CRY 1 (1)	AD CRY 0 (0)	AD CRY 1 (0)	AD 9 (0)	AD 0-7 = 0	AD 8-9 = 0	AD 10-17 = 0	AD 18-19 = 0	AD 20-27 = 0	AD 28-35 = 0	MQ 9-35 = 0	GND
1D43	2A02	AD AR+ EN CLR	AD AR+ EN SET	AD AR-EN CLR	AD AR-EN SET	AD BR+ EN CLR	AD BR+ EN SET	AD BR-EN CLR	AD BR-EN SET	AD -1 LH(0)	AD +1 LH (1)	AD CRY INS (0)	AD CRY 36(0)	AD 0 (1)	AD 0 (0)	GND
1D41	2D04	MQ 8 (0)	MQ 35(0)	MQ 35(1)	MQ 34 (0)	MQ 34(1)	ARMQ PRESERVE SIGN	ARMQ MULV ASHXV FP	ARMQ AR35 FM MQ 0 EN	ARMQ FP SW EN	AD AR+ EN(1)	AD AR-EN(1)	AD BR+ EN(1)	AD BR-EN(1)	GND	
1D42	2D03	AR FXU(0)	AR FXU (1)	AR DCK (0)	AR DCK (1)	AR OV FLAG (0)	AR OV FLAG (1)	AR FOV (0)	AR FOV(1)	AR CRY 0 FLAG (0)	AR CRY 0 FLAG (1)	AR CRY 1 FLAG (0)	AR CRY 1 FLAG (1)	BYF 6 (0)	BYF 6 (1)	GND
1F41	2F04	BR 35 (1)	EX USER(0)	EX USER(1)	EX IOT USER (0)	EX IOT USER (1)	ARI DFN CLR	ARI DFN SET	AR 8 (0)	AR 9 (0)	IR ROT	IR ROTC	ARMQ FDV NORM	IR ASHC	IR ASHC	GND
1F42	2F03	BR 8 (1)	BR 11(0)	BR11(1)	BR 12 (0)	BR 12(1)	BR18(0)	BR 18(1)	BR 28(1)	BR 29(1)	BR 30(1)	BR 31(1)	BR 32(1)	BR 33(1)	BR 34(1)	GND
1F43	2F02	BR 0(0)	BR 0 (1)	BR 1 (0)	BR 1(1)	BR 2(0)	BR 2 (1)	BR 3 (0)	BR 3(1)	BR 4(0)	BR 4(1)	BR 5 (1)	BR 6 (0)	BR 6 (1)	BR 7 (1)	GND
1N43	2H02	ARMQ LRC VMUL	ARMQ FP SH EN	ARMQ ASHC VMUL LAST	ARMQ BYTE MASK	DSF 2 (1)	IR-7 (0)	IR7 (1)	IR 8 (0)	IR 8(1)	IR 9 (0)	IR 9 (1)	IR 10(0)	IR 10(1)	IR 11 (0)	GND
1P44	2H03	IR 0 (1)	IR 0 (0)	IR 1 (0)	IR 1 (1)	IR 2(0)	IR 2(1)	IR 3 (0)	IR 3 (1)	IR 4 (0)	IR 4(1)	IR 5(0)	IR 5 (1)	IR 6 (0)	IR 6(1)	GND
1M41	2M04	IR 11 (1)	IR 12 (0)	IR 12(1)	IR 13 (0)	IR 13(1)	IR 14(0)	IR 15 (0)	IR 16(0)	IR 17 (0)	IR LT EN(1)	IR RT EN (1)	IR UUO	IR 1XX	E UUOF(1)	GND
1M42	2M03	SC STOP SW	SC STOP(0)	FMA AC EN	FMA AC2 EN	FMA MA EN	FMA XR EN	FMA FM AR (J)	AD 17 (1)	AD 17 (0)	MA TRAP OFFSET	EX NON REL UUO	JFFO SWAP	—	AR 18(1)	GND
1N41	2N04	KEY PROG STOP	KEY PI INH (0)	E XCT F(0)	EX REL A	EX REL A	EX REL B	EX REL B	MA18-31 = 0	MA18-31 = 0	MAI FMA SEL (1)	MAI FMA SEL (0)	MC REQ CYC	MC RD(1)	MC WR (1)	GND
1P42	2P03	PARILLADR	PARILLADR	KEY START (1)	IR PUSH	IR PUSHJ	IR POPS	IR JRST	PI RQ	PI IRQ	PI OV (1)	PB PAR(0)	PB PAR(1)	MQ 0 B(1)	—	GND
1R41	2R04	KEY RIM(0)	MI PROG DIS SW	AS = ELA	AS = FMA	KEY F1(1)	RUN (1)	RUN(0)	KEY CONT(1)	PI CYC (1)	KEY RDI (1)	PN PAR ODD	PN PAR EVEN	PI DATA I/O	KEY NEXT	GND
1S41	2S04	MC FM EN	PI SEL	KEY RIM(1)	KEY ITO EN	MC IGNORE PARITY (1)	—	BIO PI SEL	IOT DATAO	IOT DATAI	KEY CONT(0)	IOT BLK	—	MC STOP(0)	KEY EXECUTE (1)	GND
3C01	2T39	IOB 0	IOB 1	IOB 2	IOB 3	IOB 4	IOB 5	IOB 6	IOB 7	IOB 8	IOB 9	IOB 10	IOB 11	IOB 12	IOB 13	GND
3C02	2T38	IOB 14	IOB 15	IOB 16	IOB 17	IOB 18	IOB 19	IOB 20	IOB 21	IOB 22	IOB 23	IOB 24	IOB 25	IOB 26	IOB 27	GND
3C03 G796	2T37 G796	RUN (1)	RUN (0)	IOB RDI DATA	KEY CONT (1)	KEY CONT (0)	KEY SING INST	IOB 28	IOB 29	IOB 30	IOB 31	IOB 32	IOB 33	IOB 34	IOB 35	GND

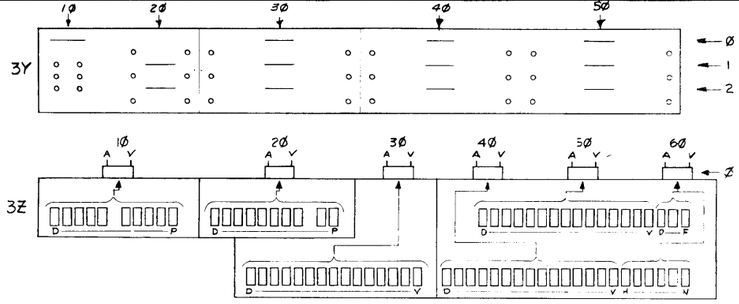
NOTES: 1.*

NAME	ORIGIN
IR UUO IND	1P26F
MC PAR STOP IND	1S18U
MC STOP IND	1T16U

CABLE PINS

FROM	TO	D	E	F	H	J	K	L	M	N	P	R	S	T	U	V
3D01 (3792)	2S40 (9756)	IOB Ø	IOB 1	IOB 2	IOB 3	IOB 4	IOB 5	IOB 6	IOB 7	IOB 8	IOB 9	IOB 10	IOB 11	IOB 12	IOB 13	GND
3D02	2S39	IOB 14	IOB 15	IOB 16	IOB 17	IOB 18	IOB 19	IOB 20	IOB 21	IOB 22	IOB 23	IOB 24	IOB 25	IOB 26	IOB 27	GND
3D03	2S38	KEY SING INST	KEY START(1)	KEY EXECUTE (1)	KEY SYNC OPS	KT 1 EN	IOB STATUS A	IOB 28	IOB 29	IOB 30	IOB 31	IOB 32	IOB 33	IOB 34	IOB 35	GND
3F01	2S42	IR 3 (Ø)	IR 3 (1)	IR 4 (Ø)	IR 4 (1)	IR 5 (Ø)	IR 5 (1)	IR 6 (Ø)	IR 6 (1)	IR 7 (Ø) (1)	IR 7 (1)	IR 8 (Ø)	IR 8 (1)	IR 9 (Ø)	IR 9 (1)	GND
3F02	2S41	IR 10 (Ø)	IR 10 (1)	IR 11 (Ø)	IR 11 (1)	IR 12 (Ø)	IR 12 (1)	IOB FM AR	AR FOV (1)	AR OV FLAG (1)	IOT DATAI	IOT DATAO	PI STATUS A	PI STATUS B	PI ACT (1)	GND
3E02	2T41	PIH 1 (1)	PIH 2 (1)	PIH 3 (1)	PIH 4 (1)	PIH 5 (1)	PIH 6 (1)	PIH 7 (1)	PIO 1 (1)	PIO 2 (1)	PIO 3 (1)	PIO 4 (1)	PIO 5 (1)	PIO 6 (1)	PIO 7 (1)	GND
3E03	2T40	KEY F1 (1)	KEY SYNC RQ (1)	KEY SYNC (1)	KEY MEM REF	KEY NEXT	KEY RDI (1)	IOB PI 1	IOB PI 2	IOB PI 3	IOB PI 4	IOB PI 5	IOB PI 6	IOB PI 7	IOT BLK	GND
3E04	1S43	KEY ADR BRK	KEY ADR INST	KEY ADR RD	KEY ADR STOP	KEY ADR STOP	KEY ADR WR	KEY AS STROBE EN	KEY SING CYCLE	KEY DEP/DEP NXT/EXE	KEY DEP NXT	KEY EX NXT	KEY NXM STOP	KEY NXM STOP	KEY PAR STOP	GND
3E05	1S44	MR PWR CLR ENB	MR PWR CLR ENB	IOT CONO SET	IOT CONO CLR	IOT DATAO SET	IOT DATAO CLR	IOB DATAI A	CPA PWR FAIL (Ø)	IOB DR SPLIT	——	EX IOT USER (1)	CPA PWR DLY	BIO CPA SEL	BIO PI SEL	GND
3E06	1L44	IOT BLK	IOT CONI	IOT CONO	IOT CONSO	IOT CONSK	IOT CONSX	IOT CONSZ	IOT T2	CPA CONO SET	IOT GO (1)	IR IOT	KEY AT INH	MA TRAP OFFSET	MC ADR BRK SET	GND
1P01 (3796)	2P04 (3796)	IOB 23	IOB 24	IOB 25	IOB 26	IOB 29	IOB 32	M1 PROG (Ø)	M1 PROG (1)	-MR PWR CLR ENB	—	—	—	—		GND
1R02 (3799)	2R03 (3799)	MAI CMC ADR ACK	MC BUS WIRES	GND	MC PARITY PULSE	GND	KT 3A	GND	*MC PAR STOP IND	GND	*MC STOP IND	GND	—	—	GND	PI CONO SET
W031 3F03	W031 1R43	IOT T3B	IOT T4	GND	IOT T5	GND	—	GND	—	GND	—	GND	KST 2	MR PWR CLR R	GND	MR START R





CABLE PINS

FROM	CABLE	TO	D	ORIGIN	E	ORIGIN	F	ORIGIN	H	ORIGIN	J	ORIGIN	K	ORIGIN	L	ORIGIN	M	ORIGIN	N	ORIGIN	P	ORIGIN	R	ORIGIN	S	ORIGIN	T	ORIGIN	U	ORIGIN	V	ORIGIN
W012		W250																													GND	
1B04		1210	SC0 IND	1C31F	SC1 IND	1C31R	SC2 IND	1C33F	SC3 IND	1C33R	SC4 IND	1C35F	SC5 IND	1C35R	SC6 IND	1C37F	SC7 IND	1C37R	SC8 IND	1C39F	SC STOP IND	1C15F	LB BYTE LOAD	1B03T	DB BYTE DEP	1B09D						
3B06		1220	CPA PWR FAIL (1)	3F40J	CPA ADR BREAKAT(1)	3F40T	CPA PAR ERR (1)	3F41J	CPA PAR ENB (1)	3F41T	CPA POL OV (1)	3F42J	CPA MEM PROT FLAG(1)	3F42T	CPA NON EX MEM (1)	3F43J	CPA CLK EN (1)	3F43T	CPA CLK FLAG (1)	3F44J	PTP HOLE 0 (1)	3A14F	PTP HOLE 7 (1)	3A14M	PTP HOLE 6 (1)	3A14T						
3B05		1230	PTP HOLE 5 (1)	3A15F	PTP HOLE 4 (1)	3A15M	PTP HOLE 3 (1)	3A15T	PTP HOLE 2 (1)	3A16F	PTP HOLE 1 (1)	3A16M	PTP NO TAPE	3F09L	PTP BIN(1)	3A19P	PTP DONE (1)	3A20L	PTP DFA 33 (1)	3A21L	PTP DFA 36 (1)	3A22M	PTP DFA 35 (1)	3A22T								
1C09		1240	BLTFI IND	1J06E	MPF1 IND	1J11F	MPF2 IND	1J11E	MSF1 IND	1J06F	BYF4 IND	1B15R	BYF5 IND	1C12F	BYF6 IND	1C15R	DSF1 IND	1F11F	DSF7 IND	1F11E	FAF1 IND	1B15F	FDF1 IND	1F18R	FDF3 IND	1F18F						
1A04		1211	SCAD0 IND	1A31R	SCAD1 IND	1A32E	SCAD2 IND	1A33R	SCAD3 IND	1A34R	SCAD4 IND	1A35R	SCAD5 IND	1A36R	SCAD6 IND	1A37R	SCAD7 IND	1A38R	SCAD8 IND	1A39R	NR SM RT COND IND	1E24F	NR NORMAL IND	1E25F	NR ROUND	1C11T						
3B04		1221	CPA FOV EN (1)	3F44T	CPA AB OVEN(1)	3E43J	CPA PIA 33 (1)	3E43T	CPA PIA 36 (1)	3E44J	CPA PIA 34 (1)	3E44T	-		TTY TEST FLAG (1)	3E41F	TTY TTI ACTIVE (1)	3C40T	TTY TTO ACTIVE (1)	3C44T	TTY TTI 8 (Ø)	3C37N	TTY TTI 7 (Ø)	3C37F	TTY TTI 6 (Ø)	3C37E						
3B03		1231	TTY TTI 5 (Ø)	3C38N	TTY TTI 4 (Ø)	3C38F	TTY TTI 3 (Ø)	2C38E	TTY TTI 2 (Ø)	3C39N	TTY TTI 1 (Ø)	3C39F	TTY TTI BUSY (1)	3D36L	TTY TTI FLAG (1)	3D37L	TTY TTO BUSY (1)	3D38L	TTY TTO FLAG (1)	3D39L	TTY PIA 33 (1)	3E40F	TTY PIA 34 (1)	3E40M	TTY PIA 35 (1)	3E40T						
1A44		1241	NRF1 IND	1C12E	KEY RTM(1)	2R28T	IOT F1 IND	1B30F	IOT GO IND	1R30R	-	-	AR OV FLAG IND	1K16F	AR CRY 0 FLAG IND	1K16R	AR CRY 1 FLAG IND	1K20F	AR FOV IND	1K20R	AR FXU IND	1K23F	AR DCK IND	1K23E	AR OV COND	1F25F						
1D44		1212	FE 0 IND	1D31F	FE 1 IND	1D31R	FE 2 IND	1D33F	FE 3 IND	1D33R	FE 4 IND	1D35F	FE 5 IND	1D35R	FE 6 IND	1D37F	FE 7 IND	1D37R	FE 8 IND	1C39R	SCAD DATA 0 IND	1A25F	SCAD DATA 1 IND	1A25R	SCAD SC COMP IND	1A26F						
1J44		1222	SCAD 1 EN IND	1A26R	SCAD BE EN IND	1B26F	SCAD AR &-11 EN IND	1B29R	SCAD 26Ø EN IND	1B25F	SCAD 33 EN IND	1B25R	AS=RLA	2N37L	AS=FMA	2P26E	EX ILL OP IND	1P22R	EX PI SYNC IND	1P16F	EX MODE SYNC IND	1P25R	EX IOT USER IND	1P25F	EX REL A	1S34H						
3A02		1232	PTR ENB(1)	3A37J	PTR PWR (1)	3A37F	PTR TAPE(1)	3A40T	PTR BIN(1)	3B31D	PTR BUSY (1)	3C31L	PTR DONE (1)	3C32L	PTR CNT Ø (1)	3A39J	PTR CNT 1 (1)	3A39T	PTR CNT 2 (1)	3A40J	PTR PIA 33 (1)	3C33F	PTR PIA 36 (1)	3C33M	PTR PIA 35 (1)	3C33T						
1E44		1292	-	-	AD AR+EN(1)	*1D42R	AD AR-EN(1)	*1D42S	AD BR+EN(1)	*1D42T	AD BR-EN(1)	*1D42U	AD CRY 36 IND	1E33R	AD CRY INS IND	1E33F	AD+1 LH IND	1E33R	AD-1 LH IND	1E33F	AD MD+ IND	1F26F	AD MD- IND	1F27F	AD COND IND	1F25F						
3A03		1213	PTR Ø (1)	3B33D	PTR 1 (1)	3B35D	PTR 2 (1)	3B37D	PTR 3 (1)	3B39D	PTR 4 (1)	3B43D	PTR 5 (1)	3B44D	PTR 6 (1)	3B33M	PTR 7 (1)	3B35H	PTR 8 (1)	3B37H	PTR 9 (1)	3B39H	PTR 10 (1)	3B43H	PTR 11 (1)	3B44H						
3A04		1223	PTR 12(1)	3B39U	PTR 13(1)	3B35U	PTR 14(1)	3B37U	PTR 15(1)	3B39U	PTR 16(1)	3B43U	PTR 17(1)	3B44U	PTR 18(1)	3B32D	PTR 19 (1)	3B34D	PTR 20(1)	3B36D	PTR 21(1)	3B38D	PTR 22 (1)	3B42D	PTR 23(1)	3B42T						
3A05		1233	PTR 24(1)	3B32U	PTR 25(1)	3B34U	PTR 26(1)	3B36U	PTR 27(1)	3B38U	PTR 28(1)	3B41J	PTR 29 (1)	3B41P	PTR 30 (1)	9B33U	PTR 31(1)	3B34U	PTR 32	3B36U	PTR 33 (1)	3B38U	PTR 34 (1)	3B40J	PTR 35 (1)	3B40T						
1M44		1243	-	-	FCE		FCE PSE		FAC INH		FACE		FCC ACLT		FCC ACBT		SCE		SAC INH		SAC INH		SAC+BE							
2B04		1214	IOB Ø	2C12D	IOB 1	2C12F	IOB 2	2C12J	IOB 3	2C12L	IOB 4	2C12N	IOB 5	3C12R	IOB 6	3C12T	IOB 7	2D13D	IOB 8	3D13F	IOB 9	3D13J	IOB 10	3D13L	IOB 11	3D13N						
2B03		1224	IOB 12	3D13R	IOB 13	3D13T	IOB 14	3C13D	IOB 15	3C13F	IOB 16	3C13J	IOB 17	3C13L	IOB 18	3E09D	IOB 19	3C13N	IOB 20	3C13R	IOB 21	3C13T	IOB 22	3D14D	IOB 23	3C14P						
2B02		1234	IOB 24	3C14J	IOB 25	3C14L	IOB 26	3C14N	IOB 27	3C14R	IOB 28	3C14T	IOB 29	3D14D	IOB 30	3D14F	IOB 31	3D14J	IOB 32	3D14L	IOB 33	3D14N	IOB 34	3D14R	IOB 35	3D14T						
1M99		1244	IFQ IND	1M05R	AF2 IND	1P09F	AF1 IND	1M04A	AF2 IND	1M04R	AF6 IND	1M05F	E UUOF IND	1M09F	E ICT F IND	1M03R	E LONG	1M07J	EF0 LONG	1N13L	SF1 IND	1E19F	SF6 IND	1E19E	SF8 IND	1S22F						
2B01		2210	AR3 IND	2C07F	AR1 IND	2C07E	AR2 IND	2C09F	AR3 IND	2C09E	AR4 IND	2C11F	AR5 IND	2C11E	AR6 IND	2C13E	AR0 IND	2C15F	AR7 IND	2C13E	AR0 IND	2C15F	AR9 IND	2C15E	AR10 IND	2C17E	AR11 IND	3F17R				
2C02		2220	AR11 IND	2C19F	AR13 IND	2C19E	AR14 IND	2C21F	AR15 IND	2C21E	AR16 IND	2C23F	AR17 IND	2C23E	AR18 IND	2C25R	AR19 IND	2C25F	AR20 IND	2C28F	AR21 IND	2C28E	AR22 IND	2C28F	AR23 IND	2C30R						
2C04		2230	AR24 IND	2C32F	AR25 IND	2C32E	AR26 IND	2C34F	AR27 IND	2C34E	AR28 IND	2C36F	AR29 IND	2C36E	AR30 IND	2C38F	AR31 IND	2C38E	AR32 IND	2C40F	AR33 IND	2C40E	AR34 IND	2C40E	AR35 IND	2C40E						
1B99		2240	PI OV IND	1P69R	PI CYC IND	1P16R	MC RQ IND	1T16R	MC RD IND	1T16M	MC WE IND	1T16L	MC RQ CYC	1T21F	MC SPLIT CYC SYNC IND	1S38R	MC MM EN	13/1A	MAR, MAA SEL IND	1S22R	FMA MC IND	1T38E	FMA AC IND	1T39F	FMA XR IND	1T39E						
2E01		2211	BR0 IND	2F07F	BR1 IND	2F07E	BR2 IND	2F09F	BR3 IND	2F09E	BR4 IND	2F11F	BR5 IND	2F11E	BR6 IND	2F13F	BR7 IND	2F13E	BR8 IND	2F15F	BR9 IND	2F15E	BR10 IND	2F17F	BR11 IND	2F17E						
2L23		2221	BR12 IND	2F19F	BR13 IND	2F19E	BR14 IND	2F21F	BR15 IND	2F21E	BR16 IND	2F23F	BR17 IND	2F23E	BR18 IND	2F26F	BR19 IND	2F26E	BR20 IND	2F28F	BR21 IND	2F28E	BR22 IND	2F30F	BR23 IND	2F30E						
2F01		2231	BR 24 IND	2F32F	BR 25 IND	2F32E	BR 26 IND	2F34F	BR 27 IND	2F34E	BR 28 IND	2F36F	BR 29 IND	2F36E	BR 30 IND	2F38F	BR 31 IND	2F38E	BR 32 IND	2F40F	BR 33 IND	2F40E	BR 34 IND	2F42F	BR 35 IND	2F42E						
3B07		2241	KEY F1 (1)	3E03D	KEY SYNC EQ (1)	*3E03E	KEY SYNC (1)	*3E03F	KEY RESET(1)	2B11M	KEY EXAM'(1)	3B10F	KEY EX NXT(1)	3B10M	KEY DEP(1)	3D10T	KEY DEP NXT (1)	3B11F	KEY ADI(1)	3B12M	KEY START(1)	3B12F	KEY EXE(1)	3B11T	KEY CONT(1)	3B12T						
2M03		2212	AD0 IND	2A07R	AD1 IND	2A08R	AD2 IND	2A09R	AD3 IND	2A10R	AD4 IND	2A11R	AD5 IND	2A12R	AD6 IND	2A13R	AD7 IND	2A14R	AD8 IND	2A15R	AD9 IND	2A16R	AD10 IND	2A17R	AD11 IND	2A18R						
2B01		2222	AD12 IND	2A19R	AD13 IND	2A20R	AD14 IND	2A21R	AD15 IND	2A22R	AD16 IND	2A23R	AD17 IND	2A24R	AD18 IND	2A25R	AD19 IND	2A27R	AD20 IND	2A28R	AD21 IND	2A29E	AD22 IND	2A30E	AD23 IND	2A31E						
2C01		2232	AD 24 IND	2A32E	AD 25 IND	2A33R	AD 26 IND	2A34R	AD 27 IND	2A35R	AD 28 IND	2A35E	AD 29 IND	2A36R	AD 30 IND	2A37E	AD 31 IND	2A38R	AD 32 IND	2A39R	AD 33 IND	2A40E	AD 34 IND	2A41R	AD 35 IND	2A42R						
2N01		2242	—	—	IR UUC IND	*2P03V	IR LT EN (1)	IM39E	IR RT EN (1)	IM39R	RL 16 (1)	2N38F	RL 19 (1)	2N37L	RL 08 (1)	2N36T	RL 21 (1)	2N36M	RL 22 (1)	2N34M	RL 24 (1)	2N40T	RL 26 (1)	3N42F	RL 25 (1)	2N42M						
2M01		2213	MQ0 IND	2M07R	MQ1 IND	2M07E	MQ2 IND	2M09F	MQ3 IND	2M09R	MQ4 IND	2M11F	MQ5 IND	2M11R	MQ6 IND	2M13F	MQ7 IND	2M13R	MQ8 IND	2M15F	MQ9 IND	2M15E	MQ10 IND	2M17F	MQ11 IND	2M17R						
2J01		2223	MQ12 IND	2M19F	MQ13 IND	2M19E	MQ14 IND	2M21F	MQ15 IND	2M21E	MQ16 IND	2M23F	MQ17 IND	2M23E	MQ18 IND	2M26F	MQ19 IND	2M26E	MQ20 IND	2M26F	MQ21 IND	2M28F	MQ22 IND	2M28E	MQ23 IND	2M28E						
2M31		2233	MQ24 IND	2M32F	MQ25 IND	2M32E	MQ26 IND	2M34F	MQ27 IND	2M34E	MQ28 IND	2M36F	MQ29 IND	2M36E	MQ30 IND	2M38F	MQ31 IND	2M38E	MQ32 IND	2M40F	MQ33 IND	2M40E	MQ34 IND	2M42F	MQ35 IND	2M42E						
2M02		2243	FMA 32	2M40E	FMA 33	2M40T	FMA 34	2M39M	FMA 35	2M38M	RLA 18 IND	2M36R	RLA 19 IND	2M37R	RLA 20 IND	2M36R	RLA 21 IND	2M39R	RLA 22 IND	2M40R	RLA 23 IND	2M41R	RLA 24 IND	2M42R	RLA 25 IND	2M43E						
2E01		2214	PB0 IND	2P07H	PB1 IND	2P07L	PB2 IND	2P09E	PB3 IND	2P09U	PB4 IND	2P83H	PB5 IND	2P89L	PB6 IND	2P89R	PB7 IND	1P89U	PB8 IND	2P11H	PB9 IND	2P11L	PB10 IND	2P11E	PB11 IND	3P11U						
2J01		3J24	PB12 IND	2P13H	PB13 IND	2P13L	PB19 IND	2P19R	PB15 IND	2P15U	PB16 IND	2P15H	PB17 IND	2P15L	PB18 IND	2P15R	PB19 IND	2P15U	PB20 IND	2P17H	PB21 IND	2P17L	PB22 IND	2P17E	PB23 IND	2P17U						
2N01	W116	2P24	PB24 IND	2P19H	PB25 IND	2P19L	PB26 IND	2P19E	PB27 IND	2P19U	PB28 IND	2P21H	PB29 IND	2P21L	PB30 IND	2P21R	PB31 IND	2P21U	PB32 IND	2P23H	PB33 IND	2P23L	PB34 IND	2P23E	PB35 IND	2P23U						
	N058																												GND	

NOTES: 1. * THIS IS A PIN ON THE IBC CABLE (ORIGIN OF SIGNAL IN ANOTHER BAY)

D-IC-KA10-0-ICSC1 Indicator and Console Switch Connections

CABLE PINS

FROM	LENGTH	TO	D	ORIGIN	E	ORIGIN	F	ORIGIN	H	ORIGIN
2PØ1 W012		2244 W25Ø	MC IGNORE PARITY (1)	*2SØ4J	PB PAR (1)	1R35N	PN PAR ODD IND	2P15F	MC PAR STOP IND	2RØ5M
2P37		3Y1Ø	RUN IND	2R28F	PI ACT(1)	2T19T	PWR ON IND	2P31F	MC STOP IND	2RØ5P
3EØ7		3Y3Ø	—	—	IOB PI 1	3E17D	IOB PI 2	3E17F	IOB PI 3	3E13J
2P38		3Y4Ø	MI PROG (Ø)	*2PØ4L	MI PROG (1)	*2PØ4M	—	—	—	—
2P39		3Y5Ø	PC 24 IND	2J32F	PC 25 IND	2J32R	PC 26 IND	2J34F	PC 27 IND	2J34R
2P4Ø		3Y21	PIH 1 IND	2SØ7F	PIH 2 IND	2SØ7R	PIH 3 IND	2SØ9F	PIH 4 IND	2SØ9R
2P41		3Y31	IR Ø IND	2JØ7F	IR 1 IND	2JØ7R	IR 2 IND	2JØ9F	IR 3 IND	2JØ9R
2P42		3Y41	IR 12 IND	2J19F	IR 13 IND	2J19R	IR 14 IND	2J21F	IR 15 IND	2J21R
2P43		3Y51	MA 24 IND	2L32F	MA 25 IND	2L32R	MA 26 IND	2L34F	MA 27 IND	2L34R
2P44		3Y22	PIO 1 (1)	2T13J	PIO 2 (1)	2T13T	PIO 3 (1)	2T15J	PIO 4 (1)	2T15T
2R41		3Y32	MI Ø IND	2MØ7H	MI 1 IND	2MØ7L	MI 2 IND	2MØ7R	MI 3 IND	2MØ7U
2R42		3Y42	MI 12 IND	2M13H	MI 13 IND	2M13L	MI 14 IND	2M13R	MI 15 IND	2M13U
2R43 W012		3Y52 W25Ø	MI 24 IND	2M19H	MI 25 IND	2M19L	MI 26 IND	2M19R	MI 27 IND	2M19U
2R4Ø W033		3X1Ø W032	SC STOP SW	†2MØ3D	MC FM EN	†2S[illegible]D	MI PROG DIS SW	†[illegible]	RDI SEL 3	2R4ØH
3AØ1		3X11	KEY REPEAT BYPASS SW	3D23P	—	-	KEY SP CNTL-J	†3AØ1F	KEY SP CNTL-K	3AØ1L
3BØ1		3Z1Ø	KEY SING INST	2R32L	KEY SING CYCLE	3BØ9S	KEY PAR STOP	3BØ8R	KEY NXM STOP	3BØ8T
3BØ2		3Z2Ø	KEY RDI SW	3B12P	KEY STA SW	3B14E	KEY CONT SW	3BØ2F	KEY STOP SW	3BØ2H
2R37		3Z3Ø	DSØ	2R37D	DS1	2R37E	DS 2	2R37F	DS 3	2R37H
2R38		3Z4Ø	DS15	2R38D	DS16	2R38E	DS17	2R38F	DS 18	2R38H
2S37		3Z5Ø	AS18	2R34E	AS19	2R34H	AS2Ø	2R34K	AS 21	2R34M
2R39 W033		3Z6Ø W033	AS33	2R36H	AS34	2R36K	AS35	2R36M	DS 3Ø	2R39H

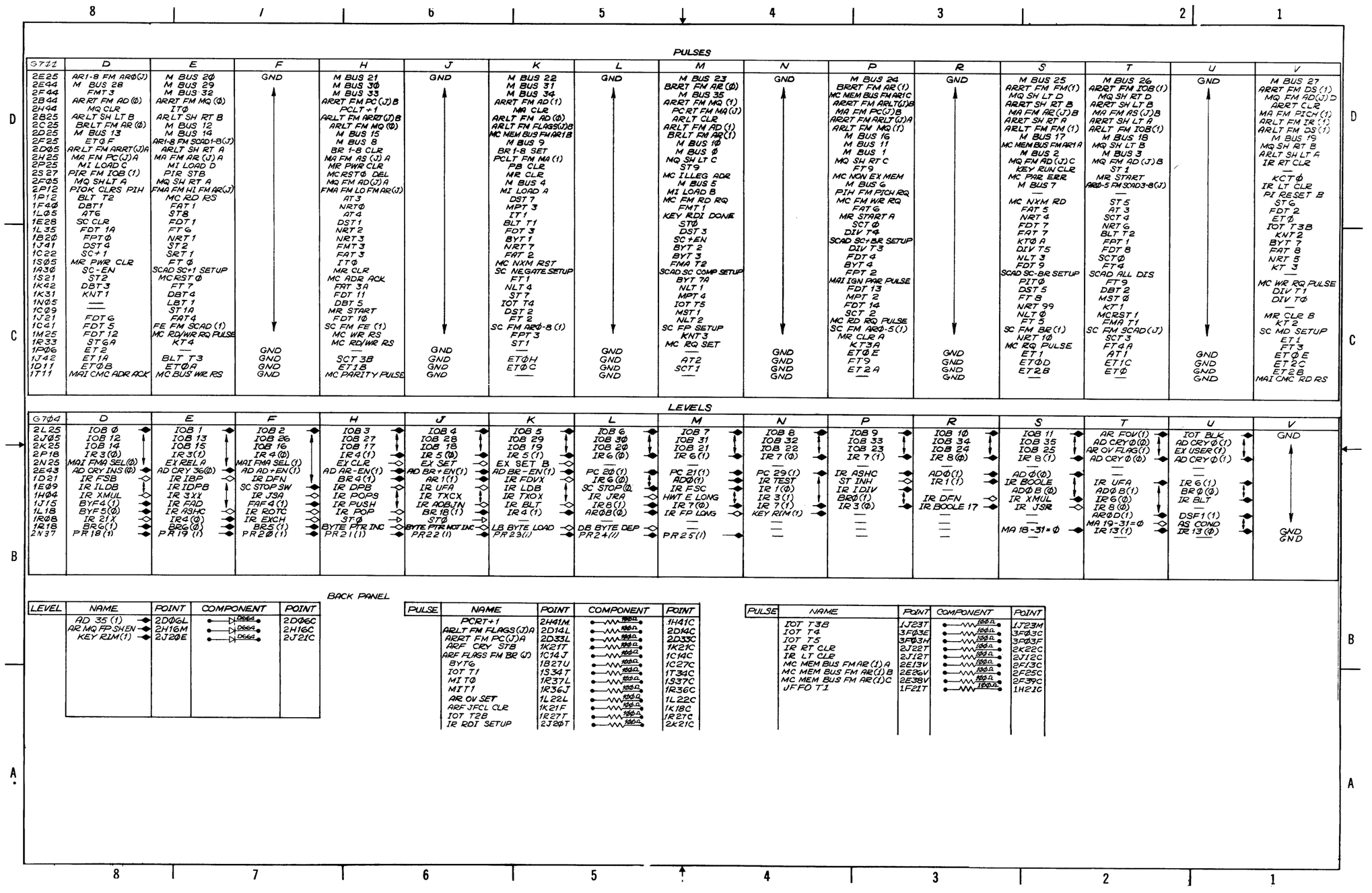
FROM	J	ORIGIN	K	ORIGIN	L	ORIGIN	M	ORIGIN
2PØ1	PR 18 (1)	2P15R	PR 19 (1)	2P15U	PR 2Ø (1)	2P17H	PR 21 (1)	2P17L
2P37	EX USER (1)	1P22F	KEY PROG STOP	2S29F	—	—	—	—
3EØ7	IOB PI 4	3E17L	IOB PI 5	3F17N	IOB PI 6	3E17R	IOB PI 7	2E17T
2P38	—	—	—	—	PC 18 IND	2J26F	PC 19 IND	2J26R
2P39	PC 28 IND	2J36F	PC 29 IND	2J36R	PC 3Ø IND	2J38F	PC 31 IND	2J38R
2P4Ø	PIH 5 IND	2S11F	PIH 6 IND	2S11R	PIH 7 IND	2S13F	PIR 1 IND	2S13R
2P41	IR 4 IND	2J11F	IR 5 IND	2J11R	IR 6 IND	2J13F	IR 7 IND	2J13R
2P42	IR 16 IND	2J23F	IR 17 IND	2J23R	MA 18 IND	2L26F	MA 19 IND	2L26R
2P43	MA 28 IND	2L36F	MA 29 IND	2L36R	MA 3Ø IND	2L38F	MA 31 IND	2L38R
2P44	PIO 5 (1)	2J17J	PIO 6 (1)	2T17J	PIO 7 (1)	2J19J	PIR 5 IND	2S17R
2R41	MI 4 IND	2MØ9H	MI 5 IND	2MØ9L	MI 6 IND	2MØ9R	MI 7 IND	2MØ9U
2R42	MI 16 IND	2M15H	MI 17 IND	2M15L	MI 18 IND	2M16R	MI 19 IND	2M15U
2R43	MI 28 IND	2M21H	MI 29 IND	2M21L	MI 3Ø IND	2M21R	MI 31 IND	2M21U
2R4Ø	RDI SEL 4	2R4ØJ	RDI SEL 5	2R4ØK	RDI SEL 6	2R4ØL	RDI SEL 7	2R4ØM
3AØ1	KEY SP CNTL-L	3AØ1K	KEY SP CNTL-M	3AØ1J	KEY SP CNTL-N	3AØ1H	GND	—
3BØ1	KEY REPEAT SW	3C25E	KEY ADR INST	3BØ8D	KEY ADR RD	3BØ8F	KEY ADR WR	3BØ8J
3BØ2	KEY RESET SW	3BØ2J	KEY EXE SW	3BØ2K	KEY EXA SW	3BØ2L	KEY EX NXT SW	3BØ2M
2R37	DS 4	2R37J	DS 5	2R37K	DS 6	2R37L	DS 7	2R37M
2R38	DS 19	2R38J	DS 2Ø	2R38K	DS 21	2R38L	DS 22	2R38M
2S37	AS 22	2R34P	AS 23	2R34S	AS 24	2R34U	AS 25	2R35E
2R39	DS 31	2R39J	DS 32	2R39K	DS 33	2R39L	DS 34	2R39M

FROM	N	ORIGIN	P	ORIGIN	R	ORIGIN	S	ORIGIN
2PØ1	PR 22 (1)	2P17R	PR 23 (1)	2P17U	PR 24 (1)	2P19H	PR 25 (1)	2P19L
2P37	—	—	—	—	—	—	—	—
3EØ7	—	—	—	—	—	—	—	—
2P38	PC 2Ø IND	2J28F	PC 21 IND	2J28R	PC 22 IND	2J3ØF	PC 23 IND	2J3ØR
2P39	PC 32 IND	2J4ØF	PC 33 IND	2J4ØR	PC 34 IND	2J42F	PC 35 IND	2J42R
2P4Ø	PIR 2 IND	2S15F	PIR 3 IND	2S15R	PIR 4 IND	2S17F	—	—
2P41	IR 8 IND	2J15F	IR 9 IND	2J15R	IR 1Ø IND	2J17F	IR 11 IND	2J17R
2P42	MA 2Ø IND	2L28F	MA 21 IND	2L28R	MA 22 IND	2L3ØF	MA 23 IND	2L3ØR
2P43	MA 32 IND	2L4ØF	MA 33 IND	2L4ØR	MA 34 IND	2L42F	MA 35 IND	2L42R
2P44	PIR 6 IND	2S19F	PIR 7 IND	2S19R	—	—	—	—
2R41	MI 8 IND	2M11H	MI 9 IND	2M11L	MI 1Ø IND	2M11R	MI 11 IND	2M11U
2R42	MI 2Ø IND	2M17H	MI 21 IND	2M17L	MI 22 IND	2M17R	MI 23 IND	2M17U
2R43	MI 32 IND	2M23H	MI 33 IND	2M23L	MI 34 IND	2M23R	MI 35 IND	2M23U
2R4Ø	RDI SEL 8	2R4ØN	RDI SEL 9	2R4ØP	—	—	—	—
3AØ1	KEY SP CNTL-P	3AØ1N	KEY SP CNTL-R	3AØ1P	—	—	—	—
3BØ1	KEY ADR STOP	3BØ8L	KEY ADR BRK	3BØ8N	—	—	—	—
3BØ2	KEY DEP SW	3BØ2N	KEY DEP NXT SW	3BØ2P	—	—	—	—
2R37	DS 8	2R37N	DS 9	2R37P	DS 1Ø	2R37R	DS 11	2R37S
2R38	DS 23	2R38N	DS 24	2R38P	DS 25	2R38R	DS 26	2R38S
2S37	AS 26	2R35H	AS 27	2R35K	AS 28	2R35M	AS 29	2R35P
2R39	DS 35	2R39N	—		—	—	—	—

FROM	T	ORIGIN	U	ORIGIN	V	ORIGIN
2PØ1					GND	
2P37					↓	
3EØ7					↓	
2P38					↓	
2P39					↓	
2P4Ø					↓	
2P41					↓	
2P42					↓	
2P43					↓	
2P44					↓	
2R41					↓	
2R42					↓	
2R43					↓	
2R4Ø	—	—	—	—	—	
3AØ1	—	—	—	—	—	
3BØ1	—	—	—	—	—	—
3BØ2	—	—	—	—	—	—
2R37	DS 12	2R37T	DS 13	2R37U	DS 14	2R37V
2R38	DS 27	2R38T	DS 28	2R38U	DS 29	2R38V
2S37	AS 3Ø	2R35S	AS 31	2R35U	AS 32	2R36E
2R39	—	—	—	—	—	—

NOTES: 1.*THIS IS A PIN ON THE IBC CABLE (ORIGIN OF SIGNAL IS IN ANOTHER BAY)
2.†THIS IS A PIN ON THE IBC CABLE (SIGNAL IS USED IN BAY 1)

D-IC-KA10-0-ICSC2 Indicator and Console Switch Connections



D-CL-KA10-0-TERM Pulse and Level Terminations (Bay 1 and Bay 2)

SIGNAL NAME	FROM PIN	TO PIN	COLOR	REMARKS
ARF FLAGS FM BR (J)	1K19F	1C14N	WHT TWP	
	1K19C	1C15M	BLK	
ARLT CLR	1H28D	1H44D		
	1H28E	1H44C		
ARLT FM DS (1)	1J25N	1H43T		
	1J25P	1H44U		
ARLT FM FLAGS (J)A	1H42S	1C14D		
	1H42N	1C13C		
ARLT FM FLAGS (J)A	1C14D	1J24D		
	1C15C	1J24E		
ARLT FM FLAGS (J)B	1J24N	1H42V		
	1J24P	1H42U		
ARLT FM IOB (1)	1J23N	1H42D		
	1J23P	1H42C		
ARLT FM IR (1)	1H23N	1H43S		
	1H23P	1H44R		
ARLT SHLT A	1H24D	1H44P		
	1H24C	1H44L		

A-WL-KA10-0-TWP1 General Wiring Sheet For TWP List KA10 Bay 1 (Sheet 1)

SIGNAL NAME	FROM PIN	TO PIN	COLOR	REMARKS
ARLT SHLT B	1H24N	1H44H	WHT TWP	
	1H24P	1H44F	BLK	
ARLT SHRT A	1H26D	1H44S		
	1H26E	1H44N		
ARLT SHRT B	1H26N	1H44K		
	1H26P	1H44J		
ARRT CLR	1H28N	1H43M		
	1H28P	1H43N		
ARRT FM DS (1)	1J25D	1H43V		
	1J25E	1H43U		
ARRT FM FM (1)	1J26N	1H43P		
	1J26P	1H43R		
ARRT FM IOB (1)	1J23D	1H42E		
	1J23E	1H42F		
ARRT FM PC (J)A	1H29D	1H42T		
	1H29E	1H42R		
ARRT FM PC (J)B	1H29N	1H41V		
	1H29P	1H41U		

A-WL-KA10-0-TWP1 General Wiring Sheet For TWP List KA10 Bay 1 (Sheet 2)

SIGNAL NAME	FROM PIN	TO PIN	COLOR	REMARKS
ARRT SHLT A	1H25D	1H43H	WHT TWP	
	1H25E	1H43J	BLK	
ARRT SHLT B	1H25N	1H43K		
	1H25P	1H43L		
ARRT SHRT A	1H27D	1H43D		
	1H27E	1H43C		
ARRT SHRT B	1H27N	1H43E		
	1H27P	1H43F		
ARLT FM FM (1)	1H41M	1J26D		
	1H41C	1J26C		
ARLT FM FM (1)	1J26D	1S35T		
	1J26E	1S35C		
ARØ-5 FM SCAD 3-8 (J)	1H23D	1H41P		
	1H23E	1H41L		
AR1-8 FM ARØ (J)	1H21D	1H41S		
	1H21E	1H41N		
AR1-8 FM SCAD 1-8 (J)	1H21N	1H41T		
	1H21P	1H41R		

A-WL-KA10-0-TWP1 General Wiring Sheet For TWP List KA10 Bay 1 (Sheet 3)

SIGNAL NAME	FROM PIN	TO PIN	COLOR	REMARKS
AT1	1S28N	1L40D	WHT TWP	
	1S28P	1L40C	BLK	
AT3	1R32D	1L40E		
	1R32E	1L39C		
AT4	1T40U	1M38U		
	1T40C	1M38K		
AT4	1M38D	1F30U		
	1M38C	1H30C		
AT4	1M03U	1F30U		
	1N03C	1F31T		
AT6	1T23N	1M34T		
	1T23P	1M34V		
AT6	1L08T	1M36M		
	1M08C	1M37C		
BLT T1	1J07T	1J32N		
	1J06M	1J31K		
BLT T2	1R14T	1J02D		
	1R14V	1J02E		

A-WL-KA10-0-TWP1 General Wiring Sheet For TWP List KA10 Bay 1 (Sheet 4)

SIGNAL NAME	FROM PIN	TO PIN	COLOR	REMARKS
BLT T2	1L36T	1J02D	WHT TWP	
	1M36C	1J02C	BLK	
BYT2	1B06L	1D26J		
	1B06M	1D26C		
BYT2	1D26J	1J39E		
	1D25C	1J39C		
BYT4	1F22P	1S03P		
	1F23M	1S02K		
BYT7A	1E39D	1T36H		
	1E39C	1T36C		
DBT2	1A04L	1E35S		
	1A04M	1E35V		
DBT3	1A03L	1E36T		
	1A03M	1F36C		
DBT5	1A02N	1J39U		
	1A02P	1J39P		
DBT5	1J39U	1N10H		
	1K39C	1N09C		

A-WL-KA10-0-TWP1 General Wiring Sheet For TWP List KA10 Bay 1 (Sheet 5)

SIGNAL NAME	FROM PIN	TO PIN	COLOR	REMARKS
DIVT5	1F17N	1N10K	WHT TWP	
	1F17P	1N10C	BLK	
DIVT5	1N10K	1J40M		
	1P10C	1J40C		
DST3	1F08L	1E31K		
	1F08M	1E31C		
DST4	1F12H	1E31H		
	1F12C	1E32C		
DST7	1F06N	1L22P		
	1F06P	1L23C		
DST7	1L22T	1R17J		
	1M22C	1R17K		
ETØ	1F19T	1K25T		
	1F19V	1K25M		
ETØ	1K25T	1R32J		
	1K25V	1R32M		
ETØ	1R28R	1M10T		
	1R28C	1M10M		

A-WL-KA10-0-TWP1 General Wiring Sheet For TWP List KA10 Bay 1 (Sheet 6)

SIGNAL NAME	FROM PIN	TO PIN	COLOR	REMARKS
ETØA	1F19N	1C23H	WHT TWP	
	1F19P	1C22C	BLK	
ETØB	1J09J	1E10R		
	1J09M	1F10C		
ETØD	1K25N	1E32M		
	1K25P	1E33M		
ETØE	1T05T	1M10N		
	1T05V	1M10P		
ETØF	1T37M	1L43D		
	1T38M	1L43C		
ETØH	1R26D	1M30K		
	1R26E	1M31C		
ETØH	1L25F	1J31L		
	1L25C	1J31C		
ET1	1T29L	1K26T		
	1T29M	1K26V		
ET1B	1R10N	1H21J		
	1R10P	1H21M		

A-WL-KA10-0-TWP1 General Wiring Sheet For TWP List KA10 Bay 1 (Sheet 7)

SIGNAL NAME	FROM PIN	TO PIN	COLOR	REMARKS
ET1C	1R26N	1L24T	WHT TWP	
	1R26P	1L24C	BLK	
ET2	1S32T	1M10J		
	1S32V	1M10C		
ET2A	1T30N	1H37V		
	1T30P	1H37U		
ET2B	1J01J	1T03T		
	1J01M	1T03V		
FMT3	1H03N	1L42M		
	1H03V	1L42L		
ET2C	1S32N	1M35J		
	1S32P	1M35M		
FAT3A	1B14N	1J38N		
	1B14P	1J38C		
FAT7	1C24U	1L33N		
	1D24E	1L33C		
FAT8	1C23M	1J38P		
	1C23C	1J37C		

A-WL-KA10-0-TWP1 General Wiring Sheet For TWP List KA10 Bay 1 (Sheet 8)

SIGNAL NAME	FROM PIN	TO PIN	COLOR	REMARKS
FDT9	1L39K	1T04T	WHT TWP	
	1L39E	1T06C	BLK	
FDT11	1F19J	1J33D		
	1F19M	1J33C		1
FMA T1	1T33L	1K39T		
	1T33M	1K39V		
FMT1	1C01D	1J04L		
	1C01E	1J04M		
FMT1	1J04L	1D23D		
	1J04C	1D23C		
FMT3	1H03N	1D17E		
	1H03P	1D17C		
FMT3	1D23K	1J39D		
	1D22M	1H38C		
FPT3	1C02L	1A22J		
	1C02M	1A22C		
FT1	1M03E	1T03J		
	1M03C	1T03M		

A-WL-KA10-0-TWP1 General Wiring Sheet For TWP List KA10 Bay 1 (Sheet 9)

SIGNAL NAME	FROM PIN	TO PIN	COLOR	REMARKS
FT3	1L09D	1J26J	WHT TWP	
	1L09E	1J26M	BLK	
FT3	1J26J	1T37F		
	1J26V	1T37C		
FT4	1M03J	1J28K		
	1M04C	1J28C		
FT4	1L40N	1T04N		
	1M39M	1T04C		
FT4A	1K08P	1J34E		
	1K09M	1J34C		
FT4A	1J37T	1T36D		
	1K37M	1S36V		
FT6	1M01L	1J37N		
	1M01M	1K37C		
FT7	1S03K	1M38E		
	1S03C	1M39C		
FT7	1M03K	1S03K		
	1L03C	1R03C		

A-WL-KA10-0-TWP1 General Wiring Sheet For TWP List KA10 Bay 1 (Sheet 10)

SIGNAL NAME	FROM PIN	TO PIN	COLOR	REMARKS
FT9	1K03N	1A19N	WHT TWP	
	1K03P	1A19C	BLK	
FT9	1L37J	1E38E		
	1L37M	1E38C		
FT9	1K03N	1P43D		
	1K03M	1P43C		
IOT T3B	1R43D	1J23T		
	1R43C	1J23V		
ITØ	1M30D	1M03T		
	1M30C	1M04M		
IT1	1M32J	1M07L		
	1M32M	1M07C		
IT1	1R31D	1M37H		
	1R31C	1M35C		
KTØA	1S13D	1C20T		
	1S13C	1C20V		
KT3	1T43T	1L37T		
	1T43U	1L37C		

A-WL-KA10-0-TWP1 General Wiring Sheet For TWP List KA10 Bay 1 (Sheet 11)

SIGNAL NAME	FROM PIN	TO PIN	COLOR	REMARKS
KT3	1L29J	1T08J	WHT TWP	
	1L29M	1T08M	BLK	
LBT1	1B16D	1J33K		
	1B16C	1H33V		
LBT1	1J33K	1N10E		
	1K33C	1M10V		
MAI CMC ADR ACK	1S09T	1R42D		
	1T09C	1R42C		
MAI CMC RD RS	1S13R	1P43E		
	1S12M	1P43F		
MAI CMC RD RS	1S13R	1T08T		
	1T13C	1T08C		
MAI CMC RD RS	1T08T	1T11V		
	1T08P	1T11U		
MAI CMC ADR ACK	1S09T	1T11D		
	1T10C	1T12C		
MAI IGN PAR PULSE	1M43V	1T32J		
	1M43U	1T32C		

A-WL-KA10-0-TWP1 General Wiring Sheet For TWP List KA10 Bay 1 (Sheet 12)

SIGNAL NAME	FROM PIN	TO PIN	COLOR	REMARKS
MAI IGN PAR PULSE	1T32J	1S21P	WHT TWP	
	1T32E	1S21N	BLK	
MC BUS WR RS	1S10H	1T11E		
	1S10C	1T11F		
MC BUS WR RS	1T11E	1R42E		
	1T12M	1R42J		
MC ILLEG ADR	1S20L	1T43M		
	1S20M	1T43L		
MC NON EX MEM	1S17T	1T43K		
	1T17C	1T43J		
MC PAR ERR	1S17N	1T43P		
	1S17C	1T43N		
MC PARITY PULSE	1R36T	1T11H		
	1R36M	1T11J		
MC PARITY PULSE	1T11H	1S10L		
	1T11L	1S09C		
MC PARITY PULSE	1R42H	1R36T		
	1R42L	1R36V		

SIGNAL NAME	FROM PIN	TO PIN	COLOR	REMARKS
MC RD RQ PULSE	1S16D	1J28N	BLK TWP	
	1S16C	1K28C	WHT	
MC RD/WR RQ PULSE	1T17K	1J28P		
	1T18M	1K27C		
MC WR RS	1S11J	1K27T		
	1S11C	1K27V		
MPT2	1J14T	1N09E		
	1J14C	1M09M		
MPT2	1N09E	1M30R		
	1M09C	1M29M		
MPT3	1H01L	1E29T		
	1H01M	1E29C		
MPT4	1J01N	1N09P		
	1J01P	1N06V		
MR CLR	1R06D	1F37U		
	1R06E	1H36C		
MR CLR	1T43E	1R02D		
	1T43F	1R02C		

SIGNAL NAME	FROM PIN	TO PIN	COLOR	REMARKS
MR CLR A	1R06N	1P17H	WHT TWP	
	1R06P	1P17C	BLK	
MR CLR B	1M06D	1J07L		
	1M06C	1J07C		
MR CLR B	1F12D	1C11D		
	1F13C	1C11C		
MR START	1M07D	1B16E		
	1L07M	1B16P		
MR START	1T35T	1S42D		
	1T35C	1S42C		
MR START R	1R06L	1S39D		
	1R06C	1S39C		
NLT1	1D02D	1C24P		
	1D02E	1C25C		
NLT1	1C24P	1J29D		
	1D24C	1J29C		
NLT2	1A27N	1J27K		
	1A27C	1J27C		

A-WL-KA10-0-TWP1 General Wiring Sheet For TWP List KA10 Bay 1 (Sheet 15)

SIGNAL NAME	FROM PIN	TO PIN	COLOR	REMARKS
NRT4	1C24N	1L21D	WHT TWP	
	1C24C	1L20C	BLK	
NRT99	1D19N	1N09S		
	1D19P	1N08V		
PI RESET B	1P15D	1P43P		
	1P15E	1P43N		
STØ	1N08N	1F30N		
	1N08M	1F30C		
ST1	1L43E	1K22D		
	1L42F	1J21U		
ST1	1K22D	1R29J		
	1K23C	1R29M		
ST1	1R38D	1S11T		
	1R38C	1T11C		
ST1A	1R13L	1C10E		
	1R13M	1C10C		
ST2	1N02D	1J40F		
	1N02E	1J41C		

A-WL-KA10-0-TWP1 General Wiring Sheet For TWP List KA10 Bay 1 (Sheet 16)

SIGNAL NAME	FROM PIN	TO PIN	COLOR	REMARKS
ST7	1R16N	1J34N	WHT TWP	
	1R16P	1K34C	BLK	
ST8	1S19T	1K22J		
	1S19C	1K22C		
ST1	1L43E	1N08D		
	1L43F	1N07C		
MR START A	1P11P	1L22H		
	1P11C	1L21C		

A-WL-KA10-0-TWP1 General Wiring Sheet For TWP List KA10 Bay 1 (Sheet 17)

SIGNAL NAME	FROM PIN	TO PIN	COLOR	REMARKS
ARLT CLR	2B03D	2C14T	WHT	
	2B03C	2C15M	BLK TWP	
ARLT FM ARRT (J)B	2B03E	2B18L		
	2B03F	2B18C		
ARLT FM FLAGS (J)B	2C03V	2D16L		
	2C03R	2D16C		
ARLT FM FM (1)	2D02M	2E15F		
	2D02N	2E15C		
ARLT SHLT B	2B03H	2C20R		
	2B03J	2C19M		
ARLT SHRT B	2B03K	2C20V		
	2B03L	2C21M		
ARRT CLR	2C02M	2C29T		
	2C02N	2C30M		
ARRT FM AD (Ø)	2D02D	2D26R		
	2D02C	2D26C		
ARRT FM AD (1)	2D02H	2D27R		
	2D02J	2D27C		

A-WL-KA10-0-TWP2 General Wiring Sheet For TWP List KA10 Bay 2 (Sheet 1)

SIGNAL NAME	FROM PIN	TO PIN	COLOR	REMARKS
ARRT FM ARLT (J)A	2B03T	2B28L	WHT	
	2B03R	2B28C	BLK TWP	
ARRT FM ARLT (J)B	2B03V	2B37L		
	2B03U	2B37C		
ARRT FM DS (1)	2C02V	2D28V		
	2C02U	2E28C		
ARRT FM FM (1)	2C02P	2D28L		
	2C02R	2D28C		
ARRT FM IOB (1)	2C03E	2D28R		
	2C03F	2D29C		
ARRT FM MQ (Ø)	2D02E	2D26V		
	2D02F	2E25C		
ARRT FM MQ (1)	2D02K	2D27V		
	2D02L	2E27C		
ARRT FM PC (J)A	2C03T	2D26L		
	2C03U	2D25C		
ARRT FM PC (J)B	2D02V	2D35L		
	2D02U	2D35C		

A-WL-KA10-0-TWP2 General Wiring Sheet For TWP List KA10 Bay 2 (Sheet 2)

SIGNAL NAME	FROM PIN	TO PIN	COLOR	REMARKS
ARRT SHLT A	2C02H	2B28V	WHT TWP	
	2C02J	2C28C	BLK	
ARRT SHLT B:	2C02K	2B37V		
	2C02L	2C37C		
ARRT SHRT A	2C02D	2B28R		
	2C02C	2B29C		
ARRT SHRT B	2C02E	2B37R		
	2C02F	2B38C		
AR ØØ BB (Ø-)	2B11D	2E10J		
	2B11C	2E11C		
AR ØØ BB (1-)	2E12J	2B14D		
	2E12C	2B14C		
BRRT FM AR (Ø)	2H04T	2E27T		
	2H04R	2F28C		
BRRT FM AR (1)	2H04V	2E29T		
	2H04U	2F29C		
ETØF	2J02D	2T34R		
	2J02C	2T34C		

A-WL-KA10-0-TWP2 General Wiring Sheet For TWP List KA10 Bay 2 (Sheet 3)

SIGNAL NAME	FROM PIN	TO PIN	COLOR	REMARKS
ETØF	2S28T	2K43F	WHT TWP	
	2S28P	2K44C	BLK	
ETØF	2L44D	2J20J		
	2L44C	2J20C		
FMT3	2J03M	2H35T		
	2J03N	2H36M		
FT9	2P02D	2R24D		
	2P02C	2R24C		
IRRT CLR	2J03S	2J22P		
	2J03R	2J22C		
ITØ	2M02T	2K43T		
	2M02U	2K43C		
KEY RDI DONE	2N03E	2S29P		
	2N03F	2S29C		
KNT1	2P02S	2S24L		
	2P02R	2S24M		
KNT2	2N03D	2S25L		
	2N03C	2S25M		

A-WL-KA10-0-TWP2 General Wiring Sheet For TWP List KA10 Bay 2 (Sheet 4)

SIGNAL NAME	FROM PIN	TO PIN	COLOR	REMARKS
KNT3	2P02T	2S26D	WHT TWP	
	2P02U	2S26E	BLK	
KTØA	2T02H	2R27D		
	2T02J	2R27C		
KT1	2N03V	2T23L		
	2N03U	2T23C		
KT2	2N03T	2S23J		
	2N03N	2S23E		
KT3	2T02T	2R25D		
	2T02U	2R25C		
KT3A	2R03K	2R24T		
	2R04C	2S24C		
KT4	2T02D	2S29N		
	2T02C	2S28V		
MA CLR	2M02D	2K27T		
	2M02C	2K27C		
MA FM AR (J)A	2M02K	2K26R		
	2M02L	2K26C		

A-WL-KA10-0-TWP2 General Wiring Sheet For TWP List KA10 Bay 2 (Sheet 5)

SIGNAL NAME	FROM PIN	TO PIN	COLOR	REMARKS
MA FM AR (J)B	2M02M	2K39R	WHT TWP	
	2M02N	2K41C	BLK	
MA FM AS (J)A	2M02P	2K26V		
	2M02R	2L26C		
MA FM AS (J)B	2M02S	2K39V		
	2N02C	2K39C		
MA FM PC (J)A	2M02E	2K26L		
	2M02F	2K25C		
MA FM PC (J)B	2M02J	2K39L		
	2M02K	2K38C		
MA FM PICH (1)	2J02S	2K40L		
	2J02U	2K40C		
MAI IGN PAR PULSE	2M02V	2L02T		
	2M01V	2M03C		
MAI CMC RD RS	2K01E	2P02E		
	2K01F	2P02N		
MAIB MC REQ CYC	2K01M	2N05E		
	2K01N	2N05M		

A-WL-KA10-0-TWP2 General Wiring Sheet For TWP List KA10 Bay 2 (Sheet 6)

SIGNAL NAME	FROM PIN	TO PIN	COLOR	REMARKS
MAIB MM 18	2K01S	2N06E	WHT TWP	
	2K01R	2N06M	BLK	
-MAIB MM 18	2K01T	2N06P		
	2J01V	2N06V		
MAIB MM 19	2K01V	2N07E		
	2L01U	2N07M		
-MAIB MM 19	2L01D	2N07P		
	2L01C	2N07V		
MAIB MM 20	2L01E	2N08E		
	2L01F	2N08M		
-MAIB MM 20	2L01H	2N08P		
	2L01J	2N08V		
MAIB MM 21	2L01K	2N09E		
	2L01L	2N09M		
-MAIB MM 21	2L01M	2N09P		
	2L01N	2N09V		
MAIB MM 35	2L01P	2N10E		
	2L01R	2N10M		

A-WL-KA10-0-TWP2 General Wiring Sheet For TWP List KA10 Bay 2 (Sheet 7)

SIGNAL NAME	FROM PIN	TO PIN	COLOR	REMARKS
-MAIB MM 35	2L01S	2N01P	WHT TWP	
	2L01V	2N10V	BLK	
MAIB FMC SELECT	2L01T	2N05P		
	2L01U	2N05V		
MAIB 22	2K02D	2N11E		
	2K02C	2N11M		
MAIB 23	2K02E	2N11P		
	2K02F	2N11V		
MAIB 24	2K02H	2N12E		
	2K02J	2N12M		
MAIB 25	2K02K	2N12P		
	2K02L	2N12V		
MAIB 26	2K02M	2N13E		
	2K02N	2N13M		
MAIB 27	2K02P	2N13P		
	2K02R	2N13V		
MAIB 28	2K02S	2N14E		
	2K05C	2N14M		

A-WL-KA10-0-TWP2 General Wiring Sheet For TWP List KA10 Bay 2 (Sheet 8)

SIGNAL NAME	FROM PIN	TO PIN	COLOR	REMARKS
MAIB 29	2K02T	2N14P	WHT TWP	
	2K06C	2N14V	BLK	
MAIB 30	2K02V	2N15E		
	2K02U	2N15M		
MAIB 31	2L02D	2N15P		
	2L02C	2N15V		
MAIB 32	2L02E	2N16E		
	2L02F	2N16M		
MAIB 33	2L02H	2N16P		
	2L02J	2N16V		
MAIB 34	2L02K	2N17E		
	2L02L	2N17M		
MAIB 35	2L02M	2N17P		
	2L02N	2N17V		
MAIB MC RD (1)	2L02P	2N18E		
	2L02R	2N18M		
MAIB MC WR (1)	2L02S	2N18P		
	2L06C	2N18V		

A-WL-KA10-0-TWP2 General Wiring Sheet For TWP List KA10 Bay 2 (Sheet 9)

SIGNAL NAME	FROM PIN	TO PIN	COLOR	REMARKS
MAIB 21	2L02V	2N19E	WHT TWP	
	2L02U	2N19M	BLK	
MAI CMC ADR ACK	2R03D	2K01D		
	2R03C	2K01C		
MC BUS WR RS	2R03E	2K01H		
	2R03F	2K01J		
MC PARITY PULSE	2R03H	2K01K		
	2R03J	2K01L		
MAIB MM 22	2N19P	2K01P		
	2N19C	2J01C		
M BUS ØØ	2K03D	2P08D		
	2K03C	2P08C		
	2P08D	2J08D		
	2P07C	2J08C		
	2J08D	2E09H		
	2J07C	2E09C		
M BUS Ø1	2K03E	2P08E		
	2K03F	2P09C		
	2P08E	2J08E		
	2N06C	2J09C		

A-WL-KA10-0-TWP2 General Wiring Sheet For TWP List KA10 Bay 2 (Sheet 10)

SIGNAL NAME	FROM PIN	TO PIN	COLOR	REMARKS
M BUS Ø1 (CONT)	2J08E	2E09L	WHT TWP	
	2J07M	2E10C	BLK	
M BUS Ø2	2K03H	2P08K		
	2K03J	2P05C		
	2P08K	2J08R		
	2P06C	2J06C		
	2J08R	2E09P		
	2J05V	2E08C		
M BUS Ø3	2K03K	2P08L		
	2K03L	2P09M		
	2P08L	2J08S		
	2P07M	2K07C		
	2J08S	2E09T		
	2K08C	2F09C		
M BUS Ø4	2KQ3M	2P08R		
	2K03N	2R08C		
	2P08R	2J10K		
	2P12F	2J10C		
	2J10K	2E13H		
	2J09M	2E13C		
M BUS Ø5	2K03P	2P08S		
	2K03R	2P12J		

A-WL-KA10-0-TWP2 General Wiring Sheet For TWP List KA10 Bay 2 (Sheet 11)

SIGNAL NAME	FROM PIN	TO PIN	COLOR	REMARKS
M BUS Ø5 (CONT)	2P08S	2J10L	WHT TWP	
	2R07C	2J11M	BLK	
	2J10L	2E13L		
	2J13M	2E14M		
M BUS Ø6	2K03S	2P10D		
	2J05C	2P10C		
	2P10D	2J14D		
	2P11C	2J14C		
	2J14D	2E13P		
	2J13C	2E14H		
M BUS Ø7	2K03T	2P10E		
	2L07C	2P12C		
	2P10E	2J14E		
	2P12U	2J15C		
	2J14E	2E13T		
	2J15M	2E14S		
M BUS Ø8	2K03V	2P10K		
	2K03U	2P07V		
	2P10K	2J18D		
	2P11M	2J18C		
	2J18D	2E17H		
	2J17C	2E17C		

A-WL-KA10-0-TWP2 General Wiring Sheet For TWP List KA10 Bay 2 (Sheet 12)

SIGNAL NAME	FROM PIN	TO PIN	COLOR	REMARKS
M BUS Ø9	2L03D	2P10L	WHT TWP	
	2L03C	2P11V	BLK	
	2P10L	2J18E		
	2P13M	2J19C		
	2J18E	2E17L		
	2J17M	2E16M		
M BUS 1Ø	2L03E	2P10R		
	2L03F	2R10C		
	2P10R	2J18K		
	2R09C	2J19M		
	2J18K	2E17P		
	2J21M	2F17C		
M BUS 11	2L03H	2P10S		
	2L03J	2R11C		
	2P10S	2J18L		
	2P09V	2K20C		
	2J18L	2E17T		
	2K19C	2E16S		
M BUS 12	2L03K	2P14D		
	2L03L	2P14C		
	2P14D	2J18R		
	2P13C	2K18C		

A-WL-KA10-0-TWP2 General Wiring Sheet For TWP List KA10 Bay 2 (Sheet 13)

SIGNAL NAME	FROM PIN	TO PIN	COLOR	REMARKS
M BUS 12 (CONT)	2J18R	2E21H	WHT TWP	
	2K17C	2E21C	BLK	
M BUS 13	2L03M	2P14E		
	2L03N	2P12L		
	2P14E	2J24E		
	2P12N	2J24C		
	2J24E	2E21L		
	2J23C	2E20C		
M BUS 14	2L03P	2P14K		
	2L03R	2P12R		
	2P14K	2J24K		
	2P13V	2J23M		
	2J24K	2E21P		
	2H25U	2F21C		
M BUS 15	2L03S	2P14L		
	2M05C	2P15M		
	2P14L	2J24L		
	2P15V	2H25R		
	2J24L	2E21T		
	2H25N	2F20C		
M BUS 16	2L03T	2P14R		
	2M06C	2R14C		

A-WL-KA10-0-TWP2 General Wiring Sheet For TWP List KA10 Bay 2 (Sheet 14)

SIGNAL NAME	FROM PIN	TO PIN	COLOR	REMARKS
M BUS 16 (CONT)	2P14R	2J24R	WHT TWP	
	2R13C	2H25L	BLK	
	2J24R	2E26H		
	2H25J	2E26C		
M BUS 17	2L03V	2P14S		
	2L03U	2R15C		
	2P14S	2J24S		
	2P17M	2K24C		
	2J24S	2E26L		
	2H25F	2E25F		
M BUS 18	2K04D	2P16D		
	2K04C	2P16C		
	2P16D	2E26P		
	2P15C	2F26C		
M BUS 19	2K04E	2P16E		
	2K04F	2P17C		
	2P16E	2E26T		
	2P17V	2F27C		
M BUS 2Ø	2K04H	2P16K		
	2K04J	2P19M		
	2P16K	2E30H		
	2P19V	2E30C		

A-WL-KA10-0-TWP2 General Wiring Sheet For TWP List KA10 Bay 2 (Sheet 15)

SIGNAL NAME	FROM PIN	TO PIN	COLOR	REMARKS
M BUS 21	2K04K	2P16L	WHT TWP	
	2K04L	2P18C	BLK	
	2P16L	2E30L		
	2R18C	2E31C		
M BUS 22	2K04M	2P16R		
	2K04N	2R16C		
	2P16R	2E30P		
	2P18V	2E29C		
M BUS 23	2K04P	2P16S		
	2K04R	2R17C		
	2P16S	2E30T		
	2N16C	2F30C		
M BUS 24	2K04S	2P20D		
	2L08C	2P20C		
	2P20D	2E34H		
	2P21C	2E34C		
M BUS 25	2K04T	2P20E		
	2J03U	2P19C		
	2P20E	2E34L		
	2N20V	2E33C		
M BUS 26	2K04V	2P20K		
	2K04U	2N21V		

A-WL-KA10-0-TWP2 General Wiring Sheet For TWP List KA10 Bay 2 (Sheet 16)

SIGNAL NAME	FROM PIN	TO PIN	COLOR	REMARKS
M BUS 26 (CONT)	2P20K	2E34P	WHT TWP	
	2P25C	2E35C	BLK	
M BUS 27	2L04D	2P20L		
	2L04C	2P24C		
	2P20L	2E34T		
	2P21M	2F34C		
M BUS 28	2L04E	2P20R		
	2L04F	2R20C		
	2P20R	2E38H		
	2R21C	2E38C		
M BUS 29	2L04H	2P20S		
	2L04J	2R19C		
	2P20S	2E38L		
	2P21V	2E37C		
M BUS 3Ø	2L04K	2P22D		
	2L04L	2P22C		
	2P22D	2E38P		
	2P23C	2E39C		
M BUS 31	2L04M	2P22E		
	2L04N	2P26C		

A-WL-KA10-0-TWP2 General Wiring Sheet For TWP List KA10 Bay 2 (Sheet 17)

SIGNAL NAME	FROM PIN	TO PIN	COLOR	REMARKS
M BUS 31 (CONT)	2P22E	2E38T	WHT TWP	
	2N22V	2F38C	BLK	
M BUS 32	2L04P	2P22K		
	2L04R	2P23M		
	2P22K	2E42H		
	2P23V	2E42C		
M BUS 33	2L04S	2P22L		
	2M07C	2N20C		
	2P22L	2E42L		
	2N21C	2E41C		
M BUS 34	2L04T	2P22R		
	2M04C	2N22C		
	2P22R	2E42P		
	2N23C	2E43C		
M BUS 35	2L04V	2P22S		
	2L04U	2R23C		
	2P22S	2E42T		
	2R22C	2E44U		
MC ILLEG ADR	2T02M	2T32L		
	2T02N	2T32C		

A-WL-KA10-0-TWP2 General Wiring Sheet For TWP List KA10 Bay 2 (Sheet 18)

SIGNAL NAME	FROM PIN	TO PIN	COLOR	REMARKS
MC MEM BUS FM AR(1)A	2H04D	2E09V	WHT TWP	
	2H04C	2F10C	BLK	
MC MEM BUS FM AR(1)B	2H04E	2E21V		
	2H04F	2F22C		
MC MEM BUS FM AR(1)C	2H04H	2E34V		
	2H04J	2F34M		
MC NON EX MEM	2T02K	2T32P		
	2T02L	2T33C		
MC PAR ERR	2T02P	2T32T		
	2T02R	2T31M		
MCRST1	2T02S	2T24T		
	2T01V	2T24V		
MI LOAD C	2N03P	2M16F		
	2N03R	2M16C		
MI LOAD D	2N03S	2M20T		
	2N03L	2M19M		
MQ FM AD (J)A	2J04P	2F14V		
	2J04R	2H14C		

A-WL-KA10-0-TWP2 General Wiring Sheet For TWP List KA10 Bay 2 (Sheet 19)

SIGNAL NAME	FROM PIN	TO PIN	COLOR	REMARKS
MQ FM AD (J)B	2J04S	2F18V	WHT TWP	
	2J06S	2H18C	BLK	
MQ FM AD (J)C	2J03H	2F24V		
	2J03J	2H23C		
MQ FM AD (J)D	2J03K	2F37V		
	2J03L	2F37C		
MQ SHLT A	2J04E	2F14L		
	2J04F	2F14C		
MQ SHLT B	2J04H	2F18L		
	2J04J	2F19M		
MQ SHLT C	2J04T	2F24L		
	2J06V	2F24C		
MQ SHLT D	2J03D	2H37L		
	2J03C	2H38M		
MQ SHRT A	2J04K	2F14R		
	2J04L	2F15M		
MQ SHRT B	2J04M	2F18R		
	2J04N	2F17M		

A-WL-KA10-0-TWP2 General Wiring Sheet For TWP List KA10 Bay 2 (Sheet 20)

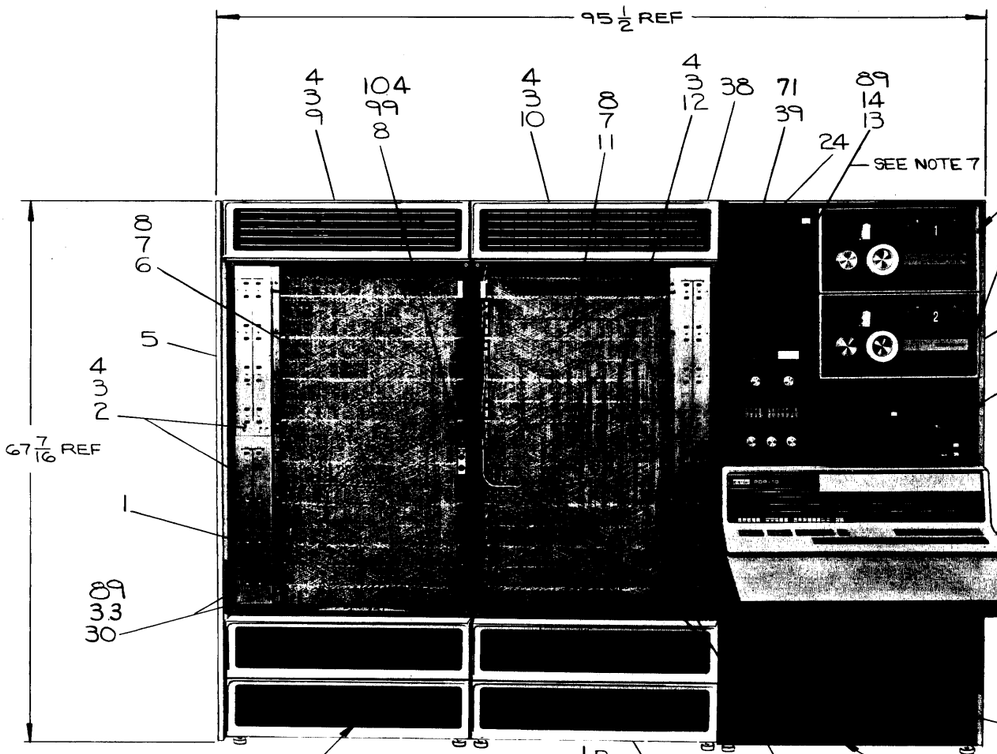
SIGNAL NAME	FROM PIN	TO PIN	COLOR	REMARKS
MQ SHLT C	2J04V	2F24R	WHT TWP	
	2J04U	2F23M	BLK	
MQ SHRT D	2J03E	2H37R		
	2J03F	2H37C		
MR CLR	2T02E	2T32D		
	2T02F	2T31C		
PCLT +1	2J02M	2H27M		
	2J02N	2H27C		
PCLT FM MA (J)	2J02H	2J27T		
	2J02J	2 J28M		
PCRT +1	2J02P	2K36M		
	2J02R	2K36C		
PCRT FM MA (J)	2J02K	2J35F		
	2J02L	2J35C		
ST9	2S03E	2S21K		
	2S03F	2S21C		
ST1	2J02E	2J20D		
	2J02F	2H20C		

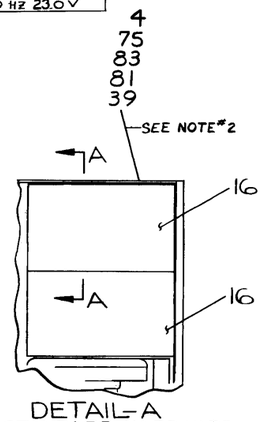
A-WL-KA10-0-TWP2 General Wiring Sheet For TWP List KA10 Bay 2 (Sheet 21)

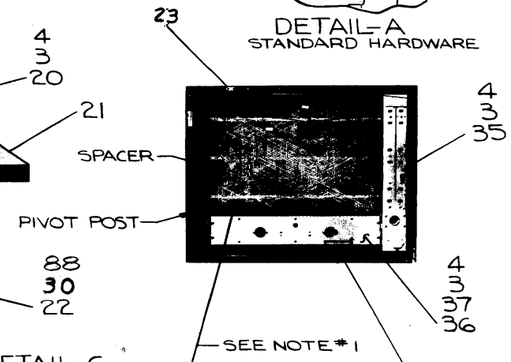
SIGNAL NAME	FROM PIN	TO PIN	COLOR	REMARKS
ST1	2J20D	2R27R	WHT TWP	
	2H19M	2R28M	BLK	

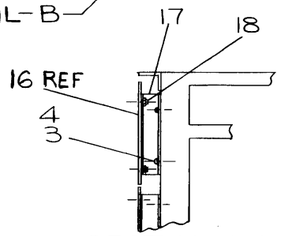
A-WL-KA10-0-TWP2 General Wiring Sheet For TWP List KA10 Bay 2 (Sheet 22)

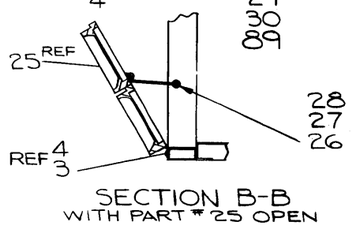
LEGEND	
NUMBER	VARIATION
KA10-A	60 HZ 115 V
KA10-B	50 HZ 115 V
KA10-C	50 HZ 230 V

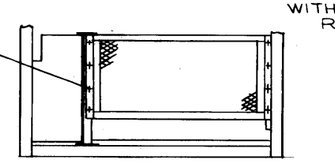












NOTES:

1. REMOVE KEPS NUT FROM SPACER. ATTACH ITEM #34 TO SPACER & PIVOT POST USING EXISTING HARDWARE
2. FOR CABINET JOINING SEE DWG # D-DA-76051120-0-0
3. PLACE PART # 80 (SHIPPING BOLT) INTO CABLE CLAMPS LOCATED ON PLENUM DOORS. WHEN SHIPPING UNIT INSTALL SHIPPING BOLTS INTO ADJACENT HOLES PREVENTING PLENUM DOORS FROM SWINGING OPEN
4. FOR DRAWING INDEX LIST SEE DWG. # D-DI-KA10-0-3
5. FOR VARIATION [illegible] HARDWARE DEPENDING [illegible] SHIPPED SEE DWG # D-DA-76051120-0-0 SHEET 4 OF 5.
6. USE EXISTING TRIM STRIP HARDWARE TO FASTEN ITEM #91 SHIPPING BRACKET TO CAB. POSITION BRACKET SO FOAM RESTS AGAINST FAN HOUSING. REMOVE AFTER SHIPPING
7. REMOVE PHENOLIC BOARD & SPACER FROM PARTS 13, 14 & 15 BEFORE ASS'Y INTO ITEM #39 THEN REASSEMBLE
8. REMOVE SIDE BPACE FROM PART # 51 & 52 AND REPLACE WITH PART # 49
9. INSTALL ITEM #100 INTERLOCK ASSY USING HDW. SUPPLIED

D-UA-KA10-0-0 KA10 Assembly (Sheet 1)