G. Bell

PDP-X Technical Memorandum # 38

Title: Parity Control in the Magtape IO Processor

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Index Keys: IO
Parity
Magtape
Control Memory
Processor

Dsitribution Keys: A

Obsolete: None

Revision: #30, "Control Memory Format"

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I. In order that the PDP-X Magtape Processor/TU-XX system create tapes which are truly compatible with IBM equipment, the correct parity must be generated during 9-track operation. Two types of parity operation are important:

a. The parity bit must be generated as the most significant bit for 9-bit data output and Cyclic Redundancy Character computation. In a 16-bit register, the parity bit will be generated as bit 7, the 8 bits of data becoming bits 8-15. Transfers of data to the IO Register, from which the IO Data Bus is driven, are made from the lower 9 bits of the Result bus. Actually, only bits 8-15 of the IO Reg drive the IO Data Bus (which is only 8 bits in size); bit 7 drives the Parity Out Line, Command Out Line 1. Similarly, Parity In, Response In Line 1, is available at the Carry Insert circuits for parity insertion at the time of accepting input data from the IO Bus, as described below.

b. The entire 9 bits read in from tape must be available for CRC computation, and for checking at the parity bit against the internally (to the IOP) computed parity of the 8 data bits.

Both types must also be capable of using either even or odd parity, as specified in the Command Word.

II. It is shown below, by μ-coded examples, that the necessary operation may be realized as follows:

1. An 8-bit exclusive-OR result will be generated from the left half of the Arithmetic Register.

2. Three additional signals will be provided in Control Memory, probably by adding a bit in the Carry Insert group plus an additional level of decoding. The functions so provided will be:

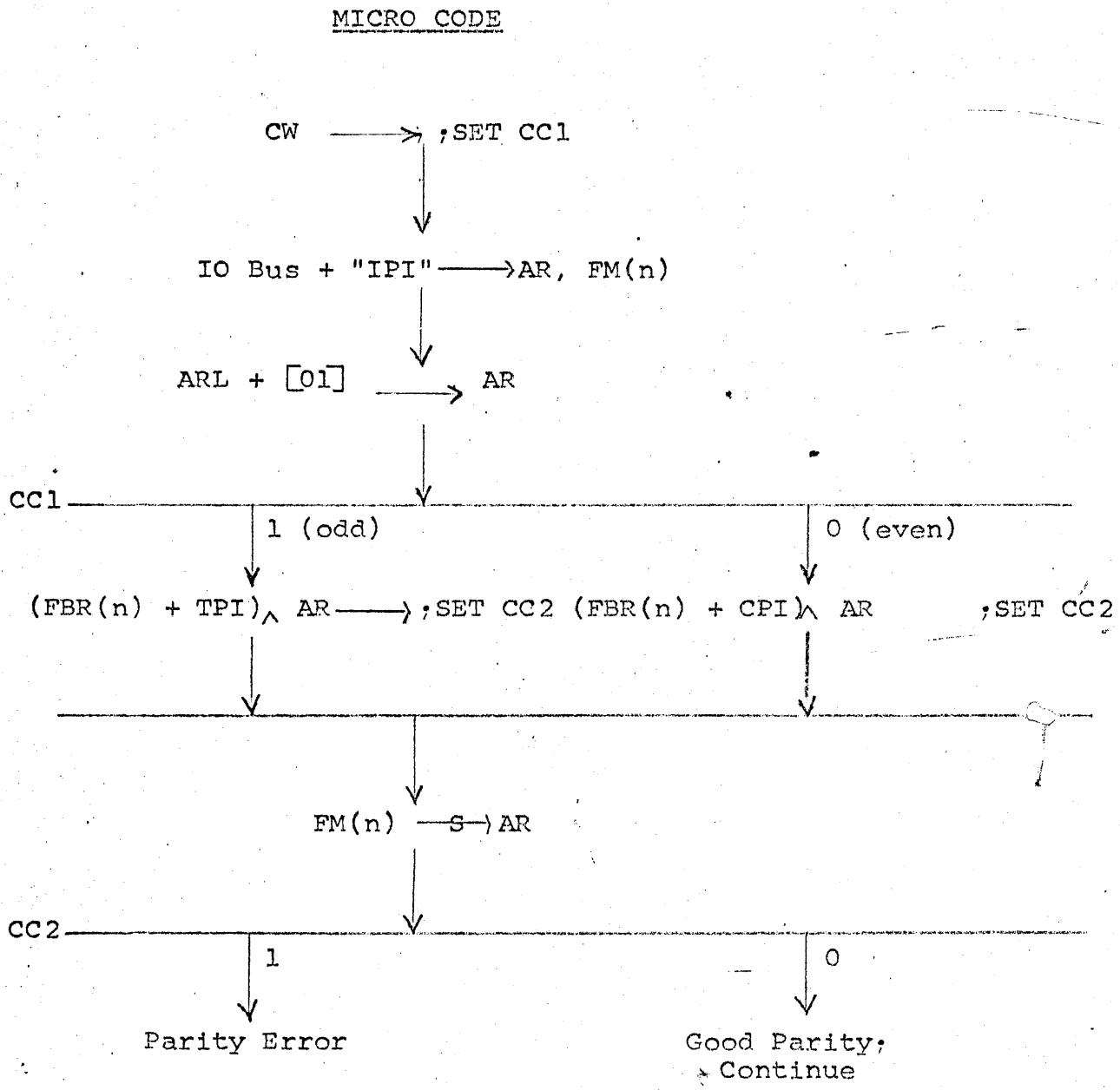
   a. Input Parity Insert - send the parity track from tape to the Carry Insert input, at bit 15 of the Conditional Sum Adder.

   b. True Parity Insert - output of the 8-bit XOR to Carry Insert.

   c. Complemented Parity Insert - complement of the 8-bit XOR output to Carry Insert.

The truth table of Appendix III shows the results of combining the TPI/CPI operations with a mask of the resulting bit 15; which may be done within a single μ-instruction.

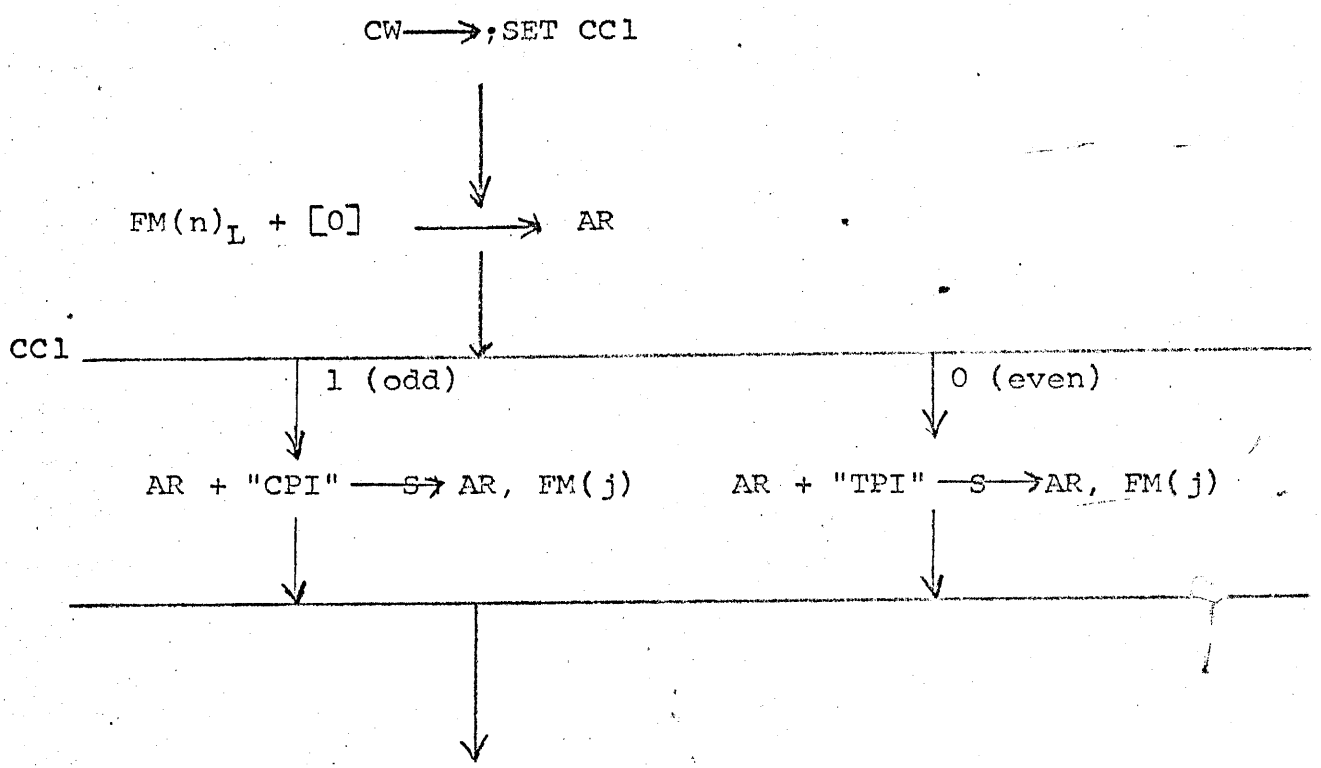
Appendices I and II are examples of parity input, testing, and generation.



Appendix I - Microcode for Data Input and Parity Check

MICRO CODE

COMMENTS



Test commanded parity.

Move data to left byte of AR and zero right byte; branch on commanded parity.

Insert appropriate parity.

9-bit result in AR now with desired parity.

Appendix II - Microcode for Parity Insertion, Even or Odd

	Bit AR15		
Parity Output; XOR of AR0-7	Initial	After CPI	After TPI
0	0	1	0
0	1	0	1
1	1	1	0
1	0	0	1

Appendix III - Truth Table for CPI/TPI Operations