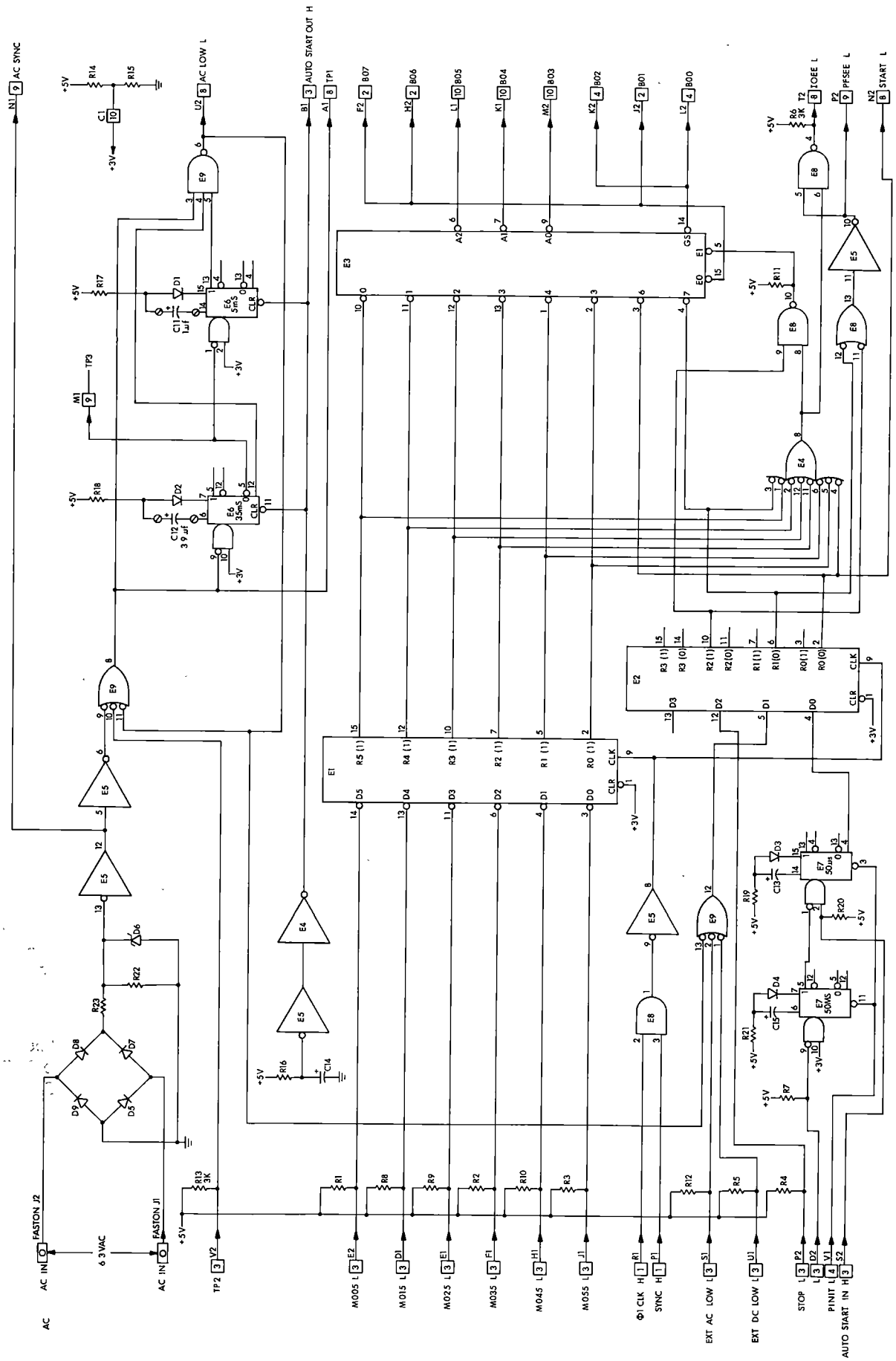

FIGURE 1. M7346 LOGIC BLOCK DIAGRAM

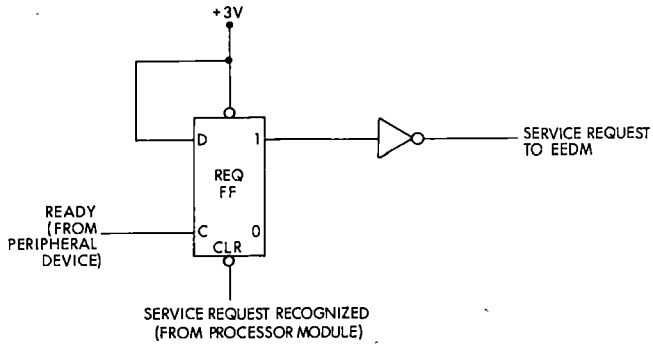

FIGURE 2. TYPICAL EXAMPLE OF PERIPHERAL SERVICE REQUEST ARBITRATION

FUNCTION

Priority Arbitration Logic

EEDM priority arbitration logic (see Figure 1) accepts nine levels of ascending priority. Eight of these levels result in a memory reference and the ninth, and highest, is executed by the Processor Module without referencing memory. Level 0 through 5, designated by the input signal lines M006 L, M015 L, M025 L, M035 L, M045 L, and M055 L, constitute the six lowest priority levels. These lines are reserved for implementing six levels of application-defined interrupt priority arbitration.

The seventh level is reserved for the automatic and manual restart function, and the eighth and highest arbitrated level, for power failure detection. The ninth, and highest absolute level, is reserved for the stop function which automatically jams a HLT instruction into the Processor Module to stop operation.

EEDM priority arbitration logic is formed by the nine-stage external event storage latch, E3 and E2, and the octal encoder, E4. Assertions of any of the nine levels are stored during the combined periods of the Processor Module synchronous timing signals SYNC H and Φ1CLCK H. These signals are ANDed to strobe the external event storage latch, E1 and E2, once during each processor state time (every 4 μs) to store asserted events. The outputs of the first eight stages of the external event storage latch are input to the octal priority encoder E3. These eight input lines are ORed by E4 to enable the encoder. The outputs of the encoder, E0 and GS, are wired to assert the code for an RST instruction on module output lines B00 to B02 and B06 and B07. The octal number corresponding to the external event input line asserted is simultaneously placed in the address field (B03 to B05) of the RST instruction generated by encoder E3.

In parallel with the generation of the RST instruction, the outputs of the first eight stages of latch E1, E2 are ORed by E4 to assert the signal IOEE L at the Processor Module. This signal, when asserted, generates an interrupt if interrupts are enabled, and initiates multiplexing of the RST instruction on EEDM output lines B00 to B07 at the Processor Module external event port DIOST0 L to DIOST7 L for fetching.

The octal number placed in the address field of the RST instruction generated is in the range of 0 to 7. Through decoding of this instruction, this value is mapped to address one of the eight locations 0, 8, 16, 24, 32, 40, 48, and 56 (octal 10, 20, 30, 40, 50, 60, and 70 respectively) in an MPS system memory. The result is a correspondence between a given external event input line and an unconditional call on a dedicated memory location. Through this mechanism, application-defined routines can be developed to implement priority interrupt schemes, start-up routines, and power-failure handling routines.

Start Circuit

The start function can be initiated in two ways: automatically by an integral EEDM circuit, or manually by an external switch. The automatic start output signal AUTO START OUT H is generated by the RC circuit R16, C14, and E5 when +5 V power is turned on and is maintained high as long as +5 V is maintained. The output of this circuit also clears the two monostable multivibrators, E6, in the power failure detection circuit. This automatically-generated start signal, when fed back to the EEDM, becomes the input signal AUTO START IN H. When asserted, this signal triggers the monostable multivibrator E7 to produce a 50 μs signal at pin 4. This signal is stored in the seventh stage of the external event latch, E1, E2, on the next assertion of Φ1CLK H and SYNC H from the Processor Module. As a consequence, an RST instruction making an unconditional call on memory location 48 (60_8) is generated and placed on output lines B00 to B07. Simultaneously, the signal START L is asserted at the Processor Module to initiate a demand interrupt and to multiplex the RST instruction into the external event port DIOST0 L to DIOST7 L for fetching. Manual restarts are implemented through the EEDM input signal START L which can be derived from an external switch. This signal is debounced by the monostable multivibrator E7 which produces a 50 ms negative-going debouncing level at pin 5 for input to E7 at pin 1. From this point, the circuit path is exactly the same as with an automatic restart. Both automatic and manual start signals take priority over all other external events except power failure detection and stop functions.

Power Failure Detection Circuit

The EEDM contains a complete ac power failure detection circuit (see Figure 1) which samples a 6.3 V, 50 or 60 Hz, ac input derived from the local line voltage by an external transformer. This sampled ac voltage, which is received through two FASTON tabs on the handle end of the module, is rectified by a full-wave diode bridge to produce a signal having a frequency twice that of the ac input frequency. This signal is input to the frequency integrator E5, E9, and E6 which detects the absence of line voltage for two complete cycles. The signal period triggered by a power failure is approximately 34 ms and is determined by the value of capacitor C12 which, together with R18, forms the RC for the monostable multivibrator E6 at pins 6 and 7. Note that C12 is connected to the circuit with split lugs. This manner of connection permits the value of C12 to be changed to accommodate different application requirements.

Input Signals (continued)

Symbol	*Description*	*Pin*	*Function*
AC PLUS IN	Ac Sampling Voltage Positive Terminal	J1	This signal is the +6.3 Vac brought into FASTON tab J1 from an external transformer for sampling by the EEDM power failure detection circuit.
AC MINUS IN	Ac Sampling Voltage Negative Terminal	J2	This signal is the —6.3 Vac brought into FASTON tab J2 from an external transformer for sampling by the EEDM power failure detection circuit.
Φ1CLK H	Processor Module Clock Signal	R1	This is the first phase of the Processor Module two-phase clock and is used in conjunction with SYNC H to strobe external event signals into the EEDM for priority arbitration.
SYNC H	Processor Module Synchronization Signal	P1	This signal is the basic machine cycle synchronization signal for the Processor Module and is used in conjunction with ΦCLK H at the EEDM to control input timing of external event signals.
PINIT L	System Initialize Signal	V1	This is the 10-ms system initialize signal from the Processor Module and is used to reset condition-sensitive EEDM logic at start-up time.
TP2	Test Point 2	V2	This test point is used to check the operation of the EEDM power failure detection circuit.

Output Signals

Symbol	*Description*	*Pin*	*Function*
B00	External Event and Power Fail/Stop Output Line 0	L2	
B01	External Event and Power Fail/Stop Output Line 1	J2	
B02	External Event and Power Fail/Stop Output Line 2	K2	
B03	External Event and Power Fail/Stop Output Line 3	M2	These eight output lines serve to convey the RST instructions generated in response to specific application-defined events to the Processor Module for fetching.
B04	External Event and Power Fail/Stop Output Line 4	K1	These lines can be connected to both the PM external event and power fail/stop port.
B05	External Event and Power Fail/Stop Output Line 5	L1	
B06	External Event and Power Fail/Stop Output Line 6	H2	
B07	External Event and Power Fail/Stop Output Line 7	F2	

INPUT/OUTPUT SYMBOLOGY

The direction of signal flow is indicated by arrows on the signal lines Arrows toward the module indicate input signals; arrows away from the module indicate output signals (see Figure 1 and Figure 3).

Fan-in and fan-out (in TTL unit loads) are indicated by the number contained in the box associated with each pin. A box containing the letter B designates that the associated signal line is connected to a bus.

INPUT—The fan-in designation box always precedes the pin designation.

OUTPUT—The fan-out designation box always follows the pin designation.

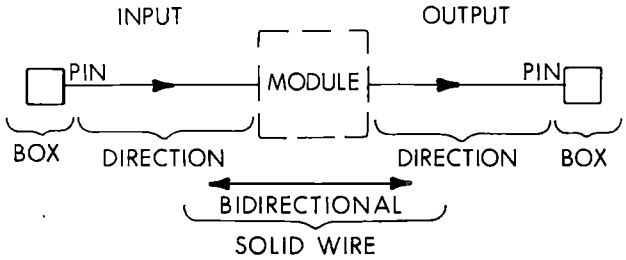

FIGURE 4. SIGNAL FLOW DIRECTION

POWER REQUIREMENTS

Volts	Power Consumption		Voltage Regulation	Ripple Regulation	Pins	
	mA	Watts			Power	Ground
+5Vdc	250	1.25	±5%	50mV	A2	C2,T1
6.3Vac	50	0.32			FASTON J2	FASTON J1

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