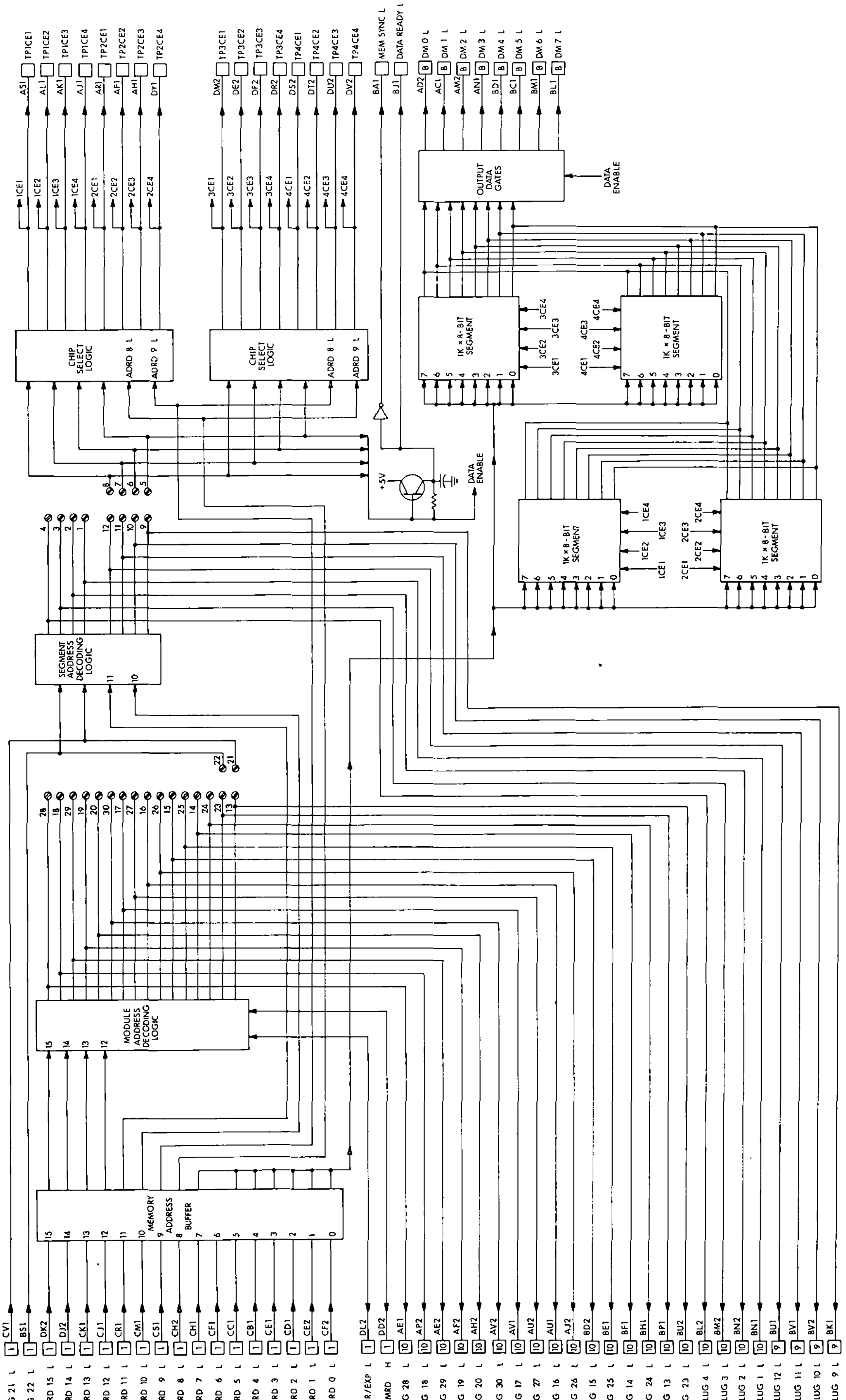

FIGURE 1. M7345 LOGIC BLOCK DIAGRAM

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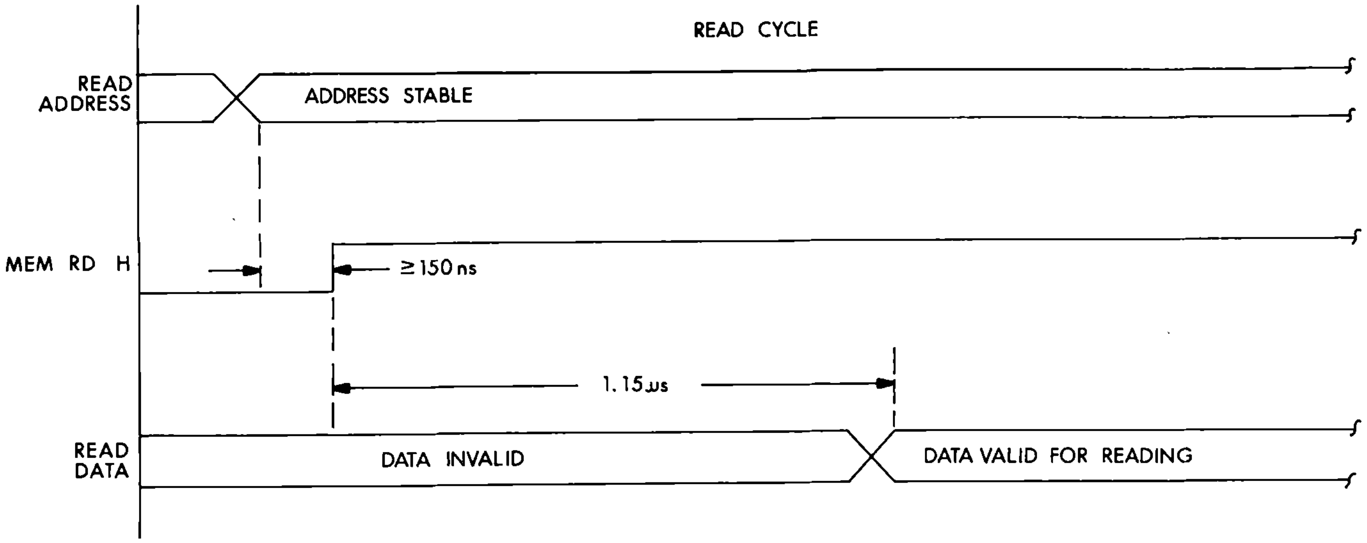

FIGURE 2. MEMORY TIMING DIAGRAM

Memory Jumper Options

In order to address multiple module memory systems containing up to 64K locations, which implements the full accessing capacity of a 16-bit address field, all of the decoded states of bits ADRD13 L to ADRD15 L can be jumper-configured. As a consequence, each 4K module in a multiple-module memory system can be uniquely jumpered to be assigned as a given set of up to 4K memory locations within a consecutive set of up to 64K locations.

Inspection of Figure 1 will show that the jumper network is configured to permit allocation of address space in 1K intervals within an address range of 4K to 8K formed by either one or two M7345 modules.

This jumper network is also brought out to the module edge fingers to permit address space allocation to be implemented by wire wrap on the connector block.

SIGNAL SPECIFICATIONS

Input Signals

Symbol	*Description*	*Pin*	*Function*
CF2	Address Line 0	ADRD00 L	These 16 parallel input lines provide a 16-bit address for reading instructions and data stored in an M7345 read-only memory module.
CE2	Address Line 1	ADRD01 L	
CD1	Address Line 2	ADRD02 L	
CE1	Address Line 3	ADRD03 L	
CB1	Address Line 4	ADRD04 L	
CC1	Address Line 5	ADRD05 L	
CF1	Address Line 6	ADRD06 L	
CH1	Address Line 7	ADRD07 L	
CH2	Address Line 8	ADRD08 L	
CS1	Address Line 9	ADRD09 L	
CM1	Address Line 10	ADRD10 L	
CR1	Address Line 11	ADRD11 L	
CJ1	Address Line 12	ADRD12 L	
CK1	Address Line 13	ADRD13 L	
DJ2	Address Line 14	ADRD14 L	
DK2	Address Line 15	ADRD15 L	

Output Signals (continued)

Symbol	*Description*	*Pin*	*Function*
DF2	3CE3 Test Point	TP3CE3	These test points permit testing access to the internal chip-enable signals and are used only to test memory operation.
DR2	3CE4 Test Point	TP3CE4	
DS2	4CE1 Test Point	TP4CE1	
DT2	4CE2 Test Point	TP4CE2	
DU2	4CE3 Test Point	TP4CE3	
DV2	4CE4 Test Point	TP4CE4	

Input/Output Signals

Symbol	*Description*	*Pin*	*Function*
AD2	Memory Data Bus Line 0	DM0 L	These are the eight parallel data lines comprising the data memory bus.
AC1	Memory Data Bus Line 1	DM1 L	
AM2	Memory Data Bus Line 2	DM2 L	
AN1	Memory Data Bus Line 3	DM3 L	
BD1	Memory Data Bus Line 4	DM4 L	
BC1	Memory Data Bus Line 5	DM5 L	
BM1	Memory Data Bus Line 6	DM6 L	
BL1	Memory Data Bus Line 7	DM7 L	

HARDWARE/ACCESSORIES

The M7345 Programmable Read-Only Memory Module is supplied with sockets for a memory capacity of up to 4K, but without the dual in-line PROM circuits which plug into the sockets. These PROM circuits are available separately and may be ordered under the following nomenclature and part number:

NOMENCLATURE	DEC PART NUMBER
2048-bit Programmable Read-Only Memory (24-pin DIP)	23-00A4-03

DIGITAL also offers the MR873-A Microprocessor ROM Programmer which provides for the electrical writing of programs into 23-00A4-03 PROM circuits. This programmer operates in conjunction with any PDP-8 computer system having OMNIBUS construction. Such a configuration permits the reading in of an object program from an associated input device (e.g. a TTY), the examination and modification of this program, and the electrical writing of the resulting program into PROM circuits. Listings and paper tapes of the written program can also be obtained.

SPECIAL WIRING

As shown in Figure 1 and discussed under FUNCTIONS, the M7345 Programmable Read-Only Memory Module is designed to respond to a 16-bit address field. As a consequence, a given module with up to 4K of memory capacity can exist within a 64K address space.

Within these 64K locations, an M7345 memory module can be configured to occupy a unique 1K or 2K address space in the 4K address space. In addition, this 4K address space can occupy any one of four groups of sequential 4K locations within the total 16K address space. Similarly, a read-only memory module can be configured to occupy a 4K block within an 8K address space, and this 8K address space can be located in either the upper or lower half of the total 16K address space.

An M7345 memory module can be assigned to occupy a given 4K or 8K address space in one of two ways:

1. By jumper-connecting specific module address space selection lugs (see Figure 3) which are part of a total set of split lugs provided on the module for the explicit purpose of address space assignment.

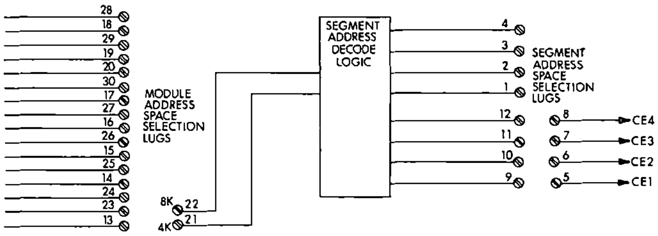

FIGURE 3. DESIGNATIONS FOR SPLIT LUGS PROVIDED FOR ADDRESS SPACE ASSIGNMENT

2. By wire wrapping the appropriate connector block pins which correspond to the specific edge connector fingers within the overall group of fingers allocated to address space assignment (see Table 1).

Within the module, each 1K segment can be assigned to one of the four 1K address spaces in a 4K space or in an 8K space through appropriate connection of the segment address space selection lugs (see Figure 3). Note that this level of address space selection must be made with jumpers since the equivalent split-lug points are not brought out to the edge connector. The actual set of 256 words addressed within a 1K segment is determined by the physical position of the PROM circuit on the board (see Figure 4). In order to clarify the manner of assigning a read-only memory module to a specific address space, a series of examples is presented which relate specific lug-to-lug connections to address space assigned. These examples require reference to Figure 3 and Table 1.

EXAMPLE 1: By placing a jumper between lug 13 and lug 21, a read-only memory module will be assigned to locations 0 to 4095. In this case, the segment address selection lugs 9, 10, 11, and 12 should be connected to lugs 5, 6, 7, and 8, respectively, in order to enable the four 1K memory sectors comprising the total 4K capacity.

EXAMPLE 2: By placing a jumper between lug 21 and lugs 23, 24 or 14, a read-only memory module can be assigned to locations 4096 to 8191, 8192 to 12287, or 12288 to 16383, respectively. With any of these assignments, the segment address space selection lugs must be connected in the same manner as in Example 1.

EXAMPLE 3: Since 8K subsets of the overall 16K address space are defined by boundaries of the four constituent 4K address spaces, 1K memory module segments can occupy any one of six unique 8K spaces. Three of these 8K spaces are formed by adjacent 4K spaces and three are nonadjacent. The three 8K spaces formed by adjacent 4K spaces are defined in this example.

The 8K address space 0 to 8191 is allocated to a module by installing a jumper between module address space selection lugs 21 and 13, and 22 and 23 on that module. The 8K address space 4096 to 12287 is allocated to a module by installing a jumper between lugs 21 and 23, and lugs 22 and 24. Finally, to allocate the 8K space 8192 to 16383 to a module, a jumper must be installed between lugs 21 and 24 and between lugs 22 and 14.

At this point, jumpers installed between specific segment address selection lugs can then assign the one, two, or four 1K segments on a module within the 8K address space allocated to that module. For example, with a read-only memory module allocated to the 8K space 8192 to 16383, a jumper installed between lugs 9 and 5 assigns the first 1K segment to the address space 8192 to 9215. Similarly, a jumper installed between lugs 1 and 6 assigns the second 1K segment to the address space 12288 to 13311. A jumper installed between lugs 7 and 11 assigns the third 1K segment to the address space 9216 to 10239. Finally, a jumper installed between lugs 8 and 2 assigns the fourth 1K segment to the address space 13312 to 14335.

It can be inferred from these examples that the 1K segments comprising a 1K, 2K, or 4K MPS system read-only memory module can be assigned by jumper-installation to any one of the 1K slots in the total 64K address space.

INPUT/OUTPUT SYMBOLOGY

The direction of signal flow is indicated by arrows on the signal lines. Arrows toward the module indicate input signals; arrows away from the module indicate output signals (see Figure 1 and Figure 5).

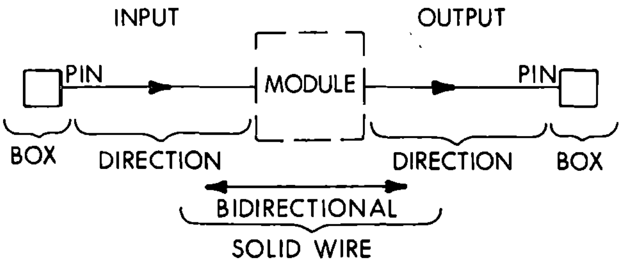

FIGURE 5. SIGNAL FLOW DIRECTION

Fan-in and fan-out (in TTL unit loads) are indicated by the number contained in the box associated with each pin. A box containing the letter B designates that the associated signal line is connected to a bus.

INPUT—The fan-in designation box always precedes the pin designation.

OUTPUT—The fan-out designation box always follows the pin designation.

POWER REQUIREMENTS

	POWER CONSUMPTION		VOLTAGE REGULATION	RIPPLE REGULATION	PINS	
VOLTS	mA (max)	WATTS (max)			POWER	GROUND
+5	1290	6.5	±5%	50 mV	AA2, BA2, CA2, DA2	AC2, AT1, BC2, BC1, CC2, CC1, DC2, DC1
−15	1085	16.3	±3%	50 mV	AB2	

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