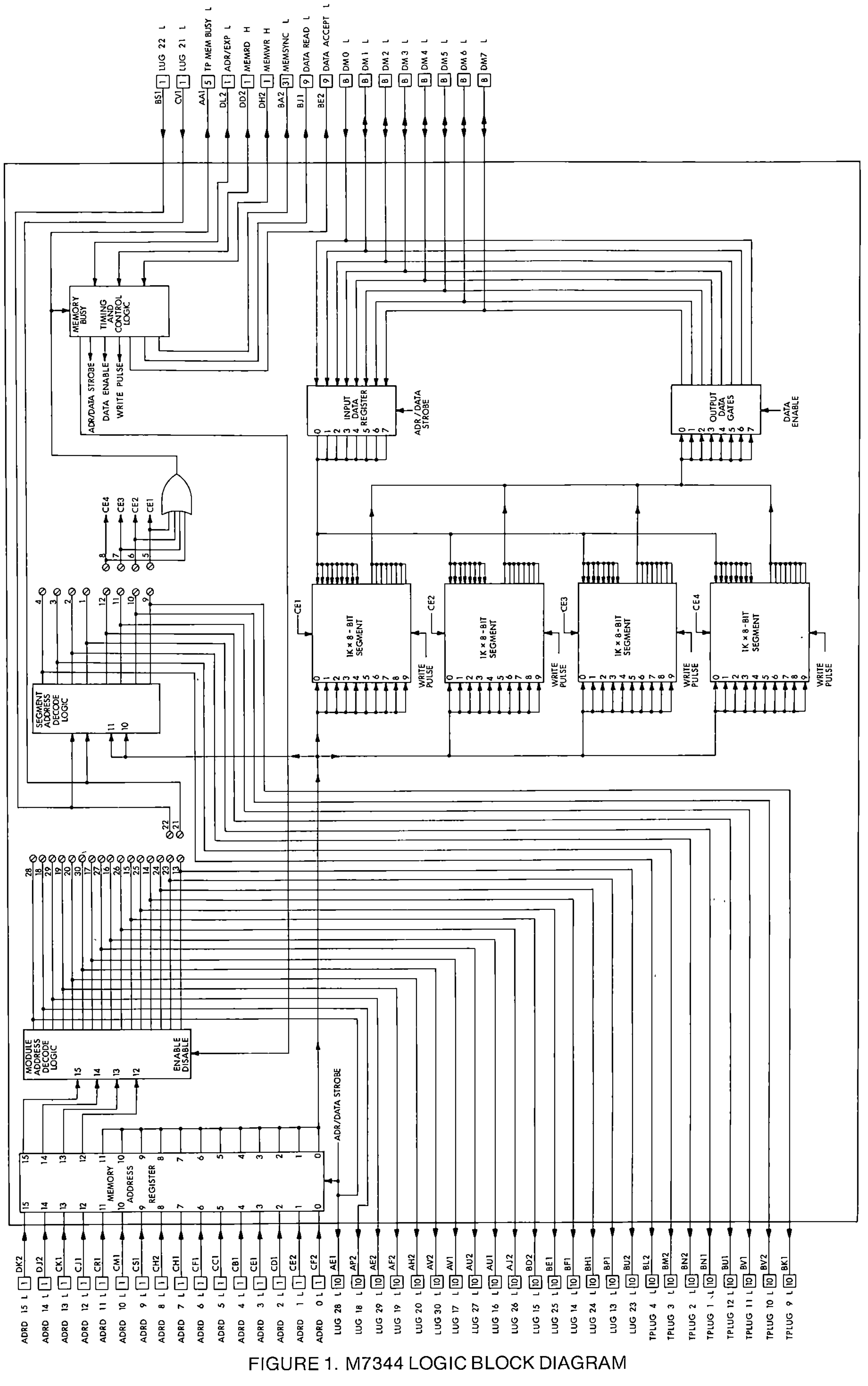

FIGURE 1. M7344 LOGIC BLOCK DIAGRAM

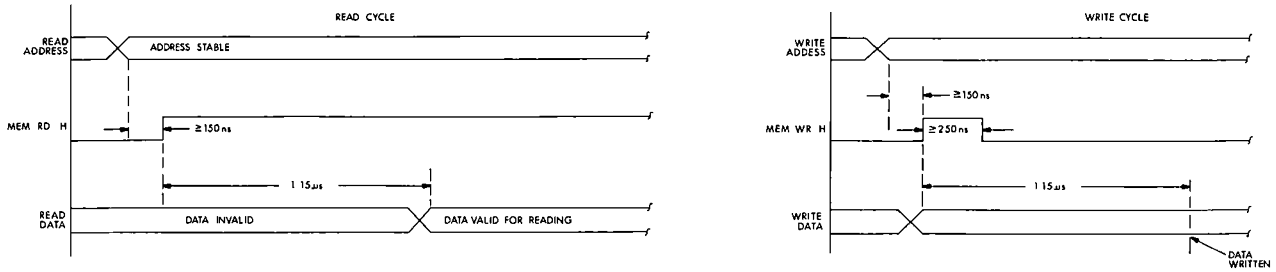

FIGURE 2. MEMORY TIMING DIAGRAM

Address Decoding
Input to the memory address decoding logic is an address furnished by an associated processor and loaded into the memory address register from the address bus ADRD00 L to ADRD15 L by the assertion of ADR/DATA STROBE H. Both the address bus and the memory address register can accommodate a 16-bit address to permit memory system capacities up to 64K. In addition, the input signal ADR/EXP L provides for implementing memory system capacities beyond 64K.

The ten low-order bits (ADRD00 L to ADRD09 L) of the memory address access the same location in each of the four 1K memory segments. The next high-order two bits (ADRD10 L and ADRD11 L) define the final magnitude of the addressed location and are decoded by the segment address decoding logic to assert one of the four signals CE1, CE2, CE3, or CE4. These signals enable the 1K segment which contains the location pointed to by the low-order 12 bits of the 14-bit address.

Note that each of the signals CE1, CE2, CE3, and CE4 is jumpered to permit assignment of address space in 1K multiples within the total memory system address space.

Memory Jumper Options
In order to address multiple module memory systems containing up to 64K locations, which implements the full accessing capacity of a 16-bit address field, all of the decoded states of bits ADRD13 L to ADRD15 L can be jumper-configured. As a consequence, each 4K module in a multiple module memory system can be uniquely jumpered to be assigned as a given set of 4K memory locations within a consecutive set of up to 16K locations.

Inspection of Figure 1 will show that the jumper network is configured to permit allocation of address space in 1K intervals within an address range of 4K to 8K formed by either one or two M7344 modules. In addition, each module can be assigned an address space of up to 4K within a total 64K address set. Each side of this jumper network is also brought out to the module edge fingers to permit address space allocation to be supplemented by wire wrap on the connector block.

Since the M7344 Read/Write Memory is electrically and logically compatible with the M7345 Programmable Read-Only Memory, these modules can be used together to form a contiguous RAM-PROM memory space.

SIGNAL SPECIFICATIONS

Input Signals

Symbol	*Description*	*Pin*	*Function*
CF2	Address Line 0	ADRD00 L	These 16 parallel input lines provide a 16-bit address for accessing the contents of an M7344 read/write memory module.
CE2	Address Line 1	ADRD01 L	
CD1	Address Line 2	ADRD02 L	
CE1	Address Line 3	ADRD03 L	
CB1	Address Line 4	ADRD04 L	
CC1	Address Line 5	ADRD05 L	
CF1	Address Line 6	ADRD06 L	
CH1	Address Line 7	ADRD07 L	
CH2	Address Line 8	ADRD08 L	
CS1	Address Line 9	ADRD09 L	
CM1	Address Line 10	ADRD10 L	
CR1	Address Line 11	ADRD11 L	
CJ1	Address Line 12	ADRD12 L	
CK1	Address Line 13	ADRD13 L	
DJ2	Address Line 14	ADRD14 L	
DK2	Address Line 15	ADRD15 L	

Input/Output Signals

Symbol	*Description*	*Pin*	*Function*
AD2	Bidirectional Memory Data Bus Line 0	DM0 L	These are the eight parallel bidirectional data lines comprising the input/output data bus. Pull-up resistors required for proper operation; 180Ω to +5V, and 390Ω to ground.
AC1	Bidirectional Memory Data Bus Line 1	DM1 L	
AM2	Bidirectional Memory Data Bus Line 2	DM2 L	
AN1	Bidirectional Memory Data Bus Line 3	DM3 L	
BD1	Bidirectional Memory Data Bus Line 4	DM4 L	
BC1	Bidirectional Memory Data Bus Line 5	DM5 L	
BM1	Bidirectional Memory Data Bus Line 6	DM6 L	
BL1	Bidirectional Memory Data Bus Line 7	DM7 L	

SPECIAL WIRING

As shown in Figure 1 and discussed under FUNCTIONS, the M7344 Read/Write Memory Module is designed to respond to a 16-bit address field. As a consequence, a given module with 1K, 2K, or 4K of memory capacity can exist within a 64K address space.

Within these 64K locations, a 1K or 2K memory module can be configured to occupy a unique 1K or 2K address space in the 4K address space. In addition, this 4K address space can occupy any one of 16 groups of sequential 4K locations within the total 64K address space. Similarly, a 4K memory module can be configured to occupy a 4K block within an 8K address space, and this 8K address space can be located in the total address space.

An M7344 memory module can be assigned to occupy a given 4K or 8K address space in one of two ways:

1. By jumper-connecting specific module address space selection lugs (see Figure 3) which are part of a total set of split lugs provided on the module for the explicit purpose of address space assignment;
2. By wire wrapping the appropriate connector block pins which correspond to the specific edge connector fingers within the overall group of fingers allocated to address space assignment.

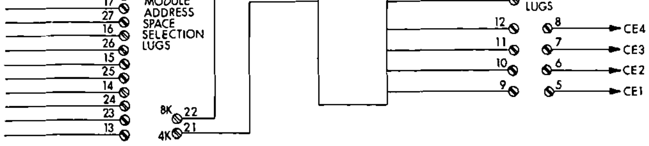

FIGURE 3. DESIGNATIONS FOR SPLIT LUGS PROVIDED FOR ADDRESS SPACE ASSIGNMENT

Within the module, each 1K segment can be assigned to one of the four 1K address spaces in a 4K space or in an 8K space through appropriate connection of the segment address space selection lugs (see Figure 3).

NOTE

This level of address space selection must be made with jumpers since the equivalent split lug points are not brought out to the edge connector.

In order to clarify the manner of assigning a memory module to a specific address space, a series of examples is presented which relate specific lug-to-lug connections to address space assigned. These examples require reference to Figure 3 and Table 1.

Table 1 shows the lug-to-lug and corresponding pin-to-pin connections for a 64K address space. However, the examples presented are, for purposes of clarity, concerned with the first or low order 16K address space. In principle, these examples are applicable throughout the full 64K address space, and differ only in the specific connections made between lugs 21 and 22 and the remaining Module Address Space Selection lugs (see Figure 3).

EXAMPLE 1: By placing a jumper between lug 13 and lug 21, an M7344-YC (4K) memory module will be assigned to locations 0 to 4095. In this case, the segment address selection lugs 9, 10, 11, and 12 should be connected to lugs 5, 6, 7, and 8 respectively in order to enable the four 1K memory segments comprising the 4K capacity.

It can be inferred from these examples that the 1K segments comprising a 1K, 2K, or 4K MPS system memory module can be assigned by jumper-installation to any one of the sixteen 1K slots in the 16K address space.

INPUT/OUTPUT SYMBOLOGY

The direction of signal flow is indicated by arrows on the signal lines. Arrows toward the module indicate input signals; arrows away from the module indicate output signals (see Figure 1 and Figure 4).

Fan-in and fan-out (in TTL unit loads) are indicated by the number contained in the box associated with each pin. A box containing the letter B designates that the associated signal line is connected to a bus.

INPUT—The fan-in designation box always precedes the pin designation.

OUTPUT—The fan-out designation box always follows the pin designation.

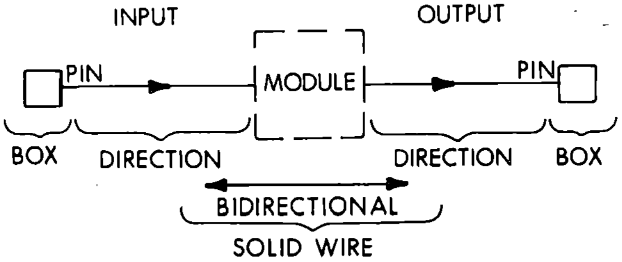

FIGURE 4. SIGNAL FLOW DIRECTION

POWER REQUIREMENTS

	VOLTS	POWER CONSUMPTION mA (max)	POWER CONSUMPTION WATTS (max)	VOLTAGE REGULATION	RIPPLE REGULATION	PINS POWER	PINS GROUND
M7344-YA	+5	1700	8.5	±5%	50 mV	AA2, BA2, CA2, DA2	AC2, AT1, BC2, BC1, CC2, CT1, DC2, DC1
M7344-YB	+5	2170	10.5				
M7344-YC	+5	3130	15.7				

digital

DIGITAL EQUIPMENT CORPORATION
COMPONENTS GROUP HEADQUARTERS
ONE IRON WAY, MARLBOROUGH, MASSACHUSETTS 01752
(617) 481-7400 TWX. 710-347-0348
For detailed information about products and policies, call 800-225-9480 toll-free (USA only); Massachusetts residents call (617) 481-7400.

DIGITAL EQUIPMENT CORPORATION, Maynard, Massachusetts, Telephone: (617) 897-5111 • ARIZONA, Phoenix • CALIFORNIA, Sunnyvale, Santa Ana, Los Angeles, Oakland, San Diego and San Francisco (Mountain View) • COLORADO, Englewood • CONNECTICUT, Meriden, Fairfield • DISTRICT OF COLUMBIA, Washington (Lanham, Md.) • FLORIDA, Orlando • GEORGIA, Atlanta • ILLINOIS, Northbrook • INDIANA, Indianapolis • LOUISIANA, Metairie • MASSACHUSETTS, Marlborough and Waltham • MICHIGAN, Ann Arbor and Detroit (Southfield) • MINNESOTA, Minneapolis • MISSOURI, Kansas City and Maryland Heights • NEW JERSEY, Fairfield, Metuchen and Princeton • NEW MEXICO, Albuquerque • NEW YORK, Huntington Station, Manhattan, New York, Syracuse and Rochester • NORTH CAROLINA, Durham/Chapel Hill • OHIO, Cleveland, Dayton and Euclid • OKLAHOMA, Tulsa • OREGON, Portland • PENNSYLVANIA, Bluebell and Pittsburgh • TENNESSEE, Knoxville • TEXAS, Dallas and Houston • UTAH, Salt Lake City • WASHINGTON, Bellevue • WISCONSIN, Milwaukee • ARGENTINA, Buenos Aires • AUSTRALIA, Adelaide, Brisbane, Canberra, Melbourne, Perth and Sydney • AUSTRIA, Vienna • BELGIUM, Brussels • BRAZIL, Rio de Janeiro, Sao Paulo and Porto Alegre • CANADA, Calgary, Montreal, Ottawa, Toronto and Vancouver • CHILE, Santiago • DENMARK, Copenhagen • FINLAND, Helsinki • FRANCE, Grenoble and Paris • GERMANY, Berlin, Cologne, Hannover, Frankfurt, Munich and Stuttgart • INDIA, Bombay • ISRAEL, Tel Aviv • ITALY, Milan and Turin • JAPAN, Tokyo • MEXICO, Mexico City • NETHERLANDS, The Hague • NEW ZEALAND, Auckland • NORWAY, Oslo • PHILIPPINES, Manila • PUERTO RICO, Santurce • SPAIN, Barcelona and Madrid • SWEDEN, Stockholm • SWITZERLAND, Geneva and Zurich • UNITED KINGDOM, Birmingham, Bristol, Edinburgh, London, Manchester and Reading • VENEZUELA, Caracas

PRINTED IN U.S.A. 5804 00874 3986/M 16 10